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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SMART MODULAR TECHNOLOGIES INC.

Petitioner

v.

NETLIST, INC.

Patent Owner

Case IPR2014-01370

Patent 8,301,833

CORRECTED PETITION FOR *INTER PARTES* REVIEW OF CLAIMS 1-30 OF U.S. PATENT NO. 8,301,833

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Michael F. Heafey (Lead Counsel)
Registration No. 38,178
King & Spalding, LLP
601 South California Avenue, Suite 100
Palo Alto, California 94304
(650) 422-6700

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TABLE OF EXHIBITS

Original Exhibit Number	Corrected Exhibit Number	Exhibit
1001	1009	U.S. Patent 8,301,833
1002	1010	Declaration of Nader Bagherzadeh
1003	1011	Declaration of Michael F. Heafey
1004	1012	U.S. Patent Publication No. 2006/0294295 to Fukuzo
1005	1013	U.S. Patent Publication No. 2004/0190210 to Leete
1006	1014	U.S. Patent No. 7,600,142 to Ichikawa
1007	1015	U.S. Patent No. 7,421,552 to Long
1008	1016	U.S. Patent No. 7,062,618 to Tsunoda *et al.*
2001	1017	2001 Webster's II Dictionary Pages (Exhibit to Declaration of Nader Bagherzadeh)
2002	1018	1998 IEEE Dictionary Pages (Exhibit to Declaration of Nader Bagherzadeh)
2003	1019	U.S. Patent 4,965,828
2004	1020	U.S. Patent 5,519,831
3001	1021	August 22, 2013 Letter from S Cunningham (Exhibit to Declaration of Michael F. Heafey)
3002	1022	August 23, 2013 Complaint for Declaratory Judgment, SMART v. Netlist Case 4:13-cv-03916-YGR (Exhibit to Declaration of Michael F. Heafey)
3003	1023	August 23, 2013 First Amended Complaint 8:13-cv-00996-DOC-JPR (Exhibit to Declaration of Michael F. Heafey)
3004	1024	August 23, 2013 Summons in a Civil Action, Netlist v. SMART (Exhibit to Declaration of Michael F. Heafey)
3005	1025	February 12, 2014 Order Granting Dismissal Without Prejudice Case 4:13-cv-03916-YGR (Exhibit to Declaration of Michael F. Heafey)
3006	1026	February 12, 2014 Order Granting Dismissal Without Prejudice Case 4:13-cv-05889-YGR (Exhibit to Declaration of Michael F. Heafey)
3007	1027	Infringement Contention Chart By Netlist from Case 4:13-cv-05889-YGR (Exhibit to Declaration of Michael F. Heafey)

I. MANDATORY NOTICES – 37 C.F.R. § 42.8

A. Fee – 35 U.S.C. §§ 311 & 312(a)(1); 37 C.F.R. §§ 42.15(a)(1&3) & 42.103

Petitioner SMART Modular Technologies, Inc. requests that the Commissioner charge deposit account number 503732, ref.: 21584-112005, at least the fee of $11,000 for the Request for *inter partes* review of claims 1-30 ("Challenged Claims") of U.S. Patent No. 8,301,833 (Ex. 1009). In addition, Petitioner requests that the Commissioner charge the same deposit account, with the same reference number, for Post-Institution and for any other fee required for *inter partes* review of the '833 patent.

B. Identification Of Challenge – 35 U.S.C. §§ 311 & 312(a)(3); 37 C.F.R. § 42.104(b)

Petitioner requests *inter partes* review of claims 1-30. *Sections* III-V, along with the Declaration of Nader Bagherzadeh (Exhibit 1010), set forth the precise relief sought for each Challenged Claim and include: 1) the Challenged Claims; 2) the statutory grounds for rejection; 3) how the claim is to be construed; 4) how the claim is unpatentable; and 5) exhibits Ex. 1009-1016 of the supporting evidence.

C. Standing – 35 U.S.C. § 315(a), (b) & (e)(1); 37 C.F.R. §§ 42.101 & 42.104(a)

Petitioner certifies that the '833 patent is available for *inter partes* review and that it is not barred or estopped from petitioning for *inter partes* review.

D. Real Party-In-Interest – 35 U.S.C. § 312(a)(2); 37 C.F.R. § 42.8(b)(1)

Petitioner certifies that the sole real party in interest to this Petition for *inter partes* review of '833 patent is: SMART Modular Technologies, Inc., 39870 Eureka Drive Newark, California 94560.

E. Related Matters – 35 U.S.C. § 315(d); 37 C.F.R. § 42.8(b)(2)

1. District Court Litigation

On August 23, 2013, Petitioner filed a complaint in the United States District Court for the Northern District of California seeking declaratory judgment that it did not infringe any claims of the '833 patent and that claims of the '833 patent are invalid. Exhibit 1022 to the Declaration of Michael F. Heafey (hereinafter, "Heafey Decl.," Ex. 1011). The Northern District assigned Petitioner's complaint Case No. 4:13-cv-03916 (the "'916 Case").

On August 23, 2013, Netlist filed a complaint in the United States District Court for the Central District of California alleging that Petitioner; Diablo Technologies, Inc.; Smart Storage Technologies, Inc.; and Smart Worldwide Holdings, Inc. infringed the '833 patent. Ex. 1023. The Central District assigned Netlist's complaint Case No. 8:13-cv-00996-DOC-JPR (the "'996 Case"). Netlist served its complaint on Petitioner on August 23, 2013. Ex. 1024.

On November 26, 2013, the Central District Court transferred the patent infringement counts of the '996 Case to the Northern District of California, to which

the Court assigned Case No. 4:13-cv-05889 (the "'889 Case"). Ex. 1011, Heafey Decl., ¶ 5.

On February 7, 2014, Petitioner and Netlist jointly stipulated to a voluntary dismissal, without prejudice, of the '916 Case and the '889 Case. Ex. 1011, Heafey Decl., ¶ 6. On February 12, 2014, the Northern District ordered both cases dismissed without prejudice. Exhibit 1025 & 1026.

2. *Inter Partes* Review

On June 20, 2014, SanDisk Corporation filed a petition for *inter partes* review of U.S. Patent No. 8,301,833. On July 2, 2014, the Patent Office assigned a filing date and case number IPR2014-00994 to SanDisk's petition for *inter partes* review of the '434 patent. A decision to institute an *inter partes* review is pending.

On June 19, 2014, SanDisk Corporation filed a petition for *inter partes* review of U.S. Patent No. 8,516,187. The '187 patent is a division of the '833 patent. On June 26, 2014, the Patent Office assigned a filing date and case number IPR2014-00982 to SanDisk's petition for *inter partes* review of the '187 patent. A decision to institute an *inter partes* review is pending.

F. Lead, Back-Up Counsel, And Service Information – 37 C.F.R. §§ 42.8(b)(3), 42.10(a) & 42.8(b)(4)

Lead counsel is: Michael F. Heafey, Registration No. 38,178. Back-up counsel is: Sanjiva K. Reddy, Registration No. 70,816.

Michael F. Heafey
Registration No. 38178
King & Spalding LLP
601 South California Avenue
Palo Alto, California 94304
(650) 422-6719 (telephone)
(650 422-6800 (facsimile)
mheafey@kslaw.com (email)

Sanjiva K. Reddy
Registration No. 70816
King & Spalding LLP
1185 Avenue of the Americas
New York, New York 10036
(212) 556-2157 (telephone)
(212) 556-2222(facsimile)
sreddy@kslaw.com (email)

Petitioner also consents to service via email at the email addresses above, with a courtesy copy to patentmailnyc@kslaw.com.

II. GROUNDS FOR STANDING – 35 U.S.C. § 315(a)(1), (b) & (c); 37 C.F.R. § 104(a)

The '833 patent is available for *inter partes* review. The '833 patent issued on October 20, 2012 from an original application filed on September 29, 2008. The '833 patent is a continuation of U.S. patent application, No. 12/131,873, filed on June 2, 2008, now abandoned. The '833 patent claims priority to provisional application 60/941,586, filed on June 1, 2007.

A. 35 U.S.C. § 315(a)(1)

Although Petitioner filed a complaint for declaratory judgment that claims of the '833 patent are invalid, it is not barred from filing this Petition for *inter partes* review. 35 U.S.C. § 315(a)(1); Clio USA, Inc. v. The Proctor And Gamble Company, Case IPR2013-00438 (PTAB Jan. 9, 2014) (Kamholz, APJ) (rehearing denied, PTAB (Feb. 4, 2014)).

On August 23, 2013, Petitioner filed in the United States District Court for the Northern District of California a complaint for declaratory judgment that claims of the '833 patent are invalid under 35 U.S.C. §§ 102, 103, and others. Ex. 1022. On February 12, 2014, the District Court dismissed Petitioner's complaint without prejudice. Ex. 1025. Because the District Court dismissed Petitioner's complaint without prejudice, § 315(a)(1) does not bar Petitioner from petitioning for *inter partes* review of the '833 patent, because it is as if the complaint never existed.

> Federal Courts treat a civil action that is dismissed without prejudice as "something that *de jure* never existed." . . . In such a situation , the action is a nullity and the parties are left in the same legal position as if the civil action had never been filed. In the context of §315(a)(1), the action never existed.

Id. at 8 (emphasis added). Accordingly, because Petitioner's declaratory judgment complaint was dismissed without prejudice, § 315(a)(1) does not bar this Petition. *Clio* at 9.

B. 35 U.S.C. §§ 315(b) & e(1)

On August 23, 2013, the assignee of the '833 patent, Netlist, Inc., filed and served a complaint accusing Petitioner, and others, of infringing the '833 patent. Exs. 1023 & 1024. Petitioner is not barred from petitioning for *inter parties* review of the '833 patent because it is filing this Petition within one year of Netlist's filing date of August 23, 2013. 35 U.S.C. § 315(b).

Petitioner is not estopped or barred from requesting *inter partes* review of the '833 patent under § 315(e)(1). To Petitioner's knowledge, the Patent Office has never instituted an *inter parties* review[1] of the '833 patent, and none of Petitioner or its privies, if any privies exist, have petitioned for *inter partes* review of the '833 patent.[1]

III. STATEMENT OF THE PRECISE RELIEF REQUESTED 37 C.F.R. §§ 42.104(B)(1) & (2)

Petitioner respectfully requests that claims 1-30 of the '833 patent be canceled. A full statement of the reasons for this request is presented *infra*. The grounds[2] are supported by the Declaration of Nader Bagherzadeh, which include detailed Claim Charts for each ground of cancellation of the claims ("Bagherzadeh Decl.," Ex. 1010; as filed with this Petition[3]).

Ground 1: Claims 1, 2, 4, 6-13, 15, 16, 18, 20, and 22-29 are unpatentable under 35 U.S.C. § 102(b) as anticipated by U.S. Patent Application Publication No. 2006/0294295 to Fukuzo ("Fukuzo '295Pub," Ex. 1012);

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[1] or *inter partes* reexamination or *ex parte* reexamination.

[2] The '833 patent issued prior to the America Invents Act ("AIA"). Accordingly, Petitioner uses pre-AIA statutory framework in this Petition. (35 U.S.C. § 100)

[3] Grounds 2-8 are different from Sandisk's Inter Partes Review, Case No. IPR2014-00994. Ground 1 includes additional claims than Sandisk's Inter Partes Review based, in part, on the same reference.

Ground 2: Claims 3, 5, 14, 17, 19, 21, and 30 are unpatentable under 35 U.S.C. § 103(a) as obvious in view of Fukuzo '295Pub and U.S. Patent Application Publication No. 2004/0190210 to Leete ("Leete '210Pub," Ex. 1013);

Ground 3: Claims 1, 2, 7, 8, 11-13, 15, 18, 23, 24, and 27-29 are unpatentable under 35 U.S.C. § 102(b) as anticipated by of U.S. Patent No. 7,600,142 to Ichikawa ("Ichikawa '142," Ex. 1014);

Ground 4: Claims 3-6, 9, 10, 14, 16, 17, 19-22, 25, 26, and 30 are unpatentable under 35 U.S.C. § 103(a) as obvious in view of Ichikawa '142 and Leete '210Pub;

Ground 5: Claims 1, 2, 4, 5, 12, 13, 15, 18, 20, 21, 28, and 29 are unpatentable under 35 U.S.C. § 102(b) as anticipated by U.S. Patent No. 7,421,552 to Long ("Long '552," Ex. 1015);

Ground 6: Claims 3, 6-11, 14, 16, 17, 19, 22-27, and 30 are unpatentable under 35 U.S.C. § 103(a) as obvious in view of Long '552 and Leete '210Pub;

Ground 7: Claims 1, 2, 4, 5, 12, 13, 15, 16, 18, 20, 21, 28, and 29 are unpatentable under 35 U.S.C. § 102(b) as anticipated by U.S. Patent No. 7,062,618 to Tsunoda *et al.* ("Tsunoda '618," Ex. 1016); and

Ground 8: Claims 3, 6-11, 14, 16, 17, 19, 22-27, and 30 are unpatentable under 35 U.S.C. § 103(a) as obvious in view of Tsunoda '618 and Leete '210Pub.

IV. PROPOSED REJECTIONS

Claims 1, 2, 4, 6-13, 15, 16, 18, 20, and 22-29 are rejected under 35 U.S.C. § 102(b) as anticipated by Fukuzo '295Pub;

Claims 3, 5, 14, 17, 19, 21, and 30 are rejected under 35 U.S.C. § 103(a) as obvious in view of Fukuzo '295Pub and Leete '210Pub;

Claims 1, 2, 7, 8, 11-13, 15, 18, 23, 24, and 27-29 are rejected under 35 U.S.C. § 102(b) as anticipated by Ichikawa '142;

Claims 3-7, 9, 10, 14, 16, 17, 19-22, 25, 26, and 30 are rejected under 35 U.S.C. § 103(a) as obvious in view of Ichikawa '142 and Leete '210Pub;

Claims 1, 2, 4, 5, 12, 13, 15, 18, 20, 21, 28, and 29 are rejected under 35 U.S.C. § 102(b) as anticipated by Long '552;

Claims 3, 6-11, 14, 16, 17, 19, 22-27, and 30 are rejected under 35 U.S.C. § 103(a) as obvious in view of Long '552 and Leete '210Pub;

Claims 1, 2, 4, 5, 12, 13, 15, 16, 18, 20, 21, 28, and 29 are rejected under 35 U.S.C. § 102(b) as anticipated by Tsunoda '618; and

Claims 3, 6-11, 14, 16, 17, 19, 22-27, and 30 are rejected under 35 U.S.C. § 103(a) as obvious in view of Tsunoda '618 and Leete '210Pub.

V. STATEMENT OF THE REASONS FOR THE RELIEF REQUESTED

A. Introduction

The '833 patent relates to providing a non-volatile memory backup for a volatile memory system, whcih include volatile memory devices, such as dynamic

random-access memories (DRAM) that are subject to loss of data in the absence of a power source. In contrast, non-volatile memory typically stores data even in the absence of a power source. Hybrid memory systems include non-volatile memory devices to provide backup for the conventional volatile memory devices on the hybrid system. Ex. 1010, Bagherzadeh Decl., ¶¶ 17-19. Further, volatile memory devices are typically high speed devices, contrasting non-volatile memory devices, which function at a slower clock rate or frequency. Ex. 1010, Bagherzadeh Decl., ¶¶ 17-19.

Systems of the type disclosed in the '833 patent specification are hybrid memory systems requiring variable clock frequencies for operation. Ex. 1010, Bagherzadeh Decl., ¶¶ 17-19.

B. Description Of The '833 Patent

The '833 patent has 2 independent method and system claims, and has a total of 30 claims. The '833 patent is a continuation of U.S. patent application, No. 12/131,873, filed on June 2, 2008, now abandoned. The '833 patent claims priority to provisional application 60/941,586, filed on June 1, 2007.

1. The Alleged Invention

The alleged invention in the '833 patent relates to a specific configuration of hybrid memory systems that purportedly addresses non-volatile memory backup, while running the volatile memory subsystem at lower power, and therefore, at lower clock speeds. '833 patent, 16:29-34. Specifically, the alleged invention of the '833 patent includes circuitry for providing a regular high-speed clock frequency (first clock

frequency) during communications between the host and the volatile memory subsystem, and a slower clock frequency during communications between the volatile memory subsystem (using third clock frequency) and the non-volatile memory subsystem (using second clock frequency). '833 patent, 21:5-21. Further, the second and third clock frequencies may be substantially equal. 21:23-24. Figure 1 and an excerpt from Fig. 8 of the '833 patent have been annotated using limitations of claim 15 to illustrate the various components of the alleged invention.

2. Challenged Claims Of The '833 Patent

Claim	Table 1: '833 patent Claim Limitations
1.a	A method for controlling a memory system operatively coupled to a host system,
1.b	the memory system including a volatile memory subsystem and a non-volatile memory subsystem, the method comprising:
1.c	operating the volatile memory subsystem at a first clock frequency when the memory system is in a first mode of operation
1.d	in which data is communicated between the volatile memory subsystem and the host system;
1.e	operating the non-volatile memory subsystem at a second clock frequency when the memory system is in a second mode of operation
1.f	in which data is communicated between the volatile memory subsystem and

	the non-volatile memory subsystem; and
1.g	operating the volatile memory subsystem at a third clock frequency when the memory system is in the second mode of operation,
1.h	the third clock frequency being less than the first clock frequency.
2	The method of claim 1, wherein the third clock frequency is substantially equal to the second clock frequency.
3	The method of claim 1, wherein the memory system is not powered by a battery when it is in the second mode of operation.
4	The method of claim 1, herein the memory system switches from the first mode of operation to the second mode of operation in response to a trigger condition.
6.a	The method of claim 1, wherein the memory system further comprises a printed circuit board and
6.b	the volatile memory subsystem and the non-volatile memory subsystem are located on the printed circuit board.
7	The method of claim 1, wherein data communicated between the volatile memory subsystem and the non-volatile memory subsystem is intermediate data from a host computer system computation.
8	The method of claim 1, wherein data communicated between the volatile memory subsystem and the non-volatile memory subsystem is backup data

	from a backup operation.
9	The method of claim 8, wherein the backup operation is conducted at repeating time intervals.
10	The method of claim 9, wherein the backup operation is initiated in response to a trigger event.
11	The method of claim 1, wherein the second mode of operation comprises a backup operation in which data is communicated from the volatile memory subsystem to the non-volatile memory subsystem.
12	The method of claim 1, wherein the second mode of operation comprises a restore operation in which data is communicated from the non-volatile memory subsystem to the volatile memory subsystem.
13	The method of claim 1, wherein one or more of the first, second or third clock frequencies is configurable by the memory system.
14	The method of claim 1, wherein one or more of the first, second or third clock frequencies is configurable by a user.
15.a	A memory system operatively coupled to a host system,
15.b	the memory system comprising: a volatile memory subsystem operable at a first clock frequency when the memory system is in a first mode of operation
15.c	in which data is communicated between the volatile memory subsystem and

	the host system; and
15.d	a non-volatile memory subsystem operable at a second clock frequency when the memory system is in a second mode of operation
15.e	in which data is communicated between the volatile memory subsystem and the non-volatile memory subsystem,
15.f	the volatile memory subsystem further being operable at a third clock frequency when the memory system is in the second mode of operation,
15.g	the third clock frequency being less than the clock first frequency.
16.a	The memory system of claim 15, further comprising: a controller configured to decouple the non-volatile memory subsystem from the volatile memory subsystem in the first mode of operation and
16.b	to couple the non-volatile memory subsystem to the volatile memory subsystem in the second mode of operation.
17.a	The memory system of claim 15, further comprising a plurality of power supplies
17.b	and a switch configured to selectively deliver power from the plurality of power supplies to the volatile memory subsystem and the non-volatile memory subsystem as a function of the mode of operation.
18	The memory system of claim 15, wherein the third clock frequency is substantially equal to the second clock frequency.

19	The memory system of claim 15, wherein the memory system is not powered by a battery when it is in the second mode of operation.
20	The memory system of claim 15, wherein the memory system switches from the first mode of operation to the second mode of operation in response to a trigger condition.
21	The memory system of claim 20, wherein the trigger condition comprises a power failure condition.
22.a	The memory system of claim 15, wherein the memory system further comprises a printed circuit board and
22.b	the volatile memory subsystem and the non-volatile memory subsystem are located on the printed circuit board.
23	The memory system of claim 15, wherein data communicated between the volatile memory subsystem and the non-volatile memory subsystem is intermediate data from a host computer system computation.
24	The memory system of claim 15, wherein data communicated between the volatile memory subsystem and the non-volatile memory subsystem is backup data from a backup operation.
25	The memory system of claim 24, wherein the backup operation is conducted at repeating time intervals.
26	The memory system of claim 25, wherein the backup operation is initiated in

	response to a trigger event.
27	The memory system of claim 15, wherein the second mode of operation comprises a backup operation in which data is communicated from the volatile memory subsystem to the non-volatile memory subsystem.
28	The memory system of claim 15, wherein the second mode of operation comprises a restore operation in which data is communicated from the non-volatile memory subsystem to the volatile memory subsystem.
29	The memory system of claim 15, wherein one or more of the first, second or third clock frequencies is configurable by the memory system.
30	The memory system of claim 15, wherein one or more of the first, second or third clock frequencies is configurable by a user.

C. Description Of The Identified Prior Art

Hybrid memory modules are well known in the art and have discussed in the literature since as far back as 1989. For example, U.S. patent 4,965,828 to Ergott *et al.* (filed 1989, Ex. 1019) and U.S. 5,519,831 to Holzhammer (filed 1991, Ex. 1020) are both related to hybrid memory modules using non-volatile ROM or flash to provide data back-up for volatile RAM memory devices. Ex. 1010, Bagherzadeh Decl., ¶¶ 28 and 29. Ergott in particular discloses a lower-power memory module configured to operate in lower power conditions using capacitor, and not battery for the low power backup operation. Also well known in the art is that flash memory has slower

operating speeds than volatile memory. Ex. 1010, Bagherzadeh Decl., ¶¶ 28 and 29. Non-volatile memory is not used in temporary memory situations for everyday computing, where volatile memory is widely used, because reading and writing to a non-volatile memory would substantially lower the performance speed of the host computer. Ex. 1010, Bagherzadeh Decl., ¶¶ 28 and 29.

1. Fukuzo '295Pub

Fukuzo '295Pub is a U.S. patent publication that was filed on June 24, 2005, and that published on December 28, 2006. Fukuzo '295Pub is prior art at least under 35 U.S.C. §§ 102(a) or 102(e), and was not considered in the prosecution of the '833 patent. Fukuzo '295Pub was included in Sandisk's petition for *inter partes* review.

Fukuzo '295Pub discloses a memory chip device, including FIFO SDRAM buffer 20 and a flash memory subsystem 30. Ex. 1012, ¶¶ [0085] and [0088]. *Id.* Fig. 5 (annotated and reproduced here). Further, Fukuzo '295Pub discloses that the device is configured to operate the FIFO SDRAM buffer 20 at 130 MHz when communicating with the host (*Id.*, ¶¶ [0084], [0086], and [00127]); and at 20 MHz while communicating with the flash memory subsystem 30 (*Id.,* ¶¶ [0084]-[0085], [0114], and [00103]). Ex. 1010, Bagherzadeh Decl., ¶ 23.

2. Ichikawa '142

Ichikawa '142 is a U.S. patent that was filed on April 21, 2006, that published on December 14, 2006, and that issued on October 6, 2009. Ichikawa '142 is prior art at least under section 102(b) or (e), and was not considered in the prosecution of the

'833 patent. Ichikawa '142 was not included in Sandisk's petition for *inter partes* review.

Ichikawa '142 discloses a system including volatile memory RAM 13 and non-volatile memory system combining serial input-output (SIO) 14 with external flash memory 30. Ex. 1014, 1:12-16, 1:23-25, 1:27-28. *Id.* Fig 2 (annotated and reproduced here). Further, Ichikawa '142 discloses that the device is configured to operate the RAM 13 at 5 MHz when communicating with the host (*Id.*, 4:29-41, 2:38-40, and 3:50-56): and at 1 MHz when communicating with the flash memory subsystem 30 (*Id.* 4:43-54, 4:55-61, and 3:57-59). Ex. 1010, Bagherzadeh Decl., ¶ 24.

3. Long '552

Long '552 is a U.S. patent that was filed on March 17, 2006, that published on September 20, 2007, and that issued on September 2, 2008. Long '552 is prior art at least under section 102(b) or (e), and was not considered in the prosecution of the '833 patent. Long '552 was not included in Sandisk's petition for *inter partes* review.

Long '552 discloses a system including volatile memory cache 42 and non-volatile memory vault 44. Ex. 1015, 3:47-50. *Id.* Fig 1 (annotated and reproduced here). Further, Long '552 discloses that the device is configured to operate the volatile memory 42 at a fast clock speed, supplied with 50 to 100 watts of power when communicating normally with the host (*Id.*, 4:46-53 and 3:50-59): and at a significantly slower clock speed, supplied with 30 watts of power when communicating with the non-volatile memory 44 (*Id.* 4:54-61). Ex. 1010, Bagherzadeh Decl., ¶ 26.

4. Tsunoda '618

Tsunoda '618 is a U.S. patent that was filed on June 13, 2002, that published on February 6, 2003, and that issued on June 13, 2006. Tsunoda '618 is prior art at least under section 102(b), and was not considered in the prosecution of the '833 patent. Tsunoda '618 was not included in Sandisk's petition for *inter partes* review.

Tsunoda '618 discloses a system including SDRAM volatile memory cache 4010 and flash non-volatile memory 4020. Ex. 1016, 4:2-6. *Id.* Fig 24 (annotated and reproduced here). Further, Tsunoda '618 discloses that the device is configured to operate the volatile memory 42 at a high SDRAM speed, when communicating normally with the host (*Id.*, 13:51-53, 11:51-54, and 12:27-31): and at a speed difference from the high speed, when communicating with the non-volatile memory 44 (*Id.* 12:21-25, 13:55-58, and 11:51-54). Ex. 1010, Bagherzadeh Decl., ¶ 25.

5. Leete '210Pub

Leete '210Pub is a U.S. patent publication that was filed on March 26, 2003, and that published on September 30, 2004. Leete '210Pub is prior art at least under section 102(b), and was cited by the Applicant in the prosecution of the '833 patent. Leete '210Pub was not incldued in Sandisk's petition for *inter partes* review.

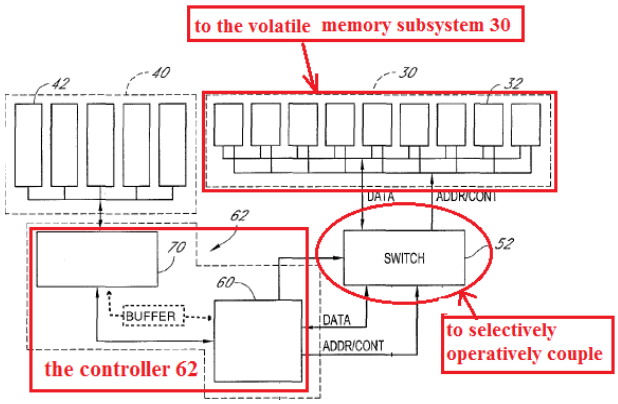
Leete '210Pub discloses a system including volatile RAM memory 704 and flash non-volatile memory 706. Ex. 1013, ¶[0057]. *Id.* Fig 7 (annotated and reproduced here). Further, Leete '210Pub discloses that the device is configured to backup data from the memory 704 to the flash memory 706 in the event of power reduction or

shutdown. *Id.* ¶[0058]. Specifically, Leete '210Pub discloses that capacitors provide the backup power 710 of during the shutdown event. *Id.* ¶¶[0055] & [0058]. Ex. 1010, Bagherzadeh Decl., ¶ 27.

D. Claim Construction

The Challenged Claims are to be interpreted according to their broadest reasonable interpretation consistent with the specification of the '833 patent. MPEP § 2258(I)(2)(G) and 37 C.F.R. § 42.100(b).

"operatively coupled" (Claims 1 & 15)

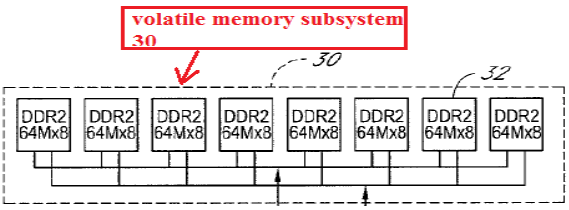
Construction	Support
"capable of operating together"	"to selectively operatively couple the controller 62 to the volatile memory subsystem 30." Ex. 1009, '833 patent, 7:3-4 and excerpt from Fig. 2 (annotated).  "**<u>something that […] connects</u>** two things together," Ex. 1017, Webster's II New College Dictionary, 2001 (emphasis added).

Construction	Support
	re. "coupling" – "**the association of two or more circuits** […] in such a way that power or signal information may be transferred from one to another," Ex. 1018, ANSI/IEEE 100 - Standard Dictionary of Electrical and Electronic Terms, Fourth Edition, 1988 (emphasis added). Ex. 1010, Bagherzadeh Decl., ¶ 38.

"couple" and "decouple" (Claim 16)

Construction	Support
"connected" and "disconnected"	"one or more switches 172 […] which can be actuated to **couple and decouple** the controller 62 to and from the volatile memory subsystem 30," Ex. 1009, '833 patent, 7:12:16 (emphasis added). "[T]he full width of the data bus is **connected** between the volatile memory subsystem 60 and the controller 62.." Ex. 1009, '833 patent, 20:58-60 (emphasis added). re. "coupling" – "**the association of two or more circuits** […] in such a way that **power or signal information may be transferred from one to another**," Ex. 1018 (emphasis added). Ex. 1010, Bagherzadeh Decl., ¶ 38.

"memory subsystem" (Claims 1, 6-8, 11-12, 15-17, 22-24, &27-28)

Construction	Support
"two or more memory components"	"volatile memory subsystem 30" Ex. 1009, '833 patent, 4:59 and Excerpt from Fig. 1 (annotated).  "The volatile memory **subsystem** 30 comprises **a plurality of volatile memory elements** 32 and the non-volatile memory **subsystem** 40 comprises **a plurality of non-volatile memory elements** 42." '833 patent, 5:48-51 (emphasis added). "where the volatile memory subsystem 30 comprises **DRAM elements, only the slice of the DRAM which is currently being accessed** (e.g., written to the buffer) during a backup is **configured in full-operational mode**." Ex. 1009,'833 patent, 20:39-42 (emphasis added). "[A] system containing **two or more integrated components which [...] may be isolated**" Ex. 1018 (emphasis added).

	Ex. 1010, Bagherzadeh Decl., ¶ 38.

"operating the […] memory subsystem" (Claim 1) and "memory subsystem operable" (Claim 15)

Construction	Support
"operating a memory component in the memory subsystem" and "operable memory component in the memory subsystem"	"where the volatile memory subsystem 30 comprises DRAM elements, **only the slice of the DRAM which is <u>currently being accessed</u>** (e.g., written to the buffer) during a backup is **configured in full-operational mode**." Ex. 1009,'833 patent, 20:39-42 (emphasis added). "subsystem-" "[A] system containing **two or more integrated components which […] may be <u>isolated</u>**" Ex. 1018, IEEE (emphasis added). Ex. 1010, Bagherzadeh Decl., ¶ 38.

"intermediate data from a […] computation" (Claims 7 & 23)

Construction	Support

"partial data, incomplete data, subset of bit, or cached bits"	"**intermediate data** results in a noisy system environment when the host computer system is engaged **in a long computation**," Ex. 1009,'833 patent, 7:49-51 (emphasis added). "**recover the data efficiently** in the event of a power outage because of the backup […to…] a write-through **cache or as some other type of cache**. Ex. 1009,'833 patent, 11:3-8 (emphasis added). "on each backup operation, but only **a partial copy** is performed…" Ex. 1009,'833 patent, 10:54-55 (emphasis added). Ex. 1010, Bagherzadeh Decl., ¶ 38.

"power failure" (Claims 5 & 21)

Construction	Support
"insufficient power"	"Upon detecting a **low voltage condition (e.g., due to a power interruption to the host system**," Ex. 1009,'833 patent, 8:38-40 (emphasis added). "**Any variation** in electric power supply that **causes unacceptable performance** of the user's equipment." Ex. 1017, Webster (emphasis added). Ex. 1010, Bagherzadeh Decl., ¶ 38.

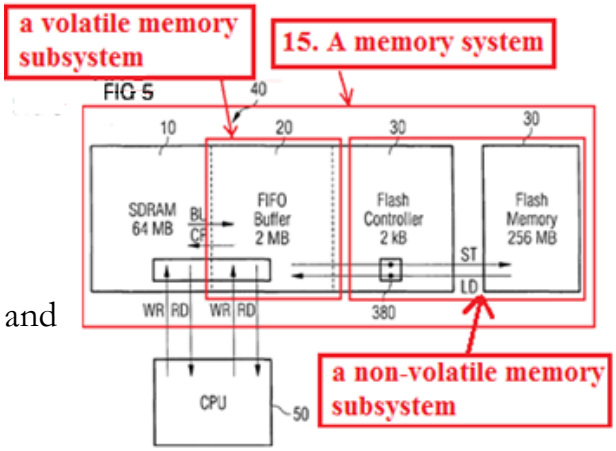
"switches" (Claims 4 & 20)

Construction	Support
"initiates"	"[U]pon detecting that a trigger condition is likely to occur and **transitions** from the second state to the third state upon detecting […] **the trigger** condition…" Ex. 1009,'833 patent, 11:55-57 (emphasis added). "to cause" Ex. 1017, Webster (emphasis added). Ex. 1010, Bagherzadeh Decl., ¶ 38.

E. Ground 1 - Fukuzo '295Pub Anticipates The Challenged Claims

1. Independent Claims 1 And 15

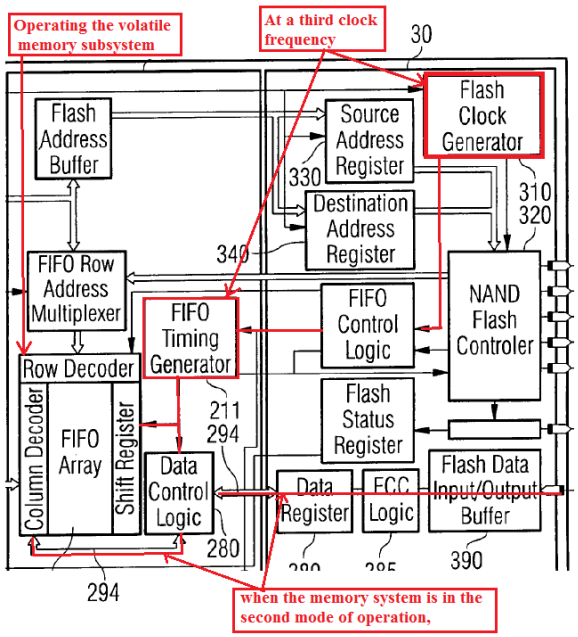
The Challenged Claims recite, in part, "[a] method of controlling a memory system operatively coupled to a host system" (Table 1, 1.a) and "[a] memory system operatively coupled to a host system" (Table 1, 15.a). Fukuzo '295Pub discloses an SDRAM-flash memory device as illustrated in Fig. 5 (annotated and reproduced below), coupled to CPU 50.



As to limitations 1.b, 15.b and 15.d (Table 1, 1.b, 15.b, 15.d), Fukuzo '295Pub discloses that FIFO SDRAM buffer 20 receives data directly from the CPU 50 (Ex.

1012, ¶[0127]), and also communicates with flash memory system 30, constituting controller and flash memory. *Id.,* ¶¶[0185] and [0088].

As to limitations 1.c-d (Table 1, 1.c-d, 15.c, and further to 15.b), Fukuzo '295Pub discloses that the FIFO SDRAM buffer 20 may be clocked at 130 MHz during read and write operations with the CPU 50, thereby disclosing limitations 1.c-d. *Id.,* ¶¶[0084] and [0127].



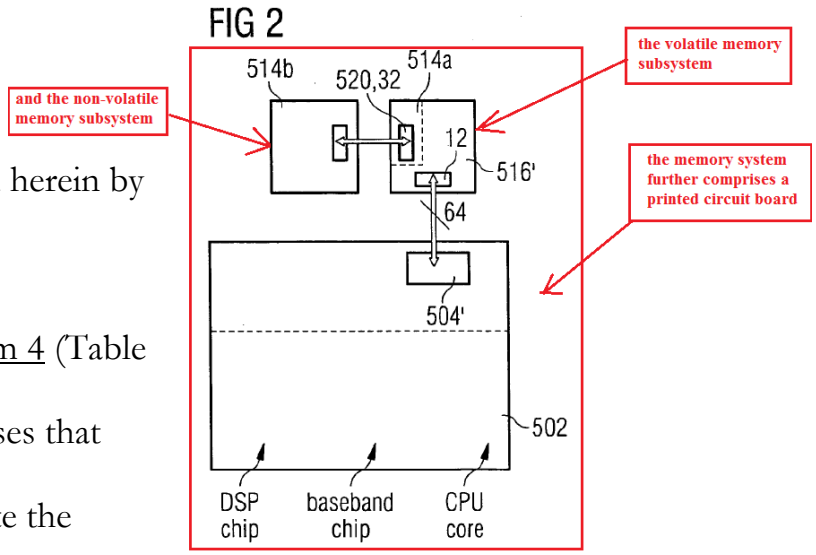
As to limitations 1.e-g and 15.d-g (Table 1, 1.e-h and 15.d-g), Fukuzo '295Pub discloses that the Flash memory controller and the memory 30 may be clocked at 20 MHz during read and write operations with the FIFO SDRAM buffer 20, thereby disclosing limitations 1.e-f and 15.d-e. *Id.,* ¶¶[0084], [0085], [0114], [0103] and [0127]. Further, a POSITA would understand from the disclosure of Fukuzo '295Pub that the FIFO SDRAM buffer receives the same clock of the flash memory system, via the FIFO timing generator, during operations with the flash memory system. *Id.,* ¶¶[0125], [0127], [0084], [0085], and Excerpt from Fig. 4 (annotated and reproduced here). Ex. 1010, Bagherzadeh Decl., ¶ 40. Accordingly, a person of ordinary skill in the art ("POSITA") would understand that the flash memory and the FIFO SDRAM buffer are communicating at the same frequency of 20 MHz to be able to transfer data between the components,

thereby meeting limitations 1.g and 15.f. Ex. 1010, Bagherzadeh Decl., ¶ 40. Since the 20 MHz clock during flash communications is less than the 130 MHz clock during host operations, the memory system of Fukuzo '295Pub discloses limitations 1.h and 15.g.

Fukuzo '295Pub anticipates Claims 1 and 15. *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987) (stating that "[a] claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference").

2. Dependent Claims 2, 4, 6-13, 16, 18, 20, And 22-29

As to Challenged Claim 2 (Table 1, 2), the reasons from Fukuzo '295Pub with respect to Challenged Claim limitation 1.h is applicable, and is therefore incorporated herein by reference.



As to Challenged Claim 4 (Table 1, 4), Fukuzo '295Pub discloses that commands LD and ST initiate the switch from host transfer to the flash transfer. Ex. 1012, ¶¶[0104] and [0087].

As to Challenged Claim 6 (Table 1, 6.a-b), Fukuzo '295Pub discloses that the memory system is on a CPU board 502. *Id.,* ¶¶[0079] and Fig. 2 (annotated and reproduced here). Further, with respect to limitation 6.b, Fukuzo '295Pub discloses

that the SDRAM 516' and flash memory 514b are connected to the CPU board. A POSITA would understand from the structures of Fukuzo '295Pub that the flash memory 514b and SDRAM 516' may be included on the CPU board 502 to provide the structure claimed here ("the volatile memory subsystem and the non-volatile memory subsystem are located on the printed circuit board," Table 1, 6.b). *Brown v. 3M*, 265 F.3d 1349, 1351, 60 USPQ2d 1375, 1376 (Fed. Cir. 2001) ("[A] claim cover[ing] several structures […] as alternatives […] is deemed anticipated if any of the structures […] within the scope of the claim is known in the prior art"). Ex. 1010, Bagherzadeh Decl., ¶¶ 44 and 45.

As to Challenged Claim 7 (Table 1, 7), Fukuzo '295Pub discloses that the data communicated between the DRAM and a non-volatile memory may be 8-bit data sequences of a 32-bit data word communicated by a host system to the DRAM . Ex. 1012, ¶¶[0112] and [0013]. A POSITA would understand that the 8-bit data sequences are intermediate data. Ex. 1010, Bagherzadeh Decl., ¶¶ 46 and 47.

As to Challenged Claim 8 (Table 1, 8), Fukuzo '295Pub discloses that the data transfer between the FIFO SDRAM 20 and the flash controller/memory 30 is part of the back-up/store operation. Ex. 1012., ¶¶[0127], [0080], [0085], and [0103].

As to Challenged Claim 9 (Table 1, 9), Fukuzo '295Pub discloses that the data transfer between the FIFO SDRAM 20 and the flash controller/memory 30 is part of the store operation, which is an automated operation controlled by a timing generator. Ex. 1012., ¶¶[0127 and [0103]. Further, Fukuzo '295Pub discloses that an automatic

backup operation is performed to accumulate data in the buffer. *Id.* A POSITA would understand that the automation of the operation must be in accordance with a repeating time interval, and that the accumulated data must be written to the non-volatile memory to avoid loss of data or lack of space in the buffer. Ex. 1010, Bagherzadeh Decl., ¶ 49 and 50.

As to Challenged Claim 10 (Table 1, 10), Fukuzo '295Pub discloses that the back-up/store operation occurs in response to a command signal. Ex. 1012., ¶¶[0127] and [0104].

As to Challenged Claim 11 (Table 1, 11), Fukuzo '295Pub discloses that an LD or load operation includes data transfer between the flash controller/memory 30 and the FIFO SDRAM 20, representing a restore mode of operation. Ex. 1012., ¶¶[0127], [0080], [0085], and [0103].

As to Challenged Claim 12 (Table 1, 12), Fukuzo '295Pub discloses that in a copy operation to restore data using the LD and CP commands ("the second mode of operation"), from the flash devices 30 to the SDRAM devices 10/20. *Id.*

As to Challenged Claim 13 (Table 1, 13), Fukuzo '295Pub discloses that pins are provided for the incoming clock signals, that may then be used to generate internal clock. *Id.,* ¶¶[0082] and [0084]. A POSITA would understand that the incoming clock is configurable by connection to the pin and that the clock generator is configured to generate the clock signals for the SDRAM FIFO buffer and the flash memory at each mode of operation. Ex. 1010, Bagherzadeh Decl., ¶¶ 55 and 56.

As to Challenged Claim 16 (Table 1, 16.a-b), Fukuzo '295Pub discloses that a FIFO data processor 210 ("a controller") is configured to control the data transfer bus 294 for connecting/disconnecting the flash buffer 390 of the flash devices 320/390/60 and the FIFO SDRAM array 290. Ex. 1012., ¶¶[0087], [0019], and [0027]. *Id.*, Excerpt from Fig. 3. A POSITA would understand that controlling the data transfer bus connects or disconnects the flash memory and the FIFO SDRAM buffer in accordance with the mode of data transfer, thereby disclosing limitations 16.a-b as claimed in part here. Ex. 1010, Bagherzadeh Decl., ¶¶ 57 and 58.

Challenged Claims 18, 20, and 22-29 (Table 1, 18, 20, and 22-29) claim subject matter similar to Corresponding Challenged Claims identified as follows, and should be rejected for similar reasons as their corresponding Challenged Claims, the reasons from which are incorporated for each: Challenged Claim 18 corresponds to Challenged Claim 2; 20 corresponds to 4; 22 corresponds to 6; 23 corresponds to 7; 24 corresponds to 8; 25 corresponds to 9; 26 corresponds to 10; 27 corresponds to 11; 28 corresponds to 12; and 29 corresponds to 13.

Fukuzo '295Pub anticipates Challenged Claims 2, 4, 6-13, 16, 18, 20, and 22-29. *Verdegaal Bros.*, 814 F.2d 628.

F. Ground 2 - Fukuzo '295Pub & Leete '210Pub Renders Obvious The Challenged Claims

Petitioner incorporates by reference, in this section, reasons for unpatentability in view of Fukuzo '295Pub for the independent claims from which the aforementioned Challenged Claims depend.

1. Dependent Claims 3, 5, 14, 17, 19, 21, And 30

As to Challenged Claim 3 (Table 1, 3), Leete '210Pub discloses a memory system including DRAM memory 704 and flash memory 706 configured to function in a reduced power mode of operation, where a capacitor provides power. Ex. 1013, ¶[0055]. A POSITA would seek to implement to the capacitor backup power from Leete '210Pub for the reduced power supply mode of operation, as disclosed in Fukuzo '295Pub (Ex. 1012, ¶[0012] and [0103]). Ex. 1010, Bagherzadeh Decl., ¶¶ 73 and 74.

As to Challenged Claim 5 (Table 1, 5), Leete '210Pub discloses that a power failure or reduction detection in power ("the trigger condition") can include a power failure ("comprises a power failure condition,"). Ex. 1013, ¶[0034] from Leete '210Pub. A POSITA would seek to implement to the power failure mode from Leete '210Pub for the reduced power supply mode of operation, as disclosed in Fukuzo '295Pub (Ex. 1012, ¶[0012]). Ex. 1010, Bagherzadeh Decl., ¶¶ 75 and 76.

As to Challenged Claim 14 (Table 1, 14), Leete '210Pub discloses aspects of the computer system, such as the real-time clock ("one or more of the first, second or

third clock frequencies") can be controlled by a user with a BIOS interface ("is configurable by a user"). Ex. 1013, ¶[0039] from Leete '210Pub. Since Fukuzo '295Pub discloses a clock generator with input pins to receive an external clock (Ex. 1012, ¶¶[0082] and [0084]), a POSITA would seek to implement the BIOS from Leete '210Pub to provide a configurable clock for all the frequencies applied to the memories. Ex. 1010, Bagherzadeh Decl., ¶¶ 77 and 78.

As to Challenged Claim 17 (Table 1, 17.a-b), Leete '210Pub discloses a memory system including a power source 716 and a capacitor-based backup battery unit 710 ("a plurality of a power supplies," Table 1, 17.a). As to limitation 17.b, Leete '210Pub discloses power failure and isolation circuitry ("a switch") that delivers power from the power source 716 to memory devices when there is no power failure or power reduction and selectively delivers power from the backup battery unit when there is a power failure or power reduction. Moreover, since Fukuzo '295Pub discloses a reduced power mode of operation (Ex. 1012, ¶[0012]), a POSITA would seek to implement the switch from Leete '210Pub to provide a switch from normal operation to the reduced power mode, thereby selecting among the multiple sources as disclosed in Leete '210Pub. Ex. 1010, Bagherzadeh Decl., ¶¶ 79 and 80.

Challenged Claims 19, 21, and 30 (Table 1, 19, 21, and 30) claim subject matter similar to Corresponding Challenged Claims identified as follows, and should be rejected for similar reasons as their corresponding Challenged Claims, the reasons

from which are incorporated for each: Challenged Claim 19 corresponds to Challenged Claim 3; 21 corresponds to 5; and 30 corresponds to 14.

Fukuzo '295Pub in view of Leete '210Pub renders obvious Challenged Claims 3, 5, 14, 17, 19, 21, and 30. *In re Royka, 490 F.2d 981, 985 (CCPA 1974).*

2. Motivation To Combine Fukuzo '295Pub and Leete '210Pub

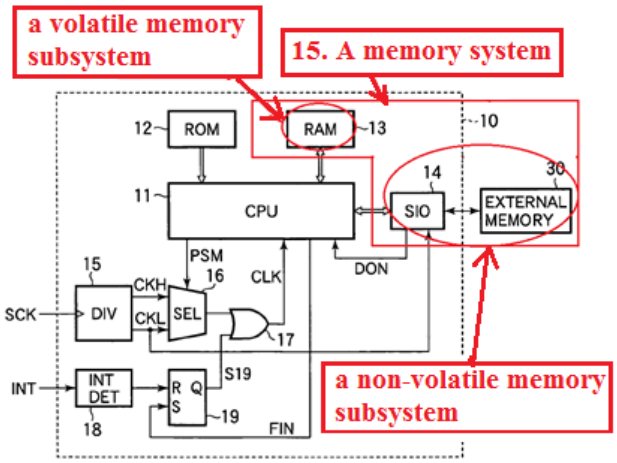
A POSITA would be motivated to combine Fukuzo '295Pub with Leete '210Pub, because both disclose a DRAM-Flash memory system functioning in a reduced power mode. Ex. 1010, Bagherzadeh Decl., ¶¶ 70-72. Specifically, Fukuzo '295Pub discloses connecting the FIFO memory array with the flash I/O buffer during <u>reduced power supply</u> (Ex. 1012, ¶¶[0012] and [0085]), while Leete '210Pub further discloses using <u>reduced power from a capacitor</u> instead of a regular battery (Ex. 1013, ¶[[0055]). Accordingly, one of ordinary skill would be motivated to combine the familiar elements in Leete '210Pub to operate Fukuzo '295Pub in the reduced power mode. Ex. 1010, Bagherzadeh Decl., ¶¶ 70-72. MPEP § 2141 Sec. I, ¶ 2; 75 F.R. 53650, *Examination Guidelines Update*, September 2010 ("The combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results.").

G. Ground 3 - Ichikawa '142 Anticipates The Challenged Claims

1. Independent Claims 1 And 15

The Challenged Claims recite, in part, "[a] method of controlling a memory system operatively coupled to a host system" (Table 1, 1.a) and "[a] memory system

operatively coupled to a host system" (Table 1, 15.a). Ichikawa '142 discloses an RAM-flash memory device as illustrated in Fig. 3 (annotated and reproduced here), coupled to CPU 11.



As to limitations 1.b, 15.b and 15.d (Table 1, 1.b, 15.b, 15.d), Ichikawa '142 discloses that RAM memory 13 receives data from the CPU 50 (Ex. 1014, 4:55-61, 3:47-49, and 3:50-52), and also communicates with flash memory system 14-30, constituting SIO and external flash memory 30. *Id.,* 3:57-59.

As to limitations 1.c-d (Table 1, 1.c-d, 15.c, and further to 15.b), Ichikawa '142 discloses that RAM 13 is clocked at <u>5 MHz</u> during read and write operations with the CPU 11, thereby disclosing limitations 1.c-d. *Id.,* 4:29-41, 2:38-40, and 3:50-56.

As to limitations 1.e-g and 15.d-g (Table 1, 1.e-h and 15.d-g), Ichikawa '142 discloses that the SIO and external flash memory 30 is clocked at <u>1 MHz</u> during read and write operations with RAM 20, thereby disclosing limitations 1.e-f and 15.d-e. *Id.,* 4:43-54, 4:55-61, and 3:57-59. Further, Ichikawa '142 discloses that RAM 20 functions at the 1 MHz clock during operations with SIO and external flash memory. *Id.,* 4:55-61. Accordingly, a POSITA would understand that the external flash memory and the RAM are communicating at the <u>same frequency</u> of 1 MHz to be able to transfer data between the components, thereby meeting limitations 1.g and 15.f.

Ex. 1010, Bagherzadeh Decl., ¶¶ 86 and 87. Since the 1 MHz clock during flash communications is less than the 5 MHz clock during host operations, the memory system of Ichikawa '142 discloses limitations 1.h and 15.g.

Ichikawa '142 anticipates Claims 1 and 15. *Verdegaal Bros.*, 814 F.2d 628 at 631.

2. Dependent Claims 2, 7, 8, 11-13, 18, 23, 24, And 27-29

As to Challenged Claim 2 (Table 1, 2), the reasons from Ichikawa '142 with respect to Challenged Claim limitation 1.h is applicable, and is therefore incorporated herein by reference.

As to Challenged Claim 7 (Table 1, 7), Ichikawa '142 discloses that the "RAM 13 is used to store application programs and data being processed" ("intermediate data from a host computer system computation"). Ex. 1014, 3:50-56.

As to Challenged Claim 8 (Table 1, 8), Ichikawa '142 discloses that the data transfer between the RAM and the flash memory is part of a data saving process in the power-saving mode operation. *Id.,* 2:43-45 and 3:57-59. A POSITA would understand that the data saved during the power-saving mode is backup data. Ex. 1010, Bagherzadeh Decl., ¶¶ 91 and 92.

As to Challenged Claim 11 (Table 1, 11), Ichikawa '142 discloses that the data transfer between the RAM and the flash memory is part of a data saving process in the power-saving mode operation. Ex. 1014, 2:43-45 and 3:57-59. A POSITA would understand that the data saved during the power-saving mode is backup data. Ex. 1010, Bagherzadeh Decl., ¶ 93.

As to Challenged Claim 12 (Table 1, 12), Ichikawa '142 discloses that the data transferred to the flash memory may be restored to the RAM volatile memory. Ex. 1014, 2:42-45.

As to Challenged Claim 13 (Table 1, 13), Ichikawa '142 discloses a selector 16 selects a low-speed clock signal CKL for the CPU 11. *Id.,*3:65-4:4 and 4:11-15. A POSITA would understand that the selector offers configurable clock signals for the RAM and the flash memory at each mode of operation. Ex. 1010, Bagherzadeh Decl., ¶ 95.

Challenged Claims 18, 23-24, and 27-29 (Table 1, 18, 23-24, and 27-29) claim subject matter similar to Corresponding Challenged Claims identified as follows, and should be rejected for similar reasons as their corresponding Challenged Claims, the reasons from which are incorporated for each: Challenged Claim 18 corresponds to Challenged Claim 2; 23 corresponds to 7; 24 corresponds to 8; 27 corresponds to 11; 28 corresponds to 12; and 29 corresponds to 13.

Ichikawa '142 anticipates Challenged Claims 2, 7-8, 11-13, 18, 23, 24, and 27-29. *Verdegaal Bros.*, 814 F.2d 628 at 631.

H. Ground 4 - Ichikawa '142 & Leete '210Pub Renders Obvious The Challenged Claims

Petitioner incorporates by reference, in this section, reasons for unpatentability in view of Ichikawa '142 for the independent claims from which the aforementioned Challenged Claims depend.

1. Dependent Claims 3-6, 9, 10, 14, 16, 17, 19-22, 25, 26, And 30

As to Challenged Claim 3 (Table 1, 3), Leete '210Pub discloses a memory system including DRAM memory 704 and flash memory 706 configured to function in a reduced power mode of operation, where a capacitor provides power ("is not powered by a battery when it is in the second mode of operation," Table 1, 3). Ex. 1013, ¶[0055] from Leete '210Pub. A POSITA would seek to implement to the capacitor backup power from Leete '210Pub for the reduced power supply mode of operation, as disclosed in Ichikawa '142 (Ex. 1014, 5:49-51). Ex. 1010, Bagherzadeh Decl., ¶¶ 106 and 107.

As to Challenged Claim 4 (Table 1, 4), Ichikawa '142 discloses a reduced power mode of operation during transfer of data between RAM 13 and external flash memory 30. Ex. 1014, 5:49-51. Further, Leete '210Pub discloses that power failure and isolation circuitry connects or disconnects the DRAM bank 1 from the computer bus powered by power source 716 to backup power 710, thereby switching the mode of operation to a low power mode. Ex. 1013, ¶¶[0042] and [0055]. The connection and disconnection representing different operation modes, based on the power failure state. A POSITA would seek to implement the switching circuitry from Leete '210Pub to manage the switch to the reduced power supply mode of operation, as disclosed in Ichikawa '142 (Ex. 1014, 5:49-51). Ex. 1010, Bagherzadeh Decl., ¶¶ 108 and 109.

As to Challenged Claim 5 (Table 1, 5), Leete '210Pub discloses that a power failure or reduction detection in power ("the trigger condition") can include a power failure ("comprises a power failure condition,"). Ex. 1013, ¶[0034. A POSITA would seek to implement the power failure mode from Leete '210Pub for the reduced power supply mode of operation, as disclosed in Ichikawa '142 (Ex. 1014, 5:49-51). Ex. 1010, Bagherzadeh Decl., ¶¶ 110 and 111.

As to Challenged Claim 6 (Table 1, 6.a-b), Leete '210Pub discloses a flash-based memory backup system for DRAM memory 704 (together constituting "memory system"). Ex. 1013, ¶[0057] and Fig. 7. Leete '210Pub also discloses that the memory system is located on a hardware mechanism, such as a memory board or DIMM. Ex. 1013, ¶¶[0078] and [0001]. A POSITA would understand that the memory boards or DIMMs from Leete '210Pub is typically in the form factor of printed circuit board, which may also include the integrated circuit RAM 13 and the SIO/external flash memory combination from Ichikawa '142 (Ex. 1014, 1:12-16), thereby disclosing limitation 6.a. Ex. 1010, Bagherzadeh Decl., ¶¶ 112 and 113.

Leete '210Pub discloses that the DRAM memory 704 and flash memory 706 (together constituting "memory system") are located on a memory board or DIMM. Ex. 1013, Leete '210Pub, ¶[0078] and [0001]. A POSITA would understand that the memory board or DIMM is in the form factor of printed circuit board with devices mounted thereon, where the devices can include both SDRAM 516' and flash 514b from Ichikawa '142 (Ex. 1014, 1:12-16). Ex. 1010, Bagherzadeh Decl., ¶ 112 and 113.

As to Challenged Claim 9 (Table 1, 9), Ichikawa '142 discloses that the data transfer between the RAM and the flash memory is part of a transitional period. Ex. 1014, 3:13-15. Further, Leete '210Pub discloses that the contents of the DRAM are copied to the non-volatile flash supplemental memory for preservation ("the backup operation") each time the contents in the cache is determined to be dirty ("is conducted at repeating time intervals"). Ex. 1013, ¶¶[0019] and [0067]. A POSITA would recognize that the verification of a dirty bit occurs periodically, and therefore the backup operation is periodic. Ex. 1010, Bagherzadeh Decl., ¶¶ 114 and115. A POSITA would also seek to apply the periodic dirty bit verification from Leete '210Pub to the transitional period of Ichikawa '142 to ensure that the data back-up in Ichikawa '142 is properly performed. Ex. 1010, Bagherzadeh Decl., ¶¶ 114 and 115.

As to Challenged Claim 10 (Table 1, 10), the reasons with respect to claim 9 apply, and are therefore incorporated herein by reference.

As to Challenged Claim 14 (Table 1, 14), Leete '210Pub discloses aspects of the computer system, such as the real-time clock ("one or more of the first, second or third clock frequencies") can be controlled by a user with a BIOS interface ("is configurable by a user"). Ex. 1013, ¶[0039]. Since Ichikawa '142 discloses a selector to select appropriate clock frequencies (Ex. 1014, 4:11-15), a POSITA would seek to implement the BIOS from Leete '210Pub to provide a configurable clock via the selector for all the frequencies applied to the memory. Ex. 1010, Bagherzadeh Decl., ¶¶ 118 and 119.

As to Challenged Claim 16 (Table 1, 16.a-b), Ichikawa '142 discloses that a CPU between the devices ("a controller") is configured to switch mode select from Power Saving to Normal mode, where in the normal mode, the high speed clock is applied to the CPU for normal operations. Ex. 1014, 5:34-45 and 4:29-41. A POSITA would understand that the flash memory does not operate under the high-speed clock, and therefore the CPU must isolate the flash memory while communicating with the volatile RAM 13 in normal operations. Ex. 1010, Bagherzadeh Decl., ¶ 120.

Further, Ichikawa '142 discloses that a low frequency clock of 1 MHz is applied to the volatile RAM memory and the SIO/external flash memory ("second mode of operation"). Ex. 1014, 4:43-55. This allows transfer of data between the RAM 13 and the SIO/external flash memory 30 during the power saving mode. *Id.* Still further, Leete '210Pub discloses that a recovery unit 708 between DRAM memory 704 and flash 706 is activated on detection of power failure using isolation circuitry. Ex. 1013, ¶¶[0034], [0060]-[0061], and [0058]. A POSITA would understand that the recovery unit 708 from Leete '210Pub may be applied to couple and decouple the RAM and the external flash memory in Ichikawa '142, thereby meeting the limitations 16.a-b. Ex. 1010, Bagherzadeh Decl., ¶¶ 121 and 122.

As to Challenged Claim 17 (Table 1, 17.a-b), Leete '210Pub discloses a memory system including a power source 716 and a capacitor-based backup battery unit 710 ("a plurality of a power supplies," Table 1, 17.a). Ex. 1013, ¶ [0058]. As to limitation

17.b, Leete '210Pub discloses power failure and isolation circuitry ("a switch") that delivers power from the power source 716 to memory devices when there is no power failure or power reduction and selectively delivers power from the backup battery unit when there is a power failure or power reduction. Since Ichikawa '142 discloses a reduced power mode of operation (Ex. 1013, 5:49-51), a POSITA would seek to implement the switch from Leete '210Pub to provide a switch from normal operation to the reduced power mode, thereby selecting among the multiple sources as disclosed in Leete '210Pub. Ex. 1010, Bagherzadeh Decl., ¶¶ 123 and 124.

Challenged Claims 19, 20-22, 25-26, and 30 (Table 1, 19, 20-22, 25-26, and 30) claim subject matter similar to Corresponding Challenged Claims identified as follows, and should be rejected for similar reasons as their corresponding Challenged Claims, the reasons from which are incorporated for each: Challenged Claim 19 corresponds to Challenged Claim 3; 20 corresponds to 4; 21 corresponds to 5; 22 corresponds to 6; 25 corresponds to 9; 26 corresponds to 10; and 30 corresponds to 14.

Ichikawa '142 in view of Leete '210Pub renders obvious Challenged Claims 3-6, 9, 10, 14, 16, 17, 19-22, 25, 26, and 30. *In re Royka, 490 F.2d 981, 985 (CCPA 1974).*

2. Motivation To Combine Ichikawa '142 And Leete '210Pub

A POSITA would be motivated to combine Ichikawa '142 with Leete '210Pub, because both references teach or suggest a volatile memory system backed by a non-volatile memory system for storage during a reduced power or power failure mode. Ex. 1010, Bagherzadeh Decl., ¶¶ 103-105. Specifically, Ichikawa '142 discloses a

RAM and external memory flash functioning in a mode using reduced power consumption (Ex. Ex. 1014, 5:49-51), while Leete '210Pub discloses a similar DRAM-Flash memory system, functioning in a mode using reduced power from a capacitor instead of a regular battery (Ex. 1013, ¶[0055]. Accordingly, a POSITA would be motivated to combine the familiar element of a capacitor in Leete '210Pub to operate Ichikawa '142 in a reduced power mode. Ex. 1010, Bagherzadeh Decl., ¶ 103-105. MPEP § 2141 Sec. I, ¶ 2; 75 F.R. 53650, *Examination Guidelines Update*, September 2010

I. Ground 5 - Long '552 Anticipates The Challenged Claims

1. Independent Claims 1 And 15

The Challenged Claims recite, in part, "[a] method of controlling a memory system operatively coupled to a host system" (Table 1, 1.a) and "[a] memory system operatively coupled to a host system" (Table 1, 15.a). Long '552 discloses an volatile memory cache 42 and a flash-based vault 44 as illustrated in Fig. 1 (annotated and reproduced here), coupled to hosts 21-22. Ex. 1015, 3:3-5 and 3:21-23.

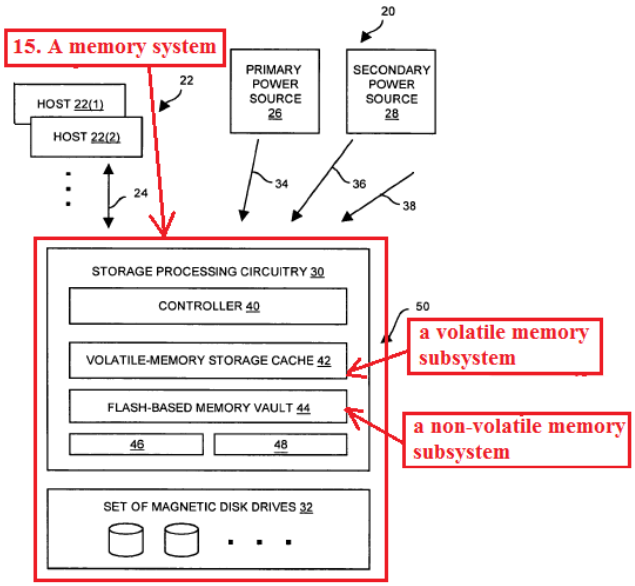


FIG. 1

As to limitations 1.b, 15.b and 15.d (Table 1, 1.b, 15.b, 15.d), Long '552 discloses that volatile memory cache 42 receives data from the host 21-22 (*Id.*, 3:50-

59, and 3:47-50), and also communicates with flash memory vault. *Id.,* 3:3-5 and 3:21-23.

As to limitations 1.c-d (Table 1, 1.c-d, 15.c, and further to 15.b), Long '552 discloses that RAM 13 is clocked at a relatively fast clock signal supported by 50-100 watts of power during read and write operations with the host, thereby disclosing limitations 1.c-d. *Id.,* 4:46-53 and 3:50-59. A POSITA would understand that the speed is proportional to the maximum power available to the components. Ex. 1010, Bagherzadeh Decl., ¶¶ 134 and 135.

As to limitations 1.e-g and 15.d-g (Table 1, 1.e-h and 15.d-g), Long '552 discloses that the flash memory vault is clocked at a significantly slower clock supported by less than 30 watts of power, which is applicable during read and write operations with the storage cache 42, thereby disclosing limitations 1.e-f and 15.d-e. Ex. 1015, 44:54-61. A POSITA would understand that since the available power is significantly less than during the host communication processes, the speed is significantly less for all the components in operation. Ex. 1010, Bagherzadeh Decl., ¶ 134 and 135. A POSITA would understand from Long '552 that the storage vault functions at the same significantly slower clock, with less than 30 watts of power, during operations with the flash memory vault, which is operating at the same clock speed. *Id.* Table 1, 1.g and 15.f. Since the clock at 50-100 watts is less than the clock at 150 watts, the memory system of Long '552 discloses limitations 1.h and 15.g.

Long '552 anticipates Claims 1 and 15. *Verdegaal Bros.*, 814 F.2d 628 at 631.

2. Dependent Claims 2, 7, 8, 11-13, 18, 23, 24, And 27-29

As to Challenged Claim 2 (Table 1, 2), the reasons from Long '552 with respect to Challenged Claim limitation 1.h is applicable, and is therefore incorporated herein by reference.

As to Challenged Claim 4 (Table 1, 4), Long '552 discloses that the controller switches from normal operating conditions ("the memory system switches from the first mode of operation") to a reduced power mode ("to the second mode of operation") upon receiving a power failure signal ("in response to a trigger condition"). Ex. 1015, 3:30-41.

As to Challenged Claim 5 (Table 1, 5), Long '552 discloses that the reduced power mode begins upon receipt of the power failure signal. *Id.*

As to Challenged Claim 7 (Table 1, 7), Long '552 discloses that any data in the cache is moved to flash memory during a loss of power so that no data is lost. Ex. 1015, 3:15-20 and 4:38-39. A POSITA would understand that the cache typically stores temporary or partial data representing the intermediate data of a

As to Challenged Claim 12 (Table 1, 12), Long '552 discloses that once the power failure signal is no longer received, the controller restores the contents ("a restore operation") of the volatile memory storage cache by moving data from the flash-based memory vault back into the volatile-memory storage cache to resume normal operations. Ex. 1015, 4:19-24 and 7:37-40.

As to Challenged Claim 13 (Table 1, 13), Long '552 discloses that the clock generator 46 configures the clock speed of the controller during normal storage operations. Ex. 1015, 4:46-51. A POSITA would understand that the clock generator 46 offers configurable clock signals for the volatile cache and the flash memory vault at each mode of operation. Ex. 1010, Bagherzadeh Decl., ¶¶ 142 and 143.

Challenged Claims 18, 20-21, 23, and 28-29 (Table 1, 18, 20-21, 23, and 28-29) claim subject matter similar to Corresponding Challenged Claims identified as follows, and should be rejected for similar reasons as their corresponding Challenged Claims, the reasons from which are incorporated for each: Challenged Claim 18 corresponds to Challenged Claim 3; 20 corresponds to 4; 21 corresponds to 5; 23 corresponds to 7; 28 corresponds to 12; and 29 corresponds to 13.

Long '552 anticipates Challenged 2, 4, 5, 12, 13, 18, 20, 21, 28, and 29. *Verdegaal Bros.*, 814 F.2d 628 at 631.

J. Ground 6 - Long '552 & Leete '210Pub Renders Obvious The Challenged Claims

Petitioner incorporates by reference, in this section, reasons for unpatentability in view of Long '552 for the independent claims from which the aforementioned Challenged Claims depend.

1. Dependent Claims 3, 6-11, 14, 16, 17, 19, 22-27, And 30

As to Challenged Claim 3 (Table 1, 3), Leete '210Pub discloses a memory system including DRAM memory 704 and flash memory 706 configured to function

in a reduced power mode of operation, where a capacitor provides power. Ex. 1013, ¶[0055] from Leete '210Pub. A POSITA would seek to implement to the capacitor backup power from Leete '210Pub for the mode of operation in Long '552 where primary power is lost (Ex. 1015, 4:54-61). Ex. 1010, Bagherzadeh Decl., ¶¶ 154 nad 155.

As to Challenged Claim 6 (Table 1, 6.a-b), Leete '210Pub discloses a flash-based memory backup system for DRAM memory 704 (together constituting "memory system"). Ex. 1013, ¶[0057] and Fig. 7. Further, Leete '210Pub discloses that the memory system is located on a hardware mechanism, such as a memory board or DIMM. Ex. 1013, ¶¶[0078] and [0001]. A POSITA would understand that the memory boards or DIMMs from Leete '210Pub is typically in the form factor of printed circuit board, which is similar to the memory card circuitry as disclosed in Long '552 (Ex. 1015, 6:39-47), thereby disclosing limitation 6.a. Ex. 1010, Bagherzadeh Decl., ¶¶ 156 and 157.

Leete '210Pub discloses that the DRAM memory 704 and flash memory 706 (together constituting "memory system") are located on a memory board or DIMM. Ex. 1013, Leete '210Pub, ¶[0078] and [0001]. A POSITA would understand that the memory board or DIMM is in the form factor of printed circuit board with devices mounted thereon, where the devices can include both volatile cache and the flash memory vault from Long '552 (Ex. 1015, 3:47-50), thereby disclosing limitation 6.b. Ex. 1010, Bagherzadeh Decl., ¶¶ 156 and 157.

As to Challenged Claim 7 (Table 1, 7), Long '552 discloses that any data in the cache is moved to flash memory during a loss of power so that no data is lost. Ex. 1015, 3:15-20 and 4:38-39. A POSITA would understand that the cache typically stores temporary or partial data representing the intermediate data of a computation. Ex. 1010, Bagherzadeh Decl., ¶¶ 158 and 159. Further, Leete '210Pub also discloses that data communicated between the memory block and the supplemental non-volatile memory includes temporary variable or other intermediate information. Ex. 1013, Leete '210Pub, ¶[0023] and [0062]. A POSITA would understand from the disclosures of Long '552 and Leete '210Pub that the cache data in Long '552 may include intermediate information as disclosed in Leete '210Pub. Ex. 1010, Bagherzadeh Decl., ¶¶ 158 and 159.

As to Challenged Claim 8 (Table 1, 8), Long '552 discloses that the data transfer between the RAM and the flash memory is part of a process to preserve data integrity in a loss of primary power mode. Ex. 1015, 4:54-58 and 3:15-20. A POSITA would understand that the data saved during data preserved refers to backup data. Ex. 1010, Bagherzadeh Decl., ¶¶ 160 and 161.

As to Challenged Claim 9 (Table 1, 9), Long '552 discloses that the data transfer between the RAM and the flash memory is part of a process to preserve data integrity in a loss of primary power mode. Ex. 1015, 4:54-58 and 3:15-20. Further, Leete '210Pub discloses that the contents of the DRAM are copied to the non-volatile flash supplemental memory for preservation ("the backup operation") each time the

contents in the cache is determined to be dirty. Ex. 1013., ¶¶[0019] and [0067]. A POSITA would recognize that the verification of a dirty bit occurs periodically, and therefore the backup operation is periodic. Ex. 1010, Bagherzadeh Decl., ¶¶ 162 and 163. A POSITA would also seek to apply the period dirty bit verification from Leete '210Pub to the data integrity process of Long '552 to ensure that the data back-up in Long '552 is properly performed. Ex. 1010, Bagherzadeh Decl., ¶¶ 162 and 163.

As to Challenged Claim 10 (Table 1, 10), the reasons with respect to claim 9 apply, and are therefore incorporated herein by reference.

As to Challenged Claim 11 (Table 1, 11), Long '552 discloses that the data transfer between the RAM and the flash memory is part of a data preservation process in the loss of primary power mode. Ex. 1015, 4:54-58 and 3:15-20. A POSITA would understand that the data saved during the power-saving mode is backup data. Ex. 1010, Bagherzadeh Decl., ¶¶ 166 and 167.

As to Challenged Claim 14 (Table 1, 14), Leete '210Pub discloses aspects of the computer system, such as the real-time clock ("one or more of the first, second or third clock frequencies") can be controlled by a user with a BIOS interface ("is configurable by a user"). Ex. 1013, ¶[0039]. Since Long '552 discloses a clock generator to select appropriate clock frequencies (Ex. 1015, 4:54-61), a POSITA would seek to implement the BIOS from Leete '210Pub to provide a configurable clock via the clock generator for all the frequencies applied to the memory. Ex. 1010, Bagherzadeh Decl., ¶¶ 168 and 169.

As to Challenged Claim 16 (Table 1, 16.a-b), Long '552 discloses that when controller 40 ("a controller") is powered by the primary power source ("in the first mode of operation"), it is configured to perform data storage operations with the volatile memory. Ex. 1015, 8:38-45. Leete '210Pub discloses that a recovery unit 708 between DRAM memory 704 and flash 706 is activated on detection of power failure using isolation circuitry ("a controller configured to decouple the non-volatile memory subsystem from the volatile memory subsystem in the first mode of operation"). Ex. 1013, ¶¶[0034], [0060]-[0061], and [0058]. A POSITA would understand that the recovery unit with the isolation circuitry to isolate the flash memory vault while the host is communicating with the volatile cache in normal operations. Ex. 1010, Bagherzadeh Decl., ¶¶ 170 and 171.

Further, Long '552 in view of Leete '210Pub discloses that once a power failure signal is received by the controller 40 ("in the second mode of operation"), the controller remains operational and moves data from the volatile-memory storage cache 42 ("the volatile memory subsystem") to the flash-based memory vault 44. Ex. 4:2-5. Leete '210Pub discloses that the recovery unit 708 between DRAM memory 704 and flash 706 is activated on detection of power failure using isolation circuitry. Ex. 1013, ¶¶[0034], [0060]-[0061], and [0058]. A POSITA would understand that the recovery unit 708 from Leete '210Pub may be applied to couple and decouple the volatile cache and the flash vault in Long '552, thereby meeting the limitations 16.a-b. Ex. 1010, Bagherzadeh Decl., ¶¶ 170 and 171.

As to Challenged Claim 17 (Table 1, 17.a-b), Leete '210Pub discloses a memory system including a power source 716 and a capacitor-based backup battery unit 710 ("a plurality of a power supplies," Table 1, 17.a). As to limitation 17.b, Leete '210Pub discloses power failure and isolation circuitry ("a switch") that delivers power from the power source 716 to memory devices when there is no power failure or power reduction and selectively delivers power from the backup battery unit when there is a power failure or power reduction. Ex. 1013, ¶¶[0059], [0060], and Fig. 7. Moreover, since Long '552 discloses mode of operation under loss of primary power (Ex. 1015, 3:38-41), a POSITA would seek to implement the switch from Leete '210Pub to provide a switch from normal operation to the mode under loss of primary power, thereby selecting among the multiple sources as disclosed in Long '552. Ex. 1010, Bagherzadeh Decl., ¶¶ 172 and 173.

Challenged Claims 19, 22-27, and 30 (Table 1, 19, 22-27, and 30) claim subject matter similar to Corresponding Challenged Claims identified as follows, and should be rejected for similar reasons as their corresponding Challenged Claims, the reasons from which are incorporated for each: Challenged Claim 19 corresponds to Challenged Claim 3; 22 corresponds to 6; 23 corresponds to 7; 24 corresponds to 8; 25 corresponds to 9; 26 corresponds to 10; 27 corresponds to 11; and 30 corresponds to 14.

Long '552 in view of Leete '210Pub renders obvious Challenged Claims 3, 6-11, 14, 16, 17, 19, 22-27, and 30. *In re Royka, 490 F.2d 981, 985 (CCPA 1974).*

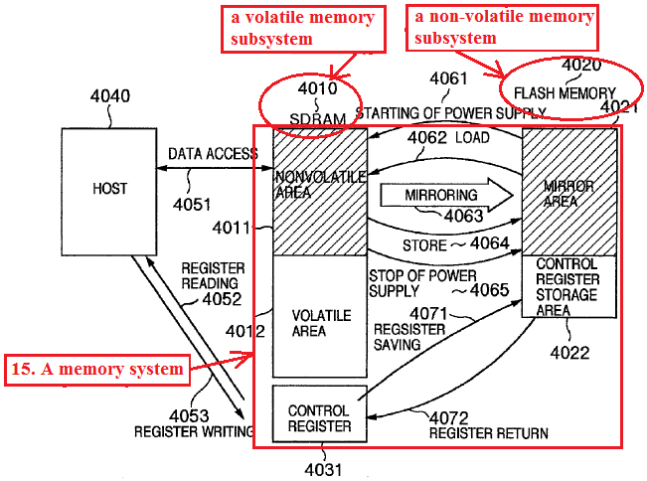
2. Motivation To Combine Long '552 And Leete '210Pub

A POSITA would be motivated to combine Long '552 with Leete '210Pub, because both references teach or suggest a volatile memory system backed by a non-volatile memory system for storage during a reduced power or power failure mode. Ex. 1010, Bagherzadeh Decl., ¶¶ 151 and 153. Furthermore, Long '552 discloses a backup process during loss of primary power (Ex. 1015, 3:38-41), while Leete '210Pub discloses using reduced power from a capacitor as a secondary source (Ex. 1013, ¶[0055]). Accordingly, a POSITA would be motivated to combine the familiar elements of Leete '210Pub to operate Long '552 in a loss of primary power mode. Ex. 1010, Bagherzadeh Decl., ¶¶ 151 and 153. MPEP § 2141 Sec. I, ¶ 2; 75 F.R. 53650, *Examination Guidelines Update*, September 2010

K. Ground 7 - Tsunoda '618 Anticipates The Challenged Claims

1. Independent Claims 1 And 15

The Challenged Claims recite, in part, "[a] method of controlling a memory system operatively coupled to a host system" (Table 1, 1.a) and "[a] memory system operatively coupled to a host system" (Table 1, 15.a). Tsunoda '618 discloses an volatile memory SDRAM 4010 and a flash



memory 4020 as illustrated in Fig. 24 (annotated and reproduced here), coupled to host 4040. Ex. 1016, 13:51-53, and 12:27-31

As to limitations 1.b, 15.b and 15.d (Table 1, 1.b, 15.b, 15.d), Tsunoda '618 discloses that volatile memory cache 42 receives data from the host 4040 during an SDRAM mode, and also communicates with flash memory during a flash mode. *Id.,*13:55-58 and 12:21-25 and Fig. 7.

As to limitations 1.c-d (Table 1, 1.c-d, 15.c, and further to 15.b), Tsunoda '618 discloses that SDRAM 4010 is clocked at <u>a high speed</u> during read and write operations with the host, thereby disclosing limitations 1.c-d. *Id.,* 13:51-53 and 11:51-54. A POSITA would understand that the high speed of a conventional SDRAM is applicable to Tsunoda '618, and would therefore know the speed as disclosed in Tsunoda '618. Ex. 1010, Bagherzadeh Decl., ¶¶ 184 and 185.

As to limitations 1.e-g and 15.d-g (Table 1, 1.e-h and 15.d-g), Tsunoda '618 discloses that the flash memory is clocked at <u>a speed different from the SDRAM,</u> which is applicable during read and write operations with the SDRAM, thereby disclosing limitations 1.e-f and 15.d-e. Ex. 1016, 12:21-25, 13:55-58, and 11:51-54. Tsunoda '618 also discloses a speed matching buffer 108 within the SDRAM that is <u>operational</u> during the flash transfer mode, to transfer data from the SDRAM to the flash memory. Ex. 1016, 11:51-54. Since Challenged Claim limitation 1.g requires in part, "<u>operating</u> the volatile memory <u>subsystem</u> at a third clock frequency" (Table 1, 1.g), a POSITA would understand that the speed matching buffer <u>is the operative</u>

component of the SDRAM when communicating with the flash memory at low speeds, thereby compensating for the speed difference and allowing communication between the slow speed flash memory and the SDRAM. Ex. 1010, Bagherzadeh Decl., ¶¶ 184 and 185. Accordingly, a POSITA would understand from Tsunoda '618 that the SDRAM operates at the slower clock, by virtue of the speed matching buffer, during operations with the flash memory, which is the speed of the flash memory. *Id.* Table 1, 1.g and 15.f. Since the SDRAM is operative at slow speeds with the flash memory compared to the high speed of the host, Tsunoda '618 discloses limitations 1.h and 15.g.

Tsunoda '618 anticipates Claims 1 and 15. *Verdegaal Bros.*, 814 F.2d 628 at 631.

2. Dependent Claims 2, 4, 5, 12, 13, 16, 18, 20, 21, 28, And 29

As to Challenged Claim 2 (Table 1, 2), the reasons from Tsunoda '618 with respect to Challenged Claim limitation 1.h is applicable, and is therefore incorporated herein by reference.

As to Challenged Claim 4 (Table 1, 4), Tsunoda '618 discloses that the system of Fig. 7 switches from an SDRAM mode 702 to a Flash transfer mode 703 in response to a CMDtx 706 command from the host. Ex. 1016, 13:49-58 and Fig. 7.

As to Challenged Claim 5 (Table 1, 5), Tsunoda '618 discloses the non-volatile memory may hold data after the power supply is stopped using the CMDtx signal from the host. *Id.,* 6:60-64 and 13:49-58.

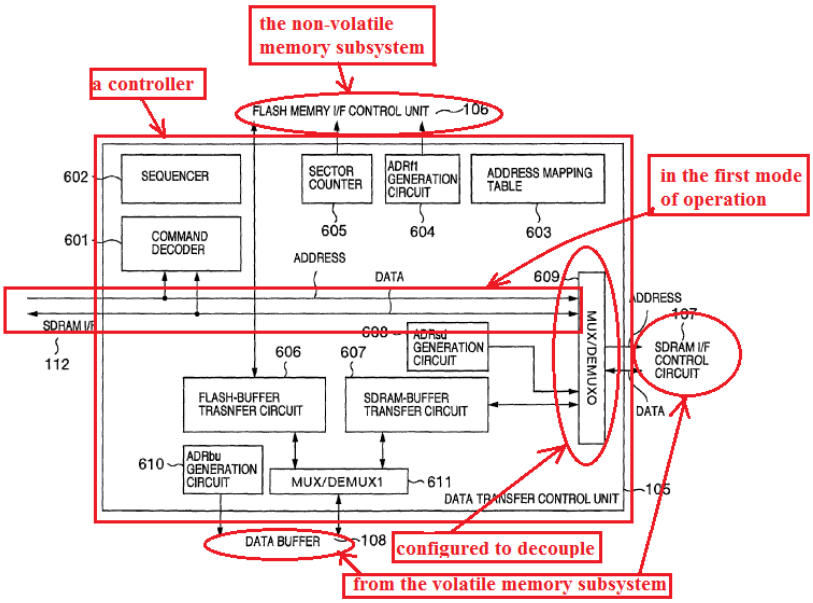
As to Challenged Claim 12 (Table 1, 12), Tsunoda '618 discloses that data is stored in the flash memory when the power is interrupted. Ex. 1016, 22:60-65. Further, Tsunoda '618 discloses that, at the start of power supply ("the second mode of operation"), data is loaded from the flash memory 4020 to the SDRAM 4010. *Id.,* 9:30-34. A POSITA would understand that the data previously stored in the flash memory at the time of power interruption is backup data. Accordingly, a POSITA understand that the operation for loading data from the flash memory at the start of the power supply is a restore operation. Ex. 1010, Bagherzadeh Decl., ¶¶ 189 and 190.

As to Challenged Claim 13 (Table 1, 13), Tsunoda '618 discloses that CLK 1 provides the clock frequency for the memory card. Furthermore, Tsunoda '618 discloses that the clock frequency CLK may be changed, thereby changing the frequencies at which the volatile and non-volatile memories communicate. Ex. 1016, 15:50-60.

As to Challenged Claim 16 (Table 1, 16, Tsunoda '618 discloses control unit 105 with multiplexer 609 to select ("a controller configured to decouple") the SDRAM-host bus, thereby isolating the SDRAM-buffer and Flash-buffer bus during the SDRAM transfer mode from the host ("in the first mode of operation"). *Id.,*14:17-23 and Fig. 6 (annotated and reproduced below). Further, Tsunoda '618 discloses transferring data from the flash memory to the SDRAM memory when the

flash transfer mode is selected using the multiplexer 609 in the second mode of operation. *Id.,*14:17-23 and 14:65-15:4.

Challenged Claims 18, 20-21, and 28-29 (Table 1, 18, 20-21, 23, and 28-29) claim subject matter similar to Corresponding Challenged Claims identified as follows, and should be rejected for similar reasons as their corresponding Challenged Claims, the reasons from which are incorporated for each: Challenged Claim 18 corresponds to Challenged Claim 2; 20 corresponds to 4; 21 corresponds to 5; 28 corresponds to 12; and 29 corresponds to 13.



Tsunoda '618 anticipates Challenged 2, 4, 5, 12, 13, 16, 18, 20, 21, 28, and 29. *Verdegaal Bros.*, 814 F.2d 628 at 631.

L. Ground 8 - Tsunoda '618 & Leete '210Pub Renders Obvious The Challenged Claims

Petitioner incorporates by reference, in this section, reasons for unpatentability in view of Tsunoda '618 for the independent claims from which the aforementioned Challenged Claims depend.

1. Dependent Claims 3, 6-11, 14, 17, 19, 22-27, And 30

As to Challenged Claim 3 (Table 1, 3), Leete '210Pub discloses a memory system including DRAM memory 704 and flash memory 706 configured to function in a reduced power mode of operation, where a capacitor provides power. Ex. 1013, ¶[0055] from Leete '210Pub. A POSITA would seek to implement to the capacitor backup power from Leete '210Pub for the mode of operation in Tsunoda '618 where power is interrupted (Ex. 1016, 22:60-65). Ex. 1010, Bagherzadeh Decl., ¶¶ 202 and 203.

As to Challenged Claim 6 (Table 1, 6.a-b), Leete '210Pub discloses a flash-based memory backup system for DRAM memory 704 (together constituting "memory system"). Ex. 1013, ¶[0057] and Fig. 7. Further, Leete '210Pub discloses that the memory system is located on a hardware mechanism, such as a memory board or DIMM. Ex. 1013, ¶¶[0078] and [0001]. A POSITA would understand that the memory boards or DIMMs from Leete '210Pub is typically in the form factor of printed circuit board, which is similar to the multimedia card circuitry as disclosed in Tsunoda '618 (Ex. 1016, 15:23-26), thereby disclosing limitation 6.a. Ex. 1010, Bagherzadeh Decl., ¶ 204 and 205.

Leete '210Pub discloses that the DRAM memory 704 and flash memory 706 (together constituting "memory system") are located on a memory board or DIMM. Ex. 1013, Leete '210Pub, ¶[0078] and [0001]. A POSITA would understand that the memory board or DIMM is in the form factor of printed circuit board with devices

mounted thereon, where the devices can include both SDRAM and the flash memory from Tsunoda '618 (Ex. 1016 , 4:2-6), thereby disclosing limitation 6.b. Ex. 1010, Bagherzadeh Decl., ¶¶ 204 and 206.

As to Challenged Claim 7 (Table 1, 7), Tsunoda '618 discloses that part of the data stored in the SDRAM during processing is transferred to the non-volatile flash memory when the power stops. Ex. 1016, 22:44-46. A POSITA would understand that the partial data is synonymous with the intermediate data from a computation. Ex. 1010, Bagherzadeh Decl., ¶ 206. Further, Leete '210Pub also discloses that data communicated between the memory block and the supplemental non-volatile memory includes temporary variable or other intermediate information. Ex. 1013, Leete '210Pub, ¶[0023] and [0062]. A POSITA would understand from the disclosures of Tsunoda '618 and Leete '210Pub that the temporary data in Tsunoda '618 may include intermediate information as disclosed in Leete '210Pub. Ex. 1010, Bagherzadeh Decl., ¶ 206 and 207.

As to Challenged Claim 8 (Table 1, 8), both Tsunoda '618 and Leete '210Pub disclose that data is communicated between the SDRAM volatile memory and flash memory when power is turned off. Ex. 1016, 12:21-25 and 13:49-58; and Ex. 1013, ¶[0067]. A POSITA would understand from these teachings that the data saved during the power off state refers to backup data. Ex. 1010, Bagherzadeh Decl., ¶¶ 208 and 209.

As to Challenged Claim 9 (Table 1, 9), Tsunoda '618 discloses that data is copied from SDRAM to flash after the SDRAM has been updated a designated number of times. Ex. 1016, 18:41-51. Further, Leete '210Pub discloses that the contents of the DRAM are copied to the non-volatile flash supplemental memory for preservation ("the backup operation") each time the contents in the cache is determined to be dirty ("is conducted at repeating time intervals"). Ex. 1013, ¶¶[0019] and [0067]. A POSITA would recognize that the verification of a dirty bit occurs periodically, and therefore the backup operation is periodic. Ex. 1010, Bagherzadeh Decl., ¶ 210. A POSITA would also seek to apply the period dirty bit verification from Leete '210Pub to verify the SDRAM updates in Tsunoda '618. Ex. 1010, Bagherzadeh Decl., ¶¶ 210 and 211.

As to Challenged Claim 10 (Table 1, 10), the reasons with respect to claim 9 apply, and are therefore incorporated herein by reference.

As to Challenged Claim 11 (Table 1, 11), Tsunoda '618 discloses that data is copied from SDRAM to flash after the SDRAM has been updated a designated number of times ("backup operation"). Ex. 1016, 18:41-51. Further, the reasons from Challenged Claim 9 pertaining to using a bit verification for a dirty bit is applicable here as a trigger condition. Accordingly, the reasons for Challenged Claim 9 are incorporated herein by reference.

As to Challenged Claim 14 (Table 1, 14), Leete '210Pub discloses aspects of the computer system, such as the real-time clock can be controlled by a user with a BIOS

interface ("is configurable by a user"). Ex. 1013, ¶[0039]. Since Tsunoda '618 discloses a terminal CLK 1 for receiving appropriate clock frequencies configured by the host (Ex. 1016, 15:50-52 and 15:56-60), a POSITA would seek to implement the BIOS from Leete '210Pub to provide a configurable clock via the clock generator for all the frequencies applied to the memory. Ex. 1010, Bagherzadeh Decl., ¶¶ 216 and 217.

As to Challenged Claim 17 (Table 1, 17.a-b), Tsunoda '618 discloses that the memory module receives power from a power supply. Ex. 1016, 7:55-57. Further, Leete '210Pub discloses a memory system including a power source 716 and a capacitor-based backup battery unit 710 ("a plurality of a power supplies," Table 1, 17.a). As to limitation 17.b, Leete '210Pub discloses power failure and isolation circuitry ("a switch") that delivers power from the power source 716 to memory devices when there is no power failure or power reduction and selectively delivers power from the backup battery unit when there is a power failure or power reduction. Moreover, since Tsunoda '618 discloses mode of operation when power is interrupted (Ex. 1016, 22:60-65), a POSITA would seek to implement the switch from Leete '210Pub to provide a switch from normal operation to the mode under loss of primary power, thereby selecting among the multiple sources as disclosed in Tsunoda '618. Ex. 1010, Bagherzadeh Decl., ¶¶ 218 and 219.

Challenged Claims 19, 22-27, and 30 (Table 1, 19, 22-27, and 30) claim subject matter similar to Corresponding Challenged Claims identified as follows, and should

be rejected for similar reasons as their corresponding Challenged Claims, the reasons from which are incorporated for each: Challenged Claim 19 corresponds to Challenged Claim 3; 22 corresponds to 6; 23 corresponds to 7; 24 corresponds to 8; 25 corresponds to 9; 26 corresponds to 10; 27 corresponds to 11; and 30 corresponds to 14.

Tsunoda '618 in view of Leete '210Pub renders obvious Challenged Claims 3, 6-11, 14, 17, 19, 22-27, and 30. *In re Royka, 490 F.2d 981, 985 (CCPA 1974).*

2. Motivation To Combine Tsunoda '618 And Leete '210Pub

A POSITA would be motivated to combine Tsunoda '618 with Leete '210Pub, because both references teach or suggest a volatile memory system backed by a non-volatile memory system for storage during a reduced power or power failure mode. Ex. 1010, Bagherzadeh Decl., ¶¶ 199 and 201. Furthermore, Tsunoda '618 discloses a memory apparatus 101 functioning in a flash transfer mode to transfer data from the SDRAM 103 to the NAND flash 102 <u>during a power interruption</u> (Ex. 1016, 22:60-65), while Leete '210Pub discloses a similar DRAM-Flash memory system, functioning in a mode using <u>reduced power from a capacitor</u> instead of a regular battery. Ex. 1013, ¶[0055]). Accordingly, a POSITA would be motivated to combine the familiar elements in Leete '210Pub to operate Tsunoda '618 in a loss of primary power mode. Ex. 1010, Bagherzadeh Decl., ¶¶ 199 and 201. MPEP § 2141 Sec. I, ¶ 2; 75 F.R. 53650, *Examination Guidelines Update*, September 2010.

VI. REASONABLE LIKELIHOOD THAT PETITIONER WOULD PREVAIL AT LEAST AS TO ONE OF THE CHALLENGED CLAIMS

The standard for instituting an *inter partes* review is:

> The Director may not authorize an *inter partes* review to be instituted unless the Director determines that the information presented in the petition filed under section 311 and any response filed under section 313 shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.

35 U.S.C. § 314(a). Petitioner has satisfied its burden under section 314(a) that there is a reasonable likelihood that Petitioner will prevail at least as to one of Challenged Claim.

Respectfully submitted,

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/Michael F. Heafey/

Michael F. Heafey
Registration No. 38,178
King & Spalding LLP
601 South California Avenue
Palo Alto, California 94304
(650) 422-6719 (telephone)
(650 422-6800 (facsimile)
mheafey@kslaw.com (email)

Sanjiva K. Reddy
Registration No. 70,816
King & Spalding LLP
1185 Avenue of the Americas
New York, New York 10036
(212) 556-2157 (telephone)
(212) 556-2222(facsimile)
sreddy@kslaw.com (email)

Certificate Of Service In Compliance With 37 C.F.R. § 42.6(e)(4)

The undersigned certifies that a complete copy of this Corrected Petition for *Inter Partes* Review was served on Counsel for Patent Owner in this proceeding:

Thomas J. Wimbiscus
Registration No. 36,059
twimbiscus@mcandrews-ip.com

Gregory C. Schodde
Registration No. 36,668
gschodde@mcandrews-ip.com

Scott P. McBride
Registration No. 42,853
smcbride@mcandrews-ip.com

Ronald H. Spuhler
Registration No. 52,245
rspuhler@mcandrews-ip.com

Wayne H. Bradley
Registration No. 39,916
wbradley@mcandrews-ip.com

All of: **McAndrews, Held & Malloy, Ltd.**
500 West Madison Street, 34th Floor
Chicago, Illinois 60661
(312) 755-8000 (telephone)
(312) 755-8100 (facsimile)

via Electronic Mail, on September 22, 2014.

/Sanjiva K. Reddy/

Sanjiva K. Reddy
Registration No. 70,816
King & Spalding LLP
1185 Avenue of the Americas
New York, New York 10036
(212) 556-2157 (telephone)
(212) 556-2222(facsimile)
sreddy@kslaw.com (email)