UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SK HYNIX INC., SK HYNIX AMERICA INC., and
SK HYNIX MEMORY SOLUTIONS INC.,
Petitioner,

v.

NETLIST, INC.,
Patent Owner.

Case IPR2017-00692
Patent 8,874,831 B2

Before STEPHEN C. SIU, MATTHEW R. CLEMENTS, and
SHEILA F. McSHANE, *Administrative Patent Judges*.

CLEMENTS, *Administrative Patent Judge*.

FINAL WRITTEN DECISION
Inter Partes Review
35 U.S.C. § 318(a) and 37 C.F.R. § 42.73

I. INTRODUCTION

In this *inter partes* review, instituted pursuant to 35 U.S.C. § 314, SK hynix Inc., SK hynix America Inc. and SK hynix memory solutions Inc. ("Petitioner") challenges claims 1–15 ("the challenged claims") of U.S. Patent No. 8,874,831 B2 (Ex. 1001, "the '831 patent"), owned by Netlist, Inc. ("Patent Owner"). We have jurisdiction under 35 U.S.C. § 6. This Final Written Decision is entered pursuant to 35 U.S.C. § 318(a) and 37 C.F.R. § 42.73. For the reasons discussed below, Petitioner has shown by a preponderance of the evidence that the challenged claims are unpatentable. Petitioner's Motion to Exclude is *dismissed*.

A. Procedural History

Petitioner filed a Petition requesting an *inter partes* review of claims 1–15 of the '831 patent. Paper 1 ("Pet."). Patent Owner filed a Preliminary Response. Paper 6. On July 21, 2017, we instituted *inter partes* review of (1) claims 1–14 of the '831 patent as unpatentable under 35 U.S.C. § 102[1] as anticipated by Best;[2] (2) claims 1–14 under 35 U.S.C. § 103(a) as obvious over Best; (3) claims 1–14 under 35 U.S.C. § 103(a) as obvious over Best and Roy;[3] and (4) claim 15 over Bowie under 35 U.S.C. § 103(a) as obvious

[1] The Leahy-Smith America Invents Act, Pub. L. No. 112–29, 125 Stat. 284 (2011) ("AIA"), amended 35 U.S.C. §§ 102 and 103. Because the '831 patent has an effective filing date before the effective date of the applicable AIA amendments, we refer to the pre-AIA versions of 35 U.S.C. §§ 102 and 103.

[2] U.S. Patent Publication No. 2010/0110748 A1 (Ex. 1006, "Best").

[3] U.S. Patent No. 6,065,092 (Ex. 1008, "Roy").

over Best, Mills,[4,5] and Bonella,[6] with or without Roy. Paper 7 ("Inst. Dec."), 28.

Thereafter, Patent Owner filed a Patent Owner Response (Paper 12, "PO Resp."), to which Petitioner filed a Reply (Paper 15, "Reply"). Petitioner filed a Motion to Exclude (Paper 17). Patent Owner filed an Opposition (Paper 20) to which Petitioner filed a Reply (Paper 22).

On April 24, 2018, we held a hearing and a transcript of the hearing is included in the record. Paper 24 ("Tr.").

On May 3, 2018, following the Supreme Court's decision in *SAS Inst., Inv. v. Iancu*, 138 S. Ct. 1348 (2018), we issued an Order (Paper 23) modifying our Institution Decision to include review of all challenged claims and all grounds presented in the Petition, including these grounds on which we had previously not instituted (Pet. 3, 28):

References	**Basis**	**Claim(s) challenged**
Best and Tsunoda, with or without Roy	§ 103	2 and 8
Best and Roohparvar,[7] with or without Roy	§ 103	5 and 12–14
Best, Mills,[8] Bonella, and Ashmore, with or without Roy	§ 103	15

[4] U.S. Patent No. 6,026,465 (Ex. 1010, "Mills").

[5] Although Petitioner does not include Mills (Ex. 1010) explicitly in its ground (Pet. 3), we include it because Petitioner's analysis relies upon it (*id.* at 61–64) for teaching part of a limitation.

[6] U.S. Patent Publication No. 2007/0136523 A1 (Ex. 1013, "Bonella").

[7] U.S. Patent Publication No. 2005/0273548 A1 (Ex. 1019, "Roohparvar").

[8] Although Petitioner does not include Mills (Ex. 1010) explicitly in its

In our order, we also stated that, "If, after conferring, the parties wish to submit further briefing, the parties must, within one week of the date of this Order, request a conference call with the panel to seek authorization for such briefing." Paper 23, 2. Neither party requested a conference call with the panel.

B. Related Proceedings

The parties indicate that the '831 patent is the subject of several district court cases and related *inter partes* reviews. Pet. 2; Paper 4, 3.

C. The '831 patent (Ex. 1001)

The '831 patent, titled "Flash-Dram Hybrid Memory Module," issued October 28, 2014, from U.S. Patent Application No. 13/559,476. Ex. 1001 at [54], [45], [21]. The '831 patent generally relates to a memory module with a non-volatile memory, a volatile memory, and a data manager through which the volatile memory and non-volatile memory may exchange data, and a controller to receive read/write commands from a memory controller hub ("MCH") and transfer data between any two or more of the MCH, volatile memory, and non-volatile memory. *Id.* at Abstract.

ground (Pet. 3), we include it because Petitioner's analysis relies upon it (*id.* at 61–64) for teaching part of a limitation.

Figure 4A is reproduced below.

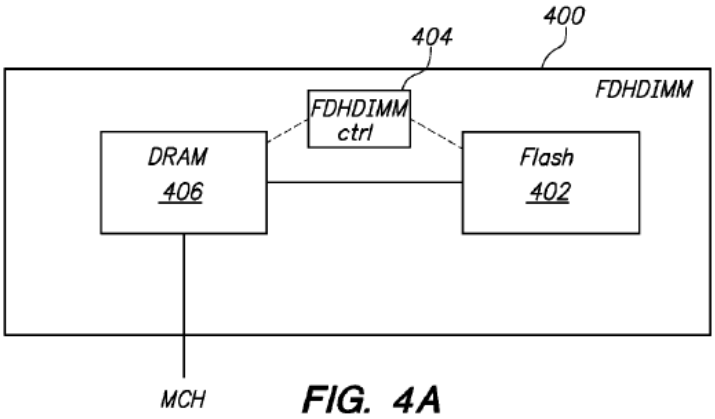


FIG. 4A

Figure 4A is a block diagram of a Flash-DRAM hybrid dynamic random access memory dual in-line memory module (DIMM). In this embodiment, volatile memory subsystem 406 (e.g. DRAM) is used as a data buffer such that data from Flash memory 402 is transferred to DRAM 406 at the Flash access speed, and buffered or collected into DRAM 406, which then transfers the buffered data to the MCH based on the access time of DRAM. *Id.* at 9:15–21. Similarly, when the MCH transfers data to DRAM 406, controller 404 manages the data transfer from DRAM 406 to Flash 402. *Id.* at 9:21–23.

Figure 5A is reproduced below.

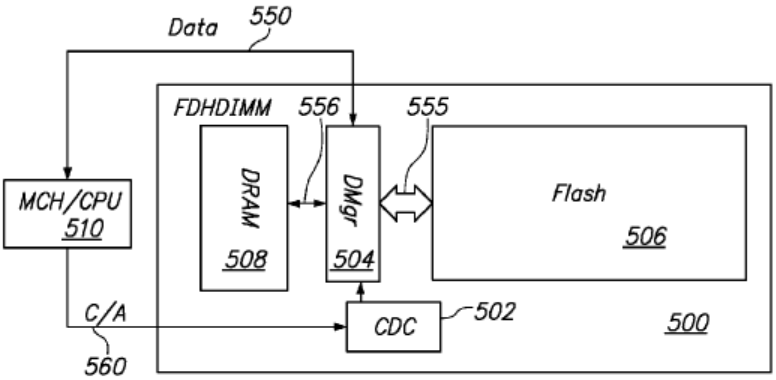


FIG. 5A

Figure 5A is a block diagram of memory module 500 in accordance with certain embodiments. Ex. 1001, 7:7–8. As shown in Figure 5, memory module 500 includes two on-module intermediary components: controller (CDC) 502 and data manager (DMgr) 504. *Id.* at 10:35–46. These components "manage the interface between a non-volatile memory subsystem such as a Flash 506, a volatile memory subsystem such as a DRAM 508, and a host system represented by MCH 510." *Id.* at 10:49–53. "In certain embodiments, CDC 502 controls the read/write access to/from Flash memory 506 from/to DRAM memory 508, and to/from DRAM memory from/to MCH 510." *Id.* at 10:54–56. "In certain embodiments and in response to communication from CDC 502, DMgr 504 provides a variety of functions to control data flow rate, data transfer size, data buffer size, data error monitoring or data error correction." *Id.* at 11:18–21.

Figure 6 is reproduced below.

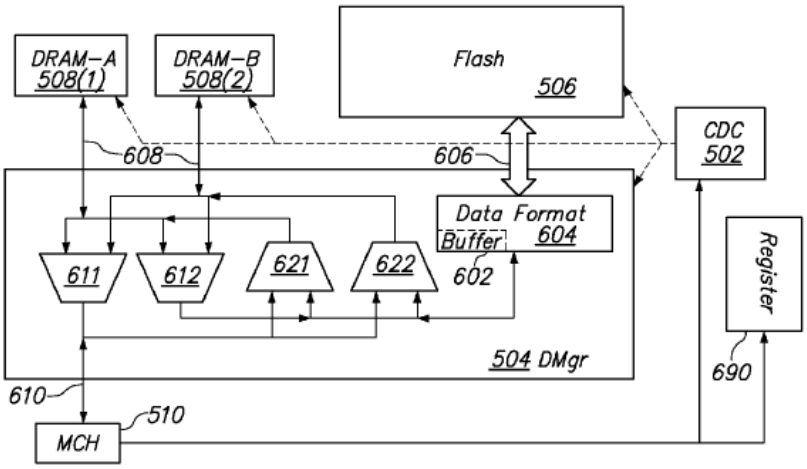


FIG. 6

Figure 6 is a block diagram showing some details of data manager 504. Ex. 1001, 7:11–12. "In certain embodiments, DMgr 504 also functions as a bi-directional data transfer fabric." *Id.* at 12:1–3. "For example, DMgr 504 may have more than 2 sets of data ports facing the Flash 506 and the DRAM

508." *Id.* at 12:3–5. "Multiplexers 611 and 612 provide controllable data paths from any one of the DRAMs 508(1) and 508(2) (DRAM-A and DRAM-B) to any one of the MCH 510 and the Flash 506." *Id.* at 12:5–8. "Similarly multiplexers 621 and 622 provide controllable data paths from any one of the MCH and the Flash memory to any one of the DRAMs 508(1) and 508(2) (DRAM-A and DRAM-B)." *Id.* at 12:8–11.

D. Illustrative Claim

Of the challenged claims, claims 1 and 7 are independent, claims 2–6 depend, directly or indirectly, from claim 1, and claims 8–15 depend, directly or indirectly, from claim 7. Independent claim 1 is illustrative of the challenged claims and is reproduced below:

> 1. A memory module couplable to a memory controller of a host system, comprising:
>
> a non-volatile memory subsystem;
>
> a data manager coupled to the non-volatile memory subsystem;
>
> a volatile memory subsystem coupled to the data manager and operable to exchange data with the non-volatile memory subsystem by way of the data manager; and
>
> a controller operable to receive commands from the memory controller and to direct (i) operation of the non-volatile memory subsystem, (ii) operation of the volatile memory subsystem, and (iii) transfer of data between any two or more of the memory controller, the volatile memory subsystem, and the non-volatile memory subsystem based on at least one received command from the memory controller, wherein:
>
> at least one of the volatile and non-volatile memory subsystems comprises one or more memory segments, each memory segment comprising at least one memory circuit, memory device, or memory die, and

> the data manager is configured as a bi-directional data transfer fabric having two or more sets of data ports, a first set of data ports of the two or more sets of data ports is coupled to the volatile memory subsystem, a second set of data ports of the two or more sets of data ports is coupled to the non-volatile memory subsystem, the two or more sets of data ports being operable by the data manager to transfer data to or from one or more memory segments of the volatile or non-volatile memory subsystems, the data manager further including a data buffer for buffering data delivered to or from the non-volatile memory subsystem, and a data format module configured to format data to be transferred between any two or more of the memory controller, the volatile memory subsystem, and the non-volatile memory subsystem based on control information received from the controller.

Ex. 1001, 17:44–18:13.

E. Instituted Grounds of Unpatentability

Petitioner asserted that the challenged claims are unpatentable based on the following grounds (Pet. 3), and trial has been instituted on these grounds (*see supra* Section I.A):

Reference(s)	**Basis**	**Claim(s) challenged**
Best	§ 102	1–14
Best and Roy	§ 103	1–14
Best and Tsunoda, with or without Roy	§ 103	2 and 8
Best and Roohparvar, with or without Roy	§ 103	5 and 12–14
Best, Mills,[9] and Bonella, with or without Roy	§ 103	15
Best, Mills,[10] Bonella, and Ashmore, with or without Roy	§ 103	15

[9] Petitioner does not include Mills (Ex. 1010) explicitly (Pet. 3), but the analysis relies upon it (*id.* at 61–64) for teaching part of a limitation.

[10] *See* n.9, above.

II. ANALYSIS

A. Claim Construction

We interpret claims of an unexpired patent using the broadest reasonable construction in light of the specification of the patent in which they appear. *See* 37 C.F.R. § 42.100(b); *see Cuozzo Speed Techs., LLC v. Lee*, 136 S. Ct. 2131, 2142–46 (2016). Under the broadest reasonable construction standard, claim terms are given their ordinary and customary meaning, as would be understood by one of ordinary skill in the art in the context of the entire disclosure. *In re Translogic Tech., Inc.*, 504 F.3d 1249, 1257 (Fed. Cir. 2007). Any special definition for a claim term must be set forth in the specification with reasonable clarity, deliberateness, and precision. *In re Paulsen*, 30 F.3d 1475, 1480 (Fed. Cir. 1994). We must be careful not to read a particular embodiment appearing in the written description into the claim if the claim language is broader than the embodiment. *See In re Van Geuns*, 988 F.2d 1181, 1184 (Fed. Cir. 1993). Only terms that are in controversy need to be construed, and then only to the extent necessary to resolve the controversy. *Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999).

1. "memory module"

Each independent claim recites a "memory module." Petitioner did not propose a construction for "memory module" in the Petition. Patent Owner argued, in its Preliminary Response, that "memory module" should be construed to mean "a carrier that contains one or more chips." Prelim. Resp. 21. In our Decision on Institution, we construed "memory module" to mean "a carrier that contains one or more memory chips," where "carrier"

encompasses an integrated circuit package. Inst. Dec. 9–10. We observed that

> The ’831 patent does not define a “memory module.” The ’831 patent depicts a memory module 500 in Figures 5A and 5B, and describes how “[i]n certain embodiments, memory module 500 is a Flash-DRAM hybrid memory module that has the DIMM (dual-inline memory module) form factor” (Ex. 1001, 10:28–31), but the ’831 patent also expressly contemplates other form factors (*see, e.g.*, *id.* at 10:32–34 (“it is to be understood that in both structure and operation [memory module 500] may be different from the FDHDIMM discussed above and described with reference to FIGS. 4A and 4B”), 10:46–49 (“While the DIMM form factor will predominate the discussion herein, it should be understood that this is for illustrative purposes only and memory systems using other form factors are contemplated as well.”).

Id.

In its Patent Owner Response, Patent Owner argues that “memory module” should be construed to mean “one or more memory segments on a printed circuit board” (“PCB”). PO Resp. 14–34. According to Patent Owner, “[e]very embodiment of a ‘memory module’ disclosed by the ’831 patent comprises a PCB” and its proposed construction “parallels how the term ‘memory module’ is used by those in the industry and standards bodies.” *Id*. at 15. Specifically, Patent Owner annotates Figure 5A, arguing that it shows “a PCB (yellow)”:

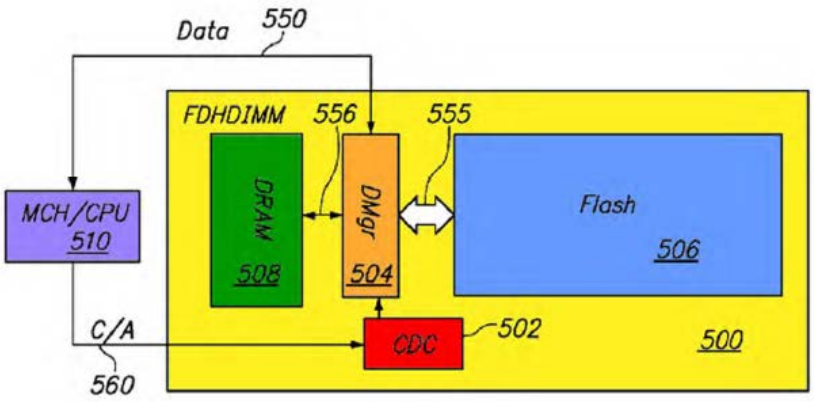


FIG. 5A

PO Resp. 16; *see also id.* at 20–23 ("Because the '831 specification only discloses embodiments including memory segments on a PCB, the claimed 'memory module' should be construed to cover such embodiments."). These arguments are not persuasive because the '831 patent does *not* describe 500, or any other embodiment, as a PCB. Instead, the '831 patent refers to 500 only as a "module." Ex. 1001, 10:14–15.

Patent Owner also argues that the '831 patent "repeatedly and consistently describes 'memory modules' as having a Dual In-Line Memory Module ('DIMM') form factor." PO Resp. 17. As Petitioner points out, however, claims are not limited to the embodiments described in the Specification. Pet. Reply 3–4 (citing *ACUMED LLC v. Stryker Corp.*, 483 F.3d 800, 805 (Fed. Cir. 2007)). Moreover, as we noted above, the '831 patent expressly contemplates other form factors for its "module" and, therefore, does not limit "module" to a DIMM form factor. *See, e.g.*, Ex. 1001, 10:32–49. The '831 patent states, for example

> These on-module intermediary components may be physically separate components, circuits, or modules, or they may be integrated onto a single integrated circuit or device, or integrated with other memory devices, for example in a three dimensional stack, or in any one of several other possible expedients for

> integration known to those skilled in the art to achieve a specific design, application, or economic goal.

Id. at 10:36–43.

For the same reasons, we are unpersuaded by Patent Owner's argument that boilerplate language cannot be used to broaden claims beyond what is disclosed in the Specification. PO Resp. 23–26.[11] The '831 patent's disclosure that "[w]hile the DIMM form factor will predominate the discussion herein, it should be understood that this is for illustrative purposes only and memory systems using other form factors are contemplated as well" (Ex. 1001, 10:46–49), is not mere boilerplate.

Patent Owner also relies upon disclosure in U.S. Patent Application No. 12/240,916 ("the '916 application"), of which the '831 patent is a continuation-in-part. PO Resp. 17–19; Ex. 1001 [63]. The '916 patent explicitly describes an embodiment in which memory system 10 comprises PCB 20. Ex. 2018 ¶ 31. This argument is not persuasive, however, because when the application leading to the '831 patent was filed, all references to "printed circuit board," "PCB," or even "board," were deleted from the Specification and the more generic word "module" was used instead. That the applicant for the '831 patent *removed* the words "PCB" and "printed circuit board" from the '916 application and used only the word "module" instead suggests, if anything, that applicant intended "module" *not* to be limited to a PCB.

[11] Patent Owner's citation to the "ID at 5–6" and the quote in parenthetical (Pet. 23–24) appears to be a citation to our Institution Decision in IPR2017-00560, not to our Institution Decision in this proceeding. Pet. Reply 10–11.

Patent Owner also relies upon a Final Written Decision in *Diablo Techs., Inc. v. Netlist, Inc.*, Case No. IPR2014-00882, concerning U.S. Patent 7,881,150 ("the '150 patent"). PO Resp. 26–27; Ex. 2021. Patent Owner's reliance on this decision is not persuasive, however, because the '150 patent is not related to the '831 patent and the Specification for the '150 patent is different from the Specification of the '831 patent. For example, the '150 patent explicitly discloses a printed circuit board, whereas the '831 patent does not.

Patent Owner also relies upon extrinsic evidence as support for its proposed construction. PO Resp. 27–31. There is no doubt that the DIMM form factor, including a PCB, was well-known. The issue, however, is whether the applicant for the '831 patent intended the term "memory module" to require a PCB. In light of the intrinsic evidence that the applicant deleted the words "printed circuit board" and "PCB" from the Specification, explicitly contemplated non-DIMM form factors, and even contemplated a controller and data manager "integrated with other memory devices" (Ex. 1001, 10:39–40), Patent Owner's extrinsic evidence does not persuade us that applicant intended "memory module" to require a PCB.

Patent Owner also argues that our preliminary determination that "carrier" encompasses an integrated circuit package is overly broad because (a) the '831 patent "does not describe any IC package comprising a PCB" and (b) it lacks any support from the industry or standards bodies. PO Resp. 33–34. We disagree. As discussed, the '831 patent explicitly contemplates integrating the controller and data manager "with other memory devices, for example in a three dimensional stack, or in any one of several other possible

expedients for integration known to those skilled in the art to achieve a specific design, application, or economic goal." Ex. 1001, 10:36–43.

Finally, Patent Owner argues, with respect to Best, that our construction "requires two layers of IC packages, in which a first IC package (the Board's 'carrier') contains one or more second IC packages (the Board's memory chips)." PO Resp. 39. Petitioner counters that "[t]he Board's construction does no such thing." Pet. Reply 18–19. We agree with Petitioner. Patent Owner's argument is predicated upon the erroneous assertion that "[e]ach memory chip in the Board's 'carrier' requires a different IC package (*i.e.*, a second IC package) that encloses at least one memory die." PO Resp. 39. Each memory chip does *not* require its own integrated circuit package. On the contrary, it may be, as Best discloses, a die enclosed with another die in a single IC package.

Having considered the arguments and evidence, we maintain our construction of "memory module" to mean "a carrier that contains one or more memory chips," where "carrier" encompasses an integrated circuit package.

B. Level of Ordinary Skill in the Art

Petitioner contends that a hypothetical person of ordinary skill in the art, with respect to and at the time of the'831 patent, "would be a person with a Bachelor's degree in materials science, electrical engineering, computer engineering, computer science, or in a related field and at least one year of experience with the design or development of semiconductor non-volatile memory circuitry or systems." Pet. 7; Ex. 1003 ¶¶ 55–56.

Patent Owner contends that such a person "would have been a person with a Bachelor's degree in electrical and/or computer engineering and at

least five years of industry experience designing memory devices and controllers" but that "[a] Master of Science degree in electrical and/or computer engineering would substitute for two years of industry experience" and "[a] Doctorate degree in electrical and/or computer engineering would substitute for four years of industry experience." PO Resp. 43; Ex. 2016 ¶ 32.

Patent Owner argues that a degree in material science would *not* be equivalent to a degree in electrical and/or computer engineering, and that Petitioner's expert, Mr. Maltiel, who has only a degree in materials science, is not competent to testify to the understanding of a person of ordinary skill in the art. PO Resp. 43–44. Patent Owner did not, however, move to exclude the testimony of Mr. Maltiel. To the extent Patent Owner is arguing that we should accord Mr. Maltiel's testimony little to no weight based on his qualifications, we decline to do so. After earning three degrees, Mr. Maltiel joined Intel in 1980 to work on the first commercial non-volatile EEPROM devices and, therefore, had 27 years of industry experience as of the earliest priority date to which the '831 patent could be entitled. Ex. 1003 ¶¶ 3–9. Mr. Maltiel was recognized as a Senior Member of the IEEE in 2008 and is a named inventor on six United States patents covering various aspects of memory devices, including for combining non-volatile and DRAM memories. *Id.* ¶¶ 10–12. As a result, we are persuaded that Mr. Maltiel is qualified to testify as to the understanding of a person of ordinary skill in the art at the time of the '831 patent.

Otherwise, we determine that no express finding on a specific corresponding level of technical education and experience is necessary. Here, the level of ordinary skill in the art is reflected by the prior art of

record. *See Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001); *In re GPAC Inc.*, 57 F.3d 1573, 1579 (Fed. Cir. 1995); *In re Oelrich*, 579 F.2d 86, 91 (CCPA 1978).

C. Whether to Give Weight to Mr. Maltiel's Testimony

Patent Owner argues that Mr. Maltiel's testimony should be given no weight because it is neither reliable nor credible. PO Resp. 41–42; *see also id.* at 62–64. In support of the argument, Patent Owner directs attention to portions of Dr. Maltiel's cross examination testimony where he allegedly (1) "contradicted himself on critical matters;" (2) "made a number of statements that are simply incorrect;" and (3) "concede[d] that he did not consider the complete intrinsic record, including the '916 patent application." *Id*.

Petitioner counters that Mr. Maltiel is qualified, reliable, and credible. Pet. Reply 24–25.

We have reviewed the arguments provided by Patent Owner and determine such arguments are insufficient to have Mr. Maltiel's declaration excluded in its entirety. Rather, it is within our discretion to assign the appropriate weight to be accorded evidence. *See* 37 C.F.R. § 42.65(a); *see also, e.g.*, *Yorkey v. Diab*, 601 F.3d 1279, 1284 (Fed. Cir. 2010) (holding the Board has discretion to give more weight to one item of evidence over another "unless no reasonable trier of fact could have done so"); *In re Am. Acad. of Sci. Tech Ctr.*, 367 F.3d 1359, 1368 (Fed. Cir. 2004) ("[T]he Board is entitled to weigh the declarations and conclude that the lack of factual corroboration warrants discounting the opinions expressed in the declarations."); and *Velander v. Garner*, 348 F.3d 1359, 1371 (Fed. Cir. 2003) ("In giving more weight to prior publications than to subsequent conclusory statements by experts, the Board acted well within [its]

discretion.”). Based on the record before us, we are not persuaded that we should give the entirety of Mr. Maltiel’s declaration no weight.

D. The Parties’ Post-Institution Arguments

In our Decision on Institution, we concluded that the arguments and evidence advanced by Petitioner demonstrated a reasonable likelihood that (1) claims 1–14 of the ’831 patent are unpatentable under 35 U.S.C. § 102 as anticipated by Best; (2) claims 1–14 under 35 U.S.C. § 103(a) are obvious over Best; (3) claims 1–14 under 35 U.S.C. § 103(a) are obvious over Best and Roy; and (4) claim 15 over Bowie under 35 U.S.C. § 103(a) is obvious over Best, Mills, and Bonella, with or without Roy. Inst. Dec. 28. We subsequently instituted on the remaining grounds asserted by Petitioner. Paper 23. We must now determine whether Petitioner has established by a preponderance of the evidence that claims 1–15 are unpatentable over the cited prior art. 35 U.S.C. § 316(e). We previously instructed Patent Owner that “any arguments for patentability not raised in the [Patent Owner Response] will be deemed waived.” Paper 3, 3; *see also* 37 C.F.R. § 42.23(a) (“Any material fact not specifically denied may be considered admitted.”); *In re Nuvasive, Inc.*, 842 F.3d 1376, 1379–1382 (Fed. Cir. 2016) (holding Patent Owner waived an argument addressed in Preliminary Response by not raising the same argument in the Patent Owner Response). Additionally, the Board’s Trial Practice Guide states that the Patent Owner Response “should identify all the involved claims that are believed to be patentable and state the basis for that belief.” Office Patent Trial Practice Guide, 77 Fed. Reg. 48,756, 48,766 (Aug. 14, 2012).

With a complete record before us, we note that we have reviewed arguments and evidence advanced by Petitioner to support its unpatentability

contentions where Patent Owner chose not to address certain limitations in its Patent Owner Response. In this regard, the record now contains persuasive, unrebutted arguments and evidence presented by Petitioner regarding the manner in which the asserted prior art teaches corresponding limitations of the claims against which that prior art is asserted. Based on the preponderance of the evidence before us, we conclude that the prior art identified by Petitioner teaches or suggests all uncontested limitations of the reviewed claims. The limitations that Patent Owner contests in the Patent Owner Response are addressed below.

E. Claims 1–14: Anticipation by Best

Petitioner argues that claims 1–14 are unpatentable under 35 U.S.C. § 102(e) as anticipated by Best. Pet. 20–49.

1. Principles of Law

To establish anticipation, "all of the elements and limitations of the claim must be shown in a single prior reference, arranged as in the claim." *Karsten Mfg. Corp. v. Cleveland Golf Co.*, 242 F.3d 1376, 1383 (Fed. Cir. 2001). When evaluating a single prior art reference in the context of anticipation, the reference must be "considered together with the knowledge of one of ordinary skill in the pertinent art." *In re Paulsen*, 30 F.3d 1475, 1480 (Fed. Cir. 1994) (citing *In re Samour*, 571 F.2d 559, 562 (CCPA 1978)). "'[T]he dispositive question regarding anticipation[, therefore, i]s whether *one skilled in the art* would reasonably understand or infer from the [prior art reference's] teaching' that every claim element was disclosed in that single reference." *Dayco Prods., Inc. v. Total Containment, Inc.*, 329 F.3d 1358, 1368 (Fed. Cir. 2003) (alterations in original) (quoting *In re Baxter Travenol Labs.*, 952 F.2d 388, 390 (Fed. Cir. 1991)). We analyze

this asserted ground based on anticipation with the principles stated above in mind.

2. Best Overview

Best is directed to a hybrid volatile and non-volatile memory device. Ex. 1006, Abstract. Specifically, Best discloses "[a]composite, hybrid memory device including a first storage die having an array of volatile storage cells and a second storage die having an array of non-volatile storage cells disposed within an integrated circuit package." *Id.* "The hybrid memory device includes a shared interface circuit to receive memory access commands directed to the first storage die and the second storage die and to convey read and write data between an external data path and the first and second storage dice." *Id.*

Figure 2 of Best is reproduced below.

FIG. 2

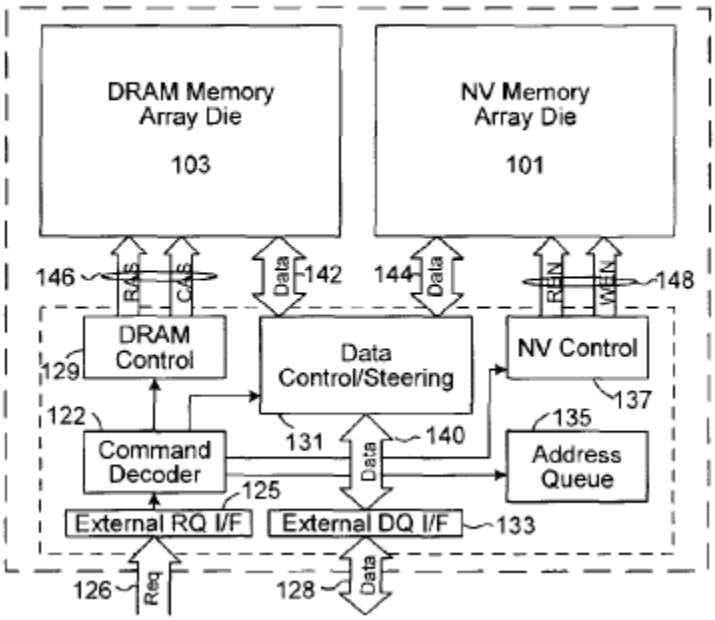


Figure 2 illustrates an embodiment of a hybrid, composite memory device with shared interface circuitry, volatile memory, and non-volatile memory.

Id. ¶ 17. "[T]he shared interface circuitry includes an external request interface 125, external data interface 133, command decoder 122, address queue 135, DRAM control circuit 129, Flash control circuit 137, and data control/steering circuit 131." *Id.* "[I]ncoming control signals and addresses . . . are received in the external request interface 125 via control/address (CA) path 126, reformatted as necessary (e.g., deserialized to form a parallel command word and one or more address values) and then forwarded to the command decoder 122." *Id.* "The command decoder 122 in turn forwards address to the address queue 135 and stores memory access commands." *Id.* "[M]emory access operations may be automatically directed to either the volatile storage die or non-volatile storage die according to the memory address to be accessed." *Id.* "[C]ommand decoder 122 outputs, from the head of the command queue, an enable signal and corresponding memory access control signals to the DRAM control circuit 129 and NV control circuit 137." *Id.* ¶ 18. "[D]ata control/steering circuit 131 is used to control the transfer of data between a shared internal data bus and dedicated internal data buses associated with the volatile and non-volatile storage dice, respectively." *Id.* ¶ 20.

Figure 3 of Best is reproduced below.

FIG. 3

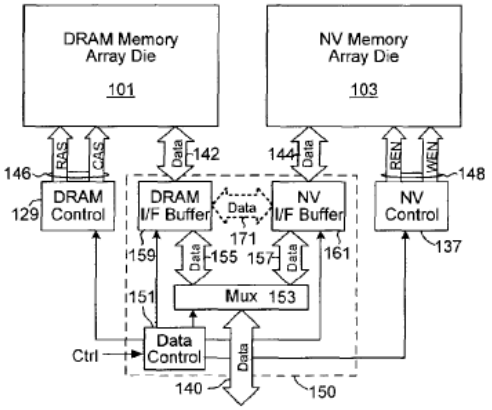


Figure 3 illustrates an embodiment of a data control/steering circuit 150 that may be used to implement the data control/steering circuit 131 of Figure 2. *Id.* ¶ 21. "[D]ata control circuit 151 receives control signals from the command decoder that indicate the direction of data flow during a memory access operation (read or write) and whether the volatile or non-volatile storage die is the target of the memory access." *Id.*

3. Petitioner's Initial Positions

Petitioner contends that Best anticipates claims 1–14 of the '831 patent. Pet. 20–49. We have reviewed the Petition, Patent Owner's Response, and Petitioner's Reply, as well as the relevant evidence discussed in those papers and other record papers, and are persuaded that the record establishes Petitioner's contentions for claims 1–14, and we adopt Petitioner's contentions discussed below as our own.

For example, Claim 1 recites "[a] memory module couplable to a memory controller of a host system." Petitioner relies upon Best's disclosure of "a 'hybrid composite memory device having non-volatile and volatile memories implemented in distinct integrated circuit (IC) dice that are packaged together and accessed through a shared interface.'" Pet. 20 (quoting Ex. 1006 ¶ 12). In light of our construction of "memory module" to mean "a carrier that contains one or more memory chips," where "carrier" encompasses an integrated circuit package, we are persuaded by Petitioner's showing and find that Best's integrated circuit package containing first and second storage die teaches the recited "memory module."

Claim 1 further recites "a non-volatile memory subsystem." Petitioner relies upon Best's disclosure of a Flash memory. Pet. 21. We are

persuaded by Petitioner's showing and find that Best's Flash memory teaches the recited "non-volatile memory subsystem."

Claim 1 further recites "a data manager coupled to the non-volatile memory subsystem." Petitioner relies upon Best's data control/steering circuit in combination with the external interface. Pet. 21–22 (citing Ex. 1006, Figure 3). We are persuaded by Petitioner's showing and find that Best's data control/steering circuit in combination with the external interface teaches the recited "data manager."

Claim 1 further recites "a volatile memory subsystem." Petitioner relies upon Best's disclosure of a DRAM. Pet. 22–23. We are persuaded by Petitioner's showing and find that Best's DRAM teaches this limitation.

Claim 1 further recites "a controller." Petitioner relies upon Best's command decoder 122, which receives "incoming control signals and addresses" and directs operation of the volatile and non-volatile memories by "output[ting] . . . an enable signal and corresponding memory access control signals to the DRAM control circuit . . . and NV control circuit," and transfers data between the memories and memory controller. Pet. 23–24 (citing Ex. 1006 ¶¶ 17–19, 21, 29). We are persuaded by Petitioner's showing and find that Best's command decoder 122 teaches the recited "controller."

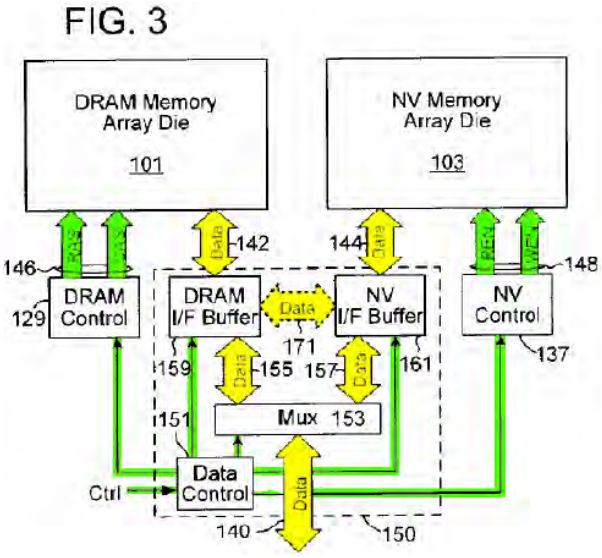
Claim 1 further recites "at least one of the volatile and non-volatile memory subsystems comprises one or more memory segments." Petitioner relies upon Best's disclosure that "the volatile and non-volatile memories [are] implemented by a DRAM die 103 and Flash memory die 101, respectively," each of which, according to Petitioner, is a memory segment. Pet. 24–25. We are persuaded by Petitioner's showing and find that Best's

DRAM die 103 and Flash memory die 101 teach the recited "one or more memory segments."

Claim 1 further recites

> the data manager is configured as a bi-directional data transfer fabric having two or more sets of data ports, a first set of data ports of the two or more sets of data ports is coupled to the volatile memory subsystem, a second set of data ports of the two or more sets of data ports is coupled to the non-volatile memory subsystem, the two or more sets of data ports being operable by the data manager to transfer data to or from one or more memory segments of the volatile or non-volatile memory subsystems.

Petitioner relies upon Best's disclosure of an interface to the primary volatile data path 142 between data control/steering circuit 150 and DRAM 101 ("a first set of data ports . . . coupled to the volatile memory subsystem"), and of an interface to primary non-volatile data path 144 between data control steering circuit 150 and NV memory 103 ("a second set of data ports . . . coupled to the non-volatile memory subsystem"). Pet. 25–26. Petitioner contends that each set of interconnections is "bi-directional" because data can flow in either direction, and illustrates the point with an annotated version of Figure 3, reproduced below:



We are persuaded by Petitioner's showing and find that Best's interfaces to primary volatile data path 142 and to primary non-volatile data path 144, respectively, as illustrated in annotated Figure 3 above, teach the recited "two or more sets of data ports."

Finally, claim 1 recites

> the data manager further including a data buffer for buffering data delivered to or from the non-volatile memory subsystem, and a data format module configured to format data to be transferred between any two or more of the memory controller, the volatile memory subsystem, and the non-volatile memory subsystem based on control information received from the controller.

Petitioner relies upon Best's disclosure of "non-volatile-storage-die interface buffer 161" as the recited "data buffer" (Pet. 27–28), and relies upon Best's disclosure of logic for serializing/deserializing within data steering/control circuit and the external data interface as the recited "data format module" (*id.* at 28–30). We are persuaded by Petitioner's showing and find that Best's non-volatile-storage-die interface buffer 161 teaches the recited "data buffer."

We also are persuaded that Petitioner's citations support its contentions with respect to claim 7, for which Petitioner relies upon largely the same disclosures in Best (Pet. 38–43).

Petitioner has provided a similar detailed analysis of claims 2–6 and 8–14. Pet. 30–37, 44–49. Notwithstanding Patent Owner's arguments, which we have considered and which we address below, we are persuaded by Petitioner's showing, which we adopt as our own findings and conclusions, that claims 1–14 are unpatentable under 35 U.S.C. § 102 as anticipated by Best.

4. Patent Owner's Assertions Concerning Best

Patent Owner argues that Best does not disclose a "memory module" because it is implemented on a single integrated circuit package—i.e., a single chip. PO Resp. 34–41. Specifically, Patent Owner argues that (1) Petitioner's expert testified that a "memory module" and an "IC package" are "totally different terms;" (2) Best's dual-die chip teaches away from a memory module; (3) Best does not teach an IC package within another IC package; and (4) Best does not teach a PCB. *Id.*

Petitioner counters that (1) Mr. Maltiel testified specifically that Best's specific disclosure of an IC package teaches a "memory module" as a person of ordinary skill in the art would have understood it; and (2) Patent Owner's alleged "teaching away" is irrelevant in an anticipation analysis. Pet. Reply 17–18. We agree.

Moreover, Patent Owner's remaining arguments are not persuasive because they are based upon Patent Owner's proposed construction of "memory module," which we do not adopt for the reasons discussed above. Because our broadest reasonable construction of "memory module" encompasses an integrated circuit package and because Best discloses an integrated circuit package with two die, we are persuaded that Best discloses this limitation.

Patent Owner does not separately argue claims 2–14.

5. Summary

For the foregoing reasons, we are persuaded that Petitioner has established, by a preponderance of the evidence, claims 1–14 of the '831 patent are unpatentable under 35 U.S.C. § 102 as anticipated by Best.

F. Claim 1–14: Obviousness over Best

Although Petitioner challenges claims 1–14 as obvious over "Best in view of Roy" (Pet. 3), its other obviousness challenges are "with or without Roy" (*id.*). We, therefore, interpret the Petition to allege that claims 1–14 also are obvious over Best alone.

As discussed above, we are persuaded that Petitioner has established, by a preponderance of the evidence, that claims 1–14 are unpatentable as anticipated by Best. Patent Owner relies upon the same argument as for Ground 1—i.e., that Best does not teach a "memory module"—and argues that the Petition fails to show that Roy teaches a "memory module." PO Resp. 45. We are not persuaded by that argument for the reasons discussed above.

Inasmuch as "anticipation is the epitome of obviousness" (*In re McDaniel*, 293 F.3d 1379, 1385 (Fed. Cir. 2002)) and because there is no evidence of objective indicia of non-obviousness on the record, we determine that Petitioner has also established, by a preponderance of the evidence, that claims 1–14 would have been obvious over Best.

G. Claims 1–14: Obviousness over Best and Roy

Petitioner argues that claims 1–14 are unpatentable under 35 U.S.C. § 103(a) as obvious over the combination of Best and Roy. Pet. 49–53.

1. Principles of Law

A claim is unpatentable under § 103(a) if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.

KSR Int'l Co. v. Teleflex Inc., 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations, including (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of skill in the art; and (4) when in evidence, objective indicia of non-obviousness (i.e., secondary considerations). *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966). We analyze this asserted ground based on obviousness with the principles identified above in mind.

2. Roy Overview

Roy is directed generally to an "independent and cooperative multichannel memory architecture" that includes a plurality of independent channels between a master device and one or more memory clusters. Ex. 1008, Abstract. Figure 1 of Roy is reproduced below.

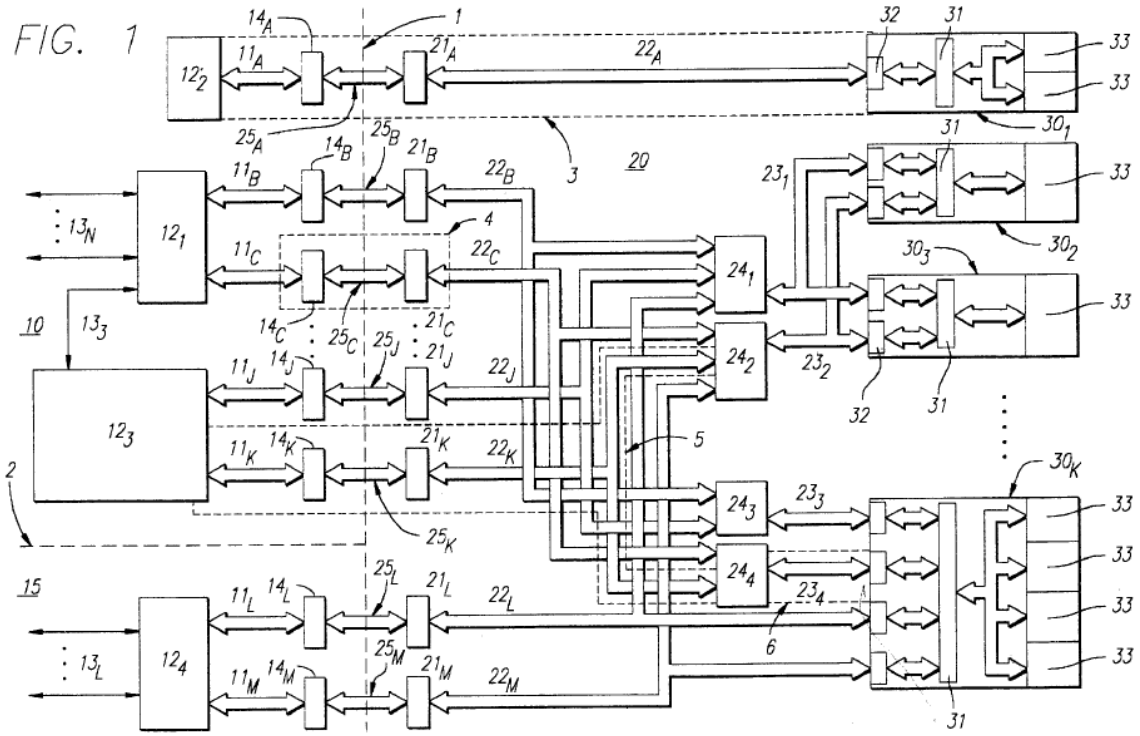


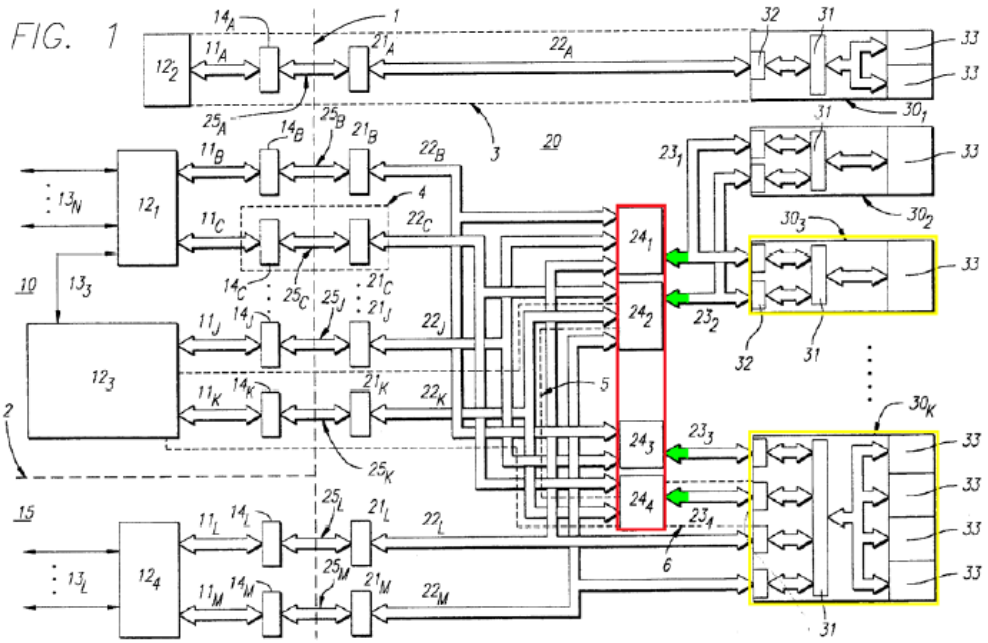
Figure 1 of Roy is a system level block diagram of a multichannel memory architecture disclosed in Roy. *Id.* at 7:59–60. As shown, "memory device 20 further includes multiplexer units $24_{1–4}$ which couple individual ones of a plurality of the channels to one or more of the memory clusters 30." *Id.* at 11:52–54.

3. Analysis

Petitioner contends that, to the extent the claims require "two or more" independent read or write paths to the "volatile memory subsystem" and "non-volatile memory subsystem," a combination of Best and Roy would have rendered obvious claims 1–14 of the '831 patent. Pet. 49–53. We have reviewed the Petition, Patent Owner's Response, and Petitioner's Reply, as well as the relevant evidence discussed in those papers and other record papers, and are persuaded that the record establishes Petitioner's contentions for claims 1–14, and we adopt Petitioner's contentions discussed below as our own.

For example, independent claims 1 and 7 recite "a bi-directional data transfer fabric [having/with] two or more sets of data ports." Petitioner argues that, if this phrase is construed to require two or more independent read/write paths to each of the volatile and non-volatile memory subsystems, such a feature was taught by Roy. Pet. 49–51. In particular, Petitioner relies upon Roy's teaching of multiplexers $24_{1–4}$ ("a bi-directional data transfer fabric"), their interfaces to buses $23_{1–4}$ ("two or more sets of data ports"), some of which are coupled to memory cluster 30_3 ("a first set . . . coupled to") and others of which are coupled to memory cluster 30_K ("a second set . . . coupled to"). Pet. 50–51. Petitioner also annotates Figure 1 of Roy to

indicate multiplexers (red), interfaces (green), and memory clusters to which they are coupled (yellow):



Id. at 50. An annotated version of Figure 1 of Roy is reproduced above.

We are persuaded by Petitioner's showing and find that Roy's multiplexers $24_{1–4}$, buses $23_{1–4,}$ memory cluster 30_3, and memory cluster 30_K teach the recited "bi-directional data transfer fabric."

With respect to why a person of ordinary skill in the art would have modified Best in view of Roy, Petitioner argues:

> One of ordinary skill in the art would have been motivated to implement this architecture for all the reasons Roy describes, including allowing independent and simultaneous transactions, Ex. 1008, 7:37-40, and increased performance by providing a wide effective channel, *id.*, 7:45-49; Ex. 1003, ¶173. Roy also teaches that a multichannel architecture provides substantial flexibility. Ex. 1008, 9:30-42; Ex. 1003, ¶173.
>
> Roy discloses that "nearly identical address and control information" can be applied to each channel such that "[s]ubsequent transfer[s] of data on each of these channels can be synchronized to provide an effectively wider channel." Ex.

> 1008, 10:28-32. This provides particular motivation to combine with Best in light of Best's disclosure that "multiple non-volatile storage dice and/or multiple volatile storage dice may be … selected … based on incoming address and/or control signals." Ex. 1006, ¶15; Ex. 1003, ¶174.
>
> Best suggests such a modification through his disclosure of overlapping and pipelined memory operations. Ex. 1006, ¶18. One of ordinary skill would understand that multiple channels allow for further overlapping or pipelining of operations, such as allowing Best to write data from volatile to non-volatile memory as part of the "Shadow Mode" operation while allowing the host to simultaneously write data to volatile memory, thus improving the operation and responsiveness of the system. Ex. 1003, ¶175.
>
> Modifying Best to use a multichannel architecture such as Roy's would have been an arrangement of old elements (Best's hybrid memory, Roy's multichannel architecture) with each performing the same function it had been known to perform and yielding no more than what one would expect from such an arrangement, *i.e.*, Best's system with a multichannel architecture. Ex. 1003, ¶176. Multichannel architectures were known in the art, and using one in Best would have involved only routine skill to implement the functionality described by Roy. *Id*. Such a modification would have therefore been obvious. *Id.*, ¶¶176, 240.

Pet. 56–53. We determine that Petitioner has provided an articulated reasoning with some rational underpinning that would support the legal conclusion of obviousness. *See KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 418 (2017) (citing *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006)).

Patent Owner relies upon the same argument as for Ground 1—i.e., that Best does not teach a "memory module"—and argues that the Petition fails to show that Roy teaches a "memory module." PO Resp. 45. We are not persuaded by that argument for the reasons discussed above.

Having considered the arguments and evidence, we are persuaded by Petitioner's showing, which we adopt as our own findings and conclusions, that claims 1–14 are unpatentable under 35 U.S.C. § 103(a) as obvious over Best and Roy.

4. Summary

For the foregoing reasons, we are persuaded that Petitioner has established, by a preponderance of the evidence, that claims 1–14 of the '831 patent are unpatentable under 35 U.S.C. § 103(a) as obvious over Best and Roy.

H. Claim 15: Obviousness over Best, Mills, and Bonella, with or without Roy

Petitioner argues that claim 15 is unpatentable under 35 U.S.C. § 103(a) as obvious over Best, Mills, and Bonella, with or without Roy.[12] Pet. 57–69.

1. Bonella Overview

Bonella describes "A memory module including a volatile memory, a non-volatile memory, and a controller that provides address, data, and control interfaces to the memories and to a host system." Ex. 1013, Abstract. Bonella teaches that, "[t]he memory module controller . . . is 'Power State Aware.'" *Id.* ¶ 45. At "Power Level 4," Bonella's controller "reduces power by limiting the DRAM performance and the PCIe transaction performance." *Id.* ¶ 48. Bonella teaches that "[r]eduction of power in the DRAM can be accomplished" by "reduc[ing] the frequency in

[12] Although Petitioner does not include Mills (Ex. 1010) explicitly in its ground (Pet. 3), we include it here because Petitioner's analysis relies upon it (*id.* at 61–64) for teaching part of a limitation.

which the DRAM is operating," which "reduces power and, in general, produces no noticeable decrease in system performance." *Id.* ¶ 49.

2. Petitioner's Initial Contentions

Petitioner contends that claim 15 of the '831 patent is unpatentable as obvious over the combination of Best, Mills, and Bonella, and over the combination of Best, Mills, Roy, and Bonella. Pet. 57–68. We have reviewed the Petition, Patent Owner's Response, and Petitioner's Reply, as well as the relevant evidence discussed in those papers and other record papers, and are persuaded that the record establishes Petitioner's contentions for claim 15, and we adopt Petitioner's contentions discussed below as our own.

i. "first clock frequency"

For example, claim 15 recites

> operating the volatile memory subsystem at a first clock frequency when the memory module is in a first mode of operation in which data is communicated between the volatile memory subsystem and the memory controller;

Ex. 1001, 20:12–15. Petitioner relies upon Best's teaching of a conventional DRAM, which one of ordinary skill in the art would have understood operates at a first clock frequency. Pet. 58–60. We are persuaded by Petitioner's showing and find that a person of ordinary skill in the art would have understood that Best's DRAM operates at a first clock frequency.

ii. "second clock frequency"

Claim 15 further recites

> operating the non-volatile memory subsystem at a second clock frequency when the memory module is in a second mode of operation in which data is communicated between the volatile memory subsystem and the non-volatile memory subsystem;

Ex. 1001, 20:16–20. Petitioner concedes that Best does not explicitly disclose this limitation, but relies upon Mills' teaching of a synchronous flash interface to argue that it would have been obvious to include this functionality in Best. Pet. 61 (citing Ex. 1010). Specifically, Petitioner argues that Mills teaches "a synchronous Flash interface where read and write operations are synchronized to the rising edge of a clock signal provided to the device and operating at a particular frequency." *Id.* at 62. Petitioner also argues that "[a]s combined, Best's Flash interface would conform to Mills' synchronous Flash protocol and include a separate clock signal that controls read and write operations." *Id.* at 63. We are persuaded by Petitioner's showing and find that Mills teaches a synchronous Flash interface operating on a separate clock.

With respect to why a person of ordinary skill in the art would have combined Best and Mills, Petitioner argues

> it would have been obvious to one of ordinary skill in the art to employ a synchronous flash memory, such as disclosed in Mills, in the system of Best because to do so would have been merely an arrangement of old elements with each performing the same function it had been known to perform and yielding no more than what one would expect from such an arrangement, *i.e.*, the non-volatile storage of data. . . .
>
> A skilled artisan would have been motivated to make such a combination because, as Mills explains, a synchronous flash interface "creates an average access time for sequential read accesses that is significantly less than the access time of an asynchronous flash device." Ex. 1010, 17:6-9. In the context of Best, restoring data from the non-volatile flash memory would therefore have been faster by use of a synchronous flash memory, and reduced sequential read access times during other operations or uses of Best's Flash memory, motivating one of ordinary skill

> in the art to use a synchronous interface generally. Ex. 1003, ¶ 299.
>
> [O]ne of ordinary skill in the art would have therefore understood Best to suggest modification to work with any known Flash interface, including Mills' synchronous Flash interface. Ex. 1003, ¶300.

Pet. 62–64. We determine that Petitioner has provided an articulated reasoning with some rational underpinning that would support the legal conclusion of obviousness. *See KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 418 (2017) (citing *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006)).

iii. "third clock frequency"

Finally, claim 15 recites

> operating the volatile memory subsystem at a third clock frequency when the memory module is in the second mode of operation, the third clock frequency being less than the first clock frequency.

Ex. 1001, 20:21–24. Petitioner concedes that Best does not explicitly disclose this limitation, but argues that Bonella teaches reducing DRAM operational frequency to reduce power. Pet. 66–67 (citing Ex. 1013 ¶ 50). The cited portion of Bonella teaches

> An improved power saving option is to slow the operating frequency of the device down and restrict the number of requests being serviced by the ExpressCard interface. By doing this a significant savings in power can be achieved. Voltage can be reduced to the DRAM, frequency is reduced to the DRAM, and the number of cycle requests to the DRAM are reduced making the device function in a very lower power state while maintaining a reasonable system performance level.

Ex. 1013 ¶ 50. We are persuaded by Petitioner's showing and find that Bonella teaches operating DRAM at a reduced frequency (i.e., the recited

"third clock frequency . . . less than the first clock frequency") to conserve power (i.e., in the recited "second mode of operation").

As for why a person of ordinary skill in the art would have modified Best in view of this knowledge, Petitioner states "(1) reducing power during volatile to non-volatile flush operations prompted by a power loss was a well-known technique, and (2) one known way to reduce the power consumption of DRAM devices was to reduce their frequency of operation." Pet. 64–65 (citing Ex. 1011; Ex. 1013). As evidence that reducing power during volatile to non-volatile flush operations was well-known, Petitioner cites U.S. Patent Publication 2006/0212651 A1 (Ex. 1011, "Ashmore"), which "reduc[es] battery power consumption during a main power loss to reduce the likelihood of loss of user write-cached data in a write-caching mass storage controller" and U.S. Patent No. 7,421,552 (Ex. 1012, "Long"), which discloses that "if there is a loss of primary power 34, … provid[ing] a significantly slower clock signal to … the controller 40 while the controller 40 moves data from the volatile-memory storage cache 42 to the flash-based memory vault 44." Pet. 65. As evidence that reducing power consumption of a DRAM by reducing its frequency of operation was well-known, Petitioner cites Bonella, which "explains that one way to reduce the power consumption of the memory module is to slow or reduce the operating frequency of the DRAM." Pet. 66. Petitioner further states that

> One of ordinary skill in the art would have been motivated to reduce the power consumption during Best's write flushing in response to a power loss. A skilled artisan would have been motivated to perform this power reduction technique for all the reasons that were known in the art: e.g., decreasing the risk of data loss due to insufficient backup power (Ex. 1011, ¶7) and enabling the use of a smaller-sized backup power source (Ex.

> 1012, 4:54-64). Reducing power consumption during write flushing in response to a power loss would also have been the arrangement of old elements, each performing the same function it had been known to perform, in a way that yields no more than one of ordinary skill in the art would expect from such an arrangement (reducing power consumption during a power loss event, as suggested by Long and Ashmore). Ex. 1003, ¶307
>
> . . .
>
> One of ordinary skill in the art would also have found it obvious to reduce power consumption during Best's write flushing in response to a power loss using any known or conventional means, and would have also considered power consumption reduction techniques other than those of Ashmore and Long to obtain the same benefits, including those described in Bonella.

Pet. 66–67. On this record, we are persuaded that Petitioner has provided an articulated reasoning with some rational underpinning that would support the legal conclusion of obviousness. *See KSR*, 550 U.S. at 418 (citing *Kahn*, 441 F.3d at 988).

Notwithstanding Patent Owner's arguments, which we have considered and which we address below, we are persuaded by Petitioner's showing, which we adopt as our own findings and conclusions, that claim 15 is unpatentable under 35 U.S.C. § 103(a) as obvious over Best, Mills, and Bonella, and over the combination of Best, Mills, Roy, and Bonella.

3. Patent Owner's Assertions Concerning the References

Patent Owner relies upon the same argument as for Ground 1—i.e., that Best does not teach a "memory module"—and argues that the Petition fails to show that Roy teaches a "memory module." PO Resp. 45. We are not persuaded by that argument for the reasons discussed above.

Patent Owner also argues that claim 15 is not obvious in view of Bonella's Power Level 4. PO Resp. 46–47. Specifically, Patent Owner argues that Bonella does not indicate "what frequency the DRAM is operating at during a power loss" because "there is no suggestion in Bonella about what frequency the DRAM runs at when powered by the UPS battery." *Id.* at 46. Thus, concludes Patent Owner, Petitioner "fails to show evidence that operating in a 'power saving' mode prior to Bonella's 'power loss algorithm' has any effect on the clock frequencies during the 'power loss algorithm.'" *Id.* at 47.

Petitioner counters that it is relying upon Bonella's teaching to reduce power consumption by reducing DRAM operating frequency, not upon Bonella's Power Level 4 as a whole. Pet. Reply 21–22.

We agree with Petitioner. The Petition relies upon Bonella's teaching that reducing the operating frequency of a DRAM reduces power, and argues that a person of ordinary skill in the art would have known how, and been motivated, to apply that teaching to Best to reduce the power consumption of Best's DRAM during a power loss (i.e., in the "second mode of operation" recited in claim 15, when data is flushed from volatile memory subsystem to non-volatile memory subsystem) by operating it at a slower frequency (i.e., the "third clock frequency" recited in claim 15). Pet. 64–68. Although Bonella teaches frequency reduction in the context of Power Level 4, we are persuaded that a person of ordinary skill in the art would have known how to apply that teaching independent of the other aspects of Power Level 4 (e.g., limiting PCIe transaction performance). Pet. Reply 22.

Patent Owner also argues that claim 15 is not obvious in view of Petitioner's cited scenarios. PO Resp. 47–54. Specifically, Patent Owner

characterizes Petitioner's proposed combination as comprising "two scenarios [that] are independent of each other," one in which power is reduced to devices other than the volatile memory subsystem during a power loss, and another in which power is reduced to the volatile memory subsystem during normal operation (i.e., *not* during a power loss). *Id.* at 48. According to Patent Owner, Long teaches away from, and Ashmore does not teach, the "third clock frequency." PO Resp. 49–52.

These arguments are not persuasive because Petitioner relies upon Bonella, not upon Ashmore and Long, for teaching a "third clock frequency." Patent Owner also constructs a hypothetical system based on teachings of Ashmore, Long, and Bonella that is *not* relied upon by Petitioner and concludes that its hypothetical combination "does not reduce the DRAM clock frequency during power loss mode as Petitioner asserts." *Id.* at 52–53. This argument also is not persuasive because Petitioner is relying upon Long and Ashmore as evidence of what a person of ordinary skill in the art would have known and been motivated by (Pet. 65–68), not for teaching the "third clock frequency," much less for collateral teachings about the specific components in Long and Ashmore to which power is reduced during a power loss. Similarly, Petitioner relies upon Bonella's teaching that DRAM power consumption can be reduced by slowing the operating frequency down (Pet. 66–67 (Ex. 1013 ¶¶ 49–50), not upon Bonella's teaching of a power-loss algorithm.

Patent Owner also argues that "Bonella does not teach that power (or frequency) is reduced during a power loss." *Id.* at 56. This argument is misplaced, however, because Petitioner is not relying upon Bonella to show power reducing frequency *during a power loss*. Petitioner is relying upon

Bonella's teaching that DRAM power consumption can be reduced by slowing the operating frequency down (Pet. 66–67 (Ex. 1013 ¶¶ 49–50)), and arguing that "[o]ne of ordinary skill in the art would have been motivated to reduce the power consumption during Best's write flushing in response to a power loss" (*id.* at 66).

Finally, Patent Owner argues a person of ordinary skill in the art would not have been motivated to combine Best with Bonella to "enable[e] the use of a smaller-sized backup power source," as Petitioner contends (Pet. 66), because "[a person of ordinary skill in the art] would know that Petitioner's power reduction will not reduce the required battery capacity or increase the amount of data that can be transferred." PO Resp. 60. Specifically, Patent Owner argues that "reducing the clock frequency . . . reduces power dissipation but simply spreads the task out over time, thereby consuming the same total energy." *Id.* at 61. Thus, according to Patent Owner, "because Petitioner's power reduction technique extends the time required to back up the DRAM, energy requirements are not reduced." *Id.* at 62.

Petitioner counters that Patent Owner's argument "ignores the energy consumption of an idle DRAM as it transfers data to a much-slower Flash memory." Pet. Reply 22. Petitioner highlights Mr. Maltiel's testimony that "the transfer of data between DRAM and FLASH could not occur faster than the speed of the FLASH, which in the case of Best would be substantially slower than the DRAM." Pet. Reply 23 (quoting Ex. 1003 ¶ 312). Patent Owner's declarant, Dr. Baker, testified that "accessing the memory in the big flash array takes considerably longer -- microseconds, as I testified -- than accessing memory in a DRAM, which could take, say, 10 to 50

nanoseconds, for example. So the access portion in a DRAM is considerably faster." Ex. 1020, 15:14–19. Thus, according to Petitioner, reducing the operating frequency of the DRAM does *not* extend the time required to flush the DRAM to the Flash as long as the operating frequency of the DRAM is still faster than that of the Flash. *Id.* at 23–24.

We agree with Petitioner. Patent Owner's argument assumes that the time to flush the DRAM to the Flash is directly proportional to the operating frequency of the DRAM. That process, however, is actually limited by the much slower operating frequency of the Flash memory. Ex. 1003 ¶ 312. We are persuaded by the arguments and evidence that a person of ordinary skill in the art would have known that reducing the operating frequency of the DRAM would enable the use of a smaller-sized backup power source because doing so reduces power consumption without extending the time required to flush the DRAM to the Flash.

4. Summary

For the foregoing reasons, we are persuaded that Petitioner has established, by a preponderance of the evidence, that claim 15 of the '831 patent are unpatentable under 35 U.S.C. § 103(a) as obvious over Best, Mills, and Bonella, and over Best, Mills, Roy, and Bonella.

I. Other Grounds

Because claims 1–14 are unpatentable over Best, with or without Roy, and because claim 15 is unpatentable over Best, Mills, and Bonella, or Best, Mills, Roy, and Bonella, we need not reach Petitioner's other grounds for unpatentability of these claims.

J. Petitioner's Motion to Exclude

Petitioner filed a Motion to Exclude (Paper 17). Patent Owner filed an Opposition (Paper 20, "Opp."), and Petitioner filed a Reply in support of its Motion (Paper 22). As movant, Petitioner has the burden of proof to establish that it is entitled to the requested relief. *See* 37 C.F.R. § 42.20(c).

We decline to assess the merits of Petitioner's Motion to Exclude. Even without excluding the identified evidence, we have concluded that Petitioner has demonstrated, by a preponderance of the evidence, that the challenged claims are unpatentable. Accordingly, Petitioner's Motion to Exclude is dismissed.

III. CONCLUSION

Petitioner has demonstrated, by a preponderance of the evidence, that (1) claims 1–14 of the '831 patent are unpatentable under 35 U.S.C. § 102 as anticipated by Best; (2) claims 1–14 are unpatentable under 35 U.S.C. § 103(a) as obvious over Best; (3) claims 1–14 are unpatentable under 35 U.S.C. § 103(a) as obvious over Best and Roy; and (4) claim 15 is unpatentable over Bowie under 35 U.S.C. § 103(a) as obvious over Best, Mills, and Bonella, with or without Roy.

IV. ORDER

Accordingly, it is

ORDERED that claims 1–15 of the '831 patent are held *unpatentable*;

FURTHER ORDERED that Petitioner's Motion to Exclude is *dismissed*; and

FURTHER ORDERED that, because this is a Final Written Decision, parties to the proceeding seeking judicial review of the decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

For PETITIONER:

Joseph A. Micallef
Samuel A. Dillon
SIDLEY AUSTIN LLP
jmicallef@sidley.com
samuel.dillon@sidley.com

For PATENT OWNER:

Thomas J. Wimbiscus
Christopher C. Winslade
Gregory C. Schodde
Scott P. McBride
Ronald H. Spuhler
Wayne H. Bradley
McANDREWS, HELD & MALLOY, LTD.
twimbiscus@mcandrews-ip.com
cwinslade@mcandrews-ip.com
gschodde@mcandrews-ip.com
smcbride@mcandrews-ip.com
rspuhler@mcandrews-ip.com
wbradley@mcandrews-ip.com