Doc Code: PA..
Document Description: Power of Attorney

PTO/AIA/82B (07-13)
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POWER OF ATTORNEY BY APPLICANT

I hereby revoke all previous powers of attorney given in the application identified in either the attached transmittal letter or the boxes below.

Application Number	Filing Date

(Note: The boxes above may be left blank if information is provided on form PTO/AIA/82A.)

☑ I hereby appoint the Patent Practitioner(s) associated with the following Customer Number as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above: 151145

OR

☐ I hereby appoint Practitioner(s) named in the attached list (form PTO/AIA/82C) as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the patent application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above. (Note: Complete form PTO/AIA/82C.)

Please recognize or change the correspondence address for the application identified in the attached transmittal letter or the boxes above to:

☑ The address associated with the above-mentioned Customer Number

OR

☐ The address associated with Customer Number:

OR

☐ Firm or Individual Name					
Address					
City		State		Zip	
Country					
Telephone		Email			

I am the Applicant (if the Applicant is a juristic entity, list the Applicant name in the box):

Netlist, Inc.

☐ Inventor or Joint Inventor (title not required below)

☐ Legal Representative of a Deceased or Legally Incapacitated Inventor (title not required below)

☑ Assignee or Person to Whom the Inventor is Under an Obligation to Assign (provide signer's title if applicant is a juristic entity)

☐ Person Who Otherwise Shows Sufficient Proprietary Interest (e.g., a petition under 37 CFR 1.46(b)(2) was granted in the application or is concurrently being filed with this document) (provide signer's title if applicant is a juristic entity)

SIGNATURE of Applicant for Patent

The undersigned (whose title is supplied below) is authorized to act on behalf of the applicant (e.g., where the applicant is a juristic entity).

Signature	/s/	Date (Optional)	12/5/12
Name	Nael G. Whitley		
Title	VP, IP & Licensing		

NOTE: Signature - This form must be signed by the applicant in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications. If more than one applicant, use multiple forms.

☐ Total of forms are submitted.

This collection of information is required by 37 CFR 1.131, 1.32, and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76)

Title of Invention	FLASH-DRAM HYBRID MEMORY MODULE

As the below named inventor, I hereby declare that:

This declaration is directed to:

☐ The attached application, or

■ United States application or PCT international application number 14/489269 filed on September 17, 2014.

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

WARNING:

Petitioner/applicant is cautioned to avoid submitting personal information in documents filed in a patent application that may contribute to identity theft. Personal information such as social security numbers, bank account numbers, or credit card numbers (other than a check or credit card authorization form PTO-2038 submitted for payment purposes) is never required by the USPTO to support a petition or an application. If this type of personal information is included in documents submitted to the USPTO, petitioners/applicants should consider redacting such personal information from the documents before submitting them to the USPTO. Petitioner/applicant is advised that the record of a patent application is available to the public after publication of the application (unless a non-publication request in compliance with 37 CFR 1.213(a) is made in the application) or issuance of a patent. Furthermore, the record from an abandoned application may also be available to the public if the application is referenced in a published application or an issued patent (see 37 CFR 1.14). Checks and credit card authorization forms PTO-2038 submitted for payment purposes are not retained in the application file and therefore are not publicly available.

LEGAL NAME OF INVENTOR

Inventor: Jeffrey C. Solomon Date (Optional) :

Signature: Jeffrey C. Solomon

Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form or must have been previously filed. Use an additional PTO/AIA/01 form for each additional inventor.

This collection of information is required by 35 U.S.C. 115 and 37 CFR 1.63. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 1 minute to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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LEGAL NAME OF INVENTOR

Inventor: Scott H. Milton Date (Optional): 10/17/2014

Signature: Scott H. Milton

Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form or must have been previously filed. Use an additional PTO/AIA/01 form for each additional inventor.

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LEGAL NAME OF INVENTOR

Inventor: Hyun Lee Date (Optional) :

Signature:

Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form or must have been previously filed. Use an additional PTO/AIA/01 form for each additional inventor.

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LEGAL NAME OF INVENTOR

Inventor: Jayesh Bhakta Date (Optional): 9-17-2014

Signature: Jayesh Bhakta

Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form or must have been previously filed. Use an additional PTO/AIA/01 form for each additional inventor.

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LEGAL NAME OF INVENTOR

Inventor: Chi-She Chen Date (Optional): Oct-17-2014

Signature: Chi-She Chen

Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form or must have been previously filed. Use an additional PTO/AIA/01 form for each additional inventor.

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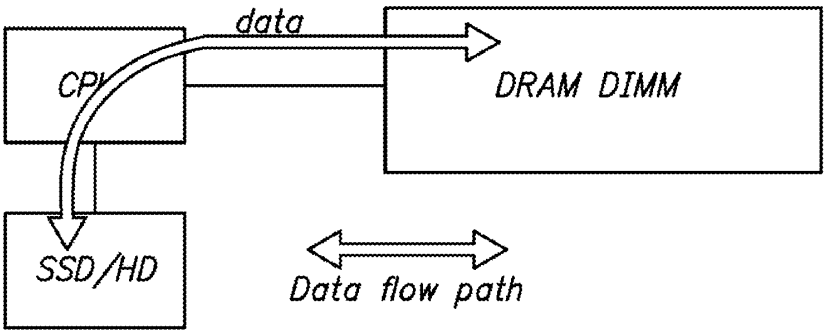


FIG. 1
(PRIOR ART)

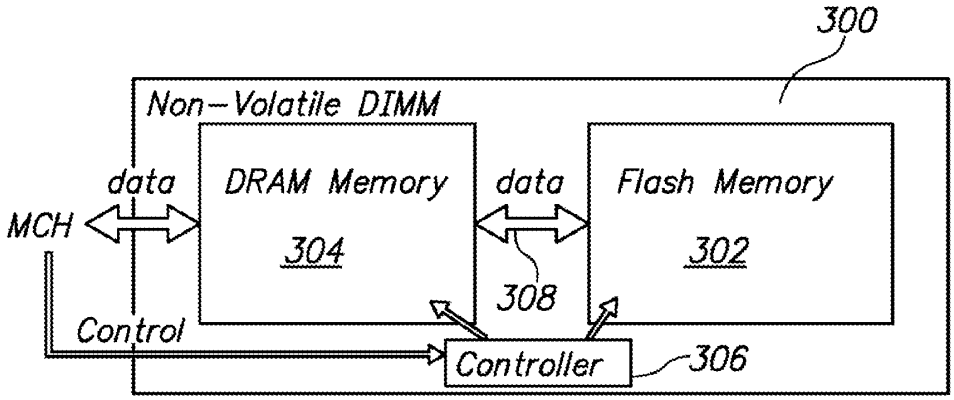
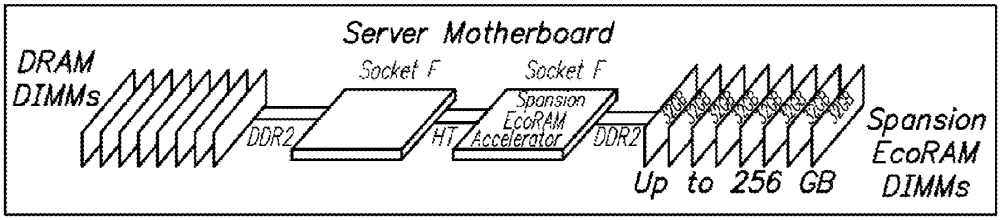


FIG. 3A

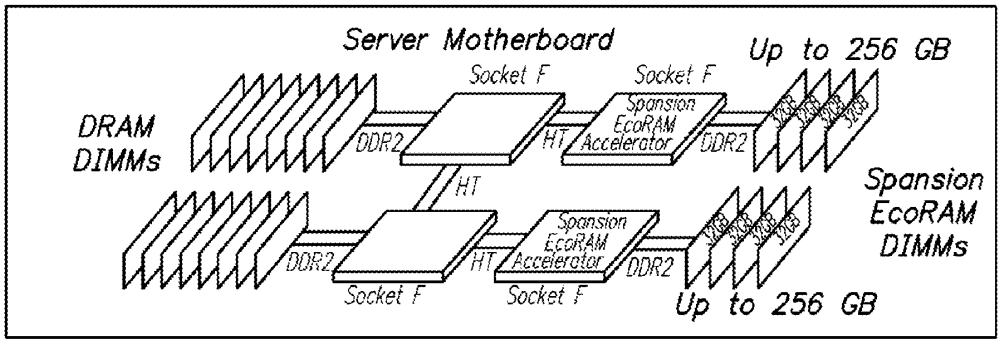
Spansion EcoRAM Configurations

256GB Spansion EcoRAM Solution – Single Accelerator



256GB Single Accelerator Spansion EcoRAM Solution

256GB Spansion EcoRAM Solution – Dual Accelerator



256GB Single Accelerator Spansion EcoRAM Solution

FIG. 2
(PRIOR ART)

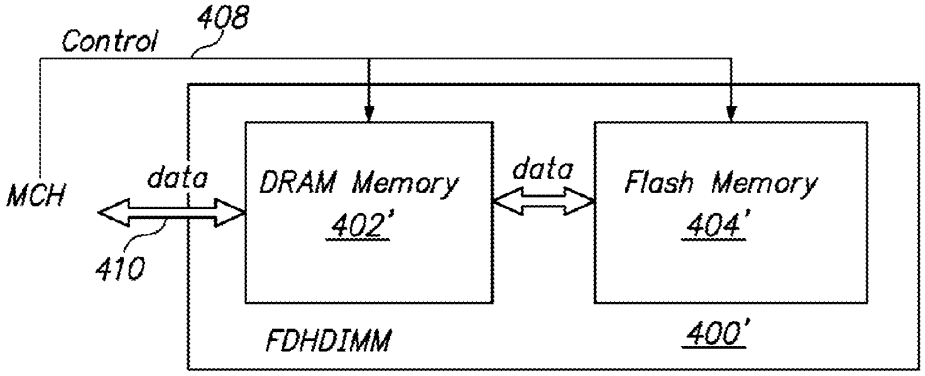


FIG. 4B

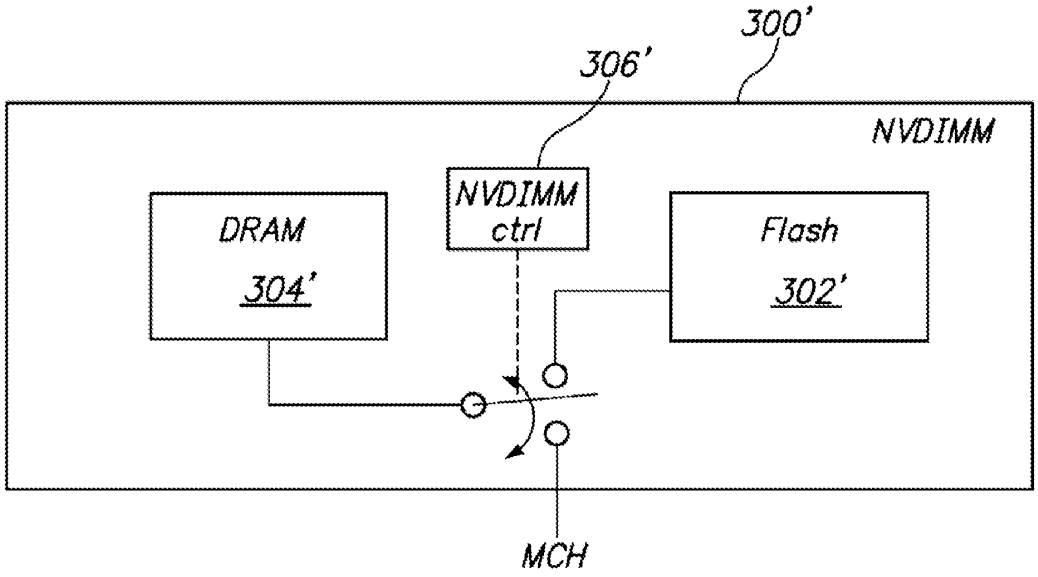

300'
306'
NVDIMM
NVDIMM ctrl
DRAM
304'
Flash
302'
MCH

FIG. 3B

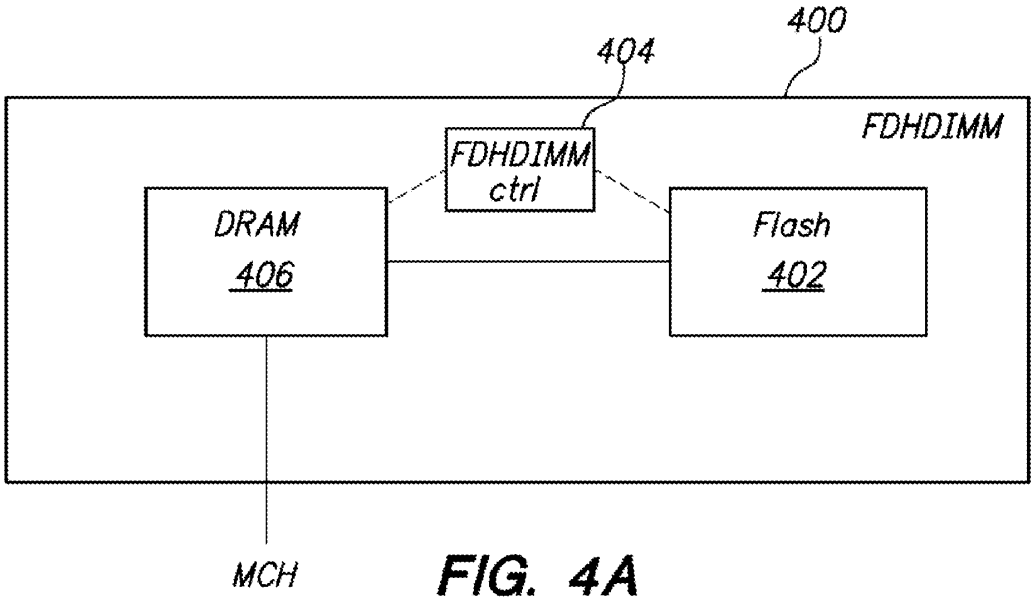

400
404
FDHDIMM
FDHDIMM ctrl
DRAM
406
Flash
402
MCH

FIG. 4A

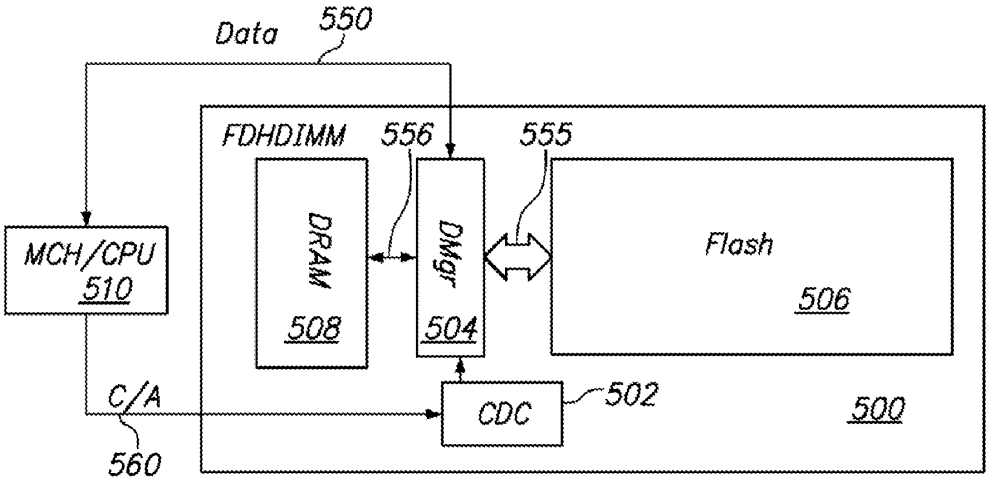

Data
550
FDHDIMM
556
555
DRAM
508
DMgr
504
Flash
506
MCH/CPU
510
C/A
560
CDC
502
500

FIG. 5A

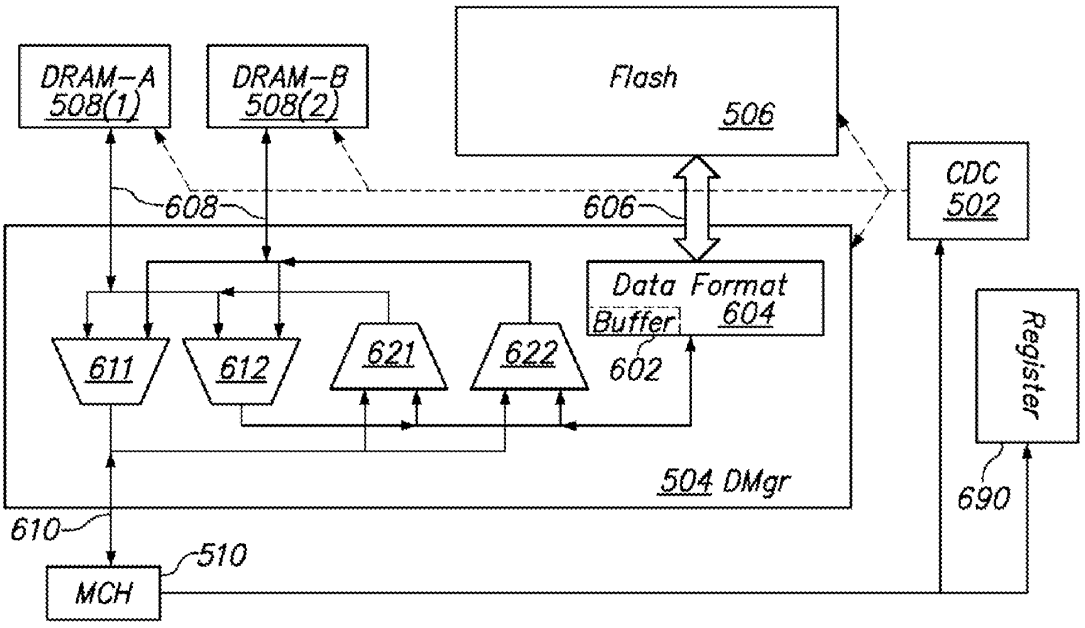

DRAM-A
508(1)
DRAM-B
508(2)
Flash
506
CDC
502
608
606
Data Format
Buffer
604
611
612
621
622
602
Register
690
504 DMgr
610
MCH
510

FIG. 6

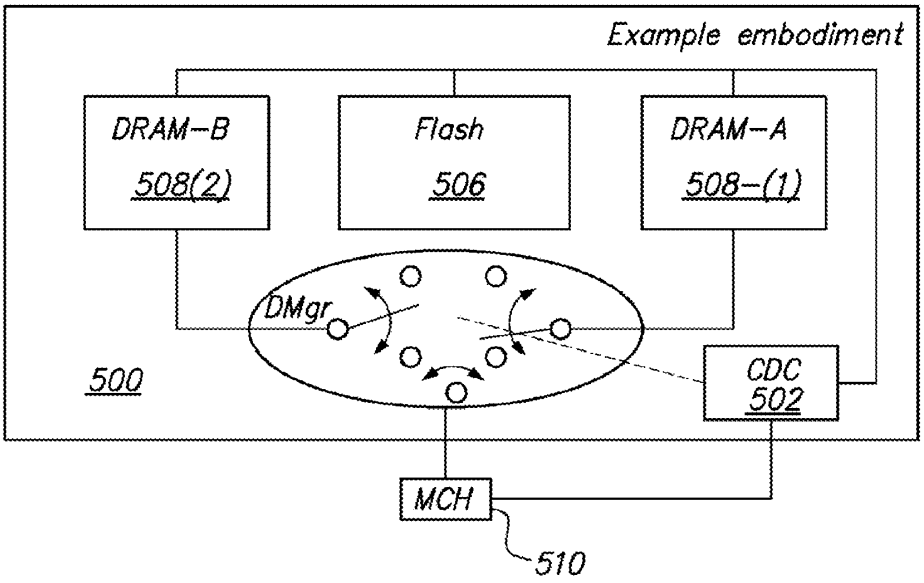

Example embodiment
DRAM–B
508(2)
Flash
506
DRAM–A
508–(1)
DMgr
500
CDC
502
MCH
510

FIG. 5B

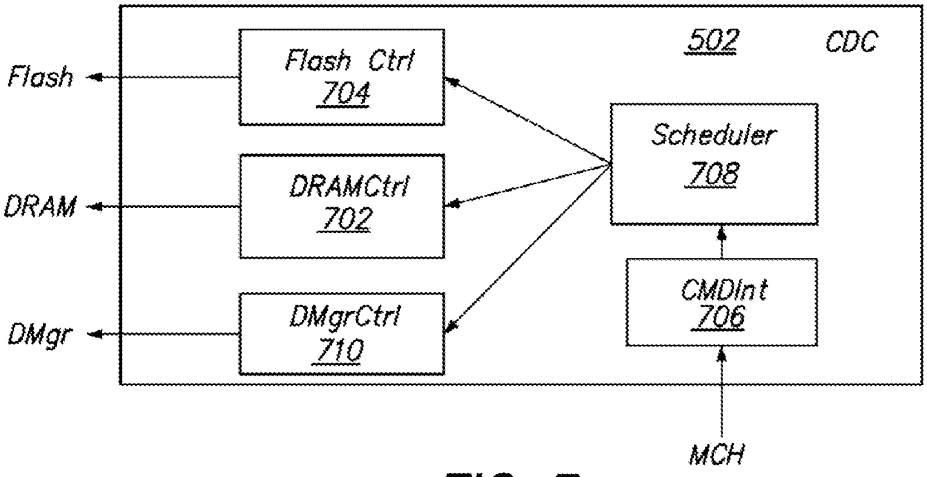

Flash
DRAM
DMgr
Flash Ctrl
704
DRAMCtrl
702
DMgrCtrl
710
502
CDC
Scheduler
708
CMDInt
706
MCH

FIG. 7

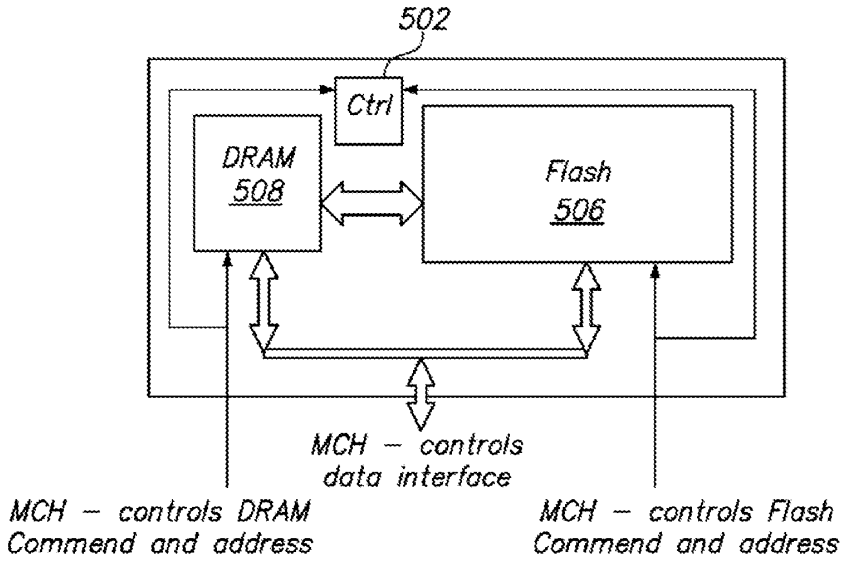

502
Ctrl
DRAM
508
Flash
506
MCH – controls
data interface
MCH – controls DRAM
Commend and address
MCH – controls Flash
Commend and address

FIG. 8A

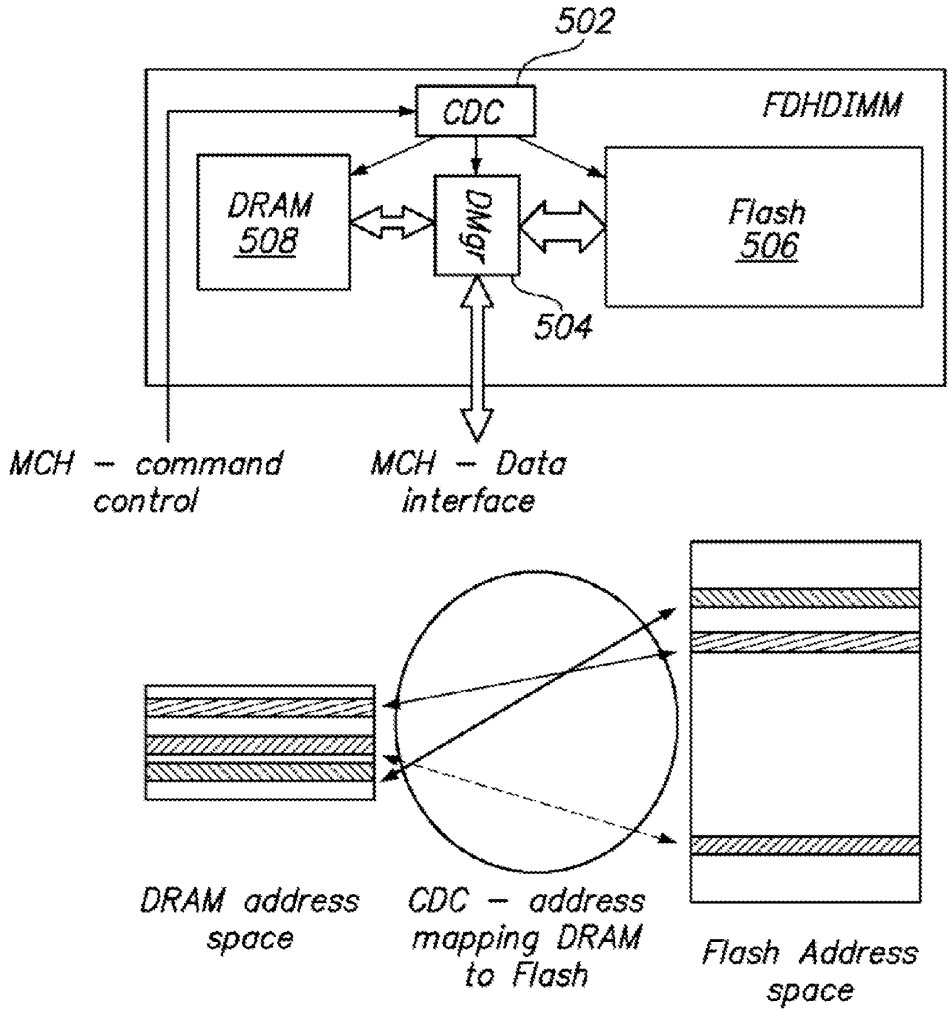

502
CDC
FDHDIMM
DRAM
508
DMgr
Flash
506
504
MCH – command
control
MCH – Data
interface
DRAM address
space
CDC – address
mapping DRAM
to Flash
Flash Address
space

FIG. 8B

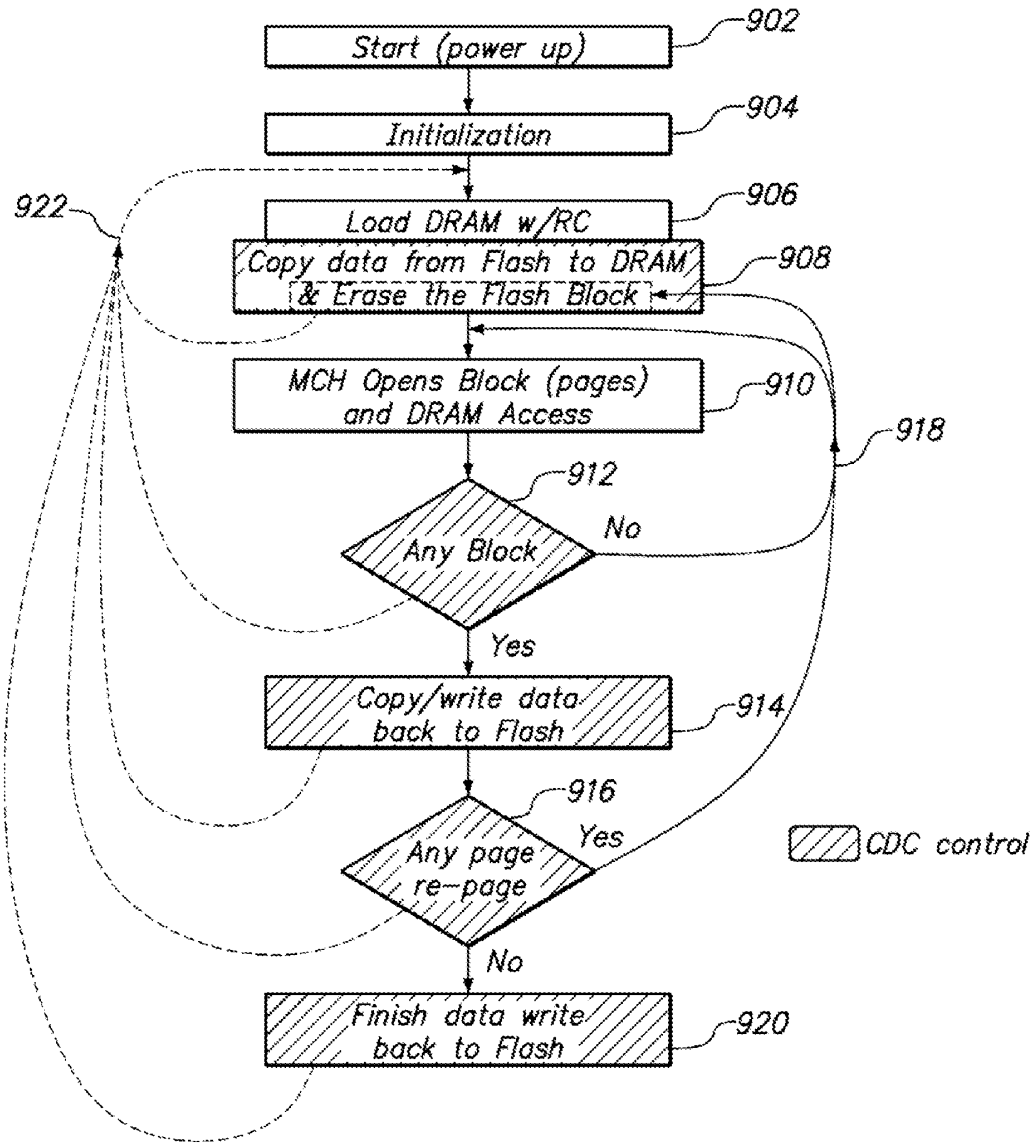

Start (power up)
902
Initialization
904
922
Load DRAM w/RC
906
Copy data from Flash to DRAM & Erase the Flash Block
908
MCH Opens Block (pages) and DRAM Access
910
918
912
Any Block
No
Yes
Copy/write data back to Flash
914
916
Any page re-page
Yes
No
Finish data write back to Flash
920
CDC control

FIG. 9

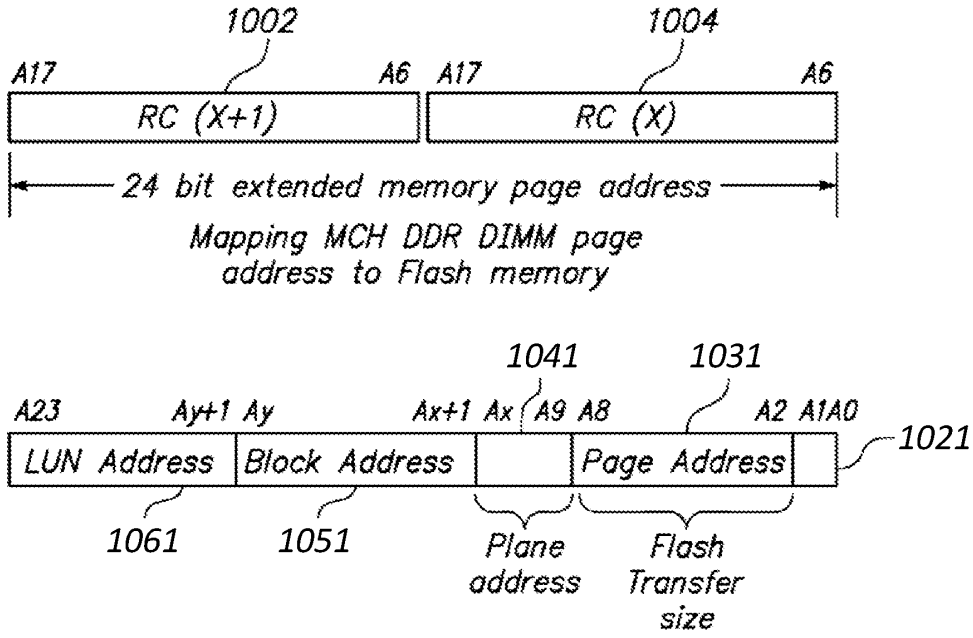

1002
1004
A17
A6
A17
A6
RC (X+1)
RC (X)
24 bit extended memory page address
Mapping MCH DDR DIMM page address to Flash memory
1041
1031
A23
Ay+1
Ay
Ax+1
Ax
A9
A8
A2
A1A0
1021
LUN Address
Block Address
Page Address
1061
1051
Plane address
Flash Transfer size

FIG. 10

DRAM density (GB)	# of blocks per bank	Flash wr-time to rd-time ratio	Avg block use time (sec)	Flash write time (sec)	Max allowed Closed Blk in queue to be written back to Flash
1	250	55	1.00E-03	2.00E-02	0
1	250	55	1.00E-02	2.00E-02	2
1	250	55	2.00E-02	2.00E-02	5
1	250	55	5.00E-02	2.00E-02	11
2	500	55	1.00E-03	2.00E-02	0
2	500	55	1.00E-02	2.00E-02	5
2	500	55	2.00E-02	2.00E-02	9
2	500	55	5.00E-02	2.00E-02	23
4	1000	55	1.00E-03	2.00E-02	1
4	1000	55	1.00E-02	2.00E-02	9
4	1000	55	2.00E-02	2.00E-02	18
4	1000	55	5.00E-02	2.00E-02	45

FIG. 11

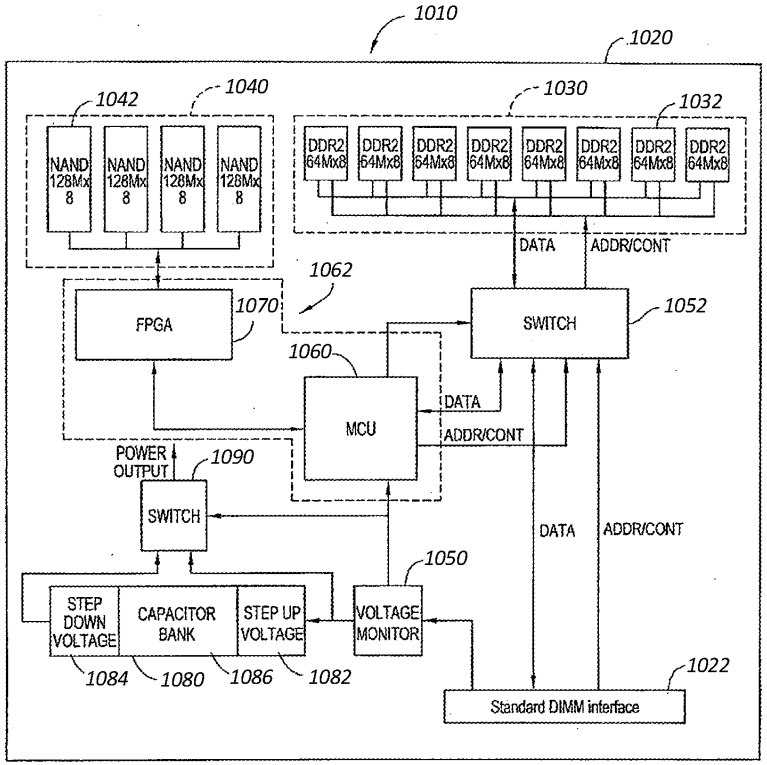

1010
1020
1042
1040
1030
1032
NAND 128Mx 8
NAND 128Mx 8
NAND 128Mx 8
NAND 128Mx 8
DDR2 64Mx8
DDR2 64Mx8
DDR2 64Mx8
DDR2 64Mx8
DDR2 64Mx8
DDR2 64Mx8
DDR2 64Mx8
DDR2 64Mx8
DATA
ADDR/CONT
1062
FPGA
1070
SWITCH
1052
1060
MCU
DATA
ADDR/CONT
POWER OUTPUT
1090
SWITCH
DATA
ADDR/CONT
1050
STEP DOWN VOLTAGE
CAPACITOR BANK
STEP UP VOLTAGE
VOLTAGE MONITOR
1084
1080
1086
1082
1022
Standard DIMM interface

FIG. 12

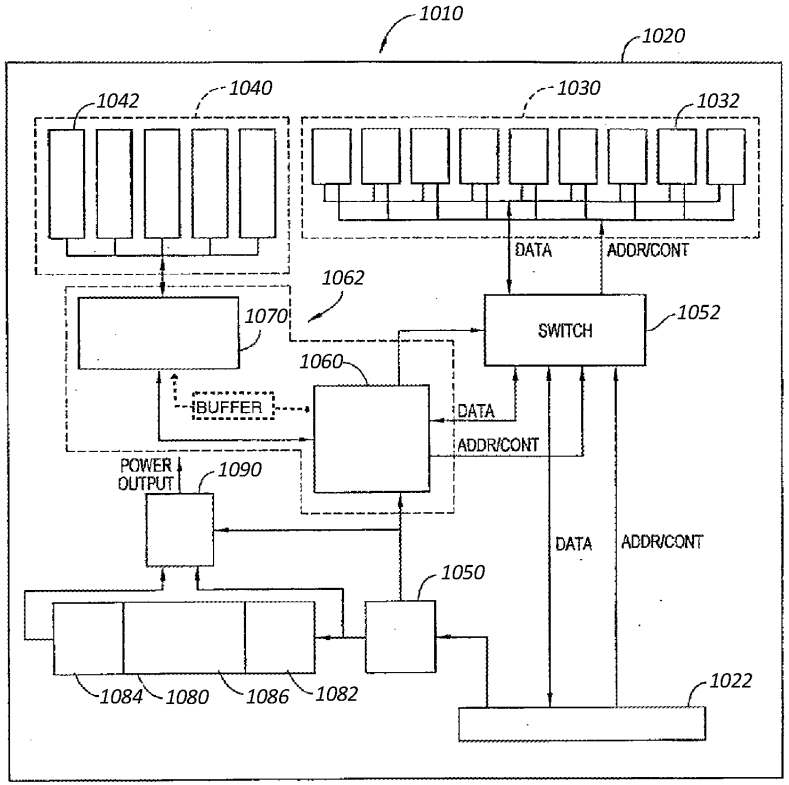

1010
1020
1042
1040
1030
1032
DATA
ADDR/CONT
1062
1070
SWITCH
1052
1060
BUFFER
DATA
ADDR/CONT
POWER OUTPUT
1090
DATA
ADDR/CONT
1050
1084
1080
1086
1082
1022

FIG. 13

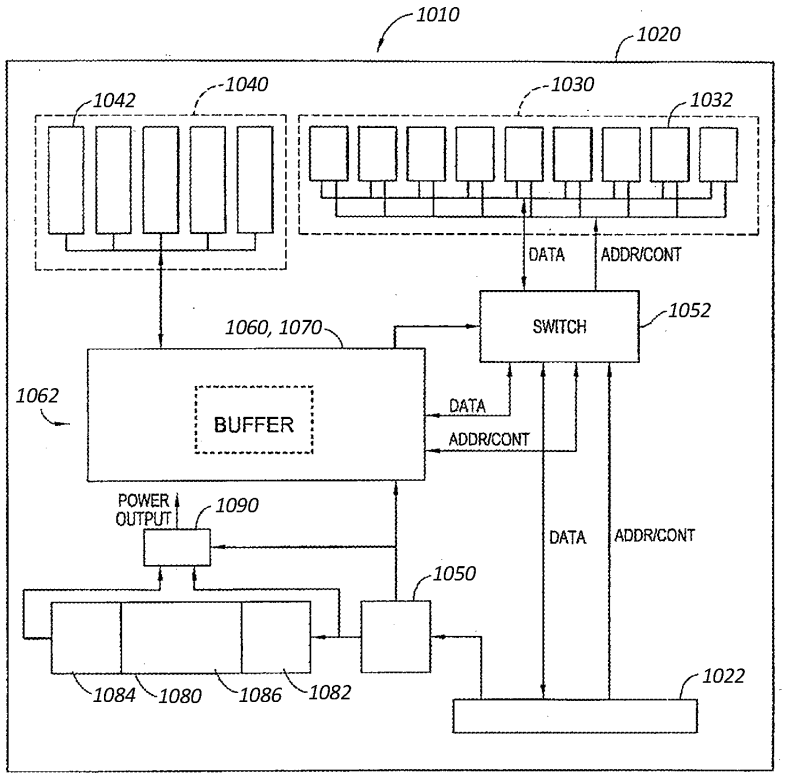

1010
1020
1042
1040
1030
1032
DATA
ADDR/CONT
SWITCH
1052
1060, 1070
1062
BUFFER
DATA
ADDR/CONT
POWER OUTPUT
1090
DATA
ADDR/CONT
1050
1084
1080
1086
1082
1022

FIG. 14

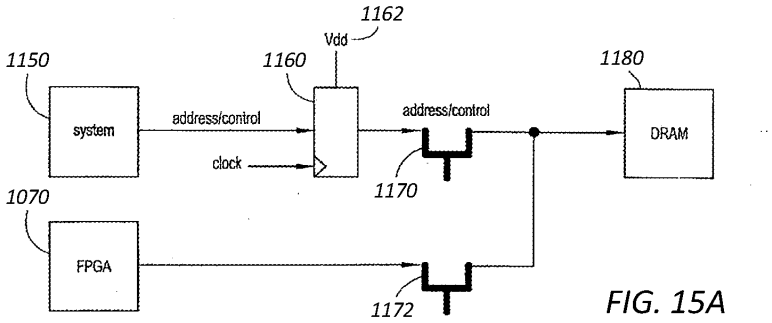


FIG. 15A

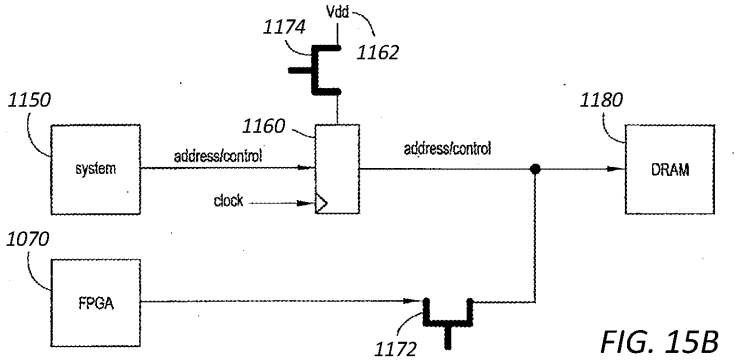


FIG. 15B

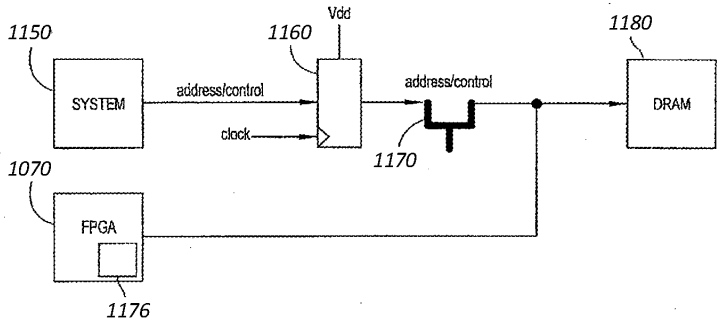

1150
SYSTEM
address/control
clock
1160
Vdd
address/control
1170
1180
DRAM
1070
FPGA
1176

FIG. 15C

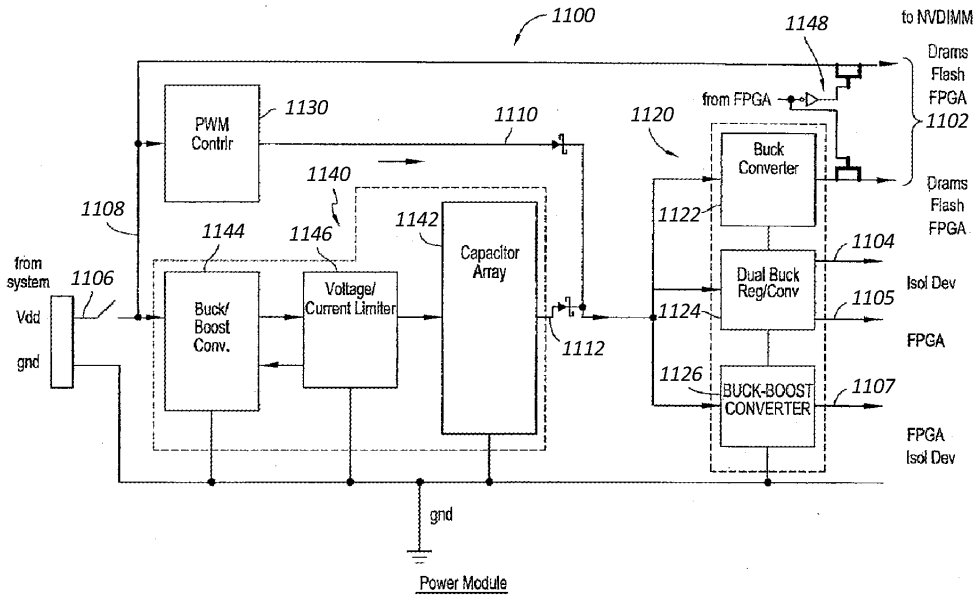

1100
1148
to NVDIMM
Drams
Flash
FPGA
1102
from FPGA
PWM
Contrlr
1130
1110
1120
Buck
Converter
1140
1108
1144
1146
1142
Capacitor
Array
1122
Drams
Flash
FPGA
1104
from
system
1106
Vdd
gnd
Buck/
Boost
Conv.
Voltage/
Current Limiter
Dual Buck
Reg/Conv
Isol Dev
1105
1124
1112
FPGA
1126
BUCK-BOOST
CONVERTER
1107
FPGA
Isol Dev
gnd
Power Module

FIG. 16

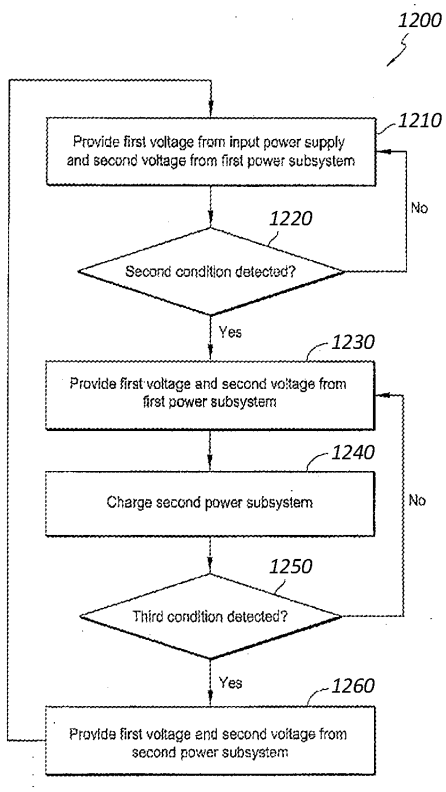

1200
1210
Provide first voltage from input power supply and second voltage from first power subsystem
No
1220
Second condition detected?
Yes
1230
Provide first voltage and second voltage from first power subsystem
1240
Charge second power subsystem
No
1250
Third condition detected?
Yes
1260
Provide first voltage and second voltage from second power subsystem

FIG. 17

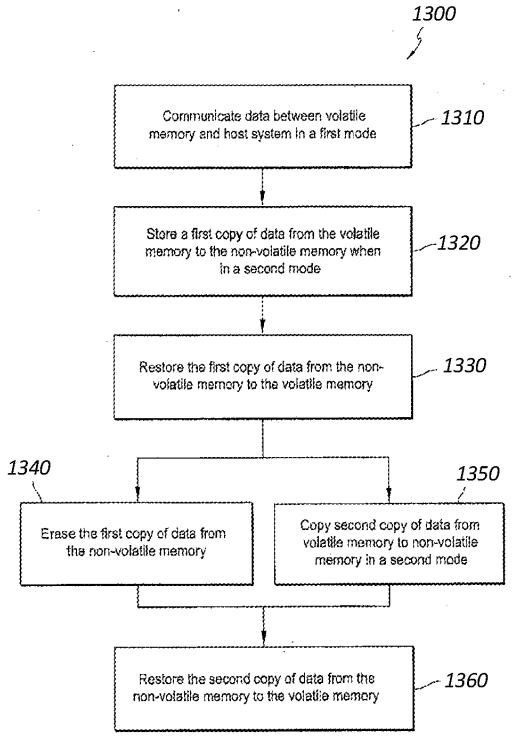

1300
Communicate data between volatile memory and host system in a first mode
1310
Store a first copy of data from the volatile memory to the non-volatile memory when in a second mode
1320
Restore the first copy of data from the non-volatile memory to the volatile memory
1330
1340
Erase the first copy of data from the non-volatile memory
1350
Copy second copy of data from volatile memory to non-volatile memory in a second mode
Restore the second copy of data from the non-volatile memory to the volatile memory
1360

FIG. 18

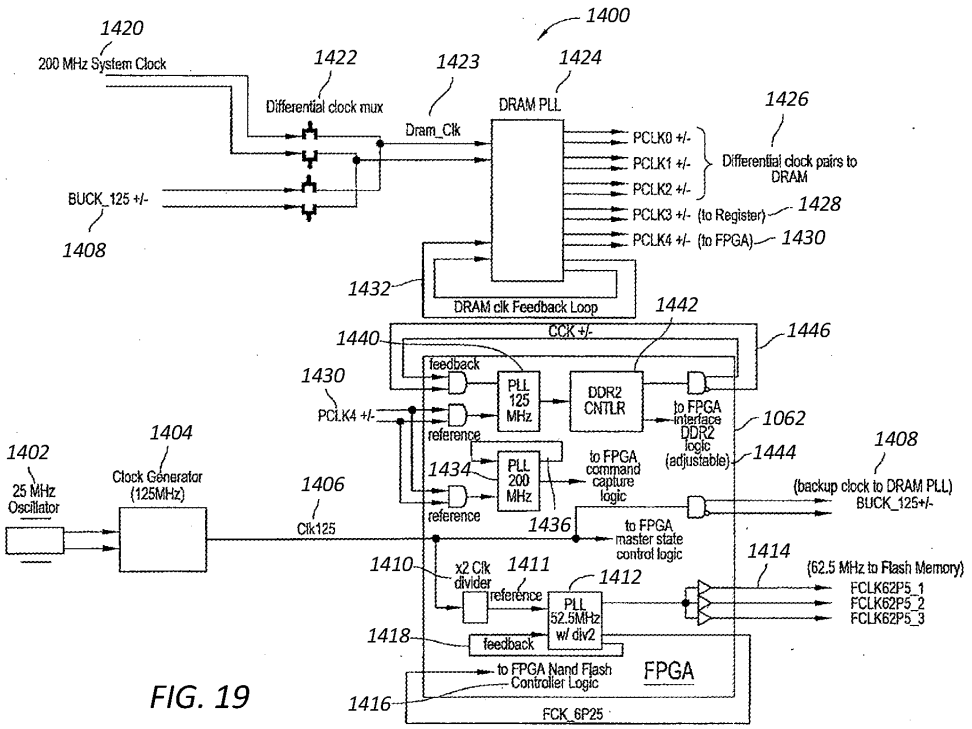

1400
1420
200 MHz System Clock
1422
Differential clock mux
1423
Dram_Clk
1424
DRAM PLL
1426
PCLK0 +/-
PCLK1 +/-
PCLK2 +/-
Differential clock pairs to DRAM
PCLK3 +/- (to Register)
1428
PCLK4 +/- (to FPGA)
1430
BUCK_125 +/-
1408
1432
DRAM clk Feedback Loop
1442
CCK +/-
1446
1440
feedback
1430
PCLK4 +/-
reference
PLL 125 MHz
DDR2 CNTLR
to FPGA interface DDR2 logic (adjustable)
1062
1444
1408
1434
PLL 200 MHz
to FPGA command capture logic
(backup clock to DRAM PLL) BUCK_125+/-
1402
25 MHz Oscillator
1404
Clock Generator (125MHz)
1406
Clk125
1436
to FPGA master state control logic
1414
(62.5 MHz to Flash Memory)
1410
x2 Clk divider
1411
reference
1412
PLL 52.5MHz w/ div2
FCLK62P5_1
FCLK62P5_2
FCLK62P5_3
1418
feedback
to FPGA Nand Flash Controller Logic
FPGA
1416
FCK_6P25

FIG. 19

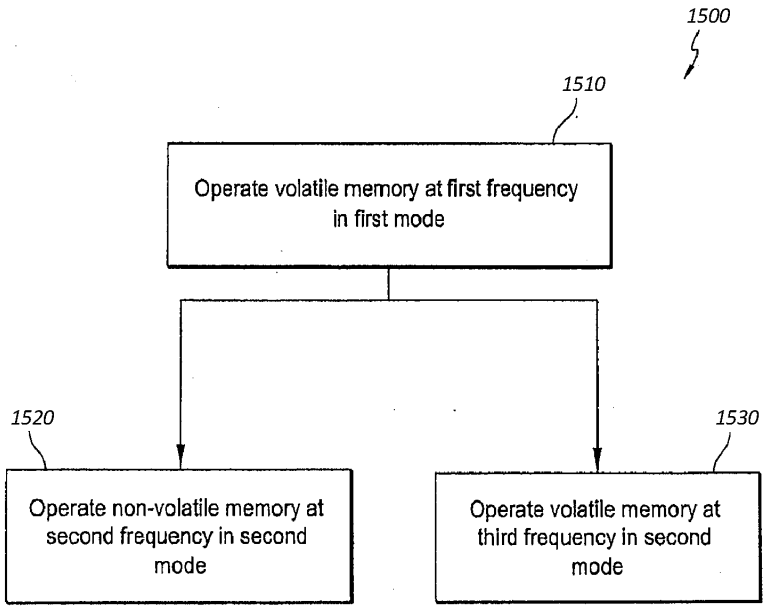

1500
1510
Operate volatile memory at first frequency in first mode
1520
Operate non-volatile memory at second frequency in second mode
1530
Operate volatile memory at third frequency in second mode

FIG. 20

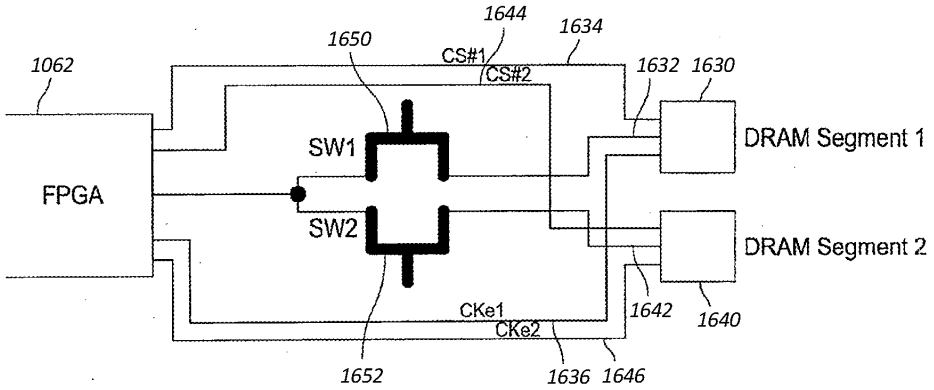

1644
1650
1634
1062
CS#1
CS#2
1632
1630
SW1
DRAM Segment 1
FPGA
SW2
DRAM Segment 2
CKe1
1642
1640
CKe2
1652
1636
1646

FIG. 21

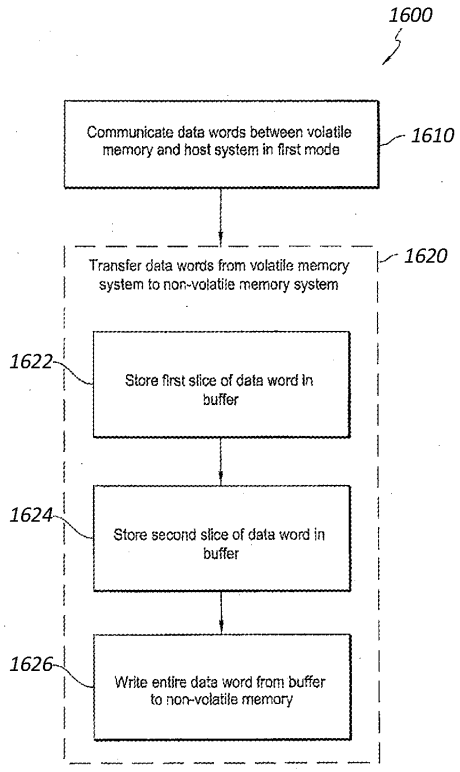

1600
Communicate data words between volatile memory and host system in first mode
1610
Transfer data words from volatile memory system to non-volatile memory system
1620
1622
Store first slice of data word in buffer
1624
Store second slice of data word in buffer
1626
Write entire data word from buffer to non-volatile memory

FIG. 22

FLASH-DRAM HYBRID MEMORY MODULE

PRIORITY CLAIM

[0001] This application is a continuation of U.S. Patent Application No. 15/934,416, filed March 23, 2018, titled "Flash-Dram Hybrid Memory Module," which is a continuation of U.S. Patent Application No. 14/840,865, filed August 31, 2015, titled "Flash-Dram Hybrid Memory Module," now U.S. Patent No. 9,928,186, which is a continuation of U.S. Patent Application No. 14/489,269, filed September 17, 2014, titled "Flash-Dram Hybrid Memory Module," now U.S. Patent No. 9,158,684, which is a continuation of U.S. Patent Application No. 13/559,476, filed July 26, 2012, titled "Flash-Dram Hybrid Memory Module," now U.S. Patent No. 8,874,831, which claims the benefit of U. S. Provisional Patent Application No. 61/512,871, filed July 28, 2011, and is a continuation-in-part of U.S. Patent Application No. 12/240,916, filed September 29, 2008, titled "Non-Volatile Memory Module," now U.S. Patent No. 8,301,833, which is a continuation of U.S. Patent Application No. 12/131,873, filed June 2, 2008, which claims the benefit of U. S. Provisional Patent Application No. 60/941,586, filed June 1, 2007, the contents of all of which are incorporated herein by reference in their entirety.

[0002] This application may be considered related to U.S. Patent Application No. 14/173,242, titled "Isolation Switching For Backup Of Registered Memory," filed February 5, 2014, which is a continuation of U.S. Patent Application 13/905,053, titled "Isolation Switching For Backup Of Registered Memory," filed May 29, 2013, now U.S. Patent 8,677,060, issued March 18, 2014, which is a continuation of U.S. Patent Application 13/536,173, titled "Data Transfer Scheme For Non-Volatile Memory Module," filed June 28, 2012, now U.S. Patent

8,516,187, issued August 20, 2013, which is a divisional of U.S. Patent Application 12/240,916, titled "Non-Volatile Memory Module," filed September 29, 2008, now U.S. Patent No. 8,301,833, issued October 30, 2012, which is a continuation of U.S. Patent Application No. 12/131,873, filed June 2, 2008, now abandoned, which claims the benefit of U.S. Provisional Application No. 60/941,586, filed June 1, 2007, the contents of which are incorporated by reference herein in their entirety.

[0003] This application may also be considered related to U.S. Patent Application No. 15/000,834, filed January 19, 2016 (abandoned), which is a continuation of U.S. Patent Application No. 14/489,332, filed September 17, 2014, now U.S. Patent No. 9,269,437, which is a continuation of U.S. Patent Application No. 14/173,219, filed February 5, 2014, now U.S. Patent No. 8,904,099, which is a continuation of U.S. Patent Application No. 13/905,048, filed May 29, 2013, now U.S. Patent No. 6,671,243, which is a continuation U.S. Patent Application 13/536,173 above.

[0004] This application may also be considered related to U.S. Patent Application No. 15/924,866, (abandoned), which is a continuation of U.S. Patent Application No. 14/489,281, filed September 17, 2014, now U.S. Patent No. 9,921,762, which is a continuation of U.S. Patent Application No. 13/625,563, filed September 24, 2012, now U.S. Patent No. 8,904,098, which claims the benefit of U.S. Provisional Application No. 61/583,775, filed September 23, 2011.

TECHNICAL FIELD

[0005] The present disclosure relates generally to computer memory devices, and more particularly, to devices that employ different types of memory devices such as combinations of Flash and random access memories.

BACKGROUND

[0006] As technology advances and the usage of portable computing devices, such as tablet notebook computers, increases, more data needs to be transferred among data centers and to/from end users. In many cases, data centers are built by clustering multiple servers that are networked to increase performance.

[0007] Although there are many types of networked servers that are specific to the types applications envisioned, the basic concept is generally to increase server performance by dynamically allocating computing and storage resources. In recent years, server technology has evolved to be specific to particular applications such as 'finance transactions' (for example, point-of-service, inter-bank transaction, stock market transaction), 'scientific computation' (for example, fluid dynamic for automobile and ship design, weather prediction, oil and gas expeditions), 'medical diagnostics' (for example, diagnostics based on the fuzzy logic, medical data processing), 'simple information sharing and searching' (for example, web search, retail store website, company home page), 'email' (information distribution and archive), 'security service', 'entertainment' (for example, video-on-demand), and so on. However, all of these applications suffer from the same information transfer bottleneck due to the inability of a high

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speed CPU (central processing unit) to efficiently transfer data in and out of relatively slower speed storage or memory subsystems, particularly since data transfers typically pass through the CPU input/output (I/O) channels.

[0008] The data transfer limitations by the CPU are exemplified by the arrangement shown in FIG. 1, and apply to data transfers between main storage (for example the hard disk (HD) or solid state drive (SSD) and the memory subsystems (for example DRAM DIMM (Dynamic Random Access Memory Dual In-line Memory Module) connected to the front side bus (FSB)). In arrangements such as that of FIG. 1, the SSD/HD and DRAM DIMM of a conventional memory arrangement are connected to the CPU via separate memory control ports (not shown). FIG. 1 specifically shows, through the double-headed arrow, the data flow path between the computer or server main storage (SSD/HD) to the DRAM DIMMs. Since the SSD/HD data I/O and the DRAM DIMM data I/O are controlled by the CPU, the CPU needs to allocate its process cycles to control these I/Os, which may include the IRQ (Interrupt Request) service which the CPU performs periodically. As will be appreciated, the more time a CPU allocates to controlling the data transfer traffic, the less time the CPU has to perform other tasks. Therefore, the overall performance of a server will deteriorate with the increased amount of time the CPU has to expend in performing data transfer.

[0009] There have been various approaches to increase the data transfer throughput rates from/to the main storage, such as SSD/HD, to local storage, such as DRAM DIMM. In one example as illustrated in FIG. 2, EcoRAM™ developed by Spansion provides a storage SSD based system that assumes a physical form factor of a DIMM . The EcoRAM™ is populated with Flash memories and a relatively small memory capacity using DRAMs which serve as a

data buffer. This arrangement is capable of delivering higher throughput rate than a standard SSD based system since the EcoRAM™ is connected to the CPU (central processing unit) via a high speed interface, such as the HT (Hyper Transport) interface, while an SSD/HD is typically connected via SATA (serial AT attachment), USB (universal serial bus), or PCI Express (peripheral component interface express). For example, the read random access throughput rate of EcoRAM™ is near 3GB/s compared with 400MB/s for a NAND SSD memory subsystem using the standard PCI Express-based. This is a 7.5X performance improvement. However, the performance improvement for write random access throughput rate is less than 2X (197MBs for the EcoRAM vs. 104MBs for NAND SSD). This is mainly due to the fact that the write speed is cannot be faster than the NAND Flash write access time. Figure 2 is an example of EcoRAM™ using SSD with the form factor of a standard DIMM such that it can be connected to the FSB (front side bus). However, due to the interface protocol difference between DRAM and Flash, an interface device, EcoRAM Accelerator™), which occupies one of the server's CPU sockets is used, and hence further reducing server's performance by reducing the number of available CPU sockets available, and in turn reducing the overall computation efficiency. The server's performance will further suffer due to the limited utilization of the CPU bus due to the large difference in the data transfer throughput rate between read and write operations.

[0010] The EcoRAM™ architecture enables the CPU to view the Flash DIMM controller chip as another processor with a large size of memory available for CPU access.

[0011] In general, the access speed of a Flash based system is limited by four items: the read/write speed of the Flash memory, the CPU's FSB bus speed and efficiency, the Flash

DIMM controller's inherent latency, and the HT interconnect speed and efficiency which is dependent on the HT interface controller in the CPU and Flash DIMM controller chip.

[0012] The published results indicate that these shortcomings are evident in that the maximum throughput rate is 1.56 GBs for the read operation and 104 MBs for the write operation. These access rates are 25% of the DRAM read access speed, and 1.7% of the DRAM access speed at 400MHz operation. The disparity in the access speed (15 to 1) between the read operation and write operation highlight a major disadvantage of this architecture. The discrepancy of the access speed between this type of architecture and JEDEC standard DRAM DIMM is expected to grow wider as the DRAM memory technology advances much faster than the Flash memory.

[0013] Certain types of memory modules comprise a plurality of dynamic random-access memory (DRAM) devices mounted on a printed circuit board (PCB). These memory modules are typically mounted in a memory slot or socket of a computer system (e.g., a server system or a personal computer) and are accessed by the computer system to provide volatile memory to the computer system.

[0014] Volatile memory generally maintains stored information only when it is powered. Batteries have been used to provide power to volatile memory during power failures or interruptions. However, batteries may require maintenance, may need to be replaced, are not environmentally friendly, and the status of batteries can be difficult to monitor.

[0015] Non-volatile memory can generally maintain stored information while power is not applied to the non-volatile memory. In certain circumstances, it can therefore be useful to backup volatile memory using non-volatile memory.

OVERVIEW

[0016] Described herein is a memory module couplable to a memory controller of a host system. The memory module includes a non-volatile memory subsystem, a data manager coupled to the non-volatile memory subsystem, a volatile memory subsystem coupled to the data manager and operable to exchange data with the non-volatile memory subsystem by way of the data manager, and a controller operable to receive commands from the memory controller and to direct (i) operation of the non-volatile memory subsystem, (ii) operation of the volatile memory subsystem, and (iii) transfer of data between any two or more of the memory controller, the volatile memory subsystem, and the non-volatile memory subsystem based on at least one received command from the memory controller.

[0017] Also described herein is a method for managing a memory module by a memory controller, the memory module including volatile and non-volatile memory subsystems. The method includes receiving control information from the memory controller, wherein the control information is received using a protocol of the volatile memory subsystem. The method further includes identifying a data path to be used for transferring data to or from the memory module using the received control information, and using a data manager and a controller of the memory module to transfer data between any two or more of the memory controller, the volatile memory

subsystem, and the non-volatile memory subsystem based on at least one of the received control information and the identified data path.

[0018] Also described herein is a memory module wherein the data manager is operable to control one or more of data flow rate, data transfer size, data buffer size, data error monitoring, and data error correction in response to receiving at least one of a control signal and control information from the controller.

[0019] Also described herein is a memory module wherein the data manager controls data traffic between any two or more of the memory controller, the volatile memory subsystem, and the non-volatile memory subsystem based on instructions received from the controller.

[0020] Also described herein is a memory module wherein data traffic control relates to any one or more of data flow rate, data transfer size, data buffer size, data transfer bit width, formatting information, direction of data flow, and the starting time of data transfer.

[0021] Also described herein is a memory module wherein the controller configures at least one of a first memory address space of the volatile memory subsystem and a second memory address space of the non-volatile memory subsystem in response to at least one of a received command from the memory controller and memory address space initialization information of the memory module.

[0022] Also described herein is a memory module wherein the data manager is configured as a bi-directional data transfer fabric having two or more sets of data ports coupled to any one of the volatile and non-volatile memory subsystems.

[0023] Also described herein is a memory module wherein at least one of the volatile and non-volatile memory subsystems comprises one or more memory segments.

[0024] Also described herein is a memory module wherein each memory segment comprises at least one memory circuit, memory device, or memory die.

[0025] Also described herein is a memory module wherein the volatile memory subsystem comprises DRAM memory.

[0026] Also described herein is a memory module wherein the non-volatile memory subsystem comprises flash memory.

[0027] Also described herein is a memory module wherein at least one set of data ports is operated by the data manager to independently and/or concurrently transfer data to or from one or more memory segments of the volatile or non-volatile memory subsystems.

[0028] Also described herein is a memory module wherein the data manager and controller are configured to effect data transfer between the memory controller and the non-volatile memory subsystem in response to memory access commands received by the controller from the memory controller.

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[0029] Also described herein is a memory module wherein the volatile memory subsystem is operable as a buffer for the data transfer between the memory controller and non-volatile memory.

[0030] Also described herein is a memory module wherein the data manager further includes a data format module configured to format data to be transferred between any two or more of the memory controller, the volatile memory subsystem, and the non-volatile memory subsystem based on control information received from the controller.

[0031] Also described herein is a memory module wherein the data manager further includes a data buffer for buffering data delivered to or from the non-volatile memory subsystem.

[0032] Also described herein is a memory module wherein the controller is operable to perform one or more of memory address translation, memory address mapping, address domain conversion, memory access control, data error correction, and data width modulation between the volatile and non-volatile memory subsystems.

[0033] Also described herein is a memory module wherein the controller is configured to effect operation with the host system in accordance with a prescribed protocol.

[0034] Also described herein is a memory module wherein the prescribed protocol is selected from one or more of DDR, DDR2, DDR3, and DDR4 protocols.

[0035] Also described herein is a memory module wherein the controller is operable to configure memory space in the memory module based on at least one of a command received from the memory controller, a programmable value written into a register, a value corresponding to a first portion of the volatile memory subsystem, a value corresponding to a first portion of the non-volatile memory subsystem, and a timing value.

[0036] Also described herein is a memory module wherein the controller configures the memory space of the memory module using at least a first portion of the volatile memory subsystem and a first portion of the non-volatile memory subsystem, and the controller presents a unified memory space to the memory controller.

[0037] Also described herein is a memory module wherein the controller configures the memory space in the memory module using partitioning instructions that are application-specific.

[0038] Also described herein is a memory module wherein the controller is operable to copy booting information from the non-volatile to the volatile memory subsystem during power up.

[0039] Also described herein is a memory module wherein the controller includes a volatile memory control module, a non-volatile memory control module, data manager control module, a command interpreter module, and a scheduler module.

[0040] Also described herein is a memory module wherein commands from the volatile memory control module to the volatile memory subsystem are subordinated to commands from the memory controller to the controller.

[0041] Also described herein is a memory module wherein the controller effects pre-fetching of data from the non-volatile to the volatile memory.

[0042] Also described herein is a memory module wherein the pre-fetching is initiated by the memory controller writing an address of requested data into a register of the controller.

[0043] Also described herein is a memory module wherein the controller is operable to initiate a copy operation of data of a closed block in the volatile memory subsystem to a target block in the non-volatile memory subsystem.

[0044] Also described herein is a memory module wherein, if the closed block is re-opened, the controller is operable to abort the copy operation and to erase the target block from the non-volatile memory subsystem.

[0045] Also described herein is a method for managing a memory module wherein the transfer of data includes a bidirectional transfer of data between the non-volatile and the volatile memory subsystems.

[0046] Also described herein is a method for managing a memory module further comprising operating the data manager to control one or more of data flow rate, data transfer size, data width size, data buffer size, data error monitoring, data error correction, and the starting time of the transfer of data.

[0047] Also described herein is a method for managing a memory module further comprising operating the data manager to control data traffic between the memory controller and at least one of the volatile and non-volatile memory subsystems.

[0048] Also described herein is a method for managing a memory module wherein data traffic control relates to any one or more of data transfer size, formatting information, direction of data flow, and the starting time of the transfer of data.

[0049] Also described herein is a method for managing a memory module wherein data traffic control by the data manager is based on instructions received from the controller.

[0050] Also described herein is a method for managing a memory module further comprising operating the data manager as a bi-directional data transfer fabric with two or more sets of data ports coupled to any one of the volatile and non-volatile memory subsystems.

[0051] Also described herein is a method for managing a memory module wherein at least one of the volatile and non-volatile memory subsystems comprises one or more memory segments.

[0052] Also described herein is a method for managing a memory module wherein each memory segment comprises at least one memory circuit, memory device, or memory die.

[0053] Also described herein is a method for managing a memory module wherein the volatile memory subsystem comprises DRAM memory.

[0054] Also described herein is a method for managing a memory module wherein the non-volatile memory subsystem comprises Flash memory.

[0055] Also described herein is a method for managing a memory module further comprising operating the data ports to independently and/or concurrently transfer data to or from one or more memory segments of the volatile or non-volatile memory subsystems.

[0056] Also described herein is a method for managing a memory module further comprising directing transfer of data bi-directionally between the volatile and non-volatile memory subsystems using the data manager and in response to memory access commands received by the controller from the memory controller.

[0057] Also described herein is a method for managing a memory module further comprising buffering the data transferred between the memory controller and non-volatile memory subsystem using the volatile memory subsystem.

[0058] Also described herein is a method for managing a memory module further comprising using the controller to perform one or more of memory address translation, memory address mapping, address domain conversion, memory access control, data error correction, and data width modulation between the volatile and non-volatile memory subsystems.

[0059] Also described herein is a method for managing a memory module further comprising using the controller to effect communication with a host system by the volatile memory subsystem in accordance with a prescribed protocol.

[0060] Also described herein is a method for managing a memory module wherein the prescribed protocol is selected from one or more of DDR, DDR2, DDR3, and DDR4 protocols.

[0061] Also described herein is a method for managing a memory module further comprising using the controller to configure memory space in the memory module based on at least one of a command received from the memory controller, a programmable value written into a register, a value corresponding to a first portion of the volatile memory subsystem, a value corresponding to a first portion of the non-volatile memory subsystem, and a timing value.

[0062] Also described herein is a method for managing a memory module wherein the controller configures the memory space of the memory module using at least a first portion of the volatile memory subsystem and a first portion of the non-volatile memory subsystem, and the controller presents a unified memory space to the memory controller.

[0063] Also described herein is a method for managing a memory module wherein the controller configures the memory space in the memory module using partitioning instructions that are application-specific.

[0064] Also described herein is a method for managing a memory module further comprising using the controller to copy booting information from the non-volatile to the volatile memory subsystem during power up.

[0065] Also described herein is a method for managing a memory module wherein the controller includes a volatile memory control module, the method further comprising generating

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commands by the volatile memory control module in response to commands from the memory controller, and transmitting the generated commands to the volatile memory subsystem.

[0066] Also described herein is a method for managing a memory module further comprising pre-fetching of data from the non-volatile memory subsystem to the volatile memory subsystem.

[0067] Also described herein is a method for managing a memory module wherein the pre-fetching is initiated by the memory controller writing an address of requested data into a register of the controller.

[0068] Also described herein is a method for managing a memory module further comprising initiating a copy operation of data of a closed block in the volatile memory subsystem to a target block in the non-volatile memory subsystem.

[0069] Also described herein is a method for managing a memory module further comprising aborting the copy operation when the closed block of the volatile memory subsystem is re-opened, and erasing the target block in the non-volatile memory subsystem.

[0070] Also described herein is a memory system having a volatile memory subsystem, a non-volatile memory subsystem, a controller coupled to the non-volatile memory subsystem, and a circuit coupled to the volatile memory subsystem, to the controller, and to a host system. In a first mode of operation, the circuit is operable to selectively isolate the controller from the volatile memory subsystem, and to selectively couple the volatile memory subsystem to the host system to allow data to be communicated between the volatile memory subsystem and the host system. In a second mode of operation, the circuit is operable to selectively couple the controller to the volatile memory subsystem to

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allow data to be communicated between the volatile memory subsystem and the nonvolatile memory subsystem using the controller, and the circuit is operable to selectively isolate the volatile memory subsystem from the host system.

[0071] Also described herein is a method for operating a memory system. The method includes coupling a circuit to a host system, a volatile memory subsystem, and a controller, wherein the controller is coupled to a non-volatile memory subsystem. In a first mode of operation that allows data to be communicated between the volatile memory subsystem and the host system, the circuit is used to (i) selectively isolate the controller from the volatile memory subsystem, and (ii) selectively couple the volatile memory subsystem to the host system. In a second mode of operation that allows data to be communicated between the volatile memory subsystem and the nonvolatile memory subsystem via the controller, the circuit is used to (i) selectively couple the controller to the volatile memory subsystem, and (ii) selectively isolate the volatile memory subsystem from the host system.

[0072] Also described herein is a nontransitory computer readable storage medium storing one or more programs configured to be executed by one or more computing devices. The programs, when executing on the one or more computing devices, cause a circuit that is coupled to a host system, to a volatile memory subsystem, and to a controller that is coupled to a nonvolatile memory subsystem, to perform a method in which, in a first mode of operation that allows data to be communicated between the volatile memory subsystem and the host system, operating the circuit to (i) selectively isolate the controller from the volatile memory subsystem, and (ii) selectively couple the volatile memory subsystem to the host system. In a second mode of operation that allows data to be communicated between the volatile memory subsystem and the nonvolatile memory subsystem via the controller, operating the circuit to (i) selectively couple the controller to the volatile memory subsystem, and (ii) selectively isolate the volatile memory subsystem from the host system.

BRIEF DESCRIPTION OF THE DRAWINGS

[0073] The accompanying drawings, which are incorporated into and constitute a part of this specification, illustrate one or more examples of embodiments and, together with the description of example embodiments, serve to explain the principles and implementations of the embodiments.

[0074] In the drawings:

FIG. 1 is a block diagram illustrating the path of data transfer, via a CPU, of a conventional memory arrangement;

FIG. 2 is a block diagram of a known EcoRAM™ architecture;

FIGS. 3A and 3B are block diagrams of a non-volatile memory DIMM or NVDIMM;

FIGS. 4A and 4B are block diagrams of a Flash-DRAM hybrid DIMM or FDHDIMM;

FIG. 5A is a block diagram of a memory module 500 in accordance with certain embodiments described herein;

FIG. 5B is a block diagram showing some functionality of a memory module such as that shown in FIG. 5A;

FIG. 6 is a block diagram showing some details of the data manager (DMgr);

FIG. 7 is a functional block diagram of the on-module controller (CDC);

FIG. 8A is a block diagram showing more details of the prior art Flash-DRAM hybrid DIMM (FDHDIMM) of FIGS. 4A and 4B;

FIG. 8B is a block diagram of a Flash-DRAM hybrid DIMM (FDHDIMM) in accordance with certain embodiments disclosed herein;

FIG. 9 is a flow diagram directed to the transfer of data from Flash memory to DRAM memory and vice versa in an exemplary FDHDIMM;

FIG. 10 is a block diagram showing an example of mapping of DRAM address space to Flash memory address space; and

FIG. 11 is a table showing estimates of the maximum allowed closed blocks in a queue to be written back to Flash memory for different DRAM densities using various average block use time.

FIG. 12 is a block diagram of an example memory system compatible with certain embodiments described herein.

FIG. 13 is a block diagram of an example memory module with ECC (error-correcting code) having a volatile memory subsystem with nine volatile memory elements and a non-volatile memory subsystem with five non-volatile memory elements in accordance with certain embodiments described herein.

FIG. 14 is a block diagram of an example memory module having a microcontroller unit and logic element integrated into a single device in accordance with certain embodiments described herein.

FIGS. 15A-15C schematically illustrate example embodiments of memory systems having volatile memory subsystems comprising registered dual in-line memory modules in accordance with certain embodiments described herein.

FIG. 16 schematically illustrates an example power module of a memory system in accordance with certain embodiments described herein.

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FIG. 17 is a flowchart of an example method of providing a first voltage and a second voltage to a memory system including volatile and non-volatile memory subsystems.

FIG. 18 is a flowchart of an example method of controlling a memory system operatively coupled to a host system and which includes at least 100 percent more storage capacity in non-volatile memory than in volatile memory.

FIG. 19 schematically illustrates an example clock distribution topology of a memory system in accordance with certain embodiments described herein.

FIG. 20 is a flowchart of an example method of controlling a memory system operatively coupled to a host system, the method including operating a volatile memory subsystem at a reduced rate in a back-up mode.

FIG. 21 schematically illustrates an example topology of a connection to transfer data slices from two DRAM segments of a volatile memory subsystem of a memory system to a controller of the memory system.

FIG. 22 is a flowchart of an example method of controlling a memory system operatively coupled to a host system, the method including backing up and/or restoring a volatile memory subsystem in slices.

DESCRIPTION OF EXAMPLE EMBODIMENTS

[0075] Example embodiments are described herein in the context of a system of computers, servers, controllers, memory modules, hard disk drives and software. Those of ordinary skill in the art will realize that the following description is illustrative only and is not intended to be in any way limiting. Other embodiments will readily suggest themselves to such skilled persons having the benefit of this disclosure. Reference will now be made in detail to

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implementations of the example embodiments as illustrated in the accompanying drawings. The same reference indicators will be used to the extent possible throughout the drawings and the following description to refer to the same or like items.

[0076] In the interest of clarity, not all of the routine features of the implementations described herein are shown and described. It will, of course, be appreciated that in the development of any such actual implementation, numerous implementation-specific decisions must be made in order to achieve the developer's specific goals, such as compliance with application- and business-related constraints, and that these specific goals will vary from one implementation to another and from one developer to another. Moreover, it will be appreciated that such a development effort might be complex and time-consuming, but would nevertheless be a routine undertaking of engineering for those of ordinary skill in the art having the benefit of this disclosure.

[0077] In accordance with this disclosure, the components, process steps, and/or data structures described herein may be implemented using various types of operating systems, computing platforms, computer programs, and/or general purpose machines. In addition, those of ordinary skill in the art will recognize that devices of a less general purpose nature, such as hardwired devices, field programmable gate arrays (FPGAs), application specific integrated circuits (ASICs), or the like, may also be used without departing from the scope and spirit of the inventive concepts disclosed herein. Where a method comprising a series of process steps is implemented by a computer or a machine and those process steps can be stored as a series of instructions readable by the machine, they may be stored on a tangible medium such as a computer memory device (e.g., ROM (Read Only Memory), PROM (Programmable Read Only

Memory), EEPROM (Electrically Eraseable Programmable Read Only Memory), Flash memory, Jump Drive, and the like), magnetic storage medium (e.g., tape, magnetic disk drive, and the like), optical storage medium (e.g., CD-ROM, DVD-ROM, paper card, paper tape and the like) and other types of program memory.

[0078] The term "exemplary" where used herein is intended to mean "serving as an example, instance or illustration." Any embodiment described herein as "exemplary" is not necessarily to be construed as preferred or advantageous over other embodiments.

[0079] Disclosed herein are arrangements for improving memory access rates and addressing the high disparity (15 to 1 ratio) between the read and write data throughput rates. In one arrangement, a Flash-DRAM-hybrid DIMM (FDHDIMM) with integrated Flash and DRAM is used. Methods for controlling such an arrangement are described.

[0080] In certain embodiments, the actual memory density (size or capacity) of the DIMM and/or the ratio of DRAM memory to Flash memory are configurable for optimal use with a particular application (for example, POS, inter-bank transaction, stock market transaction, scientific computation such as fluid dynamics for automobile and ship design, weather prediction, oil and gas expeditions, medical diagnostics such as diagnostics based on the fuzzy logic, medical data processing, simple information sharing and searching such as web search, retail store website, company home page, email or information distribution and archive, security service, and entertainment such as video-on-demand).

[0081] In certain embodiments, the device contains a high density Flash memory with a low density DRAM, wherein the DRAM is used as a data buffer for read/write operation. The Flash serves as the main memory. Certain embodiments described herein overcome the needs of having a long separation period between an Activate command (may be referred to as RAS) and a corresponding read or write command (may be referred to as first CAS command).

[0082] In accordance with one embodiment, described with reference to FIGS. 3A and 3B, a memory system 300 includes a non-volatile (for example Flash) memory subsystem 302 and a volatile (for example DRAM) memory subsystem 304. The examples of FIGS. 3A and 3B are directed to architectures of a non-volatile DIMM (NVDIMM) NVDIMM system that may use a power subsystem (not shown) that can include a battery or a capacitor as a means for energy storage to copy DRAM memory data into Flash memory when power loss occurs, is detected, or is anticipated to occur during operation. When normal power is restored, a restore NVDIMM operation is initiated and the data stored in the Flash memory is properly restored to the DRAM memory. In this architecture, the density of the Flash is about the same as the DRAM memory size or within a few multiples, although in some applications it may be higher. This type of architecture may also be used to provide non-volatile storage that is connected to the FSB (front side bus) to support RAID (Redundant Array of Independent Disks) based systems or other type of operations. An NVDIMM controller 306 receives and interprets commands from the system memory controller hub (MCH). The NVDIMM controller 306 control the NVDIMM DRAM and Flash memory operations. In FIG. 3A, the DRAM 304 communicates data with the MCH, while an internal bus 308 is used for data transfer between the DRAM and Flash memory subsystems. In FIG. 3B, the NVDIMM controller 306' of NVDIMM 300' monitors events or

commands and enables data transfer to occur in a first mode between the DRAM 304' and Flash 302' or in a second mode between the DRAM and the MCH.

[0083] In accordance with one embodiment, a general architecture for a Flash and DRAM hybrid DIMM (FDHDIMM) system 400 is shown in FIG. 4A. The FDHDIMM interfaces with an MCH (memory controller hub) to operate and behave as a high density DIMM, wherein the MCH interfaces with the non-volatile memory subsystem (for example Flash) 402 is controlled by an FDHDIMM controller 404. Although the MCH interfaces with the Flash via the FDHDIMM controller, the FDHDIMM overall performance is governed by the Flash access time. The volatile memory subsystem (for example DRAM) 406 is primarily used as a data buffer or a temporary storage location such that data from the Flash memory 402 is transferred to the DRAM 406 at the Flash access speed, and buffered or collected into the DRAM 406, which then transfers the buffered data to the MCH based on the access time of DRAM. Similarly, when the MCH transfers data to the DRAM 406, the FDHDIMM controller 404 manages the data transfer from the DRAM 406 to the Flash 402. Since the Flash memory access speed (both read and write) is relatively slower than DRAM, (e.g. for example a few hundred microseconds for read access), the average data throughput rate of FDHDIMM 400 is limited by the Flash access speed. The DRAM 406 serves as a data buffer stage that buffers the MCH read or write data. Thus, the DRAM 406 serves as a temporary storage for the data to be transferred from/to the Flash 402. Furthermore, in accordance with one embodiment, the MCH recognizes the physical density of an FDHDIMM operating as a high density DIMM as the density of Flash alone.

[0084] In accordance with one embodiment, a read operation can be performed by the MCH by sending an activate command (may be simply referred to as RAS, or row address strobe) to the FDHDIMM 400 to conduct a pre-fetch read data operation from the Flash 402 to the DRAM 406, with the pre-fetch data size being for example a page (1KB or 2KB, or may be programmable to any size). The MCH then sends a read command (may be simply referred to as CAS, or column address strobe) to read the data out input of the DRAM. In this embodiment, the data transfer from Flash to DRAM occurs at Flash access speed rates, while data transfer from DRAM to MCH occurs at DRAM access speed rates. In this example, data latency and throughput rates are the same as any DRAM operation as long as the read operations are executed onto the pages that were opened with the activate command previously sent to pre-fetch data from the Flash to DRAM. Thus, a longer separation time period between the RAS (e.g. Activate command) and the first CAS (column address strobe e.g. read or write command) is required to account for the time it takes to pre-fetch data from the Flash to DRAM.

[0085] An example of FDHDIMM operating as a DDR DIMM with SSD is shown in FIG. 4B, wherein the FDHDIMM 400'supports two different interface interpretations to the MCH. In the first interface interpretation, the MCH views the FDHDIMM 400' as a combination of DRAM DIMM and SSD (not illustrated). In this mode the MCH needs to manage two address spaces, one for the DRAMs 402' and one for the Flash 404'. The MCH is coupled to, and controls, both of the DRAM and Flash memory subsystems. One advantage of this mode is that the CPU does not need to be in the data path when data is moved from DRAM to Flash or from Flash to DRAM. In the second interface interpretation, the MCH views the FDHDIMM 400' as an on-DIMM Flash with the SSD in an extended memory space that is behind the DRAM space. Thus, in this mode, the MCH physically fetches data from the SSD to the DDR DRAM and then

the DRAM sends the data to the MCH. Since all data movement occurs on the FDHDIMM, this mode will provide better performance than if the data were to be moved through or via the CPU.

[0086] In accordance with one embodiment and as shown in FIG. 4B, the FDHDIMM 400' receives control signals 408 from the MCH, where the control signals may include one or more control signals specifically for the DRAM 402' operation and one or more control signals specifically for the Flash 404' operation. In this embodiment, the MCH or CPU is coupled to the FDHDIMM via a single data bus interface 410 which couples the MCH to the DRAM.

[0087] FIGS. 5A and 5B are block diagrams of a memory module 500 that is couplable to a host system (not shown). The host system may be a server or any other system comprising a memory system controller or an MCH for providing and controlling the read/write access to one or more memory systems, wherein each memory system may include a plurality of memory subsystems, a plurality of memory devices, or at least one memory module. The term "read/write access" means the ability of the MCH to interface with a memory system or subsystem in order to write data into it or read data from it, depending on the particular requirement at a particular time.

[0088] In certain embodiments, memory module 500 is a Flash-DRAM hybrid memory subsystem which may be integrated with other components of a host system. In certain embodiments, memory module 500 is a Flash-DRAM hybrid memory module that has the DIMM (dual-inline memory module) form factor, and may be referred to as a FDHDIMM, although it is to be understood that in both structure and operation it may be different from the FDHDIMM discussed above and described with reference to FIGS. 4A and 4B. Memory

module 500 includes two on-module intermediary components: a controller and a data manager. These on-module intermediary components may be physically separate components, circuits, or modules, or they may be integrated onto a single integrated circuit or device, or integrated with other memory devices, for example in a three dimensional stack, or in any one of several other possible expedients for integration known to those skilled in the art to achieve a specific design, application, or economic goal. In the case of a DIMM, these on-module intermediary components are an on-DIMM Controller (CDC) 502 and an on-DIMM data manager (DMgr) 504. While the DIMM form factor will predominate the discussion herein, it should be understood that this is for illustrative purposes only and memory systems using other form factors are contemplated as well. CDC 502 and data manager DMgr 504 are operative to manage the interface between a non-volatile memory subsystem such as a Flash 506, a volatile memory subsystem such as a DRAM 508, and a host system represented by MCH 510.

[0089] In certain embodiments, CDC 502 controls the read/write access to/from Flash memory 506 from/to DRAM memory 508, and to/from DRAM memory from/to MCH 510. Read/write access between DRAM 508, Flash 506 and MCH 510 may be referred to herein generally as communication, wherein control and address information C/A 560 is sent from MCH 510 to CDC 502, and possible data transfers follow as indicated by Data 550, Data 555, and/or Data 556. In certain embodiments, the CDC 502 performs specific functions for memory address transformation, such as address translation, mapping, or address domain conversion, Flash access control, data error correction, manipulation of data width or data formatting or data modulation between the Flash memory and DRAM, and so on. In certain embodiments, the CDC 502 ensures that memory module 500 provides transparent operation to the MCH in accordance with certain industry standards, such as DDR, DDR2, DDR3, DDR4 protocols. In

the arrangement shown in FIGS. 5A and 5B, there is no direct access from the MCH 510 to the Flash 506 memory subsystem. Thus in accordance with certain embodiments, the Flash access speed has minimal impact on the overall FDHDIMM access speed. In the schematic illustration of FIG. 5B and in accordance with one embodiment, the CDC controller 502 receives standard DDR commands from the MCH, interprets, and produces commands and/or control signals to control the operation of the Data manager (DMgr), the Flash memory and the DRAM memory. The DMgr controls the data path routing amongst DRAMs, Flash and MCH, as detailed below. The data path routing control signals are independently operated without any exclusivity.

[0090] An exemplary role of DMgr 504 is described with reference to FIG. 6. In certain embodiments and in response to communication from CDC 502, DMgr 504 provides a variety of functions to control data flow rate, data transfer size, data buffer size, data error monitoring or data error correction. For example, these functions or operations can be performed on-the-fly (while data is being transferred via the DMgr 504) or performed on buffered or stored data in DRAM or a buffer. In addition, one role of DMgr 504 is to provide interoperability among various memory subsystems or components and/or MCH 510.

[0091] In one embodiment, an exemplary host system operation begins with initialization. The CDC 502 receives a first command from the MCH 510 to initialize FDHDIMM 500 using a certain memory space. The memory space as would be controlled by MCH 510 can be configured or programmed during initialization or after initialization has completed. The MCH 510 can partition or parse the memory space in various ways that are optimized for a particular application that the host system needs to run or execute. In one embodiment, the CDC 502 maps the actual physical Flash 506 and DRAM 508 memory space using the information sent by MCH

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510 via the first command. In one embodiment, the CDC 502 maps the memory address space of any one of the Flash 506 and DRAM 508 memory subsystems using memory address space information that is received from the host system, stored in a register within FDHDIMM 500, or stored in a memory location of a non-volatile memory subsystem, for example a portion of Flash 506 or a separate non-volatile memory subsystem. In one embodiment, the memory address space information corresponds to a portion of initialization information of the FDHDIMM 500.

[0092] In one embodiment, MCH 510 may send a command to restore a certain amount of data information from Flash 506 to DRAM 508. The CDC 502 provides control information to DMgr 504 to appropriately copy the necessary information from Flash 506 to the DRAM 508. This operation can provide support for various host system booting operations and/or a special host system power up operation.

[0093] In one embodiment, MCH 510 sends a command which may include various fields comprising control information regarding data transfer size, data format options, and/or startup time. CDC 502 receives and interprets the command and provides control signals to DMgr 504 to control the data traffic between the Flash 506, the DRAM 508, and the MCH 510. For example, DMgr 504 receives the data transfer size, formatting information, direction of data flow (via one or more multiplexers such as 611, 612, 621, 622 as detailed below), and the starting time of the actual data transfer from CDC 502. DMgr 504 may also receive additional control information from the CDC 502 to establish a data flow path and/or to correctly establish the data transfer fabric. In certain embodiments, DMgr 504 also functions as a bi-directional data transfer fabric. For example, DMgr 504 may have more than 2 sets of data ports facing the Flash 506 and the DRAM 508. Multiplexers 611 and 612 provide controllable data paths from any one of the

DRAMs 508(1) and 508(2) (DRAM-A and DRAM-B) to any one of the MCH 510 and the Flash 506. Similarly multiplexers 621 and 622 provide controllable data paths from any one of the MCH and the Flash memory to any one of the DRAMs 508(1) and 508(2) (DRAM-A and DRAM-B). In one embodiment, DRAM 508(1) is a segment of DRAM 508, while in other embodiments, DRAM 508(1) is a separate DRAM memory subsystem. It will be understood that each memory segment can comprise one or more memory circuits, a memory devices, and/or memory integrated circuits. Of course other configurations for DRAM 508 are possible, and other data transfer fabrics using complex data paths and suitable types of multiplexing logic are contemplated.

[0094] In accordance with one embodiment, the two sets of multiplexors 611, 612 and 621, 622 allow independent data transfer to Flash 506 from DRAM-A 508(1) and DRAM-B 508(2). For example, in response to one or more control signals or a command from CDC 502, DMgr 504 can transfer data from DRAM-A 508(1) to MCH 510, via multiplexer 611, at the same time as from DRAM-B 508(2) to the Flash 506, via multiplexer 612; or data is transferred from DRAM-B 508(2) to MCH 510, via multiplexer 611, and simultaneously data is transferred from the Flash 506 to DRAM-A 508(1), via multiplexer 621. Further, in the same way that data can be transferred to or from the DRAM in both device-wide or segment-by-segment fashion, data can be transferred to or from the flash memory in device-wide or segment-by-segment fashion, and the flash memory can be addressed and accessed accordingly.

[0095] In accordance with one embodiment the illustrated arrangement of data transfer fabric of DMgr 504 also allows the CDC 502 to control data transfer from the Flash memory to the MCH by buffering the data from the Flash 506 using a buffer 602, and matching the data rate

and/or data format of MCH 510. The buffer 602 is shown in FIG. 6 as a portion of a data format module 604; however, buffer 602 may also be a distributed buffer such that one buffer is used for each one of the set of multiplexer logic elements shown as multiplexers 611, 612, 621, and 622. Various buffer arrangements may be used, such as a programmable size buffer to meet the requirement of a given system design requirement, for example the disparity between read/write access time; or overall system performance, for example latency. In certain embodiments, the buffer 604 may introduce one or more clock cycle delays into a data communication path between MCH 510, DRAM 508, and Flash 506.

[0096] In certain embodiments, data format module 604 contains a data formatting subsystem (not shown) to enable DMgr 504 to format and perform data transfer in accordance with control information received from CDC502. Data buffer 604 of data format module 602, discussed above, also supports a wide data bus 606 coupled to the Flash memory 506 operating at a first frequency, while receiving data from DRAM 508 using a relatively smaller width data bus 608 operating at a second frequency, the second frequency being larger than the first frequency in certain embodiments. The buffer 602 is designed to match the data flow rate between the DRAM 508 and the Flash 506.

[0097] A register 690 provides the ability to register commands received from MCH 510 via C/A 560 (FIG. 5A). The register 690 may communicate these commands to CDC 502 and/or to the DRAM 508 and/or Flash 506. The register 690 communicates these registered commands to CDC 502 for processing. The register 690 may also include multiple registers (not shown), such that it can provide the ability to register multiple commands, a sequence of commands, or

provide a pipeline delay stage for buffering and providing a controlled execution of certain commands received form MCH 510.

[0098] In certain embodiments, the register 690 may register commands from MCH 510 and transmit the registered commands to DRAM 508 and/or Flash 506 memory subsystems. In certain embodiments, the CDC 502 monitors commands received from MCH 510, via control and address bus C/A 560, and provides appropriate control information to DMgr 504, DRAM 508, or Flash 506 to execute these commands and perform data transfer operations between MCH 510 and FDHDIMM 500 via MCH data bus 610.

[0099] FIG. 7 illustrates a functional block diagram of the CDC 502. In certain embodiments, the major functional blocks of the CDC 502 are a DRAM control block DRAMCtrl 702, Flash control block FlashCtrl 704, MCH command interpreter CmdInt 706, DRAM-Flash interface scheduler Scheduler 708, and DMgr control block (DMgrCtrl) 710.

[00100] In accordance with one embodiment, DRAMCtrl 702 generates DRAM commands that are independent from the commands issued by the MCH 510. In accordance with one embodiment, when the MCH 510 initiates a read/write operation from/to the same DRAM 508 that is currently executing a command from the DRAMCtrl 702, then the CDC 502 may choose to instruct DRAMCtrl 702 to abort its operation in order to execute the operation initiated by the MCH. However, the CDC 502 may also pipeline the operation so that it causes DRAMCtrl 702 to either halt or complete its current operation prior to executing that of the MCH. The CDC 502 may also instruct DRAMCtrl 702 to resume its operation once the command from MCH 510 is completed.

[00101] In accordance with one embodiment, the FlashCtrl 704 generates appropriate Flash commands for the proper read/write operations. The CmdInt 706 intercepts commands received from MCH 510 and generates the appropriate control information and control signals and transmit them to the appropriate FDHDIMM functional block. For example, CmdInt 706 issues an interrupt signal to the DRAMCtrl 702 when the MCH issues a command that collides (conflicts) with the currently executing or pending commands that DRAMCtrl 702 has initiated independently from MCH 510, thus subordinating these commands to those from the MCH. The Scheduler 708 schedules the Flash–DRAM interface operation such that there is no resource conflict in the DMgr 504. In accordance with one embodiment, the Scheduler 708 assigns time slots for the DRAMCtrl 702 and FlashCtrl 704 operation based on the current status and the pending command received or to be received from the MCH. The DMgrCtrl 710 generates and sends appropriate control information and control signals for the proper operation and control of the data transfer fabric to enable or disable data paths between Flash 506, DRAM 508, and the MCH 510.

[00102] FIG. 8A is a block diagram showing a Flash-DRAM hybrid DIMM (FDHDIMM). As seen from FIG. 8A, this Flash-DRAM hybrid DIMM requires two separate and independent address buses to separately control the address spaces: one for the Flash memory Flash 506 and the other for the DRAM memory DRAM 508. The MCH treats the DRAM 508 and Flash 506 as separate memory subsystems, for example DRAM and SSD/HD memory subsystems. The memory in each address space is controlled directly by the MCH. However, the on-DIMM data path between Flash 506 and DRAM 508 allows for direct data transfer to occur between the Flash 506 and the DRAM 508 in response to control information from Ctrl 502. In this embodiment, this data transfer mechanism provides direct support for executing commands from

the MCH without having the MCH directly controlling the data transfer, and thus improving data transfer performance from Flash 506 to the DRAM 508. However, the MCH needs to manage two address spaces and two different memory protocols simultaneously. Moreover, the MCH needs to map the DRAM memory space into the Flash memory space, and the data interface time suffers due to the difference in the data access time between the Flash memory and the DRAM memory.

[00103] In accordance with one embodiment, a memory space mapping of a Flash-DRAM hybrid DIMM is shown in FIG. 8B. A memory controller of a host system (not shown) controls both of the DRAM 508 address space and the Flash 506 address space using a single unified address space. The CDC 502 receives memory access commands from the MCH and generates control information for appropriate mapping and data transfer between Flash and DRAM memory subsystem to properly carry out the memory access commands. In one embodiment, the memory controller of the host system views the large Flash memory space as a DRAM memory space, and accesses this unified memory space with a standard DDR (double data rate) protocol used for accessing DRAM. The unified memory space in this case can exhibit overlapping memory address space between the Flash 506 and the DRAM 508. The overlapping memory address space may be used as a temporary storage or buffer for data transfer between the Flash 506 and the DRAM 508. For example, the DRAM memory space may hold a copy of data from the selected Flash memory space such that the MCH can access this data normally via DDR memory access commands. The CDC 502 controls the operation of the Flash 506 and DRAM 508 memory subsystems in response to commands received from a memory controller of a host system.

[00104] In one embodiment, the unified memory space corresponds to a contiguous address space comprising a first portion of the address space of the Flash 506 and a first portion of the address space of the DRAM 508. The first portion of the address space of the Flash 506 can be determined via a first programmable register holding a first value corresponding to the desired Flash memory size to be used. Similarly, the first portion of the address space of the DRAM 508 can be determined via a second programmable register holding a second value corresponding to the desired DRAM memory size to be used. In one embodiment, any one of the first portion of the address space of the Flash 506 and the first portion of the address space of the DRAM 508 is determined via a first value corresponding to a desired performance or memory size, the first value being received by the CDC 502 via a command sent by memory controller of the host system.

[00105] In accordance with one embodiment, a flow diagram directed to the transfer of data from Flash memory to DRAM memory and vice versa in an exemplary FDHDIMM is shown in Fig. 9. In certain embodiments, data transfer from the Flash 506 to the DRAM 508 occurs in accordance with memory access commands which the CDC 502 receives from the memory controller of the host system. In certain embodiments, the CDC 502 controls the data transfer from the DRAM 508 to the Flash 506 so as to avoid conflict with any memory operation that is currently being executed. For example, when all the pages in a particular DRAM memory block are closed. The CDC 502 partitions the DRAM memory space into a number of blocks for the purpose of optimally supporting the desired application. The controller can configure memory space in the memory module based on at least one of one or more commands received from the MCH, instructions received from the MCH, a programmable value written into a register, a value corresponding to a first portion of the volatile memory subsystem, a value corresponding to a

first portion of the non-volatile memory subsystem, and a timing value. Furthermore, the block size can be configurable by the memory controller of the host system, such that the number pages in a block can be optimized to support a particular application or a task. Furthermore, the block size may be configured on-the-fly, e.g. CDC 502 can receive instruction regarding a desired block size from the memory controller via a memory command, or via a programmable value.

[00106] In certain embodiments, a memory controller can access the memory module using a standard access protocol, such as JEDEC's DDR DRAM, by sending a memory access command to the CDC 502 which in turn determines what type of a data transfer operation it is and the corresponding target address where the data information is stored, e.g. data information is stored in the DRAM 508 or Flash 506 memory subsystems. In response to a read operation, if the CDC 502 determines that data information, e.g. a page (or block), does not reside in the DRAM 508 but resides in Flash 506, then the CDC 502 initiates and controls all necessary data transfer operations from Flash 506 to DRAM 508 and subsequently to the memory controller. In one embodiment, once the CDC 502 completes the data transfer operation of the requested data information from the Flash 506 to the DRAM 508, the CDC 502 alerts the memory controller to retrieve the data information from the DRAM 508. In on embodiment, the memory controller initiates the copying of data information from Flash 506 to DRAM 508 by writing, into a register in the CDC 502, the target Flash address along with a valid block size. The CDC 502 in turn, executes appropriate operations and generates control information to copy the data information to the DRAM 508. Consequently, the memory controller can access or retrieve the data information using standard memory access commands or protocol.

[00107] An exemplary flow chart is shown in FIG. 9, a starting step or power up 902, is followed by an initialization step 904, the memory controller initiates, at step 906, a data move from the Flash 506 to the DRAM 508 by writing target address and size, to a control register in the CDC 502, which then copies, at 908, data information from the Flash 506 to the DRAM 508 and erases the block in the Flash. Erasing the data information from Flash may be accomplished independently from (or concurrently with) other steps that CDC 502 performs in this flow chart, i.e. other steps can be executed concurrently with the Erase the Flash block step. Once the data information or a block of data information is thus moved to the DRAM 508, the memory controller can operate on this data block using standard memory access protocol or commands at 910. The CDC 502 checks, at 912, if any of the DRAM 508 blocks, or copied blocks, are closed. If the memory controller closed any open blocks in DRAM 508, then the CDC 502 initiate a Flash write to write the closed block from the DRAM 508 to the Flash 506, at 914. In addition, the memory controller, at 916, reopens the closed block that is currently being written into the Flash 506, then the CDC 502 stops the Flash write operation and erases the Flash block which was being written to, as shown at 918. Otherwise, the CDC 502 continues and completes the writing operation to the Flash at 920.

[00108] The dashed lines in FIG. 9 indicate independent or parallel activities that can be performed by the CDC 502. At any time the CDC 502 receives a DRAM load command from a memory controller which writes a Flash target address and/or block size information into the RC register(s) at 922, as described above, then the CDC 502 executes a load DRAM w/RC step 906 and initiates another branch (or a thread) of activities that includes steps 908 – 922. In one embodiment, the CDC 502 controls the data transfer operations between DRAM 508 and Flash 506 such that the Flash 506 is completely hidden from the memory controller. The CDC 502

monitors all memory access commands sent by the memory controller using standard DRAM protocol and appropriately configures and manipulate both Flash 506 and DRAM 508 memory subsystems to perform the requested memory access operation and thus achieve the desired results. The memory controller does not interface directly with the Flash memory subsystem. Instead, the memory controller interfaces with the CDC 502 and/or DMgr 504 as shown in Fig. 5 and Fig. 6. Moreover, the memory controller may use one or more protocol, such as DDR, DDR2, DDR3, DDR4 protocols or the like.

[00109] In accordance with one embodiment, an example of mapping a DRAM address space to Flash memory address space is shown in FIG. 10. Two sets (1002, 1004) of address bits AD6 to AD17, forming a 24 bit extended memory page address, are allocated for the block address. For example, assuming a Block size of 256K Bytes, then a 24-bit block address space (using the two sets of AD6 to AD17 1002 and 1004) would enable access to 4TB of Flash memory storage space. If a memory module has 1GB of DRAM storage capacity, then it can hold approximately 4K Blocks of data in the DRAM memory, each Block comprise 256 K Bytes of data. The DRAM address space, corresponding to the 4K blocks, can be assigned to different virtual ranks and banks, where the number of virtual ranks and banks is configurable and can be manipulated to meet a specific design or performance needs. For example, if a 1G Bytes memory module is configured to comprise two ranks with eight banks per rank, then each bank would hold two hundred fifty (250) blocks or the equivalent of 62 M Bytes or 62K pages, where each page correspond to a 1K Bytes. Other configurations using different page, block, banks, or ranks numbers may also be used. Furthermore, an exemplary mapping of 24-bit DDR DIMM block address to Flash memory address, using Block addressing as described above, is shown in Fig. 10. The 24-bit can be decomposed into fields, such as a logical unit number LUN address 1061

field, a Block address 1051 field, a Plane address 1041, a Page address 1031, and a group of least significant address bits A_0A_1 1021. The Plane address 1041 is a sub address of the block address, and it may be used to support multiple page IO so as to improve Flash memory subsystem operation. In this example, it is understood that different number of bits may be allocated to each field of the 24-bit

[00110] The CDC 502 manages the block write-back operation by queuing the blocks that are ready to be written back to the Flash memory. As described above, if any page in a queued block for a write operation is reopened, then the CDC 502 will stop the queued block write operation, and remove the block from the queue. Once all the pages in a block are closed, then the CDC 502 restarts the write-back operation and queue the block for a write operation.

[00111] In accordance with one embodiment, an exemplary read operation from Flash 506 to DRAM 508 can be performed in approximately 400μs, while a write operation from DRAM 508 to Flash 506 can be performed in approximately 22ms resulting in a read to write ratio of 55 to 1. Therefore, if the average time a host system's memory controller spends accessing data information in a Block of DRAM is about 22ms (that is the duration that a Block comprises one or more pages that are open), then the block write-back operation from DRAM to Flash would not impact performance and hence the disparity between read and write access may be completely hidden from the memory controller. If the block usage time is 11ms instead of 22ms, then the CDC 502 control the data transfer operation between DRAM 508 and Flash 506 such that there are no more than 9 closed blocks in the queue to be written-back to the Flash memory, hence approximately an average of 100ms can be maintained for a standard DDR DRAM operation. Moreover, the number of closed Blocks in the queue to be written-back to the Flash

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memory subsystem varies with the average block usage time and the desired performance for a specific host system or for a specific application running using the host system resources.

[00112] Consequently, the maximum number of closed Blocks to be written-back to Flash can be approximated to be

((#of blocks per bank)/(ratio of 'Flash_block_write_time' to 'Flash_read_time'))*(
(Block usage time)/('Flash_block_write_time'))

[00113] In order to maintain less than 100ms time period for queued write-back Blocks, then using a Flash memory subsystem having 22ms write access time per Block would results in a maximum number of four Blocks to be queued for write operation to Flash 506. Therefore, on average approximately 88ms (= 22ms * 4) for blocks means that each bank should not have more than four Blocks that need to be written back to the Flash 506.

[00114] The above equation also indicates that bigger DRAM memory space can support shorter block usage times. For example, 2GB of DRAM memory allows the 8 closed blocks to be written-back to Flash. The table in FIG. 11 provides an estimation of the maximum allowed closed blocks in the queue to be written back to the Flash memory for different DRAM density using various average block use time.

[00115] Certain embodiments described herein include a memory system which can communicate with a host system such as a disk controller of a computer system. The memory system can include volatile and non-volatile memory, and a controller. The controller backs up

the volatile memory using the non-volatile memory in the event of a trigger condition. Trigger conditions can include, for example, a power failure, power reduction, request by the host system, etc. In order to power the system in the event of a power failure or reduction, the memory system can include a secondary power source which does not comprise a battery and may include, for example, a capacitor or capacitor array.

[00116] In certain embodiments, the memory system can be configured such that the operation of the volatile memory is not adversely affected by the non-volatile memory or by th controller when the volatile memory is interacting with the host system. For example, one or more isolation devices may isolate the non-volatile memory and the controller from the volatile memory when the volatile memory is interacting with the host system and may allow communication between the volatile memory and the non-volatile memory when the data of the volatile memory is being restored or backed-up. This configuration generally protects the operation of the volatile memory when isolated while providing backup and restore capability in the event of a trigger condition, such as a power failure.

[00117] In certain embodiments described herein, the memory system includes a power module which provides power to the various components of the memory system from different sources based on a state of the memory system in relation to a trigger condition (e.g., a power failure). The power module may switch the source of the power to the various components in order to efficiently provide power in the event of the power failure. For example, when no power failure is detected, the power module may provide power to certain components, such as the volatile memory, from system power while charging a secondary power source (e.g., a capacitor

array). In the event of a power failure or other trigger condition, the power module may power the volatile memory elements using the previously charged secondary power source.

[00118] In certain embodiments, the power module. transitions relatively smoothly from powering the volatile memory with system power to powering it with the secondary power source. For example, the power system may power volatile memory with a third power source from the time the memory system detects that power failure is likely to occur until the time the memory system detects that the power failure has actually occurred.

[00119] In certain embodiments, the volatile memory system can be operated at a reduced frequency during backup and/or restore operations which can improve the efficiency of the system and save power. In some embodiments, during backup and/or restore operations, the volatile memory communicates with the non-volatile memory by writing and/or. reading data words in bit-wise slices instead of by writing entire words at once. In certain embodiments, when each slice is being written to or read from the volatile memory the unused slice(s) of volatile memory is not active, which can reduce the power consumption of the system.

[00120] In yet other embodiments, the non-volatile memory can include at least 100 percent more storage capacity than the volatile memory. This configuration can allow the memory system to efficiently handle subsequent trigger conditions.

[00121] FIG. 12 is a block diagram of an example memory system 1010 compatible with certain embodiments described herein. The memory system 1010 can be coupled to a host computer system and can include a volatile memory subsystem 1030, a non-volatile memory

subsystem 1040, and a controller 1062 operatively coupled to the non-volatile memory subsystem 1040. In certain embodiments, the memory system 1010 includes at least one circuit 1052 configured to selectively operatively decouple the controller 1062 from the volatile memory subsystem 1030.

[00122] In certain embodiments, the memory system 1010 comprises a memory module. The memory system 1010 may comprise a printed-circuit board (PCB) 1020. In certain embodiments, the memory system 1010 has a memory capacity of 512-MB, 1-GB, 2-GB, 4-GB, or 8-GB. Other volatile memory capacities are also compatible with certain embodiments described herein. In certain embodiments, the memory system 10 has a non-volatile memory capacity of 512-MB, 1-GB, 2-GB, 4-GB, 8-GB, 16-GB, or 32-GB. Other non-volatile memory capacities are also compatible with certain embodiments described herein. In addition, memory systems 1010 having widths of 4 bytes, 8 bytes, 16 bytes, 32 bytes, or 32 bits, 64 bits, 128 bits, 256 bits, as well as other widths (in bytes or in bits), are compatible with embodiments described herein. In certain embodiments, the PCB 1020 has an industry-standard form factor. For example, the PCB 1020 can have a low profile (LP) form factor with a height of 30 millimeters and a width of 133.35 millimeters. In certain other embodiments, the PCB 1020 has a very high profile (VHP) form factor with a height of 50 millimeters or more. In certain other embodiments, the PCB 1020 has a very low profile (VLP) form factor with a height of 18.3 millimeters. Other form factors including, but not limited to, small-outline (SO-DIMM), unbuffered (UDIMM), registered (RDIMM), fully-buffered (FBDIMM), miniDIMM, mini-RDIMM, VLP mini-DIMM, micro-DIMM, and SRAM DIMM are also compatible with certain embodiments described herein. For example, in other embodiments, certain non-DIMM form factors are possible such as, for

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example, single in-line memory module (SIMM), multi-media card (MMC), and small computer system interface (SCSI).

[00123] In certain preferred embodiments, the memory system 1010 is in electrical communication with the host system. In other embodiments, the memory system 1010 may communicate with a host system using some other type of communication, such as, for example, optical communication. Examples of host systems include, but are not limited to, blade servers, 1U servers, personal computers (PCs), and other applications in which space is constrained or limited. The memory system 1010 can be in communication with a disk controller of a computer system, for example. The PCB 1020 can comprise an interface 1022 that is configured to be in electrical communication with the host system (not shown). For example, the interface 1022 can comprise a plurality of edge connections which fit into a corresponding slot connector of the host system. The interface 1022 of certain embodiments provides a conduit for power voltage as well as data, address, and control signals between the memory system 1010 and the host system. For example, the interface 1022 can comprise a standard 240-pin DDR2 edge connector.

[00124] The volatile memory subsystem 1030 comprises a plurality of volatile memory elements 1032 and the non-volatile memory subsystem 1040 comprises a plurality of non-volatile memory elements 1042. Certain embodiments described herein advantageously provide nonvolatile storage via the non-volatile memory subsystem 1040 in addition to high-performance (e.g., high speed) storage via the volatile memory subsystem 1030. In certain embodiments, the first plurality of volatile memory elements 1032 comprises two or more dynamic random-access memory (DRAM) elements. Types of DRAM elements 1032 compatible with certain embodiments described herein include, but are not limited to, DDR, DDR2, DDR3, and

synchronous DRAM (SDRAM). For example, in the block diagram of FIG. 12, the first memory bank 1030 comprises eight 64Mx8 DDR2 SDRAM elements 1032. The volatile memory elements 1032 may comprise other types of memory elements such as static random-access memory (SRAM). In addition, volatile memory elements 1032 having bit widths of 4, 8, 16, 32, as well as other bit widths, are compatible with certain embodiments described herein. Volatile memory elements 1032 compatible with certain embodiments described herein have packaging which include, but are not limited to, thin small-outline package (TSOP), ball-grid-array (BGA), fine-pitch BGA (FBOA), micro-BOA (1.1,BGA), mini-BGA (mBGA), and chip-scale packaging (CSP).

[00125] In certain embodiments, the second plurality of non-volatile memory elements 1042 comprises one or more flash memory elements. Types of flash memory elements 1042 compatible with certain embodiments described herein include, but are not limited to, NOR flash, NAND flash, ONE-NAND flash, and multi-level cell (MLC). For example, in the block diagram of FIG. 12, the second memory bank 1040 comprises 512 MB of flash memory organized as four 128Mbx8 NAND flash memory elements 1042. In addition, nonvolatile memory elements 1042 having bit widths of 4, 8, 16, 32, as well as other bit widths, are compatible with certain embodiments described herein. Non-volatile memory elements 1042 compatible with certain embodiments described herein have packaging which include, but are not limited to, thin small-outline package (TSOP), ball-grid-array (BOA), fine-pitch BOA (FBGA), micro-BOA (POA), mini-BGA (mBGA), and chip-scale packaging (CSP).

[00126] FIG. 13 is a block diagram of an example memory module 10 with ECC (error-correcting code) having a volatile memory subsystem 1030 with nine volatile memory elements

1032 and a non-volatile memory subsystem 1040 with five non-volatile memory elements 1042 in accordance with certain embodiments described herein. The additional memory element 1032 of the first memory bank 1030 and the additional memory element 1042 of the second memory bank 1040 provide the ECC capability. In certain other embodiments, the volatile memory subsystem 1030 comprises other numbers of volatile memory elements 1032 (e.g., 2, 3, 4, 5, 6, 7, more than 9). In certain embodiments, the non-volatile memory subsystem 1040 comprises other numbers of nonvolatile memory elements 1042 (e.g., 2, 3, more than 5).

[00127] Referring to FIG. 12, in certain embodiments, the logic element 1070 comprises a field-programmable gate array (FPGA). In certain embodiments, the logic element 1070 comprises an FPGA available from Lattice Semiconductor Corporation which includes an internal flash. In certain other embodiments, the logic element 1070 comprises an FPOA available from another vendor. The internal flash can improve the speed of the memory system 1010 and save physical space. Other types of logic elements 1070 compatible with certain embodiments described herein include, but are not limited to, a programmable-logic device (PLD), an application-specific integrated circuit (ASIC), a custom-designed semiconductor device, a complex programmable logic device (CPLD). In certain embodiments, the logic element 1070 is a custom device. In certain embodiments, the logic element 1070 comprises various discrete electrical elements, while in certain other embodiments, the logic element 1070 comprises one or more integrated circuits. FIG. 14 is a block diagram of an example memory module 1010 having a microcontroller unit 1060 and logic element 1070 integrated into a single controller 1062 in accordance with certain embodiments described herein. In certain embodiments, the controller 1062 includes one or more other components. For example, in one

embodiment, an FPGA without an internal flash is used and the controller 1062 includes a separate flash memory component which stores configuration information to program the FPGA.

[00128] In certain embodiments, the at least one circuit 1052 comprises one or more switches coupled to the volatile memory subsystem 1030, to the controller 1062, and to the host computer (e.g., via the interface 1022, as schematically illustrated by FIGS. 12-14). The one or more switches are responsive to signals (e.g., from the controller 1062) to selectively operatively decouple the controller 1062 from the volatile memory subsystem 1030 and to selectively operatively couple the controller 1062 to the volatile memory subsystem 1030. In addition, in certain embodiments, the at least one circuit 1052 selectively operatively couples and decouples the volatile memory subsystem 1030 and the host system.

[00129] In certain embodiments, the volatile memory subsystem 1030 can comprise a registered DIMM subsystem comprising one or more registers 1160 and a plurality of DRAM elements 1180, as schematically illustrated by FIG. 15A. In certain such embodiments, the at least one circuit 1052 can comprise one or more switches 1172 coupled to the controller 1062 (e.g., logic element 1070) and to the volatile memory subsystem 1030 which can be actuated to couple and decouple the controller 1062 to and from the volatile memory subsystem 1030, respectively. The memory system 1010 further comprises one or more switches 1170 coupled to the one or more registers 1160 and to the plurality of DRAM elements 1180 as schematically illustrated by FIG. 15A. The one or more switches 1170 can be selectively switched, thereby selectively operatively coupling the volatile memory subsystem 1030 to the host system 1150. In certain other embodiments, as schematically illustrated by FIG. 15B, the one or more switches 1174 are also coupled to the one or more registers 1160 and to a power source 1162 for the one

or more registers 1160. The one or more switches 1174 can be selectively switched to turn power on or off to the one or more registers 1160, thereby selectively operatively coupling the volatile memory subsystem 1030 to the host system 1150. As schematically illustrated by FIG. 15C, in certain embodiments the at least one circuit 1052 comprises a dynamic on-die termination (ODT) 1176 circuit of the logic element 1070. For example, the logic element 1070 can comprise a dynamic ODT circuit 1176 which selectively operatively couples and decouples the logic element 1070 to and from the volatile memory subsystem 1030, respectively. In addition, and similar to the example embodiment of FIG. 15A described above, the one or more switches 1170 can be selectively switched, thereby selectively operatively coupling the volatile memory subsystem 1030 to the host system 1150.

[00130] Certain embodiments described herein utilize the non-volatile memory subsystem 1040 as a flash "mirror" to provide backup of the volatile memory subsystem 1030 in the event of certain system conditions. For example, the non-volatile memory subsystem 1040 may backup the volatile memory subsystem 1030 in the event of a trigger condition, such as, for example, a power failure or power reduction or a request from the host system. In one embodiment, the nonvolatile memory subsystem 1040 holds intermediate data results in a noisy system environment when the host computer system is engaged in a long computation. In certain embodiments, a backup may be performed on a regular basis. For example, in one embodiment, the backup may occur every millisecond in response to a trigger condition. In certain embodiments, the trigger condition occurs when the memory system 1010 detects that the system voltage is below a certain threshold voltage. For example, in one embodiment, the threshold voltage is 1010 percent below a specified operating voltage. In certain embodiments, a trigger condition occurs when the voltage goes above a certain threshold value, such as, for example,

1010 percent above a specified operating voltage. In some embodiments, a trigger condition occurs when the voltage goes below a threshold or above another threshold. In various embodiments, a backup and/or restore operation may occur in reboot and/or non-reboot trigger conditions.

[00131] As schematically illustrated by FIGS. 12 and 13, in certain embodiments, the controller 1062 may comprise a microcontroller unit (MCU) 1060 and a logic element 1070. In certain embodiments, the MCU 1060 provides memory management for the non-volatile memory subsystem 1040 and controls data transfer between the volatile memory subsystem 30 and the nonvolatile memory subsystem 1040. The MCU 1060 of certain embodiments comprises a 16-bit microcontroller, although other types of microcontrollers are also compatible with certain embodiments described herein. As schematically illustrated by FIGS. 12 and 13, the logic element 1070 of certain embodiments is in electrical communication with the non-volatile memory subsystem 1040 and the MCU 1060. The logic element 1070 can provide signal level translation between the volatile memory elements 1032 (e.g., 1.8V SSTL-2 for DDR2 SDRAM elements) and the non-volatile memory elements 1042 (e.g., 3V TTL for NAND flash memory elements). In certain embodiments, the logic element 1070 is also programmed to perform address/address translation between the volatile memory subsystem 1030 and the non-volatile memory subsystem 1040. In certain preferred embodiments, 1-NAND type flash are used for the non-volatile memory elements 1042 because of their superior read speed and compact structure.

[00132] The memory system 1010 of certain embodiments is configured to be operated in at least two states. The at least two states can comprise a first state in which the controller 1062 and the non-volatile memory subsystem 1040 are operatively decoupled (e.g., isolated) from the

volatile memory subsystem 1030 by the at least one circuit 1052 and a second state in which the volatile memory subsystem 1030 is operatively coupled to the controller 1062 to allow data to be communicated between the volatile memory subsystem 1030 and the nonvolatile memory subsystem 1040 via the controller 1062. The memory system 1010 may transition from the first state to the second state in response to a trigger condition, such as when the memory system 1010 detects that there is a power interruption (e.g., power failure or reduction) or a system hang-up.

[00133] The memory system 1010 may further comprise a voltage monitor 1050. The voltage monitor circuit 1050 monitors the voltage supplied by the host system via the interface 1022. Upon detecting a low voltage condition (e.g., due to a power interruption to the host system), the voltage monitor circuit 1050 may transmit a signal to the controller 1062 indicative of the detected condition. The controller 1062 of certain embodiments responds to the signal from the voltage monitor circuit 1050 by transmitting a signal to the at least one circuit 1052 to operatively couple the controller to the volatile memory system 1030, such that the memory system 1010 enters the second state. For example, the voltage monitor 1050 may send a signal to the MCU 1060 which responds by accessing the data on the volatile memory system 1030 and by executing a write cycle on the nonvolatile memory subsystem 1040. During this write cycle, data is read from the volatile memory subsystem 1030 and is transferred to the non-volatile memory subsystem 1040 via the MCU 1060. In certain embodiments, the voltage monitor circuit 1050 is part of the controller 1062 (e.g., part of the MCU 1060) and the voltage monitor circuit 1050 transmits a signal to the other portions of the controller 1062 upon detecting a power threshold condition.

[00134] The isolation or operational decoupling of the volatile memory subsystem 1030 from the non-volatile memory subsystem in the first state can preserve the integrity of the operation of the memory system 1010 during periods of operation in which signals (e.g., data) are transmitted between the host system and the volatile memory subsystem 1030. For example, in one embodiment during such periods of operation, the controller 1062 and the nonvolatile memory subsystem 1040 do not add a significant capacitive load to the volatile memory system 1030 when the memory system 1010 is in the first state. In certain such embodiments, the capacitive load of the controller 1062 and the non-volatile memory subsystem 1040 do not significantly affect the signals propagating between the volatile memory subsystem 1030 and the host system. This can be particularly advantageous in relatively high-speed memory systems where loading effects can be significant. In one preferred embodiment, the at least one circuit 1052 comprises an FSA1208 Low-Power, Eight-Port, Hi-Speed Isolation Switch from Fairchild Semiconductor. In other embodiments, the at least one circuit 1052 comprises other types of isolation devices.

[00135] Power may be supplied to the volatile memory subsystem 1030 from a first power supply (e.g., a system power supply) when the memory system 1010 is in the first state and from a second power supply 1080 when the memory system 1010 is in the second state. In certain embodiments, the memory system 1010 is in the first state when no trigger condition (e.g., a power failure) is present and the memory system 1010 enters the second state in response to a trigger condition. In certain embodiments, the memory system 1010 has a third state in which the controller 1062 is operatively decoupled from the volatile memory subsystem 1030 and power is supplied to the volatile memory subsystem 1030 from a third power supply (not shown). For example, in one embodiment the third power supply may provide power to the volatile memory

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subsystem 1030 when the memory system 1010 detects that a trigger condition is likely to occur but has not yet occurred.

[00136] In certain embodiments, the second power supply 1080 does not comprise a battery. Because a battery is not used, the second power supply 1080 of certain embodiments may be relatively easy to maintain, does not generally need to be replaced, and is relatively environmentally friendly. In certain embodiments, as schematically illustrated by FIGS. 12-14, the second power supply 1080 comprises a step-up transformer 1082, a step-down transformer 1084, and a capacitor bank 1086 comprising one or more capacitors (e.g., double-layer capacitors). In one example embodiment, capacitors may take about three to four minutes to charge and about two minutes to discharge. In other embodiments, the one or more capacitors may take a longer time or a shorter time to charge and/or discharge. For example, in certain embodiments, the second power supply 1080 is configured to power the volatile memory subsystem 1030 for less than thirty minutes. In certain embodiments, the second power supply 1080 may comprise a battery. For example, in certain embodiments, the second power supply 1080 comprises a battery and one or more capacitors and is configured to power the volatile memory subsystem 1030 for no more than thirty minutes.

[00137] In certain embodiments, the capacitor bank 1086 of the second power supply 1080 is charged by the first power supply while the memory system 1010 is in the first state. As a result, the second power supply 1080 is fully charged when the memory system 1010 enters the second state. The memory system 1010 and the second power supply 1080 may be located on the same printed circuit board 1020. In other embodiments, the second power supply 1080 may not be on

the same printed circuit board 1020 and may be tethered to the printed circuit board 1020, for example.

[00138] When operating in the first state, in certain embodiments, the step-up transformer 1082 keeps the capacitor bank 1086 charged at a peak value. In certain embodiments, the step-down transformer 1084 acts as a voltage regulator to ensure that regulated voltages are supplied to the memory elements (e.g., 1.8V to the volatile DRAM elements 1032 and 3.0V to the non-volatile flash memory elements 1042) when operating in the second state (e.g., during power down). In certain embodiments, as schematically illustrated by FIGS. 12-14, the memory module 1010 further comprises a switch 1090 (e.g., FET switch) that switches power provided to the controller 1062, the volatile memory subsystem 1030, and the non-volatile memory subsystem 1040, between the power from the second power supply 1080 and the power from the first power supply (e.g., system power) received via the interface 1022. For example, the switch 1090 may switch from the first power supply to the second power supply 1080 when the voltage monitor 1050 detects a low voltage condition. The switch 1090 of certain embodiments advantageously ensures that the volatile memory elements 1032 and non-volatile memory elements 1042 are powered long enough for the data to be transferred from the volatile memory elements 1032 and stored in the non-volatile memory elements 1042. In certain embodiments, after the data transfer is complete, the switch 1090 then switches back to the first power supply and the controller 1062 transmits a signal to the at least one circuit 1052 to operatively decouple the controller 1062 from the volatile memory subsystem 1030, such that the memory system 1010 reenters the first state.

[00139] When the memory system 1010 re-enters the first state, data may be transferred back from the non-volatile memory subsystem 1040 to the volatile memory subsystem 1030 via the

controller 1062. The host system can then resume accessing the volatile memory subsystem 1030 of the memory module 1010. In certain embodiments, after the memory system 1010 enters or re-enters the first state (e.g., after power is restored), the host system accesses the volatile memory subsystem 1030 rather than the non-volatile memory subsystem 1040 because the volatile memory elements 1032 have superior read/write characteristics. In certain embodiments, the transfer of data from the volatile memory bank 1030 to the nonvolatile memory bank 1040, or from the non-volatile memory bank 1040 to the volatile. memory bank 1030, takes less than one minute per GB.

[00140] In certain embodiments, the memory system 1010 protects the operation of the volatile memory when communicating with the host-system and provides backup and restore capability in the event of a trigger condition such as a power failure. In certain embodiments, the memory system 1010 copies the entire contents of the volatile memory subsystem 1030 into the nonvolatile memory subsystem 1040 on each backup operation. Moreover, in certain embodiments, the entire contents of the non-volatile memory subsystem 1040 are copied back into the volatile memory subsystem 1030 on each restore operation. In certain embodiments, the entire contents of the non-volatile memory subsystem 1040 are accessed for each backup and/or restore operation, such that the non-volatile memory subsystem 1040 (e.g., flash memory subsystem) is used generally uniformly across its memory space and wear-leveling is not performed by the memory system 1010. In certain embodiments, avoiding wear-leveling can decrease cost and complexity of the memory system 1010 and can improve the performance of the memory system 1010. In certain other embodiments, the entire contents of the volatile memory subsystem 1030 are not copied into the non-volatile memory subsystem 1040 on each backup operation, but only a partial copy is performed. In certain embodiments, other

management capabilities such as bad-block management and error management for the flash memory elements of the non-volatile memory subsystem 1040 are performed in the controller 1062.

[00141] The memory system 1010 generally operates as a write-back cache in certain embodiments. For example, in one embodiment, the host system (e.g., a disk controller) writes data to the volatile memory subsystem 1030 which then writes the data to non-volatile storage which is not part of the memory system 1010, such as, for example, a hard disk. The disk controller may wait for an acknowledgment signal from the memory system 1010 indicating that the data has been written to the hard disk or is otherwise secure. The memory system 1010 of certain embodiments can decrease delays in the system operation by indicating that the data has been written to the hard disk before it has actually done so. In certain embodiments, the memory system 1010 will still be able to recover the data efficiently in the event of a power outage because of the backup and restore capabilities described herein. In certain other embodiments, the memory system 1010 may be operated as a write-through cache or as some other type of cache.

[00142] FIG. 16 schematically illustrates an example power module 1100 of the memory system 1010 in accordance with certain embodiments described herein. The power module 1100 provides power to the various components of the memory system 1010 using different elements based on a state of the memory system 1010 in relation to a trigger condition. In certain embodiments, the power module 1100 comprises one or more of the components described above with respect to FIG. 12. For example, in certain embodiments, the power module 1100 includes the second power supply 1080 and the switch 1090.

[00143] The power module 1100 provides a plurality of voltages to the memory system 1010 comprising non-volatile and volatile memory subsystems 1030, 1040. The plurality of voltages comprises at least a first voltage 1102 and a second voltage 1104. The power module 1100 comprises an input 1106 providing a third voltage 1108 to the power module 1100 and a voltage conversion element 1120 configured to provide the second voltage 1104 to the memory system 1010. The power module 1100 further comprises a first power element 1130 configured to selectively provide a fourth voltage 1110 to the conversion element 1120. In certain embodiments, the first power element 1130 comprises a pulse-width modulation power controller. For example, in one example embodiment, the first power element 1130 is configured to receive a 1.8V input system voltage as the third voltage 1108 and to output a modulated 5V output as the fourth voltage 1110.

[00144] The power module 1100 further comprises a second power element 1140 can be configured to selectively provide a fifth voltage 1112 to the conversion element 1120. The power module 1100 can be configured to selectively provide the first voltage 1102 to the memory system 1010 either from the conversion element 1120 or from the input 1106.

[00145] The power module 1100 can be configured to be operated in at least three states in certain embodiments. In a first state, the first voltage 1102 is provided to the memory system 1010 from the input 1106 and the fourth voltage 1110 is provided to the conversion element 1120 from the first power element 1130. In a second state, the fourth voltage 1110 is provided to the conversion element 1120 from the first power element 1130 and the first voltage 1102 is provided to the memory system 1010 from the conversion element 1120. In the third state, the fifth voltage 1112 is provided to the conversion element 1120 from the second power element

1140 and the first voltage 1104 is provided to the memory system 1010 from the conversion element 1120.

[00146] In certain embodiments, the power module 1100 transitions from the first state to the second state upon detecting that a trigger condition is likely to occur and transitions from the second state to the third state upon detecting that the trigger condition has occurred. For example, the power module 1100 may transition to the second state when it detects that a power failure is about to occur and transitions to the third state when it detects that the power failure has occurred. In certain embodiments, providing the first voltage 1102 in the second state from the first power element 1130 rather than from the input 1106 allows a smoother transition from the first state to the third state. For example, in certain embodiments, providing the first voltage 1102 from the first power element 1130 has capacitive and other smoothing effects. In addition, switching the point of power transition to be between the conversion element 1120 and the first and second power elements 1130, 1140 (e.g., the sources of the pre-regulated fourth voltage 1110 in the second state and the pre-regulated fifth voltage 1112 in the third state) can smooth out potential voltage spikes.

[00147] In certain embodiments, the second power element 1140 does not comprise a battery and may comprise one or more capacitors. For example, as schematically illustrated in FIG. 16, the second power element 1140 comprises a capacitor array 1142, a buck-boost converter 1144 which adjusts the voltage for charging the capacitor array and a voltage/current limiter 1146 which limits the charge current to the capacitor array 1142 and stops charging the capacitor array 1142 when it has reached a certain charge voltage. In one example embodiment, the capacitor array 1142 comprises two 50 farad capacitors capable of holding a total charge of 4.6V. For

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example, in one example embodiment, the buck-boost converter 1144 receives a 1.8V system voltage (first voltage 1108) and boosts the voltage to 4.3V which is outputted to the voltage current limiter 1146. The voltage/current limiter 1146 limits the current going to the capacitor array 1142 to 1A and stops charging the array 1142 when it is charged to 4.3V. Although described with respect to certain example embodiments, one of ordinary skill will recognize from the disclosure herein that the second power element 1140 may include alternative embodiments. For example, different components and/or different value components may be used. For example, in other embodiments, a pure boost converter may be used instead of a buck-boost converter. In another embodiment, only one capacitor may be used instead of a capacitor array 1142.

[00148] The conversion element 1120 can comprise one or more buck converters and/or one or more buck-boost converters. The conversion element 1120 may comprise a plurality of sub-blocks 1122, 1124, 1126 as schematically illustrated by FIG. 16, which can provide more voltages in addition to the second voltage 1104 to the memory system 1010. The sub-blocks may comprise various converter circuits such as buck-converters, boost converters, and buck-boost converter circuits for providing various voltage values to the memory system 1010. For example, in one embodiment, sub-block 1122 comprises a buck converter, sub-block 1124 comprises a dual buck converter, and sub-block 1126 comprises a buck-boost converter as schematically illustrated by FIG. 16. Various other components for the sub-blocks 1122, 1124, 1126 of the conversion element 1120 are also compatible with certain embodiments described herein. In certain embodiments, the conversion element 1120 receives as input either the fourth voltage 1110 from the first power element 1130 or the fifth voltage 1112 from the second power element 1140, depending on the state of the power module 1100, and reduces the input to an appropriate

amount for powering various components of the memory system. For example, the buck-converter of sub-block 1122 can provide 1.8V at 2A for about 60 seconds to the volatile memory elements 1032 (e.g., DRAM), the non-volatile memory elements 1042 (e.g., flash), and the controller 1062 (e.g., an FPGA) in one embodiment. The sub-block 1124 can provide the second voltage 1104 as well as another reduced voltage 1105 to the memory system 1010. In one example embodiment, the second voltage 1104 is 2.5V and is used to power the at least one circuit 1052 (e.g., isolation device) and the other reduced voltage 1105 is 1.2V and is used to power the controller 1062 (e.g., FPGA). The subblock 1126 can provide yet another voltage 1107 to the memory system 1010. For example, the voltage 1107 may be 3.3V and may be used to power both the controller 1062 and the at least one circuit 1052.

[00149] Although described with respect to certain example embodiments, one of ordinary skill will recognize from the disclosure herein that the conversion element 1120 may include alternative embodiments. For example, there may be more or less sub-blocks which may comprise other types of converters (e.g., pure boost converters) or which may produce different voltage values. In one embodiment, the volatile memory elements 1032 and nonvolatile memory elements 1042 are powered using independent voltages and are not both powered using the first voltage 1102.

[00150] FIG. 17 is a flowchart of an example method 1200 of providing a first voltage 1102 and a second voltage 1104 to a memory system 1010 including volatile and nonvolatile memory subsystems 1030, 1040. While the method 1200 is described herein by reference to the memory system 1010 schematically illustrated by FIGS. 12-15, other memory systems are also compatible with embodiments of the method 1200. During a first condition, the method 1200

comprises providing the first voltage 1102 to the memory system 1010 from an input power supply 1106 and providing the second voltage 1104 to the memory system 1010 from a first power subsystem in operational block 1210. For example, in one embodiment, the first power subsystem comprises the first power element 1130 and the voltage conversion element 1120 described above with respect to FIG. 16. In other embodiments, other first power subsystems are used.

[00151] The method 1200 further comprises detecting a second condition in operational block 1220. In certain embodiments, detecting the second condition comprises detecting that a trigger condition is likely to occur. During the second condition, the method 1200 comprises providing the first voltage 1102 and the second voltage 1104 to the memory system 1010 from the first power subsystem in an operational block 1230. For example, referring to FIG. 16, a switch 1148 can be toggled to provide the first voltage 1102 from the conversion element 1120 rather than from the input power supply.

[00152] The method 1200 further comprises charging a second power subsystem in operational block 1240. In certain embodiments, the second power subsystem comprises the second power element 1140 or another power supply that does not comprise a battery. For example, in one embodiment, the second power subsystem comprises the second power element 1140 and the voltage conversion element 1120 described above with respect to FIG. 16. In other embodiments, some other second power subsystem is used.

[00153] The method 1200 further comprises detecting a third condition in an operational block 1250 and during the third condition, providing the first voltage 1102 and the second

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voltage 1104 to the memory system 1010 from the second power subsystem 1140 in an operational block 1260. In certain embodiments, detecting the third condition comprises detecting that the trigger condition has occurred. The trigger condition may comprise various conditions described herein. In various embodiments, for example, the trigger condition comprises a power reduction, power failure, or system hang-up. The operational blocks of the method 1200 may be performed in different orders in various embodiments. For example, in certain embodiments, the second power subsystem 1140 is charged before detecting the second condition.

[00154] In certain embodiments, the memory system 1010 comprises a volatile memory subsystem 1030 and a non-volatile memory subsystem 1040 comprising at least 100 percent more storage capacity than does the volatile memory subsystem. The memory system 1010 also comprises a controller 1062 operatively coupled to the volatile memory subsystem 1030 and operatively coupled to the non-volatile memory subsystem 1040. The controller 1062 can be configured to allow data to be communicated between the volatile memory subsystem 1030 and the host system when the memory system 1010 is operating in a first state and to allow data to be communicated between the volatile memory subsystem 1030 and the non-volatile memory subsystem 1040 when the memory system 1010 is operating in a second state.

[00155] Although the memory system 1010 having extra storage capacity of the non-volatile memory subsystem 1040 has been described with respect to certain embodiments, alternative configurations exist. For example, in certain embodiments, there may be more than 100 percent more storage capacity in the non-volatile memory subsystem 1040 than in the volatile memory subsystem 1030. In various embodiments, there may be at least 200, 300, or 400 percent more

storage capacity in the non-volatile memory subsystem 1040 than in the volatile memory subsystem 1030. In other embodiments, the non-volatile memory subsystem 1040 includes at least some other integer multiples of the storage capacity of the volatile memory subsystem 1030. In some embodiments, the non-volatile memory subsystem 1040 includes a non-integer multiple of the storage capacity of the volatile memory subsystem 1030. In one embodiment, the non-volatile memory subsystem 1040 includes less than 100 percent more storage capacity than does the volatile memory subsystem 1030.

[00156] The extra storage capacity of the non-volatile memory subsystem 1040 can be used to improve the backup capability of the memory system 1010. In certain embodiments in which data can only be written to portions of the non-volatile memory subsystem 1040 which do not contain data (e.g., portions which have been erased), the extra storage capacity of the nonvolatile memory subsystem 1040 allows the volatile memory subsystem 1030 to be backed up in the event of a subsequent power failure or other trigger event. For example, the extra storage capacity of the non-volatile memory subsystem 1040 may allow the memory system 1010 to backup the volatile memory subsystem 1030 efficiently in the event of multiple trigger conditions (e.g., power failures). In the event of a first power failure, for example, the data in the volatile memory system 1030 is copied to a first, previously erased portion of the nonvolatile memory subsystem 1040 via the controller 1062. Since the non-volatile memory subsystem 1040 has more storage capacity than does the volatile memory subsystem 1030, there is a second portion of the non-volatile memory subsystem 1040 which does not have data from the volatile memory subsystem 1030 copied to it and which remains free of data (e.g., erased). Once system power is restored, the controller 1062 of the memory system 1010 restores the data to the volatile memory subsystem 1030 by copying the backed-up data from the non-volatile memory

subsystem 1040 back to the volatile memory subsystem 1030. After the data is restored, the memory system 1010 erases the non-volatile memory subsystem 1040. While the first portion of the non-volatile memory subsystem 1040 is being erased, it may be temporarily unaccessible.

[00157] If a subsequent power failure occurs before the first portion of the non-volatile memory subsystem 1040 is completely erased, the volatile memory subsystem 1030 can be backed-up or stored again in the second portion of the non-volatile memory subsystem 1040 as described herein. In certain embodiments, the extra storage capacity of the non-volatile memory subsystem 1040 may allow the memory system 1010 to operate more efficiently. For example, because of the extra storage capacity of the non-volatile memory subsystem 1040, the memory system 1010 can handle a higher frequency of trigger events that is not limited by the erase time of the non-volatile memory subsystem 1040.

[00158] FIG. 18 is a flowchart of an example method 1300 of controlling a memory system 1010 operatively coupled to a host system and which includes a volatile memory subsystem 1030 and a non-volatile memory subsystem 1040. In certain embodiments, the non-volatile memory subsystem 1040 comprises at least 100 percent more storage capacity than does the volatile memory subsystem 30 as described herein. While the method 1300 is described herein by reference to the memory system 1010 schematically illustrated by FIGS. 12-14, the method 1300 can be practiced using other memory systems in accordance with certain embodiments described herein. In an operational block 1310, the method 1300 comprises communicating data between the volatile memory subsystem 1030 and the host system when the memory system 1010 is in a first mode of operation. The method 1300 further comprises storing a first copy of data from the

volatile memory subsystem 1030 to the non-volatile memory subsystem 1040 at a first time when the memory system 1010 is in a second mode of operation in an operational block 1320.

[00159] In an operational block 1330, the method 1300 comprises restoring the first copy of data from the non-volatile memory subsystem 1040 to the volatile memory subsystem 1030. The method 1300 further comprises erasing the first copy of data from the non-volatile memory subsystem 1040 in an operational block 1340. The method further comprises storing a second copy of data from the volatile memory subsystem 1030 to the non-volatile memory subsystem 1040 at a second time when the memory system 1010 is in the second mode of operation in an operational block 1350. Storing the second copy begins before the first copy is completely erased from the non-volatile memory subsystem 1040.

[00160] In some embodiments, the memory system 1010 enters the second mode of operation in response to a trigger condition, such as a power failure. In certain embodiments, the first copy of data and the second copy of data are stored in separate portions of the nonvolatile memory subsystem 1040. The method 1300 can also include restoring the second copy of data from the non-volatile memory subsystem 1040 to the volatile memory subsystem 1030 in an operational block 1360. The operational blocks of method 1300 referred to herein may be performed in different orders in various embodiments. For example, in some embodiments, the second copy of data is restored to the volatile memory subsystem 1030 at operational block 1360 before the first copy of data is completely erased in the operational block 1340.

[00161] FIG. 19 schematically illustrates an example clock distribution topology 1400 of a memory system 1010 in accordance with certain embodiments described herein. The clock

distribution topology 1400 generally illustrates the creation and routing of the clock signals provided to the various components of the memory system 1010. A clock source 1402 such as, for example, a 25 MHz oscillator, generates a clock signal. The clock source 1402 may feed a clock generator 1404 which provides a clock signal 1406 to the controller 1062, which may be an FPGA. In one embodiment, the clock generator 1404 generates a 125 MHz clock signal 1406. The controller 1062 receives the clock signal 1406 and uses it to clock the controller 1062 master state control logic. For example, the master state control logic may control the general operation of an FPGA controller 1062.

[00162] The clock signal 1406 can also be input into a clock divider 1410 which produces a frequency-divided version of the clock signal 1406. In an example embodiment, the clock divider 1410 is a divide by two clock divider and produces a 62.5 MHz clock signal in response to the 125 MHz clock signal 1406. A non-volatile memory phase-locked loop (PLL) block 1412 can be included (e.g., in the controller 1062) which distributes a series of clock signals to the non-volatile memory subsystem 1040 and to associated control logic. For example, a series of clock signals 1414 can be sent from the controller 1062 to the non-volatile memory subsystem 1040. Another clock signal 1416 can be used by the controller logic which is dedicated to controlling the non-volatile memory subsystem 1040. For example, the clock signal 1416 may clock the portion of the controller 1062 which is dedicated to generating address and/or control lines for the non-volatile memory subsystem 1040. A feedback clock signal 1418 is fed back into the non-volatile memory PLL block 1412. In one embodiment, the PLL block 1412 compares the feedback clock 1418 to the reference clock 1411 and varies the phase and frequency of its output until the reference 1411 and feedback 1418 clocks are phase and frequency matched.

[00163] A version of the clock signal 1406 such as the backup clock signal 1408 may be sent from the controller to the volatile memory subsystem 1030. The clock signal 1408 may be, for example, a differential version of the clock signal 1406. As described herein, the backup clock signal 1408 may be used to clock the volatile memory subsystem 1030 when the memory system 1010 is backing up the data from the volatile memory subsystem 1030 into the non-volatile memory subsystem 1040. In certain embodiments, the backup clock signal 1408 may also be used to clock the volatile memory subsystem 1030 when the memory system 1010 is copying the backed-up data back into the volatile memory subsystem 1030 from the nonvolatile memory subsystem 1040 (also referred to as restoring the volatile memory subsystem 1030). The volatile memory subsystem 1030 may normally be run at a higher frequency (e.g., DRAM running at 400MHz) than the nonvolatile memory subsystem 1040 (e.g., flash memory running at 62.5MHz) when communicating with the host system (e.g., when no trigger condition is present). However, in certain embodiments the volatile memory subsystem 1030 may be operated at a reduced frequency (e.g., at twice the frequency of the non-volatile memory subsystem 1040) without introducing significant delay into the system during backup operation and/or restore operations. Running the volatile memory subsystem 1030 at the reduced frequency during a backup and/or restore operation may advantageously reduce overall power consumption of the memory system 1010.

[00164] In one embodiment, the backup clock 1408 and the volatile memory system clock signal 1420 are received by a multiplexer 1422, as schematically illustrated by FIG. 19. The multiplexer 1422 can output either the volatile memory system clock signal 1420 or the backup clock signal 1408 depending on the backup state of the memory system 1010. For example, when the memory system 1010 is not performing a backup or restore operation and is

communicating with the host system (e.g., normal operation), the volatile memory system clock signal 1420 may be provided by the multiplexer 422 to the volatile memory PLL block 1424. When the memory system 1010 is performing a backup (or restore) operation, the backup clock signal 1408 may be provided.

[00165] The volatile memory PLL block 1424 receives the volatile memory reference clock signal 1423 from the multiplexer 1422 and can generate a series of clock signals which are distributed to the volatile memory subsystem 1030 and associated control logic. For example, in one embodiment, the PLL block 1424 generates a series of clock signals 1426 which clock the volatile memory elements 1032. A clock signal 1428 may be used to clock control logic associated with the volatile memory elements, such as one or more registers (e.g., the one or more registers of a registered DIMM). Another clock signal 1430 may be sent to the controller 1062. A feedback clock signal 1432 is fed back into the volatile memory PLL block 1424. In one embodiment, the PLL block 1424 compares the feedback clock signal 1432 to the reference clock signal 1423 and varies the phase and frequency of its output until the reference clock signal 1423 and the feedback clock signal 1432 clocks are phase and frequency matched.

[00166] The clock signal 1430 may be used by the controller 1062 to generate and distribute clock signals which will be used by controller logic which is configured to control the volatile memory subsystem 1030. For example, control logic in the controller 1062 may be used to control the volatile memory subsystem 1030 during a backup or restore operation. The clock signal 1430 may be used as a reference clock signal for the PLL block 1434 which can generate one or more clocks 1438 used by logic in the controller 1062. For example, the PLL block 1434 may generate one or more clock signals 1438 used to drive logic circuitry associated with

controlling the volatile memory subsystem 1030. In certain embodiments, the PLL block 1434 includes a feedback clock signal 1436 and operates in a similar manner to other PLL blocks described herein.

[00167] The clock signal 1430 may be used as a reference clock signal for the PLL block 1440 which may generate one or more clock signals used by a sub-block 1442 to generate one or more other clock signals 1444. In one embodiment, for example, the volatile memory subsystem 1030 comprises DDR2 SDRAM elements and the sub-block 1442 generates one or more DDR2 compatible clock signals 1444. A feedback clock signal 1446 is fed back into the PLL block 1440. In certain embodiments, the PLL block 1440 operates in a similar manner to other PLL blocks described herein.

[00168] While described with respect to the example embodiment of FIG. 19, various alternative clock distribution topologies are possible. For example, one or more of the clock signals have a different frequency in various other embodiments. In some embodiments, one or more of the clocks shown as differential signals are single ended signals. In one embodiment, the volatile memory subsystem 1030 operates on the volatile memory clock signal 1420 and there is no backup clock signal 1408. In some embodiments, the volatile memory subsystem 1030 is operated at a reduced frequency during a backup operation and not during a restore operation. In other embodiments, the volatile memory subsystem 1030 is operated at a reduced frequency during a restore operation and not during a backup operation.

[00169] FIG. 20 is a flowchart of an example method 1500 of controlling a memory system 1010 operatively coupled to a host system. Although described with respect to the memory

system 1010 described herein, the method 1500 is compatible with other memory systems. The memory system 1010 may include a clock distribution topology 1400 similar to the one described above with respect to FIG. 19 or another clock distribution topology. The memory system 1010 can include a volatile memory subsystem 1030 and a non-volatile memory subsystem 1040.

[00170] In an operational block 1510, the method 1500 comprises operating the volatile memory subsystem 1030 at a first frequency when the memory system 1010 is in a first mode of operation in which data is communicated between the volatile memory subsystem 1030 and the host system. In an operational block 1520, the method 1500 comprises operating the non-volatile memory subsystem 1040 at a second frequency when the memory system 1010 is in a second mode of operation in which data is communicated between the volatile memory subsystem 1030 and the non-volatile memory subsystem 1040. The method 1500 further comprises operating the volatile memory subsystem 1030 at a third frequency in an operational block 1530 when the memory system 1010 is in the second mode of operation. In certain embodiments, the memory system 1010 is not powered by a battery when it is in the second mode of operation. The memory system 1010 may switch from the first mode of operation to the second mode of operation in response to a trigger condition. The trigger condition may be any trigger condition described herein such as, for example, a power failure condition. In certain embodiments, the second mode of operation includes both backup and restore operations as described herein. In other embodiments, the second mode of operation includes backup operations but not restore operations. In yet other embodiments, the second mode of operation includes restore operations but not backup operations.

[00171] The third frequency can be less than the first frequency. For example, the third frequency can be approximately equal to the second frequency. In certain embodiments, the reduced frequency operation is an optional mode. In yet other embodiments, the first, second and/or third frequencies are configurable by a user or by the memory system 1010.

[00172] FIG. 21 schematically illustrates an example topology of a connection to transfer data slices from two DRAM segments 1630, 1640 of a volatile memory subsystem 1030 of a memory system 1010 to a controller 1062 of the memory system 1010. While the example of FIG. 21 shows a topology including two DRAM segments 1630, 1640 for the purposes of illustration, each address location of the volatile memory subsystem 1030 comprises more than the two segments in certain embodiments. The data lines 1632, 1642 from the first DRAM segment 1630 and the second DRAM segment 1640 of the volatile memory subsystem 1030 are coupled to switches 1650, 1652 which are coupled to the controller 1062 (e.g., logic element 1070) of the memory system 1010. The chip select lines 1634, 1644 and the self-refresh lines 1636, 1646 (e.g., CKe signals) of the first and second DRAM segments 1630, 1640, respectively, are coupled to the controller 1062. In certain embodiments, the controller 1062 comprises a buffer (not shown) which is configured to store data from the volatile memory subsystem 1030. In certain embodiments, the buffer is a first-in, first out buffer (FIFO). In certain embodiments, data slices from each DRAM segment 1630, 1640 comprise a portion of the volatile memory subsystem data bus. In one embodiment, for example, the volatile memory subsystem 1030 comprises a 72-bit data bus (e.g., each data word at each addressable location is 72 bits wide and includes, for example, 64 bits of accessible SDRAM and 8 bits of ECC), the first data slice from the first DRAM segment 1630 may comprise 40 bits of the data word, and the second data slice

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from the second DRAM segment 1640 may comprise the remaining 32 bits of the data word. Certain other embodiments comprise data buses and/or data slices of different sizes.

[00173] In certain embodiments, the switches 1650, 1652 can each be selectively switched to selectively operatively couple the data lines 1632, 1642, respectively from the first and second DRAM segments 1630, 1640 to the controller 1062. The chip select lines 1634, 1644 enable the first and second DRAM segments 1630, 1640, respectively, of the volatile memory subsystem 1030, and the self-refresh lines 1636, 1646 toggle the first and second DRAM segments 1630, 1640, respectively, from self-refresh mode to active mode. In certain embodiments, the first and second DRAM segments 1630, 1640 maintain stored information but are not accessible when they are in self-refresh mode, and maintain stored information and are accessible when they are in active mode.

[00174] In certain embodiments, when the memory system 1010 is backing up the volatile memory system 1030, data slices from only one of the two DRAM segments 1630, 1640 at a time are sent to the controller 1062. For example, when the first slice is being written to the controller 1062 during a back-up, the controller 1062 sends a signal via the CKe line 1636 to the first DRAM segment 1630 to put the first DRAM segment 1630 in active mode. In certain embodiments, the data slice from the first DRAM segment 1630 for multiple words (e.g., a block of words) is written to the controller 1062 before writing the second data slice from the second DRAM segment 1640 to the controller 1062. While the first data slice is being written to the controller 1062, the controller 1062 also sends a signal via the CKe line 1646 to put the second DRAM segment 1640 in self-refresh mode. Once the first data slice for one word or for a block of words is written to the controller 1062, the controller 1062 puts the first DRAM segment 1630

into self-refresh mode by sending a signal via the CKe line 1636 to the first DRAM segment 1640. The controller 1062 also puts the second DRAM segment 1640 into active mode by sending a signal via the CKe line 1646 to the DRAM segment 1640. The second slice for a word or for a block of words is written to the controller 1062. In certain embodiments, when the first and second data slices are written to the buffer in the controller 1062, the controller 1062 combines the first and second data slices 1630, 1640 into complete words or blocks of words and then writes each complete word or block of words to the non-volatile memory subsystem 1040. In certain embodiments, this process is called "slicing" the volatile memory subsystem 1030.

[00175] In certain embodiments, the data may be sliced in a restore operation as well as, or instead of, during a backup operation. For example, in one embodiment, the nonvolatile memory elements 1042 write each backed-up data word to the controller 1062 which writes a first slice of the data word to the volatile memory subsystem 1030 and then a second slice of the data word to the volatile memory subsystem 1030. In certain embodiments, slicing the volatile memory subsystem 1030 during a restore operation may be performed in a manner generally inverse to slicing the volatile memory subsystem 1030 during a backup operation.

[00176] FIG. 22 is a flowchart of an example method 1600 of controlling a memory system 1010 operatively coupled to a host system and which includes a volatile memory subsystem 1030 and a non-volatile memory subsystem 1040. Although described with respect to the memory system 1010 described herein with respect to FIGS. 12-14 and 21, the method 1600 is compatible with other memory systems. The method 1600 comprises communicating data words between the volatile memory subsystem 1030 and the host system when the memory system 1010 is in a first mode of operation in an operational block 1610. For example, the memory

system 1010 may be in the first mode of operation when no trigger condition has occurred and the memory system is not performing a backup and/or restore operation or is not being powered by a secondary power supply.

[00177] In an operational block 1620, the method further comprises transferring data words from the volatile memory subsystem 1030 to the non-volatile memory subsystem 1040 when the memory system 1010 is in a second mode of operation. In certain embodiments, each data word comprises the data stored in a particular address of the memory system 1010. The memory system 1010 may enter the second mode of operation, for example, when a trigger condition (e.g., a power failure) occurs. In certain embodiments, transferring each data word comprises storing a first portion (also referred to as a slice) of the data word in a buffer in an operational block 1622, storing a second portion of the data word in the buffer in an operational block 1624, and writing the entire data word from the buffer to the non-volatile memory subsystem 1040 in an operational block 1626.

[00178] In one example embodiment, the data word may be a 72 bit data word (e.g., 64 bits of accessible SDRAM and 8 bits of ECC), the first portion (or "slice") may comprise 40 bits of the data word, and the second portion (or "slice") may comprise the remaining 32 bits of the data word. In certain embodiments, the buffer is included in the controller 1062. For example, in one embodiment, the buffer is a first-in, first-out buffer implemented in the controller 1062 which comprises an FPGA. The method 1600 may generally be referred to as "slicing" the volatile memory during a backup operation. In the example embodiment, the process of "slicing" the volatile memory during a backup includes bringing the 32-bit slice out of self-refresh, reading a 32-bit block from the slice into the buffer, and putting the 32-bit slice back into self-refresh. The

40-bit slice is then brought out of self-refresh and a 40-bit block from the slice is read into a buffer. Each block may comprise a portion of multiple words. For example, each 32-bit block may comprise 32-bit portions of multiple 72-bit words. In other embodiments, each block comprises a portion of a single word. The 40-bit slice is then put back into self-refresh in the example embodiment. The 32-bit and 40-bit slices are then combined into a 72-bit block by the controller 1062 and ECC detection/correction is performed on each 72-bit word as it is read from the buffer and written into the non-volatile memory subsystem (e.g., flash).

[00179] In some embodiments, the entire data word may comprise more than two portions. For example, the entire data word may comprise three portions instead of two and transferring each data word further comprises storing a third portion of each data word in the buffer. In certain other embodiments, the data word may comprise more than three portions.

[00180] In certain embodiments, the data may be sliced in a restore operation as well as, or instead of, during a backup operation. For example, in one embodiment, the nonvolatile memory elements 1040 write each backed-up data word to the controller 1062 which writes a first portion of the data word to the volatile memory subsystem 1030 and then a second portion of the data word to the volatile memory 1030. In certain embodiments, slicing the volatile memory subsystem 1030 during a restore operation may be performed in a manner generally inverse to slicing the volatile memory subsystem 1030 during a backup operation.

[00181] The method 1600 can advantageously provide significant power savings and can lead to other advantages. For example, in one embodiment where the volatile memory subsystem 1030 comprises DRAM elements, only the slice of the DRAM which is currently being accessed

(e.g., written to the buffer) during a backup is configured in full-operational mode. The slice or slices that are not being accessed may be put in self-refresh mode. Because DRAM in self-refresh mode uses significantly less power than DRAM in full-operational mode, the method 1600 can allow significant power savings. In certain embodiments, each slice of the DRAM includes a separate self-refresh enable (e.g., CKe) signal which allows each slice to be accessed independently.

[00182] In addition, the connection between the DRAM elements and the controller 1062 may be as large as the largest slice instead of as large as the data bus. In the example embodiment, the connection between the controller 1062 and the DRAM may be 40 bits instead of 72 bits. As a result, pins on the controller 1062 may be used for other purposes or a smaller controller may be used due to the relatively low number of pin-outs used to connect to the volatile memory subsystem 1030. In certain other embodiments, the full width of the data bus is connected between the volatile memory subsystem 1030 and the controller 1062 but only a portion of it is used during slicing operations. For example, in some embodiments, memory slicing is an optional mode.

[00183] While embodiments and applications have been shown and described, it would be apparent to those skilled in the art having the benefit of this disclosure that many more modifications than mentioned above are possible without departing from the inventive concepts disclosed herein. The invention, therefore, is not to be restricted except in the spirit of the appended claims.

CLAIMS

What is claimed is:

1. A memory module comprising:

a printed circuit board (PCB) having an interface configured to fit into a corresponding slot connector of a host system, the interface including a plurality of edge connections configured to couple power, data, address and control signals between the memory module and the host system;

a first buck converter configured to provide a first regulated voltage having a first voltage amplitude;

a second buck converter configured to provide a second regulated voltage having a second voltage amplitude;

a third buck converter configured to provide a third regulated voltage having a third voltage amplitude;

a converter circuit configured to provide a fourth regulated voltage having a fourth voltage amplitude; and

a plurality of components coupled to the PCB, each component of the plurality of components coupled to one or more regulated voltages of the first, second, third and fourth regulated voltages, the plurality of components comprising:

a plurality of synchronous dynamic random access memory (SDRAM) devices coupled to the first regulated voltage, and

at least one circuit coupled between a first portion of the plurality of edge connections and the plurality of SDRAM devices, the at least one circuit operable to (i) receive a first plurality of address and control signals via the first portion of the plurality of edge connections, and (ii) output a second plurality of address and control signals to the plurality of SDRAM devices, the at least one circuit coupled to both the second regulated voltage and the fourth regulated voltage, wherein one of the second and fourth voltage amplitudes is less than the other one of the second and fourth voltage amplitudes.

2. The memory module of claim 1, wherein the first and third buck converters are further configured to operate as a dual buck converter.

3. The memory module of claim 1, wherein the first voltage amplitude is 1.8 volts.

4. The memory module of claim 1, wherein the second, third, and fourth voltage amplitudes are 2.5 volts, 1.2 volts, and 3.3 volts, respectively.

5. The memory module of claim 1, further comprising:

a voltage monitor circuit configured to monitor a power input voltage received via a second portion of the plurality of edge connections, the voltage monitor circuit configured to produce a trigger signal in response to the power input voltage having a voltage amplitude that is greater than a first threshold voltage.

6. The memory module of claim 1, the plurality of components further comprising:

one or more registers coupled to one of the first, second, third and fourth regulated voltages, the one or more registers configured to register, in response to a clock, the first plurality of address and control signals, wherein the one of the first, second, third and fourth regulated voltages is selectively switched off to turn power off to the one or more registers while one or more components of the plurality of components are powered on.

7. The memory module of claim 5, wherein the voltage monitor circuit is further configured to produce the trigger signal in response to the power input voltage having a voltage amplitude that is less than a second threshold voltage.

8. The memory module of claim 6, wherein, in response to selectively switching on the one of the first, second, third and fourth regulated voltages to the one or more registers, the one or more registers is configured to output the registered first plurality of address and control signals to the plurality of SDRAM devices.

9. The memory module of claim 5, wherein the power input voltage is coupled to the first, second, and third buck converters and the converter circuit.

10. The memory module of claim 5, wherein the first threshold voltage corresponds to a voltage level that is ten percent greater than a specified operating voltage.

11. The memory module of claim 7, wherein the second threshold voltage corresponds to a voltage level that is ten percent less than a specified operating voltage.

12. The memory module of claim 5, the plurality of components further comprising:

a logic element including a non-volatile memory, the non-volatile memory is configured to store configuration information.

13. The memory module of claim 12, wherein, in response to the trigger signal, the logic element writes information into the non-volatile memory.

14. The memory module of claim 1, the plurality of components further comprising:

a logic element including one or more integrated circuits and discrete electrical elements, the one or more integrated circuit including an internal non-volatile memory, wherein the non-volatile memory is configured to store configuration information.

15. The memory module of claim 5, the plurality of components further comprising:

a non-volatile memory; and

a controller configured to receive the trigger signal, wherein, in response to the trigger signal, the controller performs a write operation to the non-volatile memory.

16. A memory module comprising:

a printed circuit board (PCB) having an interface configured to fit into a corresponding slot connector of a host system, the interface including a plurality of edge connections configured to couple power, data, address and control signals between the memory module and the host system;

first, second, and third buck converters configured to receive a pre-regulated input voltage and to produce first, second and third regulated voltages, respectively;

a converter circuit configured to reduce the pre-regulated input voltage to provide a fourth regulated voltage, wherein the first, second, third and fourth regulated voltages have first, second, third, and fourth voltage amplitudes, respectively;

a plurality of components coupled to the PCB, the plurality of components including a plurality of synchronous dynamic random access memory (SDRAM) devices, each component of the plurality of components coupled to one or more regulated voltages of the first, second, third and fourth regulated voltages; and

a voltage monitor circuit configured to monitor an input voltage received via a first portion of the plurality of edge connections, the voltage monitor circuit configured to produce a signal in response to the input voltage having a voltage amplitude that is greater than a first threshold voltage.

17. The memory module of claim 16, wherein the second and third buck converters are configured to operate as a dual buck converter.

18. The memory module of claim 16, the plurality of components further including:

a controller coupled to the voltage monitor circuit and configured to receive the signal, wherein the controller executes a write operation in response to the signal.

19. The memory module of claim 18, wherein the write operation includes writing data information into non-volatile memory.

20. The memory module of claim 16, wherein the plurality of SDRAM devices are configured to receive at least one of the first, second, third and fourth regulated voltages having a voltage amplitude of 1.8 volts.

21. The memory module of claim 16, the plurality of components further including:

at least one circuit coupled between the interface and the plurality of SDRAM devices, the at least one circuit operable to receive a first plurality of address and control signals via a second portion of the plurality of edge connections and to output a second plurality of address and control signals to the plurality of SDRAM devices, the at least one circuit coupled to both

the second regulated voltage and the fourth regulated voltage, wherein one of the second and fourth voltage amplitudes is less than the other one of the second and fourth voltage amplitudes.

22. The memory module of claim 16, the plurality of components further including:

a logic element including an internal non-volatile memory, wherein the non-volatile memory is configured to store configuration information, wherein the configuration information is used to program the logic element.

23. A memory module comprising:

a printed circuit board (PCB) having an interface configured to fit into a corresponding slot connector of a host system, the interface including a plurality of edge connections configured to couple power, data, address and control signals between the memory module and the host system;

a plurality of components coupled to the PCB, each component of the plurality of components coupled to one or more regulated voltages of first, second, third and fourth regulated voltages, the plurality of components including a plurality of synchronous dynamic random access memory (SDRAM) devices and one or more registers, the plurality of SDRAM devices coupled to the first regulated voltage, the one or more registers coupled to (i) the second regulated voltage, (ii) a portion of the plurality of edge connections, and (iii) the plurality of SDRAM devices, wherein a plurality of address and control signals are coupled to the one or more registers via the portion of the plurality of edge connections;

first, second, and third buck converters configured to provide the first, second and third regulated voltages, respectively; and

a converter circuit configured to provide the fourth regulated voltage,

wherein the second regulated voltage is configured to be selectively switched on or off to the one or more registers while at least the plurality of SDRAM devices are powered on,

wherein if the second regulated voltage is switched on while at least the plurality of SDRAM devices are powered on, the one or more registers are configured to couple the first plurality of address and control signals to the plurality of SDRAM devices, and

wherein if the second regulated voltage is switched off while the plurality of SDRAM devices are powered on, the one or more registers are configured to decouple the plurality of SDRAM devices from the first plurality of address and control signals.

24. The memory module of claim 23, further comprising:

a voltage monitor circuit configured to monitor an input voltage received from the host system via the interface, the voltage monitor circuit configured to produce a signal in response to the input voltage having a voltage amplitude that is greater than a first threshold voltage.

25. The memory module of claim 24, wherein the voltage monitor circuit is further configured to produce the signal in response to the input voltage having a voltage amplitude that is less than a second threshold voltage.

26. The memory module of claim 23, wherein the second and third buck converters are configured to operate as a dual buck converter.

27. The memory module of claim 24, the plurality of components further including:

a controller coupled to the voltage monitor circuit and configured to receive the signal, wherein, in response to the signal, the controller executes a write operation.

28. The memory module of claim 27, wherein the write operation includes writing data information to non-volatile memory.

29. The memory module of claim 23, wherein the plurality of SDRAM devices are configured to receive at least one of the first, second, third and fourth regulated voltages having a voltage amplitude of 1.8 volts.

30. The memory module of claim 23, wherein the first, second, and third buck converters are configured to receive a pre-regulated input voltage and to provide the first, second and third

regulated voltages, respectively, and wherein the converter circuit is configured to reduce the pre-regulated voltage input to provide the fourth regulated voltage.

Petitioners
Ex. 1002, p. 110

ABSTRACT

In certain embodiments, a memory module includes a printed circuit board (PCB) having an interface that couples it to a host system for provision of power, data, address and control signals. First, second, and third buck converters receive a pre-regulated input voltage and produce first, second and third regulated voltages. A converter circuit reduces the pre-regulated input voltage to provide a fourth regulated voltage. Synchronous dynamic random access memory (SDRAM) devices are coupled to one or more regulated voltages of the first, second, third and fourth regulated voltages, and a voltage monitor circuit monitors an input voltage and produces a signal in response to the input voltage having a voltage amplitude that is greater than a threshold voltage.

Petitioners
Ex. 1002, p. 111

Doc Code: TRACK1.REQ
Document Description: TrackOne Request

PTO/AIA/424 (04-14)

CERTIFICATION AND REQUEST FOR PRIORITIZED EXAMINATION UNDER 37 CFR 1.102(e) (Page 1 of 1)

First Named Inventor:	Hyun Lee	Nonprovisional Application Number (if known):	
Title of Invention:	FLASH-DRAM HYBRID MEMORY MODULE		

APPLICANT HEREBY CERTIFIES THE FOLLOWING AND REQUESTS PRIORITIZED EXAMINATION FOR THE ABOVE-IDENTIFIED APPLICATION.

1. The processing fee set forth in 37 CFR 1.17(i)(1) and the prioritized examination fee set forth in 37 CFR 1.17(c) have been filed with the request. The publication fee requirement is met because that fee, set forth in 37 CFR 1.18(d), is currently $0. The basic filing fee, search fee, and examination fee are filed with the request or have been already been paid. I understand that any required excess claims fees or application size fee must be paid for the application.

2. I understand that the application may not contain, or be amended to contain, more than four independent claims, more than thirty total claims, or any multiple dependent claims, and that any request for an extension of time will cause an outstanding Track I request to be dismissed.

3. The applicable box is checked below:

I. ☑ **Original Application (Track One) - Prioritized Examination under § 1.102(e)(1)**

i. (a) The application is an original nonprovisional utility application filed under 35 U.S.C. 111(a). This certification and request is being filed with the utility application via EFS-Web.

---OR---

(b) The application is an original nonprovisional plant application filed under 35 U.S.C. 111(a). This certification and request is being filed with the plant application in paper.

ii. An executed inventor's oath or declaration under 37 CFR 1.63 or 37 CFR 1.64 for each inventor, **or** the application data sheet meeting the conditions specified in 37 CFR 1.53(f)(3)(i) is filed with the application.

II. ☐ **Request for Continued Examination - Prioritized Examination under § 1.102(e)(2)**

i. A request for continued examination has been filed with, or prior to, this form.
ii. If the application is a utility application, this certification and request is being filed via EFS-Web.
iii. The application is an original nonprovisional utility application filed under 35 U.S.C. 111(a), or is a national stage entry under 35 U.S.C. 371.
iv. This certification and request is being filed prior to the mailing of a first Office action responsive to the request for continued examination.
v. No prior request for continued examination has been granted prioritized examination status under 37 CFR 1.102(e)(2).

Signature /Khaled Shami/	Date Dec. 30, 2020
Name (Print/Typed) Khaled Shami	Practitioner Registration Number 38,745

Note: *This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4(d) for signature requirements and certifications. Submit multiple forms if more than one signature is required.**

☐ *Total of _____ forms are submitted.

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8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	0016.001000H
	Application Number	
Title of Invention	FLASH-DRAM HYBRID MEMORY MODULE	

The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76.
This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.

Secrecy Order 37 CFR 5.2:

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	0016.001000H
	Application Number	
Title of Invention	FLASH-DRAM HYBRID MEMORY MODULE	

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	0016.001000H
	Application Number	
Title of Invention	FLASH-DRAM HYBRID MEMORY MODULE	

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Customer Number	151145		
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Application Information:

Title of the Invention	FLASH-DRAM HYBRID MEMORY MODULE		
Attorney Docket Number	0016.001000H	**Small Entity Status Claimed**	☐
Application Type			
Subject Matter			
Total Number of Drawing Sheets (if any)	22	**Suggested Figure for Publication (if any)**	

Filing By Reference:

Only complete this section when filing an application by reference under 35 U.S.C. 111(c) and 37 CFR 1.57(a). Do not complete this section if application papers including a specification and any drawings are being filed. Any domestic benefit or foreign priority information must be provided in the appropriate section(s) below (i.e., "Domestic Benefit/National Stage Information" and "Foreign Priority Information").

For the purposes of a filing date under 37 CFR 1.53(b), the description and any drawings of the present application are replaced by this reference to the previously filed application, subject to conditions and requirements of 37 CFR 1.57(a).

Application number of the previously filed application	Filing date (YYYY-MM-DD)	Intellectual Property Authority or Country

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

☐ **Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	0016.001000H
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When referring to the current application, please leave the "Application Number" field blank.

Prior Application Status	Pending		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
	Continuation of	15934416	2018-03-23

Prior Application Status	Patented				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
15934416	Continuation of	14840865	2015-08-31	9928186	2018-03-27

Prior Application Status	Patented				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
14840865	Continuation of	14489269	2014-09-17	9158684	2015-10-13

Prior Application Status	Patented				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
14489269	Continuation of	13559476	2012-07-26	8874831	2014-10-28

Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
13559476	Claims benefit of provisional	61512871	2011-07-28

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	0016.001000H
	Application Number	
Title of Invention	FLASH-DRAM HYBRID MEMORY MODULE	

Prior Application Status	Patented			Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
13559476	Continuation in part of	12240916	2008-09-29	8301833	2012-10-30

Prior Application Status	Abandoned		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
12240916	Continuation of	12131873	2008-06-02

Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
12131873	Claims benefit of provisional	60941586	2007-06-01

Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the **Add** button.

Foreign Priority Information:

This section allows for the applicant to claim priority to a foreign application. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55. When priority is claimed to a foreign application that is eligible for retrieval under the priority document exchange program (PDX) the information will be used by the Office to automatically attempt retrieval pursuant to 37 CFR 1.55(i)(1) and (2). Under the PDX program, applicant bears the ultimate responsibility for ensuring that a copy of the foreign application is received by the Office from the participating foreign intellectual property office, or a certified copy of the foreign priority application is filed, within the time period specified in 37 CFR 1.55(g)(1).

Application Number	Country	Filing Date (YYYY-MM-DD)	Access Code (if applicable)

Additional Foreign Priority Data may be generated within this form by selecting the **Add** button.

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications

☐ This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013.
NOTE: By providing this statement under 37 CFR 1.55 or 1.78, this application, with a filing date on or after March 16, 2013, will be examined under the first inventor to file provisions of the AIA.

PTO/AIA/14 (08-15)
Approved for use through 04/30/2017. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	0016.001000H
		Application Number	
Title of Invention	FLASH-DRAM HYBRID MEMORY MODULE		

Authorization or Opt-Out of Authorization to Permit Access:

When this Application Data Sheet is properly signed and filed with the application, applicant has provided written authority to permit a participating foreign intellectual property (IP) office access to the instant application-as-filed (see paragraph A in subsection 1 below) and the European Patent Office (EPO) access to any search results from the instant application (see paragraph B in subsection 1 below).

Should applicant choose not to provide an authorization identified in subsection 1 below, applicant **must opt-out** of the authorization by checking the corresponding box A or B or both in subsection 2 below.

NOTE: This section of the Application Data Sheet is **ONLY** reviewed and processed with the **INITIAL** filing of an application. After the initial filing of an application, an Application Data Sheet cannot be used to provide or rescind authorization for access by a foreign IP office(s). Instead, Form PTO/SB/39 or PTO/SB/69 must be used as appropriate.

1. Authorization to Permit Access by a Foreign Intellectual Property Office(s)

A. Priority Document Exchange (PDX) - Unless box A in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the State Intellectual Property Office of the People's Republic of China (SIPO), the World Intellectual Property Organization (WIPO), and any other foreign intellectual property office participating with the USPTO in a bilateral or multilateral priority document exchange agreement in which a foreign application claiming priority to the instant patent application is filed, access to: (1) the instant patent application-as-filed and its related bibliographic data, (2) any foreign or domestic application to which priority or benefit is claimed by the instant application and its related bibliographic data, and (3) the date of filing of this Authorization. See 37 CFR 1.14(h)(1).

B. Search Results from U.S. Application to EPO - Unless box B in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the EPO access to the bibliographic data and search results from the instant patent application when a European patent application claiming priority to the instant patent application is filed. See 37 CFR 1.14(h)(2).

The applicant is reminded that the EPO's Rule 141(1) EPC (European Patent Convention) requires applicants to submit a copy of search results from the instant application without delay in a European patent application that claims priority to the instant application.

2. Opt-Out of Authorizations to Permit Access by a Foreign Intellectual Property Office(s)

☐ A. Applicant **DOES NOT** authorize the USPTO to permit a participating foreign IP office access to the instant application-as-filed. If this box is checked, the USPTO will not be providing a participating foreign IP office with any documents and information identified in subsection 1A above.

☐ B. Applicant **DOES NOT** authorize the USPTO to transmit to the EPO any search results from the instant patent application. If this box is checked, the USPTO will not be providing the EPO with search results from the instant application.

NOTE: Once the application has published or is otherwise publicly available, the USPTO may provide access to the application in accordance with 37 CFR 1.14.

PTO/AIA/14 (08-15)
Approved for use through 04/30/2017. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	0016.001000H
	Application Number	
Title of Invention	FLASH-DRAM HYBRID MEMORY MODULE	

Applicant Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Applicant 1

If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section.

Clear

◉ Assignee	○ Legal Representative under 35 U.S.C. 117	○ Joint Inventor
○ Person to whom the inventor is obligated to assign.	○ Person who shows sufficient proprietary interest	

If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:

Name of the Deceased or Legally Incapacitated Inventor:	

If the Applicant is an Organization check here. ☒

Organization Name	Netlist, Inc.		
Mailing Address Information For Applicant:			
Address 1	175 Technology Drive		
Address 2	Suite 150		
City	Irvine	**State/Province**	CA
Country[i]	US	Postal Code	92618
Phone Number		Fax Number	
Email Address			

Additional Applicant Data may be generated within this form by selecting the Add button.

PTO/AIA/14 (08-15)
Approved for use through 04/30/2017. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	0016.001000H
	Application Number	
Title of Invention	FLASH-DRAM HYBRID MEMORY MODULE	

Assignee Information including Non-Applicant Assignee Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Assignee 1

Complete this section if assignee information, including non-applicant assignee information, is desired to be included on the patent application publication. An assignee-applicant identified in the "Applicant Information" section will appear on the patent application publication as an applicant. For an assignee-applicant, complete this section only if identification as an assignee is also desired on the patent application publication.

If the Assignee or Non-Applicant Assignee is an Organization check here. ☒

Organization Name	Netlist, Inc.

Mailing Address Information For Assignee including Non-Applicant Assignee:

Address 1	175 Technology Drive		
Address 2	Suite 150		
City	Irvine	**State/Province**	CA
Country i	US	Postal Code	92618
Phone Number		Fax Number	
Email Address			

Additional Assignee or Non-Applicant Assignee Data may be generated within this form by selecting the Add button.

PTO/AIA/14 (08-15)
Approved for use through 04/30/2017. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	0016.001000H
	Application Number	
Title of Invention	FLASH-DRAM HYBRID MEMORY MODULE	

Signature:

NOTE: This Application Data Sheet must be signed in accordance with 37 CFR 1.33(b). **However, if this Application Data Sheet is submitted with the INITIAL filing of the application and either box A or B is not checked in subsection 2 of the "Authorization or Opt-Out of Authorization to Permit Access" section, then this form must also be signed in accordance with 37 CFR 1.14(c).**

This Application Data Sheet **must** be signed by a patent practitioner if one or more of the applicants is a **juristic entity** (e. g., corporation or association). If the applicant is two or more joint inventors, this form must be signed by a patent practitioner, **all** joint inventors who are the applicant, or one or more joint inventor-applicants who have been given power of attorney (e.g., see USPTO Form PTO/AIA/81) on behalf of **all** joint inventor-applicants.

See 37 CFR 1.4(d) for the manner of making signatures and certifications.

Signature	/Khaled Shami/			Date (YYYY-MM-DD)	
First Name	Khaled	Last Name	Shami	Registration Number	38745

Additional Signature may be generated within this form by selecting the Add button.

Electronic Patent Application Fee Transmittal

Application Number:	
Filing Date:	
Title of Invention:	FLASH-DRAM HYBRID MEMORY MODULE
First Named Inventor/Applicant Name:	Hyun Lee
Filer:	Khaled Shami/Stephanie Semler
Attorney Docket Number:	0016.001000H

Filed as Large Entity

Filing Fees for Track I Prioritized Examination - Nonprovisional Application under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
UTILITY APPLICATION FILING	1011	1	320	320
UTILITY SEARCH FEE	1111	1	700	700
UTILITY EXAMINATION FEE	1311	1	800	800
REQUEST FOR PRIORITIZED EXAMINATION	1817	1	4200	4200
Pages:				
Claims:				
Miscellaneous-Filing:				
PROCESSING FEE, EXCEPT PROV. APPLS.	1830	1	140	140

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
		Total in USD ($)		**6160**

Electronic Acknowledgement Receipt	
EFS ID:	41526926
Application Number:	17138766
International Application Number:	
Confirmation Number:	8804
Title of Invention:	FLASH-DRAM HYBRID MEMORY MODULE
First Named Inventor/Applicant Name:	Hyun Lee
Customer Number:	151145
Filer:	Khaled Shami/Stephanie Semler
Filer Authorized By:	Khaled Shami
Attorney Docket Number:	0016.001000H
Receipt Date:	30-DEC-2020
Filing Date:	
Time Stamp:	21:04:29
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	$6160
RAM confirmation Number	E2020BTL11438211
Deposit Account	602034
Authorized User	Stephanie Semler
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: 37 CFR 1.16 (National application filing, search, and examination fees) 37 CFR 1.17 (Patent application and reexamination processing fees)	

37 CFR 1.19 (Document supply fees)

37 CFR 1.20 (Post Issuance fees)

37 CFR 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Power of Attorney	NetlistPostAIAPOA.pdf	711728 e45cea84246703abf611c09bfc51150cafd7cb72	no	1
Warnings:					
The page size in the PDF is too large. The pages should be 8.5 x 11 or A4. If this PDF is submitted, the pages will be resized upon entry into the Image File Wrapper and may affect subsequent processing					
Information:					
2	Oath or Declaration filed	0016001000H_InvDec.pdf	448715 e3ef024451ed3cd6e1c63ed595c4a0adf7a22b58	no	5
Warnings:					
Information:					
3	Drawings-only black and white line drawings	0016001000H_Drwgs.pdf	4555960 10944aad8e0cf3b0b62a67fd9fd555d91238f91a	no	22
Warnings:					
Information:					
4		0016001000H_Application.pdf	579398 655826dcaacfa39c576f09b511b5596571f5251b	yes	83

Multipart Description/PDF files in .zip description

Document Description	Start	End
Specification	1	75
Claims	76	82
Abstract	83	83

Warnings:

Information:

5	Power of Attorney	0016001000H_POA_Transmittal.pdf	195754 dc1b846e0e8d107ff5950cc5e22af92bbdb8de18	no	1
Warnings:					
Information:					
6	TrackOne Request	0016001000H_TrackOneRequestForm_aia0424.pdf	129042 5c434a352f92938e97546479f254e9cca34651d5	no	2
Warnings:					
Information:					
7	Application Data Sheet	WebADS.pdf	179961 64330f64bb5b9af022c5c24dd0ba25bc33aeb7eb	no	9
Warnings:					
Information:					
8	Fee Worksheet (SB06)	fee-info.pdf	38288 fa419fbe8f3b24170d0188bb4e59632311ef315b	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	6838846		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

<u>New Applications Under 35 U.S.C. 111</u>
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.
<u>National Stage of an International Application under 35 U.S.C. 371</u>
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.
<u>New International Application Filed with the USPTO as a Receiving Office</u>
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Doc Code: PA..
Document Description: Power of Attorney

PTO/AIA/82A (07-13)
Approved for use through 01/31/2018. OMB 0651-0035
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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TRANSMITTAL FOR POWER OF ATTORNEY TO ONE OR MORE REGISTERED PRACTITIONERS

NOTE: This form is to be submitted with the Power of Attorney by Applicant form (PTO/AIA/82B) to identify the application to which the Power of Attorney is directed, in accordance with 37 CFR 1.5, unless the application number and filing date are identified in the Power of Attorney by Applicant form. If neither form PTO/AIA/82A nor form PTO/AIA82B identifies the application to which the Power of Attorney is directed, the Power of Attorney will not be recognized in the application.

Application Number	To Be Assigned
Filing Date	To Be Assigned
First Named Inventor	Hyun Lee
Title	FLASH-DRAM HYBRID MEMORY MODULE
Art Unit	To Be Assigned
Examiner Name	To Be Assigned
Attorney Docket Number	0016.001000H

SIGNATURE of Applicant or Patent Practitioner

Signature	/Khaled Shami/	Date (Optional)	
Name	Khaled Shami	Registration Number	38,745
Title (if Applicant is a juristic entity)			
Applicant Name (if Applicant is a juristic entity)			

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4(d) for signature requirements and certifications. If more than one applicant, use multiple forms.

☐ *Total of _____ forms are submitted.

This collection of information is required by 37 CFR 1.131, 1.32, and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

United States Patent and Trademark Office

Office of the Chief Financial Officer

Document Code:WFEE

User :C41739

Sale Accounting Date:01/14/2021

Sale Item Reference Number	Effective Date
17138766	12/30/2020

Document Number	Fee Code	Fee Code Description	Amount Paid	Payment Method
I20211DH03073615	1202	CLAIMS IN EXCESS OF 20	$1,000.00	Deposit Account

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
17/138,766	12/30/2020	1731	2820	0016.001000H	30	3

CONFIRMATION NO. 8804

151145
Shami Messinger PLLC
1000 Wisconsin Ave. NW
Suite 200
Washington, DC 20007

FILING RECEIPT



Date Mailed: 01/19/2021

Receipt is acknowledged of this non-provisional utility patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF FIRST INVENTOR, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection.

Please verify the accuracy of the data presented on this receipt. If an error is noted on this Filing Receipt, please submit a written request for a corrected Filing Receipt, including a properly marked-up ADS showing the changes with strike-through for deletions and underlining for additions. If you received a "Notice to File Missing Parts" or other Notice requiring a response for this application, please submit any request for correction to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections provided that the request is grantable.

Inventor(s)

Hyun Lee, Ladera Ranch, CA;
Chi-She Chen, Walnut, CA;
Jeffrey C. Solomon, Irvine, CA;
Scott H. Milton, Irvine, CA;
Jayesh Bhakta, Cerritos, CA;

Applicant(s)

Netlist, Inc., Irvine, CA;

Assignment For Published Patent Application

Netlist, Inc., Irvine, CA

Power of Attorney: The patent practitioners associated with Customer Number 151145

Domestic Priority data as claimed by applicant

This application is a CON of 15/934,416 03/23/2018
which is a CON of 14/840,865 08/31/2015 PAT 9928186
which is a CON of 14/489,269 09/17/2014 PAT 9158684
which is a CON of 13/559,476 07/26/2012 PAT 8874831
which claims benefit of 61/512,871 07/28/2011
and is a CIP of 12/240,916 09/29/2008 PAT 8301833
which is a CON of 12/131,873 06/02/2008 ABN
which claims benefit of 60/941,586 06/01/2007

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.) - None.
Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

Permission to Access Application via Priority Document Exchange: Yes

Permission to Access Search Results: Yes

Applicant may provide or rescind an authorization for access using Form PTO/SB/39 or Form PTO/SB/69 as appropriate.

If Required, Foreign Filing License Granted: 01/14/2021

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 17/138,766**

Projected Publication Date: 04/29/2021

Non-Publication Request: No

Early Publication Request: No
Title

FLASH-DRAM HYBRID MEMORY MODULE

Preliminary Class

501

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

LICENSE FOR FOREIGN FILING UNDER

Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

GRANTED

The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where the conditions for issuance of a license have been met, regardless of whether or not a license may be required as set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign AssetsControl, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

SelectUSA

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The U.S. offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to promote and facilitate business investment. SelectUSA provides information assistance to the international investor community; serves as an ombudsman for existing and potential investors; advocates on behalf of U.S. cities, states, and regions competing for global investment; and counsels U.S. economic development organizations on investment attraction best practices. To learn more about why the United States is the best country in the world to develop technology, manufacture products, deliver services, and grow your business, visit http://www.SelectUSA.gov or call +1-202-482-6800.

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number: 17/138,766

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY FEE($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	320
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	700
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	800
TOTAL CLAIMS (37 CFR 1.16(i))	30 minus 20 =	* 10			OR	x 100 =	1000
INDEPENDENT CLAIMS (37 CFR 1.16(h))	3 minus 3 =	*				x 480 =	0.00
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	2820

APPLICATION AS AMENDED - PART II

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
AMENDMENT A	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
AMENDMENT B	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/138,766	12/30/2020	Hyun Lee	0016.001000H	8804

151145 7590 01/26/2021

Shami Messinger PLLC
1000 Wisconsin Ave. NW
Suite 200
Washington, DC 20007

EXAMINER	
ART UNIT	PAPER NUMBER
2135	

NOTIFICATION DATE	DELIVERY MODE
01/26/2021	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

khaled@shamimessinger.com
mike@shamimessinger.com
stephanie@shamimessinger.com

Decision Granting Request for Prioritized Examination (Track I)	**Application No.** 17/138,766	**Applicant(s)** Lee et al.	
	Examiner CHERYL P GIBSON BAYLOR	**Art Unit** OPET	**AIA (FITF) Status** No

1. THE REQUEST FILED 30 December 2020 IS **GRANTED** .

The above-identified application has met the requirements for prioritized examination

A. ☑ for an original nonprovisional application (Track I).
B. ☐ for an application undergoing continued examination (RCE).

2. **The above-identified application will undergo prioritized examination**. The application will be accorded special status throughout its entire course of prosecution until one of the following occurs:

A. filing a **petition for extension of time** to extend the time period for filing a reply;

B. filing an **amendment to amend the application to contain more than four independent claims, more than thirty total claims** , or a multiple dependent claim;

C. filing a **request for continued examination** ;

D. filing a notice of appeal;

E. filing a request for suspension of action;

F. mailing of a notice of allowance;

G. mailing of a final Office action;

H. completion of examination as defined in 37 CFR 41.102; or

I. abandonment of the application.

Telephone inquiries with regard to this decision should be directed to CHERYL GIBSON BAYLOR at (571)272-3213. In his/her absence, calls may be directed to Petition Help Desk at (571) 272-3282.

/CHERYL GIBSON BAYLOR/ Paralegal Specialist, OPET	

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/138,766	12/30/2020	Hyun Lee	0016.001000H	8804

151145 7590 03/02/2021

Shami Messinger PLLC
1000 Wisconsin Ave. NW
Suite 200
Washington, DC 20007

EXAMINER	
FARROKH, HASHEM	

ART UNIT	PAPER NUMBER
2135	

NOTIFICATION DATE	DELIVERY MODE
03/02/2021	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

khaled@shamimessinger.com
mike@shamimessinger.com
stephanie@shamimessinger.com

Office Action Summary	**Application No.** 17/138,766	**Applicant(s)** Lee et al.	
	Examiner HASHEM FARROKH	**Art Unit** 2135	**AIA (FITF) Status** No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☑ Responsive to communication(s) filed on 12/30/2020.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL.** 2b) ☑ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5) ☑ Claim(s) 1-30 is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6) ☑ Claim(s) 16-20 and 22-30 is/are allowed.

7) ☑ Claim(s) 1-15 and 21 is/are rejected.

8) ☐ Claim(s) _____ is/are objected to.

9) ☐ Claim(s) _____ are subject to restriction and/or election requirement

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to **PPHfeedback@uspto.gov.**

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☑ The drawing(s) filed on 12/30/2020 is/are: a)☑ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☑ Notice of References Cited (PTO-892)

2) ☐ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date _____.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date _____.

4) ☐ Other: _____.

Notice of Pre-AIA or AIA Status

The present application is being examined under the pre-AIA first to invent provisions.

The instant application having application No. 17/138,766 has a total of 30 claims pending in the application; there are 3 independent claim and 27 dependent claims, all of which are ready for examination by the examiner.

ACKNOWLEDGEMENT OF REFERENCES CITED BY APPLICANT

Information Disclosure Statement

*As required by **M.P.E.P. 2001.06(b)** and **37 C.F.R. 1.98(d)**, since the instant application has been identified as a continuation application of an earlier filed application and is relied upon for an earlier filing date under **35 U.S.C. 120**, the examiner has reviewed the prior art cited in the earlier related application as required by **M.P.E.P. 707.05** and **904** and as stated in **M.P.E.P. 2001.06(b),** no separate citation of the same prior art need be made by the applicants in the instant application.*

INFORMATION CONCERNING CLAIMS:

Claim Interpretation

Claim limitations in this application do not use the word "means" (or "step"), thus, they *are not being interpreted under 35 U.S.C. 112(f) or pre-AIA 35 U.S.C. 112, sixth paragraph.*

Claim Rejections - 35 USC § 112

1. Claims 1-15 and 21 are rejected under 35 U.S.C. 112(b) or 35 U.S.C. 112 (pre-AIA), second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the inventor or a joint inventor (or for applications subject to pre-AIA 35 U.S.C. 112, the applicant), regards as the invention.

2. The independent claim 1 in lines 24-25 recite limitation:

wherein one of the second and fourth voltage amplitudes is less than the other one of the second and fourth voltage amplitudes."

It is not clear what is meant by "the other one of the second and fourth voltage amplitudes". *Dependent claims 2-15 are dependent from the independent claim 1 and are rejected by virtue of their dependency from the independent claim 1. Claim 21 recites a similar limitation and rejected based on the same ground of rejection.*

3. Claims 1-15 and 21 are rejected because of lack sufficient antecedent basis.

4. Claim 1 recites the limitation "the other one of the second and fourth voltage amplitudes" *in 25. There is insufficient antecedent basis for this limitation in the claim. Dependent claims 2-15 are dependent from the independent claim 1 and are rejected by virtue of their dependency from the independent claim 1. Claim 21 recites a similar limitation and rejected based on the same ground of rejection.*

Allowable Subject Matter

5. Claim16-20 and 22-30 are allowed.

The following is an examiner's statement of reasons for allowance:

6. The primary reasons for allowance of claims 16-20 in the instant application is the combination with the inclusion of the following limitations: **"first, second, and third buck converters configured to receive a pre-regulated input voltage and to produce first, second and third regulated voltages, respectively; a plurality of components coupled to the PCB, the plurality of components including a plurality of synchronous dynamic random access memory (SDRAM) devices, each component of the plurality of components coupled to one or more regulated voltages of the first, second, third and fourth regulated voltages; and a voltage monitor circuit configured to monitor an input voltage received via a first portion of the plurality of edge connections, the voltage monitor circuit configured to produce a signal in response to the input voltage having a voltage amplitude that is greater than a first threshold voltage."**

7. The primary reasons for allowance of claims 23-30 in the instant application is the combination with the inclusion of the following limitations: **"a plurality of components coupled to the PCB, each component of the plurality of components coupled to one or more regulated voltages of first, second, third and fourth regulated voltages, the plurality of components including a plurality of synchronous dynamic random access memory (SDRAM) devices and one or**

more registers, the plurality of SDRAM devices coupled to the first regulated voltage, the one or more registers coupled to (i) the second regulated voltage, (ii) a portion of the plurality of edge connections, and (iii) the plurality of SDRAM devices, wherein a plurality of address and control signals are coupled to the one or more registers via the portion of the plurality of edge connections; first, second, and third buck converters configured to provide the first, second and third regulated voltages, respectively"

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

The prior art made of record and not relied upon are as follows:

1. *Chen et al. (US 20120271990 A1).*
2. *Bates (US 20070136523 A1).*
3. *Prete et al. (US 20080126624 A1).*

Any inquiry concerning this communication or earlier communications from the examiner should be directed to HASHEM FARROKH whose telephone number is (571)272-4193. The examiner can normally be reached Monday through Friday from 8:30 am - 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mr. Sanjiv Shah can be reached on (571)272-4098. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. For questions regarding access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/HASHEM FARROKH/
Primary Examiner, Art Unit 2135

February 25, 2021

Notice of References Cited	Application/Control No. 17/138,766	Applicant(s)/Patent Under Reexamination Lee et al.	
	Examiner HASHEM FARROKH	Art Unit 2135	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
*	A	US-20120271990-A1	10-2012	Chen; Chi-She	G06F12/00	711/103
*	B	US-20070136523-A1	06-2007	Bonella; Randy M.	G06F9/4401	711/113
*	C	US-20080126624-A1	05-2008	Prete; Edoardo	G11C7/106	710/53
	D					
	E					
	F					
	G					
	H					
	I					
	J					
	K					
	L					
	M					

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	CPC Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Petitioners
Ex. 1002, p. 144

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/138,766	Lee et al.
	Examiner	Art Unit
	HASHEM FARROKH	2135

CPC - Searched*		
Symbol	Date	Examiner
G06F13/28; G06F13/4027; G06F13/1694; G06F13/4223; G06F12/0638; G06F12/0246; G06F1/185; G06F3/0613; G06F3/0685 OR G06F3/0659; G06F2212/7208; G06F2212/205; G11C7/1072; G11C14/0018	02/24/2021	HF

CPC Combination Sets - Searched*		
Symbol	Date	Examiner

US Classification - Searched*			
Class	Subclass	Date	Examiner
711	103	02/25/2021	HF
711	104	02/25/2021	HF
711	105	02/25/2021	HF

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

Search Notes		
Search Notes	Date	Examiner
Assignee/Inventor Search	02/25/2021	HF
EAST Text Search	02/24/2021	HF
IP Search	02/25/2021	HF
Google Search	02/25/2021	HF

Petitioners
Ex. 1002, p. 145

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/138,766	Lee et al.
	Examiner	Art Unit
	HASHEM FARROKH	2135

Interference Search			
US Class/CPC Symbol	US Subclass/CPC Group	Date	Examiner

Petitioners
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Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/138,766	Lee et al.
	Examiner	**Art Unit**
	HASHEM FARROKH	2135

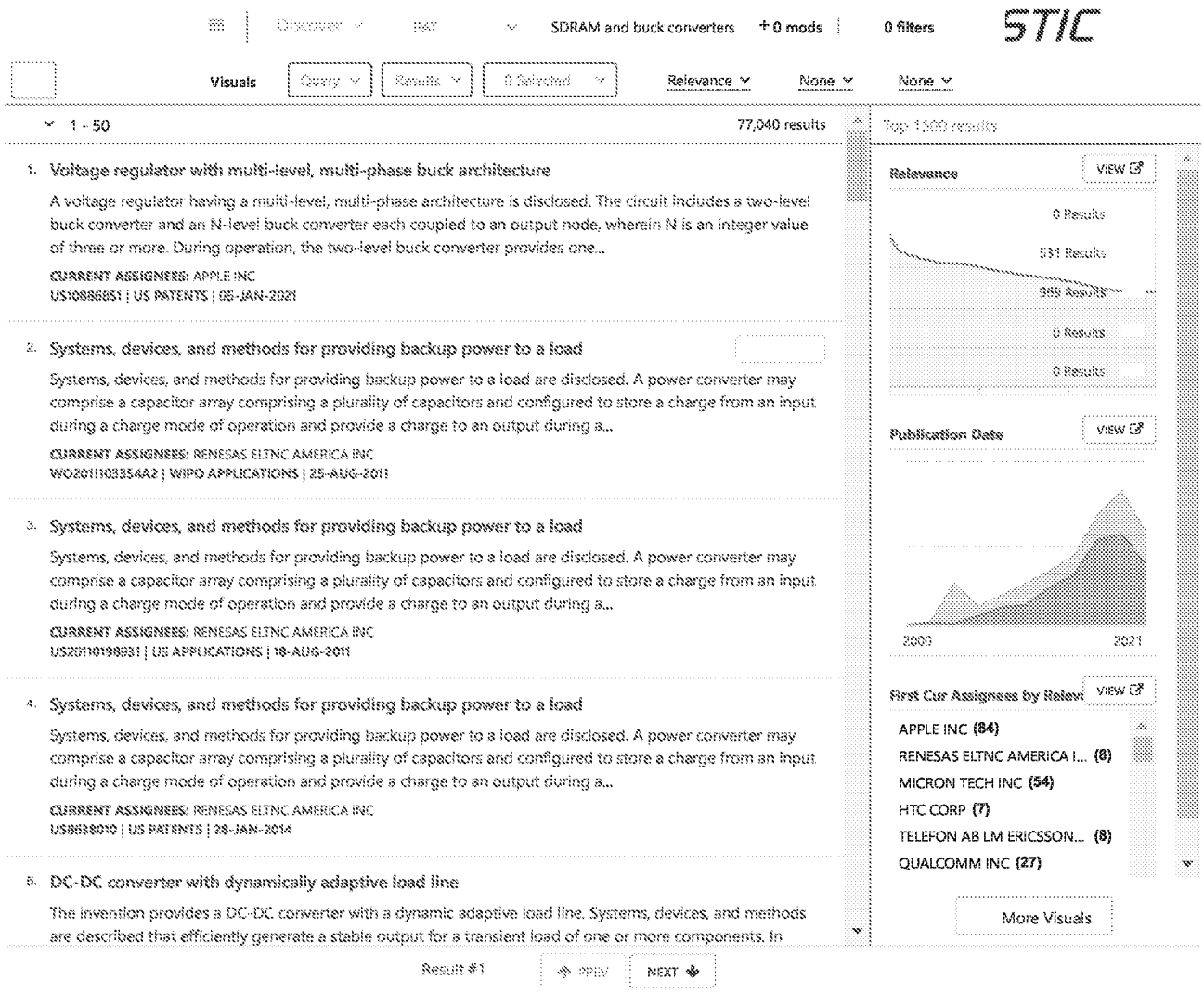
✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

CLAIMS

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	02/25/2021								
	1	✓								
	2	✓								
	3	✓								
	4	✓								
	5	✓								
	6	✓								
	7	✓								
	8	✓								
	9	✓								
	10	✓								
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	13	✓								
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	16	=								
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	18	=								
	19	=								
	20	=								
	21	✓								
	22	=								
	23	=								
	24	=								
	25	=								
	26	=								
	27	=								
	28	=								
	29	=								
	30	=								

Petitioners
Ex. 1002, p. 147



Petitioners
Ex. 1002, p. 148

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Feedback

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Guide to Choosing the Best DC-to-DC Converter for Your ...

Mar 14, 2019 — If both cases are required, a BUCKBOOST converter is used. ... under a no current load condition (e.g. CMOS RAM keepalive applications). ... Also, check the package type and size and PCB design constraints provided by the ...

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Addressing PCB effects in the design of a buck converter ...

Addressing PCB effects in the design of a buck converter. Abstract: ... Ihsan Erdin; Ram Achar ... such as open-loop, input-to-output and control-to-output transfer functions including distributed circuit parameters that account for PCB parasitics.

www.eetimes.com › proper-board-layout-makes-switch...

Proper board layout makes switchers work right the first time ...

These are the critical traces for any switcher PCB layout. ... For example, a buck-boost IC construction will usually be different from that of a buck IC, even though ...

en.wikipedia.org › wiki › Buck_converter

Buck converter - Wikipedia

A buck converter (step-down converter) is a DC-to-DC power converter which steps down ... (bulk) supply voltage (often 12 V) down to lower voltages needed by USB, DRAM and the CPU (1.8 V or less). ... (conduction) losses in the wires or PCB traces, as well as in the switches and inductor, as in any electrical circuit.

People also search for

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Design Considerations for EMI Reduction in Automotive ...

May 26, 2017 — The Buck topology DC/DC converter constitutes a circuit with the input ... the components selection, and the PCB layout as the method that does not ... thereof, WICED, PSoC, CapSense, EZ-USB, F-RAM, and Traveo are.

onlinelibrary.wiley.com › doi › full › etrj.2018-0551

Efficiency improvement of a DC/DC converter using LTCC ...

Jun 21, 2019 — Efficiency improvement of a DC/DC converter using LTCC substrate ... The power conversion efficiencies of the LTCC- and PCB-based synchronous ... bioMEMS/biochips, surface micromachining, DRAM metallization, and ...

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Wide VIN, Multi-Output DC/DC Converter and PowerPath ...

efficiency switching DC/DC converters which seamlessly transition from battery to ... 125°C, θJA = 37°C/W. EXPOSED PAD (PIN 25) IS GND, MUST BE SOLDERED TO PCB ... such as a 1.8V rail for SDRAM and a 1.2V rail to supply the system ...

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AC/DC DC/DC Fundamentals - Power Supply Design Basic

Design Procedure for AC/DC Circuits Switching **Regulator** Basics and More. Switching **Regulator** Basics by ROHM, AC/DC **Converter** Designs and more. Highlights: Engineering Tips Available, Design Support Tools Available.

Related searches

buck converter **circuit diagram with explanation**	**advantages of** buck converter
boost converter	**different types of dc-dc converters pdf**
buck converter **design**	buck converter **tutorial**
buck converter **design tutorial**	**dc to dc step-down** converter **circuit**

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S347	132	(buck$1converter or (buck near5 convert$3)) with ((regulated adj voltage) near2 (amplitude or value or potential))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/02/23 15:55
S348	0	S347 and SDRAM	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/02/23 16:00
S349	0	(((first near5 (buck adj converter)) with (second near5 (buck adj converter)) with (thirsd near5 (buck adj converter))) or ((plurality or multiple) near5 (buck adj converters))) with (supp$3 or produc$3 or generat$3 or creat$3) with ((first near5 second near5 third) near5 (regulated adj voltages))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/02/24 14:27
S350	2	(buck adj converters) with (regulated adj voltages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2021/02/24 14:32
S351	0	((printed$1circuit$1board or (printed adj circuit adj board)) or PCB) with ((plurality or muliple) near5 ((synchronous adj dynamic adj random adj access adj memor$3) or SDRAM)) with (regulated adj voltages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2021/02/24 14:55
S352	0	(monitor$3 or detect$3) with (input adj voltage) with receiv$3 with (edje adj connections)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/02/24 15:00

S353	0	(monitor$3 or detect$3) with (input adj voltage) with receiv$3 with (edje adj connections)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2021/02/24 15:00
S354	33	(monitor$3 or detect$3) with (input adj voltage) with receiv$3 with connections	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2021/02/24 15:03
S355	0	(((first near5 (buck adj converter)) same (second near5 (buck adj converter)) same (thirsd near5 (buck adj converter))) or ((plurality or multiple) near5 (buck adj converters))) same (supp$3 or produc$3 or generat$3 or creat$3) same ((first near5 second near5 third) near5 (regulated adj voltages))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/02/24 15:06
S356	0	(((first near5 (buck adj converter)) same (second near5 (buck adj converter)) same (thirsd near5 (buck adj converter))) or ((plurality or multiple) near5 (buck adj converters))) same (supp$3 or produc$3 or generat$3 or creat$3) same ((first near5 second near5 third) near5 (regulated adj voltages))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2021/02/24 15:07
S357	0	(monitor$3 or detect$3) with (input adj voltage) with receiv$3 with (edje adj connect$4)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/02/24 15:08
S358	0	((printed$1circuit$1board or (printed adj circuit adj board)) or PCB) with ((plurality or muliple) near5 ((synchronous adj dynamic adj random adj access adj memor$3) or SDRAM)) with voltages	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2021/02/24 15:11
S359	0	((printed$1circuit$1board or (printed adj circuit adj board)) or PCB) same ((plurality or muliple) near5 ((synchronous adj dynamic adj	US-PGPUB; USPAT; USOCR; FPRS; EPO;	OR	OFF	2021/02/24 15:12

		random adj access adj memor$3) or SDRAM)) same voltages	JPO; DERWENT; IBM_TDB			
S360	32	((printed$1circuit$1board or (printed adj circuit adj board)) or PCB) same ((plurality or muliple) near5 ((synchronous adj dynamic adj random adj access adj memor$3) or SDRAM))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2021/02/24 15:13
S361	128,557	(G06F13/28 OR G06F13/4027 OR G06F13/1694 OR G06F13/4223 OR G06F12/0638 OR G06F12/0246 OR G06F1/185 OR G06F3/0613 OR G06F3/0685 OR G06F3/0659 OR G06F2212/7208 OR G06F2212/205 OR G11C7/1072 OR G11C14/0018).cpc. OR 711/100.CCLS OR G06F3/06.icpr	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/02/24 15:39
S362	14	S361 and (SDRAM and (buck near5 converter))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/02/24 15:41
S363	0	(SDRAM and (buck near5 converter)).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/02/24 15:51
S364	151	((transfer$3 or cop$4 or transmi$5 or retriev$3 or read$3) near5 DRAM near5 (flash or non$1volatile)).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/02/25 11:58
S365	1,328	Lee-Hyun.in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/02/25 11:58
S366	76	Chen-Chi-She.in.	US-PGPUB; USPAT; USOCR;	OR	ON	2021/02/25 11:58

			FPRS; EPO; JPO; DERWENT; IBM_TDB			
S367	72	Solomon-Jeffrey-C.in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/02/25 11:58
S368	33	Milton-Scott-H.in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/02/25 11:58
S369	36	Bhakta-Jayesh.in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/02/25 11:58
S370	0	S364 and (S365 or S366 or S367 or S368 or S369)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/02/25 11:58
S371	11,623	(transfer$4 or cop$4 or transmi$5 or mov$3) with data with (non$1volatile or flash or SSD or NVM) with (volatile or ?RAM or ?DRAM memory).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/02/25 12:01
S372	215	NETLIST.as.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/02/25 12:01
S373	21	S371 and S372	US-PGPUB; USPAT; USOCR; FPRS; EPO;	OR	ON	2021/02/25 12:01

			JPO; DERWENT; IBM_TDB			
S374	128,598	(G06F13/28 OR G06F13/4027 OR G06F13/1694 OR G06F13/4223 OR G06F12/0638 OR G06F12/0246 OR G06F1/185 OR G06F3/0613 OR G06F3/0685 OR G06F3/0659 OR G06F2212/7208 OR G06F2212/205 OR G11C7/1072 OR G11C14/0018).cpc. OR 711/100.CCLS OR G06F3/06.icpr	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/02/25 12:04
S375	14	S374 and (SDRAM and (buck near5 converter))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/02/25 12:04
S376	0	(((synchronous adj dynamic adj random adj access adj memor$3) or SDRAM) and (buck near5 converter)).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/02/25 12:09
S377	702	(((synchronous adj dynamic adj random adj access adj memor$3) or SDRAM) and (buck near5 converter))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/02/25 12:10
S378	14	S374 and S377	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/02/25 12:12
S379	12	S372 and S378	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/02/25 12:12

2/25/2021 1:49:43 PM
C:\Users\hfarrokh\Documents\EAST\Workspaces\15934416.wsp

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT: Netlist, Inc.	CONF. NO: 8804
APPLICATION NO: 17/138,766	ART UNIT: 2135
FILING DATE: 12/30/20	EXAMINER: FARROKH, Hashem

TITLE: FLASH-DRAM HYBRID MEMORY MODULE

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

AMENDMENT AND/OR REPLY TO OFFICE ACTION

Commissioner:

In response to the non-final Office Action issued March 2, 2021, Applicant submits the following Amendment and Remarks.

Amendments to the Claims, if any, are reflected in the Listing of Claims beginning on page **2**.

Remarks begin on page **10**.

Applicant does not believe that extensions of time are required beyond those provided for in documents accompanying this paper. However, if additional extensions of time are necessary to prevent abandonment of this application, then such extensions of time are hereby petitioned under 37 C.F.R. § 1.136(a), and any additional fees required to continue prosecution or appeal of this application (including issue fee, fees for net addition of claims or forwarding to appeal) are hereby authorized to be charged to our Deposit Account No. 60-2034.

LISTING OF CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application.

1. (Currently amended) A memory module comprising:

a printed circuit board (PCB) having an interface configured to fit into a corresponding slot connector of a host system, the interface including a plurality of edge connections configured to couple power, data, address and control signals between the memory module and the host system;

a first buck converter configured to provide a first regulated voltage having a first voltage amplitude;

a second buck converter configured to provide a second regulated voltage having a second voltage amplitude;

a third buck converter configured to provide a third regulated voltage having a third voltage amplitude;

a converter circuit configured to provide a fourth regulated voltage having a fourth voltage amplitude; and

a plurality of components coupled to the PCB, each component of the plurality of components coupled to one or more regulated voltages of the first, second, third and fourth regulated voltages, the plurality of components comprising:

a plurality of synchronous dynamic random access memory (SDRAM) devices coupled to the first regulated voltage, and

at least one circuit coupled between a first portion of the plurality of edge connections and the plurality of SDRAM devices, the at least one circuit operable to (i) receive a first plurality of address and control signals via the first portion of the plurality of edge connections, and (ii) output a second plurality of address and control signals to the plurality of SDRAM devices, the at least one circuit coupled to both the second regulated voltage and the fourth

regulated voltage, wherein a first one of the second and fourth voltage amplitudes is less than ~~the other~~a second one of the second and fourth voltage amplitudes.

2. (Original) The memory module of claim 1, wherein the first and third buck converters are further configured to operate as a dual buck converter.

3. (Original) The memory module of claim 1, wherein the first voltage amplitude is 1.8 volts.

4. (Original) The memory module of claim 1, wherein the second, third, and fourth voltage amplitudes are 2.5 volts, 1.2 volts, and 3.3 volts, respectively.

5. (Original) The memory module of claim 1, further comprising:

a voltage monitor circuit configured to monitor a power input voltage received via a second portion of the plurality of edge connections, the voltage monitor circuit configured to produce a trigger signal in response to the power input voltage having a voltage amplitude that is greater than a first threshold voltage.

6. (Original) The memory module of claim 1, the plurality of components further comprising:

one or more registers coupled to one of the first, second, third and fourth regulated voltages, the one or more registers configured to register, in response to a clock, the first plurality of address and control signals, wherein the one of the first, second, third and fourth regulated voltages is selectively switched off to turn power off to the one or more registers while one or more components of the plurality of components are powered on.

7. (Original) The memory module of claim 5, wherein the voltage monitor circuit is further configured to produce the trigger signal in response to the power input voltage having a voltage amplitude that is less than a second threshold voltage.

8. (Original) The memory module of claim 6, wherein, in response to selectively switching on the one of the first, second, third and fourth regulated voltages to the one or more registers, the one or more registers is configured to output the registered first plurality of address and control signals to the plurality of SDRAM devices.

9. (Original) The memory module of claim 5, wherein the power input voltage is coupled to the first, second, and third buck converters and the converter circuit.

10. (Original) The memory module of claim 5, wherein the first threshold voltage corresponds to a voltage level that is ten percent greater than a specified operating voltage.

11. (Original) The memory module of claim 7, wherein the second threshold voltage corresponds to a voltage level that is ten percent less than a specified operating voltage.

12. (Original) The memory module of claim 5, the plurality of components further comprising:

a logic element including a non-volatile memory, the non-volatile memory is configured to store configuration information.

13. (Original) The memory module of claim 12, wherein, in response to the trigger signal, the logic element writes information into the non-volatile memory.

14. (Original) The memory module of claim 1, the plurality of components further comprising:

a logic element including one or more integrated circuits and discrete electrical elements, the one or more integrated circuit including an internal non-volatile memory, wherein the non-volatile memory is configured to store configuration information.

15. (Original) The memory module of claim 5, the plurality of components further comprising:

a non-volatile memory; and

a controller configured to receive the trigger signal, wherein, in response to the trigger signal, the controller performs a write operation to the non-volatile memory.

16. (Original) A memory module comprising:

a printed circuit board (PCB) having an interface configured to fit into a corresponding slot connector of a host system, the interface including a plurality of edge connections configured to couple power, data, address and control signals between the memory module and the host system;

first, second, and third buck converters configured to receive a pre-regulated input voltage and to produce first, second and third regulated voltages, respectively;

a converter circuit configured to reduce the pre-regulated input voltage to provide a fourth regulated voltage, wherein the first, second, third and fourth regulated voltages have first, second, third, and fourth voltage amplitudes, respectively;

a plurality of components coupled to the PCB, the plurality of components including a plurality of synchronous dynamic random access memory (SDRAM) devices, each component of the plurality of components coupled to one or more regulated voltages of the first, second, third and fourth regulated voltages; and

a voltage monitor circuit configured to monitor an input voltage received via a first portion of the plurality of edge connections, the voltage monitor circuit configured to produce a signal in response to the input voltage having a voltage amplitude that is greater than a first threshold voltage.

17. (Original) The memory module of claim 16, wherein the second and third buck converters are configured to operate as a dual buck converter.

18. (Original) The memory module of claim 16, the plurality of components further including:

a controller coupled to the voltage monitor circuit and configured to receive the signal, wherein the controller executes a write operation in response to the signal.

19. (Original) The memory module of claim 18, wherein the write operation includes writing data information into non-volatile memory.

20. (Original) The memory module of claim 16, wherein the plurality of SDRAM devices are configured to receive at least one of the first, second, third and fourth regulated voltages having a voltage amplitude of 1.8 volts.

21. (Currently amended) The memory module of claim 16, the plurality of

components further including:

at least one circuit coupled between the interface and the plurality of SDRAM devices, the at least one circuit operable to receive a first plurality of address and control signals via a second portion of the plurality of edge connections and to output a second plurality of address and control signals to the plurality of SDRAM devices, the at least one circuit coupled to both the second regulated voltage and the fourth regulated voltage, wherein a first one of the second and fourth voltage amplitudes is less than ~~the other~~a second one of the second and fourth voltage amplitudes.

22. (Original) The memory module of claim 16, the plurality of components further including:

a logic element including an internal non-volatile memory, wherein the non-volatile memory is configured to store configuration information, wherein the configuration information is used to program the logic element.

23. (Original) A memory module comprising:

a printed circuit board (PCB) having an interface configured to fit into a corresponding slot connector of a host system, the interface including a plurality of edge connections configured to couple power, data, address and control signals between the memory module and the host system;

a plurality of components coupled to the PCB, each component of the plurality of components coupled to one or more regulated voltages of first, second, third and fourth regulated voltages, the plurality of components including a plurality of synchronous dynamic random access memory (SDRAM) devices and one or more registers, the plurality of SDRAM devices coupled to the first regulated voltage, the one or more registers coupled to (i) the second regulated voltage, (ii) a portion of the plurality of edge connections, and (iii) the plurality of SDRAM devices, wherein a plurality of address and control signals are coupled to the one or

more registers via the portion of the plurality of edge connections;

first, second, and third buck converters configured to provide the first, second and third regulated voltages, respectively; and

a converter circuit configured to provide the fourth regulated voltage,

wherein the second regulated voltage is configured to be selectively switched on or off to the one or more registers while at least the plurality of SDRAM devices are powered on,

wherein if the second regulated voltage is switched on while at least the plurality of SDRAM devices are powered on, the one or more registers are configured to couple the first plurality of address and control signals to the plurality of SDRAM devices, and

wherein if the second regulated voltage is switched off while the plurality of SDRAM devices are powered on, the one or more registers are configured to decouple the plurality of SDRAM devices from the first plurality of address and control signals.

24. (Original) The memory module of claim 23, further comprising:

a voltage monitor circuit configured to monitor an input voltage received from the host system via the interface, the voltage monitor circuit configured to produce a signal in response to the input voltage having a voltage amplitude that is greater than a first threshold voltage.

25. (Original) The memory module of claim 24, wherein the voltage monitor circuit is further configured to produce the signal in response to the input voltage having a voltage amplitude that is less than a second threshold voltage.

26. (Original) The memory module of claim 23, wherein the second and third buck converters are configured to operate as a dual buck converter.

27. (Original) The memory module of claim 24, the plurality of components further including:

a controller coupled to the voltage monitor circuit and configured to receive the signal, wherein, in response to the signal, the controller executes a write operation.

28. (Original) The memory module of claim 27, wherein the write operation includes writing data information to non-volatile memory.

29. (Original) The memory module of claim 23, wherein the plurality of SDRAM devices are configured to receive at least one of the first, second, third and fourth regulated voltages having a voltage amplitude of 1.8 volts.

30. (Original) The memory module of claim 23, wherein the first, second, and third buck converters are configured to receive a pre-regulated input voltage and to provide the first, second and third regulated voltages, respectively, and wherein the converter circuit is configured to reduce the pre-regulated voltage input to provide the fourth regulated voltage.

REMARKS

The non-final Office Action issued March 2, 2021, has been carefully considered.

Reconsideration in view of the following remarks is respectfully requested.

Upon entry of the foregoing amendment, claims 1-30 are pending in this application, with claims 1, 16, and 23 being the independent claims.

Subject Matter Indicated Allowed or Allowable

Applicant gratefully acknowledges the indication of allowance of claims 16-20 and 22-30.

Rejection(s) Under 35 U.S.C. § 112(b) (or Pre-AIA 35 U.S.C. § 112, Second Paragraph)

Claims 1-15 and 21 stand rejected under 35 U.S.C. § 112(b) (or pre-AIA 35 U.S.C. § 112, second paragraph), as allegedly being indefinite for failing to particularly point out and distinctly claim the subject matter which the inventor or a joint inventor, or, for pre-AIA, the Applicant regards as the invention.

Claims 1 and 21 have been amended to recite "a first one of the second and fourth voltage amplitudes is less than ~~the other~~a second one of the second and fourth voltage amplitudes." In this manner the term "other," which seems to be the source of the alleged indefiniteness, is eliminated. While applicant believes that the usage of the term "other" as it appeared in the claim is grammatically correct, applicant has elected to remove it in the interest of advancing prosecution and gaining allowance.

It is respectfully submitted that claims 1 and 21 are now in compliance with 35 U.S.C. § 112(b) (or pre-AIA 35 U.S.C. § 112, second paragraph), and the rejection claims 1-15 and 21 should be withdrawn.

Amendment to Claims

Claims 1 and 21 have been amended for improved clarity and grammatical accuracy. The amendment does not raise any issues beyond those already considered by the Examiner. No amendment made is related to the statutory requirements of patentability unless expressly stated herein. No amendment is made for the purpose of narrowing the scope of any claim, unless Applicant argues herein that such amendment is made to distinguish over a particular identified reference or combination of references. Any remarks made herein with respect to a given claim or amendment is intended only in the context of that specific claim or amendment, and should not be applied to other claims, amendments or aspects of the claimed arrangements.

Conclusion

In view of the preceding discussion, Applicant respectfully urges that the claims of the present application define patentable subject matter and should be passed to allowance.

If the Examiner believes that a telephone call would help advance prosecution of the present application, the Examiner is kindly invited to call the undersigned attorney at the number below.

Please charge any additional required fees, including those necessary to obtain extensions of time to render timely the filing of the instant Amendment and/or Reply to Office Action, or credit any overpayment not otherwise credited, to our deposit account no. 60-2034.

Respectfully submitted,

Dated: March 11, 2021

/Khaled Shami/
Khaled Shami
Reg. No. 38,745

SHAMI MESSINGER PLLC

1000 Wisconsin Ave N.W., Suite 200
Washington, D.C. 20007
202-516-6900

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT: Netlist, Inc.	CONFIRMATION NO.: 8804
SERIAL NO.: 17/138,766	ART UNIT: 2135
FILING DATE: 12-30-2020	EXAMINER: FARROKH, HASHEM

TITLE: FLASH-DRAM HYBRID MEMORY MODULE

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Commissioner:

Notice of Related Litigation and/or Proceedings

Pursuant to MPEP 2001.06(c), Applicant notifies the Patent and Trademark Office of litigation and proceedings involving U.S. Patents related to the current patent application, the subject matter of which may be related to the present patent application.

Appendix A lists results of a Cases Search. The Cases Search was performed on January 29, 2021, on the Docket Navigator™ search tool for patent cases involving commonly-owned U.S. Patents No. 8,301,833, 8,516,187, 8,671,243, and 8,874,831. The Cases Search covered forums including U.S. federal courts, ITC, and PTAB. The Cases Search results presented includes information output by the search tool for the following fields: Case, Case Filing Date, Case Terminated, and Case Status.

Notification of the cases and proceedings identified in the attached Notice in no way operates as an admission that documents cited or filed in those cases and proceedings are material to the

patentability of the present application or that the subject matter of this application is related to the specific patents subjected to suits and/or proceedings listed in the Notice.

The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 60-2034.

Respectfully submitted,

SHAMI MESSINGER PLLC

Dated: March 11, 2021

/Khaled Shami/
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Appendix A

Cases

11 Results

Patents: 8301833, 8516187, 8671243, 8874831

Case	Case F...	Case Ter...	Case ...	Court	Case Name	Case Nu...
SK hynix Inc. et al v. Netlist, Inc. IPR2017-00692 (PTAB)	Jan. 17, 2017	Jul. 05, 2018	Terminated	PTAB	SK hynix Inc. et al v. Netlist, Inc.	IPR2017-00692

PARTIES

Party	Party Role	Firm	Attorneys
Netlist, Inc.	PATENT OWNER	McAndrews Held & Malloy	Christopher C Winslade, Gregory C Schodde, Ronald H Spuhler, Scott P McBride, Thomas J Wimbiscus, Wayne H Bradley
SK Hynix America Inc. f/k/a Hynix Semiconductor America, Inc.	PETITIONER	Sidley Austin	Joseph A Micallef, Samuel A Dillon
SK hynix Inc.	PETITIONER	Sidley Austin	Joseph A Micallef, Samuel A Dillon
SK Hynix Memory Solutions Inc.	PETITIONER	Sidley Austin	Joseph A Micallef, Samuel A Dillon

PATENTS

Number	Inventor	Name
8874831	Lee	Flash-DRAM hybrid memory module

Case	Case F...	Case Ter...	Case ...	Court	Case Name	Case Nu...
SK hynix Inc. v. Netlist, Inc. IPR2017-00649 (PTAB)	Jan. 13, 2017	May. 29, 2018	Terminated	PTAB	SK hynix Inc. v. Netlist, Inc.	IPR2017-00649

PARTIES

Party	Party Role	Firm	Attorneys
Netlist, Inc.	PATENT OWNER	McAndrews Held & Malloy	Christopher C Winslade, Ronald H Spuhler, Scott P McBride, Thomas J Wimbiscus, Wayne H Bradley
SK Hynix America Inc. f/k/a Hynix Semiconductor America, Inc.	PETITIONER	Sidley Austin	Joseph A Micallef, Samuel A Dillon
SK hynix Inc.	PETITIONER	Sidley Austin	Joseph A Micallef, Samuel A Dillon
SK Hynix Memory Solutions Inc.	PETITIONER	Sidley Austin	Joseph A Micallef, Samuel A Dillon

PATENTS

Number	Inventor	Name
8301833	Chen	Non-volatile memory module

Case	Case F...	Case Ter...	Case ...	Court	Case Name	Case Nu...
SK hynix Inc. et al v. Netlist, Inc. IPR2017-00587 (PTAB)	Jan. 06, 2017	Jun. 20, 2018	Terminated	PTAB	SK hynix Inc. et al v. Netlist, Inc.	IPR2017-00587

PARTIES

Party	Party Role	Firm	Attorneys
Netlist, Inc.	PATENT OWNER	McAndrews Held & Malloy	Christopher C Winslade, Gregory C Schodde, Ronald H Spuhler, Scott P McBride, Thomas J Wimbiscus, Wayne H Bradley
SK Hynix America Inc. f/k/a Hynix Semiconductor America, Inc.	PETITIONER	Sidley Austin	Joseph A Micallef, Wonjoo Suh
SK hynix Inc.	PETITIONER	Sidley Austin	Joseph A Micallef, Wonjoo Suh
SK Hynix Memory Solutions Inc.	PETITIONER	Sidley Austin	Joseph A Micallef, Wonjoo Suh

PATENTS

Number	Inventor	Name
8671243	Chen	Isolation switching for backup memory

SMART Modular Technologies Inc. v. Netlist, Inc. IPR2014-01370 (PTAB)	Aug. 23, 2014	Apr. 30, 2015	Terminated	PTAB	SMART Modular Technologies Inc. v. Netlist, Inc.	IPR2014-01370

PARTIES

Party	Party Role	Firm	Attorneys
Netlist, Inc.	PATENT OWNER	McAndrews Held & Malloy	Gregory C Schodde, Ronald H Spuhler, Scott P McBride, Thomas J Wimbiscus, Wayne H Bradley
Smart Modular Technologies, Inc.	PETITIONER	King & Spalding	Michael F Heafey, Sanjiva K Reddy

PATENTS

Number	Inventor	Name
8301833	Chen	Non-volatile memory module

SMART Modular Technologies Inc. v. Netlist, Inc. IPR2014-01371 (PTAB)	Aug. 23, 2014	Apr. 30, 2015	Terminated	PTAB	SMART Modular Technologies Inc. v. Netlist, Inc.	IPR2014-01371

PARTIES

Party	Party Role	Firm	Attorneys
Netlist, Inc.	PATENT OWNER	McAndrews Held & Malloy	Gregory C Schodde, Ronald H Spuhler, Scott P McBride, Thomas J Wimbiscus, Wayne H Bradley
Smart Modular Technologies, Inc.	PETITIONER	King & Spalding	Michael F Heafey, Sanjiva K Reddy

PATENTS

Number	Inventor	Name
8516187	Chen	Data transfer scheme for non-volatile memory module

SanDisk Corporation v. Netlist, Inc. IPR2014-00994 (PTAB)	Jun. 20, 2014	Jun. 02, 2015	Terminated	PTAB	SanDisk Corporation v. Netlist, Inc.	IPR2014-00994

PARTIES

Party	Party Role	Firm	Attorneys
Netlist, Inc.	PATENT OWNER	McAndrews Held & Malloy	Gregory C Schodde, Ronald H Spuhler, Scott P McBride, Thomas J Wimbiscus, Wayne H Bradley
SanDisk LLC f/k/a SanDisk Corp.	PETITIONER	Jones Day	David B Cochran, Joseph M Sauer, Joshua R Nightingale

PATENTS

Number	Inventor	Name
8301833	Chen	Non-volatile memory module

SanDisk Corporation v. Netlist, Inc. IPR2014-00982 (PTAB)	Jun. 19, 2014	Jun. 03, 2015	Terminated	PTAB	SanDisk Corporation v. Netlist, Inc.	IPR2014-00982

PARTIES

Party	Party Role	Firm	Attorneys
Netlist, Inc.	PATENT OWNER	McAndrews Held & Malloy	Gregory C Schodde, Ronald H Spuhler, Scott P McBride, Thomas J Wimbiscus, Wayne H Bradley
SanDisk LLC f/k/a SanDisk Corp.	PETITIONER	Jones Day	David B Cochran, Joseph M Sauer, Joshua R Nightingale

PATENTS

Number	Inventor	Name
8516187	Chen	Data transfer scheme for non-volatile memory module

Petitioners
Ex. 1002, p. 172

Netlist, Inc v. Smart Modular Technologies, Inc. et al 4-13-cv-05889 (NDCA)	Dec. 19, 2013	May. 19, 2020	Terminated	NDCA	Netlist, Inc v. Smart Modular Technologies, Inc. et al	4-13-cv-05889

PARTIES

Party	Party Role	Firm	Attorneys
Netlist, Inc.	PLAINTIFF, COUNTER DEFENDANT	Bartko Zankel Bunzel & Miller	Benjamin K Riley, Robert H Bunzel, Simon R Goodfellow, Sony B Barari, W Paul Schuck
Netlist, Inc.	PLAINTIFF, COUNTER DEFENDANT	DLA Piper	Erin P Gibson, Rajiv S Dharnidharka, Ryan W Cobb, Sean C Cunningham, Stanley J Panikowski, III
Netlist, Inc.	PLAINTIFF, COUNTER DEFENDANT	Keller Rackauckas Umberg Zipser	Dean J Zipser
Netlist, Inc.	PLAINTIFF, COUNTER DEFENDANT	McAndrews Held & Malloy	Gregory C Schodde, Ronald H Spuhler, Shawn L Peterson, Thomas J Wimbiscus, Wayne H Bradley
Netlist, Inc.	PLAINTIFF, COUNTER DEFENDANT		Wayne H Bradley
Smart Modular Technologies, Inc.	DEFENDANT	Orrick Herrington & Sutcliffe	Howard M Ullman, Matthew H Poppe, Michael F Heafey, Monte M F Cooper, Robert A Rosenfeld
Smart Worldwide Holdings Inc	DEFENDANT	King & Spalding	Anup M Shah
Smart Worldwide Holdings Inc.	DEFENDANT	Orrick Herrington & Sutcliffe	Howard M Ullman, Matthew H Poppe, Michael F Heafey, Monte M F Cooper, Robert A Rosenfeld
Diablo Technologies, Inc.	DEFENDANT, COUNTER CLAIMANT	King & Spalding	Jason Blake Cunningham
Diablo Technologies, Inc.	DEFENDANT, COUNTER CLAIMANT	McDermott Will & Emery	Barrington E Dyer, Daniel E Alberti, Fabio E Marino, Judith S H Hom, L Kieran Kieckhefer, Natalie A Bennett, Nitin Gambhir, Teri H P Nguyen
Diablo Technologies, Inc.	DEFENDANT, COUNTER CLAIMANT	Orrick Herrington & Sutcliffe	Michael F Heafey
Diablo Technologies, Inc.	DEFENDANT, COUNTER CLAIMANT	Steptoe & Johnson	Douglas R Peterson, Sanjeet K Dutta, William F Abrams
SanDisk LLC f/k/a SanDisk Corp.	DEFENDANT, COUNTER CLAIMANT	Jones Day	Gregory L Lippetz, Kathleen D Lynott, Steven J Corr, Tharan G Lanier
Smart Storage Systems, Inc.	DEFENDANT, COUNTER CLAIMANT	Jones Day	Gregory L Lippetz, Kathleen D Lynott, Steven J Corr, Tharan G Lanier
Smart Storage Systems, Inc.	DEFENDANT, COUNTER CLAIMANT	Orrick Herrington & Sutcliffe	Michael F Heafey

PATENTS

Number	Inventor	Name
7881150	Solomon	Circuit providing load isolation and memory domain translation for memory module
8001434	Lee	Memory board with self-testing capability
8081536	Solomon	Circuit for memory module
8301833	Chen	Non-volatile memory module
8359501	Lee	Memory board with self-testing capability
8516185	Lee	System and method utilizing distributed byte-wise buffers on a memory module
8516187	Chen	Data transfer scheme for non-volatile memory module

Petitioners
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Diablo Technologies, Inc. v. Netlist, Inc. 4-13-cv-03901 (NDCA)	Aug. 23, 2013	Apr. 08, 2014	Terminated	NDCA	Diablo Technologies, Inc. v. Netlist, Inc.	4-13-cv-03901

PARTIES

Party	Party Role	Firm	Attorneys
Diablo Technologies, Inc.	PLAINTIFF, COUNTER DEFENDANT	King & Spalding	Jason Blake Cunningham, Michael F Heafey, Sanjeet K Dutta, William F Abrams
Diablo Technologies, Inc.	PLAINTIFF, COUNTER DEFENDANT	Steptoe & Johnson	Douglas R Peterson
Netlist, Inc.	DEFENDANT, COUNTER CLAIMANT	Banko Zankel Bunzel & Miller	Benjamin K Riley, Robert H Bunzel, Simon R Goodfellow, Sony B Barari, W Paul Schuck
Netlist, Inc.	DEFENDANT, COUNTER CLAIMANT	DLA Piper	Erin P Gibson, Rajiv S Dharnidharka, Ryan W Cobb, Sean C Cunningham, Stanley J Panikowski, III
Netlist, Inc.	DEFENDANT, COUNTER CLAIMANT	McAndrews Held & Malloy	Gregory C Schodde, Thomas J Wimbiscus, Wayne H Bradley
Netlist, Inc.	DEFENDANT, COUNTER CLAIMANT		Gregory C Schodde
Smart Modular Technologies, Inc.	THIRD-PARTY PLAINTIFF	King & Spalding	Michael F Heafey

PATENTS

Number	Inventor	Name
7881150	Solomon	Circuit providing load isolation and memory domain translation for memory module
8001434	Lee	Memory board with self-testing capability
8081536	Solomon	Circuit for memory module
8301833	Chen	Non-volatile memory module
8359501	Lee	Memory board with self-testing capability
8516185	Lee	System and method utilizing distributed byte-wise buffers on a memory module
8516187	Chen	Data transfer scheme for non-volatile memory module

Smart Modular Technologies, Inc. v. Netlist, Inc. 4-13-cv-03916 (NDCA)	Aug. 23, 2013	Feb. 12, 2014	Terminated	NDCA	Smart Modular Technologies, Inc. v. Netlist, Inc.	4-13-cv-03916

PARTIES

Party	Party Role	Firm	Attorneys
Smart Modular Technologies, Inc.	PLAINTIFF, COUNTER DEFENDANT	King & Spalding	Jason Blake Cunningham, Michael F Heafey, Sanjeet K Dutta, William F Abrams
Netlist, Inc.	DEFENDANT, COUNTER CLAIMANT	Banko Zankel Bunzel & Miller	Benjamin K Riley, Robert H Bunzel, Simon R Goodfellow, Sony B Barari, W Paul Schuck
Netlist, Inc.	DEFENDANT, COUNTER CLAIMANT	DLA Piper	Erin P Gibson, Rajiv S Dharnidharka, Ryan W Cobb, Sean C Cunningham, Stanley J Panikowski, III
Netlist, Inc.	DEFENDANT, COUNTER CLAIMANT	McAndrews Held & Malloy	Gregory C Schodde, Thomas J Wimbiscus, Wayne H Bradley

PATENTS

Number	Inventor	Name
8001434	Lee	Memory board with self-testing capability
8301833	Chen	Non-volatile memory module
8359501	Lee	Memory board with self-testing capability
8516185	Lee	System and method utilizing distributed byte-wise buffers on a memory module
8516187	Chen	Data transfer scheme for non-volatile memory module

Petitioners
Ex. 1002, p. 174

Appendix A

Netlist, Inc v. Smart Modular Technologies, Inc 8-13-cv-00996 (CDCA)	Jul. 01, 2013	Dec. 23, 2013	Terminated	CDCA	Netlist, Inc v. Smart Modular Technologies, Inc	8-13-cv-00996

PARTIES

Party	Party Role	Firm	Attorneys
Netlist, Inc.	PLAINTIFF	DLA Piper	Erin P Gibson, Rajiv S Dharnidharka, Ryan W Cobb, Sean C Cunningham, Stanley J Panikowski, III
Netlist, Inc.	PLAINTIFF	Keller Rackauckas Umberg Zipser	Dean J Zipser
Netlist, Inc.	PLAINTIFF	McAndrews Held & Malloy	Gregory C Schodde, Thomas J Wimbiscus, Wayne H Bradley
Diablo Technologies, Inc.	DEFENDANT	King & Spalding	Jason Blake Cunningham, Sanjeet K Dutta
Diablo Technologies, Inc.	DEFENDANT	Orrick Herrington & Sutcliffe	Michael F Heafey
Diablo Technologies, Inc.	DEFENDANT	Steptoe & Johnson	William F Abrams
Smart Modular Technologies, Inc.	DEFENDANT	Orrick Herrington & Sutcliffe	Howard M Ullman, Matthew H Poppe, Michael F Heafey, Monte M F Cooper, Robert A Rosenfeld
Smart Modular Technologies, Inc.	DEFENDANT	Steptoe & Johnson	William F Abrams
Smart Storage Systems, Inc.	DEFENDANT	Jones Day	Gregory L Lippetz, Kathleen D Lynott, Steven J Corr
Smart Worldwide Holdings Inc.	DEFENDANT	Orrick Herrington & Sutcliffe	Howard M Ullman, Matthew H Poppe, Monte M F Cooper, Robert A Rosenfeld

PATENTS

Number	Inventor	Name
8001434	Lee	Memory board with self-testing capability
8301833	Chen	Non-volatile memory module
8359501	Lee	Memory board with self-testing capability
8516185	Lee	System and method utilizing distributed byte-wise buffers on a memory module
8516187	Chen	Data transfer scheme for non-volatile memory module

Petitioners
Ex. 1002, p. 175

Electronic Patent Application Fee Transmittal

Application Number:	17138766
Filing Date:	30-Dec-2020
Title of Invention:	FLASH-DRAM HYBRID MEMORY MODULE
First Named Inventor/Applicant Name:	Hyun Lee
Filer:	Khaled Shami/Stephanie Semler
Attorney Docket Number:	0016.001000H

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
SUBMISSION- INFORMATION DISCLOSURE STMT	1806	1	260	260
		Total in USD ($)		**260**

Electronic Acknowledgement Receipt	
EFS ID:	42149047
Application Number:	17138766
International Application Number:	
Confirmation Number:	8804
Title of Invention:	FLASH-DRAM HYBRID MEMORY MODULE
First Named Inventor/Applicant Name:	Hyun Lee
Customer Number:	151145
Filer:	Khaled Shami/Stephanie Semler
Filer Authorized By:	Khaled Shami
Attorney Docket Number:	0016.001000H
Receipt Date:	11-MAR-2021
Filing Date:	30-DEC-2020
Time Stamp:	19:24:54
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	$260
RAM confirmation Number	E20213AJ27051960
Deposit Account	602034
Authorized User	Stephanie Semler
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: 37 CFR 1.16 (National application filing, search, and examination fees) 37 CFR 1.17 (Patent application and reexamination processing fees)	

37 CFR 1.19 (Document supply fees)

37 CFR 1.20 (Post Issuance fees)

37 CFR 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Form (SB08)	20210309_IDS_0016001000H_1_OF_4.pdf	1061508 d2087e571cff87c57ecbbcc51581f4f17f87fded	no	25
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Information:					
2	Information Disclosure Statement (IDS) Form (SB08)	20210309_IDS_0016001000H_2_OF_4.pdf	1056127 09e3bd6e50f7527c0c545b481049e3abbe6873a7	no	8
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Information:					
3	Information Disclosure Statement (IDS) Form (SB08)	20210309_IDS_0016001000H_3_OF_4.pdf	1055481 f7e5e6311417c57eb3c5e2be48d9b7a681e9d05a	no	8
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Information:					
4	Information Disclosure Statement (IDS) Form (SB08)	20210309_IDS_0016001000H_4_OF_4.pdf	1055382 9bc18ca9eb17b63d6c4cdce0858d48e87cd6db09	no	7
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Information:					
5	Foreign Reference	IDS1_FP2_KR0130873Y1_and_Translation.pdf	402370 dbc2f7b0071a4338cd2e0c7607a40023f94526c0	no	8
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Information:					
6	Foreign Reference	IDS1_FP3_KR100606242B1_and_Translation.pdf	965386 8cfce5bf3cd020ec029d60b7f5b58d314e7165d9	no	32
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Information:					

7	Non Patent Literature	IDS1_NPL2_DrawingbyDr_Baker_AddressofDRAM_and_FLASH_PTAB_IPR2017_00587_1023.pdf	133927 479777e8b46a22b09082e7bf9e99d524a9e662a0	no	1
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Information:					
8	Non Patent Literature	IDS1_NPL1_THIRD_AMENDED_COMPLAINT_FOR_PATENT_INFRINGEMENT_NDCA413cv05889_267.pdf	203729 f95c9bc00e62e08ead951ceda614fd985c81fe99	no	21
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Information:					
9	Non Patent Literature	IDS1_NPL8_Amendment_and_Reply_to_Office_Action_IPR2014_00982.pdf	557562 5016da648e134cf23081d7d93b9beba47f1016ae	no	24
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10	Non Patent Literature	IDS1_NPL9_Ex_1004_Amendment_and_ReplyElection_Rest.pdf	913188 77680fe21ed5f65720de6114879020fc8edd06c2	no	9
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11	Non Patent Literature	IDS1_NPL10_Excerpts_from_the_American_Heritage_Dictionary1996_PTAB_IPR2017_00587_2014.pdf	1788746 768097f835c83ba5c0454503c4f9ba46ad39db90	no	7
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Information:					
12	Non Patent Literature	IDS1_NPL10_Excerpts_from_the_AmericanHeritageDictionary1996_PTAB_IPR2017_00587_2014.pdf	1358996 bb5326fa3e56954a2e3c55d303280470355 56ed5	no	7
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13	Non Patent Literature	IDS1_NPL12_Ex2016_134_Annotated_Exhibit1026ofBakerDepos12182017_PTAB_IPR2017_00587_1026.pdf	174992 a853db46bf1006bc6cf41fbcd10270a2053547a1	no	1
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14	Non Patent Literature	IDS1_NPL13_Ex_2016_135_Annotated_Exhibit_1027ofBakerDepos12182017_PTAB_IPR2017_00587_1027.pdf	173996 a6169e47316a46f9cd71e728a7d9eaac9cd4a64c	no	1
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15	Non Patent Literature	IDS1_NPL14_Ex_2016_135_Annotated_Exhibit_1028ofBaker_Deposi12182017_PTAB_IPR2017_00587_1028.pdf	1310232 7437b919cf8d136e27a31f76284fac9952e0462a	no	1
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16	Non Patent Literature	IDS1_NPL22_Charles_Multiplexers_and_Demultiplexers_Ex_1035_PTAB_IPR2017_00587_1035.pdf	1506358 9881437f56136a93a324aae7fde4b7be0ed05490	no	8
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17	Non Patent Literature	IDS1_NPL26_DECLARATION_OF_MICHAEL_FHEAFEY_PTABIPR2014013701011.pdf	569636 b8bb5d50e1c06e5fca592813fa7fe4ee25d1377d	no	4
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18	Non Patent Literature	IDS1_NPL27_d_Petition_For_Inter_Partes_Review_PTAB_IPR2014_01371_7.pdf	1049330 d1b6f376df468a91cd100979c94c980741c96b90	no	67
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Information:					
19	Non Patent Literature	IDS1_NPL28_Ex_Corrected_Petiton_DECLARATIONOFDRNADERBAGHERZADEH_PTAB_IPR2014_01371_012.pdf	5546098 0f59acc05350f1a10cd83c634f8e698d310c8e7c	no	306
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20	Non Patent Literature	IDS1_NPL31_Decision_Denying_Institution_of_Inter_Partes_Review_PTAB_IPR2014_01371_12.pdf	393606 e642ef16c7394ec7231f7db0fa83fdb0c46d7f7b	no	22
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21	Non Patent Literature	IDS1_NPL33_Decision_Denying_Institution_of_Inter_PartesReview_PTAB_IPR2014_00994_8.pdf	392031 2ad1654ce0fbee9ca107f21c6e42d277a4d6cab1	no	16
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22	Non Patent Literature	IDS1_NPL34_Decision_Denying_Institution_of_Inter_Partes_Review_37CFR42108_PTAB_IPR2014_00982_9.pdf	379782 aa0816d24033b9cfb9e5dba38023d823cd222295	no	16
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Information:					
23	Non Patent Literature	IDS1_NPL35_Decision_Denying_Institution_of_Inter_Partes_Revew_PTAB_IPR2014_01370_13.pdf	413442 fa56f51f3a434cad2c1a4c86e8496a1ba079f744	no	19
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24	Non Patent Literature	IDS1_NPL36_Decision_Instituted_Document_PTAB_IPR2017_00587_7.pdf	444263 7345661f6946803fc5849eba1efa9a2841c0a2fd	no	40
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25	Non Patent Literature	IDS1_NPL38_Ex_Declaration_of_R_Jacob_BakerPhDPE_PTAB_IPR2017_00692_2016.pdf	2006241 9a69b0f3f7fd97182adad97367d8993a8e988ba8	no	72
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26	Non Patent Literature	IDS1_NPL39_Declaration_of_R_JacobBakerPhDPEEx_2016_PTAB_IPR2017_00587_2016.pdf	2450517 7d1afd2a2ba7fe286938c9738418fda337945ec0	no	109
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27	Non Patent Literature	IDS1_NPL40_Ex_Declaration_of_Dr_Nader_PTAB_IPR2014-0130_1010.pdf	5984516 7cdb98de87d8e5949930654a1ea0b1c470a82d7	no	333
Warnings:					
Information:					

28	Non Patent Literature	IDS1_NPL41_DECLARATION_OF_JEFF_MCMlLLEN.pdf	100607 85b7155fe9c83ea638eaf9836f1cc783af2d6ab5	no	3
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29	Non Patent Literature	IDS1_NPL42_Ex_Declaration_of_Paul_Min_PTAB_IPR2014009 94_1020.pdf	4188828 6c11a27ad0a4fec1bc33fc7d717cecd44d8d9984	no	215
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30	Non Patent Literature	IDS1_NPL43_Declaration_of_Paul_Min_PTAB_IPR2014_00982_1013.pdf	3562443 75d2af964e22ff7afc85e264d9753fe0618f8b18	no	240
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31	Non Patent Literature	IDS1_NPL44_Declaration_of_Ron_Maltiel_RegardingUSPatent No_8671243_PTAB_IPR2017_0 0587_1003.pdf	2554536 3b507b13aad3695df5ad1736418f356ee638ea2d	no	131
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32	Non Patent Literature	IDS1_NPL45_Declaration_of_RonMaltielre831Patent_PTAB_IPR2017_00692_1003.pdf	2188026 f0ae06aa438f7293cc044c7e76cbfb0760d94a57	no	172
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33	Non Patent Literature	IDS1_NPL46_DECLARATION_OF_STEVENJCORR.pdf	145148 7b323c2167fb049fae23695d09b33fe4273e77fb	no	3
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34	Non Patent Literature	IDS1_NPL47_Baker_Deposition_Transcript_December182017_PTAB_IPR2017_00587_1030.pdf	1144729 7d26b8d4b6ca36a40c599ca2574cc1b2543881e5	no	268
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35	Non Patent Literature	IDS1_NPL48_Ex_Deposition_transcript_of_Ron_Maltiel_PTAB_IPR2017_00692_2010.pdf	6994059 2ab9d657d82dcd9d7fa20c73a203e8d1e6a4e8cc	no	155
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36	Non Patent Literature	IDS1_NPL19_Charles_Multiplexers_andDemultiplexersPTAB_IPR2017_00587_024.pdf	959653 e4c0fb645933582fa148dc775fdfc277860b794b	no	10
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37	Non Patent Literature	IDS1_NPL20_Charles_Multiplexers_andDemultiplexers_Ex1033_PTAB_IPR201700587_1033.pdf	1695832 0c39e2c92595a41e464a56bd6560f99a6d7a718b	no	8
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38	Non Patent Literature	IDS1_NPL21_Charles_Multiplexers_and_Demultiplexers_Ex1034_PTAB_IPR2017-00587_1034.pdf	2320813 b8ddd49a213bbe9ff26c4ee190b427f8b27cbe33	no	8
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39	Non Patent Literature	IDS1_NPL15_Federal_Circuit_Appeal_2016_1742_PTAB_IPR2017_00587_2015.pdf	174201 fb4db84dcbf772b277130618fc23197b4e8e2db6	no	8
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40	Non Patent Literature	IDS2_NPL5_Ex_1002_Application_As_Filed_PTAB_IPR2014_00994_1002.pdf	2780890 39d9304a6836dc7c49aa3e0a6a49e1c6eea3c80b	no	52
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41	Non Patent Literature	IDS2_NPL6_Ex_8_Denying_Institution_of_Inter_Partes_Review.pdf	381534 fba87b84ebe22850fe9120638c6ef805b0714348	no	23
Warnings:					
Information:					

42	Non Patent Literature	IDS2_NPL7_Decision_Case413cv05889_YGR_Document309_4_Filed031715.pdf	406089 763e8f8a525d8e57b785b2b3f623a2b88fa6ff7d	no	20
Warnings:					
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43	Non Patent Literature	IDS2_NPL8_Decision_Case_413cv05889YGR_Document309_5_Filed031715.pdf	900606 63623c2a0323732bd65b7af9898c3c0f04fb542b	no	28
Warnings:					
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44	Non Patent Literature	IDS2_NPL9_Decision_IPR_Case_413cv05889YGR_Document_316_9_Filed_032415.pdf	469523 02326569c73813e6e83c7a32958326073120d0e9c	no	29
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Information:					
45	Non Patent Literature	IDS2_NPL10_Decision_Case413cv05889YGRDocument3097Filed031715.pdf	362203 f26dd12e4d3fa5d4fb3f2a52a6985410497a4c00	no	17
Warnings:					
Information:					
46	Non Patent Literature	IDS2_NPL13_Ex_6_Institution_of_Inter_Partes_Review.pdf	470815 853ab569e1251c978e1dbc2a3cc1718c904d6f98	no	22
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47	Non Patent Literature	IDS2_NPL16_Ex_Letter_Case413cv05889YGRDocument305_16_Filed031015.pdf	106828 f5388fd1f8f3c1bfbdc5d0d7d36c7977ef0966b9	no	3
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48	Non Patent Literature	IDS2_NPL17_Ex_email_Case_413cv03901YGR_Document53_2Filed010614.pdf	305003 cc01306ce90629ecc31623c5a8fe7e396d46f9de	no	3
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49	Non Patent Literature	IDS2_NPL18_ORDER_DENYING_DEFENDANTS_MOTION_TO_STAY_PENDING_INTER_PARTES_REVIEW.pdf	167274 a8e0db24b23f5a0060a188f699ef74ee1384b681	no	10
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50	Non Patent Literature	IDS2_NPL19_Ex_13_USPTO_AppealsStatistics.pdf	1492920 ec5aaa0af27d51a3be9a257c17b546c20036fb25	no	23
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51	Non Patent Literature	IDS2_NPL21_REPORTERS_TRANSCRIPT_OF_PROCEEDINGS.pdf	211764 5df61a611ab8792814879cafabb3469aaa0933d4	no	15
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52	Non Patent Literature	IDS2_NPL22_Ex_TRANSCRIPT_OF_OFFICIAL_ELECTRONIC_SOUND_RECORDING_OF_PROCEEDINGS.pdf	121364 cceb10d7972cf4e2c093f2b3a010f67700dd74a0	no	10
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53	Non Patent Literature	IDS2_NPL30_FINAL_WRITTEN_DECISION_PTAB_IPR2017_00692_25.pdf	871272 7d788a881277026fd3429860731797a9f931e828	no	42
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54	Non Patent Literature	IDS2_NPL33_Ex_Hasan_etal_PTAB_IPR2017_00692_1026.pdf	258448 a432a50e2968c0e737fc98029c024a74daab109d	no	12
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55	Non Patent Literature	IDS2_NPL37_PETITION_FOR_INTERPARTESREVIEW_PTAB_IPR2017_00692_1.pdf	764405 481378d6e15e30eaf2daad68d5b8caa01ec6a840	no	78
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56		RespNFOA_0016001000H.pdf	176445 9243ae4ea7a31323272bc94a40f0317b9e192440	yes	12
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	Document Description		**Start**	**End**	
	Amendment/Req. Reconsideration-After Non-Final Reject		1	1	
	Claims		2	9	
	Applicant Arguments/Remarks Made in an Amendment		10	12	
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57	Notice of concurrent proceedings / decisions	0016001000H_Notice_Related_Litigation_and_Appendix_A2.pdf	292145 966de13502c43242708d63e6245e0dd30aa56ab7	no	7
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58	Fee Worksheet (SB06)	fee-info.pdf	30208 10e88fe64c995c30fe30caa498080e1c179dd5a8	no	2
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Information:					
		Total Files Size (in bytes):	69946053		

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New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.
National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.
New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (02-18)
Approved for use through 11/30/2020. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**		
	Application Number	17138766
	Filing Date	2020-12-30
	First Named Inventor	Hyun Lee
	Art Unit	1731
	Examiner Name	
	Attorney Docket Number	0016.001000H

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	2043099	A	1936-06-02	Hanna	Entire Document
	2	3562555	A	1971-02-09	Ahrons	Entire Document
	3	3916390	A	1975-10-28	Chang et al.	Entire Document
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	28	Corrected Petition for Inter Partes Review of Claims 1-32 of US Patent No. 8,516,187, Declaration of Dr. Nader Bagherzadeh, IPR2014-01371 (PTAB), filed September 22, 2014, 306 pages.	

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	29	Data Sheet, 74F257A Quad 2-line to 1-line selector/multiplexer, non-inverting (3-State), Product specification, IC15 Data Handbook Mar. 31, 1995, 10 pages.	
	30	David, H. et al., "Fully Buffered DIMM (FB-DIMM) Design Considerations", Intel Developer Forum, Intel Corp., Feb. 18, 2004, 36 pages.	
	31	Decision Denying Institution of Inter Partes Review, Patent 8,301,833, Case IPR2017-00649 (PTAB), Paper 7, entered July 24, 2017, 17 pages.	
	32	Decision Denying Institution of Inter Partes Review, Patent No. 8,516,187, IPR2014-01371 (PTAB), Paper 12, entered March 13, 2015, 22 pages.	
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	35	Decision Denying Institution of Inter Partes Review, Smart Modular Tech v Netlist Inc., Patent No. 8,301,833, IPR2014-01370 (PTAB), Paper 13, entered March 13, 2015, 19 pages.	
	36	Decision Instituting Inter Partes Review, Patent 8,671,243, Case No. IPR2017-00587-7(PTAB), Paper No. 7, entered June 22, 2017, 40 pages.	
	37	Decision Instituting Inter Partes Review, Patent 8,874,831, Case No. IPR2017-00692-7(PTAB), Paper No. 7, entered July 21, 2017, 40 pages.	
	38	Declaration of R. Jacob Baker, Patent No. 8,874,831, Case IPR2017-00692-2016 (PTAB), filed Nov. 10, 2017, 72 pages.	
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	40	Declaration of Dr. Nader Bagherzadeh, Patent No. 8,301,833, IPR2014-01370-1010 (PTAB), filed September 22, 2014, 333 pages.	
	41	Declaration of Jeff McMullen, Netlist, Inc. v. Diablo Technologies, Inc., Case No. 4: I 3-CV-05889-YGR (NDCA), Document 362-1, filed September 5, 2018, 3 pages.	
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	44	Declaration of Ron Maltiel, Patent No. 8,671,243, No. IPR2017-00587-1003 (PTAB), filed May 29, 2013, 131 pages.	
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	1	Elmhurst et al., "A 1.8-V 128-Mb 125-MHz Multilevel Cell Flash Memory With Flexible Read While Write", IEEE Journal of Solid-State Circuits 38(11):1929-1933 (2003).	
	2	Elmhurst, D. et al., A 1.8-V 128-Mb 125-MHz Multilevel Cell Flash Memory With Flexible Read While Write, IEEE Journal of Solid-State Circuits, Vol. 38, No. 11, Nov. 2003, 5 pages.	
	3	Ex. 1004—IPR2017-00587 Ron Maltiel CV, 7 pages.	
	4	Exhibit 1: Claim Chart Comparing Netlist's US Patent No. 8,001,434 to Smart Storage Ulltradimm, Case4:13-cv-05889-YGR Document 193-1, filed Apr. 10, 2014, 21 pages.	
	5	Exhibit, Application As Filed, SanDisk Corporation v. Netlist, Inc., Patent 8,301,833, IPR2014-00994 (PTAB), 52 pages.	
	6	Exhibit, Decision Denying Institution of Inter Partes Review, Smart Modular Technologies, Inc. v. Netlist, Inc., Case No. 4:13-cv-05889-YGR Document 309-3, filed March 17, 2015, 23 pages.	
	7	Exhibit, Decision Denying Institution of Inter Partes Review, Smart Modular Technologies, Inc. v. Netlist, Inc., Case No. 4:13-cv-05889-YGR Document 309-4, filed March 17, 2015, 20 pages.	
	8	Exhibit, Decision Denying Institution of Inter Partes Review, Smart Modular Technologies, Inc. v. Netlist, Inc., Case No. 4:13-cv-05889-YGR Document 309-5, filed March 17, 2015, 28 pages.	
	9	Exhibit, Decision Denying Institution of Inter Partes Review, Smart Modular Technologies, Inc. v. Netlist, Inc., Case No. 4:13-cv-05889-YGR Document 309-9, filed March 17, 2015,17 pages.	
	10	Exhibit, Decision Denying Institution of Inter Partes Review, Smart Modular Technologies, Inc. v. Netlist, Inc., Case No. 4:13-cv-05889-YGR Document 309-7, filed March 17, 2015, 17 pages.	
	11	Exhibit, Email from Defendant's Counsel, Netlist v. Smart Storage Systems, Inc. et. al., Case 4:13-cv-05889-YGR Document 305-17, filed March 10, 2015, 6 pages.	

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	12	Exhibit, Institution of Inter Partes Review, Sandisk Corporation v. Netlist, Inc., Case 4:13-cv-05889-YGR Document 316-9, filed March 24, 2015, 29 pages.	
	13	Exhibit, Institution of Inter Partes Review, Smart Modular Technologies, Inc. v. Netlist, Inc., Case 4:13-cv-05889-YGR Document 309-1, filed March 17, 2015, 22 pages.	
	14	JEDEC Standard, Double Data Rate (DDR) SDRAM Specification, JESD79, Jun. 2000, 77 pages.	
	15	Exhibit, Institution of Inter Partes Review, Smart Modular Technologies, Inc. v. Netlist, Inc., Case No. 4:13-cv-05889-YGR Document 309-2, filed March 17, 2015, 23 pages.	
	16	Exhibit, Letter from Defendant's Counsel, Netlist v. Smart Storage Systems, Inc. et. al., Case 4:13-cv-05889-YGR Document 305-16, filed March 10, 2015, 3 pages.	
	17	Exhibit, Letter sent via email on December 6, 2013, Case 4:13-cv-03901-YGR Document 53-2, filed January 6, 2014	
	18	Exhibit, Order Denying Defendant's Motion to Stay Pending Inter Partes Review (Doc.59), The Procter and Gamble Company v. Team Technologies, Inc, et al., Case 4:13-cv-05889-YGR Document 316-6, filed March 24, 2015, 10 pages.	
	19	Exhibit, Patent Public Advisory Committee Quarterly Meeting, Appeals Statistics USPTO, Case No. 4:13-cv-05889-YGR Document 309-8, filed March 17, 2015, 23 pages.	
	20	Exhibit, Reporter's Transcript of Proceedings, Netlist, Inc v. Smart Modular Technologies, Inc., et al., Case 4:13-cv-05889-YGR Document 316-3, filed March 24, 2015, 15 pages.	
	21	Exhibit, Transcript of Official Electronic Sound Recording Proceeding, Netlist v. Smart Modular Technologies, Inc, et al., Case 4:13-cv-05889-YGR Document 305-7, filed March 10, 2015, 10 pages.	
	22	Extended European Search Report for European Application No. 12 817 751.6, dated Jun. 9, 2015.	

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	25	File History for U.S. Appl. No. 60/941,586, filed Jun. 1, 2007, 23 pages.	
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	27	Final Office Action, dated Jun. 15, 2016, issued in U.S. Appl. No. 14/489,281, 10 pages.	
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	29	Final Written Decision, Patent 8,671,243, IPR2017-00587-34, Paper No. 34, entered June 20, 2018, 53 pages.	
	30	Final Written Decision, Patent 8,874,831, IPR2017-00692, Paper No. 25, entered July 5, 2018, 42 pages.	
	31	Final Written Decision, US Patent No. 7,881,150, Case No. Case IPR2014-00882, (PTAB), Paper 33, filed December 14, 2015, 51 pages.	
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	33	Hasan, J. et al. Efficient Use of Memory Bandwidth to Improve Network Processor Throughput, Proceedings of the 30th Annual International Symposium on Computer Architecture (ISCA'03), IEEE, 2003, 12 pages.	

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	34	Horowitz, P. et al., "The Art of Electronics", Cambridge University Press 2nd Ed. 1989, pp. 471495-496.	
	35	Innis, J., "MPC8560 PowerQUICC III Compact Flash Interface Design", Freescale Semiconductor, Inc., 2004-2006, pp. 1-23.	
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	37	Inter Partes Review No. IPR2017-00692 (PTAB), Patent No. 8,874,831, filed July 26, 2012, 78 pages.	
	38	Inter Partes Review of U.S. Patent No. 8,874,831, Case IPR2017-00692 (PTAB), filed July 26, 2012, Paper No. 1, 78 pages.	
	39	International Preliminary Report on Patentabillity in PCT/US12/48750, mailed Apr. 3, 2014pp. 1-8.	
	40	International Search Report and Written Opinion in PCT/US12/48750, dated Oct. 10, 2012pp. 1-10.	
	41	ISSCC 2006 / SESSION 7 / NON-VOLATILE MEMORY / 7.7, IEEE International Solid-State Circuits Conference, 2006, 10 pages.	
	42	Jacob, B., "Memory Systems Cache, DRAM, Disk", Morgan Kaufman Publishers, Burlington, MA, 2008, Preface and Ch. 7 pp. 315-322, 58 pages.	
	43	Jandhyala, S. et al., "Design-For-Test Analysis of a Buffered SDRAM DIMM", Semiconductor Group, Texas Instruments, Proceedings of International Workshop in Memory Technology, Design and Testing, Singapore, August 13014, 1996,15 pages.	
	44	JEDEC Definition of DIMM, Exhibit 1029, IPR No. 2017-00587, December 18, 2017, 2 pages.	

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	45	JEDEC Global Standard for the Microelectronics Industry, Why JEDEC Standards Matter, 2014, 1 page.	
	46	JEDEC Standard 21-C"Configurations for Solid State Memories," pp. 4.5.5-1 to 4.5.5-18.	
	47	JEDEC Standard No. 21-C (Release 17), Annex J: Serial Presence Detects for DDR2 SDRAM (Revision 1.3), 60 pages.	
	48	JEDEC Standard, "Configurations for Solid State Memories", JEDEC Standard 21-C, Release 9, Aug. 1999, 114 pages.	
	49	JEDEC Standard, DDR2 SDRAM Specification, JESD79-2B (Revision of JESD79-2A) Jan. 2005, 113 pages.	

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7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

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	Application Number	17138766
	Filing Date	2020-12-30
	First Named Inventor	Hyun Lee
	Art Unit	1731
	Examiner Name	
	Attorney Docket Number	0016.001000H

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	1	JEDEC Standard, FBDIMM Specification: DDR2 SDRAM Fully Buffered DIMM (FBDIMM) Design Specification: JESD205, JEDEC Solid State Tech. Assoc., Mar. 2007, 9 pages.	
	2	Joint Status Report Regarding Inter Partes Review, Netlist v. Smart Storage Systems, Inc. et. al., Case No. 4:13-CV-05889-YGR (NDCA), filed August 17, 2018, 4 pages.	
	3	Material Science & Engineering, Department of Material Science and Engineering, Stanford University, Exhibit 2011, Case No. IPR2017-00692, 2 pages.	
	4	Merriam-Webster's Collegiate Dictionary, Eleventh Ed., Merriam Webster Corporation, Springfield, MA, 2003, 7 pages.	
	5	Microsoft Computer Dictionary Fifth Edition, 2002, 3 pages.	
	6	Microsoft Computer Dictionary Fifth Edition, 2002, 9 pages.	
	7	Microsoft Press, Computer Dictionary, Second Edition, 1994, 4 pages.	
	8	Microsoft Windows 2000 Professional Resource Kit, 76 pages.	
	9	Mutnuary, B. et al., "Analysis of Fully Buffered DIMM Interface in High-speed Server Applications", IBM Corp, xSeries eServer Development, 2006 Electronic Components and Technology Conference, pp. 203-208.	
	10	Notice of Allowance in U.S. Appl. No. 12/240,916, dated Sep. 17, 2012.	
	11	Notice of Allowance in U.S. Appl. No. 13/536,173, dated Jul. 2, 2013.	

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	12	Notice of Allowance in U.S. Appl. No. 13/559,476, dated May 6, 2014.	
	13	Notice of Allowance in U.S. Appl. No. 13/559,476, dated Sep. 29, 2014.	
	14	Notice of Allowance in U.S. Appl. No. 13/905,048, dated Dec. 19, 2013, 8 pages.	
	15	Notice of Allowance in U.S. Appl. No. 13/905,053, dated Dec. 11, 2013.	
	16	Notice of Allowance in U.S. Appl. No. 14/173,219 dated Jul. 7, 2014.	
	17	Notice of Allowance in U.S. Appl. No. 14/489,269, dated Oct. 8, 2015.	
	18	Notice of Allowance, SanDisk Corporation v. Netlist, Application No. 13/536,173, IPR2014-00982 (PTAB), dated July 2, 2013, 8 pages.	
	19	Office Action dated Aug. 19, 2016 of the Chinese Patent Application No. 201280047758.X, 9 pages.	
	20	Office Action in U.S. Appl. No. 12/240,916, mailed on Apr. 3, 2012.	
	21	Office Action in U.S. Appl. No. 13/536,176, dated on Apr. 15, 2013.	
	22	Office Action in U.S. Appl. No. 13/625,563, dated Aug. 5, 2013.	

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	23	Office Action in U.S. Appl. No. 13/625,563, dated May 9, 2014.	
	24	Office Action in U.S. Appl. No. 13/905,048, dated Aug. 1, 2013.	
	25	Office Action in U.S. Appl. No. 13/905,053, dated Aug. 1, 2013.	
	26	Office Action in U.S. Appl. No. 14/173,219, dated Mar. 13, 2014.	
	27	Office Action in U.S. Appl. No. 14/302,292, dated Dec. 21, 2015.	
	28	Office Action in U.S. Application No. 12/240,916, dated Feb. 1, 2012, 14 pages.	
	29	Office Action in U.S. Application No. 14/173,242, dated March 14, 2014, 7 pages.	
	30	Office Action, Application 12/240,916, IPR2014-0099-1005 (PTAB), dated July 29, 2011, 8 pages.	
	31	Office Action, Application 12/240,916, IPR2014-0099-1010 (PTAB), dated April 3, 2012, 11 pages.	
	32	Office Action, Application No. 13/536,173, IPR2014-00982 (PTAB), dated April 15, 2013, 9 pages.	
	33	Order Granting Joint Stipulation of Dismissal, Netlist v. Smart Storage Systems, Inc. et. al., Case No. 4:13-CV-05889-YGR (NDCA), filed May 15, 2020, 2 pages.	

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	34	Patent Owner's Demonstratives, Patent Number: 8,671,243, Case No. IPR 2017-00587-2023, (PTAB), 57 pages.	
	35	Patent Owner's Listing of New Arguments and Evidence in Petitioners' Reply, Patent No. 8,671,243, Case No. IPR2017-00587 (PTAB), filed Jan. 29, 2018, 6 pages.	
	36	Patent Owner's Opposition to Petitioners' Motion to Exclude, Patent No. 8,874,831, Case No. IPR2017-00692 (PTAB), filed April 2, 2018, 2017, 11 pages.	
	37	Patent Owner's Preliminary Response, Patent Number: 8,516,187, Case IPR2014-01371 (PTAB), filed Dec. 16, 2014, 66 pages.	
	38	Patent Owner's Preliminary Response, SanDisk Corporation v. Netlist, Inc., Patent 8,301,833, IPR2014-00994 (PTAB), Paper 8, dated October 2, 2014, 60 pages.	
	39	Patent Owner's Preliminary Response, SanDisk Corporation v. Netlist, Patent Number: 8,516,187, IPR2014-00982 (PTAB), dated September 26, 2014, 57 pages.	
	40	Patent Owner's Preliminary Response, SK hynix Inc., et al., v. Netlist, Patent No. 8,301,833, Case No. IPR2017-00649 (PTAB), filed May 1, 2017, 67 pages.	
	41	Patent Owner's Preliminary Response, SK hynix Inc., et al., v. Netlist, Patent No. 8,874,831, Case No. IPR2017-00692 (PTAB), filed May 1, 2017, 48 pages.	
	42	Patent Owner's Preliminary Response, Smart Modular Tech v Netlist Inc., Patent No. 8,301,833, Case IPR2014-01370 (PTAB), filed Dec. 16, 2014, 66 pages.	
	43	Patent Owner's Response, Patent No. 8,671,243, Case No. IPR2017-00587-12 (PTAB), filed Oct. 13, 2017, 80 pages.	
	44	Patent Owner's Response, SK hynix Inc., et al., v. Netlist, Patent No. 8,874,831, Case No. IPR2017-00692-12 (PTAB), filed Nov. 10, 2017, 77 pages.	

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	45	Patterson et al., "Computer Organization & Design: The Hardware/Software Interface" Morgan Kaufmann Publishers, Inc. (1998), 71 pages.	
	46	Petition for Inter Partes Review of Claims 1-30 of US.PATENT No. 8,301,833, IPR2014-01370 (PTAB), filed August 22, 2014, 68 pages.	
	47	Petition for Inter Partes Review of U.S. Pat. No. 8,301,833 (on behalf of SanDisk, Corp.), filed Jun. 20, 2014.	
	48	Petition for Inter Partes Review of U.S. Pat. No. 8,301,833 (on behalf of SMART Modular Technologies, Inc.), filed Aug. 22, 2014.	
	49	Petition for Inter Partes Review of U.S. Pat. No. 8,301,833, filed Sep. 29, 2008.	
	50	Petition for Inter Partes Review of U.S. Pat. No. 8,516,187 (on behalf of SanDisk, Corp.), filed Jun. 19, 2014.	

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Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

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A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Khaled Shami/	Date (YYYY-MM-DD)	2021-03-11
Name/Print	Khaled Shami	Registration Number	38745

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

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	Attorney Docket Number	0016.001000H

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	1	Petition for Inter Partes Review of U.S. Pat. No. 8,516,187 (on behalf of SMART Modular Technologies, Inc.), filed Aug. 22, 2014.	
	2	Petition for Inter Partes Review of U.S. Pat. No. 8,671,243, filed May 29, 2013.	
	3	Petition for Inter Partes Review of U.S. Pat. No. 8,874,831, filed Jul. 26, 2012.	
	4	Wong, A. "The BIOS Optimization Guide", Adrian's Rojak Pot, Rev. 6.2, 1998-2001, 67 pages.	
	5	Petition for Inter Partes Review of U.S. Patent No. 8,301,833 (on behalf of SMART Modular Technologies, Inc.), filed Aug. 22, 2014.	
	6	US Patent Application No. 60/912,321, Case No. No. IPR2017-00692-1007 (PTAB), filed April 17, 2017, 42 pages.	
	7	Petition for Inter Partes Review of US Patent 8,516,187, IPR2014-00982 (PTAB), dated June 19, 2014, 67 pages.	
	8	Petition for Inter Partes Review of US Patent No. 8,671,243, Case No. IPR2017-00587-1(PTAB), May 29, 2013, 82 pages.	
	9	Petition for Inter Partes Review, SanDisk Corporation v. Netlist, Inc., Patent 8,301,833, IPR2014-00994 (PTAB), filed June 20, 2014, 69 pages.	
	10	Webster's II New College Dictionary, Houghton Mifflin Company, Boston, MA, 2001, pp. 259, 1115.	
	11	Videotaped Deposition of Russel Jacob Baker, Patent No. 8,671,243, Case Nos. IPR2017-00587-1030 (PTAB), filed December 18, 2017, 268 pages.	

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	12	Petitioners Demonstratives, SK hynix Inc., et al., v. Netlist, Inc., U.S. Patent No. 8,671,243, IPR2017-00587-1037, 89 pages.	
	13	Petitioners' Reply in Support of Its Motion to Exclude, U.S. Patent No. 8,874,831, Case No. IPR2017-00692, filed April 9, 2018, 8 pages.	
	14	Petitioners' Reply to Patent Owner's Response, Inter Partes Review No. IPR2017-00587-16, Patent No. 8,671,243, filed Jan. 12, 2018, 38 pages.	
	15	Petitioners' Reply, U.S. Patent No. 8,874,831, Case No. IPR2017-00692 (PTAB), Paper No. 15, filed March 2, 2018, 35 pages.	
	16	Petitioners' Request for Hearing, U.S. Patent No. 8,301,833, Case No. Case No. IPR2017-00649-2020 (PTAB), Paper No. 8, entered Aug, 23, 2017, 18 pages.	
	17	Prosecution History, Application No. 12,240,916, US Patent No. 8,301,833, SK hynix Inc v Netlist Inc, Case No. IPR2017-00649-1002 (PTAB), received date April 13, 2009, 320 pages.	
	18	Prosecution History, Application No. 13,559,476, US Patent No. 8,301,833, SK hynix Inc v Netlist Inc, Case No. IPR2017-00649-1002 (PTAB), received date Sep. 5, 2014, 312 pages.	
	19	Prosecution History, Provisional Application No. 60/941,586, SK hynix Inc v Netlist Inc, Case No. IPR2017-00649-1005 (PTAB), received date Oct. 15, 2012, 23 pages.	
	20	Provisional Application for Advance Dynamic Disk Memory Module, Specification, SK hynix Inc., V. Netlist, Inc., Case No. IPR2017-00649-1006 (PTAB), dated Dec. 8, 2005, 53 pages.	
	21	Provisional Application No. 60/912,321 filed Apr. 17, 2007.	
	22	Provisional Application No. 60/941,586 filed Jun. 1, 2007.	

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	23	Requirement for Restriction Election, SanDisk Corporation v. Netlist, Inc., Patent 8,301,833, IPR2014-00994-1003 (PTAB), dated March 31, 2019, 7 pages.	
	24	Restriction Requirement in U.S. Appl. No. 12/240,916, dated Mar. 31, 2011.	
	25	Search on Amazon Website for "memory module", downloaded Oct. 12, 2017, 6 pages.	
	26	Search Report (Updated) Prior Art Search for U.S.Patent No. 8,301,833, Global Patent Solutions, Nov. 24, 2020, 179 pages.	
	27	Search Report Prior Art Search for U.S.Patent No. 8,301,833, Global Patent Solutions, Nov. 2, 2020, 38 pages.	
	28	Second Amended Answer and Counterclaims to Plaintiff's Complaint for Declaratory Judgment, Diablo Technologies, Inc. v. Netlist, Inc., Case No. 4:13-CV-03901 (NDCA), YGR, filed February 17, 2014, 21 pages.	
	29	Smart Storage Systems, Inc's Invalidity Contentions, Case No. 4:13-cv-05889-YGR, dated Jun. 6, 2014.	
	30	Supplemental Declaration of Daniel E. Alberti in Response to Court Order [Docket No. 361] in Support of Motion to Withdraw as Counsel of Record, Netlist v. Smart Storage Systems, Inc. et. al., Case 4:13-cv-05889-YGR Document 362, filed September 5, 2018, 13 pages.	
	31	Supplemental Declaration of Ronald H. Spuhler, Netlist v. Smart Storage Systems, Inc. et. al., Case 4:13-cv-05889-YGR Document 305-1, filed March 10, 2015, 2 pages.	
	32	Supplemental Declaration of Steven J. Corr, Netlist v. Smart Storage Systems, Inc. et. al., Case 4:13-cv-05889-YGR Document 309, filed March 17, 2015, 3 pages.	
	33	Switches - DT Online, Switches, Exhibit 1022, Case No. IPR2017-00587, accessed October 13, 2017, 3 pages.	

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	34	U.S. Appl. No. 60/912,321, filed Apr. 17, 2007.	
	35	U.S. Office Action in U.S. Appl. No. 13/536,173, mailed on Apr. 15, 2013, pp. 1-10.	
	36	UPDATED JOINT CASE MANAGEMENT STATEMENT, U.S. DISTRICT COURT NORTHERN DISTRICT OF CALIFORNIA, Case No. 4:13-cv-03916-YGR, Document 53, filed January 6, 2014.	
	37	US Patent Application No. 12/240,916, Case No. IPR2017-00692-2018 (PTAB), dated Sep. 29, 2008, 52 pages.	

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That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

See attached certification statement.

☒ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Khaled Shami/	Date (YYYY-MM-DD)	2021-03-11
Name/Print	Khaled Shami	Registration Number	38745

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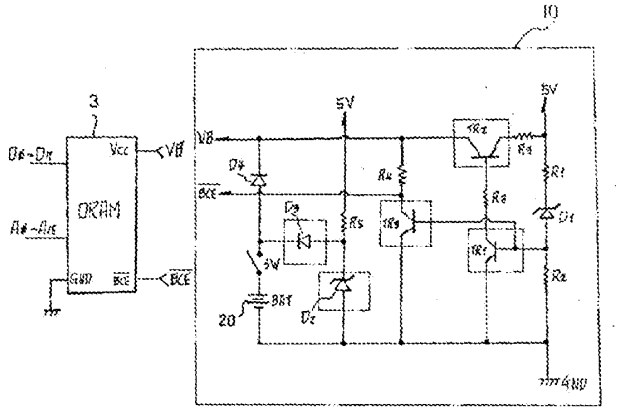
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요약

본 고안은 자동 예비전원 공급 장치에 관한 것으로, 특히 전원 공급 장치의 이상장애 발생시 데이터 처리장치에 구비된 휘발성 메모리(Volatile Memory)인 디램에 자동으로 예비전원을 공급하기 위한 자동 예비전원 공급 장치에 관한 것이다

본 고안의 데이터 처리장치용 휘발성 데이터 기억장치의 자동 예비 전원 공급 장치는 시스템 공급 전압이 일측에 인가되는 분압회로(R1,D1,R2)와, 상기 분압회로로부터 발생된 일정 전압이 베이스 단자에 인가되는 제1트랜지스터(TR1)와, 상기 제1트랜지스터(TR1)의 도통에 따라 상기 시스템 공급 전압을 시스템의 휘발성 데이터 기억장치(3)로 출력시키는 제2트랜지스터(TR2)와, 상기 분압회로로부터 일정 전압이 인가됨에 따라 상기 데이터 기억장치(3)를 활성화시키기 위한 칩 인에이블 신호(/BCE)를 출력하는 칩 인에이블 신호발생부(TR3,R4)와, 상기 시스템 공급 전압을 받아 일정 레벨의 전압을 출력하는 정전압 발생부(R5,D2,D3)와, 상기 정전압 발생부로부터 공급되는 전압에 의해 충전되며, 상기 시스템 공급 전압이 차단될 경우 상기 데이터 기억장치(3)로 충전된 전압을 인가하는 예비전원(20)으로 구성된다.

대표도



명세서

도면의 간단한 설명

제1도는 종래의 데이터 처리장치의 개략 블럭도이고,

제2도는 본 고안의 일실시예에 따른 자동 예비 전원 공급 장치의 구성을 나타낸 상세 회로도이다.

* 도면의 주요부분에 대한 부호의 설명

1 : AC/DC 컨버터 2 : DC/DC 컨버터

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3 : 디램　　4 : CPU

5 : SIO　　6 : PROM

10 : 자동 예비 전원 공급 장치　　20 : 예비전원

고안의 상세한 설명

고안의 목적

고안이 속하는 기술 및 그 분야의 종래기술

본 고안은 자동 예비 전원 공급 장치에 관한 것으로, 특히 전원 공급 장치의 이상장애 발생시 데이터 처리장치에 구비된 휘발성 메모리(Volatile Memory)인 디램(DRAM)에 자동으로 예비 전원을 공급하기 위한 자동 예비 전원 공급 장치에 관한 것이다

데이터 처리장치는 데이터 처리중에 처리된 데이터를 일시적으로 보관하기 위하여 디램을 구비하고 있다. 이러한 일반적인 데이터 처리장치가 제1도에 개시되어 있다.

제1도를 참고하면, 종래 기술에서는 110V/220V AC 상용전원을 받아서 DC 48V로 변환하기 위한 AC/DC 컨버터(1)와, 48V DC전압을 +5V로 변환하기 위한 DC/DC 컨버터(2)로 전원 공급 장치가 구성되어, 이로부터 중앙처리 장치(CPU)(4)와, CPU(4)에 연결되어 처리 중인 데이터를 일시적으로 기억하기 위한 디램(3)과, CPU(4)에 연결되어 입출력을 제어하기 위한 입출력 인터페이스(SIO)(5)와, 시스템 프로그램 운용 및 실행 데이터가 저장되어 있는 PROM(6)에 +5V 전원을 공급하는 구조를 갖고 있다.

상기와 같은 구성의 종래 기술에 있어서는 CPU(4)가 시스템 전체를 관리하는 마이크로 프로세서로 구성되어 PROM(6)에 저장되어 있는 초기화 프로그램 및 실행 데이터를 판독하여 디램(3)에 저장한 후 입출력 인터페이스(5)를 통하여 주변회로에 필요한 데이터를 보내 주거나 주변 회로에서 발생한 이벤트를 분석 처리하여 디램(3)에 저장시킨다.

입출력 인터페이스(5)는 사용자나 유지보수자가 시스템 진단시 디램(3)에 저장되어 있는 데이터를 판독한 후 분석 수정하여 디램(3)에 저장을 하거나 주변 회로가 필요한 데이터를 특정 번지에 저장할 수 있도록 한다.

디램(3)은 주변 회로나 PROM(6)으로부터 CPU(4)가 분석한 데이터를 저장하며, PROM(6)은 시스템의 초기화 프로그램 및 실행 데이터를 저장하고 있다.

이와 같은 종래 기술에 있어서는 AC 상용 전원이나 +5V DC 전원을 발생하는 컨버터 회로의 이상 장애로 인하여 +5 DC 전원이 다운되었을 경우 디램에 저장되어 있던 처리중의 데이터가 순간적으로 유실되게 된다.

따라서 차후 전원이 재인가 되었을 경우 유실된 데이터를 재 입력하고 다시 처리 과정을 거쳐야 하는 문제가 있다.

고안이 이루고자하는 기술적 과제

본 고안은 이러한 문제를 해소하기 위한 것으로 상용전원 또는 전원 공급 장치의 이상장애 발생시 데이터 처리장치에 구비된 디램에 자동으로 예비전원을 공급하기 위한 자동 예비 전원 공급 장치를 제공하는 것이 본 고안의 목적이다.

고안의 구성 및 작용

상기한 목적을 달성하기 위하여 본 고안은 시스템 공급 전압이 일측에 인가되는 분압회로와, 상기 분압회로로부터 발생된 일정 전압이 베이스 단자에 인가되는 제1트랜지스터와, 상기 제1트랜지스터의 도통에 따라 상기 시스템 공급 전압을 시스템의 휘발성 데이터 기억장치로 출력시키는 제2트랜지스터와, 상기 분압회로로부터 일정 전압이 인가됨에 따라 상기 데이터 기억장치를 활성화시키기 위한 칩 인에이블 신호를 출력하는 칩 인에이블 신호발생부와, 상기 시스템 공급 전압을 받아 일정 레벨의 전압을 출력하는 정전압 발생부와, 상기 정전압 발생부로부터 공급되는 전압에 의해 충전되며, 상기 시스템 공급 전압이 차단될 경우 상기 데이터 기억장치로 충전된 전압을 인가하는 예비전원으로 구성되는 것을 특징으로 하는 데이터 처리장치용 휘발성 데이터 기억장치의 자동 예비 전원 공급 장치를 제공한다.

이하에 첨부 도면을 참고하여 본 고안을 더욱 상세하게 설명한다.

제2도에는 본 고안의 바람직한 일실시예에 따른 자동 예비 전원 공급 장치(10)의 구성을 나타낸 상세 회로도가 도시되어 있다.

제2도를 참고하면 본 고안은 크게 트랜지스터(TR1 내지 TR3), 다이오드(D1 내지 D4), 저항(R1 내지 R5), 재충전 가능한 밧데리(BAT:Battery)로 이루어진 예비전원(20) 및 평소에는 도통 상태로 되어 있으나, 수리 또는 점검 등의 필요에 의해 예비전원(20)을 차단할 경우를 대비하는 스위치(SW)로 구성되어 있다.

본 고안의 동작을 설명하면, +5V 전압이 제1도의 DC/DC 컨버터(2)로부터 직렬 접속된 저항(R1), 제너다이오드(D1), 저항(R2)에 인가되면 저항(R2)과 제너다이오드(D1)의 접속점으로부터 하이 레벨(H) 신호가 출력되어 트랜지스터(TR1)의 베이스 단자에 인가되므로 트랜지스터(TR1)는 도통상태가 되고, 트랜지스터(TR2)의 베이스 단자에는 상기 트랜지스터(TR1)의 콜렉터에 의한 로우 레벨(L)이 인가되므로

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트랜지스터(TR2)는 도통상태가 된다.

트랜지스터(TR2)의 도통에 따라 5V 전원이 트랜지스터(TR2)를 통하고, 단지 에디터/베이스간의 전압 강하 분만 제외하고 5V 전압이 디램(3)에 대한 공급전원(VB)으로서 Vcc 단자에 인가된다.

한편 트랜지스터(TR3) 또한 베이스 단자에 하이 레벨(H) 신호가 인가되어 도통상태가 되므로 트랜지스터(TR3)의 콜렉터 단자로부터 로우 레벨(L) 신호가 밧데리 칩 인에이블 신호(/BCE)로서 출력되며, 이 신호는 디램(3)의 칩 선택이 로우액티브 상태가 되므로 디램(3)은 항상 액티브 상태가 된다.

또한 저항(R5)과 제너다이오드(D2) 직렬접속 회로의 저항(R5) 일측단자에 5V 전압이 인가되어 있으므로 저항(R5)과 제너다이오드(D2)의 접속점으로부터 일정한 전압이 다이오드(D3)를 통하여 20μA 전류 크기로 재충전 밧데리로 된 예비전원(20)을 충전시킨다. 스위치(SW)는 재충전용 밧데리의 수명이 한정적이므로 정기적으로 성능시험 등의 필요에 의해 차단할 수 있도록 구성된다.

만약 DC/DC 컨버터(2)로부터 5V 전원 공급이 중단될 경우 트랜지스터(TR1,TR2,TR3)는 모두 차단 상태로 되어 내부저항이 무한대로 된다.

이 경우 예비전원이 다이오드(D4)는 캐소드 단자가 로우 레벨로 되고 애노드 단자가 하이 레벨로 되므로 다이오드(D4)가 도통상태가 되어 예비전원(20)의 밧데리로부터 순간적으로 3.5V 전압이 VB와 /BCE에 공급된다. 그 결과 디램(3)의 밧데리 칩 인에이블 단자에 하이 레벨(H) 신호가 인가되어 디램(3)으로부터의 데이터 입출력을 정지시키며, 예비전원(20)에 의해 디램(3)에 저장된 데이터를 계속 유지할 수 있다.

고안의 효과

상기한 바와 같이 본 고안에 따르면 외부 전원이 차단되거나 DC/DC 컨버터등의전원장치의 이상으로 인하여 공급전원이 차단될지라도 디램(3)에 대한 칩 인에이블 신호를 하이 레벨 상태로 전환시키고 예비전원(20)을 전환 공급함에 의해 디램(3)에 저장되어 있는 데이터의 값들이 손실되거나 유실되는 것을 막아 줄 수 있다. 따라서 예를 들어 사용자 또는 프로그램 진단자가 디램(D-RAM)에 특수한 값을 입력시킨 것이 지워지지 않도록 보호할 수 있다.

(57) 청구의 범위

청구항 1

시스템 공급 전압이 일측에 인가되는 분압회로(R1,D1,R2)와, 상기 분압회로로부터 발생된 일정 전압이 베이스 단자에 인가되어 도통되도록 하는 제1스위칭 수단(TR1)과, 상기 제1스위칭 수단(TR1)의 도통에 따라 상기 시스템 공급 전압을 시스템의 데이터 기억장치(3)로 인가하는 제2스위칭 수단(TR2)과, 상기 분압회로로부터 일정 전압이 인가됨에 따라 상기 데이터 기억장치(3)를 활성화시키기 위한 칩 인에이블 신호(/BCE)를 출력하는 칩 인에이블 신호발생부(TR3,R4)와, 상기 시스템 공급 전압을 받아 일정 레벨의 전압을 출력하는 정전압 발생부(R5,D2,D3)와, 상기 정전압 발생부로부터 공급되는 전압에 의해 충전되며, 상기 시스템 공급 전압이 차단될 경우 상기 데이터 기억장치(3)로 충전된 전압을 인가하는 예비전원(20)으로 구성되는 것을 특징으로 하는 전원 차단시 자동 예비전원 공급 장치.

청구항 2

제1항에 있어서, 상기 시스템 공급 전원이 차단될 경우 순간적으로 하이 레벨의 칩 인에이블 신호(/BCE)가 상기 데이터 기억장치(3)에 인가되어 데이터 기억장치(3)에 대한 데이터 입출력을 정지시키는 것을 특징으로 하는 전원 차단시 자동 예비전원 공급 장치.

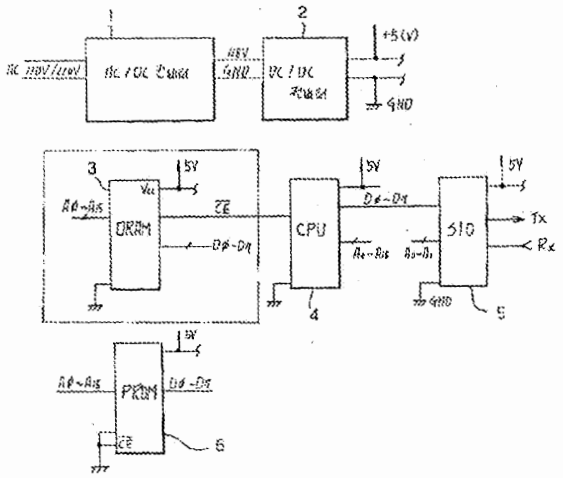
청구항 3

제1항 또는 제2항에 있어서, 상기 예비전원(20)의 출력 측에 역방향 전류 흐름을 저지하기 위한 다이오드(D4)를 더 포함하는 것을 특징으로 하는 전원 차단시 자동 예비전원 공급 장치.

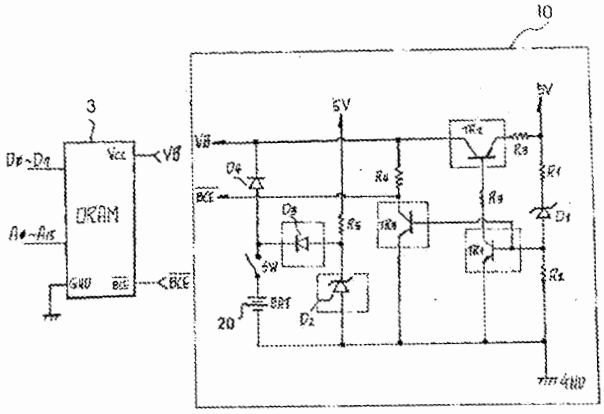
도면

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도면1



도면2



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Patents KR 0130873 Y1

An auxiliary power supply for automatic switching equipment

Abstract

The present invention relates to an automatic backup power supply device, and more particularly, to an automatic backup power supply device for automatically supplying backup power to a DRAM, a volatile memory (Volatile Memory) included in a data processing device, when an abnormal failure of the power supply device occurs. will be

In the automatic preliminary power supply of the volatile data storage device for a data processing device of the present invention, the voltage divider circuits R1, D1, and R2 to which a system supply voltage is applied to one side, and a constant voltage generated from the voltage divider circuit are applied to a base terminal. The first transistor TR1, the second transistor TR2 for outputting the system supply voltage to the volatile data storage device 3 of the system according to the conduction of the first transistor TR1, and the voltage divider circuit. When the voltage is applied, the chip enable signal generators TR3 and R4 for outputting the chip enable signal / BCE for activating the data storage device 3 and the voltage of the predetermined level in response to the system supply voltage. Is charged by a constant voltage generator (R5, D2, D3) and a voltage supplied from the constant voltage generator, and charged to the data storage device (3) when the system supply voltage is cut off. It consists of a spare power source 20 for applying voltage.

Classifications

- H02J9/061 Circuit arrangements for emergency or stand-by power supply, e.g. for emergency lighting in which the distribution system is disconnected from the normal source and connected to a standby source with automatic change-over, e.g. UPS systems for DC powered loads

KR0130873Y1

South Korea

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Other languages: Korean

Inventor: 방홍식

Worldwide applications

1993 KR

Application KR20199300299450 events

1993-12-28 Application filed by 방홍식, 엘지정보통신주식회사

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1995-07-28 Publication of KR950021729U

1999-04-15 Application granted

1999-04-15 Publication of KR0130873Y1

Info: Legal events, Similar documents, Priority and Related Applications

External links: Espacenet, Global Dossier, Discuss

Claims (3)

Hide Dependent

1. Voltage divider circuits R1, D1, and R2 to which a system supply voltage is applied to one side, first switching means TR1 to allow a constant voltage generated from the voltage divider circuit to be applied to the base terminal, and the first switching means. The second switching means TR2 for applying the system supply voltage to the data storage device 3 of the system in accordance with the conduction of TR1 and the data storage device 3 as a constant voltage is applied from the voltage dividing circuit. Chip enable signal generators TR3 and R4 for outputting a chip enable signal / BCE for activation, and constant voltage generators R5, D2 and D3 for outputting a predetermined level of voltage in response to the system supply voltage. And a preliminary power source 20 which is charged by a voltage supplied from the constant voltage generator and applies a voltage charged to the data storage device 3 when the system supply voltage is cut off. car Automatic redundant power supply.

    2. The method of claim 1, wherein when the system supply power is cut off, a high level chip enable signal (/ BCE) is instantaneously applied to the data storage device 3 to stop data input and output to the data storage device 3. Automatic pre-power supply when the power is cut off, characterized in that.

    3. The automatic preliminary power supply device according to claim 1 or 2, further comprising a diode (D4) for preventing reverse current flow on the output side of the preliminary power supply (20).

Description

Automatic Redundant Power Supply at Power Off

The present invention relates to an automatic redundant power supply device, and in particular, an automatic redundant power supply for automatically supplying redundant power to a DRAM, a volatile memory included in a data processing device, in case of an abnormal failure of the power supply device. It is about a device

The data processing apparatus includes a DRAM for temporarily storing data processed during data processing. This general data processing apparatus is disclosed in FIG.

Referring to FIG. 1, in the prior art, an AC / DC converter 1 for receiving a 110V / 220V AC commercial power and converting it into a DC 48V, and a DC / DC converter 2 for converting a 48V DC voltage to + 5V The power supply unit is composed of a central processing unit (CPU) (4), a CPU (4), a DRAM (3) for temporarily storing data being processed, and a CPU (4). A + 5V power supply is provided to an input / output interface (SIO) 5 for controlling input and output and a PROM 6 in which system program operation and execution data are stored.

In the prior art of the above-described configuration, the CPU 4 is composed of a microprocessor that manages the entire system, and reads the initialization program and execution data stored in the PROM 6 and stores it in the DRAM 3, and then inputs and outputs the interface. Through (5), necessary data is sent to the peripheral circuit or the event generated in the peripheral circuit is analyzed and stored in the DRAM (3).

The input / output interface 5 reads the data stored in the DRAM 3 and analyzes and corrects the data stored in the DRAM 3 when the system diagnosis is performed. do.

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The DRAM 3 stores data analyzed by the CPU 4 from the peripheral circuit and the PROM 6, and the PROM 6 stores the initialization program and execution data of the system.

In the prior art, when the +5 DC power supply is down due to an abnormal failure of an AC commercial power supply or a converter circuit generating + 5V DC power, the data stored in the DRAM is momentarily lost.

Therefore, when power is reapplied in the future, there is a problem of re-entering lost data and going through the process again.

An object of the present invention is to provide an automatic backup power supply device for automatically supplying backup power to a DRAM provided in a data processing device when an abnormal failure of a commercial power supply or a power supply occurs. .

1 is a schematic block diagram of a conventional data processing apparatus.

2 is a detailed circuit diagram illustrating a configuration of an automatic standby power supply apparatus according to an embodiment of the present invention.

* Explanation of symbols for main parts of the drawings

1: AC / DC converter 2: DC / DC converter

3: DRAM 4: CPU

5: SIO 6: PROM

10: automatic backup power supply 20: backup power

In order to achieve the above object, the present invention provides a voltage divider circuit in which a system supply voltage is applied to one side, a first transistor in which a constant voltage generated from the voltage divider circuit is applied to a base terminal, and according to the conduction of the first transistor. A second transistor for outputting a system supply voltage to a volatile data storage device of the system, a chip enable signal generator for outputting a chip enable signal for activating the data storage device when a predetermined voltage is applied from the voltage dividing circuit; And a constant voltage generator that receives the system supply voltage and outputs a voltage of a predetermined level, and is charged by a voltage supplied from the constant voltage generator, and applies the charged voltage to the data storage device when the system supply voltage is cut off. For the data processing apparatus, characterized in that consisting of a spare power source It provides automatic redundant power supply of the property data storage device.

Hereinafter, the present invention will be described in more detail with reference to the accompanying drawings.

2 is a detailed circuit diagram showing the configuration of the automatic backup power supply 10 according to an embodiment of the present invention.

Referring to FIG. 2, the present invention is largely made of a transistor (TR1 to TR3), a diode (D1 to D4), a resistor (R1 to R5), a rechargeable power source (BAT) consisting of a rechargeable battery (BAT: Battery), and usually conduction. Although it is in a state, it is comprised by the switch SW for the case where the preliminary power supply 20 is interrupted by the need of repair or inspection.

Referring to the operation of the present invention, when the + 5V voltage is applied to the resistor R1, the zener diode D1, and the resistor R2 connected in series from the DC / DC converter 2 of FIG. 1, the resistor R2 and the zener Since the high level H signal is output from the connection point of the diode D1 and applied to the base terminal of the transistor TR1, the transistor TR1 is in a conductive state, and the base terminal of the transistor TR2 is connected to the base terminal of the transistor TR1. Since the low level L is applied by the collector, the transistor TR2 is in a conductive state.

In accordance with the conduction of the transistor TR2, a 5V power supply is applied to the Vcc terminal as the supply power supply VB for the DRAM 3 except for the voltage drop between the editor / base through the transistor TR2.

On the other hand, since the transistor TR3 is also in the conductive state by applying the high level (H) signal to the base terminal, the low level (L) signal is output as the battery chip enable signal (/ BCE) from the collector terminal of the transistor TR3. This signal is in a low-active state when the chip selection of the DRAM 3 becomes low, so that the DRAM 3 is always in an active state.

In addition, since a 5V voltage is applied to one terminal of the resistor R5 of the resistor R5 and the zener diode D2 series connection circuit, a constant voltage is applied from the connection point of the resistor R5 and the zener diode D2 through the diode D3. Charge the backup power supply 20 with a rechargeable battery with a current size of 20 μA. Since the switch (SW) has a limited life span of the rechargeable battery, the switch (SW) is configured to be cut off periodically by need of a performance test.

If the 5V power supply is stopped from the DC / DC converter 2, the transistors TR1, TR2, and TR3 are all cut off, and the internal resistance becomes infinite.

In this case, since the diode D4 has the cathode terminal at the low level and the anode terminal at the high level, the diode D4 is in a conductive state, and the 3.5V voltage is instantaneously from the battery of the reserve power source 20. Supplied to BCE. As a result, a high level (H) signal is applied to the battery chip enable terminal of the DRAM 3 to stop input / output of the data from the DRAM 3, and the data stored in the DRAM 3 by the preliminary power supply 20 continues. I can keep it.

As described above, according to the present invention, even when the external power supply is cut off or the power supply is cut off due to an abnormality of a power supply device such as a DC / DC converter, the chip enable signal for the DRAM 3 is switched to a high level state and a reserve power supply is provided. By converting and supplying 20, the values of data stored in the DRAM 3 can be prevented from being lost or lost. Thus, for example, a user or a program diagnoser can protect the input of a special value into the D-RAM from being erased.

Similar Documents

Publication	Publication Date	Title
US7768247B2	2010-08-03	Under voltage lock out circuit and method
EP0389566B1	1996-09-18	Improved low power dual-mode cmos bias voltage generator
JP3378874B2	2003-02-17	Information processing device and memory board
US5412255A	1995-05-02	Switch device suitable for use in automotive vehicles

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US4016474A	1977-04-05	Circuit for controlling the charging current supplied to a plurality of battery loads in accordance with a predetermined program
US4492876A	1985-01-08	Power supply switching arrangement
US6025695A	2000-02-15	Battery operating system
US5519663A	1996-05-21	Preservation system for volatile memory with nonvolatile backup memory
US4675538A	1987-06-23	General purpose uninterruptible power supply
US4399524A	1983-08-16	Memory protection system
US5534734A	1996-07-09	Power shedding device
US6222570B1	2001-05-01	Uninterruptable power supply
US4313060A	1982-01-26	Uninterruptible power supply with load regulation of standby voltage source
KR100188667B1	1999-06-01	Power supply control device and its driving method
US5815409A	1998-09-29	Control system and method for automatic shutdown of a power supply
US4677311A	1987-06-30	Power supply system for an electronic apparatus having memory
US5387820A	1995-02-07	Power supply circuit
US6876585B2	2005-04-05	Circuit and method for selecting reference voltages in semiconductor memory device
US5414861A	1995-05-09	Data protection system using different levels of reserve power to maintain data in volatile memories for any period of time
US4510400A	1985-04-09	Switching regulator power supply
JP3896090B2	2007-03-28	Power supply device having a plurality of power supply outputs
US5363312A	1994-11-08	Method and apparatus for battery control
US7036010B2	2006-04-25	Method of controlling power within a disk array apparatus
US20040151022A1	2004-08-05	Memory trouble relief circuit
US5428252A	1995-06-27	Power supply interruption detection and response system for a microcontroller

Priority And Related Applications

Priority Applications (1)

Application	Priority date	Filing date	Title
KR2019930029945U	1993-12-28	1993-12-28	An auxiliary power supply for automatic switching equipment

Applications Claiming Priority (1)

Application	Filing date	Title
KR2019930029945U	1993-12-28	An auxiliary power supply for automatic switching equipment

Legal Events

Date	Code	Title	Description
1995-03-13	A201	Request for examination	
1998-02-25	E902	Notification of reason for refusal	
1998-05-30	E902	Notification of reason for refusal	
1998-08-29	E701	Decision to grant or registration of patent right	
1998-09-09	REGI	Registration of establishment	
2002-03-29	FPAY	Annual fee payment	**Payment date**: 20020329 **Year of fee payment**: 5
2003-09-10	LAPS	Lapse due to unpaid annual fee	

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Concepts

machine-extracted

Download Filter table

Name	Image	Sections	Count	Query match
response		claims,abstract	2	0.000
activation		claims	1	0.000
abnormal effects		abstract,description	4	0.000
activating		abstract,description	2	0.000

Show all concepts from the description section

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G11C 11/4093 (2006.01)

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(74) 대리인 박영우

심사관 : 고석현

(54) 불휘발성 메모리와 호스트간에 버퍼링 동작을 수행하는멀티 포트 휘발성 메모리 장치, 이를 이용한 멀티-칩패키지 반도체 장치 및 이를 이용한 데이터 처리장치

요약

비휘발성 메모리에 대해 마스터로 동작하는 휘발성 메모리를 개시한다. 본 발명의 메모리는 메인 메모리 코아와, 서브 메모리 코아를 구비한다. 또한, 외부 시스템과 데이터를 전송하기 위한 제1 포트와, 외부 플래시 메모리와 데이터를 전송하기 위한 제2 포트와, 상기 제1 포트를 통하여 마스터 모드에서 메인 메모리 코아와 외부 시스템을 인터페이싱하고, 슬레이브 모드에서 서브 메모리 코아와 외부 시스템을 인터페이싱하는 메인 인터페이스부와, 제2 포트를 통하여 슬레이브 모드에서 서브 메모리 코아와 외부 불휘발성 메모리를 인터페이싱하는 서브 인터페이스부를 포함한다. 따라서, 저속 동작의 불휘발성 메모리에 대해 고속 동작의 휘발성 메모리가 마스터로 동작하므로 시스템의 메모리 콘트롤를 간략화 할 수 있다.

대표도

도 1

명세서

도면의 간단한 설명

도 1은 본 발명에 의한 마스터 휘발성 메모리의 바람직한 일 실시예의 구성도.

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도 2는 도 1의 제어부의 상세 블록도.

도 3 및 도 4는 도 1의 동작 타이밍도.

도 5는 본 발명에 의한 데이터 처리 장치의 바람직한 일 실시예의 구성도.

도 6은 도 5의 멀티 칩 반도체 장치의 메모리 링크 휘발성 메모리 장치의 바람직한 일 실시예의 내부 구성도.

발명의 상세한 설명

발명의 목적

발명이 속하는 기술 및 그 분야의 종래기술

본 발명은 마스터 휘발성 메모리 장치에 관한 것으로서, 특히 슬레이브로 동작하는 불휘발성 메모리에 대해 마스터로 동작하는 듀얼 포트 동기형 디램에 관한 것이다.

최근에 카메라 폰이 장착된 휴대폰 또는 인터넷 접속이 가능한 휴대폰 등이 상품되면서 휴대폰의 영상 데이터를 저장하기 위한 메모리의 대용량화가 요구되고 있다.

통상적으로 휴대폰에서는 데이터 처리를 위한 코드를 저장하기 위하여 고속동작 및 랜덤 억세스가 가능한 노아형 플래시 메모리를 주로 사용하고 있었다. 그러나, 노아형 플래시 메모리는 고속 랜덤 억세스가 가능하나 용량 대비 코스트가 비싸 대용량으로 널리 보급되지 못하고 있다.

한편, 낸드 플래시 메모리는 노아 플래시 메모리에 비해 저속이나 용량 대비 코스트가 낮아 영상 데이터 저장용으로 디지털 카메라 분야 등에서 그 수요가 급팽창하고 있다.

일반적으로 휴대폰 시스템에서는 중앙처리부에서 카메라로부터 픽업된 영상 데이터를 디램에 저장한 후 압축 등의 디지털 영상 처리하여 낸드 플래시 메모리에 저장한다. 중앙처리부는 각각의 인터페이스를 통하여 디램 및 낸드 플래시 메모리를 제어하며, 디램과 낸드 플래시 메모리는 DMA(Direct Memory Access) 블록을 통하여 데이터를 주고 받는다.

따라서, 시스템 전체의 성능은 저속동작하는 낸드 플래시 메모리의 속도에 의해 시스템 성능이 저하된다. 또한, 중앙처리부와 디램과 낸드형 플래시 메모리 각각의 하드웨어 적인 연결이 요구되므로 시스템의 원칩화시 패키지 사이즈가 증가되므로, 휴대폰 시스템의 소형 경량화를 방해하는 요소로 작용한다.

일본 도시바사에서는 낸드 플래시 메모리를 SRAM(STATIC RANDOM ACCESS MEMORY)처럼 구동하는 인터페이스 기술을 소개하였다. 도시바 기술은 SRAM을 버퍼로 사용하여 시스템과 플래시 사이의 데이터 전송을 버퍼링함으로써 시스템과 SRAM 사이를 SRAM의 인터페이스 속도로 플래시를 제어하는 것이다.

또한, 한국 공개특허 2002-95109호에서 일본 히다찌사에서는 디램, 낸드형 플래시 메모리, 제어회로를 원칩으로 모듈화한 기술을 개시하였다. 이 기술의 모듈의 제어회로는 외부 데이터를 일단 디램에 저장한 다음에 외부명령에 응답하여 디램에 저장된 데이터를 플래시 메모리에 저장한다. 또한, 외부로부터 플래시에 기입된 데이터를 독출하고자 할 경우에는 일단 플래시의 데이터를 디램에 전송한 다음에 디램에 전송된 데이터를 외부로 독출한다. 따라서, 모듈은 외부 시스템과 SDRAM 인터페이스에 의해 동작한다.

이들 종래 기술들은 모두 플래시 메모리와 버퍼 메모리 사이에 인터페이스 제어회로를 매개로 하여 시스템과 버퍼 메모리, 버퍼 메모리와 플래시 메모리 사이의 데이터 전송을 제어한다.

발명이 이루고자 하는 기술적 과제

본 발명의 목적은 이와 같은 종래 기술의 문제점을 해결하기 위하여 호스트 시스템에서 메모리 콘트롤을 간략화 하기 위하여 플래시 메모리와 같은 저속 동작의 불휘발성 메모리를 슬레이브로 제어하는 마스터 듀얼 포트 동기형 디램을 제공한다.

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또한, 저속 동작의 플래시 메모리를 제어하여 저속 메모리를 호스트 시스템에 링크시키는 저속 메모리 링크형 고속 메모리 장치를 제공한다.

또한, 상기 저속 메모리 링크형 고속 메모리 장치를 포함하는 데이터 처리 장치를 제공한다.

또한, 플래시 메모리와 같은 불휘발성 메모리와 상기 메모리 링크형 고속 메모리 장치를 하나의 패키지에 실장시킨 멀티칩 반도체 장치를 제공한다.

발명의 구성 및 작용

상기 목적을 달성하기 위하여 본 발명의 멀티 포트 휘발성 메모리 장치는 외부 호스트 시스템 및 상기 멀티 포트 휘발성 메모리 장치간 데이터를 송수신하는 제1 포트; 수신된 데이터를 저장하고 요청된 저장된 데이터를 읽어들이는 휘발성 메인 메모리 코아; 수신된 데이터를 저장하고 요청된 저장된 데이터를 읽어들이는 휘발성 서브 메모리 코아; 상기 제1 포트와 결합되어, 마스터 모드에서 상기 휘발성 메인 메모리 코아와 상기 제1 포트간에 데이터를 주고받고, 슬레이브 모드에서 상기 휘발성 서브 메모리 코아와 상기 제1 포트간에 데이터를 주고받는 메인 인터페이스 회로; 외부의 비휘발성 메모리 장치와 데이터를 송수신하는 제2 포트; 및 상기 제2 포트와 결합되어, 상기 슬레이브 모드에서 상기 휘발성 서브 메모리 코아와 상기 제2 포트간에 데이터를 주고받는 서브 인터페이스 회로를 포함한다.

여기서, 본 발명의 휘발성 메모리 장치는 고속동작의 DRAM 이고, 저속동작의 불휘발성 메모리 장치는 NAND 형 플래시 메모리로 구성하는 것이 바람직하다. 또한, 여기서, 휘발성 서브 메모리 코아는 SRAM으로 구성할 수도 있다.

본 발명에서 메인 인터페이스부는 외부 호스트 시스템으로부터 제공된 명령을 디코딩하여 내부 명령제어신호를 발생하는 명령디코더와, 외부 호스트 시스템으로부터 제공된 어드레스신호를 입력하여 내부 어드레스 신호를 발생하는 어드레스 버퍼와, 상기 마스터 모드에서 상기 외부 호스트 시스템과 상기 휘발성 메인 메모리 코아 사이에 데이터를 주고받고, 상기 슬레이브 모드에서 상기 외부 호스트 시스템과 상기 휘발성 서브 메모리 코아들간에 데이터를 주고받는 데이터 입출력버퍼와, 외부 호스트 시스템으로부터 제공된 마스터/슬레이브 모드선택신호에 응답하여 어드레스버퍼 및 데이터 입출력버퍼를 통하여 제공된 제어 데이터에 의해 상기 휘발성 메인 메모리 코아 및 휘발성 서브 메모리 코아를 제어하여 마스터 및 슬레이브 동작모드를 제어하는 제어부를 포함한다.

본 발명에서 서브 인터페이스 회로는 제어부로부터 제공된 제어 데이터에 응답하여 제2 포트에 연결된 외부 플래시 메모리와 서브 메모리 코아 사이의 데이터 전송을 제어하는 낸드 플래시 메모리 제어부를 포함한다.

또한, 본 발명에서 메인 인터페이스 회로는 명령디코더로부터 제공된 명령제어신호에 응답하여 휘발성 서브 메모리 코아 및 휘발성 서브 인터페이스부의 전원을 관리하는 전원 관리부를 더 포함하는 것이 바람직하다.

상기 목적을 달성하기 위하여 본 발명의 멀티 포트 휘발성 메모리 장치는 호스트 시스템과 외부 액세스를 하는 제1 포트; 비휘발성 메모리 장치와 외부 액세스를 하는 제2 포트; 및 외부 액세스를 하도록 상기 제1 및 제2 포트에 결합된 휘발성 메모리 코어를 포함한다.

상기 목적을 달성하기 위하여 본 발명의 저속 메모리 링크형 고속 메모리 장치는 메인 메모리 코아, 버퍼 메모리 코아, 제1 데이터 입출력부, 제2 데이터 입출력부, 제1 어드레스 레지스터, 제2 어드레스 레지스터 및 제어부를 포함한다. 제1 데이터 입출력부는 호스트와 연결된 제1 데이터 입출력 포트와 상기 메인 메모리 사이에 연결되어 데이터의 입출력을 구동하고, 제2 데이터 입출력부는 플래쉬 메모리와 연결된 제2 데이터 입출력 포트와 상기 버퍼 메모리 사이에 연결되어 데이터의 입출력을 구동한다. 제1 어드레스 레지스터는 상기 메인 메모리 코아의 어드레스 신호를 저장한다. 제2 어드레스 레지스터는 상기 제1 및 제2 데이터 입출력부 사이에 연결되어 플래쉬 메모리의 어드레스 신호를 저장한다. 상기 제어부는 상기 메인 메모리 코아의 데이터 리드 또는 라이트 동작 모드에서는 상기 호스트로부터 제공된 어드레스 신호에 의해 상기 메인 메모리 코아를 어드레싱하고, 상기 제1 데이터 입출력부를 통하여 데이터를 리드 또는 라이트한다. 상기 제어부는 상기 플래쉬 메모리의 데이터 리드 동작 모드에서는, 상기 호스트로부터 제공된 소스 어드레스 신호를 상기 제1 데이터 입출력부를 통하여 상기 제2 어드레스 레지스터에 저장하고, 목적지 어드레스 신호를 상기 제1 어드레스 레지스터에 저장하고, 상기 제2 어드레스 레지스터에 저장된 소스 어드레스 신호를 상기 플래쉬 메모리의 시작 어드레스로 상기 제2 데이터 입출력부를 통하여 상기 플래쉬 메모리에 제공하고, 상기 플래쉬 메모리로부터 독출된 데이터를 상기 버퍼 메모리 코아에 저장하고, 상기 버퍼 메모리 코아에 저장된 데이터를 상기 제1 어드레스 레지스터에 저장된 목적지 어드레스를 시작 어드레스로 하여 상기 메인 메모리 코아에 카피시키고, 상기 메모리 코아에 카피된 데이터를 상기 제1 데이터 입출력부를 통하

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여 호스트로 독출시킨다. 상기 제어부는 상기 플래쉬 메모리의 데이터 라이트 동작 모드에서는, 상기 호스트로부터 제공된 목적지 어드레스 신호를 상기 제1 데이터 입출력부를 통하여 상기 제2 어드레스 레지스터에 저장하고, 소스 어드레스 신호를 상기 제1 어드레스 레지스터에 저장하고, 상기 제1 어드레스 레지스터에 저장된 소스 어드레스 신호를 상기 메인 메모리 코아의 시작 어드레스로 하여 상기 메인 메모리 코아의 데이터를 상기 버퍼 메모리 코아에 카피시키고, 상기 버퍼 메모리 코아에 카피된 데이터를 상기 제2 데이터 입출력부를 통하여 플래쉬 메모리에 출력시킨다.

상기 목적을 달성하기 위하여 본 발명의 데이터 처리 장치는 제1 속도로 동작하는 고속 메모리를 억세스하는 호스트; 상기 제1 속도보다 낮은 속도인 제2 속도로 동작하는 저속 메모리; 및 상기 저속 메모리와 저속으로 인터페이스하고 상기 호스트와 고속으로 인터페이스하여, 상기 저속 메모리를 상기 호스트에 고속으로 링크시키기 위한 메모리 링크 고속 메모리를 포함한다.

상기 목적을 달성하기 위하여 본 발명의 데이터 처리 장치는 호스트; 불휘발성 메모리; 및 상기 불휘발성 메모리와 제1포트를 통하여 인터페이스하고 상기 호스트와 제2 포트를 통하여 인터페이스하여, 상기 불휘발성 메모리를 상기 호스트에 링크시키기 위한 휘발성 메모리를 포함한다.

상기 목적을 달성하기 위하여 본 발명의 멀티 칩 반도체 장치는 호스트와 연결하기 위한 연결포트; 불휘발성 메모리; 및 상기 불휘발성 메모리와 연결되고 상기 호스트와 상기 연결포트를 통하여 인터페이스하여, 상기 불휘발성 메모리를 상기 호스트에 링크시키기 위한 메모리 링크 휘발성 메모리를 하나의 패키지에 실장시킨다.

이하, 첨부한 도면을 참조하여 본 발명의 바람직한 실시예를 구체적으로 설명하고자 한다. 이 실시예는 이 기술에 숙련된 자들이 본 발명을 실시할 수 있게 충분히 상세하게 기술한다.

< 실시예 1 >

도 1은 본 발명에 의한 마스터 휘발성 메모리의 구성을 나타낸다. 도 1을 참조하면, 시스템(100)은 마스터 휘발성 메모리, 디램(200)을 통하여 NAND 형 플래시 메모리(300)와 연결된다.

본 발명의 디램(200)은 듀얼 포트형으로 시스템(100)과 연결되는 제1 포트(202)와 NAND 플래시 메모리(300)와 연결되는 제2 포트(204)를 포함한다.

또한, 디램(200)은 메인 메모리 코아(210), 서브 메모리 코아(220)를 포함한다. 메인 메모리 코아(210)는 셀어레이(212), 로우디코더(214), 컬럼디코더(216)를 포함한다. 서브 메모리 코아(220)는 셀어레이(222), 로우디코더(224), 컬럼디코더(226)를 포함한다.

또한, 디램(200)은 메인 인터페이스부(230)와 서브 인터페이스부(240)를 포함한다. 메인 인터페이스부(230)는 명령디코더(232), 어드레스 버퍼(234), 입출력버퍼(236), 제어부(238), 모드 선택기(239)를 포함한다.

명령디코더(232)는 외부 시스템(100)으로부터 제공된 명령, 즉 디램 제어신호, 예컨대, 칩선택신호 CS, 로우 스트로브신호 /RAS, 컬럼스트로브신호 /CAS, 클럭신호 CLK, 라이트 인에이블신호 /WE, 칩인에이블신호 등을 포함한다. 명령디코더(232)는 이들 제어신호를 디코딩하여 기입 또는 독출 등의 동작모드를 해석하고 동작모드와 관련된 내부 명령제어신호들을 발생하여 메인 메모리 코아(210), 서브 인터페이스부(240) 및 제어부(238)에 제공한다.

어드레스 버퍼(234)는 외부 시스템(100)으로부터 제공된 어드레스신호를 입력받아 클럭에 동기된 내부 어드레스 신호를 발생한다. 내부 어드레스신호는 메인 메모리 코아(210), 제어부(238)에 제공된다. 메인 메모리 코아에 제공된 내부 어드레스 신호는 로우 어드레스 및 컬럼 어드레스이고, 제어부(238)에 제공되는 내부 어드레스 신호는 외부 시스템(100)으로부터 제공된 제어 데이터로 예컨대 모드 세트 데이터, NAND 플래시 메모리의 초기 어드레스 정보, 서브 메모리 코아(230)의 어드레스 정보 등이 될 수 있다.

입출력버퍼(236)는 메인 메모리 코아(210) 또는 서브 메모리 코아(220)와 외부 시스템 사이의 데이터 입출력을 버퍼링한다. 입출력버퍼(236)에서는 제어부(238)로 NAND 플래시 메모리(300)의 데이터 사이즈 정보를 제공한다.

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제어부(238)는 어드레스버퍼(234)를 통하여 제공된 제어 데이터 중 NAND 플래시 초기 어드레스 정보 및 서브 메모리 코아의 어드레스 정보는 서브 인터페이스부(240)에 전달하고, 상기 모드 세트 데이터에 기초하여 마스터/슬레이브 모드 선택신호(M/S)를 발생한다. 제어부(238)는 슬레이브 모드에서는 서브 메모리 코아(220)를 제어하여 서브 메모리 코아(220)의 데이터 기입 및 독출을 제어한다.

마스터/슬레이브 모드 선택기(239)는 상기 M/S 신호에 응답하여 입출력버퍼(236)를 메인 메모리 코아(210)와 서브 메모리 코아(220)에 선택적으로 연결한다.

서브 인터페이스부(240)는 NAND 제어부(242)와 전원 관리부(244)를 포함한다. NAND 제어부(242)는 제2 포트(204)를 통하여 슬레이브 모드에서 서브 메모리 코아(220)와 외부 플래시 메모리(300)를 인터페이싱한다. NAND 제어부(242)는 제어부(238)로부터 제공된 NAND 어드레스 정보를 제2 포트(204)를 통하여 외부 플래시 메모리(300)에 전달하여, 플래시 메모리(300)에 데이터의 기입 및 독출을 제어한다.

전원 관리부(244)는 명령 디코더(232)의 전원 제어신호에 응답하여 서브 메모리 코아(220) 및 낸드 제어부(242)의 전원을 관리하여 동작 모드에서는 전원공급을 재개하고 아이들 상태에서는 서브 메모리 코아(220) 및 서브 인터페이스부(240)의 전원을 차단하여 불필요한 전력 소모를 줄이도록 관리한다.

도 2를 참조하면, 제어부(238)는 스위치(238a), 어드레스 래치(238b), 낸드 시작 어드레스 래치(238c), 사이즈 래치(238d), 디램 시작 어드레스 래치(238e), 어드레스 비교기(238f), 어드레스 발생기(238g), 사이즈 비교기(238h) 및 래치(238i)를 포함한다.

도 2에는 제어부(238)의 구성 중 어드레스 처리에 관련된 블록만을 도시하고, 명령 디코더(232)로부터의 내부 명령 제어신호들을 처리하는 블록 및 모드 선택 신호(M/S)를 생성하는 블록에 대한 도시는 생략한다.

스위치(238a)는 입출력버퍼(236)로부터 제공된 사이즈 정보를 어드레스 래치(238b) 및 사이즈 래치(238d)에 스위칭한다.

어드레스 래치(238b)는 어드레스 버퍼(234)로부터 제공된 내부 어드레스 정보, 스위치(238a)로부터 제공된 사이즈 정보를 포함하는 데이터 및 사이즈 비교기(238h)로부터 제공된 데이터를 래치하여 어드레스 비교기(238f)에 제공한다.

낸드 시작 어드레스 래치(238c)는 어드레스 래치(238b)로부터 제공된 어드레스를 래치하여 낸드 시작 어드레스(NAND-Addr)를 발생한다.

사이즈 비교기(238h)는 어드레스 비교기(238f)로부터 제공된 데이터와 사이즈 래치(238d)로부터 제공된 사이즈 정보를 포함하는 데이터를 비교하고 그 결과를 어드레스 래치(238b)에 제공한다. 어드레스 발생기(238g)는 어드레스 비교기(238f)로부터 제공된 비교 정보를 서브 어드레스(Sub Addr)로 발생한다.

래치(238i)는 DRAM/NAND 플래시 모드 신호 DRAM/NAND에 기초하여 상기 모드 선택기(239)로 상기 마스터/슬레이브 모드 선택 신호 M/S를 출력한다.

1. 듀얼포트 전체 동작 알고리즘

전체 메인 프로그램은 아이들상태 - 디램 모드 - 낸드 플래시 모드 - 파워관리 모드 등을 수행한다.

파워관리 모드에서는 서브 메모리 코아의 아이들 상태에서 전원 차단, 전원 차단시 저장된 데이터를 유지하기 위한 리플래시 동작 관리 등을 포함한다.

2. 메인 메모리 모드

도 3에 도시한 바와 같이 디램 모드시에는 DRAM/NAND 신호가 로우상태로 되어 통상의 동기형 디램 동작모드를 수행한다.

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도 3을 참조하면, 먼저, /RAS 신호의 하강 에지에 응답하여 로우어드레스(Ra)가 어드레스(ADDR)로 출력되고, /CAS 신호의 하강 에지에 응답하여 컬럼어드레스(Ca)가 어드레스(ADDR)로 출력된다. 기입 인에이블 신호 /WE가 하이 레벨을 갖는 경우 읽기 모드로 동작하며, 로우어드레스(Ra) 및 컬럼 어드레스(Ca)에 상응하는 메인 메모리 코아(210)의 a 번지의 데이터 Qa1, Qa2, Qa3, Qa4 들이 독출(read) 된다. 다음에, /WE가 로우 레벨을 갖는 경우 쓰기 모드로 동작하며, 로우어드레스(Rb) 및 컬럼 어드레스(Cb)에 의해 메인 메모리 코아(210)의 b 번지에 데이터 Db0, Db1, Db2, Db3 들이 기입(write) 된다. 도 3에서 빗금친 구간들은 don't care 구간이다.

3. 낸드 플래시 모드

NAND 플래시에 데이터 기입할 경우에는 DRAM/NAND 신호를 하이상태로 하여 데이터 패스를 서브 메모리 코아(220)와 연결한다. 따라서, 낸드 플래시(300)에 기입될 데이터는 제어부(238)의 제어하에 서브 메모리 코아(220)에 기입된다. 제어부(238)에서는 서브 메모리 코아(220)에 기입된 데이터가 낸드 플래시 메모리(300)의 작업단위인 블록(block) 사이즈가 되었을 경우에 낸드 제어부(242)를 활성화시켜 제2 포트(204)에 연결된 플래시 메모리(300)로 블록 단위로 기입한다.

도 4를 참조하면, 낸드 플래시 메모리(300)의 쓰기 동작은 로우 레벨의 칩 인에이블 신호 /CE 및 로우 레벨의 기입 인에이블 신호 /WE에 응답하여 제2 포트(204)의 입출력 라인 I/Ox로 데이터를 출력하고, 상기 출력된 데이터를 낸드 플래시 메모리에 기입한다. CLE는 커맨드 래치 인에이블 신호이고, ALE는 어드레스 래치 인에이블 신호로서, 각각 커맨드 및 어드레스를 상기 입출력 라인 I/Ox으로 멀티플렉싱하는데 사용된다.

따라서, 서브 메모리 코아(220)의 사이즈는 상기 NAND 플래시(300)의 기입 단위인 블록 사이즈를 기초로 하여 정해질 수 있다. 예를 들어, 1Mb 이하를 이용할 수 있다.

또한, NAND 어드레스는 시스템(100)에서 발생하는 어드레스를 그대로 이용하고 로우 스트로브 신호 /RAS의 로우 상태에서, DRAM/NAND 신호를 하이로 만들어 어드레스 버퍼(234)를 이용하여 어드레스를 제어부(238) 내에 래치한다.

플래시 메모리로부터 데이터 독출은 낸드 제어부(242)를 통하여 플래시 메모리(300)로부터 독출된 데이터를 서브 메모리 코아(220)에 기입한 다음에 서브 메모리 코아(220)에 저장된 데이터를 입출력버퍼(236)를 통하여 시스템(100)으로 독출한다.

낸드 플래시 메모리(300)의 읽기 동작은 로우 레벨의 칩 인에이블 신호 /CE 및 하이 레벨의 기입 인에이블 신호 /WE에 응답하여 플래시 메모리(300)로부터 데이터를 독출하고, 제2 포트(204)의 입출력 라인 I/Ox을 통하여 상기 독출된 데이터를 상기 서브 메모리 코아(220)에 기입한다.

그러므로, 시스템은 DRAM 인터페이스 동작 속도로 플래시 메모리에 데이터의 기입 및 독출이 가능하게 된다.

< 실시예 2 >

도 5는 본 발명에 의한 데이터 처리 시스템의 블록 구성을 나타낸다. 도 5를 참조하면 데이터 처리장치는 호스트(300)와 멀티 칩 반도체 장치(310)를 포함한다. 호스트(300)는 마이크로 프로세서 및 메모리 콘트롤러를 포함한다. 호스트(300)와 멀티 칩 반도체 장치(310)는 어드레스 버스(302), 데이터 버스(304), 콘트롤 버스(306)를 통하여 서로 연결된다. 멀티 칩 반도체 장치(310)는 메모리 링크(MEMORY LINK) SDRAM(312)와 낸드 플래쉬 메모리(314)를 하나의 패키지로 구성한 멀티 칩 패키지(MCP)이다. ML-SDRAM(312)와 낸드 플래쉬 메모리(314)는 데이터 버스(316), 콘트롤 버스(318)를 통하여 서로 연결된다.

본 발명에서 어드레스 버스(302), 데이터 버스(304)는 통상의 동기식 디램의 어드레스 버스 및 데이터 버스의 구조를 가진다. 콘트롤 버스(306)는 통상의 디램 콘트롤 신호선인 CLK, CKE, DCS, RAS, CAS, WE, DQM 신호선들을 포함한다. 메모리 링크 커맨드를 수행하기 위하여 FCS, WAIT 등을 더 포함한다. FCS는 낸드 플래쉬 메모리 칩 선택신호이고, WAIT는 낸드 플래쉬 메모리 칩의 리드, 프로그램, 소거동작이 완료되었을 때 호스트에 명령이 완료되었다는 것을 통지하는 신호이다. 콘트롤버스(318)는 통상의 낸드 플래쉬 메모리 콘트롤 신호선인 CLE, ALE, CE, RE, WE, RB 신호선들을 포함한다.

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도 6은 도 5의 ML-SDRAM의 내부 블록 구성을 나탠다. 도 6을 참조하면, ML-SDRAM(312)는 어드레스 발생부(410), 메인 메모리 코아(420), 서브 메모리 코아(430), 제1 데이터 입출력부(440), 제2 데이터 입출력부(450), 제어부(460)을 포함한다.

어드레스 발생부(410)는 로우 어드레스 신호를 래치하는 제1래치(411), 컬럼 어드레스 신호를 래치하는 제2래치(412), 어드레스 신호를 저장하기 위한 제1 어드레스 레지스터(413), 로우 카운터(414), 제1선택기(416), 제2 선택기(417)를 포함한다. 어드레스 발생부(410)는 디램동작모드에서는 제1 및 제2 래치(411, 412)를 통해 로우 어드레스와 컬럼 어드레스를 래치하여 제1 및 제2 선택기(416, 417)에 제공한다. 제1 및 제2 선택기(416, 417)은 RA 및 CA 제어신호에 응답하여 디램동작모드에서는 제1 및 제2 래치(411, 412)를 선택하여 로우 어드레스와 컬럼 어드레스를 메인 메모리 코아(420)의 어드레스 신호로 제공한다. 어드레스 발생부(410)는 카피동작모드에서는 제1어드레스 레지스터(413)에 로우 어드레스와 컬럼 어드레스를 저장한다. 제1 어드레스 레지스터(413)에 저장된 로우 어드레스는 로우 카운터(414)를 통하여 제1 선택기(416)에 제공되고, 제1 어드레스 레지스터(413)에 저장된 컬럼 어드레스는 제2 선택기(417)에 제공된다. 제1 및 제2 선택기(416, 417)는 RA 및 CA 제어신호에 응답하여 카피동작모드에서는 로우 카운터(414)와 레지스터(413)를 선택하여 로우 어드레스와 컬럼 어드레스를 메인 메모리 코아(420)의 어드레스 신호로 제공한다.

메인 메모리 코아(420)는 대용량의 작업저장영역으로, 로우 디코더(421), 컬럼 디코더(422), 셀어레이(423), 컬럼 카운터(424)를 포함한다. 로우 카운터(414)는 카피동작에서 인가되는 로우 어드레스신호를 초기값으로 하여 연속적인 로우 어드레스를 발생한다. 컬럼 카운터(424)는 디램의 버스트 동작모드 및 카피동작모드에서 인가되는 컬럼 어드레스신호를 초기값으로 하여 연속적인 컬럼 어드레스를 발생한다.

서브 메모리 코아(430)는 페이지 또는 블록단위의 버퍼저장영역으로, 로우 디코더(431), 컬럼 디코더(432), 셀어레이(433)를 포함한다. 서브 메모리 코아(430)는 제어부(460)로부터 제공되는 버퍼 로우 어드레스신호(BRA)와 버퍼 컬럼 어드레스 신호(BCA)에 의해 셀을 지정한다.

제1 데이터 입출력부(440)는 SDRAM 데이터 입출력 인터페이스로, 리드 버퍼(441), 리드 레지스터(442), 라이트 버퍼(443), 라이트 레지스터(444), 입출력 구동기(445)를 포함한다. 리드 버퍼(441)는 디램 리드 제어신호(DR)에 의해 제어되고, 라이트 버퍼(443)는 디램 라이트 제어신호(DW)에 의해 제어된다. 제1 데이터 입출력부(440)는 호스트(300)와 메인 메모리 코아(420) 사이의 데이터 전송을 SDRAM 억세스 동작 속도로 제공한다.

제2 데이터 입출력부(450)는 NAND 플래쉬 메모리 데이터 입출력 인터페이스로, 리드 버퍼(451), 리드 레지스터(452), 라이트 버퍼(453), 라이트 레지스터(454), 입출력 구동기(455)를 포함한다. 리드 버퍼(451)는 플래쉬 리드 제어신호(FR)에 의해 제어되고, 라이트 버퍼(453)는 플래쉬 라이트 제어신호(FW)에 의해 제어된다. 제2 데이터 입출력부(450)는 NAND 플래쉬 메모리(314)와 서브 메모리 코아(430) 사이의 데이터 전송을 NAND 플래쉬 메모리(314) 억세스 동작 속도로 제공한다.

제어부(460)는 SDRAM 제어 로직부(461), ML 제어 로직부(462), 플래쉬 어드레스 레지스터(463), 카피 패스 스위치(464)를 포함한다.

SDRAM 제어 로직부(461)는 SDRAM 콘트롤 신호들(CKE, DCS, RAS, CAS, WE, DQM)을 입력하여 커맨드를 디코딩하고 디코딩된 커맨드에 따라 내부제어신호(DR, DW, RA, CA)를 발생한다. DR은 디램 리드 제어신호, DW는 디램 라이트 제어신호, RA는 로우 어드레스 선택신호, CA는 컬럼 어드레스 선택신호이다.

ML 제어 로직부(462)는 호스트(300)로부터 제공된 FCS 신호와, 플래쉬 메모리 콘트롤 신호들(CLE, ALE, CE, RE, WE) 등을 발생하고 플래쉬 메모리(314)로부터 제공된 준비/비지(RB : Ready/Busy) 신호에 응답하여 WAIT 신호를 발생하여 호스트(300)에 제공한다. ML 제어 로직부(462)는 로딩신호(LD)를 발생하여 카피 어드레스 레지스터(413) 및 플래쉬 어드레스 레지스터(463)를 제어한다. ML 제어 로직부(462)는 버퍼 메모리 코아(430)의 로우 및 컬럼 어드레스 신호(BRA, BCA)를 발생한다.

SDRAM 제어 로직부(461)과 ML 제어 로직부(462)는 동작상태신호(STA)를 주고 받는다.

플래쉬 어드레스 레지스터(463)는 제1 데이터 입출력부(440)을 통해 호스트로부터 플래쉬 어드레스 데이터를 받아서 저장하고, LD 제어신호에 응답하여 저장된 어드레스 데이터를 제2 데이터 입출력부를 통하여 NAND 플래쉬 메모리(413)로 제공한다.

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이와 같이 구성된 본 발명의 제2 실시예의 동작은 다음과 같다.

1. SDRAM 동작모드

SDRAM 동작 모드에서는 어드레스 발생부(410)의 제1 및 제2 선택기(416, 417)가 제1 및 제2 래치(411, 412)를 각각 선택하도록 제어된다. 그러므로, 호스트로부터 제공된 로우 어드레스와 컬럼 어드레스가 메인 메모리 코아(420)에 제공되어 특정 셀이 어드레싱된다.

리드 동작시에는 제1 데이터 입출력부(440)를 통하여 메인 메모리 코아(420)로부터 읽혀진 데이터가 호스트(300)로 출력되고, 라이트 동작시에는 호스트(300)로부터 제공되 데이터가 메인 메모리 코아(420)로 저장된다.

2. 메모리 링크 동작모드

메모리 링크 동작모드에서는 ML-SDRAM(312)이 호스트(300)와 플래쉬 메모리(314) 사이의 데이터 전송 및 명령 등을 중계하는 버퍼 역할을 수행한다.

1) 페이지 리드 모드(PRM : Page Read Mode)

호스트(300)로부터 제공된 CKE, DCS, RAS, FCS, WE 신호가 액티브되면 SDRAM 제어 로직부(461)에서는 RA, CA 제어신호를 액티브시켜서 제1 및 제2 선택기(416, 417)가 레지스터(413)를 선택하도록 스위칭시킨다. 동시에 로우 어드레스 신호가 레지스터(413)에 저장된다. 리드동작시에는 레지스터(413)에 저장된 어드레스는 목적지 어드레스가 된다.

또한, ML 제어 로직부(462)에서는 FCS 신호의 액티브 상태에 응답하여 WAIT 신호를 발생하여 호스트(300)로 출력한다. 따라서, 호스트(300)에서는 WAIT 신호의 액티브 상태를 체크하여 ML-SDRAM의 링크동작상태를 확인한다.

이어서, CAS 신호가 액티브되면서 컬럼 어드레스 신호가 레지스터(413)에 저장된다. 리드 동작시에는 레지스터(413)에 저장된 로우 및 컬럼 어드레스는 플래쉬 메모리(314)로부터 리드된 데이터가 저장될 메인 메모리 코아(420)의 목적지의 시작 어드레스로 제공된다.

데이터선(304)을 통하여 플래쉬 어드레스 데이터가 제1 데이터 입력부(440)을 통해 입력된다. 입력된 플래쉬 어드레스 데이터는 레지스터(463)에 저장된다. 레지스터(463)에 저장된 어드레스 데이터는 플래쉬 메모리(314)로부터 리드할 저장영역의 시작 어드레스로 제공된다.

호스트(300)로부터 어드레스 로딩동작이 완료되면, ML 제어 로직부(462)는 CLE, CE, RE 신호들을 액티브 상태로 발생시켜서 플래쉬 메모리(314)에 리드 커맨드를 제공한다. 이어서, CLE 신호 대신에 ALE 신호를 액티브 상태로 발생하고, 레지스터(463)에 저장된 어드레스 데이터를 제2 데이터 입출력부(450)를 통하여 플래쉬 메모리(314)에 제공한다.

플래쉬 메모리(314)에서는 제공된 어드레스 데이터를 입력받고 입력된 어드레스 데이터를 시작 어드레스로 하여 1페이지 분량의 데이터를 억세스하여 출력한다.

플래쉬 메모리로부터 독출된 데이터는 제2 데이터 입출력부(450)를 통하여 버퍼 메모리 코아(430)에 저장된다. 버퍼 메모리 코아(430)는 ML 제어 로직부(462)의 BRA, BCA 신호에 응답하여 어드레싱되어 1 페이지 분량의 데이터를 저장시킨다.

버퍼 메모리 코아(430)에 플래쉬 메모리 데이터의 저장이 완료되면, ML 제어 로직부(462)에서는 BRA, BCA 어드레스 신호를 발생하여 버퍼 메모리 코아(430)에 저장된 데이터를 액세스를 시작한다. 또한, CW 카피 라이트 제어신호를 발생하여 버퍼 메모리 코아(430)의 데이터를 메인 메모리 코아(420)에 인가되도록 카피 패스 스위치(464)를 제어한다.

또한, 레지스터(413)에 LD 제어신호를 인가시켜서 레지스터(413)에 저장된 목적지 어드레스 신호가 메인 메모리 코아(420)에 인가되도록 제어한다. 레지스터(413)에 저장된 목적지 로우 및 컬럼 어드레스가 메인 메모리 코아(420)로 제공된다. 레지스터(413)에 저장된 목적지 로우 어드레스는 로우 카운터(414)에 초기값으로 로딩된다. 이에 로우 카운터(414)에서는 이 값으로부터 카운팅을 시작한다. 또한, 레지스터(413)에 저장된 목적지 컬럼 어드레스는 컬럼 카운터(424)에 초기

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값으로 로딩된다. 이에 컬럼 카운터(424)에서는 이 값으로부터 카운팅을 시작한다. 로우 카운터(414)와 컬럼 카운터(424)는 1 페이지 분량의 데이터가 메인 메모리 코아(420)에 라이트될 때까지 카운팅 동작을 수행한다. 따라서, 메인 메모리 코아(420)는 쓰기 동작을 수행한다.

이와 같이 버퍼 메모리 코아의 카피동작 시작에서 종료시 까지 INT 신호는 액티브 상태를 유지한다. 따라서, 호스트(300)에서는 메인 메모리 코아(420)의 동작이 수행 중이라는 상태를 확인하게 된다. 이 기간동안에는 호스트에서는 SDRAM 동작 중 인터럽트 상태를 유지한다.

메인 메모리 코아(420)에 데이터 복사가 완료되면, PRM 동작이 완료된다. 이에 WAIT 신호는 넌액티브 상태로 천이되므로 호스트에서 PRM 동작의 완료를 인식하게 된다.

호스트(300)에서 WAIT 및 INT 신호의 상태를 체크하여 WAIT 신호의 액티브 기간동안에는 플래쉬 관련 새로운 명령을 발생하지 않으며, INT 신호의 액티브 기간동안에는 SDRAM 관련 새로운 명령을 발생하지 않는다. 그러나, WAIT 신호는 액티브 상태이나 INT 신호가 넌액티브(non-active) 상태인 버퍼링 기간동안에는 호스트(300)는 새로운 SDRAM 명령을 발생하여 플래쉬 동작과는 관계없이 메인 메모리 코아(420)를 통하여 동시에 다른 작업을 수행할 수 있다.

호스트(300)에서 WAIT 신호 및 INT 신호 가 모두 넌 액티브 상태로 복귀하면, 목적지 어드레스로 지정된 저장영역의 데이터를 통상적인 SDRAM 리드 동작을 통하여 액세스함으로써 플래쉬 메모리(314)에 저장된 데이터의 리드 동작을 완료한다.

2) 페이지 라이트 모드(PWM : Page Write Mode)

호스트(300)로부터 제공된 CKE, DCS, RAS, FCS, RE 신호가 액티브되면 SDRAM 제어 로직부(461)에서는 RA, CA 제어신호를 액티브시켜서 제1 및 제2 선택기(416, 417)가 레지스터(413)를 선택하도록 스위칭시킨다. 동시에 로우 어드레스 신호가 레지스터(413)에 저장된다. 라이트 동작시에는 레지스터(413)에 저장된 어드레스는 소스 어드레스가 된다.

또한, ML 제어 로직부(462)에서는 FCS 신호의 액티브 상태에 응답하여 WAIT 신호를 발생하여 호스트(300)로 출력한다. 따라서, 호스트(300)에서는 WAIT 신호의 액티브 상태를 체크하여 ML-SDRAM의 링크동작상태를 확인한다.

호스트(300)로부터 어드레스 로딩이 완료되면, 레지스터(413)에 저장된 로우 및 컬럼 어드레스를 메인 메모리 코아(420)로 제공한다. 레지스터(413)에 저장된 로우 어드레스는 로우 카운터(414)에 초기값으로 로딩된다.

데이터선(304)을 통하여 플래쉬 어드레스 데이터가 제1 데이터 입력부(440)를 통해 입력된다. 입력된 플래쉬 어드레스 데이터는 플래시 어드레스 레지스터(463)에 저장된다. 레지스터(463)에 저장된 어드레스 데이터는 플래쉬 메모리에 쓸 영역의 시작 어드레스로 제공된다.

이어서, 로우 카운터(414)에서는 이 값으로부터 카운팅을 시작한다. 또한, 레지스터(413)에 저장된 컬럼 어드레스는 컬럼 카운터(424)에 초기값으로 로딩된다. 이에 컬럼 카운터(424)에서는 이 값으로부터 카운팅을 시작한다. 로우 카운터(414)와 컬럼 카운터(424)는 1 페이지 분량의 데이터가 리드될 때까지 카운팅 동작을 수행한다. 따라서, 메인 메모리 코아(420)로부터 1 페이지 분량의 데이터가 액세스된다.

ML 제어 로직부(462)에서는 CR 카피 리드 제어신호를 발생하여 액세스된 데이터가 버퍼 메모리 코아(430)로 인가되도록 카피 패스 스위치(464)를 제어한다. 그리고, BRA, BCA 어드레스 신호를 버퍼 메모리 코아(430)에 제공하여 메인 메모리 코아(420)로부터 제공된 카피 데이터를 저장시킨다.

ML 제어 로직부(462)에서는 카피동작이 수행되는 동안 INT 신호를 액티브 상태로 유지시켜서 호스트(300)에 현재 메인 메모리 코아(420)의 동작 중임을 알린다.

카피 리드 동작이 완료되면, INT 신호는 넌 액티브 상태로 천이된다. 그리고, 카피 패스 스위치(464)는 차단된다.

호스트(300)로부터 어드레스 로딩동작이 완료되면, ML 제어 로직부(462)는 CLE, CE, WE 신호들을 액티브 상태로 발생시켜서 플래쉬 메모리(314)에 라이트 커맨드를 제공한다. 이어서, CLE 신호 대신에 ALE 신호를 액티브 상태로 발생하고, 레지스터(463)에 저장된 어드레스 데이터를 제2 데이터 입출력부(450)를 통하여 플래쉬 메모리(314)에 제공한다.

플래쉬 메모리(314)에서는 제공된 어드레스 데이터를 입력하고 입력된 어드레스 데이터를 시작 어드레스로 하여 1페이지 분량의 데이터를 라이트할 준비를 한다.

버퍼 메모리 코아(430)로부터 독출된 데이터는 제2 데이터 입출력버퍼(450)를 통하여 플래쉬 메모리(314)에 제공된다. 플래쉬 메모리(314)에서는 입력된 데이터를 지정된 저장영역에 저장시킨다. 플래쉬 메모리에서는 쓰기동작 중에는 RB 신호를 액티브 상태로 유지하여 ML 제어 로직부(462)에 알린다. 쓰기 동작이 완료되면 RB 신호가 넌액티브 상태로 천이되고, 이를 응답하여 ML 제어 로직부(462)는 WAIT 신호를 넌액티브 상태로 천이시킴으로써 호스트(300)에서는 PWM 동작이 완료되었음을 인지하게 된다.

따라서, 본 발명에서는 INT 신호가 액티브되는 기간을 제외하고는 플래쉬 메모리 동작과는 관계없이 항상 메인 메모리 코아(420)와 호스트(300) 사이의 데이터 전송이 가능하다.

3) 블록 리드 모드(BRM : Block Read Mode)

플래쉬 메모리에서 1블록은 수십 페이지 예컨대 32페이지들로 구성되므로, 버퍼 메모리 코아(430)의 사이즈가 페이지 사이즈일 경우에는 상술한 PRM 동작을 32번 반복함으로써 달성된다. 만약 버퍼 메모리 사이즈가 블록단위라면, PRM 동작에서 페이지 사이즈가 블록 사이즈로 변경됨으로써 달성된다.

4) 블록 라이트 모드(BWM : Block Write Mode)

플래쉬 메모리에서 1블록은 수십 페이지 예컨대 32페이지들로 구성되므로, 버퍼 메모리의 사이즈가 페이지 사이즈일 경우에는 상술한 PWM 동작을 32번 반복함으로써 달성된다. 만약 버퍼 메모리 사이즈가 블록단위라면, PwM 동작에서 페이지 사이즈가 블록 사이즈로 변경됨으로써 달성된다.

실시예를 참조하여 설명하였지만, 해당 기술 분야의 숙련된 당업자는 하기의 특허 청구의 범위에 기재된 본 발명의 사상 및 영역으로부터 벗어나지 않는 범위 내에서 본 발명을 다양하게 수정 및 변경시킬 수 있음을 이해할 수 있을 것이다.

상술한 실시예에서 대표적인 플래쉬 메모리 동작에 대해서만 설명하였지만 다른 동작들도 상술한 실시예와 유사한 방법으로 기존의 플래쉬 메모리 동작과 유사하게 링크 가능하다.

발명의 효과

상술한 바와 같이 본 발명에서는 디램과 같은 고속 동작의 휘발성 메모리 내부에 플래시 메모리와 같은 저속 동작 불휘발성 메모리를 인터페이스하는 제어회로를 구비함으로써 시스템에 대해 고속동작의 디램 인터페이스가 가능하므로 시스템에서는 디램 인터페이스만 하면 되므로 시스템 설계의 편리하고 작업의 용이성을 향상시킬 수 있다. 또한, 메모리 제어부가 간단해지므로 시스템 설계가 간단해져서 시스템 보드의 소형화가 가능해진다.

(57) 청구의 범위

청구항 1.

멀티 포트 휘발성 메모리 장치에 있어서,

외부 호스트 시스템 및 상기 멀티 포트 휘발성 메모리 장치간 데이터를 송수신하는 제1 포트;

수신된 데이터를 저장하고 요청된 저장된 데이터를 읽어들이는 휘발성 메인 메모리 코아;

수신된 데이터를 저장하고 요청된 저장된 데이터를 읽어들이는 휘발성 서브 메모리 코아;

상기 제1 포트와 결합되어, 마스터 모드에서 상기 휘발성 메인 메모리 코아와 상기 제1 포트간에 데이터를 주고받고, 슬레이브 모드에서 상기 휘발성 서브 메모리 코아와 상기 제1 포트간에 데이터를 주고받는 메인 인터페이스 회로;

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외부의 비휘발성 메모리 장치와 데이터를 송수신하는 제2 포트; 및

상기 제2 포트와 결합되어, 상기 슬레이브 모드에서 상기 휘발성 서브 메모리 코아와 상기 제2 포트간에 데이터를 주고받는 서브 인터페이스 회로를 구비한 것을 특징으로 하는 멀티 포트 휘발성 메모리장치.

청구항 2.

제1항에 있어서, 상기 메인 인터페이스부는

상기 외부 호스트 시스템으로부터 제공된 명령을 디코딩하여 내부 명령제어신호를 발생하는 명령디코더;

상기 외부 호스트 시스템으로부터 제공된 어드레스신호를 입력하여 내부 어드레스 신호를 발생하는 어드레스 버퍼;

상기 마스터 모드에서 상기 외부 호스트 시스템과 상기 휘발성 메인 메모리 코아 사이에 데이터를 주고받고, 상기 슬레이브 모드에서 상기 외부 호스트 시스템과 상기 휘발성서브 메모리 코아들간에 데이터를 주고받는 데이터 입출력버퍼;

상기 외부 호스트 시스템으로부터 제공된 마스터/슬레이브 모드선택신호에 응답하여 상기 어드레스버퍼 및 상기 데이터 입출력버퍼를 통하여 제공된 제어 데이터에 의해 상기 휘발성 메인 메모리 코아 및 상기 휘발성 서브 메모리 코아를 제어하여 상기 마스터 및 상기 슬레이브 동작모드를 제어하는 제어부를 구비한 것을 특징으로 하는 멀티 포트 휘발성 메모리장치.

청구항 3.

제2항에 있어서, 상기 서브 인터페이스부는

상기 제어부로부터 제공된 제어 데이터에 응답하여 상기 제2 포트에 연결된 외부 플래시 메모리와 상기 휘발성 서브 메모리 코아 사이의 데이터 전송을 제어하는 낸드 플래시 메모리 제어부를 포함하는 것을 특징으로 하는 멀티 포트 휘발성 메모리장치.

청구항 4.

제2항에 있어서, 상기 메인 인터페이스부는

상기 명령디코더로부터 제공된 전원 제어신호에 응답하여 상기 휘발성 서브 메모리 코아 및 상기 서브 인터페이스부의 전원을 관리하는 전원 관리부를 더 구비한 것을 특징으로 하는 멀티 포트 휘발성 메모리장치.

청구항 5.

제2항에 있어서, 상기 서브 메모리 코아의 사이즈는 적어도 상기 플래시 메모리의 작업단위인 페이지 사이즈 또는 블록 사이즈인 것을 특징으로 하는 멀티 포트 휘발성 메모리장치.

청구항 6.

멀티 포트 휘발성 메모리 장치에 있어서,

호스트 시스템과 어드레스, 커맨드 및 데이터를 직접 연결하기 위한 제1 포트;

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비휘발성 메모리 장치와 어드레스, 커맨드 및 데이터를 직접 연결하기 위한 제2 포트; 및

상기 제1 및 제2 포트에 결합되고, 상기 제1포트를 통하여 상기 호스트 시스템과 읽기 및 쓰기 동작을 수행하고, 상기 제2 포트를 통하여 상기 비휘발성 메모리 장치와 읽기 및 쓰기 동작을 수행하는 휘발성 메모리 코아를 포함하는 멀티 포트 휘발성 메모리 장치.

청구항 7.

제6항에 있어서, 상기 휘발성 메모리 코어는

상기 제1 포트에 결합되어 상기 호스트 시스템으로부터 마스터 모드 신호에응답하여 상기 제1 포트를 통하여 액세스 동작을 수행하는 휘발성 메인 메모리 코아; 및

상기 호스트 시스템으로부터 슬레이브 모드 신호에 응답하여 상기 제1 포트 및 상기 제2 포트를 통하여 액세스 동작을 수행하는 휘발성 서브 메모리 코아를 포함하는 멀티 포트 휘발성 메모리 장치.

청구항 8.

제7항에 있어서, 상기 휘발성 메인 메모리 코아는 상기 마스터 모드시 상기 제1 포트를 통하여 읽기 및 쓰기 동작을 수행하고, 상기 슬레이브 모드시 상기 휘발성 서브 메모리 코아와 카피 동작을 더 수행하는 것을 특징으로 하는 멀티 포트 휘발성 메모리 장치.

청구항 9.

제7항에 있어서, 상기 휘발성 서브 메모리 코아는 상기 슬레이브 모드시 상기 제1 포트를 통하여 읽기 및 쓰기 동작을 수행하고, 상기 슬레이브 모드시 상기 외부 호스트와 상기 비휘발성 메모리간에 비휘발성 읽기 및 쓰기 동작을 수행하여 상기 외부 호스트로부터 데이터를 수신하고 상기 외부 호스트로 데이터를 전송하는 것을 특징으로 하는 멀티 포트 휘발성 메모리 장치.

청구항 10.

제9항에 있어서, 상기 휘발성 서브 메모리 코어는 플래시 쓰기 동작 모드시 상기 제1 포트로부터 상기 외부 호스트로부터의 데이터를 수신하고 상기 제2 포트를 통하여 상기 데이터를 상기 비휘발성 메모리 장치로 제공하는 것을 특징으로 하는 멀티 포트 휘발성 메모리 장치.

청구항 11.

제9항에 있어서, 상기 휘발성 서브 메모리 코아는 플래시 읽기 동작 모드시 상기 제2 포트를 통하여 상기 비휘발성 메모리로부터 데이터를 수신하고, 상기 제1 포트를 통하여 상기 외부 호스트로 상기 데이터를 제공하는 것을 특징으로 하는 멀티 포트 휘발성 메모리 장치.

청구항 12.

제9항에 있어서, 상기 휘발성 서브 메모리 코어는 페이지 읽기 동작 모드시 상기 제2 포트를 통하여 상기 비휘발성 메모리로부터 데이터를 수신하고, 1 페이지 크기의 단위로 상기 휘발성 메인 메모리 코아로 상기 데이터를 제공하는 것을 특징으로하는 멀티 포트 휘발성 메모리 장치.

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청구항 13.

제12항에 있어서, 인터럽트 신호가 비활성화 상태인 경우 상기 휘발성 서브 메모리 코아로부터 수신된 상기 휘발성 메인 메모리 내의 데이터는 상기 외부 호스트에 의해 상기 제1 포트를 통하여 액세스 가능한 것을 특징으로 하는

멀티 포트 휘발성 메모리 장치.

청구항 14.

제13항에 있어서, 상기 휘발성 서브 메모리 코어는 대기 신호가 비활성화 상태인 경우 상기 비휘발성 메모리와 읽기/쓰기 동작을 수행하는 것을 특징으로 하는 멀티 포트 휘발성 메모리 장치.

청구항 15.

제9항에 있어서, 상기 휘발성 메인 메모리 코어는 페이지 쓰기 동작 모드시 상기 제1 포트를 통하여 상기 외부 호스트로부터 데이터를 수신하고, 상기 비휘발성 메모리 장치로의 쓰기 동작을 위해 1 페이지 크기의 단위로 상기 휘발성 서브 메모리 코아로 상기 데이터를 제공하는 것을 특징으로 하는 멀티 포트 휘발성 메모리 장치.

청구항 16.

제15항에 있어서, 상기 메인 메모리 코아는 상기 데이터가 상기 휘발성 서브 메모리 코아로 제공된 후에 인터럽트 신호가 비활성화 상태인 경우 상기 제1 포트를 통하여 상기 외부 호스트에 의해서 액세스 가능한 것을 특징으로 하는 멀티 포트 휘발성 메모리 장치.

청구항 17.

제15항에 있어서, 상기 휘발성 서브 메모리 코아는 대기 신호가 비활성화 상태인 경우 상기 비휘발성 메모리와 읽기/쓰기 동작을 수행하는 것을 특징으로 하는 멀티 포트 휘발성 메모리 장치.

청구항 18.

제7항에 있어서, 상기 비휘발성 메모리, 상기 휘발성 메인 메모리 코아 및 상기 휘발성 서브 메모리 코아는 단일 패키지 내에 포함되는 것을 특징으로 하는 멀티 포트 휘발성 메모리 장치.

청구항 19.

제6항에 있어서, 상기 비휘발성 메모리 장치는 NAND 플래시 메모리이고, 상기 멀티 포트 휘발성 메모리 장치는 SDRAM을 포함하는 것을 특징으로 하는 멀티 포트 휘발성 메모리 장치.

청구항 20.

메인 메모리 코아;

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버퍼 메모리 코아;

호스트와 연결된 제1 데이터 입출력 포트와 상기 메인 메모리 코아 사이에 연결되어 데이터의 입출력을 구동하는 제1 데이터 입출력부;

플래쉬 메모리와 연결된 제2 데이터 입출력 포트와 상기 버퍼 메모리 코아 사이에 연결되어 데이터의 입출력을 구동하는 제2 데이터 입출력부;

상기 메인 메모리 코아의 어드레스 신호를 저장하기 위한 제1 어드레스 레지스터;

상기 제1 및 제2 데이터 입출력부 사이에 연결되어 상기 플래쉬 메모리의 어드레스 신호를 저장하기 위한 제2 어드레스 레지스터; 및

제어부를 구비하고,

상기 제어부는

상기 메인 메모리 코아의 데이터 리드 또는 라이트 동작 모드에서는

상기 호스트로부터 제공된 어드레스 신호에 의해 상기 메인 메모리 코아를 어드레싱하고, 상기 제1 데이터 입출력부를 통하여 데이터를 리드 또는 라이트하고,

상기 플래쉬 메모리의 데이터 리드 동작 모드에서는,

상기 호스트로부터 제공된 소스 어드레스 신호를 상기 제1 데이터 입출력부를 통하여 상기 제2 어드레스 레지스터에 저장하고, 목적지 어드레스 신호를 상기 제1 어드레스 레지스터에 저장하고, 상기 제2 어드레스 레지스터에 저장된 소스 어드레스 신호를 상기 플래쉬 메모리의 시작 어드레스로 상기 제2 데이터 입출력부를 통하여 상기 플래쉬 메모리에 제공하고, 상기 플래쉬 메모리로부터 독출된 데이터를 상기 버퍼 메모리 코아에 저장하고, 상기 제1 어드레스 레지스터에 저장된 목적지 어드레스를 메인 메모리 코아의 시작 어드레스로 하여 상기 버퍼 메모리 코아에 저장된 데이터를 상기 메인 메모리 코아에 카피시키고, 상기 메인 메모리 코아에 카피된 데이터를 상기 제1 데이터 입출력부를 통하여 호스트로 독출시키며,

상기 플래쉬 메모리의 데이터 라이트 동작 모드에서는,

상기 호스트로부터 제공된 목적지 어드레스 신호를 상기 제1 데이터 입출력부를 통하여 상기 제2 어드레스 레지스터에 저장하고, 소스 어드레스 신호를 상기 제1 어드레스 레지스터에 저장하고, 상기 제1 어드레스 레지스터에 저장된 소스 어드레스 신호를 상기 메인 메모리 코아의 시작 어드레스로 하여 상기 메인 메모리 코아의 데이터를 상기 버퍼 메모리 코아에 카피시키고, 상기 버퍼 메모리 코아에 카피된 데이터를 상기 제2 데이터 입출력부를 통하여 플래쉬 메모리에 출력시키는 것을 특징으로 하는 저속 메모리 링크형 고속 메모리 장치.

청구항 21.

제1 속도로 동작하는 고속 메모리를 억세스하는 호스트;

상기 제1 속도보다 낮은 속도인 제2 속도로 동작하는 저속 메모리; 및

상기 저속 메모리와 저속으로 직접 인터페이스하고 상기 호스트와 고속으로 직접 인터페이스하여, 상기 저속 메모리를 상기 호스트에 고속으로 링크시키기 위한 메모리 링크 고속 메모리를 포함하는 것을 특징으로 하는 데이터 처리 장치.

청구항 22.

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호스트;

불휘발성 메모리; 및

상기 불휘발성 메모리와 제1포트를 통하여 직접 인터페이스하고 상기 호스트와 제2 포트를 통하여 직접 인터페이스하여, 상기 불휘발성 메모리를 상기 호스트에 링크시키기 위한 휘발성 메모리를 포함하는 것을 특징으로 하는 데이터 처리 장치.

청구항 23.

호스트와 연결하기 위한 연결포트;

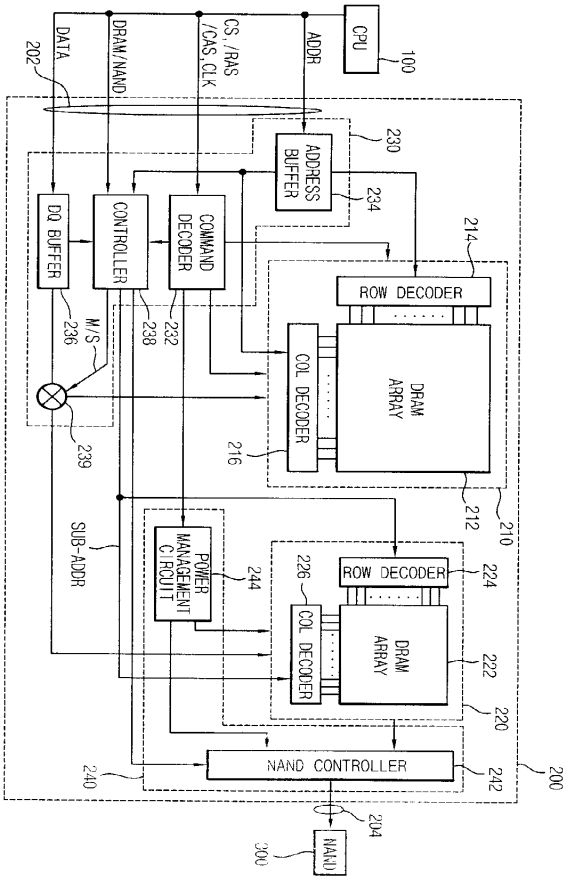
불휘발성 메모리; 및

상기 불휘발성 메모리와 직접 연결되고 상기 호스트와 상기 연결포트를 통하여 직접 인터페이스하여, 상기 불휘발성 메모리를 상기 호스트에 링크시키기 위한 메모리 링크 휘발성 메모리를 하나의 패키지에 실장시킨 것을 특징으로 하는 멀티 칩 반도체 장치.

도면

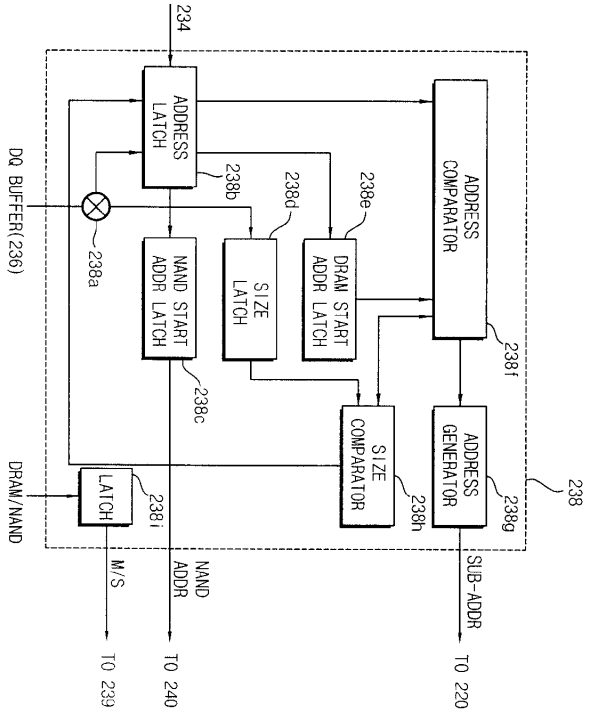
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도면



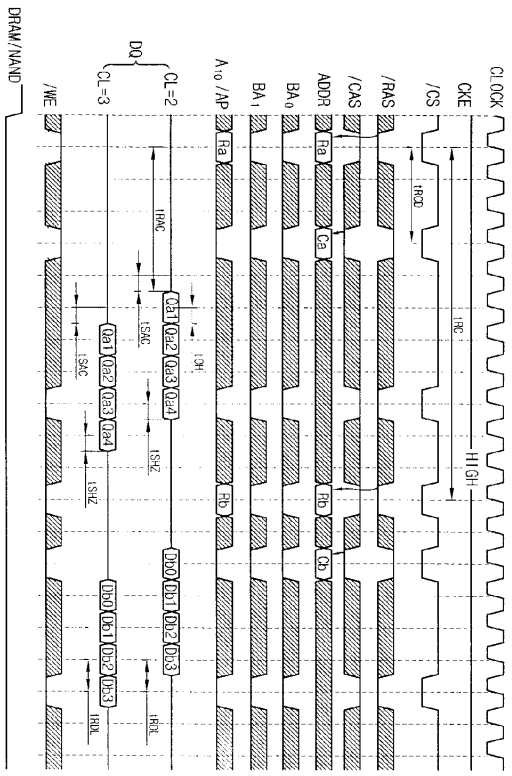
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도면2

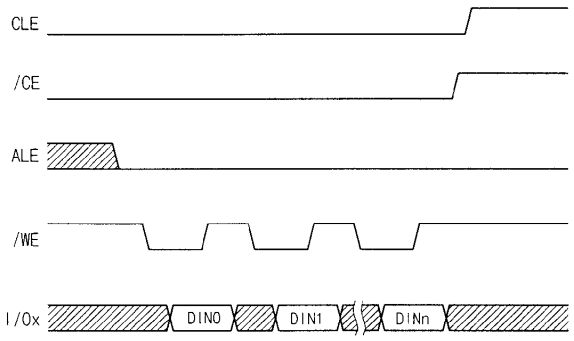


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도면3

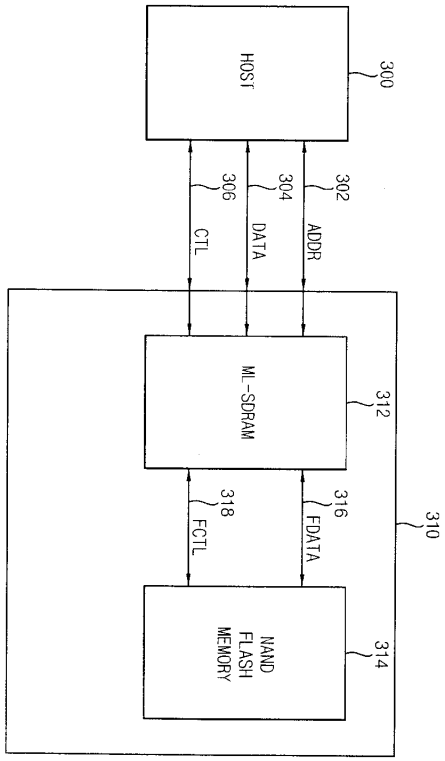


도면4



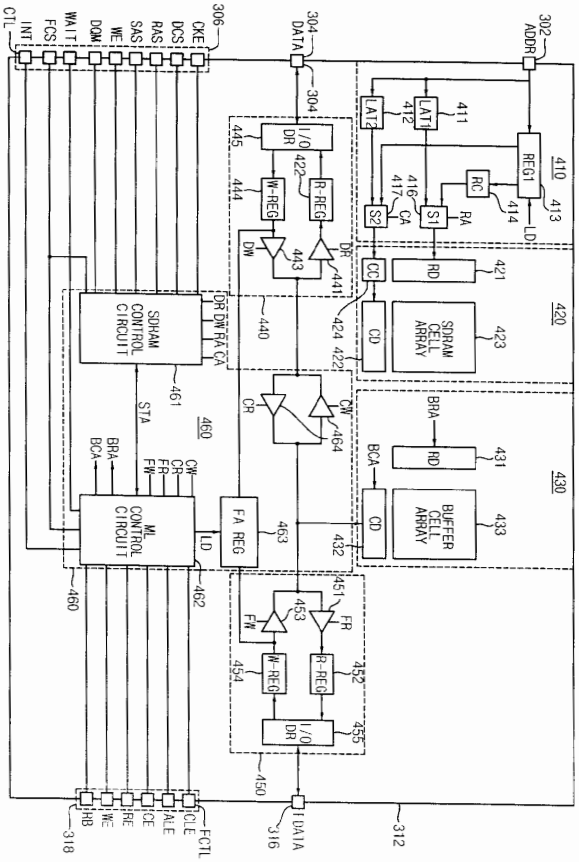
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도면5



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도면



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Patents KR 100606242 B1

Volatile Memory Device for buffering between non-Volatile Memory and host, Multi-chip packaged Semiconductor Device and Apparatus for processing data using the same

Abstract

Disclosed is a volatile memory operating as a master to a nonvolatile memory. The memory of the present invention includes a main memory core and a sub memory core. In addition, a first port for transmitting data with an external system, a second port for transmitting data with an external flash memory, and an interface between the main memory core and the external system in the master mode through the first port, the slave mode And a main interface unit for interfacing the sub-memory core with the external system, and a sub-interface unit for interfacing the sub-memory core with the external nonvolatile memory in the slave mode through the second port. Therefore, the high speed volatile memory operates as the master for the low speed nonvolatile memory, thereby simplifying the memory control of the system.

Images (6)



Classifications

» G11C7/1075 Input/output [I/O] data interface arrangements, e.g. I/O data control circuits, I/O data buffers for multiport memories each having random access ports and serial ports, e.g. video RAM

View 5 more classifications

KR100606242B1

South Korea

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Other languages: Korean

Inventor: 심재원, 손원구

Worldwide applications

2005 KR US JP CN 2008 US US

Application KR1020050006176A events

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2006-07-31 Application granted

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Info: Patent citations (21), Cited by (46), Legal events, Similar documents, Priority and Related Applications

External links: Espacenet, Global Dossier, Discuss

Claims (23)

Hide Dependent

1. A multi-port volatile memory device,

A first port for transmitting and receiving data between an external host system and the multi-port volatile memory device;

A volatile main memory core for storing the received data and reading the requested stored data;

A volatile sub memory core for storing the received data and reading the requested stored data;

A main interface circuit coupled with the first port to exchange data between the volatile main memory core and the first port in a master mode and to exchange data between the volatile sub memory core and the first port in a slave mode;

A second port for transmitting and receiving data with an external nonvolatile memory device; And

And a sub interface circuit coupled to the second port to exchange data between the volatile sub memory core and the second port in the slave mode.

2. The method of claim 1, wherein the main interface unit

A command decoder for generating an internal command control signal by decoding a command provided from the external host system;

An address buffer configured to input an address signal provided from the external host system to generate an internal address signal;

A data input / output buffer for exchanging data between the external host system and the volatile main memory core in the master mode and exchanging data between the external host system and the volatile sub memory core in the slave mode;

The volatile main memory core and the volatile sub memory core are controlled by the control data provided through the address buffer and the data input / output buffer in response to the master / slave mode selection signal provided from the external host system to control the master and the slab. A multi-port volatile memory device comprising a control unit for controlling the Eve operation mode.

3. The method of claim 2, wherein the sub interface unit

And a NAND flash memory controller configured to control data transfer between the external flash memory connected to the second port and the volatile sub memory core in response to the control data provided from the controller.

4. The method of claim 2, wherein the main interface unit

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And a power manager configured to manage power of the volatile sub memory core and the sub interface unit in response to a power control signal provided from the command decoder.

5. The multi-port volatile memory device according to claim 2, wherein the size of the sub memory core is at least a page size or a block size which is a work unit of the flash memory.

6. A multi-port volatile memory device,

A first port for directly connecting addresses, commands, and data with the host system;

A second port for directly connecting an address, a command, and data with the nonvolatile memory device; And

A volatile memory coupled to the first and second ports and performing a read and write operation with the host system through the first port and a read and write operation with the nonvolatile memory device through the second port. Multi-port volatile memory device containing core.

7. The method of claim 6, wherein the volatile memory core is

A volatile main memory core coupled to the first port to perform an access operation through the first port in response to a master mode signal from the host system; And

And a volatile sub memory core configured to perform an access operation through the first port and the second port in response to a slave mode signal from the host system.

8. 8. The method of claim 7, wherein the volatile main memory core performs a read and write operation through the first port in the master mode, and further performs a copy operation with the volatile sub memory core in the slave mode. Multi-Port Volatile Memory Device.

9. 9. The method of claim 7, wherein the volatile sub memory core performs a read and write operation through the first port in the slave mode, and performs a nonvolatile read and write operation between the external host and the nonvolatile memory in the slave mode. And receiving data from the external host and transmitting data to the external host.

10. The memory device of claim 9, wherein the volatile sub memory core receives data from the external host from the first port and provides the data to the nonvolatile memory device through the second port in a flash write operation mode. Multiport volatile memory device.

11. The method of claim 9, wherein the volatile sub memory core receives data from the nonvolatile memory through the second port and provides the data to the external host through the first port in a flash read operation mode. Multiport volatile memory device.

12. The data storage device of claim 9, wherein the volatile sub memory core receives data from the nonvolatile memory through the second port in a page read operation mode and provides the data to the volatile main memory core in units of one page size. Multi-port volatile memory device, characterized in that.

13. 13. The method of claim 12, wherein the data in the volatile main memory received from the volatile sub memory core when the interrupt signal is in an inactive state is accessible through the first port by the external host.

Multi-Port Volatile Memory Device.

14. The multi-port volatile memory device of claim 13, wherein the volatile sub memory core performs a read / write operation with the nonvolatile memory when a standby signal is in an inactive state.

15. The volatile main memory core of claim 9, wherein the volatile main memory core receives data from the external host through the first port in a page write operation mode, and in units of one page size for writing to the nonvolatile memory device. And providing the data to a volatile sub memory core.

16. 16. The multi-port volatile memory of claim 15, wherein the main memory core is accessible by the external host through the first port when the interrupt signal is inactive after the data is provided to the volatile sub memory core. Device.

17. The multi-port volatile memory device of claim 15, wherein the volatile sub memory core performs a read / write operation with the nonvolatile memory when a standby signal is in an inactive state.

18. 8. The multi-port volatile memory device of claim 7, wherein the nonvolatile memory, the volatile main memory core and the volatile sub memory core are included in a single package.

19. 7. The multi-port volatile memory device of claim 6, wherein the non-volatile memory device is a NAND flash memory and the multi-port volatile memory device comprises SDRAM.

20. Main memory core;

Buffer memory core;

A first data input / output unit connected between a first data input / output port connected to a host and the main memory core to drive input / output of data;

A second data input / output unit connected between a second data input / output port connected to a flash memory and the buffer memory core to drive input / output of data;

A first address register for storing an address signal of the main memory core;

A second address register connected between the first and second data input / output units to store an address signal of the flash memory; And

With a control unit,

The control unit

In the data read or write operation mode of the main memory core

Address the main memory core according to the address signal provided from the host, read or write data through the first data input / output unit,

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In the data read operation mode of the flash memory,

The source address signal provided from the host is stored in the second address register through the first data input / output unit, the destination address signal is stored in the first address register, and the source address signal stored in the second address register is stored in the flash. Providing the flash memory as the start address of the memory to the flash memory through the second data input / output unit, storing data read from the flash memory in the buffer memory core, and storing a destination address stored in the first address register at the start of the main memory core. Copy the data stored in the buffer memory core into the main memory core as an address, and read the data copied into the main memory core to the host through the first data input / output unit,

in the data write operation mode of the flash memory,

A destination address signal provided from the host is stored in the second address register through the first data input / output unit, a source address signal is stored in the first address register, and a source address signal stored in the first address register is stored in the main; Copying the data of the main memory core into the buffer memory core as a start address of the memory core, and outputting the data copied into the buffer memory core to the flash memory through the second data input / output unit. Type high speed memory device.

21. A host accessing a high speed memory operating at a first speed;

A low speed memory operating at a second speed, the speed lower than the first speed; And

And a memory link high speed memory for directly interfacing with the low speed memory at low speed and directly interfacing with the host at high speed to link the low speed memory to the host at high speed.

22. Host;

Nonvolatile memory; And

And a volatile memory for directly interfacing with the nonvolatile memory through a first port and directly interfacing with the host through a second port to link the nonvolatile memory to the host.

23. A connection port for connecting with the host;

Nonvolatile memory; And

And a memory link volatile memory connected directly to the nonvolatile memory and directly interfaced with the host through the connection port to link the nonvolatile memory to the host in a single package. .

Description

Multi-port volatile memory device performing a buffering operation between a nonvolatile memory and a host, a multi-chip package semiconductor device using the same, and a data processing device using the same (Volatile Memory Device for buffering between non-Volatile Memory and host, Multi-chip packaged Semiconductor Device and Apparatus for processing data using the same)

1 is a block diagram of a preferred embodiment of a master volatile memory according to the present invention.

FIG. 2 is a detailed block diagram of the controller of FIG. 1. FIG.

3 and 4 are operation timing diagrams of FIG.

5 is a configuration diagram of a preferred embodiment of a data processing apparatus according to the present invention.

FIG. 6 is an internal configuration diagram of a preferred embodiment of the memory link volatile memory device of the multichip semiconductor device of FIG. 5.

The present invention relates to a master volatile memory device, and more particularly, to a dual port synchronous DRAM operating as a master for a nonvolatile memory operating as a slave.

Recently, as mobile phones equipped with camera phones or mobile phones with Internet access are commercially available, a large capacity of memory for storing image data of mobile phones is required.

In general, a mobile phone mainly uses a quinos flash memory capable of high speed operation and random access to store codes for data processing. However, Noah-type flash memory is capable of high-speed random access, but it is not widely spread in large capacity due to high cost compared to capacity.

On the other hand, NAND flash memory is low in cost compared to Noah flash memory, and the cost of capacity is low, so the demand for digital cameras is rapidly expanding in the field of image data storage.

In general, in a mobile phone system, the central processing unit stores image data picked up from a camera in a DRAM, and processes digital images such as compression and stores them in a NAND flash memory. The central processing unit controls the DRAM and the NAND flash memory through each interface, and the DRAM and the NAND flash memory exchange data through a direct memory access (DMA) block.

Therefore, the performance of the entire system is degraded by the speed of the NAND flash memory operating at low speed. In addition, since the hardware connection between the central processing unit, the DRAM, and the NAND flash memory is required, the package size increases when the system is chipped, thereby preventing the miniaturization and weight of the mobile phone system.

Toshiba Corp., Japan, introduced an interface technology that drives NAND flash memory like SRAM (STATIC RANDOM ACCESS MEMORY). Toshiba technology uses SRAM as a buffer to buffer data transfers between the system and the flash, controlling the flash at the interface speed of the SRAM between the system and the SRAM.

In addition, Japanese Laid-Open Patent Publication No. 2002-95109 discloses a technology in which a DRAM, a NAND flash memory, and a control circuit are modularized into one chip. The control circuit of the module of this technology stores the external data in the DRAM once and then stores the data stored in the DRAM in the flash memory in response to the external command. In addition, when data to be written to the flash is to be read from the outside, the data of the flash is once transmitted to the DRAM, and then the data transmitted to the DRAM is read out to the outside. Thus, the module is operated by the external system and the SDRAM interface.

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These prior arts all control the data transfer between the system and the buffer memory, the buffer memory and the flash memory via the interface control circuitry between the flash memory and the buffer memory.

SUMMARY OF THE INVENTION An object of the present invention is to provide a master dual-port synchronous DRAM that slaves a low-speed nonvolatile memory such as a flash memory to simplify memory control in a host system in order to solve such problems of the prior art.

The present invention also provides a low speed memory link type high speed memory device that controls a low speed flash memory to link the low speed memory to a host system.

The present invention also provides a data processing device including the low speed memory link type high speed memory device.

The present invention also provides a multichip semiconductor device in which a nonvolatile memory such as a flash memory and the memory link type high speed memory device are mounted in one package.

In order to achieve the above object, the multi-port volatile memory device of the present invention comprises a first port for transmitting and receiving data between an external host system and the multi-port volatile memory device; A volatile main memory core for storing the received data and reading the requested stored data; A volatile sub memory core for storing the received data and reading the requested stored data; A main interface circuit coupled with the first port to exchange data between the volatile main memory core and the first port in a master mode and to exchange data between the volatile sub memory core and the first port in a slave mode; A second port for transmitting and receiving data with an external nonvolatile memory device; And a sub interface circuit coupled with the second port to exchange data between the volatile sub memory core and the second port in the slave mode.

Here, the volatile memory device of the present invention is a DRAM of high speed operation, and the nonvolatile memory device of low speed operation is preferably composed of a NAND type flash memory. In this case, the volatile sub memory core may be configured as an SRAM.

In the present invention, the main interface unit decodes a command provided from an external host system to generate an internal command control signal, an address buffer for inputting an address signal provided from an external host system to generate an internal address signal, and in the master mode. Data input / output buffers that exchange data between the external host system and the volatile main memory core, exchange data between the external host system and the volatile sub memory cores in the slave mode, and a master / slave provided from an external host system. The master and slave operation modes are controlled by controlling the volatile main memory core and the volatile sub memory core by control data provided through the address buffer and the data input / output buffer in response to the eve mode selection signal. And a control unit that controls.

In the present invention, the sub-interface circuit includes a NAND flash memory controller for controlling data transfer between the external flash memory connected to the second port and the sub memory core in response to control data provided from the controller.

In addition, in the present invention, the main interface circuit may further include a power management unit for managing the power of the volatile sub memory core and the volatile sub interface unit in response to the command control signal provided from the command decoder.

In order to achieve the above object, the multi-port volatile memory device of the present invention comprises: a first port having external access to a host system; A second port for external access with the nonvolatile memory device; And a volatile memory core coupled to the first and second ports for external access.

In order to achieve the above object, the low speed memory link type high speed memory device of the present invention includes a main memory core, a buffer memory core, a first data input / output unit, a second data input / output unit, a first address register, a second address register, and a controller. do. The first data input / output unit is connected between a first data input / output port connected to a host and the main memory to drive input / output of data, and the second data input / output unit is connected between a second data input / output port connected to a flash memory and the buffer memory. Drives input and output of data. The first address register stores the address signal of the main memory core. A second address register is connected between the first and second data input / output units to store an address signal of a flash memory. In the data read or write operation mode of the main memory core, the controller may address the main memory core by an address signal provided from the host, and read or write data through the first data input / output unit. In the data read operation mode of the flash memory, the controller stores a source address signal provided from the host in the second address register through the first data input / output unit. stores a destination address signal in the first address register; The source address signal stored in the second address register is provided to the flash memory through the second data input / output unit as a start address of the flash memory, the data read from the flash memory is stored in the buffer memory core, and the buffer Copy the data stored in the memory core to the main memory core with the destination address stored in the first address register as a start address, and call the data copied into the memory core through the first data input / output unit. Trojan thereby read out. In the data write operation mode of the flash memory, the controller stores a destination address signal provided from the host in the second address register through the first data input / output unit, stores a source address signal in the first address register, Copying the data of the main memory core to the buffer memory core using the source address signal stored in the first address register as the start address of the main memory core, and copying the data copied to the buffer memory core to the second data input / output unit. To the flash memory.

In order to achieve the above object, the data processing apparatus of the present invention includes a host for accessing a high speed memory operating at a first speed; A low speed memory operating at a second speed, the speed lower than the first speed; And a memory link high speed memory for low speed interface with the low speed memory and high speed interface with the host to link the low speed memory to the host at high speed.

In order to achieve the above object, the data processing apparatus of the present invention comprises a host; Nonvolatile memory; And a volatile memory for interfacing with the nonvolatile memory through a first port and interfacing with the host through a second port to link the nonvolatile memory to the host.

In order to achieve the above object, the multi-chip semiconductor device of the present invention comprises a connection port for connecting with the host; Nonvolatile memory; And a memory link volatile memory connected to the nonvolatile memory and interfacing with the host through the connection port to link the nonvolatile memory to the host in one package.

Hereinafter, exemplary embodiments of the present invention will be described in detail with reference to the accompanying drawings. This embodiment is described in sufficient detail to enable those skilled in the art to practice the invention.

<Example 1>

1 shows a configuration of a master volatile memory according to the present invention. Referring to FIG. 1, the system 100 is connected to a NAND type flash memory 300 through a master volatile memory and a DRAM 200.

The DRAM 200 of the present invention includes a first port 202 connected to the system 100 in a dual port type, and a second port 204 connected to the NAND flash memory 300.

In addition, the DRAM 200 includes a main memory core 210 and a sub memory core 220. The main memory core 210 includes a cell array 212, a low decoder 214, and a column decoder 216. The sub memory core 220 includes a cell array 222, a row decoder 224, and a column decoder 226.

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In addition, the DRAM 200 may include a main interface unit 230 and a sub interface unit 240. The main interface unit 230 includes a command decoder 232, an address buffer 234, an input / output buffer 236, a controller 238, and a mode selector 239.

The command decoder 232 is a command provided from the external system 100, i.e., a DRAM control signal, for example, a chip select signal CS, a low strobe signal / RAS, a column strobe signal / CAS, a clock signal CLK, a write enable signal / WE. , Chip enable signal, and the like. The command decoder 232 decodes these control signals to interpret an operation mode such as writing or reading, and generates internal command control signals related to the operation mode to generate the main memory core 210, the sub interface unit 240, and the controller 238. To provide.

The address buffer 234 receives an address signal provided from the external system 100 and generates an internal address signal synchronized with a clock. The internal address signal is provided to the main memory core 210 and the controller 238. The internal address signals provided to the main memory core are row addresses and column addresses, and the internal address signals provided to the controller 238 are control data provided from the external system 100, for example, mode set data, initial address information of the NAND flash memory, Address information of the sub memory core 230.

The input / output buffer 236 buffers data input / output between the main memory core 210 or the sub memory core 220 and an external system. The input / output buffer 236 provides data size information of the NAND flash memory 300 to the controller 238.

The control unit 238 transfers NAND flash initial address information and address information of the sub memory core among the control data provided through the address buffer 234 to the sub interface unit 240, and master / slave based on the mode set data. Generate the mode selection signal (M / S). In the slave mode, the controller 238 controls the sub memory core 220 to control data writing and reading of the sub memory core 220.

The master / slave mode selector 239 selectively couples the input / output buffer 236 to the main memory core 210 and the sub memory core 220 in response to the M / S signal.

The sub interface unit 240 includes a NAND controller 242 and a power manager 244. The NAND controller 242 interfaces the sub memory core 220 and the external flash memory 300 in the slave mode through the second port 204. The NAND control unit 242 transfers the NAND address information provided from the control unit 238 to the external flash memory 300 through the second port 204 to control the writing and reading of data in the flash memory 300.

The power management unit 244 manages the power of the sub memory core 220 and the NAND control unit 242 in response to the power control signal of the command decoder 232 to resume power supply in the operation mode and in the idle state the sub memory core (220 and the sub-interface unit 240 are cut off to manage unnecessary power consumption.

2, the controller 238 includes a switch 238a, an address latch 238b, a NAND start address latch 238c, a size latch 238d, a DRAM start address latch 238e, an address comparator 238f, Address generator 238g, size comparator 238h, and latch 238i.

FIG. 2 shows only blocks related to address processing in the configuration of the control unit 238, blocks for processing internal command control signals from the command decoder 232, and blocks for generating a mode selection signal (M / S), is omitted.

The switch 238a switches the size information provided from the input / output buffer 236 to the address latch 238b and the size latch 238d.

The address latch 238b latches and provides the data including the internal address information provided from the address buffer 234, the size information provided from the switch 238a, and the data provided from the size comparator 238h to the address comparator 238f.

The NAND start address latch 238c latches the address provided from the address latch 238b to generate a NAND start address NAND-Addr.

The size comparator 238h compares the data provided from the address comparator 238f with the data including the size information provided from the size latch 238d and provides the result to the address latch 238b. The address generator 238g generates the comparison information provided from the address comparator 238f as a sub address Sub Addr.

The latch 238i outputs the master / slave mode selection signal M / S to the mode selector 239 based on the DRAM / NAND flash mode signal DRAM / NAND.

1. Dual port overall operation algorithm

The entire main program performs idle state-DRAM mode-NAND flash mode-power management mode.

The power management mode includes power down in the idle state of the sub-memory core, and management of a refresh operation to maintain stored data when power is shut down.

2. Main memory mode

As shown in FIG. 3, in the DRAM mode, the DRAM / NAND signal goes low to perform a normal synchronous DRAM operation mode.

Referring to FIG. 3, first, the low address Ra is output to the address ADDR in response to the falling edge of the / RAS signal, and the column address Ca is the address ADDR in response to the falling edge of the / CAS signal. Is output. When the write enable signal / WE has a high level, the read enable mode operates in the read mode, and the data Qa1, Qa2, Qa3, and Qa4 of address a of the main memory core 210 corresponding to the low address Ra and the column address Ca are provided. Are read. Next, when / WE has a low level, it operates in the write mode, and data Db0, Db1, Db2, and Db3 are written to address b of the main memory core 210 by the low address Rb and the column address Cb. (write) The hatched sections in FIG. 3 are don't care sections.

3. Nand flash mode

When data is written to the NAND flash, the DRAM / NAND signal is turned high to connect the data path with the sub memory core 220. Accordingly, data to be written to the NAND flash 300 is written to the sub memory core 220 under the control of the controller 238. The control unit 238 activates the NAND control unit 242 when the data written in the sub memory core 220 reaches a block size, which is a unit of work of the NAND flash memory 300, to the second port 204. Writes in block units to the connected flash memory 300.

Referring to FIG. 4, the write operation of the NAND flash memory 300 is performed by the input / output line I / Ox of the second port 204 in response to the low level chip enable signal / CE and the low level write enable signal / WE. Outputs the data to the NAND flash memory. CLE is a command latch enable signal, and ALE is an address latch enable signal, which is used to multiplex a command and an address to the input / output line I / Ox, respectively

Accordingly, the size of the sub memory core 220 may be determined based on a block size that is a write unit of the NAND flash 300. For example, 1 Mb or less can be used.

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In addition, the NAND address uses the address generated in the system 100 as it is, and in the low state of the low strobe signal / RAS, the DRAM / NAND signal is made high and the address is stored in the controller 238 using the address buffer 234 Latch.

To read data from the flash memory, the data read from the flash memory 300 is written to the sub memory core 220 through the NAND controller 242, and then the data stored in the sub memory core 220 is read from the input / output buffer 236. Read to the system 100 through.

The read operation of the NAND flash memory 300 reads data from the flash memory 300 in response to the low level chip enable signal / CE and the high level write enable signal / WE, The read data is written to the sub memory core 220 through an input / output line I / Ox.

Therefore, the system can write and read data to and from the flash memory at the DRAM interface operating speed.

<Example 2>

5 shows a block configuration of a data processing system according to the present invention. Referring to FIG. 5, the data processing device includes a host 300 and a multi-chip semiconductor device 310. The host 300 includes a microprocessor and a memory controller. The host 300 and the multi-chip semiconductor device 310 are connected to each other through an address bus 302, a data bus 304, and a control bus 306. The multi-chip semiconductor device 310 is a multi-chip package (MCP) including a memory link SDRAM 312 and a NAND flash memory 314 as one package. The ML-SDRAM 312 and the NAND flash memory 314 are connected to each other through the data bus 316 and the control bus 318.

In the present invention, the address bus 302 and the data bus 304 have a structure of an address bus and a data bus of a conventional synchronous DRAM. The control bus 306 includes CLK, CKE, DCS, RAS, CAS, WE, and DQM signal lines, which are conventional DRAM control signal lines. It further includes an FCS, WAIT, etc. to perform a memory link command. The FCS is a NAND flash memory chip select signal, and the WAIT is a signal that notifies the host that the command is completed when the read, program, and erase operations of the NAND flash memory chip are completed. The control bus 318 includes CLE, ALE, CE, RE, WE, and RB signal lines, which are conventional NAND flash memory control signal lines.

6 illustrates an internal block configuration of the ML-SDRAM of FIG. 5. Referring to FIG. 6, the ML-SDRAM 312 includes an address generator 410, a main memory core 420, a sub memory core 430, a first data input / output unit 440, and a second data input / output unit 450.), And a control unit 460.

The address generator 410 may include a first latch 411 for latching a row address signal, a second latch 412 for latching a column address signal, a first address register 413 for storing an address signal, and a row counter (414, a first selector 416, and a second selector 417. In the DRAM operation mode, the address generator 410 latches the row address and the column address through the first and second latches 411 and 412 and provides them to the first and second selectors 416 and 417. The first and second selectors 416 and 417 select the first and second latches 411 and 412 in the DRAM operation mode in response to the RA and CA control signals to set the row address and the column address in the main memory core 420. It is provided as an address signal. The address generator 410 stores the row address and the column address in the first address register 413 in the copy operation mode. The row address stored in the first address register 413 is provided to the first selector 416 via the row counter 414, and the column address stored in the first address register 413 is provided to the second selector 417. . The first and second selectors 416 and 417 select the row counter 414 and the register 413 in the copy operation mode in response to the RA and CA control signals to select the row address and the column address of the main memory core 420. Provided by the address signal.

The main memory core 420 is a large work storage area, and includes a row decoder 421, a column decoder 422, a cell array 423, and a column counter 424. The row counter 414 generates continuous row addresses by setting the row address signal applied in the copy operation as an initial value. The column counter 424 generates continuous column addresses by setting the column address signals applied in the burst operation mode and the copy operation mode of the DRAM as initial values.

The sub memory core 430 is a buffer storage area of a page or block unit and includes a row decoder 431, a column decoder 432, and a cell array 433. The sub memory core 430 designates a cell by the buffer row address signal BRA and the buffer column address signal BCA provided from the controller 460.

The first data input / output unit 440 is an SDRAM data input / output interface and includes a read buffer 441, a read register 442, a write buffer 443, a write register 444, and an input / output driver 445. The read buffer 441 is controlled by the DRAM read control signal DR, and the write buffer 443 is controlled by the DRAM write control signal DW. The first data input / output unit 440 provides data transfer between the host 300 and the main memory core 420 at an SDRAM access operation speed.

The second data input / output unit 450 is a NAND flash memory data input / output interface, and includes a read buffer 451, a read register 452, a write buffer 453, a write register 454, and an input / output driver 455. The read buffer 451 is controlled by the flash read control signal FR, and the write buffer 453 is controlled by the flash write control signal FW. The second data input / output unit 450 provides data transfer between the NAND flash memory 314 and the sub memory core 430 at the NAND flash memory 314 access operation speed.

The control unit 460 includes an SDRAM control logic unit 461, an ML control logic unit 462, a flash address register 463, and a copy path switch 464.

The SDRAM control logic unit 461 inputs SDRAM control signals CKE, DCS, RAS, CAS, WE, DQM to decode a command, and outputs internal control signals DR, DW, RA, and CA according to the decoded command. Occurs. DR is a DRAM read control signal, DW is a DRAM write control signal, RA is a row address select signal, and CA is a column address select signal.

The ML control logic unit 462 generates the FCS signal provided from the host 300 and the flash memory control signals CLE, ALE, CE, RE, WE, and the like, and prepares / buses the RB provided from the flash memory 314. In response to the Ready / Busy) signal, a WAIT signal is generated and provided to the host 300. The ML control logic unit 462 generates a loading signal LD to control the copy address register 413 and the flash address register 463. The ML control logic unit 462 generates the row and column address signals BRA and BCA of the buffer memory core 430.

The SDRAM control logic unit 461 and the ML control logic unit 462 exchange operation state signals STA.

The flash address register 463 receives and stores flash address data from the host through the first data input / output unit 440, and stores address data stored in response to the LD control signal to the NAND flash memory 413 through the second data input / output unit. to provide.

The operation of the second embodiment of the present invention configured as described above is as follows.

1.SDRAM operation mode

In the SDRAM operation mode, the first and second selectors 416 and 417 of the address generator 410 are controlled to select the first and second latches 411 and 412, respectively. Therefore, the row address and column address provided from the host are provided to the main memory core 420 to address a particular cell.

In the read operation, the data read from the main memory core 420 is output to the host 300 through the first data input / output unit 440, and the data is provided from the host 300 in the write operation, and the data is supplied from the main memory core 420. is stored as

2. Memory link operation mode

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In the memory link operation mode, the ML-SDRAM 312 serves as a buffer for relaying data and commands between the host 300 and the flash memory 314.

1) Page Read Mode (PRM)

When the CKE, DCS, RAS, FCS, and WE signals provided from the host 300 are activated, the SDRAM control logic unit 461 activates the RA and CA control signals so that the first and second selectors 416 and 417 register 413. Switch to select. At the same time, the row address signal is stored in the register 413. In the read operation, the address stored in the register 413 becomes the destination address.

In addition, the ML control logic unit 462 generates a WAIT signal in response to the active state of the FCS signal and outputs the WAIT signal to the host 300. Therefore, the host 300 checks the active state of the WAIT signal to confirm the link operation state of the ML-SDRAM.

The column address signal is then stored in the register 413 while the CAS signal is active. In a read operation, the row and column addresses stored in the register 413 are provided as a start address of a destination of the main memory core 420 in which data read from the flash memory 314 is to be stored.

Flash address data is input through the first data input unit 440 through the data line 304. The input flash address data is stored in the register 463. The address data stored in the register 463 is provided as the start address of the storage area to be read from the flash memory 314.

When the address loading operation is completed from the host 300, the ML control logic unit 462 generates CLE, CE, and RE signals in an active state to provide a read command to the flash memory 314. Subsequently, the ALE signal is generated in an active state instead of the CLE signal, and the address data stored in the register 463 is provided to the flash memory 314 through the second data input / output unit 450.

The flash memory 314 receives the provided address data and accesses and outputs one page of data using the input address data as a start address.

Data read from the flash memory is stored in the buffer memory core 430 through the second data input / output unit 450. The buffer memory core 430 is addressed in response to the BRA and BCA signals of the ML control logic unit 462 to store one page of data.

When the storage of the flash memory data in the buffer memory core 430 is completed, the ML control logic unit 462 generates the BRA and BCA address signals to start accessing the data stored in the buffer memory core 430. In addition, the CW copy control signal is generated to control the copy pass switch 464 to apply the data of the buffer memory core 430 to the main memory core 420.

In addition, the LD control signal is applied to the register 413 to control the destination address signal stored in the register 413 to be applied to the main memory core 420. Destination row and column addresses stored in register 413 are provided to main memory core 420. The destination row address stored in register 413 is loaded to row counter 414 with an initial value. The row counter 414 starts counting from this value. Also, the destination column address stored in the register 413 is loaded to the column counter 424 with an initial value. The column counter 424 starts counting from this value. The row counter 414 and the column counter 424 perform counting operations until one page of data is written to the main memory core 420. Thus, the main memory core 420 performs a write operation.

As such, the INT signal remains active from the start to the end of the copy operation of the buffer memory core. Therefore, the host 300 checks the state that the operation of the main memory core 420 is being performed. During this period, the host remains interrupted during SDRAM operation.

When data copy is completed in the main memory core 420, the PRM operation is completed. As the WAIT signal transitions to the non-active state, the host recognizes the completion of the PRM operation.

The host 300 checks the states of the WAIT and INT signals and does not generate a flash related new command during the active period of the WAIT signal, and does not generate a new SDRAM related command during the active period of the INT signal. However, during the buffering period in which the WAIT signal is active or the INT signal is non-active, the host 300 generates a new SDRAM command and simultaneously changes the data through the main memory core 420 regardless of the flash operation. You can do it.

When both the WAIT signal and the INT signal return to the non-active state in the host 300, the data read operation stored in the flash memory 314 is completed by accessing the data in the storage area designated as the destination address through the normal SDRAM read operation. do.

2) Page Write Mode (PWM)

When the CKE, DCS, RAS, FCS, and RE signals provided from the host 300 are activated, the SDRAM control logic unit 461 activates the RA and CA control signals so that the first and second selectors 416 and 417 register 413. Switch to select. At the same time, the row address signal is stored in the register 413. In the write operation, the address stored in the register 413 becomes a source address.

In addition, the ML control logic unit 462 generates a WAIT signal in response to the active state of the FCS signal and outputs the WAIT signal to the host 300. Therefore, the host 300 checks the active state of the WAIT signal to confirm the link operation state of the ML-SDRAM.

When address loading from the host 300 is completed, the row and column addresses stored in the register 413 are provided to the main memory core 420. The row address stored in register 413 is loaded to row counter 414 with an initial value.

Flash address data is input through the data line 304 through the first data input unit 440. The input flash address data is stored in the flash address register 463. The address data stored in the register 463 is provided as the start address of the area to be written to the flash memory.

Row counter 414 then begins counting from this value. In addition, the column address stored in the register 413 is loaded to the column counter 424 with an initial value. The column counter 424 starts counting from this value. The row counter 414 and the column counter 424 perform counting operations until one page of data is read. Thus, one page of data is accessed from the main memory core 420.

The ML control logic unit 462 generates a CR copy read control signal to control the copy pass switch 464 so that the accessed data is applied to the buffer memory core 430. The BRA and BCA address signals are provided to the buffer memory core 430 to store copy data provided from the main memory core 420.

The ML control logic unit 462 keeps the INT signal active while the copy operation is performed to inform the host 300 that the main memory core 420 is currently operating.

When the copy read operation is complete, the INT signal transitions to the non-active state. The copy pass switch 464 is cut off.

When the address loading operation is completed from the host 300, the ML control logic unit 462 generates CLE, CE, and WE signals in an active state to provide a write command to the flash memory 314. Subsequently, the ALE signal is generated in an active state instead of the CLE signal, and the address data stored in the register 463 is provided to the flash memory 314 through the second data input / output unit 450.

The flash memory 314 prepares to write one page of data by inputting the provided address data and using the input address data as the start address.

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The data read from the buffer memory core 430 is provided to the flash memory 314 through the second data input / output buffer 450. The flash memory 314 stores the input data in a designated storage area. In the flash memory, the RB signal is kept active during the write operation to notify the ML control logic unit 462. When the write operation is completed, the RB signal transitions to the non-active state, and in response, the ML control logic unit 462 transitions the WAIT signal to the non-active state, thereby recognizing that the PWM operation is completed in the host 300.

Therefore, in the present invention, data transmission is always possible between the main memory core 420 and the host 300 regardless of the flash memory operation except for the period during which the INT signal is active.

3) Block Read Mode (BRM)

Since one block of the flash memory is composed of tens of pages, for example, 32 pages, when the size of the buffer memory core 430 is a page size, the above-described PRM operation is repeated 32 times. If the buffer memory size is in blocks, this is achieved by changing the page size to the block size in the PRM operation.

4) Block Write Mode (BWM)

Since one block in the flash memory is composed of several tens of pages, for example, 32 pages, when the size of the buffer memory is the page size, the above-described PWM operation is repeated by 32 times. If the buffer memory size is in blocks, this is achieved by changing the page size to the block size in the PwM operation.

Although described with reference to the examples, those skilled in the art can understand that the present invention can be variously modified and changed without departing from the spirit and scope of the invention described in the claims below. There will be.

Although only the representative flash memory operation has been described in the above-described embodiment, other operations may be linked similarly to the existing flash memory operation in a similar manner to the above-described embodiment.

As described above, in the present invention, a high speed operation DRAM interface is provided to the system by providing a control circuit for interfacing a low speed operation nonvolatile memory such as a flash memory to a high speed operation volatile memory such as a DRAM. This can improve system design and ease of operation. In addition, since the memory controller is simplified, the system design is simplified, and the system board can be miniaturized.

Patent Citations (21)

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Family To Family Citations				
US5600801A *	1993-07-15	1997-02-04	Dell Usa, L.P.	Multiple function interface device for option card
JP3789955B2	1994-05-20	2006-06-28	株式会社ルネサステクノロジ	Semiconductor memory device
US5604710A *	1994-05-20	1997-02-18	Mitsubishi Denki Kabushiki Kaisha	Arrangement of power supply and data input/output pads in semiconductor memory device
US5696929A *	1995-10-03	1997-12-09	Intel Corporation	Flash EEPROM main memory in a computer system
JP3188840B2 *	1996-06-14	2001-07-16	インターナショナル・ビジネス・マシーンズ・コーポレーション	Peripheral device used in computer system and control method therefor
JP3092558B2 *	1997-09-16	2000-09-25	日本電気株式会社	Semiconductor integrated circuit device
KR100512159B1	1997-11-25	2006-05-16	삼성전자주식회사	Pad layout for semiconductor memory device
JP4587500B2 *	1998-11-11	2010-11-24	ルネサスエレクトロニクス株式会社	Semiconductor integrated circuit, memory module, storage medium, and semiconductor integrated circuit relief method
JP4141581B2 *	1999-04-05	2008-08-27	株式会社ルネサステクノロジ	Storage device with flash memory
JP3868064B2 *	1999-08-27	2005-07-06	株式会社東芝	Semiconductor memory device
JP3871184B2 *	2000-06-12	2007-01-24	シャープ株式会社	Semiconductor memory device
US6691205B2 *	2001-03-05	2004-02-10	M-Systems Flash Disk Pioneers Ltd.	Method for using RAM buffers with simultaneous accesses in flash based storage systems
JP4049297B2	2001-06-11	2008-02-20	株式会社ルネサステクノロジ	Semiconductor memory device
TWI240864B *	2001-06-13	2005-10-01	Hitachi Ltd	Memory device
US7290080B2 *	2002-06-27	2007-10-30	Nazomi Communications Inc.	Application processors and memory architecture for wireless applications
JP4082913B2 *	2002-02-07	2008-04-30	株式会社ルネサステクノロジ	Memory system
JP2003303129A *	2002-04-02	2003-10-24	Brilliance Semiconductor Inc	Intelligent type multifunctional compound memory

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CN1717662B *	2002-11-26	2010-04-28	株式会社瑞萨科技	Memory module, memory system, and information device
GB2403574B *	2003-07-03	2005-05-11	Micron Technology Inc	Compact decode and multiplexing circuitry for a multi-port memory having a common memory interface
US7315951B2 *	2003-10-27	2008-01-01	Nortel Networks Corporation	High speed non-volatile electronic memory configuration
KR100666169B1 *	2004-12-17	2007-01-09	삼성전자주식회사	Flash memory data storing device

* Cited by examiner, † Cited by third party

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Publication number	Priority date	Publication date	Assignee	Title
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US8250295B2	2004-01-05	2012-08-21	Smart Modular Technologies, Inc.	Multi-rank memory module that emulates a memory module having a different number of ranks
EP1764803A1 *	2005-09-09	2007-03-21	SGS-THOMSON MICROELECTRONICS S.r.l.	Memory architecture with serial peripheral interface
KR100771113B1 *	2005-09-12	2007-10-16	삼성전자주식회사	Semiconductor memory module and semiconductor memory system
KR100737913B1 *	2005-10-04	2007-07-10	삼성전자주식회사	Read method of semiconductor memory device
TWI353124B *	2006-03-30	2011-11-21	Silicon Image Inc	Inter-port communication in a multi-port memory de
KR100764749B1	2006-10-03	2007-10-08	삼성전자주식회사	Multi-chip packaged flash memory device and copy-back method thereof
KR100800484B1 *	2006-11-03	2008-02-04	삼성전자주식회사	Data store system including the buffer for non-volatile memory and the buffer for disk, and data access method of the data store system
US8230154B2 *	2007-01-19	2012-07-24	Spansion Llc	Fully associative banking for memory
US8874831B2 *	2007-06-01	2014-10-28	Netlist, Inc.	Flash-DRAM hybrid memory module
US8301833B1	2007-06-01	2012-10-30	Netlist, Inc.	Non-volatile memory module
US10838646B2	2011-07-28	2020-11-17	Netlist, Inc.	Method and apparatus for presearching stored data
US8904098B2	2007-06-01	2014-12-02	Netlist, Inc.	Redundant backup using non-volatile memory
US10038022B2	2011-07-28	2019-08-13	Netlist, Inc.	Hybrid memory module and system and method of operating the same
US10198350B2	2011-07-28	2019-02-05	Netlist, Inc.	Memory module having volatile and non-volatile memory subsystems and method of operation
JP2009116702A *	2007-11-07	2009-05-28	Toshiba Corp	Semiconductor integrated circuit
KR100929313B1 *	2007-12-31	2009-11-27	주식회사 하이닉스반도체	Semiconductor memory device
US8244937B2 *	2008-09-30	2012-08-14	Micron Technology, Inc.	Solid state storage device controller with parallel operation mode
US8549209B2 *	2008-11-04	2013-10-01	Mosaid Technologies Incorporated	Bridging device having a configurable virtual page size
KR101556016B1	2009-03-20	2015-10-01	삼성전자주식회사	Semiconductor memory device with power saving mode
US8050092B2 *	2009-05-29	2011-11-01	Seagate Technology Llc	NAND flash memory with integrated bit line capacitance
US8149622B2 *	2009-06-30	2012-04-03	Aplus Flash Technology, Inc.	Memory system having NAND-based NOR and NAND flashes and SRAM integrated in one chip for hybrid data, code and cache storage
US8667191B2 *	2010-01-15	2014-03-04	Kingston Technology Corporation	Managing and indentifying multiple memory storage devices
US8631177B1 *	2010-06-24	2014-01-14	Smsc Holdings S.A.R.L.	Multi-port device with controller for storage media device port
US8630418B2 *	2011-01-05	2014-01-14	International Business Machines Corporation	Secure management of keys in a key repository
KR20120086952A *	2011-01-27	2012-08-06	에스케이하이닉스 주식회사	Semiconductor Memory Chip and Multi Chip Package using the same
US8694719B2	2011-06-24	2014-04-08	Sandisk Technologies Inc.	Controller, storage device, and method for power throttling memory operations
US8745369B2	2011-06-24	2014-06-03	SanDisk Technologies, Inc.	Method and memory system for managing power based on semaphores and timers

Petitioners
Ex. 1002, p. 272

US10248328B2	2013-11-07	2019-04-02	Netlist, Inc.	Direct data move between DRAM and storage on a memory module
CN104246732A *	2012-06-28	2014-12-24	慧荣发展公司，有限责任合伙企业	Memory module with a dual-port buffer
KR102020466B1	2012-10-04	2019-09-10	에스케이하이닉스 주식회사	Data storage device including a buffer memory device
US20140189192A1 *	2012-12-28	2014-07-03	Shlomo Raikin	Apparatus and method for a multiple page size translation lookaside buffer (tlb)
US10372551B2	2013-03-15	2019-08-06	Netlist, Inc.	Hybrid memory system with configurable error thresholds and failure analysis capability
US9064562B2	2013-04-03	2015-06-23	Hewlett-Packard Development Company, L.P.	Memory module having multiple memory banks selectively connectable to a local memory controller and an external memory controller
US9436600B2	2013-06-11	2016-09-06	Svic No. 28 New Technology Business Investment L.L.P.	Non-volatile memory storage for multi-channel memory system
US9412294B2 *	2013-08-22	2016-08-09	Boe Technology Group Co., Ltd.	Data transmission device, data transmission method and display device
CN103413516B *	2013-08-22	2016-03-30	京东方科技集团股份有限公司	Data transmission device, data transmission method and display device
WO2016063667A1 *	2014-10-22	2016-04-28	太陽誘電株式会社	Reconfigurable device
CN106155926B *	2015-04-09	2019-11-26	瀚邦科技股份有限公司	The data interactive method of memory and memory
KR101665667B1 *	2015-04-16	2016-10-11	황태래	Nand flash memory type controlling apparatus
US9401184B1	2015-06-16	2016-07-26	Sandisk Technologies Llc	Memory system and method for power management
US9418712B1	2015-06-16	2016-08-16	Sandisk Technologies Llc	Memory system and method for power management using a token bucket
KR20170143070A	2016-06-17	2017-12-29	삼성전자주식회사	Memory device including buffer-memory and memory module including the same
US9760311B1	2016-06-23	2017-09-12	Sandisk Technologies Llc	Storage system and method for adaptive thermal throttling
US10496584B2 *	2017-05-11	2019-12-03	Samsung Electronics Co., Ltd.	Memory system for supporting internal DQ termination of data buffer
US10719248B2	2018-04-20	2020-07-21	Micron Technology, Inc.	Apparatuses and methods for counter update operations
US20200278940A1 *	2019-03-01	2020-09-03	Micron Technology, Inc.	Command bus in memory

* Cited by examiner, † Cited by third party, ‡ Family to family citation

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US10725956B2	2020-07-28	Memory device for a hierarchical memory architecture
US9836227B2	2017-12-05	Method and system for accessing a flash memory device
US8463993B2	2013-06-11	Translating memory modules for main memory
US8060708B2	2011-11-15	Multiprocessor system having an input/output (I/O) bridge circuit for transferring data between volatile and non-volatile memory
US8595445B2	2013-11-26	Non-volatile memory and method with host controlled caching
US8437190B2	2013-05-07	Interleaved flash storage system and method
US7447805B2	2008-11-04	Buffer chip and method for controlling one or more memory arrangements
US9159438B2	2015-10-13	NAND flash memory having C/A pin and flash memory system including the same
US7149824B2	2006-12-12	Dynamically setting burst length of memory device by applying signal to at least one external pin during a read or write transaction
JP4524194B2	2010-08-11	Simultaneous refresh mode with distributed row address counter in embedded DRAM
US6647478B2	2003-11-11	Semiconductor memory device
TWI420302B	2013-12-21	Method, system, and computing device for hybird memory device with single interface, and computer readable medium for recording related instructions thereon
KR101507194B1	2015-03-30	Serial interface nand
US9304691B2	2016-04-05	Memory system and bank interleaving method

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TWI446356B	2014-07-21	Memory with output control and system thereof
KR100589556B1	2006-08-30	System signalling schemes for processor & memory module
US7764551B2	2010-07-27	Semiconductor memory system having volatile memory and non-volatile memory that share bus, and method of controlling operation of non-volatile memory
KR100780861B1	2007-11-29	Flash memory device and flash memory system including buffer memory
US6556504B2	2003-04-29	Nonvolatile semiconductor memory device and data input/output control method thereof
US7409473B2	2008-08-05	Off-chip data relocation
US6963502B2	2005-11-08	Apparatus for dividing bank in flash memory
US7567471B2	2009-07-28	High speed fanned out system architecture and input/output circuits for non-volatile memory
CN100392760C	2008-06-04	Semiconductor storage device
EP1497733B1	2011-06-15	Destructive-read random access memory system buffered with destructive-read memory cache
US5864505A	1999-01-26	Random access memory with plural simultaneously operable banks

Priority And Related Applications

Priority Applications (2)

Application	Priority date	Filing date	Title
KR20040006340		2004-01-30	
KR1020040006340		2004-01-30	

Legal Events

Date	Code	Title	Description
2005-01-24	A201	Request for examination	
2006-04-14	E902	Notification of reason for refusal	
2006-07-19	E701	Decision to grant or registration of patent right	
2006-07-21	GRNT	Written decision to grant	
2013-07-01	FPAY	Annual fee payment	**Payment date**: 20130701 **Year of fee payment**: 8
2014-06-27	FPAY	Annual fee payment	**Payment date**: 20140630 **Year of fee payment**: 9
2015-06-29	FPAY	Annual fee payment	**Payment date**: 20150630 **Year of fee payment**: 10
2016-06-29	FPAY	Annual fee payment	**Payment date**: 20160630 **Year of fee payment**: 11
2017-06-29	FPAY	Annual fee payment	**Payment date**: 20170630 **Year of fee payment**: 12
2018-06-28	FPAY	Annual fee payment	**Payment date**: 20180629 **Year of fee payment**: 13

Concepts

machine-extracted

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Name	Image	Sections	Count	Query match

Petitioners
Ex. 1002, p. 274

semiconductors	title,description	9	0.000
buffering	title,description	4	0.000
buffers	claims,description	64	0.000
response	claims,description	23	0.000
controlling effects	claims,description	4	0.000

Show all concepts from the description section

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Petitioners
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Electronic Acknowledgement Receipt	
EFS ID:	42152924
Application Number:	17138766
International Application Number:	
Confirmation Number:	8804
Title of Invention:	FLASH-DRAM HYBRID MEMORY MODULE
First Named Inventor/Applicant Name:	Hyun Lee
Customer Number:	151145
Filer:	Khaled Shami/Stephanie Semler
Filer Authorized By:	Khaled Shami
Attorney Docket Number:	0016.001000H
Receipt Date:	11-MAR-2021
Filing Date:	30-DEC-2020
Time Stamp:	19:29:22
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Non Patent Literature	IDS3_NPL3_Ex_Stanfords_Materials_Science_department_website_PTAB_IPR2017_00692_2011.pdf	1098382 dd0a1972017d81f2b4f992fb9f259aa0eda73e1e	no	2

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2	Non Patent Literature	IDS3_NPL6_Ex_MS_Computer_Dictionary.pdf	1551595 a3e376f0fe699011d8aa8ffbae8c8533fc2800ae	no	9
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3	Non Patent Literature	IDS3_NPL33_ORDER_Grantyng_Joint_Stipulation_NDCA_413cv05889_382.pdf	148436 da03d36fe274c555bb1b6d1efc8dc567c55208a3	no	2
Warnings:					
Information:					
4	Non Patent Literature	IDS3_NPL34_Patent_Owners_Demonstratives_PTAB_IPR2017_00587_2023.pdf	5671795 ba9f78805e610dd0401ea2f95b054110dbb3bc33	no	57
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5	Non Patent Literature	IDS3_NPL35_Patent_Owners_Listing_ofNew_Argumentsand_PTAB_IPR2017_00587_23.pdf	111913 67a4431aa8547bd775160061d7a844eb95bb618d	no	6
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7	Non Patent Literature	IDS3_NPL37_Patent_Owners_Preliminary_Response_PTAB_IPR2014_01371_10.pdf	1468755 212cb60a34ee7a642f08a25c7284cefef72e85cd	no	66
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8	Non Patent Literature	IDS3_NPL38_Patent_Owners_Preliminary_Response_PTAB_IPR2014_00994_7.pdf	1220159 44306458268fea599d3362b19a25fbea4a51fb04	no	60
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Warnings:					
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11	Non Patent Literature	IDS3_NPL41_PATENT_OWNERS_PRELIMINARY_RESPONSE_PTAB_IPR2017_00692_6.pdf	715159 4b1ff7d1f9e36526b779ee9a22c3b8748fa42d0d	no	48
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Information:					
13	Non Patent Literature	IDS3_NPL43_Patent_Owners_Response_PTAB_IPR2017_00587_12.pdf	1625403 3445bf06e4fdbdb2b7ef36b6d82a6aa23f38fefe	no	80
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14	Non Patent Literature	IDS3_NPL44_PATENT_OWNERS_RESPONSE_PTAB_IPR2017_00092_12.pdf	1227588 db77a4df1434a9760f4ed37bffa8133cb324a5d5	no	77
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Warnings:					
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17	Non Patent Literature	IDS4_NPL8_Petition_for_Inter_Partes_Review_ofPat8671243_PTAB_IPR2017_00587_1.pdf	1245700 5ffe72934f18a03aca6fdfba6c51b92f7ad6b27b	no	82
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18	Non Patent Literature	IDS4_NPL9_PETITION_FOR_INTER_PARTES_REVIEW_PAT8301833_PTAB_IPR2014_00994.pdf	749563 66899a3a9405ccc792e78ed10da126a087f1b5e9	no	69
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19	Non Patent Literature	IDS4_NPL12_Petitioners_Demonstratives_PTAB_IPR2017_00587_1037.pdf	15554459 72a5a4810671fc80c9e07759f81e6ac10ec818be	no	89
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20	Non Patent Literature	IDS4_NPL14_Petitioners_Reply_to_Patent_Owners_Response_PTAB_IPR2017_00587_16.pdf	551197 511019149f573a794576589cd87cb34972308646	no	38
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26	Non Patent Literature	IDS4_NPL28_SECOND_AMENDED_ANSWER_AND_COUNTERCLAIMS_NDCA413cv03901_73.pdf	542838 e6dfa717cd45d2abbf4cdd109a3fea6fb710a6b8	no	21
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27	Non Patent Literature	IDS4_NPL30_SUPPLEMENTAL_DECLARATION_OF_DANIEL_E_ALBERTI.pdf	117001 ae8d4a80bc49a63c425124fbba35af3bb4320f16	no	3
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28	Non Patent Literature	IDS4_NPL31_SUPPLEMENTAL_DECLARATION_OF_RONALD_H_SPUHLER_Case413cv05889YGRDocument305-1.pdf	43325 4b866d6a8cc3855e50cd1c7ae05981c811ef2922	no	2
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32	Non Patent Literature	IDS2_NPL45_JEDEC_2014_IPR2014_01371.pdf	395570 140b178c2453fedb0d5535aac380c533ed9c35bb	no	1
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34	Non Patent Literature	IDS3_NPL2_JOINT_STATUS_REPORT_REGARDING_INTER_PARTES_REVIEW_NDCAcase413cv05889_358.pdf	109087 7d14b8387d0ee03dedc9da1da0828c3eeecd1712	no	4
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If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

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PTO/SB/06 (09-11)
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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 17/138,766	Filing Date 12/30/2020	☐ To be Mailed

ENTITY: ☑ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA		RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A		N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A		N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A		N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*		x $100 =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*		x $480 =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).				
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))					
* If the difference in column 1 is less than zero, enter "0" in column 2.				TOTAL	

APPLICATION AS AMENDED - PART II

AMENDMENT	03/11/2021	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 30	Minus	** 30	= 0		x $100 =	0
	Independent (37 CFR 1.16(h))	* 3	Minus	*** 3	= 0		x $480 =	0
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	0

AMENDMENT		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=		x $0 =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=		x $0 =	
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.	LIE
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".	/CRYSTAL QUEEN/
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".	
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.	

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

151145 7590 03/24/2021

Shami Messinger PLLC
1000 Wisconsin Ave. NW
Suite 200
Washington, DC 20007

EXAMINER	
FARROKH, HASHEM	
ART UNIT	PAPER NUMBER
2135	

DATE MAILED: 03/24/2021

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/138,766	12/30/2020	Hyun Lee	0016.001000H	8804

TITLE OF INVENTION: FLASH-DRAM HYBRID MEMORY MODULE

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1200	$0.00	$0.00	$1200	06/24/2021

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Maintenance fees are due in utility patents issuing on applications filed on or after Dec. 12, 1980. It is patentee's responsibility to ensure timely payment of maintenance fees when due. More information is available at www.uspto.gov/PatentMaintenanceFees.

Petitioners
Ex. 1002, p. 284

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), by mail or fax, or via EFS-Web.

By mail, send to: Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

By fax, send to: (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

151145 7590 03/24/2021
Shami Messinger PLLC
1000 Wisconsin Ave. NW
Suite 200
Washington, DC 20007

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being transmitted to the USPTO via EFS-Web or by facsimile to (571) 273-2885, on the date below.

(Typed or printed name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/138,766	12/30/2020	Hyun Lee	0016.001000H	8804

TITLE OF INVENTION: FLASH-DRAM HYBRID MEMORY MODULE

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1200	$0.00	$0.00	$1200	06/24/2021

EXAMINER	ART UNIT	CLASS-SUBCLASS
FARROKH, HASHEM	2135	710-308000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-09 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document must have been previously recorded, or filed for recordation, as set forth in 37 CFR 3.11 and 37 CFR 3.81(a). Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. Fees submitted: ❑ Issue Fee ❑ Publication Fee (if required) ❑ Advance Order - # of Copies _____

4b. Method of Payment: *(Please first reapply any previously paid fee shown above)*

❑ Electronic Payment via EFS-Web ❑ Enclosed check ❑ Non-electronic payment by credit card (Attach form PTO-2038)

❑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment to Deposit Account No. _____

5. **Change in Entity Status** (from status indicated above)

❑ Applicant certifying micro entity status. See 37 CFR 1.29

❑ Applicant asserting small entity status. See 37 CFR 1.27

❑ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

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Ex. 1002, p. 285

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/138,766	12/30/2020	Hyun Lee	0016.001000H	8804

151145 7590 03/24/2021

Shami Messinger PLLC
1000 Wisconsin Ave. NW
Suite 200
Washington, DC 20007

EXAMINER	
FARROKH, HASHEM	
ART UNIT	**PAPER NUMBER**
2135	

DATE MAILED: 03/24/2021

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

PTOL-85 (Rev. 02/11)

Petitioners
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OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 30 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 17/138,766	Applicant(s) Lee et al.	
	Examiner HASHEM FARROKH	Art Unit 2135	AIA (FITF) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☑ This communication is responsive to 03/11/2021.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

3. ☑ The allowed claim(s) is/are 1-30 . As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see **http://www.uspto.gov/patents/init_events/pph/index.jsp** or send an inquiry to **PPHfeedback@uspto.gov.**

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☐ All b) ☐ Some *c) ☐ None of the:

   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____ .

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____ .

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☑ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date 03/11/2021.
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material _____.
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date. _____.
5. ☐ Examiner's Amendment/Comment
6. ☑ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/HASHEM FARROKH/
Primary Examiner, Art Unit 2135

Petitioners
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Notice of Pre-AIA or AIA Status

The present application is being examined under the pre-AIA first to invent provisions.

INFORMATION CONCERNING IDS:

The information disclosure statements (IDS') submitted on 03/11/2021 are in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statements have been considered by the examiner. However, a copy foreign priority patents listed as KR100606242 and WO2013016723 have not been provided. Therefore, these foreign priority patent documents have not been considered. Furthermore, NPL documents shown by lined-through have not been considered by the Examiner because a copy of the line-through documents have not been provide or they are not readily identifiable from title of documents listed.

PART I ***THE EXAMINER'S EVALUATION OF THE APPLICATION***

SECTION A ***RELEVANT ART CITED BY THE EXAMINER***

1. *Chen et at. (US 20120271990 A1).*
2. *Bates (US 20070136523 A1).*
3. *Prete et al. (US 20080126624 A1).*

SECTION B ***DISTINGUISHING FEATURES RECITED IN THE CLAIMS***

The following is an ***Examiner's Statement of Reasons for Allowance*** *See* ***MPEP 1302.14***

4. The primary reasons for allowance of claims 1-15 in the instant application is the combination with the inclusion of the following limitations: **"a first buck converter configured to provide a first regulated voltage having a first voltage amplitude; a second buck converter configured to provide a second regulated voltage having a second voltage amplitude; a third buck converter configured to provide a third regulated voltage having a third voltage amplitude; a converter circuit configured to provide a fourth regulated voltage having a fourth voltage amplitude a plurality of synchronous dynamic random access memory (SDRAM) devices coupled to the first regulated voltage, and at least one circuit coupled between a first portion of the plurality of edge connections and the plurality of SDRAM devices, the at least one circuit operable to (i) receive a first plurality of address and control signals via the first portion of the plurality of edge connections, and (ii) output a second plurality of address and control signals to the plurality of SDRAM devices, the at least one circuit coupled to both the second regulated voltage and the fourth regulated voltage, wherein a first one of the second and fourth voltage amplitudes is less than the a second one of the second and fourth voltage amplitudes."**

5. The primary reasons for allowance of claims 16-20 in the instant application is the combination with the inclusion of the following limitations: **"first, second, and third buck converters configured to receive a pre-regulated input voltage and to produce first, second and third regulated voltages, respectively; a plurality of components coupled to the PCB, the plurality of components including a plurality of synchronous dynamic random access memory (SDRAM) devices,**

each component of the plurality of components coupled to one or more regulated voltages of the first, second, third and fourth regulated voltages; and a voltage monitor circuit configured to monitor an input voltage received via a first portion of the plurality of edge connections, the voltage monitor circuit configured to produce a signal in response to the input voltage having a voltage amplitude that is greater than a first threshold voltage"

6. The primary reasons for allowance of claims 23-30 in the instant application is the combination with the inclusion of the following limitations: **"a plurality of components coupled to the PCB, each component of the plurality of components coupled to one or more regulated voltages of first, second, third and fourth regulated voltages, the plurality of components including a plurality of synchronous dynamic random access memory (SDRAM) devices and one or more registers, the plurality of SDRAM devices coupled to the first regulated voltage, the one or more registers coupled to (i) the second regulated voltage, (is) a portion of the plurality of edge connections, and (iii) the plurality of SDRAM devices, wherein a plurality of address and control signals are coupled to the one or more registers via the portion of the plurality of edge connections; first, second, and third buck converters configured to provide the first, second and third regulated voltages, respectively"**

The prior art of record including the disclosures of Chen et at. (US 20120271990 A1), Bates (US 20070136523 A1), and Prete et al. (US 20080126624 A1) neither anticipates nor renders obvious the above-recited combination.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays should be clearly labeled "Comments on Statement of Reasons for Allowance"

PART II **THE ATTENTION OF FUTURE CORRESPONDENT**

Any inquiry concerning this communication or earlier communications from the examiner should be directed to HASHEM FARROKH whose telephone number is (571)272-4193. The examiner can normally be reached on 8:30 am - 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mr. Sanjiv Shah can be reached on (571)272-4098. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. For questions regarding access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO

Customer Service Representative or access to the automated information system, call

800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/HASHEM FARROKH/
Primary Examiner, Art Unit 2135

March 17, 2021

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/138,766	Lee et al.
	Examiner	Art Unit
	HASHEM FARROKH	2135

CPC - Searched*		
Symbol	**Date**	**Examiner**
G06F13/28; G06F13/4027; G06F13/1694; G06F13/4223; G06F12/0638; G06F12/0246; G06F1/185; G06F3/0613; G06F3/0685 OR G06F3/0659; G06F2212/7208; G06F2212/205; G11C7/1072; G11C14/0018	02/24/2021	HF
G06F3/0659; G06F12/0246; G06F2212/7208; G06F13/4027; G06F13/28; G06F3/0613; G06F2212/205; G06F3/0685; G11C7/1072	03/17/2021	HF

CPC Combination Sets - Searched*		
Symbol	**Date**	**Examiner**

US Classification - Searched*			
Class	**Subclass**	**Date**	**Examiner**
711	103	02/25/2021	HF
711	104	02/25/2021	HF
711	105	02/25/2021	HF
710	138	03/17/2021	HF

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

/HASHEM FARROKH/ Primary Examiner, Art Unit 2135	

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Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/138,766	Lee et al.
	Examiner	Art Unit
	HASHEM FARROKH	2135

Search Notes		
Search Notes	**Date**	**Examiner**
Assignee/Inventor Search	02/25/2021	HF
EAST Text Search	02/24/2021	HF
IP Search	02/25/2021	HF
Google Search	02/25/2021	HF
Assignee/Inventor Search Updated	03/17/2021	03/17/202
Assignee/Inventor Search Updated	03/17/2021	03/17/202

Interference Search			
US Class/CPC Symbol	**US Subclass/CPC Group**	**Date**	**Examiner**
G06F3/0685	G06F3/00	03/17/202	03/17/202
G06F12/0246	G06F12/00	03/17/202	03/17/202
G06F2212/205	G06F2212/00	03/17/202	03/17/202

/HASHEM FARROKH/ Primary Examiner, Art Unit 2135	

Petitioners
Ex. 1002, p. 295

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/138,766	Lee et al.
	Examiner	**Art Unit**
	HASHEM FARROKH	2135

CPC									
Symbol								**Type**	**Version**
G06F	/	13	/	28				F	2013-01-01
G06F	/	12	/	0246				I	2013-01-01
G06F	/	13	/	1694				I	2013-01-01
G06F	/	1	/	185				I	2013-01-01
G06F	/	12	/	0638				I	2013-01-01
G06F	/	13	/	4243				I	2013-01-01
G11C	/	7	/	1072				I	2013-01-01
G11C	/	14	/	0018				I	2013-01-01
G06F	/	3	/	0613				I	2013-01-01
G06F	/	3	/	0659				I	2013-01-01
G06F	/	3	/	0685				I	2013-01-01
G06F	/	13	/	4027				I	2013-01-01
G06F	/	2212	/	205				A	2013-01-01
G06F	/	2212	/	7208				A	2013-01-01

CPC Combination Sets									
Symbol								**Type**	**Set**	**Ranking**	**Version**
	/		/								

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	30	
/HASHEM FARROKH/ Primary Examiner, Art Unit 2135	18 March 2021	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	12

U.S. Patent and Trademark Office — Part of Paper No.: 20210317

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/138,766	Lee et al.
	Examiner	**Art Unit**
	HASHEM FARROKH	2135

INTERNATIONAL CLASSIFICATION					
CLAIMED					
G06F	/	13	/	36	

NON-CLAIMED					
	/		/		

US ORIGINAL CLASSIFICATION	
CLASS	**SUBCLASS**
710	308

CROSS REFERENCES(S)						
CLASS	**SUBCLASS (ONE SUBCLASS PER BLOCK)**					

NONE		**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	30	
/HASHEM FARROKH/ Primary Examiner, Art Unit 2135	18 March 2021	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	12

U.S. Patent and Trademark Office — Part of Paper No.: 20210317

Petitioners
Ex. 1002, p. 297

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/138,766	Lee et al.
	Examiner	**Art Unit**
	HASHEM FARROKH	2135

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIMS

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	1	9	10	19	19	26	28								
2	2	7	11	20	20	29	29								
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6	7	16	16	27	25										
14	8	17	17	28	26										
8	9	18	18	25	27										

NONE		**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	30	
/HASHEM FARROKH/ Primary Examiner, Art Unit 2135	18 March 2021	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	12

Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (02-18)
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**		
	Application Number	17138766
	Filing Date	2020-12-30
	First Named Inventor	Hyun Lee
	Art Unit	1731 2135
	Examiner Name	Hashem Farrokh
	Attorney Docket Number	0016.001000H

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Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	17138766
	Filing Date	2020-12-30
	First Named Inventor	Hyun Lee
	Art Unit	1731
	Examiner Name	
	Attorney Docket Number	0016.001000H

	1	Elmhurst et al., "A 1.8-V 128-Mb 125-MHz Multilevel Cell Flash Memory With Flexible Read While Write", IEEE Journal of Solid-State Circuits 38(11):1929-1933 (2003).
	2	Elmhurst, D. et al., A 1.8-V 128-Mb 125-MHz Multilevel Cell Flash Memory With Flexible Read While Write, IEEE Journal of Solid-State Circuits, Vol. 38, No. 11, Nov. 2003, 5 pages.
	3	Ex. 1004—IPR2017-00587 Ron Mattel CV, 7 pages.
	4	Exhibit 1: Claim Chart Comparing Netlist's US Patent No. 8,001,434 to Smart Storage Ulltradimm, Case4:13-cv-05889-YGR Document 193-1, filed Apr. 10, 2014, 21 pages.
	5	Exhibit, Application As Filed, SanDisk Corporation v. Netlist, Inc., Patent 8,301,833, IPR2014-00994 (PTAB), 52 pages.
	6	Exhibit, Decision Denying Institution of Inter Partes Review, Smart Modular Technologies, Inc. v. Netlist, Inc., Case No. 4:13-cv-05889-YGR Document 309-3, filed March 17, 2015, 23 pages.
	7	Exhibit, Decision Denying Institution of Inter Partes Review, Smart Modular Technologies, Inc. v. Netlist, Inc., Case No. 4:13-cv-05889-YGR Document 309-4, filed March 17, 2015, 20 pages.
	8	Exhibit, Decision Denying Institution of Inter Partes Review, Smart Modular Technologies, Inc. v. Netlist, Inc., Case No. 4:13-cv-05889-YGR Document 309-5, filed March 17, 2015, 28 pages.
	9	Exhibit, Decision Denying Institution of Inter Partes Review, Smart Modular Technologies, Inc. v. Netlist, Inc., Case No. 4:13-cv-05889-YGR Document 309-9, filed March 17, 2015,17 pages.
	10	Exhibit, Decision Denying Institution of Inter Partes Review, Smart Modular Technologies, Inc. v. Netlist, Inc., Case No. 4:13-cv-05889-YGR Document 309-7, filed March 17, 2015, 17 pages.
	11	Exhibit, Email from Defendant's Counsel, Netlist v. Smart Storage Systems, Inc. et. al., Case 4:13-cv-05889-YGR Document 305-17, filed March 10, 2015, 6 pages.

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	First Named Inventor	Hyun Lee
	Art Unit	1731
	Examiner Name	
	Attorney Docket Number	0016.001000H

	12	Exhibit, Institution of Inter Partes Review, Sandisk Corporation v. Netlist, Inc., Case 4:13-cv-05889-YGR Document 316-9, filed March 24, 2015, 29 pages.	
	13	Exhibit, Institution of Inter Partes Review, Smart Modular Technologies, Inc. v. Netlist, Inc., Case 4:13-cv-05889-YGR Document 309-1, filed March 17, 2015, 22 pages.	
	14	JEDEC Standard, Double Data Rate (DDR) SDRAM Specification, JESD79, Jun. 2000, 77 pages.	
	15	Exhibit, Institution of Inter Partes Review, Smart Modular Technologies, Inc. v. Netlist, Inc., Case No. 4:13-cv-05889-YGR Document 309-2, filed March 17, 2015, 23 pages.	
	16	Exhibit, Letter from Defendant's Counsel, Netlist v. Smart Storage Systems, Inc. et. al., Case 4:13-cv-05889-YGR Document 305-16, filed March 10, 2015, 3 pages.	
	17	Exhibit, Letter sent via email on December 6, 2013, Case 4:13-cv-03901-YGR Document 53-2, filed January 6, 2014	
	18	Exhibit, Order Denying Defendant's Motion to Stay Pending Inter Partes Review (Doc.59), The Procter and Gamble Company v. Team Technologies, Inc, et al., Case 4:13-cv-05889-YGR Document 316-6, filed March 24, 2015, 10 pages.	
	19	Exhibit, Patent Public Advisory Committee Quarterly Meeting, Appeals Statistics USPTO, Case No. 4:13-cv-05889-YGR Document 309-8, filed March 17, 2015, 23 pages.	
	20	Exhibit, Reporter's Transcript of Proceedings, Netlist, Inc v. Smart Modular Technologies, Inc., et al., Case 4:13-cv-05889-YGR Document 316-3, filed March 24, 2015, 15 pages.	
	21	Exhibit, Transcript of Official Electronic Sound Recording Proceeding, Netlist v. Smart Modular Technologies, Inc, et al., Case 4:13-cv-05889-YGR Document 305-7, filed March 10, 2015, 10 pages.	
	22	Extended European Search Report for European Application No. 12 817 751.6, dated Jun. 9, 2015.	

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	Filing Date	2020-12-30
	First Named Inventor	Hyun Lee
	Art Unit	1731
	Examiner Name	
	Attorney Docket Number	0016.001000H

	23	File History for U.S. Appl. No. 12/240,916, filed Sep. 29, 2008, 320 pages.	
	24	File History for U.S. Appl. No. 13/905,048, filed May 29, 2013, 181 pages.	
	25	File History for U.S. Appl. No. 60/941,586, filed Jun. 1, 2007, 23 pages.	
	26	File History U.S. Pat. No. 8,671,243.	
	27	Final Office Action, dated Jun. 15, 2016, issued in U.S. Appl. No. 14/489,281, 10 pages.	
	28	Final Office Action, SanDisk Corporation v. Netlist, Inc., Patent 8,301,833, IPR2014-0099-1007 (PTAB), dated February 1, 2012, 13 pages	
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	30	Final Written Decision, Patent 8,874,831, IPR2017-00692, Paper No. 25, entered July 5, 2018, 42 pages.	
	31	Final Written Decision, US Patent No. 7,881,150, Case No. Case IPR2014-00882, (PTAB), Paper 33, filed December 14, 2015, 51 pages.	
	32	First Amended Complaint for Patent Infringement, Netlist Inc. v Smart Modular Tech. Inc., et al., Case 8:13-cv-00996-DOC-JPR, Document 5, filed Aug. 23, 2013, 99 pages.	
	33	Hasan, J. et al. Efficient Use of Memory Bandwidth to Improve Network Processor Throughput, Proceedings of the 30th Annual International Symposium on Computer Architecture (ISCA'03), IEEE, 2003, 12 pages.	

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	Art Unit	1731
	Examiner Name	
	Attorney Docket Number	0016.001000H

	34	Horowitz, P. et al., "The Art of Electronics", Cambridge University Press 2nd Ed. 1989, pp. 471495-496.	
	35	Innis, J., "MPC8560 PowerQUICC III Compact Flash Interface Design", Freescale Semiconductor, Inc., 2004-2006, pp. 1-23.	
	36	Intel 1.8 Volt Intel StrataFlash Wireless Memory (L18), 2003, 100 pages.	
	37	Inter Partes Review No. IPR2017-00692 (PTAB), Patent No. 8,874,831, filed July 26, 2012, 78 pages.	
	38	Inter Partes Review of U.S. Patent No. 8,874,831, Case IPR2017-00692 (PTAB), filed July 26, 2012, Paper No. 1, 78 pages.	
	39	International Preliminary Report on Patentabillity in PCT/US12/48750, mailed Apr. 3, 2014pp. 1-8.	
	40	International Search Report and Written Opinion in PCT/US12/48750, dated Oct. 10, 2012pp. 1-10.	
	41	ISSCC 2006 / SESSION 7 / NON-VOLATILE MEMORY / 7.7, IEEE International Solid-State Circuits Conference, 2006, 10 pages.	
	42	Jacob, B., "Memory Systems Cache, DRAM, Disk", Morgan Kaufman Publishers, Burlington, MA, 2008, Preface and Ch. 7 pp. 315-322, 58 pages.	
	43	Jandhyala, S. et al., "Design-For-Test Analysis of a Buffered SDRAM DIMM", Semiconductor Group, Texas Instruments, Proceedings of International Workshop in Memory Technology, Design and Testing, Singapore, August 13014, 1996,15 pages.	
	44	JEDEC Definition of DIMM, Exhibit 1029, IPR No. 2017-00587, December 18, 2017, 2 pages.	

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	First Named Inventor	Hyun Lee
	Art Unit	1731
	Examiner Name	
	Attorney Docket Number	0016.001000H

	45	JEDEC Global Standard for the Microelectronics Industry, Why JEDEC Standards Matter, 2014, 1 page.	
	46	~~JEDEC Standard 21-C"Configurations for Solid State Memories," pp. 4.5.5-1 to 4.5.5-18~~	
	47	JEDEC Standard No. 21-C (Release 17), Annex J: Serial Presence Detects for DDR2 SDRAM (Revision 1.3), 60 pages.	
	48	~~JEDEC Standard, "Configurations for Solid State Memories", JEDEC Standard 21-C, Release 9, Aug. 1999, 114 pages.~~	
	49	~~JEDEC Standard, DDR2 SDRAM Specification, JESD79-2B (Revision of JESD79-2A) Jan. 2005, 113 pages.~~	

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EXAMINER SIGNATURE

Examiner Signature	/HASHEM FARROKH/	Date Considered	03/15/2021

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /H.F/

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	Application Number	17138766
	Filing Date	2020-12-30
	First Named Inventor	Hyun Lee
	Art Unit	1731
	Examiner Name	
	Attorney Docket Number	0016.001000H

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

See attached certification statement.

☒ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Khaled Shami/	Date (YYYY-MM-DD)	2021-03-11
Name/Print	Khaled Shami	Registration Number	38745

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

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7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

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9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /H.F/

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S381	656	("4420821" "4449205" "4607332" "4658204" "17138766" "4882709" "4884242" "4965828" "20020053944" "20020083368" "20020199061" "20030028733" "20030076726" "20030137881" "20030147297" "20030158995" "20030204776" "20030206478" "20030210601" "20040088508" "20040163027" "20040190210" "20050044302" "20050060488" "20050132250" "20050141273" "20050144418" "20050183472" "20050204091" "20050249011" "20050273548" "20060039197" "20060069896" "20060080515" "20060126369" "20060212651" "20060294295" "20070070669" "20070147115" "20070192627" "20070255898" "20070276995" "20070288683" "20080104344" "20080126690" "20080147968" "20080189479" "20080195806" "20080235443" "20080291727" "20090031099" "20090235038" "20100110748" "20100122200" "20100274953" "20100322020" "20110078496" "20110161569" "20110320804" "20120110417" "20120117402" "20120204079" "20120265952" "20120271990" "20120317433" "20130019076" "20130086309" "20130254456" "20130254497" "20140032820" "20140059170" "20140156919" "20140156920" "20150058701" "2043099" "2737383" "8001434" "9043677" "8081536" "886955" "8102614" "9158684" "8214616" "8233303" "8301833" "9361250" "8407395" "8412879" "8516187" "3562555" "8671243" "8677060" "8874831" "8880791" "8904098" "8904099" "3916390" "5023421" "5026465" "5065092" "5112310" "5145068" "5158015" "5199142" "5216247" "5269382"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/03/15 14:25

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S384	129,386	(G06F13/28 OR G06F13/4027 OR G06F13/1694 OR G06F13/4223 OR G06F12/0638 OR G06F12/0246 OR G06F1/185 OR G06F3/0613 OR G06F3/0685 OR G06F3/0659 OR G06F2212/7208 OR G06F2212/205 OR G11C7/1072 OR G11C14/0018).cpc. OR 711/100.CCLS OR G06F3/06.icpr	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/03/17 11:32
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			DERWENT; IBM_TDB			
S386	458	S385 and (voltage near2 (converter or regulat$3))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/03/17 11:36
S387	425	S386 AND ((G06F3/0659 OR G06F12/0246 OR G06F2212/7208 OR G06F13/4027 OR G06F13/28 OR G06F3/0613 OR G06F2212/205 OR G06F3/0685 OR G11C7/1072).CPC. OR (710/308).CCLS. OR (G06F3/06).IPCR.)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/03/17 12:05
S388	286	S387 and ((voltage or buch) near5 (converter or regulator))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/03/17 12:07
S389	152	((transfer$3 or cop$4 or transmi$5 or retriev$3 or read$3) near5 DRAM near5 (flash or non$1volatile)).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/03/17 12:09
S390	1,329	Lee-Hyun.in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/03/17 12:09
S391	76	Chen-Chi-She.in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/03/17 12:09
S392	72	Solomon-Jeffrey-C.in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO;	OR	ON	2021/03/17 12:09

			DERWENT; IBM_TDB			
S393	33	Milton-Scott-H.in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/03/17 12:09
S394	36	Bhakta-Jayesh.in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/03/17 12:09
S395	0	S389 and (S390 or S391 or S392 or S393 or S394)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/03/17 12:09
S396	37	((transfer$3 or cop$4 or transmi$5 or retriev$3 or read$3) near5 ?DRAM near5 (flash or non$1volatile)).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/03/17 12:10
S397	0	S396 and (S390 or S391 or S392 or S393 or S394)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/03/17 12:11
S398	11,657	(transfer$4 or cop$4 or transmi$5 or mov$3) with data with (non$1volatile or flash or SSD or NVM) with (volatile or ?RAM or ?DRAM memory).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/03/17 12:11
S399	216	NETLIST.as.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO;	OR	ON	2021/03/17 12:11

			DERWENT; IBM_TDB			
S400	21	S398 and S399	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/03/17 12:11
S401	0	S400 and buch	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/03/17 12:13
S402	129,442	(G06F13/28 OR G06F13/4027 OR G06F13/1694 OR G06F13/4223 OR G06F12/0638 OR G06F12/0246 OR G06F1/185 OR G06F3/0613 OR G06F3/0685 OR G06F3/0659 OR G06F2212/7208 OR G06F2212/205 OR G11C7/1072 OR G11C14/0018).cpc. OR 711/100.CCLS OR G06F3/06.icpr	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/03/18 11:44
S403	10,893	S402 and (((synchronous adj dynamic adj random adj access adj memor$3) or SDRAM))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/03/18 11:44
S404	459	S403 and (voltage near2 (converter or regulat$3))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/03/18 11:44
S405	290,180	(G06F13/28 OR G06F13/4027 OR G06F13/1694 OR G06F13/4223 OR G06F12/0638 OR G06F12/0246 OR G06F1/185 OR G06F3/0613 OR G06F3/0685 OR G06F3/0659 OR G06F2212/7208 OR G06F2212/205 OR G11C7/1072 OR G11C14/0018).cpc. OR 711/100.CCLS OR (G06F3/06 OR G06F13/36)".icpr"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/03/18 11:48
S406	427	S404 AND ((G06F3/0659 OR G06F12/0246 OR G06F2212/7208 OR	US-PGPUB; USPAT;	OR	ON	2021/03/18 11:49

		G06F13/4027 OR G06F13/28 OR G06F3/0613 OR G06F2212/205 OR G06F3/0685 OR G11C7/1072).CPC. OR (710/308).CCLS. OR (G06F3/06 OR G06F13/36).IPCR.)	USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			
S407	656	("4420821" "4449205" "4607332" "4658204" "17138766" "4882709" "4884242" "4965828" "20020053944" "20020083368" "20020199061" "20030028733" "20030076726" "20030137881" "20030147297" "20030158995" "20030204776" "20030206478" "20030210601" "20040088508" "20040163027" "20040190210" "20050044302" "20050060488" "20050132250" "20050141273" "20050144418" "20050183472" "20050204091" "20050249011" "20050273548" "20060039197" "20060069896" "20060080515" "20060126369" "20060212651" "20060294295" "20070070669" "20070147115" "20070192627" "20070255898" "20070276995" "20070288683" "20080104344" "20080126690" "20080147968" "20080189479" "20080195806" "20080235443" "20080291727" "20090031099" "20090235038" "20100110748" "20100122200" "20100274953" "20100322020" "20110078496" "20110161569" "20110320804" "20120110417" "20120117402" "20120204079" "20120265952" "20120271990" "20120317433" "20130019076" "20130086309" "20130254456" "20130254497" "20140032820" "20140059170" "20140156919" "20140156920" "20150058701" "2043099" "2737383" "8001434" "9043677" "8081536" "886955" "8102614" "9158684" "8214616" "8233303" "8301833" "9361250" "8407395" "8412879" "8516187" "3562555" "8671243" "8677060" "8874831" "8880791" "8904098" "8904099" "3916390" "5023421" "5026465" "5065092" "5112310" "5145068" "5158015" "5199142" "5216247" "5269382" "5336174" "5336176" "5363450"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/03/18 12:15

		"5421279" "5430742" "5444664" "5459647" "5487102" "5487623" "5490155" "5519663" "5519831" "5563839" "5571244" "5577213" "5614685" "5619644" "5630096" "5658507" "5675725" "5691209" "5693840" "5721212" "5721860" "5757712" "5769081" "5799200" "5799241" "5799244" "5810513" "5813029" "5816982" "5839774" "5870350" "5874995" "5890192" "5910635" "5944042" "5948029" "5952368" "5953215" "5991885" "7053470" "7089412" "7102391" "7107480" "7111142" "7136978" "7155627" "7200021" "7234099" "7353325" "7409491" "7409590" "7411859" "7421552" "7467251" "7519754" "7600142" "7613877" "7716411" "7818488" "7881150" "7952179").pn.				
S408	6	"9928186".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/03/18 12:15
S409	6	"9921762".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/03/18 12:15
S410	426	S404 AND ((G06F3/0659 OR G06F12/0246 OR G06F2212/7208 OR G06F13/4027 OR G06F13/28 OR G06F3/0613 OR G06F2212/205 OR G06F3/0685 OR G11C7/1072).CPC. OR (710/308).CCLS. OR (G06F3/06).IPCR.)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/03/18 12:15
S411	287	S410 and ((voltage or buch) near5 (converter or regulator))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/03/18 12:15
S412	12	S411 and (S407 or S408 or S409)	US-PGPUB; USPAT;	OR	ON	2021/03/18 12:15

			USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			

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Doc description: Information Disclosure Statement (IDS) Filed

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT
(Not for submission under 37 CFR 1.99)

Application Number	17138766
Filing Date	2020-12-30
First Named Inventor	Hyun Lee
Art Unit	~~1731~~ 2135
Examiner Name	Hashem Farrokh
Attorney Docket Number	0016.001000H

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Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	17138766
	Filing Date	2020-12-30
	First Named Inventor	Hyun Lee
	Art Unit	1731
	Examiner Name	
	Attorney Docket Number	0016.001000H

	1	Petition for Inter Partes Review of U.S. Pat. No. 8,516,187 (on behalf of SMART Modular Technologies, Inc.), filed Aug. 22, 2014.	
	2	Petition for Inter Partes Review of U.S. Pat. No. 8,671,243, filed May 29, 2013.	
	3	Petition for Inter Partes Review of U.S. Pat. No. 8,874,831, filed Jul. 26, 2012.	
	4	~~Wong, A. "The BIOS Optimization Guide", Adrian's Rojak Pot, Rev. 6.2, 1998-2001, 67 pages.~~	
	5	Petition for Inter Partes Review of U.S. Patent No. 8,301,833 (on behalf of SMART Modular Technologies, Inc.), filed Aug. 22, 2014.	
	6	US Patent Application No. 60/912,321, Case No. No. IPR2017-00692-1007 (PTAB), filed April 17, 2017, 42 pages.	
	7	Petition for Inter Partes Review of US Patent 8,516,187, IPR2014-00982 (PTAB), dated June 19, 2014, 67 pages.	
	8	Petition for Inter Partes Review of US Patent No. 8,671,243, Case No. IPR2017-00587-1(PTAB), May 29, 2013, 82 pages.	
	9	Petition for Inter Partes Review, SanDisk Corporation v. Netlist, Inc., Patent 8,301,833, IPR2014-00994 (PTAB), filed June 20, 2014, 69 pages.	
	10	Webster's II New College Dictionary, Houghton Mifflin Company, Boston, MA, 2001, pp. 259, 1115.	
	11	Videotaped Deposition of Russel Jacob Baker, Patent No. 8,671,243, Case Nos. IPR2017-00587-1030 (PTAB), filed December 18, 2017, 268 pages.	

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	Application Number	17138766
	Filing Date	2020-12-30
	First Named Inventor	Hyun Lee
	Art Unit	1731
	Examiner Name	
	Attorney Docket Number	0016.001000H

	12	Petitioners Demonstratives, SK hynix Inc., et al., v. Netlist, Inc., U.S. Patent No. 8,671,243, IPR2017-00587-1037, 89 pages.	
	13	Petitioners' Reply in Support of Its Motion to Exclude, U.S. Patent No. 8,874,831, Case No. IPR2017-00692, filed April 9, 2018, 8 pages.	
	14	Petitioners' Reply to Patent Owner's Response, Inter Partes Review No. IPR2017-00587-16, Patent No. 8,671,243, filed Jan. 12, 2018, 38 pages.	
	15	Petitioners' Reply, U.S. Patent No. 8,874,831, Case No. IPR2017-00692 (PTAB), Paper No. 15, filed March 2, 2018, 35 pages.	
	16	Petitioners' Request for Hearing, U.S. Patent No. 8,301,833, Case No. Case No. IPR2017-00649-2020 (PTAB), Paper No. 8, entered Aug, 23, 2017, 18 pages.	
	17	Prosecution History, Application No. 12,240,916, US Patent No. 8,301,833, SK hynix Inc v Netlist Inc, Case No. IPR2017-00649-1002 (PTAB), received date April 13, 2009, 320 pages.	
	18	Prosecution History, Application No. 13,559,476, US Patent No. 8,301,833, SK hynix Inc v Netlist Inc, Case No. IPR2017-00649-1002 (PTAB), received date Sep. 5, 2014, 312 pages.	
	19	Prosecution History, Provisional Application No. 60/941,586, SK hynix Inc v Netlist Inc, Case No. IPR2017-00649-1005 (PTAB), received date Oct. 15, 2012, 23 pages.	
	20	Provisional Application for Advance Dynamic Disk Memory Module, Specification, SK hynix Inc., V. Netlist, Inc., Case No. IPR2017-00649-1006 (PTAB), dated Dec. 8, 2005, 53 pages.	
	21	Provisional Application No. 60/912,321 filed Apr. 17, 2007.	
	22	Provisional Application No. 60/941,586 filed Jun. 1, 2007.	

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
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	Filing Date	2020-12-30
	First Named Inventor	Hyun Lee
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	Examiner Name	
	Attorney Docket Number	0016.001000H

	23	Requirement for Restriction Election, SanDisk Corporation v. Netlist, Inc., Patent 8,301,833, IPR2014-00994-1003 (PTAB), dated March 31, 2019, 7 pages.	
	24	Restriction Requirement in U.S. Appl. No. 12/240,916, dated Mar. 31, 2011.	
	25	~~Search on Amazon Website for "memory module", downloaded Oct. 12, 2017, 6 pages.~~	
	26	Search Report (Updated) Prior Art Search for U.S.Patent No. 8,301,833, Global Patent Solutions, Nov. 24, 2020, 179 pages.	
	27	Search Report Prior Art Search for U.S.Patent No. 8,301,833, Global Patent Solutions, Nov. 2, 2020, 38 pages.	
	28	Second Amended Answer and Counterclaims to Plaintiff's Complaint for Declaratory Judgment, Diablo Technologies, Inc. v. Netlist, Inc., Case No. 4:13-CV-03901 (NDCA), YGR, filed February 17, 2014, 21 pages.	
	29	~~Smart Storage Systems, Inc's Invalidity Contentions, Case No. 4:13-cv-05889-YGR, dated Jun. 6, 2014.~~	
	30	~~Supplemental Declaration of Daniel E. Alberti in Response to Court Order [Docket No. 361] in Support of Motion to Withdraw as Counsel of Record, Netlist v. Smart Storage Systems, Inc. et. al., Case 4:13-cv-05889-YGR Document 362, filed September 5, 2018, 13 pages.~~	
	31	Supplemental Declaration of Ronald H. Spuhler, Netlist v. Smart Storage Systems, Inc. et. al., Case 4:13-cv-05889-YGR Document 305-1, filed March 10, 2015, 2 pages.	
	32	~~Supplemental Declaration of Steven J. Corr, Netlist v. Smart Storage Systems, Inc. et. al., Case 4:13-cv-05889-YGR~~ Document 309, filed March 17, 2015, 3 pages.	
	33	~~Switches - DT Online, Switches, Exhibit 1022, Case No. IPR2017-00587, accessed October 13, 2017, 3 pages.~~	

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ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /H.F/

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
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	Filing Date	2020-12-30
	First Named Inventor	Hyun Lee
	Art Unit	1731
	Examiner Name	
	Attorney Docket Number	0016.001000H

	34	U.S. Appl. No. 60/912,321, filed Apr. 17, 2007.	
	35	U.S. Office Action in U.S. Appl. No. 13/536,173, mailed on Apr. 15, 2013, pp. 1-10.	
	36	~~UPDATED JOINT CASE MANAGEMENT STATEMENT, U.S. DISTRICT COURT NORTHERN DISTRICT OF~~ CALIFORNIA, Case No. 4:13-cv-03916-YGR, Document 53, filed January 6, 2014.	
	37	US Patent Application No. 12/240,916, Case No. IPR2017-00692-2018 (PTAB), dated Sep. 29, 2008, 52 pages.	

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Examiner Signature	/HASHEM FARROKH/	Date Considered	03/15/2021

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ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /H.F/

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	17138766
	Filing Date	2020-12-30
	First Named Inventor	Hyun Lee
	Art Unit	1731
	Examiner Name	
	Attorney Docket Number	0016.001000H

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

See attached certification statement.

☒ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Khaled Shami/	Date (YYYY-MM-DD)	2021-03-11
Name/Print	Khaled Shami	Registration Number	38745

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**		
	Application Number	17138766
	Filing Date	2020-12-30
	First Named Inventor	Hyun Lee
	Art Unit	~~1731~~ 2135
	Examiner Name	Hashem Farrokh
	Attorney Docket Number	0016.001000H

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	Examiner Name	
	Attorney Docket Number	0016.001000H

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	Examiner Name	
	Attorney Docket Number	0016.001000H

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	Art Unit	1731
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	Attorney Docket Number	0016.001000H

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Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

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A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Khaled Shami/	Date (YYYY-MM-DD)	2021-03-11
Name/Print	Khaled Shami	Registration Number	38745

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SERIAL NUMBER	FILING or 371(c) DATE RULE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
17/138,766	12/30/2020	710	2135	0016.001000H

APPLICANTS

Netlist, Inc., Irvine, CA;

INVENTORS

Hyun Lee, Ladera Ranch, CA;
Chi-She Chen, Walnut, CA;
Jeffrey C. Solomon, Irvine, CA;
Scott H. Milton, Irvine, CA;
Jayesh Bhakta, Cerritos, CA;

**** CONTINUING DATA ***************************

This application is a CON of 15/934,416 03/23/2018
which is a CON of 14/840,865 08/31/2015 PAT 9928186
which is a CON of 14/489,269 09/17/2014 PAT 9158684
which is a CON of 13/559,476 07/26/2012 PAT 8874831
which claims benefit of 61/512,871 07/28/2011
and is a CIP of 12/240,916 09/29/2008 PAT 8301833
which is a CON of 12/131,873 06/02/2008 ABN
which claims benefit of 60/941,586 06/01/2007

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Foreign Priority claimed ❑ Yes ☑ No 35 USC 119(a-d) conditions met ❑ Yes ☑ No Verified and Acknowledged /HASHEM FARROKH/ Examiner's Signature	❑ Met after Allowance Initials	STATE OR COUNTRY	SHEETS DRAWINGS	TOTAL CLAIMS	INDEPENDENT CLAIMS
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Shami Messinger PLLC
1000 Wisconsin Ave. NW
Suite 200
Washington, DC 20007
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TITLE

FLASH-DRAM HYBRID MEMORY MODULE

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Application Number	17138766
Filing Date	2020-12-30
First Named Inventor	Hyun Lee
Art Unit	~~1731~~ 2135
Examiner Name	Hashem Farrokh
Attorney Docket Number	0016.001000H

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	48	Petition for Inter Partes Review of U.S. Pat. No. 8,301,833 (on behalf of SMART Modular Technologies, Inc.), filed Aug. 22, 2014.	
	49	Petition for Inter Partes Review of U.S. Pat. No. 8,301,833, filed Sep. 29, 2008.	
	50	Petition for Inter Partes Review of U.S. Pat. No. 8,516,187 (on behalf of SanDisk, Corp.), filed Jun. 19, 2014.	

If you wish to add additional non-patent literature document citation information please click the Add button [Add]

EXAMINER SIGNATURE

Examiner Signature	/HASHEM FARROKH/	Date Considered	03/15/2021

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /H.F/

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	17138766
	Filing Date	2020-12-30
	First Named Inventor	Hyun Lee
	Art Unit	1731
	Examiner Name	
	Attorney Docket Number	0016.001000H

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

See attached certification statement.

☒ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Khaled Shami/	Date (YYYY-MM-DD)	2021-03-11
Name/Print	Khaled Shami	Registration Number	38745

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /H.F/

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /H.F/

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT: Netlist, Inc.	CONF. NO: 8804
APPLICATION NO: 17/138,766	ART UNIT: 2135
FILING DATE: 12/30/20	EXAMINER: FARROKH, Hashem

TITLE: FLASH-DRAM HYBRID MEMORY MODULE

Mail Stop Issue Fee
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

REQUEST FOR CONSIDERATION OF TIMELY CITED REFERENCES AND COMMENTS ON STATEMENT OF REASONS FOR ALLOWANCE

Commissioner:

Applicant gratefully acknowledges the indication of allowance of Claims 1-30 in the Notice of Allowance mailed March 24, 2021.

The Notice of Allowance indicates that foreign references KR100606242 and WO2013016723 were not considered because copies thereof were not provided. Applicant respectfully disagrees. A copy of KR100606242 was submitted in the Information Disclosure Statement of March 11, 2021. In addition, a copy of WO2013016723 was cited in the information disclosure statement filed March 23, 2018 in parent application 15/934,416. Applicant respectfully requests consideration of these timely filed references and acknowledgement of same in a suitably marked Form PTO-892.

In addition, page 5 of the Notice of Allowance states:

> The prior art of record including the disclosures of Chen et al. (US 20120271990 A1), Bates (US 20070136523A1), and Prete et al. (US 2008012662A1) neither anticipates nor renders obvious the above-recited combination.

Applicant respectfully agrees that US 2008012662A1 and US 20070136523A1 do not anticipate nor render obvious the presently claimed invention. Applicant respectfully points out that the first named inventor of US 20070136523A1 is Bonnella, not Bates.

In addition, Applicant respectfully points out that Chen et al. (US 20120271990 A1) is not prior art at least because it is an issued patent from a commonly-owned ancestor application of the instant application and shares a common priority date with the instant application.

Pursuant to 37 C.F.R. § 1.104, Applicant respectfully submits the instant statement commenting on the Examiner's reasons for allowance.

Applicant maintains that additional and/or alternative reasons for allowance may exist apart from those expressed by the Examiner and the Applicant, and these reasons may be independently sufficient to establish the patentability of each of the allowed dependent or independent claims.

Applicant respectfully reserves the right to introduce, articulate, or otherwise comment on any such additional reasons for allowance as may be appropriate in any future proceedings concerning the one or more claimed embodiments.

To the extent that the Examiner's reasons for allowance are inconsistent with applicable case law, statutes, and regulations, Applicant respectfully disagrees with them. Furthermore, Applicant does not admit to any characterization or limitation of the claims or to any characterization of a reference by the Examiner, particularly any that are inconsistent with the language of the claims considered in their entirety and including all of their constituent limitations.

Respectfully submitted,

Dated: April 8, 2021

/Khaled Shami/_
Khaled Shami
Reg. No. 38,745

Shami Messinger PLLC
1000 Wisconsin Ave N.W., Suite 200
Washington, D.C. 20007
202-516-6900

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT: Netlist, Inc.	CONF. NO: 8804
APPLICATION NO: 17/138,766	ART UNIT: 2135
FILING DATE: 12/30/20	EXAMINER: FARROKH, Hashem

TITLE: FLASH-DRAM HYBRID MEMORY MODULE

Mail Stop Correction of Inventorship
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

CORRCTION OF INVENTORSHIP UNDER 37 C.F.R. § 1.48 PURSUANT TO 35 U.S.C. 116

Commissioner:

Applicants respectfully requests correction of inventorship under 37 C.F.R. § 1.48 pursuant to 35 U.S.C. 116 in the above-captioned application. The actual inventors are:

1. **CHEN, Chi-She**
2. **SOLOMON, Jeffery C.**
3. **MILTON, Scott H.**
4. **BHAKTA, Jayesh**

Submitted herewith in support of the instant request are:

1. **A corrected Application Data Sheet (ADS) in accordance with 37 C.F.R. § 1.76 that identifies each inventor by his or her legal name**
2. **The processing fee set forth in 37 C.F.R. § 1.17(i)**
3. **The fee set forth in 37 C.F.R. § 1.17(d)**

It is not believed that additional fees are required in support of this request. However, authorization is hereby granted to charge additional fees to our Deposit Account No. 60-2034 should such additional fees be required.

Respectfully submitted,

Dated: April 8, 2021

/Khaled Shami/
Khaled Shami
Reg. No. 38,745

SHAMI MESSINGER PLLC
1000 Wisconsin Ave N.W., Suite 200
Washington, D.C. 20007
202-516-6900

Doc Code: R48.REQ
Document Description: Request under Rule 48 correcting inventorship

PTO/AIA/40 (04-18)
Approved for use through 11/30/2020. OMB 0651-0031
U.S. Patent and Trademark Office, U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

REQUEST FOR CORRECTION IN A PATENT APPLICATION RELATING TO INVENTORSHIP OR AN INVENTOR NAME, OR ORDER OF NAMES, OTHER THAN IN A REISSUE APPLICATION (37 CFR 1.48)

Application Number	17/138,766
Filing Date	Dec. 30, 2020
First Named Inventor	CHEN, Chi-She
Art Unit	2135
Examiner Name	FARROKH, Hashem
Practitioner Docket Number	0016.001000H

To: Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Applicant hereby **requests that the inventorship be corrected or changed, or that the name of the inventor or a joint inventor, or the order of the names of joint inventors, be changed,** in the above-identified application. **Note**: 37 CFR 1.48 applies to any request to correct inventorship filed on or after September 16, 2012, regardless of the application filing date. **Do not submit this form after payment of the issue fee or if the application has been patented.** See 37 CFR 1.324 for correction of inventorship in a patent.

Please check the applicable box(es) below.

For a nonprovisional application:

☒ 1. This request is to correct or change the inventorship in a **nonprovisional** application (**under 37 CFR 1.48(a)**) and includes:

☒ An application data sheet (ADS) in accordance with 37 CFR 1.76(c) with the corrected or updated information shown with markings (*e.g.*, underlining for insertions, strikethrough for deletions). See the Manual of Patent Examining Procedure (MPEP) section 601.05(a) for information about filing an ADS in an application filed on/after September 16, 2012. For information about filing a Supplemental ADS in an application filed before September 16, 2012, see MPEP 601.05(b).

☒ The processing fee set forth in 37 CFR 1.17(i). $ 140

☐ An inventor is being added. An inventor's oath or declaration by any actual inventor who has not yet executed an oath or declaration is required (see 37 CFR 1.48(b)). See MPEP 602.01(a) for information about an inventor's oath or declaration for an application filed on/after September 16, 2012 (*e.g.*, form **PTO/AIA/01**). For information about an inventor's oath or declaration for an application filed before September 16, 2012 (*e.g.*, form **PTO/SB/01**), see MPEP 602.01(b).

☒ This request is being filed after the first Office action on the merits has been given or mailed (see 37 CFR 1.48(c) and 1.17(d)). Check one of the following:

☐ This request to correct or change the inventorship is due solely to the cancellation of claims in the application.

OR

☒ The fee set forth in 37 CFR 1.17(d) is due (in addition to the fee set forth in 37 CFR 1.17(i)). $ 640

This collection of information is required by 37 CFR 1.48. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

PTO/AIA/40 (04-18)
Approved for use through 11/30/2020. OMB 0651-0031
U.S. Patent and Trademark Office, U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

REQUEST FOR CORRECTION IN A PATENT APPLICATION RELATING TO INVENTORSHIP OR AN INVENTOR NAME, OR ORDER OF NAMES, OTHER THAN IN A REISSUE APPLICATION (37 CFR 1.48)

☐ 2. This request is to correct or update the name of the inventor or a joint inventor, or the order of names of joint inventors, in a **nonprovisional** application (**under 37 CFR 1.48(f)**) and includes:

☐ An application data sheet in accordance with 37 CFR 1.76(c) identifying the complete inventive entity, including the corrected or updated name of the inventor, or the new order of names shown with markings (*e.g.*, underlining for insertions, strikethrough for deletions). See the MPEP 601.05(a) for information about filing an ADS in an application filed on/after September 16, 2012. For information about filing a Supplemental ADS in an application filed before September 16, 2012, see MPEP 601.05(b).

☐ The processing fee set forth in 37 CFR 1.17(i). $ _____

For a provisional application:

☐ This request is to change or correct the inventorship, or correct or update the name of the inventor or a joint inventor, in a **provisional** application (**under 37 CFR 1.48(d)**) and includes:

☐ **Attached hereto** is a document that is signed by a party set forth in 37 CFR 1.33(b) and identifies each inventor by his or her legal name, in the preferred order. Note: the document may be an application data sheet in accordance with 37 CFR 1.76(c) that identifies the changes with markings (underlining for insertions, strikethrough for deletions).

☐ The processing fee set forth in 37 CFR 1.17(q). $ _____

Fee Payment Information:

☐ Applicant asserts small entity status. See 37 CFR 1.27.

☐ Applicant certifies micro entity status. See 37 CFR 1.29.
Form PTO/SB/15A or B or equivalent must either be enclosed or have been submitted previously

☐ A check in the amount of the fee is enclosed.

☐ Payment by credit card. Form PTO-2038 is attached.

■ The Director is hereby authorized to charge any fees which may be required, or credit any overpayment to Deposit Account No. 60-2034.

■ Payment made via EFS-Web.

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

I am the

☐ Applicant*

■ attorney or agent of record
Registration number 38,745

☐ attorney or agent acting under 37 CFR 1.34
Registration number _____

Signature /Khaled Shami/

Typed or printed name Khaled Shami

Date April 8, 2021

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications. *Juristic entities must be represented by a patent practitioner (See 37 CFR 1.31, applicable to any paper filed on or after September 16, 2012 that is presented on behalf of a juristic entity, regardless of application filing date). Submit multiple forms if more than one signature is required, see below**.

☐ ** Total of _____ forms are submitted.

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	0016.001000H
	Application Number	
Title of Invention	FLASH-DRAM HYBRID MEMORY MODULE	

The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76.
This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.

Secrecy Order 37 CFR 5.2:

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

Inventor Information:

Inventor 1

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	~~Hyun~~		~~Lee~~	

Residence Information (Select One) ◉ US Residency ○ Non US Residency ○ Active US Military Service

City	~~Ladera Ranch~~	State/Province	~~CA~~	Country of Residence i	~~US~~

Mailing Address of Inventor:

Address 1	~~21 Thalia Street~~
Address 2	

City	~~Ladera Ranch~~	State/Province	~~CA~~
Postal Code	~~92694~~	Country i	~~US~~

Inventor 2

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Chi-She		Chen	

Residence Information (Select One) ◉ US Residency ○ Non US Residency ○ Active US Military Service

City	Walnut	State/Province	CA	Country of Residence i	US

Mailing Address of Inventor:

Address 1	944 Crystal Water Lane
Address 2	

City	Walnut	State/Province	CA
Postal Code	91789	Country i	US

Inventor 3

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Jeffrey	C.	Solomon	

PTO/AIA/14 (08-15)
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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	0016.001000H
	Application Number	
Title of Invention	FLASH-DRAM HYBRID MEMORY MODULE	

Residence Information (Select One)	◉ US Residency	○ Non US Residency	○ Active US Military Service		
City	Irvine	**State/Province**	CA	**Country of Residence** [i]	US

Mailing Address of Inventor:

Address 1	6 Silver Fir		
Address 2			
City	Irvine	**State/Province**	CA
Postal Code	92604	**Country** [i]	US

Inventor 4

Legal Name

Prefix	**Given Name**	**Middle Name**	**Family Name**	**Suffix**
	Scott	H.	Milton	

Residence Information (Select One)	◉ US Residency	○ Non US Residency	○ Active US Military Service		
City	Irvine	**State/Province**	CA	**Country of Residence** [i]	US

Mailing Address of Inventor:

Address 1	49 Statehouse Place		
Address 2			
City	Irvine	**State/Province**	CA
Postal Code	92602	**Country** [i]	US

Inventor 5

Legal Name

Prefix	**Given Name**	**Middle Name**	**Family Name**	**Suffix**
	Jayesh		Bhakta	

Residence Information (Select One)	◉ US Residency	○ Non US Residency	○ Active US Military Service		
City	Cerritos	**State/Province**	CA	**Country of Residence** [i]	US

Mailing Address of Inventor:

Address 1	12220 Rose Street		
Address 2			
City	Cerritos	**State/Province**	CA
Postal Code	90703	**Country** [i]	US

All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the **Add** button. Add

Correspondence Information:

WEB ADS 1.0

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	0016.001000H
	Application Number	
Title of Invention	FLASH-DRAM HYBRID MEMORY MODULE	

Enter either Customer Number or complete the Correspondence Information section below. For further information see 37 CFR 1.33(a).			
☐ **An Address is being provided for the correspondence Information of this application.**			
Customer Number	151145		
Email Address		Add Email	Remove Email

Application Information:

Title of the Invention	FLASH-DRAM HYBRID MEMORY MODULE		
Attorney Docket Number	0016.001000H	**Small Entity Status Claimed**	☐
Application Type			
Subject Matter			
Total Number of Drawing Sheets (if any)	22	**Suggested Figure for Publication (if any)**	

Filing By Reference:

Only complete this section when filing an application by reference under 35 U.S.C. 111(c) and 37 CFR 1.57(a). Do not complete this section if application papers including a specification and any drawings are being filed. Any domestic benefit or foreign priority information must be provided in the appropriate section(s) below (i.e., "Domestic Benefit/National Stage Information" and "Foreign Priority Information").

For the purposes of a filing date under 37 CFR 1.53(b), the description and any drawings of the present application are replaced by this reference to the previously filed application, subject to conditions and requirements of 37 CFR 1.57(a).

Application number of the previously filed application	Filing date (YYYY-MM-DD)	Intellectual Property Authority or Country

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

☐ **Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32).
Either enter Customer Number or complete the Representative Name section below. If both sections are completed the customer Number will be used for the Representative Information during processing.

Please Select One:	◉ Customer Number	○ US Patent Practitioner	○ Limited Recognition (37 CFR 11.9)
Customer Number	151145		

WEB ADS 1.0

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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	0016.001000H
	Application Number	
Title of Invention	FLASH-DRAM HYBRID MEMORY MODULE	

Prefix	**Given Name**	Middle Name	**Family Name**	Suffix	Remove
Registration Number					
Prefix	**Given Name**	Middle Name	**Family Name**	Suffix	Remove
Registration Number					

Additional Representative Information blocks may be generated within this form by selecting the **Add** button.

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, 365(c), or 386(c) or indicate National Stage entry from a PCT application. Providing benefit claim information in the Application Data Sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78.
When referring to the current application, please leave the "Application Number" field blank.

Prior Application Status	Pending		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
	Continuation of	15934416	2018-03-23

Prior Application Status	Patented		Remove		
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
15934416	Continuation of	14840865	2015-08-31	9928186	2018-03-27

Prior Application Status	Patented		Remove		
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
14840865	Continuation of	14489269	2014-09-17	9158684	2015-10-13

Prior Application Status	Patented		Remove		
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
14489269	Continuation of	13559476	2012-07-26	8874831	2014-10-28

Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
13559476	Claims benefit of provisional	61512871	2011-07-28

PTO/AIA/14 (08-15)
Approved for use through 04/30/2017. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	0016.001000H
	Application Number	
Title of Invention	FLASH-DRAM HYBRID MEMORY MODULE	

Prior Application Status	Patented			Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
13559476	Continuation in part of	12240916	2008-09-29	8301833	2012-10-30

Prior Application Status	Abandoned		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
12240916	Continuation of	12131873	2008-06-02

Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
12131873	Claims benefit of provisional	60941586	2007-06-01

Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the **Add** button.

Foreign Priority Information:

This section allows for the applicant to claim priority to a foreign application. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55. When priority is claimed to a foreign application that is eligible for retrieval under the priority document exchange program (PDX) the information will be used by the Office to automatically attempt retrieval pursuant to 37 CFR 1.55(i)(1) and (2). Under the PDX program, applicant bears the ultimate responsibility for ensuring that a copy of the foreign application is received by the Office from the participating foreign intellectual property office, or a certified copy of the foreign priority application is filed, within the time period specified in 37 CFR 1.55(g)(1).

Application Number	Country	Filing Date (YYYY-MM-DD)	Access Code (if applicable)

Additional Foreign Priority Data may be generated within this form by selecting the **Add** button.

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications

☐ This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013.
NOTE: By providing this statement under 37 CFR 1.55 or 1.78, this application, with a filing date on or after March 16, 2013, will be examined under the first inventor to file provisions of the AIA.

PTO/AIA/14 (08-15)
Approved for use through 04/30/2017. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	0016.001000H
	Application Number	
Title of Invention	FLASH-DRAM HYBRID MEMORY MODULE	

Authorization or Opt-Out of Authorization to Permit Access:

When this Application Data Sheet is properly signed and filed with the application, applicant has provided written authority to permit a participating foreign intellectual property (IP) office access to the instant application-as-filed (see paragraph A in subsection 1 below) and the European Patent Office (EPO) access to any search results from the instant application (see paragraph B in subsection 1 below).

Should applicant choose not to provide an authorization identified in subsection 1 below, applicant **must opt-out** of the authorization by checking the corresponding box A or B or both in subsection 2 below.

NOTE: This section of the Application Data Sheet is **ONLY** reviewed and processed with the **INITIAL** filing of an application. After the initial filing of an application, an Application Data Sheet cannot be used to provide or rescind authorization for access by a foreign IP office(s). Instead, Form PTO/SB/39 or PTO/SB/69 must be used as appropriate.

1. Authorization to Permit Access by a Foreign Intellectual Property Office(s)

A. Priority Document Exchange (PDX) - Unless box A in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the State Intellectual Property Office of the People's Republic of China (SIPO), the World Intellectual Property Organization (WIPO), and any other foreign intellectual property office participating with the USPTO in a bilateral or multilateral priority document exchange agreement in which a foreign application claiming priority to the instant patent application is filed, access to: (1) the instant patent application-as-filed and its related bibliographic data, (2) any foreign or domestic application to which priority or benefit is claimed by the instant application and its related bibliographic data, and (3) the date of filing of this Authorization. See 37 CFR 1.14(h)(1).

B. Search Results from U.S. Application to EPO - Unless box B in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the EPO access to the bibliographic data and search results from the instant patent application when a European patent application claiming priority to the instant patent application is filed. See 37 CFR 1.14(h)(2).

The applicant is reminded that the EPO's Rule 141(1) EPC (European Patent Convention) requires applicants to submit a copy of search results from the instant application without delay in a European patent application that claims priority to the instant application.

2. Opt-Out of Authorizations to Permit Access by a Foreign Intellectual Property Office(s)

☐ A. Applicant **DOES NOT** authorize the USPTO to permit a participating foreign IP office access to the instant application-as-filed. If this box is checked, the USPTO will not be providing a participating foreign IP office with any documents and information identified in subsection 1A above.

☐ B. Applicant **DOES NOT** authorize the USPTO to transmit to the EPO any search results from the instant patent application. If this box is checked, the USPTO will not be providing the EPO with search results from the instant application.

NOTE: Once the application has published or is otherwise publicly available, the USPTO may provide access to the application in accordance with 37 CFR 1.14.

PTO/AIA/14 (08-15)
Approved for use through 04/30/2017. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	0016.001000H
	Application Number	
Title of Invention	FLASH-DRAM HYBRID MEMORY MODULE	

Applicant Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Applicant 1

If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section.

Clear

◉ Assignee	○ Legal Representative under 35 U.S.C. 117	○ Joint Inventor
○ Person to whom the inventor is obligated to assign.	○ Person who shows sufficient proprietary interest	

If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:

Name of the Deceased or Legally Incapacitated Inventor:

If the Applicant is an Organization check here. ☒

Organization Name	Netlist, Inc.		
Mailing Address Information For Applicant:			
Address 1	175 Technology Drive		
Address 2	Suite 150		
City	Irvine	**State/Province**	CA
Country[i] US		Postal Code	92618
Phone Number		Fax Number	
Email Address			

Additional Applicant Data may be generated within this form by selecting the Add button.

PTO/AIA/14 (08-15)
Approved for use through 04/30/2017. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	0016.001000H
	Application Number	
Title of Invention	FLASH-DRAM HYBRID MEMORY MODULE	

Assignee Information including Non-Applicant Assignee Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Assignee 1

Complete this section if assignee information, including non-applicant assignee information, is desired to be included on the patent application publication. An assignee-applicant identified in the "Applicant Information" section will appear on the patent application publication as an applicant. For an assignee-applicant, complete this section only if identification as an assignee is also desired on the patent application publication.

If the Assignee or Non-Applicant Assignee is an Organization check here. ☒

Organization Name	Netlist, Inc.

Mailing Address Information For Assignee including Non-Applicant Assignee:

Address 1	175 Technology Drive		
Address 2	Suite 150		
City	Irvine	**State/Province**	CA
Country i	US	Postal Code	92618
Phone Number		Fax Number	
Email Address			

Additional Assignee or Non-Applicant Assignee Data may be generated within this form by selecting the Add button.

PTO/AIA/14 (08-15)
Approved for use through 04/30/2017. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	0016.001000H
	Application Number	
Title of Invention	FLASH-DRAM HYBRID MEMORY MODULE	

Signature:

NOTE: This Application Data Sheet must be signed in accordance with 37 CFR 1.33(b). **However, if this Application Data Sheet is submitted with the INITIAL filing of the application and either box A or B is not checked in subsection 2 of the "Authorization or Opt-Out of Authorization to Permit Access" section, then this form must also be signed in accordance with 37 CFR 1.14(c).**

This Application Data Sheet **must** be signed by a patent practitioner if one or more of the applicants is a **juristic entity** (e. g., corporation or association). If the applicant is two or more joint inventors, this form must be signed by a patent practitioner, **all** joint inventors who are the applicant, or one or more joint inventor-applicants who have been given power of attorney (e.g., see USPTO Form PTO/AIA/81) on behalf of **all** joint inventor-applicants.

See 37 CFR 1.4(d) for the manner of making signatures and certifications.

Signature	/Khaled Shami/			Date (YYYY-MM-DD)	April 09, 2021
First Name	Khaled	Last Name	Shami	Registration Number	38745

Additional Signature may be generated within this form by selecting the Add button.

Electronic Patent Application Fee Transmittal

Application Number:	17138766
Filing Date:	30-Dec-2020
Title of Invention:	FLASH-DRAM HYBRID MEMORY MODULE
First Named Inventor/Applicant Name:	Hyun Lee
Filer:	Khaled Shami/Stephanie Semler
Attorney Docket Number:	0016.001000H

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
PROCESSING FEE, EXCEPT PROV. APPLS.	1830	1	140	140
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
CORRECTION OF INVENTORSHIP ON MERITS	1819	1	640	640
		Total in USD ($)		**780**

Electronic Acknowledgement Receipt	
EFS ID:	42400224
Application Number:	17138766
International Application Number:	
Confirmation Number:	8804
Title of Invention:	FLASH-DRAM HYBRID MEMORY MODULE
First Named Inventor/Applicant Name:	Hyun Lee
Customer Number:	151145
Filer:	Khaled Shami/Stephanie Semler
Filer Authorized By:	Khaled Shami
Attorney Docket Number:	0016.001000H
Receipt Date:	09-APR-2021
Filing Date:	30-DEC-2020
Time Stamp:	22:03:46
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	$780
RAM confirmation Number	E202149M04584434
Deposit Account	602034
Authorized User	Stephanie Semler
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: 37 CFR 1.16 (National application filing, search, and examination fees) 37 CFR 1.17 (Patent application and reexamination processing fees)	

37 CFR 1.19 (Document supply fees)

37 CFR 1.20 (Post Issuance fees)

37 CFR 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Amendment/Req. Reconsideration-After Non-Final Reject	Comments_on_Rsns_08_04_21_for_Allowance_03_24_21_0016001000H.pdf	116857 b53482352ee793d3d55f8527db473bf927920812	no	2
Warnings:					
Information:					
2	Request under Rule 48 correcting inventorship	00160001000H_Correction_of_Inventorship.pdf	114198 a697d0ddc462a6397b09830c9c0d472f2205ee22	no	2
Warnings:					
Information:					
3	Request under Rule 48 correcting inventorship	0016001000H_aia0040_04_08_21.pdf	199981 150981ef7e9a033a16a0c9981227754c7a023e2d	no	3
Warnings:					
Information:					
4	Application Data Sheet	Corrected_ADS_0016001000H.pdf	510157 918aa5a64fb14e5289831fd7fb1b91e500f3315b	no	9
Warnings:					
Information:					
This is not an USPTO supplied ADS fillable form					
5	Fee Worksheet (SB06)	fee-info.pdf	32354 8d509ec842da660c049f1f26da9f06bfe9d730eb	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	973547		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
17/138,766	12/30/2020	2135	2820	0016.001000H	30	3

CONFIRMATION NO. 8804

UPDATED FILING RECEIPT

151145
Shami Messinger PLLC
1000 Wisconsin Ave. NW
Suite 200
Washington, DC 20007

OC000000124856485

Date Mailed: 04/14/2021

Receipt is acknowledged of this non-provisional utility patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF FIRST INVENTOR, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection.

Please verify the accuracy of the data presented on this receipt. If an error is noted on this Filing Receipt, please submit a written request for a corrected Filing Receipt, including a properly marked-up ADS showing the changes with strike-through for deletions and underlining for additions. If you received a "Notice to File Missing Parts" or other Notice requiring a response for this application, please submit any request for correction to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections provided that the request is grantable.

Inventor(s)

Chi-She Chen, Walnut, CA;
Jeffrey C. Solomon, Irvine, CA;
Scott H. Milton, Irvine, CA;
Jayesh Bhakta, Cerritos, CA;

Applicant(s)

Netlist, Inc., Irvine, CA;

Assignment For Published Patent Application

Netlist, Inc., Irvine, CA

Power of Attorney: The patent practitioners associated with Customer Number 151145

Domestic Priority data as claimed by applicant

This application is a CON of 15/934,416 03/23/2018
which is a CON of 14/840,865 08/31/2015 PAT 9928186
which is a CON of 14/489,269 09/17/2014 PAT 9158684
which is a CON of 13/559,476 07/26/2012 PAT 8874831
which claims benefit of 61/512,871 07/28/2011
and is a CIP of 12/240,916 09/29/2008 PAT 8301833
which is a CON of 12/131,873 06/02/2008 ABN
which claims benefit of 60/941,586 06/01/2007

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.) - None.

Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

Permission to Access Application via Priority Document Exchange: Yes

Permission to Access Search Results: Yes

Applicant may provide or rescind an authorization for access using Form PTO/SB/39 or Form PTO/SB/69 as appropriate.

Projected Publication Date: 04/29/2021

Non-Publication Request: No

Early Publication Request: No

Title

FLASH-DRAM HYBRID MEMORY MODULE

Preliminary Class

710

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

LICENSE FOR FOREIGN FILING UNDER

Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

GRANTED

The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where the conditions for issuance of a license have been met, regardless of whether or not a license may be required as set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign AssetsControl, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

SelectUSA

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The U.S. offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to promote and facilitate business investment. SelectUSA provides information assistance to the international investor

community; serves as an ombudsman for existing and potential investors; advocates on behalf of U.S. cities, states, and regions competing for global investment; and counsels U.S. economic development organizations on investment attraction best practices. To learn more about why the United States is the best country in the world to develop technology, manufacture products, deliver services, and grow your business, visit http://www.SelectUSA.gov or call +1-202-482-6800.

Petitioners
Ex. 1002, p. 381

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
17/138,766	12/30/2020	Chi-She Chen	0016.001000H

CONFIRMATION NO. 8804

151145
Shami Messinger PLLC
1000 Wisconsin Ave. NW
Suite 200
Washington, DC 20007

37 CFR 1.48 ACKNOWLEDGEMENT LETTER

OC000000124856466

Date Mailed: 04/14/2021

NOTICE OF ACCEPTANCE OF REQUEST UNDER 37 CFR 1.48(a)

This is in response to the applicant's request under 37 CFR 1.48(a) submitted on 04/09/2021.

The request under 37 CFR 1.48(a) to correct the inventorship, to correct or update the name of an inventor, or to correct the order of names of joint inventors is accepted.

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

/ttran/

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/138,766	12/30/2020	Chi-She Chen	0016.001000H	8804

151145 7590 04/22/2021

Shami Messinger PLLC
1000 Wisconsin Ave. NW
Suite 200
Washington, DC 20007

EXAMINER	
FARROKH, HASHEM	

ART UNIT	PAPER NUMBER
2135	

NOTIFICATION DATE	DELIVERY MODE
04/22/2021	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

khaled@shamimessinger.com
mike@shamimessinger.com
stephanie@shamimessinger.com

Complintary ***Notice of Allowability***	**Application No.** 17/138,766	**Applicant(s)** Chen et al.	
	Examiner HASHEM FARROKH	**Art Unit** 2135	**AIA (FITF) Status** No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☑ This communication is responsive to 03/11/2021.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

3. ☑ The allowed claim(s) is/are 1-30 . As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see **http://www.uspto.gov/patents/init_events/pph/index.jsp** or send an inquiry to **PPHfeedback@uspto.gov.**

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☐ All b) ☐ Some *c) ☐ None of the:

   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____ .

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____ .

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☑ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date 03/11/2021.
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material _____.
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date. _____.
5. ☐ Examiner's Amendment/Comment
6. ☑ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/HASHEM FARROKH/
Primary Examiner, Art Unit 2135

Petitioners
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UNITED STATES DEPARTMENT OF COMMERCE
U.S. Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
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Alexandria, Virginia 22313-1450

APPLICATION NO./ CONTROL NO.	FILING DATE	FIRST NAMED INVENTOR/ PATENT IN REEXAMINATION	ATTORNEY DOCKET NO.
17/138,766	12/30/2020	Chen et al.	0016.001000H

	EXAMINER	
Shami Messinger PLLC 1000 Wisconsin Ave. NW Suite 200 Washington, DC 20007	HASHEM FARROKH	
	ART UNIT	PAPER
	2135	20210419

DATE MAILED: _____

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner for Patents

This communication is in response to the Applicant Letter received on 04/09/2021. The letter indicates that KR100606242 was submitted in the Information disclosure Statement (IDS) of March 11, 2021; and a copy WO2013016723 was cited in the IDS filed March 23, 2018. Examiner agrees, a signed copy of IDS' are enclosed. This NOA states that the prior art does not appear to teach or suggest the combination of features or limitations included in the claims, instead of the prior art of record as was stated in the NOA issued on 03/24/2021. The Letter also states that "additional and/or alternative reasons may exist apart from those expressed by the Examiner and the Applicant". The Examiner would agree. However, the Examiner has chosen to include the combination of features or limitations that appear not being disclosed or render obvious by the prior art searched. using combination features or limitations in the claims reason for allowance is consistent with MPEP (e.g., see MPEP 1302.14).

/HASHEM FARROKH/
Primary Examiner, Art Unit 2135

PTO-90C (Rev.04-03)

Notice of Pre-AIA or AIA Status

The present application is being examined under the pre-AIA first to invent provisions.

INFORMATION CONCERNING IDS:

The information disclosure statements (IDS') submitted on 03/11/2021 are in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statements have been considered by the examiner. However, a copy NPL documents shown by lined-through have not been considered by the Examiner because a copy of the lined-through documents have not been provide or they are not readily identifiable from title of documents listed.

Reason for Allowance

1. The primary reasons for allowance of claims 1-15 in the instant application is the combination with the inclusion of the following limitations: "a first buck converter configured to provide a first regulated voltage having a first voltage amplitude; a second buck converter configured to provide a second regulated voltage having a second voltage amplitude; a third buck converter configured to provide a third regulated voltage having a third voltage amplitude; a converter circuit configured to provide a fourth regulated voltage having a fourth voltage amplitude a plurality of synchronous dynamic random access memory (SDRAM) devices coupled to the first regulated voltage, and at least one circuit coupled between a first portion of the plurality of edge connections and the plurality of SDRAM devices, the at

least one circuit operable to (i) receive a first plurality of address and control signals via the first portion of the plurality of edge connections, and (ii) output a second plurality of address and control signals to the plurality of SDRAM devices, the at least one circuit coupled to both the second regulated voltage and the fourth regulated voltage, wherein a first one of the second and fourth voltage amplitudes is less than the a second one of the second and fourth voltage amplitudes."

2. *The primary reasons for allowance of claims 16-20 in the instant application is the combination with the inclusion of the following limitations:* **"first, second, and third buck converters configured to receive a pre-regulated input voltage and to produce first, second and third regulated voltages, respectively; a plurality of components coupled to the PCB, the plurality of components including a plurality of synchronous dynamic random access memory (SDRAM) devices, each component of the plurality of components coupled to one or more regulated voltages of the first, second, third and fourth regulated voltages; and a voltage monitor circuit configured to monitor an input voltage received via a first portion of the plurality of edge connections, the voltage monitor circuit configured to produce a signal in response to the input voltage having a voltage amplitude that is greater than a first threshold voltage"**

3. *The primary reasons for allowance of claims 23-30 in the instant application is the combination with the inclusion of the following limitations:* **"a plurality of components coupled to the PCB, each component of the plurality of components coupled to**

one or more regulated voltages of first, second, third and fourth regulated voltages, the plurality of components including a plurality of synchronous dynamic random access memory (SDRAM) devices and one or more registers, the plurality of SDRAM devices coupled to the first regulated voltage, the one or more registers coupled to (i) the second regulated voltage, (is) a portion of the plurality of edge connections, and (iii) the plurality of SDRAM devices, wherein a plurality of address and control signals are coupled to the one or more registers via the portion of the plurality of edge connections; first, second, and third buck converters configured to provide the first, second and third regulated voltages, respectively"

The prior art does not appear to teach or suggest the above-recited combinations.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays should be clearly labeled "Comments on Statement of Reasons for Allowance"

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays should be clearly labeled "Comments on Statement of Reasons for Allowance"

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to HASHEM FARROKH whose telephone number is (571)272-4193. The examiner can normally be reached on 8:30 am - 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mr. Sanjiv Shah can be reached on (571)272-4098. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. For questions regarding access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/HASHEM FARROKH/
Primary Examiner, Art Unit 2135

April 19, 2021

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/138,766	Chen et al.
	Examiner	Art Unit
	HASHEM FARROKH	2135

CPC - Searched*		
Symbol	**Date**	**Examiner**
G06F13/28; G06F13/4027; G06F13/1694; G06F13/4223; G06F12/0638; G06F12/0246; G06F1/185; G06F3/0613; G06F3/0685 OR G06F3/0659; G06F2212/7208; G06F2212/205; G11C7/1072; G11C14/0018	02/24/2021	HF
G06F3/0659; G06F12/0246; G06F2212/7208; G06F13/4027; G06F13/28; G06F3/0613; G06F2212/205; G06F3/0685; G11C7/1072	03/17/2021	HF

CPC Combination Sets - Searched*		
Symbol	**Date**	**Examiner**

US Classification - Searched*			
Class	**Subclass**	**Date**	**Examiner**
711	103	02/25/2021	HF
711	104	02/25/2021	HF
711	105	02/25/2021	HF
710	138	03/17/2021	HF

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

/HASHEM FARROKH/ Primary Examiner, Art Unit 2135	

Petitioners
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Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/138,766	Chen et al.
	Examiner	Art Unit
	HASHEM FARROKH	2135

Search Notes		
Search Notes	**Date**	**Examiner**
Assignee/Inventor Search	02/25/2021	HF
EAST Text Search	02/24/2021	HF
IP Search	02/25/2021	HF
Google Search	02/25/2021	HF
Assignee/Inventor Search Updated	03/17/2021	03/17/202
Assignee/Inventor Search Updated	03/17/2021	03/17/202

Interference Search			
US Class/CPC Symbol	**US Subclass/CPC Group**	**Date**	**Examiner**
G06F3/0685	G06F3/00	03/17/202	03/17/202
G06F12/0246	G06F12/00	03/17/202	03/17/202
G06F2212/205	G06F2212/00	03/17/202	03/17/202

/HASHEM FARROKH/ Primary Examiner, Art Unit 2135	

Petitioners
Ex. 1002, p. 391

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/138,766	Chen et al.
	Examiner	Art Unit
	HASHEM FARROKH	2135

CPC						
Symbol					Type	Version
G06F	/	13	/	28	F	2013-01-01
G06F	/	12	/	0246	I	2013-01-01
G06F	/	13	/	1694	I	2013-01-01
G06F	/	1	/	185	I	2013-01-01
G06F	/	12	/	0638	I	2013-01-01
G06F	/	13	/	4243	I	2013-01-01
G11C	/	7	/	1072	I	2013-01-01
G11C	/	14	/	0018	I	2013-01-01
G06F	/	3	/	0613	I	2013-01-01
G06F	/	3	/	0659	I	2013-01-01
G06F	/	3	/	0685	I	2013-01-01
G06F	/	13	/	4027	I	2013-01-01
G06F	/	2212	/	205	A	2013-01-01
G06F	/	2212	/	7208	A	2013-01-01

CPC Combination Sets								
Symbol					Type	Set	Ranking	Version
	/		/					

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	30	
/HASHEM FARROKH/ Primary Examiner, Art Unit 2135	19 April 2021	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	12

U.S. Patent and Trademark Office — Part of Paper No.: 20210419

Petitioners
Ex. 1002, p. 392

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/138,766	Chen et al.
	Examiner	Art Unit
	HASHEM FARROKH	2135

INTERNATIONAL CLASSIFICATION					
CLAIMED					
G06F	/	13	/	36	

NON-CLAIMED					
	/		/		

US ORIGINAL CLASSIFICATION	
CLASS	SUBCLASS
710	308

CROSS REFERENCES(S)						
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)					

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	30	
/HASHEM FARROKH/ Primary Examiner, Art Unit 2135	19 April 2021	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	12

U.S. Patent and Trademark Office — Part of Paper No.: 20210419

Petitioners
Ex. 1002, p. 393

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/138,766	Chen et al.
	Examiner	Art Unit
	HASHEM FARROKH	2135

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIMS

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	1	9	10	19	19	26	28								
2	2	7	11	20	20	29	29								
3	3	10	12	21	21	30	30								
4	4	11	13	22	22										
5	5	15	14	23	23										
8	6	12	15	24	24										
6	7	16	16	27	25										
14	8	17	17	28	26										
8	9	18	18	25	27										

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	30	
/HASHEM FARROKH/ Primary Examiner, Art Unit 2135	19 April 2021	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	12

U.S. Patent and Trademark Office — Part of Paper No.: 20210419

Petitioners
Ex. 1002, p. 394

Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (02-16)
Approved for use through 11/30/2020. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT
(Not for submission under 37 CFR 1.99)

Application Number	17138766
Filing Date	2020-12-30
First Named Inventor	Hyun Lee
Art Unit	1731 2135
Examiner Name	Hashem Farrokh
Attorney Docket Number	0016.001000H

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	9436600	B2	2016-09-06	Lee	Entire Document

If you wish to add additional U.S. Patent citation information please click the Add button. Add

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Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1					

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FOREIGN PATENT DOCUMENTS Remove

Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2]	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
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Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]

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ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /H.F/

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	17138766
	Filing Date	2020-12-30
	First Named Inventor	Hyun Lee
	Art Unit	1731
	Examiner Name	
	Attorney Docket Number	0016.001000H

	1	Petition for Inter Partes Review of U.S. Pat. No. 8,516,187 (on behalf of SMART Modular Technologies, Inc.), filed Aug. 22, 2014.	
	2	Petition for Inter Partes Review of U.S. Pat. No. 8,671,243, filed May 29, 2013.	
	3	Petition for Inter Partes Review of U.S. Pat. No. 8,874,831, filed Jul. 26, 2012.	
	4	~~Wong, A. "The BIOS Optimization Guide", Adrian's Rojak Pot, Rev. 6.2, 1998-2001, 67 pages.~~	
	5	Petition for Inter Partes Review of U.S. Patent No. 8,301,833 (on behalf of SMART Modular Technologies, Inc.), filed Aug. 22, 2014.	
	6	US Patent Application No. 60/912,321, Case No. No. IPR2017-00692-1007 (PTAB), filed April 17, 2017, 42 pages.	
	7	Petition for Inter Partes Review of US Patent 8,516,187, IPR2014-00982 (PTAB), dated June 19, 2014, 67 pages.	
	8	Petition for Inter Partes Review of US Patent No. 8,671,243, Case No. IPR2017-00587-1(PTAB), May 29, 2013, 82 pages.	
	9	Petition for Inter Partes Review, SanDisk Corporation v. Netlist, Inc., Patent 8,301,833, IPR2014-00994 (PTAB), filed June 20, 2014, 69 pages.	
	10	Webster's II New College Dictionary, Houghton Mifflin Company, Boston, MA, 2001, pp. 259, 1115.	
	11	Videotaped Deposition of Russel Jacob Baker, Patent No. 8,671,243, Case Nos. IPR2017-00587-1030 (PTAB), filed December 18, 2017, 268 pages.	

EFS Web 2.1.18

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /H.F/

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	17138766
	Filing Date	2020-12-30
	First Named Inventor	Hyun Lee
	Art Unit	1731
	Examiner Name	
	Attorney Docket Number	0016.001000H

	12	Petitioners Demonstratives, SK hynix Inc., et al., v. Netlist, Inc., U.S. Patent No. 8,671,243, IPR2017-00587-1037, 89 pages.	
	13	Petitioners' Reply in Support of Its Motion to Exclude, U.S. Patent No. 8,874,831, Case No. IPR2017-00692, filed April 9, 2018, 8 pages.	
	14	Petitioners' Reply to Patent Owner's Response, Inter Partes Review No. IPR2017-00587-16, Patent No. 8,671,243, filed Jan. 12, 2018, 38 pages.	
	15	Petitioners' Reply, U.S. Patent No. 8,874,831, Case No. IPR2017-00692 (PTAB), Paper No. 15, filed March 2, 2018, 35 pages.	
	16	Petitioners' Request for Hearing, U.S. Patent No. 8,301,833, Case No. Case No. IPR2017-00649-2020 (PTAB), Paper No. 8, entered Aug. 23, 2017, 18 pages.	
	17	Prosecution History, Application No. 12,240,916, US Patent No. 8,301,833, SK hynix Inc v Netlist Inc, Case No. IPR2017-00649-1002 (PTAB), received date April 13, 2009, 320 pages.	
	18	Prosecution History, Application No. 13,559,476, US Patent No. 8,301,833, SK hynix Inc v Netlist Inc, Case No. IPR2017-00649-1002 (PTAB), received date Sep. 5, 2014, 312 pages.	
	19	Prosecution History, Provisional Application No. 60/941,586, SK hynix Inc v Netlist Inc, Case No. IPR2017-00649-1005 (PTAB), received date Oct. 15, 2012, 23 pages.	
	20	Provisional Application for Advance Dynamic Disk Memory Module, Specification, SK hynix Inc., V. Netlist, Inc., Case No. IPR2017-00649-1006 (PTAB), dated Dec. 8, 2005, 53 pages.	
	21	Provisional Application No. 60/912,321 filed Apr. 17, 2007.	
	22	Provisional Application No. 60/941,586 filed Jun. 1, 2007.	

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /H.F/

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	17138766
	Filing Date	2020-12-30
	First Named Inventor	Hyun Lee
	Art Unit	1731
	Examiner Name	
	Attorney Docket Number	0016.001000H

	23	Requirement for Restriction Election, SanDisk Corporation v. Netlist, Inc., Patent 8,301,833, IPR2014-00994-1003 (PTAB), dated March 31, 2019, 7 pages.	
	24	Restriction Requirement in U.S. Appl. No. 12/240,916, dated Mar. 31, 2011.	
	25	~~Search on Amazon Website for "memory module", downloaded Oct. 12, 2017, 6 pages.~~	
	26	Search Report (Updated) Prior Art Search for U.S.Patent No. 8,301,833, Global Patent Solutions, Nov. 24, 2020, 179 pages.	
	27	Search Report Prior Art Search for U.S.Patent No. 8,301,833, Global Patent Solutions, Nov. 2, 2020, 38 pages.	
	28	Second Amended Answer and Counterclaims to Plaintiff's Complaint for Declaratory Judgment, Diablo Technologies, Inc. v. Netlist, Inc., Case No. 4:13-CV-03901 (NDCA), YGR, filed February 17, 2014, 21 pages.	
	29	~~Smart Storage Systems, Inc's Invalidity Contentions, Case No. 4:13-cv-05889-YGR, dated Jun. 6, 2014.~~	
	30	~~Supplemental Declaration of Daniel E. Alberti in Response to Court Order [Docket No. 361] in Support of Motion to Withdraw as Counsel of Record, Netlist v. Smart Storage Systems, Inc. et. al., Case 4:13-cv-05889-YGR Document 362, filed September 5, 2018, 13 pages.~~	
	31	Supplemental Declaration of Ronald H. Spuhler, Netlist v. Smart Storage Systems, Inc. et. al., Case 4:13-cv-05889-YGR Document 305-1, filed March 10, 2015, 2 pages.	
	32	~~Supplemental Declaration of Steven J. Corr, Netlist v. Smart Storage Systems, Inc. et. al., Case 4:13-cv-05889-YGR~~ Document 309, filed March 17, 2015, 3 pages.	
	33	~~Switches - DT Online, Switches, Exhibit 1022, Case No. IPR2017-00587, accessed October 13, 2017, 3 pages.~~	

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /H.F/

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	17138766
	Filing Date	2020-12-30
	First Named Inventor	Hyun Lee
	Art Unit	1731
	Examiner Name	
	Attorney Docket Number	0016.001000H

	34	U.S. Appl. No. 60/912,321, filed Apr. 17, 2007.	
	35	U.S. Office Action in U.S. Appl. No. 13/536,173, mailed on Apr. 15, 2013, pp. 1-10.	
	36	~~UPDATED JOINT CASE MANAGEMENT STATEMENT, U.S. DISTRICT COURT NORTHERN DISTRICT OF CALIFORNIA, Case No. 4:13-cv-03916-YGR, Document 53, filed January 6, 2014.~~	
	37	US Patent Application No. 12/240,916, Case No. IPR2017-00692-2018 (PTAB), dated Sep. 29, 2008, 52 pages.	

If you wish to add additional non-patent literature document citation information please click the Add button Add

EXAMINER SIGNATURE

Examiner Signature	/HASHEM FARROKH/	Date Considered	03/15/2021

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /H.F/

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	17138766
	Filing Date	2020-12-30
	First Named Inventor	Hyun Lee
	Art Unit	1731
	Examiner Name	
	Attorney Docket Number	0016.001000H

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

See attached certification statement.

☒ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Khaled Shami/	Date (YYYY-MM-DD)	2021-03-11
Name/Print	Khaled Shami	Registration Number	38745

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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(Not for submission under 37 CFR 1.99)

Application Number	17138766
Filing Date	2020-12-30
First Named Inventor	Hyun Lee
Art Unit	~~1751~~ 2135
Examiner Name	Hashem Farrokh
Attorney Docket Number	0016.001000H

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	Filing Date	2020-12-30
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	Art Unit	1731
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	17138766
	Filing Date	2020-12-30
	First Named Inventor	Hyun Lee
	Art Unit	1731
	Examiner Name	
	Attorney Docket Number	0016.001000H

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	7	Advisory Action in U.S. Appl. No. 12/240,916, dated Mar. 13, 2012.	
	8	Amendment and Reply to Office Action, SanDisk Corporation v. Netlist, Application No. 13/536,173, IPR2014-00982 (PTAB), dated May 21, 2013, 24 pages.	
	9	Amendment and Response to Election Restriction, SanDisk Corporation v. Netlist, Inc., Patent 8,301,833, IPR2014-00994-1004 (PTAB), dated May 20, 2011, 9 pages.	
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	Art Unit	1731
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Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

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SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Khaled Shami/	Date (YYYY-MM-DD)	2021-03-11
Name/Print	Khaled Shami	Registration Number	38745

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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Art Unit	1731 2135
Examiner Name	Hashem Farrokh
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	5	Exhibit, Application As Filed, SanDisk Corporation v. Netlist, Inc., Patent 8,301,833, IPR2014-00994 (PTAB), 52 pages.
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	11	Exhibit, Email from Defendant's Counsel, Netlist v. Smart Storage Systems, Inc. et. al., Case 4:13-cv-05889-YGR Document 305-17, filed March 10, 2015, 6 pages.

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	18	Exhibit, Order Denying Defendant's Motion to Stay Pending Inter Partes Review (Doc.59), The Procter and Gamble Company v. Team Technologies, Inc, et al., Case 4:13-cv-05889-YGR Document 316-6, filed March 24, 2015, 10 pages.	
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	31	Final Written Decision, US Patent No. 7,881,150, Case No. Case IPR2014-00882, (PTAB), Paper 33, filed December 14, 2015, 51 pages.	
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	Filing Date	2020-12-30
	First Named Inventor	Hyun Lee
	Art Unit	1731
	Examiner Name	
	Attorney Docket Number	0016.001000H

	34	~~Horowitz, P. et al., "The Art of Electronics", Cambridge University Press 2nd Ed. 1989, pp. 471495-496.~~	
	35	~~Innis, J., "MPC8560 PowerQUICC III Compact Flash Interface Design", Freescale Semiconductor, Inc., 2004-2006, pp. 1-23.~~	
	36	~~Intel 1.8 Volt Intel StrataFlash Wireless Memory (L18), 2003, 100 pages.~~	
	37	Inter Partes Review No. IPR2017-00692 (PTAB), Patent No. 8,874,831, filed July 26, 2012, 78 pages.	
	38	Inter Partes Review of U.S. Patent No. 8,874,831, Case IPR2017-00692 (PTAB), filed July 26, 2012, Paper No. 1, 78 pages.	
	39	International Preliminary Report on Patentabillity in PCT/US12/48750, mailed Apr. 3, 2014pp. 1-8.	
	40	International Search Report and Written Opinion in PCT/US12/48750, dated Oct. 10, 2012pp. 1-10.	
	41	ISSCC 2006 / SESSION 7 / NON-VOLATILE MEMORY / 7.7, IEEE International Solid-State Circuits Conference, 2006, 10 pages.	
	42	Jacob, B., "Memory Systems Cache, DRAM, Disk", Morgan Kaufman Publishers, Burlington, MA, 2008, Preface and Ch. 7 pp. 315-322, 58 pages.	
	43	Jandhyala, S. et al., "Design-For-Test Analysis of a Buffered SDRAM DIMM", Semiconductor Group, Texas Instruments, Proceedings of International Workshop in Memory Technology, Design and Testing, Singapore, August 13014, 1996,15 pages.	
	44	JEDEC Definition of DIMM, Exhibit 1029, IPR No. 2017-00587, December 18, 2017, 2 pages.	

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	45	JEDEC Global Standard for the Microelectronics Industry, Why JEDEC Standards Matter, 2014, 1 page.	
	46	~~JEDEC Standard 21-C"Configurations for Solid State Memories," pp. 4.5.5-1 to 4.5.5-18~~	
	47	JEDEC Standard No. 21-C (Release 17), Annex J: Serial Presence Detects for DDR2 SDRAM (Revision 1.3), 60 pages.	
	48	~~JEDEC Standard, "Configurations for Solid State Memories", JEDEC Standard 21-C, Release 9, Aug. 1999, 114 pages.~~	
	49	~~JEDEC Standard, DDR2 SDRAM Specification, JESD79-2B (Revision of JESD79-2A) Jan. 2005, 113 pages~~	

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CERTIFICATION STATEMENT

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☒ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

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Name/Print	Khaled Shami	Registration Number	38745

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7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

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Application Number	17138766
Filing Date	2020-12-30
First Named Inventor	Hyun Lee
Art Unit	~~1731~~ 2135
Examiner Name	Hashem Farrokh
Attorney Docket Number	0016.001000H

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	1	JEDEC Standard, FBDIMM Specification: DDR2 SDRAM Fully Buffered DIMM (FBDIMM) Design Specification; JESD205, JEDEC Solid State Tech. Assoc., Mar. 2007, 9 pages.	
	2	Joint Status Report Regarding Inter Partes Review, Netlist v. Smart Storage Systems, Inc. et. al., Case No. 4:13-CV-05889-YGR (NDCA), filed August 17, 2018, 4 pages.	
	3	Material Science & Engineering, Department of Material Science and Engineering, Stanford University, Exhibit 2011, Case No. IPR2017-00692, 2 pages.	
	4	Merriam-Webster's Collegiate Dictionary, Eleventh Ed., Merriam Webster Corporation, Springfield, MA, 2003, 7 pages.	
	5	Microsoft Computer Dictionary Fifth Edition, 2002, 3 pages.	
	6	Microsoft Computer Dictionary Fifth Edition, 2002, 9 pages.	
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	8	Microsoft Windows 2000 Professional Resource Kit, 76 pages.	
	9	Mutnuary, B. et al., "Analysis of Fully Buffered DIMM Interface in High-speed Server Applications", IBM Corp. xSeries eServer Development, 2006 Electronic Components and Technology Conference, pp. 203-208.	
	10	Notice of Allowance in U.S. Appl. No. 12/240,916, dated Sep. 17, 2012.	
	11	Notice of Allowance in U.S. Appl. No. 13/536,173, dated Jul. 2, 2013.	

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	12	Notice of Allowance in U.S. Appl. No. 13/559,476, dated May 6, 2014.	
	13	Notice of Allowance in U.S. Appl. No. 13/559,476, dated Sep. 29, 2014.	
	14	Notice of Allowance in U.S. Appl. No. 13/905,048, dated Dec. 19, 2013, 8 pages.	
	15	Notice of Allowance in U.S. Appl. No. 13/905,053, dated Dec. 11, 2013.	
	16	Notice of Allowance in U.S. Appl. No. 14/173,219 dated Jul. 7, 2014.	
	17	Notice of Allowance in U.S. Appl. No. 14/489,269, dated Oct. 8, 2015.	
	18	Notice of Allowance, SanDisk Corporation v. Netlist, Application No. 13/536,173, IPR2014-00982 (PTAB), dated July 2, 2013, 8 pages.	
	19	~~Office Action dated Aug. 19, 2016 of the Chinese Patent Application No. 201280047758.X, 9 pages.~~	
	20	Office Action in U.S. Appl. No. 12/240,916, mailed on Apr. 3, 2012.	
	21	Office Action in U.S. Appl. No. 13/536,176, dated on Apr. 15, 2013.	
	22	Office Action in U.S. Appl. No. 13/625,563, dated Aug. 5, 2013.	

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	23	Office Action in U.S. Appl. No. 13/625,563, dated May 9, 2014.	
	24	Office Action in U.S. Appl. No. 13/905,048, dated Aug. 1, 2013.	
	25	Office Action in U.S. Appl. No. 13/905,053, dated Aug. 1, 2013.	
	26	Office Action in U.S. Appl. No. 14/173,219, dated Mar. 13, 2014.	
	27	Office Action in U.S. Appl. No. 14/302,292, dated Dec. 21, 2015.	
	28	Office Action in U.S. Application No. 12/240,916, dated Feb. 1, 2012, 14 pages.	
	29	Office Action in U.S. Application No. 14/173,242, dated March 14, 2014, 7 pages.	
	30	Office Action, Application 12/240,916, IPR2014-0099-1005 (PTAB), dated July 29, 2011, 8 pages.	
	31	Office Action, Application 12/240,916, IPR2014-0099-1010 (PTAB), dated April 3, 2012, 11 pages.	
	32	Office Action, Application No. 13/536,173, IPR2014-00982 (PTAB), dated April 15, 2013, 9 pages.	
	33	~~Order Granting Joint Stipulation of Dismissal, Netlist v. Smart Storage Systems, Inc. et. al., Case No. 4:13-CV-05889-YGR (NDCA), filed May 15, 2020, 2 pages.~~	

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	34	Patent Owner's Demonstratives, Patent Number: 8,671,243, Case No. IPR 2017-00587-2023, (PTAB), 57 pages.	
	35	Patent Owner's Listing of New Arguments and Evidence in Petitioners' Reply, Patent No. 8,671,243, Case No. IPR2017-00587 (PTAB), filed Jan. 29, 2018, 6 pages.	
	36	Patent Owner's Opposition to Petitioners' Motion to Exclude, Patent No. 8,874,831, Case No. IPR2017-00692 (PTAB), filed April 2, 2018, 2017, 11 pages.	
	37	Patent Owner's Preliminary Response, Patent Number: 8,516,187, Case IPR2014-01371 (PTAB), filed Dec. 16, 2014, 66 pages.	
	38	Patent Owner's Preliminary Response, SanDisk Corporation v. Netlist, Inc., Patent 8,301,833, IPR2014-00994 (PTAB), Paper 8, dated October 2, 2014, 60 pages.	
	39	Patent Owner's Preliminary Response, SanDisk Corporation v. Netlist, Patent Number: 8,516,187, IPR2014-00982 (PTAB), dated September 26, 2014, 57 pages.	
	40	Patent Owner's Preliminary Response, SK hynix Inc., et al., v. Netlist, Patent No. 8,301,833, Case No. IPR2017-00649 (PTAB), filed May 1, 2017, 67 pages.	
	41	Patent Owner's Preliminary Response, SK hynix Inc., et al., v. Netlist, Patent No. 8,874,831, Case No. IPR2017-00692 (PTAB), filed May 1, 2017, 48 pages.	
	42	Patent Owner's Preliminary Response, Smart Modular Tech v Netlist Inc., Patent No. 8,301,833, Case IPR2014-01370 (PTAB), filed Dec. 16, 2014, 66 pages.	
	43	Patent Owner's Response, Patent No. 8,671,243, Case No. IPR2017-00587-12 (PTAB), filed Oct. 13, 2017, 80 pages.	
	44	Patent Owner's Response, SK hynix Inc., et al., v. Netlist, Patent No. 8,874,831, Case No. IPR2017-00692-12 (PTAB), filed Nov. 10, 2017, 77 pages.	

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	45	Patterson et al., "Computer Organization & Design: The Hardware/Software Interface" Morgan Kaufmann Publishers, Inc. (1998), 71 pages.	
	46	Petition for Inter Partes Review of Claims 1-30 of US.PATENT No. 8,301,833, IPR2014-01370 (PTAB), filed August 22, 2014, 68 pages.	
	47	Petition for Inter Partes Review of U.S. Pat. No. 8,301,833 (on behalf of SanDisk, Corp.), filed Jun. 20, 2014.	
	48	Petition for Inter Partes Review of U.S. Pat. No. 8,301,833 (on behalf of SMART Modular Technologies, Inc.), filed Aug. 22, 2014.	
	49	Petition for Inter Partes Review of U.S. Pat. No. 8,301,833, filed Sep. 29, 2008.	
	50	Petition for Inter Partes Review of U.S. Pat. No. 8,516,187 (on behalf of SanDisk, Corp.), filed Jun. 19, 2014.	

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(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/138,766	12/30/2020	Hyun Lee	0016.001000H	8804

TITLE OF INVENTION: FLASH-DRAM HYBRID MEMORY MODULE

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1200	$0.00	$0.00	$1200	06/24/2021

EXAMINER	ART UNIT	CLASS-SUBCLASS
FARROKH, HASHEM	2135	710-308000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-09 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 SHAMI MESSINGER PLLC
2
3

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document must have been previously recorded, or filed for recordation, as set forth in 37 CFR 3.11 and 37 CFR 3.81(a). Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE: Netlist, Inc.

(B) RESIDENCE: (CITY and STATE OR COUNTRY): Irvine, CA

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ☒ Corporation or other private group entity ❑ Government

4a. Fees submitted: ☒ Issue Fee ❑ Publication Fee (if required) ❑ Advance Order - # of Copies _____

4b. Method of Payment: *(Please first reapply any previously paid fee shown above)*

☒ Electronic Payment via EFS-Web ❑ Enclosed check ❑ Non-electronic payment by credit card (Attach form PTO-2038)

☒ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment to Deposit Account No. 60-2034

5. **Change in Entity Status** (from status indicated above)

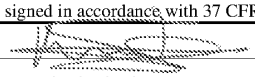
❑ Applicant certifying micro entity status. See 37 CFR 1.29

❑ Applicant asserting small entity status. See 37 CFR 1.27

❑ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature  Date April 23, 2021

Typed or printed name Khaled Shami Registration No. 38,745

PTOL-85 Part B (08-18) Approved for use through 01/31/2020 OMB 0651-0033 U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Petitioners
Ex. 1002, p. 443

Electronic Patent Application Fee Transmittal

Application Number:	17138766
Filing Date:	30-Dec-2020
Title of Invention:	FLASH-DRAM HYBRID MEMORY MODULE
First Named Inventor/Applicant Name:	Chi-She Chen
Filer:	Khaled Shami/Susanh Perez
Attorney Docket Number:	0016.001000H

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
UTILITY APPL ISSUE FEE	1501	1	1200	1200

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
			Total in USD ($)	**1200**

Electronic Acknowledgement Receipt	
EFS ID:	42534404
Application Number:	17138766
International Application Number:	
Confirmation Number:	8804
Title of Invention:	FLASH-DRAM HYBRID MEMORY MODULE
First Named Inventor/Applicant Name:	Chi-She Chen
Customer Number:	151145
Filer:	Khaled Shami/Susanh Perez
Filer Authorized By:	Khaled Shami
Attorney Docket Number:	0016.001000H
Receipt Date:	23-APR-2021
Filing Date:	30-DEC-2020
Time Stamp:	11:48:37
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	$1200
RAM confirmation Number	E20214MB51461131
Deposit Account	602034
Authorized User	Susanh Perez
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: 37 CFR 1.16 (National application filing, search, and examination fees) 37 CFR 1.17 (Patent application and reexamination processing fees)	

37 CFR 1.19 (Document supply fees)

37 CFR 1.20 (Post Issuance fees)

37 CFR 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Issue Fee Payment (PTO-85B)	IF_0016001000H.pdf	175227 f536f334c83cf749084393 6f582fbdabe2a7ceaa	no	1
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	30113 e7f39ebeb81aaf3e89d982b4e81313a05be5de71	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	205340		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.
National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.
New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/138,766	Lee et al.
	Examiner	**Art Unit**
	HASHEM FARROKH	2135

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIMS

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	1	9	10	19	19	26	28								
2	2	7	11	20	20	29	29								
3	3	10	12	21	21	30	30								
4	4	11	13	22	22										
5	5	15	14	23	23										
8	6	12	15	24	24										
6	7	16	16	27	25										
14	8	17	17	28	26										
13	9	18	18	25	27										

Change(s) applied
to document,
/N.B.H./
4/5/2021

NONE		**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	30	
/HASHEM FARROKH/ Primary Examiner, Art Unit 2135	18 March 2021	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	12

U.S. Patent and Trademark Office — Part of Paper No.: 20210317

Petitioners
Ex. 1002, p. 448

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
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Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
17/138,766	12/30/2020	Chi-She Chen	0016.001000H

CONFIRMATION NO. 8804

151145
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PUBLICATION NOTICE



Title:FLASH-DRAM HYBRID MEMORY MODULE

Publication No.US-2021-0124701-A1
Publication Date:04/29/2021

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

The publication may be accessed through the USPTO's publically available Searchable Databases via the Internet at www.uspto.gov. The direct link to access the publication is currently http://www.uspto.gov/patft/.

The publication process established by the Office does not provide for mailing a copy of the publication to applicant. A copy of the publication may be obtained from the Office upon payment of the appropriate fee set forth in 37 CFR 1.19(a)(1). Orders for copies of patent application publications are handled by the USPTO's Public Records Division. The Public Records Division can be reached by telephone at (571) 272-3150 or (800) 972-6382, by facsimile at (571) 273-3250, by mail addressed to the United States Patent and Trademark Office, Public Records Division, Alexandria, VA 22313-1450 or via the Internet.

In addition, information on the status of the application, including the mailing date of Office actions and the dates of receipt of correspondence filed in the Office, may also be accessed via the Internet through the Patent Electronic Business Center at www.uspto.gov using the public side of the Patent Application Information and Retrieval (PAIR) system. The direct link to access this status information is currently https://portal.uspto.gov/pair/PublicPair. Prior to publication, such status information is confidential and may only be obtained by applicant using the private side of PAIR.

Further assistance in electronically accessing the publication, or about PAIR, is available by calling the Patent Electronic Business Center at 1-866-217-9197.

Office of Data Managment, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

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APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/138,766	05/25/2021	11016918	0016.001000H	8804

151145 7590 05/05/2021

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ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 0 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site http://pair.uspto.gov for additional applicants):

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Netlist, Inc., Irvine, CA;
Jeffrey C. Solomon, Irvine, CA;
Scott H. Milton, Irvine, CA;
Jayesh Bhakta, Cerritos, CA;

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