UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.,
Petitioner,

v.

NETLIST, INC.,
Patent Owner

Patent No. 11,016,918
Issued: May 25, 2021
Filed: December 30, 2020
Inventors: Chi-She Chen, Jeffrey C. Solomon, Scott H. Milton, and Jayesh Bhakta

Title: Flash-DRAM Hybrid Memory Module

Inter Partes Review No. IPR2022-00996

DECLARATION OF DR. ANDREW WOLFE REGARDING U.S. PATENT NO. 11,016,918

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I. INTRODUCTION

A. Engagement

1. I have been retained by counsel for Samsung Electronics Co., Ltd. ("Samsung") as an expert witness in the above-captioned proceeding. I have been asked to provide my opinion about the state of the art of the technology described in U.S. Patent No. 11,016,918 ("the 918 Patent") (Ex. 1001) and on the patentability of the claims of this patent. The following is my written declaration on these topics.

B. Background and Qualifications

2. My professional qualifications, experience, publications and presentations, and a listing of previous cases in which I have provided expert testimony are set forth in my CV, attached as Exhibit 1004.

3. I am the founder and sole employee of Wolfe Consulting. Through Wolfe Consulting, I provide technical and business analytics to businesses on processor technology, computer systems, consumer electronics, software, design tools, data security, cryptography and intellectual property issues. I have more than thirty years' experience developing products, researching, consulting, and teaching in those fields. In that time, I have worked as a computer architect, computer system designer, and as an executive in the PC and electronics business. I have also taught at some of the world's leading institutions in those fields, including

Stanford University, Princeton University, Carnegie Mellon University, and Santa Clara University.

4. In 1985, I earned the B.S.E.E. degree in Electrical Engineering and Computer Science from the Johns Hopkins University. In 1987, I received the M.S. degree in Electrical and Computer Engineering from Carnegie Mellon University and in 1992, I received the Ph.D. degree in Computer Engineering from Carnegie Mellon University. My doctoral dissertation proposed a new approach for the architecture of a computer processor.

5. I have more than 35 years of experience as a computer architect, computer system designer, personal computer graphics designer, educator, and executive in the electronics industry.

6. In 1983, I began designing touch sensors, microprocessor-based computer systems, and I/O (input/output) cards for personal computers as a senior design engineer for Touch Technology, Inc. During the course of my design projects with Technology, I designed I/O cards for PC-compatible computer systems, including the IBM PC-AT, to interface with interactive touch-based computer terminals that I designed for use in public information systems. I continued designing and developing related technology as a consultant to the Carroll Touch division of AMP, Inc., where in 1986 I designed one of the first custom touch-screen integrated circuits. I designed the touch/pen input system for

the Linus WriteTop, which many believe to be the first commercial tablet computer.

7. From 1986 through 1987, I designed and built a high-performance computer system as a student at Carnegie Mellon University. From 1986 through early 1988, I also developed the curriculum, and supervised the teaching laboratory, for processor design courses.

8. In the latter part of 1989, I worked as a senior design engineer for ESL-TRW Advanced Technology Division. While at ESL-TRW, I designed and built a bus interface and memory controller for a workstation-based computer system, and also worked on the design of a multiprocessor system.

9. At the end of 1989, I (along with some partners) reacquired the rights to the technology I had developed at Touch Technology and at AMP, and founded The Graphics Technology Company. Over the next seven years, as an officer and a consultant for The Graphics Technology Company, I managed the company's engineering development activities and personally developed dozens of touch screen sensors, controllers, and interactive touch-based computer systems.

10. I have consulted, formally and informally, for a number of fabless semiconductor companies. In particular, I have served on the technology advisory boards for two processor design companies: BOPS, Inc., where I chaired the board, and Siroyan Ltd., where I served in a similar role for three networking chip

companies – Intellon, Inc., Comsilica, Inc., and Entridia, Inc. – and one 3D game accelerator company, Ageria, Inc.

11. I have also served as a technology advisor to Motorola and to several venture capital funds in the U.S. and Europe. Currently, I am a director at Turtle Beach Corporation, providing guidance in its development of premium audio peripheral devices for a variety of commercial electronic products.

12. From 1991 through 1997, I served on the Faculty of Princeton University as an Assistant Professor of Electrical Engineering. At Princeton, I taught undergraduate and graduate-level courses in Computer Architecture, Advanced Computer Architecture, Display Technology, and Microprocessor Systems, and conducted sponsored research in the area of computer systems and related topics. From 1999 through 2002, I taught a Computer Architecture course to both undergraduate and graduate students at Stanford University multiple times as a Consulting Professor. At Princeton, I received several teaching awards, both from students and from the School of Engineering. I have also taught advanced microprocessor architecture to industry professionals in IEEE and ACM sponsored seminars. I am currently a lecturer at Santa Clara University teaching courses on Microprocessor Systems, Advanced Logic Design, Real-Time Computing, and Mechatronics. I teach about memory, including DDR SDRAM and flash memory,

in several of my classes and rely on the JEDEC specifications as industry standards.

13. From 1997 through 2002, I held a variety of executive positions at a publicly held fabless semiconductor company originally called S3, Inc. and later called Sonicblue Inc. I held the positions of Chief Technology Officer, Vice President of System Integration Products, Senior Vice President of Business Development, and Director of Technology, among others.

14. In the roles listed above, I worked with and managed architecture and design teams responsible for the development of SRAM and DRAM memories, graphics chip memory controllers, and CPU memory controllers. I also worked with memory vendors and memory standards bodies, directly and through my staff, on the development of memory technology and standards. I have been involved with interpreting and understanding JEDEC memory standards since at least 1997. For many years, I had a direct-report staff member who would attend JEDEC meetings and bring me both proposed and final standards for review and comment. I also have used proposed and final JEDEC standards for chips, modules, and protocols to guide product decisions and to facilitate technical discussions with corporate partners and with consulting clients. I supervised design teams that implemented memory controllers for successful commercial products that interoperated with JEDEC-compliant DDR memory chips and memory modules.

15. My teams also developed the Rio MP3 players and a music delivery platform and webstore backend service for selling music. In 1999, this music delivery system was spun out as a separate company called RioPort.com. I served on the RioPort.com board of directors and became involved in their product and technology strategy. I also managed engineering and marketing for the Rio product line for a period of time as an interim general manager. The Rio MP3 players were among the first consumer products to incorporate large quantities of NAND flash memory. I worked with CEOs and General Managers at several leading flash memory suppliers on strategic planning for the flash market. I also worked with my engineering teams to evaluate and implement flash memory protocols and select flash memory form factors. During my time at SonicBlue we launched more than 30 new consumer electronics products.

16. I served as a board member and technical advisor as KBGear Inc. from 1999-2001. KBGear Inc. designed and produced digital cameras and music players.

17. I have published more than fifty peer-reviewed papers in computer architecture and computer systems and IC design. I have also chaired IEEE and ACM conferences in microarchitecture and integrated circuit design and served as an associate editor for IEEE and ACM journals. I served on the IEEE Computer Society Awards committee. I am an IEEE Fellow and a Member of ACM. I am a

named inventor on at least fifty-seven U.S. patents and thirty-seven foreign patents.

18. I have been the invited keynote speaker at the ACM/IEEE International Symposium on Microarchitecture and at the International Conference on Multimedia. I have also been an invited speaker on various aspects of technology or the PC industry at numerous industry events including the Intel Developer's Forum, Microsoft Windows Hardware Engineering Conference, Microprocessor Forum, Embedded Systems Conference, Comdex, and Consumer Electronics Show as well as at the Harvard Business School and the University Illinois Law School. I have been interviewed on subjects related to technology and the electronics industry by publications such as the Wall Street Journal, New York Times, LA Times, Time, Newsweek, Forbes, and Fortune as well as CNN, NPR, and the BBC. I have also spoken at dozens of universities including MIT, Stanford, University of Texas, Carnegie Mellon, UCLA, University of Michigan, Rice University, and Duke University.

C. Compensation and Prior Testimony

19. I am being compensated at a rate of $600.00 per hour for my study and testimony in this matter. My compensation is not contingent on the outcome of this matter or the specifics of my testimony.

20. My CV, attached as Exhibit 1004, lists all other cases in which, during the previous 4 years, I have testified as an expert at trial or by deposition.

D. Information Considered

21. My opinions are based on my years of education, research and experience, as well as my investigation and study of relevant materials. In forming my opinions, I have considered the materials I identify in this report and those listed in the Exhibit List at the end of this declaration.

22. I may rely upon these materials and/or additional materials to respond to arguments raised by the Patent Owner. I may also consider additional documents and information in forming any necessary opinions — including documents that may not yet have been provided to me.

23. My analysis of the materials produced in this matter is ongoing and I will continue to review any new materials as it is provided. This declaration represents only those opinions I have formed to date.

II. LEGAL STANDARDS FOR PATENTABILITY

24. In expressing my opinions and considering the subject matter of the claims of the 918 Patent, I am relying upon certain basic legal principles that have been explained to me.

25. First, I understand that for an invention claimed in a patent to be found patentable, it must be, among other things, new and not obvious from what was known before the invention was made.

26. I understand the information that is used to evaluate whether an invention is new and not obvious is generally referred to as "prior art" and generally includes patents and printed publications (e.g., books, journal publications, articles on websites, product manuals, etc.).

27. I understand that in this proceeding the Petitioner has the burden of proving that the claims of the 918 Patent are anticipated by or obvious from the prior art by a preponderance of the evidence. I understand that "a preponderance of the evidence" is evidence sufficient to show that a fact is more likely true than it is not.

28. I understand that in this proceeding, the claims should be given their ordinary and accustomed meaning as understood by one of ordinary skill in the art in view of the patent and its file history. The claims after being construed in this manner are then to be compared to the information in the prior art.

29. I understand that in this proceeding, the information that may be evaluated is limited to patents and printed publications. My analysis below compares the claims to patents and printed publications that are prior art to the claims.

30. I understand that there are two ways in which prior art may render a patent claim unpatentable. First, the prior art can be shown to "anticipate" the claim. Second, the prior art can be shown to have made the claim "obvious" to a person of ordinary skill in the art. In this declaration I focus on "obviousness." My understanding of the legal standard for "obviousness" is set forth below.

31. I understand that a claimed invention is not patentable if it would have been obvious to a person of ordinary skill in the field of the invention at the time the invention was made.

32. I understand that the obviousness standard is defined in the patent statute (35 U.S.C. § 103(a)) as follows:

> A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

33. I understand that the following standards govern the determination of whether a claim in a patent is obvious. I have applied these standards in my evaluation of whether the asserted claims of the 918 Patent would have been considered obvious as of the priority date of the patent.

34. I understand that to find a claim in a patent obvious, one must make certain findings regarding the claimed invention and the prior art. Specifically, I

understand that the obviousness question requires consideration of four factors (although not necessarily in the following order):

- The scope and content of the prior art;
- The differences between the prior art and the claims at issue;
- The knowledge of a person of ordinary skill in the pertinent art; and
- Whatever objective factors indicating obviousness or non-obviousness may be present in any particular case.

35. In addition, I understand that the obviousness inquiry should not be done in hindsight, but must be done using the perspective of a person of ordinary skill in the relevant art as of the effective filing date of the patent claim.

36. I understand the objective factors indicating obviousness or non-obviousness may include: commercial success of products covered by the patent claims; a long-felt need for the invention; failed attempts by others to make the invention; copying of the invention by others in the field; unexpected results achieved by the invention; praise of the invention by those in the field; the taking of licenses under the patent by others; expressions of surprise by experts and those skilled in the art at the making of the invention; and the patentee proceeded contrary to the accepted wisdom of the prior art. I also understand that any of this evidence must be specifically connected to the invention rather than being associated with the prior art or with marketing or other efforts to promote an invention. I am not presently aware of any evidence of "objective factors"

suggesting the claimed methods are not obvious, and reserve my right to address any such evidence if it is identified in the future.

37. I understand the combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results. I also understand that an example of a solution in one field of endeavor may make that solution obvious in another related field. I also understand that market demands or design considerations may prompt variations of a prior art system or process, either in the same field or a different one, and that these variations will ordinarily be considered obvious variations of what has been described in the prior art.

38. I also understand that if a person of ordinary skill can implement a predictable variation, that variation would have been considered obvious. I understand that for similar reasons, if a technique has been used to improve one device, and a Skilled Artisan would recognize that it would improve similar devices in the same way, using that technique to improve the other device would have been obvious unless its actual application yields unexpected results or challenges in implementation.

39. I understand that the obviousness analysis need not seek out precise teachings directed to the specific subject matter of the challenged claim, but instead can take account of the "ordinary innovation" and experimentation that

does no more than yield predictable results, which are inferences and creative steps that a Skilled Artisan would employ.

40. I understand that sometimes it will be necessary to look to interrelated teachings of multiple patents; the effects of demands known to the design community or present in the marketplace; and the background knowledge possessed by a person having ordinary skill in the art. I understand that all these issues may be considered to determine whether there was an apparent reason to combine the known elements in the fashion claimed by the patent at issue.

41. I understand that the obviousness analysis cannot be confined by a formalistic conception of the words "teaching, suggestion, and motivation." I understand that in 2007, the Supreme Court issued its decision in *KSR Int'l Co. v. Teleflex, Inc.*, 550 U.S. 398 (2007), where the Court rejected the previous requirement of a "teaching, suggestion, or motivation to combine" known elements of prior art for purposes of an obviousness analysis as a precondition for finding obviousness. It is my understanding that *KSR* confirms that any motivation that would have been known to a person of skill in the art, including common sense, or derived from the nature of the problem to be solved, is sufficient to explain why references would have been combined.

42. I understand that a person of ordinary skill attempting to solve a problem will not be led only to those elements of prior art designed to solve the

same problem. I understand that under the *KSR* standard, steps suggested by common sense are important and should be considered. Common sense teaches that familiar items may have obvious uses beyond their primary purposes, and in many cases a person of ordinary skill will be able to fit the teachings of multiple patents together like pieces of a puzzle. As such, the prior art considered can be directed to any need or problem known in the field of endeavor as of the priority date of the patent and can provide a reason for combining the elements of the prior art in the manner claimed. In other words, the prior art does not need to be directed towards solving the same problem that is addressed in the patent. Further, the individual prior art references themselves need not all be directed towards solving the same problem.

43. I understand that obviousness does not require that the features of a secondary reference be bodily incorporated into the structure of the primary reference. Rather, the test is what the combined teachings of those references would have suggested to a Skilled Artisan. The disclosures of the prior art references need not be physically combinable. Combining the teachings of references should be the focus of the analysis.

44. I understand that an invention that might be considered an obvious variation or modification of the prior art may be considered non-obvious if one or more prior art references discourages or lead away from the line of inquiry

disclosed in the reference(s). A reference does not "teach away" from an invention simply because the reference suggests that another embodiment of the invention is better or preferred. My understanding of the doctrine of teaching away requires a clear indication that the combination should not be attempted (*e.g.*, because it would not work or explicit statements saying the combination should not be made).

45. I understand that a person of ordinary skill is also a person of ordinary creativity.

46. I further understand that in many fields, it may be that there is little discussion of obvious techniques or combination, and it often may be the case that market demand, rather than scientific literature or knowledge, will drive design trends. When there is such a design need or market pressure to solve a problem and there are a finite number of identified, predictable solutions, a person of ordinary skill has good reason to pursue the known options within their technical grasp. If this leads to the anticipated success, it is likely the product not of innovation but of ordinary skill and common sense. In that instance the fact that a combination was obvious to try might show that it was obvious. The fact that a particular combination of prior art elements was "obvious to try" may indicate that the combination was obvious even if no one attempted the combination. If the combination was obvious to try (regardless of whether it was actually tried) or

leads to anticipated success, then it is likely the result of ordinary skill and common sense rather than innovation.

III. THE 918 PATENT

A. Effective Filing Date of the 918 Patent: No Earlier Than June 2, 2008

47. The 918 Patent is a continuation of, *inter alia*, a utility application filed March 23, 2018, and also claims priority to U.S. Provisional Application No. 60/941,586 ("586 Provisional Application" or "586 Provisional") (Ex. 1005), filed June 1, 2007. Ex. 1001 (918 Patent), (60). The 918 Patent is a continuation-in-part of a utility application, U.S. Patent Application No. 12/240,916, filed September 29, 2008, which is a continuation of an abandoned utility application, U.S. Application No. 12/131,873 ("873 Application") (Ex. 1006), filed June 2, 2008.

48. In my opinion, as explained below, the effective filing date for the claims of the 918 Patent is no earlier than June 2, 2008 (the filing date of the 873 Application, Ex. 1006). In any event, all of the prior art I rely upon for my invalidity opinions predates June 1, 2007.

1. Several Limitations in All Claims Are Unsupported by the 586 Provisional Application Filed June 1, 2007

49. I have been asked to give my opinion as to whether, from the perspective of a Skilled Artisan, the 586 Provisional Application shows that the inventor actually invented what is claimed in each of the claims of the 918 patent, and possessed the claimed subject matter, as of the provisional filing date of June

1, 2007. When considering that question, I have considered whether the 586 Provisional Application explicitly or inherently discloses the elements of the claims. To determine whether the provisional inherently discloses an element, I considered whether any element not explicitly disclosed would be necessarily comprehended in the description provided by a Skilled Artisan. I understand that the knowledge of ordinary artisans may be used to inform what is actually in the provisional, but not to teach limitations that are not in the provisional, even if those limitations would be rendered obvious by the disclosure in the provisional.

50. I conclude that certain elements of each claim in the 918 patent is not adequately disclosed in the 586 Provisional Application, including but not limited to those discussed below.

a) Buck Converters – Claims 1, 16, 23

51. Each of independent claims 1, 16, and 23 include one or more limitations requiring first, second, and third "buck converters." Ex. 1001 (918 Patent), cls. 1, 16, 23.

52. There is no disclosure in the 586 Provisional Application of the claimed "buck converters." A Skilled Artisan would have understood at the time that a "buck converter" refers to a certain type of dc-dc switch-mode converter which produces a lower (step-down) average output voltage than the input dc voltage. Ex. 1032 (Mohan) at pp. 161 and 164. Instead of a "buck converter," the

586 Provisional discloses a "step-down transformer 84" which "acts as a voltage regulator to ensure that regulated voltages are supplied to the memory elements (e.g., 1.8V to the volatile DRAM elements 32 and 3.0V to the non-volatile flash memory elements 42) during power down." Ex. 1005 at [0017].

53. A Skilled Artisan would have understood at the time that a "buck converter" is different from a "step-down transformer" described in the 586 Provisional. To the extent the term "transformer" is meant to cover changing the voltage by any means which produces a regulated voltage, a Skilled Artisan would have understood that a step-down regulated voltage can also be provided by means other than a "buck converter," e.g., by a linear regulator, such as a low-dropout regulator (LDO). A Skilled Artisan would have understood that an LDO is different from the claimed "buck converter." *See*, *e.g.*, Ex. 1059 at 5:23-30 ("Switch mode buck converters have become popular due to two attractive features: first, they are more efficient than traditional low drop out regulators (LDO) (e.g., up to 95%) and second, they can provide relatively high currents with lower power dissipation on chip than an LDO can.").

54. Thus, it is my opinion that Patent Owner cannot show that the 586 Provisional Application's disclosure supports the limitations of the "buck converters" as recited in the independent claims of the 918 Patent.

b) Converter Circuit – Claims 1, 16, 23

55. Each of independent claims 1, 16, and 23 include a limitation requiring a "converter circuit" in addition to the three "buck converters." Ex. 1001 (918 Patent), cls. 1 ("a converter circuit configured to provide a fourth regulated voltage having a fourth voltage amplitude"), 16 ("a converter circuit configured to reduce the pre-regulated input voltage to provide a fourth regulated voltage"), 23 ("a converter circuit configured to provide the fourth regulated voltage").

56. There is no disclosure in the 586 Provisional Application of the claimed "converter circuit" in addition to the three claimed "buck converters." For the reasons discussed above, there is no disclosure in the 586 Provisional Application of the claimed "buck converters." *Supra* ¶¶51-54. Instead, the 586 Provisional discloses two transformers. A "step-up transformer 82 keeps the capacitor bank 86 charged at a peak value," and a "step-down transformer 84 acts as a voltage regulator to ensure that regulated voltages are supplied to the memory elements (e.g., 1.8V to the volatile DRAM elements 32 and 3.0V to the non-volatile flash memory elements 42) during power down." Ex. 1005 at [0017].

57. A Skilled Artisan would have understood at the time that these two transformers do not disclose a "converter circuit" in addition to the three "buck converters." Specifically, there is no disclosure of four different regulated voltages

being supplied in the 586 Provisional such that the fourth regulated voltage is provided by a "converter circuit."

58. Thus, it is my opinion that Patent Owner cannot show that the 586 Provisional Application's disclosure supports the limitation of the "converter circuit" as recited in the independent claims of the 918 Patent.

c) Dual Buck Converter – Claims 2, 17

59. Each of claims 2, 17, and 28 include a limitation requiring two buck converters to "operate as a dual buck converter." Ex. 1001 (918 Patent), cls. 2, 17, 28.

60. There is no disclosure in the 586 Provisional Application of buck converters or dual buck converters.

61. Thus, it is my opinion that Patent Owner cannot show that the 586 Provisional Application's disclosure supports the limitations of a "dual buck converter" as recited in claims 2 and 17 of the 918 Patent.

2. Some Limitations Appear Unsupported by the 873 Application Filed June 2, 2008, or by Any Later Application

62. I have also been asked to give my opinion as to whether, from the perspective of a Skilled Artisan, the 873 Application shows that the inventor actually invented what is claimed in each of the claims of the 918 Patent, and possessed the claimed subject matter, as of the 873 Application's filing date of June 2, 2008.

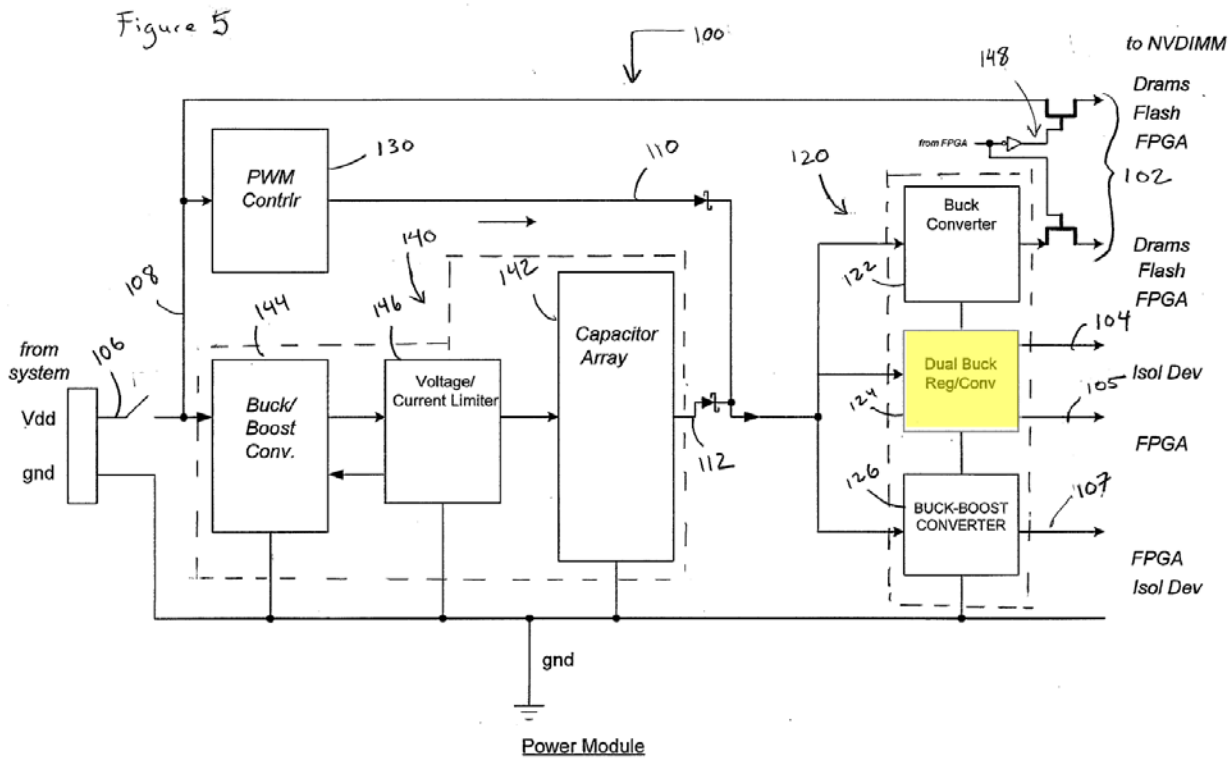
63. Using the same understanding of the legal standard discussed above, *supra* ¶49, I conclude that certain elements in the claims do not appear to be adequately disclosed in the 873 Application or any later application, as explained below.

a) First and Third Buck Converters Are Configured to Operate as a Dual Buck Converter – Claim 2

64. Claim 2 includes a limitation "wherein the first and third buck converters are further configured to operate as a dual buck converter." Ex. 1001 (918 Patent), cl. 2. Claim 1, from which claim 2 depends, includes a limitation for "a first buck converter configured to provide a first regulated voltage having a first voltage amplitude." Ex. 1001 (918 Patent), cl. 1. Claim 1 further requires "a plurality of synchronous dynamic random access memory (SDRAM) devices coupled to the first regulated voltage." Ex. 1001 (918 Patent), cl. 1.

65. There is no disclosure in the 873 Application, or any later application, of first and third buck converters configured to operate as a dual buck converter wherein a first regulated voltage from the dual buck converter is coupled to a plurality of SDRAM devices. The only disclosure of a dual buck converter in the 873 Application, or any later application, depicts the dual buck converter providing second and third regulated voltages to the isolation device and the FPGA. Ex. 1006 at 19-20 (¶0057) ("sub-block 124 comprises a dual buck converter. . . . The sub-block 124 can provide . . . . the second voltage 104 . . . to power the at least one

circuit 52 (e.g., isolation device) and the other reduced voltage 105 . . . to power the controller 62 (e.g., FPGA)."); *see also id.* at 49 (FIG. 5) (annotated below).



66. Thus, the 873 Application does not appear to provide support for the limitation of first and third buck converters "configured to operate as a dual buck converter" as recited in claim 2 of the 918 Patent.

B. Person of Ordinary Skill in the Art

67. Based on my experience and the prior art I discuss herein, I believe a person of ordinary skill in the art in the field of the 918 Patent in 2008 ("Skilled Artisan" or "POSITA") would have had an advanced degree in electrical or computer engineering, or a related field, and two years working or studying in the field of design or development of memory systems, or a bachelor's degree in such

engineering disciplines and at least three years working in the field. Additional training can substitute for educational or research experience, and vice versa. Such a hypothetical person would have been familiar with the JEDEC industry standards, and knowledgeable about the design and operation of standardized DRAM and SDRAM memory devices and memory modules and how they interacted with a memory controller and other parts of a computer system, including standard communication busses and protocols, such as PCI and SMBus busses and protocols. Such a hypothetical person would also have been familiar with the structure and operation of circuitry used to access and control computer memories, including sophisticated circuits such as ASICs, FPGAs, and CPLDs, and more low-level circuits such as tri-state buffers. Such a hypothetical person would further have been familiar with voltage supply requirements of such structures (e.g., memory modules, memory devices, memory controller, and associated access and control circuitry), including voltage conversion and voltage regulation circuitry.

C. Overview of the 918 Patent

68. The 918 Patent states that it describes "a memory system having a volatile memory subsystem, a non-volatile memory subsystem, a controller coupled to the non-volatile memory subsystem, and a circuit coupled to the volatile memory subsystem, to the controller, and to a host system." Ex. 1001 (918 Patent)

at 8:1-5. The 918 Patent explains that "[i]n a first mode of operation, the circuit is operable to selectively isolate the controller from the volatile memory subsystem, and to selectively couple the volatile memory subsystem to the host system to allow data to be communicated between the volatile memory subsystem and the host system." Ex. 1001 (918 Patent) at 8:5-10. The 918 Patent further explains that "[i]n a second mode of operation, the circuit is operable to selectively couple the controller to the volatile memory subsystem to allow data to be communicated between the volatile memory subsystem and the nonvolatile memory subsystem using the controller, and the circuit is operable to selectively isolate the volatile memory subsystem from the host system." Ex. 1001 (918 Patent) at 8:10-16.

69. The 918 Patent describes embodiments wherein "[t]he controller backs up the volatile memory using the non-volatile memory in the event of a trigger condition." Ex. 1001 (918 Patent) at 20:21-22. It lists "trigger conditions" including "a power failure, power reduction, request by the host system, etc." Ex. 1001 (918 Patent) at 20:23-24. It further describes that the trigger condition can occur when the memory system detects that the system voltage is above or below a certain threshold. Ex. 1001 (918 Patent) at 24:23-33.

70. Figure 12 of the 918 Patent depicts an exemplary memory system of the invention:

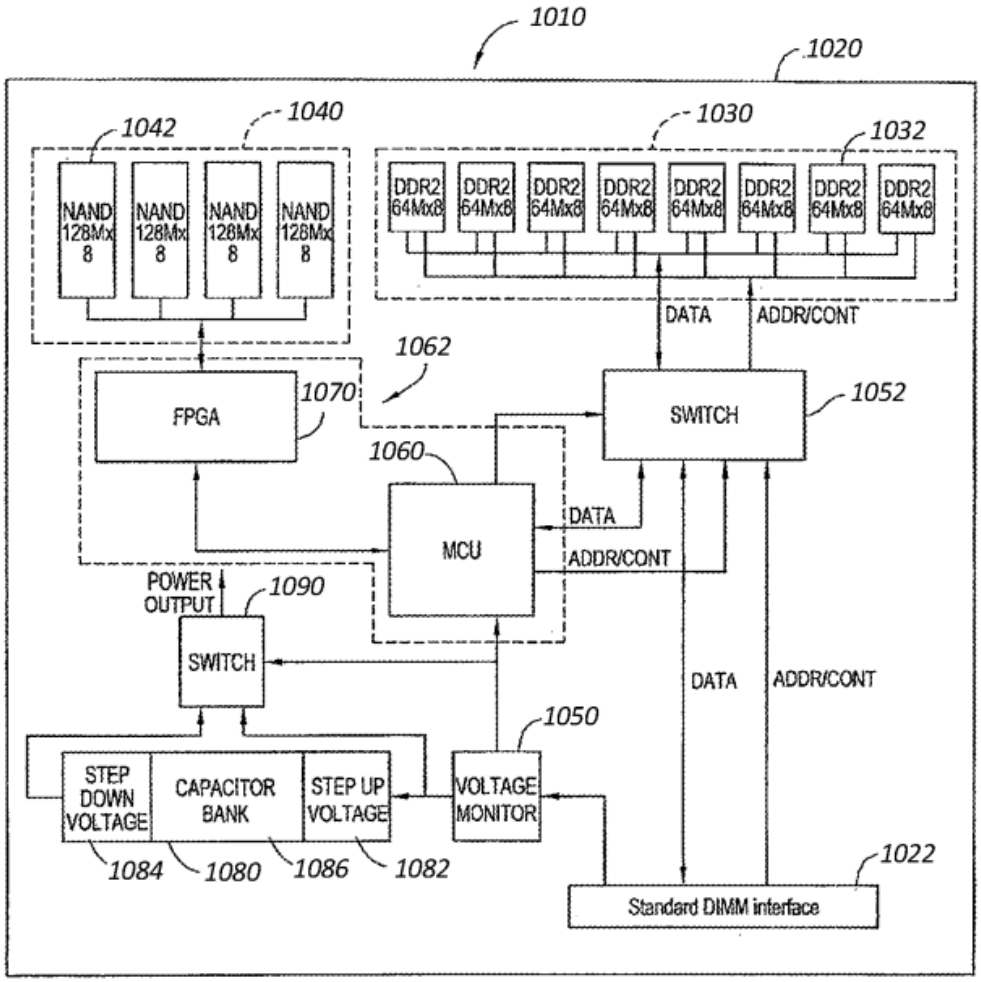


FIG. 12

Ex. 1001 (918 Patent) at FIG. 12. With reference to figure 12, the 918 Patent describes that "[t]he memory system 1010 can be coupled to a host computer system and can include a volatile memory subsystem 1030, a non-volatile memory subsystem 1040, and a controller 1062 operatively coupled to the non-volatile memory subsystem 1040." Ex. 1001 (918 Patent) at 21:16-20. The system includes

a “second power supply 1080” comprising either “capacitors” or a “battery” to supply power during a power disruption. *Id.* at 26:8-43.

71. The volatile memory subsystem 1030 “comprises a plurality of volatile memory elements 1032.” Ex. 1001 (918 Patent) at 22:9-10. The volatile memory elements 1032 can comprise “dynamic random-access memory (DRAM) elements” including, but not limited to, “DDR, DDR2, DDR3, and synchronous DRAM (SDRAM)” elements. Ex. 1001 (918 Patent) at 22:17-22. The volatile memory elements 1032 may also comprise “other types of memory elements such as static random-access memory (SRAM).” Ex. 1001 (918 Patent) at 22:24-26.

72. The controller 1062 “may comprise a microcontroller unit (MCU) 1060 and a logic element 1070.” Ex. 1001 (918 Patent) at 24:36-37. The MCU 1060 “provides memory management for the non-volatile memory subsystem 1040 and controls data transfer between the volatile memory subsystem 30 [*sic*, 1030] and the nonvolatile memory subsystem 1040.” Ex. 1001 (918 Patent) at 24:38-41. The logic element 1070 in figure 12 is labeled as an FPGA (field-programmable gate array). Ex. 1001 (918 Patent) at FIG. 12, 23:1-3.

73. The non-volatile memory subsystem 1040 “comprises a plurality of non-volatile memory elements 1042.” Ex. 1001 (918 Patent) at 22:10-12. The non-volatile memory elements 1042 can comprise “one or more flash elements” including, but not limited to, “NOR flash, NAND flash, ONE-NAND flash, and

multi-level cell (MLC).” Ex. 1001 (918 Patent) at 22:36-40. The 918 Patent describes that the non-volatile memory subsystem 1040 may be used “as a flash ‘mirror’ to provide backup of the volatile memory subsystem 1030 in the event of certain system conditions,” i.e. trigger conditions. Ex. 1001 (918 Patent) at 24:9-16.

74. As shown in figure 12, the above-described components of the memory system 1010 reside on “a printed-circuit board (PCB) 1020.” Ex. 1001 (918 Patent) at 21:25-26. The PCB 1020 can “comprise an interface 1022 that is configured to be in electrical communication with the host system.” Ex. 1001 (918 Patent) at 21:65-67. The interface 1022 can further “comprise a plurality of edge connections” that connect to the host system. Ex. 1001 (918 Patent) at 22:1-3. The interface 1022 “provides a conduit for power voltage as well as data, address, and control signals between the memory system 1010 and the host system.” Ex. 1001 (918 Patent) at 22:3-6.

75. The 918 Patent further describes that, in some embodiments, “the memory system 1010 includes at least one circuit 1052 configured to selectively operatively decouple the controller 1062 from the volatile memory subsystem 1030.” Ex. 1001 (918 Patent) at 21:20-23. It further describes that, in some embodiments, “the at least one circuit 1052 comprises one or more switches coupled to the volatile memory subsystem 1030, to the controller 1062, and to the

host computer." Ex. 1001 (918 Patent) at 23:28-32. These switches "respon[d] to signals (e.g., from the controller 1620) to selectively operatively decouple the controller 1062 from the volatile memory subsystem 1030 and to selectively operatively couple the controller 1062 to the volatile memory subsystem 1030." Ex. 1001 (918 Patent) at 23:32-40.

76. As depicted in figure 12, the memory system 1010 may also include a "voltage monitor 1050" which "monitors the voltage supplied by the host system via the interface 1022." Ex. 1001 (918 Patent) at 25:8-10. The 918 Patent describes that "upon detecting a low voltage condition," the voltage monitor 1050 "may transmit a signal to the controller 1062 indicative of the detected condition." Ex. 1001 (918 Patent) at 25:11-15. The controller 1062 can then respond to the signal by "transmitting a signal to the at least one circuit 1052 to operatively couple the controller [(1062)] to the volatile memory system 1030." Ex. 1001 (918 Patent) at 25:15-19. This process can result in the execution of a write cycle whereby "data is read from the volatile memory subsystem 1030 and is transferred to the non-volatile memory subsystem 1040 via the MCU 1060." Ex. 1001 (918 Patent) at 25:20-27.

77. Figure 15A of the 918 patent depicts a registered DIMM subsystem of the volatile memory subsystem 1030:

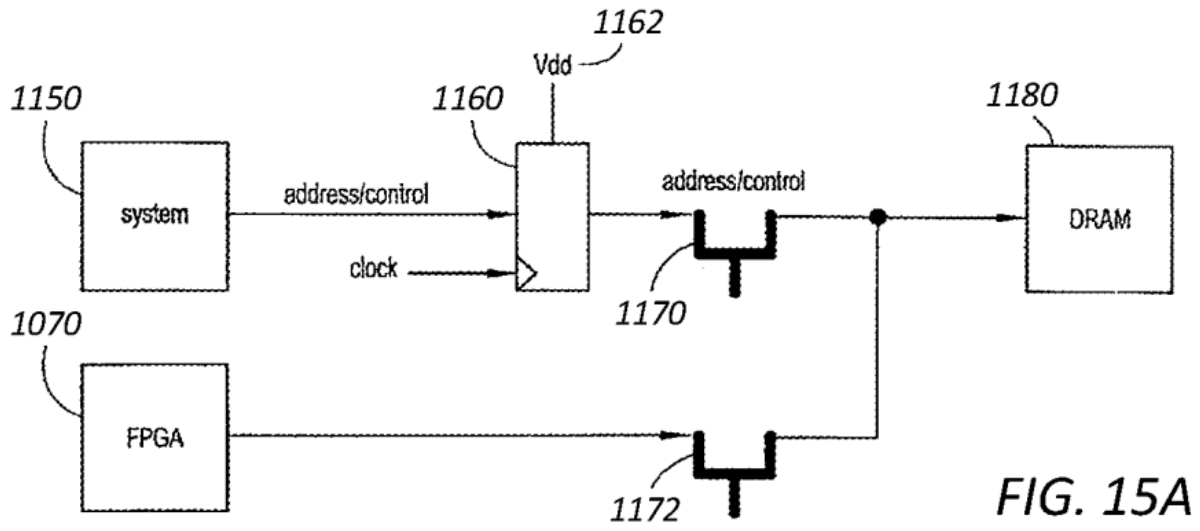


FIG. 15A

Ex. 1001 (918 Patent) at FIG. 15A, 23:41-42. In reference to figure 15A, the 918 patent describes that the registered DIMM subsystem comprises "one or more registers 1160 and a plurality of DRAM elements 1180." Ex. 1001 (918 Patent) at 23:42-44. The registered DIMM subsystem can also comprise "one or more switches 1170 coupled to the one or more registers 1160 and to the plurality of DRAM elements 1180," which "can be selectively switched, thereby selectively operatively coupling the volatile memory subsystem 1030 to the host system." Ex. 1001 (918 Patent) at 23:51-56.

78. Figure 16 of the 918 Patent depicts an exemplary power module of the memory system:

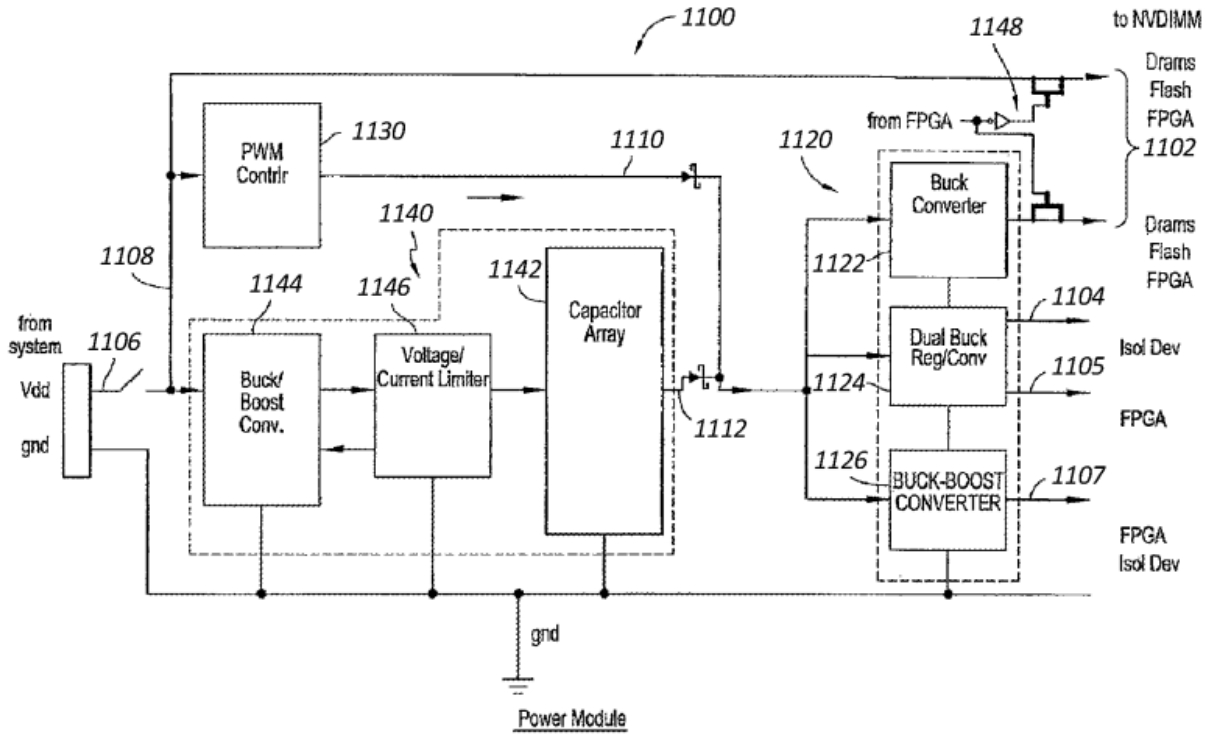
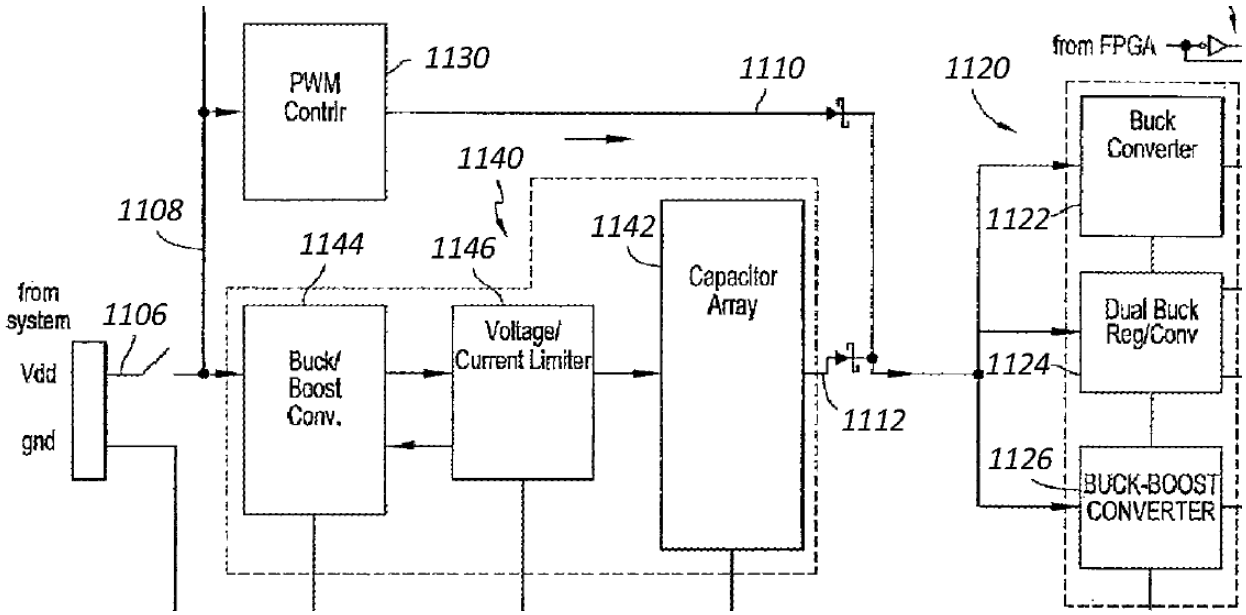


FIG. 16

Ex. 1001 (918 Patent) at FIG. 16. The power module 1100 depicted in figure 16, "provides power to the various components of the memory system 1010 using different elements based on a state of the memory system 1010 in relation to a trigger condition." Ex. 1001 (918 Patent) at 27:61-65. Specifically, the 918 Patent describes that "[t]he power module 1100 provides a plurality of voltages to the memory system 1010 comprising non-volatile and volatile memory subsystems 1030, 1040." Ex. 1001 (918 Patent) at 28:3-5. It states that "[t]he plurality of voltages comprises at least a first voltage 1102 and a second voltage 1104." Ex. 1001 (918 Patent) at 28:5-7.

79. As illustrated in figure 16, the 918 Patent describes that the power module 1100 includes block 1130 as a "first power element," block 1140 as a "second power element," and block 1120 as a "voltage conversion element." Ex. 1001 (918 Patent) at 28:7-22. As depicted in the excerpt of figure 16 below, "the first power element 1130" can "comprise a pulse-width modulation power controller."



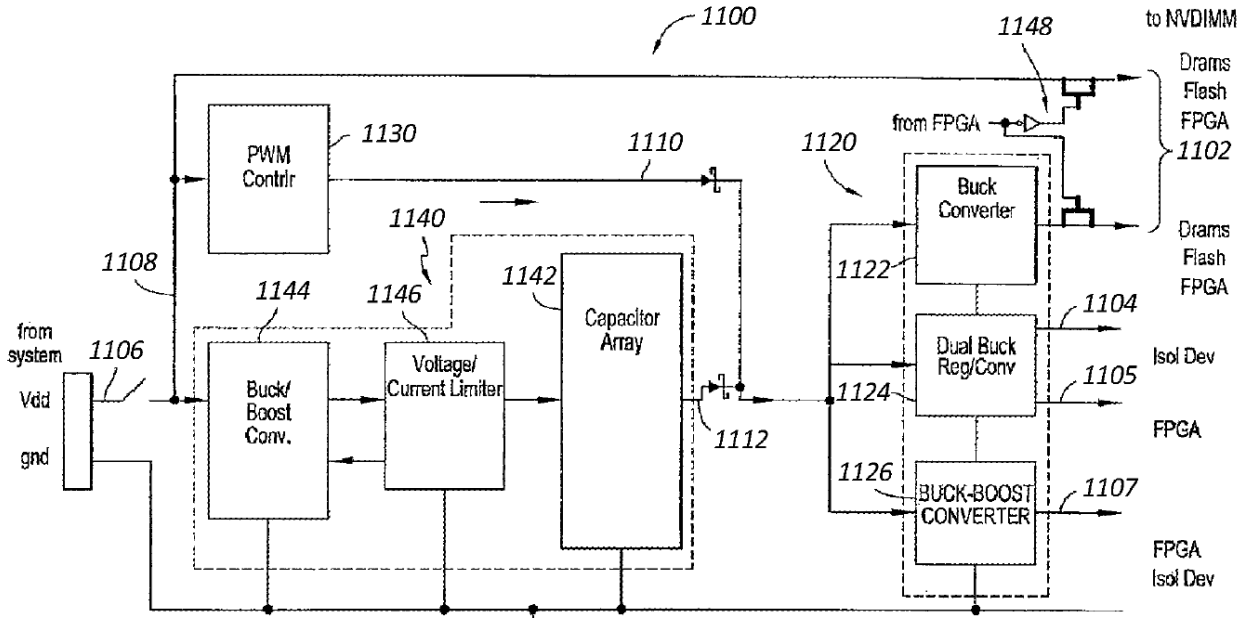
Ex. 1001 (918 Patent) at 28:13-15, FIG. 16 (excerpted). The first power element 1130 receives an input voltage, described in the patent as "the third voltage 1108." Ex. 1001 (918 Patent) at 28:18. Upon receiving the input voltage 1108, the first power element "selectively provide[s] a fourth voltage 1110 to the conversion element 1120." Ex. 1001 (918 Patent) at 28:11-13. For example, the patent describes that the first power element 1130 can "receive a 1.8V input system

voltage as the third voltage 1108" and "output a modulated 5V output as the fourth voltage 1110." Ex. 1001 (918 Patent) at 28:15-19.

80. As depicted in the excerpt of figure 16 above, "the second power element 1140" comprises "a capacitor array 1142," "a buck-boost converter 1144," and "a voltage/current limiter 1146." Ex. 1001 (918 Patent) at 28:61-65. In other embodiments "a pure boost converter may be used instead of a buck-boost converter." Ex. 1001 (918 Patent) at 29:14-16. Additionally, "only one capacitor may be used instead of a capacitor array 1142." Ex. 1001 (918 Patent) at 29:16-17. The second power element 1140 receives the same input voltage as the first power element (1108 as shown in figure 16). Ex. 1001 (918 Patent) at FIG. 16, 29:3-6. Upon receiving the input voltage 1108, the second power element 1140 "selectively provide[s] a fifth voltage 1112 to the conversion element 1120." Ex. 1001 (918 Patent) at 28:21-22. For example, the patent describes that the "the buck-boost converter 1144 receives a 1.8V system voltage (first voltage 1108) and boosts the voltage to 4.3V which is outputted to the voltage current limiter 1146." Ex. 1001 (918 Patent) at 29:3-6. The voltage current limiter "limits the current going to the capacitor array 1142 to 1A and stops charging the array 1142 when it is charged to 4.3V." Ex. 1001 (918 Patent) at 29:6-9.

81. The 918 Patent describes generally that "[t]he conversion element 1120" can comprise "one or more buck converters and/or one or more buck-boost

converters." Ex. 1001 (918 Patent) at 29:18-19. As shown in the excerpt of figure 16 below, the conversion element 1120 may contain "a plurality of sub-blocks 1122, 1124, 1126."



Ex. 1001 (918 Patent) at FIG. 16 (excerpted). The sub-blocks can comprise "various converter circuits such as buck-converters, boost converters, and buck-boost converter circuits for providing various voltage values to the memory system 1010." Ex. 1001 (918 Patent) at 29:20-27. Specifically, "sub-block 1122 comprises a buck converter, sub-block 1124 comprises a dual buck converter, and sub-block 1126 comprises a buck-boost converter." Ex. 1001 (918 Patent) at 29:27-31. The conversion element 1120 receives as voltage input "either the fourth voltage 1110 from the first power element 1130 or the fifth voltage 1112 from the second power element 1140." Ex. 1001 (918 Patent) at 29:33-37. The conversion element 1120

then "reduces the input to an appropriate amount for powering various components of the memory system." Ex. 1001 (918 Patent) at 29:38-39. For example, "the buck-converter of sub-block 1122 can provide 1.8V," labeled as first voltage 1102 in figure 16 (and described as a first voltage), to the volatile memory elements, the non-volatile memory elements, and the controller. Ex. 1001 (918 Patent) at 29:39-44, FIG. 16. The "sub-block 1124 can provide the second voltage 1104 as well as another reduced voltage 1105 to the memory subsystem 1010." Ex. 1001 (918 Patent) at 29:44-46. For example, "the second voltage 1104 is 2.5V and is used to power the at least one circuit 1052," and the third "voltage 1105 is 1.2V and is used to power the controller 1062." Ex. 1001 (918 Patent) at 29:46-50. And sub-block 1126 can provide a fourth "voltage 1107 to the memory system 1010." Ex. 1001 (918 Patent) at 29:50-51. For example, "the voltage 1107 may be 3.3V and may be used to power both the controller 1062 and the at least one circuit 1052." Ex. 1001 (918 Patent) at 29:51-52.

D. The Prosecution History of the 918 Patent

1. Provisional Application No. 60/941,586 (June 1, 2007)

82. The applicants filed Provisional Application No. 60/941,586, titled "Non-Volatile Memory Module," on June 1, 2007. Ex. 1005 at 1, 13. As discussed above, this application does not provide support for all of the limitations in the claims of the 918 Patent. *Supra* ¶¶ 49-61.

2. Application No. 12/131,873 (June 2, 2008) (abandoned)

83. The applicants filed U.S. Patent Application No. 12/131,873, titled "Non-Volatile Memory Module," on June 2, 2008. Ex. 1006 at 1. The 873 Application claims benefit of the 586 Provisional Application, filed on June 1, 2007. *Supra* Section III.D.1. The 873 Application presented 54 claims at filing, 1-54. Ex. 1006 at 33-40. As discussed above, this application does not provide support for all of the limitations in the claims of the 918 Patent. *Supra* ¶¶ 62-66.

84. On September 16, 2008, the applicants of the 873 Application filed a Preliminary Amendment, cancelling claims 21-54. Ex. 1006 at 67-71.

85. The applicants subsequently abandoned the 873 Application. Ex. 1006 at 96.

3. Application No. 12/240,916 ('833 Patent)

86. The applicants filed U.S. Patent Application No. 12/240,916 ("916 Application"), titled "Non-Volatile Memory Module," on September 29, 2008. Ex. 1007 at 61. The 916 Application is a continuation of the 873 Application, filed on June 2, 2008, and claims benefit of the 586 Provisional Application, filed on June 1, 2007. *Supra* Sections III.D.1-III.D.2. The 916 Application presented 54 claims at filing, 1-54. Ex. 1007 at 35-43.

87. On March 31, 2011, the examiner issued an Office Action subjecting claims 1-54 to a restriction and/or election requirement as being drawn to four distinct inventions. Ex. 1007 at 120-123.

1) First Invention: "Claims 1-20, and 43-49, drawn to a non-volatile and a volatile memory systems." *Id.* at 120.
2) Second Invention: "Claims 21-26, drawn to a power module for a volatile and non-volatile memory including a voltage conversion element." *Id.*
3) Third Invention: "Claims 37-42, drawn to non-volatile and a volatile memory systems wherein the memory systems operate at different frequencies depending on the mode of operation." *Id.*
4) Fourth Invention: "Claims 50-54, drawn to restoring data." *Id.*

88. On May 20, 2011, the applicants of the 916 Application filed a Preliminary Amendment in response to the restriction requirement, withdrawing claims 1-36 and 43-54 and electing to prosecute only the third invention identified by the examiner, including claims 37-42. Ex. 1007 at 125-133. The applicants made this election without traverse. *Id.* at 133.

89. In my opinion, the claims of the 918 Patent differ from the "Third Invention" that was elected for prosecution in the 916 Application (which later issued as the '833 Patent, as discussed below). For example, the "Third Invention"

requires that "the memory systems operate at different frequencies depending on the mode of operation," which is not a limitation found in any of the claims of the 918 Patent.

90. On July 29, 2011, the examiner rejected claims 37-42 as being obvious over Li et al. [US 6,336,174] in view of Oshikiri [US 2007/0192627]. Ex. 1007 at 141-147.

91. On October 18, 2011, the applicants of the 916 Application filed a reply to the Office Action dated July 29, 2011, adding claims 55-90 and arguing that the examiner's obviousness rejection was improper. Ex. 1007 at 169-184.

92. On February 1, 2012, the examiner issued a Final Office Action maintaining the obviousness rejection, rejecting newly added claims 61-62, 64-76, 83-84, and 86-90 as being similarly unpatentable over Li et al. in view of Oshikiri, and rejecting claims 63 and 85 as being indefinite. Ex. 1007 at 191-200. The examiner also restricted newly added claims 55-60 and 77-82 as being directed to a non-elected invention, namely "different embodiments for the claimed trigger condition." Ex. 1007 at 190-191. These restricted claims included limitations defining the trigger condition as "a drop below a voltage threshold," "a rise above a voltage threshold," and "a drop below a first voltage threshold or a rise above a second voltage threshold," among others. *Id.* at 177, 180.

93. On March 2, 2012, the applicants of the 916 Application filed a reply to the Final Office Action dated February 1, 2012, including claim amendments to overcome the obviousness and indefiniteness rejections. Ex. 1007 at 204-208, 210. Applicants also canceled claims 55-60 and 77-82 in response to the examiner's restriction. Ex. 1007 at 205, 207, 209.

94. On April 3, 2012, after a request for continued examination, the examiner issued an Office Action rejecting claims 37-42, 61-62, 64-76, 83-84, and 86-90 as being obvious over Li et al. in view of Cope [US 2008/0195806]. Ex. 1007 at 232-239. The examiner also rejected claims 38 and 72 as being indefinite. Ex. 1007 at 231-232.

95. On May 24, 2012, the applicants filed a reply to the Office Action dated April 3, 2012, including claim amendments to overcome the indefiniteness rejections. Ex. 1007 at 246-251. Applicants also argued that the obviousness rejections were improper. Ex. 1007 at 251-259.

96. On September 17, 2012, the examiner issued a Notice of Allowance, allowing claims 37-42, 61-76, and 83-90 of the 916 Application. Ex. 1007 at 288-294. The 916 Application issued as U.S. Patent No. 8,301,833 ("'833 Patent") on October 30, 2012. Ex. 1007 at 320.

97. To my knowledge, four IPR petitions have been filed against the '833 Patent, by SanDisk Corporation, Smart Modular Technologies Inc., SK hynix Inc.

et al., and Micron Technology, Inc. et al., respectively. *See* Ex. 1014; Ex. 1016; Ex. 1018; Ex. 1022. The PTAB denied institution for the first three IPR petitions. *See* Ex. 1015; Ex. 1017; Ex. 1019. The PTAB has not yet made an institution decision in response to the fourth IPR petition, which was filed on January 14, 2022. *See* Ex. 1022.

4. Provisional App No. 61/512,871 (July 28, 2011)

98. The applicants filed Provisional Application No. 61/512,871 ("871 Provisional Application"), titled "High Density DIMMs," on July 28, 2011. Ex. 1008 at 1-3, 47.

5. Application No. 13/559,476 ('831 Patent)

99. The applicants filed U.S. Patent Application No. 13/559,476 ("476 Application"), titled "Flash-DRAM Hybrid Memory Module," on July 26, 2012. Ex. 1009 at 63. The 476 application claims the benefit of the 871 Provisional Application, filed July 28, 2011, and is a continuation-in-part of the 916 Application, filed September 29, 2008, which is a continuation of the 873 Application, filed June 2, 2008, which claims the benefit of the 586 Provisional Application, filed June 1, 2007. Ex. 1009 at 237; *supra* Sections III.D.1-III.D.4. The 476 Application presented 24 claims at filing, 1-24. Ex. 1009 at 38-43.

100. On March 28, 2014, the applicants of the 476 Application filed a Preliminary Amendment, amending claims 1, 13, and 25 and cancelling claims 6-8, 10-12, 15, 17, and 20. Ex. 1009 at 141-147.

101. On May 6, 2014, the examiner issued a Notice of Allowance, allowing claims 1-5, 9, 13, 14, 16, 18, 19, and 21-24 of the 476 Application. Ex. 1009 at 151-160. However, the examiner granted a later priority date than the applicants claimed:

> [T]he inventive entity of each of the prior-filed applications is/are not the same inventive entity of the present application. Prior filed provisional application 61/512871 has single inventor, Hyun Lee (a distinct inventive entity), and prior filed CIP application 12/240916 has four inventors: Chi-She Chen, Jeffrey Solomon, Scott Milton, and Jayesh Bhakta (a different distinct inventive entity), while the present application has five inventors: Hyun Lee, Chi-She Chen, Jeffrey Solomon, Scott Milton, and Jayesh Bhakta (another different distinct inventive entity).

Ex. 1009 at 157. The examiner concluded that "[t]he priority date granted to the examination of the present application is 7/26/2012." Ex. 1009 at 157.

102. On May 16, 2014, the examiner conducted an interview with the applicant's representative after which the examiner concluded that the 476 Application is entitled to claim priority based on the 871 Provisional Application, filed July 28, 2011, and the 916 Application, filed September 29, 2008. Ex. 1009 at 212-217.

103. The 476 Application issued as U.S. Patent No. 8,874,831 ("'831 Patent") on October 28, 2014. Ex. 1009 at 312. On January 17, 2017, an IPR petition was filed against the '831 Patent by SK hynix Inc., et al. *See* Ex. 1020. On July 5, 2018, the PTAB issued a final written decision invalidating all claims of the '831 Patent. *See* Ex. 1021 at 41.

6. Application No. 14/489,269 ('830 Patent)

104. The applicants filed U.S. Patent Application No. 14/489,269 ("269 Application"), titled "Flash-DRAM Hybrid Memory Module," on September 17, 2014. Ex. 1010 at 57. The 269 Application is a continuation of the 476 Application, filed July 26, 2012, which claims the benefit of the 871 Provisional Application, filed July 28, 2011, and is a continuation-in-part of the 916 Application, filed September 29, 2008, which is a continuation of the 873 Application, filed June 2, 2008, which claims the benefit of the 586 Provisional Application, filed June 1, 2007. Ex. 1010 at 1; *supra* Sections III.D.1-III.D.5. The 269 Application presented 1 claim at filing. Ex. 1010 at 37.

105. On May 15, 2015, the applicants of the 269 Application filed a Preliminary Amendment, cancelling claim 1 and adding new claims 2-25. Ex. 1010 at 88-93.

106. On July 8, 2015, the examiner issued a Notice of Allowance, allowing claims 2-25 of the 269 Application. Ex. 1010 at 103-112. However, the examiner granted a later priority date than the applicants claimed because "[t]he disclosures of the prior-filed applications [Nos. 12/240,916, 12/131,873, and 60/941,586] fail to provide adequate support or enablement" because "the claimed feature 'data manager' . . . lacks proper antecedent basis or clear support [in the identified applications]." Ex. 1010 at 108-109. The examiner concluded that "[t]he effective priority date that the present claims are entitled to therefore becomes 7/28/2011 based upon the earliest priority claim to Non-provisional 61/512,871." Ex. 1010 at 109.

107. The 269 Application issued as U.S. Patent No. 9,128,830 on September 8, 2015. Ex. 1010 at 145.

7. Application No. 14/840,865 ('186 Patent)

108. The applicants filed U.S. Patent Application No. 14/840,865 ("865 Application"), titled "Flash-DRAM Hybrid Memory Module," on August 31, 2015. Ex. 1011 at 63. The 865 Application is a continuation of the 269 Application, filed September 17, 2014, which is a continuation of the 476

Application, filed July 26, 2012, which claims the benefit of the 871 Provisional Application, filed July 28, 2011, and is a continuation-in-part of the 916 Application, filed September 29, 2008, which is a continuation of the 873 Application, filed June 2, 2008, which claims the benefit of the 586 Provisional Application, filed June 1, 2007. Ex. 1011 at 25; *supra* Sections III.D.1-III.D.6. The 865 Application presented 1 claim at filing. Ex. 1011 at 61.

109. On April 21, 2016, the examiner rejected claim 1 on the ground of double patenting as claiming the same invention as claim 1 of U.S. Patent 9,158,684. Ex. 1011 at 100-101.

110. On October 20, 2016, the applicants of the 865 Application filed a reply to the Office Action dated April 21, 2016, cancelling claim 1 and adding claims 2-22. Ex. 1011 at 133-140.

111. On November 18, 2016, the examiner issued a Notice of Allowance, allowing claims 2-22 of the 865 Application. Ex. 1011 at 155-159. However, the examiner granted a later priority date than the applicants claimed because "[t]he disclosures of the prior-filed applications [Nos. 12/240,916, 12/131,873, and 60/941,586] fail to provide adequate support or enablement" because "the claimed feature 'data manager' . . . lacks proper antecedent basis or clear support [in the identified parent applications]." Ex. 1011 at 160-161. The examiner concluded that "[t]he effective priority date that claims 2-22 are entitled to therefore becomes

7/28/2011 based upon the earliest priority claim being that to parent application to Non-provisional 61/512,871." Ex. 1011 at 161.

112. On May 5, 2017, in response to a request for continued examination, the examiner issued an Office Action rejecting claims 2-13 and 17-22 as being anticipated by Best, [U.S. 2010/0110748 Al] and objecting to claims 10 and 14-16. Ex. 1011 at 218-228.

113. On November 06, 2017, the applicants of the 865 Application filed a reply to the Office Action dated May 5, 2017, amending claims 2, 10, and 14-17 and arguing that the examiner's anticipation-based rejection was improper. Ex. 1011 at 273-291.

114. On November 11, 2017, the examiner issued a Notice of Allowance, allowing claims 2-22 of the 865 Application. Ex. 1011 at 293-297. The 865 Application issued as U.S. Patent No. 9,928,186 on March 27, 2018. Ex. 1011 at 338.

8. Application No. 15/934,416 (abandoned)

115. The applicants filed U.S. Patent Application No. 15/934,416 ("416 Application"), titled "Flash-DRAM Hybrid Memory Module," on March 23, 2018. Ex. 1012 at 76. The 416 Application is a continuation of the 865 Application, filed August 31, 2015, which is a continuation of the 269 Application, filed September 17, 2014, which is a continuation of the 476 Application, filed July 26, 2012,

which claims the benefit of the 871 Provisional Application, filed July 28, 2011, and is a continuation-in-part of the 916 Application, filed September 29, 2008, which is a continuation of the 873 Application, filed June 2, 2008, which claims the benefit of the 586 Provisional Application, filed June 1, 2007. Ex. 1012 at 19; *supra* Sections III.D.1-III.D.7. The 416 Application presented 1 claim at filing. Ex. 1012 at 55.

116. On March 21, 2019, the examiner rejected claim 1 on the ground of double patenting as claiming the same invention as claim 1 of U.S. Patent 9,928,186. Ex. 1012 at 203.

117. On July 22, 2019, the applicants of the 416 Application filed a reply to the Office Action dated March 21, 2019, cancelling claim 1 and adding claims 2-21. Ex. 1012 at 249-255. On August 26, 2019, the applicants filed supplemental amendments to the claims. Ex. 1012 at 262-269.

118. On October 15, 2019, the examiner filed a Final Office Action, rejecting claims 6-8, 13-17, and 21 for failing to comply with written description requirement. Ex. 1012 at 275-277. The examiner also rejected claims 2-5, 9-12, and 18-19 as either anticipated by Fukuzo [US 2006/0294295 A1] or obvious over Fukuzo in view of Shiota et al. [US 2003/0147297 Al]. Ex. 1012 at 277-282.

119. On March 12, 2020, after a request for continued examination, the applicants filed a reply to the Office Action dated October 15, 2019, amending

claim 2 and arguing that examiner's rejections were improper. Ex. 1012 at 307-318.

120. On April 2, 2020, the examiner filed an Office Action, rejecting claims 6-8, 13-17, and 21 for failing to comply with written description requirement. Ex. 1012 at 331-332. The examiner also rejected claims 2-5, 9-12, and 18-19 as either anticipated by Fukuzo [US 2006/0294295 A1] or obvious over Fukuzo in view of Shiota et al. [US 2003/0147297 Al]. Ex. 1012 at 324-340.

121. On October 2, 2020, the applicants filed a reply to the Office Action dated April 2, 2020, amending claims 2-21 and arguing that the examiner's anticipation/obviousness rejections were improper. Ex. 1012 at 377-390.

122. On January 1, 2021, the examiner filed a Final Office Action, rejecting claims 2, 6-7, 10, 12, 17, and 19 as anticipated by Bonella et al. [US 2007/0136523 Al], claims 3-5, 11, and 15 as obvious over Bonella et al. in view of Prete et al. [US 2008/0126624 Al], claims 8 and 16 as obvious over Bonella et al. in view of Randell et al. [US 2005/0183472 A1] [*sic*, U.S. Patent No. 8,086,788], and claims 9, 13-14, 18, and 20-21 as obvious over Bonella et al. in view of Kita [US 2005/0144418 A1]. Ex. 1012 at 397-413.

123. The applicants subsequently abandoned the 416 Application. Ex. 1012 at 454-455.

9. Application No. 17/138,766 ('918 Patent)

124. The applicants filed U.S. Patent Application No. 17/138,766 ("766 Application"), titled "Flash-DRAM Hybrid Memory Module," on December 30, 2020. Ex. 1002. The 766 Application is a continuation of the 416 Application, filed March 23, 2018, which is a continuation of the 865 Application, filed August 31, 2015, which is a continuation of the 269 Application, filed September 17, 2014, which is a continuation of the 476 Application, filed July 26, 2012, which claims the benefit of the 871 Provisional Application, filed July 28, 2011, and is a continuation-in-part of the 916 Application, filed September 29, 2008, which is a continuation of the 873 Application, filed June 2, 2008, which claims the benefit of the 586 Provisional Application, filed June 1, 2007. Ex. 1002 at 29; *supra* Sections III.D.1-III.D.8. The 766 Application presented 30 claims at filing, 1-30. Ex. 1002 at 104-110.

125. On March 2, 2021, the examiner issued an Office Action rejecting claims 1-15 and 21 as being indefinite and allowing claims 1-16 and 22-30. Ex. 1002 at 137-143.

126. On March 11, 2021, the applicants of the 766 Application filed a reply to the Office Action dated March 2, 2021, amending claims 1 and 21 to recite "a first one of the second and fourth voltage amplitudes is less than ~~the other~~a second one of the second and fourth voltage amplitudes." Ex. 1002 at 166.

127. On March 24, 2021, the examiner issued a Notice of Allowance, allowing claims 1-30 of the 766 Application. Ex. 1002 at 284-288. The 766 Application issued as U.S. Patent No. 11,016,918 on May 25, 2021. Ex. 1002 at 450.

E. Construction of Terms Used in the 918 Patent Claims

128. I understand that claim terms should be given their ordinary and accustomed meaning as understood by one of ordinary skill in the art in view of the patent and its file history. For purposes of my analysis below, I do not believe that any of the claims of the 918 Patent require an explicit claim construction. While I understand that Patent Owner appears to have interpreted some of the claim terms broadly for purposes of infringement, *see*, *e.g.*, Ex. 1071 at 39-46; Ex. 1073 at 46-63, and that a narrower interpretation may be more reasonable, in my opinion the claims are obvious under either interpretation, as shown by my analysis below.

IV. OVERVIEW OF THE PRIOR ART

A. Prior Art

1. U.S. Patent Publication No. 2006/0174140 to Harris (Ex. 1023)

129. U.S. Patent Publication No. 2006/0174140 to Harris ("Harris"), titled "Voltage Distribution System and Method for a Memory Assembly," was published on August 3, 2006 and relates to U.S. Patent Application No. 11/047,304 filed on January 31, 2005. Ex. 1023 at 1. Harris was not cited during prosecution of

the 918 Patent. *See* Ex. 1001 at 2-3 ("U.S. PATENT DOCUMENTS"). Harris discloses a memory assembly module including an on-board voltage regulator module to convert an externally supplied voltage to appropriate local voltage levels. *Id.* at Abstract. Figure 1A illustrates such a memory module.

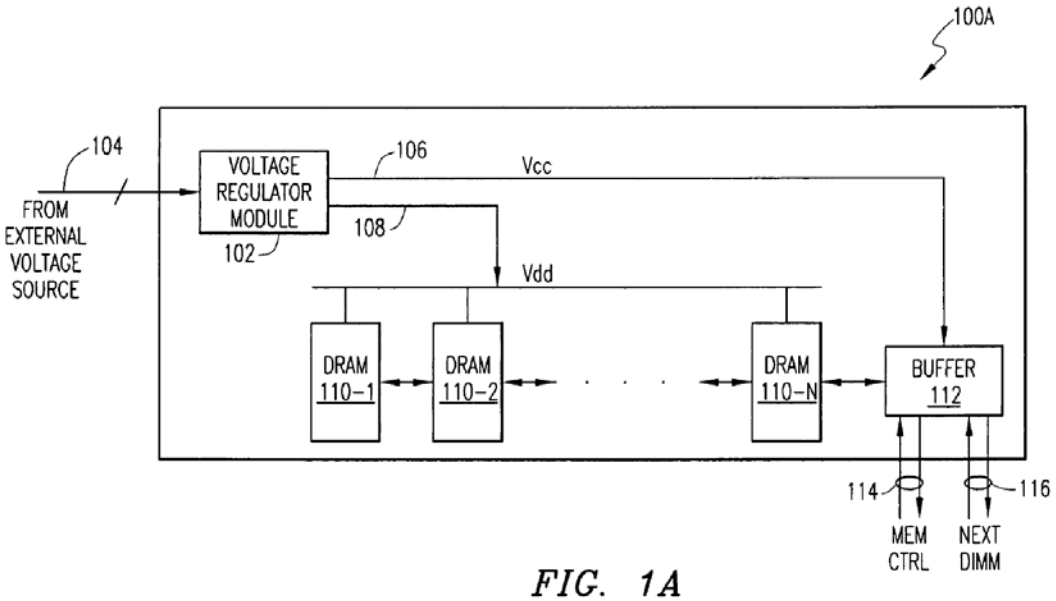


FIG. 1A

Id. at Fig. 1A. The memory module 100A connected to an input voltage path from an external voltage source (104), a bidirectional memory controller interface path (114), and a daisy-chain interface (116). *Id.* at [0009], Fig. 1A. A voltage regulator module (102), or VRM, is provided on-board the memory module 100A to convert the externally supplied voltage (104) into the appropriate local voltage levels. *Id.* at [0010], Fig. 1A. As shown in Figure 1A above, VRM (102) outputs Vcc (106) and Vdd (108). *Id.* Vcc (106) is provided to a buffer (112), and Vdd (108) is provided

to dynamic random access memory (DRAM) devices (110-1 to 100-N). *Id.*, [0009], Fig. 1A.

130. Harris explicitly contemplates implementations using any one of several common and known memory technologies. For example, Harris explains that one benefit of its power supply solution is DRAM technology independence. *Id.* at [0011]. That technology expressly includes DDR2, DDR3, and DDR4. *Id.* Harris also explains that local supply voltage conversion for a memory module can be implemented in a form factor with a component height compatible with applicable Joint Electron Device Engineering Counsel (JEDEC) standards. *See id.* at [0013]. In addition to implementations for various standard DRAM technologies, Harris explains that its memory module can be an unbuffered DIMM, registered DIMM (RDMM), or fully buffered DIMM (FBD). *See id.* at [0009]. As explained below and above, *supra* ¶ 67, a Skilled Artisan would have been familiar with these well-known technologies and the corresponding JEDEC standards.

2. U.S. Patent No. 7,724,604 to Amidi (Ex. 1024)

131. U.S. Patent No. 7,724,604 to Amidi ("Amidi"), titled "Clock and Power Fault Detection for Memory Modules," was filed on October 25, 2006, *see* Ex. 1024, and was published on May 1, 2008, *see* Ex. 1055. Amidi was not cited during prosecution of the 918 Patent. *See* Ex. 1001 at 2-3 ("U.S. PATENT DOCUMENTS").

132. Amidi discloses a system for fault detection, such as detecting voltage or power faults, that includes a "battery, battery regulation circuitry, volatile memory, memory control state machine, controller, clock detection circuit and voltage detection circuit [that] are all collectively included in a unitary memory module." Ex. 1024 at Abstract. As shown below in Figure 5 of Amidi, the power management block is provided two voltage supplies and outputs a third voltage supply.

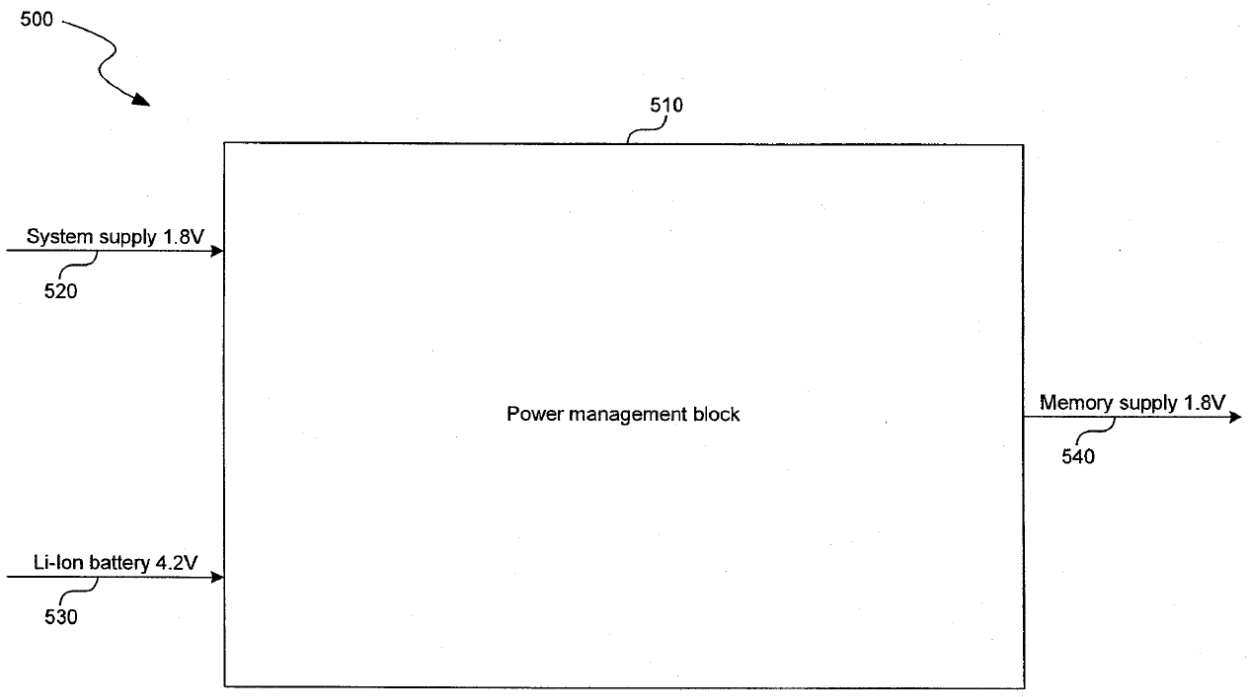


FIG. 5

Id. at Fig. 5. In particular, the system supply 520 and li-ion battery 530 are provided to the power management module 510 that outputs memory supply 540. *Id.* at 4:14-22, Fig. 5 (power management block 510). Amidi explains that the

power management block 500 ensures "a stable power supply even in the face of disruptions in system supply 520, for example." *Id.* at 4:20-22. Amidi also explains that these disruptions are detected by, for example, comparing the external power supply to a reference voltage (e.g., 3.0-volt reference for a 3.3-volt supply) to determine whether the power supply is below the reference. *See id.* at 8:23-36, Fig. 14.

3. U.S. Patent Publication No. 2006/0080515 to Spiers (Ex. 1025)

133. U.S. Patent Publication No. 2006/0080515 to Spiers ("Spiers"), titled "Non-Volatile Memory Backup for Network Storage System," was published on April 13, 2006, and relates to U.S. Patent Application No. 10/711,901 filed on October 12, 2004. Ex. 1025 at 1. Spiers was cited during prosecution of the 918 Patent but was not discussed by the applicant or the examiner in that application or any earlier applications. *See* Ex. 1001 at 3 ("U.S. PATENT DOCUMENTS"); *see generally* Ex. 1002. As shown in Figure 5 of Spiers, reproduced below, Spiers discloses a memory module (backup device 144).

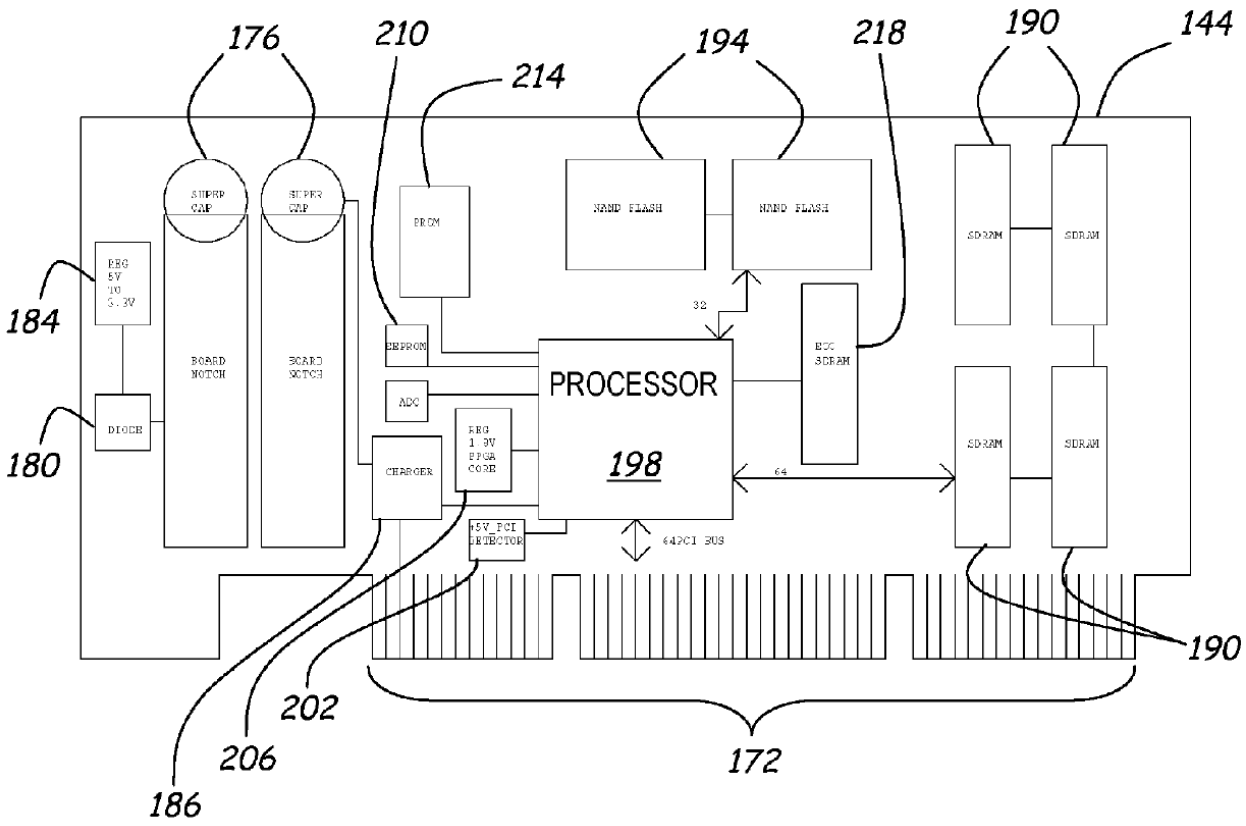


FIG.5

Id. at Fig. 5. The module includes a processor (198) for interfacing with the host computer system through an interface (connector 172), with on-board volatile memory (190 and 218), and with on-board, non-volatile memory (194). *Id.* The module also includes a temporary backup power supply (including supercapacitors 176) to provide a power source for moving data from the volatile memory to the non-volatile memory in the event of a power failure. *Id.* at [0037].

4. JEDEC Standards for Fully Buffered Dual In-Line Memory Module ("FBDIMM Standards") (Exs. 1027-28)

134. I understand that the JEDEC Solid State Technology Association published the standard Fully Buffered Dual In-Line Memory Module (FBDIMM) Advanced Memory Buffer (AMB) in March 2007 ("JESD82-20"). Ex. 1027 at Cover; *see* Ex. 1029 at ¶7. JESD82-20 was not cited during prosecution of the 918 Patent. *See* Ex. 1001 at 3-5 ("Other Publications"). In addition, I understand that the JEDEC Solid State Technology Association published the standard DDR2 SDRAM FBDIMM Design Specification in March 2007 ("JESD205"). Ex. 1028 at Cover; *see* Ex. 1029 at ¶7. JESD205 was disclosed in an IDS filed by the applicant of the 918 Patent but was not discussed by the examiner or applicant in that application or any earlier applications. *See* Ex. 1001 at 3-5 ("Other Publications"); *see generally* Ex. 1002.

135. JESD82-20 (Ex. 1027) and JESD205 (Ex. 1028) (collectively, "FBDIMM Standards") are related to each other, and cite to each other, and both concern Fully Buffered DIMMs (FBDIMMs). *See* Ex. 1027 (JESD82-20) at 5 (citing "DDR2 Fully Buffered DIMM Design Specification," which is Ex. 1028 (JESD205)). JESD82-20 concerns the "AMB" buffer on the FBDIMM, and explains that the AMB buffer "supports DDR2 SDRAM main memory" and "allows buffering of memory traffic to support large memory capacities." Ex. 1027 at p.1. The AMB interface "is responsible for handling FBD channel and

memory requests to and from the local DIMM and for forwarding requests to other DIMMs on the FBD channel." *Id.* "Fully Buffered DIMMs use commodity DRAMs isolated from the channel behind [the AMB] on the DIMM." *Id.* Similar to the 918 Patent, JESD82-20 specifies multiple supply voltages for the AMB buffer, as shown in the table below.

Power Supplies		
VCC (24 pins)	A	1.5V nominal supply for core IO
VCCFBD (8 pins)	A	1.5V nominal supply for FBD high speed IO
VDD (24 pins)	A	1.8V nominal supply for DDR IO
VSS (156 pins)	A	Ground
VDDSPD	A	3.3V nominal supply for SMB receivers and ESD diodes

Id. at p.83 (excerpt of Table 9.2). In particular, there are four voltage supplies at three different voltage amplitudes. VCC provides a 1.5-volt nominal supply for core input/output (I/O), VCCFBD provides a 1.5-volt nominal supply for high-speed I/O on the fully-buffered DIMM (FBD), VDD provides a 1.8-volt nominal supply for double-data rate (DDR) I/O, and VDDSPD provides a 3.3-volt nominal supply for system management bus (SMB or SMBus) receivers and electro-static discharge (ESD) diodes. *Id.*

136. JESD205 describes the electrical and mechanical requirements for the FBDIMM module itself (which includes the AMB buffer described in JESD82-20 discussed above). Ex. 1028 at p.9. Similar to the 918 Patent, JESD205 specifies multiple supply voltages, as shown in the table below.

Supply voltages (nominal)	min	typ	max	
	1.7	1.8	1.9	(DRAM V_{DD}/V_{DDQ}, AMB V_{DDQ})
	1.455[1]	1.5	1.575[1]	(AMB V_{CC}/V_{CCFBD})
	0.453*V_{DD}	0.5*V_{DD}	0.547*V_{DD}	(DRAM Interface V_{TT}) This supply should track as 0.5 * 1.8 volt supply
	3.0	3.3	3.6	(V_{DDSPD})

Id. at 9. In particular, there are several voltage supplies at four different voltage amplitudes. The first supply voltage listed in the table is typically 1.8 volts for V_{DD} and V_{DDQ} on the DRAM and V_{DDQ} for the AMB. The second supply voltage listed in the table is typically 1.5 volts for V_{CC} and V_{CCFBD} on the AMB. The third supply voltage listed is typically one-half of V_{DD} or 0.9 volts for V_{TT} on the DRAM interface. And the fourth supply voltage listed in the table is typically 3.3 volts for V_{DDSPD}.

5. U.S. Patent No. 6,856,556 to Hajeck (Ex. 1038)

137. U.S. Patent No. 6,856,556 to Hajeck ("Hajeck"), titled "Storage subsystem with embedded circuit for protecting against anomalies in power signal from host," was issued on February 15, 2005 and relates to U.S. Patent Application No. 10/406,805 filed April 3, 2003. Ex. 1038 at 1. Hajeck was not cited during prosecution of the 918 Patent. Ex. 1001 at 2-3 ("U.S. PATENT DOCUMENTS"). Hajeck recognizes the need to detect "anomalies" by monitoring the power input to a memory subsystem, including those with volatile and non-volatile memory. Ex. 1038 at Abstract, Fig. 1, 2:64-3:2. Hajeck also recognizes that its protection of

memory subsystems is not limited to flash memory cards, but applies to volatile memory subsystems that store data in DRAM. *See id.* at 1:10-13 ("protecting storage subsystems, such as but not limited to flash memory cards, from damage and data loss caused by irregularities in a power signal provided by a host"), 4:62-65 ("The protection circuitry and methods of the present invention may also be incorporated into other types of storage subsystems, including volatile storage subsystems that store data within DRAM or SRAM."). In particular, Hajeck discloses a voltage detection circuit 48, as shown in Figure 1 below.

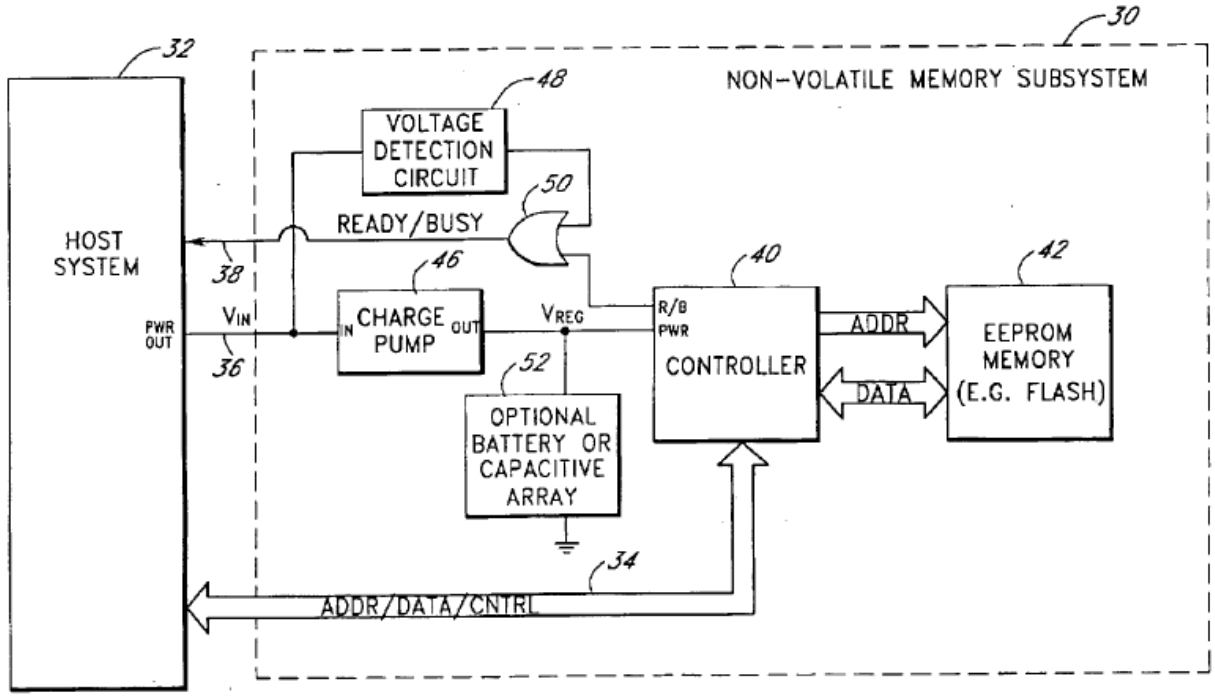


FIG. 1

Id. at Fig. 1. Hajeck explains that the circuit can be a "conventional voltage detection circuit" and is "responsible for detecting anomalies in the power signal V_{IN} supplied by the host on line 36, and for driving the ready/busy signal to the 'busy' state when such anomalies are detected." *Id.* at 3:30-34. For example, the circuit may be designed for undervoltage detection by "generat[ing] a 'busy' signal whenever V_{IN} falls below a certain level, such as 2.6 or 2.7 volts." *Id.* at 3:34-37. The circuit can also be designed for overvoltage detection by "generat[ing] a busy signal when the voltage exceeds a certain level . . . ." *Id.* at 3:37-39. In addition, Hajeck teaches that to avoid "rapid transitions between the 'ready' and 'busy' states, the voltage detection circuit may be designed to provide a degree of hysteresis, and/or to hold its output for a particular time period after a state transition." Further, Hajeck teaches how a memory subsystem continues operations for a period of time after an anomaly is detected. *See id.* at 4:10-20 ("Even if the anomaly is in the form of a complete interruption or termination of power from the host 32, the charge pump 46 continues to provide power to the controller 40 (and possibly to other active components, as mentioned above) for at least the minimum time period, T_{VREG}, needed to complete all outstanding operations. For example, if a write operation is in progress and the memory subsystem 30 has write data stored in its volatile RAM buffer (not shown), backup power will be provided for a time period sufficient for the controller 40 to finish writing this data to the EEPROM

memory 42, and if necessary, to back up any configuration data stored in volatile memory.").

B. Background Technology

1. JEDEC Standards

138. A Skilled Artisan would have been familiar with memory systems and corresponding standards, including the JEDEC standards for memory devices and memory modules at the time. *See supra* ¶ 67. For example, Harris discloses Double Data Rate (DDR) memory devices, including DDR2, DDR3 and DDR4 memories. *See* Ex. 1023 at [0009], [0011]. A Skilled Artisan would have understood that these memories were already standardized, such as DDR2 and DDR3, or were in the process of being standardized by JEDEC, such as DDR4. DDR2 and DDR3 standard JEDEC memory devices are discussed below. Harris also discloses Dual In-Line Memory Modules (DIMMs), including unbuffered DIMMs (UDIMMs), registered DIMMs (RDIMMs), and fully-buffered DIMMs (FBDs or FBDIMMs). *See* Ex. 1023 at [0009]. A Skilled Artisan would have understood that these memory modules were already standardized, including the Advanced Memory Buffers (AMB) for FBDIMMs discussed above, *supra* ¶¶134-136.

a) DDR SDRAM Specification (JESD79) (Ex. 1045)

139. I understand that the JEDEC Solid State Technology Association published the standard DDR SDRAM Specification in June 2000 ("JESD79").

Ex. 1045 at Cover. Similar to the 918 Patent, JESD79 specifies multiple supply voltages, as shown in the table below.

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage (for devices with a nominal VDD of 3.3 V)	VDD	3	3.6	V	
Supply Voltage (for devices with a nominal VDD of 2.5 V)	VDD	2.3	2.7	V	
I/O Supply Voltage	VDDQ	2.3	2.7	V	
I/O Reference Voltage	VREF	0.49*VDDQ	0.51*VDDQ	V	6
I/O Termination Voltage (system)	VTT	VREF–0.04	VREF+0.04	V	7

Id. at p.54 (excerpt of "Electrical Characteristics and DC Operation Conditions"). In particular, the nominal supply voltage VDD is 2.5 volts or 3.3 volts. The nominal input/output (I/O) supply voltage VDDQ is 2.5 volts, which is the average of the minimum voltage at 2.3 volts and maximum voltage at 2.7 volts. The nominal I/O reference voltage VREF is half of VDDQ or 1.25 volts, as is the nominal I/O termination voltage VTT.

b) DDR2 SDRAM Specification (JESD79-2B) (Ex. 1026)

140. I understand that the JEDEC Solid State Technology Association published the standard DDR2 SDRAM Specification in September 2003 ("JESD79-2B"). Ex. 1026 at Cover. Similar to the 918 Patent, JESD79-2B specifies multiple supply voltages, as shown in the table below.

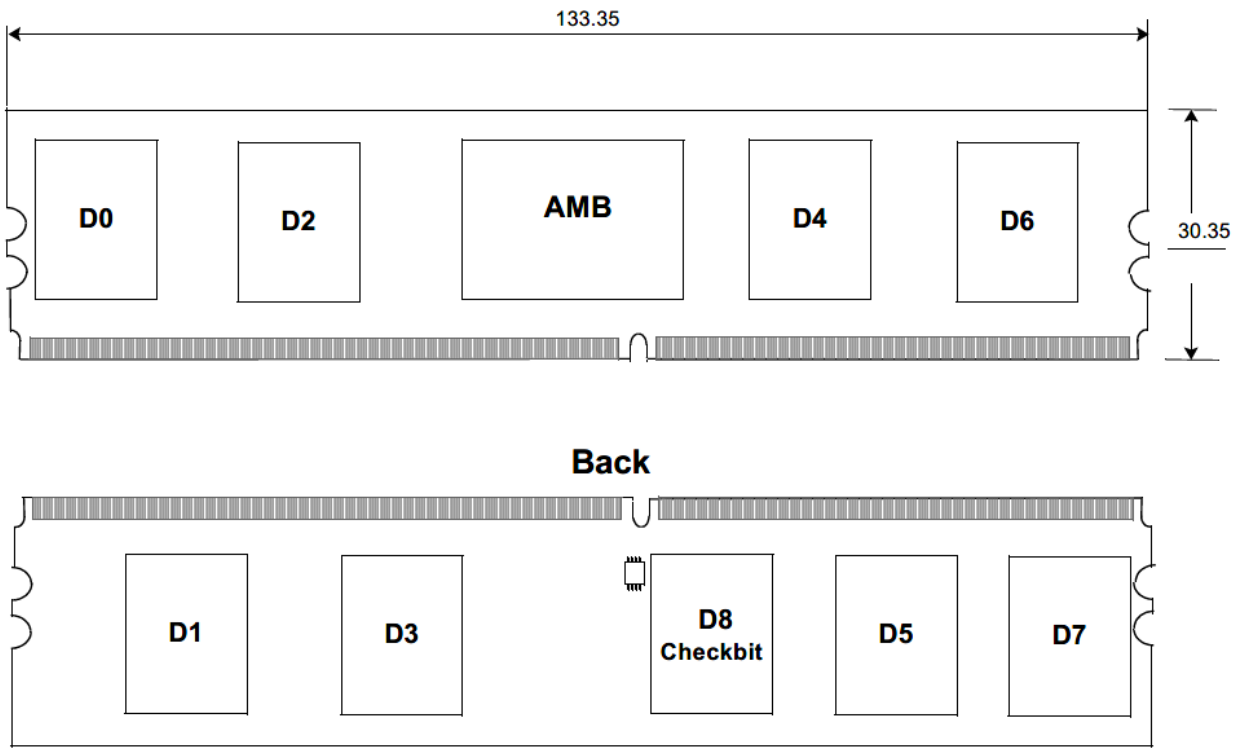
Symbol	Parameter	Rating			Units	Notes
		Min.	Typ.	Max.		
VDD	Supply Voltage	1.7	1.8	1.9	V	1
VDDL	Supply Voltage for DLL	1.7	1.8	1.9	V	5
VDDQ	Supply Voltage for Output	1.7	1.8	1.9	V	1, 5
VREF	Input Reference Voltage	0.49*VDDQ	0.50*VDDQ	0.51*VDDQ	mV	2. 3
VTT	Termination Voltage	VREF-0.04	VREF	VREF+0.04	V	4

NOTE 1 There is no specific device VDD supply voltage requirement for SSTL-1.8 compliance. However under all conditions VDDQ must be less than or equal to VDD.
NOTE 2 The value of VREF may be selected by the user to provide optimum noise margin in the system. Typically the value of VREF is expected to be about 0.5 x VDDQ of the transmitting device and VREF is expected to track variations in VDDQ.
NOTE 3 Peak to peak ac noise on VREF may not exceed +/-2% VREF (dc).
NOTE 4 VTT of transmitting device must track VREF of receiving device.
NOTE 5 VDDQ tracks with VDD, VDDL tracks with VDD. AC parameters are measured with VDD, VDDQ and VDDDL tied together

Ex. 1026 at p.49 (Table 16). In particular, there are five symbols for voltages at two different voltage amplitudes. VDD is a supply voltage typically at 1.8 volts, VDDL is a supply voltage for a delay-locked loop (DLL) typically at 1.8 volts, VDDQ is a supply voltage for output typically at 1.8 volts, VREF is an input reference voltage typically at one-half of VDDQ or 0.9 volts, and VTT is a termination voltage that is typically at VREF, or one-half of VDDQ (0.9 volts). As I noted above, Harris explicitly references standard DDR2 memory technology. *Supra* ¶130.

c) FBDIMM Standards (Exs. 1027-28)

141. As mentioned above, Harris expressly states that its memory module can be implemented as a fully-buffered DIMM (FBD or FBDIMM). *Supra* ¶¶130, 134, 136, 138. As shown in the example FBDIMM below, a Skilled Artisan would have understood that an FBDIMM includes an advanced memory buffer (AMB) and one or more memory devices (e.g., DDR2 SDRAM).



Ex. 1028 at 37; *see also id.* at 9, 13-16, 38-40. The AMB has a high-speed differential point-to-point link terminated at 1.5 volts and the DRAM uses an interface terminated at 0.9 volts. *Id.* at 9 ("Supply voltages," "Buffer Interface," and "DRAM Interface"), 13-16 (illustrating AMB device with V_{CC} termination and DRAM devices with V_{TT} termination).

a) DDR3 SDRAM Specification (JESD79-3A) (Ex. 1046)

142. I understand that the JEDEC Solid State Technology Association published revision A of the standard DDR3 SDRAM Specification in September 2007 ("JESD79-3A"). Ex. 1046 at Cover. Similar to the 918 Patent, JESD79-3A specifies multiple supply voltages, including those shown in the table below.

V_{DDQ}	Supply	DQ Power Supply: 1.5 V +/- 0.075 V
V_{SSQ}	Supply	DQ Ground
V_{DD}	Supply	Power Supply: 1.5 V +/- 0.075 V

Id. at p.13. The power supply VDD is provided at 1.5 volts +/- 0.075 volts and the power supply VDDQ is provided at 1.5 volts +/- 0.075 volts.

2. PCI Bus Standards (Ex. 1031)

143. At the time of the 918 Patent, devices utilizing the peripheral component interconnect ("PCI") local bus were well known. Accordingly, a Skilled Artisan would have been familiar with the PCI Local Bus Specification, which governed the "protocol, electrical, mechanical, and configuration specification" for such components and expansion boards. *See* Ex. 1031 at p.1.

144. For example, a Skilled Artisan would have known that the PCI Local Bus Specification established the required and optional pins for each device under the PCI standard. *See id.* at p.7, Fig. 2-1 (reproduced below).

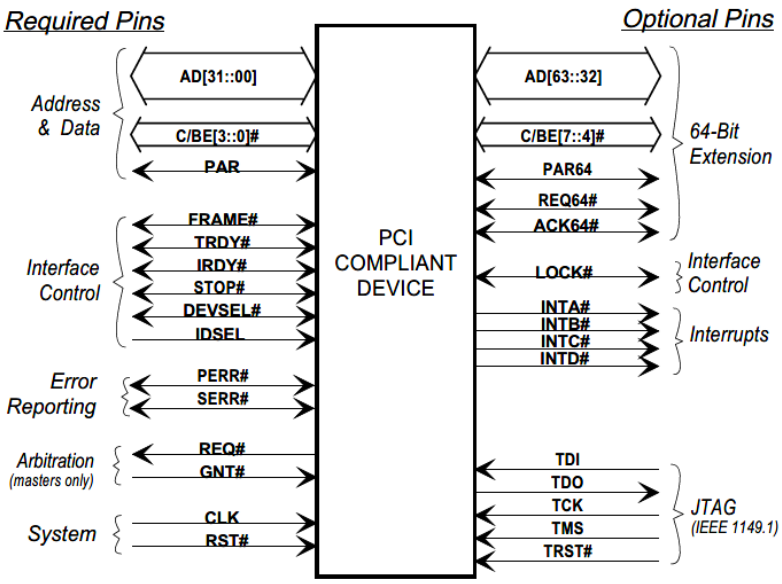


Figure 2-1: PCI Pin List

Accordingly, a Skilled Artisan would have known that all PCI devices receive, among other signals, address, data, and clock signals through pins connecting the PCI device to the host system. *See id.* at Fig. 2-1, pp.8-9.

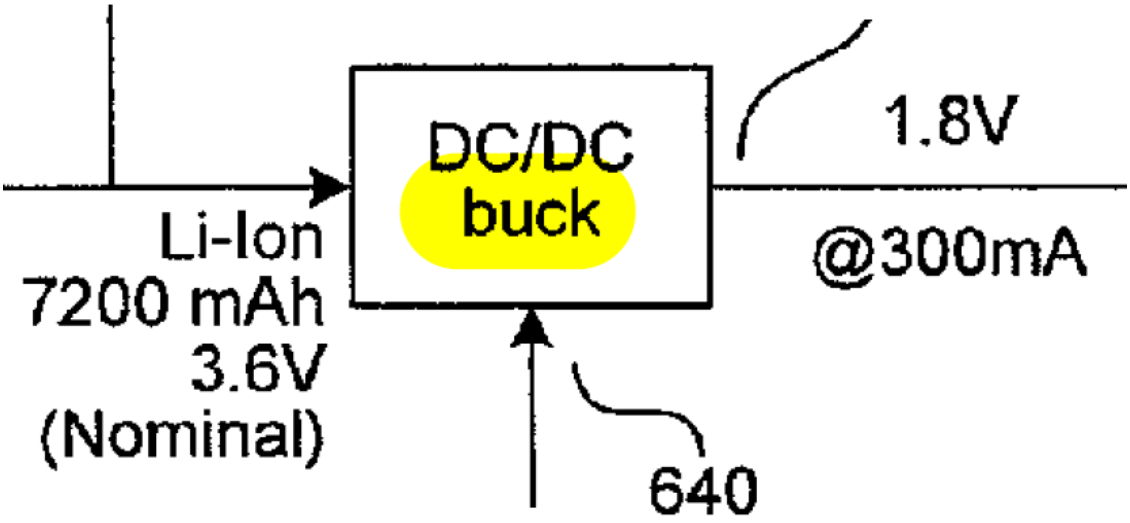
145. A Skilled Artisan would have also known that the PCI Local Bus Standard established the power requirements for PCI devices, including expansion boards. *See id.* at p.137 (discussing power requirements generally), pp.150-51 (discussing power requirements for expansion boards). In particular, the standard specifies that all PCI connectors require four power rails (+5V, +3.3V, +12V, and -12V). *See id.* at p.137. However, the standard further specifies that expansion boards can draw all of their power through the +5V or +3.3V power rails. *See id.* at p.150. Accordingly, a Skilled Artisan would have known that a PCI expansion board could be powered via the +5V input from the host system.

3. Buck Converters (Exs. 1032, 1058)

146. At the time of the 918 Patent, buck converters were well-known switching devices used to step down the voltage between its input and output. Buck converters were one of "the most basic building blocks in power electronics." EX1050 at 1:21. For example, Simplified Design of Switching Power Supplies by John D. Lenk ("Lenk") discloses that a "buck circuit is used when the input voltage is always greater than the desired output voltage (and is also known as a *step-down* converter)." Ex. 1058 at 3 (describing Fig. 1-3), 5 (Fig. 1-3). In particular, the duty cycle of the switching converter determines the output voltage relative to the input voltage. *Id.* at 5 ("1.3 Switching-Regulatory Theory") ("The output voltage V_O is always equal to the input voltage V_{IN}, times the duty cycle D, or $V_O = DV_{IN}$."). Lenk also shows that the configurations and waveforms for a theoretical buck converter were well-known to a Skilled Artisan. *See id.* at 12-16 ("1.5.4. Buck or Step-Down").

147. As another example, Power Electronics: Converters, Applications, and Design by Ned Mohan et al. ("Mohan") discloses that a step-down or buck converter is a "basic converter topolog[y]." Ex. 1032 at 161. Mohan explains that, "[a]s the name implies, a step-down converter produces a lower average output voltage than the dc input voltage V_d." *Id.* at 164. Similar to Lenk, Mohan explains that the output voltage can be controlled "[b]y varying the duty ratio." *Id.*

148. As a further example, Amidi discloses using a buck converter on a memory module to convert a higher input voltage to a lower output voltage. *See, e.g.*, Ex. 1024 at Fig. 6 (showing a DC/DC buck converter 640 to step down a higher voltage to a lower one, reproduced below in part, annotated).



149. As I explained above, a Skilled Artisan would have understood that a step-down regulated voltage can also be provided by means other than a "buck converter." *Supra* ¶53. For example, a non-switching, linear regulator, such as a low-dropout regulator (LDO) can be used to reduce the output voltage relative to the input voltage. However, a Skilled Artisan would have also understood that an LDO is substantially different from the claimed "buck converter." *See, e.g.*, Ex. 1059 at 5:23-30 ("Switch mode buck converters have become popular due to two attractive features: first, they are more efficient than traditional low drop out

regulators (LDO) (e.g., up to 95%) and second, they can provide relatively high currents with lower power dissipation on chip than an LDO can.").

C. The Combinations Relied on Here

150. The combinations analyzed here were obvious to a Skilled Artisan at the time and are straightforward applications of the teaching of the prior art. Each of the Grounds discussed below involves the combination of prior art references in view of the knowledge of a Skilled Artisan.

151. Ground 1 involves Harris in view of the FBDIMM Standards. In this combination, I discuss three voltage mappings (A, B, and C), as described below.

152. Ground 2 involves the references in Ground 1 (Harris in view of the FBDIMM Standards) in combination with Amidi, which discloses a memory module with battery backup. In this combination, I discuss four voltage mappings (A, B, C, and D), as described below.

153. Ground 3 involves the references in Ground 2 in view of Hajeck, which discloses detecting undervoltage and overvoltage conditions. Ground 3 involves the same voltage mappings as Ground 2.

154. Ground 4 involves Spiers in view of Amidi. In this combination, I discuss three voltage mappings (A, B, and C), including voltages corresponding to DDR2 or DDR3 DRAMs.

155. Ground 5 involves the references in Ground 4 in view of Hajeck, which discloses detecting undervoltage and overvoltage conditions. Ground 5 involves the same voltage mappings as Ground 4.

D. Reasons to Combine

156. A Skilled Artisan would have been motivated to make these combinations for at least the following reasons.

1. Ground 1: Harris in view of JEDEC's FBDIMM Standards

157. As mentioned above, Ground 1 involves Harris in view of the FBDIMM Standards. *Supra* ¶150.

158. A Skilled Artisan would have been familiar with memory systems and corresponding standards, including the JEDEC standards for memory devices and memory modules already standardized, or in the process of being standardized, at the time. For example, Harris discloses Double Data Rate (DDR) memory devices, including DDR2 and DDR3 memories. *See* Ex. 1023 at [0009], [0011]. A Skilled Artisan would have understood that these memories were already standardized. *Supra* ¶139 (DDR SDRAM), ¶140 (DDR2 SDRAM), ¶141 (FBDIMM), ¶142 (DDR3 SDRAM). Harris also discloses Dual In-Line Memory Modules (DIMMs), including unbuffered DIMMs (UDIMMs), registered DIMMs (RDIMMs), and fully-buffered DIMMs (FBDIMMs). *See* Ex. 1023 at [0009]. A Skilled Artisan would have understood that these memory modules were already standardized,

including FBDIMMs with an Advanced Memory Buffer (AMB). *See id.*; *see also* Ex. 1027, Ex. 1028.

159. Similarly, the 918 Patent discloses widely-known JEDEC standards. For example, the background of the 918 Patent references a "JEDEC standard DRAM DIMM." Ex. 1001 at 3:42-43; *see also id.* at 3:12-13 ("form factor of a standard DIMM"), 17:59-61 ("standard access protocol, such as JEDEC's DDR DRAM"). The 918 Patent also references specific standards, "such as DDR, DDR2, DDR3, DDR4" (*id.* at 13:42-43), and connectors, such as "a standard 240-pin DDR2 edge connector" (*id.* at 22:7-8).

160. Like the 918 Patent, Harris discloses that its memory module with on-board voltage conversion can be implemented in a form factor that is compatible with JEDEC standards. *Supra* ¶129; *see* Ex. 1023 at Abstract, Fig. 1A, [0009], [0011], [0013]. Indeed, Harris discloses different types of standard memory devices (e.g., DDR2, DDR3, and DDR4) and standard memory modules (e.g., UDIMM, RDIMM, FBDIMM). *Id.* The JEDEC standards describe requirements for many aspects of memory modules and devices, including for the voltage supply of JEDEC-compliant devices. In fact, Harris expressly discloses "industry standard memory modules" and such "power requirements." Ex. 1023 at [0002], [0012] (describing power supply rails for standard modules). Harris also teaches generating appropriate local voltage levels for powering memory devices and

buffer circuits on the memory module. *See, e.g., id.* at Abstract ("A memory assembly module including an on-board voltage regulator for converting an externally supplied voltage into appropriate local voltage levels for powering memory devices of the memory assembly module."), [0009] ("a Vdd path, that may be energized to appropriate voltage levels depending on the type, functionality, and design of the memory devices" and "the Vcc path may be energized to appropriate voltage levels depending on the buffer and DIMM technology"). Thus, a Skilled Artisan implementing the memory module teachings of Harris would have done so in view of this knowledge as evidenced by the relevant JEDEC memory standards.

161. In my view, a Skilled Artisan would have been familiar with the relevant JEDEC memory standards, including the FBDIMM Standards. Even if one were to argue that Harris does not sufficiently disclose a memory module in accordance with the teachings of these JEDEC memory standards or that a Skilled Artisan would not be familiar with the FBDIMM Standards, it would have been obvious to a Skilled Artisan, who would have been motivated to implement Harris's module using memory devices and/or buffer devices standardized by JEDEC, including the FBDIMM Standards, as explained below.

162. Harris expressly refers to JEDEC and describes JEDEC-standardized memory. *Supra* ¶157. Such memory standards were widely-recognized and used to

implement memory at the time and standard memory devices compliant with the JEDEC standards were readily available as well. In particular, a Skilled Artisan would have been motivated to combine Harris with the FBDIMM Standards. *See generally* Exs. 1027, 1028. Harris expressly contemplates implementing its module as an FBDIMM, which includes an AMB (buffer). Ex. 1023 at [0009] ("[T]he DIMM configuration of an exemplary memory module may include . . . fully buffered DIMMs (FBDs) . . . ."), [0012] (providing an example of a "standard FBD module").

163. In fact, Harris provides embodiments that relate to an FBDIMM. For example, as shown in Figure 1A below, the DIMM 100A includes a buffer 112 that receives voltage supplies through a Vcc path and is coupled to a bidirectional memory controller interface path 114 and daisy-chain interface 116. *Id.* at Fig. 1A, [0009] ("bidirectional memory controller interface path 114 as well as a second voltage path 106, typically referred to as a V_{CC} path, are provided with respect to the buffer component 112 , wherein the V_{CC} path may be energized to appropriate voltage levels depending on the buffer and DIMM technology" and "a suitable daisy-chain interface 116 is provided for coupling the buffer component 112 to a next memory module").

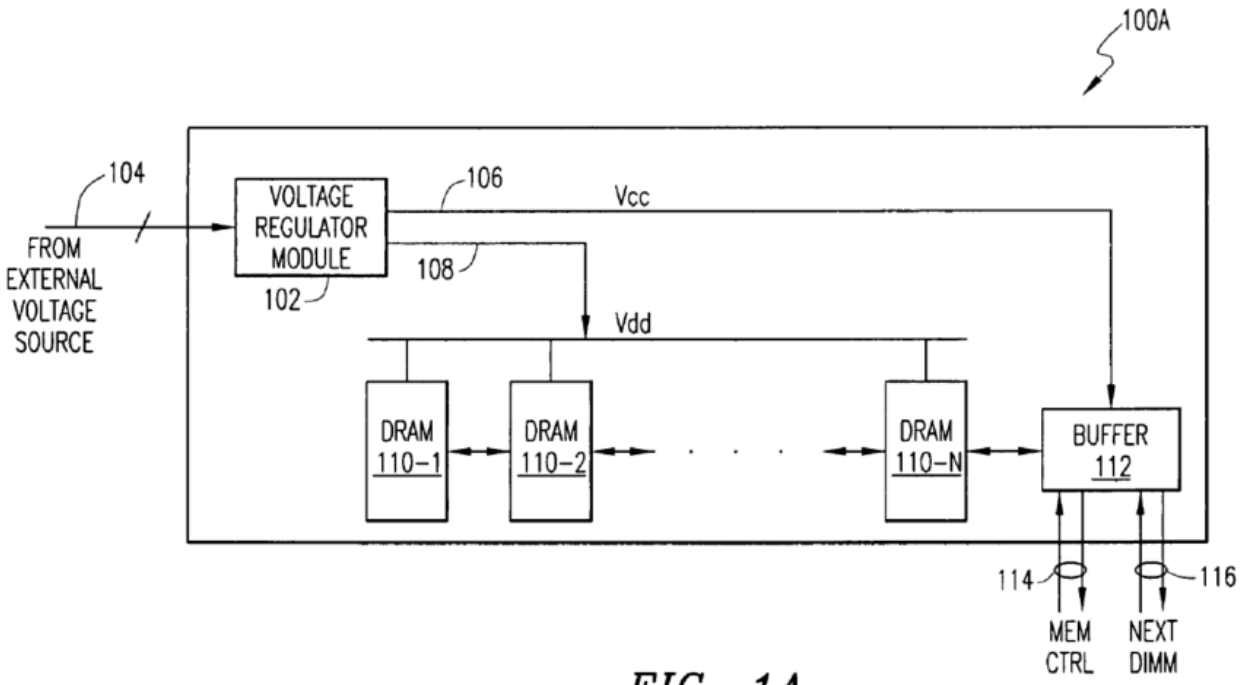


FIG. 1A

Harris explains that the buffer is provided for buffering command, address, and data signals for the memory devices—a function of FBDIMMs that a Skilled Artisan would have recognized. *Id.* at [0009] ("In the illustrated embodiment of FIG. 1A, for instance, the DIMM configuration of the memory module 100A is exemplified as a fully buffered DIMM wherein a buffer/logic component 112 is provided for buffering command/address (C/A) space as well as data space at least for a portion of the memory devices 110-1 through 110-N").

164. As another example of FBDIMMs, Figure 3 of Harris is a block diagram of a memory assembly 300 with daisy-chained memory boards 306-1 through 306-M.

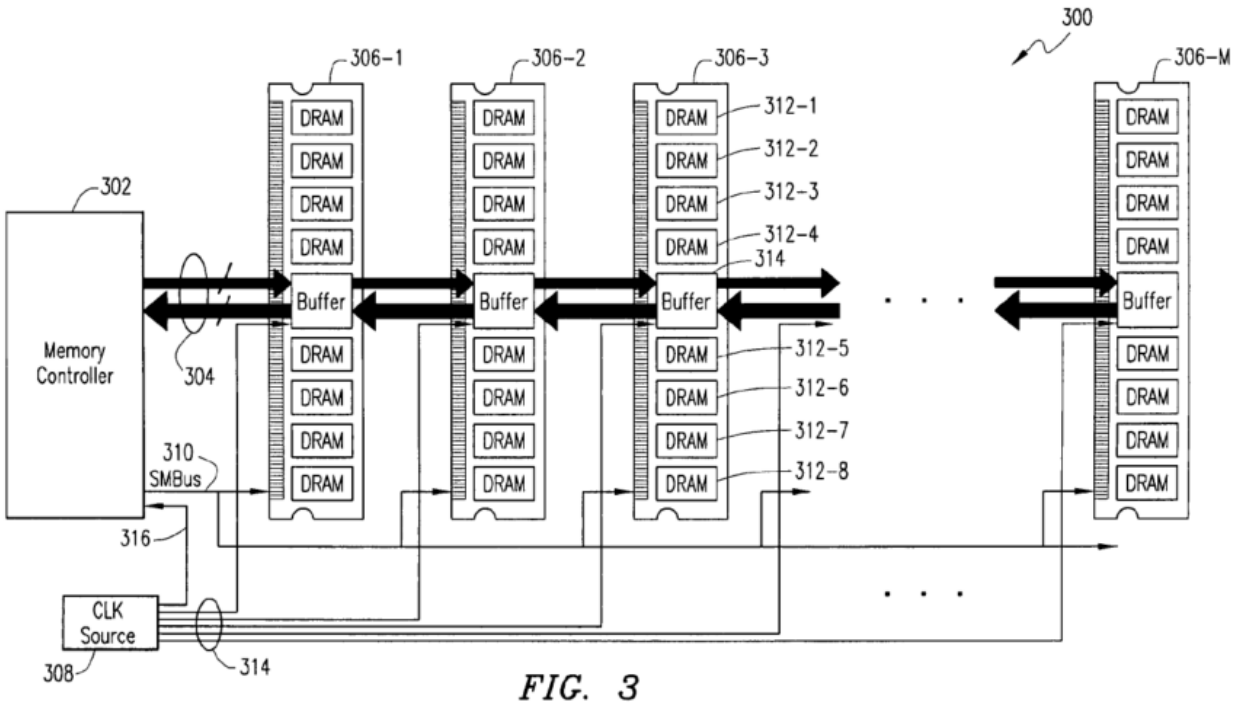


FIG. 3

Ex. 1023 at Fig. 3, [0017]. As shown, memory boards 306 include buffers 314 that are daisy-chained together by a bidirectional memory link. *See id.* Again, this is a feature of FBDIMMs that a Skilled Artisan would have recognized. Accordingly, a Skilled Artisan would have looked to the FBDIMM Standards to implement the memory module teachings of Harris to create an FBDIMM with an AMB buffer. In addition to this explicit motivation in Harris, using the FBDIMM Standards to implement an FBDIMM with an AMB buffer is a predictable variation to a Skilled Artisan given that the AMB standard was well-known in the field of memory technology that was readily available at the time in a cost-effective manner for daisy-chain topologies. *See, e.g.*, Ex. 1027 (JESD82-20) at p. 1 ("The Advanced Memory Buffer allows buffering of memory traffic to support large memory

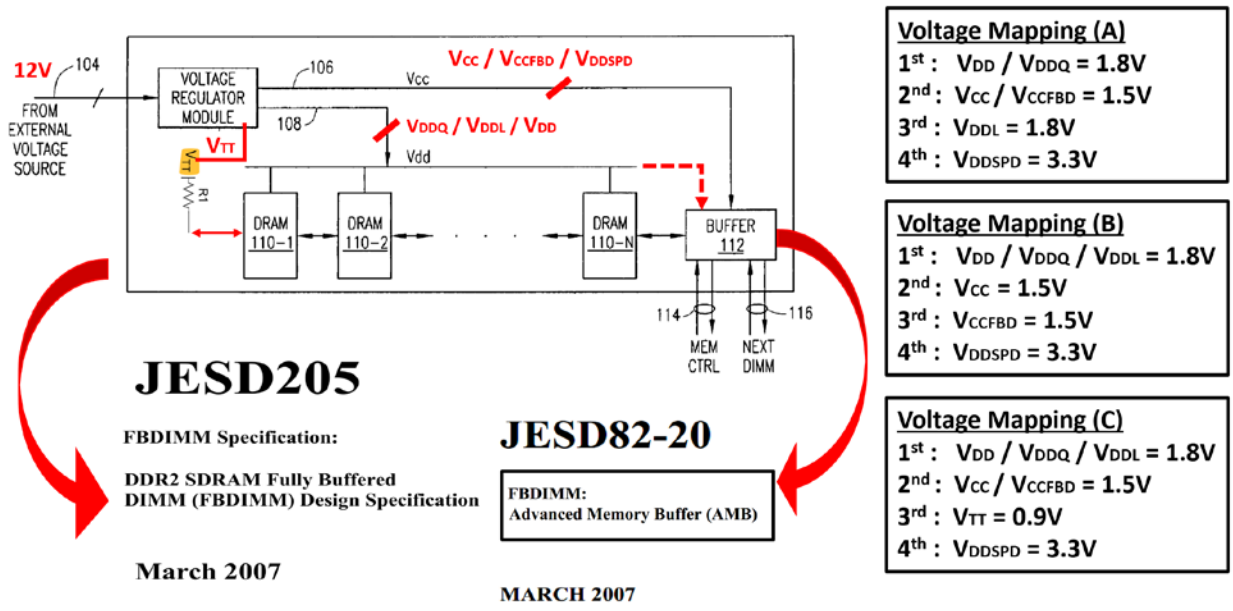
capacities. ... Fully Buffered DIMM (FBD) provides a high memory bandwidth, large capacity channel solution that has a narrow host interface. Fully Buffered DIMMs use commodity DRAMs isolated from the channel behind a buffer on the DIMM."); *see also* Ex. 1060 at 1:65-2:3 (describing the desirability of "meeting JEDEC standards for synchronous DRAMs so that versatile synchronous DRAMs may be provided and applied in many design applications"). Additionally, the combination simply combines prior art elements (e.g., Harris's memory module with a standard AMB) in known ways to yield predictable results in accordance with the relevant standards (e.g., an FBDIMM-compliant memory module with on-board voltage conversion).

165. As part of the FBDIMM Standards, the JESD205 DDR2 SDRAM FBDIMM Design Specification is a document that a Skilled Artisan would have been motivated to combine with Harris. *See generally* Ex. 1028. As explained above, Harris expressly contemplates implementing its module as an FBDIMM. *Supra* ¶¶162-164; *see also* Ex. 1023 at [0009], [0012], [0017], Figs. 1A, 3. Accordingly, a Skilled Artisan would have looked to the FBDIMM Standards (including JESD205) to implement the memory module teachings of Harris for an FBDIMM, such as one with DDR2 SDRAM memory. In addition to this explicit motivation in Harris, using the FBDIMM Standards (including JESD205) to implement an FBDIMM is a predictable variation to a Skilled Artisan given that

the FBDIMM Standards were well-known in the field of memory technology and were readily available at the time in a cost-effective manner for daisy-chain topologies. *See, e.g.*, Ex. 1027 (JESD82-20) at p. 1 ("The Advanced Memory Buffer allows buffering of memory traffic to support large memory capacities. ... Fully Buffered DIMM (FBD) provides a high memory bandwidth, large capacity channel solution that has a narrow host interface. Fully Buffered DIMMs use commodity DRAMs isolated from the channel behind a buffer on the DIMM."); *see also* Zuravleff (5,630,096) Ex. 1060 at 1:65-2:3 (describing the desirability of "meeting JEDEC standards for synchronous DRAMs so that versatile synchronous DRAMs may be provided and applied in many design applications"). Additionally, the combination simply combines prior art elements (e.g., Harris's memory module satisfying the FBDIMM design specification) to yield predictable results in accordance with the relevant standards at the time (e.g., an FBDIMM-compliant memory module with on-board voltage conversion).

166. In the combination of Harris and the FBDIMM Standards, a Skilled Artisan would have understood that multiple voltage supplies would be provided to the components of the memory module for proper operation. Accordingly, at least the following three voltage mappings would have been apparent to a Skilled Artisan, as shown in the figure below with examples of voltage amplitudes for the voltage supplies.

Ground 1: Harris with JEDEC's FBDIMM Standards



Ex. 1023 (Harris) at Fig. 1A (annotated); Ex. 1027 (JESD82-20); Ex. 1028 (JESD205). As shown, a 12-volt supply from an external voltage source is provided to the FBDIMM, as disclosed by Harris. *See e.g.*, Ex. 1023 at [0012], [0013], [0016], [0020]. In accordance with JEDEC's FBDIMM Standards, Harris's Voltage Regulator Module provides several voltage supplies to the Advanced Memory Buffer (AMB, buffer 112), including VCC, VCCFBD, VDDSPD and VDD. Ex. 1023 (Harris) at [0009] ("the Vcc path may be energized to appropriate voltage levels depending on the buffer and DIMM technology"); *see also id.* at [0014] (disclosing a redundancy implementation with a "plurality of on-board VRMs"), Fig. 1B. In accordance with JEDEC's FBDIMM Standards, Harris's Voltage Regulator Module provides several voltage supplies to the memory devices (DRAM 110-1 to 110-N), including VDD, VDDL, VDDQ, and VTT. *Id.*

at [0009] ("a Vdd path, that may be energized to appropriate voltage levels depending on the type, functionality, and design of the memory devices").

167. To the extent Patent Owner argues that two different voltage amplitudes recited in the claims can have the same amplitude, voltage mapping (A) ("Ground 1A") includes four voltage supplies at four voltage amplitudes. The first voltage is VDD or VDDQ (e.g., each at 1.8 volts); the second voltage is VCC or VCCFBD (e.g., each at 1.5 volts); the third voltage is VDDL (e.g., at 1.8 volts); and the fourth voltage is VDDSPD (e.g., at 3.3 volts):

- VDD or VDDQ (e.g., each at 1.8 volts). *See, e.g.*, Ex. 1023 (Harris) at [0009], [0010], Fig. 1A; Ex. 1028 (JESD205) at 9; *see also* Ex. 1027 (JESD82-20) at 31-32 (AMB receiving "V_{DD} Supply voltage DRAM interface"), 44 (describing DRAM interface on AMB receiving V_{DD}), 83 (same), Ex. 1028 at 9 (V_{DD}/V_{DDQ} for DRAM and AMB), 11, 13-16, 30, 33 (same).
- VCC or VCCFBD (e.g., each at 1.5 volts). *See, e.g.*, Ex. 1023 (Harris) at [0009], [0010], Fig. 1A; Ex. 1027 at 78, 82, 83; Ex. 1028 (JESD205) at 9, 30-32.
- VDDL (e.g., at 1.8 volts). *See, e.g.*, Ex. 1028 (JESD205) at 17-20; Ex. 1026 (JESD79-2B) at p.6.
- VDDPSD (e.g., at 3.3 volts). *See, e.g.*, Ex. 1023 (Harris) at [0017], Fig. 3; Ex. 1027 (JESD82-20) at 83; Ex. 1028 (JESD205) at 9, 15.

168. Similarly, to the extent Patent Owner argues that two different voltage amplitudes recited in the claims can have the same amplitude, voltage mapping (B) ("Ground 1B") includes four voltage supplies at four voltage amplitudes. The first voltage is VDD, VDDQ, or VDDL (e.g., each at 1.8 volts); the second voltage is

VCC (e.g., at 1.5 volts); the third voltage is VCCFBD (e.g., at 1.5 volts); and the fourth voltage is VDDSPD (e.g., at 3.3 volts):

- VDD, VDDQ, VDDL (e.g., each at 1.8 volts). *See, e.g.*, Ex. 1023 (Harris) at [0009], [0010], Fig. 1A; Ex. 1028 (JESD205) at 9, 17-20; Ex. 1026 (JESD79-2B) at pp.6-7; *see also* Ex. 1027 (JESD82-20) at 31-32 (AMB receiving "V_{DD} Supply voltage DRAM interface"), 44 (describing DRAM interface on AMB receiving V_{DD}), 83 (same), Ex. 1028 at 9 (V_{DD}/V_{DDQ} for DRAM and AMB), 11, 13-16, 30, 33 (same).

- VCC (e.g., at 1.5 volts). *See, e.g.*, Ex. 1023 (Harris) at [0009], [0010], Fig. 1A; Ex. 1027 at 78, 82, 83; Ex. 1028 (JESD205) at 9.

- VCCFBD (e.g., at 1.5 volts). *See, e.g.*, Ex. 1023 (Harris) at [0009], [0010], Fig. 1A; Ex. 1027 at 78, 82, 83; Ex. 1028 (JESD205) at 9, 30-32.

- VDDPSD (e.g., at 3.3 volts). *See, e.g.*, Ex. 1023 (Harris) at [0017], Fig. 3; Ex. 1027 (JESD82-20) at 83; Ex. 1028 (JESD205) at 9, 15.

169. Voltage mapping (C) ("Ground 1C") includes four voltage supplies at four different voltage amplitudes. The first voltage is VDD, VDDQ, VDDL (e.g., each at 1.8 volts); the second voltage is VCC or VCCFBD (e.g., each at 1.5 volts); the third voltage is VTT (e.g., at 0.9 volts); and the fourth voltage is VDDSPD (e.g., at 3.3 volts):

- VDD, VDDQ, VDDL (e.g., each at 1.8 volts). *See, e.g.*, Ex. 1023 (Harris) at [0009], [0010], Fig. 1A; Ex. 1028 (JESD205) at 9, 17-20; Ex. 1026 (JESD79-2B) at pp.6-7; *see also* Ex. 1027 (JESD82-20) at 31-32 (AMB receiving "V_{DD} Supply voltage DRAM interface"), 44 (describing DRAM interface on AMB

receiving V_{DD}), 83 (same), Ex. 1028 at 9 (V_{DD}/V_{DDQ} for DRAM and AMB), 11, 13-16, 30, 33 (same).

- VCC or VCCFBD (e.g., each at 1.5 volts). *See, e.g.*, Ex. 1023 (Harris) at [0009], [0010], Fig. 1A; Ex. 1027 at 78, 82, 83; Ex. 1028 (JESD205) at 9, 30-32.

- VTT (e.g., at 0.9 volts). *See, e.g.*, Ex. 1028 (JESD205) at 9, 15, 68.

- VDDPSD (e.g., at 3.3 volts). *See, e.g.*, Ex. 1023 (Harris) at [0017], Fig. 3; Ex. 1027 (JESD82-20) at 83; Ex. 1028 (JESD205) at 9, 15.

2. Ground 2: Ground 1 in view of Amidi

170. Ground 2 involves Ground 1 in view of Amidi. *Supra* ¶152. As explained above, Ground 1 involves Harris in view of the FBDIMM Standards. *Supra* ¶¶150, 157-169. As explained below, it would have been obvious to a Skilled Artisan to incorporate battery backup power, as taught by Amidi, when implementing the memory module teachings of Harris to address the case of a power outage or clock malfunction. *See, e.g.*, Ex. 1024 at 1:28-35. Harris and Amidi are both in the field of memory technology, and more specifically disclose memory modules. *See* Ex. 1023 at Abstract; Ex. 1024 at Abstract. Harris itself is concerned with power reliability and teaches an option to use redundant external power sources. *See* Ex. 1023 at [0014] (describing a "redundancy implementation"), [0016] (describing a "redundant VRM" to "power a redundant voltage path"), Figs. 1B, 2. Similar to the redundant implementation in Harris, Amidi teaches a redundant power source. *See, e.g.*, Ex. 1024 at Abstract. Amidi

recognizes that it is useful to keep data on the memory module with a backup power supply on the module itself, such as a battery supply, when the entire system surrounding the memory module loses power. *See* Ex. 1024 at 1:28-35 ("Thus, it may be useful to provide an option for keeping data in volatile memory even when a surrounding system loses power. Moreover, it may also be useful to keep data in volatile memory when a surrounding system suffers some form of an error which causes a clock to malfunction even though power is still supplied. Likewise, it may be useful to provide volatile memory which has non-volatile characteristics in short- or medium-term time periods."), 2:6-26 ("A system, method and apparatus is provided for a clock and power fault detection for a memory module. . . . For example, one may provide a system with a controller which detects voltage levels and clock signals, a state machine for operating a memory in backup mode, and a battery and supporting circuitry for supplying backup power. Similarly, one may provide a process which operates to detect voltage and clock signals, initiate backup operations, maintain memory (through refresh, for example), and detect a recovery status. Providing such a system or process within a memory module can be very helpful, as it avoids the need for system circuitry in a computer system or similar device which can maintain a memory module from outside the module. Moreover, such a system or process may be tuned to the specific memory module, instead of requiring overhead to deal with many different types of memory

modules, for example."). Therefore, a Skilled Artisan would have been motivated to use Amidi's on-board redundant power source when implementing the FBDIMM memory module of Harris to keep data on the memory module with a backup power supply when the external supply to the memory module loses power.

171. In particular, a Skilled Artisan would have been motivated to use the backup power management and logic functionality of Amidi that includes monitoring the system supply, detecting faults, initiating backup power, and initiating refresh operations in the volatile memory to maintain data. Ex. 1024 at 2:6-26, Fig. 15. Although I understand that bodily incorporation is not required for obviousness, Amidi's functionality could be incorporated in the FBDIMM memory module of Harris as illustrated below in an annotated version of Figure 5 of Amidi and Figure 1A of Harris.

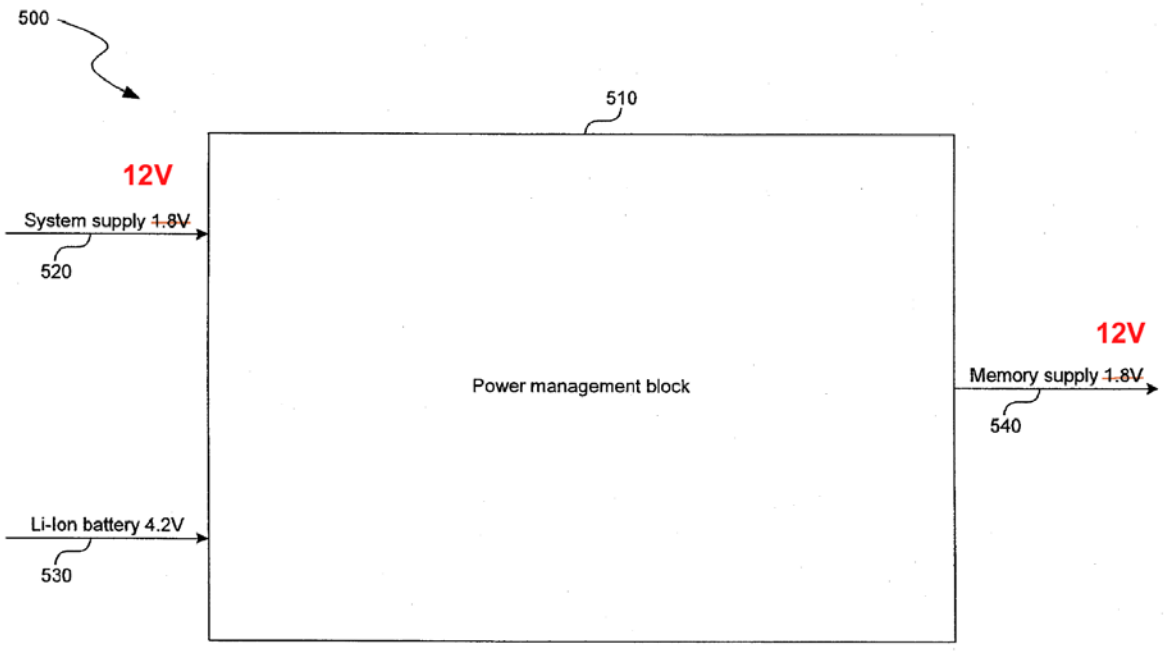


FIG. 5

Ex. 1024 at Fig. 5 (annotated with teachings of Harris). As shown in annotated Figure 5 of Amidi, a Skilled Artisan would have recognized that the power management block of Amidi would be modified to receive the external voltage source of Harris instead of the 1.8-volt system supply in Amidi. *See* Ex. 1024 at Fig. 5 (annotated above). Such a modification would have been well within the level of skill at the time. *See, e.g.*, Ex. 1058 at 5 ("Switching-Regulator Theory") and 12-15 ("Buck or Step-Down"). Amidi itself discloses converting the 4.2-volt lithium-ion battery input to the power management block 510 to a voltage of 1.8V for the memory supply 540. *See* Ex. 1024 at Fig. 5. Amidi also discloses in its Figure 6 embodiment that a DC/DC boost converter is used to step-up a voltage to a higher voltage level, a DC/DC buck converter is used to step-down a voltage to a

lower voltage level, and a lithium-ion battery charger is provided a 5.0-volt supply. *See id.* at Fig. 6 (DC/DC boost converter 610 converting 1.8 volts system supply to 5.0 volts for a Li-Ion battery charger 620, DC/DC buck converter 640 converting 3.6 volts (nominal) from the battery to 1.8 volts for the memory power supply), 4:23-60 (describing Figure 6 embodiment). In addition, Harris expressly describes an embodiment in which the external voltage source of 12-volts is converted by the on-board VRM to the stepped-down voltage levels required on the memory module. *See* Ex. 1023 at [0012], [0013], [0016], [0020]; *see also* Ex. 1023 at pp. 3-4 (claims 4, 15, 23, 33).

172. In the combination, a Skilled Artisan would have understood to use switching DC-DC converters, such as buck and boost converters as taught by both Harris and Amidi, and select those to correspond to the voltages used in Harris. Ex. 1023 at [0010] ("Preferably, a high-frequency switching voltage converter capable of generating tightly-controlled voltage levels may be implemented as the on-board VRM 102 for purposes of the present patent disclosure."); Ex. 1024 at Fig. 6 (showing the use of buck and boost converters to convert voltages to different levels). For example, a buck converter would step-down the 12-volt supply to a 5-volt supply for the lithium-ion battery charger, and a boost converter would step-up the lithium-ion battery's voltage (e.g., 4.2 volts) to the 12-volt level used by the memory module, as Harris teaches. *See* Ex. 1024 at 4:14-60, Figs. 5-6; *see also* Ex.

1058 at 5 (“Switching-Regulator Theory”) and 12-15 (“Buck or Step-Down”); Ex. 1032 at 161 (describing “dc-dc Switch-Mode Converters,” including “Step-down (buck) converter[s]” and “Step-up (boost) converter[s],” and explaining that “only the step-down and the step-up are the basic converter topologies”). Thus, the power management block of Amidi outputs either the 12-volt external voltage or the battery supply boosted to the same voltage level.

173. Furthermore, a Skilled Artisan would have understood that Harris’s module has a mode called S3 mode when implemented in accordance with the FBDIMM standards. In S3 mode, power to selected parts of the FBDIMM is switched off and the DRAM devices are put into a self-refreshing mode to save power without losing the data stored in those volatile DRAM devices. Ex. 1027 (JESD82-20) at 21 (“When the Advanced Memory Buffer core logic is in S3 power mode, … 1.8V supply is on. 1.5V, Vtt, and 3.3V are off. DRAMs are in self refresh …”), 39 (“S3 is an ACPI mode in which the DIMMs are put into a very lower power state, with the DRAMs in self refresh mode”). A Skilled Artisan would have recognized that the FBDIMM S3 mode of Harris’s module is similar to Amidi’s DRAM self-refreshing functionality. Ex. 1024 at Fig. 11, 2:16-19 (“Similarly, one may provide a process which operates to … maintain memory (through refresh, for example)”). Thus, a Skilled Artisan would have been motivated to use the S3 mode that was already available in Harris’s module when

implementing the backup power supply and logic functionality of Amidi, because S3 mode performs the function of refreshing the memory (e.g., self refresh), just like in Amidi. Indeed, a Skilled Artisan would have understood that the S3 mode was described in the FBDIMM standards for the very purpose of saving power in FBDIMM modules like Harris's which are used in servers and workstations. Ex. 1027 (JESD82-20) at 39 ("S3 current Specification … "very lower power state"); Ex. 1028 at 9 ("These SDRAM FB-DIMMs are intended for use as main memory when installed in systems such as servers and workstations.").

174. As shown in the annotations to Figure 1A of Harris in view of Amidi's teachings, a Skilled Artisan would have been motivated to implement the memory module of Harris with the functionality of Amidi's power management and logic blocks for detecting system failures, and switching over to battery backup power.

Ground 2: Ground 1 and Battery Backup of Amidi

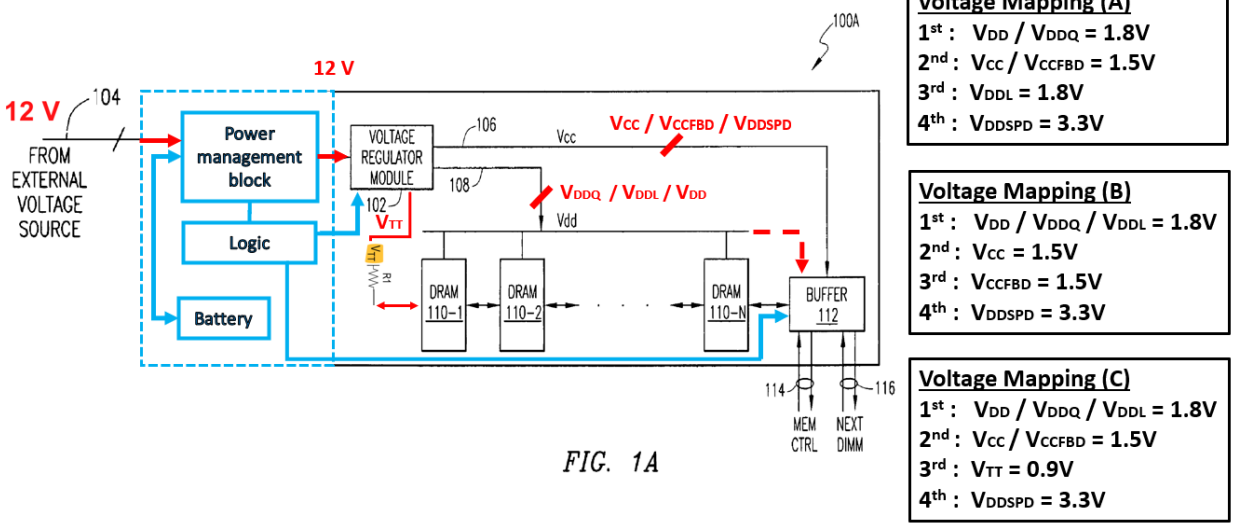


FIG. 1A

Ground 2: Ground 1 and Battery Backup of Amidi

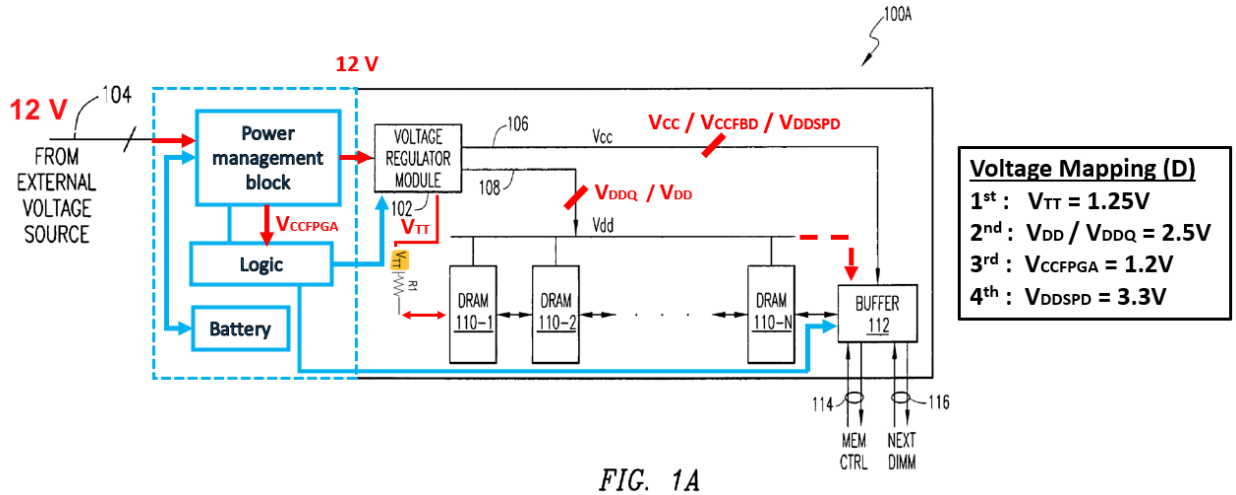


FIG. 1A

Ex. 1023 at Fig. 1A (annotated with teachings of Amidi). As shown, a 12-volt supply, sourced from either the 12-volt external voltage source or the boosted battery supply, is provided to Voltage Regulator Module (102). *See e.g.*, Ex. 1023 at [0012], [0013], [0016], [0020]. Several voltage supplies are provided to the Advanced Memory Buffer (AMB, buffer 112), including VCC, VCCFBD, VDDSPD and VDD. In addition, several voltage supplies are provided to the memory devices (DRAM 110-1 to 110-N), including VDD, VDDL, VDDQ, and VTT. Further, a voltage supply VCCFPGA is provided to the logic coupled to the power management block.

175. This straightforward modification of Harris's memory module in view of the teachings of Harris and Amidi and the knowledge of a Skilled Artisan simply uses a known technique (e.g., Amidi's battery backup techniques) to improve a similar device (e.g., Harris's memory module) in the same way (e.g., to

provide a backup power supply using a battery). In addition, the modification merely applies a known technique (e.g., providing a backup power supply) to a known device (e.g., a memory module) that is ready for improvement to yield predictable results (e.g., redundancy when the system supply or clock fails).

176. As shown in the annotated figure above, there are four voltage mappings apparent to a Skilled Artisan. To the extent Patent Owner argues that two different voltage amplitudes recited in the claims can have the same amplitude, voltage mapping (A) ("Ground 2A") includes four voltage supplies at, for example, four voltage amplitudes. The first voltage is VDD or VDDQ (e.g., each at 1.8 volts); the second voltage is VCC or VCCFBD (e.g., each at 1.5 volts); the third voltage is VDDL (e.g., at 1.8 volts); and the fourth voltage is VDDSPD (e.g., at 3.3 volts). Voltage mapping (A) under Ground 2 is nearly identical to voltage mapping (A) under Ground 1. *See supra* ¶167.

177. Similarly, to the extent Patent Owner argues that two different voltage amplitudes recited in the claims can have the same amplitude, voltage mapping (B) ("Ground 2B") includes four voltage supplies, for example, at four voltage amplitudes. The first voltage is VDD, VDDQ, or VDDL (e.g., each at 1.8 volts); the second voltage is VCC (e.g., at 1.5 volts); the third voltage is VCCFBD (e.g., at 1.5 volts); and the fourth voltage is VDDSPD (e.g., at 3.3 volts). Voltage

mapping (B) under Ground 2 is nearly identical to voltage mapping (B) under Ground 1. *See supra* ¶168.

178. Voltage mapping (C) ("Ground 2C") includes four voltage supplies, for example, at four different voltage amplitudes. The first voltage is VDD, VDDQ, VDDL (e.g., each at 1.8 volts); the second voltage is VCC or VCCFBD (e.g., each at 1.5 volts); the third voltage is VTT (e.g., at 0.9 volts); and the fourth voltage is VDDSPD (e.g., at 3.3 volts). Voltage mapping (C) under Ground 2 is nearly identical to voltage mapping (C) under Ground 1. *See supra* ¶169.

179. Voltage mapping (D) ("Ground 2D") includes four voltage supplies, for example, at four different voltage amplitudes. The first voltage is VTT (e.g., at 1.25 volts); the second voltage is VDD or VDDQ (e.g., each at 2.5 volts); the third voltage is VCCFPGA (e.g., at 1.2 volts); and the fourth voltage is VDDSPD (e.g., at 3.3 volts):

- VTT (e.g., at 1.25 volts). *See, e.g.*, Ex. 1023 (Harris) at [0002], [0009]; Ex. 1045 (JESD79) at 1, 7, 54, 60; Ex. 1028 (JESD205) at 9.
- VDD or VDDQ (e.g., each at 2.5 volts). *See, e.g.*, Ex. 1023 (Harris) at [0002], [0009]; Ex. 1045 (JESD79) at 1, 7, 54, 60; Ex. 1028 (JESD205) at 9.
- VCCFPGA (e.g., at 1.2 volts). *See, e.g.*, Ex. 1024 (Amidi) at 2:12-16, 6:40-43; Ex. 1025 (Spiers) at [0037]; Ex. 1042 at 2; Ex. 1042 at 1.

- VDDPSD (e.g., at 3.3 volts). *See, e.g.*, Ex. 1023 (Harris) at [0017], Fig. 3; Ex. 1027 (JESD82-20) at 83; Ex. 1028 (JESD205) at 9, 15.

3. Ground 3: Ground 2 in view of Hajeck

180. Ground 3 involves Ground 2 in view of Hajeck, Ex. 1038 (US 6,856,556). It would have been obvious to a Skilled Artisan to combine the references in Ground 2 for the reasons discussed above. As discussed below, it would have been also obvious to a Skilled Artisan to combine the references in Ground 2 with the disclosure of Hajeck.

181. As discussed above, Hajeck is directed to "protecting storage subsystems, such as but not limited to flash memory cards, from damage and data loss caused by irregularities in a power signal provided by a host." Ex. 1038 at 1:10-13; *see supra* ¶137. In particular, Hajeck explains that "[t]he protection circuitry and methods of the present invention may also be incorporated into other types of storage subsystems, including volatile storage subsystems that store data within DRAM." *Id*. at 4:62-65.

182. Therefore, a Skilled Artisan would have understood that Hajeck is in the same field of memory subsystems as and analogous art to the 918 Patent and the prior art references of Ground 2, including Amidi and Harris, as each is directed to solving the problem of reliable data storage and, in particular, to protect against power failures. *See, e.g.*, Ex. 1038 (Hajeck) at Title ("Storage subsystem

with embedded circuit for protecting against anomalies in power signal from host"), Ex. 1024 (Amidi) at Title ("Clock and power fault detection for memory modules"), Ex. 1023 (Harris) at Figs. 1B and 2, [0014], [0016] (disclosing using redundant power sources), Ex. 1001 at 11:15-21 ("The examples of FIGS. 3A and 3B are directed to architectures of a non-volatile DIMM (NVDIMM) NVDIMM system that may use a power subsystem (not shown) that can include a battery or a capacitor as a means for energy storage to copy DRAM memory data into Flash memory when power loss occurs, is detected, or is anticipated to occur during operation.").

183. For example, Amidi discloses that "[s]ignal 670 is controlled by voltage supervisory block 665, which receives system supply 605 and a reference voltage 675, and compares the two. If system supply 605 has a greater magnitude than reference voltage 675, signal 670 causes power switch multiplexer 655 to choose system supply 605 as a source for memory supply 660. If system supply 605 has a magnitude lower than reference voltage 675, then signal 670 causes power switch multiplexer 655 to choose battery power 650 for memory supply 660." Ex.1024 at 4:44-53. A Skilled Artisan would have understood from this disclosure that Amidi's voltage supervisory functionality switches to backup power when the input voltage is below a first threshold.

184. Hajeck explains that a "significant problem in the area of storage subsystems relates to data loss, data corruption, and circuitry damage caused by interruptions and other irregularities in the power signal supplied by the host system." Ex. 1038 at 1:15-18. For example, "power signal anomalies, such as power surges and spikes, can additionally cause permanent damage to the circuitry of the storage subsystem." *Id*. at 1:28-31. To solve these problems, Hajeck discloses a "voltage detection circuit 48 [that] is responsible for detecting anomalies in the power signal VIN supplied by the host on line 36, and for driving the ready/busy signal to the 'busy' state when such anomalies are detected. A conventional voltage detection circuit may be used. The voltage detection circuit 48 may be designed to generate a 'busy' signal whenever VIN falls below a certain level, such as 2.6 or 2.7 volts. The voltage detection circuit may also be designed to generate a busy signal when the voltage exceeds a certain level, and/or when other types of anomalies are detected. To inhibit rapid transitions between the 'ready' and 'busy' states, the voltage detection circuit may be designed to provide a degree of hysteresis, and/or to hold its output for a particular time period after a state transition." Ex. 1038 at 3:30-40.

185. A Skilled Artisan would have understood from this disclosure of Amidi and Hajeck that Amidi's voltage supervisory block can be modified to detect voltage anomalies and switch to the backup power not only "[i]f system

supply 605 has a magnitude lower than reference voltage 675" as disclosed by Amidi, Ex. 1024 at 4:44-53, but also "when the voltage exceeds a certain level" as taught by Hajeck, Ex. 1038 at 3:30-40. A Skilled Artisan would have been motivated to detect voltage anomalies when the input voltage is above a threshold in order to protect against "power signal anomalies, such as power surges and spikes, [which] can additionally cause permanent damage to the circuitry of the storage subsystem" as taught by Hajeck. Ex. 1038 at 1:28-31. For example, Harris specifically discloses a need to detect input voltages more than 15% above the expected voltage, thus providing a motivation to include the functionality of Hajeck's voltage detection circuit 48 in the combination of Ground 3. *See* Ex. 1023 (Harris) at [0013] ("Further, since the +12V power supply is not used directly by DRAM devices or buffer/logic components of the memory assembly, a wide tolerance (e.g., around +/−15%) can be accommodated, allowing low cost power distribution for system boards (such as, e.g., motherboards, cell boards, et cetera) wherein design requirements for bypass/hold-up capacitors may be relaxed or minimized.").

186. Indeed, the problems caused by such overvoltage conditions, and solutions to detect and protect against them, were well known at the time. *See, e.g.*, Ex. 1065 (Resnick) at [0002] ("Semiconductor devices, like most electronic products, are sensitive in their operation to supplied voltage levels. If voltage

levels at working parts are lower than specified minimum requirements, the parts may malfunction. If voltage levels are higher than specified maximum requirements, the parts may malfunction and can also suffer catastrophic failure. In semiconductor memory devices, for example, such as Dynamic Random Access Memories (DRAMs), inadequate voltage levels may cause memory parts to malfunction by reading out or storing incorrect information."). A Skilled Artisan would have understood that, to avoid these well-known problems, a "conventional voltage detection circuit" referenced by Hajeck was readily available at the time and was configured to detect both under and over voltage conditions. Ex. 1038 at 3:30-40; *see also* Ex. 1061 (ADM1060 Supervisory/Sequencing Circuit) at 15 ("All of the [supply fault] detectors can be programmed to detect undervoltage, overvoltage, or out-of-window (undervoltage or overvoltage) conditions"); Ex. 1063 (LMC6953 PCI Local Bus Power Supervisor) at 1 ("Under and over voltage detectors for 5V and 3.3.V") and 2 (listing specific Over Voltage and Under-Voltage Thresholds).

187. Therefore, modifying Amidi's voltage supervisory block to detect both undervoltage and over voltage conditions would have been obvious to a Skilled Artisan to prevent known problems caused by overvoltage conditions and was well within the level of skill at the time since "conventional," readily available voltage detection circuits implemented over and under voltage protection and the

combination provided the predictable result of switching to backup power when such overvoltage and undervoltage conditions were detected.

4. Ground 4: Spiers in view of Amidi

188. Ground 4 involves Spiers in view of Amidi. *Supra* ¶150.

189. Spiers and Amidi are analogous art to the 918 Patent, as they are directed to providing data backup in memory modules in case of power failure.

190. The 918 Patent discloses a memory module for data backup that includes a volatile memory subsystem (1030, yellow), a non-volatile memory subsystem (1040, green), circuitry (red) for interfacing with the computer system through a standard interface (orange), on one hand, and with the volatile (yellow) and non-volatile (green) memory subsystems on the other hand. Ex. 1001 at Fig. 12 (reproduced below, annotated).

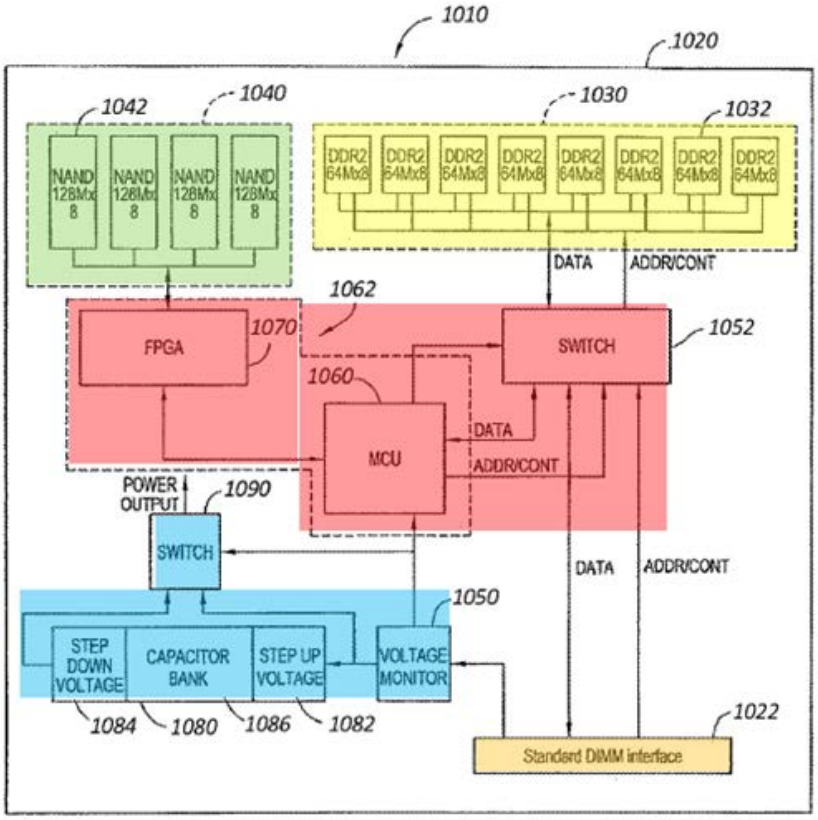
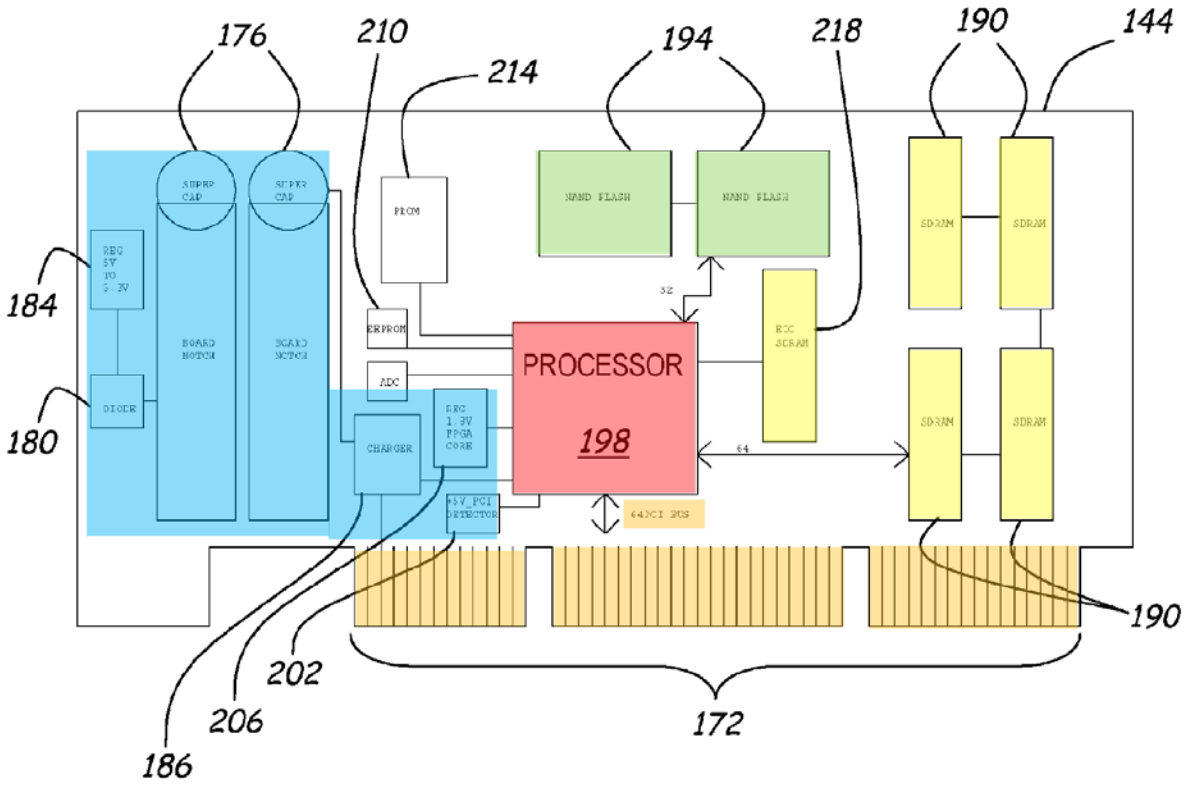


FIG. 12

191. The 918 Patent's module also includes a backup power supply (blue) based on a capacitor bank (180) which is used to power the memory module while the circuitry (red) transfers data from the volatile (yellow) to the non-volatile (green) memory if a voltage monitor (1050) detects a power interruption. *Id*. at 11:15-21, 20:43-57.

192. Years before the earliest priority date claimed by the 918 Patent, Spiers disclosed substantially the same structure. Just like in the 918 Patent, the memory module of Spiers (backup device 144) includes a processor (red) for interfacing with the computer system through a standard interface (orange), on one

hand, and with on-board volatile (yellow) and non-volatile (green) memory, on the other hand. Ex. 1025 at Title, [0001], Fig. 5 (reproduced below, annotated). The backup device of Spiers also includes its own temporary power supply (blue). *Id*. at Fig. 5.



193. As shown in Fig. 5, the backup device of Spiers, in an embodiment, is implemented in a PCI card with volatile SDRAM memories (190 and 218, yellow) and non-volatile memories (green) including NAND flash memories (194). *Id*. at [0037]. The 918 Patent uses the same type of memories. A Skilled Artisan would have understood that SDRAM and flash memory devices were "off-the-shelf components that are commercially available." *See*, *e.g.*, Ex. 1064 (Bonella) at

[0029] (disclosing a memory module with DRAM and FLASH memory) and [0032] (explaining that these were "off-the-shelf components"); *see also id*. at [0036] (identifying DDR2 DRAM as an example for DRAM devices).

194. As in the 918 Patent, Spiers's backup power supply (blue) is implemented using capacitors (176), although Spiers also discloses that it can use "a battery, or any other suitable power source." Ex. 1025 at Abstract. The backup power supply also includes a charger (186) to charge the capacitors (or the battery) when the power through the PCI connector is available. *Id.* at [0037]. If a power detection circuit 202 detects power interruption, the processor (198) "switches to the backup power source and receives power from the backup power source while moving the data from the backup volatile memory to the backup non-volatile memory." *Id.* at Abstract, [0037]. Spiers discloses that the backup power supply includes voltage converters, such as voltage regulators 184 and 206, to supply regulated voltage to the components, including processor 198, that participate in this operation of moving the data from the volatile to the non-volatile memory. *Id.*

195. Amidi also discloses power fault detection for memory modules. Ex. 1024 at Title. Amidi uses a battery as the backup power source (like the alternative implementation of Spiers), and discloses further details about its power management block that handles power interruptions, including the use of buck converters (e.g., 640) to provide backup power for the memory devices and logic

devices controlling the power management in case of power failure. *Id*. at Fig. 6 (reproduced below).

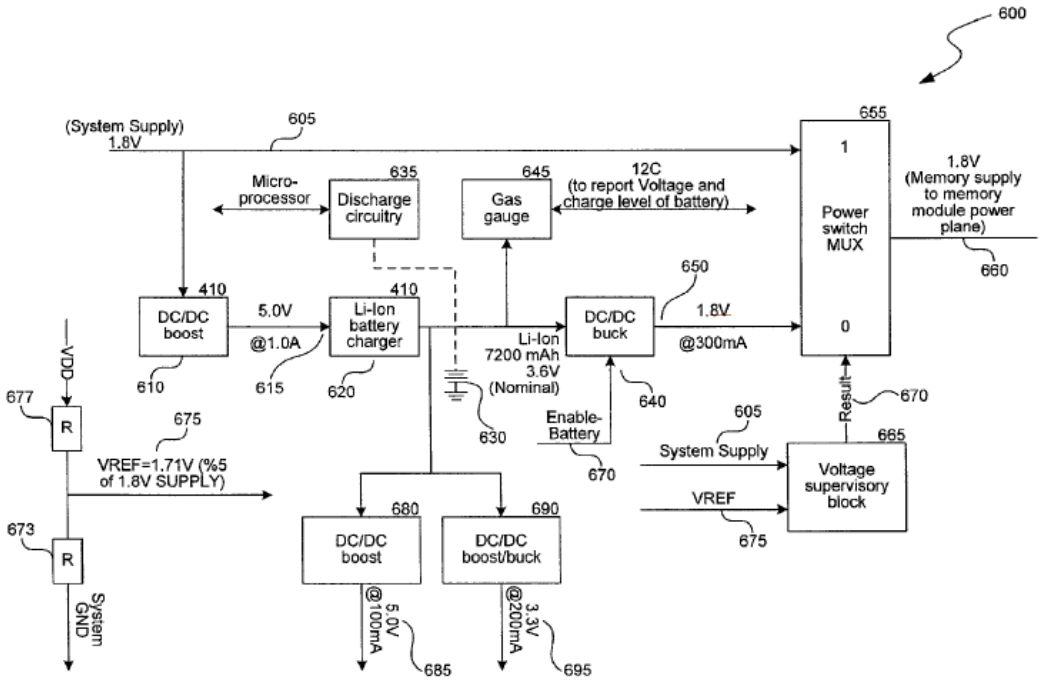
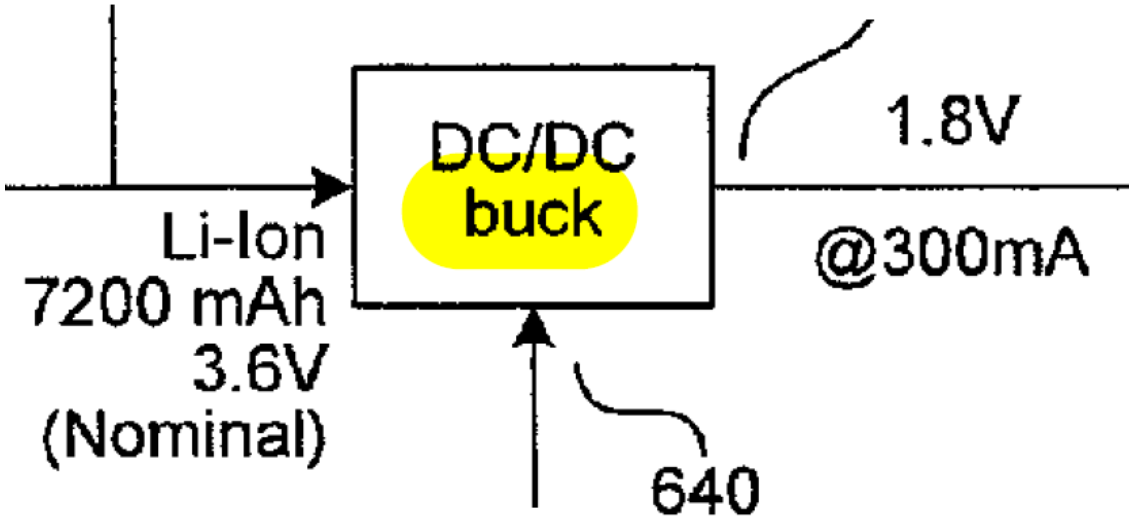


FIG. 6

196. Accordingly, a Skilled Artisan would have been motivated to consult Amidi's disclosure and look for specific implementation details when implementing the memory module of Spiers. For example, Spiers discloses volatile memory including SDRAM devices without identifying any specific SDRAM devices. Ex. 1025, e.g., at Fig. 5 and [0010, 0037-38]. Therefore, a Skilled Artisan would have been motivated to look at analogous prior art references, such as Amidi, which discloses specific types of SDRAM devices, such as DDR, and DDR2 SDRAMs, to be used in memory modules. Ex. 1024 at Figs. 3 and 13, 7:52-59, 10:17-20. As another example, Spiers discloses voltage

regulators 184 and 206 without identifying any specific voltage regulator. Ex. 1025 at Fig. 5 and [0037]. Therefore, a Skilled Artisan would have been motivated to look at analogous prior art references, such as Amidi, which discloses specific types of voltage regulators, such as boost, buck, and boost/buck voltage converters, to be used for providing regulated voltages on a memory module. Ex. 1024 at Fig. 6 (reproduced below in part, annotated) and 4:30-43.



197. Similarly, Spiers discloses switching a power supply from the system power to the backup power, Ex.1025, e.g., at Abstract and Fig. 14, and Amidi discloses a specific structure, a power switch multiplexer, for implementing such a switch, Ex. 1024 at Fig. 7 and 4:56-5:9. Therefore, it would have been obvious to a Skilled Artisan to combine the teaching of Spiers and Amidi.

198. Furthermore, a Skilled Artisan would have been familiar with memory systems and corresponding standards, including the JEDEC standards for memory

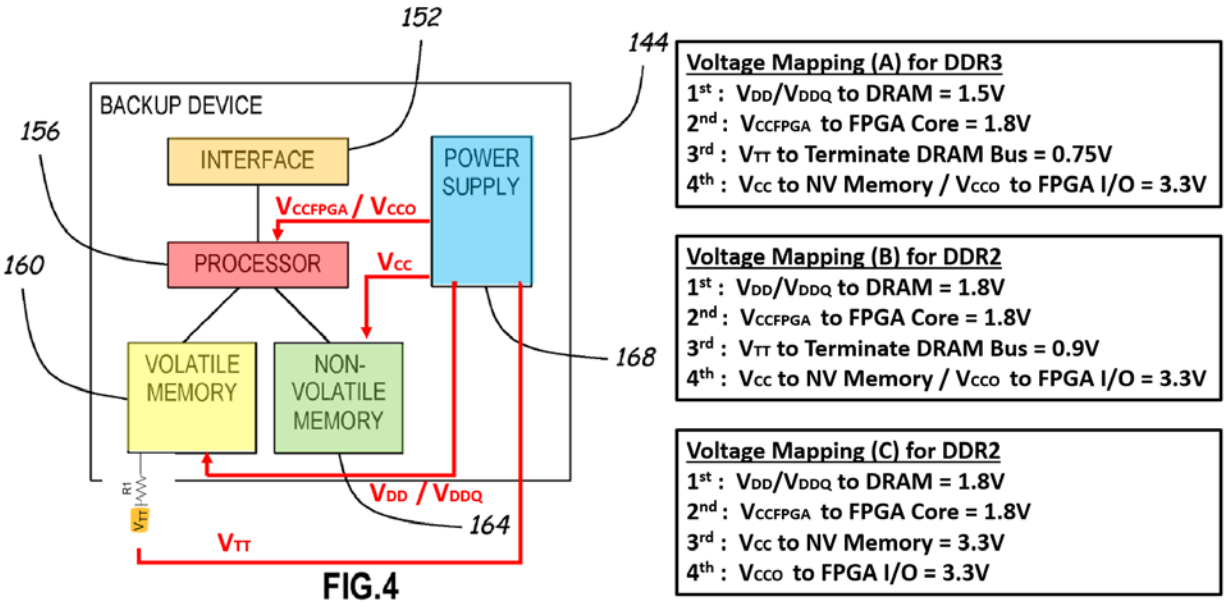
devices and memory modules already standardized, or in the process of being standardized, at the time. *See supra* ¶ 67. For example, Spiers discloses SDRAM memory devices. *See* Ex. 1025 at [0010]. A Skilled Artisan would have understood that such SDRAM memory devices were already standardized, including DDR2 and DDR3 SDRAMs. *See* Ex. 1026; Ex. 1046. A Skilled Artisan would have also understood that these JEDEC standards describe requirements, among others, for the voltage supply of the corresponding JEDEC-compliant devices.

199. Similarly, the 918 Patent discloses and relies on widely-known JEDEC standards. For example, the background of the 918 Patent references a "JEDEC standard DRAM DIMM." Ex. 1001 at 3:42-43; *see also id.* at 3:12-13 ("form factor of a standard DIMM"), 17:59-61 ("standard access protocol, such as JEDEC's DDR DRAM"). The 918 Patent also references specific standards, "such as DDR, DDR2, DDR3, DDR4" (*id.* at 13:42-43), and standard connectors, such as "a standard 240-pin DDR2 edge connector" (*id.* at 22:7-8).

200. A Skilled Artisan would have thus recognized, and been motivated to use, DDR2 or DDR3 SDRAMs when implementing the SDRAMs in the backup device of Spiers, and to power the DRAMs according to the relevant JEDEC standards (e.g., JESD79-2B and JESD79-3A). *See* Ex. 1026; Ex. 1046. Accordingly, at least the following voltage mappings would have been apparent to

a Skilled Artisan, as shown in the figure below with examples of voltage amplitudes for the voltage supplies.

Ground 4: Spiers in view of Amidi, with DDR2 or DDR3 DRAMs



Ex. 1025 at Fig. 4 (annotated). A Skilled Artisan would have also understood that the choice to use either DDR2 or DDR3 DRAMs would dictate the voltages that must be produced by the power supply (blue, above) for V_{DD}/V_{DDQ} and V_{TT}.

201. Voltage Mapping (A) ("Ground 4A") corresponds to an implementation of Spiers's backup device with DDR3 DRAMs and includes four voltage supplies, for example, at four different voltage amplitudes. The first voltage is VDD/VDDQ (e.g., at 1.5 volts); the second voltage is VCCFPGA (e.g., at 1.8 volts); the third voltage is VTT (e.g., at 0.75 volts); and the fourth voltage is VCC or VCCO (e.g., each at 3.3 volts):

- VDD/VDDQ (e.g., at 1.5 volts). *See, e.g.*, Ex. 1046 (JESD 79-3A) at p.10.

- VCCFPGA (e.g., at 1.8 volts). *See, e.g.*, Ex. 1025 (Spiers) at Fig. 5, [0037]; Ex. 1042 (Murata Power Supply Reference Guide for Xilinx FPGAs) at 2, 16.

- VTT (e.g., at 0.75 volts). *See, e.g.*, Ex. 1046 (JESD79-3A) at pp. 15 (VTT at power-up), 109 (disclosing $V_{TT}=V_{DDQ}/2$), 123; Ex. 1045 (JESD79) at pp. 8, 54, 60.

- VCC or VCCO (e.g., each at 3.3 volts). *See, e.g.*, Ex. 1025 (Spiers) at Fig. 5, [0037]; Ex. 1042 (Murata Power Supply Reference Guide for Xilinx FPGAs) at 2, 16; Ex. 1049 (Micron, NAND Flash Memory Datasheet) at 1, 38.

202. For example, a Skilled Artisan would have understood that, in an implementation of Spiers where DDR3 DRAMs are used for the volatile memory (yellow, above), the VDD/VDDQ supply voltage is provided to the DRAMs at 1.5 volts and that the DRAMs are coupled, through a termination resistor, to the termination voltage VTT, which is equal to one-half of VDD/VDDQ or 0.75 volts ("Voltage Mapping A"). *See* Ex. 1046 at pp. 10, 15 (explaining the order of turning on VDD, VDDQ and VTT), 109 (defining VTT as half of VDDQ), 123 (showing VTT being coupled through RTT).

203. Voltage Mapping (B) ("Ground 4B") corresponds to an implementation of Spiers's backup device with DDR2 DRAMs and includes four voltage supplies, for example, at three different voltage amplitudes. The first voltage is VDD/VDDQ (e.g., at 1.8 volts); the second voltage is VCCFPGA (e.g.,

at 1.8 volts); the third voltage is VTT (e.g., at 0.9 volts); and the fourth voltage is VCC or VCCO (e.g., each at 3.3 volts):

- VDD/VDDQ (e.g., at 1.8 volts). *See, e.g.*, Ex. 1026 (JESD79-2B) at pp.6-7.
- VCCFPGA (e.g., at 1.8 volts). *See, e.g.*, Ex. 1025 (Spiers) at Fig. 5, [0037]; Ex. 1042 (Murata Power Supply Reference Guide for Xilinx FPGAs) at 2, 16.
- VTT (e.g., at 0.9 volts). *See, e.g.*, Ex. 1026 (JESD79-2B) at p.71 (disclosing $V_{TT}=V_{DDQ}/2$), Ex. 1028 (JESD205) at 9, 15, 68.
- VCC or VCCO (e.g., each at 3.3 volts). *See, e.g.*, Ex. 1025 (Spiers) at Fig. 5, [0037]; Ex. 1042 (Murata Power Supply Reference Guide for Xilinx FPGAs) at 2, 16; Ex. 1049 (Micron, NAND Flash Memory Datasheet) at 1, 38.

204. A Skilled Artisan would have understood that, in an implementation of Spiers where DDR2 DRAMs are used for the volatile memory (yellow, above), the VDD/VDDQ supply voltage is provided to the DRAMs at 1.8 volts and that the DRAMs are coupled, through a termination resistor, to the termination voltage VTT at 0.9 volts ("Voltage Mapping B" and "Voltage Mapping C"). *See* Ex. 1026 at pp. 6-7 ($V_{DD}=V_{DDQ}=1.8V$), 71 ($V_{TT}=V_{DDQ}/2$).

205. Voltage Mapping (C) ("Ground 4C") corresponds to an implementation of Spiers's backup device with DDR2 DRAMs and includes four voltage supplies, for example, at two different voltage amplitudes. The first voltage is VDD/VDDQ (e.g., at 1.8 volts); the second voltage is VCCFPGA (e.g., at 1.8

volts); the third voltage is VCC (e.g., at 3.3 volts); and the fourth voltage is VCCO (e.g., at 3.3 volts):

- VDD/VDDQ (e.g., at 1.8 volts). *See, e.g.*, Ex. 1026 (JESD79-2B) at pp.6-7.
- VCCFPGA (e.g., at 1.8 volts). *See, e.g.*, Ex. 1025 (Spiers) at Fig. 5, [0037]; Ex. 1042 (Murata Power Supply Reference Guide for Xilinx FPGAs) at 2, 16.
- VCC (e.g., at 3.3 volts). *See, e.g.*, Ex. 1025 (Spiers) at Fig. 5, [0037]; Ex. 1049 (Micron, NAND Flash Memory Datasheet) at 1, 38
- VCCO (e.g., at 3.3 volts). *See, e.g.*, Ex. 1025 (Spiers) at Fig. 5, [0037]; Ex. 1042 (Murata Power Supply Reference Guide for Xilinx FPGAs) at 2, 16.

206. "Voltage Mapping C" maps the VCC voltage to the third voltage at 3.3 volts for the non-volatile memory (green, figure above) and the VCCO voltage to the fourth voltage at 3.3 volts for the FPGA input/output (I/O) (red, above).

5. Ground 5: Ground 4 in view of Hajeck

207. Ground 5 involves Ground 4 in view of Hajeck. Ex. 1038 (US 6,856,556). It would have been obvious to a Skilled Artisan to combine the references in Ground 4 for the reasons discussed above. As discussed below, it would have been also obvious to a Skilled Artisan to combine Ground 4 with the disclosure of Hajeck.

208. For the reasons discussed above with reference to Ground 3, Hajeck is analogous art to the '918 patent and to Amidi. *Supra* ¶¶ 180-187. Hajeck is also

analogous art to Spiers since both are directed to solving the problem of preventing data loss in memory modules in case of power anomalies, such as power failure. Ex. 1038 (Hajeck) at 4:10-21 ("Even if the anomaly is in the form of a complete interruption or termination of power from the host 32, the charge pump 46 continues to provide power to the controller 40 (and possibly to other active components, as mentioned above) for at least the minimum time period, TVREG, needed to complete all outstanding operations. For example, if a write operation is in progress and the memory subsystem 30 has write data stored in its volatile RAM buffer (not shown), backup power will be provided for a time period sufficient for the controller 40 to finish writing this data to the EEPROM memory 42, and if necessary, to back up any configuration data stored in volatile memory."); Ex. 1025 (Spiers) at Abstract ("The backup data storage device further includes a backup power source such as a capacitor, a battery, or any other suitable power source, and upon detection of a power interruption, switches to the backup power source and receives power from the backup power source while moving the data from the backup volatile memory to the backup non-volatile memory.").

209. Spiers explains that a "common requirement is that the data storage system securely store data, meaning that stored data will not be lost in the event of a power loss or other failure of the storage system." Ex. 1025 at [0002]. To detect a power failure, Spiers discloses "monitoring the voltage at a +5 volt pin" and "a

power detection circuit that, in this [PCI card] embodiment, is a +5V PCI detector 202." *Id*. at [0037] and [0054]. A Skilled Artisan would have understood from this disclosure that, in the PCI implementation, Spiers uses a known PCI voltage detector which monitors the +5 volt power supply to detect a power failure.

210. As discussed above with reference to Ground 3, Hajeck discloses the problems related to both undervoltage and overvoltage conditions and, to solve these problems, Hajeck discloses a "voltage detection circuit 48 [that] is responsible for detecting anomalies in the power signal VIN .... A conventional voltage detection circuit may be used … to generate a 'busy' signal whenever VIN falls below a certain level … [and] may also be designed to generate a busy signal when the voltage exceeds a certain level, and/or when other types of anomalies are detected." Ex. 1038 at 3:30-40. A Skilled Artisan would have understood that, to avoid these well-known problems, a "conventional voltage detection circuit" referenced by Hajeck was readily available at the time and was configured to detect both under and over voltage conditions. Ex. 1038 at 3:30-40; *see also* Ex. 1061 (ADM1060 Supervisory/Sequencing Circuit) at 15 ("All of the [supply fault] detectors can be programmed to detect undervoltage, overvoltage, or out-of-window (undervoltage or overvoltage) conditions"). A Skilled Artisan would have understood that such a voltage detection circuit was available specifically for monitoring PCI power supplies. Ex. 1063 (LMC6953 PCI Local Bus Power

Supervisor) at 1 ("Under and over voltage detectors for 5V and 3.3.V") and 2 (listing a typical Over Voltage Threshold of 5.6V and a typical Under-Voltage Threshold of 4.4V for a 5V power supply).

211. A Skilled Artisan would have understood from this disclosure of Spiers and Hajeck that Spiers's +5V PCI detector can be implemented to detect voltage anomalies and switch to the backup power "whenever VIN falls below a certain level … [and] when the voltage exceeds a certain level" as taught by Hajeck, Ex. 1038 at 3:30-40. A Skilled Artisan would have been motivated to detect voltage anomalies in both cases. For example, when Spiers's +5V PCI detector detects that the input voltage is above a threshold, switching to the backup voltage would protect against "power signal anomalies, such as power surges and spikes, [which] can additionally cause permanent damage to the circuitry of the storage subsystem" as taught by Hajeck. Ex. 1038 at 1:28-31.

212. Therefore, implementing Spiers's +5V PCI detector to detect both undervoltage and overvoltage conditions would have been obvious to a Skilled Artisan at the time in order to prevent known problems caused by overvoltage conditions. Such an implementation was well within the level of skill at the time since "conventional," readily available voltage detection circuits for PCI cards implemented over and under voltage protection and provided the predictable result

of switching to backup power when such overvoltage and undervoltage conditions were detected.

V. COMPARISON OF THE PRIOR ART TO THE CLAIMS OF THE 918 PATENT

213. My analysis below is based on my understanding of the law and the other information discussed above, including the five Grounds and various voltage mappings discussed above.

A. Claims 1-30 Are Unpatentable Over Grounds 1, 2, and/or 3

214. As explained below claims 1-3, 15 are unpatentable over Ground 1 (Harris in view of the FBDIMM Standards). In addition, claims 1-30 are unpatentable over Ground 2 (Ground 1 further in view of Amidi) and Ground 3 (Ground 2 further in view of Hajeck).

1. Claim 1 is Unpatentable

215. Claim 1 is unpatentable as the prior art references in each of Ground 1 (Voltage Mappings A, B, and C) and Grounds 2 and 3 (Voltage Mappings A, B, C, and D) render the claim obvious.

a) [1.a] Preamble

216. The preamble of claim 1 recites "*[a] memory module comprising.*"

217. Harris teaches and discloses this limitation to a Skilled Artisan in each of Grounds 1 through 3. In addition, for Grounds 1 through 3, Harris in view of the FBDIMM Standards teaches and discloses this limitation to a Skilled Artisan.

218. Harris explains that "industry standard memory modules, e.g., Dual In-line ***Memory Modules*** (DIMMS) [are] populated with dynamic random access memory (DRAM) devices." Ex. 1023 at [0002] (emphasis added); *see also id.* at [0009] ("memory module 100A [] may be embodied as a memory board assembly operable in a computer system"). Harris discloses that the DIMM can have different configurations, including registered DIMMs (RDIMMs) or fully buffered DIMMs (FBDs). *See id.* at [0009] ("[T]he DIMM configuration of an exemplary memory module may include unbuffered DIMMs, registered DIMMs (RDIMMs), or fully buffered DIMMs (FBDs) . . . .").

219. For example, as shown in Figure 1A of below, Harris discloses an embodiment with an FBD.

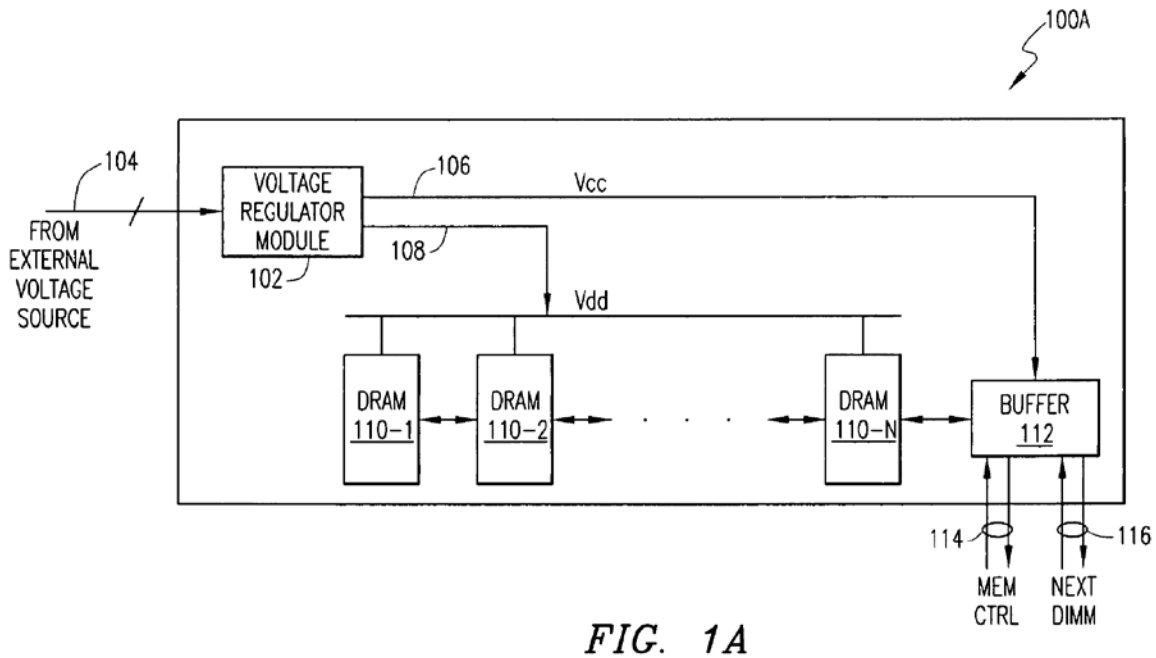


FIG. 1A

Id. at Fig. 1A; *see also id.* at [0009] ("[T]he DIMM configuration of the memory module 100A is exemplified as ***a fully buffered DIMM*** wherein a buffer/logic component 112 is provided for buffering command/address (C/A) space as well as data space at least for a portion of the memory devices 110-1 through 110-N.") (emphasis added).

220. As shown below in Figure 3, Harris also discloses an FBD implemented in a system such that the "memory controller 302 is operable to drive a bidirectional memory link 304 to which a plurality of memory boards 306-1 through 306-M are coupled in a daisy-chain fashion at their respective buffers." *Id.* at [0017].

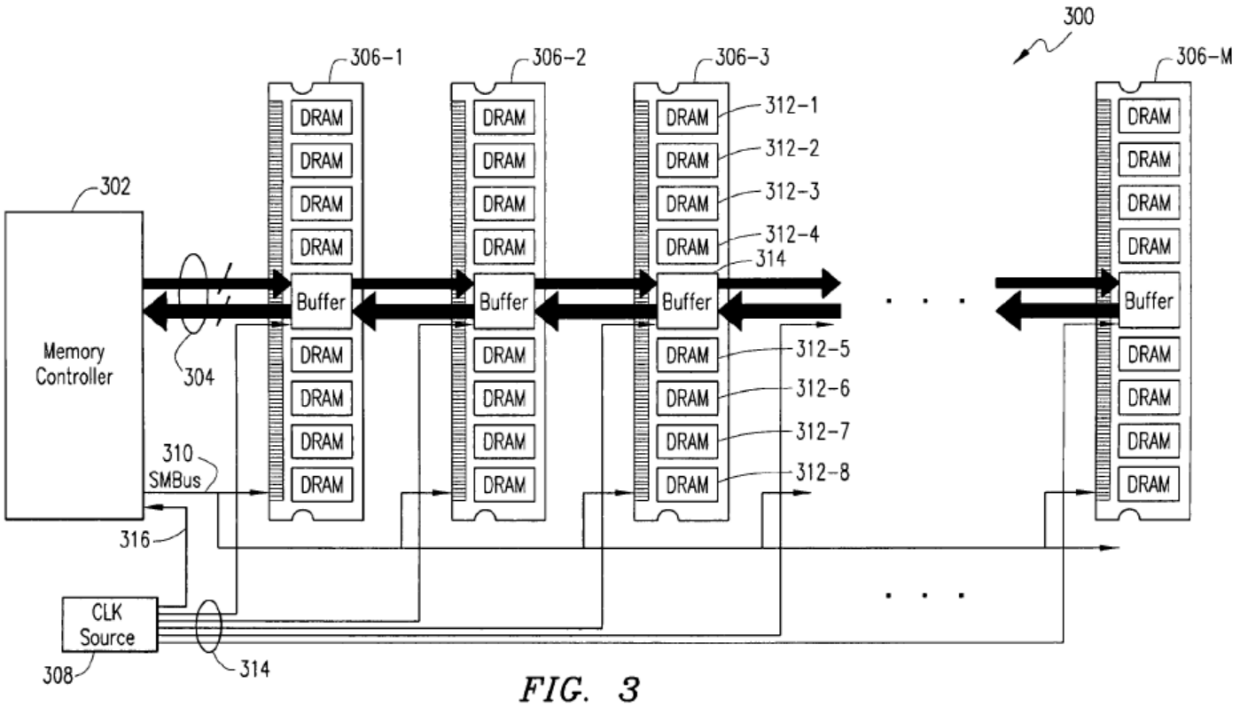
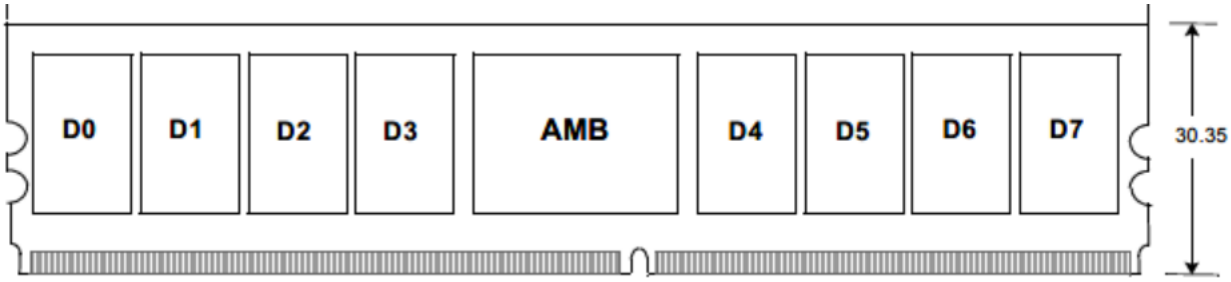


FIG. 3

Id. at Fig. 3.

221. A Skilled Artisan would have recognized that "industry standard memory modules" include fully buffered memory modules with form factors standardized by the Joint Electron Device Engineering Council (JEDEC). Ex. 1023 at [0013]; [0020] ("advantageously accommodat[ing]" "industry-standard form factors"). For example, a Skilled Artisan would have recognized that the JEDEC standard JESD205 (part of the FBDIMM Standards) discloses a "DDR2 SDRAM Fully Buffered DIMM (FBDIMM) Design Specification." Ex. 1028 at 1. A Skilled Artisan would have also readily recognized that Harris discloses a form factor for its fully buffered memory module that is similar to that in the corresponding JEDEC standard. *Compare* a "memory board 306" of Ex. 1023 at Fig. 3 (reproduced above) *with* the front of raw cards B and C in Ex. 1028 at 38 (reproduced below, in part).



222. Accordingly, to the extent the preamble of claim 1 is limiting, Harris alone, or in combination with the FBDIMM Standards, satisfies "*[a] memory module comprising*."

b) [1.b] Printed Circuit Board Having an Interface

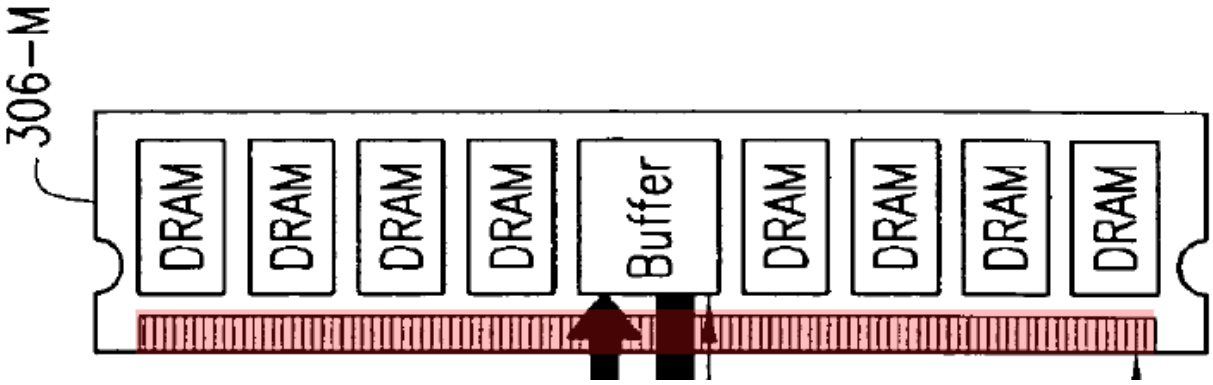
223. Claim 1 requires "*a printed circuit board (PCB) having an interface configured to fit into a corresponding slot connector of a host system, the interface including a plurality of edge connections configured to couple power, data, address and control signals between the memory module and the host system.*"

224. Harris teaches and discloses this limitation to a Skilled Artisan in each of Grounds 1 through 3. In addition, for Grounds 1 through 3, Harris in view of the FBDIMM Standards teaches and discloses this limitation to a Skilled Artisan.

225. Harris discloses a printed circuit board (PCB), such as one for the fully buffered DIMM 100A. Ex. 1023 at Fig. 1A. In particular, Harris contemplates using "both sides of the printed circuit board" to implement a DIMM and using a form factor including the printed circuit board that is compatible with the JEDEC standards. *Id.* at [0013] ("It is contemplated that local supply voltage conversion for double-rank DIMMs can be accommodated with a form factor design of approximately about one square inch (both sides of the ***printed circuit board***, and at a component height compatible with applicable Joint Electron Device Engineering Council (JEDEC) standards.") (emphasis added); *see also id.* at [0003], [0009], [0016], [0017] (reciting "memory board"), 3-4 (claims 1-36) (same), Figs. 1B, 3. This disclosure in Harris is consistent with the understanding of a Skilled Artisan that a memory module in the form factor of a fully buffered

DIMM is implemented on a printed circuit board. *See* Ex. 1028 at 10 ("The reference designs for the DIMM PCBs are called the "raw cards", abbreviated R/C."), 84 ("DIMM printed circuit board design uses six, eight or ten layers of glass epoxy material"); *see also* Ex. 1027 at 77 (discussing "simplifie[d] PCB routing"). Examples of PCB "raw cards" are also disclosed by the JEDEC standards. *See, e.g.*, Ex. 1028 at 38 (illustrating Raw Cards B and C); Ex. 1027 at 38-39 (addressing various Raw Cards). Thus, Harris satisfies a "*printed circuit board (PCB).*"

226. Harris discloses that the PCB of its memory module has a DIMM connector with pins. Ex. 1023 at [0019] ("one or more of the following advantages may be realized in an exemplary voltage distribution embodiment: . . . reduction in the pin count on DIMM connector to system board or memory riser card (whereby a smaller connector or wider pin spacing may be accommodated)"); *see also id.* at [0002] and [0012] (discussing specific pin counts for power). For example, Figure 3 of Harris is annotated in red below to show an edge connector of the DIMM with multiple connections.



Id. at Fig. 3 (reproduced in part and annotated).

227. A Skilled Artisan would have recognized that such a DIMM connector is part of an interface and is configured to fit into a corresponding slot connector of a host system according to relevant industry standards. *See, e.g.*, Ex. 1023 at [0002] and [0012] (discussing specific pin counts of the interface for power), [0013] ("By way of an additional variation in implementation, the form factor associated with the memory assembly module 100A may be suitably modified (e.g., removing the board's connector keyway) so as to ensure that a memory assembly module embodying the teachings of the present disclosure is not interchangeable with the standard DIMM, thereby preventing any accidental damage."), Figs. 3, 4 (showing memory controller 302 or memory control 408 of host system); Ex. 1028 at 38 (illustrating raw cards B and C with a connector keyway). For example, JESD82-20 (part of the FBDIMM Standards) discloses that there could be large lane-to-lane skew at the DIMM "gold finger." Ex. 1027 at 43. As another example, JESD205 (part of the FBDIMM Standards) discloses that an

FBD includes "PCB edge connector contacts [that] shall be gold-plated" (Ex. 1028 at 84), and that there is a voltage drop between the edge connector and the motherboard (*id.* at 100). Thus, Harris satisfies the PCB "*having an interface configured to fit into a corresponding slot connector of a host system, the interface including a plurality of edge connections*."

228. Harris also discloses edge connections of the interface "*configured to couple power, data, address and control signals between the memory module and the host system*." As shown below in Figure 1A, Harris discloses that the memory module 100A is provided an input 104 from an external voltage source.

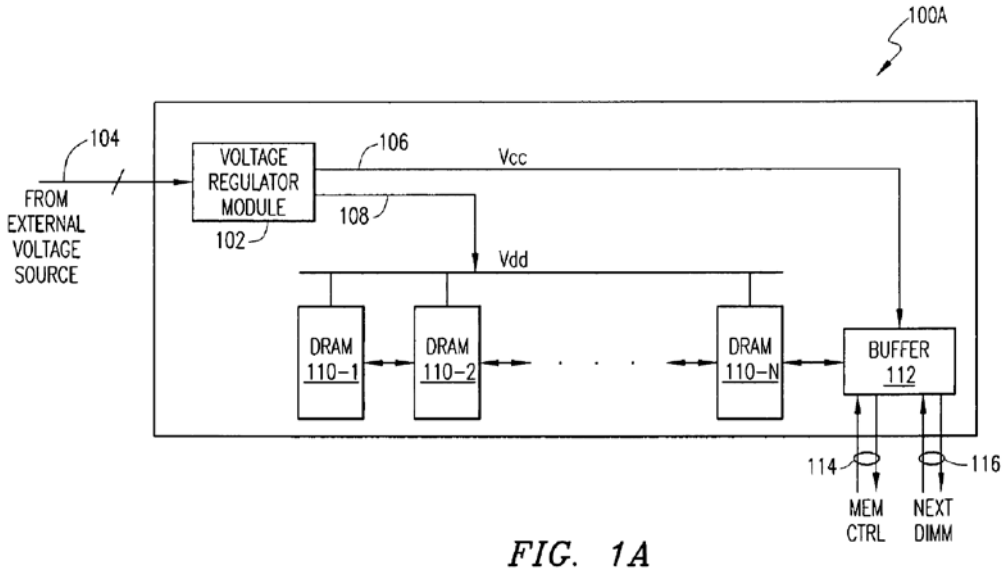


FIG. 1A

Ex. 1023 at Fig. 1A, [0010]. Harris also discloses that a standard FBD module has a connector with a specific number of pins to couple power between the module and host system. *See* Ex. 1023 at [0012] ("By way of example, a standard FBD

module requires 28 Vdd pins (for DRAM devices) and 8 Vcc pins (for buffer and logic) and associated Ground returns, resulting in a total of 72 pins that provide a power supply interface for up to two x4 DRAM ranks (36 devices) and buffer logic."). Harris also provides examples of voltage-independent designs with differing number of pins for power. *See id.* (describing designs with six pins, 12 pins, and 24 pins); *see also id.* at [0019] ("reduction in the pin count on DIMM connector to system board").

229. Harris also discloses a connector with pins for data, address, and control signals between the memory module and host system. As shown below in Figure 1A of Harris, the buffer 112 of memory module 100A is coupled to a bidirectional memory controller interface path 114 and a daisy-chain interface 116 to the next DIMM.

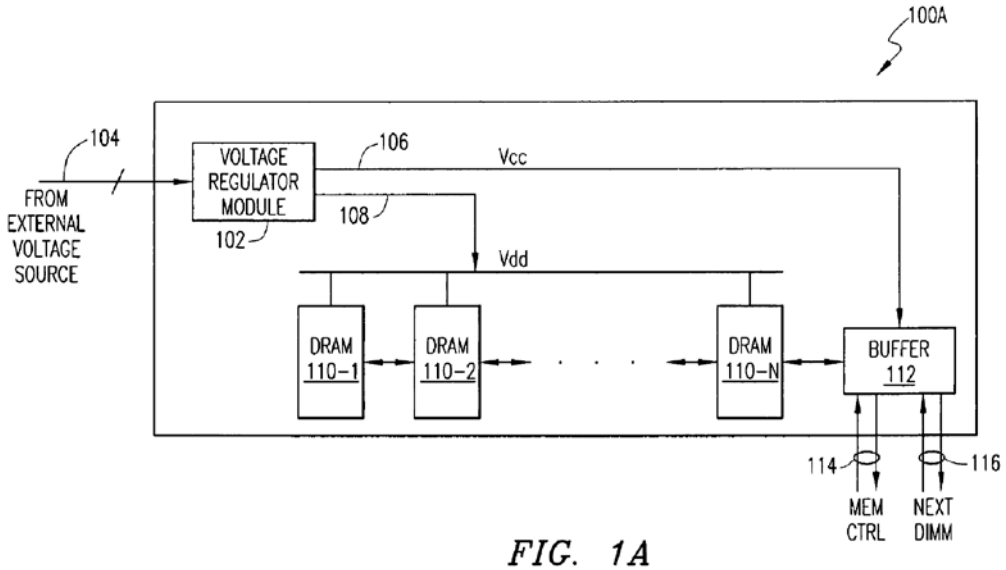
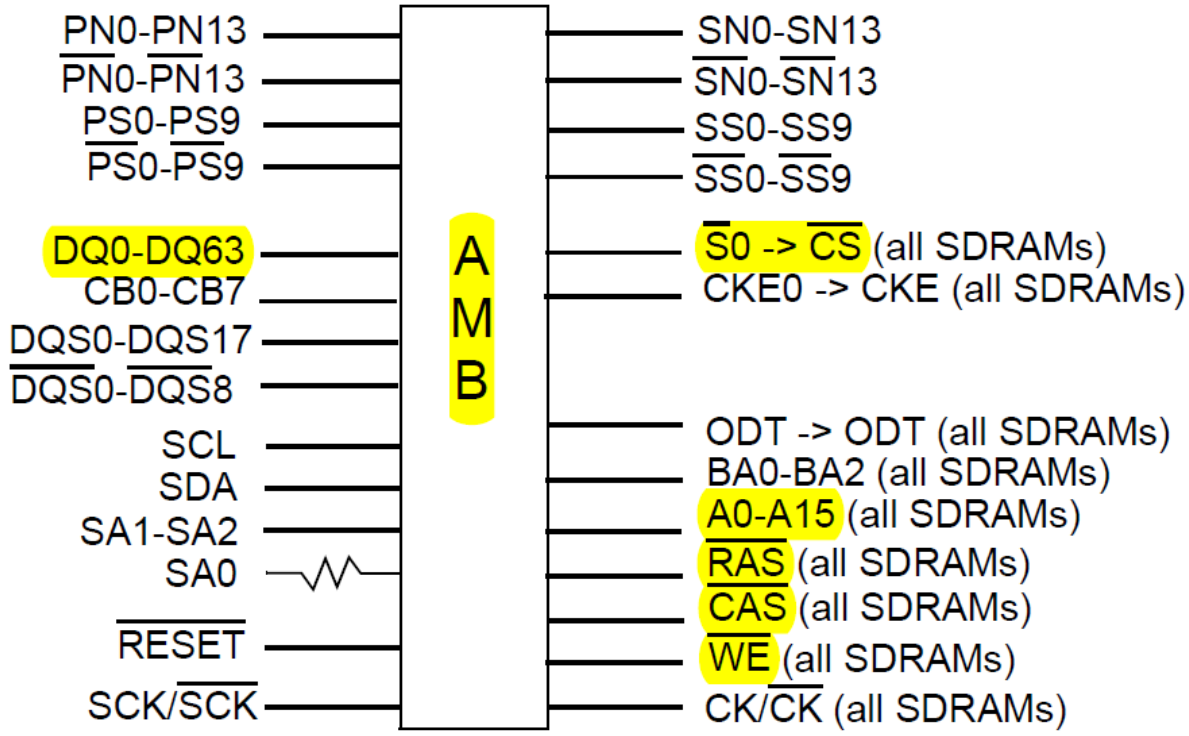


FIG. 1A

Id. at Fig. 1A; *see also id.* at Fig. 3 (buffer 314 and bidirectional memory link 304), [0017] (describing Fig. 3). A Skilled Artisan would have recognized that these connections couple data, address, and control signals. For example, Harris discloses that the buffer 112 is provided for "buffering ***command/address (C/A)*** space as well as ***data*** space at least for a portion of the memory devices 110-1 through 110-N." *Id.* at [0009] (emphasis added). In addition, Figure 1A of Harris identifies the bidirectional memory controller path 114 as for "MEM CTRL" or memory control.

230. A Skilled Artisan would also have recognized that an FBDIMM connector, such as the one disclosed in Figures 1A and 3 of Harris, couples data, address, and control signals between the DIMM and host system. For example, below is an excerpt of a block diagram for Raw Card Version A from JESD205 (part of the FBDIMM Standards).



Ex. 1028 at 13 (excerpted); *see also id.* at 29 (AMB Pin Description). As shown, the AMB is coupled to multiple data signals (e.g., DQ0-DQ63), address signals (e.g., A0-A15), and control signals (e.g., RAS, CAS, WE, CS). *Id.*; *see also* Ex. 1026 (JESD79-2B) at 6, 46-47, 52. The AMB is also coupled to multiple signals for bi-directional communication, such as the Primary Northbound (e.g., PN0-PN13) and Primary Southbound (e.g., PS0-PS9) links. A Skilled Artisan would have recognized that the AMB buffers and converts the bi-directional communications with data, address, and control signal information into data, address, and control signals for the memory devices. For example, the block diagram for Raw Card Version A from JESD205 (part of the FBDIMM Standards)

indicates that the data, address, and control signals are for "all SDRAMs." Ex. 1028 at 13. This indicates to a Skilled Artisan that the signals are provided for the memory devices on the DIMM. As another example, JESD82-20 (part of the FBDIMM Standards) discloses that each link to the AMB connects the AMB "to a host memory controller or an adjacent FBD." Ex. 1027 at 4. A block diagram of these connections is shown in Figure 1.2 below.

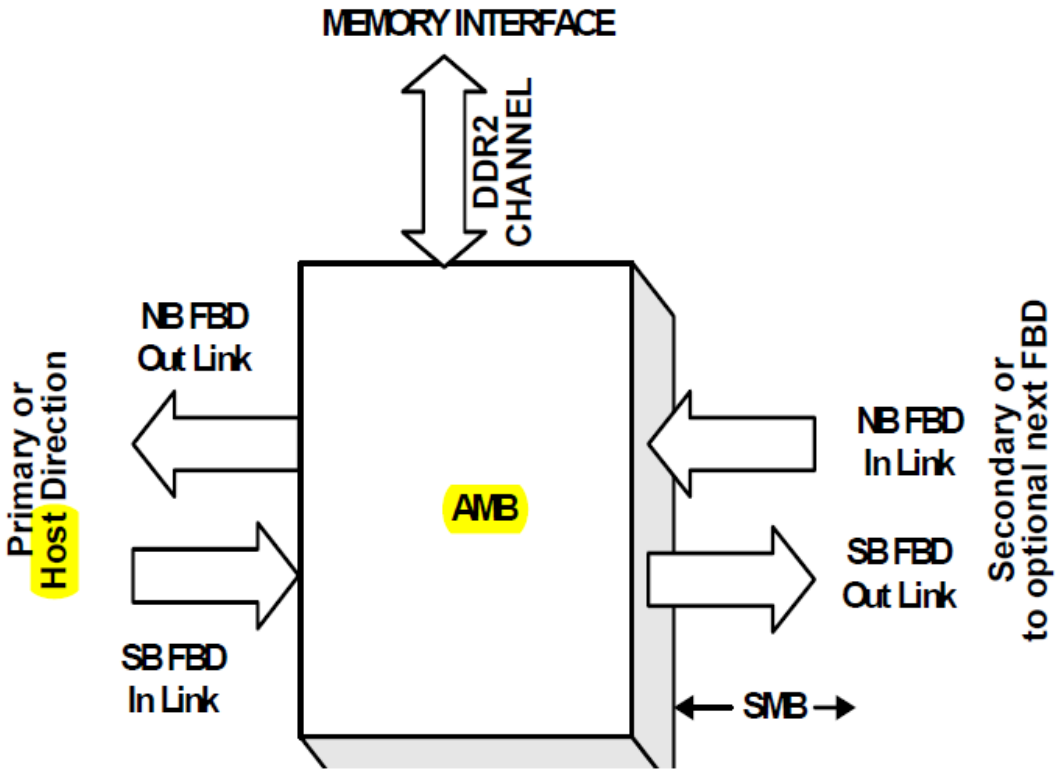


Figure 1.2 — Advanced Memory Buffer Interfaces

Id. JESD82-20 also discloses the following block diagram of the AMB.

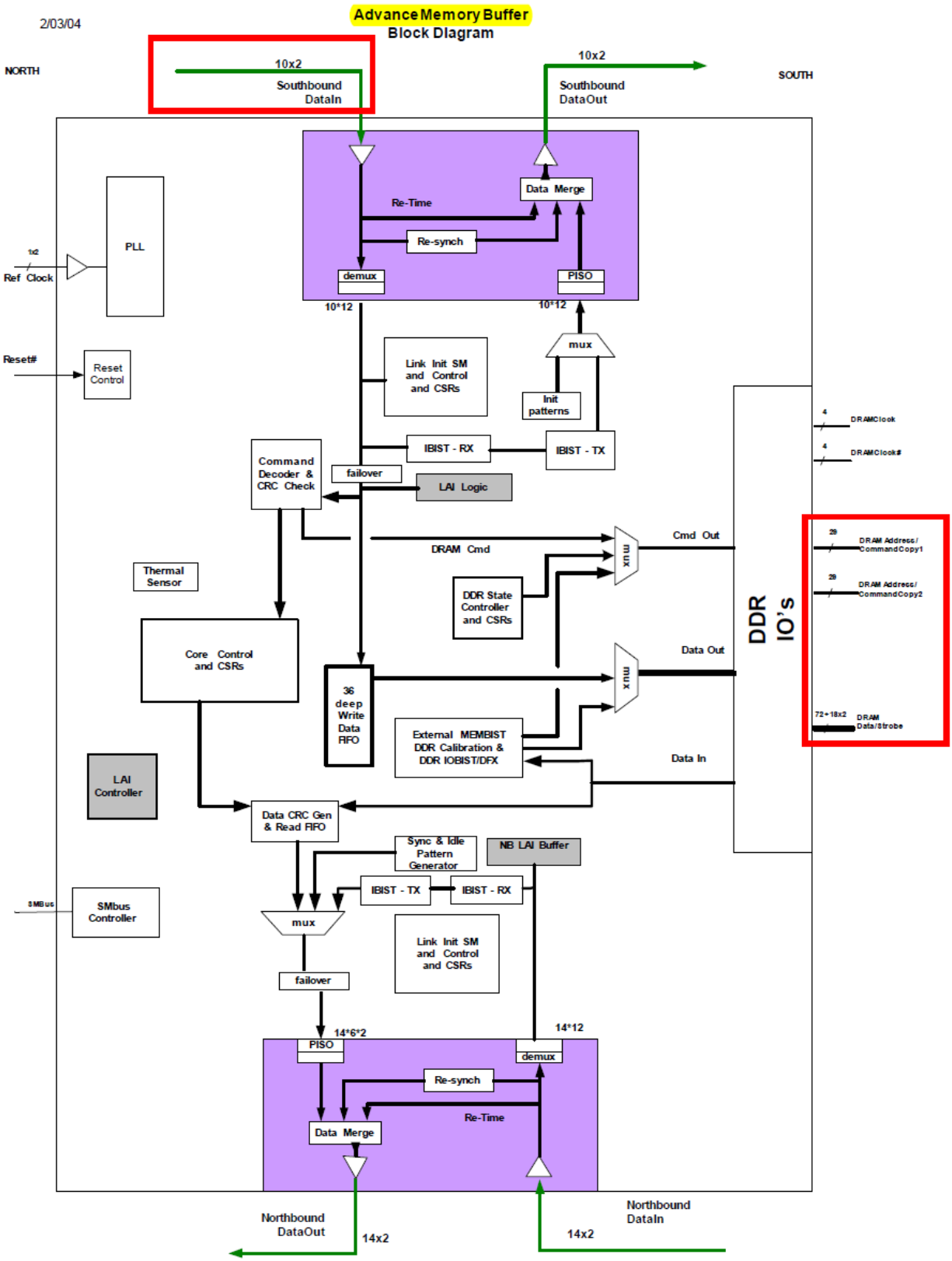


Figure 1.1 — Advanced Memory Buffer Block Diagram

See id. at 3 (Figure 1.1). As shown, the data flow of the AMB includes conversion of bi-directional communications, such as those on the Northbound and Southbound links, into data, address, and control signals for the memory devices, such as the signals coupled to the "DDR IO's" block. Harris satisfies "*configured to couple power, data, address and control signals between the memory module and the host system*."

231. Accordingly, Harris alone, or in combination with the FBDIMM Standards, satisfies "*a printed circuit board (PCB) having an interface configured to fit into a corresponding slot connector of a host system, the interface including a plurality of edge connections configured to couple power, data, address and control signals between the memory module and the host system.*"

c) [1.c] A First Buck Converter

232. Claim 1 requires "*a first buck converter configured to provide a first regulated voltage having a first voltage amplitude.*"

233. The prior art references in each of Grounds 1 through 3 teach this limitation to a Skilled Artisan.

234. Harris discloses a memory module with an on-board voltage regulator module (VRM) to convert an externally supplied voltage level to appropriate local voltage levels. Ex. 1023 at [0010] ("[A]t least one on-board voltage regulator module (VRM) is provided as part of the memory board assembly module 100A

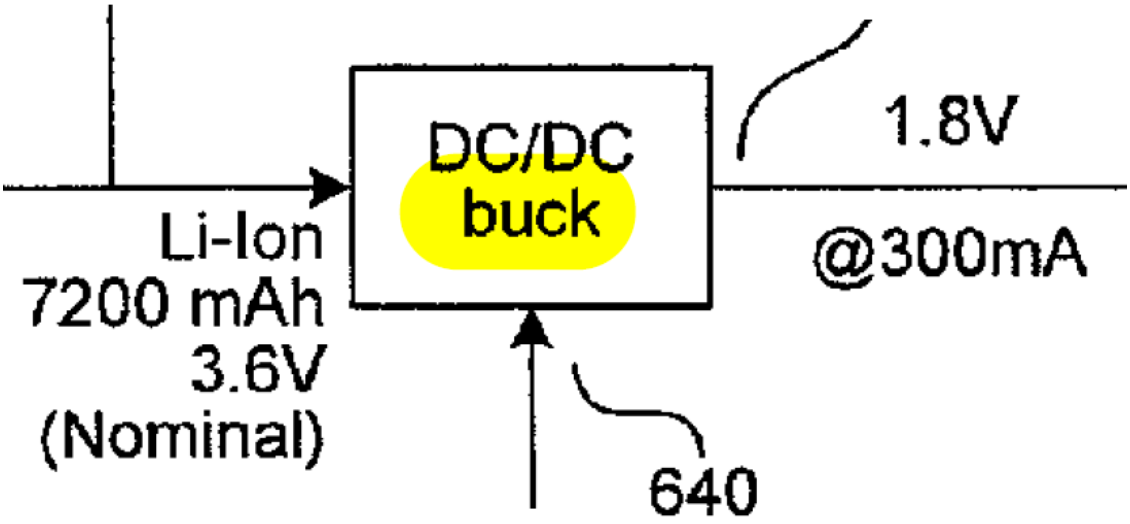
for converting an externally supplied voltage level available on external source path 104 into appropriate local voltage levels that power the first and second voltage paths, i.e., the Vdd and Vcc paths 108, 106, respectively."). According to Harris, the on-board conversion is preferably implemented using a high-frequency switching voltage converter. *Id.* ("Preferably, a high-frequency switching voltage converter capable of generating tightly-controlled voltage levels."). A Skilled Artisan would have recognized the "tightly-controlled voltage level" generated by the high-frequency switching voltage converter, as Harris discloses, is a "*regulated voltage"* as required by the claim.

235. Harris also discloses examples of the externally supplied voltage level and appropriate local voltage levels. For example, the externally supplied voltage level is implemented as 12-volts with as few as six pins. *See id.* at [0012] ("A voltage-independent FBD design incorporating the embodiment of FIG. 1A is capable of replacing these power supply interface pins with ***as few as six +12V pins (from an external voltage source)***, with local conversion to Vdd (to DRAM) and Vcc (to buffer/logic) being added. Alternatively, using additional power supply pins would provide the capability to support even more devices. For instance, with 12 supply pins (at +12V), the embodiment of FIG. 1A can provide enough power to supply 4 ranks (i.e., 72 devices). Likewise, a memory assembly of 8 ranks (144 devices) may be powered with 24 pins at +12V.") (emphasis

added). Also, the appropriate local voltage levels for the Vdd and Vcc supplies range from around 0.5 to 3.5 volts. *See id.* at [0009] ("a first voltage path 108, typically referred to as a Vdd path, that may be energized to appropriate voltage levels depending on the type, functionality, and design of the memory devices, e.g., ***from about 0.5V to 3.5V or more***" and "a second voltage path 106, typically referred to as a Vcc path, are provided with respect to the buffer component 112, wherein the Vcc path may be energized to appropriate voltage levels depending on the buffer and DIMM technology, e.g., ***from about 0.5V to 3.5V or more***") (emphasis added).

236. A Skilled Artisan would have understood it would have been obvious to implement the high-frequency switching converter in Harris that steps down the input voltage (e.g., 12 volts) to lower output voltage (e.g., less than 3.5 volts) as a "*buck converter configured to provide a first regulated voltage*" as required by the claim. As explained above, buck converters were well-known switching devices commonly used to step down the voltage between its input and output. *Supra* ¶¶146-149; *see also* Ex. 1058 at 3 (describing Fig. 1-3), 5 (Fig. 1-3, "1.3 Switching-Regulatory Theory," "The output voltage V_O is always equal to the input voltage V_{IN}, times the duty cycle D, or $V_O = DV_{IN}$."), 12-16 ("1.5.4. Buck or Step-Down"); Ex. 1032 at 161 (step-down or buck converter is a "basic converter topolog[y]."), 164 ("[a]s the name implies, a step-down converter produces a lower

average output voltage than the dc input voltage V_d."); Ex. 1024 at Fig. 6 (showing a DC/DC buck converter 640 to step down a higher voltage to a lower one, reproduced below in part, annotated).



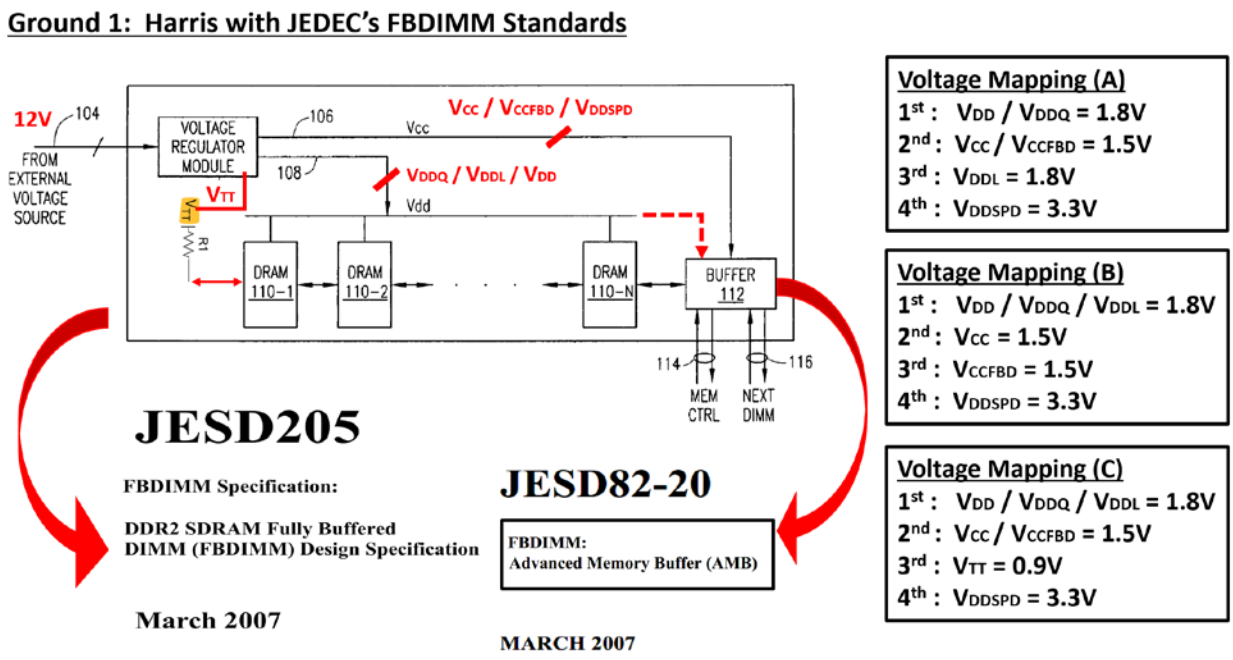
In fact, a buck converter was a conventional device that a Skilled Artisan would have recognized as a voltage-reducing implementation of "a ***high-frequency switching voltage converter*** capable of generating tightly-controlled voltage levels," as disclosed by Harris (Ex. 1023, at [0012, 0010]), because a "***voltage-reducing switching converter***" was commonly referred to as a "***buck converter***." Ex. 1030 (Boldo), 2:41-43; *see also id.* at 2:32-40, 5:34-44.

237. In addition, a Skilled Artisan would have understood, and been motivated by, the fact that a buck converter efficiently steps down the voltage without generating excess heat or requiring excessively large cooling devices. For example, U.S. Patent No. 7,061,214 to Mayega *et al.* states that "[s]witch mode

buck converters have become popular due to two attractive features: first, they are more efficient than traditional low drop out regulators (LDO) (e.g., up to 95%) and second, ***they can provide relatively high currents with lower power dissipation on chip than an LDO can***." Ex. 1059 at 5:23-30 (emphasis added); *see also* Ex. 1034 at 1:58-2:1 (describing charge pump circuits as "generally inefficient and consume large amounts of current"); Ex. 1040 (Texas Instruments TPS51020) at 1 (describing "high efficiency applications" across loads), Figs. 22-25 (showing efficiency versus output current); Ex. 1041 (FAN5026 Dual DDR/Dual-Output PWM Controller) at 1, 13 (describing high efficiency operation "over a wide range of loads"); Ex. 1048 at 3 (specifying an efficiency of 75%); Ex. 1058 at 5 ("1.3 Switching-Regulator Theory") ("The high efficiency of switching regulators is the result of operating the series transistor in a switching mode."); Ex. 1062 at 11 (explaining that "lower dissipation" of electronic devices, such as a Class D amplifier, "saves the cost (and space) of cooling apparatus like heat sinks or fans"); Ex. 1064 at [0101] (discussing "Power loss algo[r]ithm" to flash DRAM to FLASH during a "power los event" in which the "VR Efficiency" is 85%).

(1) Ground 1: VDD, VDDQ, or VDDL at 1.8 Volts

238. For Ground 1, Harris in view of the FBDIMM Standards discloses the claimed "*regulated voltage[s]*," including the following three voltage mappings shown in the figure below.



Ex. 1023 at Fig. 1A (annotated). In Grounds 1B and 1C, the VDD, VDDQ, or VDDL voltage supply is the "*first regulated voltage*" at 1.8 volts ("*having a first voltage amplitude*"). And, in Ground 1A, the VDD or VDDQ voltage supply is the "*first regulated voltage*" at 1.8 volts ("*having a first voltage amplitude*").

239. Harris discloses, for example, that the VDD supply is 1.8 volts for DDR2 memory devices. Ex. 1023 at Fig. 1A; [0009]. In particular, Harris explains that the memory devices on the memory module "can be of any known or heretofore unknown DDR type, e.g., DDR2 (operable with 1.8 V)." *Id.* at [0009]. A Skilled Artisan would have recognized that, as disclosed by the relevant JEDEC standards, an implementation of Harris with DDR2 memory devices couples those devices to multiple, separate voltage sources, called VDD, VDDQ, and VDDL, which each provide a 1.8-volt supply.

240. For example, JESD205 (part of the FBDIMM Standards) discloses that the memory devices (DRAM) are provided several supply voltages, as shown in the table below.

	min	typ	max	
Supply voltages (nominal)	1.7	1.8	1.9	(DRAM V_{DD}/V_{DDQ}, AMB V_{DDQ})
	1.455[1]	1.5	1.575[1]	(AMB V_{CC}/V_{CCFBD})
	0.453*V_{DD}	0.5*V_{DD}	0.547*V_{DD}	(DRAM Interface V_{TT}) This supply should track as 0.5 * 1.8 volt supply

Ex. 1028 at 9 (excerpted). As shown, the DRAM is provided VDD and VDDQ, each typically at 1.8 volts. *Id.* JESD205 also discloses the pin assignments of DDR2 SDRAM memory, which include a VDDL supply voltage. *See id.* at 17-20.

241. A Skilled Artisan would have recognized the VDDL voltage supply for DDR2 SDRAM memory and its voltage amplitude of 1.8 volts. For example, JESD79-2B discloses that VDDL, similar to VDD and VDDQ, has a voltage amplitude of 1.8 volts. Ex. 1026 at pp.6-7.

242. JESD79-2B also discloses that, in one implementation, the three voltage supplies—VDD, VDDQ, and VDDL—can be turned on and off separately, thus suggesting to a Skilled Artisan that these voltages are provided by separate converters. *See* Ex. 1026 at p.9; *see also id.* at pp.2-3 (expressly recommending using an isolated voltage source for VDDL). In the combinations of Grounds 1-3, Harris discloses that the input voltage (e.g., 12 volts) to the high-frequency switching voltage converter is higher than the output voltage (e.g., 1.8 volts for

VDD, VDDQ, or VDDL). Accordingly, a Skilled Artisan would have understood, and it would have been obvious to her, to implement each voltage reducing high-frequency switching converters in Harris as a buck converter. *Supra* ¶¶236, 146-149; *see also* Ex. 1058 at 3, 5, 12-16, Fig. 1-3; Ex. 1032 at 161, 164; Ex. 1030 at 2:32-43, 5:39-44; Ex. 1024 at Fig. 6; Ex. 1062 (ADI Power Supply Management) at 13 ("In addition, a particular standard voltage level may have to be independently furnished in numerous places. For example, separate analog- and digital supplies … may be required. Generating the same voltage numerous times may be necessary to improve efficiency … or to meet sequencing requirements"). Thus, a Skilled Artisan would have recognized that any of the converters generating VDD, VDDQ, or VDDL satisfies this limitation as each converts a higher voltage (e.g., 12 volts) to a lower one at, for example, 1.8 volts.

243. Accordingly, Harris alone, or in view of the FBDIMM Standards, (Ground 1) satisfies this limitation.

(2) Grounds 2 and 3: VDD, VDDQ, or VDDL at 1.8 Volts, or VTT at 1.25 Volts

244. For Ground 2 (Ground 1 in view of Amidi) and Ground 3 (Ground 2 in view of Hajeck), there are four mappings for the "*regulated voltage[s]*," as shown in the figures below. The Voltage Mappings for Ground 3 are the same as Ground 2.

Ground 2: Ground 1 and Battery Backup of Amidi

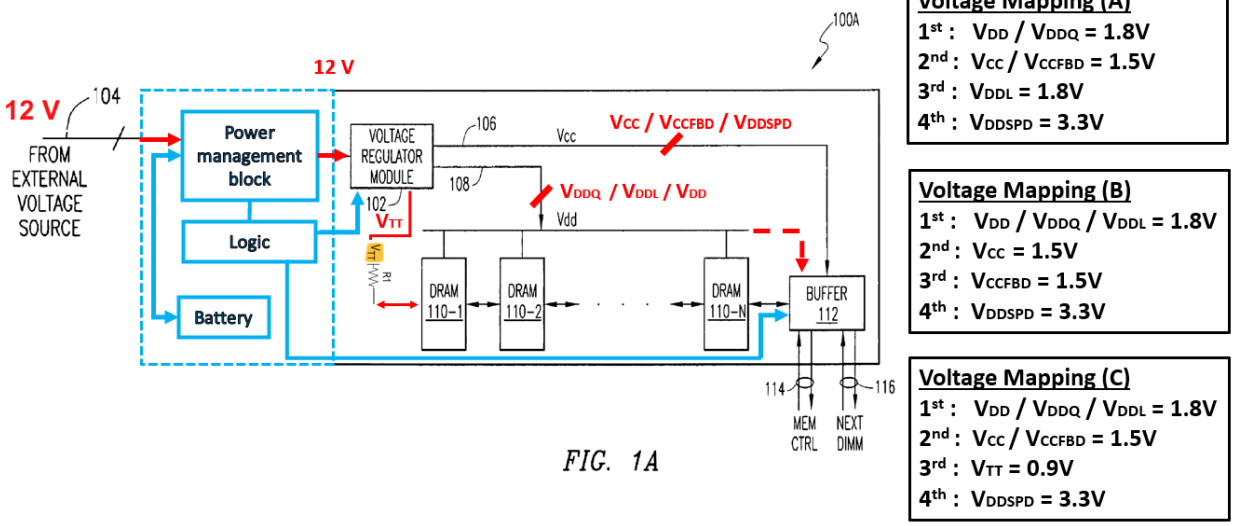


FIG. 1A

Grounds 2A-2C and 3A-3C have the same voltage mapping as Grounds 1A-1C. As discussed above for Ground 1, Harris alone, or in view of the FBDIMM Standards, satisfies this claim limitation. *Supra* ¶¶238-243.

245. For Grounds 2D and 3D, the VTT voltage supply is the "*first regulated voltage*" at 1.25 volts ("*having a first voltage amplitude*"), as shown below.

Ground 2: Ground 1 and Battery Backup of Amidi

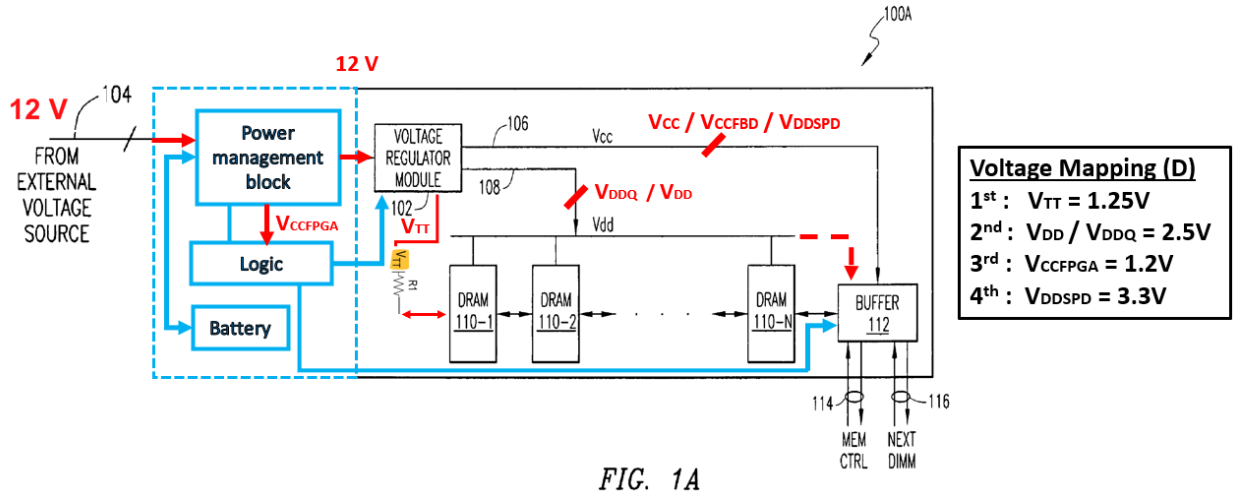


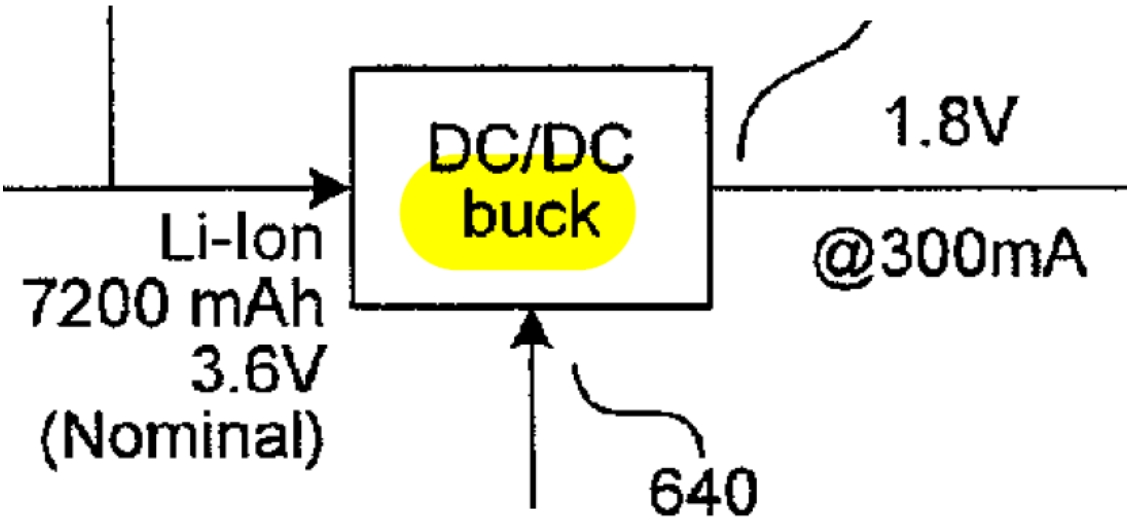
FIG. 1A

246. Harris discloses, for example, that the VDD supply is 2.5 volts for certain memory devices. Ex. 1023 at [0002] (explaining that ""each generation of DIMM/DRAM technology requires a different power supply which keeps getting lower (e.g., 3.3V, **2.5V**, 1.8V, 1.5V and beyond)") (emphasis added); *see also id.* at [0009] ("energized to appropriate voltage levels" depending on "the type, functionality, and design of the memory devices" and on "the buffer and DIMM technology"). A Skilled Artisan would have recognized that a VDD and/or VDDQ voltage supply of 2.5 volts is required for certain DDR SDRAM devices. *See, e.g.*, Ex. 1045 (JESD79) at 1 ("+2.5 V ±0.2 V"); *see also id.* at 7 (same).

247. A Skilled Artisan would have also understood that DDR SDRAM devices require an input/output termination voltage VTT "for signal termination resistors" coupled to the memory devices. *See* Ex. 1045 at 60 ("VTT is not applied directly to the device. VTT is a system supply for signal termination resistors . . . ."). VTT is set equal to a reference voltage, VREF, which is approximately one-half of VDDQ or 1.25 volts. *Id.* ("VTT is a system supply for signal termination resistors . . . is expected to be set equal to VREF"); *see also id.* at p.54 (disclosing electrical characteristics and DC operating conditions for VREF and VTT); Ex. 1028 at 9 (disclosing that the DRAM is also provided an interface supply voltage VTT, which is typically one-half the voltage of VDD, or in the example of DDR2 SDRAM memory, 0.9 volts). Accordingly, Harris teaches a VTT voltage

supply at 1.25 volts, and Harris alone, or in view of the FBDIMM Standards, and further in view of Amidi (Ground 2) and further in view of Hajeck (Ground 3) satisfies this limitation.

248. Further, a Skilled Artisan would have understood it would have been obvious to implement a high-frequency switching converter in Harris that steps down the input voltage (e.g., 12 volts) to lower output voltage (e.g., at 1.25 volts) as a "*buck converter configured to provide a first regulated voltage*" as required by the claim. As explained above, buck converters were well-known switching devices commonly used to step down the voltage between its input and output. *Supra* ¶¶146-149; *see also* Ex. 1058 at 3 (describing Fig. 1-3), 5 (Fig. 1-3, "1.3 Switching-Regulatory Theory," "The output voltage V_O is always equal to the input voltage V_{IN}, times the duty cycle D, or $V_O = DV_{IN}$."), 12-16 ("1.5.4. Buck or Step-Down"); Ex. 1032 at 161 (step-down or buck converter is a "basic converter topolog[y]."), 164 ("[a]s the name implies, a step-down converter produces a lower average output voltage than the dc input voltage V_d."); Ex. 1030 at 2:32-43, 5:39-44 (describing "a buck converter (a voltage-reducing switching converter)"); Ex. 1024 at Fig. 6 (showing a DC/DC buck converter 640 to step down a higher voltage to a lower one, reproduced below in part, annotated).



249. Accordingly, Harris in view of the FBDIMM Standards, further in view of Amidi (Ground 2), and further in view of Hajeck (Ground 3) satisfies "*a first buck converter configured to provide a first regulated voltage having a first voltage amplitude*."

d) [1.d] A Second Buck Converter

250. Claim 1 requires "*a second buck converter configured to provide a second regulated voltage having a second voltage amplitude*."

251. The prior art references in each of Grounds 1 through 3 teach this limitation to a Skilled Artisan.

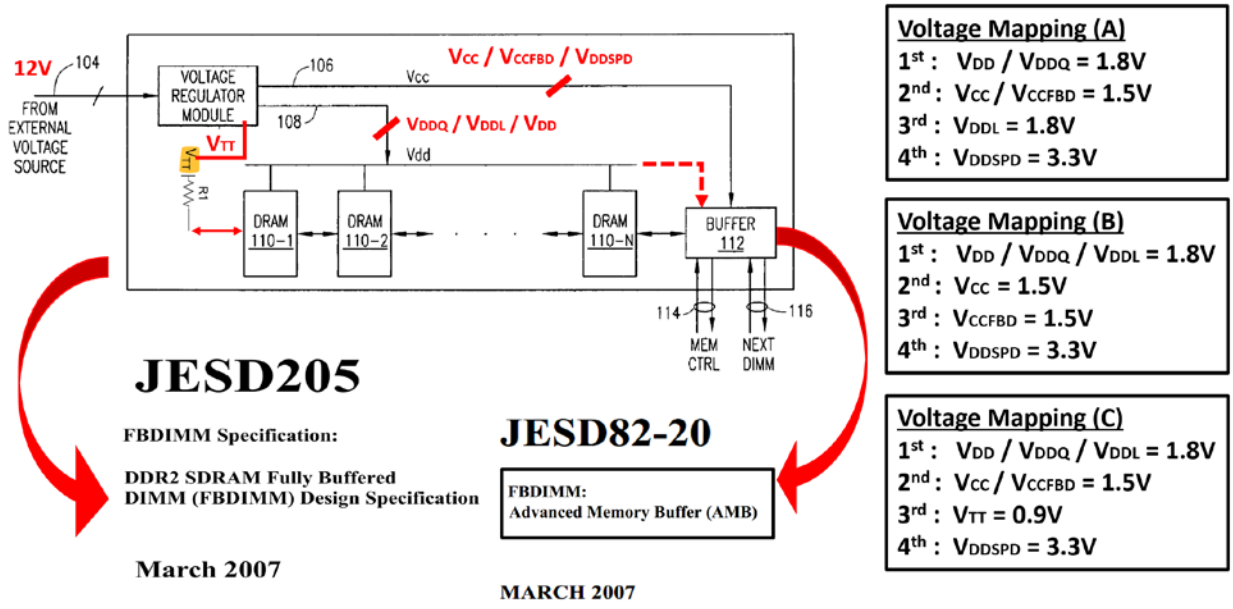
252. As explained above, Harris discloses at least one on-board voltage regulator module (VRM) is provided on the memory module that is preferably implemented using a high-frequency switch voltage converter that provides a regulated voltage. *Supra* ¶233; Ex. 1023 at [0010]. Harris also discloses examples

of the externally supplied voltage level and appropriate local voltage levels. *Supra* ¶236; Ex. 1023 at [0012]. For example, the externally supplied voltage level is implemented as 12-volts with as few as six pins, and the appropriate local voltage levels include the Vdd and Vcc supplies that range from around 0.5 to 3.5 volts. *Supra* ¶236; Ex. 1023 at [0009]. As explained, a Skilled Artisan would have understood it would have been obvious to implement the high-frequency switching converter in Harris that steps down the input voltage (e.g., 12 volts) to lower output voltage (e.g., less than 3.5 volts) as a "*buck converter*." *Supra* ¶¶236, 146-149; *see also* Ex. 1058 at 3, 5, 12-16, Fig. 1-3; Ex. 1032 at 161, 164; Ex. 1030 at 2:32-43, 5:39-44; Ex. 1024 at Fig. 6.

(1) Grounds 1A-1C, 2A-2C, and 3A-3C: VCC or VCCFBD at 1.5 Volts

253. For Grounds 1A-1C (Harris in view of the FBDIMM Standards), Grounds 2A-2C (Ground 1 in view of Amidi), and Grounds 3A-3C (Ground 2 in view of Hajeck), there are at least three mappings for the "*regulated voltage[s]*," as shown in the figures below, any of which meets this limitation. The voltage mappings of Ground 3 are the same as Ground 2.

Ground 1: Harris with JEDEC's FBDIMM Standards



Voltage Mapping (A)
1st : VDD / VDDQ = 1.8V
2nd : VCC / VCCFBD = 1.5V
3rd : VDDL = 1.8V
4th : VDDSPD = 3.3V

Voltage Mapping (B)
1st : VDD / VDDQ / VDDL = 1.8V
2nd : VCC = 1.5V
3rd : VCCFBD = 1.5V
4th : VDDSPD = 3.3V

Voltage Mapping (C)
1st : VDD / VDDQ / VDDL = 1.8V
2nd : VCC / VCCFBD = 1.5V
3rd : VTT = 0.9V
4th : VDDSPD = 3.3V

Ground 2: Ground 1 and Battery Backup of Amidi

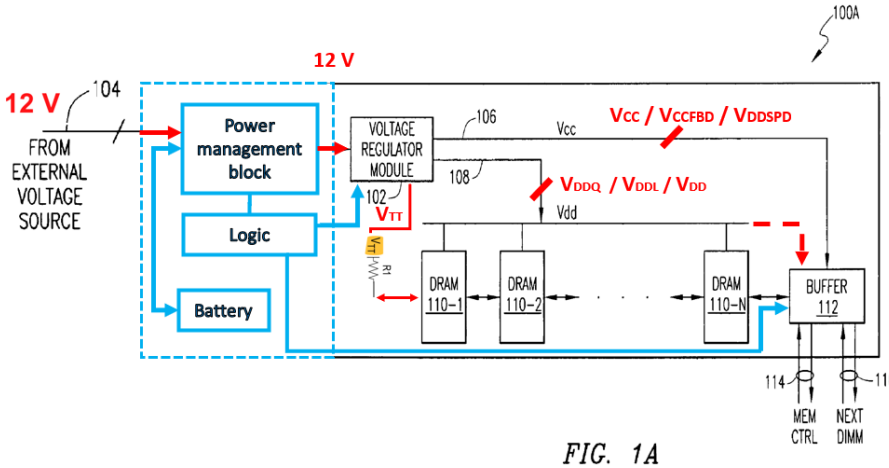


FIG. 1A

Voltage Mapping (A)
1st : VDD / VDDQ = 1.8V
2nd : VCC / VCCFBD = 1.5V
3rd : VDDL = 1.8V
4th : VDDSPD = 3.3V

Voltage Mapping (B)
1st : VDD / VDDQ / VDDL = 1.8V
2nd : VCC = 1.5V
3rd : VCCFBD = 1.5V
4th : VDDSPD = 3.3V

Voltage Mapping (C)
1st : VDD / VDDQ / VDDL = 1.8V
2nd : VCC / VCCFBD = 1.5V
3rd : VTT = 0.9V
4th : VDDSPD = 3.3V

Ex. 1023 at Fig. 1A (annotated). In Grounds 1A, 1C, 2A, 2C, 3A, and 3C, the VCC or VCCFBD voltage supply is the "*second regulated voltage*" at 1.5 volts ("*having a second voltage amplitude*"). And, in Grounds 1B, 2B, and 3B, the VCC voltage supply is the "*second regulated voltage*" at 1.5 volts ("*having a second voltage amplitude*").

254. In addition to the "*first regulated voltage*" discussed above, Harris also discloses a "*second regulated voltage*," such as VCC. *Supra* ¶¶232-249; Ex. 1023 at Fig. 1A. In particular, VCC is generated by voltage regulator module 102 and provided to buffer 112. Ex. 1023 at Fig. 1A. As discussed above with reference to claim limitation [1.c], Harris discloses to a Skilled Artisan that it would have been obvious to implement the voltage regulator module as high-frequency switching converters that are buck converters, which includes using a buck converter to provide Vcc to buffer 112. *Supra* ¶¶236, 146-149; *see also* Ex. 1058 at 3, 5, 12-16, Fig. 1-3; Ex. 1032 at 161, 164; Ex. 1030 at 2:32-43, 5:39-44; Ex. 1024 at Fig. 6; Ex. 1023 at Fig. 1A, [0010], [0012]. Harris also explains that the appropriate voltage levels for the VCC path depend on the buffer and DIMM technology, such as from 0.5 volts to 3.5 volts. Ex. 1023 at [0009] ("In the illustrated embodiment of FIG. 1A, for instance, the DIMM configuration of the memory module 100A is exemplified as a fully buffered DIMM wherein a buffer/logic component 112 is provided for buffering command/address (C/A) space as well as data space at least for a portion of the memory devices 110-1 through 110-N. A bidirectional memory controller interface path 114 as well as a second voltage path 106, typically referred to as a Vcc path, are provided with respect to the buffer component 112, wherein the Vcc path may be energized to

appropriate voltage levels depending on the buffer and DIMM technology, e.g., from about 0.5V to 3.5V or more.").

255. A Skilled Artisan would have recognized that, as disclosed by the relevant JEDEC standards, an implementation of Harris with buffer/logic component 112 for buffering command, address, and data signals requires multiple separate voltage sources in accordance with the relevant JEDEC standards. Ex. 1023 at [0009], Fig. 1A; Ex. 1027 at 83 (listing VCC, VCCFBD, VDD, and VDDSPD power supplies provided to AMB); Ex. 1028 at 9 (listing VDDQ, VCC, and VCCFBD power supplied provided to AMB). In particular, a Skilled Artisan would have recognized that an Advanced Memory Buffer (AMB) for a Fully Buffered DIMM (FB-DIMM) performed the functions Harris describes for buffer/logic component 112. Harris describes memory module 100A in Figure 1A as a "fully buffered DIMM" and explains that buffer/logic component 112 on memory module 100A buffers command, address, and data signals. *See* Ex. 1023 at [0009]. The multiple power supplies for the AMB include VCC and VCCFBD, which are each 1.5 volts. Ex. 1023 at Fig. 1A; Ex. 1027 at 83; Ex. 1028 at 9. Thus, a Skilled Artisan would have recognized that, in Harris's FB-DIMM implementation with the buffer/logic 112 (AMB), the voltage regulator module 102 includes a "*second buck converter*" that converts the input supply voltage

(e.g., 12 volts) down to VCC or VCCFBD supply voltage at 1.5 volts ("*a second regulated voltage having a second voltage amplitude*").

256. Similar to the multiple voltage sources for the memory devices (DRAMs) in Harris (e.g., 1.8 volts for DDR2 SDRAMs), a Skilled Artisan would have recognized that, as disclosed by the relevant JEDEC standards, an implementation of Harris with FBDIMMs couples the AMBs to multiple, separate voltage sources called VCC and VCCFBD. *Supra* ¶¶236, 146-149; *see also* Ex. 1058 at 3, 5, 12-16, Fig. 1-3; Ex. 1032 at 161, 164; Ex. 1030 at 2:32-43, 5:39-44; Ex. 1024 at Fig. 6; Ex. 1023 at Fig. 1A, [0010], [0012]. In particular, the AMB specification, JESD82-20 (part of the FBDIMM Standards), specifies that VCC and VCCFBD each has a voltage level of 1.5 volts. Ex. 1023 at Fig. 1A (annotated above); Ex. 1027 at 78, 82; Ex. 1028 at 9. For example, a Skilled Artisan would have understood that having separate power converters for VCC and VCCFBD, as suggested by the standard by specifying separate power supplies, provides independence of these power supplies to allow improved stability for each supply and flexibility for power management. *See id.*; *supra* ¶242 (citing Ex. 1026 at pp. 2, 3, 9 (explaining that voltage supplies can be turned on and off separately and a voltage can be "isolated")); *see also* Ex. 1062 (ADI Power Supply Management) at 13 ("In addition, a particular standard voltage level may have to be independently furnished in numerous places. For example, separate analog- and digital supplies

… may be required. Generating the same voltage numerous times may be necessary to improve efficiency … or to meet sequencing requirements"). Accordingly, a Skilled Artisan would have recognized that any of the converters generating VCC or VCCFBD satisfies this limitation as each converts a higher voltage (e.g., 12 volts) to a lower one at, for example, 1.5 volts.

257. Accordingly, the prior art references for each of Grounds 1A-1C, 2A-2C, and 3A-3C, alone or in combination, satisfies "*a second buck converter configured to provide a second regulated voltage having a second voltage amplitude.*"

(2) Grounds 2D and 3D: VDD or VDDQ at 2.5 Volts

258. For Ground 2D (Ground 1 (Harris in view of the FBDIMM Standards) further in view of Amidi) and Ground 3D (Ground 2 in view of Hajeck), the VDD or VDDQ voltage supply is the "*second regulated voltage*" at 2.5 volts ("*having a second voltage amplitude*"), as shown in the figure below. The voltage mapping of Ground 3D is the same as Ground 2D.

Ground 2: Ground 1 and Battery Backup of Amidi

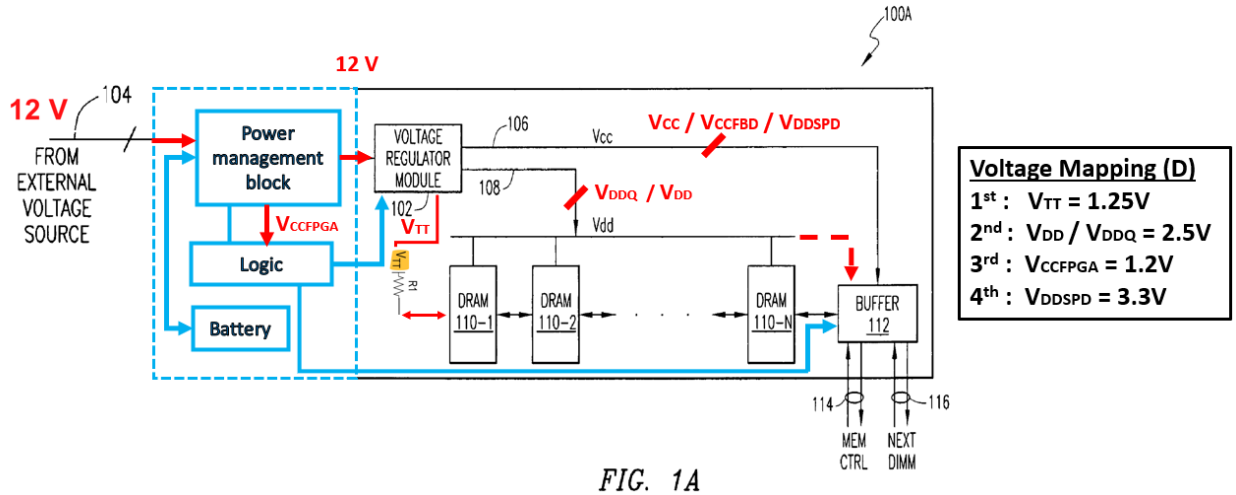


FIG. 1A

259. A Skilled Artisan would have recognized that, as disclosed by the relevant JEDEC standards, an implementation of Harris with DDR SDRAM coupled at least the memory devices to voltage sources called VDD and VDDQ. Ex. 1045 (JESD79) at 1, 7, and 54 (describing VDD and VDDQ for DDR SDRAM, both at nominal value of 2.5V); *Supra* ¶¶236, 146-149; *see also* Ex. 1058 at 3, 5, 12-16, Fig. 1-3; Ex. 1032 at 161, 164; Ex. 1030 at 2:32-43, 5:39-44; Ex. 1024 at Fig. 6. A Skilled Artisan would have understood that VDD/VDDQ is also coupled to the Buffer 112 so that it can communicate with the SDRAMs in accordance with the voltage requirements of the SDRAM interface. *See, e.g.*, Ex. 1027 (JESD82-20) at 31-32 (AMB receiving "V_{DD} Supply voltage DRAM interface"), 44 (describing DRAM interface on AMB receiving V_{DD}), 83 (same), Ex. 1028 at 9 (V_{DD}/V_{DDQ} for DRAM and AMB), 11, 13-16, 30, 33 (same); *see also* Ex. 1045 (JESD79) at 54-60 (describing AC and DC characteristics of DDR

SDRAMs). As explained above for claim limitation [1.c] and Grounds 2D and 3D, the VTT voltage supply at 1.25 volts is the "first regulated voltage having a first voltage amplitude." *Supra* ¶¶245-249. As explained, VTT is set equal to a reference voltage, VREF, which is approximately one-half of VDDQ or 1.25 volts. *Id.*; *see* Ex. 1045 at 60; *see also supra* ¶254. Accordingly, VDDQ is 2.5 volts. In addition, Harris discloses, for example, that the VDD supply is 2.5 volts for certain memory devices. Ex. 1023 at [0002] (explaining that ""each generation of DIMM/DRAM technology requires a different power supply which keeps getting lower (e.g., 3.3V, **2.5V**, 1.8V, 1.5V and beyond)") (emphasis added). A Skilled Artisan would have recognized that a VDD and/or VDDQ voltage supply of 2.5 volts is required for certain DDR SDRAM devices. *See, e.g.*, Ex. 1045 (JESD79) at 1 ("+2.5 V ±0.2 V"); *see also id.* at 7 and 54 (same).

260. A Skilled Artisan would have understood that having separate power converters for VDD and VDDQ, as suggested by the standard by specifying separate power supplies, provides independence of these power supplies to allow improved stability for each supply and flexibility for power management. *See id.*; *supra* ¶242 (citing Ex. 1026 at 2, 3, 9 (explaining that voltage supplies can be turned on and off separately and a voltage can be "isolated")). Accordingly, a Skilled Artisan would have recognized that any of the buck converters generating VDD or VDDQ satisfies this limitation as each converts a higher voltage (e.g., 12

volts) to a lower one at, for example, 2.5 volts. *Supra* ¶¶236, 146-149; *see also* Ex. 1058 at 3, 5, 12-16, Fig. 1-3; Ex. 1032 at 161, 164; Ex. 1030 at 2:32-43, 5:39-44; Ex. 1024 at Fig. 6; Ex. 1023 at Fig. 1A, [0010], [0012].

261. Accordingly, Harris in view of the FBDIMM Standards, in view of Amidi (Ground 2D), and further in view of Hajeck (Ground 3D) satisfies "*a second buck converter configured to provide a second regulated voltage having a second voltage amplitude.*"

e) [1.e] A Third Buck Converter

262. Claim 1 requires "*a third buck converter configured to provide a third regulated voltage having a third voltage amplitude*."

263. The prior art references in each of Grounds 1 through 3 teach this limitation to a Skilled Artisan.

264. As explained above, Harris discloses at least one on-board voltage regulator module (VRM) is provided on the memory module that is preferably implemented using a high-frequency switch voltage converter that provides a regulated voltage. *Supra* ¶233; Ex. 1023 at [0010]. Harris also discloses examples of the externally supplied voltage level and appropriate local voltage levels. *Supra* ¶236; Ex. 1023 at [0012]. For example, the externally supplied voltage level is implemented as 12-volts with as few as six pins. *Id.* As explained above, a Skilled Artisan would have understood it would have been obvious to implement the high-

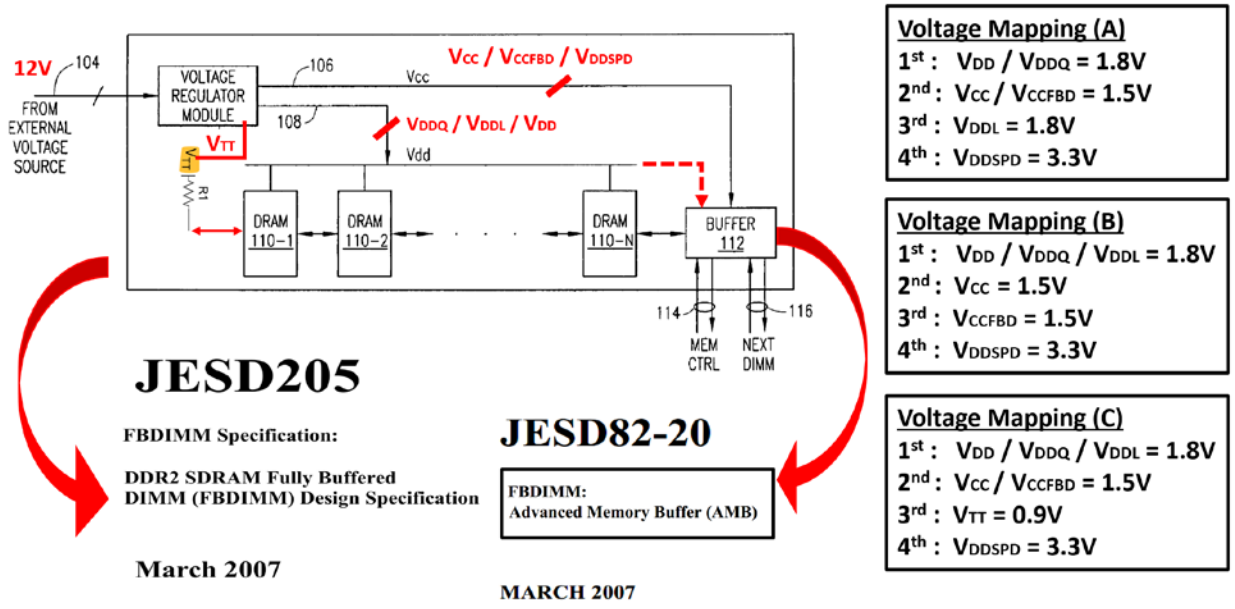
frequency switching converter in Harris that steps down the input voltage (e.g., 12 volts) to lower output voltage (e.g., less than 3.5 volts) as a "*buck converter*." *Supra* ¶¶236, 146-149; *see also* Ex. 1058 at 3, 5, 12-16, Fig. 1-3; Ex. 1032 at 161, 164; Ex. 1030 at 2:32-43, 5:39-44; Ex. 1024 at Fig. 6; Ex. 1023 at Fig. 1A, [0010], [0012].

(1) Grounds 1A, 2A, 3A: VDDL at 1.8 volts

265. I understand that Patent Owner has asserted that two of the claimed "*voltage amplitude[s]*" can be the same. Ex. 1071 at 43 (illustrating two of the alleged buck converters providing the same voltage of 1.1 volts); Ex. 1073 at 49-53 (similar).

266. Under such a claim interpretation, Ground 1A (Harris in view of the FBDIMM Standards), Ground 2A (Ground 1 in view of Amidi), and Ground 3A (Ground 2 in view of Hajeck), teaches a VDDL supply voltage ("*third regulated voltage*") has a voltage amplitude of 1.8 volts ("*having a third voltage amplitude*"), as shown in the figures below. The voltage mapping of Ground 3A is the same as Ground 2A.

Ground 1: Harris with JEDEC's FBDIMM Standards



Voltage Mapping (A)
1st : VDD / VDDQ = 1.8V
2nd : VCC / VCCFBD = 1.5V
3rd : VDDL = 1.8V
4th : VDDSPD = 3.3V

Voltage Mapping (B)
1st : VDD / VDDQ / VDDL = 1.8V
2nd : VCC = 1.5V
3rd : VCCFBD = 1.5V
4th : VDDSPD = 3.3V

Voltage Mapping (C)
1st : VDD / VDDQ / VDDL = 1.8V
2nd : VCC / VCCFBD = 1.5V
3rd : VTT = 0.9V
4th : VDDSPD = 3.3V

Ground 2: Ground 1 and Battery Backup of Amidi

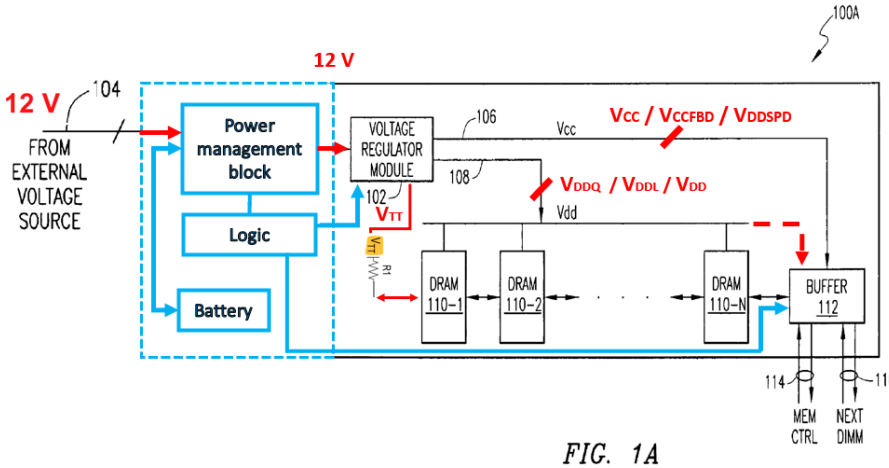


FIG. 1A

Voltage Mapping (A)
1st : VDD / VDDQ = 1.8V
2nd : VCC / VCCFBD = 1.5V
3rd : VDDL = 1.8V
4th : VDDSPD = 3.3V

Voltage Mapping (B)
1st : VDD / VDDQ / VDDL = 1.8V
2nd : VCC = 1.5V
3rd : VCCFBD = 1.5V
4th : VDDSPD = 3.3V

Voltage Mapping (C)
1st : VDD / VDDQ / VDDL = 1.8V
2nd : VCC / VCCFBD = 1.5V
3rd : VTT = 0.9V
4th : VDDSPD = 3.3V

Ex. 1023 at Fig. 1A (annotated).

267. Harris discloses, for example, that the VDD supply is 1.8 volts for DDR2 memory devices. Ex. 1023 at Fig. 1A; [0009]. In particular, Harris explains that the memory devices on the memory module "can be of any known or heretofore unknown DDR type, e.g., DDR2 (operable with 1.8 V)." *Id.* at [0009].

As explained above for claim limitation [1.c], a Skilled Artisan would have recognized that, as disclosed by the relevant JEDEC standards, an implementation of Harris with DDR2 memory devices couples those devices to multiple, separate voltage sources, called VDD, VDDQ, and VDDL, which each provide a 1.8-volt supply. *Supra* ¶239-243. For example, JESD205 (part of the FBDIMM Standards) discloses pin assignments of DDR2 SDRAM memory, which include a VDDL supply voltage. *See* Ex. 1028 at 17-20. A Skilled Artisan would have recognized the VDDL voltage supply for DDR2 SDRAM memory and its voltage amplitude of 1.8 volts. *See* Ex. 1026 at p.6.

268. Moreover, as explained above, a Skilled Artisan would have understood that each of the voltage supplies (VDD, VDDQ, and VDDL) can be turned on and off separately. *See* Ex. 1026 at pp.6-7, 9; *see also id.* at pp.2-3 (expressly recommending using an isolated voltage source for VDDL). In the combinations of Ground 1A, Harris discloses that the input voltage (e.g., 12 volts) to the high-frequency switching voltage converter is higher than the output voltage (e.g., 1.8 volts for VDDL). Accordingly, a Skilled Artisan would have understood it would have been obvious to implement each of the high-frequency switching converters in Harris as a buck converter. *Supra* ¶¶236, 146-149; *see also* Ex. 1058 at 3, 5, 12-16, Fig. 1-3; Ex. 1032 at 161, 164; Ex. 1030 at 2:32-43, 5:39-44; Ex. 1024 at Fig. 6. Thus, a Skilled Artisan would have recognized that the

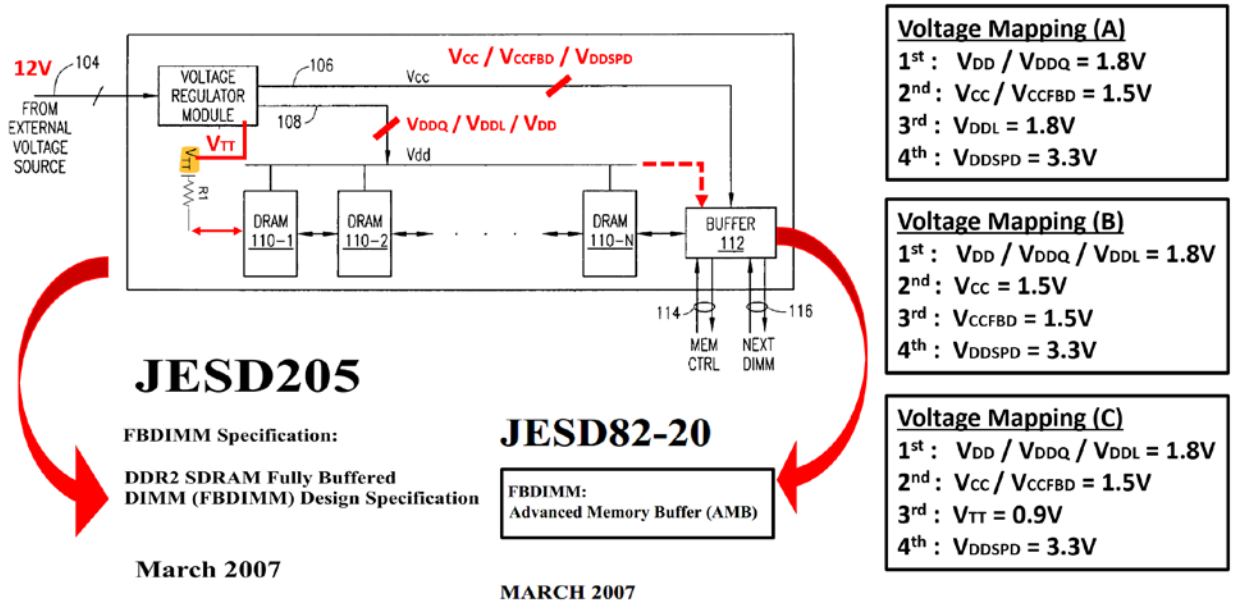
converter generating VDDL satisfies this limitation as each converts a higher voltage (e.g., 12 volts) to a lower one at, for example, 1.8 volts.

269. Accordingly, Harris in view of the FBDIMM Standards, or in further view of Amidi, or in further view of Hajeck (Grounds 1A, 2A, and 3A) satisfies this limitation.

(2) Grounds 1B, 2B, 3B: VCCFBD at 1.5 volts

270. Under Patent Owner's claim interpretation that two of the claimed "*voltage amplitude[s]*" can be the same (*supra* ¶265; Ex. 1071 at 43; Ex. 1073 at 49-53), Ground 1B (Harris in view of the FBDIMM Standards), Ground 2B (Ground 1 in view of Amidi), and Ground 3B (Ground 2 in view of Hajeck), teaches that a VCCFBD supply voltage ("*third regulated voltage*") has a voltage amplitude of 1.5 volts ("*having a third voltage amplitude*"), as shown in the figures below. The voltage mapping of Ground 3B is the same as Ground 2B.

Ground 1: Harris with JEDEC's FBDIMM Standards



Voltage Mapping (A)
1st : VDD / VDDQ = 1.8V
2nd : VCC / VCCFBD = 1.5V
3rd : VDDL = 1.8V
4th : VDDSPD = 3.3V

Voltage Mapping (B)
1st : VDD / VDDQ / VDDL = 1.8V
2nd : VCC = 1.5V
3rd : VCCFBD = 1.5V
4th : VDDSPD = 3.3V

Voltage Mapping (C)
1st : VDD / VDDQ / VDDL = 1.8V
2nd : VCC / VCCFBD = 1.5V
3rd : VTT = 0.9V
4th : VDDSPD = 3.3V

Ground 2: Ground 1 and Battery Backup of Amidi

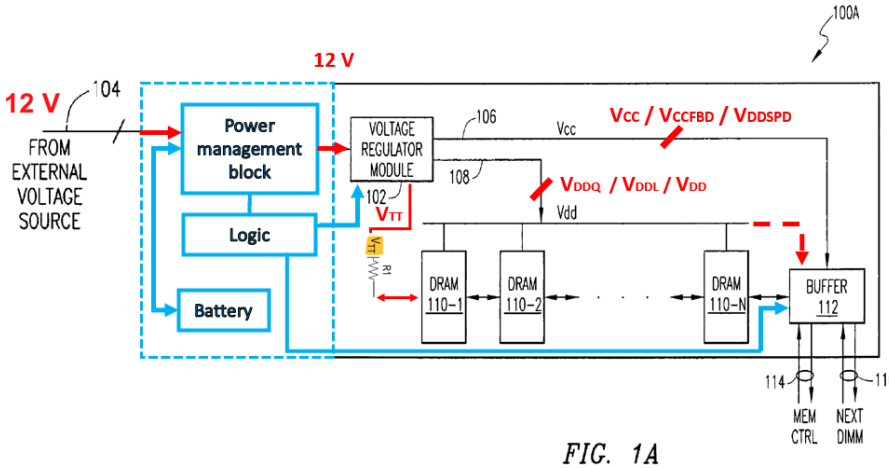


FIG. 1A

Voltage Mapping (A)
1st : VDD / VDDQ = 1.8V
2nd : VCC / VCCFBD = 1.5V
3rd : VDDL = 1.8V
4th : VDDSPD = 3.3V

Voltage Mapping (B)
1st : VDD / VDDQ / VDDL = 1.8V
2nd : VCC = 1.5V
3rd : VCCFBD = 1.5V
4th : VDDSPD = 3.3V

Voltage Mapping (C)
1st : VDD / VDDQ / VDDL = 1.8V
2nd : VCC / VCCFBD = 1.5V
3rd : VTT = 0.9V
4th : VDDSPD = 3.3V

Ex. 1023 at Fig. 1A (annotated).

271. For similar reasons as discussed above with reference to an FB-DIMM and claim limitation [1.d], the FBDIMM AMB standard discloses separate power connections to the AMB for VCC and VCCFBD. Ex. 1027 at 83; Ex. 1028 at 9; *supra* ¶¶250-257. Accordingly, a Skilled Artisans would have understood, and

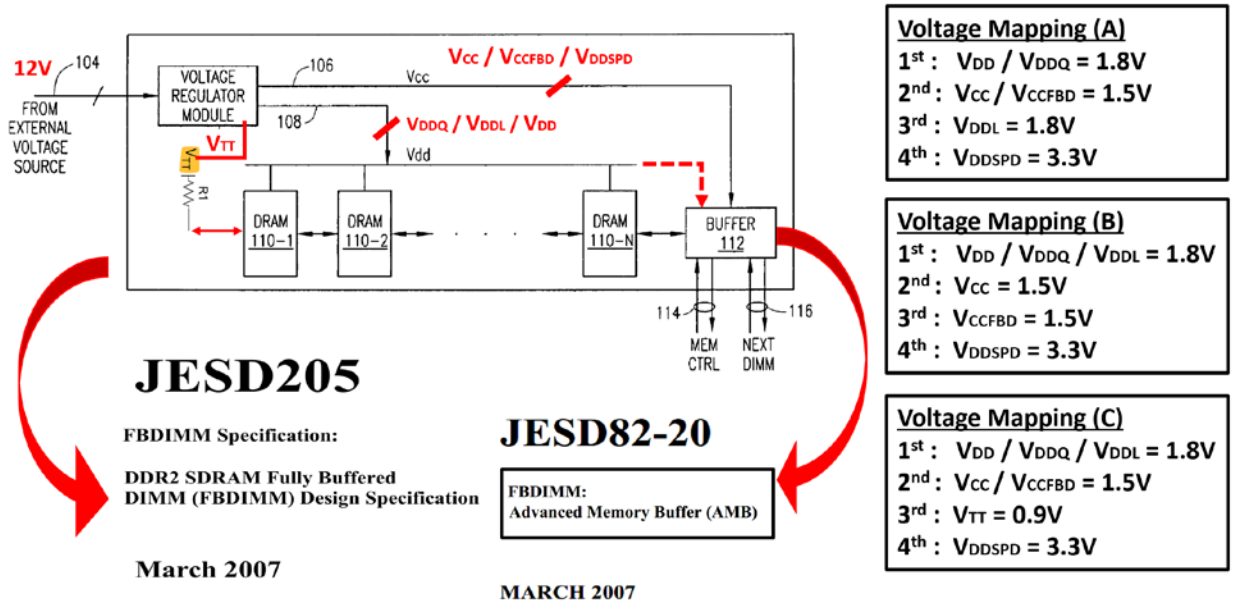
been motivated, to use separate power sources for these supply voltages, even though they have the same nominal voltage amplitude of 1.5 volts.

272. Therefore, under Patent Owner's apparent claim interpretation, Harris in view of the FBDIMM Standards, or in further view of Amidi, or in further view of Hajeck (Grounds 1B, 2B, and 3B) satisfies this limitation.

(3) Grounds 1C, 2C, 3C: VTT at 0.9 Volts

273. Under a claim interpretation that the different claimed "*voltage amplitude[s]*" have different amplitudes, Ground 1C (Harris in view of the FBDIMM Standards), Ground 2C (Ground 1 in view of Amidi), and Ground 3C (Ground 2 in view of Hajeck), teaches a VTT voltage ("*third regulated voltage*") has a voltage amplitude of 0.9 volts ("*having a third voltage amplitude*"), as shown in the figures below. The voltage mapping of Ground 3C is the same as Ground 2C.

Ground 1: Harris with JEDEC's FBDIMM Standards



Voltage Mapping (A)
1st : VDD / VDDQ = 1.8V
2nd : VCC / VCCFBD = 1.5V
3rd : VDDL = 1.8V
4th : VDDSPD = 3.3V

Voltage Mapping (B)
1st : VDD / VDDQ / VDDL = 1.8V
2nd : VCC = 1.5V
3rd : VCCFBD = 1.5V
4th : VDDSPD = 3.3V

Voltage Mapping (C)
1st : VDD / VDDQ / VDDL = 1.8V
2nd : VCC / VCCFBD = 1.5V
3rd : VTT = 0.9V
4th : VDDSPD = 3.3V

Ground 2: Ground 1 and Battery Backup of Amidi

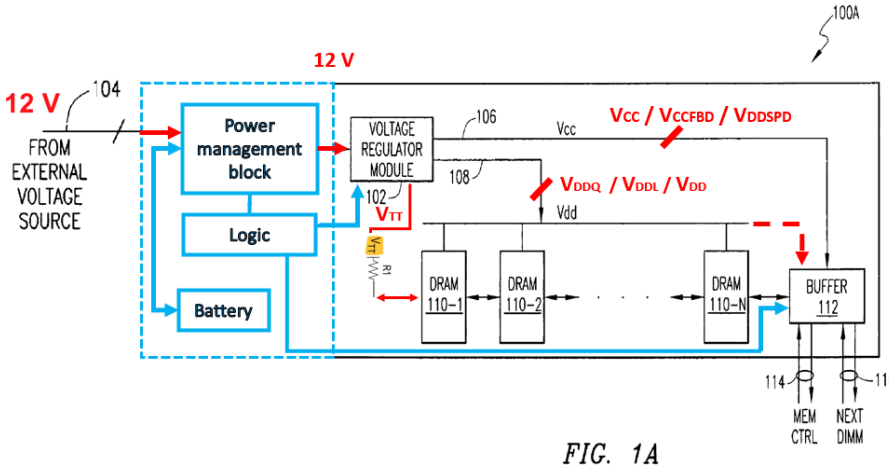


FIG. 1A

Voltage Mapping (A)
1st : VDD / VDDQ = 1.8V
2nd : VCC / VCCFBD = 1.5V
3rd : VDDL = 1.8V
4th : VDDSPD = 3.3V

Voltage Mapping (B)
1st : VDD / VDDQ / VDDL = 1.8V
2nd : VCC = 1.5V
3rd : VCCFBD = 1.5V
4th : VDDSPD = 3.3V

Voltage Mapping (C)
1st : VDD / VDDQ / VDDL = 1.8V
2nd : VCC / VCCFBD = 1.5V
3rd : VTT = 0.9V
4th : VDDSPD = 3.3V

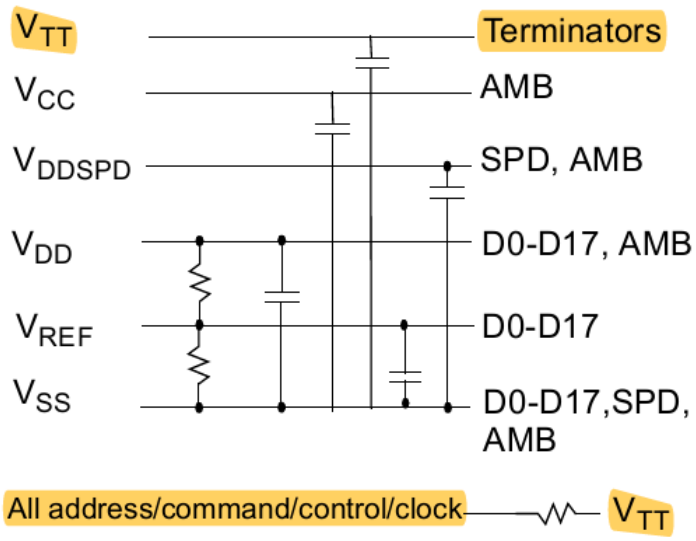
Ex. 1023 at Fig. 1A (annotated).

274. As discussed above with the reference to an FBDIMM with DDR2 SDRAM, a Skilled Artisan would have understood that an FBDIMM, like that disclosed in Harris, requires a supply voltage called VTT for proper operation of the DDR2 memory devices. *Supra* ¶¶140, 136, 139, 140, 155, 166, 169.

275. For example, JESD205 (part of the FBDIMM Standards) discloses that the memory devices (DRAM) are provided an interface supply voltage VTT.

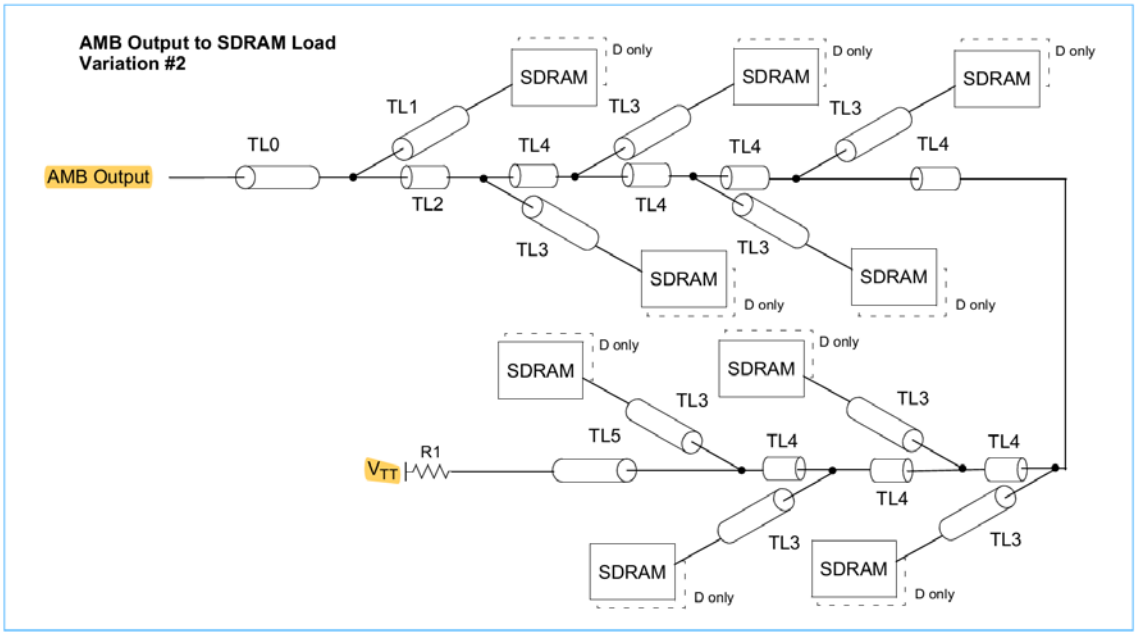
	min	typ	max	
Supply voltages (nominal)	1.7	1.8	1.9	(DRAM V_{DD}/V_{DDQ}, AMB V_{DDQ})
	1.455[1]	1.5	1.575[1]	(AMB V_{CC}/V_{CCFBD})
	$0.453*V_{DD}$	$0.5*V_{DD}$	$0.547*V_{DD}$	(DRAM Interface V_{TT}) This supply should track as 0.5 * 1.8 volt supply

Ex. 1028 at 9 (excerpted). As shown, VTT is typically one-half the voltage of VDD, or in the case of DDR2 SDRAM, 0.9 volts. *See id.* A Skilled Artisan would have recognized that the JEDEC standard requires VTT as a termination voltage whose amplitude is half of VDD, and the same as a reference voltage, VREF. *Id.* at 43 ("VREF [] tracks VDD/2"). A Skilled Artisan would have also recognized that an FBDIMM with DDR2 SDRAM devices, like an embodiment disclosed in Harris, requires a VTT voltage supply to properly terminate the signals on the clock, address, command, and/or control lines between the buffer/logic component 112 and the DRAM memory devices 110. *See*, *e.g.*, Ex. 1028 at 15 (excerpted and reproduced below, and annotated); Ex. 1023 at Fig. 1A.



For example, JESD205 explains in detail how to apply the VTT termination voltage for the address and command signal lines to the DDR2 SDRAM. *See*, *e.g.*, Ex. 1028 at 68 (excerpted and reproduced below).

Net Structure Routing for Address/Command to SDRAM (Raw Cards B, C)



Therefore, a Skilled Artisan would have recognized that, to properly terminate the clock, address, command, and/or control signals, the FBDIMM implementation of

Harris includes "*a third buck converter configured to provide a third regulated voltage*" VTT which has "*a third voltage amplitude*" of half of VDD, such as 0.9 volts for standard DDR2 SDRAM memory devices.

276. Therefore, Harris in view of the FBDIMM Standards, or in further view of Amidi, or further in view of Hajeck (Grounds 1C, 2C, and 3C) satisfies this limitation.

(4) Grounds 2D, 3D: VCCFPGA at 1.2 Volts

277. Under a claim interpretation that the different claimed "*voltage amplitude[s]*" have different amplitudes, Ground 2D (Ground 1 in view of Amidi) and Ground 3D (Ground 2 in view of Hajeck) teaches a VCCFPGA voltage supply ("*third regulated voltage*") has a voltage amplitude of 1.2 volts ("*having a third voltage amplitude*"), as shown in the figure below. The voltage mapping of Ground 3D is the same as Ground 2D.

Ground 2: Ground 1 and Battery Backup of Amidi

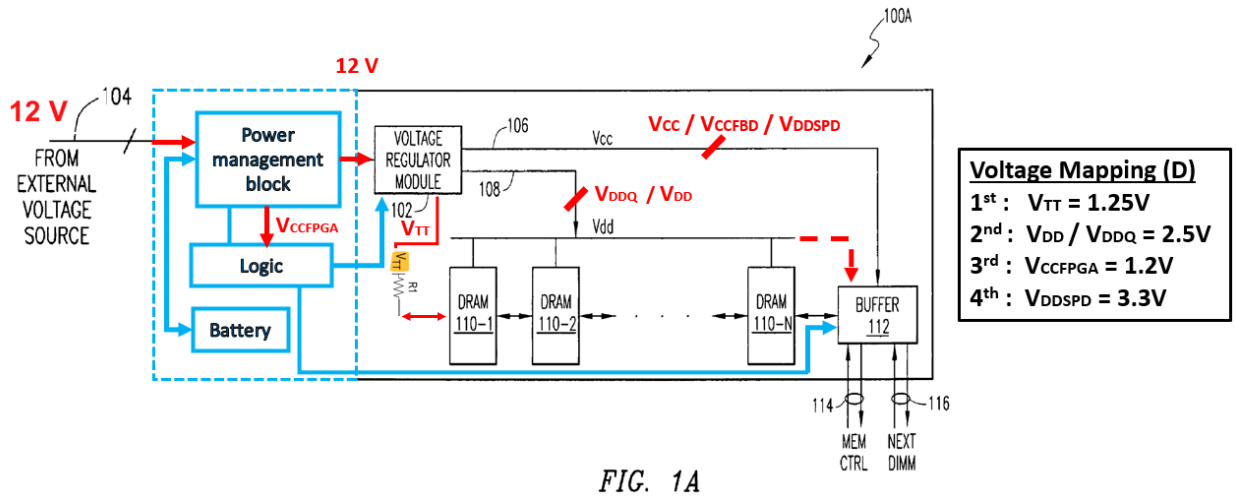


FIG. 1A

Ex. 1023 at Fig. 1A (annotated with teachings of Amidi, Ex. 1024).

278. Amidi suggests using a Xilinx device for implementing its control logic functionalities, such as for a state machine for operating the memory module in backup mode. *See* Ex. 1024 at 2:12-16 ("For example, one may provide a system with a controller which detects voltage levels and clock signals, a state machine for operating a memory in backup mode, and a battery and Supporting circuitry for Supplying backup power."), 6:40-43 ("Control of a state machine allows for a state machine to be implemented and operated, such as in a complex programmable logic device (e.g. a CPLD available from Xilinx)."

279. A Skilled Artisan would have understood that such a programmable logic device can be implemented as a field programmable gate array (FPGA) from Xilinx which commonly required a power supply of 1.2 volts. It was well known that FPGAs were commercially available devices at the time that a Skilled Artisan would have used to implement logic. For example, Spiers uses an FPGA for its processor. Ex. 1025 at [0037]. As another example, the Power Supply Reference Guide for Xilinx FPGAs lists a VCCINT power supply at 1.2 volts. *See* Ex. 1042 at 2. Similarly, the Power Supply Reference Guide for Altera FPGAs lists a VCCINT power supply at 1.2 volts. *See* Ex. 1043 at 1. As another example, U.S. Patent Publication No. 2010/0205470 to Moshayedi et al. ("Moshayedi") discloses that Altera FPGAs at the time were powered by a 1.2 volt power supply. *See*

Ex. 1044 at Fig. 8. In addition, I have designed FPGA interface chips to implement logic for VME-bus systems and to implement processors. Ex. 1004 at 2.

280. Therefore, Harris in view of the FBDIMM Standards, and further in view of Amidi (Ground 2D), and further in view of Hajeck (Ground 3D) satisfies this limitation.

f) [1.f] A Converter Circuit

281. Claim 1 requires "*a converter circuit configured to provide a fourth regulated voltage having a fourth voltage amplitude.*"

282. The prior art references in each of Grounds 1 through 3 teach this limitation to a Skilled Artisan. Each of the Grounds, and each of the voltage mappings for Grounds 1, 2, and 3, teaches that a VDDSPD supply voltage ("fourth regulated voltage") has a voltage amplitude of 3.3 volts ("having a fourth voltage amplitude"). *Supra* ¶¶157-169 (Ground 1 including voltage mappings A-C), ¶¶170-179 (Ground 2 including voltage mappings A-D), ¶¶180-187 (Ground 3 including voltage mappings A-D).

283. Harris discloses a system management bus (SMBus) 310 coupled between a memory controller and the memory modules, as shown in Figure 3 of Harris below.

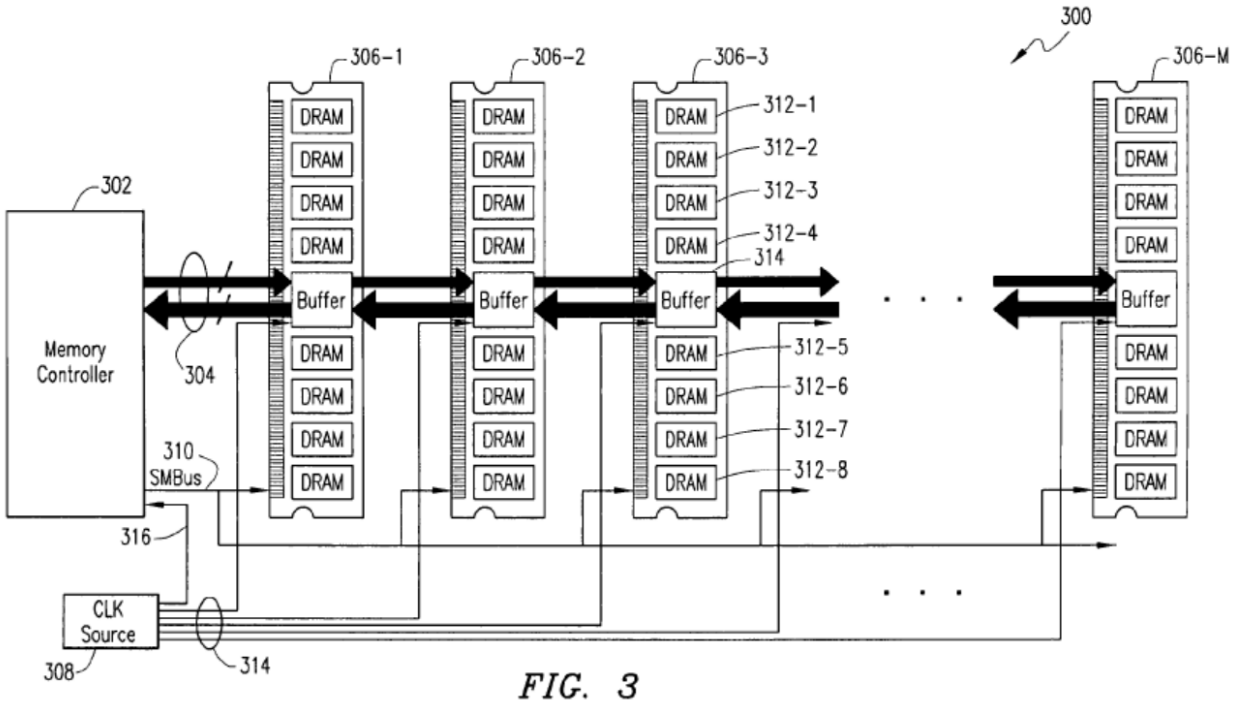


FIG. 3

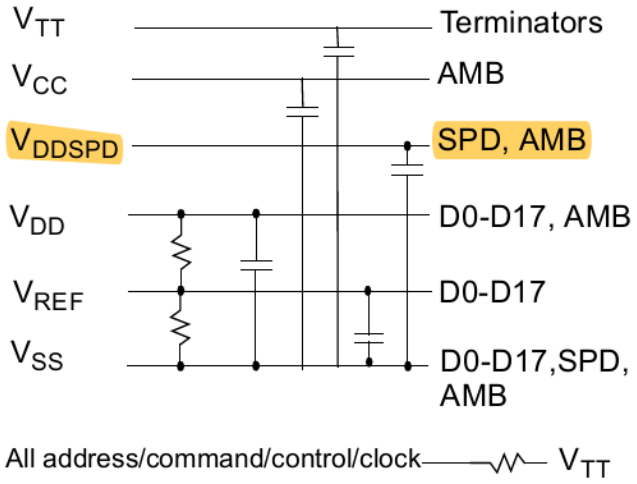
Ex. 1023 at Fig. 3; *see also id.* at [0017] ("A system management bus (SM bus) 310 coupled to the memory boards 306-1 through 306-M is driven by the memory controller 302.").

284. In addition, Skilled Artisan would have recognized that, as discussed above with reference to claim limitation [1.d], the memory module of Harris is implemented in an embodiment as an FB-DIMM with a buffer 112 in accordance with the JEDEC standard for an Advanced Memory Buffer (AMB), which at the time, required a VDDSPD voltage supply at 3.3 volts for the SMB receivers and ESD diodes. *Supra* ¶¶250-261. This is shown in the table below.

Power Supplies		
VCC (24 pins)	A	1.5V nominal supply for core I/O
VCCFBD (8 pins)	A	1.5V nominal supply for FBD high speed I/O
VDD (24 pins)	A	1.8V nominal supply for DDR I/O
VSS (156 pins)	A	Ground
VDDSPD	A	3.3V nominal supply for SMB receivers and ESD diodes

Ex. 1027 at 83 (excerpted and annotated).

285. Further, a Skilled Artisan would have recognized that VDDSPD is supplied for both the buffer (AMB) and serial presence detect (SPD) device on the memory module. This is confirmed, for example, by the JEDEC standard for FB-DIMMs that shows the voltage supply connections.



Ex. 1028 at 15 (excerpted and annotated). In particular, the AMB is supplied V_{DDSPD} in addition to V_{CC}, V_{DD}, and V_{SS} (ground). As shown, VDDSPD is also supplied to the SPD in addition to V_{SS} (ground). The JESD205 standard (part of the

FBDIMM Standards) also confirms that the amplitude of VDDSPD was 3.3 volts, as shown by the table below.

	min	typ	max	
Supply voltages (nominal)	1.7	1.8	1.9	(DRAM V_{DD}/V_{DDQ}, AMB V_{DDQ})
	1.455[1]	1.5	1.575[1]	(AMB V_{CC}/V_{CCFBD})
	0.453*V_{DD}	0.5*V_{DD}	0.547*V_{DD}	(DRAM Interface V_{TT}) This supply should track as 0.5 * 1.8 volt supply
	3.0	3.3	3.6	(V_{DDSPD})

Ex. 1028 at 9 (excerpted and annotated).

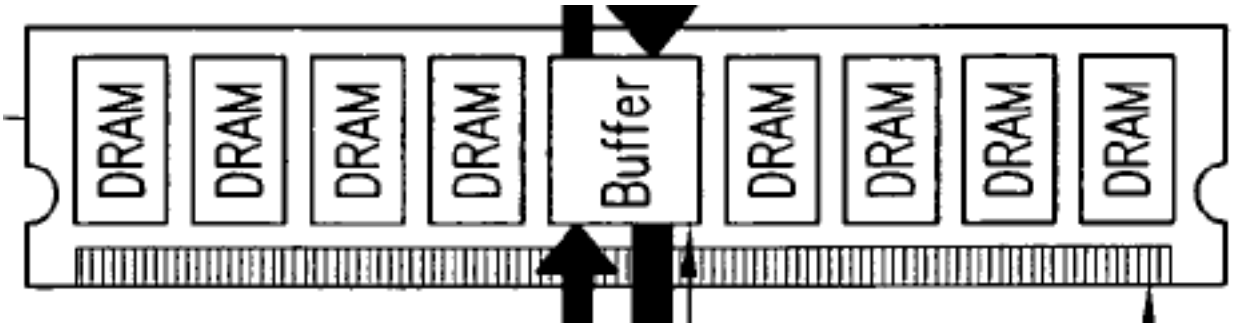
286. Accordingly, Harris alone, or in combination with the prior art references in Grounds 1 through 3, teaches "*a converter circuit configured to provide a fourth regulated voltage having*" in the voltage regulator module 102 which converts the input supply voltage (e.g., 12 volts) down to VDDSPD at 3.3 volts ("*a fourth voltage amplitude*"). For example, a Skilled Artisan would have understood it would have been obvious to implement the high-frequency switching converter in Harris for VDDSPD as a buck converter. *Supra* ¶¶236, 146-149; *see also* Ex. 1058 at 3, 5, 12-16, Fig. 1-3; Ex. 1032 at 161, 164; Ex. 1030 at 2:32-43, 5:39-44; Ex. 1024 at Fig. 6.

287. Accordingly, the prior art references in each of Grounds 1 through 3 satisfies "*a converter circuit configured to provide a fourth regulated voltage having a fourth voltage amplitude*."

g) [1.g] A Plurality of Components Coupled to the PCB

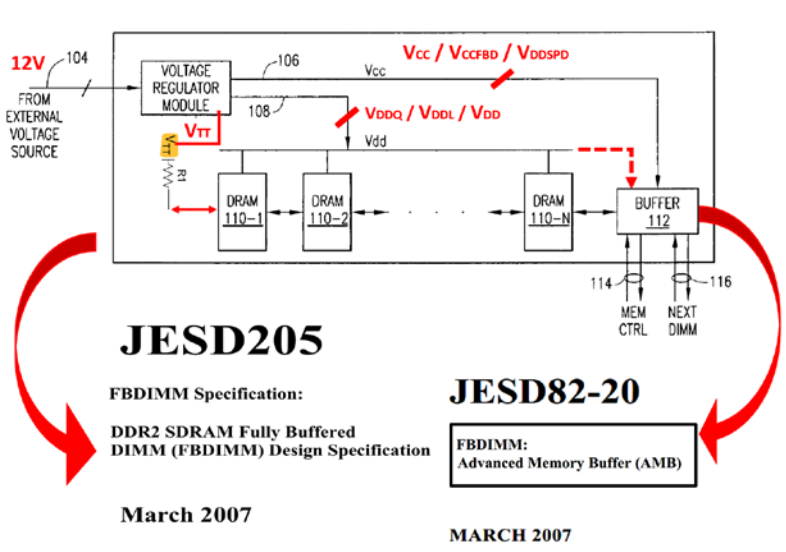
288. Claim 1 requires "*a plurality of components coupled to the PCB, each component of the plurality of components coupled to one or more regulated voltages of the first, second, third and fourth regulated voltages, the plurality of components comprising.*"

289. As explained above for claim limitation [1.b], Harris discloses using both sides of "*a printed circuit board (PCB)*" to implement a memory module. *Supra* ¶224. For example, Harris discloses that a Buffer and DRAMs are "*components coupled to the PCB.*" Ex.1023 at Fig. 3 (reproduced below in part).



290. For the reasons discussed above with reference to claim elements [1.c], [1.d], [1.e], and [1.f], Harris also discloses that "*each component of the plurality of components [is] coupled to one or more regulated voltages of the first, second, third and fourth regulated voltages*." For example, in Ground 1, DRAMs 110 are coupled to regulated voltages VDD, VDDQ, and VDDL, and Buffer 112 is coupled to VCC, VCCFBD, and VDDSPD.

Ground 1: Harris with JEDEC's FBDIMM Standards



Voltage Mapping (A)
1st : V_{DD} / V_{DDQ} = 1.8V
2nd : V_{CC} / V_{CCFBD} = 1.5V
3rd : V_{DDL} = 1.8V
4th : V_{DDSPD} = 3.3V

Voltage Mapping (B)
1st : V_{DD} / V_{DDQ} / V_{DDL} = 1.8V
2nd : V_{CC} = 1.5V
3rd : V_{CCFBD} = 1.5V
4th : V_{DDSPD} = 3.3V

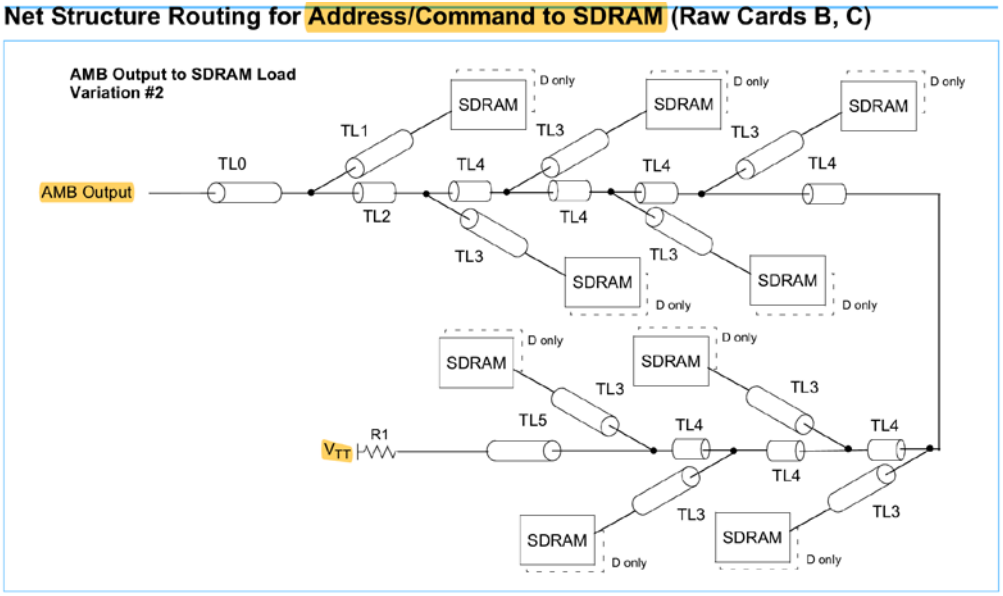
Voltage Mapping (C)
1st : V_{DD} / V_{DDQ} / V_{DDL} = 1.8V
2nd : V_{CC} / V_{CCFBD} = 1.5V
3rd : V_{TT} = 0.9V
4th : V_{DDSPD} = 3.3V

Furthermore, as explained by the FBDIMM standards, the regulated voltage VDD/VDDQ is also coupled to the Buffer (AMB). Ex. 1028 (JESD205) at 9 (disclosing V_{DD} and V_{DDQ} supply for DRAM and AMB).

	min	typ	max	
Supply voltages (nominal)	1.7	1.8	1.9	(DRAM V_{DD}/V_{DDQ}, AMB V_{DDQ})
	1.455[1]	1.5	1.575[1]	(AMB V_{CC}/V_{CCFBD})
	0.453*V_{DD}	0.5*V_{DD}	0.547*V_{DD}	(DRAM Interface V_{TT}) This supply should track as 0.5 * 1.8 volt supply

See also id. at 11 (describing VDD as "DRAM Power and AMB DRAM I/O Power"), 30 (same), 33 (describing VDDQ as a critical specification of the AMB's SDRAM interface), 13-16 (showing VDD coupled to memory chips and AMB); Ex. 1027 (JESD82-20) at 31-32 (describing AMB receiving "V_{DD} Supply voltage DRAM Interface"), 44 (describing DRAM interface on AMB receiving V_{DD}), 83

(same). A Skilled Artisan would have understood from this disclosure that the AMB receives the VDD/VDDQ voltage in order to interface with DRAM devices. The JESD205 FBDIMM standard further discloses that the regulated voltage VTT is coupled to termination resistors RTT and, through those resistors, to the SDRAMs and the Buffer (AMB). EX. 1028 at 68 (reproduced below in part, annotated).



291. In Ground 2, for the reasons discussed with reference to Ground 1, DRAMs 110 are coupled to regulated voltages VDD, VDDQ, and VDDL, and Buffer 112 is coupled to VCC, VCCFBD, VDDSPD, and VDDQ, and regulated voltage VTT is coupled to termination resistors RTT and Buffer 112 and SDRAMs 110.

Ground 2: Ground 1 and Battery Backup of Amidi

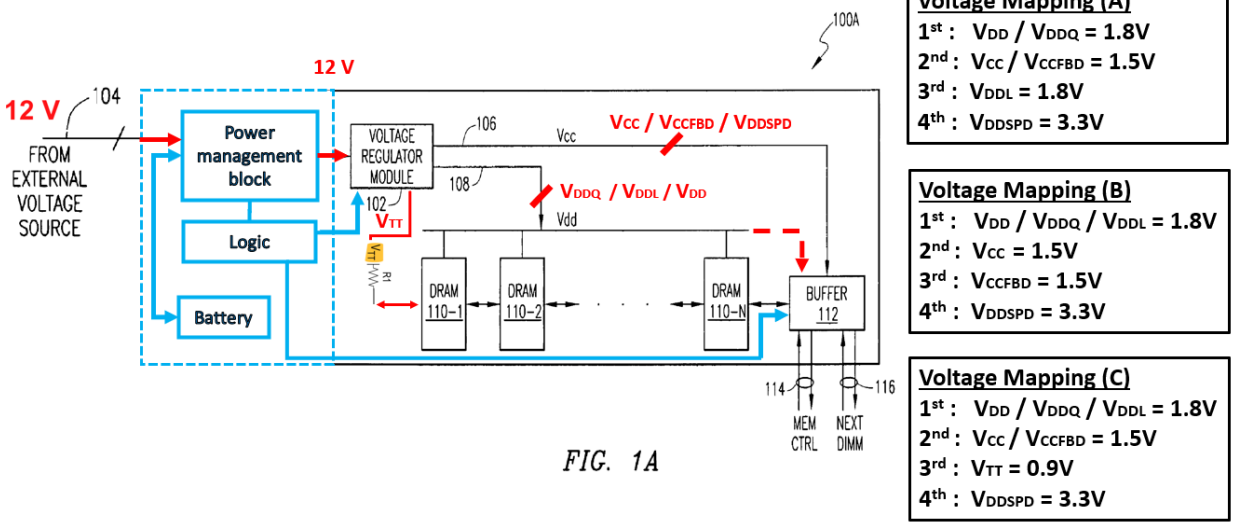


FIG. 1A

Furthermore, in voltage mapping 2D, the regulated voltage VCCFPGA is coupled to an FPGA that implements Amidi's power logic.

Ground 2: Ground 1 and Battery Backup of Amidi

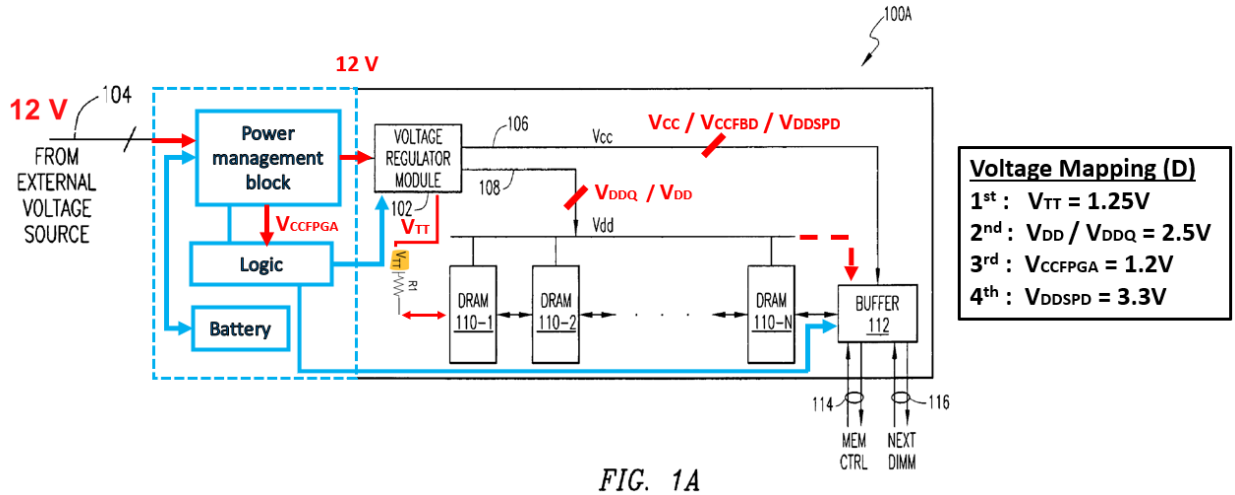


FIG. 1A

292. In Ground 3, the regulated voltages are coupled to the same components as in Ground 2.

293. As explained above for claim limitation [1.c], the prior-art references in each of Grounds 1-3 satisfies "*a first buck converter configured to provide a*

first regulated voltage having a first voltage amplitude." *Supra* ¶¶232-249. As explained for Grounds 1, 2A, 2B, 2C, 3A, 3B, and 3C, the on-board voltage regulator module includes the "*first buck converter*" that provides, for example, any one of VDD, VDDQ, or VDDL as the "*first regulated voltage*" to the memory devices, such as DDR2 SDRAM. *Supra* ¶¶238-243, 244. As explained for Grounds 2D and 3D, the on-board voltage regulator module includes the "*first buck converter*" that provides, for example, VTT as the "*first regulated voltage*" as a termination voltage coupled to the memory devices. *Supra* ¶¶245-249.

294. As explained above for claim limitation [1.d], the prior art references in each of Grounds 1-3 satisfies "*a second buck converter configured to provide a second regulated voltage having a second voltage amplitude*." *Supra* ¶¶250-261. As explained for Grounds 1A-1C, 2A-2C, and 3A-3C, the on-board voltage regulator includes the "*second buck converter*" that provides, for example, any one of VCC or VCCFBD as the "*second regulated voltage*" to the buffer/logic component 112, such as an FBDIMM Advanced Memory Buffer (AMB). *Supra* ¶¶253-257. As explained for Grounds 2D and 3D, the on-board voltage regulator includes the "*second buck converter*" that provides, for example, any one of VDD or VDDQ as the "*second regulated voltage*" to the memory devices and/or buffer/logic component 112, such as an FBDIMM Advanced Memory Buffer (AMB). *Supra* ¶¶258-261.

295. As explained above for claim limitation [1.e], the prior art references in each of Grounds 1-3 satisfies "*a third buck converter configured to provide a third regulated voltage having a third voltage amplitude*." *Supra* ¶¶262-280. As explained for Grounds 1A, 2A, and 3A, the on-board voltage regulator includes the "*third buck converter*" that provides, for example, VDDL coupled to the memory devices if the "*voltage amplitude[s]*" can be the same voltage under Patent Owner's interpretation. *Supra* ¶¶265-269. As explained for Grounds 1B, 2B, and 3B, the on-board voltage regulator includes the "*third buck converter*" that provides, for example, VCCFBD coupled to the buffer if the "*voltage amplitude[s]*" can be the same voltage under Patent Owner's interpretation. *Supra* ¶¶270-272. As explained for Grounds 1C, 2C, and 3C, the on-board voltage regulator includes the "*third buck converter*" that provides, for example, VTT coupled to the memory devices if each of the "*voltage amplitude[s]*" is interpreted to be different. *Supra* ¶¶273-276. As explained for Grounds 2D and 3D, the on-board voltage regulator includes the "*third buck converter*" that provides, for example, VCCFPGA coupled to the Amidi's logic (e.g., FPGA) if each of the "*voltage amplitude[s]*" is interpreted to be different. *Supra* ¶¶277-280.

296. As explained above for claim limitation [1.f], the prior art references in each of Grounds 1-3 satisfies "*a converter circuit configured to provide a fourth regulated voltage having a fourth voltage amplitude*." *Supra* ¶¶281-287. As

explained, the "*converter circuit*" provides, for example, VDDSPD to the buffer (AMB) and serial presence detect (SMB) as the "fourth regulated voltage." *Id.*

297. Accordingly, the prior art references in each of Grounds 1-3 satisfies "*a plurality of components coupled to the PCB, each component of the plurality of components coupled to one or more regulated voltages of the first, second, third and fourth regulated voltages, the plurality of components comprising*."

h) [1.h] A Plurality of SDRAM Devices

298. Claim 1 requires "*a plurality of synchronous dynamic random access memory (SDRAM) devices coupled to the first regulated voltage*."

299. The prior art references in each of Grounds 1 through 3 teach this limitation to a Skilled Artisan.

300. Harris teaches and discloses "*a plurality of synchronous dynamic random access memory (SDRAM) devices*" to a Skilled Artisan. In an embodiment, Harris discloses that the memory devices are standard dynamic random access memory (DRAM) devices, such as DDR2, which a Skilled Artisan would have understood are synchronous DRAM devices. *See* Ex. 1023 at Fig. 1A, [0009] ("In one configuration, the memory module 100A may be implemented as a Dual In-line Memory Module (DIMM) wherein each of the memory devices 110-1 through 110-N comprises a Double Data Rate (DDR) dynamic random access memory (DRAM) device . . . . Also, the memory devices can be of any known or heretofore

unknown DDR type, e.g., DDR2 (operable with 1.8 V), DDR3 (operable with 1.35V to 1.5V), and the like."); *see also* Ex. 1023 at [0011] ("Since the V_{dd} and V_{cc} power supply rails are rendered independent from external voltage sources, the overall power supply interface to the memory module 100A is improved to better support . . . DRAM technology independence (e.g., DDR2, DDR3, DDR4, and other DRAM types) . . . ."); Ex. 1045 at 1 (Double Data Rate (DDR) SDRAM Specification, JESD79, a JEDEC standard), Ex. 1026 (DDR2 SDRAM Specification, JESD79-2B, a JEDEC standard), Ex. 1046 (DDR3 SDRAM, JESD79-3A, a JEDEC standard), Ex. 1028 (DDR2 SDRAM FBDIMM Design Specification, JESD205, a JEDEC standard).

301. As explained above for claim limitation [1.c], the prior art references in each of Grounds 1-3 satisfies "*a first buck converter configured to provide a first regulated voltage having a first voltage amplitude*." *Supra* ¶¶232-249. As explained for Grounds 1, 2A-C, and 3A-C, the on-board voltage regulator module includes the "*first buck converter*" that provides, for example, any one of VDD, VDDQ, or VDDL as the "*first regulated voltage*" to the memory devices, such as DDR2 SDRAM. *Supra* ¶¶238-243, 244. And, as explained for Grounds 2D and 3D, the on-board voltage regulator module includes the "*first buck converter*" that provides, for example, VTT as the "*first regulated voltage*" as a termination voltage coupled to the memory devices. *Supra* ¶¶245-249.

302. As explained below, each of the voltages in Grounds 1 through 3—VDD, VDDQ, VDDL, and VTT—is coupled to the memory devices. *Supra* ¶¶232-249. Harris discloses in Figure 1A that VDD is coupled to the memory devices (DRAM 110-1 to 110-N), as shown below.

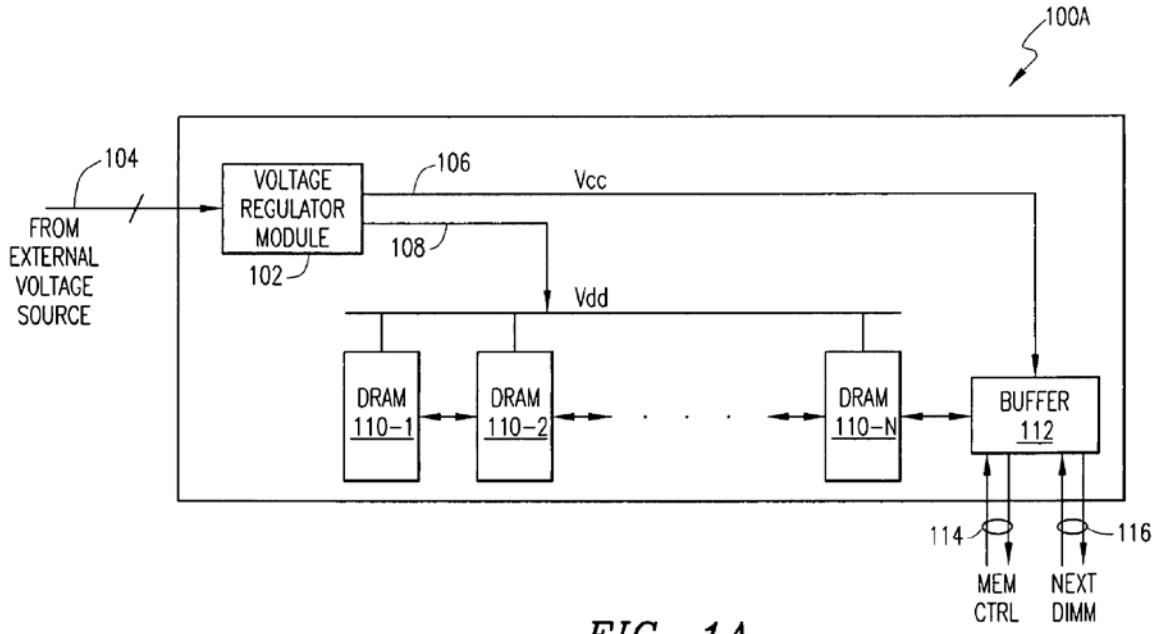


FIG. 1A

Ex. 1023 at Fig. 1A. As explained for claim limitation [1.c], a Skilled Artisan would have recognized that, as disclosed by the relevant JEDEC standards, an implementation of Harris with DDR2 memory devices couples those devices to multiple, separate voltage sources, called VDD, VDDQ, and VDDL. *Supra* ¶¶239-242 (Ground 1), ¶244 (Grounds 2A-2C, 3A-3C); *see also* Ex. 1023 at [0009]; Ex. 1028 at 9, 17-20; Ex. 1026 at pp.2-3, 6-7, 9. Furthermore, a Skilled Artisan would have recognized that, as disclosed by the relevant JEDEC standards, an

implementation of Harris with DDR memory devices (e.g., DDR) couples those devices to the termination voltage VTT at 1.25 volts. *Supra* ¶¶245-249 (Grounds 2D, 3D); *see also* Ex. 1023 at [0002]; Ex. 1045 (JESD79) at 1, 7, 54, 60.

303. Accordingly, the prior art references in each of Grounds 1-3 satisfies "*a plurality of synchronous dynamic random access memory (SDRAM) devices coupled to the first regulated voltage*."

i) [1.i] At Least One Circuit

(1) [1.i.1] Coupled between the edge connections and the SDRAM devices

304. Claim 1 requires "*at least one circuit coupled between a first portion of the plurality of edge connections and the plurality of SDRAM devices.*"

305. The prior art references in each of Grounds 1 through 3 teach this limitation to a Skilled Artisan.

306. As discussed for claim limitation [1.b], Harris alone, or in combination with the FBDIMM Standards, satisfies "*a printed circuit board (PCB) having an interface configured to fit into a corresponding slot connector of a host system, the interface including a plurality of edge connections configured to couple power, data, address and control signals between the memory module and the host system.*" *Supra* ¶¶223-231.

307. Harris discloses that the buffer 112 ("*at least one circuit*") is coupled to a bidirectional memory interface paths and buffers command, address, and data

space for at least a portion of the memory devices. As shown in Figure 1A of Harris below, buffer 112 is coupled between paths 114 and 116, on one hand, and DRAM 110-1 through 110-N, on the other.

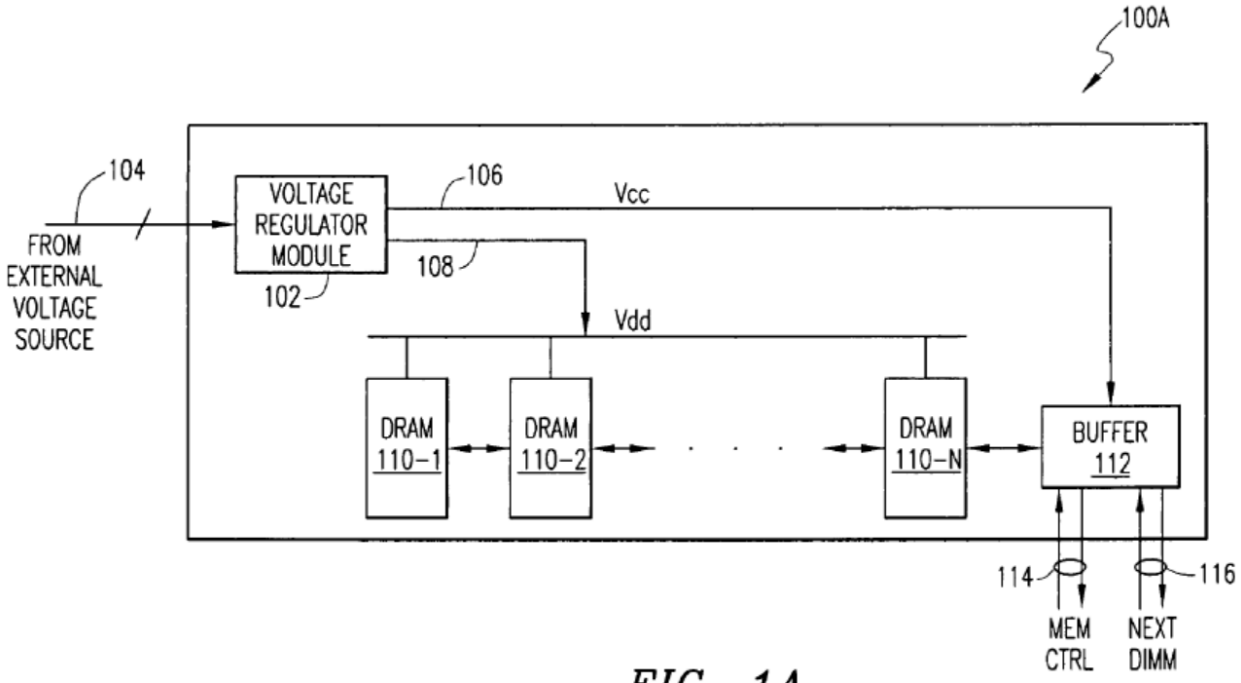


FIG. 1A

Ex. 1023 at Fig. 1A; *see also id.* at [0009] ("In the illustrated embodiment of FIG. 1A, for instance, the DIMM configuration of the memory module 100A is exemplified as a fully buffered DIMM wherein a buffer/logic component 112 is provided for buffering command/address (C/A) space as well as data space at least for a portion of the memory devices 110-1 through 110-N. A bidirectional memory controller interface path 114 as well as a second voltage path 106, typically referred to as a Vcc path, are provided with respect to the buffer component 112, wherein the Vcc path may be energized to appropriate voltage levels depending on

the buffer and DIMM technology, e.g., from about 0.5V to 3.5V or more. In addition, where multiple memory assemblies are daisy-chained on a single memory controller channel, a suitable daisy-chain interface 116 is provided for coupling the buffer component 112 to a next memory module.").

308. In addition, as shown in Figure 3 of Harris, the bidirectional interface paths 304 are coupled through a plurality of connections on the edge connector(s) of the memory module(s) 306-1 through 306-M.

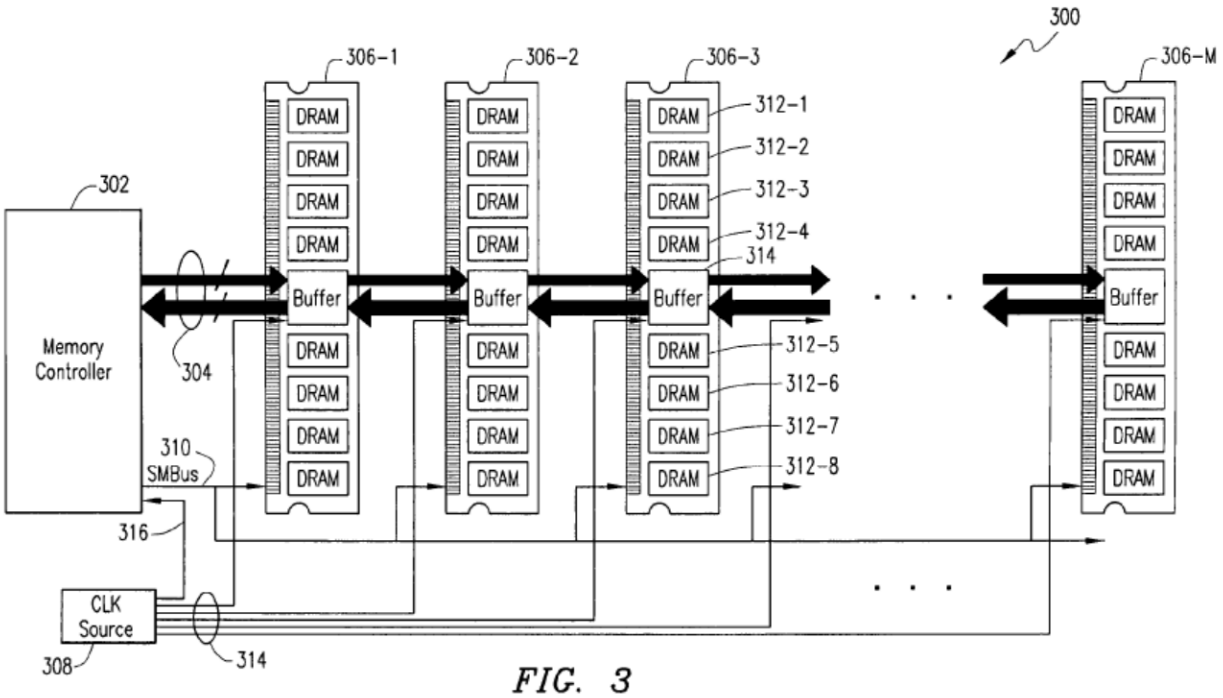


FIG. 3

Ex. 1023 at Fig. 3; *see also id.* at [0019] ("one or more of the following advantages may be realized in an exemplary voltage distribution embodiment: . . . reduction in the pin count on DIMM connector to system board or memory riser card (whereby

a smaller connector or wider pin spacing may be accommodated)"); *see also id.* at [0002] and [0012] (discussing specific pin counts for power).

309. In addition, a Skilled Artisan would have recognized that the buffer in Harris is coupled between a first portion of the plurality of edge connections and the SDRAM devices. For example, JESD205 (part of the FBDIMM Standards) discloses that an FBDIMM includes a "PCB edge connector contacts [that] shall be gold-plated" (Ex. 1028 at 84), and that there is a voltage drop between the edge connector and the motherboard (*id.* at 100). Additionally, JESD205 discloses that standard FBDIMM connector pins include northbound and southbound data (*id.* at 11 (listing PN, PS, SN, and SS pins)) that are coupled to the Advanced Memory Buffer (AMB) (*id.* at 13 (showing AMB connected to PN, PS, SN, and SS signals)). Similarly, JESD82-20 (part of the FBDIMM Standards) discloses a DIMM "gold finger[s]" (Ex. 1027 at 43) that include PN, PS, SN, and SS pins (*id.* at 81), which are represent read and write data paths between the AMB and either a host or the next AMB in a daisy-chained configuration (*id.* at 81). *See also* Ex. 1027 at 3 (Figure 1.1) (showing data flow for the AMB buffer including conversion of communications, such as those on the Northbound and Southbound links, into data, address, and control signals for the memory devices, such as the signals coupled to the "DDR IO's" block).

310. Accordingly, the prior art references in each of Grounds 1-3 satisfies "*at least one circuit coupled between a first portion of the plurality of edge connections and the plurality of SDRAM devices*."

(2) [1.i.2] Operable to receive/output address and control signals

311. Claim 1 requires "*the at least one circuit operable to (i) receive a first plurality of address and control signals via the first portion of the plurality of edge connections, and (ii) output a second plurality of address and control signals to the plurality of SDRAM devices*."

312. The prior art references in each of Grounds 1 through 3 teach this limitation to a Skilled Artisan.

313. As discussed for claim limitation 1[.b], Harris alone, or in combination with the FBDIMM Standards, satisfies "*a printed circuit board (PCB) having an interface configured to fit into a corresponding slot connector of a host system, the interface including a plurality of edge connections configured to couple power, data, address and control signals between the memory module and the host system.*" *Supra* ¶¶223-231. As discussed for claim limitation [1.ii.1], Harris alone, or in combination with the FBDIMM Standards, satisfies "*at least one circuit coupled between a first portion of the plurality of edge connections and the plurality of SDRAM devices*." *Supra* ¶¶304-310.

314. Harris teaches and discloses to a Skilled Artisan that its buffer is operable to "*receive a first plurality of address and control signals via the first portion of the plurality of edge connections*" and "*output a second plurality of address and control signals to the plurality of SDRAM devices*." As shown in Figure 1A of Harris below, the buffer 112 receives signals via the bidirectional memory controller interface path 114 (labeled "MEM CTRL" in the figure) and outputs signals to the DRAM devices 110-1 through 110-N (e.g., DDR2 SDRAMs).

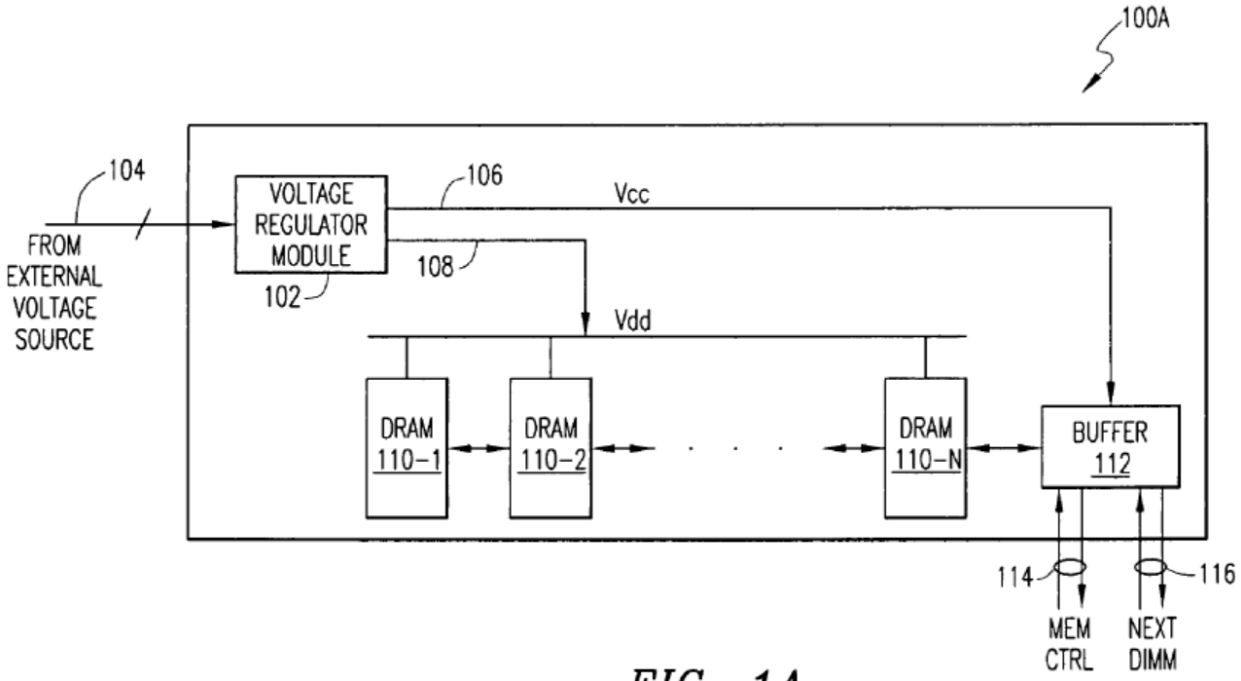
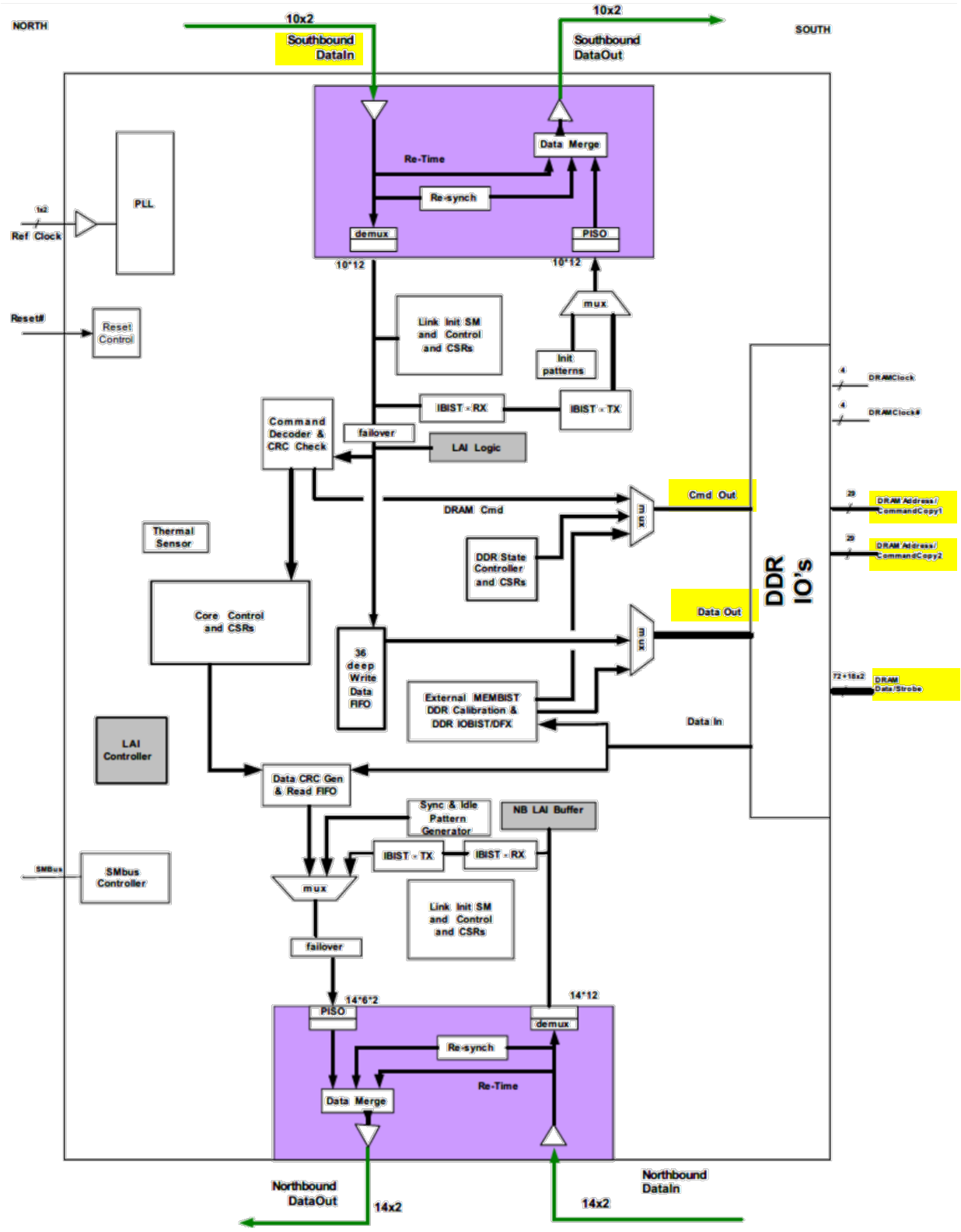


FIG. 1A

Ex. 1023 at Fig. 1A. Harris explains that a "bidirectional memory controller interface path 114 as well as a second voltage path 106, typically referred to as a Vcc path, are provided with respect to the buffer component 112 . . . ." *Id.* at

[0009]. The buffer 112 "is provided for buffering command/address (C/A) space as well as data space at least for a portion of the memory devices 110-1 through 110-N." *Id.*

315. Further, a Skilled Artisan would have recognized that the signals received via the edge connections on the memory module of Harris include command and address signals, such as the northbound and southbound signals that include command, address, and data signals (e.g., PN, PS, SN, SS). *See, e.g.*, Ex. 1027 at 81 (Table 9.2); Ex. 1028 at 11 (listing PN, PS, SN, and SS pins), 13 (showing AMB connected to PN, PS, SN, and SS signals). For example, JESD82-20 (part of the FBDIMM Standards) shows these signals in a block diagram of the Advanced Memory Buffer (AMB), as shown below.


NORTH
SOUTH
10x2
Southbound DataIn
10x2
Southbound DataOut
Re-Time
Data Merge
Re-synch
demux
PISO
10*12
10*12
PLL
1x2
Ref Clock
Reset#
Reset Control
Link Init SM and Control and CSRs
mux
Init patterns
IBIST - RX
IBIST - TX
Command Decoder & CRC Check
failover
LAI Logic
DRAM Cmd
Cmd Out
mux
DDR State Controller and CSRs
Thermal Sensor
Core Control and CSRs
36 deep Write Data FIFO
Data Out
mux
External MEMBIST DDR Calibration & DDR IOBIST/DFX
Data In
LAI Controller
Data CRC Gen & Read FIFO
Sync & Idle Pattern Generator
NB LAI Buffer
SMBus
SMbus Controller
IBIST - TX
IBIST - RX
mux
Link Init SM and Control and CSRs
failover
14*6*2
14*12
PISO
demux
Re-synch
Re-Time
Data Merge
Northbound DataOut
14x2
Northbound DataIn
14x2
DDR IO's
4
DRAMClock
4
DRAMClock#
29
DRAM Address/ CommandCopy1
29
DRAM Address/ CommandCopy2
72+18x2
DRAM Data/Strobe

Ex. 1027 at 3 (Fig. 1.1) (annotated). As shown by the annotations in yellow, the "Southbound DataIn" signal is coupled to the "Cmd Out" and "Data Out" signals internal to the buffer. *See id.* JESD82-20 states that "[t]he southbound input link is 10 lanes wide and carries commands and write data from the host memory controller or the adjacent DIMM in the host direction." *Id.* at 4; *see also id.* at 4 ("The northbound input link is 13 to 14 lanes wide and carries read return data or status information from the next FB DIMM in the chain back towards the host."). Accordingly, a Skilled Artisan would have recognized that the "commands and write data" and "read return data" include command, address, and data signals to, for example, write to or read from the memory devices. *See, e.g.*, *id.* at 1 ("The Advanced Memory Buffer will perform the following FBD channel functions: . . . Acts as DRAM memory buffer for all read, write, and configuration accesses addressed to the DIMM.").

316. A Skilled Artisan would also have recognized that the buffer outputs a second plurality of address and control signals to the plurality of SDRAM devices. *See, e.g.*, Ex. 1027 at 81-82 (Table 9.2, "DRAM Interface"); Ex. 1028 at 13 (showing AMB connected to DQ0-DQ63 and DQS0-17). For example, as shown in Figure 1.1 (reproduced above), the internal "Cmd Out" and "Data Out" signals are coupled to the "DRAM Address/CommandCopy 1," "DRAM Address/CommandCopy 2," and "DRAM Data/Strobe" signals (highlighted in

yellow) that are output to the DRAM. *See* Ex. 1027 at 3 (Fig. 1.1) (reproduced above and annotated). JESD82-20 states that "[t]here are two copies of address and command signals to support DIMM routing and electrical requirements" and that "four copies of the command clock phase references (CLK[3:0]) and write data/check-bit strobes (DQSs) for each DRAM nibble" is provided by the buffer. *Id*. at 4.

317. Accordingly, the prior art references in each of Grounds 1-3 satisfies "*the at least one circuit operable to (i) receive a first plurality of address and control signals via the first portion of the plurality of edge connections, and (ii) output a second plurality of address and control signals to the plurality of SDRAM devices*."

(3) [1.i.3] Coupled to both the second and fourth regulated voltage

318. Claim 1 requires "*the at least one circuit coupled to both the second regulated voltage and the fourth regulated voltage*."

319. As explained above for claim limitation [1.d], the prior art references in each of Grounds 1-3 satisfies "*a second buck converter configured to provide a second regulated voltage having a second voltage amplitude*." *Supra* ¶¶250-261. As explained for Grounds 1A-1C, 2A-2C, and 3A-3C, the on-board voltage regulator includes the "*second buck converter*" that provides, for example, any one of VCC or VCCFBD as the "*second regulated voltage*" to the buffer/logic

component 112, such as an FBDIMM Advanced Memory Buffer (AMB). *Supra* ¶¶253-257. As explained for Grounds 2D and 3D, the on-board voltage regulator includes the "*second buck converter*" that provides, for example, any one of VDD or VDDQ as the "*second regulated voltage*" to the memory devices and/or buffer/logic component 112, such as an FBDIMM Advanced Memory Buffer (AMB). *Supra* ¶¶258-261.

320. As explained below, each of the second regulated voltages in Grounds 1 through 3—VCC, VCCFBD, VDD, and VDDQ—and the fourth regulated voltage, VDDSPD, is coupled to the buffer/logic component 112 of Harris.

321. In particular, Harris discloses that a voltage supply VCC is provided to the buffer/logic component 112 ("*the at least one circuit*"). *See, e.g.*, Ex. 1023 at Fig. 1A. Also, a Skilled Artisan would have recognized that an Advanced Memory Buffer (AMB) for an FB-DIMM, such as the FB-DIMM disclosed by Harris in an embodiment, is also provided a voltage supply VCCFBD at 1.5 volts. *See, e.g.*, Ex. 1027 at 78, 82-83. As explained above, a Skilled Artisan would have recognized that, as disclosed by the relevant JEDEC standards, an implementation of Harris with DDR SDRAM coupled at least the memory devices to voltage supplies called VDD and VDDQ. *Supra* ¶¶259, 236, 146-149; *see also* Ex. 1058 at 3, 5, 12-16, Fig. 1-3; Ex. 1032 at 161, 164; Ex. 1030 at 2:32-43, 5:39-44; Ex. 1024 at Fig. 6. A Skilled Artisan would have also recognized that VDD and VDDQ are

coupled to the buffer. JESD82-20 (part of the FBDIMM Standards) discloses that VDD is "supply for DDR IO" (Ex. 1027 at p.83) and VDDQ is the "I/O buffer voltage" (Ex. 1027 at 20). *See also* Ex. 1027, pp.168-175 (Pin Assignments for the buffer including VDD), p.44 (describing recommendation voltages for DRAM interface), p. 3 (Figure 1.1) (showing data flow for the AMB buffer including signals coupled to the "DDR IO's" block). Similarly, JESD205 (part of the FBDIMM Standards) discloses that VDD is a supply for I/O (Ex. 1028 at 30) and VDDQ is an interface voltage (Ex. 1028 at 33). *See also* Ex. 1028 at 9 (listing VDD and VDDQ, including VDDQ coupled to the buffer), 31-32 (pin assignments for the buffer including VDD). Thus, VDD and VDDQ are coupled to the buffer.

322. Further, as explained above for claim limitation [1.f], the prior art references in each of Grounds 1-3 satisfies "*a converter circuit configured to provide a fourth regulated voltage having a fourth voltage amplitude*." *Supra* ¶¶281-287. In particular, Harris discloses to a Skilled Artisan that a voltage supply VDDSPD at 3.3V is provided to the buffer (AMB) for a system management bus (SM Bus or SMB) and electro-static discharge (ESD) diodes. *See, e.g.*, Ex. 1023 at Fig. 3, [0017]; Ex. 1027 at 83; Ex. 1028 at 15. Thus, VDDSPD is also coupled to the buffer.

323. Accordingly, the prior art references in each of Grounds 1-3 satisfies "*the at least one circuit coupled to both the second regulated voltage and the fourth regulated voltage*."

(4) [1.i.4] Wherein one of second and fourth regulated voltage amplitudes is less than the other

324. Claim 1 requires "*wherein a first one of the second and fourth voltage amplitudes is less than a second one of the second and fourth voltage amplitudes*."

325. As explained above for claim limitation [1.d], the prior art references in each of Grounds 1-3 satisfies "*a second buck converter configured to provide a second regulated voltage having a second voltage amplitude*." *Supra* ¶¶250-261. As explained for Grounds 1A-1C, 2A-2C, and 3A-3C, the on-board voltage regulator includes the "*second buck converter*" that provides, for example, any one of VCC or VCCFBD as the "*second regulated voltage*" at 1.5 volts ("*second voltage amplitude*") to the buffer/logic component 112. *Supra* ¶¶253-257. As explained for Grounds 2D and 3D, the on-board voltage regulator includes the "*second buck converter*" that provides, for example, any one of VDD or VDDQ as the "*second regulated voltage*" at 2.5 volts ("fourth voltage amplitude") to the memory devices and/or buffer/logic component 112. *Supra* ¶¶258-261.

326. Further, as explained above for claim limitation [1.f], the prior art references in each of Grounds 1-3 satisfies "*a converter circuit configured to provide a fourth regulated voltage having a fourth voltage amplitude*." *Supra*

¶¶281-287. In particular, Harris discloses to a Skilled Artisan that a voltage supply VDDSPD at 3.3 volts is provided to the buffer (AMB) for a system management bus (SM Bus or SMB) and electro-static discharge (ESD) diodes. *See, e.g.*, Ex. 1023 at Fig. 3, [0017]; Ex. 1027 at 83; Ex. 1028 at 15.

327. The second voltage amplitude—1.5 volts or 2.5 volts—is less than fourth voltage amplitude of 3.3 volts. Accordingly, the prior art references in each of Grounds 1-3 satisfies "*wherein a first one of the second and fourth voltage amplitudes is less than a second one of the second and fourth voltage amplitudes*."

2. Claim 2 is Unpatentable

328. Claim 2 is unpatentable as the prior art references in each of Ground 1 (Voltage Mappings A, B, and C) and Grounds 2 and 3 (Voltage Mappings A, B, C, and D) render the claim obvious.

329. Claim 2 requires "*[t]he memory module of claim 1, wherein the first and third buck converters are further configured to operate as a dual buck converter*."

330. The 918 Patent illustrates a "*dual buck converter*" as simply having two outputted voltages:

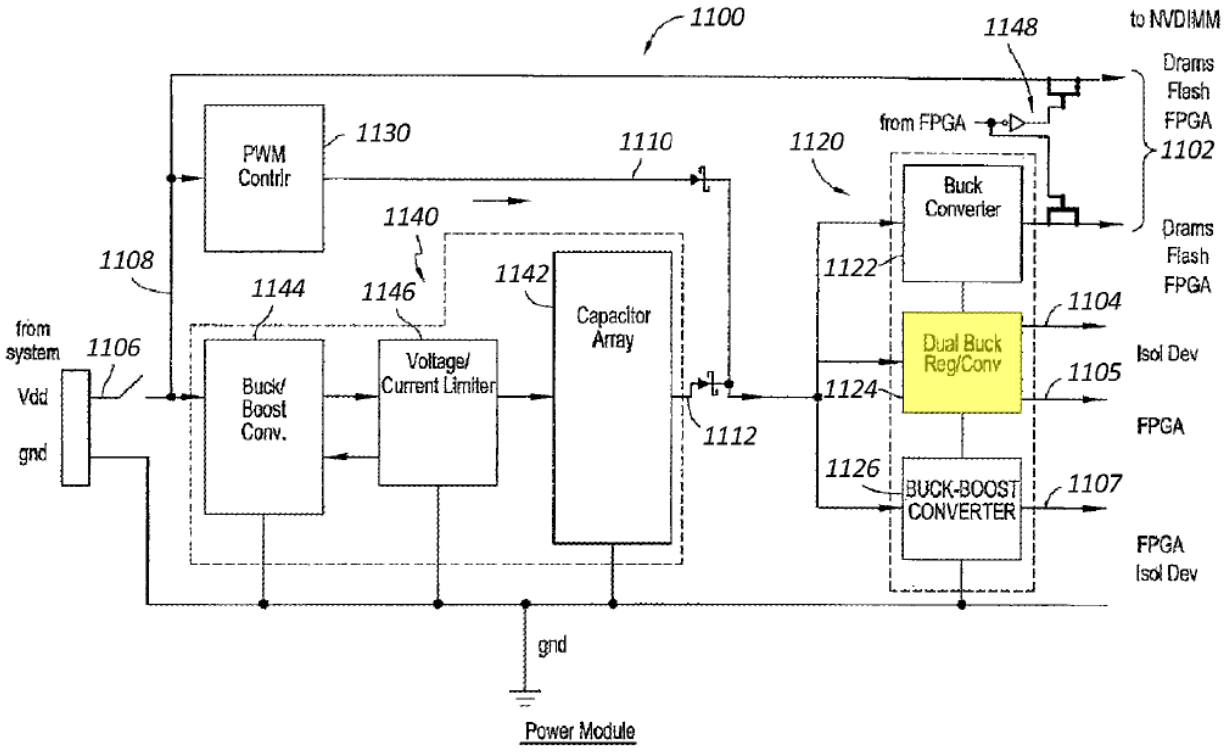


FIG. 16

Ex. 1001, at 29:28-29 ("sub-block 1124 comprises a dual buck converter"), Fig. 16 (annotated above, "Dual Buck Reg/Conv" 1124).

331. It would have been obvious, in view of the prior art references in each of Grounds 1 through 3, and the knowledge of a Skilled Artisan, to implement the first and third buck converters as a dual buck converter.

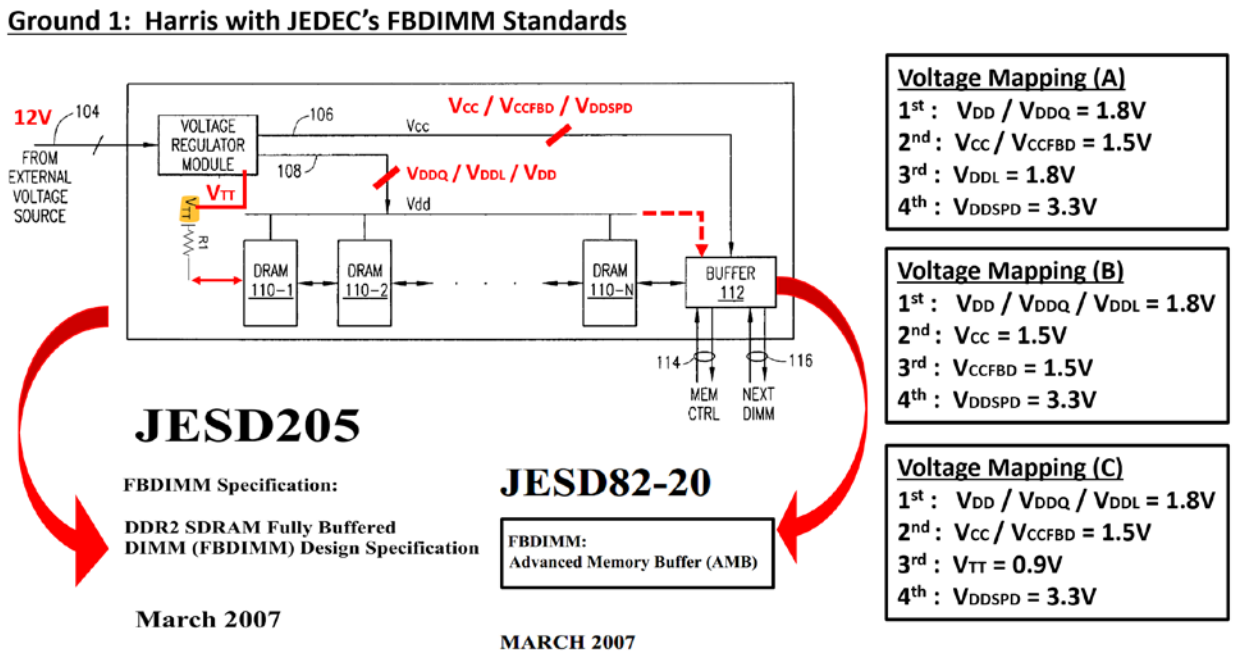
332. As explained above for claim limitation [1.c], the prior-art references in each of Grounds 1-3 satisfies "*a first buck converter configured to provide a first regulated voltage having a first voltage amplitude*." *Supra* ¶¶232-249. As explained for Grounds 1, 2A-2C, and 3A-3C, the on-board voltage regulator module includes the "*first buck converter*" that provides, for example, any one of

VDD, VDDQ, or VDDL as the "*first regulated voltage*" to the memory devices, such as DDR2 SDRAM. *Supra* ¶¶238-243, 244. And, as explained for Grounds 2D and 3D, the on-board voltage regulator module includes the "*first buck converter*" that provides, for example, VTT as the "*first regulated voltage*" as a termination voltage coupled to the memory devices. *Supra* ¶¶245-249.

333. In addition to the explanation above for claim limitation [1.c], as explained above for claim limitation [1.e], the prior art references in each of Grounds 1-3 satisfies "*a third buck converter configured to provide a third regulated voltage having a third voltage amplitude*." *Supra* ¶¶262-280. As explained for Grounds 1A, 2A, and 3A, the on-board voltage regulator includes the "*third buck converter*" that provides, for example, VDDL coupled to the memory devices and/or the buffer if the "*voltage amplitude[s]*" can be the same voltage under Patent Owner's interpretation. *Supra* ¶¶265-269. As explained for Grounds 1B, 2B, and 3B, the on-board voltage regulator includes the "*third buck converter*" that provides, for example, VCCFBD coupled to the buffer if the "*voltage amplitude[s]*" can be the same voltage under Patent Owner's interpretation. *Supra* ¶¶270-272. As explained for Grounds 1C, 2C, and 3C, the on-board voltage regulator includes the "*third buck converter*" that provides, for example, VTT coupled to the memory devices if each of the "*voltage amplitude[s]*" is interpreted to be different. *Supra* ¶¶273-276. As explained for Grounds 2D and 3D, the on-

board voltage regulator includes the "*third buck converter*" that provides, for example, VCCFPGA coupled to the Amidi's logic (e.g., FPGA) if each of the "*voltage amplitude[s]*" is interpreted to be different. *Supra* ¶¶277-280.

334. For Ground 1 (Harris in view of the FBDIMM Standards), I discussed three mappings for the "*regulated voltage[s]*," as shown in the figure below.



Ex. 1023 at Fig. 1A (annotated). For Ground 1A, the first voltage is VDD or VDDQ and the third voltage is VDDL. For Ground 1B, the first voltage is VDD, VDDQ, or VDDL, and the third voltage is VCCFBD. Ground 1C, the first voltage is VDD, VDDQ, or VDDL, and the third voltage is VTT.

335. For Ground 2 (Ground 1 in view of Amidi) and Ground 3 (Ground 2 in view of Hajeck), there are four mappings for the "*regulated voltage[s]*," as

shown in the figures below. As discussed before, the voltage mappings of Ground 3 are the same as Ground 2.

Ground 2: Ground 1 and Battery Backup of Amidi

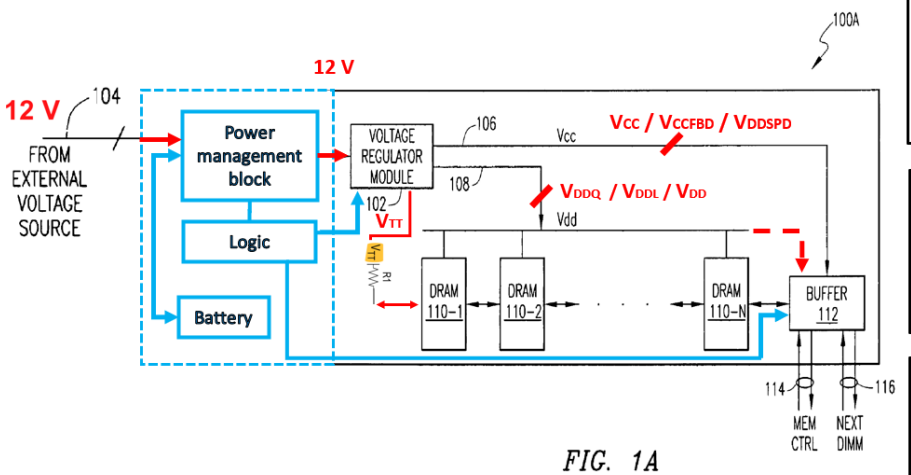


FIG. 1A

Voltage Mapping (A)
1st : VDD / VDDQ = 1.8V
2nd : VCC / VCCFBD = 1.5V
3rd : VDDL = 1.8V
4th : VDDSPD = 3.3V

Voltage Mapping (B)
1st : VDD / VDDQ / VDDL = 1.8V
2nd : VCC = 1.5V
3rd : VCCFBD = 1.5V
4th : VDDSPD = 3.3V

Voltage Mapping (C)
1st : VDD / VDDQ / VDDL = 1.8V
2nd : VCC / VCCFBD = 1.5V
3rd : VTT = 0.9V
4th : VDDSPD = 3.3V

Ground 2: Ground 1 and Battery Backup of Amidi

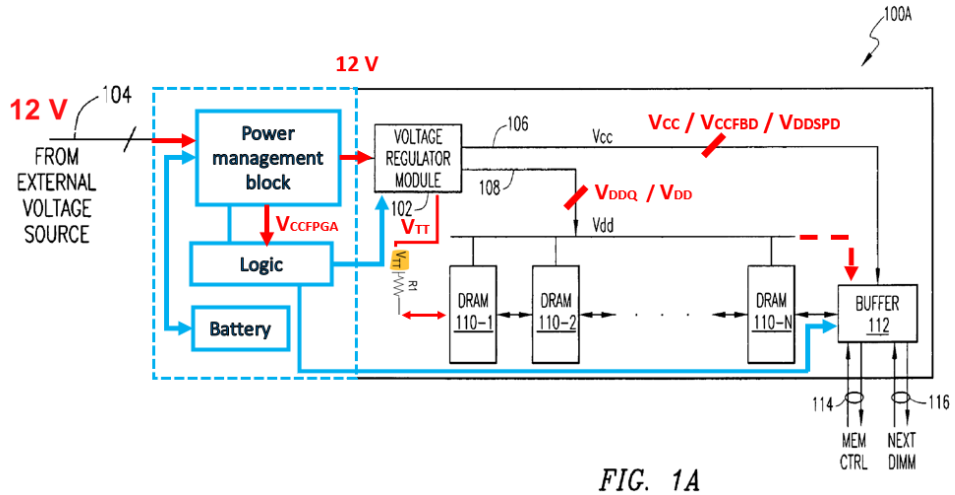


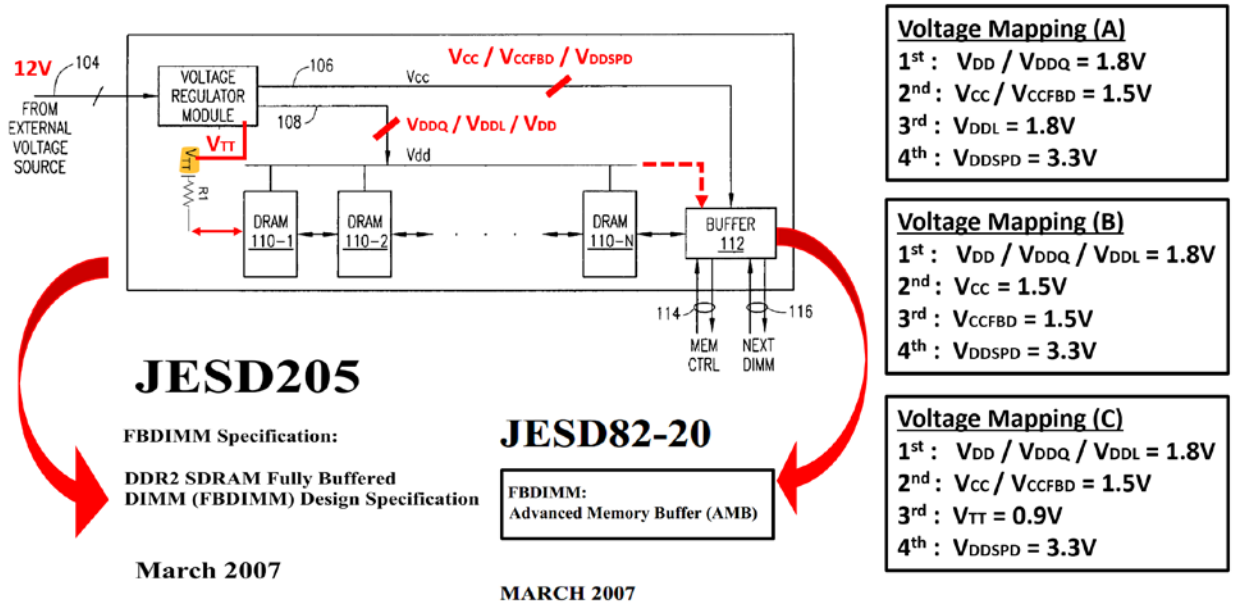
FIG. 1A

Voltage Mapping (D)
1st : VTT = 1.25V
2nd : VDD / VDDQ = 2.5V
3rd : VCCFPGA = 1.2V
4th : VDDSPD = 3.3V

336. For Grounds 2A-2C and 3A-3C, the voltage mappings are the same as Grounds 1A-1C, respectively. For Grounds 2D and 3D, the first voltage is VTT and the third voltage is VCCFPGA.

337. Additionally, as discussed for claim limitation [1.e] for the third buck converter, under Patent Owner's interpretation that the first and third buck converters can provide the same voltage amplitude, the "*first buck converter*" and "*third buck converter*" provide the same voltage amplitude. *Supra* ¶265; Ex. 1071 at 43; Ex. 1073 at 49-53. For example, as shown in the annotated figure below for Ground 1A, a Skilled Artisan would have recognized that the VDD voltage supply (e.g., "*first regulated voltage*") and VDDL voltage supply (e.g., "*third regulated voltage*") each have a voltage amplitude of 1.8 volts.

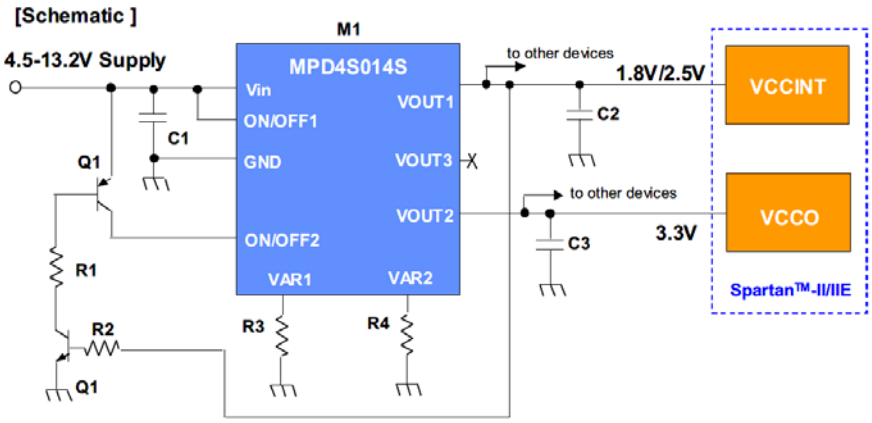
Ground 1: Harris with JEDEC's FBDIMM Standards



Ex. 1023 at Fig. 1A (annotated); Ex. 1008 at 6-7 (annotated). Similarly, the first and third voltages for Grounds 2A and 3A each have a voltage amplitude of 1.8 volts.

338. In each of the implementations with a first and third buck converter, and corresponding first and third regulated voltage, a Skilled Artisan would have been motivated to use a "*dual buck converter*" to provide the "*first regulated voltage*" and "*third regulated voltage*" because the two converters in a dual buck converter can be operated independently to provide different required voltages, and using a dual buck converter would use fewer integrated circuits, pins, and interconnections on the module, therefore simplifying its design as described below. Further, a Skilled Artisan would have recognized that such "*dual buck converters*" were designed, and readily available on the market at the time, for the functionality required by memory devices or modules.

339. For example, Murata offered a MPD4S014S dual buck converter with two different output voltages (e.g., 1.8V and 3.3V, similar to Ground 1B):

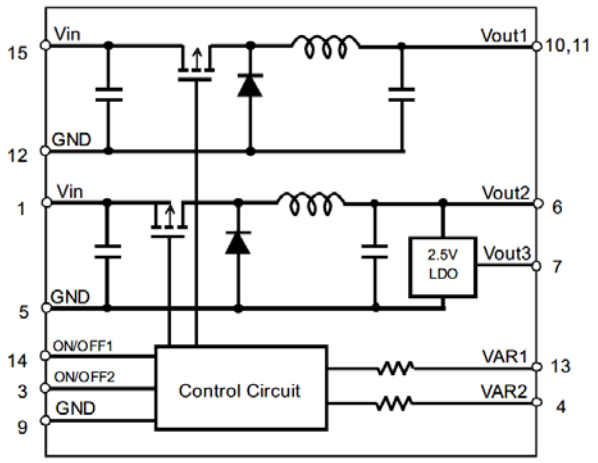


Ex. 1042 at 16. The block diagram for the MPDS014S is shown below:

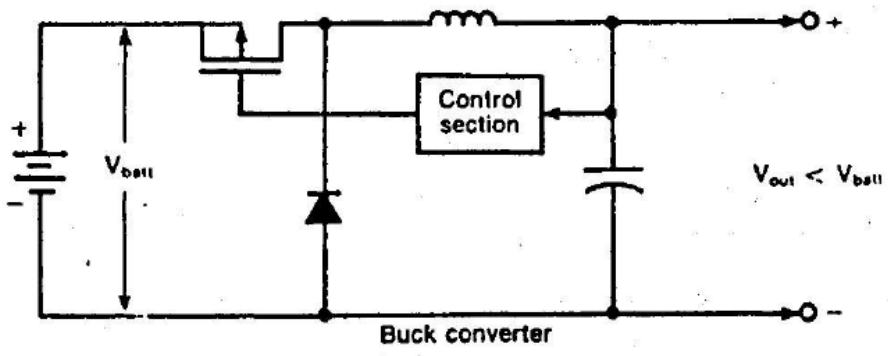
DC-DC Converter Specification(DRAFT)

MPD4S014S

6. Block Diagram



Ex. 1048 at 1-2. A Skilled Artisan would recognize from the block diagram above that there are two buck converters, as confirmed by the following figure from the Lenk textbook:

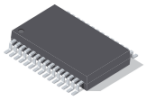


Ex. 1058 at 5. Thus, as shown above, the Murata MPD4S014S is a "*dual buck converter*" similar to Figure 16 of the 918 Patent because it outputs two regulated voltages from two buck converters.

340. As another example, Texas Instruments offered a TPS51020 dual buck voltage converter for DDR or DDR2.

TEXAS INSTRUMENTS

TPS51020



SLUS564B – JULY 2003 – REVISED DECEMBER 2003

DUAL, VOLTAGE MODE, DDR SELECTABLE, SYNCHRONOUS, STEP-DOWN CONTROLLER FOR NOTEBOOK SYSTEM POWER

Ex. 1040 at 1. The TPS51020 was used, for example, to implement a dual buck converter for the VDDQ and VTT voltage supplies (similar to Ground 1C). *See id.* at 11 ("TPS51020 gives a complete function set required for the DDR termination supply such as VDDQ/2 tracking V_{TT}").

341. As another example, Fairchild Semiconductor offered a FAN5026 Dual-Output PWM Controller:

FAIRCHILD SEMICONDUCTOR®

October 2005

FAN5026
Dual DDR/Dual-Output PWM Controller

Applications

- DDR V_{DDQ} and V_{TT} voltage generation

Circuit Description

Overview

The FAN5026 is a multi-mode, dual channel PWM controller intended for graphic chipset, SDRAM, DDR DRAM or other low output voltage power applications in PC's, VGA Cards and set top boxes. The IC integrates a control circuitry for two synchronous buck converters. The output voltage of each controller can be set in the range of 0.9V to 5.5V by an external resistor divider.

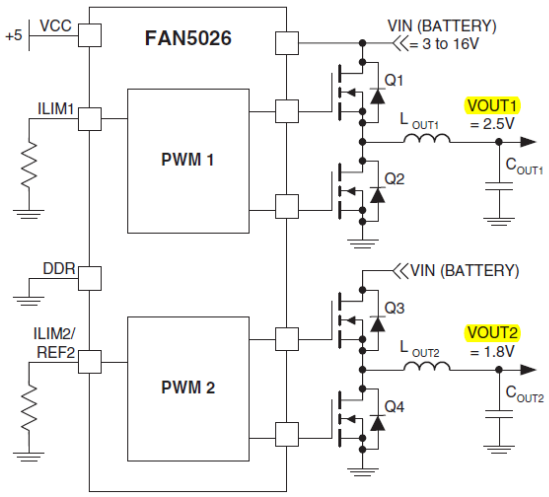


Figure 1. Dual Output Regulator

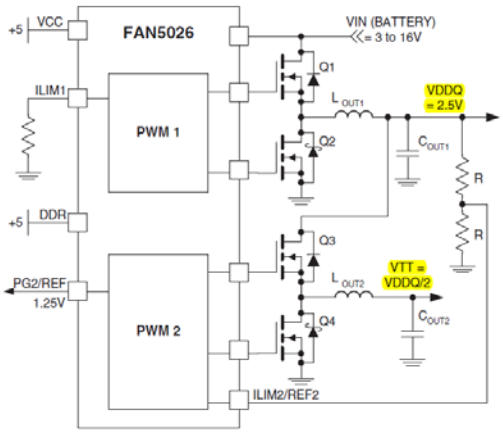


Figure 2. Typical Application

Ex. 1041 at 1 ("The output voltage of each controller can be set in the range of 0.9V to 5.5V by an external resistor divider."); *see also id.* at 2, 9. The two outputs could be implemented to provide two different voltages, such as VDDQ and VTT (similar to Ground 1C) or voltage supplies at 2.5 volts and 1.8 volts (similar to Ground 1A or 1B). *See, e.g.*, *id.* at 2 (Figs. 1 and 2), 7-8 (Figs. 4 and 5).

342. As shown above, dual buck converters were common and commercially available. Furthermore, an additional benefit of dual buck converters, like those above, was that the phases of the two voltages could be adjusted relative to each other, thus reducing any input "ripple" and improving performance. *See, e.g.*, Ex. 1041 at 9 ("When used as a dual converter …, out-of-phase operation with 180 degree phase shift reduces input current ripple."); Ex. 1040 at 10 ("Two channels are operated in 180 degrees out-of-phase interleave

switching mode. This interleaving helps reduce the input current ripple requirement for the input capacitor.").

343. As a further example, U.S. Patent No. 7,023,187 to Shearon ("Shearon") discloses a "dual buck-mode PWM power supply" that outputs two voltage supplies, such as VDDQ and VTT (similar to Ground 1C), with phase shifting. *See* Ex. 1047 at 3:49-50 (brief description of Fig. 2), 4:7-10, 4:37-56 (describing Vout1), 5:4-13, 5:46-59 (describing Vout2), Fig. 2 (illustrating dual buck-mode converter with Vout1 and Vout2).

344. Accordingly, it would have been obvious, in view of the prior art references in each of Grounds 1 through 3, and the knowledge of a Skilled Artisan, to implement the first and third buck converters as a dual buck converter.

345. I understand that Patent Owner has interpreted the claimed "*dual buck converter*" as reading on a *dual-phase* buck converter with a *single* output (such as VDD). *See* Ex. 1071 at 41, 43; Ex. 1073 at 49-50. The 918 Patent neither shows nor describes a dual-phase buck converter with a single output as a "*dual buck converter*."

346. Under Patent Owner's interpretation of the "*dual buck converter*," Ex. 1071 at 41, 43; Ex. 1073 at 49-50, a dual-phase buck converter would have been obvious given that Harris specifically discloses that the appropriate local voltage levels are, for example, provided by "multi-phase synchronous Pulse-

Width Modulated (PWM) controllers." Ex. 1023 at [0010] ("Preferably, a high-frequency switching voltage converter capable of generating tightly-controlled voltage levels may be implemented as the on-board VRM 102 for purposes of the present patent disclosure. For instance, multi-phase synchronous Pulse-Width Modulated (PWM) controllers . . . ."); *see also* Ex. 1032 at 161-64 (describing use of PWM controllers for buck converters). The "multiphase buck converter" circuits disclosed by Harris were known to provide several advantages, including "lower ripple," "higher current capability," and "smaller size." Ex. 1050 at 3:36-37, 2:19-20. Thus, in light of Harris's express teaching, it would have been obvious to use a dual-phase buck converter (for VDD, for example) to reduce ripples and decrease the size of the circuit, thus satisfying Patent Owner's apparent interpretation for "*dual buck converter*."

347. Accordingly, the prior art references in each of Grounds 1 through 3 satisfies the "*wherein the first and third buck converters are further configured to operate as a dual buck converter*" limitation.

3. Claim 3 is Unpatentable

348. Claim 3 is unpatentable as the prior art references in each of Ground 1 (Voltage Mappings A, B, and C) and Grounds 2 and 3 (Voltage Mappings A, B, and C) render the claim obvious

349. Claim 3 requires "*[t]he memory module of claim 1, wherein the first voltage amplitude is 1.8 volts.*"

350. The prior art references in each of Grounds 1, 2A-2C, and 3A-3C teach this limitation to a Skilled Artisan. In particular, each of these grounds map the first voltage to 1.8 volts.

351. Harris discloses in an embodiment that the memory devices implemented on the memory module are DDR2 devices with a voltage of 1.8 volts. *Supra* ¶¶232-249; Ex. 1023 at [0009] ("Also, the memory devices can be of any known or heretofore unknown DDR type, e.g., **DDR2 (operable with 1.8 V)**, DDR3 (operable with 1.35V to 1.5V), and the like.") (emphasis added); *see also id.* at [0002] ("Furthermore, each generation of DIMM/DRAM technology requires a different power supply which keeps getting lower (e.g., 3.3V, 2.5V, **1.8V**, 1.5V and beyond) . . . .") (emphasis added), [0011] ("Since the Vdd and Vcc power supply rails are rendered independent from external voltage sources, the overall power supply interface to the memory module 100A is improved to better support large memory capacity scaling, hot-pluggability, DRAM technology independence (e.g., **DDR2**, DDR3, DDR4, and other DRAM types) . . . .") (emphasis added).

352. These disclosures in Harris are confirmed by JEDEC standards related to DDR2. JESD79-2B discloses that DDR2 SDRAM is provided the voltage supplies VDD, VDDQ, and VDDL, each at 1.8 volts. *See* Ex. 1026 at 6-7.

JESD82-20 (part of the FBDIMM Standards) discloses that the Advanced Memory Buffer (AMB) on an FB-DIMM is provided the voltage supply VDD and/or VDDQ at 1.8 volts. *See* Ex. 1027 at 83. And, JESD205 (part of the FBDIMM Standards) discloses that the DDR2 SDRAM and AMB on an FB-DIMM are each provided the voltage supply VDD and/or VDDQ at 1.8 volts. *See* Ex. 1028 at 9, 15.

353. Accordingly, the prior art references in each of Grounds 1, 2A-2C, and 3A-3C satisfies the "*wherein the first voltage amplitude is 1.8 volts*" limitation.

4. Claim 4 is Unpatentable

354. Claim 4 is unpatentable as the prior art references in Grounds 2 and 3 (Voltage Mapping D) render the claim obvious.

355. Claim 4 requires *"[t]he memory module of claim 1, wherein the second, third, and fourth voltage amplitudes are 2.5 volts, 1.2 volts, and 3.3 volts, respectively*."

356. Harris in view of the FBDIMM Standards, and further in view of Amidi (Ground 2D), and further in view of Hajeck (Ground 3D) teaches this limitation to a Skilled Artisan.

Ground 2: Ground 1 and Battery Backup of Amidi

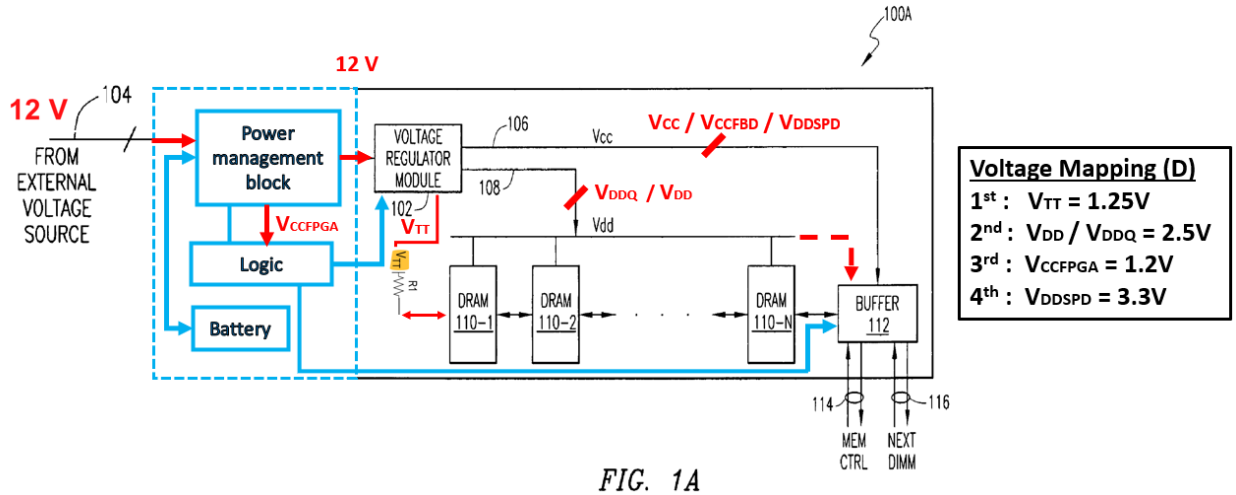


FIG. 1A

357. As explained above for Grounds 2D and 3D, the second voltage is VDD or VDDQ at 2.5 volts (*supra* ¶¶258-261), the third voltage is VCCFPGA at 1.2 volts (*supra* ¶¶277-280), and the fourth voltage is VDDSPD at 3.3 volts (¶¶281-287).

358. Accordingly, Harris in view of the FBDIMM Standards, and Amidi (Ground 2D), and further in view of Hajeck (Ground 3D) satisfies the "*wherein the second, third, and fourth voltage amplitudes are 2.5 volts, 1.2 volts, and 3.3 volts, respectively*" limitation.

5. Claim 5 is Unpatentable

359. Claim 5 is unpatentable as the prior art references in each of Grounds 2 and 3 (Voltage Mappings A, B, C, and D) render the claim obvious.

a) [5.a] Preamble

360. The preamble of claim 5 requires "*[t]he memory module of claim 1, further comprising*."

361. As explained above for claim 1, to the extent the preamble is limited, it is satisfied by Harris, which discloses a memory module. *Supra* ¶¶216-327; *see, e.g.*, Ex. 1023 at Figs. 1A, 3.

362. Accordingly, to the extent the preamble of claim 5 is limiting, the prior art references in each of Grounds 2-3 satisfies "*[t]he memory module of claim 1, further comprising*."

b) [5.b] Voltage Monitor Circuit

363. Claim 5 requires "*a voltage monitor circuit configured to monitor a power input voltage received via a second portion of the plurality of edge connections, the voltage monitor circuit configured to produce a trigger signal in response to the power input voltage having a voltage amplitude that is greater than a first threshold voltage*."

364. The prior art references in each of Grounds 2 through 3 teaches this limitation to a Skilled Artisan.

365. As discussed above, it would have been obvious to a Skilled Artisan to incorporate battery backup power, as taught by Amidi, when implementing the memory module teachings of Harris to address the case of a power or clock

malfunction. *Supra* ¶¶170-175. As shown in the figures below, Grounds 2 and 3 disclose a memory module with battery backup power for when there is a power or clock malfunction. As previously discussed, Ground 3 has the same Voltage Mappings as Ground 2. *Supra* ¶¶ 180-187.

Ground 2: Ground 1 and Battery Backup of Amidi

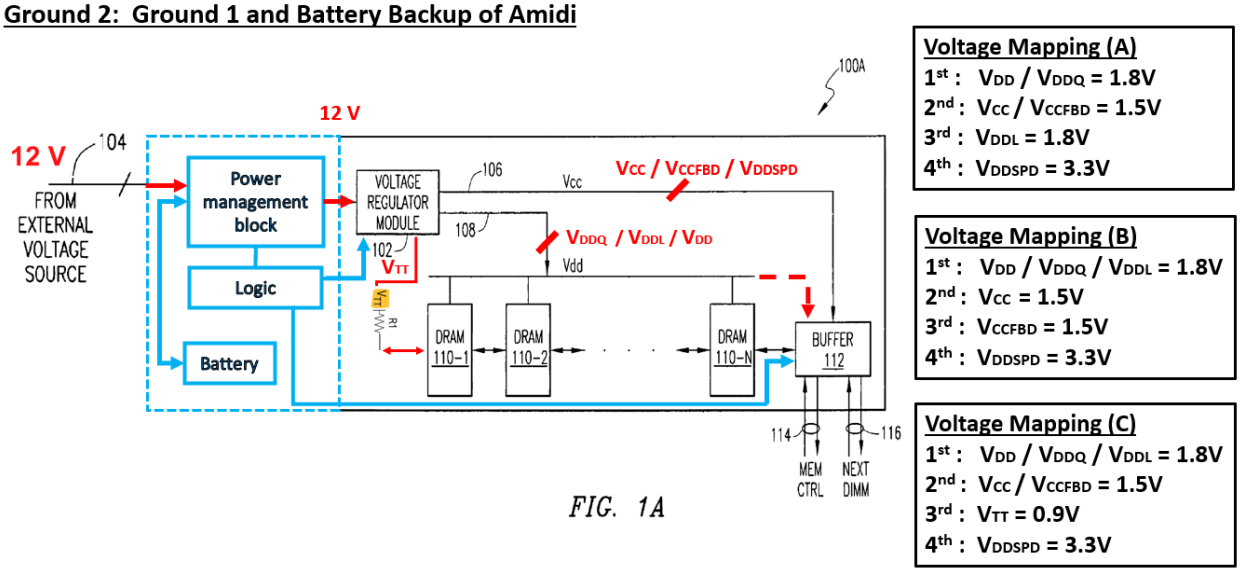


FIG. 1A

Ground 2: Ground 1 and Battery Backup of Amidi

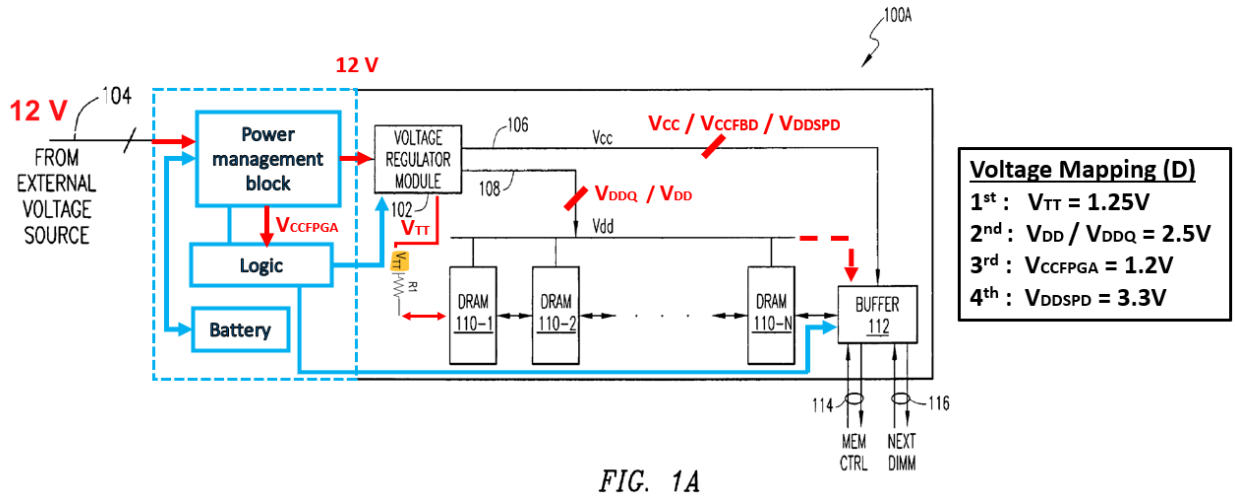
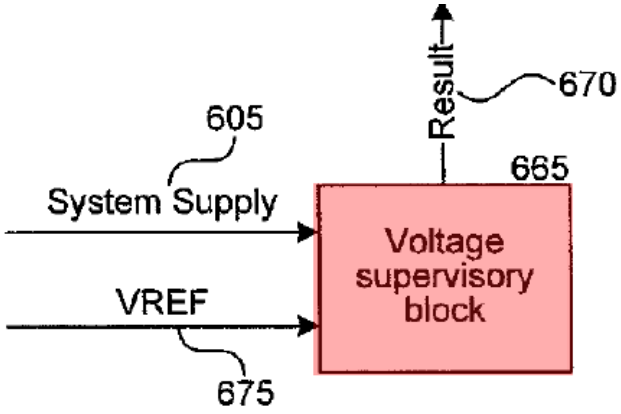


FIG. 1A

Ex. 1023 at Fig. 1A (annotated with teachings of Amidi); *see, e.g.*, Ex. 1024 at Abstract, 1:28-35, 2:6-26, Figs 5, 6. As shown, the memory module includes a

power management block, logic, and battery, as taught by Amidi. The power management block is coupled between the external voltage source 104 and battery, on one hand, and the voltage regulator module 102, on the other. And, the logic block is coupled to the power management block, the voltage regulator module 102, and the buffer 112. *See id.*

366. It would have been obvious to a Skilled Artisan that the prior art in each of Grounds 2 and 3 teaches and discloses "*a voltage monitor circuit configured to monitor a power input voltage received via a second portion of the plurality of edge connections*." As shown in the figure below from Amidi, each of the combinations discloses a "Voltage supervisory block" 665 (annotated in red) that is a "*voltage monitor circuit*."



Ex. 1024 at Fig. 6 (excerpted and annotated). The "Voltage supervisory block" is configured to monitor the "System Supply" 605 to determine if there is a power malfunction. *See id.* at 4:44-52, Fig. 6; *see also id.* at 5:25-43.

367. In the combinations illustrated and described above for Grounds 2 and 3, Amidi's voltage supervisory block is part of the power management block that is coupled to the external voltage source of Harris that is input at 12 volts. *See, e.g.*, Ex. 1024 (Amidi) at Figs. 5, 6. Thus, Amidi's voltage supervisory block monitors the external voltage source 104, such as one at 12 volts, which is received through some of the edge connections in Harris's memory module, as explained for claim limitation [1.b] ("*. . . plurality of edge connections configured to couple power, data, address and control signals between the memory module and the host system*"). *See supra* ¶¶228-231; *see also* Ex. 1023 (Harris) at [0010], [0012] (describing the number of pins for a 12 volt input from an external voltage source in various implementations), [0019], Fig. 1A; Ex. 1024 (Amidi) 8:23-29 and Fig. 14 (reproduced below) (illustrating a method that includes monitoring the input power supply at 1435), Fig. 15 and 9:8-12 (describing monitoring system, including monitoring input power supply for proper levels).

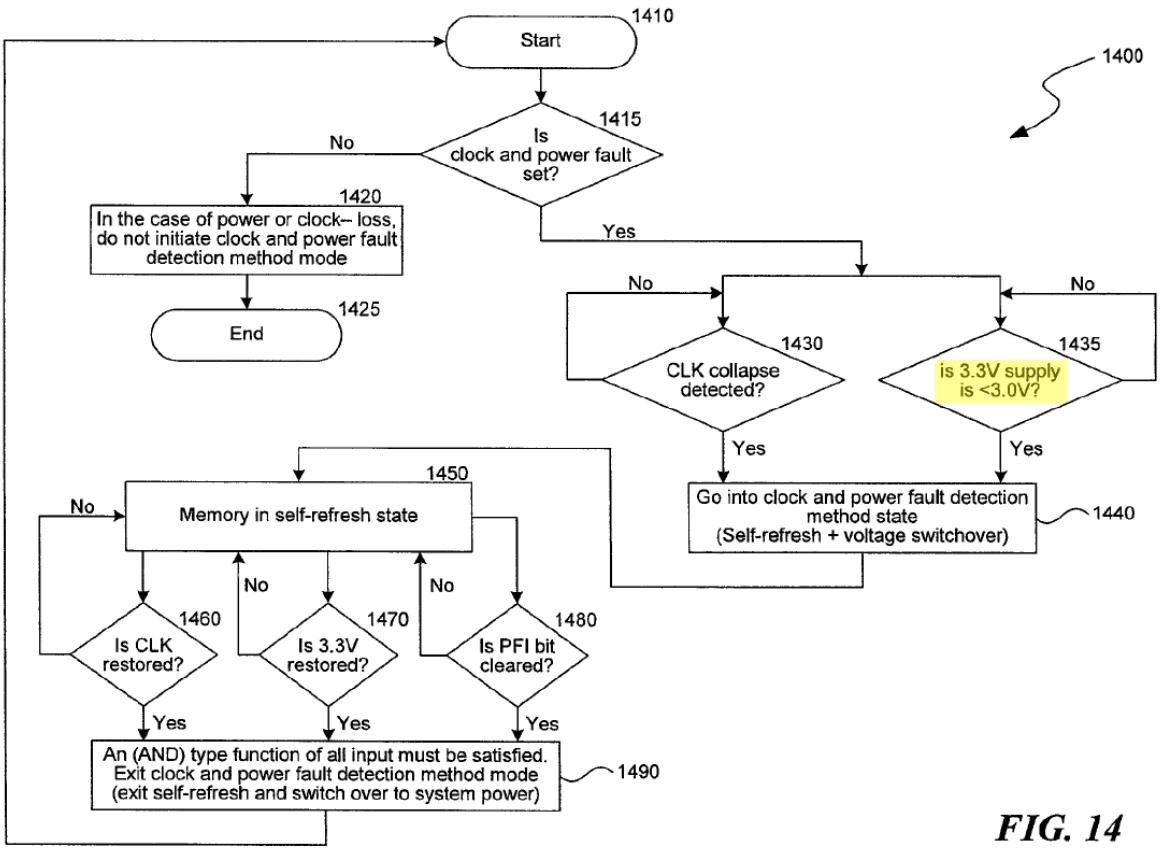


FIG. 14

Thus, each of the combinations teach and disclose that Amidi's "Voltage supervisory block" ("*a voltage monitor circuit*") is configured to monitor Harris's external voltage source input at 12 volts ("*configured to monitor a power input voltage*") that is received via a set of pins of the edge connections ("*received via a second portion of the plurality of edge connections*").

368. In addition, it would have been obvious to a Skilled Artisan that the prior art in each of Grounds 2 and 3 teaches "*the voltage monitor circuit* [is] *configured to produce a trigger signal in response to the power input voltage having a voltage amplitude that is greater than a first threshold voltage*." Although

Amidi teaches and discloses a circuit configured to "*produce the trigger signal in response to the power input voltage having a voltage amplitude that is less than a second threshold voltage*" (undervoltage protection), as recited in claim 6 and addressed below, Harris teaches both undervoltage and overvoltage protection. *See infra* ¶¶377-384 (claim 6); *see also* Ex. 1024 (Amidi) at 5:35-43, 8:23-29, 9:8-12, Figs. 6, 14. In particular, Harris teaches that a memory module can accommodate up to 15% variation above and below the nominal external supply voltage ("*power input voltage*"), which is not supplied directly to the memory devices or logic components of the memory module. Ex. 1023 (Harris) at [0013] ("Further, since the +12V power supply is not used directly by DRAM devices or buffer/logic components of the memory assembly, a wide tolerance (e.g., around +/−15%) can be accommodated . . . ."). Accordingly, Harris teaches that an input voltage amplitude greater than 15% above a nominal value or less than 15% below a nominal value cannot be accommodated.

369. A Skilled Artisan would have understood from, and been motivated by, this disclosure and teaching in Harris to include overvoltage protection in addition to undervoltage protection as taught by Amidi. As long as the input voltage amplitude remains within that range above or below 15% of the nominal value, such as 12 volts, that system supply voltage is provided to Harris's voltage regulator module, but when the system supply is beyond this range, the

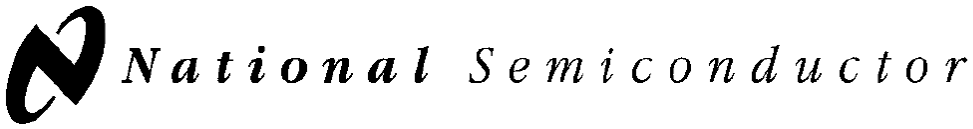
combination switches to battery backup, as Amidi teaches, to avoid supplying voltages that Harris's memory module cannot accommodate. *See* Ex. 1023 (Harris) at [0013]. Thus, a Skilled Artisan would have been motivated to modify Amidi's Voltage Supervisory Block 665 to generate a signal ("*trigger signal*") such that the battery backup is selected if the system supply voltage is less than 85% of the nominal value, such as 10.2 volts for a 12-volt supply, (*see* "*second threshold voltage*" of claim 6 below) or if it is greater than 115% of the nominal value, such as 13.8 volts for a 12-volt supply ("*first threshold voltage*"). Otherwise, the system supply is selected when the system supply voltage ("*power input voltage*") is between the "*second*" and "*first*" threshold voltages.

370. Such a modification of Amidi's Voltage Supervisory Block was well within the level of skill of a Skilled Artisan at the time.

371. For example, U.S. Patent Publication No. 2009/0034354 to Resnick ("Resnick") describes generating "an alarm signal if the difference between the operating voltage and the reference voltage indicates the operating voltage is outside of a normal operating range" for a memory device. Ex. 1065 at Abstract, [0014], Fig. 1. For example, the alarm signal is generated when "the operating voltage [is] above an upper threshold or below a lower threshold." *Id.* at Fig. 5 (block 530). Resnick explains that a "voltage sensor 110 may be configured to signal an alarm in the case where the operating voltage is outside of a range" which

relates to the "magnitude of the voltage [going] beyond a predetermined threshold level, which may be an upper or lower level relative to an expected, or normal operating voltage." *Id.* at [0018]. Further, "[i]f the operating voltage is above or below the relevant threshold, voltage sensor 110 may indicate the voltage failure by sending a flag such as alarm signal 112 to a pin on semiconductor memory device 100 for signaling the alarm externally." *Id.* at [0019]; *see also id.* at [0031], [0033], Figs. 1-3. Thus, by way of example, Resnick shows that, at the time, a Skilled Artisan would have been able to design a voltage detection circuit that detects different types of anomalies on a memory module, including the amplitude of the voltage going beyond a predetermined level, and that indicates a voltage failure by sending a flag such as an alarm signal.

372. As another example, a National Semiconductor datasheet for LMC6953 describes an over-voltage threshold of 5.6 volts for a 5-volt power supply. *See* Ex. 1063 at 1-2 (reproduced below and annotated for both over-voltage and under-voltage).



LMC6953
PCI Local Bus Power Supervisor

DC Electrical Characteristics

Unless otherwise specified, all **boldface** limits guaranteed for T_J = 0°C to 70°C, V_{DD} = 5V, $R_{PULL-UP}$ = 4.7 kΩ and C_{EXT} = 0.01 µF. Typical numbers are room temperature (25°C) performance.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{H5}	V_{DD} Over-Voltage Threshold	(Note 4)	**5.45**	5.6	**5.75**	V
V_{L5}	V_{DD} Under-Voltage Threshold	(Note 4)	**4.25**	4.4	**4.55**	V
$V_{H3.3}$	3.3V Over-Voltage Threshold	(Note 5)	**3.8**	3.95	**4.1**	V
$V_{L3.3}$	3.3V Under-Voltage Threshold	(Note 5)	**2.5**	2.65	**2.8**	V

373. As another example, an Analog Devices datasheet for ADM1066 describes programmable circuits to "detect an undervoltage fault (the input voltage drops below a preprogrammed value), an overvoltage fault (the input voltage rises above a preprogrammed value), or an out-of-window fault (undervoltage or overvoltage)." Ex. 1061 at 15; *see also* Ex. 1062 at 15 ("Two comparators are dedicated to each input so that undervoltage and overvoltage detection can be implemented . . . .").

374. Accordingly, the prior art references in Ground 2 (Grounds 1 in view of Amidi) satisfies the limitation.

375. To the extent one were to argue that overvoltage protection was not obvious in light of Ground 2, it would have been obvious in further view of Hajeck, as part of Ground 3. As explained above, a Skilled Artisan would have been motivated to combine the references in Ground 2 with Hajeck. *See supra* ¶¶180-187; *see also supra* ¶137. U.S. Patent No. 6,858,556 to Hajeck ("Hajeck") describes the operation of a "conventional voltage detection circuit." Ex. 1038 at 3:33-34; *see also id.* at Abstract, 1:62-2:7, 3:30-4:9. Hajeck discloses:

> "[A] voltage detection circuit 48 [that] is responsible for detecting anomalies in the power signal V_{IN} supplied by the host on line 36, and for driving the ready/busy signal to the 'busy' state when such anomalies are detected. A conventional voltage detection circuit may be used. The voltage detection circuit 48 may be designed to generate a 'busy' signal whenever V_{IN} falls below a certain level, such as 2.6 or 2.7 volts. **The voltage detection circuit may also be designed to generate a busy signal when the voltage exceeds a certain level, and/or when other types of anomalies are detected**. To inhibit rapid transitions between the 'ready' and 'busy' states, the **voltage detection circuit may be designed to provide a degree of hysteresis, and/or to hold its output for a particular time period after a state transition**."

Id. at 3:30-43 (emphasis added). Thus, Hajeck shows that, at the time, a Skilled Artisan would have been able to design a voltage detection circuit that detects multiple types of anomalies, including when the voltage exceeds a certain level, and that provides hysteresis and holds its output for a period of time after a state transition. In light of Hajeck's and Amidi's teachings, a Skilled Artisan would have understood that Amidi's voltage supervisory block would be modified to detect voltage anomalies and switch to the backup power not only "[i]f system supply 605 has a magnitude lower than reference voltage 675" as disclosed by Amidi (Ex. 1024 at 4:44-53), but also "when the voltage exceeds a certain level" as taught by Hajeck (Ex. 1038 at 3:30-40). Indeed, as discussed above, the problems caused by such overvoltage conditions, and solutions to detect and protect against them, were well known at the time. Accordingly, Skilled Artisan would have understood that, to avoid these well-known problems, Hajeck's "conventional

voltage detection circuit" teachings on detecting both under- and over-voltage conditions were readily available at the time. Ex. 1038 at 3:30-40.

376. Accordingly, the prior art references in Ground 3 (Ground 2 in view of Hajeck) also satisfies the "*a voltage monitor circuit configured to monitor a power input voltage received via a second portion of the plurality of edge connections, the voltage monitor circuit configured to produce a trigger signal in response to the power input voltage having a voltage amplitude that is greater than a first threshold voltage*" limitation.

6. Claim 6 is Unpatentable

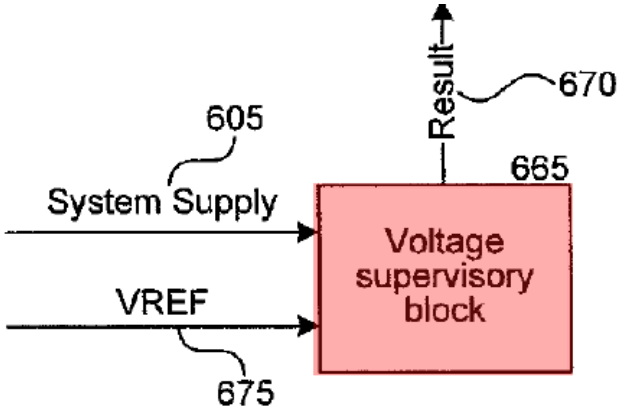
377. Claim 6 is unpatentable as the prior art references in each of Grounds 2 and 3 (Voltage Mappings A, B, C, and D) render the claim obvious.

378. Claim 6 requires "*[t]he memory module of claim 5, wherein the voltage monitor circuit is further configured to produce the trigger signal in response to the power input voltage having a voltage amplitude that is less than a second threshold voltage*."

379. The prior art references in Grounds 2 and 3 each teaches this limitation to a Skilled Artisan.

380. As discussed above with reference to claim limitation [5.b], Amidi teaches and discloses undervoltage protection ("*the power input voltage having a voltage amplitude that is less than a second threshold voltage*"). *See supra* ¶¶363-

376. In particular, Amidi discloses a "Voltage supervisory block" 665 as shown in red in the figure below.



Ex. 1024 at Fig. 6 (excerpted and annotated). The "Voltage supervisory block" is configured to monitor the "System Supply" 605 to determine if there is a power malfunction. *See id.*; *see also id.* at 5:35-43. As Amidi explains, "Signal 670 is controlled by voltage supervisory block 665, which receives system supply 605 and a reference voltage 675, and compares the two. If system supply 605 has a greater magnitude than reference voltage 675, signal 670 causes power switch multiplexer 655 to choose system supply 605 as a source for memory supply 660. If system supply 605 has a magnitude lower than reference voltage 675, then signal 670 causes power switch multiplexer 655 to choose battery power 650 for memory supply 660." *Id.* at 5:35-43. Therefore, Amidi discloses that its voltage supervisory block 665 ("*voltage monitor circuit*") produces signal 670 that causes system supply 605 to be selected as the voltage source for the memory module ("*a trigger*

signal") in response to the input system supply ("*power input voltage*") having a greater magnitude than a reference voltage 675 ("*having a voltage amplitude that is greater than a first threshold voltage*").

381. Indeed, in addition to overvoltage protection, implementing undervoltage protection was well within the level of skill of a Skilled Artisan at the time. *See supra* ¶¶370-373. For example, Resnick shows that, at the time, a Skilled Artisan would have been able to design a voltage detection circuit that detects different types of anomalies on a memory module, including the amplitude of the voltage going beyond a predetermined level, and that indicates a voltage failure by sending a flag such as an alarm signal. *See* Ex. 1065 (Resnick) at Abstract, [0014], [0018], [0031], [0033], Figs. 1-3, 5. As another example, a National Semiconductor datasheet for LMC6953 describes an under-voltage threshold of 4.4 volts for a 5-volt power supply. *See* Ex. 1063 at 1-2 (describing both over-voltage and under-voltage). As another example, an Analog Devices datasheet for ADM1066 describes programmable circuits to "detect an undervoltage fault (the input voltage drops below a preprogrammed value), an overvoltage fault (the input voltage rises above a preprogrammed value), or an out-of-window fault (undervoltage or overvoltage)." Ex. 1061 at 15; *see also* Ex. 1062 at 15 ("Two comparators are dedicated to each input so that undervoltage and overvoltage detection can be implemented . . . .").

382. As explained above, a Skilled Artisan would have understood from, and been motivated by, this disclosure and teaching in Harris to include overvoltage protection in addition to undervoltage protection as taught by Amidi. *See supra* ¶¶369-374. Accordingly, a Skilled Artisan would have been motivated to modify Amidi's Voltage Supervisory Block 665 to generate a signal ("*trigger signal*") such that the battery backup is selected if the system supply voltage less than 85% of the nominal value, such as 10.2 volts for a 12-volt supply, (*see* "*second threshold voltage*" of claim 6 below) and if it is greater than 115% of the nominal value, such as 13.8 volts for a 12-volt supply ("*first threshold voltage*"). Otherwise, the system supply is selected when the system supply voltage ("*power input voltage*") is between the "*second*" and "*first*" threshold voltages.

383. To the extent one were to argue that overvoltage protection was not obvious in light of Ground 2, it would have been obvious in light of Hajeck, as part of Ground 3. As explained for claim limitation [5.b], a Skilled Artisan would have understood that Amidi's voltage supervisory block would be modified to detect voltage anomalies and switch to the backup power not only "[i]f system supply 605 has a magnitude lower than reference voltage 675" as disclosed by Amidi (Ex. 1024 at 4:44-53), but also "when the voltage exceeds a certain level" as taught by Hajeck (Ex. 1038 at 3:30-40). *See supra* ¶¶137, 180-187, 375.

384. Accordingly, the prior art references in each of Grounds 2 and 3 satisfies the "*wherein the voltage monitor circuit is further configured to produce the trigger signal in response to the power input voltage having a voltage amplitude that is less than a second threshold voltage*" limitation.

7. Claim 7 is Unpatentable

385. Claim 7 is unpatentable as the prior art references in each of Grounds 2 and 3 (Voltage Mappings A, B, C, and D) render the claim obvious.

386. Claim 7 requires *"[t]he memory module of claim 6, wherein the second threshold voltage corresponds to a voltage level that is ten percent less than a specified operating voltage*."

387. The prior art references in Grounds 2 and 3 each teaches this limitation to a Skilled Artisan.

388. As discussed above with reference to claims 5 and 6, the combinations including Harris and Amidi teaches and discloses that the "*second threshold voltage*" is 15 percent less than a nominal value of the system supply voltage. *Supra* ¶¶360-376 (claim 5), ¶¶377-384 (claim 6).

389. In addition, a 5 percent tolerance was also obvious to a Skilled Artisan at the time. For example, Amidi discloses a 5 percent tolerance in the specific implementation shown in its Figure 6. *See* Ex. 1024 (Amidi) at Fig. 6 ("VREF=1.71V (%5 of 1.8V SUPPLY"). Similarly, JEDEC's DDR2 SDRAM

Specification, JESD79-2B, discloses a tolerance of approximately 5 percent. Ex. 1026 at pp.6-7 ("1.8V +/- 0.1V").

390. A Skilled Artisan would have understood that any values between 5 and 15 percent were equally obvious and accounted for nothing more than an obvious design choice. For example in Harris, the external voltage (12V) is stepped down by voltage regulators to the voltages used by the parts in the module, including the memory devices. Thus, a Skilled Artisan would have understood that the tolerance on the input voltage (+/-15%, Ex. 1023 at [0013]) can be larger than the tolerance of the memory devices (5%, e.g., Ex. 1026 at pp.6-7). Therefore, a Skilled Artisan would have understood and been motivated to select a tolerance between 5% and 15% for the module. A Skilled Artisan would have also understood that allowing too high a tolerance carries the risk of losing data or damaging the devices on the memory module because the module cannot "tolerate" the voltage change. Ex. 1023 at [0013] (explaining the "tolerance" Harris's module can handle). A Skilled Artisan would have also understood that setting too low a tolerance carries the risk of unnecessary interruptions of operation powered by the system supply, because the module could "tolerate" the temporary change of the power. *Id*. In particular, a Skilled Artisan would have understood that the choice of around a 10 percent tolerance provided a reasonable compromise between the risks associated with too high a tolerance and too low a tolerance. For example, a

National Semiconductor datasheet for LMC6953 describes a tolerance for over-voltage and under-voltage protection of approximately 10 percent. Ex. 1063 at 1-2 (describing an Over-Voltage Threshold of about 5.6V and an Under-Voltage Threshold of about 4.4V for a +5V power supply, excerpted and annotated below).

National Semiconductor

LMC6953
PCI Local Bus Power Supervisor

DC Electrical Characteristics

Unless otherwise specified, all **boldface** limits guaranteed for T_J = 0°C to 70°C, V_{DD} = 5V, $R_{PULL-UP}$ = 4.7 kΩ and C_{EXT} = 0.01 μF. Typical numbers are room temperature (25°C) performance.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{H5}	V_{DD} Over-Voltage Threshold	(Note 4)	**5.45**	5.6	**5.75**	V
V_{L5}	V_{DD} Under-Voltage Threshold	(Note 4)	**4.25**	4.4	**4.55**	V
$V_{H3.3}$	3.3V Over-Voltage Threshold	(Note 5)	**3.8**	3.95	**4.1**	V
$V_{L3.3}$	3.3V Under-Voltage Threshold	(Note 5)	**2.5**	2.65	**2.8**	V

391. As another example of the choice of around a 10 percent tolerance providing a reasonable compromise between the risks associated with too high a tolerance and too low a tolerance, Amidi discloses an implementation for monitoring a power rail of 3.3V and comparing it to a 3.0V reference voltage, corresponding to a "*second threshold voltage*" of about 10 percent below the power rail's nominal voltage. *See* Ex. 1024 at Fig. 14 (reproduced below, annotated), 8:23-36; *see also* Ex. 1027 at 32 (stating VDDSPD has a typical voltage of 3.3 volts with a minimum voltage 10 percent below the typical voltage,

or 3.0 volts, and a maximum voltage 10 percent above the typical voltage, or 3.6 volts); Ex. 1061, p.15 (programmable under- and over-voltage protection over a wide range, including 10%).

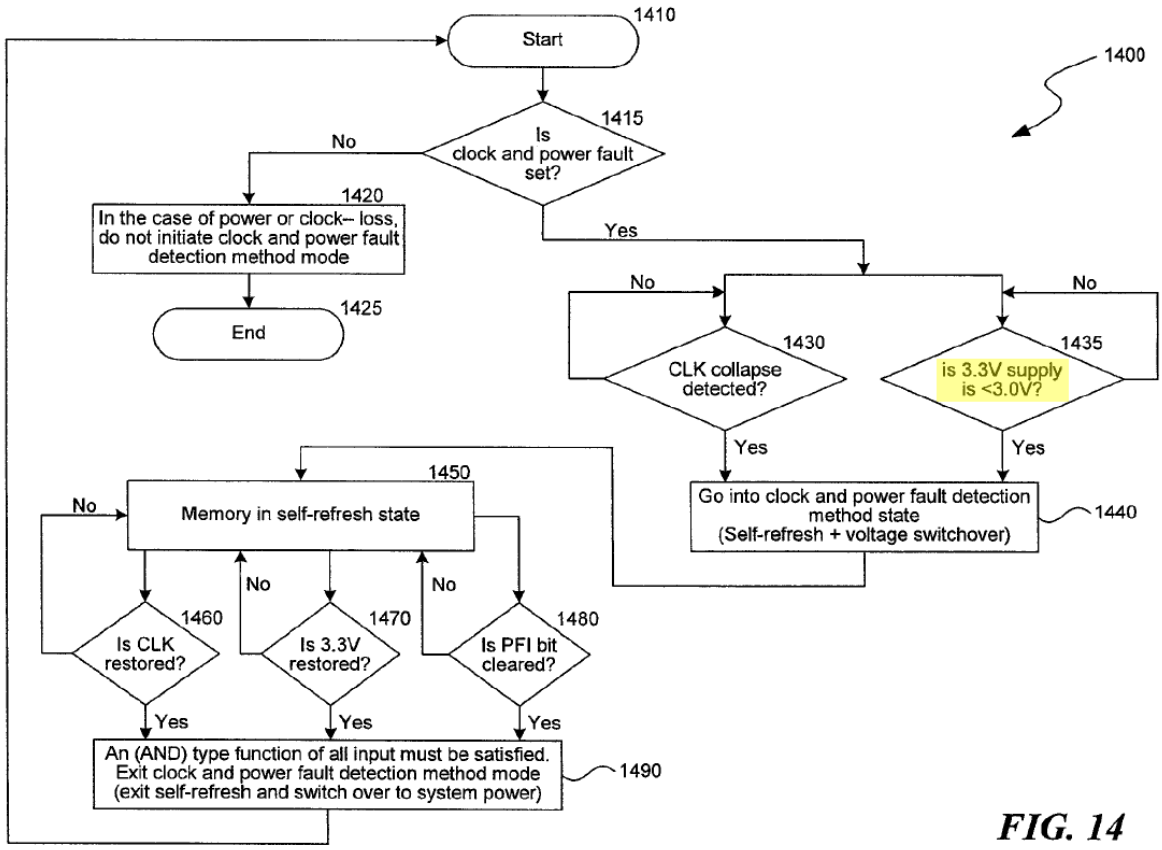


FIG. 14

Therefore, a Skilled Artisan would have understood that "*the second threshold voltage corresponds to a voltage level that is ten percent less than a specified operating voltage*" was obvious in view of the prior art references in Grounds 2 and 3.

392. Accordingly, the prior art references in each of Grounds 2 and 3 satisfies the "*wherein the second threshold voltage corresponds to a voltage level that is ten percent less than a specified operating voltage*" limitation.

8. Claim 8 is Unpatentable

393. Claim 8 is unpatentable as the prior art references in each of Grounds 1 through 3 (Voltage Mappings A, B, and C) render the claim obvious.

a) [8.a] Preamble

394. The preamble of claim 8 requires "*[t]he memory module of claim 1, the plurality of components further comprising*."

395. The prior art references in each of Grounds 1 through 3 teach this limitation to a Skilled Artisan.

396. As explained above for claim 1, the prior art references in each of Grounds 1 through 3 satisfy the limitations of claim 1. *Supra* ¶¶215-327.

397. Accordingly, the prior art references in each of Grounds 1 through 3 satisfies "*[t]he memory module of claim 1, the plurality of components further comprising*."

b) [8.b] One or More Registers

(1) [8.b.1] Coupled to one of the regulated voltages

398. Claim 8 requires "*one or more registers coupled to one of the first, second, third and fourth regulated voltages*."

399. The prior art references in each of Grounds 1 through 3 teach this limitation to a Skilled Artisan.

400. A Skilled Artisan would have understood and it would have been obvious to her that the prior art in Grounds 1 through 3 teaches and discloses a memory module including "*one or more registers*." A Skilled Artisan would have understood that a "*register*" can buffer incoming signals and then output them according to a clock signal. Thus, a Skilled Artisan would have understood that buffer 112 in Harris includes "*one or more registers*" for the address, control, and data signals. Ex. 1023 at Fig. 1A, [0009] ("a fully buffered DIMM wherein a buffer/logic component 112 is provided for buffering command/address (C/A) space as well as data space at least for a portion of the memory devices 110-1 through 110-N."). A Skilled Artisan would have understood that such a "buffering" in a fully buffered DIMM includes registering the address, control, and data signals in response to a clock signal. For example, JESD82-20 (part of the FBDIMM Standards) discloses that the "DDR interface on the Advanced Memory Buffer consists of . . . [a] DDR cluster which serves as a DIMM buffer by registering outbound commands and data at output flops. The cluster also captures and levelizes incoming read data." Ex. 1027 at 19.

401. Harris also discloses the use of clock signals on the memory module, including by buffer 112. Ex. 1023 at Fig. 3 (reproduced below, annotated), [0017]

("A clock source 308 is operable to drive a plurality of clock signals to the memory boards via a clock bus 314. Additionally, the clock source 308 is also operable to drive a clock signal 316 to the memory controller 302 for providing a time base with respect to its operations.").

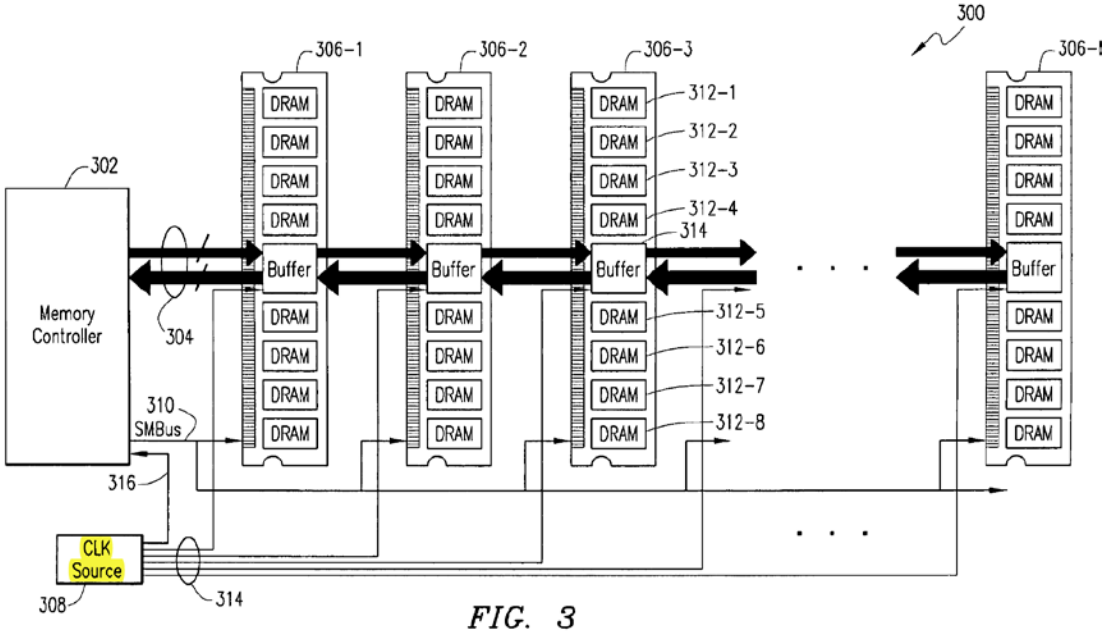
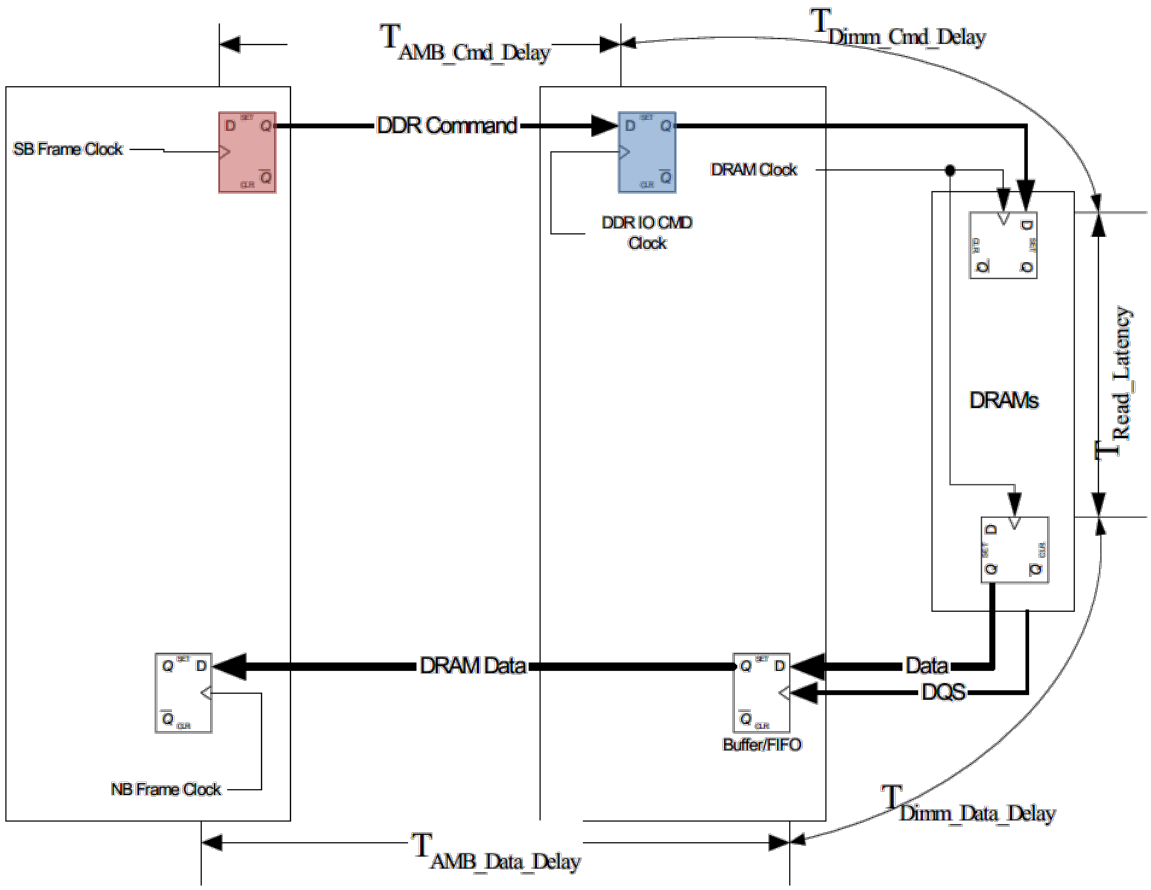


FIG. 3

402. Accordingly, a Skilled Artisan would have understood from Harris's disclosure that address and control signals for the DRAM memory devices are registered in registers ("*one or more registers*") at the system bus interface by the buffer 112 according to the system clock. *See e.g.*, Ex. 1027 (JESD82-20) at 16, Fig. 2.1. As shown below, Figure 2.1 of JESD82-20 (part of the FBDIMM Standards) describes an AMB buffer (like buffer 112 in Harris) that includes registers, annotated in red, using the SB Frame Clock to register DDR commands and, (after decoding) forwarding those commands to another set of registers of the

AMB, annotated in blue, which are clocked by a DDR IO CMD Clock for interfacing with the DRAMs.

Figure 2.1 — Delays Through an AMB



Id.; *see also id.* at p.3 (Fig. 1.1) (Advanced Memory Buffer Block Diagram) (showing "DRAM Cmd" and "DDR State Controller and CSRs" input to mux providing "Cmd Out" to "DDR IO's," which provides "DRAM **Address**/CommandCopy1") (emphasis added), 7 (defining "Resample" and "Resync"), 19 ("FIFO write buffer" that "fills at half of the DDR data rate, and empties at the DDR data rate"), 20 ("Two sets, or copies, of DRAM command and

address output pins are provided for loading and timing considerations."), (showing registers, like the ones above, for "DRAM CMD/ADD"), 82 ("SCK" AMB Clock"). Thus, prior art references in each of Grounds 1 through 3 satisfy "*one or more registers*."

403. In addition, a Skilled Artisan would have understood and it would have been obvious to her that the prior art in Grounds 1 through 3 teaches and discloses a memory module with one or more registers that are "*coupled to one of the first, second, third and fourth regulated voltages*." For example, a Skilled Artisan would have recognized that the registers (red) registering the command and address signals from the FBD bus in the buffer 112 are coupled to one of the regulated voltages VCC and VCCFBD (1.5V for "core IO" and "FBD high speed IO"). Ex. 1027 at 83.

Power Supplies		
VCC (24 pins)	A	1.5V nominal supply for core IO
VCCFBD (8 pins)	A	1.5V nominal supply for FBD high speed IO
VDD (24 pins)	A	1.8V nominal supply for DDR IO
VSS (156 pins)	A	Ground
VDDSPD	A	3.3V nominal supply for SMB receivers and ESD diodes

See also Ex. 1028 at 30 (describing VCC and VCCFBD as 1.5V for AMB Core and Channel I/O Power).

Power/Ground Signals		213
V_{CC}	AMB Core Power (1.5 Volt)	24
V_{CCFBD}	AMB Channel I/O Power (1.5 Volt)	8
V_{DD}	AMB DRAM I/O Power (1.8 Volt)	24
V_{DDSPD}	SPD Power (3.3 Volt)	1
V_{SS}	Ground	156

Indeed, a Skilled Artisan would have understood that the address and command signals are captured and communicated in the AMB using the 1.5V supply of VCCFBD and VCC power for the core and channel input/output (I/O).

404. For the reasons discussed above with reference to claim 1, VCC and VCCFBD are at least "*one of the first, second, third and fourth regulated voltages,*" for example the "*second*" and/or the "*third*" regulated voltages. *Supra* ¶¶250-261 (claim limitation [1.d] ("*second regulated voltage*")), ¶¶262-280 (claim limitation [1.e] ("*third regulated voltage*")), ¶¶318-323 (claim limitation [1.i.3] ("*the at least one circuit coupled to both the second regulated voltage and the fourth regulated voltage*"); *see also* ¶¶270-272 (claim limitation [1.e] ("*third regulated voltage*") for Grounds 1B, 2B, and 3B, discussing VCCFBD as the "*third regulated voltage*" supplied to the buffer (AMB)).

405. Accordingly, the prior art references in each of Grounds 1 through 3 satisfies "*one or more registers coupled to one of the first, second, third and fourth regulated voltages*."

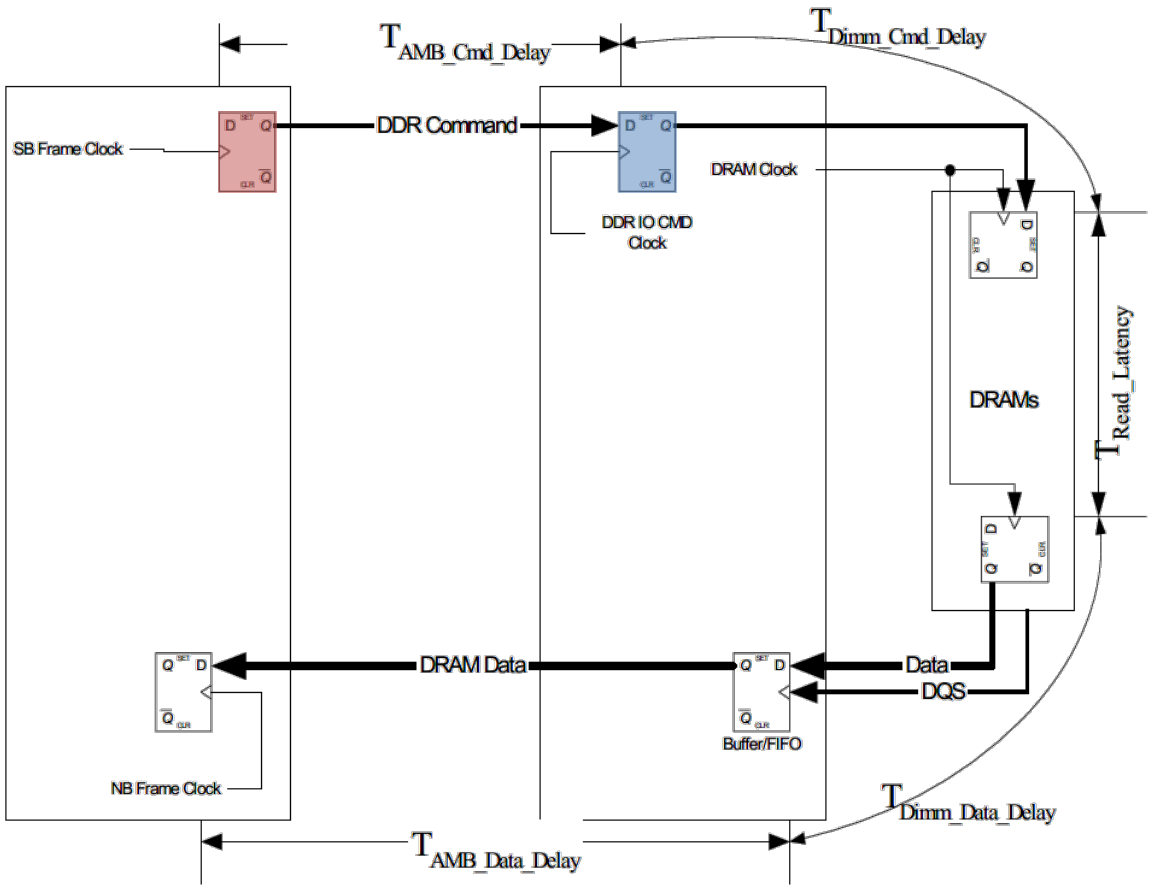
(2) [8.b.2] Configured to register address and control signals

406. Claim 8 requires "*the one or more registers configured to register, in response to a clock, the first plurality of address and control signals*."

407. The prior art references in each of Grounds 1 through 3 teach this limitation to a Skilled Artisan.

408. As explained above for claim limitation [8.b.1], Harris teaches and discloses that its buffer 112 includes registers and provides buffering for the address, control, and data signals and that a clock source provides clock signals to the memory modules, such as FB-DIMMs. *Supra* ¶¶398-405; Ex. 1023 at Fig. 1A, 3, [0009], [0017]. A Skilled Artisan would have understood from Harris's disclosure that the registers "*register, in response to a clock, the first plurality of address and control signals*." As shown below, Figure 2.1 of JESD82-20 (part of the FBDIMM Standards) shows registers, annotated in red, that register DDR commands (that include address and control signals) in response to the SB Frame Clock, and similar registers, annotated in blue, that again register those commands in response to a DDR IO CMD Clock for interfacing with the DRAMs.

Figure 2.1 — Delays Through an AMB



Id.; *see also id.* at p.3 (Fig. 1.1) (Advanced Memory Buffer Block Diagram) (showing "DRAM Cmd" and "DDR State Controller and CSRs" input to mux providing "Cmd Out" to "DDR IO's," which provides "DRAM **Address**/CommandCopy1") (emphasis added), 7 (defining "Resample" and "Resync"), 19 ("FIFO write buffer" that "fills at half of the DDR data rate, and empties at the DDR data rate"), 20 ("Two sets, or copies, of DRAM command and address output pins are provided for loading and timing considerations."), 82 ("SCK" AMB Clock").

409. Accordingly, the prior art references in each of Grounds 1 through 3 satisfies "*the one or more registers configured to register, in response to a clock, the first plurality of address and control signals*."

(3) [8.b.3] Wherein one of the voltages is selectively switched off

410. Claim 8 requires "*wherein the one of the first, second, third and fourth regulated voltages is selectively switched off to turn power off to the one or more registers while one or more components of the plurality of components are powered on*."

411. The prior art references in Grounds 1 through 3 each teaches this limitation to a Skilled Artisan.

412. With respect to Grounds 2-3, Amidi discloses that, in the case of power failure, the system address and control signals are disconnected from the memory module and, instead of these signals, the memory devices are controlled by a Finite State Machine which generates refresh commands. As annotated in Figure 12 of Amidi, reproduced below, the "FSM Control, Command Bus" 1245 provides the "Memory Control, Command Bus" signals at the output of the multiplexer array 1240 rather than the "System Control, Command Bus" 1235 in this scenario.

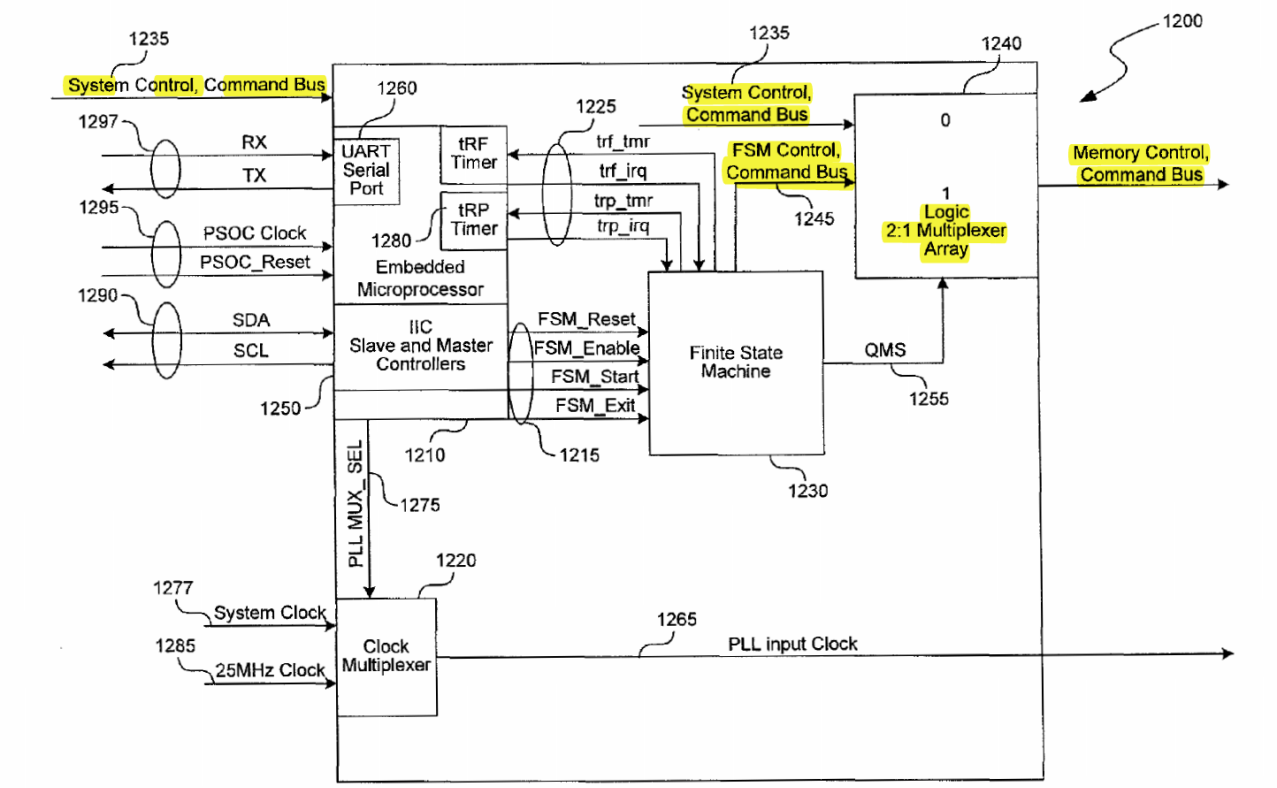


FIG. 12

Ex. 1024 at Fig. 12 (annotated). Amidi explains that "[t]his allows PSOC 1210 to produce finite state machine signals 1215 and timer signals 1225. These signals are used to **control finite state machine 1230, which produces signals that control refresh of memory of a memory module**. This also produces signal logic multiplexer select signal 1255, which **selects an input for multiplexer 1240**. Multiplexer 1240 is a logic signal multiplexer, accepting as input a set of system control and command bus signals 1235 and sets of finite state machine control and command bus signals 1245 to produce memory control and command bus signals." *Id.* at 7:24-34 (emphasis added).

413. A Skilled Artisan would have understood from this disclosure that, in the combination of Harris and Amidi, there is no need for the buffer 112 of Harris to register address, control, and data signals from the host, because those signals would not be acted upon, because the memory devices are only refreshed when battery backup power is used, as disclosed by Amidi. Furthermore, a Skilled Artisan would have understood that interfaces, such as the interface between the buffer 112 of Harris and the host computer (e.g., memory controller 302 in Figure 3 of Harris), include analog circuits that, when switched off, provide a "large power saving potential." Ex. 1033 (Prete) at 1:51-53 ("analog circuits used in interfaces exhibit, for example, a large power saving potential"), 9:57-60 ("analog circuits, especially used in the interface of the module 230, have an enormous power saving potential"), 12:50-58 ("In the case of a memory system according to the FBDIMM architecture, the power saving mode implemented in the embodiment of a memory buffer 100 cannot only differ with respect to analog circuit components and digital circuit components being switched off or deactivated according to the power saving mode, but also, components of the memory buffer 100 can be selectively switched on, depending on the direction of the bus structure of the bus 140 to which they are connected."). In addition, a Skilled Artisan would also have understood that power can be turned off by a switch which connects and disconnects the supply of power from a buck converter,

or by turning off the buck converter itself. A Skilled Artisan would have also understood that each of these implementations would have been an obvious design choice. On one hand, turning off the buck converter would save power and extend the life of the battery backup. Thus, a Skilled Artisan would turn off the buck converter if extending the life of the battery backup is a primary concern. On the other hand, using a switch without turning off the buck converter itself would reduce any delays associated with starting the operation of the buck converter when the power is switched back to the system power supply. Thus, a Skilled Artisan would only use a switch without turning off the buck converter if reducing delays when returning to normal operation is important. For example, the FAN5026 data sheet discloses that "Initialization and Soft start" is measured "in seconds" for a capacitance value that "is in µF." Ex. 1041 (FAN5026) at 10; *see also id.* at 7, 10 (describing a 10nF soft-start capacitor (e.g., C2 or C3) that would require a start time of approximately 1,800 microseconds, or (0.9 * 10nF)/5); *see also id.* at 13, 21 (Fig. 12) (showing a soft-start time up to 50,000 microseconds, or 0.05 seconds). In comparison to the start time of a buck converter which may be thousands of microseconds, NAND flash memory, for example, is able to write a page of data in only 300 or so microseconds. *See* Ex. 1049 at 1 ("Write Performance," "Page program: 300µs (TYP)"). As another example, U.S. Patent No. 5,563,839 to Herdt *et al.* discloses "isolation switch circuitry" including a

large n-channel MOSFET "for connecting and disconnecting" a device from its power supply. *See* Ex. 1056 at 5:15-26, Fig. 3. Either way, a Skilled Artisan would have been motivated to switch off power for the buffer 112, including its analog circuits and input registers to register address, command, and data signals, to save power and extend the lifetime of the backup battery power supply. However, the power is not switched off for the DRAM memory devices because they perform refresh operations, as taught by Amidi. Thus, the VCC supply to the buffer is switched off whereas the VDD supply to at least the memory devices remains switched on.

414. Furthermore, a Skilled Artisan would have recognized that when implementing the memory module in Harris, the buffer 112 would have supported being put into an S3 sleeping mode when the external voltage source is decoupled by Amidi's voltage supervisory block. For example, JESD82-20 (part of the FBDIMM Standards, focused on the AMB buffer), discloses that "S3 is an ACPI mode in which the DIMMs are put into a very lower power state, with the DRAMs in self refresh mode." Ex. 1027 at 39 (Section 4.1.3). It also discloses that "[w]hen the Advanced Memory Buffer [AMB] core logic is in S3 power mode, all command/address outputs, including CKE, ODT, CLK, and all other command/address pins, will be driven low. In S3 mode, 1.8V supply is on. 1.5V, Vtt, and 3.3V are off. DRAMs are in self refresh, and the CKE signals must be

driven low." *Id.* at 21 (point 6). Therefore, a Skilled Artisan would have been motivated to use the S3 mode of the buffer 112 when implementing the backup power supply functionality as disclosed in Amidi because the S3 mode performs the function of refreshing the memory, just like in Amidi. Amidi's logic would have been implemented in a simpler way as it would put the buffer 112 into S3 sleep mode and does not have to duplicate this functionality already implemented in the buffer 112. A Skilled Artisan would have understood that the S3 sleep mode uses a small amount of power, thus extending the life of the battery when backup power is used. *See also* Ex. 1039 at [0065] (describing power saving operations for AMB).

415. A Skilled Artisan would have also understood that, in S3 sleep mode, the registers for capturing the address and command signals in the buffer 112 are also powered off because the 1.5 volt (VCC and VCCFBD) supply is off, and "all command/address outputs, including CKE, ODT, CLK, and all other command/address pins, will be driven low." Ex. 1027 at 21 (point 6). Indeed, in S3 sleep mode, the address and command signals going to the memories are "driven low," thus no address and command signals are sent to the memory devices and there is no need for powering the registers whose function is to register such address and command signals. *Id.* at 39 (Section 4.1.3) (explained that S3 is a "very low power state").

416. A Skilled Artisan would have also been motivated to selectively switch off power at least to the interfaces, including the registers and corresponding analog circuitry, because they provide an "enormous power saving potential." Ex. 1033 at 9:57-60 ("analog circuits, especially used in the interface of the module 230, have an enormous power saving potential"). Accordingly, a Skilled Artisan would have been at least motivated to switch off power to the interfaces, including the registers and corresponding analog circuitry, to extend the battery life. As discussed above, ¶413, a Skilled Artisan would also have understood that either the buck converter providing that voltage is switched off, or a switch would be used to connect and disconnect the supply of power from the buck converter to reduce any delays associated with starting operation of the buck converter itself when the power supply is switched back to the system power supply. *See, e.g.*, Ex. 1040 at 13, 21; Ex. 1041 at 10; Ex. 1049 at 1; Ex. 1056 at 5:15-26, Fig. 3.

417. Such an implementation would have been well within the level of skill, because the S3 sleep mode was standardized at the time, thus a Skilled Artisan would have known how to implement it. Additionally, selectively turning off the power to interfaces, including registers in an FBDIMM like that of Harris, was also well within the level of skill at the time. *See, e.g.*, Ex. 1033 at 12:50-58 ("In the case of a memory system according to the FBDIMM architecture, the

power saving mode implemented in the embodiment of a memory buffer 100 cannot only differ with respect to analog circuit components and digital circuit components being switched off or deactivated according to the power saving mode, but also, components of the memory buffer 100 can be selectively switched on, depending on the direction of the bus structure of the bus 140 to which they are connected.").

418. Additionally, a Skilled Artisan would also have been familiar with memory systems that powered down their buffer for buffering command, address, and/or data signals. For example, U.S. Patent No. 5,563,839 to Herdt ("Herdt") discloses disabling input buffers to reduce current draw in response to a sleep signal. *See* Ex. 1056 at Abstract, 3:5-11 ("Lastly, the preferred embodiment of the present invention includes at least one input buffer for buffering signals being transmitted into the nvSRAM device. The input buffer is known to sink current whenever the input signal being applied to it is at an intermediate level between power supply and ground. The invention provides circuitry for disabling the input buffers in response to a sleep signal."). As another example, U.S. Patent No. 6,693,840 to Shimada discloses decoupling the volatile memory from the external memory controller so its data can be saved to non-volatile memory. *See, e.g.*, Ex. 1057 at Figs. 2-3, 3:45-4:34 (disclosing that a memory device, when running

on temporary backup power, transfers data internally from volatile to non-volatile memories and "shuts out any access to the volatile memory … from the outside").

419. With respect to Ground 1, a Skilled Artisan would have understood that the S3 sleep mode was available for the memory module of Harris with or without the battery backup of Amidi. For the reasons discussed above, Harris discloses an FBDIMM implementation, and a Skilled Artisan would have understood that the FBDIMM can be put into the S3 sleep mode, and she would have been motivated to use the S3 mode to save power. *Supra* at ¶¶414-418; *see also* Ex. 1023 (Harris) at [0009] (disclosing that the implementation of Fig. 1A is a fully buffered DIMM), Ex. 1027 (JESD82-20) at 21 ("When the Advanced Memory Buffer core logic is in S3 power mode, all command/address outputs, including CKE, ODT, CLK, and all other command/address pins, will be driven low. In S3 mode, 1.8V supply is on. 1.5V, Vtt, and 3.3V are off. DRAMs are in self refresh, and the CKE signals must be driven low.") and 39 (Section 4.1.3 disclosing S3 specifications, including switching off VCC, and drawing power only from VDD to maintain the DRAMs in self refresh). As also discussed above, when the module is in S3 mode, the power (VCC/VCCFBD) for the registers in the AMB is turned off while the power VDD for the memory devices is on. *Id*. Therefore, it would have been at least obvious to a Skilled Artisan to put Harris's module into S3 mode and selectively switch off regulated voltages, including

VCC/VCCFBD that power the input/output registers of the AMB, while the volatile DRAMs are still powered on, so they can refresh the stored information.

420. Accordingly, the prior art references in each of Grounds 1 through 3 satisfies "*wherein the one of the first, second, third and fourth regulated voltages is selectively switched off to turn power off to the one or more registers while one or more components of the plurality of components are powered on*."

9. Claim 9 is Unpatentable

421. Claim 9 is unpatentable as the prior art references in each of Grounds 2 and 3 (Voltage Mappings A, B, C, and D) render the claim obvious.

422. Claim 9 requires "*[t]he memory module of claim 5, wherein the first threshold voltage corresponds to a voltage level that is ten percent greater than a specified operating voltage*."

423. The prior art references in Grounds 2 and 3 each teaches this limitation to a Skilled Artisan.

424. As discussed for claim 7, the prior art references in each of Grounds 2 and 3 satisfies the "*wherein the second threshold voltage corresponds to a voltage level that is ten percent less than a specified operating voltage*" limitation. *Supra* ¶¶385-392. For the same reasons why the "*second threshold voltage*" is "*ten percent less than a specified operating voltage*," the same combination renders

obvious "*the first threshold voltage corresponds to a voltage level that is ten percent greater than a specified operating voltage*."

425. As discussed for claim 5, to the extent one were to argue that overvoltage protection was not obvious in light of Ground 2, it would have been obvious in light of Hajeck, as part of Ground 3. *Supra* ¶¶375-376.

426. Accordingly, the prior art references in each of Grounds 2 and 3 satisfies the "*wherein the first threshold voltage corresponds to a voltage level that is ten percent greater than a specified operating voltage*" limitation.

10. Claim 10 is Unpatentable

427. Claim 10 is unpatentable as the prior art references in each of Grounds 2 and 3 (Voltage Mappings A, B, C, and D) render the claim obvious.

a) [10.a] Preamble

428. The preamble of claim 10 requires "*[t]he memory module of claim 5, the plurality of components further comprising*."

429. The prior art references in Grounds 2 and 3 each teaches this limitation to a Skilled Artisan.

430. As explained above for claim 5, the prior art references in each of Grounds 2 and 3 satisfy the limitations of claim 5. *Supra* ¶¶359-376.

431. Accordingly, the prior art references in each of Grounds 2 and 3 satisfies "*[t]he memory module of claim 5, the plurality of components further comprising*."

b) [10.b] A Logic Element

432. Claim 10 requires "*a logic element including a non-volatile memory, the non-volatile memory is configured to store configuration information*."

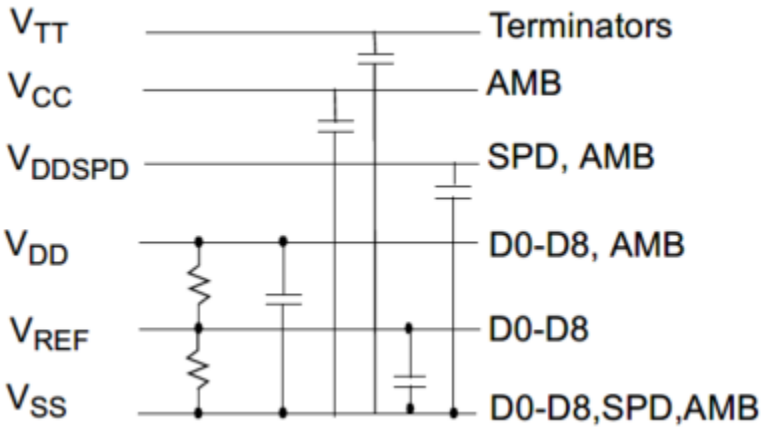
433. The prior art references in Grounds 2 and 3 each teaches this limitation to a Skilled Artisan.

434. As discussed above with reference to claim limitation [8.b.3], the combination of Harris (in Grounds 2 and 3) with Amidi discloses to a Skilled Artisan that when implementing the memory module of Harris with the buffer 112, the module and buffer include support for S3 sleep mode to be used during backup power to enable self-refresh of the memory devices. *See supra* ¶¶410-420.

435. In addition, Harris discloses to a Skilled Artisan that when implementing a memory module with the buffer 112, the components on the memory module include a logic element, including, e.g., logic implemented in the buffer 112, that writes configuration data into non-volatile memory before entering S3 sleep mode and recovers the stored configuration data before resuming normal operations. *See* Ex. 1027 at 25 (Section 3.7.3) ("The following [Control and Status Registers] should be stored in non-volatile memory before entering S3 mode and

restored before normal DRAM transactions begin."); *see also id.* at 95 (Table 11.7) (showing DAREFTC, MTR, DSREFTC, DRC registers), 96 (Table 11.8) (showing S3RESTORE registers), 141 ("Section 11.6.1.3 S3RESTORE[15:0] : DDR State Restore").

436. A Skilled Artisan would have understood that the non-volatile memory can be internal or external to the buffer 112. For example, JESD205 (part of the FBDIMM Standards) discloses that the VDDSPD voltage supply at 3.3 volts is coupled to both the AMB buffer and serial presence detect (SPD) EEPROM. Ex. 1028 at 13-16 (excerpt from p.13 reproduced below), 30 ("SPD Power (3.3 Volt)"), 32 (illustrating AMB pin assignment for VDDSPD at AB27).

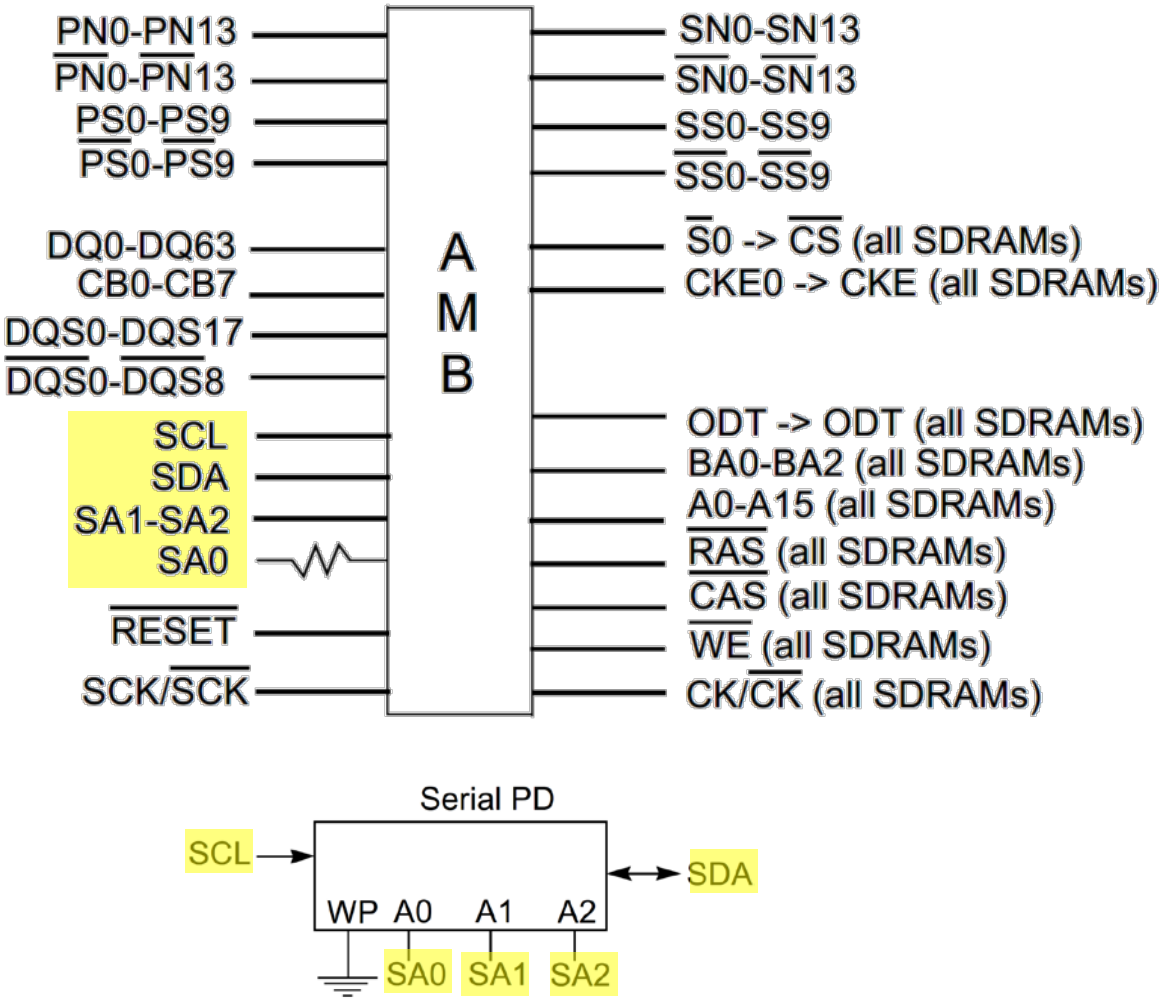


This indicates to a Skilled Artisan that the AMB buffer, like the SPD, can contain non-volatile memory, such as an EEPROM, for storing configuration information using a higher voltage supply at 3.3 volts. Furthermore, it would have been obvious to a Skilled Artisan to implement the buffer 112 with an internal non-volatile memory because it would decrease the number of components, interfaces

and interconnections on the memory module, resulting in a cheaper, faster, and more secure solution. *See e.g.*, Ex. 1023 (Harris) at [0002] (discussing cost-effective support for next generation DRAM technology), [0012] (discussing reduced pins), [0019] (discussing a "reduction in the pin count" and reserving "extra pins for implementing additional or proprietary functions"); Ex. 1066 at 26:64-27:4 ("In embodiments, modes of operation are determined in response to a control signal from master 2101, or other circuit or in response to reading configuration information ***stored in a separate storage circuit in a device, such as an SPD device or register on the buffer or controller device***, disposed on system 2600. Modes of operation may be determined at initialization, periodically or during calibration of system 2600.") (emphasis added); Ex. 1067 (LatticeXP Datasheet) at 1-1 (describing FPGA technology with internal non-volatile memory and explaining its advantages, including "Instant-on—powers up in microseconds," "No external configuration memory," "Excellent design security, no bitstream to intercept") and 2 ("With this [re-programmable non-volatile] technology, expensive external configuration memories are not required and designs are secured from unauthorized read-back. In addition, instant-on capability allows for easy interfacing in many applications.").

437. With regards to non-volatile memory that is external to the buffer, JESD205 (part of the FBDIMM Standards) illustrates that the SPD EEPROM, a

non-volatile memory, is coupled to the AMB buffer via SCL, SA0, SA1, SA2, and SDA.



Ex. 1028 at 13 (excerpted and annotated). Accordingly, a Skilled Artisan would have understood that the non-volatile memory is internal or external to the buffer 112. Thus, the "*logic element*" includes the logic in the buffer 112 and non-volatile memory (e.g., internal or external to the buffer) for storing configuration information as required by the S3 sleep mode.

438. Accordingly, the prior art references in each of Grounds 2 and 3 satisfies "*a logic element including a non-volatile memory, the non-volatile memory is configured to store configuration information*."

11. Claim 11 is Unpatentable

439. Claim 11 is unpatentable as the prior art references in each of Grounds 2 and 3 (Voltage Mappings A, B, C, and D) render the claim obvious.

440. Claim 11 requires "*[t]he memory module of claim 10, wherein, in response to the trigger signal, the logic element writes information into the non-volatile memory*."

441. The prior art references in Grounds 2 and 3 each teaches this limitation to a Skilled Artisan.

442. As discussed above with reference to claim limitation [5.b] and claim 6, the combination of Harris (in Grounds 2 and 3) with Amidi teaches a voltage monitor circuit configured to produce a trigger signal for backup power in response to the power input voltage having an amplitude greater than a first threshold voltage (e.g., overvoltage) or less than a second threshold voltage (e.g., undervoltage). *Supra* ¶¶363-376, 377-384. As discussed above with reference to claim limitation [8.b.3], the combination of Harris (in Grounds 2 and 3) with Amidi discloses to a Skilled Artisan that when implementing the memory module of Harris with the buffer 112, the module and buffer include support for S3 sleep

mode to be used during backup power to enable self-refresh of the memory devices. *Supra* ¶¶410-420. Further, as discussed with reference to claim 10, the prior art references in each of Grounds 2 and 3 satisfies "*a logic element including a non-volatile memory, the non-volatile memory is configured to store configuration information*." *Supra* ¶¶432-438. In particular, the buffer 112 includes a logic element which in response to the trigger signal, writes configuration data into non-volatile memory before entering S3 sleep mode and recovers the stored configuration data before resuming normal operations, such as after the system power supply is restored. *See* Ex. 1027 at 25 (Section 3.7.3) ("The following [Control and Status Registers] should be stored in non-volatile memory before entering S3 mode and restored before normal DRAM transactions begin.").

443. Accordingly, the prior art references in each of Grounds 2 and 3 satisfies the "*wherein, in response to the trigger signal, the logic element writes information into the non-volatile memory*" limitation.

12. Claim 12 is Unpatentable

444. Claim 12 is unpatentable as the prior art references in each of Grounds 2 and 3 (Voltage Mappings A, B, C, and D) render the claim obvious.

a) [12.a] Preamble

445. The preamble of claim 12 requires "*[t]he memory module of claim 5, the plurality of components further comprising*."

446. The prior art references in Grounds 2 and 3 each teaches this limitation to a Skilled Artisan.

447. As explained above for claim 5, the prior art references in each of Grounds 2 and 3 satisfy the limitations of claim 5. *Supra* ¶¶359-376.

448. Accordingly, the prior art references in each of Grounds 2 and 3 satisfies "*[t]he memory module of claim 5, the plurality of components further comprising*."

b) [12.b] A Non-Volatile Memory

449. Claim 12 requires "*a non-volatile memory*."

450. The prior art references in Grounds 2 and 3 each teaches this limitation to a Skilled Artisan.

451. The combination of Harris (in Grounds 2 and 3) with Amidi discloses a "*non-volatile memory*" for the reasons discussed above with reference to claims 10 and 11. *Supra* ¶¶432-438 (claim limitation [10.b]), ¶¶439-443 (claim 11).

452. Accordingly, the prior art references in each of Grounds 2 and 3 satisfies "*a non-volatile memory*."

c) [12.c] A Controller

453. Claim 12 requires "*a controller configured to receive the trigger signal, wherein, in response to the trigger signal, the controller performs a write operation to the non-volatile memory*."

454. To the extent Netlist asserts that the limitation of "*a write operation to the non-volatile memory*" is satisfied by writing configuration information into a non-volatile memory, the prior art references in Grounds 2 and 3 each teaches this limitation to a Skilled Artisan. In particular, the combination of Harris with Amidi (in Grounds 2 and 3) discloses "*a controller configured to receive the trigger signal, wherein, in response to the trigger signal, the controller performs a write operation to the non-volatile memory*" for the reasons discussed above with reference to claim 10. *Supra* ¶¶432-438 (claim limitation [10.b]). For example, the buffer 112 in Harris includes "*a controller*" that receives the trigger signal from Amidi's Voltage Supervisory Block and in response, performs a write operation to the non-volatile memory to store configuration data before entering S3 sleep mode. *See* Ex. 1027 at 25 (Section 3.7.3) ("The following [Control and Status Registers] should be stored in non-volatile memory before entering S3 mode and restored before normal DRAM transactions begin."); *see also id.* at 95 (Table 11.7) (showing DAREFTC, MTR, DSREFTC, DRC registers), 96 (Table 11.8) (showing S3RESTORE registers), 141 ("Section 11.6.1.3 S3RESTORE[15:0] : DDR State Restore"); *supra* ¶¶363-376 (discussing the voltage supervisory block in the combination).

455. Therefore, under the interpretation that the claimed write operation is satisfied by writing configuration information, the prior art references in each of

Grounds 2 and 3 satisfies "*a controller configured to receive the trigger signal, wherein, in response to the trigger signal, the controller performs a write operation to the non-volatile memory*."

456. To the extent the limitation of "*a write operation to the non-volatile memory*" requires writing user data from volatile memory to non-volatile memory, such an interpretation would have been also obvious to a Skilled Artisan for the reasons discussed with reference to Grounds 4-5.

13. Claim 13 is Unpatentable

457. Claim 13 is unpatentable as the prior art references in each of Grounds 2 and 3 (Voltage Mappings A, B, C, and D) render the claim obvious.

458. Claim 13 requires "*[t]he memory module of claim 5, wherein the power input voltage is coupled to the first, second, and third buck converters and the converter circuit*."

459. The prior art references in Grounds 2 and 3 each teaches this limitation to a Skilled Artisan.

460. For the reasons discussed above with reference to claim limitations [1.c] ("*a first buck converter . . .*"), [1.d] ("*a second buck converter . . .*"), [1.e] ("*a third buck converter . . .*"), [1.f] ("*a converter circuit . . .*"), and specifically for the combination of Harris (in Grounds 2 and 3) and Amidi with reference to claim limitation [5.b] ("*voltage monitor circuit . . .*"), the external voltage source, as

disclosed in Harris and shown below, is coupled via Amidi's Power management block to the voltage regulator module 102, which includes the "*first*," "*second*," and "*third buck converter[s]*" and the "*converter circuit*," when the voltage amplitude of the external voltage source is in a normal operating range.

Ground 2: Ground 1 and Battery Backup of Amidi

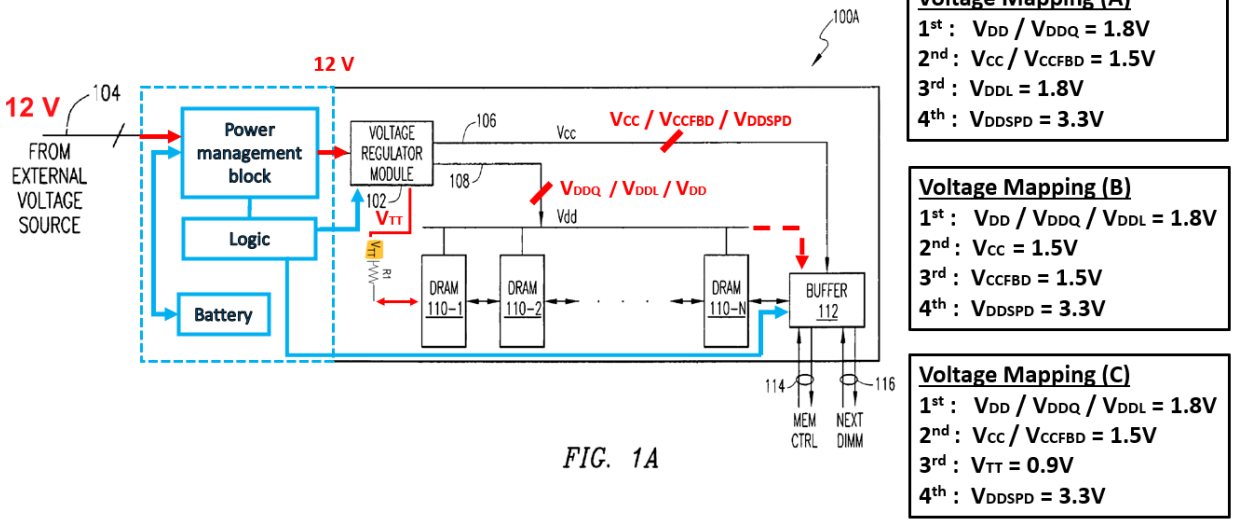


FIG. 1A

Ground 2: Ground 1 and Battery Backup of Amidi

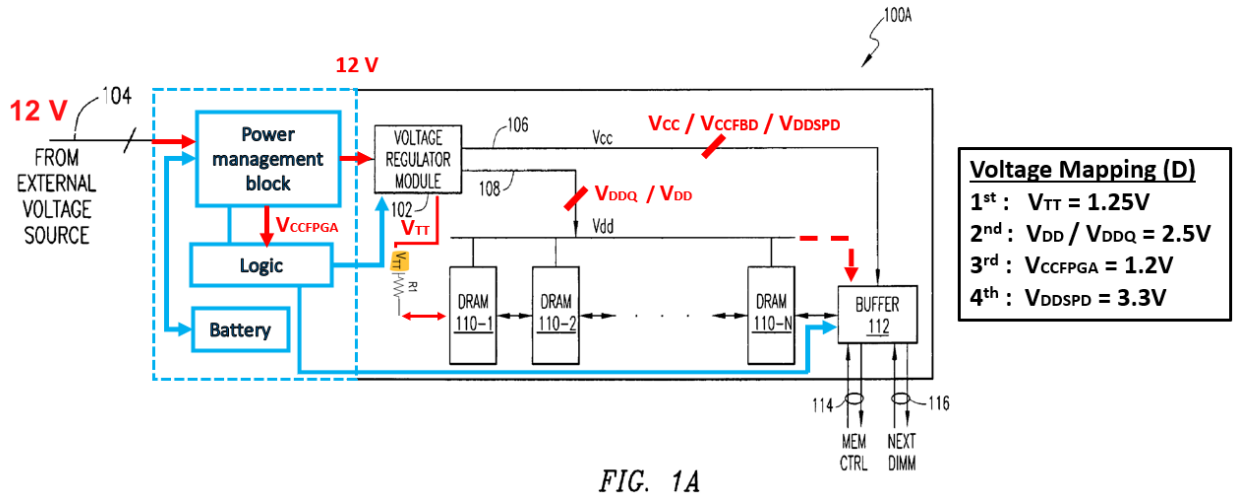


FIG. 1A

Ex. 1023 at Fig. 1A (annotated with teachings of Amidi); *see also* Ex. 1024 at Figs. 5, 6.

461. Accordingly, the prior art references in each of Grounds 1 through 3 satisfies the "*wherein the power input voltage is coupled to the first, second, and third buck converters and the converter circuit*" limitation.

14. Claim 14 is Unpatentable

462. Claim 14 is unpatentable as the prior art references in each of Grounds 1 through 3 render the claim obvious.

463. Claim 14 requires "*[t]he memory module of claim 8, wherein, in response to selectively switching on the one of the first, second, third and fourth regulated voltages to the one or more registers, the one or more registers is configured to output the registered first plurality of address and control signals to the plurality of SDRAM devices*."

464. The prior art references in Grounds 1 through 3 each teaches this limitation to a Skilled Artisan.

465. For the reasons discussed above with reference to claim 8, a Skilled Artisan would have been motivated to implement the buffer 112 in Harris according to a Skilled Artisan's knowledge, which includes the FBDIMM Standards, and use the S3 sleep mode to save power with or without the system power supply so that the supply of VCC and VCCFBD are selectively switched off while the supply of VDD remains switched on to allow the memory devices to refresh their data. *Supra* ¶¶410-420. When the S3 sleep mode ends and "normal

DRAM transactions begin" again, Ex. 1027 at 25, the supply of the VCC and VCCFBD voltages are switched back on so that the buffer 112 can receive address and command signals from the host and output corresponding signals to the DRAM devices in order to control them according to those address and command signals. *See, e.g., supra* at ¶315; *see also* Ex. 1024 (Amidi) at Fig. 15 (returning control to the host after power failure). Therefore, a Skilled Artisan would have understood that, when the S3 sleep mode ends, the voltages to the registers in the AMB are selectively switched on so that "*the one or more registers is configured to output the registered first plurality of address and control signals to the plurality of SDRAM devices.*"

466. Accordingly, the prior art references in each of Grounds 1 through 3 satisfies the "*wherein, in response to selectively switching on the one of the first, second, third and fourth regulated voltages to the one or more registers, the one or more registers is configured to output the registered first plurality of address and control signals to the plurality of SDRAM devices*" limitation.

15. Claim 15 is Unpatentable

467. Claim 15 is unpatentable as the prior art references in each of Ground 1 (Voltage Mappings A, B, and C) and Grounds 2 and 3 (Voltage Mappings A, B, C, and D) render the claim obvious.

a) [15.a] Preamble

468. The preamble of Claim 15 requires "*[t]he memory module of claim 1, the plurality of components further comprising*."

469. The prior art references in each of Grounds 1 through 3 teach this limitation to a Skilled Artisan.

470. As explained above for claim 1, the prior art references in each of Grounds 1 through 3 satisfy the limitations of claim 1. *Supra* ¶¶215-327.

471. Accordingly, the prior art references in each of Grounds 1 through 3 satisfies "*[t]he memory module of claim 1, the plurality of components further comprising*."

b) [15.b] A Logic Element

472. Claim 15 requires "*a logic element including one or more integrated circuits and discrete electrical elements, the one or more integrated circuit including an internal non-volatile memory, wherein the non-volatile memory is configured to store configuration information*."

473. The prior art references in each of Grounds 1 through 3 teach this limitation to a Skilled Artisan.

474. For the reasons discussed above with reference to claim 10, a Skilled Artisan would have understood the prior art to teach and disclose a "*logic element including one or more integrated circuits*" in which "*the one or more integrated*

circuit includ[es] an internal non-volatile memory, wherein the non-volatile memory is configured to store configuration information." *Supra* ¶¶432-438 (claim limitation [10.b]); *see also* Ex. 1027 (JESD82-20) at 25 (Section 3.7.3) ("The following [Control and Status Registers] should be stored in non-volatile memory before entering S3 mode and restored before normal DRAM transactions begin."); *see also id.* at 95 (Table 11.7) (showing DAREFTC, MTR, DSREFTC, DRC registers), 96 (Table 11.8) (showing S3RESTORE registers), 141 ("Section 11.6.1.3 S3RESTORE[15:0] : DDR State Restore"); Ex. 1028 (JESD205) at 13-16, 30, 32; Ex. 1066 at 26:64-27:4. For example, the "*logic element*" includes logic in the buffer 112 of Harris related to S3 sleep mode and non-volatile memory, which is either internal or external to the logic in the buffer 112, ("*an internal non-volatile memory*") for storing configuration information in S3 Recovery Configuration Registers as required by the S3 sleep mode ("*wherein the non-volatile memory is configured to store configuration information*"). *See id.* A Skilled Artisan would have understood this "*logic element*" to include "*one or more integrated circuits,*" such as an integrated circuit, like an SPD, including the non-volatile memory, and an integrated circuit within the buffer 112. *See id.* For example, Harris illustrates the buffer 112 to a Skilled Artisan as a chip with integrated circuits in Figure 3.

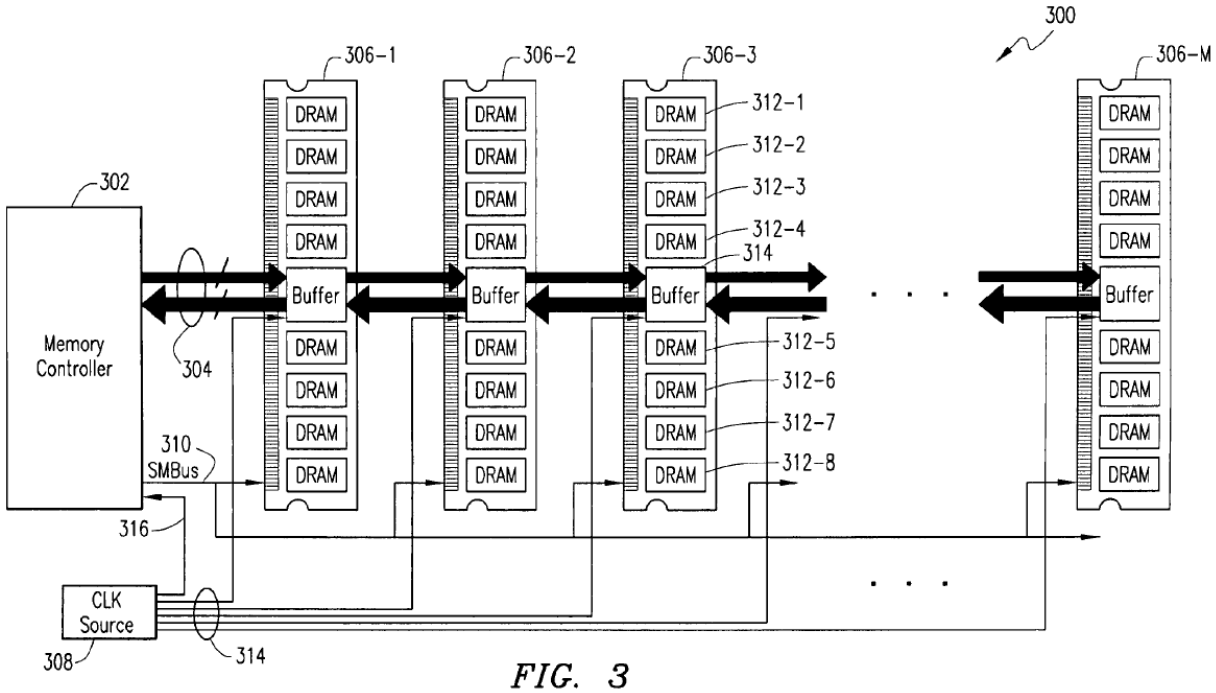
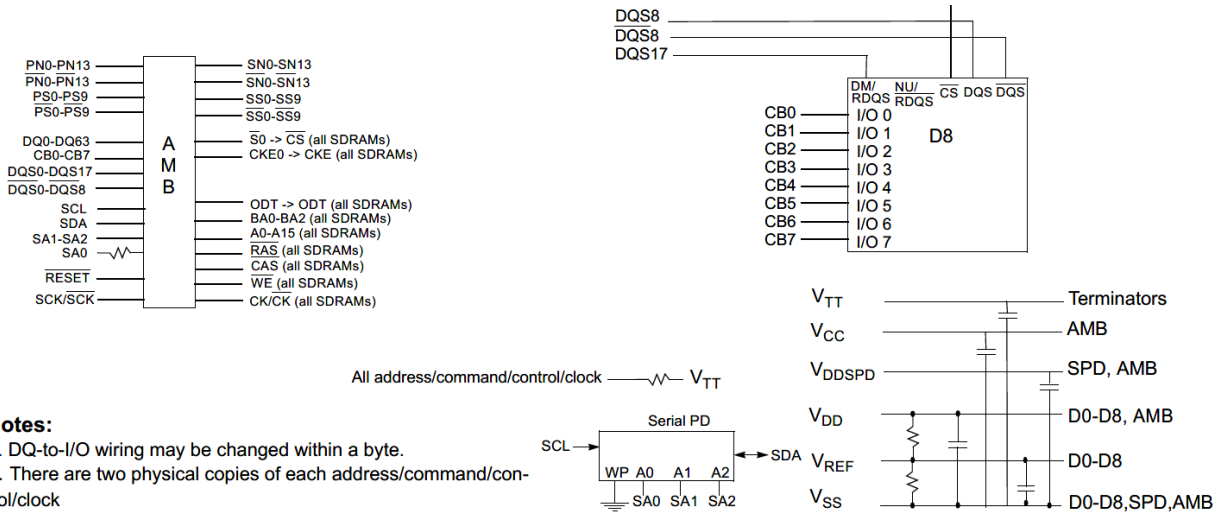


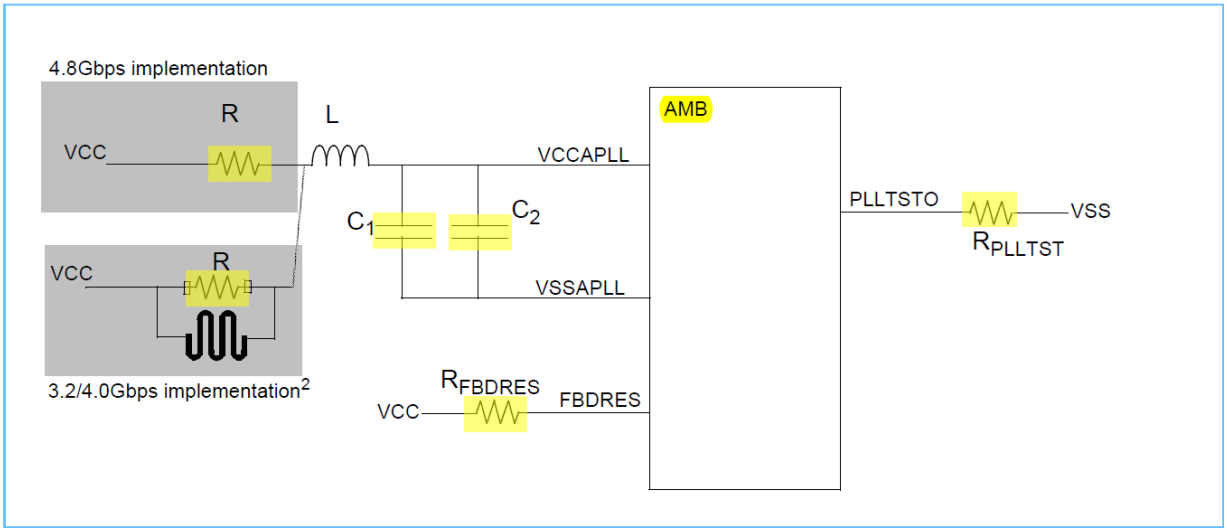
FIG. 3

Ex. 1023 at Fig. 3. Furthermore, a Skilled Artisan would have understood that a non-volatile memory can be implemented in an SPD device that is separate from an integrated circuit implementing an AMB (and including the logic to store the configuration information in the non-volatile memory. *See*, *e.g.*, Ex. 1028 (JESD205) at 13 (reproduced below in part, showing integrated circuits for AMB and SPD and their interconnections); *see also id*. at 38 (showing an exemplary arrangement for the integrated circuits).



475. A Skilled Artisan would have also understood that the "*logic element*" in Harris includes "*discrete electrical elements*." For example, Harris discloses multiple interfaces on the Buffer, such as the bidirectional memory controller interfaces (114, 116). *See e.g.*, Ex. 1023 at Fig. 1A, [0009]. These interfaces would include resistors and capacitors according to the FBDIMM Standards:

PLL and Channel Bias



NOTE 1: There is no connection to ground from VSSAPLL.
NOTE 2: Users must ensure AMB requirements are met by their implementation. Example, in VCCAPLL network, R implemented as copper trace serpentine may not achieve acceptable tolerances for all AMBs.
NOTE 3: VCC power delivery requirements (as specified for VCC balls) are assumed to be met at inputs of VCCAPLL and FBDRES networks, not at VCCAPLL and FBDRES balls.

Ex. 1028 at 43; *see id.* at 42-45 (describing "Common AMB Bias Detail," including "*one or more integrated circuits and discrete electrical elements*"). Similarly, the voltages to and from the "*logic element*" must be terminated, conditioned, and set as required to operate properly, and JESD205 (part of the FBDIMM Standards) discloses that the voltages to the AMB Buffer and/or SPD (e.g., VTT, VCC, VDDSPD, VDD) are terminated, conditioned, and set using resistors and/or capacitors. *See, e.g.*, Ex. 1028 at 13 (bottom right figure).

476. Accordingly, the prior art references in each of Grounds 1 through 3 satisfies "*a logic element including one or more integrated circuits and discrete electrical elements, the one or more integrated circuit including an internal non-*

volatile memory, wherein the non-volatile memory is configured to store configuration information."

16. Claim 16 is Unpatentable

477. Claim 16 is unpatentable as the prior art references in each of Grounds 2 and 3 (Voltage Mappings A, B, C, and D) render the claim obvious.

a) [16.a] Preamble

478. The preamble of claim 16 requires "*[a] memory module comprising*."

479. As shown in the table below, the preamble of Claim 16 is identical to the preamble Claim 1:

Claim 1	**Claim 16**
[1.a] A memory module comprising:	[16.a] A memory module comprising:

480. As discussed above with reference to claim limitation [1.a], to the extent the preamble of claim 1 is limiting, Harris satisfies "[a] memory module." *Supra* ¶¶216-222.

b) [16.b] Printed Circuit Board

481. Claim 16 requires "*a printed circuit board (PCB) having an interface configured to fit into a corresponding slot connector of a host system, the interface including a plurality of edge connections configured to couple power, data, address and control signals between the memory module and the host system*."

482. As shown in the table below, claim limitation [16.b] is identical to claim limitation [1.b]:

Claim 1	Claim 16
[1.b] a printed circuit board (PCB) having an interface configured to fit into a corresponding slot connector of a host system, the interface including a plurality of edge connections configured to couple power, data, address and control signals between the memory module and the host system;	[16.b] a printed circuit board (PCB) having an interface configured to fit into a corresponding slot connector of a host system, the interface including a plurality of edge connections configured to couple power, data, address and control signals between the memory module and the host system;

483. As discussed above with reference to claim limitation [1.b], Harris alone, or in combination with the FBDIMM Standards, satisfies this limitation. *Supra* ¶¶223-231.

c) [16.c] First, Second, and Third Buck Converters

484. Claim 16 requires "*first, second, and third buck converters configured to receive a pre-regulated input voltage and to produce first, second and third regulated voltages, respectively*."

485. As shown in the table below, claim limitation [16.c] is very similar to claim limitations [1.c] – [1.e]:

Claim 1	Claim 16
[1.c] a first buck converter configured to provide a first regulated voltage having a first voltage amplitude; [1.d] a second buck converter configured to provide a second regulated voltage having a second voltage amplitude; [1.e] a third buck converter configured to provide a third regulated voltage having a third voltage amplitude;	[16.c] first, second, and third buck converters configured to receive a pre-regulated input voltage and to produce first, second and third regulated voltages, respectively;

486. For the reasons discussed above with reference to claim limitations [1.c] – [1.e], Harris alone, or the combinations of Grounds 1 through 3, satisfies this limitation. *See supra* ¶¶232-280.

487. To the extent the "*pre-regulated input voltage*" can be satisfied by the "*input voltage*" of [16.f] being within pre-determined limits, as suggested by Netlist, *see* Ex. 1071 at 43 (pointing to input voltage received from "Power edge connections"); Ex. 1073 at 49-50 (similar), Harris discloses that, in an embodiment, the external supply voltage is 12 volts +/-15 percent. *See* Ex. 1023 at [0013] ("Further, since the +12V power supply is not used directly by DRAM devices or buffer/logic components of the memory assembly, a wide tolerance (e.g., around +/−15%) can be accommodated, allowing low cost power distribution for system boards (such as, e.g., motherboards, cell boards, et cetera) wherein

design requirements for bypass/hold-up capacitors may be relaxed or minimized."). Harris also expressly discloses that the external supply voltage can be regulated and used as a source for local supply voltages. *See id.* at [0014] ("It should be readily recognized that the external voltage sources may comprise any combination of known or heretofore unknown voltage supplies, either regulated or unregulated, and even including variable voltages.").

488. Moreover, a Skilled Artisan would have been motivated to select a tighter tolerance for the external supply voltage than 15 percent. For example, a Skilled Artisan would have recognized that the DDR2 SDRAM specification discloses a tolerance of 5 percent. Ex. 1026 at pp.6-7. As another example, Amidi discloses an example with a tolerance of 10 percent. Ex. 1024 at 8:23-36, Fig. 14. And, as explained above, a Skilled Artisan would have understood that the choice of around a 10 percent tolerance provided a reasonable compromise between the risks associated with too high a tolerance and too low a tolerance. *Supra* ¶390; *see also* Ex. 1063 at 1-2; Ex. 1027 at 32.

489. To the extent the "*pre-regulated input voltage*" requires a voltage be "pre-regulated" on the memory board itself, *see* Ex. 1001 at 28:53-58, or one argues that a voltage within a fixed percentage of a typical value is not "pre-regulated," Grounds 2 and 3 each discloses that Amidi's lithium ion battery voltage (e.g., around 3.6 to 4.2 volts) is converted (and thus pre-regulated) with a boost

converter to 12 volts, as shown in the annotated figures below. *See* Ex. 1032 (Mohan) at 161-162 (describing switch-mode converters as being used in "regulated switch-mode dc power supplies" where "the average dc output voltage must be controlled to equal a desired level").

Ground 2: Ground 1 and Battery Backup of Amidi

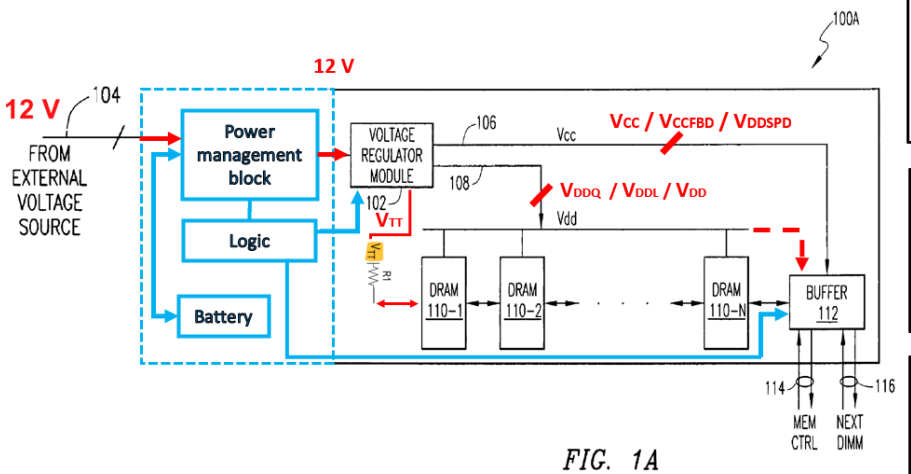


FIG. 1A

Voltage Mapping (A)
1st : VDD / VDDQ = 1.8V
2nd : VCC / VCCFBD = 1.5V
3rd : VDDL = 1.8V
4th : VDDSPD = 3.3V

Voltage Mapping (B)
1st : VDD / VDDQ / VDDL = 1.8V
2nd : VCC = 1.5V
3rd : VCCFBD = 1.5V
4th : VDDSPD = 3.3V

Voltage Mapping (C)
1st : VDD / VDDQ / VDDL = 1.8V
2nd : VCC / VCCFBD = 1.5V
3rd : VTT = 0.9V
4th : VDDSPD = 3.3V

Ground 2: Ground 1 and Battery Backup of Amidi

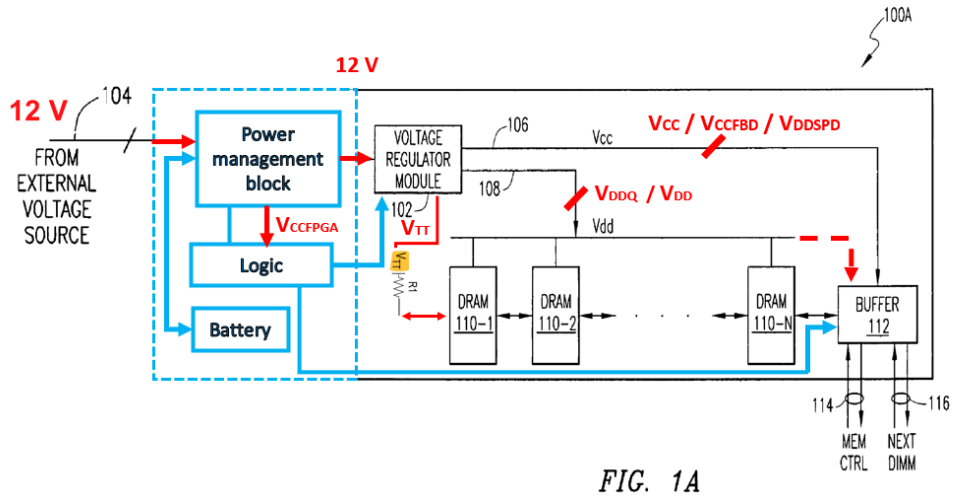


FIG. 1A

Voltage Mapping (D)
1st : VTT = 1.25V
2nd : VDD / VDDQ = 2.5V
3rd : VCCFPGA = 1.2V
4th : VDDSPD = 3.3V

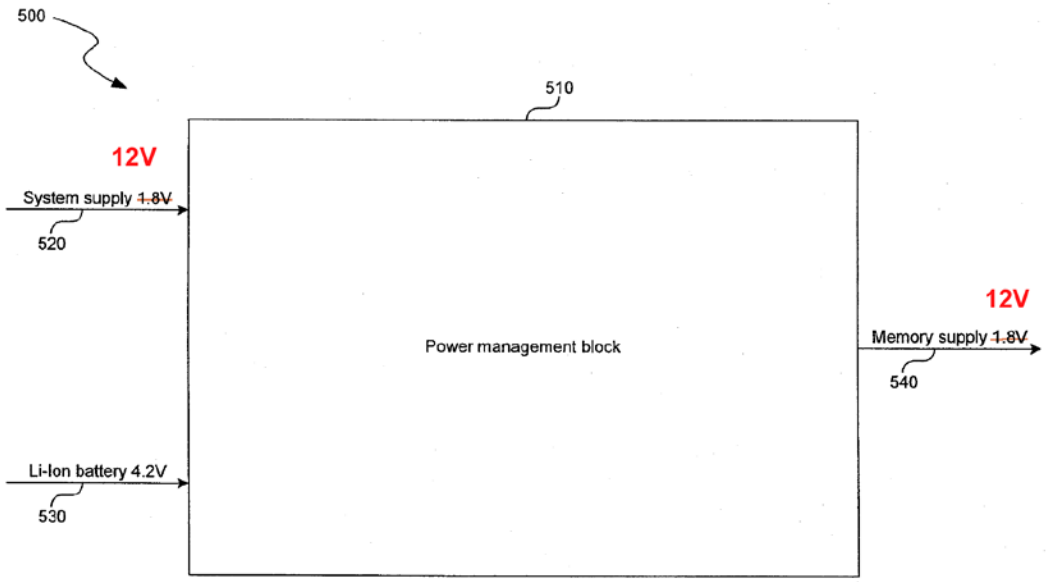


FIG. 5

Ex. 1023 at Fig. 1A (annotated with teachings of Amidi and knowledge of a Skilled Artisan); Ex. 1024 at Fig. 5 (annotated with teachings of Harris); *see also* Ex. 1024 at Fig. 6 (showing a lithium ion battery at 3.6 volts that requires DC/DC voltage conversion to be charged and used). Furthermore, a Skilled Artisan would have been motivated to include a power regulator in Amidi's Power management block to pre-regulate the input voltage of Harris's voltage regulator module if the external power source provides—or there is a chance it may provide—an unregulated voltage, to ensure that the input of Harris's voltage regulator module remains within a tolerated interval around 12V. Ex. 1023 at [0013] ("tolerance (e.g., around +/−15%) can be accommodated"), [0014] ("It should be readily recognized that the external voltage sources may comprise any combination of known or heretofore unknown voltage supplies, either regulated or unregulated,

and even including variable voltages."). A Skilled Artisan would have also understood that such an additional voltage regulator in Amidi's power management block can be used to convert an external supply voltage other than 12V into 12V, thus allowing Harris's module to be adapted to a system which provides an external supply voltage other than 12V without altering other parts of the module. Ex. 1023 (Harris) at [0020] ("voltage-independent embodiments disclosed herein can provide upgradeability and extensibility without changing system board power distribution").

490. Accordingly, the prior art references in each of Grounds 2 and 3 further satisfies this limitation, to the extent the "*pre-regulated input voltage*" requires the voltage be "pre-regulated" on the memory board itself or one argues that a voltage within a fixed percentage of a typical value is not "pre-regulated."

d) [16.d] A Converter Circuit

(1) [16.d.1] Configured to provide a fourth regulated voltage

491. Claim 16 requires "*a converter circuit configured to reduce the pre-regulated input voltage to provide a fourth regulated voltage*."

492. As shown in the table below, claim limitation [16.d.1] is very similar to claim limitation [1.f]:

Claim 1	Claim 16
[1.f] a converter circuit configured to provide a fourth regulated voltage having a fourth voltage amplitude; and	[16.d.1] a converter circuit configured to reduce the pre-regulated input voltage to provide a fourth regulated voltage,

493. As discussed above with reference to claim limitations [1.f] and [16.c], Harris alone, in combination with Amidi, or in further combination with the FBDIMM Standards, satisfies this limitation. *Supra* ¶¶281-287 (claim limitation [1.f]), ¶¶484-490 (claim limitation [16.c]) ("*first, second, and third buck converters configured to receive a pre-regulated input voltage…*").

(2) [16.d.2] Wherein the regulated voltages each have respective amplitudes

494. Claim 16 requires "*wherein the first, second, third and fourth regulated voltages have first, second, third, and fourth voltage amplitudes, respectively*."

495. As shown in the table below, claim limitation [16.d.2] is very similar to claim limitations [1.c] – [1.f]:

Claim 1	**Claim 16**
[1.c] a first buck converter configured to provide a first regulated voltage having a first voltage amplitude; [1.d] a second buck converter configured to provide a second regulated voltage having a second voltage amplitude; [1.e] a third buck converter configured to provide a third regulated voltage having a third voltage amplitude; [1.f] a converter circuit configured to provide a fourth regulated voltage having a fourth voltage amplitude; and	[16.d.2] wherein the first, second, third and fourth regulated voltages have first, second, third, and fourth voltage amplitudes, respectively;

496. As discussed above with reference to claim limitations [1.c] – [1.f], Harris alone, or the combinations of Grounds 1 through 3, satisfies this limitation. *Supra* ¶¶ 232-287.

e) [16.e] A Plurality Of Components Coupled To The PCB

497. Claim 16 requires "*a plurality of components coupled to the PCB, the plurality of components including a plurality of synchronous dynamic random access memory (SDRAM) devices, each component of the plurality of components coupled to one or more regulated voltages of the first, second, third and fourth regulated voltages*."

498. As shown in the table below, claim limitation [16.e] is very similar to claim limitations [1.g] – [1.h]:

Claim 1	**Claim 16**
[1.g] a plurality of components coupled to the PCB, each component of the plurality of components coupled to one or more regulated voltages of the first, second, third and fourth regulated voltages, the plurality of components comprising: [1.h] a plurality of synchronous dynamic random access memory (SDRAM) devices coupled to the first regulated voltage, and	[16.e] a plurality of components coupled to the PCB, the plurality of components including a plurality of synchronous dynamic random access memory (SDRAM) devices, each component of the plurality of components coupled to one or more regulated voltages of the first, second, third and fourth regulated voltages; and

499. As discussed above with reference to claim limitations [1.g] – [1.h], Harris alone, or the combinations of Grounds 1 through 3, satisfies this limitation. *Supra* ¶¶ 288-303.

f) [16.f] A Voltage Monitor Circuit

500. Claim 16 requires "*a voltage monitor circuit configured to monitor an input voltage received via a first portion of the plurality of edge connections, the voltage monitor circuit configured to produce a signal in response to the input voltage having a voltage amplitude that is greater than a first threshold voltage*."

501. As shown in the table below, claim limitation [16.f] is very similar to claim limitations [5.a] – [5.b]:

Claim 5	**Claim 16**
[5.a] The memory module of claim 1, further comprising: [5.b] a voltage monitor circuit configured to monitor a power input voltage received via a second portion of the plurality of edge connections, the voltage monitor circuit configured to produce a trigger signal in response to the power input voltage having a voltage amplitude that is greater than a first threshold voltage.	[16.f] a voltage monitor circuit configured to monitor an input voltage received via a first portion of the plurality of edge connections, the voltage monitor circuit configured to produce a signal in response to the input voltage having a voltage amplitude that is greater than a first threshold voltage.

502. In particular, the "*power input voltage received via a second portion of the plurality of edge connections*" in claim [5.b] corresponds to the "*input voltage received via a first portion of the plurality of edge connections*" in claim 16. As discussed above with reference to claim limitations [5.a] – [5.b], Harris (in Ground 2) in view of Amidi discloses this limitation. *Supra* ¶¶360-376.

503. As also discussed, to the extent one were to argue that overvoltage protection was not obvious in light of Ground 2, it would have been obvious in light of Hajeck, as part of Ground 3. *Supra* ¶¶375-376.

17. Claim 17 is Unpatentable

504. Claim 17 is unpatentable as the prior art references in each of Grounds 2 and 3 (Voltage Mappings A, B, C, and D) render the claim obvious.

505. Claim 17 requires "*[t]he memory module of claim 16, wherein the second and third buck converters are configured to operate as a dual buck converter*."

506. As shown in the table below, claim 17 is very similar to claim 2:

Claim 2	**Claim 17**
[2] The memory module of claim 1, wherein the first and third buck converters are further configured to operate as a dual buck converter.	[17] The memory module of claim 16, wherein the second and third buck converters are configured to operate as a dual buck converter.

507. In particular, both claims 2 and 17 recite two buck converters that "*are configured to operate as a dual buck converter*." Claim 2 recites the "*first and third buck converters*" and claim 17 recites "*the second and third buck converters*."

508. For the reasons discussed above with reference to claim 2, it would have been obvious to implement the two buck converters as a dual buck converter. *See supra* ¶¶328-347.

509. For Ground 2 (Ground 1 in view of Amidi) and Ground 3 (Ground 2 in view of Hajeck), there are four mappings for the "*regulated voltage[s]*," as shown in the figures below.

Ground 2: Ground 1 and Battery Backup of Amidi

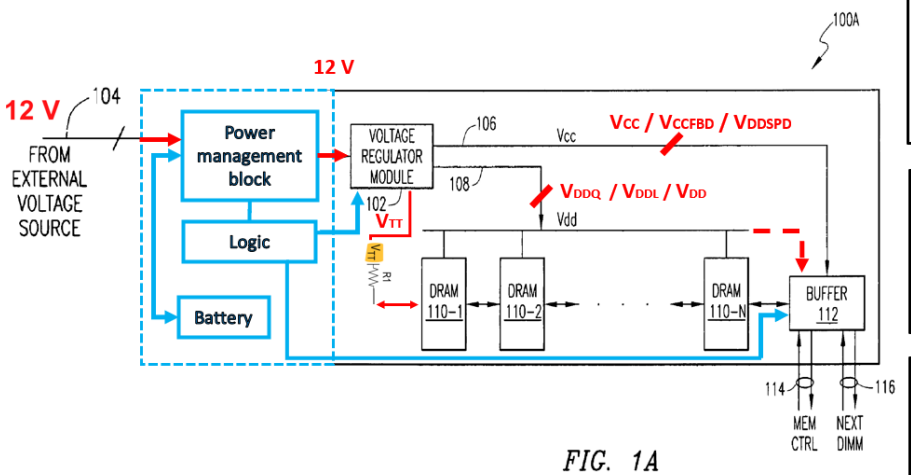


FIG. 1A

Voltage Mapping (A)
1st : VDD / VDDQ = 1.8V
2nd : VCC / VCCFBD = 1.5V
3rd : VDDL = 1.8V
4th : VDDSPD = 3.3V

Voltage Mapping (B)
1st : VDD / VDDQ / VDDL = 1.8V
2nd : VCC = 1.5V
3rd : VCCFBD = 1.5V
4th : VDDSPD = 3.3V

Voltage Mapping (C)
1st : VDD / VDDQ / VDDL = 1.8V
2nd : VCC / VCCFBD = 1.5V
3rd : VTT = 0.9V
4th : VDDSPD = 3.3V

Ground 2: Ground 1 and Battery Backup of Amidi

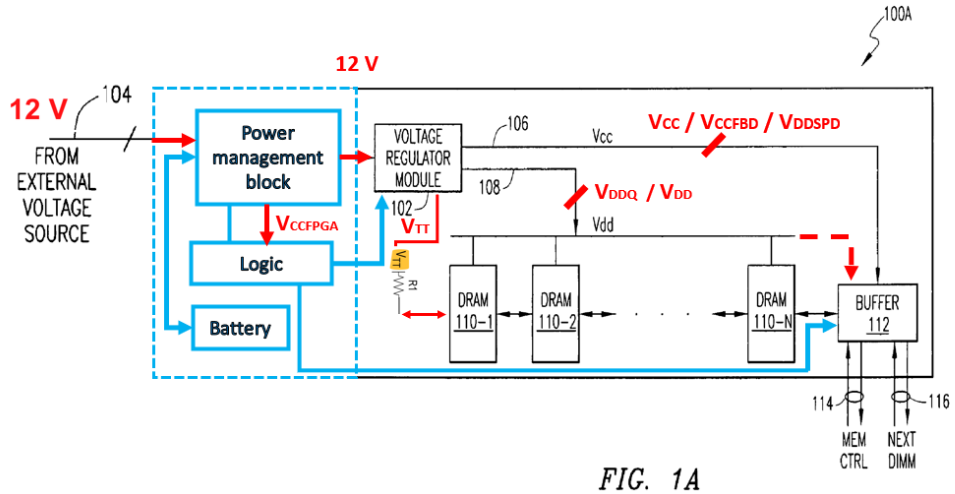


FIG. 1A

Voltage Mapping (D)
1st : VTT = 1.25V
2nd : VDD / VDDQ = 2.5V
3rd : VCCFPGA = 1.2V
4th : VDDSPD = 3.3V

In each of the voltage mappings above, a Skilled Artisan would have been motivated with a reasonable expectation of success to use a "*dual buck converter*" to provide the "*second regulated voltage*" and "*third regulated voltage*" for the same reasons discussed above for claim 2 with respect to the "*first*" and "*third*" voltages in Ground 1, including because dual buck converters were commercially available and simplified the design by reducing the number of parts, and the phases

of the two voltages could be adjusted relative to each other, thus reducing any input "ripple" and improving performance. *See supra* ¶¶328-331, 338-347.

510. Accordingly, the prior art references in each of Grounds 2 and 3 satisfies the "*second and third buck converters are configured to operate as a dual buck converter*" limitation.

18. Claim 18 is Unpatentable

511. Claim 18 is unpatentable as the prior art references in each of Grounds 2 and 3 (Voltage Mappings A, B, C, and D) render the claim obvious.

a) [18.a] Preamble

512. The preamble of claim 18 requires "*[t]he memory module of claim 16, the plurality of components further including*."

513. The prior art references in Grounds 2 and 3 each teaches this limitation to a Skilled Artisan.

514. As discussed above with reference to claim 16, Harris, alone or in the combinations of Grounds 2 and 3 satisfies "*[t]he memory module of claim 16, the plurality of components further including*." *Supra* ¶¶478-503 (claim 16).

b) [18.b] A Controller

515. Claim 18 requires "*a controller coupled to the voltage monitor circuit and configured to receive the signal, wherein the controller executes a write operation in response to the signal*."

516. To the extent Netlist asserts that the limitation of "*the controller executes a write operation in response to the signal*" is satisfied by writing configuration information into a non-volatile memory, the prior art references in Grounds 2 and 3 each teaches this limitation to a Skilled Artisan.

517. As shown in the table below, claim limitation [18.b] is very similar to claim limitation [12.c]:

Claim 12	**Claim 18**
[12.c] a controller configured to receive the trigger signal, wherein, in response to the trigger signal, the controller performs a write operation to the non-volatile memory.	[18.b] a controller coupled to the voltage monitor circuit and configured to receive the signal, wherein the controller executes a write operation in response to the signal.

518. As discussed above with reference to claim limitation [12.c], the prior art references in each of Grounds 2 and 3 satisfies this limitation. *Supra* ¶¶ 453-456.

19. Claim 19 is Unpatentable

519. Claim 19 is unpatentable as the prior art references in each of Grounds 2 and 3 (Voltage Mappings A, B, C, and D) render the claim obvious.

520. Claim 19 requires "*[t]he memory module of claim 18, wherein the write operation includes writing data information into non-volatile memory*."

521. To the extent Netlist asserts that the limitation of "*the write operation includes writing data information into non-volatile memory*" is satisfied by writing

configuration information into a non-volatile memory, the prior art references in Grounds 2 and 3 each teaches this limitation to a Skilled Artisan.

522. As shown in the table below, claim 19 is very similar to claim limitation [12.c]:

Claim 12	**Claim 19**
[12.c] a controller configured to receive the trigger signal, wherein, in response to the trigger signal, the controller performs a write operation to the non-volatile memory.	[19] The memory module of claim 18, wherein the write operation includes writing data information into non-volatile memory.

523. As discussed above with reference to claim limitation [12.c], the prior art references in each of Grounds 2 and 3 satisfies this limitation. *Supra* ¶¶ 453-455.

20. Claim 20 is Unpatentable

524. Claim 20 is unpatentable as the prior art references in Grounds 2 and 3 (Voltage Mappings A, B, and C) render the claim obvious.

525. Claim 20 requires "*[t]he memory module of claim 16, wherein the plurality of SDRAM devices are configured to receive at least one of the first, second, third and fourth regulated voltages having a voltage amplitude of 1.8 volts*."

526. The prior art references in Grounds 2A-2C (Ground 1 in view of Amidi) and Grounds 3A-3C (Ground 2 in view of Hajeck) each teaches this limitation to a Skilled Artisan.

527. As shown in the table below, claim 20 is very similar to claim limitation [1.h] and claim 3:

Claims 1 and 3	**Claim 20**
[1.h] a plurality of synchronous dynamic random access memory (SDRAM) devices coupled to the first regulated voltage [3] The memory module of claim 1, wherein the first voltage amplitude is 1.8 volts.	[20] The memory module of claim 16, wherein the plurality of SDRAM devices are configured to receive at least one of the first, second, third and fourth regulated voltages having a voltage amplitude of 1.8 volts.

528. As discussed above with reference to claim limitation [1.h] and claim 3, the prior art references in each of Grounds 2A-2C and 3A-3C satisfies this limitation. *Supra* ¶¶298-303 (claim limitation [1.h]), ¶¶ 348-353 (claim 3).

Ground 2: Ground 1 and Battery Backup of Amidi

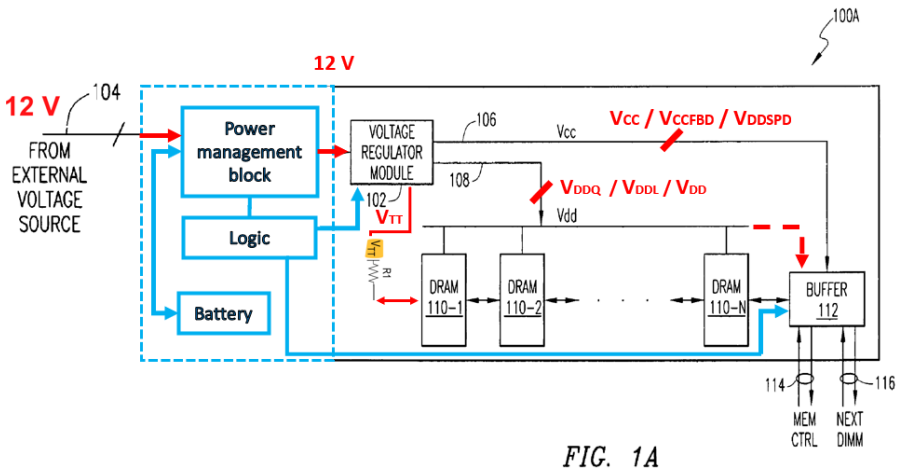


FIG. 1A

Voltage Mapping (A)
1st : VDD / VDDQ = 1.8V
2nd : VCC / VCCFBD = 1.5V
3rd : VDDL = 1.8V
4th : VDDSPD = 3.3V

Voltage Mapping (B)
1st : VDD / VDDQ / VDDL = 1.8V
2nd : VCC = 1.5V
3rd : VCCFBD = 1.5V
4th : VDDSPD = 3.3V

Voltage Mapping (C)
1st : VDD / VDDQ / VDDL = 1.8V
2nd : VCC / VCCFBD = 1.5V
3rd : VTT = 0.9V
4th : VDDSPD = 3.3V

21. Claim 21 is Unpatentable

529. Claim 21 is unpatentable as the prior art references in each of Grounds 2 and 3 (Voltage Mappings A, B, C, and D) render the claim obvious.

a) [21.a] Preamble

530. The preamble of claim 21 requires that "*[t]he memory module of claim 16, the plurality of components further including*."

531. The prior art references in Grounds 2 and 3 each teaches this limitation to a Skilled Artisan.

532. As discussed above with reference to claim 16, the prior art references in each of Grounds 2 and 3 satisfies "*[t]he memory module of claim 16, the plurality of components further including*." *Supra* ¶¶478-503 (claim 16).

b) [21.b] At Least One Circuit

(1) [21.b.1] Coupled between the interface and SDRAM devices

533. Claim 21 requires "*at least one circuit coupled between the interface and the plurality of SDRAM devices*."

534. The prior art references in Grounds 2 and 3 each teaches this limitation to a Skilled Artisan.

535. As shown in the table below, claim limitation [21.b.1] is very similar to claim limitation [1.i.1]:

Claim 1	Claim 21
[1.i.1] at least one circuit coupled between a first portion of the plurality of edge connections and the plurality of SDRAM devices,	[21.b.1] at least one circuit coupled between the interface and the plurality of SDRAM devices,

536. As discussed above with reference to claim limitation [1.i.1], the prior art references in each of Grounds 2 and 3 satisfies this limitation. *Supra* ¶¶ 304-310.

(2) [21.b.2] Operable to receive/output address and control signals

537. Claim 21 requires "*the at least one circuit operable to receive a first plurality of address and control signals via a second portion of the plurality of edge connections and to output a second plurality of address and control signals to the plurality of SDRAM devices*."

538. The prior art references in Grounds 2 and 3 each teaches this limitation to a Skilled Artisan.

539. As shown in the table below, claim limitation [21.b.2] is very similar to claim limitation [1.i.2]:

Claim 1	Claim 21
[1.i.2] the at least one circuit operable to (i) receive a first plurality of address and control signals via the first portion of the plurality of edge connections, and (ii) output a second plurality of address and control signals to the plurality of SDRAM devices,	[21.b.2] the at least one circuit operable to receive a first plurality of address and control signals via a second portion of the plurality of edge connections and to output a second plurality of address and control signals to the plurality of SDRAM devices,

540. As discussed above with reference to claim limitation [1.i.2], the prior art references in each of Grounds 2 and 3 satisfies this limitation. *Supra* ¶¶ 311-317. In particular, the "*a first plurality of address and control signals via the first portion of the plurality of edge connections*" in claim 1 corresponds to the "*a first plurality of address and control signals via a second portion of the plurality of edge connections*" in claim 21.

(3) [21.b.3] Coupled to the second and fourth regulated voltages

541. Claim 21 requires "*the at least one circuit coupled to both the second regulated voltage and the fourth regulated voltage*."

542. The prior art references in Grounds 2 and 3 each teaches this limitation to a Skilled Artisan.

543. As shown in the table below, claim limitation [21.b.3] is very similar to claim limitation [1.i.3]:

Claim 1	**Claim 21**
[1.i.3] the at least one circuit coupled to both the second regulated voltage and the fourth regulated voltage,	[21.b.3] the at least one circuit coupled to both the second regulated voltage and the fourth regulated voltage,

544. As discussed above with reference to claim limitation [1.i.3], the prior art references in each of Grounds 2 and 3 satisfies this limitation. *See* ¶¶ 318-323.

(4) [21.b.4] Wherein one of second and fourth regulated voltage amplitudes is less than the other

545. Claim 21 requires "*wherein a first one of the second and fourth voltage amplitudes is less than a second one of the second and fourth voltage amplitudes*."

546. The prior art references in Grounds 2 and 3 each teaches this limitation to a Skilled Artisan.

547. As shown in the table below, claim limitation [21.b.4] is very similar to claim limitation [1.i.4]:

Claim 1	**Claim 21**
[1.i.4] wherein a first one of the second and fourth voltage amplitudes is less than a second one of the second and fourth voltage amplitudes.	[21.b.4] wherein a first one of the second and fourth voltage amplitudes is less than a second one of the second and fourth voltage amplitudes.

548. As discussed above with reference to claim limitation [1.i.4], the prior art references in each of Grounds 2 and 3 satisfies this limitation. *Supra* ¶¶ 324-327.

22. Claim 22 is Unpatentable

549. Claim 22 is unpatentable as the prior art references in each of Grounds 2 and 3 (Voltage Mappings A, B, C, and D) render the claim obvious.

a) [22.a] Preamble

550. The preamble of claim 22 requires "*[t]he memory module of claim 16, the plurality of components further including*."

551. The prior art references in Grounds 2 and 3 each teaches this limitation to a Skilled Artisan.

552. As discussed above with reference to claim 16, the prior art references in each of Grounds 2 and 3 satisfies "*[t]he memory module of claim 16, the plurality of components further including*." *Supra* ¶¶478-503 (claim 16).

b) [22.b] A Logic Element

553. Claim 22 requires "*a logic element including an internal non-volatile memory, wherein the non-volatile memory is configured to store configuration information, wherein the configuration information is used to program the logic element*."

554. The prior art references in Grounds 2 and 3 each teaches this limitation to a Skilled Artisan.

555. As shown in the table below, claim limitation [22.b] is very similar to claim limitations [10.b] and [15.b]:

Claims 10 and 15	**Claim 22**
[10.b] a logic element including a non-volatile memory, the non-volatile memory is configured to store configuration information. [15.b] a logic element including one or more integrated circuits and discrete electrical elements, the one or more integrated circuit including an internal non-volatile memory, wherein the non-volatile memory is configured to store configuration information.	[22.b] a logic element including an internal non-volatile memory, wherein the non-volatile memory is configured to store configuration information, wherein the configuration information is used to program the logic element.

556. For the reasons discussed above with reference to claim limitation [10.b] and [15.b], Harris discloses to a Skilled Artisan a "*logic element*" (e.g., including logic in buffer 112 to implement AMB configuration register functionalities) "*including [a] … non-volatile memory, wherein the non-volatile memory is configured to store configuration information*" (e.g, including an internal non-volatile memory for storing S3 Recovery Configuration information), "*wherein the configuration information is used to program the logic element*" (e.g., Configuration Registers are programmed and used to restore state when exiting S3). *See* Ex. 1027at 25, 39, 141; *supra* ¶¶432-438, 472-476. As explained above, it would have been obvious to a Skilled Artisan to implement the buffer 112 with an internal non-volatile memory because it would decrease the number of components, interfaces and interconnections on the memory module, resulting in a cheaper, faster, and more secure solution. *See supra* ¶¶ 432-438; *see, e.g.*, Ex. 1023

(Harris) at [0002], [0012], [0019]; Ex. 1066 at 26:64-27:4; Ex. 1067 at 1-2. Thus, as discussed above with reference to claim limitations [10.b] and [15.b], the prior art references in each of Grounds 2 and 3 satisfies this limitation. *See supra* ¶¶ 432-438, 472-476.

23. Claim 23 is Unpatentable

557. Claim 23 is unpatentable as the prior art references in each of Grounds 1 through 3 render the claim obvious.

a) [23.a] Preamble

558. The preamble of claim 23 requires "*[a] memory module comprising*."

559. Harris teaches and discloses this limitation to a Skilled Artisan in each of Grounds 1 through 3.

560. As shown in the table below, claim limitation [23.a] is identical to claim limitation [1.a]:

Claim 1	**Claim 23**
[1.a] A memory module comprising:	[23.a] A memory module comprising:

561. As discussed above with reference to claim limitation [1.a], Harris satisfies "[a] memory module." *Supra* ¶¶216-222.

b) [23.b] A Printed Circuit Board (PCB)

562. Claim 23 requires "*a printed circuit board (PCB) having an interface configured to fit into a corresponding slot connector of a host system, the interface*

including a plurality of edge connections configured to couple power, data, address and control signals between the memory module and the host system."

563. Harris teaches and discloses this limitation to a Skilled Artisan in each of Grounds 1 through 3. In addition, for Grounds 1, 2, and 3, Harris in view of the FBDIMM Standards, teaches and discloses this limitation to a Skilled Artisan.

564. As shown in the table below, claim limitation [23.b] is very similar to claim limitation [1.b]:

Claim 1	**Claim 23**
[1.b] a printed circuit board (PCB) having an interface configured to fit into a corresponding slot connector of a host system, the interface including a plurality of edge connections configured to couple power, data, address and control signals between the memory module and the host system;	[23.b] a printed circuit board (PCB) having an interface configured to fit into a corresponding slot connector of a host system, the interface including a plurality of edge connections configured to couple power, data, address and control signals between the memory module and the host system;

565. As discussed above with reference to claim limitation [1.b], Grounds 1 through 3 satisfy this limitation. *Supra* ¶¶223-231.

c) [23.c] A Plurality of Components Coupled To The PCB

(1) [23.c.1] Each component coupled to one or more regulated voltages

566. Claim 23 requires "*a plurality of components coupled to the PCB, each component of the plurality of components coupled to one or more regulated voltages of first, second, third and fourth regulated voltages*."

567. The prior art references in each of Grounds 1 through 3 teach this limitation to a Skilled Artisan.

568. As shown in the table below, claim limitation [23.c.1] is very similar to claim limitation [1.g]:

Claim 1	**Claim 23**
[1.g] a plurality of components coupled to the PCB, each component of the plurality of components coupled to one or more regulated voltages of the first, second, third and fourth regulated voltages,	[23.c.1] a plurality of components coupled to the PCB, each component of the plurality of components coupled to one or more regulated voltages of first, second, third and fourth regulated voltages,

569. As discussed with reference to claim limitation [1.g], the prior art references in each of Grounds 1-3 satisfies this limitation. *Supra* ¶¶ 288-297.

(2) [23.c.2] Including SDRAM devices and one or more registers

570. Claim 23 requires "*the plurality of components including a plurality of synchronous dynamic random access memory (SDRAM) devices and one or*

more registers, the plurality of SDRAM devices coupled to the first regulated voltage, the one or more registers coupled to (i) the second regulated voltage, (ii) a portion of the plurality of edge connections, and (iii) the plurality of SDRAM devices."

571. The prior art references in each of Grounds 1 through 3 teach this limitation to a Skilled Artisan.

572. As shown in the table below, claim limitation [23.c.2] is very similar to claim limitations [1.h], [1.i.1], [1.i.3], and [8.b.1]:

Claims 1, 8	**Claim 23**
[1.h] a plurality of synchronous dynamic random access memory (SDRAM) devices coupled to the first regulated voltage, and [1.i.1] at least one circuit coupled between a first portion of the plurality of edge connections and the plurality of SDRAM devices [1.i.3] the at least one circuit coupled to both the second regulated voltage and the fourth regulated voltage, [8.b.1] one or more registers coupled to one of the first, second, third and fourth regulated voltages,	[23.c.2] a plurality of synchronous dynamic random access memory (SDRAM) devices and one or more registers, the plurality of SDRAM devices coupled to the first regulated voltage, the one or more registers coupled to (i) the second regulated voltage, (ii) a portion of the plurality of edge connections, and (iii) the plurality of SDRAM devices,

573. As discussed above with reference to claim limitations [1.h], [1.i.1], [1.i.3], and [8.b.1], the prior art references in each of Grounds 1-3 satisfies this limitation. *Supra* ¶¶298-303 (claim limitation [1.h]), ¶¶304-310 (claim limitation [1.i.1]), ¶¶318-323 (claim limitation [1.i.3]), ¶¶398-405 (claim limitation [8.b.1]).

(3) [23.c.3] Wherein address and control signals are coupled to one or more registers

574. Claim 23 requires "*wherein a plurality of address and control signals are coupled to the one or more registers via the portion of the plurality of edge connections*."

575. The prior art references in each of Grounds 1 through 3 teach this limitation to a Skilled Artisan.

576. As shown in the table below, claim limitation [23.c.3] is very similar to claim limitations [1.i.2] and [8.b.2]:

Claims 1, 8	**Claim 23**
[1.i.2] the at least one circuit operable to (i) receive a first plurality of address and control signals via the first portion of the plurality of edge connections, and (ii) output a second plurality of address and control signals to the plurality of SDRAM devices [8.b.2] the one or more registers configured to register, in response to a clock, the first plurality of address and control signals	[23.c.3] wherein a plurality of address and control signals are coupled to the one or more registers via the portion of the plurality of edge connections

577. As discussed above with reference to claim limitation [1.i.2] and [8.b.2], the prior art references in each of Grounds 1-3 satisfies this limitation. *Supra* ¶¶311-317 (claim limitation [1.i.2]), ¶¶406-409 (claim limitation [8.b.2]).

d) [23.d] First, Second, And Third Buck Converters

578. Claim 23 requires "*first, second, and third buck converters configured to provide the first, second and third regulated voltages, respectively*."

579. The prior art references in each of Grounds 1 through 3 teach this limitation to a Skilled Artisan.

580. As shown in the table below, claim limitation [23.d] is very similar to claim limitations [1.c] – [1.e]:

Claim 1	**Claim 23**
[1.c] a first buck converter configured to provide a first regulated voltage having a first voltage amplitude; [1.d] a second buck converter configured to provide a second regulated voltage having a second voltage amplitude; [1.e] a third buck converter configured to provide a third regulated voltage having a third voltage amplitude;	[23.d] first, second, and third buck converters configured to provide the first, second and third regulated voltages, respectively; and

581. As discussed above with reference to claim limitations [1.c] – [1.e], the prior art references in each of Grounds 1-3 satisfies this limitation. *Supra* ¶¶232-280.

e) [23.e] A Converter Circuit

582. Claim 23 requires "*a converter circuit configured to provide the fourth regulated voltage*."

583. The prior art references in each of Grounds 1 through 3 teach this limitation to a Skilled Artisan.

584. As shown in the table below, claim limitation [23.e] is very similar to claim limitation [1.f]:

Claim 1	Claim 23
[1.f] a converter circuit configured to provide a fourth regulated voltage having a fourth voltage amplitude; and	[23.e] a converter circuit configured to provide the fourth regulated voltage,

585. As discussed above with reference to claim limitation [1.f], the prior art references in each of Grounds 1-3 satisfies this limitation. *Supra* ¶¶281-287.

f) [23.f] Wherein The Second Regulated Voltage Is Configured To Be Selectively Switched On or Off

586. Claim 23 requires "*wherein the second regulated voltage is configured to be selectively switched on or off to the one or more registers while at least the plurality of SDRAM devices are powered on*."

587. The prior art references in Grounds 1 through 3 each teaches this limitation to a Skilled Artisan.

588. As shown in the table below, claim limitation [23.f] is very similar to claim limitation [8.b.3] and claim 14:

Claims 8, 14	Claim 23
[8.b.3] wherein the one of the first, second, third and fourth regulated voltages is selectively switched off to turn power off to the one or more registers while one or more components of the plurality of components are powered on. [14] The memory module of claim 8, wherein, in response to selectively switching on the one of the first, second, third and fourth regulated voltages to the one or more registers, the one or more registers is configured to output the registered first plurality of address and control signals to the plurality of SDRAM devices.	[23.f] wherein the second regulated voltage is configured to be selectively switched on or off to the one or more registers while at least the plurality of SDRAM devices are powered on,

589. As discussed above with reference to claim limitation [8.b.3] and claim 14, the prior art references in each of Grounds 1 through 3 satisfies this limitation. *See* ¶¶410-417 (claim limitation [8.b.3]) and ¶¶462-466 (claim 14).

g) [23.g] Wherein If The Second Regulated Voltage Is Switched On . . .

590. Claim 23 requires "*wherein if the second regulated voltage is switched on while at least the plurality of SDRAM devices are powered on, the one or more registers are configured to couple the first plurality of address and control signals to the plurality of SDRAM devices*."

591. The prior art references in Grounds 1 through 3 each teaches this limitation to a Skilled Artisan.

592. As shown in the table below, claim limitation [23.g] is very similar to claim 14:

Claim 14	**Claim 23**
[14] The memory module of claim 8, wherein, in response to selectively switching on the one of the first, second, third and fourth regulated voltages to the one or more registers, the one or more registers is configured to output the registered first plurality of address and control signals to the plurality of SDRAM devices.	[23.g] wherein if the second regulated voltage is switched on while at least the plurality of SDRAM devices are powered on, the one or more registers are configured to couple the first plurality of address and control signals to the plurality of SDRAM devices, and

593. As discussed above with reference to claim 14, the prior art references in each of Grounds 1 through 3 satisfies this limitation. *Supra* ¶¶ 462-464.

h) [23.h] Wherein If The Second Regulated Voltage Is Switched Off . . .

594. Claim 23 requires "*wherein if the second regulated voltage is switched off while the plurality of SDRAM devices are powered on, the one or more registers are configured to decouple the plurality of SDRAM devices from the first plurality of address and control signals*."

595. The prior art references in Grounds 1 through 3 each teaches this limitation to a Skilled Artisan.

596. As shown in the table below, claim limitation [23.h] is very similar to claim limitation [8.b.3]:

Claim 8	**Claim 23**
[8.b.3] wherein the one of the first, second, third and fourth regulated voltages is selectively switched off to turn power off to the one or more registers while one or more components of the plurality of components are powered on.	[23.h] wherein the second regulated voltage is configured to be selectively switched on or off to the one or more registers while at least the plurality of SDRAM devices are powered on, the one or more registers are configured to decouple the plurality of SDRAM devices from the first plurality of address and control signals.

597. As discussed above with reference to claim limitation [8.b.3], the prior art references in each of Grounds 1 through 3 satisfies this limitation. *Supra* ¶¶410-417 (claim limitation [8.b.3]). Furthermore, a Skilled Artisan would have understood that, in S3 sleep mode, "*the one or more registers are configured to decouple the plurality of SDRAM devices from the first plurality of address and control signals*" because the registers are not powered and because the address and control lines are driven low in S3 mode. *See, e.g.*, Ex. 1027 (JESD82-20) at 21 (point 6) ("When the Advanced Memory Buffer core logic is in S3 power mode, all command/address outputs, including CKE, ODT, CLK, and all other command/address pins, will be driven low. In S3 mode, 1.8V supply is on. 1.5V,

Vtt, and 3.3V are off. DRAMs are in self refresh, and the CKE signals must be driven low.").

24. Claim 24 is Unpatentable

598. Claim 24 is unpatentable as the prior art references in each of Grounds 2 and 3 (Voltage Mappings A, B, and C) render the claim obvious.

a) [24.a] Preamble

599. The preamble of claim 24 requires "*[t]he memory module of claim 23, further comprising*."

600. As discussed above with reference to claim limitation 23, the prior art references in each of Grounds 2 and 3 satisfies "*[t]he memory module of claim 23*." *Supra* ¶¶558-597.

b) [24.b] A Voltage Monitor Circuit

601. Claim 24 requires "*a voltage monitor circuit configured to monitor an input voltage received from the host system via the interface, the voltage monitor circuit configured to produce a signal in response to the input voltage having a voltage amplitude that is greater than a first threshold voltage*."

602. The prior art references in Grounds 2 and 3 each teaches this limitation to a Skilled Artisan.

603. As shown in the table below, claim limitation [24.b] is very similar to claim limitation [5.b]:

Claim 5	Claim 24
[5.b] a voltage monitor circuit configured to monitor a power input voltage received via a second portion of the plurality of edge connections, the voltage monitor circuit configured to produce a trigger signal in response to the power input voltage having a voltage amplitude that is greater than a first threshold voltage.	[24.b] a voltage monitor circuit configured to monitor an input voltage received from the host system via the interface, the voltage monitor circuit configured to produce a signal in response to the input voltage having a voltage amplitude that is greater than a first threshold voltage.

604. As discussed above with reference to claim limitation [5.b], the prior art references in each of Grounds 2 and 3 satisfies this limitation. *Supra* ¶¶363-376. In particular, to the extent one were to argue that overvoltage protection was not obvious in light of Ground 2, it would have been obvious in light of Hajeck, as part of Ground 3. *Supra* ¶¶375-376

25. Claim 25 is Unpatentable

605. Claim 25 is unpatentable as the prior art references in each of Grounds 2 and 3 (Voltage Mappings A, B, and C) render the claim obvious.

a) [25.a] Preamble

606. The preamble of claim 25 requires "*[t]he memory module of claim 24, the plurality of components further including*."

607. The prior art references in Grounds 2 and 3 each teaches this limitation to a Skilled Artisan.

608. As discussed above with reference to claim 24, the prior art references in each of Grounds 2 and 3 satisfies "*[t]he memory module of claim 24*." *Supra* ¶¶599-604.

b) [25.b] A Controller

609. Claim 25 requires "*a controller coupled to the voltage monitor circuit and configured to receive the signal, wherein, in response to the signal, the controller executes a write operation*."

610. To the extent Netlist asserts that the limitation of "*a write operation*" is satisfied by writing configuration information, the prior art references in Grounds 2 and 3 each teaches this limitation to a Skilled Artisan.

611. As shown in the table below, claim limitation [25.b] is very similar to claim limitation [12.c]:

Claim 12	**Claim 25**
[12.c] a controller configured to receive the trigger signal, wherein, in response to the trigger signal, the controller performs a write operation to the non-volatile memory.	[25.b] a controller coupled to the voltage monitor circuit and configured to receive the signal, wherein, in response to the signal, the controller executes a write operation.

612. As discussed above with reference to claim limitation [12.c], the prior art references in each of Grounds 2 and 3 satisfies this limitation. *Supra* ¶¶ 453-455.

613. To the extent the limitation of "*a write operation*" requires writing user data, for example, from volatile memory to non-volatile memory, such an interpretation would have been also obvious to a Skilled Artisan for the reasons discussed with reference to Grounds 4-5.

26. Claim 26 is Unpatentable

614. Claim 26 requires "*[t]he memory module of claim 25, wherein the write operation includes writing data information to non-volatile memory*."

615. To the extent Netlist asserts that the limitation of "*the write operation includes writing data information to non-volatile memory*" is satisfied by writing configuration information to non-volatile memory, the prior art references in Grounds 2 and 3 (Voltage Mappings A, B, and C) each teaches this limitation to a Skilled Artisan.

616. As shown in the table below, claim 26 is very similar to claim limitation [12.c]:

Claim 12	**Claim 26**
[12.c] a controller configured to receive the trigger signal, wherein, in response to the trigger signal, the controller performs a write operation to the non-volatile memory.	[26] The memory module of claim 25, wherein the write operation includes writing data information to non-volatile memory.

617. As discussed above with reference to claim limitation [12.c], the prior art references in each of Grounds 2 and 3 satisfies this limitation. *Supra* ¶¶453-455.

618. To the extent the limitation of "*the write operation includes writing data information to non-volatile memory*" requires writing user data from volatile memory to non-volatile memory, such an interpretation would have been also obvious to a Skilled Artisan for the reasons discussed with reference to Grounds 4-5.

27. Claim 27 is Unpatentable

619. Claim 27 is unpatentable as the prior art references in each of Grounds 2 and 3 (Voltage Mappings A, B, and C) render the claim obvious.

620. Claim 27 requires "*[t]he memory module of claim 24, wherein the voltage monitor circuit is further configured to produce the signal in response to the input voltage having a voltage amplitude that is less than a second threshold voltage*."

621. The prior art references in Grounds 2 and 3 each teaches this limitation to a Skilled Artisan.

622. As shown in the table below, claim 27 is very similar to claim 6:

Claim 6	Claim 27
[6] The memory module of claim 5, wherein the voltage monitor circuit is further configured to produce the trigger signal in response to the power input voltage having a voltage amplitude that is less than a second threshold voltage.	[27] The memory module of claim 24, wherein the voltage monitor circuit is further configured to produce the signal in response to the input voltage having a voltage amplitude that is less than a second threshold voltage.

623. As discussed above with reference to claim 6, the prior art references in each of Grounds 2 and 3 satisfies this limitation. *Supra* ¶¶377-384.

28. Claim 28 is Unpatentable

624. Claim 28 is unpatentable as the prior art references in each of Grounds 2 and 3 (Voltage Mappings A, B, and C) render the claim obvious.

625. Claim 28 requires "*[t]he memory module of claim 23, wherein the second and third buck converters are configured to operate as a dual buck converter*."

626. The prior art references in Grounds 2 and 3 each teaches this limitation to a Skilled Artisan.

627. As shown in the table below, claim 28 is very similar to claim 17:

Claim 17	Claim 28
[17] The memory module of claim 16, wherein the second and third buck converters are configured to operate as a dual buck converter.	[28] The memory module of claim 23, wherein the second and third buck converters are configured to operate as a dual buck converter.

628. For the reasons discussed above with reference to claim 17, the prior art references in each of Grounds 2 and 3 satisfies this limitation. *See* ¶¶504-0.

29. Claim 29 is Unpatentable

629. Claim 29 is unpatentable as the prior art references in Grounds 2 and 3 (Voltage Mappings A, B, and C) render the claim obvious.

630. Claim 29 requires "*[t]he memory module of claim 23, wherein the plurality of SDRAM devices are configured to receive at least one of the first, second, third and fourth regulated voltages having a voltage amplitude of 1.8 volts*."

631. The prior art references in Grounds 2 and 3 each teaches this limitation to a Skilled Artisan.

632. As shown in the table below, claim 29 is very similar to claim 20:

Claim 20	Claim 29
[20] The memory module of claim 16, wherein the plurality of SDRAM devices are configured to receive at least one of the first, second, third and fourth regulated voltages having a voltage amplitude of 1.8 volts.	[29] The memory module of claim 23, wherein the plurality of SDRAM devices are configured to receive at least one of the first, second, third and fourth regulated voltages having a voltage amplitude of 1.8 volts.

633. As discussed above with reference to claim 20, the prior art references in each of Grounds 2 and 3 satisfies this limitation. *Supra* ¶¶524-528.

30. Claim 30 is Unpatentable

634. Claim 30 is unpatentable as the prior art references in each of Grounds 2 and 3 (Voltage Mappings A, B, and C) render the claim obvious.

635. Claim 30 requires "*[t]he memory module of claim 23, wherein the first, second, and third buck converters are configured to receive a pre-regulated input voltage and to provide the first, second and third regulated voltages, respectively, and wherein the converter circuit is configured to reduce the pre-regulated voltage input to provide the fourth regulated voltage*."

636. The prior art references in Grounds 2 and 3 each teaches this limitation to a Skilled Artisan.

637. As shown in the table below, claim 30 is very similar to claim 13 and claim limitations [1.c] – [1.f] and [16.c] – [16.d.1]:

Claims 1, 13	**Claim 16**	**Claim 30**
[1.c] a first buck converter configured to provide a first regulated voltage having a first voltage amplitude; [1.d] a second buck converter configured to provide a second regulated voltage having a second voltage amplitude; [1.e] a third buck converter configured to provide a third regulated voltage having a third voltage amplitude; [1.f] a converter circuit configured to provide a fourth regulated voltage having a fourth voltage amplitude; and [13] The memory module of claim 5, wherein the power input voltage is coupled to the first, second, and third buck converters and the converter circuit.	[16.c] first, second, and third buck converters configured to receive a pre-regulated input voltage and to produce first, second and third regulated voltages, respectively; [16.d.1] a converter circuit configured to reduce the pre-regulated input voltage to provide a fourth regulated voltage,	[30] The memory module of claim 23, wherein the first, second, and third buck converters are configured to receive a pre-regulated input voltage and to provide the first, second and third regulated voltages, respectively, and wherein the converter circuit is configured to reduce the pre-regulated voltage input to provide the fourth regulated voltage.

638. As discussed above with reference to claim 13 and claim limitations [1.c] – [1.f] and [16.c] – [16.d.1], the prior art references in each of Grounds 2 and

3 satisfies this limitation. *See* ¶¶232-287 (claim limitations [1.c] – [1.f]), ¶¶457-461 (claim 13), ¶¶484-493 (claim limitations [16.c] – [16.d.1]).

B. Claims 1-30 Are Unpatentable Over Grounds 4 and/or 5

639. As explained below, claims 1--30 are unpatentable over Ground 4 (Spiers in view of Amidi) and Ground 5 (Ground 4 further in view of Hajeck).

1. Claim 1 is Unpatentable

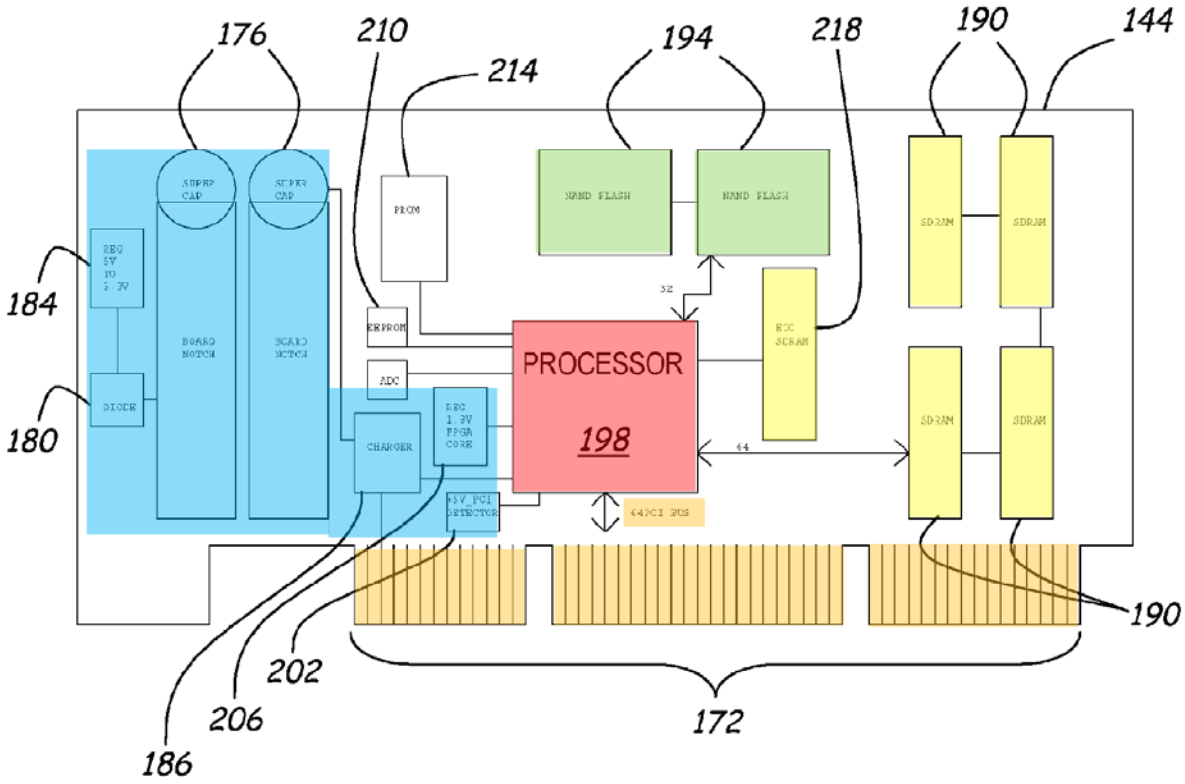
640. Claim 1 is unpatentable as the prior art references in each of Grounds 4 and 5 (Voltage Mappings A, B, and C) render the claim obvious.

a) [1.a] Preamble

641. The preamble of claim 1 recites "*[a] memory module comprising.*"

642. The prior art references in each of Grounds 4 and 5 teach this limitation to a Skilled Artisan.

643. As shown in the annotated figure below, Spiers discloses a "*memory module*" to a Skilled Artisan, such as backup device 144 implemented in a PCI card, and including volatile memory devices (*e.g.*, SDRAMs 190 annotated in yellow) and non-volatile memory devices (*e.g.*, NAND Flash 194 annotated in green).



Ex. 1025 at Fig. 5 (annotated). Spiers explains that, "[i]n this embodiment, the backup device is embodied in a PCI card having a 64-bit PCI connector 172 . . . the volatile memory comprises a number of SDRAM modules 190 . . . [and the] non-volatile memory in this embodiment comprises a number of NAND flash modules 194." *Id*. at [0037].

644. A Skilled Artisan would have understood that this backup device is a "*memory module*" because it includes a card (PCI card) with memories mounted on it and configured to store data received from the system, as shown in Figure 3 of Spiers reproduced below.

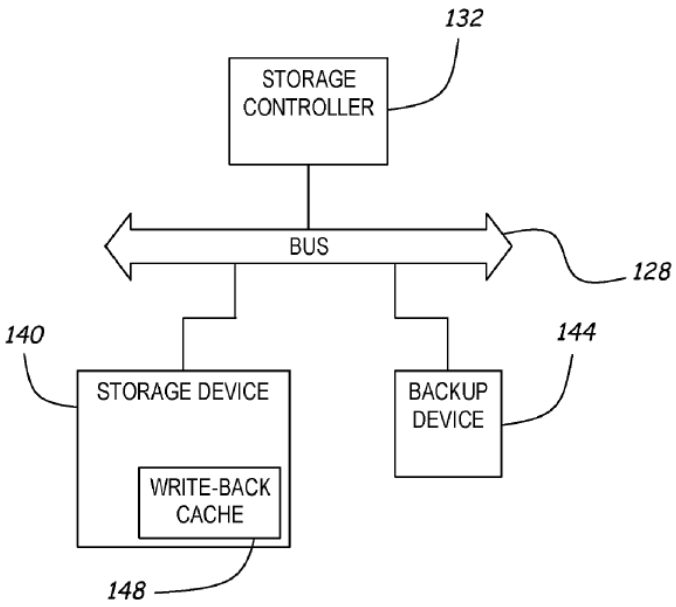


FIG.3

See id. at Fig. 3. For example, Spiers discloses that "the storage controller 132 stores a copy of the data in the backup device 144 as well as writing the data to the storage device 140. In this embodiment, if a failure occurs which results in the storage device 140 not storing the data to the storage media, a copy of the data is maintained in the backup device 144." *Id*. at [0034].

645. The backup device disclosed by Spiers is also consistent with how the 918 Patent describes a "*memory module*." For example, the 918 Patent states "[c]ertain types of memory modules comprise a plurality of dynamic random-access memory (DRAM) devices mounted on a printed circuit board (PCB). These memory modules are typically mounted in a memory slot or socket of a computer system (e.g., a server system or a personal computer) and are accessed by the

computer system to provide volatile memory to the computer system." Ex. 1001 at 3:46-52.

646. Accordingly, to the extent the preamble of claim 1 is limiting, the prior art references in each of Grounds 4 and 5 satisfy "*[a] memory module comprising*."

b) [1.b] Printed Circuit Board Having an Interface

647. Claim 1 requires "*a printed circuit board (PCB) having an interface configured to fit into a corresponding slot connector of a host system, the interface including a plurality of edge connections configured to couple power, data, address and control signals between the memory module and the host system.*"

648. The prior art references in each of Grounds 4 and 5 teach this limitation to a Skilled Artisan.

649. Spiers discloses to a Skilled Artisan a printed circuit board (PCB), such as a PCB of a PCI card of backup device 144. Ex. 1025 at Fig. 5; *see also*, *e.g.*, Ex. 1031 at 298 (defining a PCI "expansion board" as a "circuit board that plugs into a mother board"), 152 (Section 4.4.3.2 describing routing for four-layer boards). Thus, Spiers satisfies a "*printed circuit board (PCB)*."

650. Spiers also discloses that the PCB has a 64-bit PCI connecter 172. *See* Ex. 1025 at Fig. 5. A Skilled Artisan would have understood that the PCI connector 172 is an interface that includes edge connections configured to fit into a

corresponding slot connector on a PCI bus. For example, the figure below shows that a PCI board has a connecter with a keyway to fit into the corresponding slot on the motherboard.

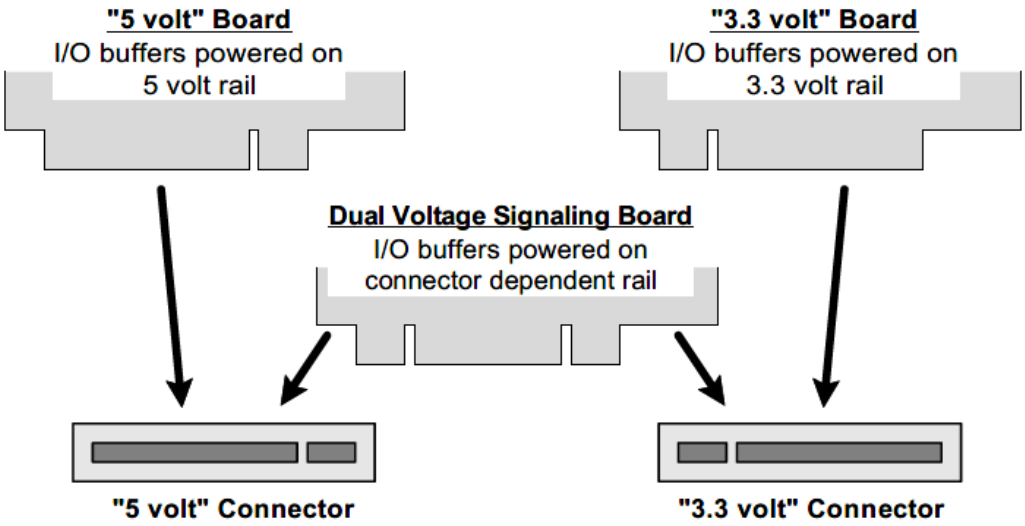


Figure 4-1: PCI Board Connectors

Ex. 1031 at 114, Fig. 4-1 (reproduced below), 3 ("Typical PCI Local Bus implementations will support up to four add-in board connectors . . . PCI extension cards use an edge connector and motherboards that allow a female connector . . . ."). Thus, Spiers satisfies the PCB "*having an interface configured to fit into a corresponding slot connector of a host system, the interface including a plurality of edge connections*."

651. Spiers also discloses edge connections of the interface "*configured to couple power, data, address and control signals between the memory module and the host system*." In particular, a Skilled Artisan would have understood that PCI

connector 172 is for a dual-voltage signaling board since it has two notches or keyways that are configured to fit into a corresponding slot connector of a host system. *Id.* Accordingly, its "*edge connections [are] configured to couple power*," e.g., to a +5 volt power supply. *Id.* at 146-150 (describing pins of the board, including power pins for +5V power supply). For example, Spiers discloses receiving power at a 5-volt pin of the PCI card. Ex. 1025 at [0054] ("In the PCI card embodiment, this monitoring is performed by monitoring the voltage at a +5 volt pin.").

652. A Skilled Artisan would have also understood that, through the "64-bit PCI bus," Spiers's module receives address and data with corresponding read or write commands to store or retrieve the user data. Ex. 1025 at [0037]; Ex. 1031 at 1 ("The PCI Local Bus is a high performance 32-bit or 64 bit bus with multiplexed address and data lines"), 7 (Fig. 2-1, reproduced below, describing PCI pins including AD pins for address and data and C/BE pins for bus control signals), 10; *see also id*. at 21-25 (describing C/BE commands for read and write operations).

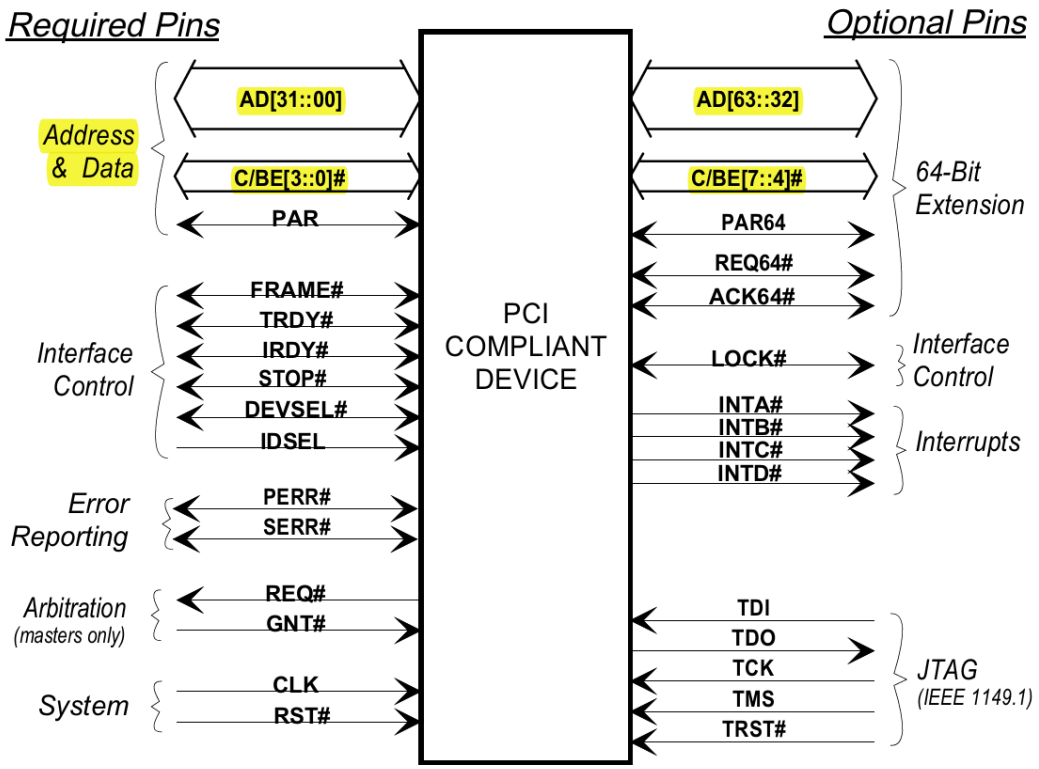


Figure 2-1: PCI Pin List

653. Spiers also discloses that "the backup device 144 utilizes a descriptor pointer queue contained within the FPGA processor 198 to receive commands from the storage controller." Ex. 1025 at [0039]; *see also id*. at Figs. 9, 10 and 11 (describing operational steps of the backup device processor when receiving commands and transferring data between the host memory and the SDRAMs on the module at corresponding addresses). Thus, Spiers satisfies the edge connections "*configured to couple power, data, address and control signals between the memory module and the host system*."

654. Accordingly, the prior art references in each of Grounds 4 and 5 satisfy "*a printed circuit board (PCB) having an interface configured to fit into a*

corresponding slot connector of a host system, the interface including a plurality of edge connections configured to couple power, data, address and control signals between the memory module and the host system."

c) [1.c] A First Buck Converter

655. Claim 1 requires "*a first buck converter configured to provide a first regulated voltage having a first voltage amplitude.*"

656. The prior art references in each of Grounds 4 and 5 teach this limitation to a Skilled Artisan.

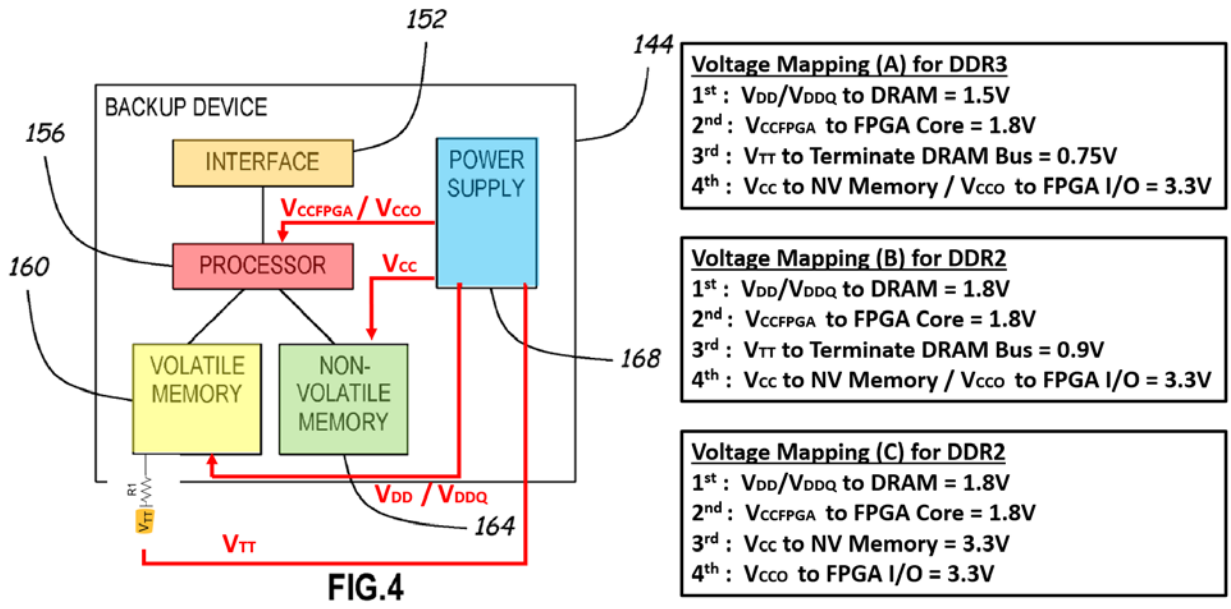
657. Spiers discloses "monitoring the voltage at a +5 volt pin" of the PCI card to detect power failure. Ex. 1025 at [0054], Fig. 14. A Skilled Artisan would have understood from this disclosure that the PCI card uses the "+5 volt" power supply of the PCI bus to power components of the card, including the SDRAM devices (e.g., SDRAMs 190 and 218). *See id.* at Fig. 5. Indeed, Spiers transfers data from the SDRAMs in case of power failure detected at the "+5 volt" pin, indicating that Spiers powers the SDRAM devices from the +5V power source. *See id.*

658. In addition, a Skilled Artisan would have recognized that SDRAM devices at the time required power supply voltages, such as VDD and VDDQ, that are less than, or stepped down from, 5 volts (and often even less than 3.3 volts, the other power supply in the PCI bus), and these power supply voltages need to be

regulated to keep them within the limits, as required by the specification for those SDRAM devices. For example, the JEDEC DDR SDRAM standard, JESD79, requires a VDDQ supply of 2.5 volts +/- 0.2 volts and a VDD supply of, for example, 2.5 volts +/- 0.2 volts. Ex. 1045 (JESD79) at Cover, p.7. As another example, the JEDEC DDR2 SDRAM standard, JESD79-2B, requires VDD, VDDQ, and VDDL supplies of 1.8 volts +/- 0.1V. Ex. 1026 at pp.6-7. As a further example, the JEDEC DDR3 SDRAM standard, JESD79-3A, requires VDD and VDDQ supplies of 1.5 volts +/- 0.075V. Ex. 1046 at p.10.

659. For Ground 4 (Spiers in view of Amidi) and Ground 5 (Speirs in view of Amidi and Hajeck), there are three mappings for the "*regulated voltage[s]*," as shown in the figure below. While the figure below references Ground 4, the voltage mappings of Ground 5 are the same. These voltage mappings correspond to the implementation of Spier's backup device with DDR3 (Voltage Mapping (A)) or DDR2 (Voltage Mapping (B) and Voltage Mapping (C)) DRAMs.

Ground 4: Spiers in view of Amidi, with DDR2 or DDR3 DRAMs



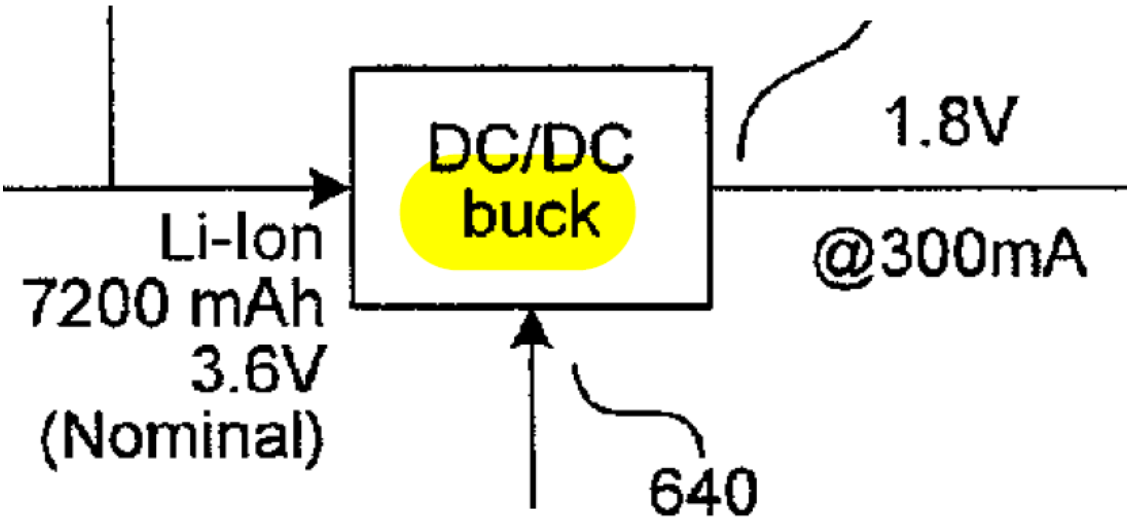
Ex. 1025 at Fig. 4 (annotated).

660. As previously explained, a Skilled Artisan would understand that JESD79-3A specifies a VDD/VDDQ power supply voltage of 1.5 volts for DDR3 DRAMs (i.e., the "*first regulated voltage*" for Mapping A of Grounds 4 and 5). Ex. 1046 at p.10. Similarly, she would understand that JESD79-2B specifies a VDD/VDDQ of 1.8 volts for DDR2 DRAMs (i.e., the "*first regulated voltage*" for Mappings B and C of Grounds 4 and 5). Ex. 1026 at p.7.

661. Thus, for Mappings A through C of Grounds 4 and 5, Spiers teaches and discloses to a Skilled Artisan a "*first* … [step-down] *converter configured to provide a first regulated voltage having a first voltage amplitude"* for the SDRAM devices from the +5 volt external power supply.

662. Furthermore, it would have been obvious to a Skilled Artisan to use a "*buck converter*" as the step-down converter to achieve high efficiency, reliable power conversion. *See*, *e.g.*, Ex. 1059 at 5:23-30 ("Switch mode buck converters have become popular due to two attractive features: first, they are more efficient than traditional low drop out regulators (LDO) (e.g., up to 95%) and second, they can provide relatively high currents with lower power dissipation on chip than an LDO can."). A Skilled Artisan would have understood that the efficiency of power conversion is particularly important in implementations like Spiers, designed to handle power outages by transferring data from volatile to non-volatile memories using a temporary power supply, such as a capacitor, because any loss at the power conversion takes away time for this backup operation, risking its successful completion. *See*, *e.g.*, Ex. 1025 at Fig. 14 (step 752 checking if capacitors have sufficient charge to transfer data from volatile to non-volatile memory).

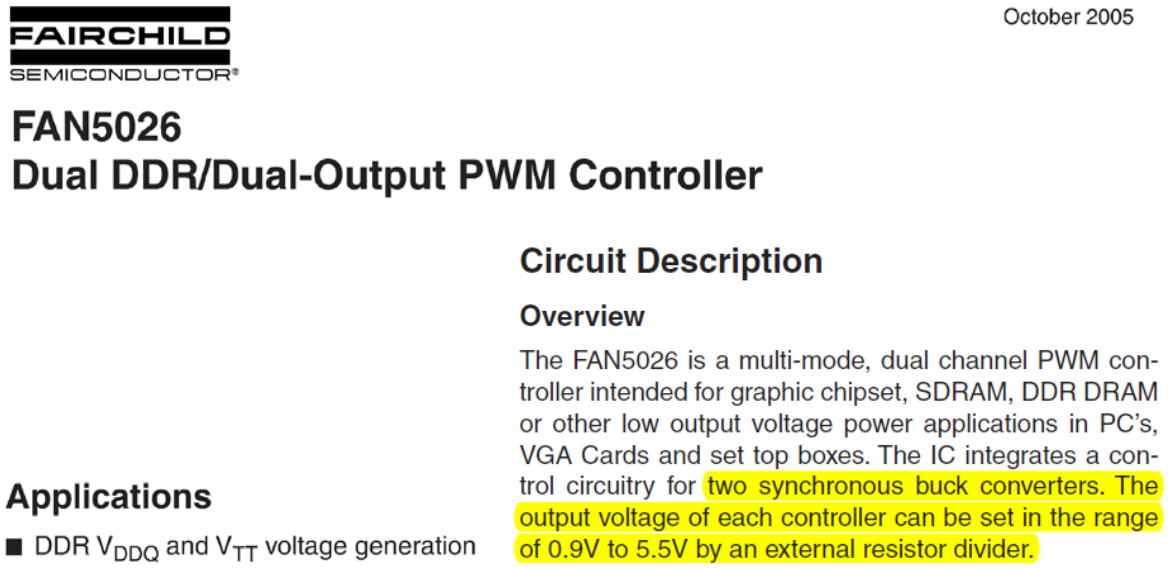
663. Indeed, it was well known at the time to use buck converters to power SDRAM devices. For example, Amidi discloses using a buck converter to convert backup battery power to a lower voltage for SDRAM memory devices. Ex. 1024 at Fig. 6 (buck converter 640), 4:38-41.



664. This was a well-known common practice at the time, as evidenced, for example, by Shearon (US7,023,187), which discloses "a multi (dual) voltage power supply architecture, in which an upstream buck converter stage is coupled in cascade with a downstream buck converter stage." Ex. 1047 at 2:47-55; *see also id.* at 5:56-59 (disclosing its buck converter for "supplying a regulated voltage to a DDR DRAM").

665. Such buck converters for SDRAMs were also commercially available at the time. *See id*. at 7:6-14 ("An embodiment of the dual buck mode power supply of the invention has been implemented in an integrated circuit, identified as part number ISL6530 by Intersil Corporation of Irvine, Calif., the assignee of the present application. Details regarding this part may be found in an advance data sheet, entitled 'Dual 5V Buck and Synchronous Buck Pulse-Width Modulator (PWM) Controller for DDRAM Memory VDDQ and VTT Termination', a copy of

which has been submitted as an Appendix."); *see also* Ex. 1041 at 1, 2 and 9 disclosing buck converters for SDRAM devices (reproduced below in part, annotated).



FAIRCHILD SEMICONDUCTOR®

October 2005

FAN5026
Dual DDR/Dual-Output PWM Controller

Circuit Description

Overview

The FAN5026 is a multi-mode, dual channel PWM controller intended for graphic chipset, SDRAM, DDR DRAM or other low output voltage power applications in PC's, VGA Cards and set top boxes. The IC integrates a control circuitry for two synchronous buck converters. The output voltage of each controller can be set in the range of 0.9V to 5.5V by an external resistor divider.

Applications

- DDR V_{DDQ} and V_{TT} voltage generation

666. In addition, a Skilled Artisan would have understood, and been motivated by, the fact that a buck converter efficiently steps down the voltage without generating excess heat or requiring excessively large cooling devices. For example, U.S. Patent No. 7,061,214 to Mayega *et al.* states that "[s]witch mode buck converters have become popular due to two attractive features: first, they are more efficient than traditional low drop out regulators (LDO) (e.g., up to 95%) and second, ***they can provide relatively high currents with lower power dissipation on chip than an LDO can***." Ex. 1059 at 5:23-30 (emphasis added); *see also* Ex. 1034 at 1:58-2:1 (describing charge pump circuits as "generally inefficient and consume large amounts of current"); Ex. 1040 (Texas Instruments TPS51020) at 1

(describing "high efficiency applications" across loads), Figs 22-25 (showing efficiency versus output current); Ex. 1041 (FAN5026 Dual DDR/Dual-Output PWM Controller) at 1, 13 (describing high efficiency operation "over a wide range of loads"); Ex. 1048 at 3 (specifying an efficiency of 75%); Ex. 1058 at 5 ("1.3 Switching-Regulator Theory") ("The high efficiency of switching regulators is the result of operating the series transistor in a switching mode."); Ex. 1062 at 11 (explaining that "lower dissipation" of electronic devices, such as a Class D amplifier, "saves the cost (and space) of cooling apparatus like heat sinks or fans"); Ex. 1064 at [0101] (discussing "Power loss algo[r]ithm" to flash DRAM to FLASH during a "power los event" in which the "VR Efficiency" is 85%).

667. Accordingly, the prior art references in each of Grounds 4 and 5 satisfy "*a first buck converter configured to provide a first regulated voltage having a first voltage amplitude*."

d) [1.d] A Second Buck Converter

668. Claim 1 requires "*a second buck converter configured to provide a second regulated voltage having a second voltage amplitude*."

669. The prior art references in each of Grounds 4 and 5 teach this limitation to a Skilled Artisan.

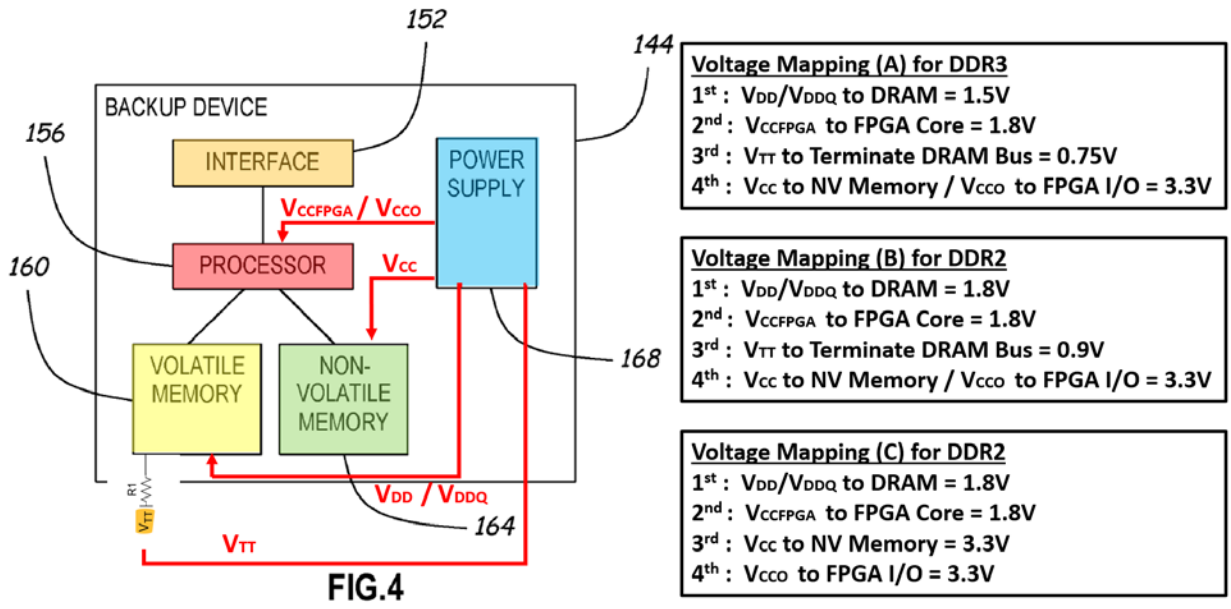
670. Spiers discloses that "[t]he FPGA processor receives power through a voltage regulator 206, which regulates the voltage required for the FPGA core."

Ex. 1025 at [0037]. For the reasons discussed above with reference to claim limitation [1.c], a Skilled Artisan would have understood, and it at least would have been obvious to her, that voltage regulator 206 includes a buck converter to generate a supply voltage of, for example, 1.8 volts, as shown in Fig. 5 of Spiers (reproduced below in part, annotated), from the +5 volt external power supply. *Supra* ¶¶655-666; Ex. 1025 at Fig. 5.



671. This understanding is reflected below in Voltage Mappings A through C of Grounds 4 and 5, where a 1.8V supply voltage (labeled "VCCFPGA") is generated in the voltage regulator 206 (blue, below) and provided to processor 198 (red, below).

Ground 4: Spiers in view of Amidi, with DDR2 or DDR3 DRAMs



Ex. 1025 at Fig. 4 (annotated).

672. A Skilled Artisan would have also understood that the specific voltage value of 1.8 volts in Fig. 5 of Spiers is just one example and that different FPGAs had different voltage requirements for VCCFPGA (labeled as "VCCINT" in the figure below). *See*, *e.g.*, Ex. 1042 at 2 (reproduced below, in part, showing different FPGAs and their power requirements).

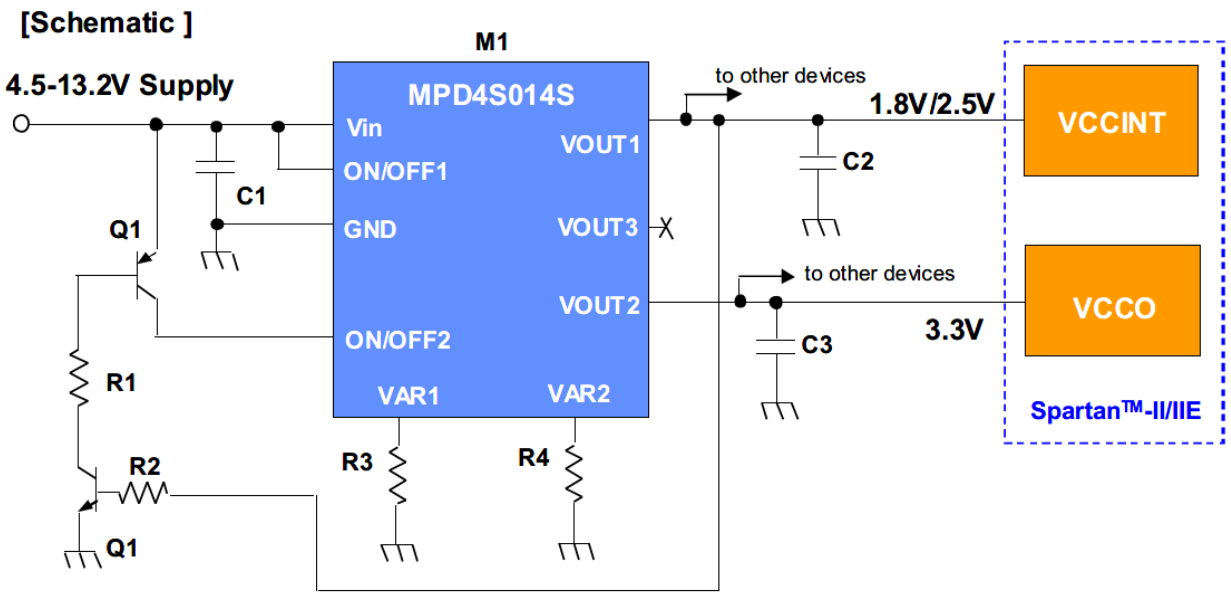
673. Indeed, a POSITA would have understood that FPGA devices operate at voltages within a known range. For example, Harris discloses that the buffer/logic component operates in the range between 0.5 and 3.5 volts. *See* Ex. 1023 at [0009] ("a second voltage path 106, typically referred to as a Vcc path, are provided with respect to the buffer component 112, wherein the Vcc path may be energized to appropriate voltage levels depending on the buffer and DIMM

technology, e.g., ***from about 0.5V to 3.5V or more***") (emphasis added). As another example, the Power Supply Reference Guide for Xilinx FPGAs discloses voltages between 1.0V and 3.3V. *See, e.g.*, Ex. 1042 at 2 (reproduced below, in part, showing different FPGAs and their power requirements).

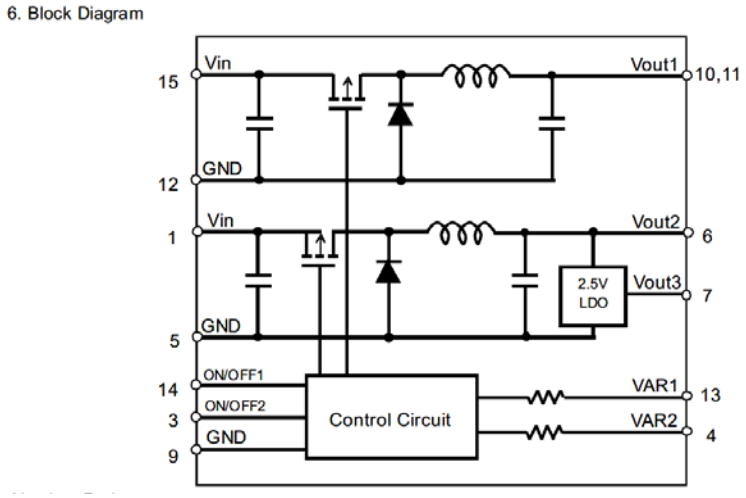
	Spartan™-3/3E/3L	Spartan™-IIE	Spartan™-II	Virtex™-5	Virtex™-4	Virtex-II Pro™	Virtex™-II
V_{CCINT}	1.2V @0.2A-5A	1.8V @0.2A-1.5A	2.5V @0.2A-1A	1.0V @0.2A-15A	1.2V @0.2A-20A	1.5V @0.2A-20A	1.5V @0.2A-20A
V_{CCO}	1.2V-3.3V @50mA-3A	1.5V-3.3V @50mA-0.5A	1.5V-3.3V @50mA-0.5A	1.2V-3.3V @50mA-5A	1.2V-3.3V @50mA-3A	1.5V-3.3V @50mA-3A	1.5V-3.3V @50mA-3A
V_{CCAUX}	2.5V @50mA-0.3A	–	–	2.5V @50mA-0.7A	2.5V @50mA-0.7A	2.5V @50mA-0.3A	3.3V @50mA-0.3A

Further, a Skilled Artisan would have understood that it would have been an obvious design choice to select one or more FPGAs, and it was at least obvious to try an FPGA with a 1.8V supply, such as a Spartan II-E. *See* Ex. 1042 at 2 (reproduced above).

674. Additionally, a Skilled Artisan would have understood that buck converters were commercially available to power those FPGAs. *See* Ex. 1042 at 16 (reproduced below in part, showing the use of a commercially available dual buck converter, MPD4S014S, to supply those voltages, including 1.8V and 3.3V).



Compare Ex. 1048 at 2 (depicting internal structure of MPD4S014S with two typical buck converters, below), *with* Ex. 1058 at 5, Fig. 2 (illustrating a buck converter); Ex. 1032 at 164-165, Fig. 7-4(a) (same).



675. Thus, Spiers in view of Amidi teaches and discloses to a Skilled Artisan that Spiers's voltage regulator 206 includes a "*second buck converter*" to

generate a supply voltage, for example, VCCFPGA of 1.8 volts (i.e., "*a second regulated voltage*"), provided to the FPGA.

676. Accordingly, the prior art references in each of Grounds 4 and 5 satisfy "*a second buck converter configured to provide a second regulated voltage having a second voltage amplitude.*"

e) [1.e] A Third Buck Converter

677. Claim 1 requires "*a third buck converter configured to provide a third regulated voltage having a third voltage amplitude.*"

678. The prior art references in each of Grounds 4 and 5 teach this limitation to a Skilled Artisan.

679. As discussed above with reference to claim limitation [1.c], Spiers discloses "monitoring the voltage at a +5 volt pin" of the PCI card to detect power failure. *Supra* ¶¶655-666*;* Ex. 1025 at [0054], Fig. 14. A Skilled Artisan would have understood from this disclosure that the PCI card uses the "+5 volt" power rail of the PCI bus to power the SDRAM devices.

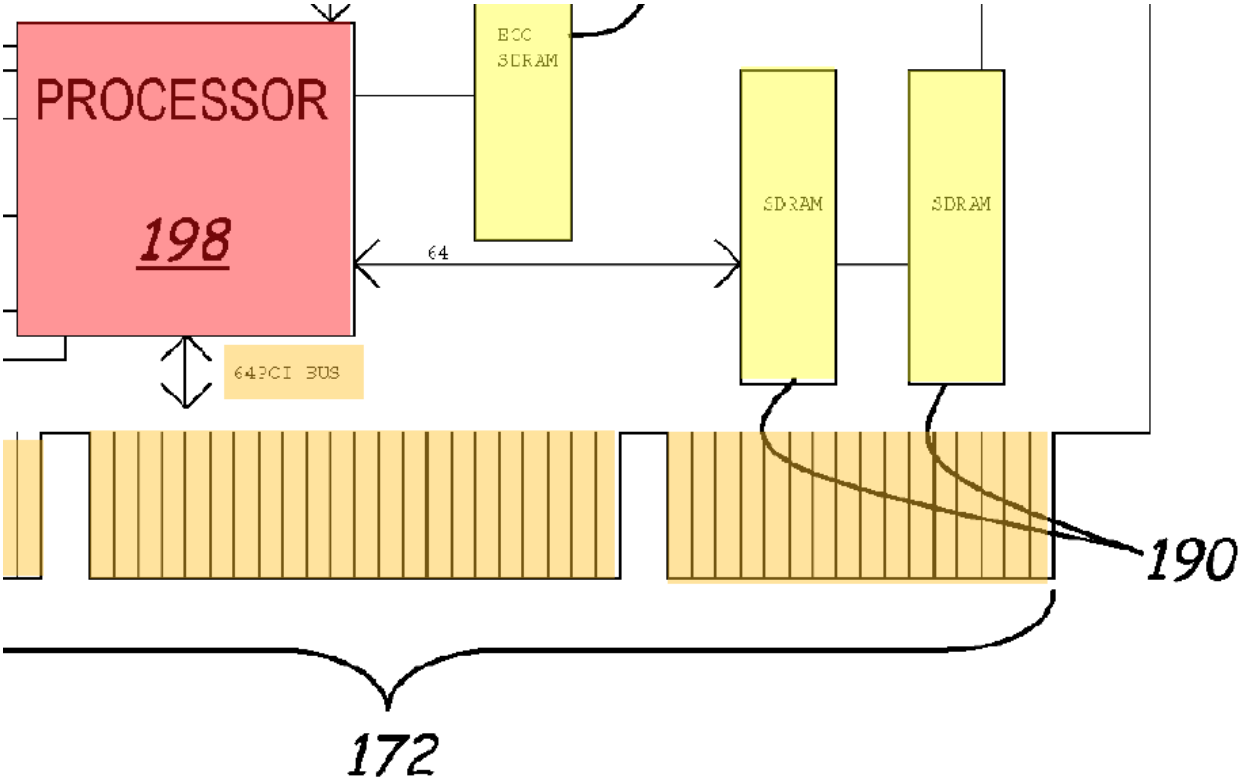
680. A Skilled Artisan would have recognized that DRAM devices, at the time, required two supply voltages which are less than 5 volts. *See, e.g.*, Ex. 1047 at 2:7-15 ("In a number of situations, it may be necessary to provide one or more operating voltages that are different from the available supply voltage on a single card. In at least one application, such as a dual-data-rate (DDR) memory system

employing DDR random access memories (DRAMs), two supply voltages are required. Typically, a second supply voltage will be a prescribed fraction (e.g., one-half) of a first supply voltage, and generally may not exceed the first supply voltage."). For example, "a regulated voltage to a DDR DRAM, output voltage Vout2 may provide a VTT supply voltage to the DRAM." *Id*. at 5:56-59

681. A Skilled Artisan would have also recognized that VTT is a termination voltage whose value is half of VDD/VDDQ (and the same voltage as a reference voltage, VREF) and that VTT is required for the proper operation of the SDRAM devices. *See, e.g.*, Ex. 1045 at pp. 8, 54, 60 ("VTT is a system supply for signal termination resistors, is expected to be set equal to VREF and must track variations in the dc level of VREF."); Ex. 1026 at pp. 9, 49 (similar); Ex. 1046 at p.15 (similar)

682. Furthermore, a Skilled Artisan would have understood that the processor 198 of Spiers's module, similar to an AMB in a fully buffered memory module (FBDIMM), buffers address, command, and data signals for the SDRAM devices. ¶¶652-653. For example, Spiers discloses that processor 198 (red) receives read and write commands with corresponding address and data signals on a 64-bit PCI bus interface 172, buffers those in a FIFO, decodes the commands, and performs the corresponding read and write operations into the SDRAM devices on the SDRAM interface. Ex. 1025 (Spiers) at Fig. 5 (reproduced below in

part, showing 64 bits of data to/from processor 198 and then to/from SDRAM 190).



See also id. at Fig. 9 (reproduced below and annotated) (showing the process of Spiers's processor 198 receiving read and write commands from the storage controller on a PCI bus and, in response, reading or writing corresponding data from and to SDRAMs 190 and 218 on an SDRAM bus), [0037] ("A FPGA processor 198 that provides PCI interfacing through a 64-bit PCI bus, is connected to the SDRAM modules 190 through a 64-bit bus, and is connected to the NAND flash modules 194 through a 32-bit bus."), [0046] ("At block 464 is it determined if the command code indicates that the source of the data is the host and the

destination of the data is the SDRAM. If so, the processor performs the operational steps for transferring data from the host memory to the SDRAM, as indicated at block 468.").

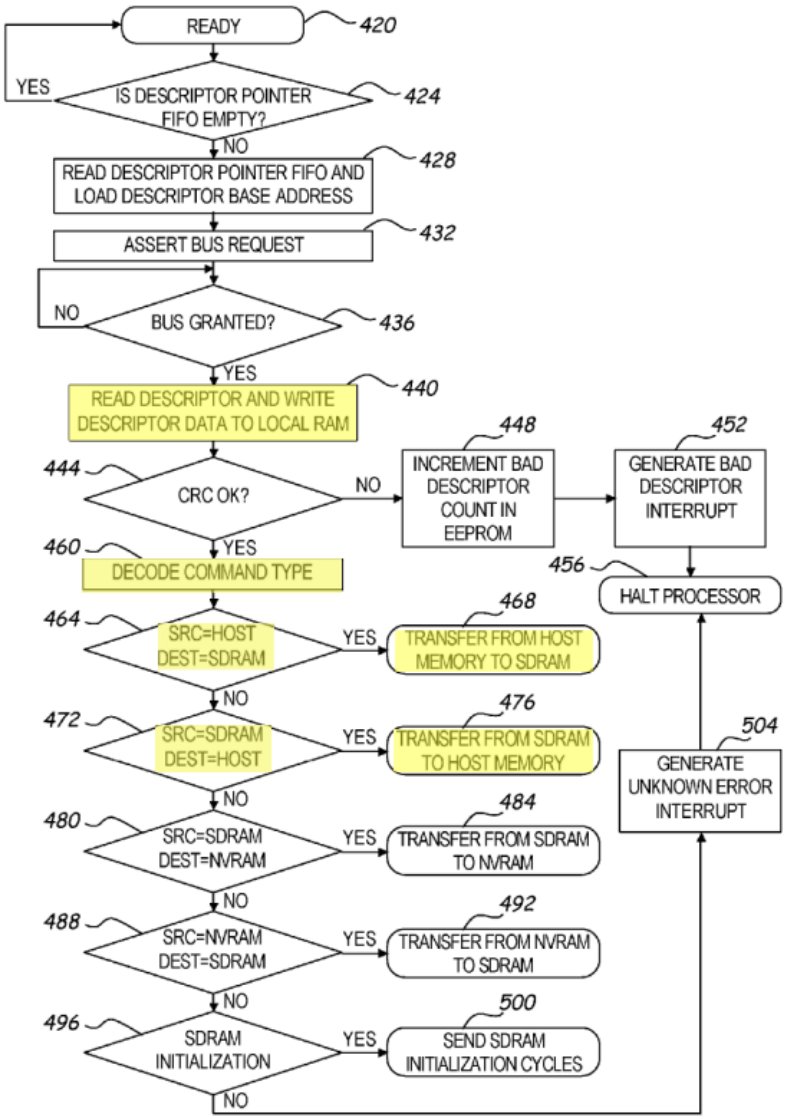
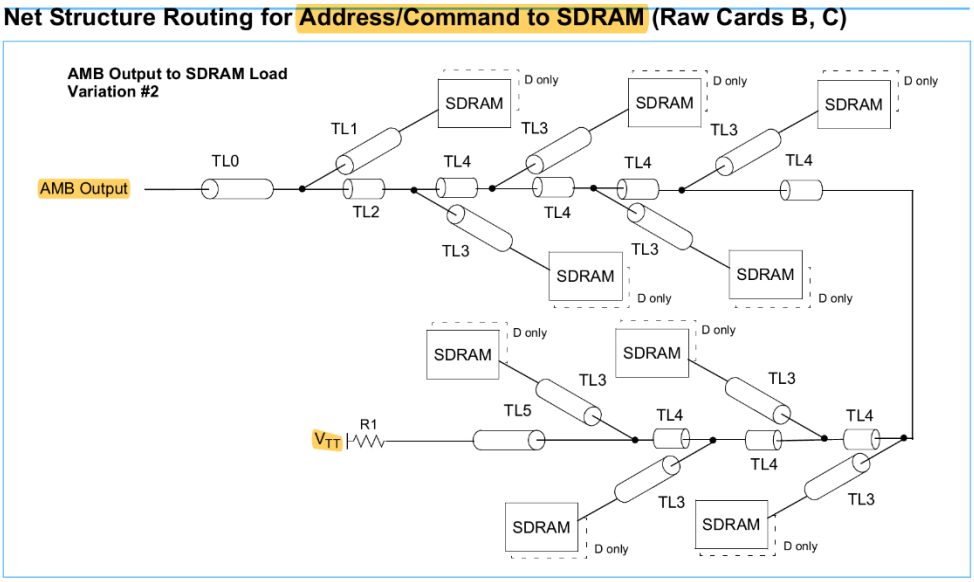


FIG.9

683. Therefore, a Skilled Artisan would have recognized that, in order to read and write the data from and to the SDRAMs, those SDRAM devices require

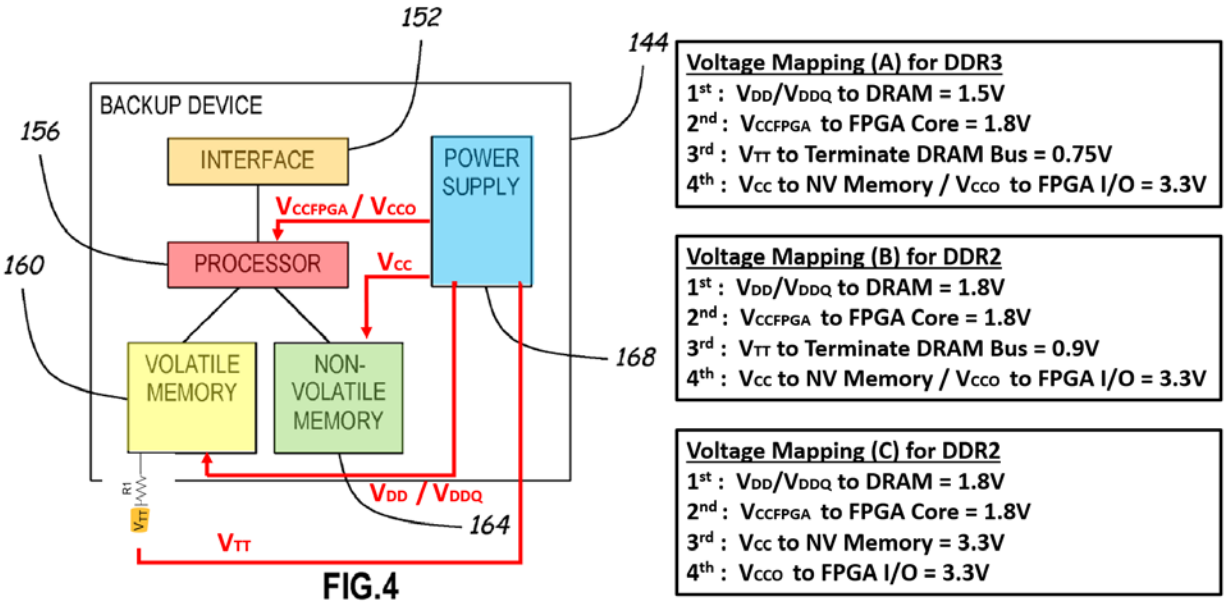
proper termination voltages VTT. *See*, *e.g.*, Ex. 1046 (JESD79-3A) at 10 (disclosing VDD/VDDQ=1.5V for DDR3 devices), 15 (disclosing how to turn on supply voltages, including VTT), 109 (disclosing that VTT=VDDQ/2); Ex 1026 (JESD79-2B) at 6-7 (disclosing VDD/VDDQ/VDDL=1.8V for DDR2 devices), 9 (disclosing how to turn on supply voltages, including VTT), 49 (disclosing tolerances, including for VTT), 55 and 71 (disclosing that VTT=VDDQ/2). A Skilled Artisan would have also understood how to apply this VTT termination voltage on a memory module. *See*, *e.g.*, Ex. 1028 at 68 (reproduced below in part, annotated).



684. Thus, as reflected in Voltage Mappings A and B of Grounds 4 and 5 (below), a Skilled Artisan would have understood that, in order to properly terminate the clock, address, command and control signals, the module of Spiers includes "*a third buck converter configured to provide a third regulated voltage*"

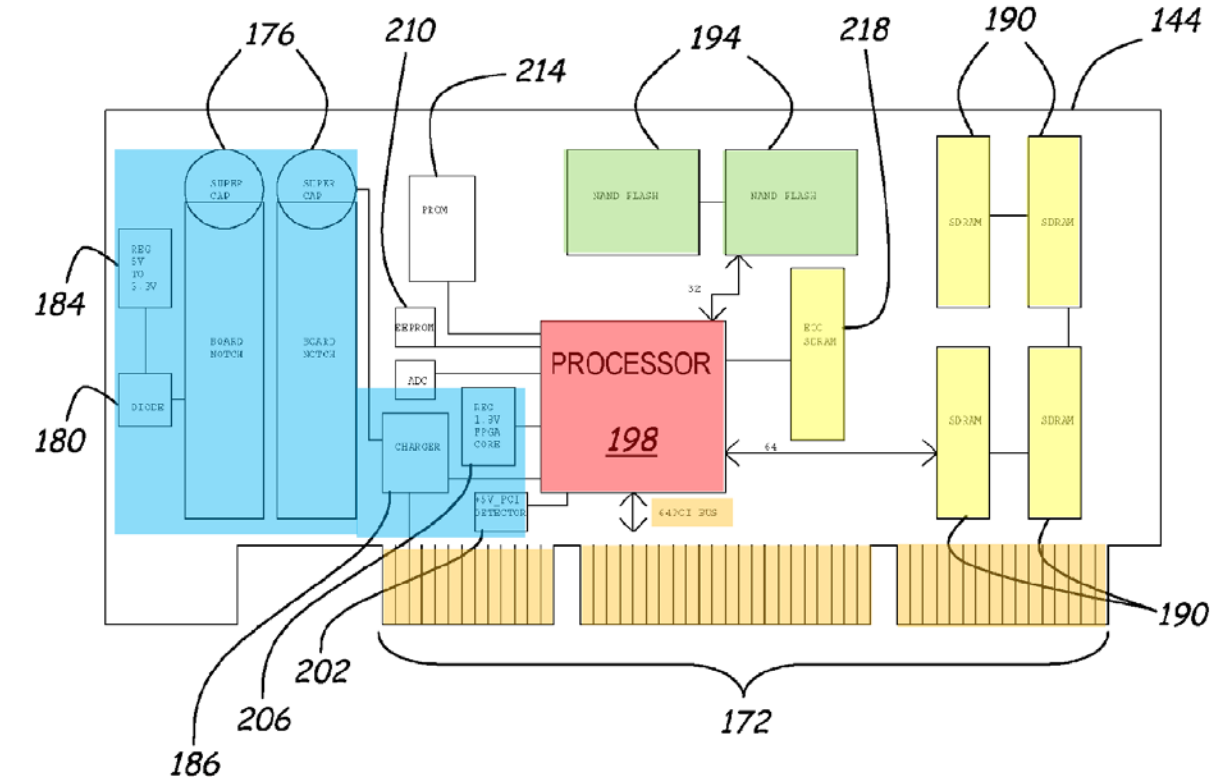
VTT which has "*a third voltage amplitude*," e.g., 0.75V for DDR3 (Voltage Mapping A) and 0.9V for DDR2 (Voltage Mapping B) DRAMs.

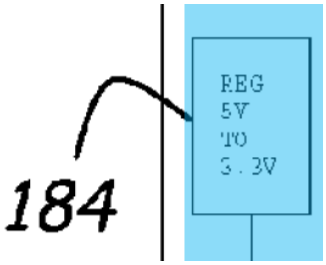
Ground 4: Spiers in view of Amidi, with DDR2 or DDR3 DRAMs



Ex. 1025 at Fig. 4 (annotated).

685. With regards to Voltage Mapping C of Grounds 4 and 5, Spiers discloses to a Skilled Artisan that a converter, such as voltage regulator 184 or another, similar voltage converter, is configured to step down a 5 volt input supply to a 3.3 volt output supply (e.g., VCC) to be provided to the non-volatile memories 194. Ex. 1025 at Fig. 5 (reproduced below and annotated).





686. In particular, Spiers discloses to a Skilled Artisan that parts of its module are powered by 3.3 volts, as evidenced by a voltage regulator 184 that provides a 3.3-volt backup voltage. With regards to the backup voltage, Spiers explained that "the capacitors 176 are connected to a diode 180[,] a voltage regulator 184, and a charger 186. The charger 186 is utilized to charge the capacitors 176, and in the event of a power failure the capacitors are used as the power source to power the backup device 144 when moving data from the volatile

memory **to the non-volatile memory**." Ex. 1025 at [0037] (emphasis added). A Skilled Artisan would have understood that some NAND Flash memory devices (194, green in the above figure) also use a power supply voltage of 3.3 volts at the time. *See, e.g.*, Ex. 1049 (NAND Flash Memory datasheet) at 1 ("VCC: 2.7V–3.6V"), 38 (recommending a VCC supply voltage of 3.3 volts, reproduced below in part and annotated).

Table 12: Recommended Operating Conditions

Parameter/Condition		Symbol	Min	Typ	Max	Unit
Operating temperature	Commercial	^{t}A	0	–	+70	°C
	Extended	^{t}A	–40	–	+85	°C
Vcc supply voltage		Vcc	2.7	3.3	3.6	V
Supply voltage		Vss	0	0	0	V

687. Thus, as reflected in Voltage Mapping C of Grounds 4 and 5 (above), a Skilled Artisan would have understood that, to properly operate the non-volatile memory, such as NAND Flash memory devices, the module in Spiers includes "*a third buck converter configured to provide a third regulated voltage*" VCC which has "*a third voltage amplitude*," e.g., 3.3V for the NAND Flash memory devices (Voltage Mapping C).

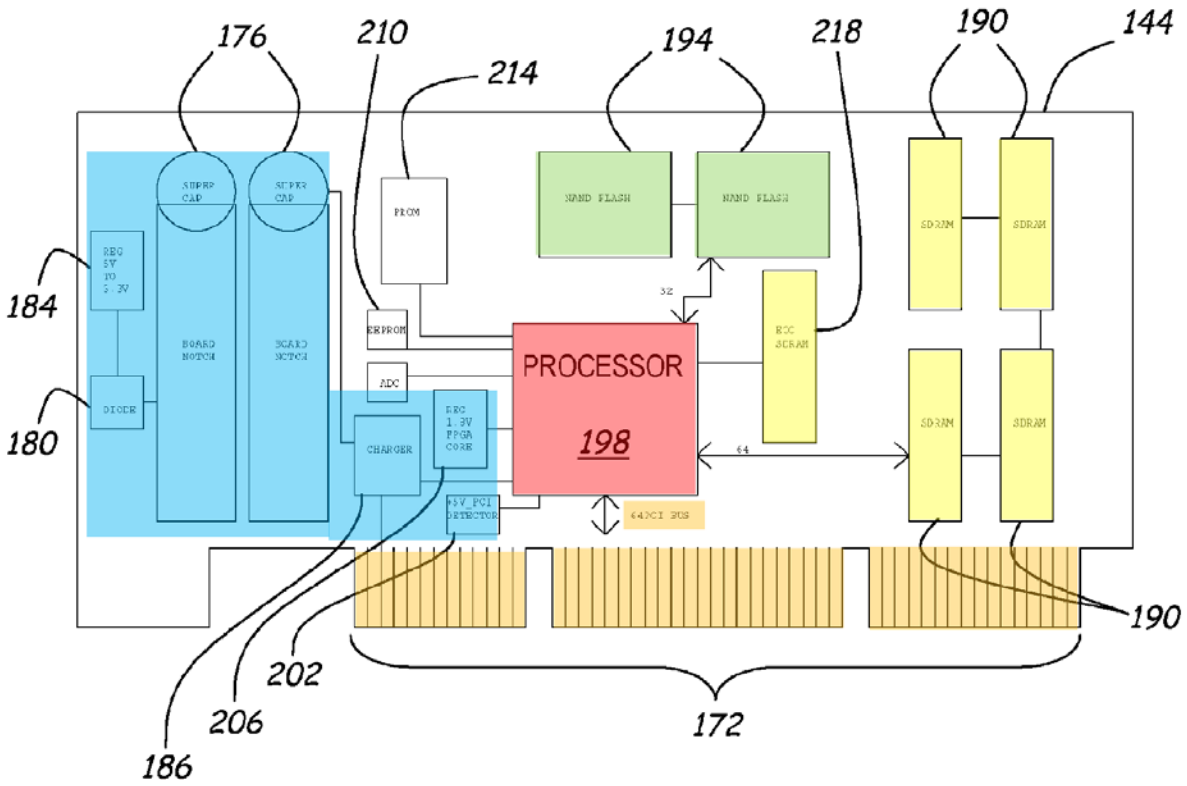
688. Accordingly, the prior art references in each of Grounds 4 and 5 satisfy "*a third buck converter configured to provide a third regulated voltage having a third voltage amplitude.*"

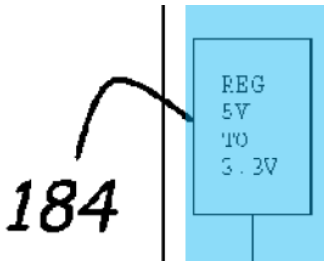
f) [1.f] A Converter Circuit

689. Claim 1 requires "*a converter circuit configured to provide a fourth regulated voltage having a fourth voltage amplitude.*"

690. The prior art references in each of Grounds 4 and 5 teach this limitation to a Skilled Artisan.

691. Spiers discloses to a Skilled Artisan a converter circuit, such as voltage regulator 184 or another, similar voltage converter, is configured to provide a fourth regulated voltage, for example VCC, of 3.3 volts for the processor 198 and/or the non-volatile memories 194. Ex. 1025 at Fig. 5 (reproduced below and annotated).





692. In particular, Spiers discloses to a Skilled Artisan that parts of its module are powered by 3.3 volts, as evidenced by a voltage regulator 184 that provides a 3.3-volt backup voltage. With regards to the backup voltage, Spiers explained that "the capacitors 176 are connected to a diode 180[,] a voltage regulator 184, and a charger 186. The charger 186 is utilized to charge the capacitors 176, and in the event of a power failure the capacitors are used as the power source to power the backup device 144 when moving data from the volatile memory to the non-volatile memory." Ex. 1025 at [0037].

693. Furthermore, as discussed above, a Skilled Artisan would have understood that Spiers uses the 5-volt power source from the PCI connector because its PCI detector 202 monitors a +5V pin to detect a power outage. *Supra* ¶¶655-666; Ex. 1025 at [0037] ("The FPGA processor 198 utilizes a power detection circuit that, in this embodiment, is a +5V PCI detector 202."). A Skilled Artisan would have also understood that, as disclosed by Spiers, the PCI standard allows the card (*e.g.*, backup device 144, "*memory module*") to use the 5-volt power source for all its power. Ex. 1031 at p.150 ("The expansion board may optionally draw all this power from either the +5V or +3.3V rail.").

694. To the extent one might argue that Spiers does not disclose using the 5-volt power source for all its power, it would have been obvious to a Skilled Artisan. For example, Spiers discloses using a +5V PCI detector to monitor a +5 volt rail of the PCI bus, Ex. 1025 at [0037], and a Skilled Artisan would have understood that all power can be drawn from this +5 volt rail, Ex. 1031 at p.150. Therefore, Spiers's express disclosure suggests to a Skilled Artisan to use the +5 volt rail for all of its power. A Skilled Artisan would have also understood and would have been motivated to use only the higher voltage source (5 volts) and convert that higher voltage locally on the board, because doing so would require smaller currents than receiving the same power on lower voltage rail. Furthermore, using the higher voltage source only would allow mixing and upgrading different technologies requiring different voltage levels. *See, e.g.*, Ex. 1023 at [0011] ("Those skilled in the art should recognize upon reference hereto that by providing a tightly-controlled VRM as local voltage supply for on-board power requirements, a number of advantages may be obtained in the power supply design of an electronic component such as the memory module 100A. Since the Vdd and Vcc power supply rails are rendered independent from external voltage sources, the overall power supply interface to the memory module 100A is improved to better support large memory capacity scaling, hot-pluggability, DRAM technology independence (e.g., DDR2, DDR3, DDR4, and other DRAM

types), high DRAM device count (i.e., amenable to multi-ranking), as well as provide improved system-level cost sharing. Additionally, memory performance is also improved because of tighter voltage regulation.").

695. For example, a Skilled Artisan would have understood that Spiers's module uses a power converter which draws power from the +5 volt rail and converts that +5V down to 3.3 volts, similar to voltage regulator 184 which converts +5V down to 3.3V. A Skilled Artisan would have also understood that such a regulated 3.3V is provided to the processor 198, since FPGAs at the time used a 3.3V supply for VCCO, as discussed above with reference to claim limitation [1.d]. *Supra* ¶¶668-676. A Skilled Artisan would have also understood that the specific VCCO voltage value of 3.3 volts is just one example in a range of possibilities and that different FPGAs had different voltage requirements. *See, e.g.*, Ex. 1042 at 2 (reproduced below, in part, showing different FPGAs and their power requirements). Therefore, using the +5V rail and a down converter provides flexibility in selecting the VCCO value.

	Spartan™-3/3E/3L	Spartan™-IIE	Spartan™-II	Virtex™-5	Virtex™-4	Virtex-II Pro™	Virtex™-II
V_{CCINT}	1.2V @0.2A-5A	1.8V @0.2A-1.5A	2.5V @0.2A-1A	1.0V @0.2A-15A	1.2V @0.2A-20A	1.5V @0.2A-20A	1.5V @0.2A-20A
V_{CCO}	1.2V-3.3V @50mA-3A	1.5V-3.3V @50mA-0.5A	1.5V-3.3V @50mA-0.5A	1.2V-3.3V @50mA-5A	1.2V-3.3V @50mA-3A	1.5V-3.3V @50mA-3A	1.5V-3.3V @50mA-3A
V_{CCAUX}	2.5V @50mA-0.3A	–	–	2.5V @50mA-0.7A	2.5V @50mA-0.7A	2.5V @50mA-0.3A	3.3V @50mA-0.3A

Indeed, as explained above for claim limitation [1.d], a Skilled Artisan would have understood that FPGA devices operate at voltages within a known range. *Supra*

¶673. Further, a Skilled Artisan would have understood that it would have been an obvious design choice to select one or more FPGAs, and it was at least obvious to try an FPGA with a VCCO supply at 3.3 volts or some other values in that range, such as Spartan or Virtex FPGAs. *See id.*; *see also, e.g.*, Ex. 1042 at 2 (reproduced above).

696. As reflected in Voltage Mappings A and B of Grounds 4 and 5 (below), a Skilled Artisan would also have understood that some NAND Flash memory devices (194, green in the above figure) also use a power supply voltage of 3.3 volts at the time. *See*, *e.g.*, Ex. 1049 at 1 ("VCC: 2.7V–3.6V"), 38 (recommending a VCC supply voltage of 3.3 volts, reproduced below in part and annotated).

Table 12: Recommended Operating Conditions

Parameter/Condition		Symbol	Min	Typ	Max	Unit
Operating temperature	Commercial	^{t}A	0	–	+70	°C
	Extended	^{t}A	–40	–	+85	°C
Vcc supply voltage		Vcc	2.7	3.3	3.6	V
Supply voltage		Vss	0	0	0	V

697. A Skilled Artisan would have further understood that the 3.3-volt supply voltage is provided to both the processor (198, annotated in red in Figure 5 of Spiers above) and the Flash memories (194, green) when the processor transfers the data from the SDRAMs (190, yellow) to the Flash memories.

698. Thus, as reflected in Voltage Mappings A and B of Grounds 4 and 5 (below), a Skilled Artisan would have understood that Spiers includes a converter,

such as voltage regulator 184 or another, similar voltage converter, that converts input supply voltage (e.g., 5 volts) down to 3.3 volts ("*a converter circuit configured to provide a fourth regulated voltage having a fourth voltage amplitude*") for the processor 198 and/or the non-volatile memories 194.

Ground 4: Spiers in view of Amidi, with DDR2 or DDR3 DRAMs

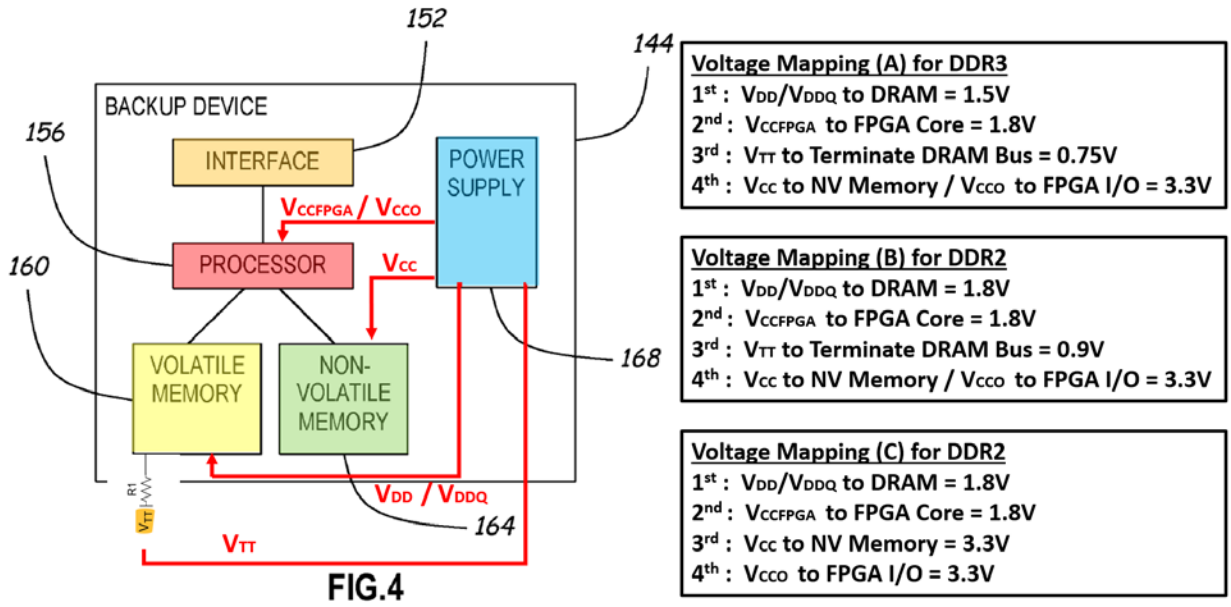


FIG.4

Ex. 1025 at Fig. 4 (annotated).

699. Further, as reflected in Voltage Mapping C of Grounds 4 and 5 (above), a Skilled Artisan would have understood that Spiers includes a converter that is separate from the third buck converter, such as voltage regulator 184 or another, similar voltage converter, that converts input supply voltage (e.g., 5 volts) down to 3.3 volts ("*a converter circuit configured to provide a fourth regulated voltage having a fourth voltage amplitude*") for the processor 198.

700. Accordingly, the prior art references in each of Grounds 4 and 5 satisfy "*a converter circuit configured to provide a fourth regulated voltage having a fourth voltage amplitude*."

g) [1.g] A Plurality of Components Coupled to the PCB

701. Claim 1 requires "*a plurality of components coupled to the PCB, each component of the plurality of components coupled to one or more regulated voltages of the first, second, third and fourth regulated voltages, the plurality of components comprising.*"

702. The prior art references in each of Grounds 4 and 5 teach this limitation to a Skilled Artisan.

703. As explained above for claim limitation [1.b], Spiers discloses to a Skilled Artisan using "*a printed circuit board (PCB)*" to implement a memory module. *Supra* ¶647-654.

704. For the reasons discussed above with reference to claim elements [1.c], [1.d], [1.e], and [1.f], Spiers also discloses to a Skilled Artisan that "*each component of the plurality of components [is] coupled to one or more regulated voltages of the first, second, third and fourth regulated voltages*."

705. For example, in Grounds 4 and 5, the DRAM devices in the Volatile Memory 160 are coupled to VDD/VDDQ, Processor 156 is coupled to VCCFPGA and VCCO, and Flash memory devices in Non-Volatile Memory 164 are coupled

to VCC. For the reasons discussed above with reference to the Harris-based combinations, the DDR SDRAM devices also required a regulated voltage VTT which is coupled to termination resistors RTT and, through those resistors, to the SDRAMs and the Processor controlling the SDRAMs.

Ground 4: Spiers in view of Amidi, with DDR2 or DDR3 DRAMs

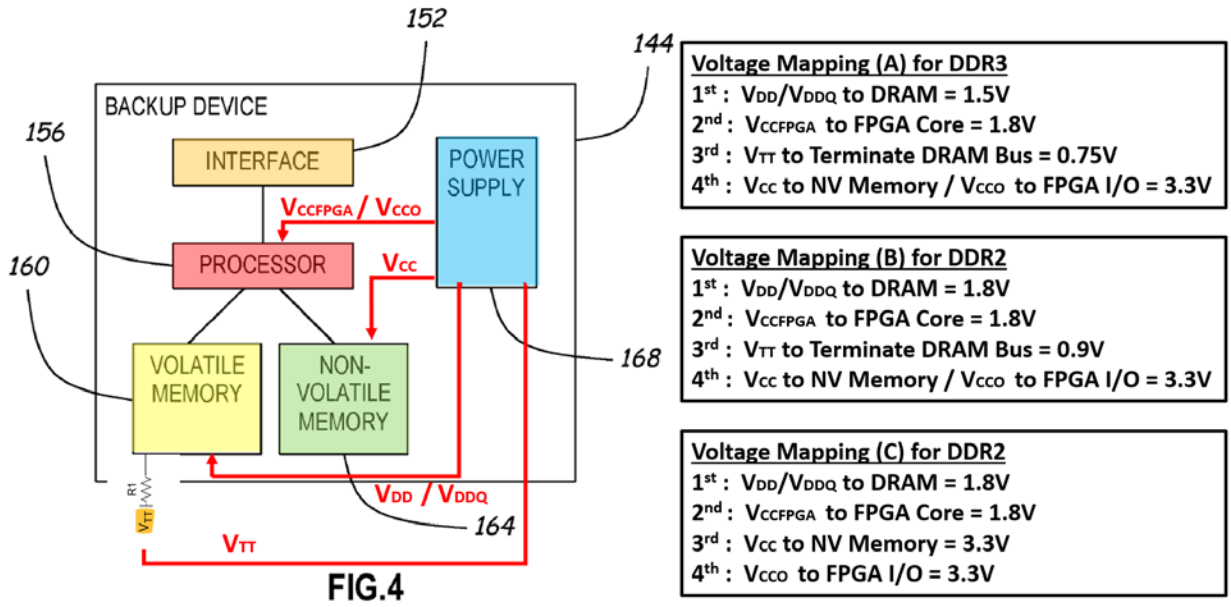


FIG.4

706. As explained above for claim limitation [1.c], Spiers in view of Amidi satisfies "*a first buck converter configured to provide a first regulated voltage having a first voltage amplitude*." *Supra* ¶¶655-666. As previously discussed, the prior art references in each of Grounds 4 and 5 disclose to a Skilled Artisan using a "*first buck converter*" to provide a "*first regulated voltage*" to the SDRAM devices, e.g., VDD/VDDQ of 1.5V (e.g. for DDR3 SDRAM devices) (Grounds 4 and 5, Mapping A), VDD/VDDQ of 1.8V (e.g., DDR2 SDRAM devices) (Grounds 4 and 5, Mappings B and C). *See id.*

707. In addition, Spiers in view of Amidi satisfies "*a second buck converter configured to provide a second regulated voltage having a second voltage amplitude*." *Supra* ¶¶668-676. As explained, a Skilled Artisan would understand the voltage regulator 206 includes a "*second buck converter*" that provides a supply voltage to processor 198, e.g., VCCFPGA of 1.8V (Grounds 4 and 5, Mappings A through C). *See id.*

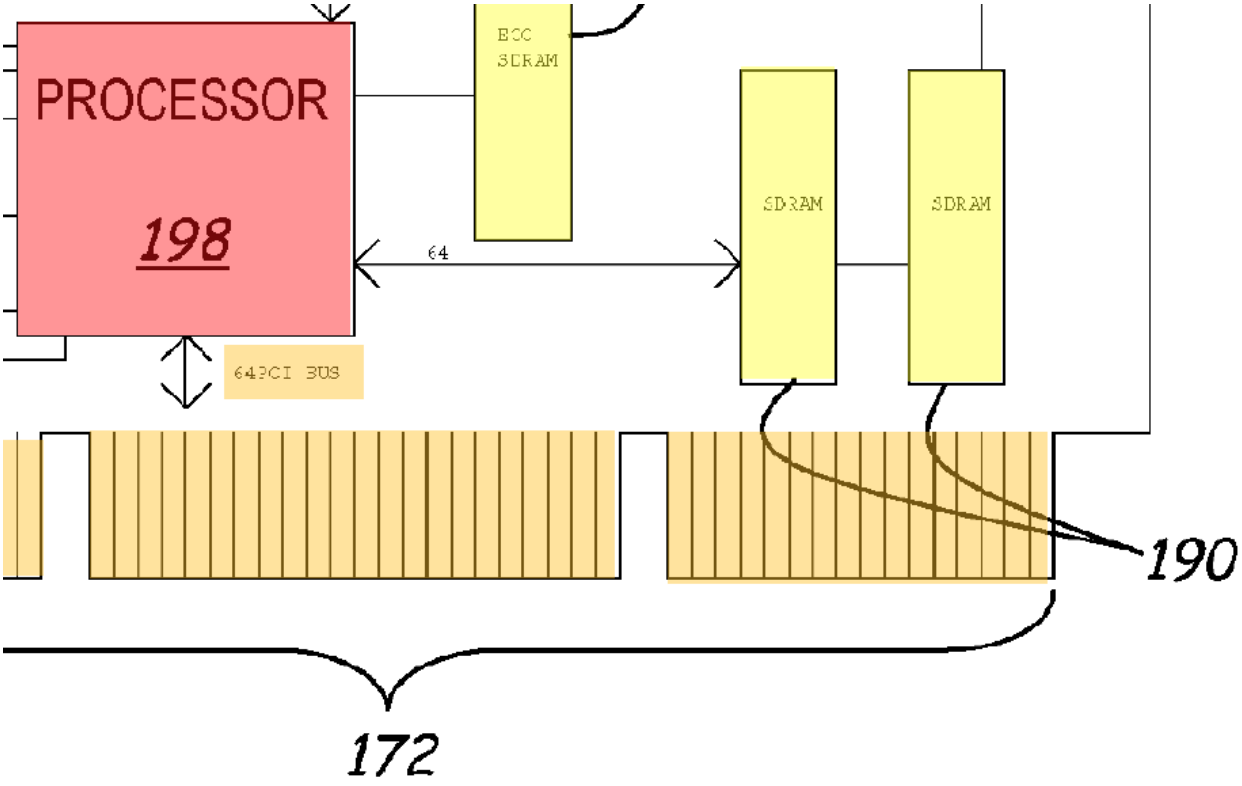
708. Further, Spiers in view of Amidi satisfy "*a third buck converter configured to provide a third regulated voltage having a third voltage amplitude*." *Supra* ¶¶677-687. As explained, the prior art references in each of Grounds 4 and 5 disclose to a Skilled Artisan a "*third buck converter*" to convert power from a 5-volt supply of the PCI card to provide a "*third regulated voltage*" to the SDRAM devices, e.g., VTT of 0.75V for DDR3 (Grounds 4 and 5, Mapping A), VTT of 0.9V for DDR2 (Grounds 4 and 5, Mapping B), VCC of 3.3V for NV Memory (Grounds 4 and 5, Mapping C). *See id.* Regarding voltage supply VTT, a Skilled Artisan would have recognized that DRAM devices, at the time, required two supply voltages which are less than 5 volts. *See, e.g.*, Ex. 1046 (JESD79-3A) at 10 (disclosing VDD/VDDQ=1.5V for DDR3 devices), 15 (disclosing how to turn on supply voltages, including VTT), 109 (disclosing that VTT=VDDQ/2); Ex 1026 (JESD79-2B) at 6-7 (disclosing VDD/VDDQ/VDDL=1.8V for DDR2 devices), 9 (disclosing how to turn on supply voltages, including VTT), 49 (disclosing

tolerances, including for VTT), 55 and 71 (disclosing that VTT=VDDQ/2); *see also* Ex. 1047 at 2:7-15 ("In a number of situations, it may be necessary to provide one or more operating voltages that are different from the available supply voltage on a single card. In at least one application, such as a dual-data-rate (DDR) memory system employing DDR random access memories (DRAMs), two supply voltages are required. Typically, a second supply voltage will be a prescribed fraction (e.g., one-half) of a first supply voltage, and generally may not exceed the first supply voltage."). For example, "a regulated voltage to a DDR DRAM, output voltage Vout2 may provide a VTT supply voltage to the DRAM." *Id*. at 5:56-59.

709. A Skilled Artisan would have also recognized that VTT is a termination voltage whose value is half of VDD/VDDQ (and the same voltage as a reference voltage, VREF) and that VTT is required for the proper operation of the DRAM devices, including DDR2, DDR3, and DDR4 DRAMs. *See, e.g.*, Ex. 1045 at pp. 8, 54, 60 ("VTT is a system supply for signal termination resistors, is expected to be set equal to VREF and must track variations in the dc level of VREF."); Ex. 1026 at pp. 9, 49 (similar); Ex. 1046 at p.15 (similar).

710. Furthermore, a Skilled Artisan would have understood that the processor 198 of Spiers's module, similar to an AMB in a fully buffered memory module (FBDIMM), buffers address, command, and data signals for the SDRAM devices. *Supra* at ¶652. For example, Spiers discloses that processor 198 (red)

receives read and write commands with corresponding address and data signals on a 64-bit PCI bus interface 172, buffers those in a FIFO, decodes the commands, and performs the corresponding read and write operations into the SDRAM devices on the SDRAM interface. Ex. 1025 (Spiers) at Fig. 5 (reproduced below in part, showing 64 bits of data to/from processor 198 and then to/from SDRAM 190).



See also id. at Fig. 9 (reproduced below and annotated) (showing the process of Spiers's processor 198 receiving read and write commands from the storage controller on a PCI bus and, in response, reading or writing corresponding data from and to SDRAMs 190 and 218 on an SDRAM bus), [0037] ("A FPGA

processor 198 that provides PCI interfacing through a 64-bit PCI bus, is connected to the SDRAM modules 190 through a 64-bit bus, and is connected to the NAND flash modules 194 through a 32-bit bus."), [0046] ("At block 464 is it determined if the command code indicates that the source of the data is the host and the destination of the data is the SDRAM. If so, the processor performs the operational steps for transferring data from the host memory to the SDRAM, as indicated at block 468.").

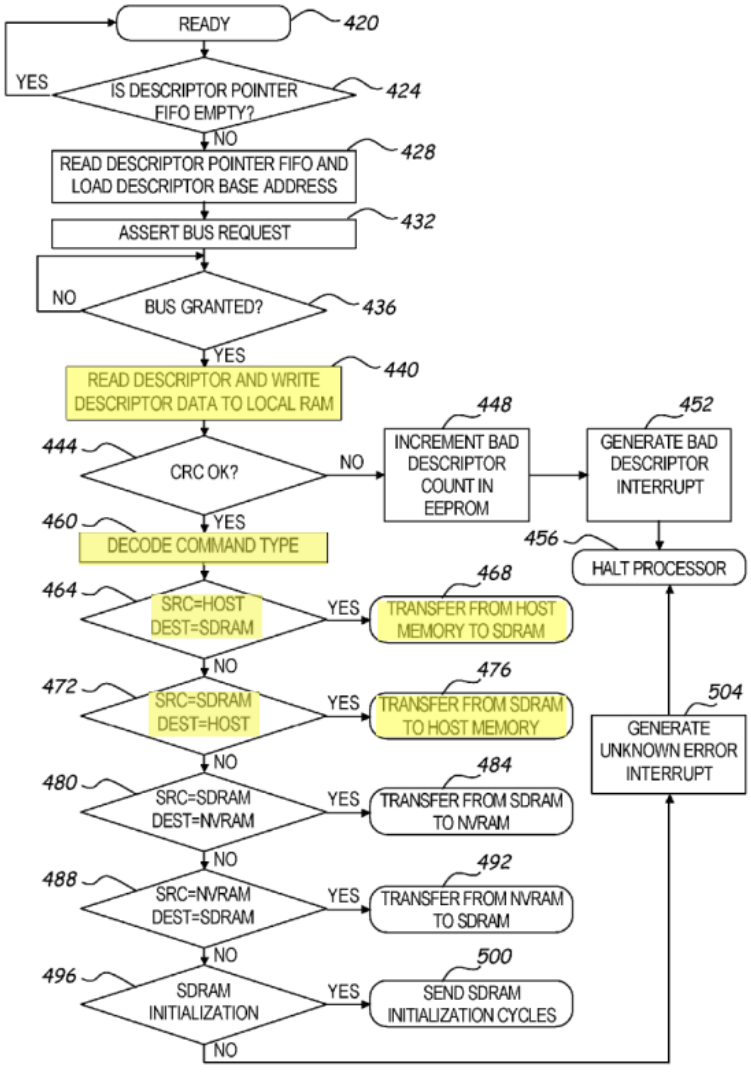
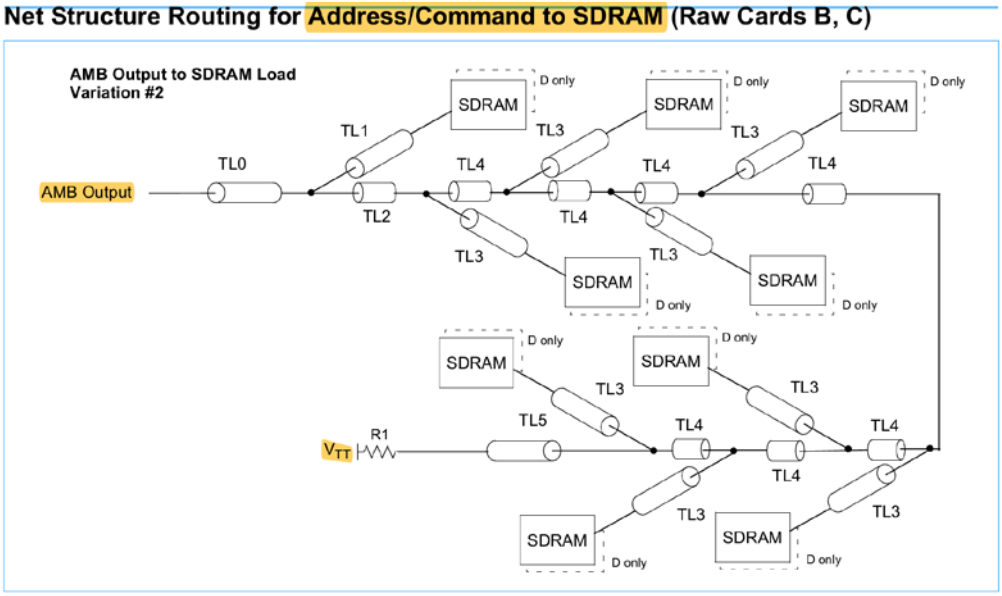


FIG.9

711. Therefore, a Skilled Artisan would have recognized that, in order to read and write the data from and to the SDRAMs, those SDRAM devices require proper termination voltages VTT. *See*, *e.g.*, Ex. 1046 (JESD79-3A) at 10 (disclosing VDD/VDDQ=1.5V for DDR3 devices), 15 (disclosing how to turn on supply voltages, including VTT), 109 (disclosing that VTT=VDDQ/2); Ex 1026 (JESD79-2B) at 6-7 (disclosing VDD/VDDQ/VDDL=1.8V for DDR2 devices), 9 (disclosing how to turn on supply voltages, including VTT), 49 (disclosing tolerances, including for VTT), 55 and 71 (disclosing that VTT=VDDQ/2). A Skilled Artisan would have also understood how to apply this VTT termination voltage on a memory module. *See*, *e.g.*, Ex. 1028 at 68 (reproduced below in part, annotated).



712. As explained above for claim limitation [1.f], Spiers in view of Amidi satisfy "*a converter circuit configured to provide a fourth regulated voltage having*

a fourth voltage amplitude." *Supra* ¶¶689-700. As explained, a converter, such as voltage regulator 184 or another, similar voltage converter, (i.e., a "*converter circuit*") converts input supply voltage (e.g., 5 volts) down to 3.3 volts (i.e., a "*fourth regulated voltage*") that is provided to the processor 198 and/or the non-volatile memories 194. *Id.*

713. Accordingly, the prior art references in each of Grounds 4 and 5 satisfy "*a plurality of components coupled to the PCB, each component of the plurality of components coupled to one or more regulated voltages of the first, second, third and fourth regulated voltages, the plurality of components comprising*."

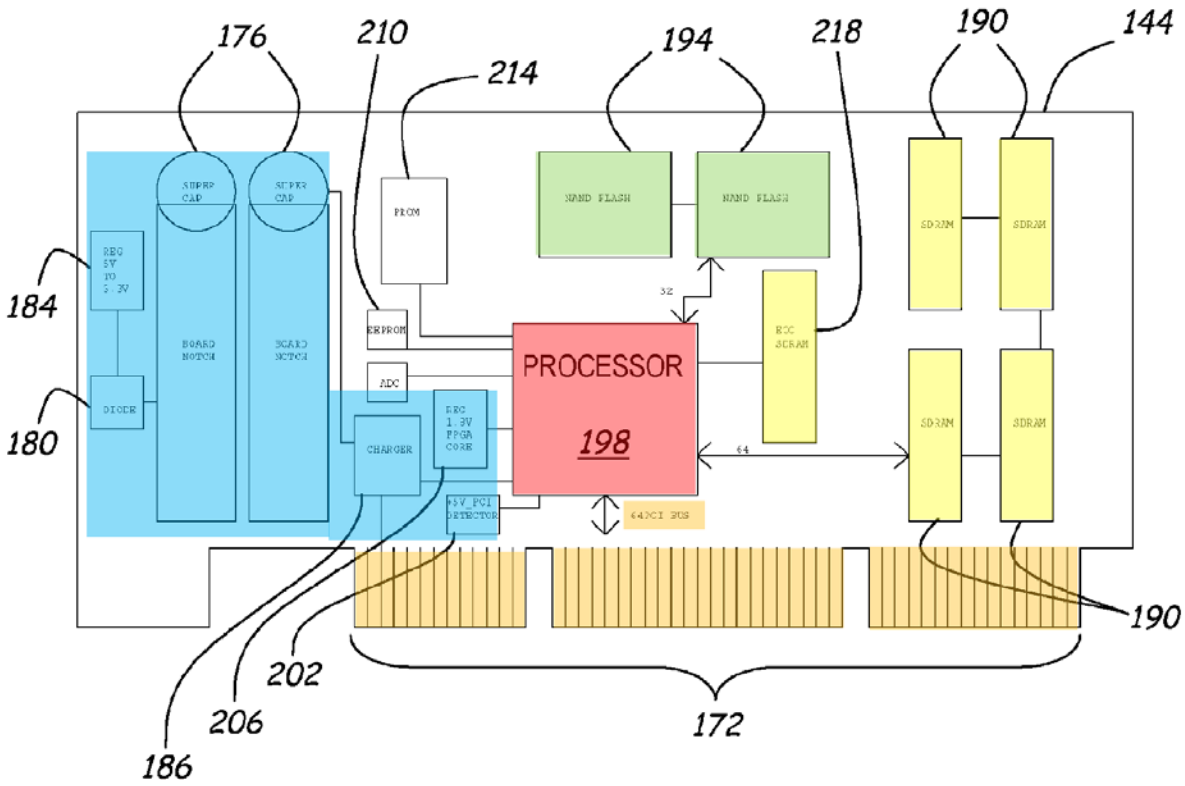
h) [1.h] A Plurality of SDRAM Devices

714. Claim 1 requires "*a plurality of synchronous dynamic random access memory (SDRAM) devices coupled to the first regulated voltage*."

715. The prior art references in each of Grounds 4 and 5 teach this limitation to a Skilled Artisan.

716. As discussed above for claim limitation [1.c], Spiers discloses "*a plurality of synchronous dynamic random access memory (SDRAM) devices*" (e.g., SDRAMs 190 and 218). *Supra* ¶¶655-666; *see also* Ex. 1025 at [0036] ("The volatile memory 160, in one embodiment, is SDRAM utilized to store data from

the storage controller 132 during typical write operations."), [0037-38] (describing SDRAMs 190 and 218 in Fig. 5), Fig. 5 (reproduced below and annotated).



717. As previously explained, for Voltage Mappings A through C of Grounds 4 and 5, these SDRAM devices are "coupled to the first regulated voltage" VDD/VDDQ. *Supra* ¶¶658-665.

718. Accordingly, the prior art references in each of Grounds 4 and 5 satisfy "*a plurality of synchronous dynamic random access memory (SDRAM) devices coupled to the first regulated voltage*."

i) [1.i] At Least One Circuit

(1) [1.i.1] Coupled between the edge connections and the SDRAM devices

719. Claim 1 requires "*at least one circuit coupled between a first portion of the plurality of edge connections and the plurality of SDRAM devices*."

720. The prior art references in each of Grounds 4 and 5 teach this limitation to a Skilled Artisan.

721. As discussed above for claim limitation [1.b], Spiers satisfies "*a printed circuit board (PCB) having an interface configured to fit into a corresponding slot connector of a host system, the interface including a plurality of edge connections configured to couple power, data, address and control signals between the memory module and the host system.*" *Supra* ¶¶ 647-654.

722. Spiers discloses processor 198 (i.e., "*at least one circuit*") that is coupled between a first portion of the plurality of edge connections in PCI connector 172 and the plurality of SDRAM devices 190 and 218. *See, e.g.*, Ex. 1025 at Fig. 5, [0037] ("A FPGA processor 198 that provides PCI interfacing through a 64-bit PCI bus, is connected to the SDRAM modules 190 through a 64-bit bus, and is connected to the NAND flash modules 194 through a 32-bit bus").

723. Accordingly, the prior art references in each of Grounds 4 and 5 satisfy "*at least one circuit coupled between a first portion of the plurality of edge connections and the plurality of SDRAM devices*."

(2) [1.i.2] Operable to receive/output address and control signals

724. Claim 1 requires "*the at least one circuit operable to (i) receive a first plurality of address and control signals via the first portion of the plurality of edge connections, and (ii) output a second plurality of address and control signals to the plurality of SDRAM devices*."

725. The prior art references in each of Grounds 4 and 5 teach this limitation to a Skilled Artisan.

726. As discussed, Spiers satisfies "*a printed circuit board (PCB) having an interface configured to fit into a corresponding slot connector of a host system, the interface including a plurality of edge connections configured to couple power, data, address and control signals between the memory module and the host system.*" *Supra* ¶¶647-654 (claim limitation [1.b]). Further, Spiers satisfies "*at least one circuit coupled between a first portion of the plurality of edge connections and the plurality of SDRAM devices*." *Supra* ¶¶719-723 (claim limitation [1.i.1]).

727. Spiers discloses to a Skilled Artisan that processor 198 is operable to "*receive a first plurality of address and control signals via the first portion of the plurality of edge connections*," and "*output a second plurality of address and control signals to the plurality of SDRAM devices*." *See, e.g.*, Ex. 1025 at [0037], Ex. 1031 at p.1 ("The PCI Local Bus is a high performance 32-bit or 64 bit bus

with multiplexed address and data lines"), p.7 (Fig. 2-1, reproduced below, describing PCI pins AD for address and data signals and pins C/BE for bus control signals).

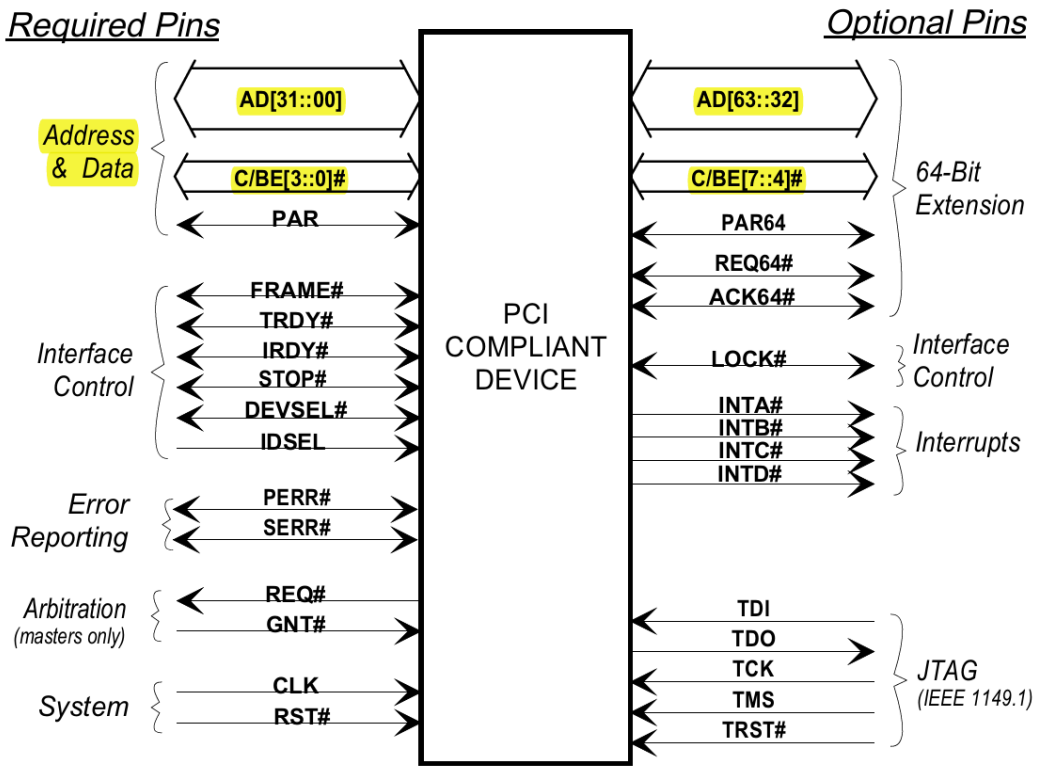


Figure 2-1: PCI Pin List

See also id. at p.21 (below, listing C/BE commands, including commands for read and write operations), pp.146-49 (pin assignments for "AD" and "C/BE"), p.172 (below, showing edge connections of 5V/64-bit PCI bus).

3.1.1. Command Definition

PCI bus command encodings and types are listed below, followed by a brief description of each. Note: The command encodings are as viewed on the bus where a "1" indicates a high voltage and "0" is a low voltage. Byte enables are asserted when "0".

C/BE[3::0]#	Command Type
0000	Interrupt Acknowledge
0001	Special Cycle
0010	I/O Read
0011	I/O Write
0100	Reserved
0101	Reserved
0110	Memory Read
0111	Memory Write
1000	Reserved
1001	Reserved
1010	Configuration Read
1011	Configuration Write
1100	Memory Read Multiple
1101	Dual Address Cycle
1110	Memory Read Line
1111	Memory Write and Invalidate

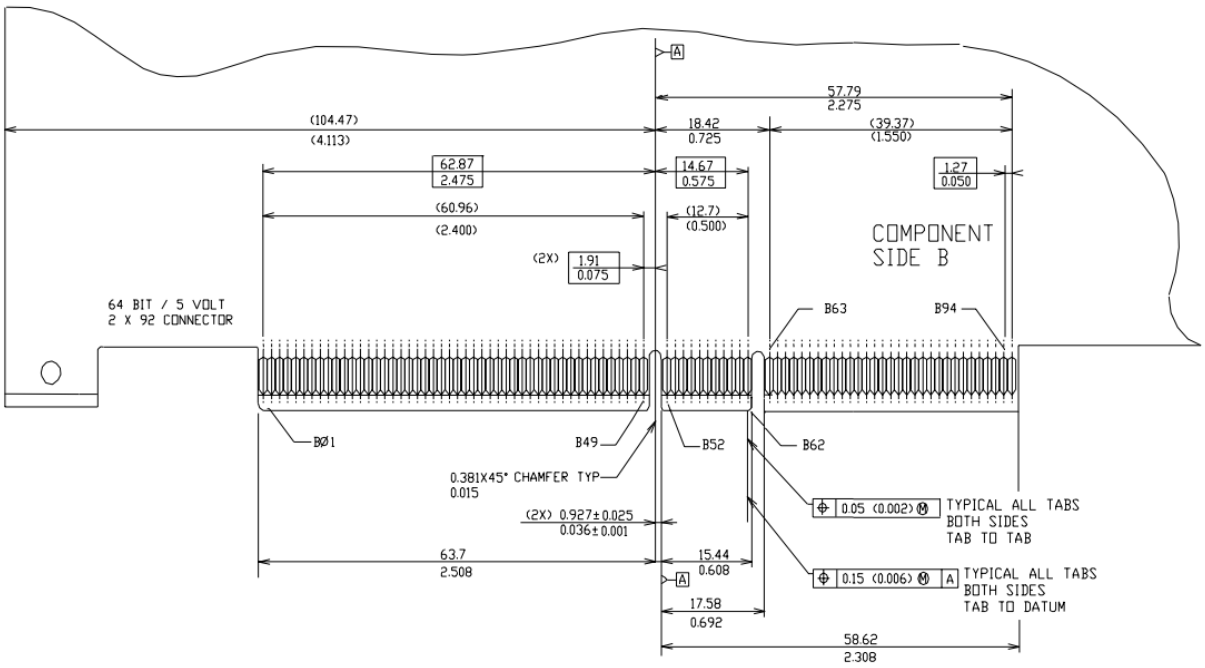
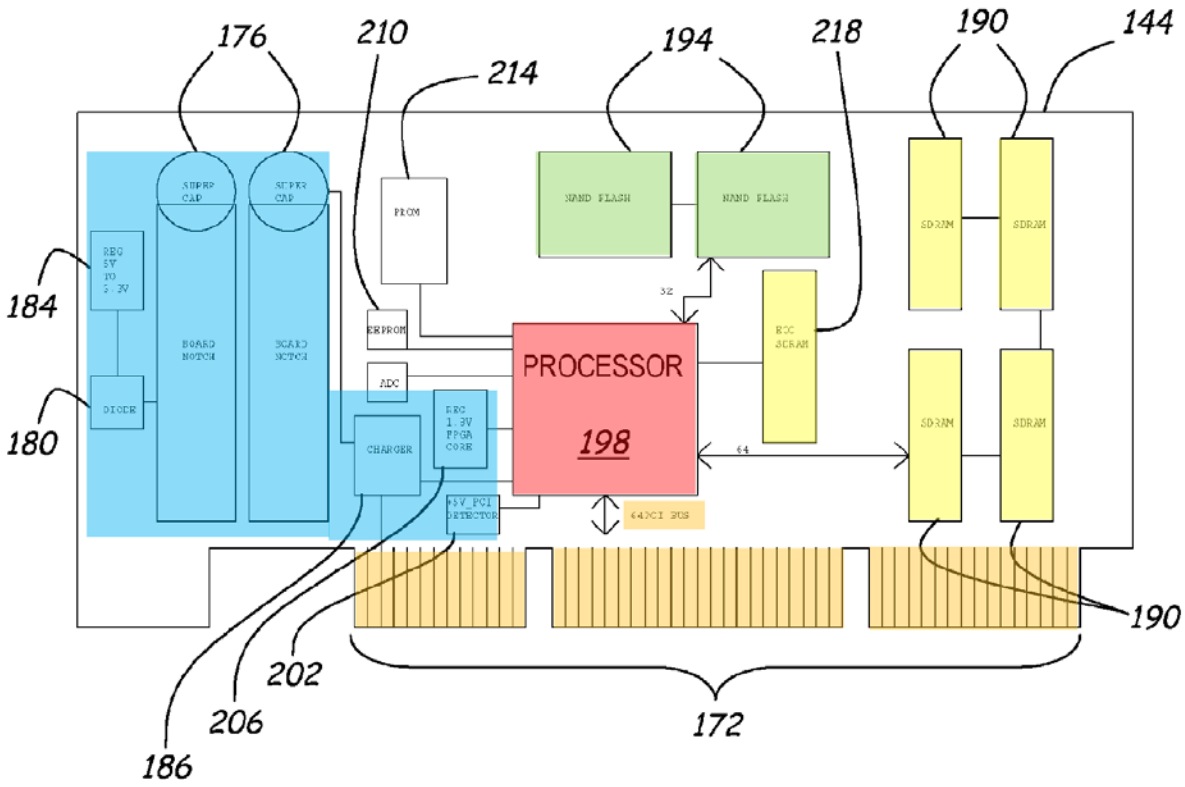


Figure 5-27: 5V/64-bit Card Edge Connector Dimensions and Tolerances

See also Ex. 1025 at Fig. 5 (reproduced below showing connection between processor 198 (red) and the 64-bit PCI connection 172, annotated)) and Fig. 9 (annotated).



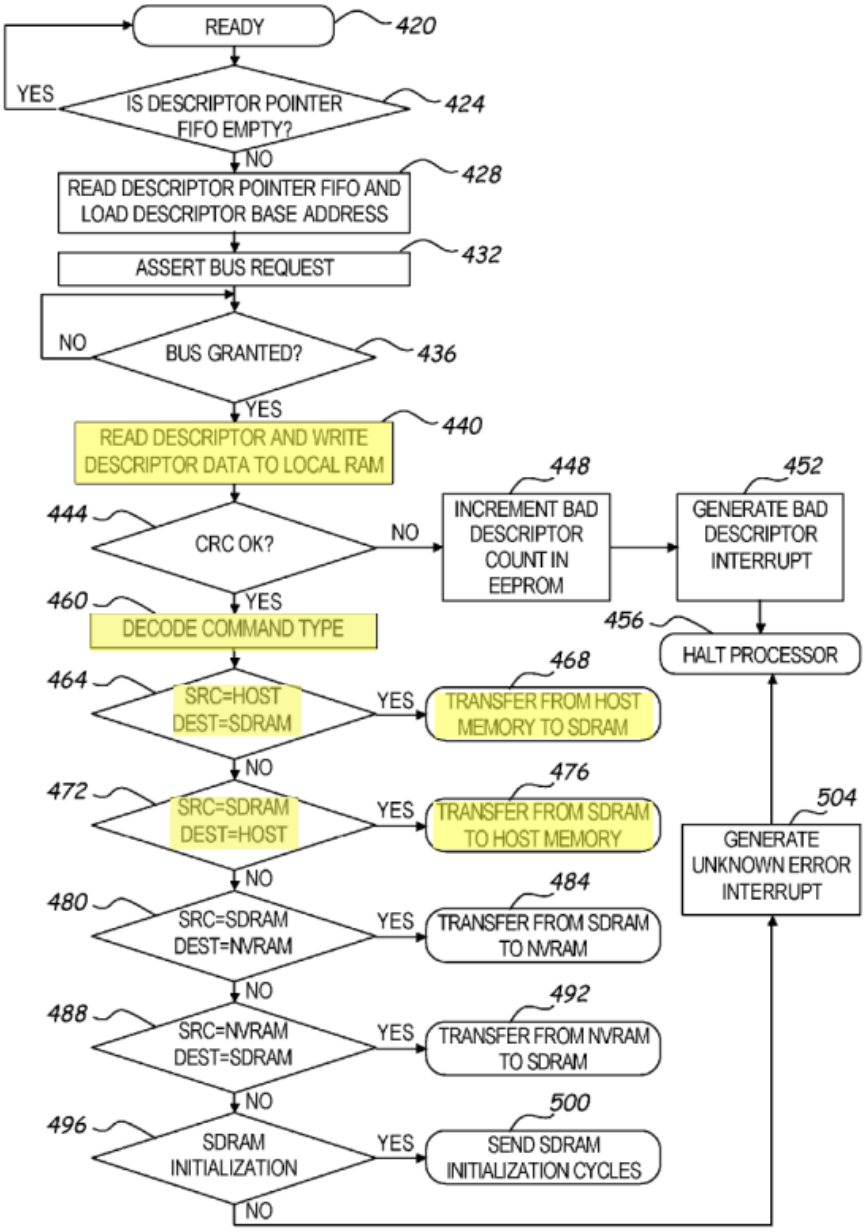


FIG.9

728. For example, Spiers discloses the backup device processor receiving read and write commands from the storage controller. *See* Ex. 1025 at [0039] ("In an embodiment, the backup device 144 utilizes a descriptor pointer queue contained within the FPGA processor 198 to receive commands from the storage controller. In this embodiment, the descriptor pointer queue is a FIFO queue that

receives pointers to descriptor chains that the FPGA processor 198 reads. The pointers, in an embodiment, are 64 bits in length, and contain commands for the processor to perform various functions."). Spiers further discloses the backup device processor reading and writing data from and to the SDRAM memory devices in response to these commands. *See* Ex. 1025 at [0044] ("As discussed previously, in one embodiment the backup device utilizes descriptors to receive commands from the storage controller. Descriptor pointers are placed in a FIFO and the PCI base address is read to obtain the descriptor. … If it is determined that the bus is granted, the descriptor is read and the descriptor data is written to the processor local RAM, as indicated at block 440."), [0045] ("If, at block 444, the CRC is good, the command type is decoded, as noted at block 460."), [0046] ("At block 464 is it determined if the command code indicates that the source of the data is the host and the destination of the data is the SDRAM. If so, the processor performs the operational steps for transferring data from the host memory to the SDRAM, as indicated at block 468. If block 464 generates a negative result, at block 472 it is determined if the command code indicates that the source of the data is the SDRAM and the destination of the data is the host. If so, the processor performs the operational steps for transferring data from the SDRAM to the host memory, as indicated at block 476.").

729. Accordingly, the prior art references in each of Grounds 4 and 5 satisfy "*the at least one circuit operable to (i) receive a first plurality of address and control signals via the first portion of the plurality of edge connections, and (ii) output a second plurality of address and control signals to the plurality of SDRAM devices*."

(3) [1.i.3] Coupled to both the second and fourth regulated voltage

730. Claim 1 requires "*the at least one circuit coupled to both the second regulated voltage and the fourth regulated voltage*."

731. The prior art references in each of Grounds 4 and 5 teach this limitation to a Skilled Artisan.

732. As explained above, the prior art references in each of Grounds 4 and 5 satisfy "*a second buck converter configured to provide a second regulated voltage having a second voltage amplitude*." *Supra* ¶¶668-676. In particular, Spiers discloses to a Skilled Artisan that a voltage supply from voltage regulator 206 of, for example, VCCFPGA of 1.8 volts (Grounds 4 and 5, Mappings A through C) is coupled to the processor 198. *See id.*

733. Further, as explained above, the prior art references in each of Grounds 4 and 5 satisfy "*a converter circuit configured to provide a fourth regulated voltage having a fourth voltage amplitude*." *Supra* ¶¶689-700. In particular, Spiers discloses to a Skilled Artisan that a voltage supply from voltage

regulator 184 or a similar circuit, for example VCC/VCCO of 3.3 volts (all Grounds), is coupled to the processor 198 and/or the non-volatile memories 194. *See id.*

734. Accordingly, the prior art references in each of Grounds 4 and 5 satisfy "*the at least one circuit coupled to both the second regulated voltage and the fourth regulated voltage*."

(4) [1.i.4] Wherein one of second and fourth regulated voltage amplitudes is less than the other

735. Claim 1 requires "*wherein a first one of the second and fourth voltage amplitudes is less than a second one of the second and fourth voltage amplitudes*."

736. The prior art references in each of Grounds 4 and 5 teach this limitation to a Skilled Artisan.

737. As explained above, the prior art references in each of Grounds 4 and 5 satisfy "*the at least one circuit coupled to both the second regulated voltage and the fourth regulated voltage*." *Supra* ¶¶730-734. In particular, Spiers in view of Amidi discloses to a Skilled Artisan that processor 198 is coupled to the "*second regulated voltage*," for example, VCCFPGA of 1.8 volts (Grounds 4 and 5, Mappings A through C) and to the "*fourth regulated voltage*," for example, VCC of 3.3 volts (Grounds 4 and 5, Mappings A and B) or VCCO of 3.3 volts (Grounds 4 and 5, Mapping C; *see also* Grounds 4 and 5, Mappings A and B).

738. Accordingly, the prior art references in each of Grounds 4 and 5 satisfy "*wherein a first one of the second and fourth voltage amplitudes is less than a second one of the second and fourth voltage amplitudes*."

2. Claim 2 is Unpatentable

739. Claim 2 is unpatentable as the prior art references in each of Grounds 4 and 5 (Voltage Mappings A, B, and C) render the claim obvious.

740. Claim 2 requires "*[t]he memory module of claim 1, wherein the first and third buck converters are further configured to operate as a dual buck converter*."

741. The prior art references in each of Grounds 4 and 5 teach this limitation to a Skilled Artisan.

742. As explained above for claim limitation [1.c], Spiers in view of Amidi satisfy "*a first buck converter configured to provide a first regulated voltage having a first voltage amplitude*." *Supra* ¶¶655-666. As previously discussed for Voltage Mapping A through C of Grounds 4 and 5, the "*first buck converter*" provides, for example, VDD/VDDQ as the "*first regulated voltage*" to the memory devices, such as DDR2 or DDR3 DRAMs. *See id.*

743. As explained above for claim limitation [1.e], Spiers in view of Amidi satisfy "*a third buck converter configured to provide a third regulated voltage having a third voltage amplitude*." *Supra* ¶¶677-687. As previously discussed for

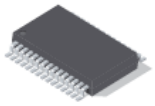
Voltage Mappings A, B, and C of Grounds 4 and 5, the "*third buck converter*" provides, for example, VTT as the "*third regulated voltage*" as a termination voltage coupled to the memory devices, such as DDR2 and DDR3 DRAMS, or VCC as the "*third regulated voltage*" as a supply voltage coupled to the non-volatile memory. *See id.*

744. For Voltage Mappings A and B of Grounds 4 and 5, where the first and third regulated voltages are VDD/VDDQ and VTT (in either order), a Skilled Artisan would have been motivated to use a dual buck converter to have VTT follow the fluctuations of VDD/VDDQ, thus maintaining the fixed ratio between VTT and VDD/VDDQ.

745. In each of these cases, a Skilled Artisan would have been motivated to use a "*dual buck converter*" to provide the "*first*" and "*third*" voltages because using a dual buck converter would use fewer integrated circuits, pins, and interconnections on the module, therefore simplifying its design. *Supra* ¶¶338-344. She would have understood that such "*dual buck converters*" were designed and readily available on the market at the time for this very functionality. *Id.*; Ex. 1040 at 1 (reproduced below in part), 11 ("TPS51020 gives a complete function set required for the DDR termination supply such as VDDQ/2 tracking V_{TT}").

TEXAS INSTRUMENTS

TPS51020



SLUS564B – JULY 2003 – REVISED DECEMBER 2003

DUAL, VOLTAGE MODE, DDR SELECTABLE, SYNCHRONOUS, STEP-DOWN CONTROLLER FOR NOTEBOOK SYSTEM POWER

APPLICATIONS

- Notebook Computers System Bus and I/O
- DDR I or DDR II Termination

See also Ex. 1041 at 1, 2 (reproduced below in part, annotated), 9 (disclosing how using different phases for the two converters can reduce ripples); Ex. 1047 at 3:49-50, 4:7-10, 4:37-56, 5:4-13, 5:46-59 & Fig.2 (illustrating dual buck converter with Vout1=V_{DDQ} and Vout2=V_{TT} and phase shifting).

FAIRCHILD SEMICONDUCTOR®

October 2005

FAN5026
Dual DDR/Dual-Output PWM Controller

Applications

■ DDR V_{DDQ} and V_{TT} voltage generation

Circuit Description

Overview

The FAN5026 is a multi-mode, dual channel PWM controller intended for graphic chipset, SDRAM, DDR DRAM or other low output voltage power applications in PC's, VGA Cards and set top boxes. The IC integrates a control circuitry for two synchronous buck converters. The output voltage of each controller can be set in the range of 0.9V to 5.5V by an external resistor divider.

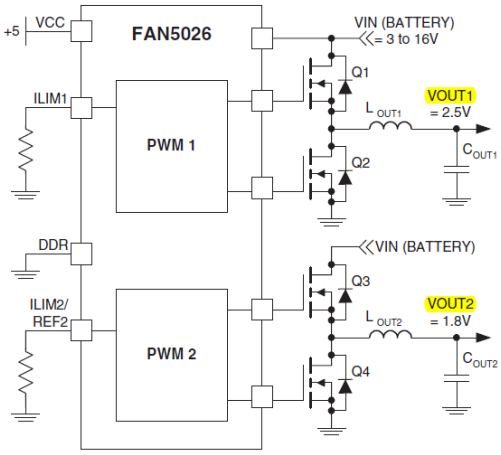


Figure 1. Dual Output Regulator

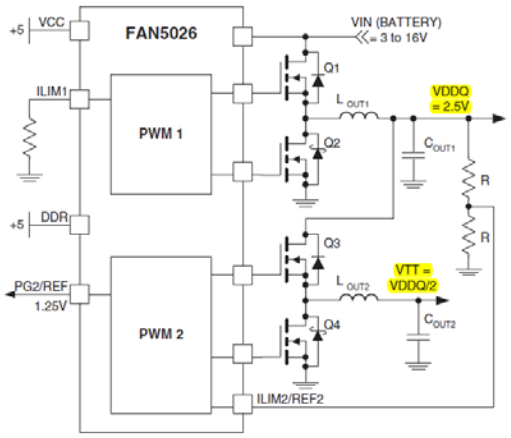


Figure 2. Typical Application

746. Accordingly, the prior art references in each of Grounds 4 and 5 satisfy "*wherein the first and third buck converters are further configured to operate as a dual buck converter*."

3. Claim 3 is Unpatentable

747. Claim 3 is unpatentable as the prior art references in Grounds 4 and 5 (Voltage Mappings B and C) render the claim obvious.

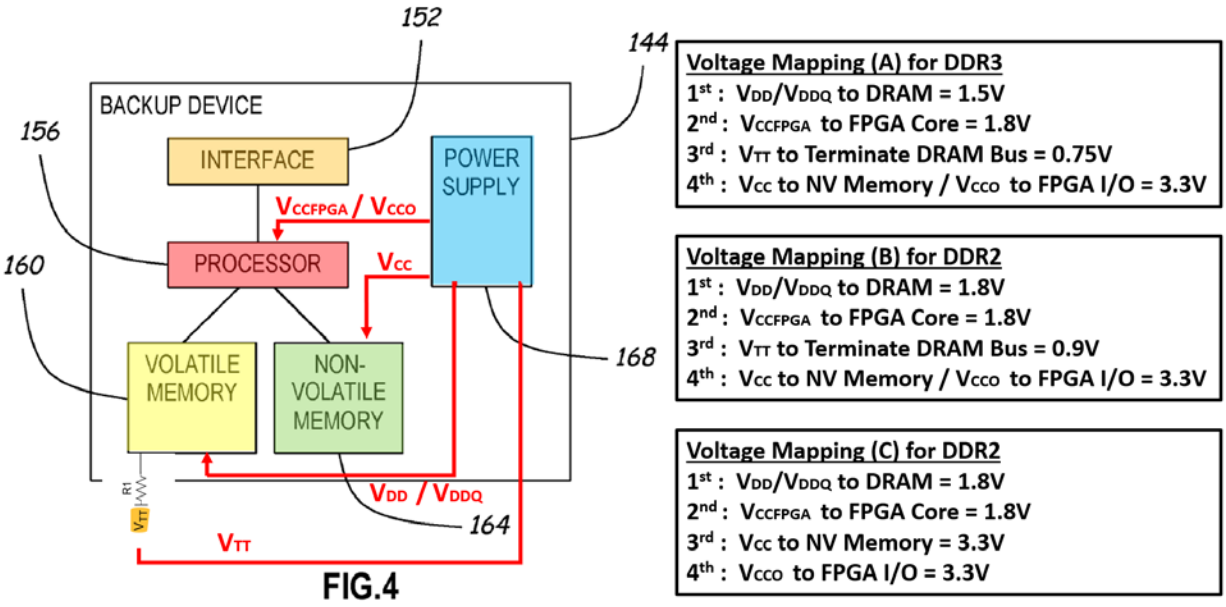
748. Claim 3 requires "*[t]he memory module of claim 1, wherein the first voltage amplitude is 1.8 volts.*"

749. The prior art references in Grounds 4 and 5 (Voltage Mappings B and C) teach this limitation to a Skilled Artisan.

750. As discussed above for claim limitation [1.c], a Skilled Artisan would understand that, in an embodiment of Spiers's backup device where the SDRAM devices 190 and 218 are DDR2 devices, the amplitude of the "*first regulated voltage*" VDD/VDDQ is 1.8 volts. *Supra* ¶¶655-666; *see also* Ex. 1026 at pp.6-7

(disclosing that DDR2 SDRAM is provided the voltage supplies VDD, VDDQ, and VDDL, each at 1.8 volts); Ex. 1025 at Fig. 4 (reproduced below, annotated).

Ground 4: Spiers in view of Amidi, with DDR2 or DDR3 DRAMs



751. Accordingly, Spiers in view of Amidi (Voltage Mappings B and C of Grounds 4 and 5) satisfies the "*wherein the first voltage amplitude is 1.8 volts*" limitation.

4. Claim 4 is Unpatentable

752. Claim 4 is unpatentable as the prior art references in Grounds 4 and 5 render the claim obvious.

753. Claim 4 requires "*[t]he memory module of claim 1, wherein the second, third, and fourth voltage amplitudes are 2.5 volts, 1.2 volts, and 3.3 volts, respectively*."

754. The prior art references in each of Grounds 4 and 5 teach this limitation to a Skilled Artisan.

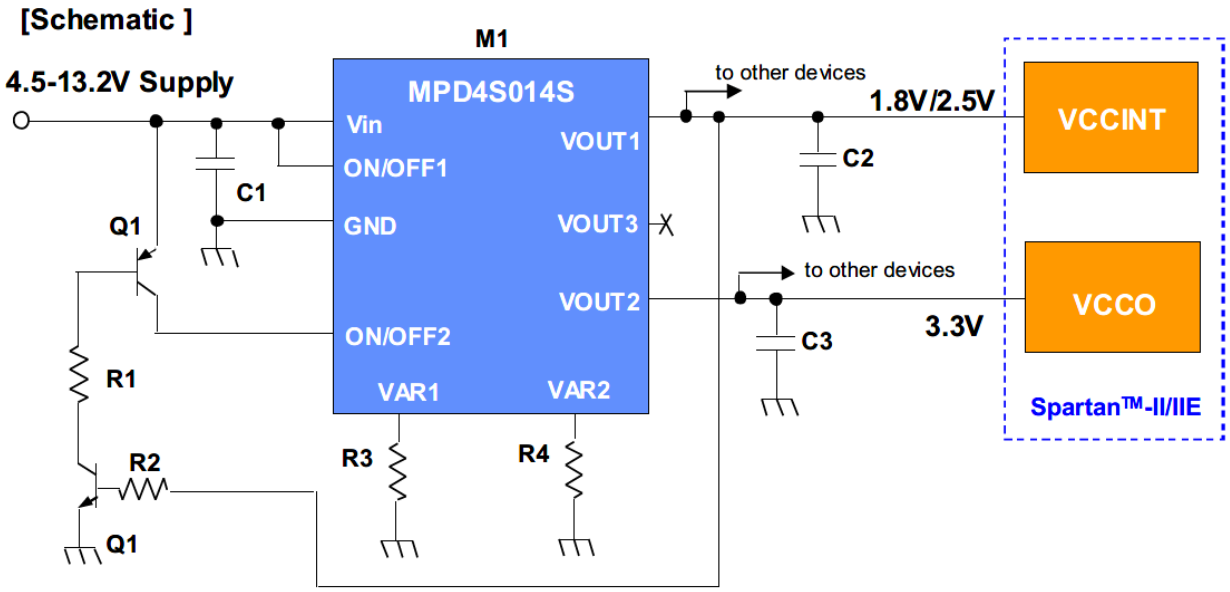
755. A Skilled Artisan would have understood that the specific choice of voltages and the respective voltage amplitudes depend on the parts selected for implementing the backup device of Spiers, including the SDRAM and FPGA processor.

756. As previously discussed, a Skilled Artisan would have recognized, and been motivated to use, DDR2 or DDR3 SDRAMs when implementing the SDRAMs in the backup device of Spiers, and to power the DRAMs according to the relevant JEDEC standards (e.g., JESD79-2B (VDD/VDDQ of 1.8V) and JESD79-3A (VDD/VDDQ of 1.5V)). *See* Ex. 1026; Ex. 1046; *supra* ¶¶198, 200, 655-667 (claim limitation [1.c]).

757. As also discussed above, it would have been obvious to a Skilled Artisan to implement the FPGA processor of Spiers's backup device with a commercially available FPGA device. *Supra* ¶¶668-676 (claim limitation [1.d]), ¶¶689-700 (claim limitation [1.f]). A Skilled Artisan would have also understood that FPGA devices operate at voltages within a known range. For example, the Power Supply Reference Guide for Xilinx FPGAs discloses voltages between 1.0V and 3.3V. *See* Ex. 1042 at 2 (reproduced below in part).

	Spartan™-3/3E/3L	Spartan™-IIE	Spartan™-II	Virtex™-5	Virtex™-4	Virtex-II Pro™	Virtex™-II
V_{CCINT}	1.2V @0.2A-5A	1.8V @0.2A-1.5A	2.5V @0.2A-1A	1.0V @0.2A-15A	1.2V @0.2A-20A	1.5V @0.2A-20A	1.5V @0.2A-20A
V_{CCO}	1.2V-3.3V @50mA-3A	1.5V-3.3V @50mA-0.5A	1.5V-3.3V @50mA-0.5A	1.2V-3.3V @50mA-5A	1.2V-3.3V @50mA-3A	1.5V-3.3V @50mA-3A	1.5V-3.3V @50mA-3A
V_{CCAUX}	2.5V @50mA-0.3A	–	–	2.5V @50mA-0.7A	2.5V @50mA-0.7A	2.5V @50mA-0.3A	3.3V @50mA-0.3A

758. Accordingly, a Skilled Artisan would have understood that it would have been an obvious design choice to select one or more FPGAs, and it was at least obvious to try an FPGA with an input voltage, VCCFPGA (labeled as "VCCINT" in the figure above), of 1.2V, another input voltage, VCCO, of 3.3V, and another input voltage, VCCAUX, of 2.5V, such as a Virtex-4 FPGA. *See* Ex. 1042 at 2 (reproduced above in part); *see also* Ex. 1042 at 16 (reproduced below in part, showing the use of a commercially available dual buck converter to supply voltages to an FPGA, including 2.5V and 3.3V).



759. In an implementation of Spiers's backup device with DDR3 DRAMs and a commercially available FPGA with power requirements in the disclosed range from 1.0V to 3.3V, such as Virtex-4, the "*first regulated voltage*" is VDD/VDDQ with a "*first voltage amplitude*" of 1.5V, the "*second regulated voltage*" is VCCAUX with a "*second voltage amplitude*" of 2.5V, the "*third regulated voltage*" is VCCFPGA (labeled as "VCCINT" in the figure above) with a "*third voltage amplitude*" of 1.2V, and the "*fourth regulated voltage*" is VCCO with a "*fourth voltage amplitude*" of 3.3V.

760. In an implementation of Spiers's backup device with DDR2 DRAMs and a commercially available FPGA with power requirements in the disclosed range from 1.0V to 3.3V, such as Virtex-4, the "*first regulated voltage*" is VDD/VDDQ with a "*first voltage amplitude*" of 1.8V, the "*second regulated voltage*" is VCCAUX with a "*second voltage amplitude*" of 2.5V, the "*third regulated voltage*" is VCCFPGA (labeled as "VCCINT" in the figure above) with a "*third voltage amplitude*" of 1.2V, and the "*fourth regulated voltage*" is VCCO with a "*fourth voltage amplitude*" of 3.3V.

761. Therefore, it would have been obvious to a Skilled Artisan to implement the processor of Spiers with an FPGA that has three voltage supplies at 2.5 volts, 1.2 volts, and 3.3 volts (like Virtex-4) and implement the SDRAMs of

Spiers with memory devices that have a voltage supply at 1.8 volts (like DDR2) or 1.5 volts (like DDR3), rendering the claimed voltage amplitudes also obvious.

762. Accordingly, the prior art references in each of Grounds 4 and 5 satisfy the "*wherein the second, third, and fourth voltage amplitudes are 2.5 volts, 1.2 volts, and 3.3 volts, respectively*" limitation.

5. Claim 5 is Unpatentable

763. Claim 5 is unpatentable as the prior art references in each of Grounds 4 and 5 (Voltage Mappings A, B, and C) render the claim obvious.

a) [5.a] Preamble

764. The preamble of claim 5 requires "*[t]he memory module of claim 1, further comprising*."

765. As explained above for claim 1, the prior art references in each of Grounds 4 and 5 satisfy the limitations of claim 1. *Supra* ¶¶641-738.

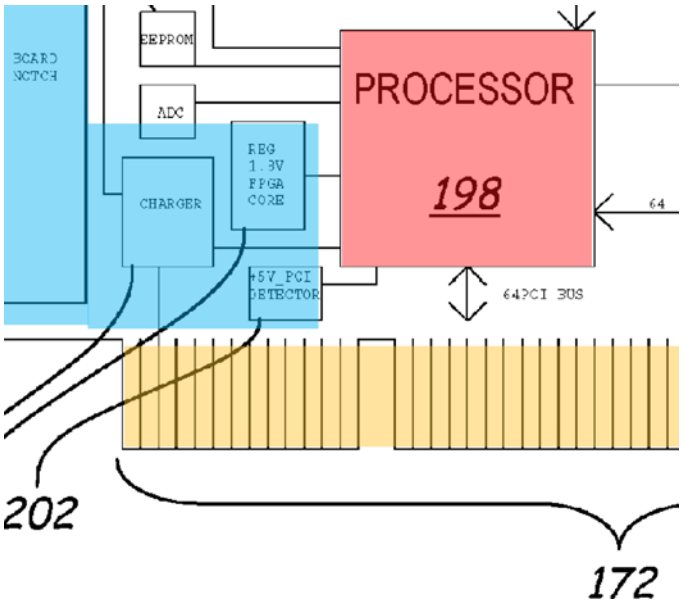
766. Accordingly, the prior art references in each of Grounds 4 and 5 satisfy "*[t]he memory module of claim 1, further comprising*."

b) [5.b] Voltage Monitor Circuit

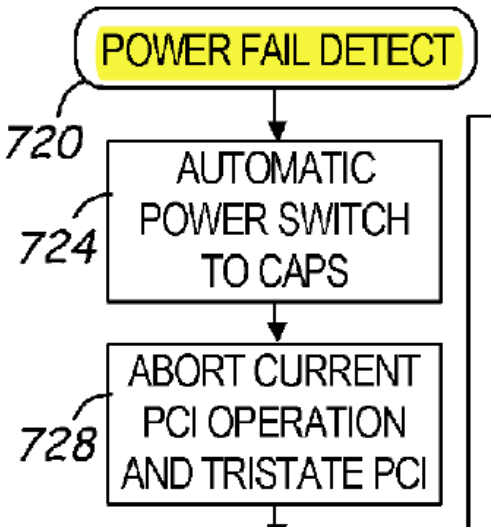
767. Claim 5 requires "*a voltage monitor circuit configured to monitor a power input voltage received via a second portion of the plurality of edge connections, the voltage monitor circuit configured to produce a trigger signal in response to the power input voltage having a voltage amplitude that is greater than a first threshold voltage*."

768. The prior art references in each of Grounds 4 and 5 teach this limitation to a Skilled Artisan.

769. It would have been obvious to a Skilled Artisan that the prior art in each of Grounds 4 and 5 teaches and discloses "*a voltage monitor circuit configured to monitor a power input voltage received via a second portion of the plurality of edge connections*." Spiers discloses a power detection circuit 202 ("*a voltage monitor circuit*") configured to monitor the +5 volt supply voltage at a +5 volt pin of PCI connector 172 ("*power input voltage received via a second portion of the plurality of edge connections*"). *See* Ex. 1025 at Figs. 5, 14 (reproduced below in part, annotated), [0037] ("The FPGA processor 198 utilizes a power detection circuit that, in this embodiment, is a +5V PCI detector 202."), [0054] ("Referring now to FIG. 14, the operational steps performed by the backup device upon detection of a power failure are now described. As discussed previously, the backup device monitors the primary power supply. In the PCI card embodiment, this monitoring is performed by monitoring the voltage at a +5 volt pin.").



Ex. 1025 at Fig. 5 (excerpted and annotated).



Id. at Fig. 14 (excerpted and annotated).

770. In addition, it would have been obvious to a Skilled Artisan that the prior art in each of Grounds 4 and 5 teaches "*the voltage monitor circuit* [is] *configured to produce a trigger signal in response to the power input voltage*

having a voltage amplitude that is greater than a first threshold voltage." Spiers alone and in view of Amidi renders obvious to a Skilled Artisan that the +5V voltage detector 202 is "*configured to produce a trigger signal*" to switch power to capacitors and disconnect from PCI bus "*in response to the power input voltage having a voltage amplitude that is greater than a first threshold voltage*," indicating an anomaly in the external power source. *See* Ex. 1025 at Figs. 5, 14 (reproduced above in part, annotated).

771. For example, Spiers explains that, "[i]nitially, at block 720, a power failure is detected. At block 724, the backup device processor switches the power to the capacitors. At block 728, the processor aborts any current PCI operation and tristates the PCI." Ex. 1025 at [0054]. A Skilled Artisan would have understood from Spiers's disclosure that the voltage monitor circuit 202 produces a "*trigger signal*" when it detects a power failure. The backup device processor (198, red) receives this "*trigger signal*" (*see* connection between voltage detector 202 (blue) and processor 198 (red)), switches the power source from the PCI connector pin to the capacitors, and disconnects ("tristates") the PCI bus. *See id.* at Fig. 5 (reproduced above in part, annotated).

772. Spiers further describes the function of its "+5V PCI detector 202." In particular, Spiers discloses that the "FPGA processor 198 utilizes a power detection circuit" such as "+5V PCI detector 202." Ex. 1025 at [0037]. In relation

to power detection, Spiers explains that "[t]he non-volatile memory 164 . . . is utilized in the event of a power failure detection." *Id.* at [0036]. Although Spiers does not expressly disclose the details of how that function is performed, a Skilled Artisan would have understood that such a voltage detector operation includes comparing the input voltage to a "*first threshold voltage*." *See, e.g.*, Ex. 1024 at 4:44-52, 5:35-43, 8:23-29, 9:8-12, Fig. 6 (disclosing a voltage supervisory block 665 comparing the system supply voltage 605 to a reference voltage 675, defining a threshold, and generating a "trigger signal" 670 as a result of the comparison), 8 (similar), 14-15.

773. A Skilled Artisan would have also understood, and it would have been at least obvious to her, that Spiers's "+5V PCI detector 202" can detect a power failure when the input voltage is outside of a preset interval, defined by an upper and a lower limit, which the backup device 144 can tolerate without losing data or damaging the circuits. *See, e.g.*, Ex. 1023 at [0013] ("Further, since the +12V power supply is not used directly by DRAM devices or buffer/logic components of the memory assembly, a wide tolerance (e.g., around +/−15%) can be accommodated.").

774. For example, U.S. Patent Publication No. 2009/0034354 to Resnick ("Resnick") describes generating "an alarm signal if the difference between the operating voltage and the reference voltage indicates the operating voltage is

outside of a normal operating range" for a memory device. Ex. 1065 at Abstract, [0014], Fig. 1. Resnick describes that the alarm signal is generated when "the operating voltage [is] above an upper threshold or below a lower threshold." *Id.* at Fig. 5 (block 530). Resnick explains that a "voltage sensor 110 may be configured to signal an alarm in the case where the operating voltage is outside of a range" which relates to the "magnitude of the voltage [going] beyond a predetermined threshold level, which may be an upper or lower level relative to an expected, or normal operating voltage." *Id.* at [0018]. Further, "[i]f the operating voltage is above or below the relevant threshold, voltage sensor 110 may indicate the voltage failure by sending a flag such as alarm signal 112 to a pin on semiconductor memory device 100 for signaling the alarm externally." *Id.* at [0019]; *see also id.* at [0031], [0033], Figs. 1-3. Thus, by way of example, Resnick shows that, at the time, a Skilled Artisan would have understood that a voltage detection circuit could be implemented to detect different types of anomalies on a memory module, including the amplitude of the voltage going above or below predetermined levels, and to indicate a voltage failure by sending a flag such as an alarm signal.

775. As another example, a National Semiconductor datasheet for LMC6953 describes an over-voltage threshold of 5.6 volts for a 5-volt power supply. *See* Ex. 1063 at 1-2 (reproduced below and annotated for both over-voltage and under-voltage).

National Semiconductor

LMC6953
PCI Local Bus Power Supervisor

DC Electrical Characteristics

Unless otherwise specified, all **boldface** limits guaranteed for T_J = 0°C to 70°C, V_{DD} = 5V, $R_{PULL-UP}$ = 4.7 kΩ and C_{EXT} = 0.01 μF. Typical numbers are room temperature (25°C) performance.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{H5}	V_{DD} Over-Voltage Threshold	(Note 4)	**5.45**	5.6	**5.75**	V
V_{L5}	V_{DD} Under-Voltage Threshold	(Note 4)	**4.25**	4.4	**4.55**	V
$V_{H3.3}$	3.3V Over-Voltage Threshold	(Note 5)	**3.8**	3.95	**4.1**	V
$V_{L3.3}$	3.3V Under-Voltage Threshold	(Note 5)	**2.5**	2.65	**2.8**	V

776. As yet another example, an Analog Devices datasheet for ADM1066 describes programmable circuits to "detect an undervoltage fault (the input voltage drops below a preprogrammed value), an overvoltage fault (the input voltage rises above a preprogrammed value), or an out-of-window fault (undervoltage or overvoltage)." Ex. 1061 at 15; *see also* Ex. 1062 at 15 ("Two comparators are dedicated to each input so that undervoltage and overvoltage detection can be implemented . . . .").

777. Accordingly, it would have been obvious for a Skilled Artisan to implement Spier's "+5V PCI detector 202" to detect voltage anomalies and switch to the backup power based on detection of an undervoltage or overvoltage condition. As described above, implementing Spier's +5V PCI detector 202 in this manner was well within the level of skill at the time. *See e.g.*, Ex. 1024 (Amidi) at

5:35-43, 8:23-29, 9:8-12, Figs. 6, 14; Ex. 1065 at Abstract, [0014], [0018], Fig. 5 (block 530); Ex. 1063 at 1-2; Ex. 1061 at 15; Ex. 1062 at 15. Thus, Spiers alone and in view of Amidi renders obvious this limitation in view of the knowledge of a Skilled Artisan.

778. Accordingly, the prior art references in Ground 4 satisfies this limitation.

779. To the extent one were to argue that overvoltage protection was not obvious in light of Ground 4, it would have been obvious in light of Hajeck, as part of Ground 5. As explained above, a Skilled Artisan would have been motivated to combine Ground 4 with Hajeck. *See supra* ¶¶207-212. Hajeck describes the operation of a "conventional voltage detection circuit." Ex. 1038 at 3:33-34; *see also id.* at Abstract, 1:62-2:7, 3:30-4:9. Hajeck discloses:

> "[A] voltage detection circuit 48 [that] is responsible for detecting anomalies in the power signal V_{IN} supplied by the host on line 36, and for driving the ready/busy signal to the 'busy' state when such anomalies are detected. A conventional voltage detection circuit may be used. The voltage detection circuit 48 may be designed to generate a 'busy' signal whenever V_{IN} falls below a certain level, such as 2.6 or 2.7 volts. **The voltage detection circuit may also be designed to generate a busy signal when the voltage exceeds a certain level, and/or when other types of anomalies are detected**. To inhibit rapid transitions between the 'ready' and 'busy' states, the **voltage detection circuit may be designed to provide a degree of hysteresis, and/or to hold its output for a particular time period after a state transition**."

Id. at 3:30-43 (emphasis added). Thus, Hajeck shows that, at the time, a Skilled Artisan would have been able to design a voltage detection circuit that detects multiple types of anomalies, including when the voltage exceeds a certain level, and that provides hysteresis and holds its output for a period of time after a state transition. In light of Hajeck's and Amidi's teachings, a Skilled Artisan would have understood and been motivated to implement Spiers's "+5V PCI detector 202" to detect voltage anomalies and switch to the backup power not only if an undervoltage is detected, such as taught in Amidi (Ex. 1024 at 4:44-53 ("[i]f system supply 605 has a magnitude lower than reference voltage 675"), but also "when the voltage exceeds a certain level" as taught by Hajeck (Ex. 1038 at 3:30-40). Indeed, as discussed above, the problems caused by such overvoltage conditions, and solutions to detect and protect against them, were well known at the time. Accordingly, Skilled Artisan would have understood that, to avoid these well-known problems, Hajeck's "conventional voltage detection circuit" teachings on detecting both under- and over-voltage conditions were readily available at the time. Ex. 1038 at 3:30-40.

780. Accordingly, the prior art references in Ground 5 (Ground 4 in view of Hajeck) also satisfies the "*a voltage monitor circuit configured to monitor a power input voltage received via a second portion of the plurality of edge connections, the voltage monitor circuit configured to produce a trigger signal in*

response to the power input voltage having a voltage amplitude that is greater than a first threshold voltage" limitation

6. Claim 6 is Unpatentable

781. Claim 6 is unpatentable as the prior art references in each of Grounds 4 and 5 (Voltage Mappings A, B, and C) render the claim obvious.

782. Claim 6 requires "*[t]he memory module of claim 5, wherein the voltage monitor circuit is further configured to produce the trigger signal in response to the power input voltage having a voltage amplitude that is less than a second threshold voltage*."

783. The prior art references in each of Grounds 4 and 5 teach this limitation to a Skilled Artisan.

784. As discussed above with reference to claim limitation [5.b], the prior art references in each of Grounds 4 and 5 render obvious to a Skilled Artisan that Spiers's +5V voltage detector 202 is "*configured to produce a trigger signal*" to switch power to capacitors and disconnect from PCI bus "*in response to the power input voltage having a voltage amplitude that is less than a second threshold voltage*." *Supra* ¶¶767-780; *see also* Ex. 1024 at Fig. 6 (showing that a threshold of -5% is used for the selection between system and backup power).

785. As previously discussed, a Skilled Artisan would have understood, and it would have been at least obvious to her, that Spiers's "+5V PCI detector

202" can detect a power failure when the input voltage is outside of a preset interval, defined by an upper and a lower limit, which the backup device 144 can tolerate without losing data or damaging the circuits. *Supra* ¶¶774-778; *see, e.g.*, Ex. 1023 at [0013] ("Further, since the +12V power supply is not used directly by DRAM devices or buffer/logic components of the memory assembly, a wide tolerance (e.g., around +/−15%) can be accommodated.").

786. Indeed, as previously discussed, in addition to overvoltage protection, implementing undervoltage protection was well within the level of skill of a Skilled Artisan at the time. *See supra* ¶¶773-778. For example, Resnick shows that, at the time, a Skilled Artisan would have been able to design a voltage detection circuit that detects different types of anomalies on a memory module, including the amplitude of the voltage going beyond a predetermined level, and that indicates a voltage failure by sending a flag such as an alarm signal. *See* Ex. 1065 (Resnick) at Abstract, [0014], [0018], [0031], [0033], Figs. 1-3, 5. As another example, a National Semiconductor datasheet for LMC6953 describes an under-voltage threshold of 4.4 volts for a 5-volt power supply. *See* Ex. 1063 at 1-2 (describing both over-voltage and under-voltage). As yet another example, an Analog Devices datasheet for ADM1066 describes programmable circuits to "detect an undervoltage fault (the input voltage drops below a preprogrammed value), an overvoltage fault (the input voltage rises above a preprogrammed value), or an out-

of-window fault (undervoltage or overvoltage)." Ex. 1061 at 15; *see also* Ex. 1062 at 15 ("Two comparators are dedicated to each input so that undervoltage and overvoltage detection can be implemented . . . .").

787. Accordingly, it would have been obvious for a Skilled Artisan to implement Spier's "+5V PCI detector 202" to detect voltage anomalies and switch to the backup power based on detection of both undervoltage and overvoltage conditions. Thus, the prior art references in each of Grounds 4 and 5 renders obvious this limitation in view of the knowledge of a Skilled Artisan.

788. To the extent one were to argue that overvoltage protection was not obvious in light of Ground 4, it would have been obvious in light of Hajeck, as part of Ground 5. As explained for claim limitation [5.b], a Skilled Artisan would have understood that Spiers's "+5V PCI detector 202" would be implemented to detect voltage anomalies and switch to the backup power not only for undervoltage conditions as taught by Spiers and Amidi, *see* Ex. 1025, ¶¶[0002, 36-37], Fig.14; Ex. 1024 at 4:44-53, but also "when the voltage exceeds a certain level" as taught by Hajeck, *see* Ex. 1038 at 3:30-43; *see also id.* Abstract, 1:10-18, 1:28-31, 1:62-2:7, 3:30-4:9, 4:62-65, FIG. 1. *See supra* ¶¶137, 207-212, 779-780.

789. Accordingly, the prior art references in each of Grounds 4 and 5 satisfy the "*wherein the voltage monitor circuit is further configured to produce*

the trigger signal in response to the power input voltage having a voltage amplitude that is less than a second threshold voltage" limitation.

7. Claim 7 is Unpatentable

790. Claim 7 is unpatentable as the prior art references in each of Grounds 4 and 5 (Voltage Mappings A, B, and C) render the claim obvious.

791. Claim 7 requires "*[t]he memory module of claim 6, wherein the second threshold voltage corresponds to a voltage level that is ten percent less than a specified operating voltage*."

792. The prior art references in each of Grounds 4 and 5 teach this limitation to a Skilled Artisan.

793. As discussed above with reference to claims 5 and 6, the prior art references in each of Grounds 4 and 5 renders obvious to a Skilled Artisan that the "*second threshold voltage*" corresponds to a tolerance the module can safely handle in the external voltage. *Supra* ¶¶764-780 (claim 5), ¶¶781-789 (claim 6).

794. In Spiers (like in Harris), the external voltage (5V) is stepped down by voltage regulators to the voltages used by the parts in the module, including the memory devices. Thus, a Skilled Artisan would have understood that, just like in Harris, the tolerance on the input voltage (+/-15%) can be larger than the tolerance of the memory devices (e.g., roughly 5% for DDR2 SDRAMs). Ex. 1023 at [0013] (describing +/- 15% tolerance); Ex. 1026 at pp.6-7 (describing +/- 0.1V tolerance

for 1.8V supply voltage to DDR2 SDRAM devices); *see also* Ex. 1024 at Fig. 6 (showing a VREF 5% below nominal value when the external voltage is directly used by the memory devices).

795. Therefore, a Skilled Artisan would have understood and been motivated to select a tolerance between 5% and 15% for the module of Spiers, where the specific value selected would be nothing more than an obvious design choice. A Skilled Artisan would have also understood that allowing too high a tolerance carries the risk of losing data or damaging the devices on the memory module, while setting too low a tolerance carries the risk of unnecessary interruptions of operation. In particular, a Skilled Artisan would have understood that the choice of a 10 percent tolerance provided a reasonable compromise between the risks associated with too high a tolerance and too low a tolerance. *See, e.g.*, Ex. 1063 at 1-2 (describing an Over-Voltage Threshold of about 5.6V and an Under-Voltage Threshold of about 4.4V for a +5V power supply, annotated).

796. For example, Amidi discloses an alternative implementation for monitoring a power rail of 3.3V and comparing it to a 3.0V reference voltage, corresponding to a "*second threshold voltage*" of about 10 percent below the power rail's nominal voltage. *See* Ex. 1024 at Fig. 14 (reproduced below, annotated), 8:23-36; *see also* Ex. 1027 at 32 (stating VDDSPD has a typical voltage of 3.3 volts with a minimum voltage 10 percent below the typical voltage,

or 3.0 volts, and a maximum voltage 10 percent above the typical voltage, or 3.6 volts).

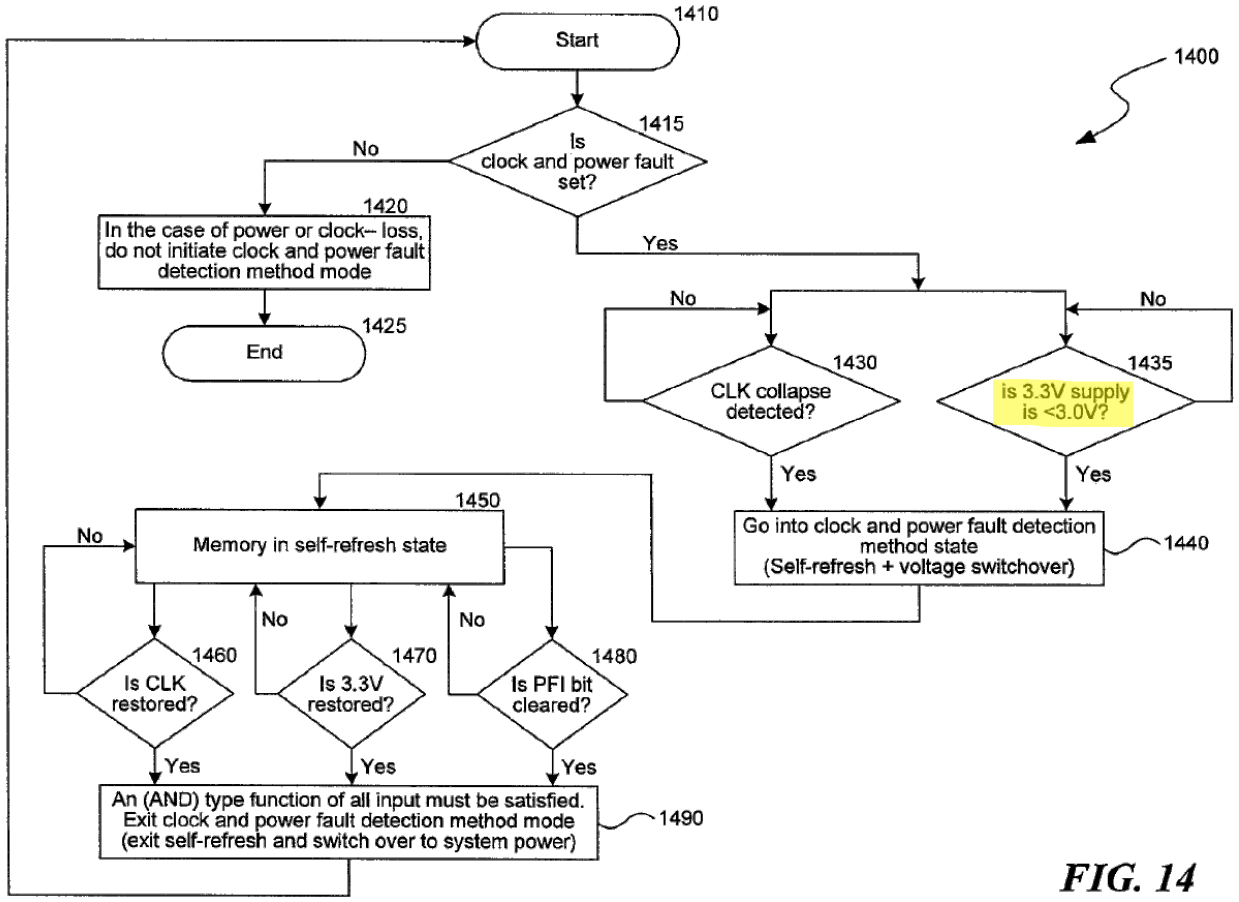


FIG. 14

797. Therefore, a Skilled Artisan would have understood that "the second threshold voltage corresponds to a voltage level that is ten percent less than a specified operating voltage" was obvious.

798. Accordingly, the prior art references in each of Grounds 4 and 5 satisfy the "*wherein the second threshold voltage corresponds to a voltage level that is ten percent less than a specified operating voltage*" limitation.

8. Claim 8 is Unpatentable

799. Claim 8 is unpatentable as the prior art references in each of Grounds 4 and 5 (Voltage Mappings A, B, and C) render the claim obvious.

a) [8.a] Preamble

800. The preamble of claim 8 requires "*[t]he memory module of claim 1, the plurality of components further comprising*."

801. As explained above for claim 1, the prior art references in each of Grounds 4 and 5 satisfy the limitations of claim 1. *Supra* ¶¶641-738.

802. Accordingly, the prior art references in each of Grounds 4 and 5 satisfy "*[t]he memory module of claim 1, the plurality of components further comprising*."

b) [8.b] One or More Registers

(1) [8.b.1] Coupled to one of the regulated voltages

803. Claim 8 requires "*one or more registers coupled to one of the first, second, third and fourth regulated voltages*."

804. The prior art references in each of Grounds 4 and 5 teach this limitation to a Skilled Artisan.

805. As discussed above for claim limitations [1.i.2], Spiers discloses that its processor 198 receives read and write commands from the storage controller on a PCI bus and, in response, reads or writes corresponding data from and to

SDRAMs 190 and 218. *Supra* ¶¶724-729; *see* Ex. 1025 at Fig. 9 (reproduced below and annotated), [0037], [0044-46].

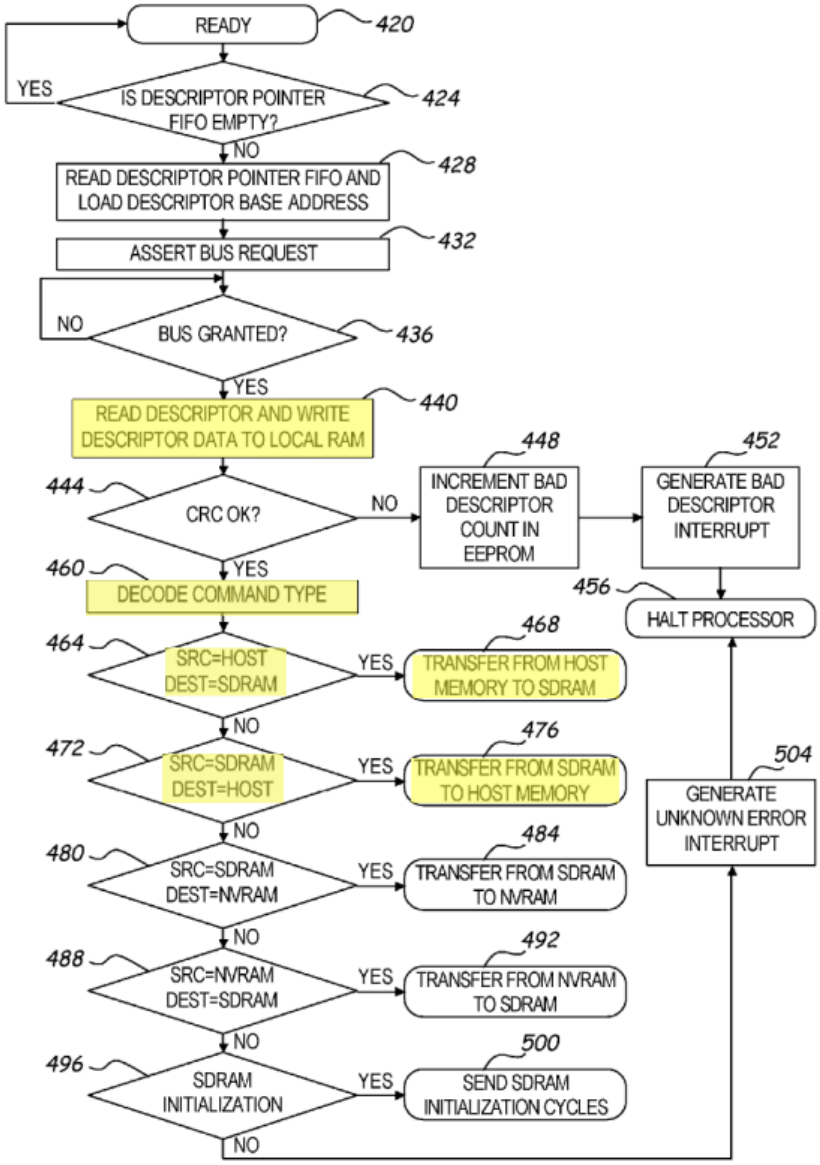


FIG.9

806. A Skilled Artisan would have understood that the signaling for read and write commands is different on the PCI bus than the signaling used by the SDRAMs. *Compare, e.g.*, Ex. 1031 at p.7 (Fig. 2-1 for PCI, reproduced below), *with* Ex. 1045 at p.5 (Functional Block Diagram for SDRAM, reproduced below).

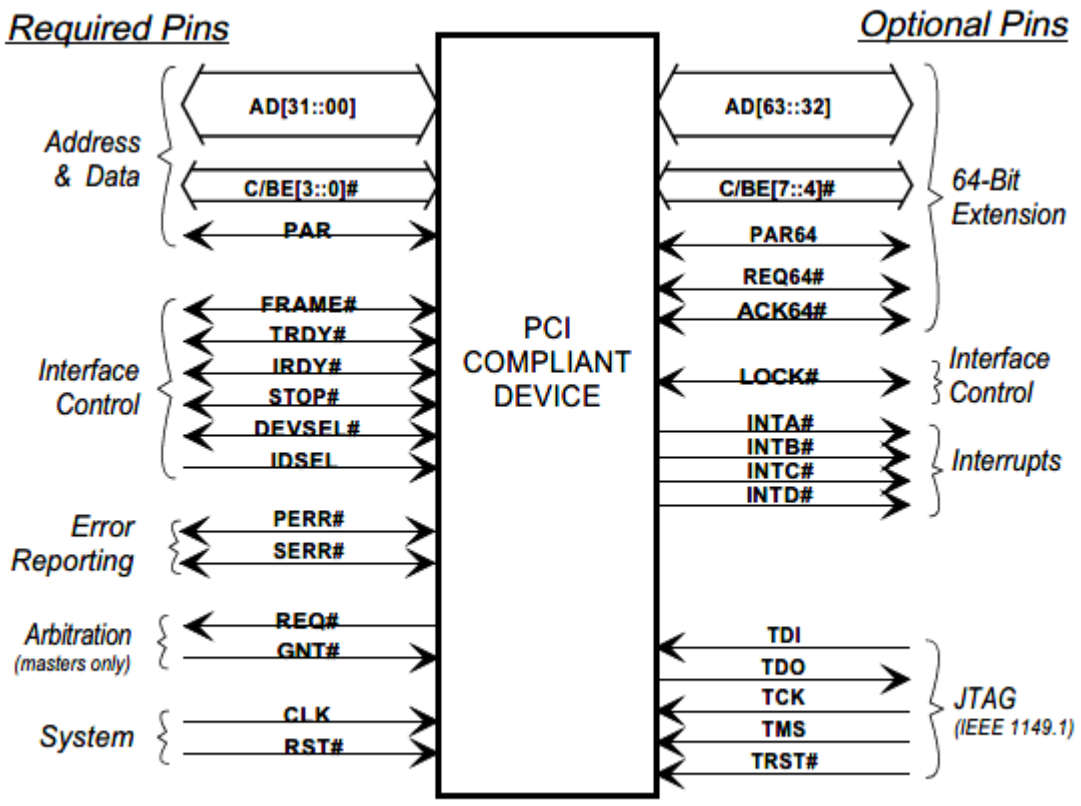
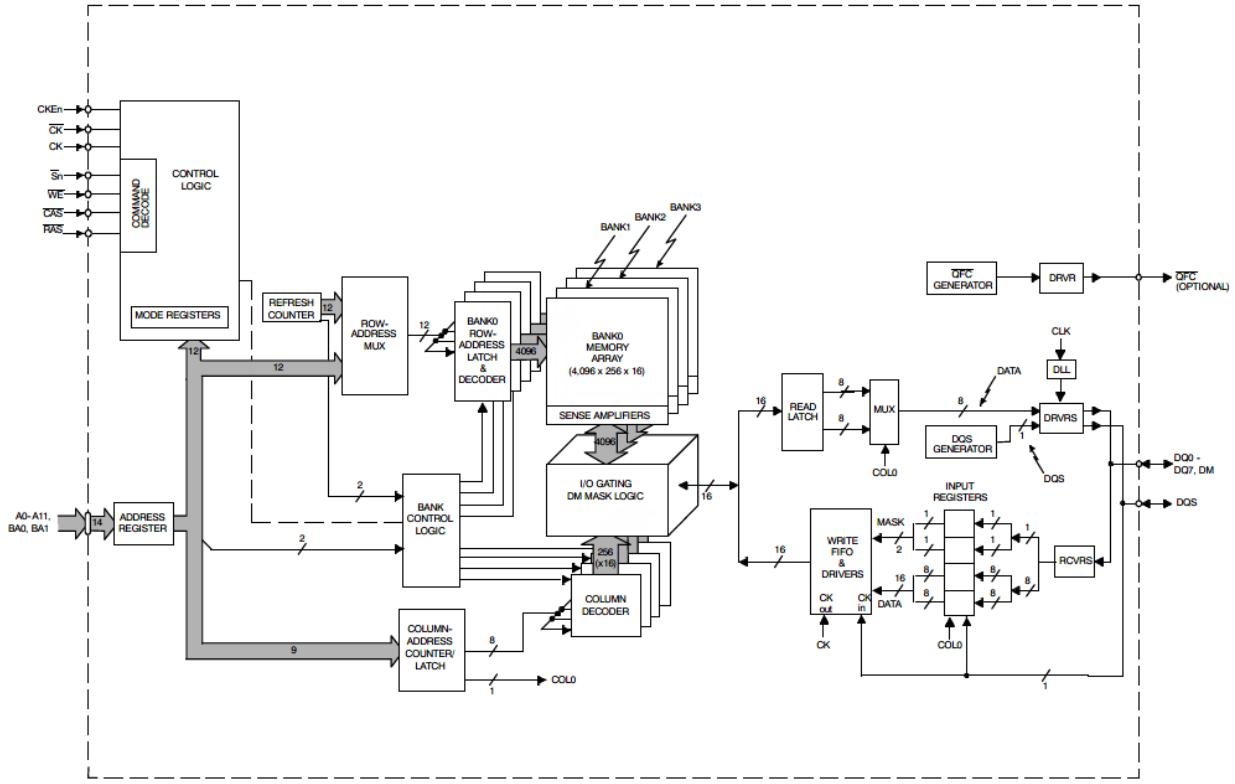


Figure 2-1: PCI Pin List

FUNCTIONAL BLOCK DIAGRAM – x8 CONFIGURATION



807. Therefore, a Skilled Artisan would have understood that the received PCI signals cannot be directly used to control the SDRAMs and need to be translated to corresponding commands and signals according to the JEDEC standards. A Skilled Artisan would have also understood that such a translation requires registers and a logic circuit: the registers capture the values of the address, control, and data signals on the PCI bus in response to the clock on the PCI bus, and the logic circuit performs the translation of the captured signal values for the SDRAM devices. *See*, *e.g.*, Ex. 1031 at pp.47-48 (showing PCI read and write

operations with address (on lines AD), command (on lines C/BE), and data (on lines AD) signals transmitted in sync with the bus clock (CLK)).

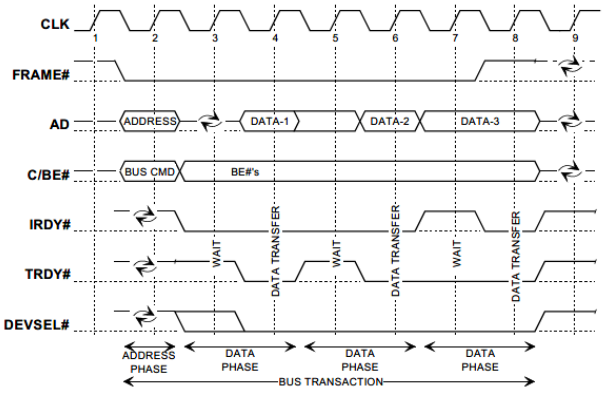


Figure 3-5: Basic Read Operation

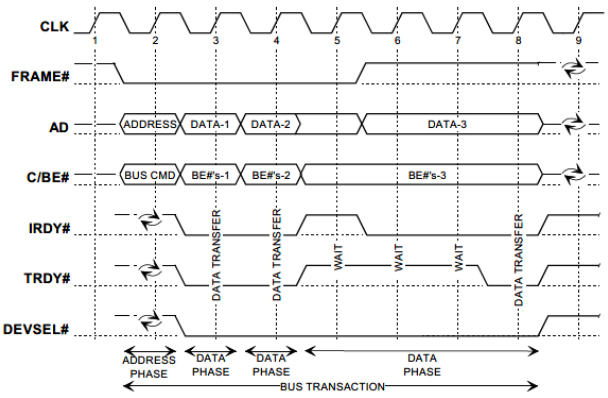


Figure 3-6: Basic Write Operation

808. A Skilled Artisan would have recognized that these registers in the processor 198 are coupled to one of the voltages received by processor 198 (e.g., the "*second regulated voltage*," for example, VCCFPGA, or the "*fourth regulated voltage*," for example, VCCO) for the reasons discussed above with reference to claim 1. *Supra* ¶¶668-676 (claim limitation [1.d]),¶¶689-700 (claim limitation [1.f]),¶¶730-734 (claim limitation [1.i.3]).

809. Accordingly, the prior art references in each of Grounds 4 and 5 satisfy "*one or more registers coupled to one of the first, second, third and fourth regulated voltages*."

(2) [8.b.2] Configured to register address and control signals

810. Claim 8 requires "*the one or more registers configured to register, in response to a clock, the first plurality of address and control signals*."

811. The prior art references in each of Grounds 4 and 5 teach this limitation to a Skilled Artisan.

812. As explained above for claim limitation [8.b.1], Spiers discloses to a Skilled Artisan that processor 198 contains "*one or more registers*" and that these registers are "*configured to register, in response to a clock, the first plurality of address and control signals*." *Supra* ¶¶ 803-809.

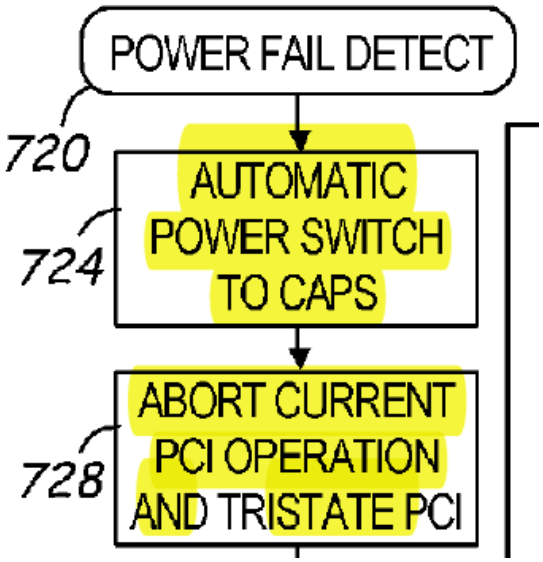
813. Accordingly, the prior art references in each of Grounds 4 and 5 satisfy "*the one or more registers configured to register, in response to a clock, the first plurality of address and control signals*."

(3) [8.b.3] Wherein one of the voltages is selectively switched off

814. Claim 8 requires "*wherein the one of the first, second, third and fourth regulated voltages is selectively switched off to turn power off to the one or more registers while one or more components of the plurality of components are powered on*."

815. The prior art references in each of Grounds 4 and 5 teach this limitation to a Skilled Artisan.

816. Spiers discloses that, in the case of power failure, the backup device processor switches the power to the capacitors and "aborts any current PCI operation and tristates the PCI." Ex. 1025 at [0054], Fig. 14 (reproduced below in part, annotated).



817. A Skilled Artisan would have understood from this disclosure that the registers for registering the PCI address and command signals are not necessary when the PCI operations are aborted and the PCI bus inputs are essentially disconnected ("tristated"). Spiers discloses that the backup voltage source of capacitors is used when the system power fails, and a Skilled Artisan would have understood that such a capacitor power source has a limited capacity. Therefore, a Skilled Artisan would have been motivated to switch off all unnecessary power, including power to the PCI bus registers (e.g., VCCO) which are not used in that state, thereby saving power and allowing the processor 198 to move the user data from the volatile to the non-volatile memory.

818. A Skilled Artisan would have also understood that disconnecting the system bus from the module and switching off power to the unnecessary components in case of power failure was well known at the time and well within

the level of skill. *See, e.g.*, Ex. 1033 at 12:50-58 ("In the case of a memory system according to the FBDIMM architecture, the power saving mode implemented in the embodiment of a memory buffer 100 cannot only differ with respect to analog circuit components and digital circuit components being switched off or deactivated according to the power saving mode, but also, components of the memory buffer 100 can be selectively switched on, depending on the direction of the bus structure of the bus 140 to which they are connected."). In addition, a Skilled Artisan would also have understood that power can be turned off by a switch which connects and disconnects the supply of power from a buck converter, or by turning off the buck converter itself. A Skilled Artisan would have also understood that each of these implementations would have been an obvious design choice. On one hand, turning off the buck converter would save power and extend the life of the battery backup. Thus, a Skilled Artisan would turn off the buck converter if extending the life of the battery backup is a primary concern. On the other hand, using a switch without turning off the buck converter itself would reduce any delays associated with starting the operation of the buck converter when the power is switched back to the system power supply. Thus, a Skilled Artisan would only use a switch without turning off the buck converter if reducing delays when returning to normal operation is important. For example, the FAN5026 data sheet discloses that "Initialization and Soft start" is measured "in

seconds" for a capacitance value that "is in µF." Ex. 1041 (FAN5026) at 10; *see also id.* at 7, 10 (describing a 10nF soft-start capacitor (e.g., C2 or C3) that would require a start time of approximately 1,800 microseconds, or (0.9 * 10nF)/5); *see also* at 13, 21 (Fig. 12) (showing a soft-start time up to 50,000 microseconds, or 0.05 seconds). In comparison to the start time of a buck converter which may be thousands of microseconds, NAND flash memory, for example, is able to write a page of data in only 300 or so microseconds. *See* Ex. 1049 at 1 ("Write Performance," "Page program: 300µs (TYP)"). As another example, U.S. Patent No. 5,563,839 to Herdt *et al.* discloses "isolation switch circuitry" including a large n-channel MOSFET "for connecting and disconnecting" a device from its power supply. *See* Ex. 1056 at 5:15-26, Fig. 3. Either way, a Skilled Artisan would have been motivated to switch off all unnecessary power, including power to the PCI bus registers (e.g., VCCO), which are not used when the PCI operations are aborted and the PCI bus inputs are essentially disconnected ("tri-stated"), to save power and allow Spiers's processor 198 to move the user data from the volatile to the non-volatile memory while operating on the backup voltage source.

819. Further, Amidi discloses that, in the case of power failure, the system address and command signals are disconnected from the memory module and, instead, controlled by a Finite State Machine which generates refresh commands for the memory devices. As annotated in Figure 12 of Amidi, reproduced below,

the “FSM Control, Command Bus” 1245 provides the “Memory Control, Command Bus” signals rather than the “System Control, Command Bus” 1235 in this scenario.

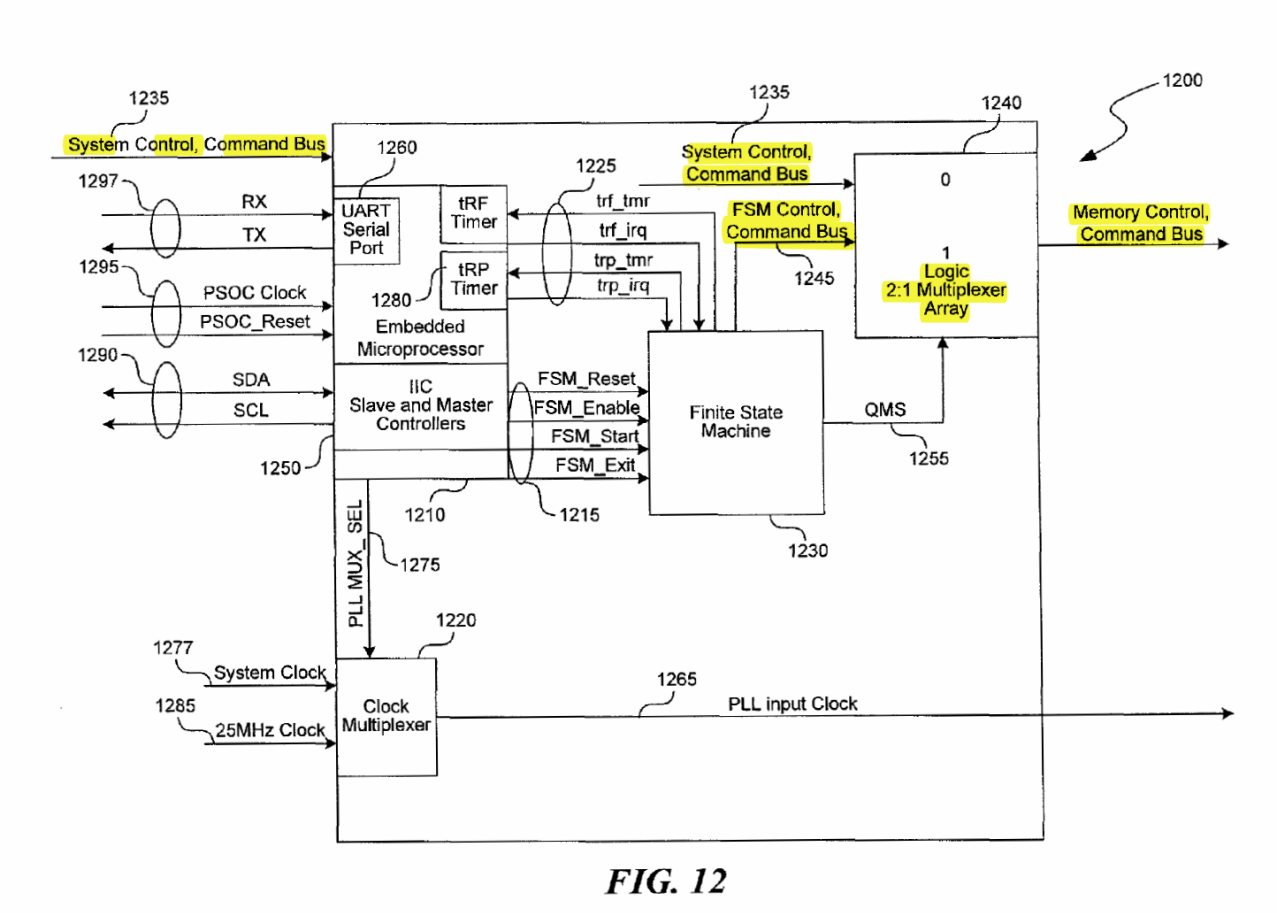


FIG. 12

Ex. 1024 at Fig. 12 (annotated). Amidi explains that “[d]uring normal operation of the system with proper power and/or clock operation the system control and command bus input to signal logic multiplexer 1240 will be chosen by multiplexer select signal 1255. During either power interruption or system clock fault cycles the finite state machine control and command bus signals will be supplied as

memory control and command bus signals through the other inputs of signal logic multiplexer 1240—and selected by multiplexer select signal 1255." *Id.* at 7:35-43.

820. As another example, the JEDEC AMB standard for FBDIMM, JESD82-20, describes an S3 sleeping mode for memory modules where the address and control lines are disconnected (grounded or tristated) and power to the corresponding interface is switched off. *See* Ex. 1027 at p.39 (Section 4.1.3) ("S3 is an ACPI mode in which the DIMMs are put into a very lower power state, with the DRAMs in self refresh mode."). It also discloses that "[w]hen the Advanced Memory Buffer core logic is in S3 power mode, all command/address outputs, including CKE, ODT, CLK, and all other command/address pins, will be driven low. In S3 mode, 1.8V supply is on. 1.5V, Vtt, and 3.3V are off. DRAMs are in self refresh, and the CKE signals must be driven low." *Id.* at 21 (point 6). A Skilled Artisan would have understood that the S3 sleep mode uses a small amount of power, thus extending the life of the battery when backup power is used. *See also* Ex. 1039 at [0065] (describing power saving operations for AMB).

821. A Skilled Artisan would have also understood that, in S3 sleep mode, the registers for capturing the address and command signals are also powered off because the 1.5 volt (VCC) supply is off, and "all command/address outputs, including CKE, ODT, CLK, and all other command/address pins, will be driven low." Ex. 1027 (JESD82-20) at 21 (point 6). Indeed, in S3 sleep mode, the address

and command signals going to the memories are "driven low," thus no address and command signals are sent to the memory devices and there is no need for powering the registers whose function is to register such address and command signals. *Id.* at 39 (Section 4.1.3) (explained that S3 is a "very low power state").

822. Additionally, a Skilled Artisan would also have been familiar with memory systems that switched off their buffer for buffering external command, address, and/or data signals when power has to be saved. For example, U.S. Patent No. 5,563,839 to Herdt ("Herdt") discloses disabling input buffers to reduce current draw in response to a sleep signal. *See* Ex. 1056 at Abstract, 3:5-11 ("Lastly, the preferred embodiment of the present invention includes at least one input buffer for buffering signals being transmitted into the nvSRAM device. The input buffer is known to sink current whenever the input signal being applied to it is at an intermediate level between power supply and ground. The invention provides circuitry for disabling the input buffers in response to a sleep signal."); *see also* Ex. 1057 at Figs. 2-3, 3:45-4:34 (disclosing that a memory device, when running on temporary backup power, transfers data internally from volatile to non-volatile memories and "shuts out any access to the volatile memory … from the outside").

823. Therefore, a Skilled Artisan would have understood from the disclosure of Spiers that, in case of a power failure, the system bus is disconnected

from the module, and there is no need to register address and command signals, because those signals would not be acted upon. Accordingly, a Skilled Artisan would have been motivated to switch off power to the input registers for the system PCI bus (e.g., VCCO) to save power and extend the lifetime of the backup power from the capacitor.

824. A Skilled Artisan would have also understood that the backup power from the capacitor is provided for the SDRAM, NAND Flash, and EEPROM devices of Spiers while data is transferred from the volatile SDRAM devices to the non-volatile NAND flash devices and corresponding configuration information is stored in EEPROM 210. For example, Spiers discloses that "the backup device 144 includes a volatile memory, and a non-volatile memory into which data is moved in the event of a power failure." Ex. 1025 at [0034]. Moreover, in this embodiment, the processor "upon detecting a power failure, switches the backup device 144 to the power supply 168, and moves the data in the volatile memory 160 to the non-volatile memory 164." *Id.* at [0036]. Spiers also describes that "in the event of a power failure the capacitors are used as the power source to power the backup device 144 when moving data from the volatile memory to the non-volatile memory." *Id.* at [0037]. Annotated Figure 14 below depicts this data transfer process.

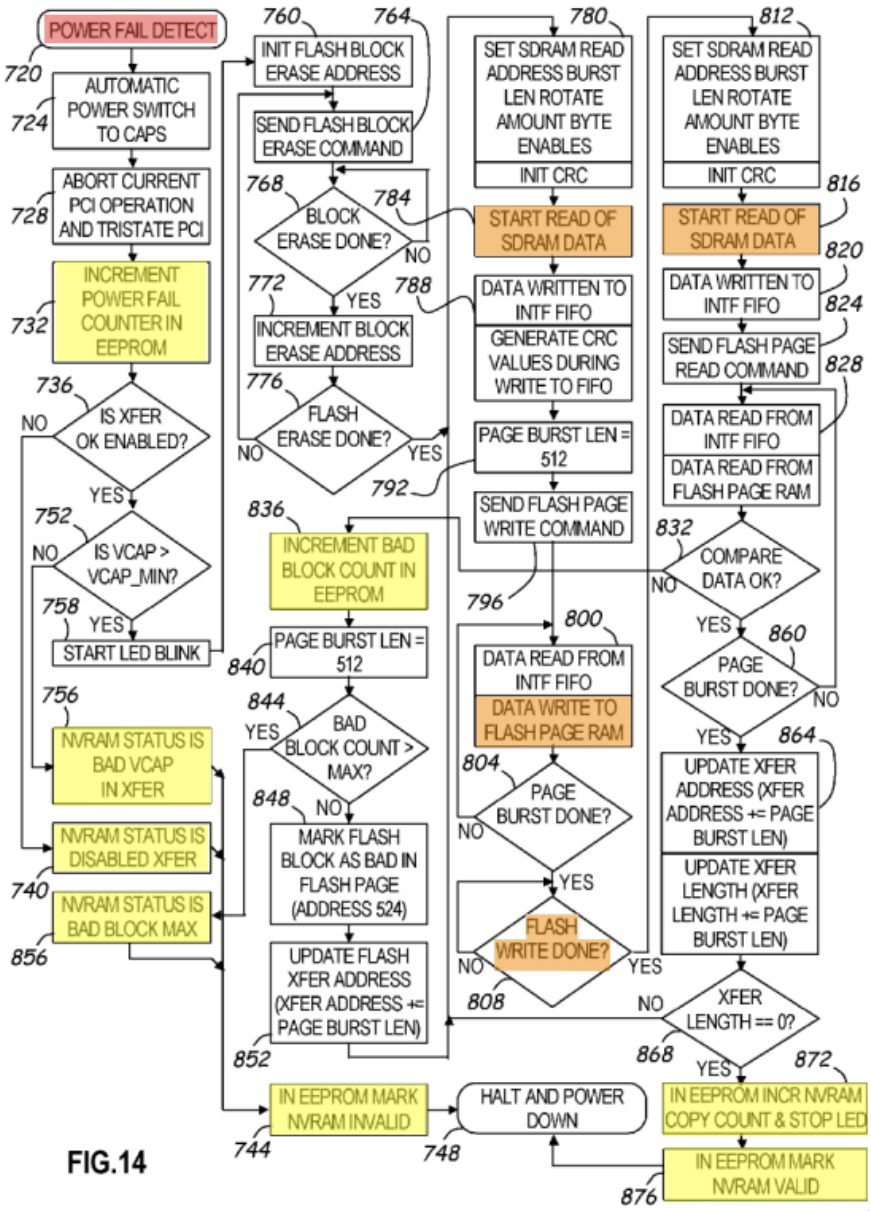


FIG.14

Id. at Fig. 14 (reproduced above with annotations, red indicating the power failure detection, yellow indicating examples of storing information in a non-volatile memory, and orange indicating data transfer from the volatile SDRAM devices to the non-volatile NAND flash devices); *see also id.* at [0054-56] ("The power fail counted in the EEPROM is incremented, according to block 732 … If the transfer

is not enabled, the NVRAM status is set as 'disabled transfer,' as noted at block 740. At block 744, the EEPROM is marked to indicate that the NVRAM is invalid . . .. At block 784, the backup device processor starts the read of SDRAM data. . .. At block 796, the backup device processor sends a flash page write command. The data is then read from the FIFO, and written to the flash page RAM, as noted by block 800….If the comparison indicates that the data is not the same, the backup device processor increments a bad block count in the EEPROM, at noted by block 836. …If the transfer length is zero, the backup device processor increments the NVRAM copy count in the EEPROM and stops the LED blink, as noted at block 872. At block 876, the backup device processor marks the EEPROM to indicate that the NVRAM is valid.").

825. Accordingly, the prior art references in each of Grounds 4 and 5 satisfy "*wherein the one of the first, second, third and fourth regulated voltages is selectively switched off to turn power off to the one or more registers while one or more components of the plurality of components are powered on*."

9. Claim 9 is Unpatentable

826. Claim 9 is unpatentable as the prior art references in each of Grounds 4 and 5 (Voltage Mappings A, B, and C) render the claim obvious.

827. Claim 9 requires "*[t]he memory module of claim 5, wherein the first threshold voltage corresponds to a voltage level that is ten percent greater than a specified operating voltage*."

828. The prior art references in each of Grounds 4 and 5 teach this limitation to a Skilled Artisan.

829. As discussed for claim 7, the prior art references in each of Grounds 4 and 5 satisfy the "*wherein the second threshold voltage corresponds to a voltage level that is ten percent less than a specified operating voltage*" limitation. *Supra* ¶¶790-798. For the same reasons why the "*second threshold voltage*" is "*ten percent less than a specified operating voltage,*" the same combinations render obvious that "*the first threshold voltage corresponds to a voltage level that is ten percent greater than a specified operating voltage*."

830. As discussed for claim 5, to the extent one were to argue that overvoltage protection was not obvious in light of Ground 4, it would have been obvious in light of Hajeck, as part of Ground 5. *Supra* ¶¶779-780.

831. Accordingly, the prior art references in each of Grounds 4 and 5 satisfy the "*wherein the first threshold voltage corresponds to a voltage level that is ten percent greater than a specified operating voltage*" limitation.

10. Claim 10 is Unpatentable

832. Claim 10 is unpatentable as the prior art references in each of Grounds 4 and 5 (Voltage Mappings A, B, and C) render the claim obvious.

a) [10.a] Preamble

833. The preamble of claim 10 requires "*[t]he memory module of claim 5, the plurality of components further comprising*."

834. As explained above for claim 5, the prior art references in each of Grounds 4 and 5 satisfy the limitations of claim 5. *Supra* ¶¶764-780.

835. Accordingly, the prior art references in each of Grounds 4 and 5 satisfy "*[t]he memory module of claim 5, the plurality of components further comprising*."

b) [10.b] A Logic Element

836. Claim 10 requires "*a logic element including a non-volatile memory, the non-volatile memory is configured to store configuration information*."

837. The prior art references in each of Grounds 4 and 5 teach this limitation to a Skilled Artisan.

838. As explained above for claim limitation [8.b.3], Spiers discloses to a Skilled Artisan that its module includes "*a logic element*" implementing the process of Figure 14, including part of the processor 198 and non-volatile memories EEPROM 210 and NAND Flash memory 194, where EEPROM 210 is "*configured to store configuration information*" such as status indicators. *Supra*

¶¶814-825; *see* Ex. 1025 at Fig. 14 (reproduced below with annotations, yellow indicating examples of storing information in a non-volatile memory).

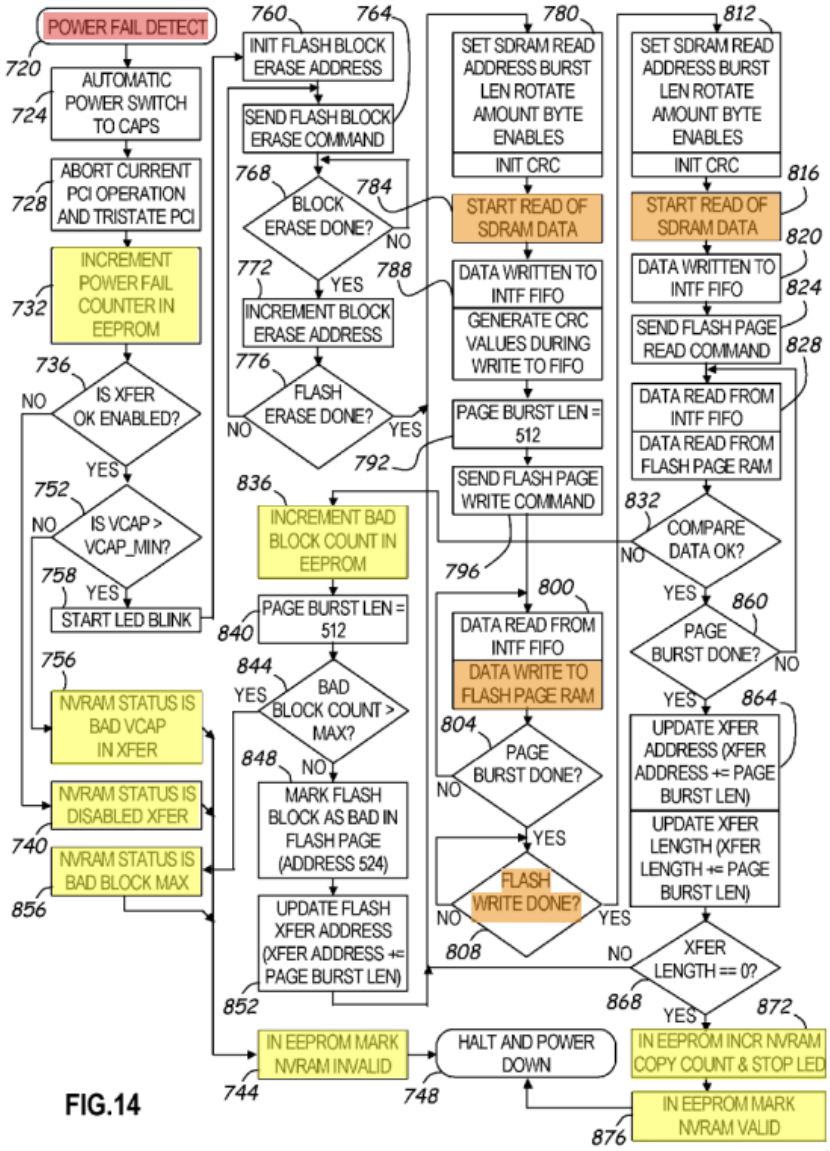


FIG.14

See also id. at [0038] ("An EEPROM 210 is connected to the FPGA processor 198, and is utilized to store various status indicators and counters, which may be utilized during operations. For example, if the backup device 144 restarts following a power failure, the EEPROM indicates that data is stored in the non-volatile

memory of the NAND flash modules 194. Similarly, if the backup device encountered errors that resulted in an aborted attempt to move data from the SDRAM to the NAND flash following a power failure, the EEPROM would indicate that the NVRAM is not valid.").

839. Accordingly, the prior art references in each of Grounds 4 and 5 satisfy "*a logic element including a non-volatile memory, the non-volatile memory is configured to store configuration information*."

11. Claim 11 is Unpatentable

840. Claim 11 is unpatentable as the prior art references in each of Grounds 4 and 5 (Voltage Mappings A, B, and C) render the claim obvious.

841. Claim 11 requires "*[t]he memory module of claim 10, wherein, in response to the trigger signal, the logic element writes information into the non-volatile memory*."

842. The prior art references in each of Grounds 4 and 5 teach this limitation to a Skilled Artisan.

843. As discussed above with reference to claim 10, Spiers discloses to a Skilled Artisan that when the device receives an indication of power failure (i.e., "*the trigger signal*") a part of the processor 198 (i.e., "*the logic element*") writes information including status information and data from the SDRAM devices into

EEPROM 210 and NAND Flash memory 194 (i.e., "*non-volatile memory*"). *Supra* ¶¶833-839; *see* Ex. 1025 at Fig. 14.

844. Accordingly, the prior art references in each of Grounds 4 and 5 satisfy the "*wherein, in response to the trigger signal, the logic element writes information into the non-volatile memory*" limitation.

12. Claim 12 is Unpatentable

845. Claim 12 is unpatentable as the prior art references in each of Grounds 4 and 5 (Voltage Mappings A, B, and C) render the claim obvious.

a) [12.a] Preamble

846. The preamble of claim 12 requires "*[t]he memory module of claim 5, the plurality of components further comprising*."

847. As explained above for claim 5, the prior art references in each of Grounds 4 and 5 satisfy the limitations of claim 5. *Supra* ¶¶764-780.

848. Accordingly, the prior art references in each of Grounds 4 and 5 satisfy "*[t]he memory module of claim 5, the plurality of components further comprising*."

b) [12.b] A Non-Volatile Memory

849. Claim 12 requires "*a non-volatile memory*."

850. The prior art references in each of Grounds 4 and 5 teach this limitation to a Skilled Artisan.

851. As discussed above with reference to claims 10 and 11, Spiers discloses to a Skilled Artisan that when the device receives an indication of power failure, a part of the processor 198 writes information including status information and data from the SDRAM devices into non-volatile memory. *Supra* ¶¶836-839 (claim limitation [10.b]), ¶¶840-844 (claim 11).

852. To the extent Netlist argues that an EEPROM for configuration information is the claimed "*non-volatile memory*," Spiers discloses an EEPROM 210 that is configured to store configuration information such as status indicators. *See id.*; Ex. 1025 at Fig. 14 ("EEPROM"), [0038] ("An EEPROM 210 is connected to the FPGA processor 198, and is utilized to store various status indicators and counters, which may be utilized during operations.").

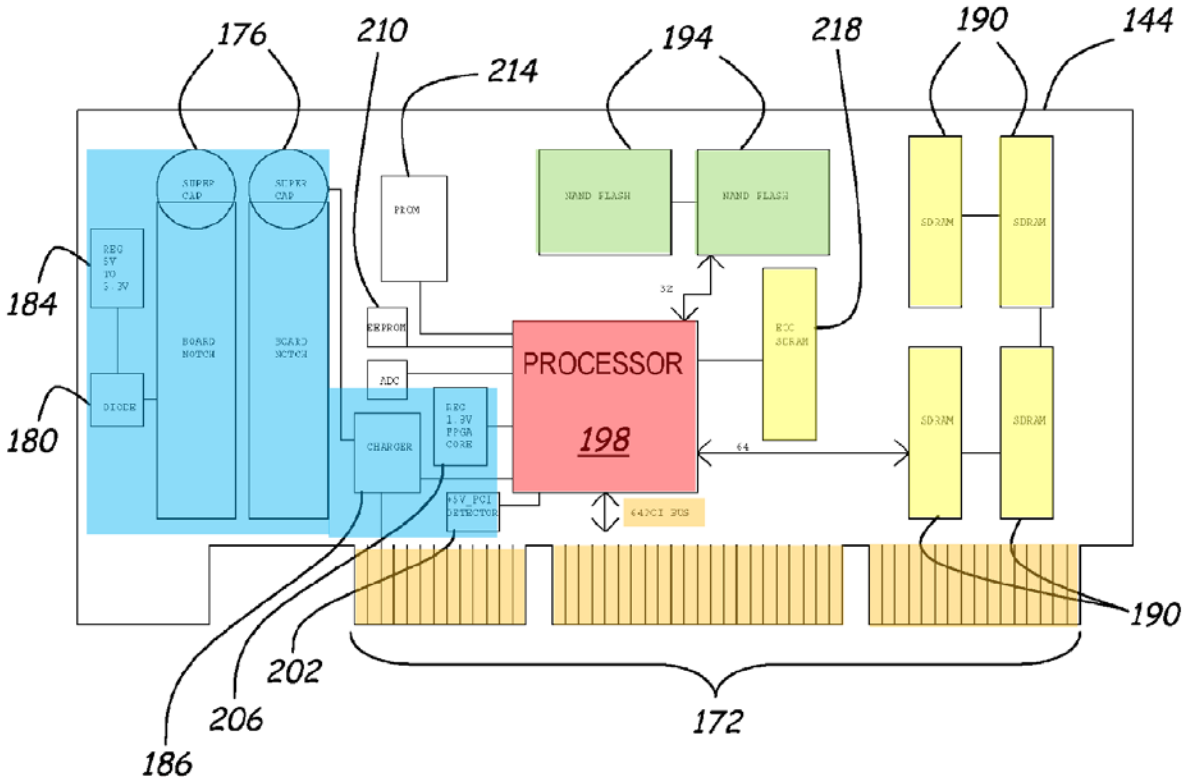
853. To the extent one argues that the claimed "*non-volatile memory*" requires a large array of (e.g., flash) memory for user data, Spiers discloses a module that includes NAND Flash memory 194 ("*non-volatile memory*"). *See* Ex. 1025 at Fig. 14, [0038] ("For example, if the backup device 144 restarts following a power failure, the EEPROM indicates that data is stored in the non-volatile memory of the NAND flash modules 194. Similarly, if the backup device encountered errors that resulted in an aborted attempt to move data from the SDRAM to the NAND flash following a power failure, the EEPROM would indicate that the NVRAM is not valid").

854. Accordingly, the prior art references in each of Grounds 4 and 5 satisfy "*a non-volatile memory*."

c) [12.c] A Controller

855. Claim 12 requires "*a controller configured to receive the trigger signal, wherein, in response to the trigger signal, the controller performs a write operation to the non-volatile memory*."

856. To the extent Netlist asserts that the limitation of "*a write operation to the non-volatile memory*" is satisfied by writing configuration information into a non-volatile memory, the prior art references in each of Grounds 4 and 5 teach this limitation to a Skilled Artisan for the reasons discussed above with reference to claim 10. *Supra* ¶¶836-839 (claim limitation [10.b]). In particular, the processor 198 includes "*a controller*" that receives the trigger signal and, in response, performs a write operation to the non-volatile memory to store configuration data. *See id.* For example, Figure 5 of Spiers shows that the "+5V PCI Detector 202" is coupled to Processor 198, as shown below.



Ex. 1025 at Fig. 5 (annotated); *see also id.* at [0037] ("The FPGA processor 198 utilizes a power detection circuit that, in this embodiment, is a +5V PCI detector 202.").

857. To the extent the limitation of "*a write operation to the non-volatile memory*" requires writing user data from volatile memory to non-volatile memory, the prior art references in each of Grounds 4 and 5 teach this limitation to a Skilled Artisan. In particular, the processor 198 includes "*a controller*" that receives the trigger signal and, in response, "mov[es] data from the volatile memory to the non-volatile memory." *See id.* at [0037]. The volatile memory includes "a number of SDRAM modules 190" and the non-volatile memory includes "a number of

NAND flash memory modules 194." *Id.*; *see also id.*, Fig. 5 (reproduced and annotated above with "SDRAM 190" annotated in yellow and "NAND FLASH 194" annotated in green).

858. A Skilled Artisan would have understood that, through the "64-bit PCI bus," Spiers's module receives address and data with corresponding read or write commands to store or retrieve the user data. Ex. 1025 at [0037]; Ex. 1031 at 1 ("The PCI Local Bus is a high performance 32-bit or 64 bit bus with multiplexed address and data lines"), 7 (Fig. 2-1, reproduced below, describing PCI pins including AD pins for address and data and C/BE pins for bus control signals); *see also id*. at 21-25 (describing C/BE commands for read and write operations).

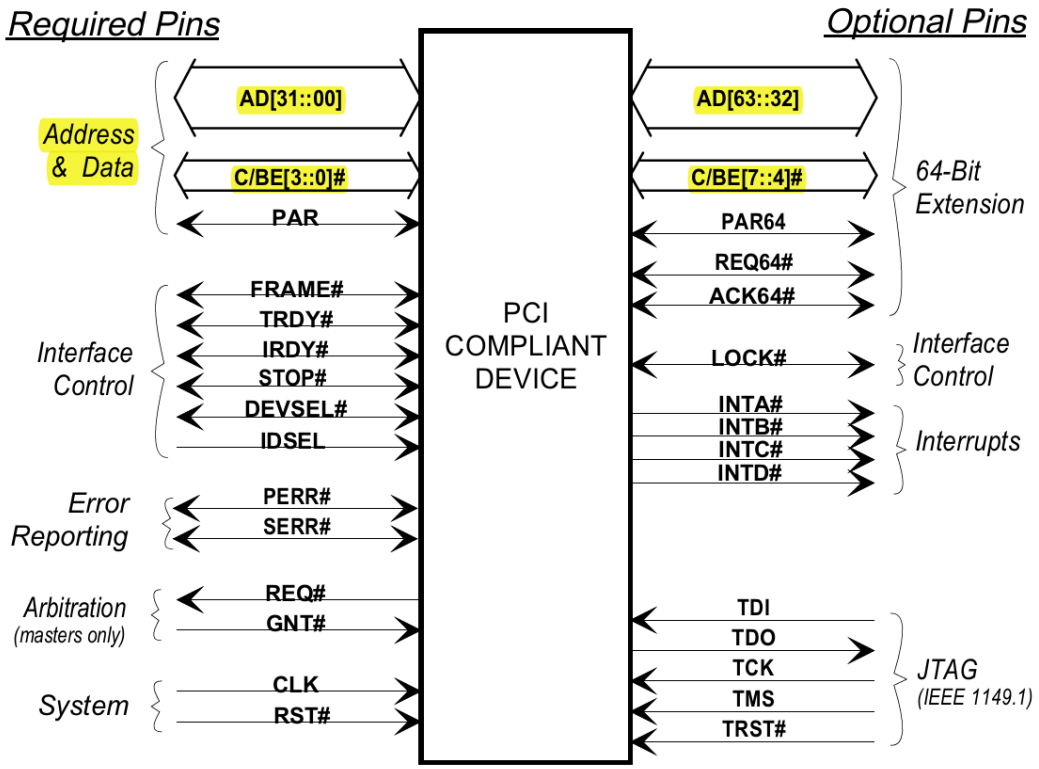


Figure 2-1: PCI Pin List

Spiers also discloses that "the backup device 144 utilizes a descriptor pointer queue contained within the FPGA processor 198 to receive commands from the storage controller." Ex. 1025 at [0039]; *see also id*. at Figs. 9, 10 and 11 (describing operational steps of the backup device processor when receiving commands and transferring data between the host memory and the SDRAMs on the module at corresponding addresses). Further, unlike devices that merely use a storage cache that cannot preserve data in the event of a failure, Spiers teaches that the backup device (144) includes both volatile and nonvolatile memory "into which data is moved in the event of a power failure." *Id.* at [0034]. Thus, Spiers alone and in combination with the references in Grounds 4 and 5 teaches that the processor 198 (includes "*the controller*") performs write operations of user data to the NAND flash 194 ("*performs a write operation to the non-volatile memory*").

859. Accordingly, the prior art references in each of Grounds 4 and 5 satisfy "*a controller configured to receive the trigger signal, wherein, in response to the trigger signal, the controller performs a write operation to the non-volatile memory*."

13. Claim 13 is Unpatentable

860. Claim 13 is unpatentable as the prior art references in each of Grounds 4 and 5 (Voltage Mappings A, B, and C) render the claim obvious.

861. Claim 13 requires "*[t]he memory module of claim 5, wherein the power input voltage is coupled to the first, second, and third buck converters and the converter circuit*."

862. The prior art references in each of Grounds 4 and 5 teach this limitation to a Skilled Artisan.

863. For the reasons discussed above with reference to claim limitations [1.c] ("*a first buck converter . . .*"), [1.d] ("*a second buck converter . . .*"), [1.e] ("*a third buck converter . . .*"), [1.f] ("*a converter circuit . . .*") and claim 5, Spiers in view of Amidi teaches and discloses to a Skilled Artisan that the +5V power input voltage is coupled to the "*first*," "*second*," and "*third buck converter[s]*" and the "*converter circuit*" when the voltage amplitude of the input voltage is in a normal operating range. *Supra* ¶¶655-666 (claim limitation [1.c]), ¶¶668-676 (claim limitation [1.d]), ¶¶677-687 (claim limitation [1.e]), ¶¶689-700 (claim limitation [1.f]), ¶¶764-780 (claim 5).

864. Accordingly, the prior art references in each of Grounds 4 and 5 satisfy the "*wherein the power input voltage is coupled to the first, second, and third buck converters and the converter circuit*" limitation.

14. Claim 14 is Unpatentable

865. Claim 14 is unpatentable as the prior art references in each of Grounds 4 and 5 (Voltage Mappings A, B, and C) render the claim obvious.

866. Claim 14 requires "*[t]he memory module of claim 8, wherein, in response to selectively switching on the one of the first, second, third and fourth regulated voltages to the one or more registers, the one or more registers is configured to output the registered first plurality of address and control signals to the plurality of SDRAM devices*."

867. The prior art references in each of Grounds 4 and 5 teach this limitation to a Skilled Artisan.

868. For the reasons discussed above with reference to claim 8, Spiers discloses to a Skilled Artisan that, when power is restored, control of the SDRAM devices is returned to the system controller so that "*in response to selectively switching on the one of the first, second, third and fourth regulated voltages to the one or more registers, the one or more registers is configured to output the registered first plurality of address and control signals to the plurality of SDRAM devices*." *Supra* ¶¶800-825. For example, Spiers describes that "[f]ollowing the restoration of power after a power failure, power interruption, or other failure that resulted in the backup device storing data in the non-volatile memory, the data may be recovered from the backup device and written to the storage devices associated with the system." Ex. 1025 at [0041]; *see also* Fig. 8 (reproduced below, describing resetting the backup device after a power failure), [0043] (same).

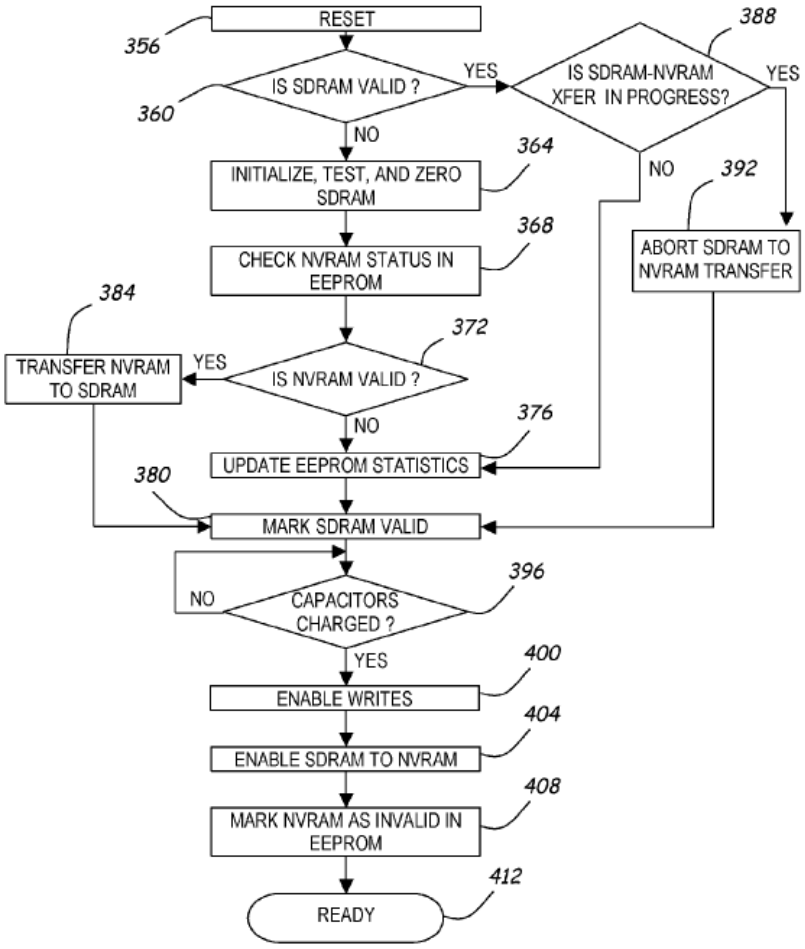


FIG.8

869. Accordingly, the prior art references in each of Grounds 4 and 5 satisfy the "*wherein, in response to selectively switching on the one of the first, second, third and fourth regulated voltages to the one or more registers, the one or more registers is configured to output the registered first plurality of address and control signals to the plurality of SDRAM devices*" limitation.

15. Claim 15 is Unpatentable

870. Claim 15 is unpatentable as the prior art references in each of Grounds 4 and 5 (Voltage Mappings A, B, and C) render the claim obvious.

a) [15.a] Preamble

871. The preamble of Claim 15 requires "*[t]he memory module of claim 1, the plurality of components further comprising*."

872. As explained above for claim 1, the prior art references in each of Grounds 4 and 5 satisfy the limitations of claim 1. *Supra* ¶¶641-738.

873. Accordingly, the prior art references in each of Grounds 4 and 5 satisfy "*[t]he memory module of claim 1, the plurality of components further comprising*."

b) [15.b] A Logic Element

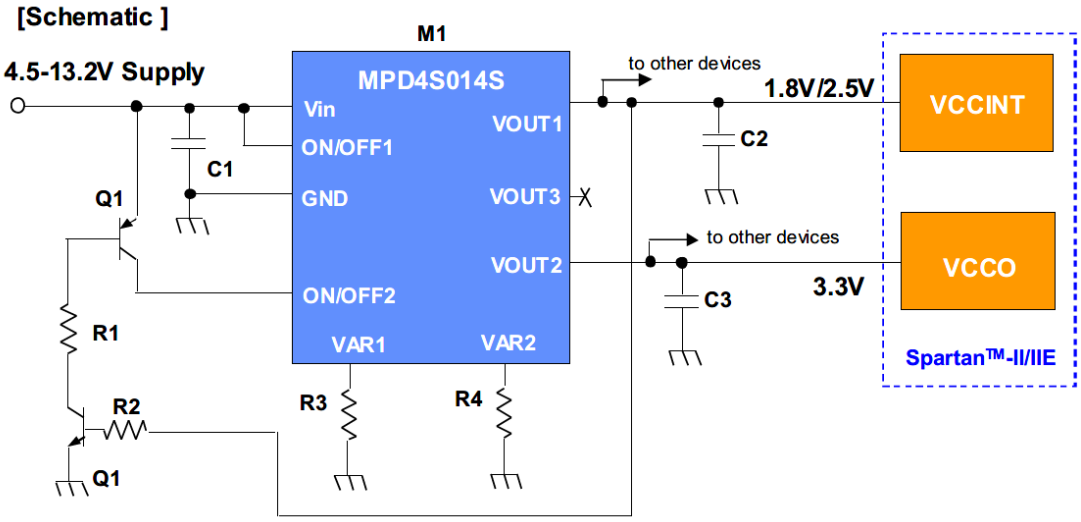
874. Claim 15 requires "*a logic element including one or more integrated circuits and discrete electrical elements, the one or more integrated circuit including an internal non-volatile memory, wherein the non-volatile memory is configured to store configuration information*."

875. The prior art references in each of Grounds 4 and 5 teach this limitation to a Skilled Artisan.

876. As discussed above with reference to claim 10, Spiers discloses to a Skilled Artisan that its module includes "*a logic element*" implementing the process of Figure 14, including "*one or more integrated circuits*" such as parts of

the processor 198 and non-volatile memories EEPROM 210, where EEPROM 210 is "*configured to store configuration information*." *Supra* ¶¶833-839.

877. Spiers further discloses to a Skilled Artisan that the "*logic element*" also includes "*discrete electrical elements*," such as resistors, capacitors as required for interconnections and certain settings. *See, e.g.*, Ex. 1042 at 16 (reproduced below in part, showing capacitors and resistors used for interconnections and settings); *see also* Ex. 1028 (JESD205) at 13 (showing integrated circuits and their connections for an FBDIMM also including capacitors and resistors).



878. To the extent the term "*the one or more integrated circuit including an internal non-volatile memory*" is satisfied by an integrated circuit that includes non-volatile memory and an interface, Spiers discloses such an "*internal non-volatile memory*" as EEPROM 210. Ex. 25 at [0038]. To the extent one might

argue that "*an internal non-volatile memory*" requires that it is integrated with processor 198 of Spiers, it would have been obvious to a Skilled Artisan. Spiers discloses that processor 198 can be implemented as an "FPGA processor." Ex. 1025 at [0037]. A Skilled Artisan would have understood that some commercially available FPGAs at the time had internal non-volatile memories for storing configuration information. Ex. 1067 (LatticeXP Datasheet) at 1-1 (describing FPGA technology with internal non-volatile memory). Furthermore, it would have been obvious to a Skilled Artisan to implement processor 198 with an FPGA having such an internal non-volatile memory because it would decrease the number of components, interfaces and interconnections on the memory module, resulting in a cheaper, faster, and more secure solution. *Id*. at 1 (explaining the advantages FPGA technology with internal non-volatile memory, including "Instant-on—powers up in microseconds," "No external configuration memory," "Excellent design security, no bitstream to intercept") and 2 ("With this [re-programmable non-volatile] technology, expensive external configuration memories are not required and designs are secured from unauthorized read-back. In addition, instant-on capability allows for easy interfacing in many applications."); *see also* Ex. 1023 (Harris) at [0002] (discussing cost-effective support for next generation DRAM technology), [0012] (discussing reduced pins), [0019] (discussing a "reduction in the pin count" and reserving "extra pins for implementing additional

or proprietary functions"); Ex. 1066 at 26:64-27:4 ("In embodiments, modes of operation are determined in response to a control signal from master 2101, or other circuit or in response to reading configuration information ***stored in a separate storage circuit in a device, such as an SPD device or register on the buffer or controller device***, disposed on system 2600. Modes of operation may be determined at initialization, periodically or during calibration of system 2600.") (emphasis added).

879. Accordingly, the prior art references in each of Grounds 4 and 5 satisfy "*a logic element including one or more integrated circuits and discrete electrical elements, the one or more integrated circuit including an internal non-volatile memory, wherein the non-volatile memory is configured to store configuration information*."

16. Claim 16 is Unpatentable

880. Claim 16 is unpatentable as the prior art references in each of Grounds 4 and 5 (Voltage Mappings A, B, and C) render the claim obvious.

a) [16.a] Preamble

881. The preamble of claim 16 requires "*[a] memory module comprising*."

882. The prior art references in each of Grounds 4 and 5 teach this limitation to a Skilled Artisan.

883. As shown in the table below, the preamble of Claim 16 is identical to the preamble Claim 1:

Claim 1	**Claim 16**
[1.a] A memory module comprising:	[16.a] A memory module comprising:

884. As discussed above with reference to claim limitation [1.a], to the extent the preamble of claim 1 is limiting, the prior art references in each of Grounds 4 and 5 satisfy this limitation. *Supra* ¶¶641-646.

b) [16.b] Printed Circuit Board

885. Claim 16 requires "*a printed circuit board (PCB) having an interface configured to fit into a corresponding slot connector of a host system, the interface including a plurality of edge connections configured to couple power, data, address and control signals between the memory module and the host system*."

886. The prior art references in each of Grounds 4 and 5 teach this limitation to a Skilled Artisan.

887. As shown in the table below, claim limitation [16.b] is identical to claim limitation [1.b]:

Claim 1	Claim 16
[1.b] a printed circuit board (PCB) having an interface configured to fit into a corresponding slot connector of a host system, the interface including a plurality of edge connections configured to couple power, data, address and control signals between the memory module and the host system;	[16.b] a printed circuit board (PCB) having an interface configured to fit into a corresponding slot connector of a host system, the interface including a plurality of edge connections configured to couple power, data, address and control signals between the memory module and the host system;

888. As discussed above with reference to claim limitation [1.b], the prior art references in each of Grounds 4 and 5 satisfy this limitation. *Supra* ¶¶647-654.

c) [16.c] First, Second, and Third Buck Converters

889. Claim 16 requires "*first, second, and third buck converters configured to receive a pre-regulated input voltage and to produce first, second and third regulated voltages, respectively*."

890. The prior art references in each of Grounds 4 and 5 teach this limitation to a Skilled Artisan.

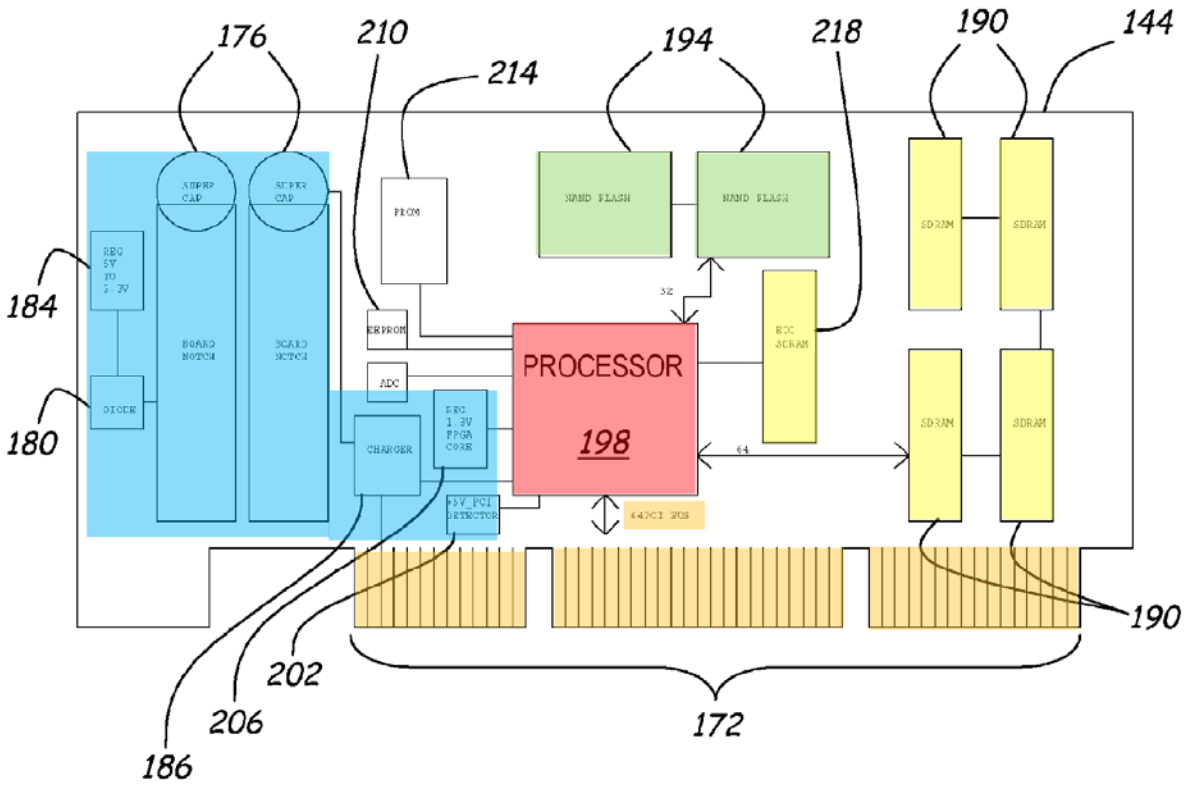
891. As shown in the table below, claim limitation [16.c] is very similar to claim limitations [1.c] – [1.e]:

Claim 1	Claim 16
[1.c] a first buck converter configured to provide a first regulated voltage having a first voltage amplitude; [1.d] a second buck converter configured to provide a second regulated voltage having a second voltage amplitude; [1.e] a third buck converter configured to provide a third regulated voltage having a third voltage amplitude;	[16.c] first, second, and third buck converters configured to receive a pre-regulated input voltage and to produce first, second and third regulated voltages, respectively;

892. For the reasons discussed above with reference to claim limitations [1.c] – [1.e], the prior art references in each of Grounds 4 and 5 satisfy this limitation. *Supra* ¶¶655-688.

893. To the extent the claimed "*pre-regulated input voltage*" can be satisfied by the "*input voltage*" of [16.f] being within pre-determined limits, as suggested by Netlist, *see* Ex. 1071 at 43 (pointing to input voltage received from "Power edge connections"); Ex. 1073 at 49-50 (similar), a Skilled Artisan would have understood that power in the PCI bus of Spiers is within predetermined limits. *See* Ex. 1031 at p.117 (disclosing +5V supply voltage having +/- 0.25V tolerance); *see also* Ex. 1023 at [0013] (disclosing that the input voltage can have a tolerance of +/- 15%).

894. To the extent the claimed "*pre-regulated input voltage*" has to be "pre-regulated" on the memory board itself, *see* Ex. 1001 at 28:53-58, Spiers disclose that, in case of a power failure, power is switched to the capacitors 176 which provide power to the module through the voltage regulator 184, which a Skilled Artisan would have understood provides a regulated voltage. *See* Ex. 1025 at Fig. 5; Ex. 1032 (Mohan) at 161-162 (describing switch-mode converters as being used in "regulated switch-mode dc power supplies" where "the average dc output voltage must be controlled to equal a desired level").



895. Accordingly, the prior art references in each of Grounds 4 and 5 satisfy this limitation.

d) [16.d] A Converter Circuit

(1) [16.d.1] Configured to provide a fourth regulated voltage

896. Claim 16 requires "*a converter circuit configured to reduce the pre-regulated input voltage to provide a fourth regulated voltage*."

897. The prior art references in each of Grounds 4 and 5 teach this limitation to a Skilled Artisan.

898. As shown in the table below, claim limitation [16.d.1] is very similar to claim limitation [1.f]:

Claim 1	**Claim 16**
[1.f] a converter circuit configured to provide a fourth regulated voltage having a fourth voltage amplitude; and	[16.d.1] a converter circuit configured to reduce the pre-regulated input voltage to provide a fourth regulated voltage,

899. As discussed above with reference to claim limitations [1.f] and [16.c], the prior art references in each of Grounds 4 and 5 satisfy this limitation. *Supra* ¶¶689-700 (claim limitation [1.f]), ¶¶889-895 (claim limitation [16.c]).

(2) [16.d.2] Wherein the regulated voltages each have respective amplitudes

900. Claim 16 requires "*wherein the first, second, third and fourth regulated voltages have first, second, third, and fourth voltage amplitudes, respectively*."

901. The prior art references in each of Grounds 4 and 5 teach this limitation to a Skilled Artisan.

902. As shown in the table below, claim limitation [16.d.2] is very similar to claim limitations [1.c] – [1.f]:

Claim 1	**Claim 16**
[1.c] a first buck converter configured to provide a first regulated voltage having a first voltage amplitude; [1.d] a second buck converter configured to provide a second regulated voltage having a second voltage amplitude; [1.e] a third buck converter configured to provide a third regulated voltage having a third voltage amplitude; [1.f] a converter circuit configured to provide a fourth regulated voltage having a fourth voltage amplitude; and	[16.d.2] wherein the first, second, third and fourth regulated voltages have first, second, third, and fourth voltage amplitudes, respectively;

903. As discussed above with reference to claim limitations [1.c] – [1.f], the prior art references in each of Grounds 4 and 5 satisfy this limitation. *Supra* ¶¶655-700.

e) [16.e] A Plurality Of Components Coupled To The PCB

904. Claim 16 requires "*a plurality of components coupled to the PCB, the plurality of components including a plurality of synchronous dynamic random*

access memory (SDRAM) devices, each component of the plurality of components coupled to one or more regulated voltages of the first, second, third and fourth regulated voltages."

905. The prior art references in each of Grounds 4 and 5 teach this limitation to a Skilled Artisan.

906. As shown in the table below, claim limitation [16.e] is very similar to claim limitations [1.g] – [1.h]:

Claim 1	**Claim 16**
[1.g] a plurality of components coupled to the PCB, each component of the plurality of components coupled to one or more regulated voltages of the first, second, third and fourth regulated voltages, the plurality of components comprising: [1.h] a plurality of synchronous dynamic random access memory (SDRAM) devices coupled to the first regulated voltage, and	[16.e] a plurality of components coupled to the PCB, the plurality of components including a plurality of synchronous dynamic random access memory (SDRAM) devices, each component of the plurality of components coupled to one or more regulated voltages of the first, second, third and fourth regulated voltages; and

907. As discussed above with reference to claim limitations [1.g] – [1.h], the prior art references in each of Grounds 4 and 5 satisfy this limitation. *Supra* ¶¶701-718.

f) [16.f] A Voltage Monitor Circuit

908. Claim 16 requires "*a voltage monitor circuit configured to monitor an input voltage received via a first portion of the plurality of edge connections, the*

voltage monitor circuit configured to produce a signal in response to the input voltage having a voltage amplitude that is greater than a first threshold voltage."

909. The prior art references in each of Grounds 4 and 5 teach this limitation to a Skilled Artisan.

910. As shown in the table below, claim limitation [16.f] is very similar to claim limitations [5.a] – [5.b]:

Claim 5	**Claim 16**
[5.a] The memory module of claim 1, further comprising: [5.b] a voltage monitor circuit configured to monitor a power input voltage received via a second portion of the plurality of edge connections, the voltage monitor circuit configured to produce a trigger signal in response to the power input voltage having a voltage amplitude that is greater than a first threshold voltage.	[16.f] a voltage monitor circuit configured to monitor an input voltage received via a first portion of the plurality of edge connections, the voltage monitor circuit configured to produce a signal in response to the input voltage having a voltage amplitude that is greater than a first threshold voltage.

911. In particular, the "*power input voltage received via a second portion of the plurality of edge connections*" in claim 2 corresponds to the "*input voltage received via a first portion of the plurality of edge connections*" in claim 16. As discussed above with reference to claim limitations [5.a] – [5.b], the prior art references in each of Grounds 4 and 5 satisfy this limitation. *Supra* ¶¶764-780.

912. As also discussed for claim limitation [5.b], to the extent one were to argue that overvoltage protection was not obvious in light of Ground 4, it would have been obvious in light of Hajeck, as part of Ground 5. *Supra* ¶¶779-780.

17. Claim 17 is Unpatentable

913. Claim 17 is unpatentable as the prior art references in each of Grounds 4 and 5 (Voltage Mappings A, B, and C) render the claim obvious.

914. Claim 17 requires "*[t]he memory module of claim 16, wherein the second and third buck converters are configured to operate as a dual buck converter*."

915. The prior art references in each of Grounds 4 and 5 teach this limitation to a Skilled Artisan.

916. As shown in the table below, claim 17 is very similar to claim 2:

Claim 2	**Claim 17**
[2] The memory module of claim 1, wherein the first and third buck converters are further configured to operate as a dual buck converter.	[17] The memory module of claim 16, wherein the second and third buck converters are configured to operate as a dual buck converter.

917. In particular, both claims 2 and 17 recite two buck converters that "*are configured to operate as a dual buck converter*." Claim 2 recites the "*first and third buck converters*" and claim 17 recites "*the second and third buck converters*."

918. For the reasons discussed above with reference to claim 2, it would have been obvious to implement the two buck converters as a dual buck converter. *Supra* ¶¶739-746.

919. As shown in the figures below, Ground 4 disclose several voltages that are each provided by a buck converter, as explained for claim limitations [16.c] and [1.c] – [1.e]. *Supra* ¶¶889-895 (claim limitation [16.c]); *see also supra* ¶¶655-688 (claim limitations [1.c] – [1.e]). As previously discussed, Ground 5 has the same Voltage Mappings as Ground 4.

920. For Grounds 4 and 5, there are three mappings for the "*regulated voltage[s]*," as shown in the figure below.

Ground 4: Spiers in view of Amidi, with DDR2 or DDR3 DRAMs

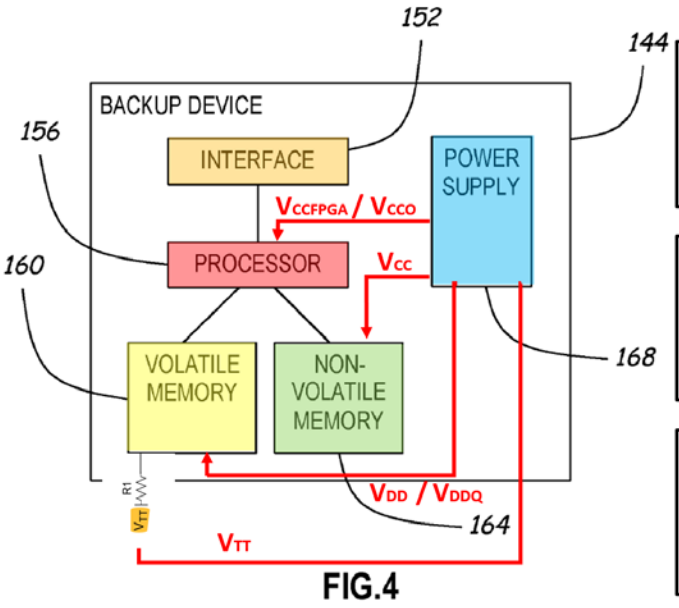


FIG.4

Voltage Mapping (A) for DDR3
1st : V_{DD}/V_{DDQ} to DRAM = 1.5V
2nd : V_{CCFPGA} to FPGA Core = 1.8V
3rd : V_{TT} to Terminate DRAM Bus = 0.75V
4th : V_{CC} to NV Memory / V_{CCO} to FPGA I/O = 3.3V

Voltage Mapping (B) for DDR2
1st : V_{DD}/V_{DDQ} to DRAM = 1.8V
2nd : V_{CCFPGA} to FPGA Core = 1.8V
3rd : V_{TT} to Terminate DRAM Bus = 0.9V
4th : V_{CC} to NV Memory / V_{CCO} to FPGA I/O = 3.3V

Voltage Mapping (C) for DDR2
1st : V_{DD}/V_{DDQ} to DRAM = 1.8V
2nd : V_{CCFPGA} to FPGA Core = 1.8V
3rd : V_{CC} to NV Memory = 3.3V
4th : V_{CCO} to FPGA I/O = 3.3V

921. In all voltage mappings of Grounds 4 and 5, the second voltage is VCCFPGA. In Grounds 4A and 5A, the third voltage is VTT. Likewise, in

Grounds 4B and 5B, the third voltage is VTT. In Grounds 4C and 5C, the third voltage is VCC.

922. In each of the voltage mappings above, a Skilled Artisan would have been motivated with a reasonable expectation of success to use a "*dual buck converter*" to provide the "*second regulated voltage*" and "*third regulated voltage*" for the same reasons discussed above for claim 2 with respect to the "*first*" and "*third*" voltages in Ground 4, including because dual buck converters were commercially available and simplified the design by reducing the number of parts, and the phases of the two voltages could be adjusted relative to each other, thus reducing any input "ripple" and improving performance. *See supra* ¶¶739-746, 338-347. Accordingly, it would have been obvious, in view of the prior art references in each of Grounds 4 and 5, and the knowledge of a Skilled Artisan, to implement the second and third buck converters as a dual buck converter.

18. Claim 18 is Unpatentable

923. Claim 18 is unpatentable as the prior art references in each of Grounds 4 and 5 (Voltage Mappings A, B, and C) render the claim obvious.

a) [18.a] Preamble

924. The preamble of claim 18 requires "*[t]he memory module of claim 16, the plurality of components further including*."

925. The prior art references in each of Grounds 4 and 5 teach this limitation to a Skilled Artisan.

926. As discussed above with reference to claim 16, the prior art references in each of Grounds 4 and 5 satisfy this limitation. *Supra* ¶¶881-911 (claim 16).

b) [18.b] A Controller

927. Claim 18 requires "*a controller coupled to the voltage monitor circuit and configured to receive the signal, wherein the controller executes a write operation in response to the signal*."

928. The prior art references in each of Grounds 4 and 5 teach this limitation to a Skilled Artisan.

929. As shown in the table below, claim limitation [18.b] is very similar to claim limitation [12.c]:

Claim 12	**Claim 18**
[12.c] a controller configured to receive the trigger signal, wherein, in response to the trigger signal, the controller performs a write operation to the non-volatile memory.	[18.b] a controller coupled to the voltage monitor circuit and configured to receive the signal, wherein the controller executes a write operation in response to the signal.

930. As discussed above with reference to claim limitation [12.c], the prior art references in each of Grounds 4 and 5 satisfy this limitation. *Supra* ¶¶855-859.

19. Claim 19 is Unpatentable

931. Claim 19 is unpatentable as the prior art references in each of Grounds 4 and 5 (Voltage Mappings A, B, and C) render the claim obvious.

932. Claim 19 requires "*[t]he memory module of claim 18, wherein the write operation includes writing data information into non-volatile memory*."

933. The prior art references in each of Grounds 4 and 5 teach this limitation to a Skilled Artisan.

934. As shown in the table below, claim 19 is very similar to claim limitation [12.c]:

Claim 12	**Claim 19**
[12.c] a controller configured to receive the trigger signal, wherein, in response to the trigger signal, the controller performs a write operation to the non-volatile memory.	[19] The memory module of claim 18, wherein the write operation includes writing data information into non-volatile memory.

935. As discussed above with reference to claim limitation [12.c], the prior art references in each of Grounds 4 and 5 satisfy this limitation. *Supra* ¶¶855-859.

20. Claim 20 is Unpatentable

936. Claim 20 is unpatentable as the prior art references in Grounds 4 and 5 (Voltage Mappings B and C) render the claim obvious.

937. Claim 20 requires "*[t]he memory module of claim 16, wherein the plurality of SDRAM devices are configured to receive at least one of the first,*

second, third and fourth regulated voltages having a voltage amplitude of 1.8 volts."

938. Spiers in view of Amidi (Voltage Mappings B and C of Grounds 4 and 5) teaches this limitation to a Skilled Artisan.

939. As shown in the table below, claim 20 is very similar to claim limitation [1.h] and claim 3:

Claims 1, 3	**Claim 20**
[1.h] a plurality of synchronous dynamic random access memory (SDRAM) devices coupled to the first regulated voltage [3] The memory module of claim 1, wherein the first voltage amplitude is 1.8 volts.	[20] The memory module of claim 16, wherein the plurality of SDRAM devices are configured to receive at least one of the first, second, third and fourth regulated voltages having a voltage amplitude of 1.8 volts.

940. As discussed above with reference to claim limitation [1.h] and claim 3, Spiers in view of Amidi (Voltage Mappings B and C of Grounds 4 and 5) satisfies this limitation. *Supra* ¶¶714-718 (claim limitation [1.h]), ¶¶747-751 (claim 3).

21. Claim 21 is Unpatentable

941. Claim 21 is unpatentable as the prior art references in each of Grounds 4 and 5 (Voltage Mappings A, B, and C) render the claim obvious.

a) [21.a] Preamble

942. The preamble of claim 21 requires that "*[t]he memory module of claim 16, the plurality of components further including*."

943. The prior art references in each of Grounds 4 and 5 teach this limitation to a Skilled Artisan.

944. As discussed above with reference to claim 16, the prior art references in each of Grounds 4 and 5 satisfy this limitation. *Supra* ¶¶881-911 (claim 16).

b) [21.b] At Least One Circuit

(1) [21.b.1] Coupled between the interface and SDRAM devices

945. Claim 21 requires "*at least one circuit coupled between the interface and the plurality of SDRAM devices*."

946. The prior art references in each of Grounds 4 and 5 teach this limitation to a Skilled Artisan.

947. As shown in the table below, claim limitation [21.b.1] is very similar to claim limitation [1.i.1]:

Claim 1	**Claim 21**
[1.i.1] at least one circuit coupled between a first portion of the plurality of edge connections and the plurality of SDRAM devices,	[21.b.1] at least one circuit coupled between the interface and the plurality of SDRAM devices,

948. As discussed above with reference to claim limitation [1.i.1], the prior art references in each of Grounds 4 and 5 satisfy this limitation. *Supra* ¶¶719-723.

(2) [21.b.2] Operable to receive/output address and control signals

949. Claim 21 requires "*the at least one circuit operable to receive a first plurality of address and control signals via a second portion of the plurality of edge connections and to output a second plurality of address and control signals to the plurality of SDRAM devices*."

950. The prior art references in each of Grounds 4 and 5 teach this limitation to a Skilled Artisan.

951. As shown in the table below, claim limitation [21.b.2] is very similar to claim limitation [1.i.2]:

Claim 1	**Claim 21**
[1.i.2] the at least one circuit operable to (i) receive a first plurality of address and control signals via the first portion of the plurality of edge connections, and (ii) output a second plurality of address and control signals to the plurality of SDRAM devices,	[21.b.2] the at least one circuit operable to receive a first plurality of address and control signals via a second portion of the plurality of edge connections and to output a second plurality of address and control signals to the plurality of SDRAM devices,

952. As discussed above with reference to claim limitation [1.i.2], the prior art references in each of Grounds 4 and 5 satisfy this limitation. *Supra* ¶¶724-729. In particular, the "*a first plurality of address and control signals via the first portion of the plurality of edge connections*" in claim 1 corresponds to the "*a first plurality of address and control signals via a second portion of the plurality of edge connections*" in claim 21.

(3) [21.b.3] Coupled to the second and fourth regulated voltages

953. Claim 21 requires "*the at least one circuit coupled to both the second regulated voltage and the fourth regulated voltage*."

954. The prior art references in each of Grounds 4 and 5 teach this limitation to a Skilled Artisan.

955. As shown in the table below, claim limitation [21.b.3] is very similar to claim limitation [1.i.3]:

Claim 1	**Claim 21**
[1.i.3] the at least one circuit coupled to both the second regulated voltage and the fourth regulated voltage,	[21.b.3] the at least one circuit coupled to both the second regulated voltage and the fourth regulated voltage,

956. As discussed above with reference to claim limitation [1.i.3], the prior art references in each of Grounds 4 and 5 satisfy this limitation. *Supra* ¶¶730-734.

(4) [21.b.4] Wherein one of second and fourth regulated voltage amplitudes is less than the other

957. Claim 21 requires "*wherein a first one of the second and fourth voltage amplitudes is less than a second one of the second and fourth voltage amplitudes*."

958. The prior art references in each of Grounds 4 and 5 teach this limitation to a Skilled Artisan.

959. As shown in the table below, claim limitation [21.b.4] is very similar to claim limitation [1.i.4]:

Claim 1	Claim 21
[1.i.4] wherein a first one of the second and fourth voltage amplitudes is less than a second one of the second and fourth voltage amplitudes.	[21.b.4] wherein a first one of the second and fourth voltage amplitudes is less than a second one of the second and fourth voltage amplitudes.

960. As discussed above with reference to claim limitation [1.i.4], the prior art references in each of Grounds 4 and 5 satisfy this limitation. *Supra* ¶¶735-738.

22. Claim 22 is Unpatentable

961. Claim 22 is unpatentable as the prior art references in each of Grounds 4 and 5 (Voltage Mappings A, B, and C) render the claim obvious.

a) [22.a] Preamble

962. The preamble of claim 22 requires "*[t]he memory module of claim 16, the plurality of components further including*."

963. The prior art references in each of Grounds 4 and 5 teach this limitation to a Skilled Artisan.

964. As discussed above with reference to claim 16, the prior art references in each of Grounds 4 and 5 satisfy this limitation. *Supra* ¶¶881-911 (claim 16).

b) [22.b] A Logic Element

965. Claim 22 requires "*a logic element including an internal non-volatile memory, wherein the non-volatile memory is configured to store configuration*

information, wherein the configuration information is used to program the logic element."

966. The prior art references in each of Grounds 4 and 5 teach this limitation to a Skilled Artisan.

967. As shown in the table below, claim limitation [22.b] is very similar to claim limitations [10.b] and [15.b]:

Claims 10, 15	**Claim 22**
[10.b] a logic element including a non-volatile memory, the non-volatile memory is configured to store configuration information. [15.b] a logic element including one or more integrated circuits and discrete electrical elements, the one or more integrated circuit including an internal non-volatile memory, wherein the non-volatile memory is configured to store configuration information.	[22.b] a logic element including an internal non-volatile memory, wherein the non-volatile memory is configured to store configuration information, wherein the configuration information is used to program the logic element.

968. For the reasons discussed above with reference to claim limitations [10.b] and [15.b], the prior art references in each of Grounds 4 and 5 satisfy this limitation. *Supra* ¶¶836-839 (claim limitation [10.b]), ¶¶874-878 (claim limitation [15.b]). In particular, Spiers discloses to a Skilled Artisan a "*logic element*" (e.g., EEPROM 210 and the part of the processor 198 implementing the process of Figure 14) "*including [a] … non-volatile memory, wherein the non-volatile memory is configured to store configuration information*" (e.g, EEPROM 210),

"*wherein the configuration information* [e.g., status indicators] *is used to program the logic element*" (e.g., to transfer data to non-volatile memory during a power disruption). *See id.* Furthermore, it would have been obvious to a Skilled Artisan to implement processor 198 with an internal non-volatile memory because it would decrease the number of components, interfaces and interconnections on the memory module. *See, e.g.*, Ex. 1067 (LatticeXP datasheet) at 1-2 ("The re-programmable non-volatile technology used in the LatticeXP family is the next generation ispXP™ technology. With this technology, expensive external configuration memories are not required and designs are secured from unauthorized read-back. In addition, instant-on capability allows for easy interfacing in many applications.").

23. Claim 23 is Unpatentable

969. Claim 23 is unpatentable as the prior art references in each of Grounds 4 and 5 (Voltage Mappings A, B, and C) render the claim obvious.

a) [23.a] Preamble

970. The preamble of claim 23 requires "*[a] memory module comprising*."

971. The prior art references in each of Grounds 4 and 5 teach this limitation to a Skilled Artisan.

972. As shown in the table below, claim limitation [23.a] is identical to claim limitation [1.a]:

Claim 1	Claim 23
[1.a] A memory module comprising:	[23.a] A memory module comprising:

973. As discussed above with reference to claim limitation [1.a], to the extent the preamble is limiting, the prior art references in each of Grounds 4 and 5 satisfy this limitation. *Supra* ¶¶641-646.

b) [23.b] A Printed Circuit Board (PCB)

974. Claim 23 requires "*a printed circuit board (PCB) having an interface configured to fit into a corresponding slot connector of a host system, the interface including a plurality of edge connections configured to couple power, data, address and control signals between the memory module and the host system*."

975. The prior art references in each of Grounds 4 and 5 teach this limitation to a Skilled Artisan.

976. As shown in the table below, claim limitation [23.b] is very similar to claim limitation [1.b]:

Claim 1	Claim 23
[1.b] a printed circuit board (PCB) having an interface configured to fit into a corresponding slot connector of a host system, the interface including a plurality of edge connections configured to couple power, data, address and control signals between the memory module and the host system;	[23.b] a printed circuit board (PCB) having an interface configured to fit into a corresponding slot connector of a host system, the interface including a plurality of edge connections configured to couple power, data, address and control signals between the memory module and the host system;

977. As discussed above with reference to claim limitation [1.b], the prior art references in each of Grounds 4 and 5 satisfy this limitation. *Supra* ¶¶647-654.

c) [23.c] A Plurality of Components Coupled To The PCB

(1) [23.c.1] Each component coupled to one or more regulated voltages

978. Claim 23 requires "*a plurality of components coupled to the PCB, each component of the plurality of components coupled to one or more regulated voltages of first, second, third and fourth regulated voltages*."

979. The prior art references in each of Grounds 4 and 5 teach this limitation to a Skilled Artisan.

980. As shown in the table below, claim limitation [23.c.1] is very similar to claim limitation [1.g]:

Claim 1	Claim 23
[1.g] a plurality of components coupled to the PCB, each component of the plurality of components coupled to one or more regulated voltages of the first, second, third and fourth regulated voltages,	[23.c.1] a plurality of components coupled to the PCB, each component of the plurality of components coupled to one or more regulated voltages of first, second, third and fourth regulated voltages,

981. As discussed with reference to claim limitation [1.g], the prior art references in each of Grounds 4 and 5 satisfy this limitation. *Supra* ¶¶701-713.

(2) [23.c.2] Including SDRAM devices and one or more registers

982. Claim 23 requires "*the plurality of components including a plurality of synchronous dynamic random access memory (SDRAM) devices and one or more registers, the plurality of SDRAM devices coupled to the first regulated voltage, the one or more registers coupled to (i) the second regulated voltage, (ii) a portion of the plurality of edge connections, and (iii) the plurality of SDRAM devices*."

983. The prior art references in each of Grounds 4 and 5 teach this limitation to a Skilled Artisan.

984. As shown in the table below, claim limitation [23.c.2] is very similar to claim limitations [1.h], [1.i.1], [1.i.3], and [8.b.1]:

Claims 1, 8	Claim 23
[1.h] a plurality of synchronous dynamic random access memory (SDRAM) devices coupled to the first regulated voltage, and [1.i.1] at least one circuit coupled between a first portion of the plurality of edge connections and the plurality of SDRAM devices [1.i.3] the at least one circuit coupled to both the second regulated voltage and the fourth regulated voltage, [8.b.1] one or more registers coupled to one of the first, second, third and fourth regulated voltages,	[23.c.2] a plurality of synchronous dynamic random access memory (SDRAM) devices and one or more registers, the plurality of SDRAM devices coupled to the first regulated voltage, the one or more registers coupled to (i) the second regulated voltage, (ii) a portion of the plurality of edge connections, and (iii) the plurality of SDRAM devices,

985. As discussed above with reference to claim limitations [1.h], [1.i.1], [1.i.3], and [8.b.1], the prior art references in each of Grounds 4 and 5 satisfy this limitation. *Supra* ¶¶714-718 (claim limitation [1.h]), ¶¶719-723 (claim limitation [1.i.1]), ¶¶730-734 (claim limitation [1.i.3]), ¶¶803-809 (claim limitation [8.b.1]).

(3) [23.c.3] Wherein address and control signals are coupled to one or more registers

986. Claim 23 requires "*wherein a plurality of address and control signals are coupled to the one or more registers via the portion of the plurality of edge connections*."

987. The prior art references in each of Grounds 4 and 5 teach this limitation to a Skilled Artisan.

988. As shown in the table below, claim limitation [23.c.3] is very similar to claim limitations [1.i.2] and [8.b.2]:

Claim 1	**Claim 23**
[1.i.2] the at least one circuit operable to (i) receive a first plurality of address and control signals via the first portion of the plurality of edge connections, and (ii) output a second plurality of address and control signals to the plurality of SDRAM devices [8.b.2] the one or more registers configured to register, in response to a clock, the first plurality of address and control signals	[23.c.3] wherein a plurality of address and control signals are coupled to the one or more registers via the portion of the plurality of edge connections

989. As discussed above with reference to claim limitation [1.i.2] and [8.b.2], the prior art references in each of Grounds 4 and 5 satisfy this limitation. *Supra* ¶¶724-729 (claim limitation [1.i.2]), ¶¶810-813 (claim limitation [8.b.2]).

d) [23.d] First, Second, And Third Buck Converters

990. Claim 23 requires "*first, second, and third buck converters configured to provide the first, second and third regulated voltages, respectively*."

991. The prior art references in each of Grounds 4 and 5 teach this limitation to a Skilled Artisan.

992. As shown in the table below, claim limitation [23.d] is very similar to claim limitations [1.c] – [1.e]:

Claim 1	**Claim 23**
[1.c] a first buck converter configured to provide a first regulated voltage having a first voltage amplitude; [1.d] a second buck converter configured to provide a second regulated voltage having a second voltage amplitude; [1.e] a third buck converter configured to provide a third regulated voltage having a third voltage amplitude;	[23.d] first, second, and third buck converters configured to provide the first, second and third regulated voltages, respectively; and

993. As discussed above with reference to claim limitations [1.c] – [1.e], the prior art references in each of Grounds 4 and 5 satisfy this limitation. *Supra* ¶¶655-688.

e) [23.e] A Converter Circuit

994. Claim 23 requires "*a converter circuit configured to provide the fourth regulated voltage*."

995. The prior art references in each of Grounds 4 and 5 teach this limitation to a Skilled Artisan.

996. As shown in the table below, claim limitation [23.e] is very similar to claim limitation [1.f]:

Claim 1	Claim 23
[1.f] a converter circuit configured to provide a fourth regulated voltage having a fourth voltage amplitude; and	[23.e] a converter circuit configured to provide the fourth regulated voltage,

997. As discussed above with reference to claim limitation [1.f], the prior art references in each of Grounds 4 and 5 satisfy this limitation. *Supra* ¶¶689-700.

f) [23.f] Wherein The Second Regulated Voltage Is Configured To Be Selectively Switched On or Off

998. Claim 23 requires "*wherein the second regulated voltage is configured to be selectively switched on or off to the one or more registers while at least the plurality of SDRAM devices are powered on*."

999. The prior art references in each of Grounds 4 and 5 teach this limitation to a Skilled Artisan.

1000. As shown in the table below, claim limitation [23.f] is very similar to claim limitation [8.b.3] and claim 14:

Claims 8, 14	Claim 23
[8.b.3] wherein the one of the first, second, third and fourth regulated voltages is selectively switched off to turn power off to the one or more registers while one or more components of the plurality of components are powered on. [14] The memory module of claim 8, wherein, in response to selectively switching on the one of the first, second, third and fourth regulated voltages to the one or more registers, the one or more registers is configured to output the registered first plurality of address and control signals to the plurality of SDRAM devices.	[23.f] wherein the second regulated voltage is configured to be selectively switched on or off to the one or more registers while at least the plurality of SDRAM devices are powered on,

1001. As discussed above with reference to claim limitation [8.b.3] and claim 14, the prior art references in each of Grounds 4 and 5 satisfy this limitation. *Supra* ¶¶814-825 (claim limitation [8.b.3]), ¶¶865-869 (claim 14).

g) [23.g] Wherein If The Second Regulated Voltage Is Switched On . . .

1002. Claim 23 requires "*wherein if the second regulated voltage is switched on while at least the plurality of SDRAM devices are powered on, the one or more registers are configured to couple the first plurality of address and control signals to the plurality of SDRAM devices*."

1003. The prior art references in each of Grounds 4 and 5 teach this limitation to a Skilled Artisan.

1004. As shown in the table below, claim limitation [23.g] is very similar to claim 14:

Claim 14	**Claim 23**
[14] The memory module of claim 8, wherein, in response to selectively switching on the one of the first, second, third and fourth regulated voltages to the one or more registers, the one or more registers is configured to output the registered first plurality of address and control signals to the plurality of SDRAM devices.	[23.g] wherein if the second regulated voltage is switched on while at least the plurality of SDRAM devices are powered on, the one or more registers are configured to couple the first plurality of address and control signals to the plurality of SDRAM devices, and

1005. As discussed above with reference to claim 14, the prior art references in each of Grounds 4 and 5 satisfy this limitation. *Supra* ¶¶865-869.

h) [23.h] Wherein If The Second Regulated Voltage Is Switched Off . . .

1006. Claim 23 requires "*wherein if the second regulated voltage is switched off while the plurality of SDRAM devices are powered on, the one or more registers are configured to decouple the plurality of SDRAM devices from the first plurality of address and control signals*."

1007. The prior art references in each of Grounds 4 and 5 teach this limitation to a Skilled Artisan.

1008. As shown in the table below, claim limitation [23.h] is very similar to claim limitation [8.b.3]:

Claim 8	**Claim 23**
[8.b.3] wherein the one of the first, second, third and fourth regulated voltages is selectively switched off to turn power off to the one or more registers while one or more components of the plurality of components are powered on.	[23.h] wherein if the second regulated voltage is switched off while the plurality of SDRAM devices are powered on, the one or more registers are configured to decouple the plurality of SDRAM devices from the first plurality of address and control signals.

1009. As discussed above with reference to claim limitation [8.b.3], the prior art references in each of Grounds 4 and 5 satisfy this limitation. *Supra* ¶¶814-825 (claim limitation [8.b.3]). Furthermore, a Skilled Artisan would have understood that, when the power to the registers is switched off, the registers "*decouple the plurality of SDRAM devices from the first plurality of address and control signals*" because the registers are not powered on and because the address and control lines are grounded in S3 mode. *See, e.g.*, Ex. 1027 (JESD82-20) at 21 (point 6) ("When the Advanced Memory Buffer core logic is in S3 power mode, all command/address outputs, including CKE, ODT, CLK, and all other command/address pins, will be driven low. In S3 mode, 1.8V supply is on. 1.5V, Vtt, and 3.3V are off. DRAMs are in self refresh, and the CKE signals must be driven low.").

24. Claim 24 is Unpatentable

1010. Claim 24 is unpatentable as the prior art references in each of Grounds 4 and 5 (Voltage Mappings A, B, and C) render the claim obvious.

a) [24.a] Preamble

1011. The preamble of claim 24 requires "*[t]he memory module of claim 23, further comprising*."

1012. The prior art references in each of Grounds 4 and 5 teach this limitation to a Skilled Artisan.

1013. As discussed above with reference to claim 23, the prior art references in each of Grounds 4 and 5 satisfy this limitation. *Supra* ¶¶970-1009.

b) [24.b] A Voltage Monitor Circuit

1014. Claim 24 requires "*a voltage monitor circuit configured to monitor an input voltage received from the host system via the interface, the voltage monitor circuit configured to produce a signal in response to the input voltage having a voltage amplitude that is greater than a first threshold voltage*."

1015. The prior art references in each of Grounds 4 and 5 teach this limitation to a Skilled Artisan.

1016. As shown in the table below, claim limitation [24.b] is very similar to claim limitation [5.b]:

Claim 5	Claim 24
[5.b] a voltage monitor circuit configured to monitor a power input voltage received via a second portion of the plurality of edge connections, the voltage monitor circuit configured to produce a trigger signal in response to the power input voltage having a voltage amplitude that is greater than a first threshold voltage.	[24.b] a voltage monitor circuit configured to monitor an input voltage received from the host system via the interface, the voltage monitor circuit configured to produce a signal in response to the input voltage having a voltage amplitude that is greater than a first threshold voltage.

1017. As discussed above with reference to claim limitation [5.b], the prior art references in each of Grounds 4 and 5 satisfy this limitation. *Supra* ¶¶767-780. In particular, to the extent one were to argue that overvoltage protection was not obvious in light of Ground 4, it would have been obvious in light of Hajeck, as part of Ground 5. *Supra* ¶¶779-780.

25. Claim 25 is Unpatentable

1018. Claim 25 is unpatentable as the prior art references in each of Grounds 4 and 5 (Voltage Mappings A, B, and C) render the claim obvious.

a) [25.a] Preamble

1019. The preamble of claim 25 requires "*[t]he memory module of claim 24, the plurality of components further including*."

1020. The prior art references in each of Grounds 4 and 5 teach this limitation to a Skilled Artisan.

1021. As discussed above with reference to claim 24, the prior art references in each of Grounds 4 and 5 satisfy this limitation. *Supra* ¶¶1011-1017.

b) [25.b] A Controller

1022. Claim 25 requires "*a controller coupled to the voltage monitor circuit and configured to receive the signal, wherein, in response to the signal, the controller executes a write operation*."

1023. The prior art references in each of Grounds 4 and 5 teach this limitation to a Skilled Artisan.

1024. As shown in the table below, claim limitation [25.b] is very similar to claim limitation [12.c]:

Claim 12	**Claim 25**
[12.c] a controller configured to receive the trigger signal, wherein, in response to the trigger signal, the controller performs a write operation to the non-volatile memory.	[25.b] a controller coupled to the voltage monitor circuit and configured to receive the signal, wherein, in response to the signal, the controller executes a write operation.

1025. As discussed above with reference to claim limitation [12.c], the prior art references in each of Grounds 4 and 5 satisfy this limitation. *Supra* ¶¶855-859.

26. Claim 26 is Unpatentable

1026. Claim 26 is unpatentable as the prior art references in each of Grounds 4 and 5 (Voltage Mappings A, B, and C) render the claim obvious.

1027. Claim 26 requires "*[t]he memory module of claim 25, wherein the write operation includes writing data information to non-volatile memory*."

1028. The prior art references in each of Grounds 4 and 5 teach this limitation to a Skilled Artisan.

1029. As shown in the table below, claim 26 is very similar to claim limitation [12.c]:

Claim 12	**Claim 26**
[12.c] a controller configured to receive the trigger signal, wherein, in response to the trigger signal, the controller performs a write operation to the non-volatile memory.	[26] The memory module of claim 25, wherein the write operation includes writing data information to non-volatile memory.

1030. As discussed above with reference to claim limitation [12.c], the prior art references in each of Grounds 4 and 5 satisfy this limitation. *Supra* ¶¶855-859.

27. Claim 27 is Unpatentable

1031. Claim 27 is unpatentable as the prior art references in each of Grounds 4 and 5 (Voltage Mappings A, B, and C) render the claim obvious.

1032. Claim 27 requires "*[t]he memory module of claim 24, wherein the voltage monitor circuit is further configured to produce the signal in response to the input voltage having a voltage amplitude that is less than a second threshold voltage*."

1033. The prior art references in each of Grounds 4 and 5 teach this limitation to a Skilled Artisan.

1034. As shown in the table below, claim 27 is very similar to claim 6:

Claim 6	**Claim 27**
[6] The memory module of claim 5, wherein the voltage monitor circuit is further configured to produce the trigger signal in response to the power input voltage having a voltage amplitude that is less than a second threshold voltage.	[27] The memory module of claim 24, wherein the voltage monitor circuit is further configured to produce the signal in response to the input voltage having a voltage amplitude that is less than a second threshold voltage.

1035. As discussed above with reference to claim 6, the prior art references in each of Grounds 4 and 5 satisfy this limitation. *Supra* ¶¶781-789.

28. Claim 28 is Unpatentable

1036. Claim 28 is unpatentable as the prior art references in each of Grounds 4 and 5 (Voltage Mappings A, B, and C) render the claim obvious.

1037. Claim 28 requires "*[t]he memory module of claim 23, wherein the second and third buck converters are configured to operate as a dual buck converter*."

1038. The prior art references in each of Grounds 4 and 5 teach this limitation to a Skilled Artisan.

1039. As shown in the table below, claim 28 is very similar to claim 17:

Claim 2	Claim 28
[17] The memory module of claim 16, wherein the second and third buck converters are configured to operate as a dual buck converter.	[28] The memory module of claim 23, wherein the second and third buck converters are configured to operate as a dual buck converter.

1040. For the reasons discussed above with reference to claim 17, the prior art references in each of Grounds 4 and 5 satisfy this limitation. *Supra* ¶¶913-917.

29. Claim 29 is Unpatentable

1041. Claim 29 is unpatentable as the prior art references in Grounds 4 and 5 (Voltage Mappings B and C) render the claim obvious.

1042. Claim 29 requires "*[t]he memory module of claim 23, wherein the plurality of SDRAM devices are configured to receive at least one of the first, second, third and fourth regulated voltages having a voltage amplitude of 1.8 volts*."

1043. Spiers in view of Amidi (Voltage Mappings B and C of Grounds 4 and 5) teaches this limitation to a Skilled Artisan.

1044. As shown in the table below, claim 29 is very similar to claim 20:

Claim 20	Claim 29
[20] The memory module of claim 16, wherein the plurality of SDRAM devices are configured to receive at least one of the first, second, third and fourth regulated voltages having a voltage amplitude of 1.8 volts.	[29] The memory module of claim 23, wherein the plurality of SDRAM devices are configured to receive at least one of the first, second, third and fourth regulated voltages having a voltage amplitude of 1.8 volts.

1045. As discussed above with reference to claim 20, Voltage Mappings B and C of Grounds 4 and 5 satisfies this limitation. *Supra* ¶¶936-940.

30. Claim 30 is Unpatentable

1046. Claim 30 is unpatentable as the prior art references in each of Grounds 4 and 5 (Voltage Mappings A, B, and C) render the claim obvious.

1047. Claim 30 requires "*[t]he memory module of claim 23, wherein the first, second, and third buck converters are configured to receive a pre-regulated input voltage and to provide the first, second and third regulated voltages, respectively, and wherein the converter circuit is configured to reduce the pre-regulated voltage input to provide the fourth regulated voltage*."

1048. The prior art references in each of Grounds 4 and 5 teach this limitation to a Skilled Artisan.

1049. As shown in the table below, claim 30 is very similar to claim 13 and claim limitations [1.c] – [1.f] and [16.c] – [16.d.1]:

Claims 1, 13	**Claim 16**	**Claim 30**
[1.c] a first buck converter configured to provide a first regulated voltage having a first voltage amplitude; [1.d] a second buck converter configured to provide a second regulated voltage having a second voltage amplitude; [1.e] a third buck converter configured to provide a third regulated voltage having a third voltage amplitude; [1.f] a converter circuit configured to provide a fourth regulated voltage having a fourth voltage amplitude; and [13] The memory module of claim 5, wherein the power input voltage is coupled to the first, second, and third buck converters and the converter circuit.	[16.c] first, second, and third buck converters configured to receive a pre-regulated input voltage and to produce first, second and third regulated voltages, respectively; [16.d.1] a converter circuit configured to reduce the pre-regulated input voltage to provide a fourth regulated voltage,	[30] The memory module of claim 23, wherein the first, second, and third buck converters are configured to receive a pre-regulated input voltage and to provide the first, second and third regulated voltages, respectively, and wherein the converter circuit is configured to reduce the pre-regulated voltage input to provide the fourth regulated voltage.

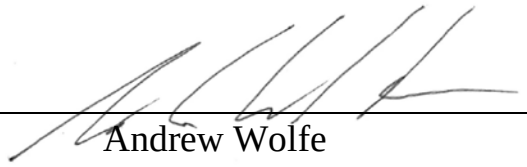
1050. As discussed above with reference to claim 13 and claim limitations [1.c] – [1.f] and [16.c] – [16.d.1], the prior art references in each of Grounds 4 and

5 satisfy this limitation. *Supra* ¶¶655-700 (claim limitations [1.c] – [1.f]), ¶¶860-864 (claim 13), ¶¶889-899 (claim limitations [16.c] – [16.d.1]).

* * *

I, Andrew Wolfe, do hereby declare and state, that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, under Section 1001 of Title 18 of the United States Code.

Executed on: May 16, 2022



Andrew Wolfe

EXHIBIT LIST

Exhibit #	Description
1001	U.S. Patent No. 11,016,918
1002	File History of U.S. Patent No. 11,016,918
1003	Declaration of Dr. Andrew Wolfe
1004	Curriculum Vitae of Dr. Andrew Wolfe
1005	File History of U.S. Provisional Application No. 60/941,586
1006	File History of U.S. Patent Application No. 12/131,873
1007	File History of U.S. Patent Application No. 12/240,916
1008	File History of U.S. Provisional Application No. 61/512,871
1009	File History of U.S. Patent Application No. 13/559,476
1010	File History of U.S. Patent Application No. 14/489,269
1011	File History of U.S. Patent Application No. 14/840,865
1012	File History of U.S. Patent Application No. 15/934,416
1013	[Intentionally Omitted]
1014	*SanDisk Corp. v. Netlist, Inc.*, IPR2014-00994, Paper No. 1 (PTAB June 20, 2014) (833 Patent IPR Petition)
1015	*SanDisk Corp. v. Netlist, Inc.*, IPR2014-00994, Paper No. 8 (PTAB Dec. 16, 2014) (833 Patent Institution Decision)
1016	*Smart Modular Techs. Inc. v. Netlist, Inc.*, IPR2014-01370, Paper No. 8 (PTAB Sept. 22, 2014) (833 Patent IPR Corrected Petition)
1017	*Smart Modular Techs. Inc. v. Netlist, Inc.*, IPR2014-01370, Paper No. 13 (PTAB Mar. 13, 2015) (833 Patent Institution Decision)

Exhibit #	Description
1018	*SK hynix Inc. et al. v. Netlist, Inc*., IPR2017-00649, Paper No. 1 (PTAB Jan. 13, 2017) (833 Patent IPR Petition)
1019	*SK hynix Inc. et al. v. Netlist, Inc*., IPR2017-00649, Paper No. 7 (PTAB July 24, 2017) (833 Patent Institution Decision)
1020	*SK hynix Inc. et al. v. Netlist, Inc*., IPR2017-00692, Paper No. 1 (PTAB Jan. 17, 2017) (831 Patent IPR Petition)
1021	*SK hynix Inc. et al. v. Netlist, Inc*., IPR2017-00692, Paper No. 25 (PTAB July 5, 2018) (831 Patent Final Written Decision)
1022	*Micron Tech., Inc. et al. v. Netlist, Inc.*, IPR2022-00418, Paper No. 2 (PTAB Jan. 14, 2022) (833 Patent IPR Petition)
1023	U.S. Patent Application Publication No. 2006/0174140 to Harris *et al.*
1024	U.S. Patent No. 7,724,604 to Amidi *et al.*
1025	U.S. Patent Application Publication No. 2006/0080515 to Spiers *et al.*
1026	JEDEC Standard, DDR2 SDRAM Specification, JESD79-2B (January 2005) ("JESD79-2B")
1027	JEDEC Standard, FBDIMM: Advanced Memory Buffer (AMB), JESD82-20 (March 2007) ("JESD82-20")
1028	JEDEC Standard, FBDIMM Specification: DDR2 SDRAM Fully Buffered DIMM (FBDIMM) Design Specification, JESD205 (March 2007) ("JESD205")
1029	Declaration of Julie Carlson for JESD82-20 and JESD205
1030	U.S. Patent No. 7,719,866 to Boldo
1031	PCI Local Bus Specification Revision 2.2 (1998)

Exhibit #	Description
1032	Mohan et al., Power Electronics: Converters, Applications, and Design (2d ed. 1995)
1033	U.S. Patent No. 7,721,130 to Prete *et al.*
1034	U.S. Patent No. 6,798,709 to Sim *et al.*
1035	[Intentionally Omitted]
1036	[Intentionally Omitted]
1037	U.S. Patent Application Publication No. 2008/0238536 to Hayashi *et al.*
1038	U.S. Patent No. 6,856,556 to Hajeck
1039	U.S. Patent Application Publication No. 2010/0257304 to Rajan *et al.*
1040	Texas Instruments, TPS51020 Datasheet (December 2003)
1041	Fairchild Semiconductor, FAN5026 Datasheet (October 2005)
1042	Murata Power Supply Reference Guide for Xilinx FPGAs (September 2006)
1043	Murata Power Supply Reference Guide for Altera FPGAs (February 2008)
1044	U.S. Patent Application Publication No. 2010/0205470 to Moshayedi *et al.*
1045	JEDEC Standard, Double Data Rate (DDR) SDRAM Specification, JESD79 (June 2000) ("JESD79")
1046	JEDEC Standard, DDR3 SDRAM, JESD79-3A (September 2007) ("JESD79-3A")
1047	U.S. Patent No. 7,023,187 to Shearon *et al.*

Exhibit #	Description
1048	Murata, DC-DC Converter Specification (DRAFT), MPD4S014S Datasheet (Jan. 21, 2008)
1049	Micron, NAND Flash Memory Datasheet (January 2006)
1050	U.S. Patent No. 7,692,938 to Petter
1051	[Intentionally Omitted]
1052	[Intentionally Omitted]
1053	[Intentionally Omitted]
1054	[Intentionally Omitted]
1055	U.S. Patent Application Publication No. 2008/0101147 to Amidi
1056	U.S. Patent No. 5,563,839 to Herdt *et al.*
1057	U.S. Patent No. 6,693,840 to Shimada *et al.*
1058	Lenk, John D., *Simplified Design of Switching Power Supplies* (1995)
1059	U.S. Patent No. 7,061,214 to Mayega *et al.*
1060	U.S. Patent No. 5,630,096 to Zuravleff *et al.*
1061	Analog Devices, ADM1066 Datasheet (2006)
1062	Alan Moloney, *Power-Supply Management—Principles, Problems, and Parts*, Analog Dialogue (May 2006)
1063	National Semiconductor, LMC6953 PCI Local Bus Power Supervisor Datasheet (October 1996)
1064	U.S. Patent Application Publication No. 2007/0136523 to Bonella *et al.*
1065	U.S. Patent Application Publication No. 2009/0034354 to Resnick

Exhibit #	Description
1066	U.S. Patent No. 10,672,458 to Shaeffer *et al.*
1067	LatticeXP Family Data Sheet (March 2006)
1068	Complaint for Declaratory Judgment of Non-Infringement and Unenforceability; Breach of Contract, *Samsung Electronics Co., Ltd. et al. v. Netlist, Inc.*, No. 1:21-cv-01453 (D. Del. filed Oct. 15, 2021)
1069	First Amended Complaint for Declaratory Judgment of Non-Infringement and Unenforceability; Breach of Contract, *Samsung Electronics Co., Ltd. et al. v. Netlist, Inc.*, No. 1:21-cv-01453 (D. Del. filed Jan. 18, 2022)
1070	Netlist's motion to dismiss the First Amended Complaint, *Samsung Electronics Co., Ltd. et al. v. Netlist, Inc.*, No. 1:21-cv-01453 (D. Del. filed Feb. 16, 2022)
1071	Complaint in *Netlist, Inc. v. Samsung Electronics Co., Ltd. et al.*, No. 2:21-cv-00463 (E.D. Tex. filed Dec. 20, 2021)
1072	Answer in *Netlist, Inc. v. Samsung Electronics Co., Ltd. et al.*, No. 2:21-cv-00463 (E.D. Tex. filed Apr. 12, 2022)
1073	Amended Complaint in *Netlist, Inc. v. Samsung Electronics Co., Ltd. et al.*, No. 2:21-cv-00463 (E.D. Tex. filed May 3, 2022)

CLAIM LISTING

Ref. #	Listing of Challenged Claims
1.a	1. A memory module comprising:
1.b	a printed circuit board (PCB) having an interface configured to fit into a corresponding slot connector of a host system, the interface including a plurality of edge connections configured to couple power, data, address and control signals between the memory module and the host system;
1.c	a first buck converter configured to provide a first regulated voltage having a first voltage amplitude;
1.d	a second buck converter configured to provide a second regulated voltage having a second voltage amplitude;
1.e	a third buck converter configured to provide a third regulated voltage having a third voltage amplitude;
1.f	a converter circuit configured to provide a fourth regulated voltage having a fourth voltage amplitude; and
1.g	a plurality of components coupled to the PCB, each component of the plurality of components coupled to one or more regulated voltages of the first, second, third and fourth regulated voltages, the plurality of components comprising:
1.h	a plurality of synchronous dynamic random access memory (SDRAM) devices coupled to the first regulated voltage, and
1.i	[1] at least one circuit coupled between a first portion of the plurality of edge connections and the plurality of SDRAM devices, [2] the at least one circuit operable to (i) receive a first plurality of address and control signals via the first portion of the plurality of edge connections, and (ii) output a second plurality of address and control signals to the plurality of SDRAM devices, [3] the at least one circuit coupled to both the second regulated voltage and the fourth regulated voltage, [4] wherein a first one of the second and fourth voltage amplitudes is less than a second one of the second and fourth voltage amplitudes.
2	2. The memory module of claim 1, wherein the first and third buck converters are further configured to operate as a dual buck converter.

Ref. #	Listing of Challenged Claims
3	3. The memory module of claim 1, wherein the first voltage amplitude is 1.8 volts.
4	4. The memory module of claim 1, wherein the second, third, and fourth voltage amplitudes are 2.5 volts, 1.2 volts, and 3.3 volts, respectively.
5.a	5. The memory module of claim 1, further comprising:
5.b	a voltage monitor circuit configured to monitor a power input voltage received via a second portion of the plurality of edge connections, the voltage monitor circuit configured to produce a trigger signal in response to the power input voltage having a voltage amplitude that is greater than a first threshold voltage.
6	6. The memory module of claim 5, wherein the voltage monitor circuit is further configured to produce the trigger signal in response to the power input voltage having a voltage amplitude that is less than a second threshold voltage.
7	7. The memory module of claim 6, wherein the second threshold voltage corresponds to a voltage level that is ten percent less than a specified operating voltage.
8.a	8. The memory module of claim 1, the plurality of components further comprising:
8.b	[1] one or more registers coupled to one of the first, second, third and fourth regulated voltages, [2] the one or more registers configured to register, in response to a clock, the first plurality of address and control signals, [3] wherein the one of the first, second, third and fourth regulated voltages is selectively switched off to turn power off to the one or more registers while one or more components of the plurality of components are powered on.
9	9. The memory module of claim 5, wherein the first threshold voltage corresponds to a voltage level that is ten percent greater than a specified operating voltage.
10.a	The memory module of claim 5, the plurality of components further comprising:
10.b	a logic element including a non-volatile memory, the non-volatile memory is configured to store configuration information.

Ref. #	Listing of Challenged Claims
11	11. The memory module of claim 10, wherein, in response to the trigger signal, the logic element writes information into the non-volatile memory.
12.a	12. The memory module of claim 5, the plurality of components further comprising:
12.b	a non-volatile memory; and
12.c	a controller configured to receive the trigger signal, wherein, in response to the trigger signal, the controller performs a write operation to the non-volatile memory.
13	13. The memory module of claim 5, wherein the power input voltage is coupled to the first, second, and third buck converters and the converter circuit.
14	14. The memory module of claim 8, wherein, in response to selectively switching on the one of the first, second, third and fourth regulated voltages to the one or more registers, the one or more registers is configured to output the registered first plurality of address and control signals to the plurality of SDRAM devices.
15.a	15. The memory module of claim 1, the plurality of components further comprising:
15.b	a logic element including one or more integrated circuits and discrete electrical elements, the one or more integrated circuit including an internal non-volatile memory, wherein the non-volatile memory is configured to store configuration information.
16.a	A memory module comprising:
16.b	a printed circuit board (PCB) having an interface configured to fit into a corresponding slot connector of a host system, the interface including a plurality of edge connections configured to couple power, data, address and control signals between the memory module and the host system;
16.c	first, second, and third buck converters configured to receive a pre-regulated input voltage and to produce first, second and third regulated voltages, respectively;

Ref. #	Listing of Challenged Claims
16.d	[1] a converter circuit configured to reduce the pre-regulated input voltage to provide a fourth regulated voltage, [2] wherein the first, second, third and fourth regulated voltages have first, second, third, and fourth voltage amplitudes, respectively;
16.e	a plurality of components coupled to the PCB, the plurality of components including a plurality of synchronous dynamic random access memory (SDRAM) devices, each component of the plurality of components coupled to one or more regulated voltages of the first, second, third and fourth regulated voltages; and
16.f	a voltage monitor circuit configured to monitor an input voltage received via a first portion of the plurality of edge connections, the voltage monitor circuit configured to produce a signal in response to the input voltage having a voltage amplitude that is greater than a first threshold voltage.
17	17. The memory module of claim 16, wherein the second and third buck converters are configured to operate as a dual buck converter.
18.a	18. The memory module of claim 16, the plurality of components further including:
18.b	a controller coupled to the voltage monitor circuit and configured to receive the signal, wherein the controller executes a write operation in response to the signal.
19	19. The memory module of claim 18, wherein the write operation includes writing data information into non-volatile memory.
20	20. The memory module of claim 16, wherein the plurality of SDRAM devices are configured to receive at least one of the first, second, third and fourth regulated voltages having a voltage amplitude of 1.8 volts.
21.a	21. The memory module of claim 16, the plurality of components further including:

Ref. #	Listing of Challenged Claims
21.b	[1] at least one circuit coupled between the interface and the plurality of SDRAM devices, [2] the at least one circuit operable to receive a first plurality of address and control signals via a second portion of the plurality of edge connections and to output a second plurality of address and control signals to the plurality of SDRAM devices, [3] the at least one circuit coupled to both the second regulated voltage and the fourth regulated voltage, [4] wherein a first one of the second and fourth voltage amplitudes is less than a second one of the second and fourth voltage amplitudes.
22.a	22. The memory module of claim 16, the plurality of components further including:
22.b	a logic element including an internal non-volatile memory, wherein the non-volatile memory is configured to store configuration information, wherein the configuration information is used to program the logic element.
23.a	A memory module comprising:
23.b	a printed circuit board (PCB) having an interface configured to fit into a corresponding slot connector of a host system, the interface including a plurality of edge connections configured to couple power, data, address and control signals between the memory module and the host system;
23.c	[1] a plurality of components coupled to the PCB, each component of the plurality of components coupled to one or more regulated voltages of first, second, third and fourth regulated voltages, [2] the plurality of components including a plurality of synchronous dynamic random access memory (SDRAM) devices and one or more registers, the plurality of SDRAM devices coupled to the first regulated voltage, the one or more registers coupled to (i) the second regulated voltage, (ii) a portion of the plurality of edge connections, and (iii) the plurality of SDRAM devices, [3] wherein a plurality of address and control signals are coupled to the one or more registers via the portion of the plurality of edge connections;
23.d	first, second, and third buck converters configured to provide the first, second and third regulated voltages, respectively; and

Ref. #	Listing of Challenged Claims
23.e	a converter circuit configured to provide the fourth regulated voltage,
23.f	wherein the second regulated voltage is configured to be selectively switched on or off to the one or more registers while at least the plurality of SDRAM devices are powered on,
23.g	wherein if the second regulated voltage is switched on while at least the plurality of SDRAM devices are powered on, the one or more registers are configured to couple the first plurality of address and control signals to the plurality of SDRAM devices, and
23.h	wherein if the second regulated voltage is switched off while the plurality of SDRAM devices are powered on, the one or more registers are configured to decouple the plurality of SDRAM devices from the first plurality of address and control signals.
24.a	24. The memory module of claim 23, further comprising:
24.b	a voltage monitor circuit configured to monitor an input voltage received from the host system via the interface, the voltage monitor circuit configured to produce a signal in response to the input voltage having a voltage amplitude that is greater than a first threshold voltage.
25.a	25. The memory module of claim 24, the plurality of components further including:
25.b	a controller coupled to the voltage monitor circuit and configured to receive the signal, wherein, in response to the signal, the controller executes a write operation.
26	26. The memory module of claim 25, wherein the write operation includes writing data information to non-volatile memory.
27	27. The memory module of claim 24, wherein the voltage monitor circuit is further configured to produce the signal in response to the input voltage having a voltage amplitude that is less than a second threshold voltage.
28	28. The memory module of claim 23, wherein the second and third buck converters are configured to operate as a dual buck converter.
29	29. The memory module of claim 23, wherein the plurality of SDRAM devices are configured to receive at least one of the first, second, third and fourth regulated voltages having a voltage amplitude of 1.8 volts.

Ref. #	Listing of Challenged Claims
30	30. The memory module of claim 23, wherein the first, second, and third buck converters are configured to receive a pre-regulated input voltage and to provide the first, second and third regulated voltages, respectively, and wherein the converter circuit is configured to reduce the pre-regulated voltage input to provide the fourth regulated voltage.