PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 8,301,833

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In the *Inter Partes* Review of U.S. Patent No. 8,301,833

Trial No.: Not Yet Assigned

Issued: October 30, 2012

Filed: September 29, 2008

Inventors: Chi-She Chen, *et al.*

Assignee: Netlist, Inc.

Title: NON-VOLATILE MEMORY MODULE

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PETITION FOR *INTER PARTES* REVIEW UNDER 37 C.F.R. § 42.100

On behalf of SanDisk Corporation ("SanDisk" or "Petitioner") and in accordance with 35 U.S.C. § 311 and 37 C.F.R. § 42.100, *inter partes* review is respectfully requested for claims 1-30 of U.S. Patent No. 8,301,833 ("the '833 Patent"), attached hereto as Exhibit 1001.

The undersigned representative of Petitioner authorizes the Patent Office to charge the $31,000 Request and Post-Institution Fees, along with any additional fees, to Deposit Account 501432, ref: 305529-600058. Thirty claims are being reviewed, so the required Request and Post-Institution Fees are $23,000, plus an excess claim fee of $8,000.

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I. INTRODUCTION

The '833 patent is currently being wielded by the patent owner, Netlist, Inc. ("Netlist"), in an attempt to cover long-known memory systems and methods for controlling a memory system. The subject matter claimed in the '833 patent includes standard elements, such as a host system, a volatile memory subsystem, and a non-volatile memory subsystem (*see* '833 patent, claim 1), that were well-known in the prior art before the filing date of the '833 patent. This is evidenced in the "Background" section of the '833 patent, which discloses not only these standard elements, but also first and second modes of operation that are recited in the independent claims of the '833 patent:

> Certain types of memory modules comprise a plurality of dynamic random-access memory (DRAM) devices (*i.e.*, "a volatile memory subsystem") mounted on a printed circuit board (PCB). These memory modules are typically mounted in a memory slot or socket of a computer system (*i.e.*, "a host system") . . . and are accessed by the computer system to provide volatile memory to the computer system (*i.e.*, "a first mode of operation in which data is communicated between the volatile memory subsystem and the host system").
>
> . . .
>
> Non-volatile memory (*i.e.*, "a non-volatile memory subsystem") can generally maintain stored information while power is not applied to the non-volatile memory. . . . [I]t can therefore be useful to backup

> volatile memory using non-volatile memory (*i.e.*, "a second mode of operation in which data is communicated between the volatile memory subsystem and the non-volatile memory subsystem").

('833 patent, 1:15-31, underlined annotations added.)

Unfortunately, the Office was not presented with, nor did it apply, the best prior art during examination of the '833 patent, and Netlist was able to gain allowance based on a single feature that allegedly distinguished over the prior art. Specifically, Netlist argued during prosecution that the prior art did not disclose operating the volatile memory subsystem at two different clock frequencies, with the clock frequency depending on whether the volatile memory subsystem was communicating with the host system or the non-volatile memory subsystem. (Ex. 1011 at 7-15.)

But this feature was not new when the '833 patent was filed, as evidenced by the submission herewith of U.S. Patent Pub. No. 2006/0294295 (Ex. 1013, "Fukuzo") and U.S. Patent No. 7,716,411 (Ex. 1014, "Panabaker"). Both Fukuzo and Panabaker disclose the single feature that was allegedly missing from the prior art – operating the volatile memory subsystem at the two different clock frequencies depending on the mode of operation – as well as all of the other elements of the independent claims of the '833 patent. The dependent claims of the '833 patent add nothing more than well-known concepts that are explicitly disclosed in Fukuzo, Panabaker, or one or more additional prior art references

presented herein. Petitioner submits that had these references been considered by the Patent Office during prosecution, claims 1-30 of the '833 patent would not have issued, and therefore this petition for *inter partes* review should be granted.

II. GROUNDS FOR STANDING PURSUANT TO 37 C.F.R. § 42.104(a)

Petitioner certifies that the '833 patent is available for *inter partes* review and that Petitioner is not barred or estopped from requesting *inter partes* review challenging the patent claims on the grounds identified herein.

III. OVERVIEW OF THE '833 PATENT

The '833 patent was filed on September 29, 2008, and issued on October 30, 2012. The '833 patent is a continuation of U.S. Application No. 12/131,873, filed on June 2, 2008, and claims priority to U.S. Provisional Application No. 60/941,586, filed on June 1, 2007.

The '833 patent is directed to a memory system coupled to a host system where the memory system includes a volatile memory subsystem and a non-volatile memory subsystem. ('833 patent at Abstract, 4:56-61.) The volatile memory subsystem communicates with both the host system and the non-volatile memory subsystem. (*Id.* at 3:60-65.) When data transfer is occurring between the volatile memory subsystem and the host system, the volatile memory subsystem is operated at a first frequency. (*Id.* at 17:50-53.) And when data transfer is occurring between the volatile memory subsystem and the non-volatile memory

subsystem, the non-volatile memory subsystem is operated at a second frequency and the volatile memory subsystem is operated at a third frequency. (*Id.* at 17:53-62; Fig. 9.) The third frequency is less than the first frequency (*id*. at 18:8-10), and the second frequency is equal to the third frequency (*id.*).

Application No. 12/240,916, which later issued as the '833 patent, was originally filed with 54 claims, including seven independent claims. (*See* Ex. 1002 at 32-39.) On March 31, 2011, the Office issued a restriction requirement, identifying four claim groups (Ex. 1003 at 2), and Netlist elected Group III, consisting of claims 37-42 (Ex. 1004 at 9). Independent claim 37 was a method claim that recited three steps: (1) operating a volatile memory subsystem at a first frequency when the memory system is in a first mode of operation in which data is communicated between the volatile memory subsystem and a host system; (2) operating a non-volatile memory subsystem at a second frequency when the memory system is in a second mode of operation in which data is communicated between the volatile memory subsystem and a non-volatile memory subsystem; and (3) operating the volatile memory subsystem at a third frequency when the memory system is in the second mode of operation, the third frequency being less than the first frequency. (*Id*. at 6.)

In a first non-final Office Action, the Office rejected all pending claims as being obvious over U.S. Patent No. 6,336,174 (Ex. 1017, "Li") and U.S. Patent

Pub. No. 2007/0192627 ("Oshikiri"). (Ex. 1004 at 2.) Specifically, the Office found that Li disclosed all features of the independent claims, except for the operation of the memory system at the first, second, and third frequencies. (*Id.* at 2-3.) In response, Netlist did not argue against the Office's application of Li to the claims and instead argued only that Oshikiri did not disclose the first, second, and third frequencies. (Ex. 1006 at 14-15.) In its reply to the first non-final Office Action, Netlist also added new claims 55-91. (*Id.* at 9-13.)

After the claims were again rejected as being obvious over Li and Oshikiri (Ex. 1007), Netlist amended the claims to recite "a first <u>clock</u> frequency," "a second <u>clock</u> frequency," and "a third <u>clock</u> frequency," and argued that these amendments overcame the prior art rejections. (Ex. 1008 at 9-10; *see also* Ex. 1009.) Subsequently, in a second non-final Office Action, the Office rejected all pending claims as being obvious over Li and a new reference, U.S. Patent Pub. No. 2008/0195806 ("Cope"). (Ex. 1010 at 3.) In response, Netlist again did not argue against the application of Li to the claims and only argued that Cope did not disclose the first, second, and third clock frequencies. (Ex. 1011 at 7-15.)

On September 17, 2012, the Office issued a Notice of Allowance, allowing claims 37-42, 61-76, and 83-90. (Ex. 1012.) These claims were then renumbered and issued as claims 1-30 of the '833 patent.

IV. IDENTIFICATION OF CHALLENGE PURSUANT TO 37 C.F.R. § 42.104(b)

A. 37 C.F.R. § 42.104(b)(1): Claims For Which *Inter Partes* Review Is Requested

Inter partes review is requested for claims 1-30 of the '833 patent.

B. 37 C.F.R. § 42.104(b)(2): The Prior Art and Specific Grounds On Which The Challenge to the Claims Is Based

Inter Partes review is requested in view of the following prior art references:

- U.S. Patent Pub. No. 2006/0294295 ("Fukuzo") (Ex. 1013). Fukuzo was filed on June 24, 2005, and published on December 28, 2006, and is prior art to the '833 patent at least under 35 U.S.C. §§ 102(a) and (e).
- U.S. Patent No. 7,716,411 to Panabaker ("Panabaker") (Ex. 1014). Panabaker was filed on June 7, 2006, and issued on May 11, 2010, and is prior art to the '833 patent at least under 35 U.S.C. § 102(e).
- U.S. Patent No. 6,336,174 to Li ("Li") (Ex. 1015). Li was filed on August 9, 1999, and issued on January 1, 2002, and is prior art to the '833 patent under 35 U.S.C. § 102(b).
- U.S. Patent Pub. No. 2006/0080515 ("Spiers") (Ex. 1016). Spiers was filed on October 12, 2004, and published on April 13, 2006, and is prior art to the '833 patent under 35 U.S.C. § 102(b).
- U.S. Patent Pub. No. 2005/0132250 ("Hansen") (Ex. 1017). Hansen was filed on December 16, 2003, and published on June 16, 2005, and is prior

art to the '833 patent under 35 U.S.C. § 102(b).

- U.S. Patent No. 7,102,391 to Sun ("Sun") (Ex. 1018). Sun was filed on July 29, 2004, and issued on September 5, 2006, and is prior art to the '833 patent at least under 35 U.S.C. §§ 102(a) and (e).
- U.S. Patent No. 6,944,042 to Komatsuzaki ("Komatsuzaki") (Ex. 1019). Komatsuzaki was filed on December 31, 2002, and issued on September 13, 2005, and is prior art to the '833 patent under 35 U.S.C. § 102(b).

The specific statutory grounds under 35 U.S.C. §§ 102 or 103 on which the challenge to the claims is based and the patents and publications relied upon for each ground are as follows:

a) Claims 1, 2, 13, 15, 18, and 29 are anticipated by Fukuzo under 35 U.S.C. 102 §§ (a) and (e);

b) Claims 1, 2, 6, 8, 11, 12, 15, 18, 22, 24, 27, and 28 are anticipated by Panabaker under 35 U.S.C. § 102(e);

c) Claims 1-6, 8, 11-13, 15, 17-22, 24, and 27-29 are unpatentable under 35 U.S.C. § 103(a) over Fukuzo and Li;

d) Claims 3 and 19 are unpatentable under 35 U.S.C. § 103(a) over Fukuzo and Spiers;

e) Claims 3 and 19 are unpatentable under 35 U.S.C. § 103(a) over Fukuzo, Li, and Spiers;

f) Claims 7 and 23 are unpatentable under 35 U.S.C. § 103(a) over Fukuzo and Hansen;

g) Claims 7, 9, 10, 23, 25, and 26 are unpatentable under 35 U.S.C. § 103(a) over Fukuzo, Li, and Hansen;

h) Claims 14 and 30 are unpatentable under 35 U.S.C. § 103(a) over Fukuzo and Sun;

i) Claims 14 and 30 are unpatentable under 35 U.S.C. § 103(a) over Fukuzo, Li, and Sun;

j) Claim 16 is unpatentable under 35 U.S.C. § 103(a) over Fukuzo and Komatsuzaki;

k) Claim 16 is unpatentable under 35 U.S.C. § 103(a) over Fukuzo, Li, and Komatsuzaki;

l) Claims 1-6, 8, 11, 12, 15, 17-22, 24, 27, and 28 are unpatentable under 35 U.S.C. § 103(a) over Panabaker and Li;

m) Claims 3 and 19 are unpatentable under 35 U.S.C. § 103(a) over Panabaker and Spiers;

n) Claims 3 and 19 are unpatentable under 35 U.S.C. § 103(a) over Panabaker, Li, and Spiers;

o) Claims 7, 9, 23, and 25 are unpatentable under 35 U.S.C. § 103(a) over Panabaker and Hansen;

p) Claims 7, 9, 10, 23, 25, and 26 are unpatentable under 35 U.S.C. § 103(a) over Panabaker, Li, and Hansen;

q) Claims 13 and 29 are unpatentable under 35 U.S.C. § 103(a) over Panabaker and Fukuzo;

r) Claims 13 and 29 are unpatentable under 35 U.S.C. § 103(a) over Panabaker, Li, and Fukuzo;

s) Claims 14 and 30 are unpatentable under 35 U.S.C. § 103(a) over Panabaker and Sun;

t) Claims 14 and 30 are unpatentable under 35 U.S.C. § 103(a) over Panabaker, Li, and Sun;

u) Claim 16 is unpatentable under 35 U.S.C. § 103(a) over Panabaker and Komatsuzaki; and

v) Claim 16 is unpatentable under 35 U.S.C. § 103(a) over Panabaker, Li, and Komatsuzaki.

C. 37 C.F.R. § 42.104(b)(3): Claim Construction

Pursuant to 37 C.F.R. § 42.100(b), and solely for the purposes of this review, Petitioner construes the claim language such that the claims are given their broadest reasonable interpretation in light of the specification of the '833 patent. Petitioner submits that, for the purposes of this review, each claim should be construed in accordance with its plain and ordinary meaning under the required

broadest reasonable interpretation. Because the standard for claim construction at the Patent Office is different than that used during a U.S. District Court litigation, Petitioner expressly reserves the right to argue a different claim construction in litigation for any term of the '833 patent as appropriate in that proceeding.

D. 37 C.F.R. § 42.104(b)(4): How the Construed Claims are Unpatentable

An explanation of how claims 1-30 are unpatentable, including identification of how each claim feature is found in the prior art, is set forth below in Section V.

E. 37 C.F.R. § 42.104(b)(5): Supporting Evidence

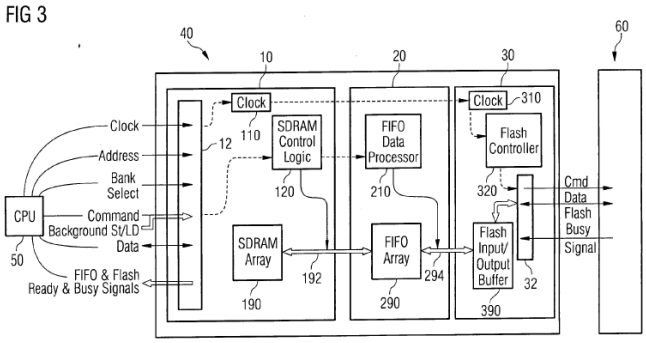
An Appendix of Exhibits supporting this Petition is attached. Included at Exhibit 1020 is a Declaration of Paul Min, Ph.D., under 37 C.F.R. § 1.68.

V. THERE IS A REASONABLE LIKELIHOOD THAT AT LEAST ONE CLAIM OF THE '833 PATENT IS UNPATENTABLE

A. Claims 1, 2, 13, 15, 18, and 29 are Anticipated by Fukuzo (U.S. Patent Pub. No. 2006/0294295)

1. Claims 1 and 15

Fukuzo (Ex. 1013) discloses a synchronous dynamic random access memory (SDRAM) memory chip device that includes i) a volatile SDRAM memory array, and ii) a non-volatile memory controller for transferring data between the volatile SDRAM memory array and a non-volatile memory device (*e.g.*, a NAND-flash device). (Fukuzo, Abstract.) In Fig. 3, volatile SDRAM memory array 190 transfers data to non-volatile flash memory device 60 via flash controller section 30.



The SDRAM memory chip device further includes an SDRAM core section 10 with an interface 12 for transferring data between a central processing unit (CPU) 50 and the volatile SDRAM memory array 190. (*Id.* at ¶ 0082; *see also* Fig. 3.) Thus, in Fukuzo, the volatile memory array 190 transfers data to and receives data from both the host system 50 and the non-volatile memory 60.

The preamble of '833 patent claim 1 recites "[a] method for controlling a memory system operatively coupled to a host system, the memory system including a volatile memory subsystem and a non-volatile memory subsystem." Fukuzo discloses in Fig. 3 a memory system including SDRAM chip device 40 (*i.e.*, "a volatile memory subsystem") and flash memory device 60 (*i.e.*, "a non-volatile memory subsystem"). (Fukuzo at ¶ 0081.) The memory system including the devices 40, 60 is connected to and communicates with the CPU 50 (*i.e.*, "a host system") via the interface 12 (*i.e.*, "[the] memory system operatively coupled to a host system"). (*Id.* at ¶ 0082.)

The first element of claim 1 recites "operating the volatile memory subsystem at a first clock frequency when the memory system is in a first mode of

operation in which data is communicated between the volatile memory subsystem and the host system." A core section 10 of the SDRAM chip device 40 of Fukuzo operates at a clock frequency of 130 MHz (*i.e.*, "operating the volatile memory subsystem at a first clock frequency"). (*Id.* at ¶ 0084.) The core section 10 operates at 130 MHz when it is sending data to and receiving data from the CPU 50 (*i.e.*, "in a first mode of operation in which data is communicated between the volatile memory subsystem and the host system"). (*Id.* at ¶¶ 0082-0084.)

The second element of claim 1 recites "operating the non-volatile memory subsystem at a second clock frequency when the memory system is in a second mode of operation in which data is communicated between the volatile memory subsystem and the non-volatile memory subsystem." Fukuzo discloses that the flash memory device 60 (*i.e.*, "the non-volatile memory subsystem") operates at a clock frequency of 20 MHz (*i.e.*, "a second clock frequency"). (Fukuzo at ¶¶ 0084, 0088.) The flash memory device 60 operates at the clock frequency of 20 MHz when the flash controller section 30 of the SDRAM chip device 40 is sending data to and receiving data from the flash memory device 60 (*i.e.*, "in a second mode of operation in which data is communicated between the volatile memory subsystem and the non-volatile memory subsystem"). (*Id.*)

The third element of claim 1 recites "operating the volatile memory subsystem at a third clock frequency when the memory system is in the second

mode of operation, the third clock frequency being less than the first clock frequency." Fukuzo discloses that the flash controller section 30 of the SDRAM chip device 40 operates at a clock frequency of 20 MHz (*i.e.*, "operating the volatile memory subsystem at a third clock frequency"). (*Id.* at ¶ 0084.) The flash controller section 30 operates at 20 MHz when the flash controller section 30 is sending data to and receiving data from the flash memory 60 (*i.e.*, "in the second mode of operation"). (*Id.* at ¶¶ 0082-0084 and 0088.) The third clock frequency of 20 MHz is less than the first clock frequency of 130 MHz.

The claim chart below along with the referenced Declaration of Dr. Paul Min (Ex. 1020) demonstrate in further detail how Fukuzo anticipates claim 1.

1. A method for controlling a memory system operatively coupled to a host system, the memory system including a volatile memory subsystem and a non-volatile memory subsystem, the method comprising:	Fukuzo discloses this claim element. (*See* Ex. 1020, ¶¶ 120-25.) *See* Fig. 3, reproduced above; *see also* Abstract and ¶¶ 0078 and 0080-0082.
operating the volatile memory subsystem at a first clock frequency when the memory system is in a first mode of operation in which data is communicated between the volatile memory subsystem and	Fukuzo discloses this claim element. (*See* Ex. 1020, ¶¶ 126-30.) ¶ 0084: "The SDRAM core section 10 has a clock generator 110, which generates an internal clock (running at, e.g., 130 MHz) from the incoming clock signals. This clock is valid for the SDRAM core section 10 and the FIFO memory buffer section 20." *See also* ¶¶ 0008, 0082, 0086, 0111, 0112, and Fig. 3 at 110.

the host system;	
operating the non-volatile memory subsystem at a second clock frequency when the memory system is in a second mode of operation in which data is communicated between the volatile memory subsystem and the non-volatile memory subsystem; and	Fukuzo discloses this claim element. (*See* Ex. 1020, ¶¶ 131-35.) ¶¶ 0087-0088: "This latter buffer and register section performs the transfer speed adaption with regard to the slower flash controller clock 310. . . . A standard NAND-flash interface 32 provides the data transfer and the command control to or from the flash memory device 60. Therein, the NAND-flash controller 320, which controls this operation is positioned on the present memory chip device 40." ¶ 0084: "The clock is forwarded to the flash controller section 30, where a flash clock generator 310 generates a flash clock from the SDRAM section clock, which is valid for this section, e.g., at 20 MHz." *See also* ¶¶ 0008, 0019, 0025, 0027, 0085, 0099-0101, 0103, 0114, Fig. 3 at 310, and Fig. 5 ("ST" and "LD").
operating the volatile memory subsystem at a third clock frequency when the memory system is in the second mode of operation, the third clock frequency being less than the first clock frequency.	Fukuzo discloses this claim element. (*See* Ex. 1020, ¶¶ 136-41.) ¶¶ 0084 and 0087-0088, reproduced above. *See also* ¶¶ 0008, 0019, 0025, 0027, 0085, 0099-0101, 0103, 0114, 0125, 0127, Fig. 3 at 310, and Fig. 5 ("ST" and "LD").

Fukuzo anticipates claim 1 under 35 U.S.C. §§ 102(a) and (e). Claim 15 recites a memory system with substantially the same limitations as claim 1, and Fukuzo anticipates claim 15 for the reasons described above. (Ex. 1020, ¶¶ 153-75.)

2. Claims 2 and 18

Claim 2 depends from claim 1 and adds the limitation "wherein the third clock frequency is substantially equal to the second clock frequency." Fukuzo discloses that the flash memory device 60 and the flash controller section 30 both

operate at 20 MHz when data transfer is occurring between the flash controller section and the flash memory device. (*See* Section V.A.1; Ex. 1020, ¶¶ 142-46.)

Fukuzo anticipates claim 2 under 35 U.S.C. §§ 102(a) and (e). Claim 18 depends from claim 15 and recites substantially the same limitations as claim 2, and Fukuzo anticipates claim 18 for the reasons described above. (Ex. 1020, ¶¶ 176-80.)

3. Claim 13 and 29

Claim 13 depends from claim 1 and adds the limitation "wherein one or more of the first, second or third clock frequencies is configurable by the memory system." Fukuzo discloses that the memory system including the devices 40, 60 further includes clock generators 110, 310. (Fukuzo at ¶¶ 0025, 0084; Fig. 3.) The clock generators 110, 310 generate the 130 MHz and 20 MHz clock frequencies (*i.e.*, "the first, second, [and] third clock frequencies"), such that these clock frequencies are configurable by the memory system. (*Id.*; Ex. 1020, ¶¶ 147-52.)

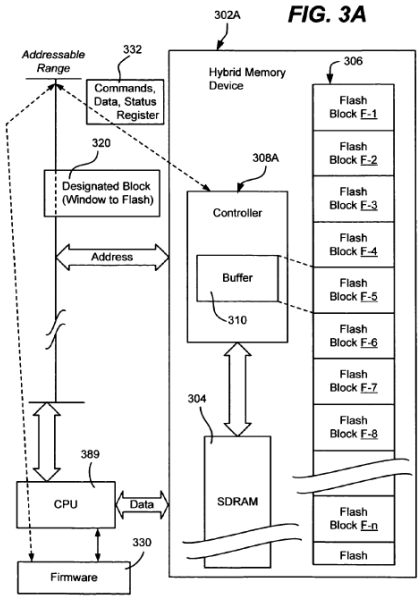
Fukuzo anticipates claim 13 under 35 U.S.C. §§ 102(a) and (e). Claim 29 depends from claim 15 and recites substantially the same limitations as claim 13, and Fukuzo anticipates claim 29 for the reasons described above. (Ex. 1020, ¶¶ 181-86.)

B. Claims 1, 2, 6, 8, 11, 12, 15, 18, 22, 24, 27, and 28 are Anticipated by Panabaker (U.S. Patent No. 7,716,411)

1. Claims 1 and 15

Panabaker discloses a hybrid memory device that includes i) RAM memory devices, and ii) a controller for transferring data from the RAM memory devices to

flash memory. (Panabaker, Abstract and 4:26-64.) For example, in Fig. 3A, RAM devices 304, 310 transfer data to flash memory 306 via controller 308A.



(*Id.* at 4:55-5:25.) Buffer 310 of Fig. 3A is described herein as being a RAM device because Panabaker discloses that its buffers are "SDRAM, DRAM or SRAM" (*id.* at 4:40) and "typically comprise[] memory such as SDRAM or static RAM (SRAM) that is at least as fast as a given SDRAM chip" (*id.* at 4:43-45).

Panabaker's controller 308A is further configured to act as an interface for transferring data between a CPU 389 and the RAM devices 304, 310. (*Id.* at 4:55-5:7.) Thus, in Panabaker, the RAM devices 304, 310 send data to and receive data from both the CPU 389 and the flash memory 306.

The preamble of '833 patent claim 1 recites "[a] method for controlling a memory system operatively coupled to a host system, the memory system including a volatile memory subsystem and a non-volatile memory subsystem."

Panabaker discloses in Fig. 3A a memory system including the RAM devices 304, 310 and the controller 308A (*i.e.*, "a volatile memory subsystem") and the flash memory 306 (*i.e.*, "a non-volatile memory subsystem"). (Panabaker, 4:26-55.) The memory system including these components is connected to and communicates with the CPU 389 (*i.e.*, "a host system") via the controller 308A (*i.e.*, "[the] memory system operatively coupled to a host system"). (*Id.*, 4:55-64.)

The first element of claim 1 recites "operating the volatile memory subsystem at a first clock frequency when the memory system is in a first mode of operation in which data is communicated between the volatile memory subsystem and the host system." Panabaker discloses that the controller 308A operates the buffer 310 and the SDRAM 304 (*i.e.*, parts of the claimed "volatile memory subsystem") at a high clock frequency that "compl[ies] with the SDRAM protocol with respect to speed . . . requirements" (*i.e.*, "operating the volatile memory subsystem at a first clock frequency"). (*Id.*, 1:34-36; 4:33-42, 6:67-7:2, and 12:1-36.) The controller 308A operates the RAM devices 304, 310 at the high clock frequency when these devices are sending data to and receiving data from the CPU 389 (*i.e.*, "in a first mode of operation in which data is communicated between the volatile memory subsystem and the host system"). (*Id.*, 4:26-47, 4:55-61, 4:65-5:7, and 12:1-36.)

The second element of claim 1 recites "operating the non-volatile memory

subsystem at a second clock frequency when the memory system is in a second mode of operation in which data is communicated between the volatile memory subsystem and the non-volatile memory subsystem." Panabaker discloses that the flash memory 306 operates at a low clock frequency (*i.e.*, "a second clock frequency"). (Panabaker, 1:34-36, 4:33-42, 6:32-44, 6:63-67, and 12:1-36.) The flash memory 306 operates at the low clock frequency when data is being transferred between the controller 308A (*i.e.*, part of the "volatile memory subsystem") and the flash memory 306 (*i.e.*, "in a second mode of operation in which data is communicated between the volatile memory subsystem and the non-volatile memory subsystem"). (*Id.*, 5:8-25, 6:19-31, 6:63-67, 12:1-36, 12:43-47.)

The third element of claim 1 recites "operating the volatile memory subsystem at a third clock frequency when the memory system is in the second mode of operation, the third clock frequency being less than the first clock frequency." Panabaker discloses that the controller 308A operates at the low clock frequency (*i.e.*, "operating the volatile memory subsystem at a third clock frequency"). (Panabaker, 1:34-36, 6:19-31, 6:32-44, 6:63-67, 9:5-24, and 12:1-36.) The controller 308A operates at the low clock frequency when data is being transferred between the controller 308A and the flash memory 306 (*i.e.*, "operating . . . at a third clock frequency when the memory system is in the second mode of operation"). (*Id.*, 6:19-31, 6:63-67, 9:5-24, 12:1-36, and 12:43-47.) The low clock

frequency (*i.e.*, "the third clock frequency") is less than the high clock frequency (*i.e.*, "the first clock frequency"). (*See id.* at 1:34-36 and 12:5-6.)

The claim chart below along with the referenced Declaration of Dr. Paul Min (Ex. 1020) demonstrate in further detail how Panabaker anticipates claim 1.

1. A method for controlling a memory system operatively coupled to a host system, the memory system including a volatile memory subsystem and a non-volatile memory subsystem, the method comprising:	Panabaker discloses this claim element. (*See* Ex. 1020, ¶¶ 188-94.) *See* Fig. 3A; *see also* Fig. 2 and Abstract, 1:6-13, 4:26-64, and 2:54-3:3.
operating the volatile memory subsystem at a first clock frequency when the memory system is in a first mode of operation in which data is communicated between the volatile memory subsystem and the host system;	Panabaker discloses this claim element. (*See* Ex. 1020, ¶¶ 195-99.) 4:33-47: ". . . For example, at present SDRAM is significantly faster than flash, and thus a hybrid memory chip that has an interface that appears to external components be an SDRAM device needs to buffer data in the buffer set 210 (e.g., SDRAM, DRAM or SRAM) in order to comply with the SDRAM protocol with respect to speed and output requirements, including burst mode requirements. Thus, the buffer set 210 typically comprises memory such as SDRAM or static RAM (SRAM) that is at least as fast as a given SDRAM chip and its protocol requires. . . ." *See also* 1:34-36, 4:26-32, 4:50-64, 4:65-5:7, 6:32-44, 6:67-7:2, 7:56-60, 11:34-37, 11:47-50, 12:1-36.
operating the non-volatile memory subsystem at a second clock frequency when the memory system is in a second mode of	Panabaker discloses this claim element. (*See* Ex. 1020, ¶¶ 200-04.) 1:34-36: "Moreover, there is a large difference in bus speeds between non-volatile and DRAM-based memory." 6:63-67: "Writes are similarly handled, with the data at the

operation in which data is communicated between the volatile memory subsystem and the non-volatile memory subsystem; and	designated block copied by the controller 308A into the buffer 310, while the controller provides a busy signal that is polled by the firmware until the write request is actually completed by writing to the slower flash." *See also* 4:26-32, 4:33-49, 4:50-64, 4:65-5:7, 5:8-25, 5:63-6:7, 6:19-31, 6:32-44, 8:31-38, 9:5-24, 11:34-37, 11:47-50, 12:1-36, 12:37-42, and 12:42-47.
operating the volatile memory subsystem at a third clock frequency when the memory system is in the second mode of operation, the third clock frequency being less than the first clock frequency.	Panabaker discloses this claim element. (*See* Ex. 1020, ¶¶ 205-08.) 12:1-36: "In a computing device, a system comprising . . . flash-type memory having a speed less than a speed of the DRAM-based memory; . . . a controller having a speed-matching buffer set of at least the speed of the DRAM-based memory; . . . a component that . . . fill[s] the speed-matching buffer set with data . . . [and] output[s] the data from the speed-matching buffer set . . . ." *See also* 1:34-36, 4:26-32, 4:33-49, 4:50-64, 4:65-5:7, 5:8-25, 5:63-6:7, 6:19-31, 6:32-44, 6:63-37, 9:5-24, 11:34-37, 11:47-50, 12:37-42, and 12:42-47.

Panabaker anticipates claim 1 under 35 U.S.C. § 102(e). Independent claim 15 recites a memory system with substantially the same limitations as claim 1, and Panabaker anticipates claim 15 for the reasons described above. (Ex. 1020, ¶¶ 231-50.)

2. Claims 2 and 18

Claim 2 depends from claim 1 and adds the limitation "wherein the third clock frequency is substantially equal to the second clock frequency." As explained above, Panabaker discloses that both the flash memory 306 and the controller 308A operate at a same, low clock frequency when data is being transferred between the controller 308A and the flash memory 306. (*See*

Panabaker 9:16-24 and Section V.B.1 above, discussing disclosure of claim 1 in Panabaker; *see also* Ex. 1020, ¶¶ 209-13.)

Panabaker anticipates claim 2 under 35 U.S.C. § 102(e). Claim 18 depends from claim 15 and recites substantially the same limitations as claim 2, and Panabaker anticipates claim 18 for the reasons described above. (*See* Ex. 1020, ¶¶ 251-55.)

3. Claims 6 and 22

Claim 6 depends from claim 1 and adds the limitation "wherein the memory system further comprises a printed circuit board and the volatile memory subsystem and the non-volatile memory subsystem are located on the printed circuit board." Fig. 9 of Panabaker discloses that DRAM devices and a controller (*e.g.*, controller 308A including the buffer 310 comprising RAM) (*i.e.*, "the volatile memory subsystem") may be located on a DIMM package (*i.e.*, "a printed circuit board") that also includes flash memory (*i.e.*, "the non-volatile memory subsystem"). (Fig. 9, 9:60-67, 2:62-66, and 3:37-67; *see also* Ex. 1020, ¶¶ 214-18.)

Panabaker anticipates claim 6 under 35 U.S.C. § 102(e). Claim 22 depends from claim 15 and recites substantially the same limitations as claim 6, and Panabaker anticipates claim 22 for the reasons described above. (*See* Ex. 1020, ¶¶ 256-60.)

4. Claims 8 and 24

Claim 8 depends from claim 1 and adds the limitation "wherein data communicated between the volatile memory subsystem and the non-volatile

memory subsystem is backup data from a backup operation." Panabaker discloses that an entirety of the data included in SDRAM memory (*i.e.*, "the volatile memory subsystem") is transferred to flash memory (*i.e.*, "the non-volatile memory subsystem"). (Panabaker, 10:1-11.) The data transferred between the SDRAM memory and the flash memory is backup data from a backup operation. (*Id.*; *see also* Ex. 1020, ¶¶ 219-22.)

Panabaker anticipates claim 8 under 35 U.S.C. § 102(e). Claim 24 depends from claim 15 and recites substantially the same limitations as claim 8, and Panabaker anticipates claim 24 for the reasons described above. (*See* Ex. 1020, ¶¶ 261-64.)

5. Claims 11 and 27

Claim 11 depends from claim 1 and adds the limitation "wherein the second mode of operation comprises a backup operation in which data is communicated from the volatile memory subsystem to the non-volatile memory subsystem." The scope of claim 11 is similar to that of claim 8, and Panabaker anticipates claim 11 for reasons similar to those described above in Section V.B.4. (Panabaker, 10:1-11, 8:17-30; *see also* Ex. 1020, ¶¶ 223-26.) Panabaker also discloses that the second mode of operation is entered and exited based on a state of a signal #CE. (*Id.*, 8:31-38.)

Panabaker anticipates claim 11 under 35 U.S.C. § 102(e). Claim 27 depends from claim 15 and recites substantially the same limitations as claim 11, and Panabaker anticipates claim 27 for the reasons described above. (*See* Ex. 1020, ¶¶ 265-68.)

6. Claims 12 and 28

Claim 12 depends from claim 1 and adds the limitation "wherein the second mode of operation comprises a restore operation in which data is communicated from the non-volatile memory subsystem to the volatile memory subsystem." Panabaker discloses that data located in flash memory is transferred to RAM memory for a "boot" or "resume" operation or to load an entire operating system. (Panabaker, 10:1-11.) The communication of such data from the flash memory to the RAM memory comprises "a restore operation." (*Id.*; Ex. 1020, ¶¶ 227-30.)

Panabaker anticipates claim 12 under 35 U.S.C. § 102(e). Claim 28 depends from claim 15 and recites substantially the same limitations as claim 12, and Panabaker anticipates claim 28 for the reasons described above. (*See* Ex. 1020, ¶¶ 269-72.)

C. Claims 1-6, 8, 11-13, 15, 17-22, 24, and 27-29 are Unpatentable Under 35 U.S.C. § 103(a) over Fukuzo and Li (U.S. Patent No. 6,336,174)

1. Claims 1 and 15

As discussed above, Fukuzo discloses all limitations of claim 1. (*See* Section V.A.1.) To the extent it could be argued that any further disclosure may be required with respect to the claimed "first mode of operation" and "second mode of operation," Li (Ex. 1015) provides such further disclosure. (Ex. 1020, ¶¶ 274-78.)

Li discloses a hardware assisted memory module (HAMM) 104 (*i.e.*, "a memory system") coupled to a client (*i.e.*, "a host system"). (Li, Fig. 1.) As illustrated in Fig. 2 of Li, the HAMM 104 includes volatile memory 202 (*i.e.*, "a

volatile memory subsystem") and non-volatile memory 204 (*i.e.*, "a non-volatile memory subsystem"). Data is written from the client to volatile memory 202 during a normal mode of operation (*i.e.*, "the memory system is in a first mode of operation in which data is communicated between the volatile memory subsystem and the host system"). (*Id.*, 5:55-57.) If a trigger event occurs, the HAMM 104 enters a backup mode of operation and data is written from the volatile memory 202 to the non-volatile memory 204 (*i.e.*, "the memory system is in a second mode of operation in which data is communicated between the volatile memory subsystem and the non-volatile memory subsystem"). (*Id.*, 5:67-6:3.)

The claim chart below along with the referenced Declaration of Dr. Paul Min (Ex. 1020) demonstrate in further detail how Li provides such disclosure for claim 1. The Office previously found that Li disclosed these claim limitations, and this finding was not disputed by Netlist. (*See* Ex. 1010 at 3-4; *see also* Exs. 1006, 1008, 1011.)

1. . . . a first mode of operation in which data is communicated between the volatile memory subsystem and the host system;	Li discloses this claim element. (*See* Ex. 1020, ¶¶ 274-76.) 5:55-67: "In accordance with the operation of host system 100, a client computer (not shown) communicates with host system 100 via network interface 108. Depending on the communication protocol (e.g., TCP/IP), if a client computer wants to store data in disk storage 114, the client computer sends a 'write' request to host system 100. Upon acceptance of the client's 'write' request, host system 100 receives data over the network and stores the data in volatile memory. Once the data is in volatile memory, host system 100 signals back to the client computer that the 'write' transaction has

	been completed. . . ." Abstract: "During normal operation of the computer system, the HAMM behaves like a conventional memory module." *See also* 6:48-57 and 3:5-9.
. . . a second mode of operation in which data is communicated between the volatile memory subsystem and the non-volatile memory subsystem	Li discloses this claim element. (*See* Ex. 1020, ¶¶ 277-78.) 5:67-6:3: "If a catastrophic event occurs while all or some of the data is still in volatile memory, the HAMM 104 copies all or some of the data to nonvolatile memory to prevent data loss, as described below with respect to FIG. 2." Abstract: "Upon detection of a trigger event, the HAMM electronically isolates itself from the host computer system before copying digital information from volatile memory to nonvolatile memory." *See also* 9:49-67.

Motivation to Combine

A person of ordinary skill in the art (POSITA) would have been motivated to combine Li's teachings with Fukuzo because both references are related to hybrid memory systems including volatile and non-volatile memory subsystems, such that the similar purposes and overlapping teachings would have motivated the POSITA to combine the teachings of the references. As another example, the POSITA would have been motivated to supplement Fukuzo's hybrid memory system with the teachings of Li regarding a trigger event that causes a hybrid memory system to enter a backup mode of operation in which data is transferred from volatile to non-volatile memory. Specifically, the POSITA would have recognized the disadvantage of the volatility of Fukuzo's DRAM array and would have been motivated to supplement Fukuzo with

Li's teachings of a backup mode of operation to lower the risk that data could be lost. Further, the use of non-volatile memory to backup volatile memory in response to a trigger condition was well-known at the time of the alleged invention of the '833 patent (*see*, *e.g.*, Ex. 1021; *see also* Ex. 1020, ¶¶ 279, 286).

Claim 1 is obvious over Fukuzo and Li. Independent claim 15 recites a memory system with substantially the same limitations as claim 1, and claim 15 is obvious over Fukuzo and Li for the reasons described above. (*See* Ex. 1020, ¶¶ 281-87.)

2. Claims 2 and 18

Claim 2 depends from claim 1, which, as discussed above, is obvious over Fukuzo and Li. Fukuzo discloses the additional limitations in claim 2 (*see* Section V.A.2), which accordingly is obvious over Fukuzo and Li. (*See* Ex. 1020, ¶¶ 288-93.) Li is combinable with Fukuzo for the reasons stated in Section V.C.1. (*See also* Ex. 1020 ¶¶ 279, 286.) Claim 18 depends from claim 15 and recites substantially the same limitations as claim 2, and claim 18 is obvious over Fukuzo and Li for the reasons described above. (*See* Ex. 1020, ¶¶ 288-93.)

3. Claims 3 and 19

Claim 3 depends from claim 1, which, as discussed above, is obvious over Fukuzo and Li. Li discloses the limitations added in claim 3, "wherein the memory system is not powered by a battery when it is in the second mode of operation." Specifically, Li discloses that when an operating system (O/S) hang-up

event causes the memory system to enter a backup mode (*i.e.*, "the second mode of operation"), an auxiliary battery is not used to power the memory system during the backup mode. (Li, 7:58-8:15; *see also* Ex. 1020, ¶¶ 294-97.) The Office previously found that Li disclosed these claim limitations, and this finding was not disputed by Netlist. (*See* Ex. 1010 at 5; *see also* Exs. 1006, 1008, 1011.)

Accordingly, claim 3 is obvious over Fukuzo and Li. Li is combinable with Fukuzo for the reasons stated in Section V.C.1 and for the reasons indicated in Ex. 1020, ¶¶ 279, 286, 298. Claim 19 depends from claim 15 and recites substantially the same limitations as claim 3, and claim 19 is obvious over Fukuzo and Li for the reasons described above. (*See* Ex. 1020, ¶¶ 294-98.)

4. Claims 4 and 20

Claim 4 depends from claim 1, which, as discussed above, is obvious over Fukuzo and Li. Li discloses the limitations added in claim 4, "wherein the memory system switches from the first mode of operation to the second mode of operation in response to a trigger condition." Li discloses trigger events (*e.g.*, power failure, O/S hang-up, unexpected system reset) that cause data to be transferred from volatile memory to non-volatile memory. (Li, Abstract; *see also* Ex. 1020, ¶¶ 299-302.) The Office previously found that Li disclosed these claim limitations, and this finding was not disputed by Netlist. (*See* Ex. 1010 at 5-6; *see also* Exs. 1006, 1008, 1011.)

Accordingly, claim 4 is obvious over Fukuzo and Li. Li is combinable with Fukuzo for the reasons stated in Section V.C.1 and for the reasons indicated in Ex. 1020, ¶¶ 279, 286, 303. Claim 20 depends from claim 15 and recites substantially the same limitations as claim 4, and claim 20 is obvious over Fukuzo and Li for the reasons described above. (*See* Ex. 1020, ¶¶ 299-303.)

5. Claims 5 and 21

Claim 5 depends from claim 4, which, as discussed above, is obvious over Fukuzo and Li. Li discloses the limitations added in claim 5, "wherein the trigger condition comprises a power failure condition." Specifically, Li discloses a power failure trigger event. (Li, Abstract; *see also* Ex. 1020, ¶¶ 304-07.) The Office previously found that Li disclosed this claim limitation, and this finding was not disputed by Netlist. (*See* Ex. 1010 at 6; *see also* Exs. 1006, 1008, 1011.)

Accordingly, claim 5 is obvious over Fukuzo and Li. Li is combinable with Fukuzo for the reasons stated in Section V.C.1 and for the reasons indicated in Ex. 1020, ¶¶ 279, 286, 308. Claim 21 depends from claim 20 and recites substantially the same limitations as claim 5, and claim 21 is obvious over Fukuzo and Li for the reasons described above. (*See* Ex. 1020, ¶¶ 304-08.)

6. Claims 6 and 22

Claim 6 depends from claim 1, which, as discussed above, is obvious over Fukuzo and Li. Li discloses the limitations added in claim 6, "wherein the

memory system further comprises a printed circuit board and the volatile memory subsystem and the non-volatile memory subsystem are located on the printed circuit board." Li discloses that the HAMM 104, including both the volatile and non-volatile memories 202, 204, is located on a DIMM package (*i.e.*, "a printed circuit board"). (Li, 5:46-52, 2:44-51, 2:58-3:4, and Fig. 2; *see also* Ex. 1020, ¶¶ 309-12.) The Office previously found that Li disclosed these claim limitations, and this finding was not disputed by Netlist. (Ex. 1010 at 6; Exs. 1006, 1008, 1011.)

Accordingly, claim 6 is obvious over Fukuzo and Li. Li is combinable with Fukuzo for the reasons stated in Section V.C.1 and for the reasons indicated in Ex. 1020, ¶¶ 279, 286, 313. Claim 22 depends from claim 15 and recites substantially the same limitations as claim 6, and claim 22 is obvious over Fukuzo and Li for the reasons described above. (*See* Ex. 1020, ¶¶ 309-13.)

7. Claims 8 and 24

Claim 8 depends from claim 1, which, as discussed above, is obvious over Fukuzo and Li. Li discloses the limitations added in claim 8, "wherein data communicated between the volatile memory subsystem and the non-volatile memory subsystem is backup data from a backup operation." Li discloses that the copying of data from volatile memory to non-volatile memory is data from a "memory backup operation." (Li, 3:10-16, 9:49-67; *see* Ex. 1020, ¶¶ 314-17.) The Office previously found that Li disclosed these claim limitations, and this finding

was not disputed by Netlist. (*See* Ex. 1010 at 6-7; *see also* Exs. 1006, 1008, 1011.)

Accordingly, claim 8 is obvious over Fukuzo and Li. Li is combinable with Fukuzo for the reasons stated in Section V.C.1 and for the reasons indicated in Ex. 1020, ¶¶ 279, 286, 318. Claim 24 depends from claim 15 and recites substantially the same limitations as claim 8, and claim 24 is obvious over Fukuzo and Li for the reasons described above. (*See* Ex. 1020, ¶¶ 314-18.)

8. Claims 11 and 27

Claim 11 depends from claim 1 and adds the limitation "wherein the second mode of operation comprises a backup operation in which data is communicated from the volatile memory subsystem to the non-volatile memory subsystem." Li discloses that the copying of data from volatile memory to non-volatile memory is data from a "memory backup operation." (Li, 3:10-16, 9:49-67; *see* Ex. 1020, ¶¶ 319-22.) The Office previously found that Li disclosed these limitations, and this finding was not disputed by Netlist. (*See* Ex. 1010 at 7; Exs. 1006, 1008, 1011.)

Accordingly, claim 11 is obvious over Fukuzo and Li. Li is combinable with Fukuzo for the reasons stated in Section V.C.1 and for the reasons indicated in Ex. 1020, ¶¶ 279, 286, 323. Claim 27 depends from claim 15 and recites substantially the same limitations as claim 11, and claim 27 is obvious over Fukuzo and Li for the reasons described above. (*See* Ex. 1020, ¶¶ 319-23.)

9. Claims 12 and 28

Claim 12 depends from claim 1, which, as discussed above, is obvious over Fukuzo and Li. Li discloses the limitations added in claim 12, "wherein the second mode of operation comprises a restore operation in which data is communicated from the non-volatile memory subsystem to the volatile memory subsystem." Li discloses a restore operation in which data is copied from non-volatile memory 204 to the volatile memory 202. (Li, 7:9-13 and Abstract; *see also* Ex. 1020, ¶¶ 324-27.) The Office previously found that Li disclosed these claim limitations, and this finding was not disputed by Netlist. (Ex. 1010 at 7-8; Exs. 1006, 1008, 1011.)

Accordingly, claim 12 is obvious over Fukuzo and Li. Li is combinable with Fukuzo for the reasons stated in Section V.C.1 and for the reasons indicated in Ex. 1020, ¶¶ 279, 286, 328. Claim 28 depends from claim 15 and recites substantially the same limitations as claim 12, and claim 28 is obvious over Fukuzo and Li for the reasons described above. (*See* Ex. 1020, ¶¶ 324-28.)

10. Claims 13 and 29

Claim 13 depends from claim 1, which, as discussed above, is obvious over Fukuzo and Li. Fukuzo discloses the additional limitations in claim 13 (*see* Section V.A.3 and Ex. 1020, ¶¶ 329-33), which accordingly is obvious over Fukuzo and Li. Li is combinable with Fukuzo for the reasons stated in Section V.C.1. (*See also* Ex. 1020, ¶¶ 279, 286.) Claim 29 depends from claim 15 and recites

substantially the same limitations as claim 13, and claim 29 is obvious over Fukuzo and Li for the reasons described above. (*See* Ex. 1020, ¶¶ 329-33.)

11. Claim 17

Claim 17 depends from claim 15, which, as discussed above, is obvious over Fukuzo and Li. Li discloses the limitations added in claim 17, "a plurality of power supplies and a switch configured to selectively deliver power from the plurality of power supplies to the volatile memory subsystem and the non-volatile memory subsystem as a function of the mode of operation." (*See* Ex. 1020, ¶¶ 334-37.) Specifically, Li discloses a system power supply and an auxiliary power supply (*i.e.*, "a plurality of power supplies"). (Li, 9:18-20.) Isolation devices 208 (*i.e.*, "a switch") stop delivery of power from the system power supply to the memory system (*i.e.*, "to the volatile memory subsystem and the non-volatile memory subsystem") following a power failure trigger event that causes the backup mode of operation to begin (*i.e.*, "as a function of the mode of operation"). (*Id.*, 8:5-7 and 6:48-57.) The auxiliary power supply is used during the backup mode of operation and turned off at the completion of the backup mode of operation before re-entering a normal mode of operation (*i.e.*, "as a function of the mode of operation"). (*Id.*, 9:57-10:3.) The Office previously found that Li disclosed these claim limitations, and this finding was not disputed by Netlist. (*See* Ex. 1010 at 9; *see also* Exs. 1006, 1008, 1011.)

Accordingly, claim 17 is obvious over Fukuzo and Li. Li is combinable with Fukuzo for the reasons stated in Section V.C.1 and for the reasons indicated in Ex. 1020, ¶¶ 279, 286, 338.

D. Claims 3 and 19 are Unpatentable Under 35 U.S.C. § 103(a) over Fukuzo and Spiers (U.S. Patent Pub. No. 2006/0080515)

Claim 3 depends from claim 1, which, as discussed above, is anticipated by Fukuzo. Spiers (Ex. 1016) discloses the limitations added in claim 3, "wherein the memory system is not powered by a battery when it is in the second mode of operation." Specifically, Spiers discloses that during a backup mode of operation (*i.e.*, "the second mode of operation"), the memory system is powered by one or more capacitors (*i.e.*, "the memory system is not powered by a battery"). (Spiers, ¶¶ 0036 and 0037 and Figs. 4 and 5; *see also* Ex. 1020, ¶¶ 340-44.)

<u>Motivation to Combine</u>

The POSITA would have been motivated to combine Spiers's teachings with Fukuzo because both references are related to hybrid memory systems including volatile and non-volatile memory subsystems, such that the similar purposes and overlapping teachings would have motivated the POSITA to combine the teachings of the references. As another example, the POSITA would have been motivated to supplement Fukuzo's hybrid memory system with the teachings of Spiers regarding the use of one or more capacitors to power a memory system during a backup operation. Specifically, the POSITA would have recognized the disadvantages inherent in using

batteries to power a memory system during a backup operation (*e.g.*, batteries tolerate a fixed number of charge-discharge cycles and may have a relatively short life, such that batteries may have associated replacement costs, etc.) and would have been motivated to supplement Fukuzo with Spiers's teachings of a capacitor power supply that does not have such disadvantages. Further, the POSITA would have recognized that batteries can be bulky and costly and that capacitors can be incorporated into the memory system itself. Further, the use of one or more capacitors as a power supply for a memory system during a backup operation was well-known at the time of the alleged invention of the '833 patent (*see*, *e.g.*, Ex. 1022; *see also* Ex. 1020, ¶ 345).

Claim 3 is obvious over Fukuzo and Spiers. Claim 19 depends from claim 15 and recites substantially the same limitations as claim 3, and claim 19 is obvious over Fukuzo and Spiers for the reasons described above. (*See* Ex. 1020, ¶¶ 347-52.)

E. Claims 3 and 19 are Unpatentable Under 35 U.S.C. § 103(a) over Fukuzo, Li, and Spiers

As discussed above, claim 3 is obvious over Fukuzo and Li. (*See* Section V.C.3.) To the extent it could be argued that any further disclosure may be required with respect to the claimed "memory system . . . not powered by a battery when it is in the second mode of operation," Spiers provides such further disclosure as explained above in Section V.D. (*See* Ex. 1020, ¶¶ 354-56.)

<u>Motivation to Combine</u>

The POSITA would have been motivated to combine Spiers's teachings with

Fukuzo and Li because all three references are related to hybrid memory systems including volatile and non-volatile memory subsystems, such that the similar purposes and overlapping teachings would have motivated the POSITA to combine the teachings of the references. As another example, the POSITA would have been motivated to supplement Fukuzo and Li's hybrid memory systems with the teachings of Spiers regarding the use of one or more capacitors to power a memory system during a backup mode. Specifically, the POSITA would have recognized the disadvantages inherent in using batteries to power a memory system during a backup mode (*see* Section V.D) and would have been motivated to supplement Fukuzo and Li with Spiers's teachings of a capacitor power supply that does not have such disadvantages. (*See* Ex. 1020, ¶ 355.)

Accordingly, claim 3 is obvious over Fukuzo, Li, and Spiers. Claim 19 recites substantially the same limitations as claim 3, and claim 19 is obvious over Fukuzo, Li, and Spiers for the reasons described above. (*See* Ex. 1020, ¶¶ 354-56.)

F. Claims 7 and 23 are Unpatentable Under 35 U.S.C. § 103(a) over Fukuzo and Hansen (U.S. Patent Pub. No. 2005/0132250)

Claim 7 depends from claim 1, which, as discussed above, is anticipated by Fukuzo. Hansen (Ex. 1017) discloses the limitations added in claim 7, "wherein data communicated between the volatile memory subsystem and the non-volatile memory subsystem is intermediate data from a host computer system computation." (*See* Ex. 1020, ¶¶ 358-61.) Hansen discloses transferring process state data from volatile memory to non-volatile memory during execution of a process. (Hansen,

¶¶ 0001-0003, 0041.) The process state data includes intermediate calculations (*i.e.*, "intermediate data from a host computer system computation"). (*Id.*)

Motivation to Combine

The POSITA would have been motivated to combine Hansen's teachings with Fukuzo because both references are related to hybrid memory systems including volatile and non-volatile memory subsystems, such that the similar purposes and overlapping teachings would have motivated the POSITA to combine the teachings of the references. As another example, the POSITA would have been motivated to supplement Fukuzo's hybrid memory system with the teachings of Hansen regarding backing up process state data including intermediate calculations to non-volatile memory during process execution. Specifically, the POSITA would have recognized that by failing to backup such intermediate calculations, regenerating the process's state after a system failure would require extensive effort (*see* Hansen at ¶ 0001), and the POSITA would have been motivated to supplement Fukuzo with Hansen's teachings to overcome such issues. Also, because power failure can occur at unpredictable times, the POSITA would have been motivated to implement Hansen's backup process that occurs at successive, regular time intervals in the system of Fukuzo. Further, saving the process state to non-volatile memory was well-known at the time of the alleged invention of the '833 patent (*see* Ex. 1023; *see also* Ex. 1020, ¶¶ 362, 368).

Accordingly, claim 7 is obvious over Fukuzo and Hansen. Claim 23 recites

substantially the same limitations as claim 7, and claim 23 is obvious over Fukuzo and Hansen for the reasons described above. (*See* Ex. 1020, ¶¶ 364-69.)

G. Claims 7, 9, 10, 23, 25, and 26 are Unpatentable Under 35 U.S.C. § 103(a) over Fukuzo, Li, and Hansen

1. Claims 7 and 23

Claim 7 depends from claim 1, which, as discussed above, is obvious over Fukuzo and Li. Hansen discloses the additional limitations in claim 7 (*see* Section V.F; Ex. 1020, ¶ 371), which accordingly is obvious over Fukuzo, Li, and Hansen.

<u>Motivation to Combine</u>

The POSITA would have been motivated to combine Hansen's teachings with Fukuzo and Li because all three references are related to hybrid memory systems including volatile and non-volatile memory subsystems, such that the similar purposes and overlapping teachings would have motivated the POSITA to combine the teachings of the references. As another example, the POSITA would have been motivated to supplement Fukuzo and Li's hybrid memory systems with the teachings of Hansen regarding backing up process state data including intermediate calculations to non-volatile memory during process execution. Specifically, the POSITA would have recognized that by failing to backup such intermediate calculations, regenerating the process's state after a system failure would require extensive effort (*see* Hansen at ¶ 0001), and the POSITA would have been motivated to combine Hansen with Fukuzo and Li to overcome such issues. (*See* Ex. 1020, ¶ 372.)

Claim 7 is obvious over Fukuzo, Li, and Hansen. Claim 23 depends from claim 15 and recites substantially the same limitations as claim 7, and claim 23 is obvious over Fukuzo, Li, and Hansen for the reasons described above. (Ex. 1020, ¶¶ 371-73.)

2. Claims 9 and 25

Claim 9 depends from claim 8, which, as discussed above, is obvious over Fukuzo and Li. Hansen discloses the limitations added in claim 9, "wherein the backup operation is conducted at repeating time intervals." (*See* Ex. 1020, ¶¶ 374-76.) Specifically, Hansen discloses conducting backup operations at "successive time intervals." (Hansen at ¶ 0010.)

Accordingly, claim 9 is obvious over Fukuzo, Li, and Hansen. Hansen is combinable with Fukuzo and Li for the reasons stated in Section V.G.1 and for the reasons indicated in Ex. 1020, ¶¶ 377, 386. Claim 25 depends from claim 24 and recites substantially the same limitations as claim 9, and claim 25 is obvious over Fukuzo, Li, and Hansen for the reasons described above. (*See* Ex. 1020, ¶¶ 383-87.)

3. Claims 10 and 26

Claim 10 depends from claim 9, which, as discussed above, is obvious over Fukuzo, Li, and Hansen. Li discloses the limitations added in claim 10, "wherein the backup operation is initiated in response to a trigger event." (*See*, *e.g.*, Li, Abstract, 3:10-16, 9:49-67; *see also* Ex. 1020, ¶¶ 379-81.) The Office previously found that Li disclosed these claim limitations, and this finding was not disputed

by Netlist. (*See* Ex. 1010 at 7; *see also* Exs. 1006, 1008, 1011.)

Accordingly, claim 10 is obvious over Fukuzo, Li, and Hansen. Hansen is combinable with Fukuzo and Li for the reasons stated in Section V.G.1 and for the reasons indicated in Ex. 1020, ¶¶ 372, 377, 382, 391. Claim 26 depends from claim 25 and recites substantially the same limitations as claim 10, and claim 26 is obvious over Fukuzo, Li, and Hansen for the reasons described above. (Ex. 1020, ¶¶ 388-91.)

H. Claims 14 and 30 are Unpatentable Under 35 U.S.C. § 103(a) over Fukuzo and Sun (U.S. Patent No. 7,102,391)

Claim 14 depends from claim 1, which, as discussed above, is anticipated by Fukuzo. Sun (Ex. 1018) discloses the limitations added in claim 14, "wherein one or more of the first, second or third clock frequencies is configurable by a user." (*See* Ex. 1020, ¶¶ 393-96.) Specifically, Sun discloses a memory system including volatile and non-volatile memories and describes that one or more of the clock frequencies used in the memory system are set by a clock-generator architecture that is configurable by a user. (Sun, 22:1-23:34 and 23:61-67.)

<u>Motivation to Combine</u>

The POSITA would have been motivated to combine Sun's teachings with Fukuzo because both references are related to memory systems including volatile and non-volatile memory subsystems, such that the similar purposes and overlapping teachings would have motivated the POSITA to combine the teachings of the references. As another example, the POSITA would have been motivated to

supplement Fukuzo's hybrid memory system with the teachings of Sun regarding the use of a user-configurable clock-generator. Specifically, the POSITA would have recognized that a user may wish to change a type of memory used in the hybrid memory system (*e.g.*, swap out one type of flash memory for another type of flash memory). In changing the type of memory used in the hybrid memory system, the new type of memory may operate at a different clock rate than the memory previously used. Consequently, the POSITA would have been motivated to supplement Fukuzo's memory system with Sun's teaching of a user-configurable clock-generator so that the user could generate multiple clock frequencies according to his or her needs and the types of memory used in the hybrid memory system. (*See* Ex. 1020, ¶ 397.)

Accordingly, claim 14 is obvious over Fukuzo and Sun. Claim 30 depends from claim 15 and recites substantially the same limitations as claim 14, and claim 30 is obvious over Fukuzo and Sun for the reasons described above. (Ex. 1020, ¶¶ 399-403.)

I. Claims 14 and 30 are Unpatentable Under 35 U.S.C. § 103(a) over Fukuzo, Li, and Sun

Claim 14 depends from claim 1, which, as discussed above, is obvious over Fukuzo and Li. Sun discloses the additional limitations in claim 14 (*see* Section V.H; *see* Ex. 1020, ¶ 405), which accordingly is obvious over Fukuzo, Li, and Sun.

<u>Motivation to Combine</u>

The POSITA would have been motivated to combine Sun's teachings with Fukuzo and Li because all three references are related to memory systems including

volatile and non-volatile memory subsystems, such that the similar purposes and overlapping teachings would have motivated the POSITA to combine the teachings of the references. As another example, the POSITA would have been motivated to supplement Fukuzo and Li's hybrid memory systems with the teachings of Sun regarding the use of a user-configurable clock-generator. Specifically, the POSITA would have recognized that a user may wish to change a type of memory used in the hybrid memory system (*e.g.*, swap out one type of flash memory for another type of flash memory). In changing the type of memory used in the hybrid memory system, the new type of memory may operate at a different clock rate than the memory previously used. Consequently, the POSITA would have been motivated to supplement Fukuzo and Li's memory systems with Sun's teaching of a user-configurable clock-generator so that the user could generate multiple clock frequencies according to his or her needs. (*See* Ex. 1020, ¶ 406.)

Claim 14 is obvious over Fukuzo, Li, and Sun. Claim 30 depends from claim 15 and recites substantially the same limitations as claim 14, and claim 30 is obvious over Fukuzo, Li, and Sun for the reasons described above. (*See* Ex. 1020, ¶ 405.)

J. Claim 16 is Unpatentable Under 35 U.S.C. § 103(a) over Fukuzo and Komatsuzaki (U.S. Patent No. 6,944,042)

Claim 16 depends from claim 15, which, as discussed above, is anticipated by Fukuzo. Komatsuzaki (Ex. 1019) discloses the limitations added in claim 16, "a controller configured to decouple the non-volatile memory subsystem from the

volatile memory subsystem in the first mode of operation and to couple the non-volatile memory subsystem to the volatile memory subsystem in the second mode of operation." (*See* Ex. 1020, ¶¶ 409-12.) Komatsuzaki discloses a control circuit 120 (*i.e.*, "a controller") that outputs an enable control signal FEN. (Komatsuzaki, 10:49-64.) During SRAM read and write operations (*i.e.*, "in the first mode of operation"), the control circuit 120 uses the control signal FEN to decouple non-volatile memory from the volatile SRAM memory. (*Id.*) When transferring data between the volatile SRAM memory and the non-volatile memory (*i.e.*, "in the second mode of operation"), the control circuit 120 uses the control signal FEN to couple the non-volatile memory to the volatile SRAM memory. (*Id.*; 6:7-62.)

Motivation to Combine

The POSITA would have been motivated to combine Komatsuzaki's teachings with Fukuzo because both references are related to memory systems including volatile and non-volatile memory subsystems, such that the similar purposes and overlapping teachings would have motivated the POSITA to combine the teachings of the references. As another example, the POSITA would have been motivated to supplement Fukuzo's hybrid memory system with the teachings of Komatsuzaki regarding the use of a controller and transistors to couple and decouple non-volatile memory from volatile memory. Specifically, the POSITA would have recognized the advantages of isolating non-volatile memory from volatile memory in a hybrid memory

system, such as to protect one type of memory from being damaged due to an occurrence of events in the other type of memory (*e.g.*, power spikes, short circuits, current surges, etc.). Further, the concept of using electrical isolation to protect parts of a circuit or system from such damaging events was well-known at the time of the alleged invention of the '833 patent (*see*, *e.g.*, Ex. 1024; *see also* Ex. 1020, ¶ 413).

In summary, claim 16 is obvious over Fukuzo and Komatsuzaki.

K. Claim 16 is Unpatentable Under 35 U.S.C. § 103(a) over Fukuzo, Li, and Komatsuzaki

Claim 16 depends from claim 15, which, as discussed above, is obvious over Fukuzo and Li. Komatsuzaki discloses the limitations of claim 16 (*see* Section V.J; Ex. 1020, ¶ 416), which accordingly is obvious over Fukuzo, Li, and Komatsuzaki.

<u>Motivation to Combine</u>

The POSITA would have been motivated to combine Komatsuzaki's teachings with Fukuzo and Li because all three references are related to memory systems including volatile and non-volatile memory subsystems, such that the similar purposes and overlapping teachings would have motivated the POSITA to combine the teachings of the references. As another example, the POSITA would have been motivated to supplement Fukuzo and Li's hybrid memory systems with the teachings of Komatsuzaki regarding the use of a controller and transistors to couple and decouple non-volatile memory from volatile memory. Specifically, the POSITA would have recognized the advantages of isolating non-volatile memory from volatile memory in a

hybrid memory system, such as to protect one type of memory from being damaged due to an occurrence of events in the other type of memory (*e.g.*, power spikes, short circuits, current surges, electrostatic discharges). (*See* Li, 4:16-20; Ex. 1020, ¶ 417.)

In summary, claim 16 is obvious over Fukuzo, Li, and Komatsuzaki.

L. Claims 1-6, 8, 11, 12, 15, 17-22, 24, and 26-28 are Unpatentable Under 35 U.S.C. § 103(a) over Panabaker and Li

1. Claims 1 and 15

As discussed above, Panabaker discloses all limitations of claim 1. (*See* Section V.B.1.) To the extent it could be argued that any further disclosure may be required with respect to the claimed "first mode of operation" and "second mode of operation," Li provides such disclosure. (*See* Section V.C.1; Ex. 1020, ¶¶ 420-24.)

<u>Motivation to Combine</u>

The POSITA would have been motivated to combine Li's teachings with Panabaker because both references are related to hybrid memory systems including volatile and non-volatile memory subsystems, such that the similar purposes and overlapping teachings would have motivated the POSITA to combine the teachings of the references. As another example, the POSITA would have been motivated to supplement Panabaker's hybrid memory system with the teachings of Li regarding a trigger event that causes the hybrid memory system to enter a backup mode of operation in which data is transferred from volatile memory to non-volatile memory. Specifically, the POSITA would have recognized the disadvantage of the volatility of

Panabaker's SDRAM memory and would have been motivated to supplement Panabaker with Li's teachings of a backup mode of operation to lower the risk that data could be lost. Further, the use of non-volatile memory to backup volatile memory in response to a trigger condition was well-known at the time of the alleged invention of the '833 patent (*see, e.g.*, Ex. 1021; *see also* Ex. 1020, ¶¶ 425, 432).

Claim 1 is obvious over Panabaker and Li. Independent claim 15 recites a memory system with substantially the same limitations as claim 1, and claim 15 is obvious over Panabaker and Li for the reasons described above. (Ex. 1020, ¶¶ 427-33.)

2. Claims 2 and 18

Claim 2 depends from claim 1, which, as discussed above, is obvious over Panabaker and Li. Panabaker discloses the additional limitations in claim 2 (*see* Section V.B.2; Ex. 1020, ¶¶ 434-39), which accordingly is obvious over Panabaker and Li. Li is combinable with Panabaker for the reasons stated in Section V.L.1. (*See* Ex. 1020, ¶¶ 425, 432.) Claim 18 depends from claim 15 and recites substantially the same limitations as claim 2, and claim 18 is obvious over Panabaker and Li for the reasons described above. (*See* Ex. 1020, ¶¶ 434-39.)

3. Claims 3 and 19

Claim 3 depends from claim 1, which, as discussed above, is obvious over Panabaker and Li. Li discloses the limitations added in claim 3 (*see* Section V.C.3; Ex. 1020, ¶¶ 440-43), which accordingly is obvious over Panabaker and Li. Li is

combinable with Panabaker for the reasons stated in Section V.L.1 and for the reasons indicated in Ex. 1020, ¶¶ 425, 432, 444. Claim 19 depends from claim 15 and recites substantially the same limitations as claim 3, and claim 19 is obvious over Panabaker and Li for the reasons described above. (*See* Ex. 1020, ¶¶ 440-44.)

4. Claims 4 and 20

Claim 4 depends from claim 1, which, as discussed above, is obvious over Panabaker and Li. Li discloses the limitations added in claim 4 (*see* Section V.C.4; Ex. 1020, ¶¶ 445-48), which accordingly is obvious over Panabaker and Li. Li is combinable with Panabaker for the reasons stated in Section V.L.1 and for the reasons indicated in Ex. 1020, ¶¶ 425, 432, 449. Claim 20 depends from claim 15 and recites substantially the same limitations as claim 4, and claim 20 is obvious over Panabaker and Li for the reasons described above. (*See* Ex. 1020, ¶¶ 445-49.)

5. Claims 5 and 21

Claim 5 depends from claim 4, which, as discussed above, is obvious over Panabaker and Li. Li discloses the limitations added in claim 5 (*see* Section V.C.5; Ex. 1020, ¶¶ 450-53), which accordingly is obvious over Panabaker and Li. Li is combinable with Panabaker for the reasons stated in Section V.L.1 and for the reasons indicated in Ex. 1020, ¶¶ 425, 432, 454. Claim 21 depends from claim 20 and recites substantially the same limitations as claim 5, and claim 21 is obvious over Panabaker and Li for the reasons described above. (*See* Ex. 1020, ¶¶ 450-54.)

6. Claims 6 and 22

Claim 6 depends from claim 1, which is obvious over Panabaker and Li. Both Panabaker and Li disclose the limitations added in claim 6 (*see* Sections V.B.3, V.C.6; Ex. 1020, ¶¶ 455-58), which accordingly is obvious over Panabaker and Li. Li is combinable with Panabaker for the reasons stated in Section V.L.1 and for the reasons indicated in Ex. 1020, ¶¶ 425, 432, 459. Claim 22 depends from claim 15 and recites substantially the same limitations as claim 6, and claim 22 is obvious over Panabaker and Li for the reasons described above. (Ex. 1020, ¶¶ 455-59.)

7. Claims 8 and 24

Claim 8 depends from claim 1, which is obvious over Panabaker and Li. Both Panabaker and Li disclose the limitations added in claim 8 (*see* Sections V.B.4, V.C.7; Ex. 1020, ¶¶ 460-63), which accordingly is obvious over Panabaker and Li. Li is combinable with Panabaker for the reasons stated in Section V.L.1 and for the reasons indicated in Ex. 1020, ¶¶ 425, 432, 464. Claim 24 depends from claim 15 and recites substantially the same limitations as claim 8, and claim 24 is obvious over Panabaker and Li for the reasons described above. (Ex. 1020, ¶¶ 460-64.)

8. Claims 11 and 27

Claim 11 depends from claim 1, which, as discussed above, is obvious over Panabaker and Li. Both Panabaker and Li disclose the limitations added in claim 11 (*see* Sections V.B.5 and V.C.8; *see also* Ex. 1020, ¶¶ 465-67), which accordingly is obvious over Panabaker and Li. Li is combinable with Panabaker for the reasons

stated in Section V.L.1 and for the reasons indicated in Ex. 1020, ¶¶ 425, 432, 468. Claim 27 recites substantially the same limitations as claim 11, and claim 27 is obvious over Panabaker and Li for the reasons described above. (*See* Ex. 1020, ¶¶ 465-68.)

9. Claims 12 and 28

Claim 12 depends from claim 1, which, as discussed above, is obvious over Panabaker and Li. Both Panabaker and Li disclose the limitations added in claim 12 (*see* Sections V.B.6 and V.C.9; *see also* Ex. 1020, ¶¶ 469-72), which accordingly is obvious over Panabaker and Li. Li is combinable with Panabaker for the reasons stated in Section V.L.1 and for the reasons indicated in Ex. 1020, ¶¶ 425, 432, 473. Claim 28 recites substantially the same limitations as claim 12, and claim 28 is obvious over Panabaker and Li for the reasons described above. (*See* Ex. 1020, ¶¶ 469-73.)

10. Claim 17

Claim 17 depends from claim 15, which is obvious over Panabaker and Li. Li discloses the limitations added in claim 17 (*see* Section V.C.11; Ex. 1020, ¶¶ 474-77), which accordingly is obvious over Panabaker and Li. Li is combinable with Panabaker for the reasons stated in Section V.L.1 and for the reasons indicated in Ex. 1020, ¶¶ 425, 432, 478.

M. Claims 3 and 19 are Unpatentable Under 35 U.S.C. § 103(a) over Panabaker and Spiers

Claim 3 depends from claim 1, which, as discussed above, is anticipated by Panabaker. Spiers discloses the limitations added in claim 3 (*see* Section V.D; *see*

also Ex. 1020, ¶¶ 480-84), which accordingly is obvious over Panabaker and Spiers.

Motivation to Combine

The POSITA would have been motivated to combine Spiers's teachings with Panabaker because both references are related to hybrid memory systems including volatile and non-volatile memory subsystems, such that the similar purposes and overlapping teachings would have motivated the POSITA to combine the teachings of the references. As another example, the POSITA would have been motivated to supplement Panabaker's memory system with the teachings of Spiers regarding the use of one or more capacitors to power a memory system during a backup operation (*e.g.*, to avoid the disadvantages inherent in using batteries to power a memory system during a backup operation (*see* Section V.D). The use of capacitors as a power supply for a memory system was well-known at the time of the alleged invention of the '833 patent (*see* Ex. 1022; *see also* Ex. 1020, ¶ 485).

Claim 3 is obvious over Panabaker and Spiers. Claim 19 depends from claim 15 and recites substantially the same limitations as claim 3, and claim 19 is obvious over Panabaker and Spiers for the reasons described above. (*See* Ex. 1020, ¶¶ 487-92.)

N. Claims 3 and 19 are Unpatentable Under 35 U.S.C. § 103(a) over Panabaker, Li, and Spiers

As discussed above, claim 3 is obvious over Panabaker and Li. (*See* Sections V.L.3.) To the extent it could be argued that any further disclosure may be required with respect to the claimed "memory system . . . not powered by a battery

when it is in the second mode of operation," Spiers provides such further disclosure as explained above in Section V.M. (*See* Ex. 1020, ¶ 494.)

Motivation to Combine

The POSITA would have been motivated to combine Spiers's teachings with Panabaker and Li because all three references are related to hybrid memory systems including volatile and non-volatile memory subsystems, such that the similar purposes and overlapping teachings would have motivated the POSITA to combine the teachings of the references. As another example, the POSITA would have been motivated to supplement Panabaker and Li's hybrid memory systems with the teachings of Spiers regarding the use of one or more capacitors to power a memory system during a backup mode. Specifically, the POSITA would have recognized the disadvantages inherent in using batteries to power a memory system during a backup mode (*see* Section V.D) and would have been motivated to supplement Panabaker and Li with Spiers's capacitor power supply that does not have such disadvantages. (*See* Ex. 1020, ¶ 495.)

Claim 3 is obvious over Panabaker, Li, and Spiers. Claim 19 recites substantially the same limitations as claim 3, and claim 19 is obvious over Panabaker, Li, and Spiers for the reasons described above. (Ex. 1020, ¶ 494-96.)

O. Claims 7, 9, 23, and 25 are Unpatentable Under 35 U.S.C. § 103(a) over Panabaker and Hansen

1. Claims 7 and 23

Claim 7 depends from claim 1, which, as discussed above, is anticipated by

Panabaker. Hansen discloses the limitations added in claim 7 (*see* Section V.F; *see also* Ex. 1020, ¶¶ 498-502), which is obvious over Panabaker and Hansen.

Motivation to Combine

The POSITA would have been motivated to combine Hansen's teachings with Panabaker because both references are related to hybrid memory systems including volatile and non-volatile memory subsystems, such that the similar purposes and overlapping teachings would have motivated the POSITA to combine the teachings of the references. The POSITA would have been motivated to supplement Panabaker's hybrid memory system with the teachings of Hansen regarding backing up process state data including intermediate calculations to non-volatile memory during process execution. Specifically, the POSITA would have recognized that by failing to backup such intermediate calculations, regenerating the process's state after a system failure would require extensive effort (*see* Hansen at ¶ 0001). Further, saving the process state to non-volatile memory during normal execution was well-known at the time of the alleged invention of the '833 patent (*see, e.g.*, Ex. 1023; *see also* Ex. 1020, ¶ 503).

Claim 7 is obvious over Panabaker and Hansen. Claim 23 depends from claim 15 and recites substantially the same limitations as claim 7, and claim 23 is obvious over Panabaker and Hansen for the reasons described above. (Ex. 1020, ¶¶ 498-504.)

2. Claims 9 and 25

Claim 9 depends from claim 8, which is anticipated by Panabaker. Hansen

discloses the limitations added in claim 9 (*see* Section V.G.2; Ex. 1020, ¶¶ 505-08), which accordingly is obvious over Panabaker and Hansen. Hansen is combinable with Panabaker for the reasons stated in Section V.O.1 and for the reasons indicated in Ex. 1020, ¶¶ 503, 509. Claim 25 depends from claim 24 and recites substantially the same limitations as claim 9, and claim 25 is obvious over Panabaker and Hansen for the reasons described above. (*See* Ex. 1020, ¶¶ 505-10.)

P. Claims 7, 9, 10, 23, 25, and 26 are Unpatentable Under 35 U.S.C. § 103(a) over Panabaker, Li, and Hansen

1. Claims 7 and 23

Claim 7 depends from claim 1, which is obvious over Panabaker and Li. Hansen discloses the additional limitations in claim 7 (*see* Section V.F; *see also* Ex. 1020, ¶ 512), which accordingly is obvious over Panabaker, Li, and Hansen.

<u>Motivation to Combine</u>

The POSITA would have been motivated to combine Hansen's teachings with Panabaker and Li because all three references are related to hybrid memory systems including volatile and non-volatile memory subsystems, such that the similar purposes and overlapping teachings would have motivated the POSITA to combine the teachings of the references. As another example, the POSITA would have been motivated to supplement Panabaker and Li's hybrid memory systems with the teachings of Hansen regarding backing up process state data including intermediate calculations to non-volatile memory during process execution. Specifically, the POSITA would have

recognized that by failing to backup such intermediate calculations, regenerating the process's state after a system failure would require extensive effort (*see* Hansen at ¶ 0001), and the POSITA would have been motivated to combine Hansen with Panabaker and Li to overcome such issues. (*See* Ex. 1020, ¶ 513.)

Claim 7 is obvious over Panabaker, Li, and Hansen. Claim 23 recites substantially the same limitations as claim 7, and claim 23 is obvious over Panabaker, Li, and Hansen for the reasons described above. (*See* Ex. 1020, ¶¶ 512-14.)

2. Claims 9 and 25

Claim 9 depends from claim 8, which, as discussed above, is obvious over Panabaker and Li. Hansen discloses the limitations added in claim 9 (*see* Section V.G.2; *see also* Ex. 1020, ¶¶ 515-16), which accordingly is obvious over Panabaker, Li, and Hansen. Hansen is combinable with Panabaker and Li for the reasons stated in Section V.P.1 and for the reasons indicated in Ex. 1020, ¶¶ 513, 517, 526. Claim 25 depends from claim 24 and recites substantially the same limitations as claim 9, and claim 25 is obvious over Panabaker, Li, and Hansen for the reasons described above. (*See* Ex. 1020, ¶¶ 523-27.)

3. Claims 10 and 26

Claim 10 depends from claim 9, which, as discussed above, is obvious over Panabaker, Li, and Hansen. Li discloses the limitations added in claim 10 (*see* Section V.G.3; *see also* Ex. 1020, ¶¶ 519-21), which accordingly is obvious over

Panabaker, Li, and Hansen. Hansen is combinable with Panabaker and Li for the reasons stated in Section V.P.1 and for the reasons indicated in Ex. 1020, ¶¶ 513, 517, 522, 531. Claim 26 depends from claim 25 and recites substantially the same limitations as claim 10, and claim 26 is obvious over Panabaker, Li, and Hansen for the reasons described above. (*See* Ex. 1020, ¶¶ 528-31.)

Q. Claims 13 and 29 are Unpatentable Under 35 U.S.C. § 103(a) over Panabaker and Fukuzo

Claim 13 depends from claim 1, which, as discussed above, is anticipated by Panabaker. Fukuzo discloses the limitations added in claim 13 (*see* Section V.A.3; *see* Ex. 1020, ¶ 533), which accordingly is obvious over Panabaker and Fukuzo.

Motivation to Combine

The POSITA would have been motivated to combine Fukuzo's teachings with Panabaker because both references are directed to decreasing a number of interfaces required to allow a host system to communicate with both volatile and non-volatile memories. (*See* Fukuzo at ¶¶ 0004-0013 and Panabaker at 3:36-4:64.) Additionally, the POSITA would have been motivated to implement Fukuzo's clock generators 110, 310 in Panabaker because the POSITA would have recognized the advantages of using such clock generators 110, 310 in Panabaker's memory system. The POSITA would recognize that the clock generators 110, 310 would allow Panabaker's memory system to generate a variety of different clock signals for different parts of the memory system, thus providing flexibility to Panabaker's memory system. (*See* Ex. 1020, ¶ 534.)

Claim 13 is obvious over Panabaker and Fukuzo. Claim 29 depends from claim 15 and recites substantially the same limitations as claim 13, and claim 29 is obvious over Panabaker and Fukuzo for the reasons described above. (Ex. 1020, ¶¶ 532-34.)

R. Claims 13 and 29 are Unpatentable Under 35 U.S.C. § 103(a) over Panabaker, Li, and Fukuzo

Claim 13 depends from claim 1, which, as discussed above, is obvious over Panabaker and Li. Fukuzo discloses the limitations added in claim 13 (*see* Section V.A.3; *see* Ex. 1020, ¶ 536), which is obvious over Panabaker, Li, and Fukuzo.

Motivation to Combine

The POSITA would have been motivated to combine Fukuzo's teachings with Panabaker because all three references are related to hybrid memory systems. As another example, the POSITA would have been motivated to implement Fukuzo's clock generators 110, 310 in the systems of Panabaker and Li because the POSITA would have recognized the advantages of using such clock generators 110, 310 in Panabaker and Li's memory systems. The POSITA would recognize that the clock generators 110, 310 would allow Panabaker and Li's memory systems to generate a variety of different clock signals for different parts of the memory system, thus providing flexibility to the memory systems. (Ex. 1020, ¶ 537.)

Claim 13 is obvious over Panabaker, Li, and Fukuzo. Claim 29 recites substantially the same limitations as claim 13, and claim 29 is obvious over Panabaker, Li, and Fukuzo for the reasons described above. (*See* Ex. 1020, ¶¶ 535-37.)

S. Claims 14 and 30 are Unpatentable Under 35 U.S.C. § 103(a) over Panabaker and Sun

Claim 14 depends from claim 1, which, as discussed above, is anticipated by Panabaker. Sun discloses the limitations added in claim 14 (*see* Section V.H; *see also* Ex. 1020, ¶¶ 539-42), which accordingly is obvious over Panabaker and Sun.

Motivation to Combine

The POSITA would have been motivated to combine Sun's teachings with Panabaker because both references are related to memory systems including volatile and non-volatile memory subsystems. As another example, the POSITA would have been motivated to supplement Panabaker's hybrid memory system with the teachings of Sun regarding the use of a user-configurable clock-generator. Specifically, the POSITA would have recognized that a user may wish to change a type of memory used in the hybrid memory system. In changing the type of memory used in the hybrid memory system, the new type of memory may operate at a different clock rate than the memory previously used. Thus, the POSITA would have been motivated to supplement Panabaker's memory system with Sun's teaching of a user-configurable clock-generator so that the user could generate multiple clock frequencies according to his or her needs. (*See* Ex. 1020, ¶ 543.)

Claim 14 is obvious over Panabaker and Sun. Claim 30 depends from claim 15 and recites substantially the same limitations as claim 14, and claim 30 is obvious over Panabaker and Sun for the reasons described above. (*See* Ex. 1020, ¶¶ 545-49.)

T. Claims 14 and 30 are Unpatentable Under 35 U.S.C. § 103(a) over Panabaker, Li, and Sun

Claim 14 depends from claim 1, which, as discussed above, is obvious over Panabaker and Li. Sun discloses the limitations added in claim 14 (*see* Section V.H; Ex. 1020, ¶ 551), which accordingly is obvious over Panabaker, Li, and Sun.

Motivation to Combine

The POSITA would have been motivated to combine Sun's teachings with Panabaker and Li to supplement Panabaker and Li's hybrid memory systems with the teachings of Sun regarding the use of a user-configurable clock-generator. For example, the POSITA would have known that volatile memory and non-volatile memory operate at substantially different clock frequency and that without specific care, undesired conditions such as overflow/underflow could occur. As such, the POSITA would have recognized the benefits of generating clocks at different clock frequencies in order to ensure the correct operation of the hybrid memory systems in Panabaker and Li. (*See* Ex. 1020, ¶ 552.)

Claim 14 is obvious over Panabaker, Li, and Sun. Claim 30 depends from claim 15 and recites substantially the same limitations as claim 14, and claim 30 is obvious over Panabaker, Li, and Sun for the reasons described above. (*See* Ex. 1020, ¶¶ 550-53.)

U. Claim 16 is Unpatentable Under 35 U.S.C. § 103(a) over Panabaker and Komatsuzaki

Claim 16 depends from claim 15, which is anticipated by Panabaker.

Komatsuzaki discloses the limitations added in claim 16 (*see* Section V.J; Ex. 1020, ¶ 555-58), which accordingly is obvious over Panabaker and Komatsuzaki.

Motivation to Combine

The POSITA would have been motivated to combine Komatsuzaki's teachings with Panabaker to supplement Panabaker's hybrid memory system with the teachings of Komatsuzaki regarding the use of a controller and transistors to couple and decouple non-volatile memory from volatile memory (*e.g.*, to protect one type of memory from being damaged due to an occurrence of power spikes, short circuits, current surges, electrostatic discharges, etc., in the other type of memory). The concept of using electrical isolation to protect parts of a circuit or system was well-known at the time of the alleged invention of the '833 patent (*see, e.g.*, Ex. 1024; Ex. 1020, ¶ 559).

V. Claim 16 is Unpatentable Under 35 U.S.C. § 103(a) over Panabaker, Li, and Komatsuzaki

Claim 16 depends from claim 15, which is obvious over Panabaker and Li. Komatsuzaki discloses the additional limitations in claim 16 (*see* Section V.J; Ex. 1020, ¶ 562), which accordingly is obvious over Panabaker, Li, and Komatsuzaki.

Motivation to Combine

The POSITA would have been motivated to supplement Panabaker and Li's hybrid memory systems with the teachings of Komatsuzaki regarding the use of a controller and transistors to couple and decouple non-volatile memory from volatile memory (*e.g.*, to protect one type of memory from being damaged due to an occurrence

of events in the other type of memory). (Li, 4:16-20; Ex. 1020, ¶ 563.)

VI. MANDATORY NOTICES PURSUANT TO 37 C.F.R. § 42.8(a)(1)

Pursuant to 37 C.F.R. § 42.8(a)(1), the mandatory notices identified in 37 C.F.R. § 42.8(b) are provided below as part of this Petition.

A. C.F.R. § 42.8(b)(1): Real Party-In-Interest

SanDisk is the Petitioner and real party-in-interest.

B. C.F.R. § 42.8(b)(2): Related Matters

The '833 Patent is currently the subject of a patent infringement lawsuit brought by the assignee of the '833 patent, Netlist. (*See Netlist, Inc. v. Smart Modular Technologies, Inc.*, U.S. District Court for the Northern District of California, Civil Action No. 3:13-CV-05889-YGR; *Diablo Technologies, Inc. v. Netlist, Inc.*, U.S. District Court for the Northern District of California, Civil Action No. 4:13-CV-03901-YGR; and *Smart Modular Technologies, Inc. v. Netlist, Inc.*, U.S. District Court for the Northern District of California, Civil Action No. 4:13-CV-03916-YGR.) These judicial matters may affect decisions made in this proceeding.

Additionally, Petitioner has filed petitions for *inter partes* review for the following patents, which are related to the '833 patent:

- U.S. Patent No. 8,516,187 (IPR2014-00982)

C. C.F.R. § 42.8(b)(3) and (4): Lead and Back-up Counsel and Service Information

SanDisk provides the following designation of counsel:

Lead Counsel	Back-up Counsel	Back-up Counsel
David B. Cochran Reg. No. 39,142 JONES DAY 901 Lakeside Avenue Cleveland, Ohio 44114 (216) 586-7029 dcochran@jonesday.com	Joseph M. Sauer Reg. No. 47,919 JONES DAY 901 Lakeside Avenue Cleveland, Ohio 44114 (216) 586-7506 jmsauer@jonesday.com	Joshua R. Nightingale Reg. No. 67,865 JONES DAY One Mellon Center 500 Grant Street Pittsburgh, PA 15219 (412) 394-7950 jrnightingale@jonesday.com

Pursuant to 37 C.F.R. § 42.10(b), a Power of Attorney accompanies this Petition. Please address all correspondence to lead and back-up counsel at the address above. SanDisk consents to electronic service by email at the email addresses listed above.

VII. CONCLUSION

Petitioner respectfully requests that the Patent Office order an *Inter Partes* Review trial and proceed to cancel claims 1-30 of the '833 patent.

Respectfully submitted,

Date: 6/20/14

By: _____

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PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 8,301,833

CERTIFICATE OF SERVICE

The undersigned hereby certifies that a copy of the foregoing Petition for *Inter Partes* Review of U.S. Patent No. 8,301,833, including all Exhibits, was served on June 20, 2014 via Express Mail delivery directed to the attorney of record for the patent at the following address:

Erik Birkeneder
Nixon Peabody LLP
P.O. Box 60610
Palo Alto CA 94306

Date: 6/20/14

Joseph M. Sauer

EXHIBIT LIST

EXHIBIT NO.	TITLE
1001	U.S. Patent No. 8,301,833 ("the '833 patent")
1002	Excerpt from the file history of the '833 patent: U.S. Appl. No. 12/240,916, Application As Filed
1003	Excerpt from the file history of the '833 patent: Requirement for Restriction/Election dated March 31, 2011
1004	Excerpt from the file history of the '833 patent: Preliminary Amendment and Reply to Election/Restriction Requirement dated May 20, 2011
1005	Excerpt from the file history of the '833 patent: Non-Final Office Action dated July 29, 2011
1006	Excerpt from the file history of the '833 patent: Amendment and/or Reply to Office Action dated October 18, 2011
1007	Excerpt from the file history of the '833 patent: Final Office Action dated February 1, 2012
1008	Excerpt from the file history of the '833 patent: Amendment and/or Reply to Office Action dated March 2, 2012
1009	Excerpt from the file history of the '833 patent: Applicant Initiated Interview Summary dated March 13, 2012
1010	Excerpt from the file history of the '833 patent: Non-Final Office

	Action dated April 3, 2012
1011	Excerpt from the file history of the '833 patent: Supplemental Amendment and/or Reply to Office Action dated June 14, 2012
1012	Excerpt from the file history of the '833 patent: Notice of Allowance dated September 17, 2012
1013	U.S. Patent Pub. No. 2006/0294295 ("Fukuzo")
1014	U.S. Patent No. 7,716,411 ("Panabaker")
1015	U.S. Patent No. 6,336,174 ("Li")
1016	U.S. Patent Pub. No. 2006/0080515 ("Spiers")
1017	U.S. Patent Pub. No. 2005/0132250 ("Hansen")
1018	U.S. Patent No. 7,102,391 ("Sun")
1019	U.S. Patent No. 6,944,042 ("Komatsuzaki")
1020	Declaration of Dr. Paul Min Under 37 C.F.R. § 1.68 in Support of Petition for *Inter Partes* Review of U.S. Patent No. 8,301,833
1021	U.S. Patent No. 3,916,390
1022	U.S. Patent No. 3,562,555
1023	U.S. Patent No. 4,234,920
1024	U.S. Patent No. 2,043,099

1025	*Curriculum vitae* of Dr. Paul Min