Paper No. 1

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SK HYNIX INC., SK HYNIX AMERICA INC., and SK HYNIX MEMORY SOLUTIONS INC.,

Petitioners,

v.

NETLIST, INC.

Patent Owner

Patent No. 8,301,833

Issued: October 30, 2012

Filed: September 29, 2008

Inventors: Chi-She Chen, Jeffrey C. Solomon, Scott Milton, Jayesh Bhakta

Title: Non-Volatile Memory Module

Inter Partes Review No. IPR2017-00649

PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 8,301,833 UNDER 35 U.S.C. §§ 311-319 AND 37 C.F.R. § 42.1-.80 & 42.100-.123

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I. COMPLIANCE WITH REQUIREMENTS FOR A PETITION FOR INTER PARTES REVIEW

A. Certification the 833 Patent May Be Contested by Petitioners

Petitioners certify they are not barred or estopped from requesting *inter partes* review of U.S. Patent No. 8,301,833 ("the 833 Patent") (Ex. 1001). No Petitioner, nor any party in privity with a Petitioner, has filed a civil action challenging the validity of any claim of the 833 Patent. The 833 Patent has not been the subject of a prior *inter partes* review by any Petitioner or a privy of a Petitioner.

Petitioners also certify this petition for *inter partes* review is filed within one year of the date of service of a complaint alleging infringement of a patent – no complaint alleging infringement of the 833 Patent has been served on any Petitioner. Petitioners therefore certify this patent is available for *inter partes* review.

B. Fee for Inter Partes Review (§ 42.15(a))

The Director is authorized to charge the fee specified by 37 CFR § 42.15(a) to Deposit Account No. 50-1597.

C. Mandatory Notices (37 CFR § 42.8(b))

The real parties of interest of this petition are the Petitioners: SK hynix Inc., SK hynix America Inc. and SK hynix memory solutions Inc.

The 833 Patent is involved in the following legal proceedings: *Netlist, Inc. v. SMART Modular Technologies, Inc.*, Case No. 8-13-cv-00996 (C.D. Cal.); *Smart Modular Technologies, Inc. v. Netlist, Inc.*, Case No. 4-13-cv-03916 (N.D. Cal.); *Diablo Technologies, Inc. v. Netlist, Inc.*, Case No. 4-13-cv-03901 (N.D. Cal.); *Netlist, Inc. v. Smart Modular Technologies, Inc.*, 4-13-cv-05889 (N.D. Cal.); *SanDisk Corp. v. Netlist, Inc.*, IPR2014-00994 (institution denied); and *SMART Modular Technologies Inc. v. Netlist, Inc.*, IPR2014-01370 (institution denied).

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Service on Petitioner may be made by e-mail (Sidley-SKH-IPR@sidley.com), mail, or hand delivery to: Sidley Austin LLP, 1501 K Street, N.W., Washington, D.C. 20005. The fax number for lead and backup counsel is (202) 736-8711.

D. Proof of Service (§§ 42.6(e) and 42.105(a))

Proof of service of this petition is provided in **Attachment A**.

II. IDENTIFICATION OF CLAIMS BEING CHALLENGED

Petitioners propose several grounds for trial as set forth below, none of which is redundant. Each ground is based primarily on U.S. Patent Application Publication No. 2007/0136523 to Bonella ("Bonella") (Ex. 1005). However,

Petitioners also address several arguments that Patent Owner may raise in response by proposing grounds that more closely satisfy the claim limitations to which such arguments would be directed. Such additional grounds are not redundant because they are "rational, narrowly targeted, and not burdensome." IPR2015-01912, Paper 10 at 17-18. Petitioners therefore respectfully request that trial be instituted on all grounds and arguments advanced herein. Specifically, this Petition seeks a finding that claims 1-30 of the '833 Patent are unpatentable as follows:

(i) **Claims 1-30** are obvious under 35 U.S.C. § 103 over Bonella (Ex. 1005) in view of Mills (Ex. 1007);

(ii) **Claims 1-30** are obvious under § 103 over Bonella in view of Mills and Ashmore (Ex. 1008);

(iii) **Claims 7 and 23** are obvious under § 103 over Bonella, Mills, with or without Ashmore, and in further view of Larson (Ex. 1019);

(iv) **Claims 8-10 and 24-26** are obvious under § 103 over Bonella, Mills, with or without Ashmore, and in further view of Windows 2000 (Ex. 1021);

(v) **Claim 16** is obvious under § 103 over Bonella, Mills, with or without Ashmore, and in further view of Klein (Ex. 1009); and

(vi) **Claim 17** is obvious under § 103 over Bonella, Mills, with or without Ashmore, and in further view of U.S. Patent App. Pub. No. 2005/0249011A1 to Maeda (Ex. 1013).

Petitioner's proposed claim constructions, the evidence relied upon, and the precise reasons why the claims are unpatentable are provided in §§ **III-V**, below. The evidence relied upon in this petition is listed in **Attachment B**.

III. RELEVANT INFORMATION CONCERNING THE CONTESTED PATENT

A. Effective Filing Date of the 833 Patent

The 833 Patent resulted from U.S. Patent Application Serial No. 12/240,916, filed September 29, 2008, Ex. 1001, Face, which ultimately claims priority to U.S. Provisional Application No. 60/941,586, filed on June 1, 2007. Because the prior art relied upon in this petition was either filed or published well before the June 1, 2007 date, for the purposes of the analysis here Petitioners will assume a June 1, 2007 effective date.

B. Person of Ordinary Skill in the Art

A person of ordinary skill in the art in the field of the 833 Patent in the 2007 time frame would have been someone with a Bachelor's degree in materials science, electrical engineering, computer engineering, computer science, or in a related field and at least one year of experience with the design or development of semiconductor non-volatile memory circuitry or systems. Decl. of Ron Maltiel (Ex. 1003), ¶¶48-49.

C. The 833 Patent

1. Technical Overview

The 833 Patent discloses a memory system which can communicate with a host system such as a disk controller of a computer system. Ex. 1001, Abstract. The memory system can include volatile and non-volatile memory and a controller configured to back up the volatile memory using the non-volatile memory in the even of a trigger condition. *Id.* In order to power the system in the event of a power failure or reduction, the memory system can include a secondary power source such as a capacitor bank. *Id.* Figure 1 shows an example memory system:

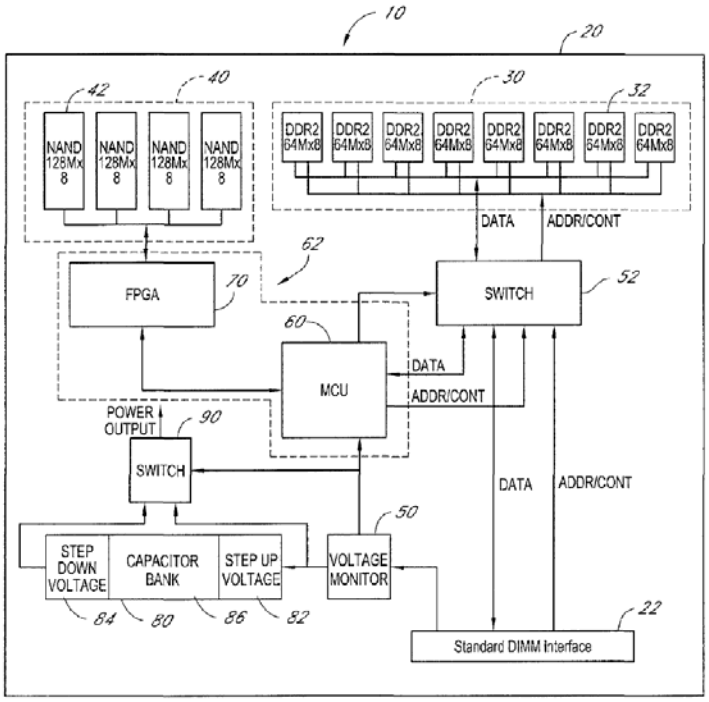

FIG. 1

Ex. 1001, Fig. 1, 3:16-17; Ex. 1003, ¶50.

The volatile memory system can be operated at a reduced frequency during backup and/or restore operations to improve the efficiency of the system and save power. Ex. 1001, 4:41-44. Figure 9 depicts an example method of operating a volatile memory subsystem at a reduced rate in a back-up mode:

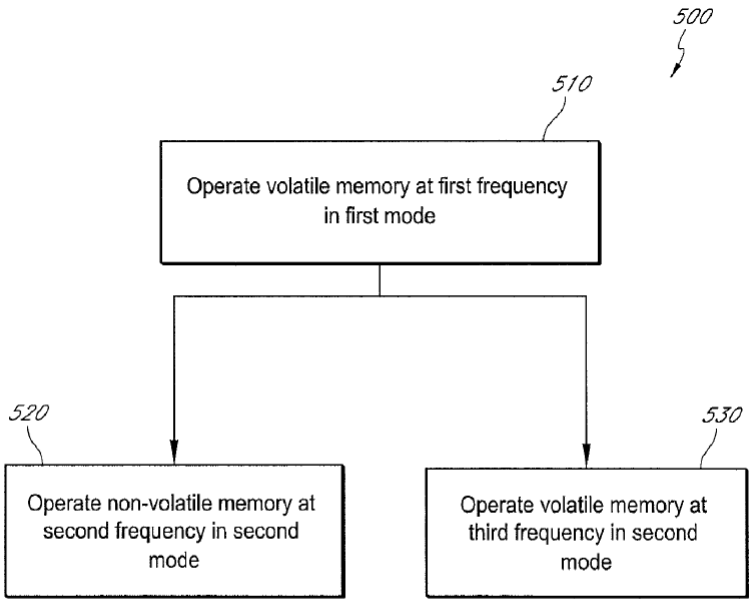

FIG. 9

Ex. 1001, Fig. 9, 3:45-48; *see id.*, 17:39-18:13; Ex. 1003, ¶51.

2. Relevant Prosecution History

The application underlying the 833 Patent was filed on September 29, 2008. The claims were initially rejected as obvious in view of the Li and Oshikiri references. Ex. 1002, 166-172. Patent Owner responded by arguing that the art merely showed "different processing speeds," not "different memory subsystem

operation frequenc[ies]." *Id.*, 134-149. The Examiner again rejected the claims as obvious, explaining that the claims were "not directed to the operating speed of a memory, but instead … to the operating speed of a memory subsystem." Ex. 1002, 123. Patent Owner submitted claim amendments that specified a "first clock frequency," a "second clock frequency," and a "third clock frequency." Ex. 1002, 107-117; Ex. 1003, ¶¶52-56.

The claims were again rejected as obvious, this time over the Li and Cope references. Ex. 1002, 59-73. The Examiner also rejected what are now claims 2 and 18 as indefinite because they recited "approximately equal" clock frequencies. *Id.* Patent Owner responded by amending the claims to replace the word "approximately" with "substantially," stating that "in practice there will always be a difference" between clock frequencies. *Id*. Patent Owner also argued that Cope "cannot be used to describe two modes of operation, where a DRAM in a first mode operates at a first clock frequency and in a second mode operates at another frequency." *Id.*, 71. The Examiner subsequently withdrew the rejections and the 833 Patent issued on October 10, 2012. *Id.*, 1; Ex. 1003, ¶¶57-58.

Two previous petitions for *inter partes* review were filed against the 833 Patent. In IPR2014-00994, filed by SanDisk Corporation, the Board construed the term "clock frequency" and ultimately denied review of claims 1-30, Paper 8, and later denied SanDisk's request for rehearing, Paper 10. In IPR2014-01370, filed

by SMART Modular Technologies Inc., the Board determined that no claim terms required explicit construction and denied review of claims 1-30. Paper 13.

D. Construction of Terms Used in the Claims

In this proceeding, claims must be given their broadest reasonable construction in light of the specification. 37 CFR § 42.100(b). If Patent Owner contends terms in the claims should be read to have a special meaning, those contentions should be disregarded unless Patent Owner also amends the claims compliant with 35 U.S.C. § 112 to make them expressly correspond to those contentions. *See* 77 Fed. Reg. 48764 at II.B.6 (Aug. 14, 2012); *cf. In re Youman*, 679 F.3d 1335, 1343 (Fed. Cir. 2012).

1. "*Operable at a … Clock Frequency*"

The Board has previously interpreted the term "*clock frequency*" to require "identification of a clock running at a particular frequency." IPR2014-00994, Paper 8 at 6. This interpretation is consistent with the 833 Patent's specification. *See, e.g.*, Ex. 1001, 17:25-38; Ex. 1003, ¶63. Petitioners have applied this interpretation below.

IV. OVERVIEW OF THE PRINCIPAL PRIOR ART

A. U.S. Patent Application Publication No. 2007/0136523 to Bonella (Ex. 1005)

Bonella was filed on December 8, 2006, and claimed priority to a provisional application (11/635,926) (Ex. 1006) filed on December 8, 2005.

Bonella is thus prior art under 35 U.S.C. § 102(e) (pre-AIA). Bonella expressly incorporates its provisional application by reference. Ex. 1005, ¶1; Ex. 1003, ¶¶64-65.

1. Overview of Bonella

Bonella is directed to a plug-and-play end-user add-in memory module for computers and consumer electronic devices. Ex. 1005, ¶2. Bonella discloses a memory module including a volatile memory, a non-volatile memory, and a controller that provides address, data, and control interfaces to the memories and to a host system, such as, for example, a personal computer, and provides one or more additional layers in the memory hierarchy of the host system. Ex. 1005, ¶6. Bonella teaches that this hybrid memory module fills the performance gap between main memory and a hard disk drive, and "can improve HDD reliability by keeping the HDD turned off for significant amounts of time, which also can reduce overall power consumption on laptops." *Id.*, ¶65; Ex. 1003, ¶66.

Figure 1 is a high level system block diagram of an illustrative memory module in accordance with the present invention:

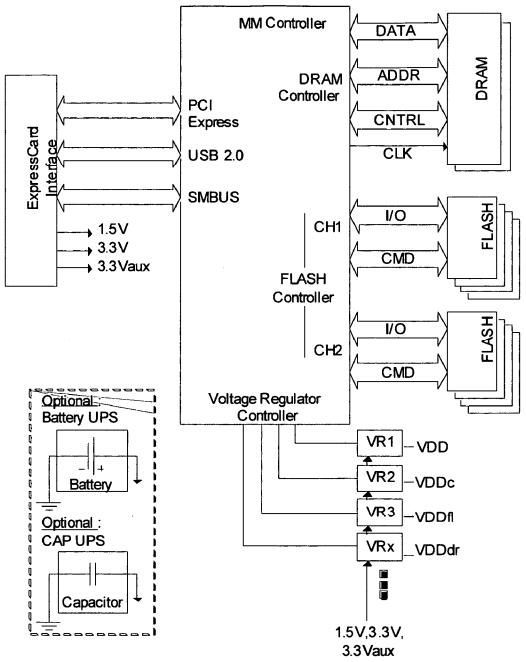

FIG. 1 Memory Module Block Diagram

Figure 1 shows the illustrative memory module with "five major functional blocks and two lesser functional blocks." Ex. 1005, ¶29. "The major blocks are: an Express Card Interface; a memory module controller; a DRAM memory; a FLASH memory; and a voltage regulator (and/or one or more power transistors)." *Id.* "The lesser blocks illustrated in FIG. 1 are: optional Uninterruptible Power Supply (UPS) capacitors or battery (for emergency shut-down operations); and various other electrical components such as decoupling capacitors, inductors, and so on, which are used for well-known miscellaneous functions in electronic products such as memory modules." *Id.*; Ex. 1003, ¶¶67-68. Bonella discloses that the memory module implements the DDR2 DRAM Specification and the

NAND Flash Specification, but can be modified to implement different interfaces and conform with alternative specifications. Ex. 1005, ¶¶36-37; Ex. 1003, ¶69.

Bonella teaches that using a combination of storage types can "gain dramatic improvements in operational performance and storage capacity," but that doing so requires "special embedded operational functions" in order to allow the memory module to operate independently so as to limit interference with normal system operation. Ex. 1005, ¶25. These functions include Flash write leveling, DRAM write buffer flushing to Flash, Flash flushing to HDD, device failure management, a power loss algorithm, security management, etc. *Id.*, ¶¶92-108; Ex. 1003, ¶70.

2. DRAM Write Buffer

Bonella teaches that its hybrid memory includes a DRAM write buffer "which allows the HDD to be shut off for extended periods of time. This does two things: 1) lowers power consumption; and 2) reduces HDD failures." Ex. 1005, ¶99. By maintaining "[a] certain amount of DRAM" for "write buffering and data read buffering," Bonella's system can "maintain a very high level of system performance for" data accesses "that are traditionally targeted for the hard disk drive." *Id.*, ¶80. Bonella teaches that write buffering allows for the HDD to be shut off, meaning that write data is initially stored only to the DRAM and is later copied to the HDD. *Id.*, ¶99. One of ordinary skill in the art would be readily familiar with the concept of write buffering or write caching. Ex. 1003, ¶¶71-72;

see, e.g., Microsoft Computer Dictionary (5th Ed.) (2002) (Ex. 1020), 76 (describing a "buffer"), 575 (defining an analogous "write-behind cache").

Bonella also teaches that the DRAM write buffer is occasionally backed up to the internal Flash memory so as to ensure data integrity in case of a power loss. Ex. 1005, ¶96. This write buffer flushing can be triggered by a power loss event, which then causes Bonella's "Power loss algorithm" to be executed:

> When the memory module controller detects a power loss event, the data that is flagged as critical is flushed to the FLASH, a flag is set and the memory module then shuts down. At new power on the normal power on sequence is followed and data restored to the DRAM.

Id., ¶101. During the execution of the power loss algorithm, Bonella's memory relies on backup power such as, for example, Uninterruptible Power Supply (UPS) capacitors. *Id.*, ¶29. The memory maintains a sufficiently large power reserve so as to write the data to Flash memory. *Id.*, ¶33; Ex. 1003, ¶¶73-75.

3. Configurable Power Consumption

Bonella also teaches that the hybrid memory module includes "Power State Aware" functionality that allows the module to significantly reduce power consumption when required. Ex. 1005, ¶45. For example, Bonella teaches a "Power Level 5" state that allows for full function, full performance operation. *Id.*, ¶47. Bonella also teaches a "Power Level 4" state that reduces the power

consumption of the memory module by limiting the DRAM performance. *Id.*, ¶48. Bonella explains that one way to reduce the power consumption of the memory module is to slow or reduce the operating frequency of the DRAM. *Id.*, ¶¶49-50; Ex. 1003, ¶¶76-79. Bonella teaches that reducing the DRAM frequency in this way can result in "major power savings." Ex. 1005, ¶50.

B. U.S. Patent No. 6,026,465 to Mills (Ex. 1007)

Mills was issued on February 15, 2000, and is therefore prior art under 35 U.S.C. § 102(b) (pre-AIA). Mills describes several interfaces for a Flash memory device, one of which is a synchronous flash interface: "FIG. 6 illustrates a block diagram of a synchronous flash interface (SFI) flash memory integrated circuit 600 that incorporates a complete synchronous flash interface in a single flash memory chip." Ex. 1007, 16:60-63. The synchronous flash interface includes a clock input such that all the external operations of the device are synchronized to the rising edge of the clock. *Id.*, 17:10-25.

Mills teaches that this synchronous operation is used for both read operations and write operations: "When SFI is enabled, interlace control 670 and [bank] select logic 674 operate to interlace read (and write) operations between flash bank A 610 and a flash bank B 620 …." *Id.*, 17:33-39. Because "the device is interleaved internally," it "creates an average access time for sequential read

accesses that is significantly less than the access time of an asynchronous flash device." *Id.*, 17:1-9; Ex. 1003, ¶¶81-82.

C. U.S. Patent Application Publication No. 2006/0212651 to Ashmore (Ex. 1008)

Ashmore was filed on December 22, 2005, and is therefore prior art under 35 U.S.C. § 102(e) (pre-AIA). Ashmore "provides a method for reducing battery power consumption during a main power loss to reduce the likelihood of loss of user write-cached data in a write-caching mass storage controller." Ex. 1008, ¶9. Ashmore's specific technique is explained as follows:

> In response to a loss of main power, the controller only provides battery power to the critical memory banks, but not to the non-critical memory banks, in order to reduce the amount of battery power consumed during the main power outage, thereby extending the time the critical memory banks can store the critical data to reduce the likelihood of user data loss.

Id., ¶7; Ex. 1003, ¶84.

V. PRECISE REASONS FOR RELIEF REQUESTED

A. Claims 1-30 Are Obvious Over Bonella and Mills

1. Claims 1 and 15 Are Unpatentable

a) Preambles

The preamble of claim 1 recites a "*method for controlling a memory system operatively coupled to a host system, the memory system including a volatile*

memory subsystem and a non-volatile memory subsystem." The preamble of claim 15 recites a "*memory system operatively coupled to a host system*."

Bonella is directed to "a **memory module** including a **volatile memory**, a **non-volatile memory**, and a controller that provides address, data, and control interfaces to the memories and to a **host system**, such as, for example, a personal computer, is operable to interact with the host system so as to provide one or more additional layers in the memory hierarchy of the host system." Ex. 1005, ¶6 (emphasis added); *see also id*., Fig. 1, ¶10. Bonella thus discloses a "*memory system*" (*e.g.*, memory module, Fig. 1) "*operatively coupled to*" (*e.g.*, via an ExpressCard Interface) "*a host system*" (*e.g.*, host system). *Id.*, Fig. 1, ¶6. The memory system also includes a "*volatile memory subsystem*" (*e.g.*, DRAM) and a "*non-volatile memory subsystem*" (*e.g.*, Flash). *Id.*; Ex. 1003, ¶¶86-88. Therefore, Bonella discloses the preambles of claims 1 and 15 to the extent they are limiting.

b) Operating a "Volatile Memory Subsystem" at a "First Clock Frequency"

Claim 1 recites "*operating the volatile memory subsystem at a first clock frequency when the memory system is in a first mode of operation in which data is communicated between the volatile memory subsystem and the host system*." Claim 15 recites "*a volatile memory subsystem operable at a first clock frequency when the memory system is in a first mode of operation in which data is communicated between the volatile memory subsystem and the host system*."

Bonella discloses a "*volatile memory subsystem*" in the form of a DRAM and its associated controller. Ex. 1005, Fig. 1. Bonella also discloses "*operating the volatile memory subsystem at a first clock frequency*." For example, in the top right corner of Figure 2 Bonella shows a "CLK" signal being provided to the DRAM Interface by the DRAM Controller:

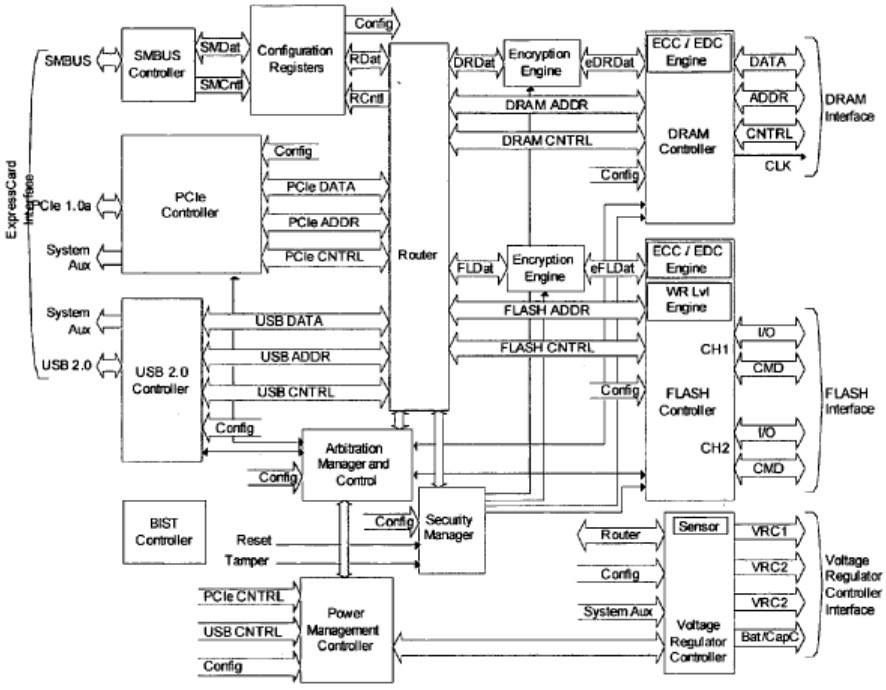

FIG. 2 Memory Module Controller Block Diagram

Id., Fig. 2; Ex. 1003, ¶91. One of ordinary skill in the art would understand that Bonella's DRAM is operating at the particular frequency of the clock signal ("CLK"). Ex. 1003, ¶92; Ex. 1005, ¶52 ("frequency of the clock"). Indeed, Bonella's provisional application, which is incorporated by reference, explains that "[a]ll address and control input signals are sampled on the crossing of the positive

edge of CK and negative edge of CK#" and "[d]ata is referenced to all CK and CK# crossings." Ex. 1006, 22.

This operation is further confirmed by the usual operation of DDR2 DRAM, Ex. 1003, ¶93, which Bonella explains can be used with his system. Ex. 1005, ¶36. According to the DDR2 specification at the time of Bonella's priority date, a conforming DDR2 DRAM device receives two input clock signals, CK and $\overline{CK}$, and "[a]ll address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of $\overline{CK}$." *DDR2 SDRAM Specification*, JESD79-2B (Jan. 2005) (Ex. 1010), 6, 29. A skilled artisan would understand Bonella's DRAM "CK" signal to be a clock signal operating at a particular frequency. Ex. 1003, ¶93.

Bonella also discloses that the "*volatile memory subsystem [is] operable at a first clock frequency when the memory system is in a first mode of operation*." Bonella's memory module has multiple power states, including Power Level 5 which "allows for full function, full performance operation" with "no preset restrictions placed on the DRAM." Ex. 1005, ¶47. This is contrasted with certain power saving options Bonella contemplates such as "slow[ing] the operating frequency of the device down" such that the clock "frequency is reduced to the DRAM …." *Id.*, ¶50. The default operating frequency of Bonella's DRAM clock is therefore a "*first clock frequency*" and is used during the conventional full-

power operation of the system, which a skilled artisan would understand included where "*data is communicated between the volatile memory subsystem and the host system*" during a read from and write to the DRAM write buffer. *E.g.*, *Id.*, Abstract, ¶6, 8-9; Ex. 1003, ¶98.

Bonella also discloses a specific example in the first mode in which *"data is communicated between the volatile memory subsystem and the host system.*" For example, Bonella's system includes several uses for the memory module, one of which is as a write buffer: "[a] certain amount of DRAM is required to be kept available for write buffering and data read buffering … this is done to maintain a very high level of system performance for the program(s) that are executing from memory module that are traditionally targeted for the hard disk drive." Ex. 1005, ¶80. Bonella also explains that this "allow[s] the volatile memory of the memory module to be used at times in place of writes to the non-volatile memory, thereby effectively increasing the write life of the non-volatile memory." *Id.*, ¶27 This means that the DRAM receives write data from the host system ("*data is communicated between the volatile memory subsystem and the host system*"). *See id.*; Ex. 1003, ¶94; *see also id.*, ¶¶95-97. Bonella therefore discloses these claim elements.

To the extent one might argue that the Board's interpretation of "*clock frequency*" requires a particular numeric value (*i.e.*, as in number of cycles per

second), it would have been obvious to operate Bonella's DRAM at frequencies from 67-400MHz because Bonella teaches that his DRAM interface can correspond to the "DDR2 DRAM specification" or to any other DRAM specification. Ex. 1005, ¶36. It was known that DDR DRAM could be operated at frequencies as low as 67MHz (*DDR SDRAM Specification*, JESD79 (Jun. 2000) (Ex. 1014), 58; Ex. 1003, ¶99) while DDR2 DRAM could be operated at frequencies as high as 400MHz (Ex. 1010, 69; Ex. 1003, ¶99).

It would have been obvious to use one of the known DDR or DDR2 DRAM modules in Bonella's system, and to subsequently clock the module at standards-specified rates. Ex. 1003, ¶100. To do so would have been merely the use of a known structure (a standard DRAM module and clock frequency) for its known use (operation as a DRAM module) to achieve a predictable result (operating a DRAM module at a standard clock frequency in Bonella's system). *Id.* Moreover, a skilled artisan would have been motivated to operate such memory at the standard-specified frequencies in order to ensure proper operation of the memory. *Id.*, ¶100-101. Therefore, operating Bonella's volatile memory "*at a first clock frequency,*" even under this narrow interpretation, would have been obvious.

c) Operating a "Non-Volatile Memory Subsystem" at a "Second Clock Frequency"

Claim 1 recites "*operating the non-volatile memory subsystem at a second clock frequency when the memory system is in a second mode of operation in*

which data is communicated between the volatile memory subsystem and the non-volatile memory subsystem." Claim 15 recites "*a non-volatile memory subsystem operable at a second clock frequency when the memory system is in a second mode of operation in which data is communicated between the volatile memory subsystem and the non-volatile memory subsystem*."

Bonella discloses a "*non-volatile memory subsystem*" in the form of Flash memory and its associated controller. Ex. 1005, Fig 1. As explained with respect to the claimed "*first mode*," *see* Ex. 1003, ¶¶94-97, Bonella discloses utilizing DRAM as a write buffer and periodically flushing the write data to the Flash memory. Ex. 1005, ¶96. During a power loss event, however, the memory module controller flushes critical data to the FLASH: "When the memory module controller detects a power loss event, the data that is flagged as critical is flushed to the FLASH …." *Id.*, ¶101; Ex. 1003, ¶103.

The operation of Bonella's system under this power loss algorithm causes "*data*" to be "*communicated between the volatile memory subsystem and the non-volatile memory subsystem*" (*e.g.*, flushing write data from DRAM to Flash), and is a "*second mode of operation*" when compared to the conventional operation of Bonella's system. Ex. 1003, ¶104. Bonella thus discloses "*a non-volatile memory subsystem operable … when the memory system is in a second mode of operation*

in which data is communicated between the volatile memory subsystem and the non-volatile memory subsystem."

Bonella does not explicitly disclose "*operating the non-volatile memory subsystem*" (the FLASH memory) "*at a second clock frequency*" during this second mode, but it would have been obvious to include that claimed functionality in the system of Bonella. Synchronous Flash memory interfaces that were operated by clock signals were well-known in the art by the 833 Patent's priority date. Ex. 1003, ¶¶105-106.

One such prior art Flash implementation is described by Mills et al., US Patent No. 6,026,465 ("Mills") (Ex. 1007). Mills describes several interfaces for a Flash memory device, one of which is a synchronous flash interface. Ex. 1007, 16:60-63. The synchronous flash interface causes the Flash memory system to "*operat[e] … at a second clock frequency*":

> A clock input is a part of the interface. … All the external operations of the device are synchronized to the rising edge of the clock. … The user can cycle the device at frequencies as high as 33 MHz ….

Id., 17:10-25; Ex. 1003, ¶106. Mills teaches that this synchronous operation can be used for both read operations and write operations. *Id.*, 17:1-9, 28-39. Mills therefore discloses a synchronous Flash interface where read and write operations are synchronized to the rising edge of a clock signal provided to the device and

operating at a particular frequency (*i.e.*, "*operating [a] non-volatile memory subsystem at a second clock frequency*"). Ex. 1003, ¶107. To the extent one might argue that the Board's interpretation of "*clock frequency*" requires a particular numeric value (*i.e.*, as in number of cycles per second), Mills discloses the use of his Flash memory at, for example, a frequency "as high as 33 MHz." Ex. 1007, 17:10-25; Ex. 1003, ¶107.

Bonella and Mills are both analogous art to the 833 Patent because each is from the field of memory systems. Ex. 1001, 3:60-63; Ex. 1005, ¶2; Ex. 1007, 6:57-59; Ex. 1003, ¶108.

As of the priority date of the 833 Patent, it would have been obvious to one of ordinary skill in the art to employ a synchronous flash memory, such as disclosed in Mills, in the system of Bonella because to do so would have been merely an arrangement of old elements with each performing the same function it had been known to perform and yielding no more than what one would expect from such an arrangement, i.e., the non-volatile storage of data. Ex. 1003, ¶109.

As combined, Bonella's Flash interface (*see, e.g.*, Ex. 1005, Fig. 2 ("FLASH Interface")) would conform to Mills' synchronous Flash protocol and thus include a separate clock signal that controls read and write operations. *See* Ex. 1007, 17:10-25, 17:28-39. This means that Bonella's Flash memory would operate at "*a second clock frequency*" (*i.e.*, the frequency of the synchronous Flash interface

clock up to 33 MHz**,** *id.*, 17:10-25)) during its operation, including when Bonella's power loss algorithm writes data from DRAM to Flash ("*when the memory system is in a second mode of operation in which data is communicated between the volatile memory subsystem and the non-volatile memory subsystem*"). Ex. 1003, ¶110.

A skilled artisan would have been motivated to make such a combination because, as Mills explains, a synchronous flash interface "creates an average access time for sequential read accesses that is significantly less than the access time of an asynchronous flash device." Ex. 1007, 17:6-9. In the context of Bonella, restoring data from the non-volatile flash memory would therefore have been faster by use of a synchronous flash memory. Mills' synchronous flash interface would also have decreased sequential read access times during other operations or uses of Bonella's Flash memory. Ex. 1003, ¶111.

Moreover, Bonella discloses that his FLASH memory conforms to the "IEEE NAND Flash Specification," but can be made to conform with essentially any FLASH supplier or specification. Ex. 1005, ¶37. Bonella also discloses that "[a]ll other elements of the interface, DRAM/FLASH types, can be customized for any supplier to any application or availability of parts." *Id.*, ¶30. One of ordinary skill in the art would have therefore understood Bonella to suggest modification of his system to work with any known Flash interface, including Mills' synchronous

Flash interface, and would have been motivated to follow that suggestion. Ex. 1003, ¶112.

Therefore, Bonella in view of Mills discloses these claim elements.

d) Operating the "Volatile Memory Subsystem" at a "Third Clock Frequency"

Claim 1 recites "*operating the volatile memory subsystem at a third clock frequency when the memory system is in the second mode of operation, the third clock frequency being less than the first clock frequency*." Claim 15 recites "*the volatile memory subsystem further being operable at a third clock frequency when the memory system is in the second mode of operation, the third clock frequency being less than the clock first frequency*."[1]

Bonella discloses "*the volatile memory subsystem further being operable at a third clock frequency*." Bonella's DRAM system operates at a first clock frequency during normal operation, which Bonella refers to as "Power Level 5," where "[t]here are no preset restrictions placed on the DRAM." Ex. 1005, ¶47; Ex. 1003, ¶116. Bonella also discloses other modes of operation supported by his system, including a power saving mode which saves power in part by reducing the

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[1] The phrase "*clock first frequency*" appears to be a typographical error that should read "*first clock frequency.*" Ex. 1003, ¶115 n.6.

frequency at which the DRAM is operating. Ex. 1005, ¶50 ("...frequency is reduced to the DRAM ..."). One of ordinary skill in the art would understand that Bonella is describing several different, though complimentary, techniques for reducing power consumption, such as reducing the voltage to the DRAM, reducing the frequency of the DRAM, and reducing the number of cycle requests to the DRAM. *Id.*; Ex. 1003, ¶117.

A skilled artisan would understand a DRAM operating at a "reduced" frequency in such a power saving mode to be operating at a clock frequency lower than the clock frequency at which the DRAM would operate in a normal operating mode, such as Power level 5 of Bonella. Ex. 1003, ¶118. As explained above, *see* §V.A.1.b), DRAM operation requires a clock signal as an input to a DRAM that operates at a regular interval (*i.e.*, a frequency). *Id.*, ¶¶91-93, 118. According to the DDR2 specification at the time of Bonella's priority date, a conforming DDR2 DRAM device allows the input clock frequency to change between minimum and maximum operating frequencies. Ex. 1010, 45 ("SDRAM input clock frequency is allowed to change"); *see, e.g.*, *id.*, 67 (listing minimum and maximum clock cycle times (tCK) (*i.e.*, the inverse of the input clock frequency) for DDR2-400); Ex. 1003, ¶118.

Bonella's power flush algorithm (*i.e.*, the "*second mode*") would still be triggered during Bonella's "power saving" mode of operation (*i.e.*, when the

DRAM was operating at a "*third clock frequency*") if a power loss event occurred. Bonella teaches that the memory module's backup power source is located within the memory module, Ex. 1005, ¶29, and that the external power source can be a "Line" or "Battery," even under less than "full power" operation, *id.*, ¶46. One of ordinary skill in the art would understand that Bonella's memory module, when operating under a "power saving" mode that reduced the DRAM operating frequency (*i.e.*, a "*third clock frequency*"), could still lose its external power source and be forced to switch to the power loss algorithm (*i.e.*, the "*second mode*"). Ex. 1003, ¶119. Bonella thus teaches to one of ordinary skill in the art at least one situation where the "*volatile memory subsystem*" operates "*at a third clock frequency when the memory system is in the second mode of operation, the third clock frequency being less than the clock first frequency*."

To the extent one might argue that the Board's interpretation of "*clock frequency*" requires a particular numeric value (*i.e.*, as in number of cycles per second), it would have been obvious to operate the volatile memory at its maximum rate during normal operation (*i.e.*, in the "*first mode*"), which for DDR DRAM would be 133 MHz, and at its minimum rate during the power loss mode (*i.e.*, in the "*second mode*"), which would be 67MHz for DDR DRAM. Ex. 1014, 58. It would have been obvious to do so in order to obtain the best performance

during normal operation while saving power in the backup power system during the power loss mode. Ex. 1003, ¶¶99-100.

To the extent one might argue the claim requires the "*second mode*" necessitate or cause the "*volatile memory subsystem*" to operate "*at a third clock frequency*," such a feature would have been obvious. Specifically, it would have been obvious to use the power saving mode of Bonella ("*third clock frequency*") during performance of Bonella's power loss algorithm ("*second mode of operation*").

As explained above, *see* §V.A.1.b), Bonella's power loss algorithm ("*second mode of operation*") is triggered by emergency power loss situations. Ex. 1005, ¶¶96, 101; Ex. 1003, ¶¶94-95. Bonella discloses a backup power supply (Ex. 1005, ¶29), and states that "if power were lost and contents in the DRAM have not been saved … the intent would be to maintain a power reserve large enough to write the volatile data to a non-volatile location on the memory module" (*id.*, ¶33). One of ordinary skill in the art would know that Bonella's backup power supply is not unlimited and therefore would have been motivated to conserve power during such emergency backup operations in order to ensure backup of all unsaved data, or at least as much as possible. Ex. 1003, ¶122. That motivation would have led such an artisan to use the power saving mode of Bonella during the "*second mode*

of operation in which data is communicated between the volatile memory subsystem and the non-volatile memory subsystem."

It was well-known by the priority date of the 833 Patent that reducing power consumption while performing a volatile-to-nonvolatile flush operation would reduce the likelihood of data loss or reduce the necessary size for the backup power source. Ex. 1003, ¶¶123-124. For example, U.S. Patent Application Publication 2006/0212651 ("Ashmore") (Ex. 1008) "provides a method for reducing battery power consumption during a main power loss to reduce the likelihood of loss of user write-cached data in a write-caching mass storage controller." Ex. 1008, ¶9. Ashmore's specific technique is to "only provide[] battery power to the critical memory banks, but not to the non-critical memory banks, in order to reduce the amount of battery power consumed during the main power outage." *Id.*, ¶7. This "extend[s] the time the critical memory banks can store the critical data to reduce the likelihood of user data loss." *Id.* As another example, U.S. Patent No. 7,421,552 to Long ("Long") (Ex. 1011), discloses "provid[ing] a significantly slower clock signal to the processing circuitry" of a memory "while the controller 40 moves data from the volatile-memory storage cache 42 to the flash-based memory vault 44." Ex. 1011 (Long), 4:54-64. "As a result, less power is consumed thus enabling the use of a smaller-sized backup power source 28 (e.g., a relatively small battery)." *Id.*

One of ordinary skill in the art in possession of Bonella's system would have been motivated to reduce the power consumption during the power loss event write flushing using any known or conventional means, and would have also considered power consumption reduction techniques other than those of Ashmore and Long to obtain the same benefits, including those described in Bonella. Bonella describes reducing the operational frequency of the DRAM in order to reduce the power consumption generally, Ex. 1005, ¶50). One of ordinary skill in the art would have found it obvious to perform Bonella's power reduction technique (DRAM operational frequency reduction) during the performance of Bonella's power loss algorithm. Ex. 1003, ¶¶117-118, 125.

A skilled artisan would also have been motivated to perform this power reduction technique to decrease the risk of data loss due to insufficient backup power or to enable the use of a smaller-sized backup power source. *Id.*, ¶126; Ex. 1008, ¶7; Ex. 1011, 4:54-64. Bonella also motivates the use of his own power reduction algorithm, teaching that it "can result in major power savings." Ex. 1005, ¶50. Using Bonella's power reduction technique during the power loss algorithm would also have been the arrangement of old elements (Bonella's power reduction mode and Bonella's power loss algorithm), each performing the same function it had been known to perform, in a way that yields no more than one of ordinary skill in the art would expect from such an arrangement (reducing power

consumption during a power loss event, as suggested by Long and Ashmore). Ex. 1003, ¶126.

Reducing the operational frequency of the DRAM in such a situation would not have caused any performance issues because the transfer of data between DRAM and FLASH could not occur faster than the speed of the FLASH, which in the case of Bonella would be substantially slower than the DRAM. Ex. 1003, ¶127. Bonella teaches that various levels of a computer's memory hierarchy have different performance levels, and lists DRAM as higher performance than Flash memory. Ex. 1005, ¶65, Fig. 3. Mills discloses operating the Flash memory at a frequency "as high as 33 MHz." Ex. 1007, 17:10-25; *see also 1.8 Volt Intel StrataFlash(R) Wireless Memory (L18) (Apr. 2003)* (Ex. 1012), 25 (disclosing speeds up to 54MHz). Conversely, DRAM implementations in 2005 operated at speeds up to 400MHz. Ex. 1003, ¶127 (citing and discussing Ex. 1010, 67, 69). One of ordinary skill in the art, when considering this differential in operating frequencies, would have understood that reducing the DRAM operating frequency would not cause performance issues.

Therefore, Bonella discloses or renders obvious this claim element.

2. Claims 2 and 18 Are Unpatentable

Claims 2 and 18 depend on claims 1 and 15 respectively, and further recite "*wherein the third clock frequency is substantially equal to the second clock frequency*."

To the extent that Bonella as described above does not disclose this feature, off-the-shelf DRAM and Flash memories were available in 2007 that operated at frequencies that were "*substantially equal*" and it would have been obvious to include that limitation in the system of Bonella. Off-the-shelf Flash memories with operational frequencies between 22 MHz and 125 MHz were available, as were DDR DRAMs with operational frequencies between 67 MHz and 400 MHz. Ex. 1003, ¶133. For example, the Intel StrataFlash Memory operated at clock speeds of up to 54MHz, Ex. 1012, 25 (Table 8), and other Flash memories operated at speeds up to 125 MHz, *see, e.g.*, Elmhurst & Goldman, *A 1.8-V 128-Mb 125-MHz Multilevel Cell Flash Memory With Flexible Read While Write*, IEEE (Nov. 2003) (Ex. 1024), 4 ("The clock is operating at 125 MHz"); U.S. Pat. No. 6,614,685 to Wong (issued Sep. 2, 2003) (Ex. 1025), 1:50-58 (discussing a Flash memory operating at 100 MHz). DDR DRAM could be operated at speeds as low as 67MHz. Ex. 1014, 58; Ex. 1003, ¶133. Reducing the DRAM frequency to be substantially the same as the Flash frequency would thus be the arrangement of old elements (DRAM and Flash memories operating at frequencies they were known

to be capable of), each performing the same function it had been known to perform, in a way that yields no more than one of ordinary skill in the art would expect from such an arrangement. Ex. 1003, ¶132.

Moreover, Bonella discloses no substantial buffering mechanism that could be used to address a difference in data rates between the DRAM and Flash memories during a flush operation. Ex. 1003, ¶134; *compare with* U.S. Pat. App. Pub. No. 2003/0028733 to Tsunoda (Feb. 6, 2003) (Ex. 1015), ¶97 (buffering "to absorb a transfer speed difference between the two devices"). Bonella teaches that the power consumption of DRAM is directly proportional to its operating frequency, Ex. 1005, ¶50, so a skilled artisan would therefore be motivated to make the volatile and non-volatile clock frequencies substantially equal during the power loss algorithm flush operations (*i.e.*, the "*second mode*") to minimize transfer time and power consumption. Ex. 1003, ¶134. One of ordinary skill in the art would have thus been motivated to reduce Bonella's DRAM operating frequency to be substantially equal to the Flash memory's operating frequency during the power loss algorithm flush operations so as to obtain the maximum power savings. *Id.*, ¶134. Therefore, Bonella renders obvious these claims.

3. Claims 3 and 19 Are Unpatentable

Claims 3 and 19 depend on claims 1 and 15 respectively, and further recite "*wherein the memory system is not powered by a battery when it is in the second*

mode of operation." The 833 Patent provides "a capacitor" as an example of a non-battery power source. Ex. 1001, 4:2-4.

Bonella explains that the power loss event is powered by either a battery or capacitors: "optional Uninterruptible Power Supply (UPS) capacitors ***or*** battery (for emergency shutdown operations)." Ex. 1005, ¶29 (emphasis added). Capacitors are not a "*battery*," so when Bonella's capacitors power the memory module for emergency shutdown operations ("*the second mode of operation*"), the memory module "*is not powered by a battery*." Ex. 1003, ¶137. Therefore, Bonella discloses these claims.

4. Claims 4 and 20 Are Unpatentable

Claims 4 and 20 depend on claims 1 and 15 respectively, and further recite "*wherein the memory system switches from the first mode of operation to the second mode of operation in response to a trigger condition*."

As explained above, *see* §V.A.1.b), Bonella's "*first mode of operation*" is the memory's normal operation, and Bonella's "*second mode of operation*" is the memory's operation under the power loss algorithm. Ex. 1003, ¶¶94-97. The power loss algorithm is triggered "[w]hen the memory module controller detects a power loss event" ("*trigger condition*"). Ex. 1005, ¶101. One of ordinary skill in the art would consider this a "trigger." Ex. 1003, ¶140; *see, e.g.*, Microsoft

Computer Dictionary (5th Ed. 2002) (Ex. 1020), 530 (defining "trigger"). Therefore, Bonella discloses these claims.

5. Claims 5 and 21 Are Unpatentable

Claims 5 and 21 depend on claims 4 and 20 respectively, and further recite "*wherein the trigger condition comprises a power failure condition*."

As explained above, *see* §V.A.1.b), Bonella's "*second mode of operation*" is the memory's operation during a power loss event ("*power failure condition*"), where the memory module controller flushes critical data to the FLASH. Ex. 1005, ¶101; Ex. 1003, ¶¶94-97, 140. Bonella characterizes this power loss event as triggering a "power failure data save function." Ex. 1005, ¶96. One of ordinary skill in the art would understand Bonella's power loss event to thus be a "*power failure condition*" because it is a event triggered by a power failure. Ex. 1003, ¶143. Therefore, Bonella discloses these claims.

6. Claims 6 and 22 Are Unpatentable

Claims 6 and 22 depend on claims 1 and 15 respectively, and further recite "*wherein the memory system further comprises a printed circuit board and the volatile memory subsystem and the non-volatile memory subsystem are located on the printed circuit board*."

Bonella discloses "a memory module including a volatile memory, a non-volatile memory, and a controller" that interfaces "to a host system, such as, for

example, a personal computer ….” Ex. 1005, ¶6. The memory module is characterized as a “plug-and-play end-user add-in memory module,” *id.*, ¶2, and “an end-user add-in device,” *id.*, ¶23. Bonella’s provisional application also teaches that certain functionality is “on board” the module. Ex. 1006, 30 (§4.2.2.10.6.2). One of ordinary skill in the art, when considering Bonella’s disclosure as a whole, would understand that Bonella’s memory module is implemented on a “*printed circuit board*.” Ex. 1003, ¶146.

To the extent one might argue that Bonella as combined above does not sufficiently disclose this claim element, it would have been obvious to so include it in the system of Bonella. Bonella teaches that the memory module “may be custom designed, and/or integrated in any suitable manner,” Ex. 1005, ¶32, and that “[t]he present invention is not limited to any particular portioning, distribution, or grouping of functional blocks onto one or more integrated circuits,” *id.*, ¶30.

The use of printed circuit boards on which multiple memories were located for computer memory modules such as that of Bonella was known by the priority date of the 833 patent and in fact common. Ex. 1003, ¶¶147-148; *see, e.g*. U.S. Patent App. Pub. No. 2007/0070669 to Tsern (Ex. 1016), Fig. 9A, ¶52; Patterson & Hennessy, Computer Organization & Design (2d Ed. 1998) (Ex. 1017), 623; *see also id.*, 624. Indeed, the 833 patent admits as much. Ex. 1001, 1:14-17. It was also known to implement hybrid memory modules such as Bonella’s on a single

printed circuit board. Ex. 1003, ¶149. For example, U.S. Patent No. 7,136,978 to Miura (filed May 28, 2003) (Ex. 1018) discloses a single printed circuit board that contains a Flash memory, two DRAMs, and a memory controller. Ex. 1018, Figs. 27A-B, 26:45-27:25.

To use such a physical configuration in the system of Bonella would therefore have been merely the use of a known structure for its known use to achieve a predictable result. Ex. 1003, ¶150. Moreover, a skilled artisan would have been motivated to locate the volatile and non-volatile memories of Bonella on a printed circuit board as claimed because that was a standard configuration on the market for computer systems such as those with which Bonella is concerned. *Id.*, ¶150; *see* Ex. 1017, 623-24. Printed circuit boards were the most common substrate for memory modules, and one of ordinary skill would have been motivated to use a printed circuit board due to its low cost, superior performance, reliability, and widespread use, and. Ex. 1003, ¶150; *see* Catsoulis, *Designing Embedded Hardware* (2d Ed. 2005) (Ex. 1023), 140-141.

One of ordinary skill in the art would also have been motivated to implement a hybrid memory module such as Bonella's on a single printed circuit board because, by placing the chips in "proximity to one another" on a single board, "the length of the wiring between the chips can be reduced" and "the memory module can be manufactured with a less number of processes." Ex. 1018, 27:6-25. It was

also well-known that placing chips on a single board can improve communication latency between the chips, reduce noise, and improve the overall reliability. Ex. 1003, ¶151. A skilled artisan would have been motivated to implement Bonella's memory module on a single printed circuit board to obtain these same efficiencies and benefits. Ex. 1003, ¶151. It therefore would have been obvious to implement Bonella's memory module on a single printed circuit board such that "*the volatile memory subsystem and the non-volatile memory subsystem are located on the printed circuit board*."

Therefore, Bonella renders obvious these claims.

7. Claims 7 and 23 Are Unpatentable

Claims 7 and 23 depend on claims 1 and 15 respectively, and further recite "*wherein data communicated between the volatile memory subsystem and the non-volatile memory subsystem is intermediate data from a host computer system computation*."

Claims 7 and 23 recite non-functional descriptive material because there is no claimed relationship between the characterization of the data ("*intermediate data from a host computer system computation*") and the functionality of the system. The characterization of the "*data*" is thus printed matter devoid of any functional relationship with the claimed functionality, and should not be given patentable weight. *See In re Ngai*, 367 F.3d 1336, 1339 (Fed. Cir. 2004).

Bonella teaches that "*data communicated between the volatile memory subsystem and the non-volatile memory subsystem*" includes write buffer data flushed from DRAM to Flash memory as part of Bonella's power loss algorithm. Ex. 1005, ¶96; Ex. 1003, ¶¶103-104, 154. Bonella's provisional application contemplates video recording, video editing, and gaming applications, Ex. 1006, 7-9, but this data could be any conceivable critical data still pending in the DRAM write buffer at the time of a power loss event. Bonella's power loss algorithm does not depend on the specific characterization of the data contained in the DRAM write buffer, and will instead operate the same way regardless of whether the data comprises video data, gaming data, or "*intermediate data from a host computer system computation*." Ex. 1003, ¶154. Bonella therefore discloses the claimed functionality regardless of whether it discloses the specific characterization of the claimed "*data*."

Additionally, Bonella's write buffer data could be considered "*intermediate data from a host computer system computation*" under the broadest reasonable interpretation of that phrase. First, it is "*intermediate data*" because it is stored in an intermediate location (Bonella's DRAM write buffer) on its way from the host to the hard disk drive. Ex. 1003, ¶155. Bonella teaches periodically flushing the DRAM write buffer data to the Flash "[d]ue to the volatile nature of DRAM." Ex. 1005, ¶96. Second, it is "*from a host computer system computation*" because the

write data resulted from a write operation, which an ordinary artisan would understand is one common type of computation performed by a computer. Ex. 1003, ¶155.

Therefore, Bonella discloses these claims.

8. Claims 8 and 24 Are Unpatentable

Claims 8 and 24 depend on claims 1 and 15 respectively, and further recite "*wherein data communicated between the volatile memory subsystem and the non-volatile memory subsystem is backup data from a backup operation*." The claim does not require that the "*backup data from a backup operation*" be associated in any way with the claimed "*second mode*" other than that data is "*communicated between the volatile memory subsystem and the non-volatile memory subsystem*" in both cases.

Claims 8 and 24 recite non-functional descriptive material because there is no claimed relationship between the characterization of the data ("*backup data from a backup operation*") and the functionality of the system. The characterization of the "*data*" is thus printed matter devoid of any functional relationship with the claimed functionality, and should not be given patentable weight. *See In re Ngai*, 367 F.3d at 1339.

As explained above, *see*, Bonella teaches that "*data communicated between the volatile memory subsystem and the non-volatile memory subsystem*" includes

write buffer data flushed from DRAM to Flash memory as part of Bonella's power loss algorithm. Ex. 1005, ¶96; Ex. 1003, ¶¶103-104. This write buffer data can include data intended for the hard disk drive. Ex. 1005, ¶99. This data could be any conceivable data still pending in the DRAM write buffer at the time of a power loss event. Bonella's power loss algorithm does not depend on the specific characterization of the data contained in the DRAM write buffer, and will instead operate the same way regardless of whether the data comprises video data, gaming data, or "*backup data from a backup operation*." Ex. 1003, ¶164. Bonella therefore discloses the claimed functionality regardless of whether it discloses the specific characterization of the claimed "*data*."

Additionally, Bonella teaches that the conventional operation of the DRAM write buffer is to periodically write the buffer data to Flash for backup. Ex. 1005, ¶96; Ex. 1003, ¶165. Specifically, this means that *all* data written to the DRAM write buffer will be backed up to Flash based on one of the various trigger events, including a timer, a critical function such as closing a program, or a power loss event. Ex. 1005, ¶96; Ex. 1003, ¶166. In this context, all data written to the DRAM write buffer is "*backup data from a backup operation*" because it is data destined to be backed up to Flash memory, regardless of whether a power loss event occurs. Ex. 1003, ¶166. The data is thus "*backup data*" (data that will be backed up from DRAM to Flash) from a "*backup operation*" (the flushing of data

from DRAM to Flash). Bonella also teaches that the disk drive may be used "to hold a back-up image of the memory module," so updates to this image would contain "*backup data*" to be stored within the back-up image. Ex. 1005, ¶88; Ex. 1003, ¶166.

Therefore, Bonella discloses these claims.

9. Claims 9 and 25 Are Unpatentable

Claims 9 and 25 depend on claims 8 and 24 respectively, and further recite "*wherein the backup operation is conducted at repeating time intervals*."

Bonella discloses that the flushing of DRAM data to Flash is normally performed periodically on a timer: "Due to the volatile nature of DRAM, periodic writing of the critical DRAM data to flash for backup is advantageous" and can be "done based on a timer." Ex. 1005, ¶96. Specifically, the flushing of data from DRAM to Flash is a "*backup operation*," *see* Ex. 1003, ¶¶165-166, and Bonella teaches that the flushing can occur periodically based on a timer ("*at repeating time intervals*"). Ex. 1003, ¶172. Therefore, Bonella discloses these claims.

10. Claims 10 and 26 Are Unpatentable

Claims 10 and 26 depend on claims 9 and 25 respectively, and further recite "*wherein the backup operation is initiated in response to a trigger event*."

Bonella discloses "*wherein the backup operation is initiated in response to a trigger event,*" *e.g.*, the timer triggers the write buffer flushing. Ex. 1005, ¶96.

Alternatively, closing a program can trigger the write buffer flushing, and is also a "*trigger event*." *Id.*; Ex. 1003, ¶176. Therefore, Bonella discloses these claims.

11. Claims 11 and 27 Are Unpatentable

Claims 11 and 27 depend on claims 1 and 15 respectively, and further recite "*wherein the second mode of operation comprises a backup operation in which data is communicated from the volatile memory subsystem to the non-volatile memory subsystem*."

Bonella discloses "*the second mode of operation*" (the operations during the power loss event) "*comprises a backup operation in which data is communicated from the volatile memory subsystem to the non-volatile memory subsystem*." Specifically, Bonella discloses a "power failure data save function" Ex. 1005, ¶96, that flushes critical data to the Flash memory during a power loss event, *id.*, ¶101; Ex. 1003, ¶180. Therefore, Bonella discloses these claims.

12. Claims 12 and 28 Are Unpatentable

Claims 12 and 28 depend on claims 1 and 15 respectively, and further recite "*wherein the second mode of operation comprises a restore operation in which data is communicated from the non-volatile memory subsystem to the volatile memory subsystem*."

Bonella explains that during a power loss event, "the data that is flagged as critical is flushed to the FLASH, a flag is set and the memory module then shuts

down." Ex. 1005, ¶101. Once power is restored, the data is "restored to the DRAM" ("*a restore operation in which data is communicated from the non-volatile memory subsystem to the volatile memory subsystem*"). *Id.* This functionality is part of the power loss algorithm, and therefore part of the "*second mode of operation*." Ex. 1003, ¶183.

Therefore, Bonella discloses these claims.

13. Claims 13 and 29 Are Unpatentable

Claims 13 and 29 depend on claims 1 and 15 respectively, and further recite "*wherein one or more of the first, second or third clock frequencies is configurable by the memory system*."

Bonella explains that the memory module has power management features that are "user configured and/or system configured." Ex. 1005, ¶45. These power management features include the DRAM frequency reduction functionality. *Id.*, ¶¶49-50. Specifically, Bonella explains that Power Level 4, which "reduces power by limiting the DRAM performance" and is "user configurable," *id.*, ¶48. This configuration information is obtained by the memory controller, which then uses the information to carry out any necessary power reduction. *Id.*, ¶45.

Bonella also teaches that the DRAM interface can correspond to the "DDR2 DRAM specification," *id.*, ¶36, and the operational frequencies of DDR2 DRAM were configurable, Ex. 1003, ¶187; *see, e.g.*, Ex. 1010, 39 ("The user may change

the external clock frequency …."), 45 ("DDR2 SDRAM input clock frequency can be changed"); *see, e.g.*, *id.*, 67 (listing a minimum and maximum clock cycle time (tCK) (*i.e.*, the inverse of the input clock frequency) for DDR2-400). Bonella thus teaches to one of ordinary skill in the art that the primary operating frequency of the DRAM (i.e., the "*first clock frequency*") "*is configurable by the memory system*" based on the user configuration. Ex. 1003, ¶¶186-187.

To the extent Bonella does not disclose this feature, it would have been obvious to make "*one or more of the first, second or third clock frequencies*" be "*configurable by the memory system*" at the direction of a user. Memory devices including configurable frequency settings were well known by 2007. For example, as explained above DDR2 SDRAM allowed for configurable input clock frequencies (either the "*first*" or "*third clock frequencies*"), and Bonella suggests that the system's power management features are "user configured and/or system configured." *See* Ex. 1003, ¶¶186, 188. Bonella also suggests adjusting the operational frequency of DRAM so as to reduce power consumption. Ex. 1005, ¶¶49-50. Even Flash memory clocks were known to be configurable. Ex. 1003, ¶188; *see, e.g.*, Ex. 1012, 25 (Table 8) (showing configurable frequencies).

One of ordinary skill in the art would have thus been motivated to make one or more of Bonella's clock frequencies "*configurable by the memory system*" at the direction of the user so as to obtain the benefit of configurability and power

savings. Ex. 1003, ¶189. To allow for such configurability in the system of Bonella would also have been merely the use of a known technique (configurability of memory input clock frequencies) for its known use (to selectively reduce power based on user need) to achieve a predictable result. *Id.*, ¶189.

Therefore, Bonella discloses these claims.

14. Claims 14 and 30 Are Unpatentable

Claims 14 and 30 depend on claims 1 and 15 respectively, and further recite "*wherein one or more of the first, second or third clock frequencies is configurable by a user*."

As explained above, *see* §V.A.13, Bonella explains that "*one or more of the first, second or third clock frequencies is configurable by the memory system*" at the direction of the user. *See* Ex. 1003, ¶¶186-187; *see, e.g.*, Ex. 1005, ¶45 ("user configured and/or system configured."), ¶48 (explaining that Power Level 4, which "reduces power by limiting the DRAM performance," is "user configurable."); Ex. 1010, 39 ("The user may change the external clock frequency ….").

As explained above, *see* §V.A.13, to the extent Bonella does not disclose this feature, it would have been obvious. *See* Ex. 1003, ¶¶188, 193.

Therefore, Bonella discloses these claims.

15. Claim 16 Is Unpatentable

Claim 16 depends on claim 15, and further recites "*a controller configured to decouple the non-volatile memory subsystem from the volatile memory subsystem in the first mode of operation and to couple the non-volatile memory subsystem to the volatile memory subsystem in the second mode of operation*."

As demonstrated above, *see* §§V.A.1.b)-c), the controller of Bonella discloses (1) "*a first mode of operation in which data is communicated between the volatile memory subsystem and the host system*" and (2) "*a second mode of operation in which data is communicated between the volatile memory subsystem and the non-volatile memory subsystem.*" Ex. 1003, ¶¶94-97, 103-104.

Specifically, during Bonella's conventional operation ("*a first mode*"), write data is sent from a host to the DRAM write buffer. *Id.*, ¶¶94-97. Unless and until a write buffer flush event occurs, this data remains in the DRAM write buffer and is not transferred to "*the non-volatile memory subsystem from the volatile memory subsystem in the first mode of operation*." *Id.*, ¶197. Conversely, during operation of Bonella's power loss algorithm ("*a second mode*"), data is sent from the DRAM to the Flash memory, *id.*, ¶¶103-104 above, and is transferred to "*the non-volatile memory subsystem to the volatile memory subsystem in the second mode of operation*," *id.*, ¶197.

Bonella discloses that this transferring occurs via "*decouple[ing]*" and "*coupl[ing]*" the subsystems as needed for a given transfer. For example, Bonella discloses the internal structure of his controller as including a router through which data may be communicated between the two memories. Ex. 1005, Fig. 2, ¶¶41-44. Bonella further discloses that the router "is made up of path multiplexers." *Id.*, ¶43. A skilled artisan would understand a multiplexer to comprise a series of switches (similar to the switches of the 833 Patent, *see, e.g.*, Ex. 1001, 6:63-7:7) that functionally and electrically couple or decouple components to which they are connected, Ex. 1003, ¶198; *see, e.g.*, Ex. 1017, B-9 (describing multiplexers); *see also id.*, B-19 (same).

Therefore, Bonella discloses these claims.

16. Claim 17 Is Unpatentable

Claim 17 depends on claim 15, and further recites "*a plurality of power supplies and a switch configured to selectively deliver power from the plurality of power supplies to the volatile memory subsystem and the non-volatile memory subsystem as a function of the mode of operation*."

Bonella discloses that the memory module is provided a standard power source and also a backup power source. Ex. 1005, ¶33; Ex. 1003, ¶205. Bonella's system selectively delivers power from one of these power sources depending on whether it is operating conventionally ("*first mode*") or is responding to a power

loss event ("*second mode*"). Ex. 1005, ¶101. Bonella's power functionality as a whole operates to fulfill the claimed "*switch*" because it switches between the standard power source to the backup power source when necessary. Ex. 1003, ¶206; *see, e.g.*, Ex. 1005, ¶¶29-31.

Therefore, Bonella discloses these claims.

B. Claims 1-30 Are Obvious Over Bonella, Mills, and Ashmore

To the extent one might argue Bonella as combined above with Mills does not (1) disclose using the power saving mode of Bonella while in the "*second mode of operation*," *i.e.*, during performance of Bonella's power loss algorithm, or (2) render doing so obvious in view of the knowledge of one of ordinary skill in the art, it would have been obvious to do so in view of the specific teachings of Ashmore. Ex. 1003, ¶128. As explained above, *see* §V.A.1.d), Ashmore teaches "reducing battery power consumption during a main power loss to reduce the likelihood of loss of user write-cached data in a write-caching mass storage controller." Ex. 1008, ¶¶7, 9. Bonella and Ashmore are analogous art to the 833 Patent because each is from the field of memory systems. Ex. 1001, 3:60-63; Ex. 1005, ¶2; Ex. 1008, ¶1 ("The present invention relates … particularly to write-caching controllers that use a battery to avoid loss of write-cached user data."); Ex. 1003, ¶128.

One of ordinary skill in the art would have found it obvious to perform Bonella's power reduction technique (DRAM operational frequency reduction) during the performance of Bonella's power loss algorithm. Ex. 1003, ¶129. Ashmore's disclosure of the benefits of power reduction during would have motivated one of ordinary skill to consider other power consumption reduction techniques to obtain the same benefits, *i.e.*, "to reduce the amount of battery power consumed during the main power outage … to reduce the likelihood of user data loss" (*see* Ex. 1008, ¶9), including those described in Bonella. Ashmore thus motivates one of ordinary skill in the art in possession of Bonella's system to reduce the power consumption during the power loss event write flushing using any known or conventional means, including Bonella's existing mechanism of reducing the DRAM operational frequency. Ex. 1003, ¶129.

As explained above, *see* §V.A.1.d), this would also have been the arrangement of old elements, each performing the same function it had been known to perform, in a way that yields no more than one of ordinary skill in the art would expect from such an arrangement. Ex. 1003, ¶126. It would also have not caused any performance issues due to DRAM's higher comparative speed than Flash. Ex. 1003, ¶127 (citing and discussing, *e.g.*, Exs. 1010, 1012, 1015).

C. Claims 7 and 23 Are Obvious Over Bonella, Mills, with or without Ashmore, and Larson

Claims 7 and 23 depend on claims 1 and 15 respectively, and further recite "*wherein data communicated between the volatile memory subsystem and the non-volatile memory subsystem is intermediate data from a host computer system computation.*"

To the extent one might argue that Bonella as combined above does not sufficiently disclose this claim element, it would have been obvious to so include it in the system of Bonella. Ex. 1003, ¶156. Storing "intermediate" data from host computations to persistent storage before retrieving it again for later use was well-known in the art by the 833 Patent's priority date. For example, U.S. Patent No. 6,571,244 to Larson ("Larson") (published May 27, 2003) (Ex. 1019) teaches that the large scale sorting of database records often involves storing intermediate data to persistent storage for later retrieval:

> Operations performed on databases can be easily accommodated if all of the data records are first loaded into volatile main memory (i.e., RAM) for processing. However, databases often contain large numbers of data records, which far surpass the volatile memory resources. As a result, subsets of data records are processed in the main memory and then written back to disk after they are processed.

Ex. 1019, 1:14-31.

Larson specifically describes a method of sorting a large number of data records using "Mergesort," the standard technique for sorting large sets, called Load-Sort-Store where data sets are repeatedly analyzed, stored to memory, and re-loaded for later analysis. Ex. 1019, 1:40-63, 1:14-31; Ex. 1003, ¶157. Larson then describes various improvements to the run formation phase of the Load-Sort-Store technique. Ex. 1019, 1:30-31, 6:30-63. Larson's improved run formation functionality will still perform Mergesort's merge phase "that repeatedly merges runs into larger and larger runs, until a single run has been created," thus loading the runs ("*intermediate data*") back into memory. *See, e.g.*, *id.*, 1:23-31. Regardless whether one were to use the prior art method or Larson's improved run formation process, one of ordinary skill in the art would understand that Larson discloses writing "*intermediate data*" (a run of sorted records) "*from a host computer system computation*" (a large scale sorting operation) to persistent storage, *id.*, *e.g.*, a hard disk, *id.*, 6:20-22; Ex. 1003, ¶158.

Bonella and Larson are analogous art to the 833 Patent because each is from the field of memory systems and their operations. Ex. 1001, 3:60-63; Ex. 1005, ¶2; Ex. 1019, 1:14-31. Mills and Ashmore are likewise analogous art as explained above. *See* §§V.A.1.c), V.B; Ex. 1003, ¶¶108, 128. Additionally, Larson is particularly pertinent to the problems with which the 833 Patent was concerned:

"hold[ing] intermediate data results … when the host computer system is engaged in a long computation." Ex. 1001, 7:48-51; *see, e.g.*, Ex. 1019, 1:14:31.

It would have been obvious to one of ordinary skill in the art to modify Bonella's system to execute a large scale sorting operation such as the Mergesort operation described by Larson. Ex. 1003, ¶160. As explained above, Bonella teaches a write buffer that buffers any writes to its hard disk and Larson teaches a process that writes "*intermediate data from a host computer system computation*" to persistent storage, *e.g.*, a hard disk. Running either Larson's Load-Sort-Store or his improved algorithm on a system that includes Bonella's memory module would therefore buffer writes of Larson's runs in Bonella's write buffer. Ex. 1003, ¶160. If a power loss event occurred during such a computation, Bonella would flush that write data from DRAM to Flash memory ("*wherein data communicated between the volatile memory subsystem and the non-volatile memory subsystem is intermediate data from a host computer system computation*"). *Id.*

Such a combination would have been obvious because it would be the arrangement of old elements (Bonella's general purpose memory module being used for Larson's sorting algorithm), each performing the same function it had been known to perform (Larson's algorithm sorting and Bonella's memory module caching writes), in a way that yields no more than one of ordinary skill in the art would expect from such an arrangement. Ex. 1003, ¶161. One of ordinary skill

would also have been motivated to execute Larson's sorting algorithms on Bonella's system because it would allow the sorting of databases that can only fit on a hard disk. Ex. 1019, 1: 14-22; Ex. 1003, ¶161. Therefore, such a combination would have been obvious.

D. Claims 8-10 and 24-26 Are Obvious Over Bonella, Mills, with or without Ashmore, and Windows 2000

1. Claims 8 and 24 Are Unpatentable

Claims 8 and 24 depend on claims 1 and 15 respectively, and further recite "*wherein data communicated between the volatile memory subsystem and the non-volatile memory subsystem is backup data from a backup operation*." The claim does not require that the "*backup operation*" be associated in any way with the claimed "*second mode*" other than that "*data communicated between the volatile memory subsystem and the non-volatile memory subsystem*" in both cases.

To the extent one might argue that Bonella as combined above does not sufficiently disclose this claim element, it would have been obvious to so include it in the system of Bonella. Backup operations that backup data to persistent memory were ubiquitous in the art by the priority date of the 833 patent. Ex. 1003, ¶167. For example, Microsoft Windows 2000 included functionality that allowed users to perform a variety of different types of backups, including backups on a daily basis: "A daily backup copies all selected files that have been modified on the day that the daily backup is performed." Microsoft Windows 2000

Professional Resource Kit ("Windows 2000") (2000) (Ex. 1021), 798; *see also* Ex. 1022 (listing Feb. 2, 2000 date of first publication). "Windows 2000 can back up files to a variety of storage devices, including … disk volumes" and "another local hard disk." Ex. 1021, 799. "Regular backups of local hard disks prevents data loss from disk drive failures, disk controller errors, power outages, virus infection, and other possible problems." Ex. 1021, 797.; Ex. 1003, ¶167.

Bonella and Windows 2000 are analogous art to the 833 Patent because each is from the field of memory systems and their operations. Ex. 1001, 3:60-63; Ex. 1005, ¶2; Ex. 1021, 1:14-31. Mills and Ashmore are likewise analogous art as explained above. *See* §§V.A.1.c), V.B; Ex. 1003, ¶¶108, 128. Additionally, Windows 2000 is particularly pertinent to the problems with which the 833 Patent was concerned: backing up data. Ex. 1001, 1:28-31; *see, e.g.*, Ex. 1021, 797; Ex. 1003, ¶168.

One of ordinary skill in the art would have been motivated to perform the daily backup taught by Windows 2000 in Bonella's system for the benefit of preventing data loss. Such a backup operation would have involved writing that backup data to the other local hard disk, where it would be buffered using Bonella's DRAM write buffer. Ex. 1003, ¶169. Such a combination would have been obvious because it would be the arrangement of old elements (Bonella's DRAM write buffer and Windows 2000's daily backup), each performing the same

function it had been known to perform (Bonella's DRAM write buffer buffering writes and Windows 2000's daily backup performing a daily backup), in a way that yields no more than one of ordinary skill in the art would expect from such an arrangement. *Id.*, ¶169.

2. Claims 9 and 25 Are Unpatentable

Claims 9 and 25 depend on claims 8 and 24 respectively, and further recite "*wherein the backup operation is conducted at repeating time intervals*."

To the extent one might argue that Bonella as combined above does not sufficiently disclose this claim element, it would have been obvious to so include it in the system of Bonella. As explained above, *see* §V.A.8, Windows 2000 discloses daily backup operations that backup data to persistent memory, and it would have been obvious to incorporate such functionality into Bonella's system. Ex. 1003, ¶¶167-169. As combined, Windows 2000 daily backup operation would be "*conducted at repeating time intervals*" because it is performed daily. Ex. 1003, ¶173.

3. Claims 10 and 26 Are Unpatentable

Claims 10 and 26 depend on claims 9 and 25 respectively, and further recite "*wherein the backup operation is initiated in response to a trigger event*."

To the extent one might argue that Bonella as combined above does not sufficiently disclose this claim element, it would have been obvious to so include it

in the system of Bonella. As explained above, *see* §V.D.1, Windows 2000 discloses daily backup operations that backup data to persistent memory, and it would have been obvious to incorporate such functionality into Bonella's system. Ex. 1003, ¶¶167-169. As combined, Windows 2000 daily backup operation would be "*initiated in response to a trigger event,*" *i.e.*, a new day. For example, Windows 2000 explains that a daily backup can be run every Monday through Thursday. Ex. 1003, ¶177; Ex. 1021, 804.

E. Claim 16 Is Obvious Over Bonella, Mills, with or without Ashmore, and Klein

Claim 16 depends on claim 15, and further recites "*a controller configured to decouple the non-volatile memory subsystem from the volatile memory subsystem in the first mode of operation and to couple the non-volatile memory subsystem to the volatile memory subsystem in the second mode of operation*."

To the extent one might argue that Bonella does not sufficiently disclose this claim element, it would have been obvious to include it in the system of Bonella. Temporarily decoupling unused memory to obtain power savings was well-known at the time of the invention. Ex. 1003, ¶200.

For example, U.S. Patent No. 6,721,860 to Klein (Ex. 1009) discloses a method of reducing data bus capacitance by decoupling un-accessed memory circuits during transfers to or from other memory circuits. Ex. 1009, Abstract. Klein explains that reducing the capacitance of the bus by decoupling unused

memory banks can increase the memory access speed. *Id.*, 1:39-48, 1:66-2:4. Klein discloses an embodiment with one memory controller and two memory circuits, the memory circuits separated from a common bus via switches. *Id.*, Fig. 3, 3:47-67. When the memory controller needs to access data in one of the memories, it can switch off the unused memory, thereby reducing the parasitic capacitance. *Id.*, 4:7-17; Ex. 1003, ¶200.

Bonella and Klein are analogous art to the 833 Patent because each is from the field of memory systems. Ex. 1001, 3:60-63; Ex. 1005, ¶2; Ex. 1009, 1:16-18; Ex. 1003, ¶201. Mills and Ashmore are likewise analogous art as explained above. *See* §§V.A.1.c), V.B; Ex. 1003, ¶¶108, 128.

At the time of the invention, it would have been obvious to one of ordinary skill in the art to decouple Bonella's Flash memory when it was not being used and to re-couple it when it was needed, per the teachings of Klein. Ex. 1003, ¶202. Bonella contemplates certain situations where the Flash memory is not utilized (such as when writes are being cached by DRAM, Ex. 1005, ¶96), and Klein explains that decoupling unused memories reduces the parasitic capacitance of a shared bus (*e.g.*, data, address, and control lines between components) and can allow for increased access speed, (Ex. 1009, 1:39-48, 1:66-2:4). Ex. 1003, ¶202. Bonella discloses that it's shared data, address, and control lines may be implemented in part by a router block that includes multiplexers for address,

command, and data lines. Ex. 1005, ¶43. Such functionality would benefit from decreased parasitic capacitance in the same way as Klein's shared bus. Ex. 1003, ¶202. One of ordinary skill in the art would have thus been motivated to modify Bonella to selectively "*couple*" and "*decouple*" the Flash memory based on whether it was needed so as to reduce this parasitic capacitance and allow for a higher access speed between Bonella's host and DRAM, per the teachings of Klein. *Id.* Such a modification of Bonella would have therefore been obvious.

F. Claim 17 Is Obvious Over Bonella, Mills, with or without Ashmore, and Maeda

Claim 17 depends on claim 15, and further recites "*a plurality of power supplies and a switch configured to selectively deliver power from the plurality of power supplies to the volatile memory subsystem and the non-volatile memory subsystem as a function of the mode of operation*."

To the extent one might argue that Bonella does not sufficiently disclose using a "*switch*" to "*selectively deliver power from the plurality of power supplies*," it would have been obvious to include such a switch in the system of Bonella. Using switches to select between power sources was well-known in the art. For example, U.S. Patent Application Publication No. 2005/0249011 to Maeda ("Maeda") (Ex. 1013) discloses a switch that switches a power supply from a main power supply to a backup power supply, such as a battery power supply, once a power loss event is detected. Ex. 1013, ¶9, Figs 1, 3; Ex. 1003, ¶207.

Bonella and Maeda are analogous art to the 833 Patent because each is from the field of memory systems. Ex. 1003, ¶208; Ex. 1001, 3:60-63; Ex. 1005, ¶2; Ex. 1013, ¶2. Mills and Ashmore are likewise analogous art as explained above. *See* §§V.A.1.c), V.B; Ex. 1003, ¶¶108, 128.

It would have been obvious in 2007 to modify Bonella to use a switch such as is disclosed by Maeda to switch between the system power and a backup power source once a power loss event is detected. Ex. 1003, ¶209. As explained above, Bonella already discloses switching to a backup power source, and, to the extent that the claim requires a specific hardware switch element, Maeda shows that such hardware switch elements were known in the art. The use of Maeda's switch in Bonella would simply be the arrangement of old elements (Bonella's system and Maeda's switch), each performing the same function it had been known to perform (Maeda's switch being used to switch power in Bonella's system), in a way that yields no more than one of ordinary skill in the art would expect from such an arrangement (Bonella's power switching accomplished using Maeda's switch). Ex. 1003, ¶209. Such a modification of Bonella would have therefore been obvious.

VI. CONCLUSION

For the foregoing reasons, the challenged claims are unpatentable.

Dated: January 13, 2017 Respectfully Submitted,

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CERTIFICATE OF COMPLIANCE

I hereby certify that this petition complies with the type-volume limitations of 37 C.F.R. § 42.24, because it contains 12,758 words (as determined by the Microsoft Word word-processing system used to prepare the petition), excluding the parts of the petition exempted by 37 C.F.R. § 42.24.

Dated: January 13, 2017

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PETITION FOR INTER PARTES REVIEW

OF U.S. PATENT NO. 8,301,833

Attachment A:

Proof of Service of the Petition

CERTIFICATE OF SERVICE

I hereby certify that on this 13th day of January, 2017, a copy of this Petition, including all attachments, appendices and exhibits, has been served in its entirety by overnight mail on the following counsel of record for patent owner:

Nixon Peabody LLP
P.O. Box 26769
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Dated: January 13, 2017

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PETITION FOR INTER PARTES REVIEW

OF U.S. PATENT NO. 8,301,833

Attachment B:

List of Evidence and Exhibits Relied Upon in Petition

Exhibit #	Reference Name
1001	U.S. Patent No. 8,301,833
1002	File History of U.S. Patent No. 8,301,833
1003	Declaration of Ron Maltiel
1004	Curriculum Vitae of Ron Maltiel
1005	U.S. Patent App. Pub. No. 2007/0136523 A1 to Bonella
1006	U.S. Provisional Pat. App. No. 60/749,267 to Bonella
1007	U.S. Patent No. 6,026,465 to Mills
1008	U.S. Patent App. Pub. No. 2006/0212651 A1 to Ashmore
1009	U.S. Patent No. 6,721,860 to Klein
1010	JEDEC Standard, DDR2 SDRAM Specification, JESD79-2B (Jan. 2005)
1011	U.S. Patent No. 7,421,552 to Long
1012	Intel, *1.8 Volt Intel StrataFlash(R) Wireless Memory* (L18) (Apr. 2003)
1013	U.S. Patent App. Pub. No. 2005/0249011 A1 to Maeda
1014	JEDEC Standard, DDR SDRAM Specification, JESD79 (Jun. 2000)
1015	U.S. Patent App. Pub. No. 2003/0028733 to Tsunoda
1016	U.S. Patent App. Pub. No. 2007/0070669 to Tsern
1017	Patterson & Hennessy, Computer Organization & Design (2d Ed. 1998)
1018	U.S. Patent No. 7,136,978 to Miura
1019	U.S. Patent No. 6,571,244 to Larson

Exhibit #	Reference Name
1020	Microsoft Computer Dictionary (5th Ed.) (2002)
1021	Microsoft Windows 2000 Professional Resource Kit (2000)
1022	U.S. Copyright Office registration for Microsoft Windows 2000 Professional Resource Kit (2000)
1023	Catsoulis, *Designing Embedded Hardware* (2d Ed. 2005)
1024	Elmhurst & Goldman, *A 1.8-V 128-Mb 126-MHz Multilevel Cell Flash Memory With Flexible Read While Write*, IEEE J. OF SOLID-STATE CIRCUITS, vol. 38, no. 11 (Nov. 2003)
1025	U.S. Patent No. 6,614,685 to Wong