I, Julie Carlson, declare as follows:

1. I have personal knowledge of the facts set forth herein, and if called to testify, I could and would competently testify to the same.

2. I have been involved in semiconductor standardization and publication services for over twenty years. For nearly all of this time, I have worked at JEDEC, a standards-setting organization for the microelectronics industry, to edit, publish, and maintain JEDEC business records and standards developed by its numerous committees and subcommittees.

3. I have been involved with the standardization and publication activities of JEDEC continuously since 1997. I was the Manager of Standards and Publications at JEDEC from February 1997 through June 2005. Since June 2005, I have continued to work for JEDEC as a Consultant where my responsibilities include the maintenance and publication of JEDEC documents and standards. In addition, I am familiar with JEDEC's historical record-keeping and publication practices since at least 1992, based on my review of JEDEC's business records since that time and my regular discussions with JEDEC employees and members.

4. For over 50 years, JEDEC has been the global leader in developing and publishing open standards for the microelectronics industry. JEDEC's membership consists of more than 3,000 volunteers representing nearly 300

member companies, and includes key technical individuals from most device, assembly, system and testing companies. JEDEC publications and standards are adopted worldwide. JEDEC is accredited by ANSI and maintains liaisons with numerous standards bodies throughout the world.

5. Since at least 2000, JEDEC standards have been publicly available for download from the JEDEC website (https://www.jedec.org), where they are cataloged and indexed by keyword and technological subject matter. By 2000, the JEDEC website was publicly available and commonly used by manufactures, companies in the microelectronics industry, and other interested parties to access and obtain standards information pertaining to that industry. Anyone interested can join JEDEC online, at JEDEC.org.

6. This declaration concerns two JEDEC standards. The first standard is JEDEC STANDARD, FBDIMM: Advanced Memory Buffer (AMB), JESD82-20 (March 2007) (hereinafter, "JESD82-20 Standard"), which is a standard published by JEDEC. I have reviewed the JESD82-20 Standard. The copy of the JESD82-20 Standard attached to this declaration as Exhibit A is identical to the copy of the JESD82-20 Standard in JEDEC's files. The second standard is JEDEC STANDARD, FBDIMM Specification: DDR2 SDRAM Fully Buffered DIMM (FBDIMM) Design Specification, JESD205 (March 2007) (hereinafter, "JESD205 Standard"), which is a standard published by JEDEC. I have reviewed the

JESD205 Standard. The copy of the JESD205 Standard attached to this declaration as Exhibit B is identical to the copy of the JESD205 Standard in JEDEC's files.

7. The following statements on the public availability of the JESD82-20 Standard and the JESD205 Standard as of March 2007 are based on personal knowledge. The development of all JEDEC documents follows the process set forth in JM21: JEDEC Manual of Organization and Procedure. According to that process, the date on the cover of a JEDEC document is the month the document was finalized, approved by legal, and posted to the website. For both the JESD82-20 Standard and the JESD205 Standard, the date on the cover (and thus the date it was posted to JEDEC's website) is March 2007.

8. I am familiar with the circulation and publication procedures used by JEDEC. Upon approval of the Board of Directors, the JEDEC publications department prepares documents for publication, and seeks final review and approval to publish from the JEDEC legal department. Once legal approval is received, the JEDEC publications department uploads the approved document to the JEDEC website with a brief description. An email announcement is then sent to the sponsoring committee and any approved resellers. By 2000, JEDEC made its published standards available for download from www.jedec.org, as mentioned above.

9. Based on my personal knowledge of JEDEC's policies, both the JESD82-20 Standard and the JESD205 Standard were made publicly available in March 2007 for download from the JEDEC website (https://www.jedec.org), consistent with the dates on the cover pages of the JESD82-20 Standard and the JESD205 Standard. My knowledge of the procedures surrounding the creation of the date notation and publication is based on JEDEC's policies and practices as I understand them through my work at JEDEC. I rely on these policies and practices in the course of my work. I have no reason to believe that JEDEC's typical practice was not followed. I have no reason to believe that the JESD82-20 Standard and the JESD205 Standard were not made publicly accessible in March 2007.

10. To further confirm my statements above, I have visited the Internet Archive to look at the first capture of the online catalog at www.jedec.org after March 2007 that contained both the JESD82-20 Standard and the JESD205 Standard, which occurred on October 21, 2007: <http://web.archive.org/web/20071021053839/http://www.jedec.org:80/Catalog/display.cfm>. A printout of this capture is attached as Exhibit C and is consistent with my personal recollection of the JEDEC website. As can be seen from this capture on October 21, 2007, the JESD82-20 Standard was cataloged as "JESD 82-20," indexed under the "CMOS Digital Logic" technical subject matter and under

the keywords “Advanced Memory Buffer,” “AMB,” “AMB Component Specification,” “DDR2,” “FB-DIMM,” “FBD,” and “FBDIMM,” and was available to the public by that date, consistent with my statements above. *See* Exhibit C at pages 41, 91, 95, 103, 107, 108. As can also be seen from this capture on October 21, 2007, the JESD205 Standard was cataloged as “JESD 205,” indexed under the “Fully Buffered DIMM’s” technical subject matter and under the keywords “Advanced Memory Buffer,” “AMB,” “FB-DIMM,” “FBD,” “FBDIMM,” and “Fully Buffered DIMM,” and was available to the public by that date, consistent with my statements above. *See* Exhibit C at pages 50, 94, 95, 107, 110.

11. Exhibit D is a printout of <http://web.archive.org/web/20070401184420/http://www.jedec.org:80/service_members/New_Members/memberco.cfm>, which is a capture on April 1, 2007, of the list of member companies on JEDEC’s website as of that date, which is consistent with my personal recollection of JEDEC’s membership. All of those member companies would have had access to both the JESD82-20 Standard and the JESD205 Standard attached as Exhibits A and B, respectively, no later than that date.

I, Julie Carlson, do hereby declare and state, that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, under Section 1001 of Title 18 of the United States Code.

Executed on 3/25/2022 Julie D. Carlson

Julie D. Carlson

Exhibit A

JEDEC STANDARD

FBDIMM:
Advanced Memory Buffer (AMB)

JESD82-20

SPECIAL DISCLAIMER: JEDEC has received information that certain patents or patent applications may be relevant to this standard, and, as of the publication date of this standard, no statements regarding an assurance or refusal to license such patents or patent applications have been provided.

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MARCH 2007

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§

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FBDIMM: Advanced Memory Buffer (AMB)

(From JEDEC Board ballot JCB-06-42, formulated under the cognizance of the JC-40 Committee on Digital Logic.)

1 Introduction

This document is a core specification for a Fully Buffered DIMM (FBD) memory system. This document, along with the other core specifications, must be treated as a whole. Information critical to a Advanced Memory Buffer design appears in the other specifications, with specific cross-references provided.

1.1 Advanced Memory Buffer Overview

The Advanced Memory Buffer (AMB) reference design complies with the *FB-DIMM Architecture and Protocol Specification* . It supports DDR2 SDRAM main memory. The Advanced Memory Buffer allows buffering of memory traffic to support large memory capacities. All memory control for the DRAM resides in the host, including memory request initiation, timing, refresh, scrubbing, sparing, configuration access, and power management. The Advanced Memory Buffer interface is responsible for handling FBD channel and memory requests to and from the local DIMM and for forwarding requests to other DIMMs on the FBD channel.

Fully Buffered DIMM (FBD) provides a high memory bandwidth, large capacity channel solution that has a narrow host interface. Fully Buffered DIMMs use commodity DRAMs isolated from the channel behind a buffer on the DIMM. The memory capacity is 288 devices per channel and total memory capacity scales with DRAM bit density. The Advanced Memory Buffer is the buffer that isolates the DRAMs from the channel.

1.2 Advanced Memory Buffer Functionality

1.2.1 Advanced Memory Buffer

The Advanced Memory Buffer will perform the following FBD channel functions:

- Supports channel initialization procedures as defined in the initialization chapter of the *FB-DIMM Architecture and Protocol Specification* to align the clocks and the frame boundaries, verify channel connectivity, and identify AMB DIMM position.
- Supports the forwarding of southbound and northbound frames, servicing requests directed to a specific AMB or DIMM, as defined in the protocol chapter, and merging the return data into the northbound frames.
- If the AMB resides on the last DIMM in the channel, the AMB initializes northbound frames.
- Detects errors on the channel and reports them to the host memory controller.
- Support the FBD configuration register set as defined in the register chapters.
- Acts as DRAM memory buffer for all read, write, and configuration accesses addressed to the DIMM.
- Provides a read buffer FIFO and a write buffer FIFO.
- Supports an SMBus protocol interface for access to the AMB configuration registers.
- Provides logic to support MEMBIST and IBIST Design for Test functions.
- Provides a register interface for the thermal sensor and status indicator.
- Functions as a repeater to extend the maximum length of FBD Links.

1.2.2 Transparent Mode for DRAM Test Support

In this mode, the Advanced Memory Buffer will provide lower speed tester access to DRAM pins through the FBD I/O pins. This allows the tester to send an arbitrary test pattern to the DRAMs. Transparent mode only supports a maximum DRAM frequency equivalent to DDR2 400.

Transparent mode functionality:

- Reconfigures FBD inputs from differential high speed link receivers to two single ended lower speed receivers (~200 MHz)
- These inputs directly control DDR2 Command/Address and input data that is replicated to all DRAMs
- Uses low speed direct drive FBD outputs to bypass high speed Parallel/Serial circuitry and provide test results back to tester

1.2.3 Debug and Logic Analyzer Interface

When optional LAI functionality is supported, the Advanced Memory Buffer can be used to support the connection of FBD links to a Logic Analyzer (LA) for debug.

Advanced Memory Buffer debug functionality:

- Reconfigures DDR2 interface to act as a Logic Analyzer Interface (LAI) to observe activity on FBD high speed links
- Triggers on programmable events in normal operation

1.2.4 DDR SDRAM

DDR2 SDRAM support:

- Supports DDR2 at speeds of 533, 667 and 800 MT/s
- Supports 256, 512, 1024, 2048 and 4096 Mb devices in x4 and x8 configurations
- 288 devices/channel (8 DIMMs/channel, 1 and 2 ranks/DIMM)
- 72-bit DDR2 SDRAM unregistered, unbuffered memory interface

1.3 Advanced Memory Buffer Block Diagram

Figure 1.1 is a conceptual block diagram of the Advanced Memory Buffer’s data flow and clock domains.

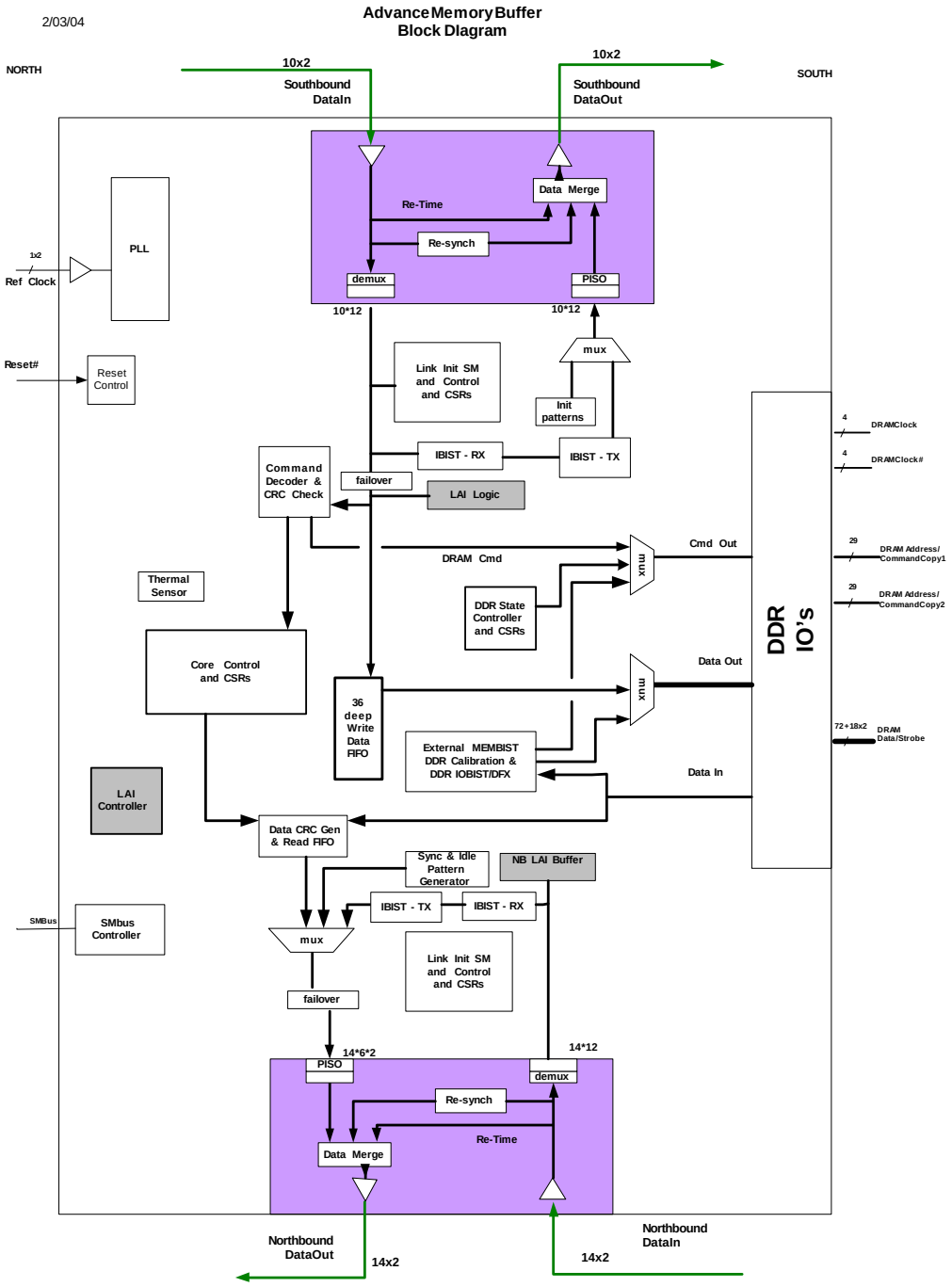


Figure 1.1 — Advanced Memory Buffer Block Diagram

1.4 Interfaces

Figure 1.2 illustrates the Advanced Memory Buffer and all of its interfaces. They consist of two FBD links, one DDR2 channel and an SMBus interface. Each FBD link connects the Advanced Memory Buffer to a host memory controller or an adjacent FBD. The DDR2 channel supports direct connection to the DDR2 SDRAMs on a Fully Buffered DIMM.

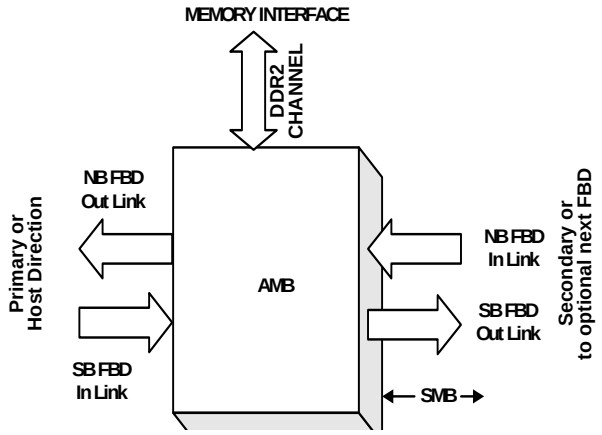


Figure 1.2 — Advanced Memory Buffer Interfaces

1.4.1 FBD High-Speed Differential Point-to-Point Link (at 1.5 V) Interfaces

The Advanced Memory Buffer supports one FBD Channel consisting of two bidirectional link interfaces using high-speed differential point-to-point electrical signaling.

The southbound input link is 10 lanes wide and carries commands and write data from the host memory controller or the adjacent DIMM in the host direction. The southbound output link forwards this same data to the next FBD.

The northbound input link is 13 to 14 lanes wide and carries read return data or status information from the next FB DIMM in the chain back towards the host. The northbound output link forwards this information back towards the host and multiplexes in any read return data or status information that is generated internally.

1.4.2 DDR2 Channel

The DDR2 channel on the Advanced Memory Buffer supports direct connection to DDR2 SDRAMs. The DDR2 channel supports two ranks of eight banks with 16 row/column request, 64 data signals, and eight check-bit signals. There are two copies of address and command signals to support DIMM routing and electrical requirements. Four-transfer bursts are driven on the data and check-bit lines at 800 MHz.

Propagation delays between read data/check-bit strobe lanes on a given channel can differ. Each strobe can be calibrated by hardware state machines using write/read trial and error (or equivalent implementation). Hardware aligns the read data and check-bits to a single core clock.

The Advanced Memory Buffer provides four copies of the command clock phase references (CLK[3:0]) and write data/check-bit strobes (DQSs) for each DRAM nibble.

1.4.3 SMBus Slave Interface

The Advanced Memory Buffer supports an SMBus interface to allow system access to configuration registers independent of the FBD link. The Advanced Memory Buffer will never be a master on the SMBus, only a slave. Serial SMBus data transfer is supported at 100 kHz.

SMBus access to the Advanced Memory Buffer may be a requirement to boot a system. This provides a mechanism to set link strength, frequency and other parameters needed to insure robust operation given platform specific configurations. It is also required for diagnostic support when the link is down.

The SMBus address straps located on the DIMM connector are used by the Advanced Memory Buffer to get its unique ID.

More information is available in the SMBus chapter of this document.

1.5 References

This revision of the *Advanced Memory Buffer Component Specification* is consistent with the following documents:

- *FB DIMM Architecture and Protocol Specification,* [1]
- *FBD Design for Test, Design for Validation (DFx) Specification,* [2]
- *FB4300/5300/6400 DDR2 Fully Buffered DIMM Design Specification,* [3]
- *JEDEC DDR2 SDRAM Specification,* JC 42.3 [4]
- *High Speed Differential Point-to-Point Link at 1.5 V for Fully Buffered DIMM,* [5]
- *System Management Bus (SMBus) Specification Version 2.0 as published by www.smbus.org* [6]
- *Advanced Configuration and Power Interface Specification Version 2.0c as published by www.acpi.info* [7]

1.6 Glossary

Term	Definition
AMB	Advanced Memory Buffer
Chip disable	An ECC encoding specifically tailored for memory such that the data from any defective memory device can be reconstructed from some aggregate of surviving memory devices. Corrects data from failed device. The AMB employs an “x8” ECC, which means that all data from a partially or completely failed 8-bit device can be recovered without stopping the system. This same ECC provides the same level of coverage for 4-bit (“x4”) devices.
DDR	Double Data Rate (SDRAM)
DDR Branch	The minimum aggregation of DDR channels which operate in lock-step to support error correction. Two channels per branch supports x8 chip disable ECC. A rank spans a branch.
DDR Channel	A DDR channel consists of a data channel with 72 bits of data and an ADDR/CNTRL channel
DDR Data channel	A DDR data channel consists of 72 bits of data, divided into 18 data groups
DDR Data group	Each data group consists of 4 data signals and a differential strobe pair

Term	Definition
DIMM	Dual In-Line Memory Module. A packaging arrangement of memory devices on a socketable substrate.
DIMM Slot	Receptacle (socket) for a DIMM. Also, the relative physical location of a specific DIMM on a DDR channel.
DIMM Stack	Dual-ranked x4 DRAM DIMM physical topology: refers to two physical rows of DRAM “stacked” one above another
DRAM Page (Row)	The DRAM cells selected by the Row Address
DPM	Defects per million
DRAM	Dynamic Random Access Memory
ECC	Error Correction Code. For the AMB, this is a chip disable code.
EMI	Electromagnetic interference
FBD Channel	Combination of 10 lane Southbound Links and 13 or 14 lane Northbound Links that make up a logical memory channel from host perspective
FBDIMM	Fully-Buffered DIMM
Frame	Group of bits containing commands or data
HCSL	High-speed Current Steering Logic
Host	Memory controller agent on an FBD channel
ISI	Inter Symbol Interference – see section “Initialization / Clocking” for definition
Mesochronous	Small ppm frequency difference.
NB	Nouth Bound
NBI	Nouth Bound Interface control logic
Northbound	The direction of signals running from the furthest DIMM toward the host.
JEDEC	JEDEC Solid State Technology Association (once known as the Joint Electron Device Engineering Council)
JESD79	JEDEC Standard 79, *DDR SDRAM Specification*
LA	Logic Analyzer
LAI	Logic Analyzer Interface
Lane	Differential pair of receivers or transmitters
Link	High speed parallel Differential Point-to-Point interface
Page Replace aka Page Miss, Row Hit / Page Miss	An access to a row that has another page open. The page must be transferred back from the sense amps to the array, and the bank must be precharged.
Page Hit	An access to an open page, or DRAM row. The data can be supplied from the sense amps at low latency.
Page Miss (Empty Page)	An access to a page that is not buffered in sense amps and must be fetched from DRAM array.
Plesiochronous	Having the same frequency but arbitrary phase differences.

Term	Definition
Primary	In the direction towards the Host controller
PLL	Phase Locked Loop
PTH	Plated Through-Hole
PVT	Process, Voltage and Temperature
Rank	A DIMM is organized as one or two physical sets of memory, called ranks. Note that single rank or dual rank is different from single-sided or double-sided, e.g. a single rank DIMM build from x4 DRAM devices is actually double-sided. It is also common practice to distribute the 9 devices of an x8 DIMM between both sides of the DIMM to enhance the thermal performance of the module. The standard 4-slot DDR2 topology is limited to single rank DIMM due to loading constraints.
RAS	Reliability, Availability, Serviceability
Resample	A resampler is a serial data in and serial data out node that attenuates jitter by regenerating the serial data using a clock recovered from the incoming data stream derived from a common reference clock. It also resets the voltage budget of the retransmitted data.
Resync	A resync repeater is a serial data in and serial data out node that resynchronizes data to a local clock after it has been sampled with a recovered clock derived from a common reference clock. The local clock is also generated from the same reference clock by a PLL multiplier. A drift compensation buffer is inserted between the two clock domains which absorbs the maximum link delay change over worst case voltage and temperature changes only, and not for compensating lane-to-lane skew. Both the jitter and voltage budgets for the retransmitted data are reset.
RPD	Return Path Discontinuity
SDRAM	Synchronous Dynamic Random Access Memory
SB	South Bound
SBI	South Bound Interface control logic
SI	Signal Integrity
Secondary	In the direction away from the Host controller
Serial Present Detect (aka SMBus protocol	A 2-signal serial bus used to read and write control registers in the AMB and SDRAM
SMBus	System Management Bus. Mastered by a system management controller to read and write configuration registers. Limited to 100 kHz.
Southbound	The direction of signals running from the host controller toward the DIMMs.
SSC	Spread Spectrum Clocking. Utilized to lower EMI
SSO	Simultaneously Switching Outputs
SSTL_18	Series Stub Terminated Logic for 1.8V
NB	North Bound
NBI	North Bound Interface control logic

Term	Definition
Throttled	Temporarily prohibiting memory accesses when a thermal or electrical limit has been reached.
Transparent Mode	High speed FBD linked I/Os are bypassed with lower speed CMOS I/Os to allow lower speed tester to control and test DRAMs on the DIMM.
Unit Interval	Average time interval between voltage transitions of a signal
V_{SS}	Ground (0V)
V_{DDQ}	I/O buffer voltage for DDR2 buffers. Nominally 1.8V

2 FBD Channel Interface

2.1 Advanced Memory Buffer Support for FBD Operating Modes

The Advanced Memory Buffer (AMB) may not support all operating modes documented in the *FB-DIMM Architecture and Protocol Specification* [1]. The following list defines which features/modes are supported:

- 14 lane northbound (NB) with and without single lane Fail Over
- 13 lane NB with and without single lane Fail Over
- 10 lane southbound (SB) with and without single lane Fail Over
- Repeater mode
- Transparent mode
- Recalibrate state
- Voltage Margin Test

The following are optional FBD features :

- LAI mode
- 12 lane NB non-ECC
- L0s low power state
- Data mask
- Variable read latency
- Timing Margin Test

2.2 Channel Initialization

Refer to Chapter 3, “Channel Initialization” in the *FB DIMM Architecture and Protocol Specification* [1] for FBD initialization protocol. The reset chapter covers some additional details about the initialization process.

2.3 Channel Protocol

2.3.1 General

Refer to Chapter 4, “Channel Protocol” in the *FB DIMM Architecture and Protocol Specification* [1] for FBD protocol.

2.3.2 Timeouts during TS0

The FBDLOCKTO register is used to help the AMB determine when to give up waiting for individual lanes to bit lock. The NBLINKCFG field is used to communicate when lanes are intentionlly not in use. The BLTOCNT field is used to set a time out on waiting for a lane to bit lock. Lanes not bit locked by this time will be marked as failed.

2.3.3 Recalibrate state considerations

In addition to what the FBD Architecture and Protocol specification describes around Recalibrate State, the AMB further requires that the host be sending NOP commands in at least the 2 frames preceding the exit from recalibrate state.

Requirement: 2 Cycles before the recalibrate counter expires, NOPs must be sent from the host.

Time	Frame Description	Recal Frame Counter
N	Sync with ERC bit set	0
N+1	NOP frame	RECALDUR
N+2	NOP frame	RECALDUR - 1
...	NOP frame	....
N+8	NOP frame	RECALDUR - 7
N+9	NOP frame - host may begin recalibration	RECALDUR - 8
...	.....	....
N + RECALDUR - 7	NOP frame - host must be finished with recalibration	8
...	.....	....
N + RECALDUR - 3	NOP frame	4
N + RECALDUR - 2	NOP frame	3
N + RECALDUR - 1	NOP frame - must be received at AMB without corruption	2
N + RECALDUR	NOP frame - must be received at AMB without corruption	1
0	Valid Sync Frame	0

Recal Frame Counter:	5	4	3	2	1	0
Rx Data:	X	X	X	NOP	NOP	Valid Cmd
where X represents “don’t care” data						

2.3.4 Address Mapping of DDR Commands to DRAMs

DDR2 x4 Config		20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
256Mb (64Mbx4)	Row	1	X	X	RS	X	X	B1	B0	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
1KB page	Col	0	1	r/w	RS	X	X	B1	B0	X	A11	AP	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
512Mb (128Mbx4)	Row	1	X	X	RS	A13	X	B1	B0	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
1KB page	Col	0	1	r/w	RS	X	X	B1	B0	X	A11	AP	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
1Gb (256Mbx4)	Row	1	X	X	RS	A13	B2	B1	B0	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
1KB page	Col	0	1	r/w	RS	X	B2	B1	B0	X	A11	AP	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
2Gb (512Mbx4)	Row	1	X	A14	RS	A13	B2	B1	B0	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
1KB page	Col	0	1	r/w	RS	X	B2	B1	B0	X	A11	AP	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
4Gb (1Gbx4) *	Row	1	A15	A14	RS	A13	B2	B1	B0	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
1KB page	Col	0	1	r/w	RS	X	B2	B1	B0	X	A11	AP	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
4Gb (1Gbx4) *	Row	1	X	A14	RS	A13	B2	B1	B0	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
2KB page	Col	0	1	r/w	RS	X	B2	B1	B0	A12	A11	AP	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0

DDR2 x8 Config		20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
256Mb (32Mbx8)	Row	1	X	X	RS	X	X	B1	B0	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
1KB page	Col	0	1	r/w	RS	X	X	B1	B0	X	X	AP	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
512Mb (64Mbx8)	Row	1	X	X	RS	A13	X	B1	B0	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
1KB page	Col	0	1	r/w	RS	X	X	B1	B0	X	X	AP	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
1Gb (128Mbx8)	Row	1	X	X	RS	A13	B2	B1	B0	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
1KB page	Col	0	1	r/w	RS	X	B2	B1	B0	X	X	AP	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
2Gb (256Mbx8)	Row	1	X	A14	RS	A13	B2	B1	B0	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
1KB page	Col	0	1	r/w	RS	X	B2	B1	B0	X	X	AP	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
4Gb (512Mbx8) *	Row	1	A15	A14	RS	A13	B2	B1	B0	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
1KB page	Col	0	1	r/w	RS	X	B2	B1	B0	X	X	AP	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
4Gb (512Mbx8) *	Row	1	X	A14	RS	A13	B2	B1	B0	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
2KB page	Col	0	1	r/w	RS	X	B2	B1	B0	X	A11	AP	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0

2.3.5 FBD L0s State

The L0s state provides a low latency power down state for the FBD channel. The L0s state will nominally last for 41 frame times such that no sync packets are missed. The actual amount of time is programmable in the AMB. Times greater than 41 frames are not supported at this time. The L0s state may be used when the memory controller is throttling, and producing no transfers.

The duration of the L0s state is pre-programmed into the MC and AMB registers, and is triggered by a sync command with the L0s command indicated. The basic sequence is:

L0 to L0s Transition

- MC issues L0s command in the SYNC command.
- The MC continues sending one additional command, which is a NOP.
- AMB must gate its inputs and stop accepting commands following the NOP. It need not accept and decode the NOP itself.
- Southbound output drivers and input receivers are disabled following the NOP. The turnoff may be staggered for power supply di/dt reduction.
- Northbound channels are shut down following the status packet corresponding to the sync command.
- AMB takes CKE low to all DRAMs and floats the commands and address bus to the DRAMS (all signals except clock, CKE, and ODT).
- The PLL is never powered down before, during, or after the transition.

L0s to L0 Transition

- When the timer expires, interface must be fully functional and ready to receive the sync command. The turning on of circuits occurs the proper amount of time prior to the timer expiring, and is an implementation detail of the AMB.
- Southbound channel begins power-up. The drivers must begin driving a valid state one clock prior to the NOP below.
- The AMB drives command and address lines, and restores CKEs to their previous state with appropriate timing to be able to process a DRAM command which is received on the clock following the sync command.
- MC sends a NOP on the clock prior to the timer expiring. The receiver need not accept and decode the NOP itself.
- MC sends a sync command on the clock that the timer expires.
- Normal commands may commence.
- Northbound lanes are brought back in a similar manner to southbound lanes, but are timed to be able to successfully send the status packet response for the sync command.

Note: DRAM pages need not be closed during the power down, but any DRAM with open pages will consume additional power. This is solely a function of the MC policy.

Note: Upon return to L0, the MC may place the bus back into L0s by issuing another L0s command in the sync command.

2.4 Reliability, Availability, and Serviceability

2.4.1 General

Refer to Chapter 5, “Reliability, Availability and Serviceability” in the *FB DIMM Architecture and Protocol Specification* [1] for FBD RAS requirements.

2.4.2 Channel Error Detection and Logging

See “Errors” chapter for details on the error handling.

2.5 Channel Configuration

2.5.1 Re-sync and Resample Modes

A separate control is available for both the NB and SB FBD links to select between lower latency re-sample and lower jitter re-sync modes for repeating received data. Selection between these two modes is a function of platform design and configuration and should be set by BIOS prior to link initialization

The FBDSBCFGNXT.SBRESYNCEN and FBDNBCFGNXT.NBRESYNCEN bits make this selection.

Descriptions of these two modes follows.

2.5.1.1 Accumulated Tracking Effects (Re-Sample Mode)

Each AMB acts as a repeater for the FBD channel. Since the data driven from each DIMM to the next DIMM may experience random or periodic phase shifts, the affect of these phase shifts must be accommodated in the design. Consider a system with three DIMMs daisy-chained together. A phase shift generated in the first DIMM will be seen by the second DIMM but will not be immediately propagated to the third DIMM. Unlike an analog buffer, the phase shift is not automatically driven to subsequent DIMMs since the data driven to the subsequent DIMMs is re-sampled in the AMB to reduce jitter. The lowest latency implementation would use the derived clock to retransmit the outbound signal. The second DIMM will see the phase shift as a slight change in the position of the data eye at its receiver. The clock tracking loop filter in the second DIMM will measure several bit cells and may eventually

determine that it should adjust the phase of its derived clock to capture the data closer to the center of the new data eye location. Only when the second DIMM makes its phase change will the effect propagate to the third DIMM. More detail of the data sampling technique may be found in the “High Speed Differential Point-to-Point Link at 1.5V for Fully Buffered DIMM Specification”.

2.5.1.2 Accumulated Tracking Effects (Re-Sync Mode)

An alternative implementation would place a voltage/thermal (VT) drift compensation buffer between the receiver and the transmitter section of the AMB IO cell. The drift compensation buffer would re-synchronize the signal with a multiple of the reference clock. This buffer would have to be deep enough to handle the absolute magnitude of delay change of the daisy-chain channel over voltage and temperature. More detail of the data sampling technique may be found in the “High Speed Differential Point-to-Point Link at 1.5V for Fully Buffered DIMM Specification”.

2.5.2 Other Channel Configuration Modes

Other channel electrical configuration parameters that should be set up prior to link initialization include

- Link frequency (LINKPARNXT.CFREQ)
- SB Transmitter drive current (FBDSBCFGNXT.SBTXDRVCUR)
- SB Transmitter de-emphasis values (FBDSBCFGNXT.SBTXPREEMP)
- NB Transmitter drive current (FBDNBCFGNXT.NBTXDRVCUR)
- NB Transmitter de-emphasis values (FBDNBCFGNXT.NBTXPREEMP)

The parameters contained in these registers are described more completely in the “High Speed Differential Point-to-Point Link at 1.5V for Fully Buffered DIMM Specification”.

Additional channel configuration registers that should be set up prior to link initialization include
- First 6 bytes of the SPD parameter registers

  PERSBYTE[5:0]
- FBD Bit Lock Time Out Register (FBDLOCKTO)

2.5.3 Lane to Lane Skew on a Channel

The FBD Channel is expected to support a maximum skew of upto 46UI. The deskew buffers on an individual AMB need to be able to support this amount of accumulated skew. The actual skew observed will be a function of the skew introduced by platform layout, DIMM layout, the number of active AMBs in the channel and skew introduced by AMBs.

2.6 Repeater Mode

The AMB may also be used as an FBD link repeater to extend distances at which links can operate. This mode can be automatically set by the BFUNC and SA pins. In this mode, the AMB functions in the same way as a regular DIM with the exception that DRAM commands are not supported.

Link behavior is the same as for normal DIMMs
- Participates in link initialization like a normal DIMM
- Responds to Reads and Writes to AMB configuration registers,
- status is returned in response to Sync commands,
- link errors are detected and alerts generated,

SMBus access is the same except for the base Slave address is different than from normal DIMM.

Slave address[6:3] = 4’b0011 for Repeaters, instead of

Slave address[6:3] == 4’b1011 for normal DIMMs

2.7 Performance

This section describes the performance characteristics of FBD: idle memory read latencies, loaded memory read latencies, channel throughput, and system memory capacity.

2.7.1 Idle Memory Read Latency

Memory read latency is an important factor in system level performance. Processor and I/O devices are often blocked from doing other work when reading from memory, until their read requests are satisfied. Therefore, minimizing the amount of time that it takes to satisfy a read request can increase the amount of work that a processor or I/O device can perform. This can improve overall system or benchmark performance.

Memory read latency (also referred as loaded memory read latency) consists of two components: idle memory read latency and queuing delays for various resources such as the front-side bus, memory controller queues, etc. Idle memory read latency is the latency of only one transaction running in the entire system, and is the least amount of latency that is possible for a read transaction. The following sections describe how to measure the FBD channel latency, as well as the overall system latency.

2.7.1.1 FBD Channel Latency

FBD channel latency is measured from the time a read request is driven on the FBD channel pins to the time when the first 16 bytes (2nd chunk) of read completion data is sampled by the memory controller.

When not using the Variable Read Latency capability, the latency for a specific FBD DIMM on an FBD channel is always equal to the latency for any other FBD DIMM on that channel. However, the latency for each FBD DIMM in a specific configuration with some number of FBD DIMMs installed may not be equal to the latency for each FBD DIMM in a configuration with some different number of FBD DIMMs installed.

As more DIMMs are added to the FBD channel, additional latency is required to read from each DIMM on the channel. Because the FBD channel is based on the point-to-point interconnection of buffer components between DIMMs, memory requests are required to travel through N-1 buffers before reaching the Nth buffer. The result is that a 4 DIMM channel configuration will have greater idle read latency compared to a 1 DIMM channel configuration.

The Variable Read Latency capability can be used to reduce latency for DIMMs closer to the host.

The idle latencies listed in this section are representative of what might be achieved in typical AMB designs. Actual implementations with latencies less than the values listed will have higher application performance and vice versa.

The following table shows typical idle read latency, using DDR2 667 (4-4-4) DRAM technology (for a page empty read). Actual values depend on platform board and DIMM routing, AMB timing specs, DRAM characteristics, etc.

Table 2.1 — Example FBD-667 Channel Idle Memory Read Latencies

DIMMs per Channel	Typical Latencies
1	43-47 ns
2	49-53 ns
3	52-56 ns
4	58-62 ns

Table assumptions:

- Measure from latest valid SB output pin at host to latest valid NB input pin at host
- Includes 4UI serialization delay SB (A slot command) and 12 UI serialization delay NB
- Routing delay of 850ps from host to first DIMM and 600ps DIMM to DIMM
- 4-4-4 SDRAM Access Timing (24ns) plus 400ps Tdqsck
- On-DIMM Clk and DQS propagation delays of 800ps
- FBD SB Cmd In to DDR Clk out that Latches Cmd Out of 8.1ns +/- 1ns
- DDR Read Data In to FBD NB Out (last DIMM) of 5ns +/- 1ns
- Resample cross AMB delays of 1.25ns and Resync pass thru delays of 2.25ns
- First AMB in Resync and other AMBs in Resample mode

2.8 AMB Components of Channel Latency

The critical elements that AMB contributes to the latency calculation are the chip crossing delays.

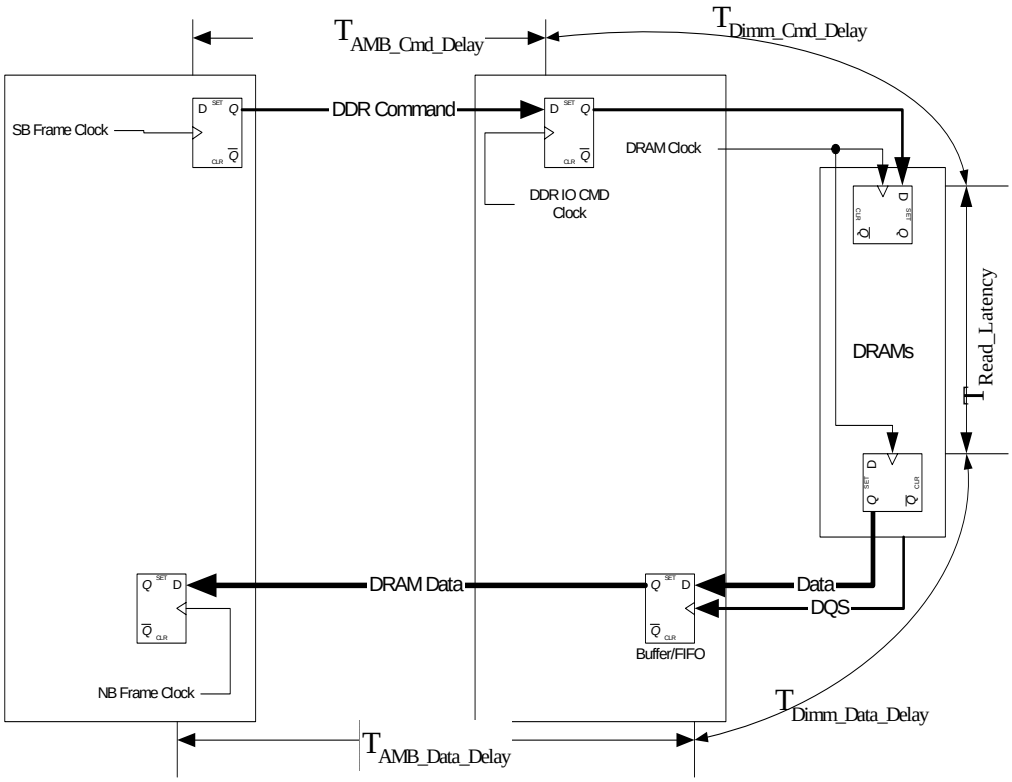
- Southbound latency contributions
  - — Delay from an input FBD link transaction to commands on the DDR interface and
  - — Pass-thru delay of forwarded Southbound FBD transactions.
- Northbound latency contributions
  - — Delay from DDR Read data input on the last DIMM to FBD link transactions and
  - — Pass-thru delay of forwarded Northbound FBD transactions back towards the host.

These timing delay values are documented in Chapter 4, “Electrical, Power, and Thermal.”

2.8.1 Command to Data Delay Calculation

Figure 2.1 shows the various components that make up the over all delay through an AMB for a memory command.

Figure 2.1 — Delays Through an AMB



The definition for terms used in Figure 2.1 are given below.

- UI: This is the unit interval on the FBD link. This is same as the period of the FBD link bit-rate clock.
- NB: Northbound
- SB: Southbound
- $T_{Read\_Latency}$: DRAM Parameter. $T_{CAS} + T_{Additive\_Latency}$
- $T_{AMB\_Cmd\_Delay}$: This value is very specific to an AMB implementation. This is the time it takes for the FBD command to be transferred from the point at which a deskewed and frame aligned command is available to core to the DDR IO Cluster. This includes any differences between the FBD frame clock and the DDR IO clock that latches the command into the DDR IO cluster. This can be different for different DRAM frequencies.
- $T_{AMB\_Data\_Delay}$: This value is very specific to an AMB implementation. This is the minimum time it takes for the data that is returned from the DRAMs to be transferred from the DDR IO cluster to the FBD IO for transmission on the link. This includes any buffering and clocking delays for the data within the chip. This can be different for different DRAM frequencies.
- $T_{Dimm\_Cmd\_Delay}$: This includes the delays for the command through the DDR IO cluster, differences between DDR IO CMD Clock and DRAM clock, any routing delays for the clock and command on the DIMM and any set-up and hold-times in the AMB and the DRAMs.
- $T_{Dimm\_Data\_Delay}$: This includes the routing delays for the data and strobes from the DRAM to the AMB, skews between the DRAMs, delays through the DDR IO cluster and any set-up and hold-times in the AMB and DRAMs.
- $T_{CMD\_To\_Data}$: This is equal to ($T_{Read\_Latency} + T_{AMB\_Cmd\_Delay} + T_{Dimm\_Cmd\_Delay} + T_{Dimm\_Data\_Delay} + T_{AMB\_Data\_Delay}$). This can be specified with 1UI granularity. This will be different for each DRAM type. It does not include any delays inside the IO to deskew and frame align the incoming data on the SB side nor does it include the delays inside the NB IO on the transmit side.

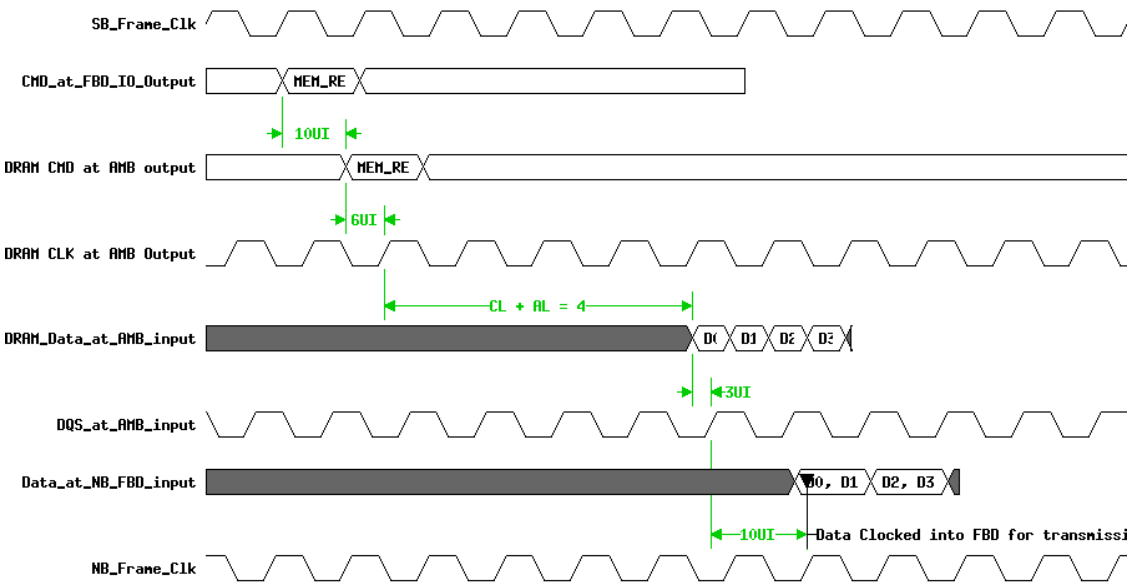
The TCAS and TAdditive_Latency are specified in the DRC register (DRC.cl and DRC.al). The AL and CL values are latched from the DRC register during TS2's to establish TRead_Latency . Later changes to AL and CL do not take effect for link data return timing until the next link reset.

The CMD2DATANXT register is initialized with a value equal to ($T_{CMD\_To\_Data}$ - $T_{Read\_Latency}$). This value of CMD2DATANXT is specified in the SPD EEPROM. All AMBs are expected to receive the data from the DRAMs with the calculated value of $T_{CMD\_To\_Data}$.

All AMBs power up with a default value of 5 for $T_{CMD\_To\_Data}$. This can be done either by setting the default values of DRC.CL and DRC.AL or by setting the default value of the CMD2DATACUR.FRMS to be 5. The AMBs must be able to return status and configuration register reads with this default timing. This will enable the BIOS to initialize the proper values from SPD.

The following simplified timing diagram illustrates how the last AMB uses the values specified in DRC.CL, DRC.AL, CMD2DATANXT.DLYFRMS and CMD2DATANXT.DLYFRAC.

Figure 2.2 — Command to Data Delay timing



In Figure 2.2, it is assumed that there are no routing delays on the DIMM itself. The command takes 10UI to get from SB FBD to the DDR IO ($T_{AMB\_Cmd\_Delay}$). This includes time it takes to validate CRC of the frame and to decode the command. It is assumed DDR_IO_Cmd_Clk shown in Figure 2.1 is delayed from the SB_Frame_Clk by 10 UI. The DRAM SCLK is placed at the center of the command window which adds an additional 6UI of delay. The DRAMs are programmed with a $T_{Read\_Latency}$ of 4. The DQS strobes are centered when they get to the AMB (3UI delay) and the data takes an additional 10 UI to propagate from the DDR IO to the NB FBD IO (including setup time at NB FBD and CRC generation) before it can be clocked into the NB FBD for transmission. The total delay without including the DRAM access time in this case is (10 + 6 + 3 + 10UI) 29UI. The CMD2DATANXT.DLYFRMS will be programmed with a value 2 and the CMD2DATANXT.DLYFRAC with 5UI. If the AMB supports only a 2UI granularity, then the values should be 2 frames and 6UI respectively. If an AMB does not support sub-frame delays, it is expected that the value in SPD will be round up the to the nearest frame. Any additional delays caused by rounding up should be supported by additional buffering in the DDR IO.

The above figure shows the last arriving data from the DDR. It is expected that any data arriving earlier than this, due to differences in routing, etc. is buffered up in some way inside the DDR IO. The expectation is that all AMBs (last and intermediate) unload the data from the DDR IO with the timing specified by the $T_{CMD\_To\_DATA}$. The Last AMB

is expected to be able send data on the NB links with no additional delay added, if C2DINCRCUR.INCRDLY is 0. Any additional delay needed due to the value programmed in C2DINCRCUR.INCRDLY register in the last AMB or to delay the data in intermediate AMB before the merge, is handled by FIFOs in the AMB core.

In the above figure, it is assumed that the AMB can place the clocks in position shown above. If this is not the case, then additional delays due to non-optimal placement of the clocks should be taken into account to calculate the total delay to be programmed into the SPD.

2.8.2 Channel Throughput

2.8.2.1 Peak Theoretical Throughput

An FBD channel transfers read completion data on the FBD Northbound data connection. 144 bits of data are transferred for every FBD Northbound data frame. This matches the 18-byte data transfer of an ECC DDR DRAM in a single DRAM command clock. A DRAM burst of 8 from a single channel or a DRAM burst of four from two lock-stepped channels provides a total of 72 bytes of data (64 bytes plus 8 bytes ECC).

The FBD frame rate matches the DRAM command clock because of the fixed 6:1 ratio of the FBD channel clock to the DRAM command clock. Therefore, the Northbound data connection will exhibit the same peak theoretical throughput as a single DRAM channel. For example, when using DDR2 533 DRAMs, the peak theoretical bandwidth of the Northbound data connection is 4.267 GB/sec.

Write data is transferred on the FBD Southbound command and data connection, via Command+Wdata frames. 72 bits of data are transferred for every FBD Command+Wdata frame. Two Command+Wdata frames match the 18-byte data transfer of an ECC DDR DRAM in a single DRAM command clock. A DRAM burst of 8 transfers from a single channel, or a burst of 4 from two lock-step channels provides a total of 72 bytes of data (64 bytes plus 8 bytes ECC).

When the FBD frame rate matches the DRAM command clock, the Southbound command and data connection will exhibit one half the peak theoretical throughput of a single DRAM channel. For example, when using DDR2 533 DRAMs, the peak theoretical bandwidth of the Southbound command and data connection is 2.133 GB/sec.

The total peak theoretical throughput for a single FBD channel is defined as the sum of the peak theoretical throughput of the Northbound data connection and the Southbound command and data connection. When the FBD frame rate matches the DRAM command clock, this is equal to 1.5 times the peak theoretical throughput of a single DRAM channel. For example, when using DDR2 533 DRAMs, the peak theoretical throughput of a DDR2 533 channel would be 4.267 GB/sec, while the peak theoretical throughput of an FBD-533 channel would be 6.4 GB/sec

3 DDR Interface

3.1 Advanced Memory Buffer DDR Interface Overview

The DDR interface on the Advanced Memory Buffer consists of:

- A command decoder.
- A FIFO write buffer to hold the write data before it is written to the DDR channel. The write FIFO buffer has 36 entries of 72 bits (36 x 72b). A maximum of 35 entries can be used to store DDR bursts. Write data targeted for other Advanced Memory Buffer parts on the channel will use three of the 35 entries until the target Advanced Memory Buffer is known. The write FIFO buffer fills at half of the DDR data rate, and empties at the DDR data rate. The write FIFO buffer must support an invalidate write FIFO command (FBD Soft Reset command).
- A FIFO read buffer to hold the read data so that each DIMM returns data with the same latency as the southernmost DIMM in the chain. Latency is measured in increments of core clock periods. The core clock runs at the DDR command clock rate (half the data rate frequency). The latency through the FIFO read buffer on the southernmost DIMM is expected to be zero.
- A DDR cluster which serves as a DIMM buffer by registering outbound commands and data at output flops. The cluster also captures and levelizes incoming read data.
- A reset FSM which puts the DIMM in self-refresh when reset is asserted, and exits self-refresh when reset is deasserted and southbound frame training is complete.
- A calibration FSM that automatically sets the timing for DQS receiver enable and DQS delay or equivalent DDR timing control mechanism.
- A configuration register set to allow software to issue DRAM power up and DRAM MRS/EMRS commands. These registers are accessible through FBD channel commands and the SMBUS interface.
- "Burst Write Interrupt" is not supported.

3.2 Data Mapping

See the protocol chapter of the *FB DIMM Architecture and Protocol Specification* for the mapping between data in DDR DRAM devices and data in FBD frame formats for 4-bit and 8-bit devices.

3.2.1 Data Mask

Data mask is supported for non-ECC (64-bit) DIMMs only. The AMB is required to support data mask if it supports non-ECC DIMMs.

Non-ECC DIMMs using x4 DRAMs are not supported by the standard AMB pinout, as there are not adequate data mask pins available. 16 data mask pins would be required for proper load matching.

The data mask signals share pins with the DQS[16:9] pins. This puts them in the proper place on the package and die to be matched with the timing of the appropriate DQ pins. DQS#[16:9] are not used in this mode. The following table shows the mapping between DQS pins and data mask pins.

Data Lane	Signal	x4 Usage	Non-ECC Usage	x8 or x16 ECC Usage
DQ[7:0]	DQS[9]/DM0	DQS[9]	DM0	Not used
DQ[15:8]	DQS[10]/DM1	DQS[10]	DM1	Not used
DQ[23:16]	DQS[11]/DM2	DQS[11]	DM2	Not used
DQ[31:17]	DQS[12]/DM3	DQS[12]	DM3	Not used
DQ[39:32]	DQS[13]/DM4	DQS[13]	DM4	Not used
DQ[47:40]	DQS[14]/DM5	DQS[14]	DM5	Not used
DQ[55:48]	DQS[15]/DM6	DQS[15]	DM6	Not used
DQ[63:56]	DQS[16]/DM7	DQS[16]	DM7	Not used
DQ[71:64]	DQS[17]	DQS[17]	Not used	Not used
As above	DQS[17:9]#	DQS[17:9]#	Not used	Not used

An AMB in non-ECC mode implies the following:

- 12 lane Northbound mode
- There is no Northbound fail-over mechanism.
- Data Mask Capability.
- Southbound write data frames use the Data Mask version of the frame format.
- 10 lane Southbound with fail-over capability.
- x4 DRAMs are not supported by the standard AMB pinout.

For AMB silicon that supports both ECC and non-ECC modes, there is no strapping signal to indicate which DIMM type it is installed on. The AMB will use the information in the configuration state, transferred from the host in the TS3 packet to determine ECC or non-ECC mode. If programmed for 12-bit northbound mode non-ECC mode is used. If programmed into 14-bit, 14-bit Fail Over, 13-bit, or 13-bit Fail Over modes, ECC mode is used. The host will determine the type of DIMM by reading the SPD.

3.3 Command / Address Outputs

The DDR2 command and address signals are terminated to 0.9V on the DIMM. In order to reduce power, this termination is performed using series resistors to a Vtt power supply, which is generated by voltage regulators on the system board and provided to the DIMM via connector pins. This power supply must be capable of sourcing and syncing current.

Two sets, or copies, of DRAM command and address output pins are provided for loading and timing considerations. Each set drives the same DRAM commands, but the two address busses are inverted from each other in order to reduce power consumption and heat produced on the DIMM. The command and address output pin behavior is detailed below:

1. Minimum address toggling. The address associated with the last command issued on the DRAM bus is retained during DRAM NOP/Deselect commands. The address and bank bits do not revert to all 1's (or all 0's) when the command bus is idle.
2. Balanced bank and address busses. With some exceptions, the bank and address busses on the two bus copies are inverted from each other. This minimizes the current load on the V_{TT} supply regulator because the balanced address bus sinks as much current as it sources. There are exceptions to the inversion behavior to allow for commands that use one or more address bits to control DRAM functionality. Balancing can also be disabled by setting the DRC.BALDIS register field.

Balancing Exceptions:

a. Address bit A10 is not balanced during all read, write, and precharge commands.

b. No address or bank bits are balanced during any MRS and EMRS commands.

c. Some MEMBIST operations that are pattern specific. Note that this will limit the number of DIMMs that may run MEMBIST simultaneously.

d. No address or bank bits are balanced during any command when the DRC.BALDIS register field is set.

3. Balanced idle command bus. When the command bus is idle, a deselect command is issued with all chip selects high and all RAS/CAS/WE signals driven low on both command/address copies.

4. Command/Address output control with CKE. All command and address pin outputs, except for ODT, CKE, and CLK, will float one DRAM clock cycle after both CKE pins transition from high to low. The command/address pins will be driven to valid signal levels on the same cycle that either CKE pin is driven from low to high.

5. Output control during link reset (i.e., fast reset). When the Advanced Memory Buffer core logic is in reset, CKE and ODT will be driven low, and CLK will run at normal levels and frequency. The remaining command/address pins will float during reset.

6. Command/Address output control in S3 mode. When the Advanced Memory Buffer core logic is in S3 power mode, all command/address outputs, including CKE, ODT, CLK, and all other command/address pins, will be driven low. In S3 mode, 1.8V supply is on. 1.5V, Vtt, and 3.3V are off. DRAMs are in self refresh, and the CKE signals must be driven low.

7. CSR output control of command/address. All command/address pin outputs will float when the appropriate DRC bits are set. Setting the DRC.CADIS field will float the RAS, CAS, WE, Bank, and Address pins. DRC.CSDIS controls the chip select pins. DRC.ODTDIS, DRC.CKEDIS, and DRC.CLKDIS float the ODT, CKE, and clock pins respectively.

3.3.1 CKE Output Control

During normal operation the CKE outputs can be controlled directly with dedicated FBD channel commands and with configuration register writes to the DRC.CKEN0/1 CSR's. Channel commands that affect the CKE outputs are reflected in the DRC.CKEN0/1 CSR's. During channel fast reset events the self-refresh FSM controls the CKE outputs, as well as all other command/address outputs.

3.3.2 Memory Controller / BIOS requirements

The memory controller must take care to not issue multiple MRS/EMRS commands to multiple DIMMs simultaneously in rapid succession if the Vtt supply cannot handle the current.

The memory controller may also be required to limit the number of DIMMs in MEMBIST mode at the same time. Vdd power supply and thermal limitations may also put a limit on how many DIMMs may be in MEMBIST at one time. These will be system dependent.

3.4 DQS IO and DM Outputs

Advanced Memory Buffer sends and receives source synchronous differential strobes (DQS) to transfer data (DQ/CB) during write and read DRAM transactions. DQS9 through DQS17 also support the data mask (DM) function in x8 mode. Setting the MTR.WIDTH configuration register enables x8 mode. When driving DM, the timing of the transition from floating, to driving, and back to floating is unchanged, but DQS[17:9] do not toggle and instead drive a constant level. DQSP[17:9] drive low and DQSN[17:9] drive high. In x8 mode DQS[17:9] are not used to capture read data. The table below lists which DQS signals are associated with which DQ/CB pins in x8 and x4 mode.

Table 3.1 — DQS association with DQ/CB pins in x8 and x4 mode.

DQS pin	x4 Mode: MTR.WIDTH=0		x8 Mode: MTR.WIDTH=1	
	Output Function	Input/Output Data Mapping	Output Function	Input/Output Data Mapping
DQS17	Write DQS	CB[7:4]	DM	N/A
DQS8	Write DQS	CB[3:0]	Write DQS	CB[7:0]
DQS16	Write DQS	DQ[63:60]	DM	N/A
DQS7	Write DQS	DQ[59:56]	Write DQS	DQ[63:56]
DQS15	Write DQS	DQ[55:52]	DM	N/A
DQS6	Write DQS	DQ[51:48]	Write DQS	DQ[55:48]
DQS14	Write DQS	DQ[47:44]	DM	N/A
DQS5	Write DQS	DQ[43:40]	Write DQS	DQ[47:40]
DQS13	Write DQS	DQ[39:36]	DM	N/A
DQS4	Write DQS	DQ[35:32]	Write DQS	DQ[39:32]
DQS12	Write DQS	DQ[31:28]	DM	N/A
DQS3	Write DQS	DQ[27:24]	Write DQS	DQ[31:24]
DQS11	Write DQS	DQ[23:20]	DM	N/A
DQS2	Write DQS	DQ[19:16]	Write DQS	DQ[23:16]
DQS10	Write DQS	DQ[15:12]	DM	N/A
DQS1	Write DQS	DQ[11:8]	Write DQS	DQ[15:8]
DQS9	Write DQS	DQ[7:4]	DM	N/A
DQS0	Write DQS	DQ[3:0]	Write DQS	DQ[7:0]

3.5 Refresh

3.5.1 Self-Refresh During Channel Reset

The Advanced Memory Buffer is required to manage DRAM refresh during channel resets and when refresh is enabled through the DAREFTC CSR. When a channel reset event is detected, the Advanced Memory Buffer will take the DRAM's from an unknown state and put them into self-refresh mode. The Advanced Memory Buffer does not track the DRAM state during normal operation, and so has a single process for getting from any DRAM state starting point to the self-refresh state.

When a reset event is detected, the Advanced Memory Buffer's self-refresh FSM will execute the following steps:

1. Clear the DAREFTC.AREFEN CSR to stop the Advanced Memory Buffer auto-refresh engine if enabled.
2. Block all DRAM commands, except those initiated by the self-refresh FSM.
3. Wait until any in-process read or write commands complete, with a minimum wait time of DSREFTC.TCKE, the DRAM "Minimum CKE pulse width time" specification. In-process reads/writes must complete to ensure that the DRAM ODT control outputs are driven low. The minimum time allows for the case where self-refresh entry or power-down entry was executed just before the channel reset.
4. Assert both CKE output pins by setting the DRC.CKE0/1 CSR fields. This will have no effect on the DRAM's if the CKE pins were already asserted.
5. Wait DSREFTC.TXSNR, the DRAM's "Exit self-refresh to a non-read command" specification, to allow any in process DRAM command to complete. This allows time to complete any command that may have been issued just before the channel reset event, such as an auto-refresh, as well as allows for self-refresh exit that may have been initiated when the self-refresh FSM asserted the CKE pins high.
6. Issue a "precharge all" command to both ranks. This guarantees that the DRAM's will be in an "idle" state.
7. Wait as required by DSREFTC.TRP, the DRAM "Precharge time."
8. Issue an auto-refresh command to both ranks. This meets the DRAM requirement that at least one auto-refresh command is issued between any self-refresh exit to self-refresh entry transition.
9. Wait as required by DAREFTC.TRFC, the DRAM "Refresh to active/refresh command time."
10. Issue a self-refresh entry command to both ranks.

When the channel comes out of "fast reset" (exiting the FBD link disable state), the Advanced Memory Buffer will automatically issue a self-refresh exit command to both ranks after the FBD Link Testing State is reached and the Advanced Memory Buffer core clock is stable. Note that this does not apply when the DISSREXIT bit is set as it should be when the Advanced Memory Buffer is powering up, when exiting S3 mode, or when exiting a channel reset that is a part of powering up or exiting S3 mode.

3.5.2 Automatic Refresh

The Advanced Memory Buffer has a refresh FSM for issuing auto-refresh commands to the DRAM's on regular intervals. This can be enabled when the DRAM bus is otherwise idle, but not during any other mode that generates DRAM commands, including DRAM power up and initialization, DDR I/O calibration, and normal operation where the FBD channel issues DRAM commands. The DAREFTC CSR controls the refresh interval and period.

3.6 Back to Back Turnaround Time

The host controller is required to observe a turnaround time on the DRAM data pins within a DIMM when switching between read and write cycles, and when switching from reads from one rank vs. the other rank on the DIMM. The nominal turnaround time is one clock for each parameter, which is the minimum time required to prevent a collision of the postamble of the first transaction and preamble of the second transaction. Additional clocks may be required by the DIMM, especially at higher speeds.

The three timing parameters are:

- Read to write turnaround time. The number of additional DRAM clocks in which the DRAM data bus must be idle between a read from either rank and a write cycle to either rank.
- Write to read turnaround time. The number of additional DRAM clocks in which the DRAM data bus must be idle between a write to one rank and a read from either rank. The write to read turnaround time to the same rank will generally dominated by the tWTR specification, which must also be observed.
- Read to read turnaround time. The number of additional DRAM clocks in which the DRAM data bus must be idle between a read from one rank and a read from the opposite rank.

These parameters are dependent on the AMB design and the DIMM PC board layout. The parameters are stored in the SPD. Each parameter is a 2 bit field allowing 0 to 3 additional clocks of turnaround time. See the *SPD Specification* for additional details.

Figure 1 shows the nominal turnaround times, with no additional clocks. Note that the DQS preamble and postamble may merge slightly when the first transaction is at worst case timings and the second transaction is at best case timings.

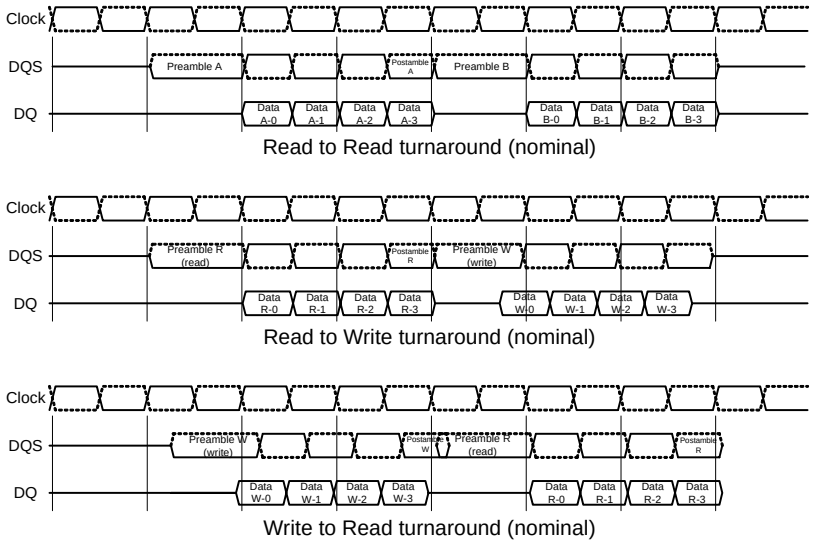


Figure 3.1 — Nominal Turnaround Time Timing Diagram

3.7 DDR Calibration

The following sections describe these DDR calibration and initialization features:

- DRAM initialization and (E)MRS command CSR's and FSM
- DQS failure CSR
- DQS receive enable calibration
- DQS delay calibration

3.7.1 DRAM Initialization and (E)MRS

The Advanced Memory Buffer provides a set of CSR's that allow BIOS to manage DRAM power up initialization and set DRAM mode register bits. All commands needed for DRAM initialization can be generated, including precharge, refresh, mode register set (MRS), and extended mode register set EMRS commands. The initialization/ (E)MRS FSM only controls the issuing of single commands, and does not automatically initialize the DRAM. It is the responsibility of software to control the command sequence to correctly initialize the DRAM.

The set of CSR's include the DCALCSR and DCALADDR registers. The fields of these CSR's are described in detail in the configuration register chapter.

The DCALCSR is used to select the command to be issued, which ranks to select, start the FSM that issues the command, and provide completion status.

The DCALADDR sets the bank and address issued to the DRAM, and therefore defines the type of (E)MRS to be issued, including limited OCD commands. DCALADDR[31:16] defines the DDR address bus during these commands, and DCALADDR[2:0] defines the ddr bank address bus.

3.7.1.1 OCD EMRS commands

FB DIMM DRAM timing is set up to work with OCD default calibration. Using the MRS/EMRS registers an EMRS OCD default is sent to the DRAMs. When the DCALCSR bit 31 is cleared to zero, an OCD exit command needs to be sent. When the DCALCSR bit 31 is cleared to zero the DRAMs should be in the default state.

Sending OCD EMRS drive(0), drive(1), adjust or exit OCD cal may have implementation dependent outcomes and should not be used in normal operation.

3.7.1.2 MRS Command Example

The following example shows how to send out an MRS command:

1. Write a value of 0x02320000 to the DCALADDR csr. This will configure the address/bank bus for an MRS command with burst length 4, CAS latency 3, and write recovery 2.
2. Write a value of 0x80000003 to the DCALCSR. This selects the (E)MRS command mode and initiates the FSM that will issue the command.
3. Poll the DCALCSR until bit 31 is cleared to zero by hardware. This indicates that the FSM has completed the selected operation.

3.7.2 Automatic DDR Bus Calibration

The Advanced Memory Buffer has two automatic DDR bus calibration functions that must be executed before read data can be captured reliably. These functions issue a series of write and read transactions on the DRAM bus, analyze the read data captured, and program a set of calibration results configuration registers. During subsequent operations, these configuration registers control the DDR IO circuits and ensure proper data capture. DIMM memory contents are not preserved during calibration. Calibration can take up to several ms to complete. The following steps run the calibration:

1. Program the DCALCSR to 0x8000000c. This selects and initiates the first of two calibrations.
2. Poll the DCALCSR until bit 31 is cleared to zero by hardware.
3. Program the DCALCSR to 0x80000005. This selects/initiates the second calibration.
4. Poll the DCALCSR until bit 31 is cleared to zero by hardware.

3.7.3 S3 Recovery Configuration Registers

The following CSRs should be stored in non-volatile memory before entering S3 mode and restored before normal DRAM transactions begin.

- DRC
- MTR
- DSREFTC
- DAREFTC
- S3RESTORE[15:0]
- SPDPAR[15:0] - SPD Personality Bytes

NOTE: Refer to "Advanced Configuration and Power Interface Specification Version 2.0c" as published by www.acpi.info for S3 mode definition.

3.7.4 Receive Enable Calibration

The DQS input receiver needs to be disabled when the DDR bus is floating (tri-stated), e.g. between the read and write data transfers. Otherwise, the floating strobe would cause spurious data to be written into the read data FIFO. Also, the DQS input receiver needs to be disabled during a write so that the write data strobes do not cause unwanted data or check-bits to be written into the read data FIFO.

During a read, the DRAM's initially drive the DQS signals low for a full cycle. This is the preamble. After the preamble, the DQS signals are toggled twice per cycle, for every cycle there is a data transfer, which is determined by the configured burst length and the number of back-to-back read commands that were issued to the selected rank. After the last DQS falling edge, the DQS signal is driven low for a half cycle. This is the post-amble. After the post-amble the DQS signals are tri-stated.

The Advanced Memory Buffer automatically finds the end of the preamble of each of the 18 DQS pairs on the DDR bus. That is, it finds the location of the first waveform transition that defines the end of the preamble of each DQS pair. Once this is complete, the Advanced Memory Buffer calculates the location of the center of the preambles, and stores this information for use during read transactions. Receiver calibration is initiated by setting the DCALCSR.START CSR. Hardware clears this bit when the calibration is complete. The calibration method modifies the data contents of the DIMM.

3.7.5 DQS Delay Calibration

The DQS Delay calibration adjusts the Advanced Memory Buffer's on-chip delay circuits that align DQS signals to the center of their associated DQ/CB data eyes at the capture flops in the DDR I/O cluster. This maximizes the DQ/CB setup and hold time at these flops, which capture source synchronous data from the DDR data bus.

DQS delay calibration is initiated by setting the DCALCSR.START CSR. Hardware clears this bit when the calibration is complete. The calibration method modifies the data contents of the DIMM. The calibration is accomplished by issuing a series of write and read transactions, and comparing expected to captured data.

3.8 DDR MEMBIST

The AMB supports memory self test for memory initialization during system boot up and for testing the installed memory. During DIMM manufacturing this mode may be used to apply tests at speed to test the AMB-DRAM interface. The table below describes the features of the MEMBIST engine.

At system level MEMBIST may be executed on multiple DIMMs simultaneously. This is expected to speed memory test during system boot.

During DIMM manufacturing, MEMBIST offers a fast method to detect assembly-related defects, interface defects and the majority of core-related defects during DIMM manufacturing. This testing may be initiated either in or out of band, making MEMBIST compatible with motherboards, low cost ATE, or standalone equipment such as continuity testers. During motherboard testing an FBD-enabled system will be required for in-band.

Transparent mode will be used for memory core testing while BIST will be more useful for DRAM interface testing. For this reason there is no plan to specify a comprehensive BIST capability. Traditional system test methods will be used for operating system or application-based testing of the memory subsystem. This may include existing memory stress tests, applications or other tests selected by the DIMM manufacturer.

3.8.1 MEMBIST Features

DATA Type

1. Fixed nibble data patterns (0, 3, 5, 6, 9, A, C, F)
2. 144-bit user defined data pattern and inverted user defined data pattern
3. 32-bit user defined circular shift data pattern
4. Random data generated from LFSR 32-bit CRC data

Those data patterns combined with addressing should be sufficient to test memory interface defect and DIMM assembly-related defect.

Address Type

1. Increased or decreased address type controlled by user
2. FastX, FastY, FastXY support
3. User defined test address range

DRAM Timing Parameter

1. BL4/BL8 support.
2. Various DDR2 DRAM timing support.
3. DRAM Refresh

Failure status:

1. Pass/Fail indicator, test abort, and halt on error features.
2. Up to five failure address recording.
3. Record one, and optionally up to 4, sets of 144 bits failure data.
4. 144 bit failure data location accumulator through entire test.

Table 3.2 — MEMBIST Feature Summary

Failure Status	Pass/Fail indicator
Address Pattern	
X address bits	15-16
Y address bits	15-16
Z address (bank) bits	3
Address pattern in tests	User defined init/end physical address scan with increased/ decreased FastX, FastY, FastXY support.
Failure Address logger	Up to 5 failure address loggers.
Data Patterns	
Fixed data pattern	fixed nibble data patterns (0, 3, 5, 6, 9, A, C, F)
User defined data pattern	144 bit data, defined in 5 MBDATA registers by user
LFSR	LFSR (CRC32),
Data Error logger	First 144 bit failure data logger
	144 bits lane failure data location
	Halt on error or run to completion of test
	Test abort during the test
DRAM Timing control	
Programmable Timings	
tCL, tRCD, tRP, tWR, tRC	various DDR2 DRAM timing support
BL	4 or 8
Refresh control	Capable of various DDR2 refresh intervals
BIST Engine	
Access method	all registers and settings could be accessed from FSB or SMBus
DRAM data width	x4 or x8
DRAM initialization and mode register settings	statically set by host
Pattern execution method	SMBus or Host
Failure data access	Failing data is available for read out by the host/SMBus at completion of test
Algorithms Support	

Table 3.2 — MEMBIST Feature Summary

Failure Status	Pass/Fail indicator
Notation: ^ = increasing addr from start to end v = decreasing addr R/W = Read/Write D/I = Data/ Inverted Data number = sequence of events	
Scan	^ (WD1); ^(RD2); ^ (WI3); ^ (RI4)
Init	^ (WD1)
DATA retention	^ (WD1); Pause; ^ (RD2)
Mats+	^(WD_1); ^(RD_2, WI_3); v(RI_4, WD_5);
MarchC–	^(WD1); ^(RD2, WI3); ^(RI4, WD5); v(RD6, WI7); v(RI8, WD9); v(RD10);
Read	^(RD_1);

3.9 DIMM Organization

The Advanced Memory Buffer supports DIMMs with 1 or 2 independent ranks (chip-selects). Each rank consists of 18 4bit DDR SDRAM devices or 9 8bit DDR SDRAM devices. Dual rank DIMMs consist of 36 4bit DDR SDRAM devices or 18 8bit DDR SDRAM devices. Non-ECC DIMMs could also be built with 16bit DDR SDRAM devices .

4 Electrical, Power, and Thermal

This chapter contains a description of the Advanced Memory Buffer's (AMB) electrical DC parameters, timing parameters, power considerations, and thermal considerations.

4.1 Electrical DC Parameters

4.1.1 Absolute maximum ratings

Table 4. 1 contains absolute maximum ratings over operating free-air temperature range (see Note 1).

Table 4.1 — Absolute maximum ratings over operating free-air temperature range (see Note 1)

Symbol	Parameter	Min	Max	Unit
V_{DD}	Supply voltage DRAM Interface	–0.5	+2.3	V
$V_{IN\ (DDR2)}$, $V_{OUT\ (DDR2)}$	Voltage on any DDR2 interface pin relative to Vss (See Notes 2 and 3)	–0.5	+2.3	V
I_{INK} ($V_{IN} < 0$ or $V_{IN} > V_{DD}$)	Input clamp current		±30	mA
I_{OUTK} ($V_{OUT} < 0$ or $V_{OUT} > V_{DD}$)	Output clamp current		±30	mA
I_{OUT} (V_{OUT} = 0 to V_{DD})	Continous output current		±30	mA
N/A	Continuous current through each V_{DD} or GND		±100	mA
V_{CC}	Supply voltage for Core and High Speed Interface	–0.3	+1.75	V
T_{stg}	Storage temperature range	–55	+100	°C

NOTE 1 Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 2 The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

This value is limited to 2.3V maximum.

4.1.2 Normal Mode

Table 4. 2 contains the electrical DC parameters for the Advanced Memory Buffer part in normal mode.

Table 4.2 — Advanced Memory Buffer Normal Mode DC Electrical Parameters

Parameter		Units	Min	Typ	Max
V_{CC} link / core	0kHz - 30kHz	Volts	1.455	1.5	1.575
V_{DD}		Volts	1.7	1.8	1.9
V_{DDSPD}		Volts	3.0	3.3	3.6

Note: There will also be a V_{TT} termination supply at $V_{DD}/2$ available on the DIMM but does not connect to the Advanced Memory Buffer.

Table 4. 2A contains the electrical DC+AC parameters for the Advanced Memory Buffer part in normal mode.

Table 4.2A — Advanced Memory Buffer Normal Mode DC+AC Electrical Parameters

Parameter		Units	Min	Typ	Max
V_{CC} link / core	30kHz - 1MHz	Volts	1.425	1.5	1.590

Note: There is also a +7/-5% tolerance allowed for current load steps associated with initialization/error-recovery state transitions, such as into and out of EI, IBIST, and MEMBIST. For these transitions, a temporary voltage overshoot is expected and acceptable as long as it is within +7% (step transition for 20µs and max duty cycle of 10^{-6}). Transitions between Active and Idle states are not included in this +7%/-5% tolerance.

Table 4. 3 contains the AMB Power Specification Parameters for the Advanced Memory Buffer part in normal mode.

Table 4.3 — AMB Power Specification Parameters and Test Conditions

Symbol	Conditions	Power Supply	Max	Units	Notes
Idd_Idle_0	**Idle Current, single or last DIMM** L0 state, idle (0 BW) Primary channel enabled, Secondary Channel Disabled CKE high. Command and address lines stable. DRAM clock active.	@1.5V		mA	
		@1.8V		mA	
		@3.3V		mA	
Idd_Idle_0 Total Power				W	
Idd_Idle_1	**Idle Current, first DIMM** L0 state, idle (0 BW) Primary and Secondary channels enabled CKE high. Command and address lines stable. DRAM clock active.	@1.5V		mA	
		@1.8V		mA	
		@3.3V		mA	
Idd_Idle_1 Total Power				W	
Idd_Idle_2	**Idle Current, DRAM power down** L0 state, idle (0 BW) Primary and Secondary channels enabled CKE low. Command and address lines floated. DRAM clock active, ODT and CKE driven low.	@1.5V		mA	
		@1.8V		mA	
		@3.3V		mA	
Idd_Idle_2 Total Power				W	

Table 4.3 — AMB Power Specification Parameters and Test Conditions

Symbol	Conditions	Power Supply	Max	Units	Notes
Idd_Active_1	**Active Power** L0 state. 50% DRAM BW, 67% read, 33% write. Primary and Secondary channels enabled. DRAM clock active, CKE high.	@1.5V		mA	
		@1.8V		mA	
		@3.3V		mA	
Idd_Active_1 Total Power				W	
Idd_Active_2	**Active Power, data pass through** L0 state. 50% DRAM BW to downstream DIMM, 67% read, 33% write. Primary and Secondary channels enabled CKE high. Command and address lines stable. DRAM clock active.	@1.5V		mA	
		@1.8V		mA	
		@3.3V		mA	
Idd_Active_2 Total Power				W	
Idd_L0s	**Channel Standby** Average power over 42 frames where the channel enters and exits L0s. DRAMs Idle (0 BW). CKE low. Command and address lines floated DRAM clock active, ODE and CKE driven low.	@1.5V		mA	
		@1.8V		mA	
		@3.3V		mA	
Idd_L0s Total Power				W	
Idd_Training (for AMB spec, Not in SPD)	Training Primary and Secondary channels enabled. 100% toggle on all channel lanes DRAMs idle. 0 BW. CKE high, Command and address lines stable. DRAM clock active.	@1.5V		mA	
		@1.8V		mA	
		@3.3V		mA	
Idd_Training Total Power				W	

Assumptions for all parameters:

Primary channel Drive strength at 100% with De-emphasis at -6.5dB

Secondary channel drive strength at 60% with De-emphasis at -3dB when enabled.

Address and Data fields are pseudo-random, which provides a 50% toggle rate on DRAM data lines and link lanes when data is being transferred.

Assuming 1 activate command and 1 read/write command per BL=4 transfer

BL=4.

10 lanes southbound and 14 lanes northbound are enabled and active (12 lanes NB if non-ECC DIMM).

SPD specific assumption:

Number of devices on the specific DIMM assumed.

Termination of command, address, and control is actual value used on the DIMM.

ECC or non-ECC as per the specific DIMM.

SPD specifies Delta T

AMB power spec specific assumptions:

Dual rank x8 ECC DIMM assumed (18 DRAM devices present on DIMM)

ECC DIMM assumed (72 bit data, 14 lanes northbound).

AMB specification specifies current for each rail.

Table 4.4 contains the AMB Power Specification Parameters for the Advanced Memory Buffer part in normal mode.

Table 4.4 — Values for x8 DIMMs

			533 MHz		667 MHz		800 MHz			
Symbol	**Conditions**	**Power Supply**	**Thermal Design**	**Max Current**	**Thermal Design**	**Max Current**	**Thermal Design**	**Max Current**	**Units**	**Notes**
Idd_Idle_0	**Idle Current, single or last DIMM** L0 state, idle (0 BW) Primary channel enabled, Secondary Channel Disabled CKE high. Command and address lines stable. DRAM clock active.	@1.5V	2.1	2.2	2.4	2.6	*TBD*	*TBD*	A	
		@1.8V	0.6	0.7	0.6	0.7	*TBD*	*TBD*	A	
		@3.3V							A	
Idd_Idle_0 Total Power			**3.5**		**4.0**		***TBD***		W	
Idd_Idle_1	**Idle Current, first DIMM** L0 state, idle (0 BW) Primary and Secondary channels enabled CKE high. Command and address lines stable. DRAM clock active.	@1.5V	2.7	3.0	3.1	3.4	*TBD*	*TBD*	A	
		@1.8V	0.6	0.7	0.6	0.7	*TBD*	*TBD*	A	
		@3.3V							A	
Idd_Idle_1 Total Power			**4.6**		**5.1**		***TBD***		W	
Idd_TDP_0 (for AMB spec, Not in SPD)	**Active Power, TDP BW, Single or Last DIMM** L0 state TDP Channel BW = 2.0GB/s@533; 2.4GB/s@667; 3.0GB/s@800 DIMM BW = 2.0GB/s@533; 2.4GB/s@667; 3.0GB/s@800 67% read, 33% write. Primary channel Enabled Secondary channel Disabled CKE high. Command and Addres	@1.5V	2.4	2.6	2.8	3.0	*TBD*	*TBD*	A	1
		@1.8V	1.1	1.3	1.2	1.3	*TBD*	*TBD*	A	1
		@3.3V							A	
Idd_TDP_0 Total Power			**5.2**		**5.8**		***TBD***		W	1
Idd_TDP_1 (for AMB spec, Not in SPD)	**Active Power, TDP BW, First DIMM** L0 state TDP Channel BW = 2.0GB/s@533; 2.4GB/s@667; 3.0GB/s@800 DIMM BW =2/3 Channel BW = 1.3GB/s@533; 1.6GB/s@667; 2GB/s@800 67% read, 33% write. Primary channel Enabled Secondary channel Enabled CKE high. Command and Ad	@1.5V	3.0	3.3	3.5	3.8	*TBD*	*TBD*	A	1
		@1.8V	0.9	1.0	0.9	1.0	*TBD*	*TBD*	A	1
		@3.3V							A	

Table 4.4 — Values for x8 DIMMs

			533 MHz		667 MHz		800 MHz			
Symbol	**Conditions**	**Power Supply**	**Thermal Design**	**Max Current**	**Thermal Design**	**Max Current**	**Thermal Design**	**Max Current**	**Units**	**Notes**
Idd_TDP_1 Total Power			**5.8**		**6.4**		***TBD***		W	1
Idd_Active_1	**Active Power** L0 state. 50% DRAM BW, 67% read, 33% write. Primary and Secondary channels enabled. DRAM clock active, CKE high.	@1.5V	3.1	3.4	3.6	3.9	*TBD*	*TBD*	A	
		@1.8V	1.2	1.3	1.2	1.3	*TBD*	*TBD*	A	
		@3.3V							A	
Idd_Active_1 Total Power			**6.4**		**7.1**		***TBD***		W	
Idd_Active_2	**Active Power, data pass through** L0 state. 50% DRAM BW to downstream DIMM, 67% read, 33% write. Primary and Secondary channels enabled CKE high. Command and address lines stable. DRAM clock active.	@1.5V	2.9	3.2	3.3	3.7	*TBD*	*TBD*	A	
		@1.8V	0.6	0.7	0.6	0.7	*TBD*	*TBD*	A	
		@3.3V							A	
Idd_Active_2 Total Power			**5.0**		**5.6**		***TBD***		W	
Idd_Training (for AMB spec, Not in SPD)	**Training** Primary and Secondary channels enabled. 100% toggle on all channel lanes DRAMs idle. 0 BW. CKE high, Command and address lines stable. DRAM clock active.	@1.5V		3.5		4.0	*TBD*	*TBD*	A	
		@1.8V		0.7		0.7	*TBD*	*TBD*	A	
		@3.3V							A	
Idd_Training Total Power							***TBD***		W	
Idd_IBIST (for AMB spec, Not in SPD)	**IBIST** Over all IBIST modes DRAM Idle (0 BW) Primary channel Enabled Secondary channel Enabled CKE high. Command and Address lines stable DRAM clock active	@1.5V		3.8		4.5	*TBD*	*TBD*	A	
		@1.8V		0.7		0.7	*TBD*	*TBD*	A	
		@3.3V							A	
Idd_IBIST Total Power							***TBD***		W	
Idd_MemBIST (for AMB spec, Not in SPD)	**MemBIST** Over all MemBIST modes >50% DRAM BW (as dictated by the AMB) Primary channel Enabled Secondary channel Enabled CKE high. Command and Address lines stable DRAM clock active	@1.5V		3.3		3.8	*TBD*	*TBD*	A	
		@1.8V		2.1		2.1	*TBD*	*TBD*	A	
		@3.3V							A	
Idd_MemBIST Total Power							***TBD***		W	
Idd_EI (for AMB spec, Not in SPD)	**Electrical Idle** DRAM Idle (0 BW) Primary channel Disabled Secondary channel Disabled CKE low. Command and Address lines Floated DRAM clock active, ODT and CKE driven low	@1.5V		2.0		2.5	*TBD*	*TBD*	A	
		@1.8V		0.2		0.2	*TBD*	*TBD*	A	
		@3.3V							A	
Idd_EI Total Power							***TBD***		W	

Table 4.4A contains the AMB Power Specification Parameters for the Advanced Memory Buffer part in normal mode.

Table 4.4A — Values for x4 DIMMs

			533 MHz		667 MHz		800 MHz			
Symbol	**Conditions**	**Power Supply**	**Thermal Design**	**Max Current**	**Thermal Design**	**Max Current**	**Thermal Design**	**Max Current**	**Units**	**Notes**
Idd_Idle_0	**Idle Current, single or last DIMM** L0 state, idle (0 BW) Primary channel enabled, Secondary Channel Disabled CKE high. Command and address lines stable. DRAM clock active.	@1.5V	2.1	2.2	2.4	2.6	*TBD*	*TBD*	A	
		@1.8V	0.9	0.9	0.9	0.9	*TBD*	*TBD*	A	
		@3.3V							A	
Idd_Idle_0 Total Power			**3.9**		**4.4**		***TBD***		W	
Idd_Idle_1	**Idle Current, first DIMM** L0 state, idle (0 BW) Primary and Secondary channels enabled CKE high. Command and address lines stable. DRAM clock active.	@1.5V	2.7	3.0	3.1	3.4	*TBD*	*TBD*	A	
		@1.8V	0.9	0.9	0.9	0.9	*TBD*	*TBD*	A	
		@3.3V							A	
Idd_Idle_1 Total Power			**4.9**		**5.5**		***TBD***		W	
Idd_TDP_0 (for AMB spec, Not in SPD)	**Active Power, TDP BW, Single or Last DIMM** L0 state TDP Channel BW = 2.0GB/s@533; 2.4GB/s@667; 3.0GB/s@800 DIMM BW = 2.0GB/s@533; 2.4GB/s@667; 3.0GB/s@800 67% read, 33% write. Primary channel Enabled Secondary channel Disabled CKE high. Command and Addres	@1.5V	2.4	2.6	2.8	3.0	*TBD*	*TBD*	A	1
		@1.8V	1.5	1.6	1.5	1.6	*TBD*	*TBD*	A	1
		@3.3V							A	
Idd_TDP_0 Total Power			**5.9**		**6.5**		***TBD***		W	1
Idd_TDP_1 (for AMB spec, Not in SPD)	**Active Power, TDP BW, First DIMM** L0 state TDP Channel BW = 2.0GB/s@533; 2.4GB/s@667; 3.0GB/s@800 DIMM BW =2/3 Channel BW = 1.3GB/s@533; 1.6GB/s@667; 2GB/s@800 67% read, 33% write. Primary channel Enabled Secondary channel Enabled CKE high. Command and Ad	@1.5V	3.0	3.3	3.5	3.8	*TBD*	*TBD*	A	1
		@1.8V	1.3	1.4	1.3	1.4	*TBD*	*TBD*	A	1
		@3.3V							A	
Idd_TDP_1 Total Power			**6.3**		**6.9**		***TBD***		W	1
Idd_Active_1	**Active Power** L0 state. 50% DRAM BW, 67% read, 33% write. Primary and Secondary channels enabled. DRAM clock active, CKE high.	@1.5V	3.1	3.4	3.6	3.9	*TBD*	*TBD*	A	
		@1.8V	1.6	1.7	1.6	1.7	*TBD*	*TBD*	A	
		@3.3V							A	
Idd_Active_1 Total Power			**6.9**		**7.6**		***TBD***		W	

Table 4.4A — Values for x4 DIMMs

			533 MHz		667 MHz		800 MHz			
Symbol	**Conditions**	**Power Supply**	**Thermal Design**	**Max Current**	**Thermal Design**	**Max Current**	**Thermal Design**	**Max Current**	**Units**	**Notes**
Idd_Active_2	**Active Power, data pass through** L0 state. 50% DRAM BW to downstream DIMM, 67% read, 33% write. Primary and Secondary channels enabled CKE high. Command and address lines stable. DRAM clock active.	@1.5V	2.9	3.2	3.3	3.7	*TBD*	*TBD*	A	
		@1.8V	0.9	0.9	0.9	0.9	*TBD*	*TBD*	A	
		@3.3V							A	
Idd_Active_2 Total Power			**5.5**		**6.1**		***TBD***		W	
Idd_Training (for AMB spec, Not in SPD)	**Training** Primary and Secondary channels enabled. 100% toggle on all channel lanes DRAMs idle. 0 BW. CKE high, Command and address lines stable. DRAM clock active.	@1.5V		3.5		4.0	*TBD*	*TBD*	A	
		@1.8V		0.9		0.9	*TBD*	*TBD*	A	
		@3.3V							A	
Idd_Training Total Power							***TBD***		W	
Idd_IBIST (for AMB spec, Not in SPD)	**IBIST** Over all IBIST modes DRAM Idle (0 BW) Primary channel Enabled Secondary channel Enabled CKE high. Command and Address lines stable DRAM clock active	@1.5V		3.8		4.5	*TBD*	*TBD*	A	
		@1.8V		0.9		0.9	*TBD*	*TBD*	A	
		@3.3V							A	
Idd_IBIST Total Power							***TBD***		W	
Idd_MemBIST (for AMB spec, Not in SPD)	**MemBIST** Over all MemBIST modes >50% DRAM BW (as dictated by the AMB) Primary channel Enabled Secondary channel Enabled CKE high. Command and Address lines stable DRAM clock active	@1.5V		3.3		3.8	*TBD*	*TBD*	A	
		@1.8V		2.4		2.4	*TBD*	*TBD*	A	
		@3.3V							A	
Idd_MemBIST Total Power							***TBD***		W	
Idd_EI (for AMB spec, Not in SPD)	**Electrical Idle** DRAM Idle (0 BW) Primary channel Disabled Secondary channel Disabled CKE low. Command and Address lines Floated DRAM clock active, ODT and CKE driven low	@1.5V		2.0		2.5	*TBD*	*TBD*	A	
		@1.8V		0.2		0.2	*TBD*	*TBD*	A	
		@3.3V							A	
Idd_EI Total Power							***TBD***		W	

Notes and Assumptions:

NOTE 1 Values highlighted in 'Red' are for reference (i.e. placeholder value)

Vdd : Thermal Design = 1.845V (+2.5%) ; Max Current = 1.900V (+5.5%)

Vcc : Thermal Design = 1.530V (+2%) ; Max Current = 1.575V (+5%)

Includes all DIMM DRAM organizations (SRx4, DRx4, SRx8, DRx8) and Raw Cards (A, B, C, D, E, H, J)

For x8, measured with DRx8 raw card B with 39 ohm termination for command, address, and clocks, and 47 ohm termination for CS and CKE

For x4, measured with DRx4 raw card E with parallel 33 ohm termination for command, address, and 39 ohm termination for CS, CKE and clocks

Note: cards using smaller termination resistors will have higher powers. e.g. x4 cards parallel 22 ohm termination for command and address could add as much as 0.4W to the power for all states.

Primary channel Drive strengths at 100% with De-emphasis at -6.5dB

Secondary channel Drive strengths at 60% with De-emphasis at -3.5dB when enabled

Address and Data fields are pseudo-random, which provides a 50% toggle rate on DRAM data lines and link lanes when data is being transferred.

Assuming 1 activate command and 1 read/write command per BL=4 transfer BL=4.

10 lanes southbound and 14 lanes northbound are enabled and active (12 lanes NB if non-ECC DIMM).

Vddspd rail assumed to be insignificant (<0.1 A max @ 3.3v)

Thermal Max is for cooling and heat sink / heat spreader requirements

VR Max is for voltage regulator sizing and voltage distribution and tolerance requirements

Total Power assumes some 1.8v current is dissipated in the DIMM terminations (not in the AMB)

4.1.3 S3 current Specification

S3 is an ACPI mode in which the DIMMs are put into a very lower power state, with the DRAMs in self refresh mode. This AMB S3 current specification is required for the sizing of the power supply used for the S3 mode.

In this mode is defined as:
DRAMs in self refresh.
AMB maintaining the DRAMs in self refresh by driving the CKE signals low.
REFCLK not toggling.
VDD = VDDmax (1.9V).
VCC = 0V
VTT = 0V

			533 MHz		667 MHz		800 MHz		
Symbol	Conditions	Power Supply	Nominal	Max Current	Nominal	Max Current	Nominal	Max Current	Units
Idd_S3	**S3 current** VDD = 1.9V VCC = 0V VTT = 0V Across process variations Across the operating TCASE temperature range. DIMM types: Raw Card A, B, C, D, E, H, J, and future raw card type as adopted by FB-DIMM.	VDD (1.8V)		75		75		75	mA

Note that the total DIMM current will include the AMB IDD_S3 value as well as the self refresh current of all of the DRAMs on the DIMM.

4.2 FBD Channel Interface

Refer to “High Speed Differential PTP Link at 1.5V Specification” for recommended operating conditions.

4.2.1 FBD Electrical Timing Specifications

Table 4.5 contains the FBD electrical timing specifications.

Table 4.5 — Advanced Memory Buffer FBD Timing/Electrical

Symbol	Parameter	Units	Min	Typ	Max	Notes
tEI Propagate	EI Assertion Pass-Thru Timing	nS			60	
tEID	EI Deassertion Pass-Thru Timing	clks			bit lock	
tEI	EI Assertion Duration	clks	100			1
tBitLock	Bit Lock Interval	frames			119	1
tFrameLock	Frame Lock Interval	frames			154	1

NOTE 1 Defined in FBD Architecture and Protocol Spec

4.2.2 AMB Latency Parameters

Parameter	Date Rate	Min	Typ	Max	Units	Comments
tSCL Southbound Command Latency	533				ns	1, 8, 9
	667				ns	
	800				ns	
tNDL Northbound Data Latency	533				ns	2, 9
	667				ns	
	800				ns	
tCCL Core Command Latency	533				ns	3, 5
	667				ns	
	800				ns	
tCDL Core Data Latency	533				ns	4, 5
	667				ns	
	800				ns	
tRESAMPLE Resample Delay	533				ns	6
	667				ns	
	800				ns	
tRESYNC Resync Delay	533				ns	7, 8, 9
	667				ns	
	800				ns	

NOTE1 tSCL is measured from the center of the data eye of the first bit of the command frame at the SB input to the DDR clock rising edge that latches the A-slot command to the DRAMs. See diagram below.

NOTE2 tNDL is measured from the rising edge of the latest DQS input to the AMB to the center of the data eye of the first bit of the matching data frame at the NB outputs. See diagram below.

NOTE3 tCCL is calculated as the maximum time from an internal point where the deskewed frame aligned command is available to the core from the SB IO (the start of the Command to Data Delay) until the DDR clock rising edge that latches the A-slot command to the DRAMs. See diagram below. This maximum considers worst case operating conditions.

NOTE4 tCDL is calculated as the maximum time from the rising edge of the latest DQS input to the time where the data is available to be sent to the NB IO (end point of the Command to Data Delay). See diagram below. This maximum considers worst case operating conditions.

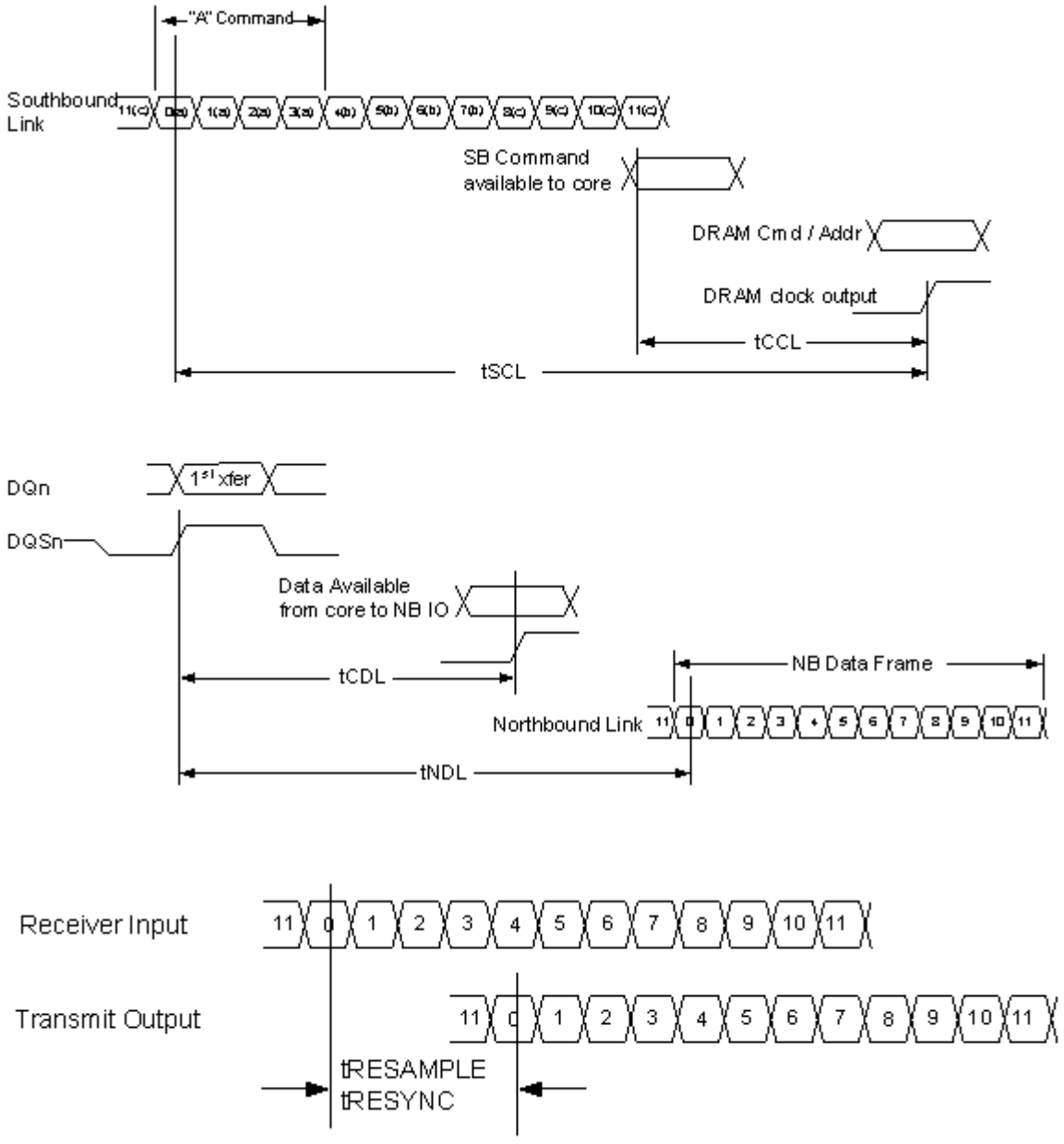
NOTE5 tCCL and tCDL are meant to provide the DIMM vendor with the AMB portion of the Command to Data delay which is included in the SPD. The Command to Data Delay in the SPD consists of tCCL + tCMD_FLT + tDQSCK (DRAM spec) + tDQS_FLT + tCDL. The XXXX_FLT parameters are PCB flight delays. tSCL may have a programmable added delay on some DIMM configurations which must also be added in.

NOTE6 tRESAMPLE is the delay from the southbound input to the southbound output, or the northbound input to the northbound output when in resample mode, measured from the center of the data eye.

NOTE7 tRESYNC is the delay from the southbound input to the southbound output, or the northbound input to the northbound output when in resync mode, measured from the center of the data eye.

NOTE8 Measured upon entering L0 state immediately after channel reset, before the input has drifted with respect to REFCLK.

NOTE9 Typical numbers include the average of any clock synchronizing.



4.2.2.1 AMB Latency Range

Description	Parameter	Data Rate	Min	Max	Units	Comments
Command to Data Latency	tC2D_AMB	533	20.3	25.1	ns	1
		667	17.1	21.1	ns	
		800	TBD	TBD	ns	
Southbound Command Latency	tSCL	533			ns	2
		667			ns	
		800			ns	
Northbound Data Latency	tNDL	533			ns	2
		667			ns	
		800			ns	
Core Command Latency	tCCL	533			ns	2
		667			ns	
		800			ns	
Core Data Latency	tCDL	533			ns	2
		667			ns	
		800			ns	
RESAMPLE Delay	tRESAMPLE_AMB_SB	533	0.9	2.2	ns	3
	tRESAMPLE_AMB_NB	533	0.9	2.2	ns	4
	tRESAMPLE_AMB_SB	667	0.9	1.9	ns	3
	tRESAMPLE_AMB_NB	667	0.9	1.9	ns	4
	tRESAMPLE_AMB_SB	800	TBD	TBD	ns	3
	tRESAMPLE_AMB_NB	800	TBD	TBD	ns	4
RESYNC Delay	tRESYNC_AMB_SB	533	2.3	3.9	ns	5
	tRESYNC_AMB_NB	533	2.3	3.9	ns	6
	tRESYNC_AMB_SB	667	2.0	3.2	ns	5
	tRESYNC_AMB_NB	667	2.0	3.2	ns	6
	tRESYNC_AMB_SB	800	TBD	TBD	ns	5
	tRESYNC_AMB_NB	800	TBD	TBD	ns	6

Notes:

1. **tC2D_AMB** = Measured delay at AMB balls between the center of the1st UI of command frame on the primary southbound lane 8[1] (AMB balls U29 & U28) and the center of the 1st UI of return data on the primary northbound lane 0 (AMB balls U1 & U2) - CL (DRAM CAS latency) value * frame clock period - AL (DRAM additional latency) value * frame clock period.

2. These parameters are included in the Command to Data Latency tC2D_AMB and there is no need for them to be specified individually for interoperability.

3. **tRESAMPLE_AMB_SB** = Measured delay at AMB balls between the center of the 1st UI of a frame on the primary south-bound lane 8 (AMB balls U29 & U28) and the center of the 1st UI of the same frame on the secondary southbound lane 8 (AMB balls Y26 & W26).
4. **tRESAMPLE_AMB_NB** = Measured delay at AMB balls between the center of the 1st UI of a frame on the secondary northbound lane 0 (AMB balls V4 & V5) and the center of the 1st UI of the same frame on the primary northbound lane 0 (AMB balls U1 & U2).

5. **tRESYNC_AMB_SB** = Measured delay at AMB balls between the center of the 1st UI of a frame on the primary southbound lane 8 (AMB balls U29 & U28) and the center of the 1st UI of the same frame on the secondary southbound lane 8 (AMB balls Y26 & W26)..

6. **tRESYNC_AMB_NB** = Measured delay at AMB balls between the center of the 1st UI of a frame on the secondary northbound lane 0 (AMB balls V4 & V5) and the center of the 1st UI of the same frame on the primary northbound lane 0 (AMB balls U1 & U2).

[1]This definition assumes that SB lane 8 is the latest lane to arrive at the AMB balls. This will typically be the case since SB lane 8 is the longest SB lane on FBDIMMs. If, due to large lane-to-lane skew at the DIMM gold finger, another lane is the latest lane to arrive at the AMB balls this other lane must be used instead for the tC2D_AMB measurement.

4.2.2.2 AMB CMD2DATANXT Utilization for Merge Data Training

AMB designs support a limited range of CMD2DATANXT register (refer to 11.3.4.1 in Register chapter) settings during runtime.

The AMB CMD2DATANXT mechanism will be used temporarily by firmware during memory subsystem training to ensure each memory channel with adequate timing margin to prevent Merge Data Errors when mixing different AMB's on a channel. Firmware will over ride the SPD CMD2DATANXT value only during TS2[2], and not while accessing DRAM. Firmware can set the Next Value of Command to Data Delay by as much as 16UI higher than what is programmed in the SPD. The new value will be used after the next fast reset. Once training is completed, the original CMD2DATANXT value from the SPD will be restored. The original value of the Command to Data Delay will take effect after the next fast reset before normal system operation initiates.

AMB designs need to support a range of CMD2DATANXT values for purposes of non-DRAM access, Merge Data training ONLY. The supported range needs to extend at least 16UI higher than the value programmed in the SPD for normal operation.

AMB designs that do not support a particular DLYFRAC value due implementation granularity must functionally round up to the next supported value.

[2]**TS2** – Used during the Polling state to determine the round trip latency of the channel and to test that each individual AMB can perform data merge properly.

4.3 DDR2 DRAM Interface Electrical Specifications

Table 4.6 contains the electrical DC parameters for the DDR2 DRAM Interface on an AMB.

Table 4.6 — Recommended operating conditions for DRAM Interface

Symbol	Parameter	Min	Nom	Max	Unit
V_{DD}	Supply voltage	1.7	1.8	1.9	V
V_{REF}	Input reference voltage	0.49 * V_{DD}	0.50 * V_{DD}	0.51 * V_{DD}	mV
V_{TT}	Termination voltage	V_{REF} – 40	V_{REF}	V_{REF} + 40	mV
Single Ended Signals					
V_{IN}	Input voltage	0	-	V_{DD}	
$V_{IH(dc)}$	DC HIGH-level input voltage	**V_{DD} / 2 + 100**	-	V_{DD} + 300	mV
$V_{IL(dc)}$	DC LOW-level input voltage	-300	-	**V_{DD} / 2 - 100**	mV
$V_{IH(ac)}$	AC HIGH-level input voltage	V_{DD} / 2 + 200	-	-	mV
$V_{IL(ac)}$	AC LOW-level input voltage	-	-	V_{DD} / 2 – 200	mV
V_{OH}	Minimum Required Output Pull-up under AC Test Load	V_{DD} / 2 + 575	-	-	mV
V_{OL}	Maximum Required Output Pull-down under AC Test Load	-	-	V_{DD} / 2 - 575	mV
V_{OTR}	Output Timing Measurement Reference Level	-	0.5*V_{DD}	-	V
$I_{OH(dc)}$	Output minimum source dc current	-13.8	-	-	mA
$I_{OL(dc)}$	Output minimum sink dc current	13.8	-	-	mA
Differential Signals					
$V_{ID(dc)}$	DC differential input voltage	**0.2**	-	-	V
$V_{ID(ac)}$	AC differential input voltage	0.4	-	-	V
$V_{IX(ac)}$	AC differential input crossing voltage	0.5 * VDD - 0.175	-	0.5 * VDD + 0.175	V
Vr	Input timing measurement reference level		$V_{IX(ac)}$		
$V_{OX(ac)}$	AC differential output crossing voltage	0.5 * VDD - 0.125	-	0.5 * VDD + 0.125	V
$V_{OUT\ (slew)}$	Output slew-rate requirement	2.2	-	3.2	V/ns
Iih	Input leakage current (HIGH)	-	-	10	uA
Iil	Input leakage current (LOW)	-	-	10	uA
C_{IO}	Input/Output Capacitance	2.0	-	2.5	pF
R_{OUT}	Output Impedance	13	-	20	Ohms
T_C	Package surface (case) temperature for AMB (In our case, $T_C = T_J$)	-	-	110	^oC

NOTE 1 Values highlighted in 'Red' are for reference (i.e. placeholder value)

NOTE 2 No V_{REF} pin on AMB

NOTE 3 $V_{OUT\ (slew)}$ covers all other outputs slew rate including clock

NOTE 4 Input voltage for all pins is limited to a maximum of 2.3v

NOTE 5 VDD/2 = 1.7/2 = 850mV; V_{OUT} = 575mV. (V_{OUT} - VDD/2)/I_{OH} must be less than 20 Ohm for values of VOUT between VDD/2 and VDD/2 - 275mV.

NOTE 6 VDD/2 = 1.7/2 = 850mV; V_{OUT} = 275mV. V_{OUT}/I_{OH} must be less than 20 Ohm for values of VOUT between 0V and 275mV.

NOTE 7 C_{IO} is the Input/Output capacitance for DQ/DQS, and Output capacitance for CMD/ADDR/CK

This chapter contains a description of the Advance Memory Buffer component's AC electrical parameters

4.4 DDR2 Electrical Output Timing Specifications

4.4.1 Description of DQ/DQS Alignment

The DQS output rising edge aligns with the CLK output rising edge and the DQS output falling edge aligns with the CLK output falling edge. The DQ outputs are 1/4 cycle offset from the DQS outputs.

DQ/DQS inputs are edge aligned and will be skewed by internal receiver DLL. Inputs are terminated on-die by a resistive circuit during reads only.

4.4.2 Description of ADD/CMD/CNTL Outputs

ADD/CMD/CNTL outputs can be adjusted relative to CLK (see Figure 4.6.) to improve setup or hold times. The value of this delay is fixed at boot time. These outputs are either aligned with CLK falling, or with a certain timing offset before CLK falling. The amount of offset is implementation specific (e.g., can be a constant timing offset, or a known ratio of the DRAM clock period).

4.4.3 Test Load Specification

DDR2 timings are specified for a 25 Ohm test load terminated to Vdd/2, measured at the Advance Memory Buffer component package pins.

4.4.4 tDVA and tDVB Parameter Description

The timing parameters tDVA and tDVB indicate the time the DQ is valid after or before DQS. tDVA is used to indicate the time that Data is Valid After. tDVA is used for DQ/DQS write hold calculations (tDH). tDVB is used to indicate the time that Data is Valid Before. tDVB is used for DQ/DQS write setup calculations (tDS).

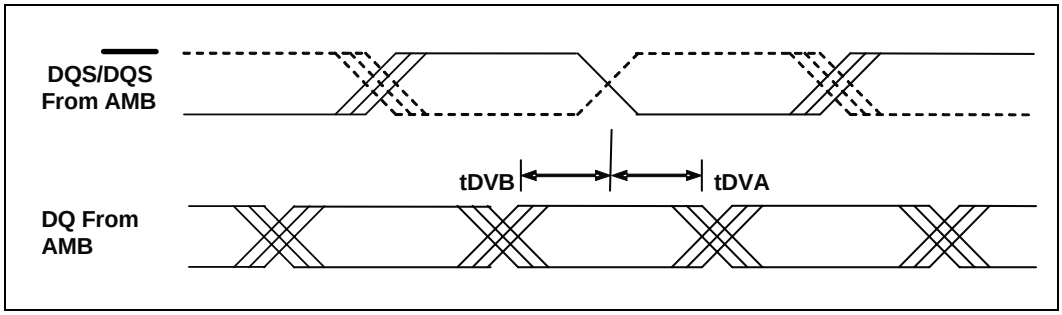


Figure 4.1 — tDVA and tDVB Timing Diagram

4.4.5 tjit and $tjit_{HP}$ Parameter Description

The parameter tjit is the full period jitter, and $tjit_{HP}$ is the half-period jitter.

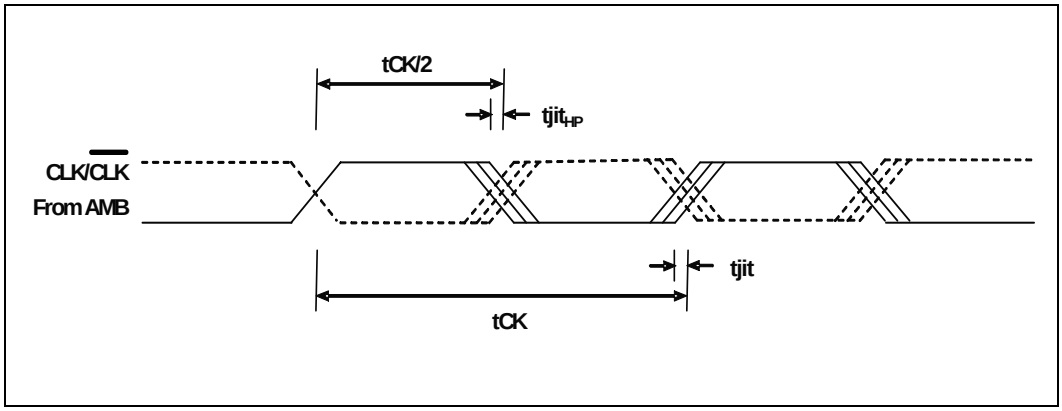


Figure 4.2 — tjit and $tjit_{HP}$ Timing Diagram

4.4.6 tCVA, tCVB, tECVA and tECVB Parameter Description

The parameters tCVA and tCVB specify the time that command is valid after and before CLK. tCVA stands for the time that the Command is Valid After the CLK/$\overline{\text{CLK}}$ crossing point. tCVA is used for CA/CLK hold calculations (tIH). tCVB stands for the time that the Command is Valid Before the CLK/$\overline{\text{CLK}}$ crossing point. tCVB is used for CA/CLK setup calculations (tIS). Figure 4.3 shows tCVA and tCVB.

tECVA and tECVB apply in early mode. For DIMMs with 36 devices, the command, address and control signals can be shifted by 1/6 clock in early mode. Figure 4.4 shows tECVA and tECVB.

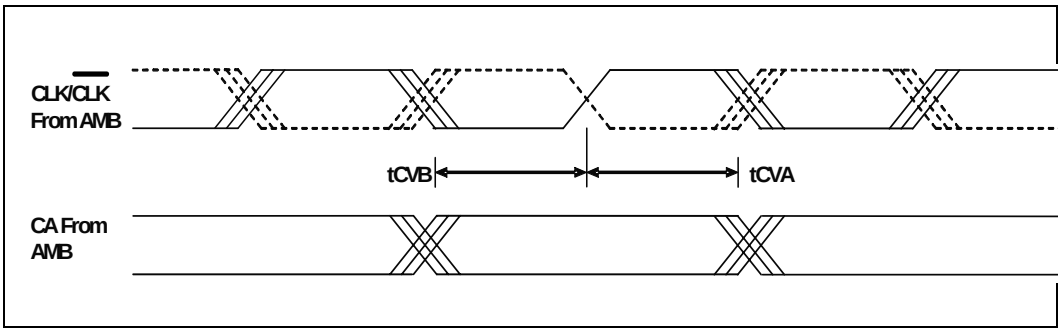


Figure 4.3 — tCVA and tCVB Timing Diagram

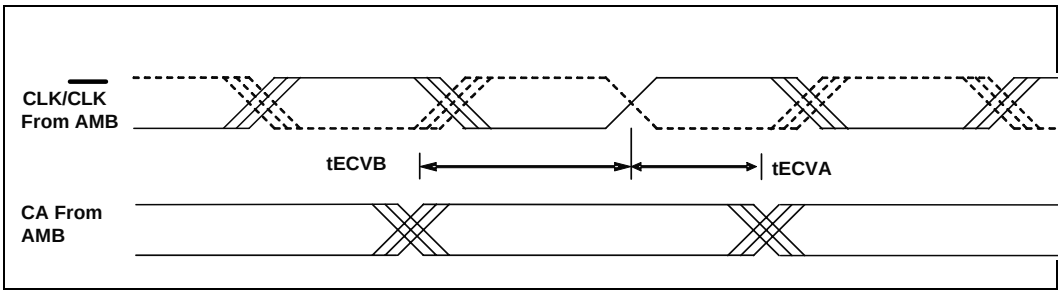


Figure 4.4 — tECVA and tECVB Timing Diagram

4.4.7 tDQSCK Timing Parameter Description

tDQSCK indicated the CLK to DQS delay. This value is used for tDQSS, tDSS and tDSH timing calculations. In order to determine these numbers accurately, package parameters must be taken into account. This adjusts the minimum time by -110 ps and the maximum by -70 ps.

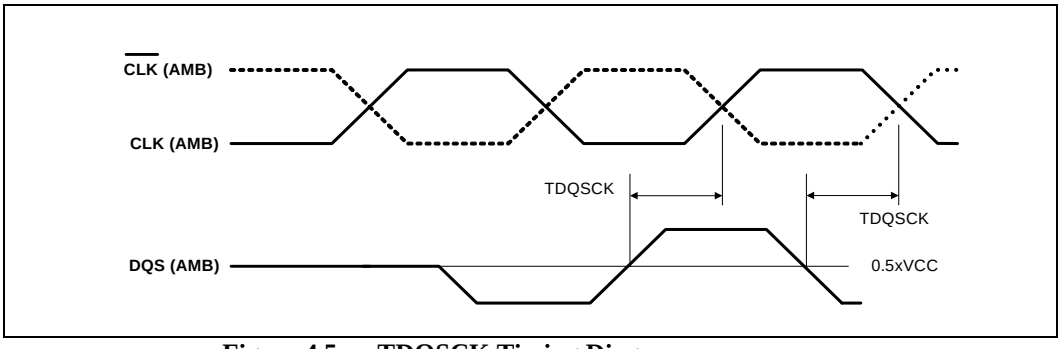


Figure 4.5 — TDQSCK Timing Diagram

4.4.8 DQ and CB (ECC) Setup/Hold Relationships to/from DQS (Read Operation)

Figure 4.6 shows the timing diagram for tHDamb and tSUamb. The data is launched from the DRAM "edge aligned," meaning that the DQ data signals switch coincident with the DQS strobe rising and falling edges. Internal to the Advance Memory Buffer, the DQS strobe is delayed by approximately a quarter clock, and this delayed clock is then used to capture the DQ data. Thus, the setup time tSUamb is negative, meaning that the data can arrive at the Advance Memory Buffer inputs after the strobe, and tHDamb is greater than a quarter clock, so that the data will not change until after it has been captured by the internally delayed strobe. The Advance Memory Buffer determines the correct internal delay of strobe DQS based on a search of the data eye during the initialization of the system. The tHDamb and tSUamb specifications are based on an idealized data eye, where the search delays the strobe by exactly one quarter clock. The sum of tHDamb and tSUamb is equivalent to the minimum data valid window at the Advance Memory Buffer inputs.

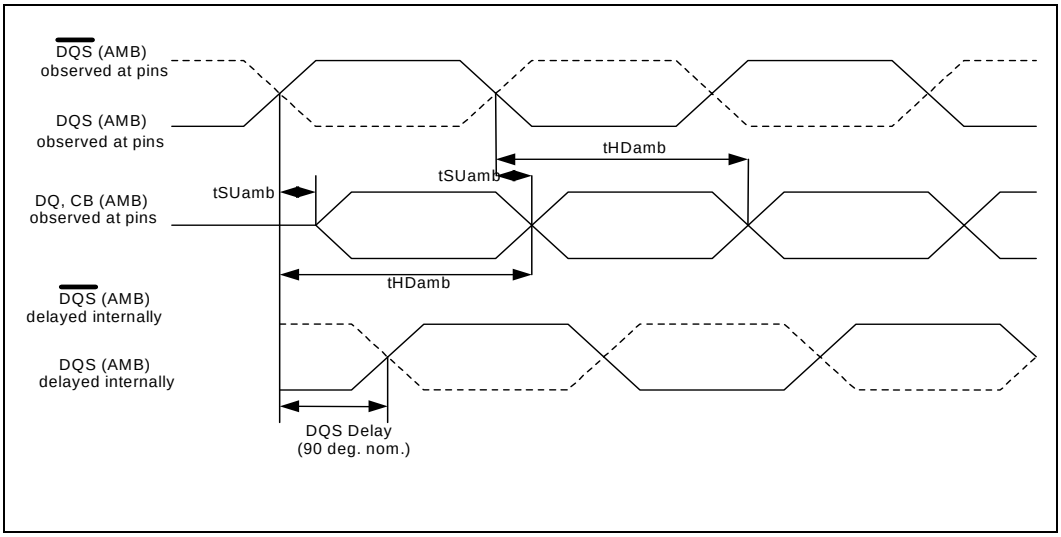


Figure 4.6 — DQ and CB (ECC) Setup/Hold Relationship to/from DQS Timing Diagram

4.4.9 Write Preamble Duration

The write preamble duration is the measurement from the point when DQS and $\overline{DQS}$ start to be driven, to the crossing point of DQS and $\overline{DQS}$. Typically, to determine when DQS and $\overline{DQS}$ are starting to be driven, timing measurements are made at 0.5xVCC +/- 50 mV, and 0.5xVCC +/- 100 mV, and then the measurements are linearly extrapolated back to 0.5xVCC.

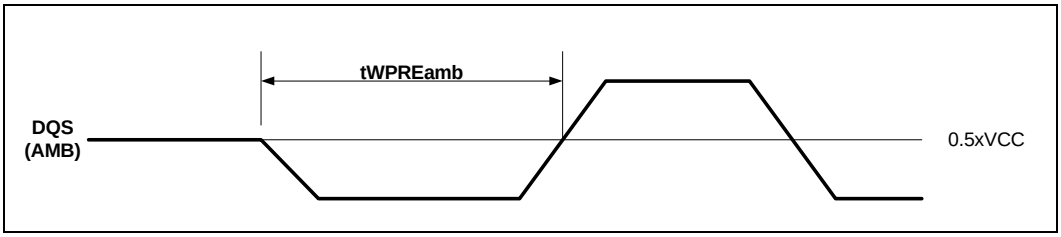


Figure 4.7 — Write Preamble Duration Timing Diagram

4.4.10 Write Postamble Duration

The write postamble duration is the measurement from the crossing point of DQS and $\overline{DQS}$, to the point where DQS and $\overline{DQS}$ start to go into a high impedance state. Typically, to determine when DQS and $\overline{DQS}$ are starting to go into a high impedance state, for DQS, timing measurements are made at Vlow + 50 mV, and Vlow + 100 mV, and then the measurements are linearly extrapolated back to Vlow. For $\overline{DQS}$, timing measurements are made at Vhigh - 50 mV, and Vhigh - 100 mV, and then the measurements are extrapolated back to Vhigh.

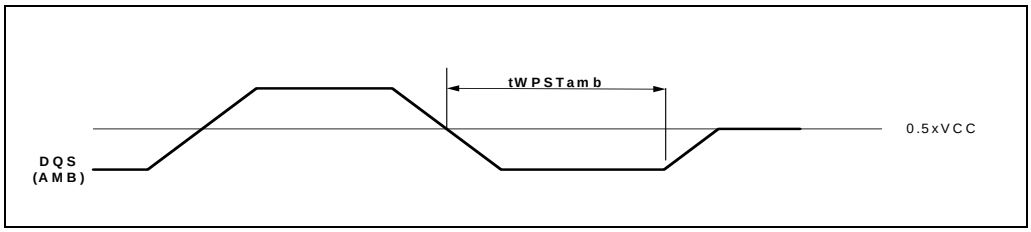


Figure 4.8 — Write Postamble Duration Timing Diagram

4.4.11 Advance Memory Buffer Component Electrical Timing Summary

Table 4.7 and Table 4.8 contain the electrical timing specifications for the Advance Memory Buffer component DDR2 interface.

Table 4.7 — Advance Memory Buffer Component DDR2 Electrical Timing Specifications (Sheet 1 of 3)

Note: Values in the DDR2 800 column are for example only. Subject to change based on JEDEC DDR2 Specification timing closure).

Symbol	Parameter	DDR2 800		DDR2 667		DDR2 533		Units	Fig #
		Min	Max	Min	Max	Min	Max		
System Memory Clock Timings									
t_{CK}	Ideal clock (CK) period	2.5		3.0		3.75		ns	
tCH	CK high time	1.12		1.35		1.70		ns	
tCL	CK low time	1.12		1.35		1.70		ns	
tjit	CK cycle to cycle Jitter		130		150		175	ps	4-7
$tjit_{HP}$	CK half-cycle jitter		130		150		175	ps	4-7
TDQSCK	Clock rising edge to DQS rising edge, or clock falling edge to DQS falling edge --includes -110/-70 ps for package	-190	10	-200	20	-210	30	ps	4-10
System Memory Address/Command/Control Signal Timings (Normal)									
tCVB	CMD/ADD/CNTL output valid before CLK/$\overline{CLK}$	1030		1260		1615		ps	4-8

Table 4.7 — Advance Memory Buffer Component DDR2 Electrical Timing Specifications (Sheet 2 of 3)

Note: Values in the DDR2 800 column are for example only. Subject to change based on JEDEC DDR2 Specification timing closure).

Symbol	Parameter	DDR2 800		DDR2 667		DDR2 533		Units	Fig #
		Min	Max	Min	Max	Min	Max		
tCVA	CMD/ADD/CNTL output valid after CLK/$\overline{CLK}$ -- includes -140 ps for package	890		1120		1475		ps	4-8
System Memory Address/Command/Control Signal Timings (Early)									
tECVB	Early CMD/ADD/CNTL output valid before CLK/$\overline{CLK}$	1440		1760		2240			4-9
tECVA	Early CMD/ADD/CNTL output valid after CLK/$\overline{CLK}$ -- includes -140 ps for package	480		620		850			4-9

Table 4.7 — Advance Memory Buffer Component DDR2 Electrical Timing Specifications (Sheet 3 of 3)

Note: Values in the DDR2 800 column are for example only. Subject to change based on JEDEC DDR2 Specification timing closure).

Symbol	Parameter	DDR2 800		DDR2 667		DDR2 533		Units	Fig #
		Min	Max	Min	Max	Min	Max		
System Memory Data and Strobe Signal Timings									
tDVB	DQ[63:0], CB[7:0], valid before DQS[15:0]/ DQS[15:0] crossing	470		575		750		ps	4-6
tDVA	DQ[63:0], CB[7:0], valid after DQS[15:0]/ DQS[15:0] crossing	470		575		750		ps	4-6
tDOPW	DQ[63:0]. CB[7:0] Output Valid Pulse Width	1.12		1.35		1.70		ns	
tSU_{AMB}	DQ and CB Input Setup Time to DQS Crossing	-425		-530		-700		ps	4-11
tHD_{AMB}	DQ and CB Input Hold Time After DQS Crossing	825		970		1180		ps	4-11
$tWPRE_{AMB}$	DQS Write Preamble Duration	2.37	3	2.85	3.5	3.58	4.25	ns	4-12
$tWPST_{AMB}$	DQS Write Postamble Duration	1.12	1.38	1.35	1.65	1.7	2.05	ns	4-13

4.4.12 Reference DDR2 Interface Package Trace Lengths

The following reference package trace lengths have been incorporated into the Advance Memory Buffer timings in Table 4.7.

Table 4.8 — Advance Memory Buffer DDR2 Package Lengths

Signal Group	Min Length	Max Length	Units
CLK/$\overline{CLK}$	24	26	mm
Command/Address	4	20	mm
CKE, CS#	9	22	mm
ODT	10	16	mm
DQS/$\overline{DQS}$/DQ	9	13	mm

§

4.5 SMBUS Interface

Table 4.9 — Recommended operating conditions for SMBUS Interface

Symbol	Parameter	Min	Typ	Max	Unit	Comments
V_{DDSPD}	Supply voltage (SMBUS)	3.0	3.3	3.6	V	3.3v $\pm$10%
V_{IL}	SMBus signal input low voltage	-	-	0.8	V	
V_{IH}	SMBus signal input high voltage	2.1	-	V_{DDSPD}	V	
V_{OL}	SMBus signal output low voltage	-	-	0.4	V	@I_{PULLUP}
$I_{LEAK-BUS}$	Input Leakage per bus segment	-	-	$\pm$200	uA	
$I_{LEAK-PIN}$	Input Leakage per device pin	-	-	$\pm$10	uA	
I_{PULLUP}	Current sinking, V_{OL} = 0.4V	4	-	-	mA	
C_{BUS}	Capacitive load per bus segment	-	-	400	pF	
C_I	Capacitance for SMBDAT or SMBCLK pin	-	-	10	pF	
V_{NOISE}	Signal noise immunity from 10MHz to 100MHz	300	-	-	mV p-p	This is AC item applies to the high-power DC specification only

NOTE 1: Based on High-power SMBus DC Specification

4.6 Misc I/O (1.5 CMOS Driver)

Table 4.10 — Recommended operating conditions for $\overline{\text{RESET}}$ and BFUNC pins

Symbol	Parameter	Min	Typ	Max	Unit	Comments
$V_{IH(dc)}$	DC HIGH-level input voltage	1.0	-	-	V	
$V_{IL(dc)}$	DC LOW-level input voltage	-	-	0.5	V	
ILEAK	Input leakage	-	-	$\pm$ 90	uA	

4.7 Thermal Diode and Analog to Digital Converter (ADC)

A thermal diode with an analog to digital converter (ADC) is required. This is required to enable closed loop thermal control from the host. The host will throttle system memory activity to reduce power.

An 8-bit register will store the temperature. The sensor measures from 0 to 127 degrees C measured in 0.5 degree increments in a register with values from 0 to 255. Internal analog nodes (anode, cathode, etc.) of this circuit will not be brought out to package pins to keep noise at a minimum.

- Sensor Range: 0 °C - 127.5 °C
- Resolution: 0.5 °C
- Accuracy: ±3.0 °C

4.7.1 Thermal Sensor Effects on the Advanced Memory Buffer's Functional Behavior

When enabled, the results of the thermal trip points TEMPLO and TEMPMID are reported in FBD Status 0 responses following Sync commands.

If the temperature exceeds TEMPHI, errors are logged. If the TEMPHIENABLE bit in the TEMPSTAT register is set, DDR shutdown occurs and FBD links go into electrical idle mode. This over TEMPHI behavior also applies when in LAI mode. See the error chapter for a more complete description of chip behavior when TEMPHI is exceeded.

The thermal sensor does **NOT** have any effect on the behavior of the memory refresh during FBD link resets .

A temperature TEMPSTAT.INCREASING bit is also generated depending on whether the temp is greater or less than the last time the INCREASING bit was sampled. Sampling to create INCREASING bit is controlled by writes to register UPDATED. When temperature is above TEMPMID, this information also shows up in the FBDS0.Thermal_Trip register field and in the Status response of FBD Sync commands targeted to FBDS0.

5 Error Handling

5.1 Types of Errors and Responses

5.1.1 FBD Link Errors

5.1.1.1 Link Initialization Errors

Table 5.1 shows link errors that can occur during initialization.

Table 5.1 — Link Errors in Initialization

Error	Response
Multi-lane failures - unable to achieve bit lock on at least 9 of 10 SB lanes	Never come out of Training state
Multi-lane failures - unable to achieve bit lock on at least 12 NB lanes	Never come out of Training state
NB_Data_Merge_Disable - able to achieve bit lock (pass thru link data) but internal errors prevent receiving valid link cmds or merging data	Host sets NB_Merge_Disable bit in TS2 to cause DIMM to be in a pass-thru mode both SB and NB - act as a blind repeater 1. No attempt to decode commands, no response to link register RD/WR, generate no alerts, neither generate or merge any NB traffic 2. SMBus access enabled
Single Lane failure - SB and/or NB	Support normal initialization protocol and Fail Over mode if commanded by host

5.1.1.2 Errors during Channel Operation

Table 5.2 — Link Errors in Normal Operation

Error	Response
CRC Error on SB frame "A" Command - detected by 14-bit CRC (or reduced 10-bit CRC in Fail Over mode) or CRC Error on SB data or "BC" Commands in Command Frame - detected by 22-bit CRC (or reduced 10bit CRC in Fail Over mode	If CMDCRC error type enabled in EMASK Register 1. No command executed 2. 120-bit Raw SB Frame captured in RECFBD Error Log Registers 3. Type of error logged in FERR/NERR registers 4. Error/Alert Asserted bit set in FBD Status 0 register 5. Ignore future commands except Soft Channel Reset until Soft Channel Reset or Link Reset Received 6. Alert Frame sent continuously starting with NB frame in which returned data pattern would be sent if aborted command had been a config read. Alert patterns continue until Soft Channel Reset or Link Fast Reset received. **NOTE:** Will NOT close DRAM pages or place DRAM into Self Refresh until detection of Link Reset. Else ignore error

Table 5.2 — Link Errors in Normal Operation (Continued)

Error	Response
Lose transition density on channel as detected by no Sync in within 2 times the SYNCTRAININT value (typically last 84 frames). **NOTE:** Purpose of this error is not to detect violation of required transition density (6 out of 512) but to detect hang in the host and put DRAM into self refresh. Any corruption caused by lack of transitions will be detected by CRC violations.	If FEWEDGES error type enabled in EMASK Register 1. No command executed in expected Sync slot 2. 120 bit Raw SB Frame captured in RECFBD Error Log Registers 3. Type of error logged in FERR/NERR registers 4. Error/Alert Asserted bit set in FBD Status 0 register 5. DDR Self Refresh FSM triggered to put DRAMs into Self Refresh 6. Ignore future commands including Soft Channel Reset until Link Reset Received 7. Alert Frame sent continuously starting with NB frame in which returned data pattern would be sent if aborted command had been a config read. Alert patterns continue until Link Fast Reset received. Else ignore error
Access to unimplemented register	If UNIMPLCFG error type enabled in EMASK Register 1. Drop Config Write cmds 2. Capture Addr in RECCFG register if not previously set 3. Return 0's data if Config Read (or return -1 if Read addr to unimplemented function - though currently expect all functions to be used) 4. UNIMPLCFG error type logged in FERR or NERR registers 5. Error/Alert Asserted bit set in FBD Status 0 register 6. Else ignore error
Undefined command	Undefined commands with good CRC are ignored. This is not considered an error condition, and is not logged. Treat as reserved command or Channel NOP
TID error on config writes	If the TID bit on a config write matches the value of the previous TID bit, the write is ignored. The TID bit stored in the AMB is left unchanged in this case. This error does not cause an alert frame, and is not logged. The purpose of the TID bit is to allow the host to retry a config write command following a fast reset if it does not know if it had been executed prior to an alert. If the config write had occurred the TID bit will be the same, the retried write will be ignored. If it had not occurred, the TID bit will be opposite, and the retried write to will be executed.

5.1.2 DDR Errors

Table 5.3 — DDR Errors

Error	Response
Failure of software to achieve calibration	This is detected through firmware during the calibration routine. Firmware should treat the DIMM as a repeater if it is an intermediate DIMM or map it out if it is the last DIMM in the chain
DDR voltage does not power up	if normal FBD interface comes up, should at least act like a repeater. Does not bring down FBD channel - like above. DDR cmds directed at DIMM will fail to return valid responses..

5.1.3 Host Protocol Errors

AMBs are not expected to detect bad protocol from the host.

Table 5.4 — Host Protocol Errors

Error	Response
Illegal combinations of commands • see Concurrent Command Delivery Rules section of the FBD Architecture and Protocol Specification	AMB response to illegal command combinations is undefined
Commands to multiple AMBs to return data in the same return frame.	If multiple AMBs attempt to return data in the same frame, the host will see the data from the northern most AMB which is providing data, as it will replace any data sent from AMBs to its south. A host controller should not produce commands which would cause multiple AMBs to respond with data in the same frame. A special case can occur where Alert frames are being sent by one or more AMBs while another AMB is returning data from a command. These cases are discussed in the Architecture and Protocol spec in the Northbound Alert Frame section.

5.1.4 Other Errors

Table 5.5 — Other Errors

Error	Response
Overtemp - Temp > TEMPHI and overtemp enabled	If OVERTEMP error type enabled in EMASK Register 1. The OVERTEMP bit will be set in the FERR or NERR register as appropriate 2. Error/Alert Asserted bit set in FBD Status 0 register If TEMPHIENABLE set in TEMPSTAT register also 3. Shut down DDR channel: • Drive CKE low to the DRAMs and float the command, address, and data signals. CKE, ODT, and clock continue to be driven. The clocks to the DRAMS may be stopped after the CKE has been registered low 4. The FBD interface goes to electrical idle, with the receivers shut off to reduce power. 5. The core will continue to be clocked, and the Advanced Memory Buffer will respond to SMBus commands. This allows the host controller to determine the error condition **NOTE:** No recovery expected, just trying to prevent Si meltdown The AMB will remain in this state until the temperature is below TEMPHI and the OVERTEMP bit is reset via SMBus or a hardware reset. Else ignore error **NOTE:** A hardware reset will place the TEMPHIENABLE bit in its default state of disabled.
Injected alert	If INJCRC error type enabled in EMASK Register 1. No command executed 2. 120 bit Raw SB Frame captured in RECFBD Error Log Registers 3. Type of error logged in FERR/NERR registers 4. Error/Alert Asserted bit set in FBD Status 0 register 5. Ignore future commands except Soft Channel Reset until Soft Channel Reset or Link Reset Received 6. Alert Frame sent continuously starting with NB frame in which returned data pattern would be sent if aborted command had been a config read. Alert patterns continue until Soft Channel Reset or Link Fast Reset received. Else ignore error

Table 5.5 — Other Errors

Error	Response
Injected error	If INJERR error type enabled in EMASK Register 1. Type of error logged in FERR/NERR registers 2. Error/Alert Asserted bit set in FBD Status 0 register Else ignore error
No REFCLK	Reset should not be released if no REFCLK present.PLL will not achieve lock, the Advanced Memory Buffer will not come out of reset.

5.2 Error Logging

5.2.1 Error Logging Procedure

There are three basic types of errors in FBD: OverTemp, Alerts and Status Only Errors.The first occurrence of errors are flagged in the FERR register. Multiple bits can be set in this register. Subsequesnt errors are flagged in the NERR register.

Unmasked “Alert” errors generate in-band link alert messages. Unmasked “Status Only Errors” an error bit that is returned in regularly scheduled in-band status response messages that occur following Sync commands.

There are error data logs associated with some of the errors . Once the first “Alert” error has been flagged in the FERR or NERR (and matching SB frame data logged), the log registers for that error remain locked until either 1) all "Alert" error bits in the FERR and/or NERR aer cleared, or 2) a power-up reset. Once the first Unimplemented Cofiguration Register Access error has been flagged (and matching address logged), the log registers for that error cannot be over-written until 1) that bit in the FERR and/or NERR cleared or 2) a power-up reset.

5.3 Fail Over Mode Support

The Advanced Memory Buffer supports single lane Fail Over mode as described in the *FB-DMM Architecture & Protocol Specification*. This is done under host control or through the SMBus.

5.4 Failback to Pass-Thru

In general, the Advanced Memory Buffer attempts to minimize the number of Single Points Of Failure (SPOF) that could bring down the entire channel. Errors in any one lane can be mapped out with Fail Over. Errors on the DDR interface can be handled by disabling the DRAM interface and leaving the Advanced Memory Buffer in a repeater like mode. The goal is to allow the system (following a reset or fast reset sequence) to work around the bad DIMM and keep the DIMMs downstream in operation until there is time for system maintenance.

So, in the face of a number of error cases, an Advanced Memory Buffer in an intermediate DIMM should continue to operate in pass-thru mode so that NB and SB data are relayed to the next links in the channel with minimal functionality. Only the following parts of the Advanced Memory Buffer need to be healthy to support this mode:

- Clock inputs and PLL circuitry to generate FBD clocks
- Minimal core logic around FBD I/O enabling and reset
  - — Reset generation
  - — Bit lock detection.
- at least N-1 FBD lanes operational in NB and SB channels

6 Transparent Mode

6.1 Transparent Mode

Refer to the JEDEC publication: *FB-DIMM Draft Specification: Design for Test, Design for Validation (DFx) Specification* for information regarding Transparent Mode.

Transparent mode is designed to allow access to the DRAM behind the AMB. In this mode high speed pins are converted into low speed pins and mapped to DRAM pins. The objective is to allow the use of existing test equipment and manufacturing processes. The tester must be capable of operation at 200 MHz. Transparent mode offers potential improvements in test capacity over traditional DIMMs. In this mode, FBD requires only 60 active pins to test the DIMM.

Data from the tester is 16 bits wide at 200 MHz (single data rate). The data rate is doubled and the width halved on the way to the DRAM (by clocking out 8 bits of data on the rising edge of the clock and the remaining 8 bits on the falling edge).

The tester will drive data to be written to the DRAM on a write pass and data to be compared on a read. DRAM data and the expected data from the tester is compared in the AMB. If the actual and expected data differ the pass/fail outputs will indicate which DRAM failed.

6.1.1 Block Diagram

The data paths for transparent mode will bypass all link logic and normal DRAM control logic. The DDR interfaces are used intact. Figure 6.1 is a block diagram of the Advanced Memory Buffer part in transparent mode.

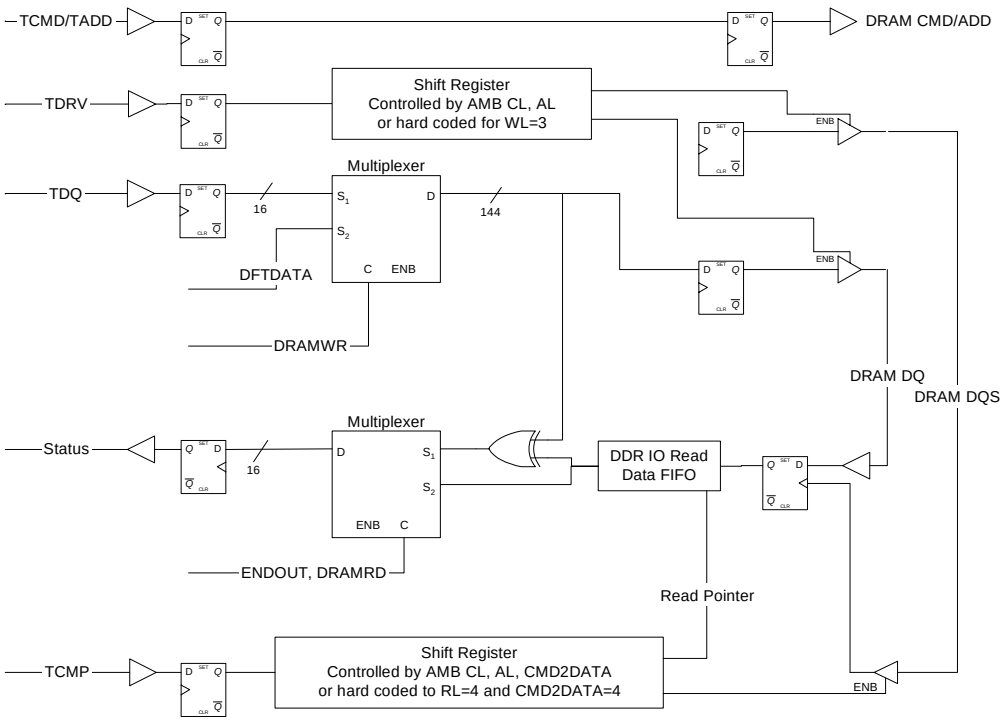


Figure 6.1 — Transparent Mode Simplified Block Diagram

6.1.2 Transparent Mode Signal Definitions

When the transparent mode is enabled. The FBD differential input pins designed in the Advanced Memory Buffer part become two single ended inputs. In transparent mode the FBD input pins require 0 to 500mV swing (half of the normal differential input voltage). Input slew rates should be at least 2V/ns or faster. This parameter is not critical, but it must be fast enough to be recognized by the AMB receiver. The DDR pins will operate with normal DDR2 timings and levels.

The AMB clock input pins will be used for transparent mode as well as normal mode. This also allows use of most of the existing on-chip clock distribution network

Table 6.1 — Additional Signals in Transparent Mode

Transparent Mode Signal Name	Pin Count	Frequency	Direction	Definition
TCKE[1:0]	2	200 MHz	In	Controls CKE[1:0]{A,B}
TCS#[1:0]	2	200 MHz	In	
TODT	1	200 MHz	In	Controls both ODT[1:0]{A,B}
TRAS#	1	200 MHz	In	
TCAS#	1	200 MHz	In	
TWE#	1	200 MHz	In	Controls $\overline{\text{WE}}${A,B}
TBA[2:0]	3	200 MHz	In	
TA[14:0]	15	200 MHz	In	
TDRV	1	200 MHz	In	Tester signal to drive data on writes
TCMP	1	200 MHz	In	Tester signal to compare on reads
TDQ[15:8]	8	200 MHz	In	Early data to each byte
TDQ[7:0]	8	200 MHz	In	Late data to each byte
TPF[8:0] or TDQO[15:0]	9 or 16	200 MHz	Out	Used for pass/fail (8:0) or direct access (15:0)
Sum of receivers Sum of drivers	44 16			

6.1.3 Transparent Mode to FBD Pin Mapping

The FBD pin mapping is shown in Table 6.2.

Table 6.2 — Mapping of FBD Pins in Transparent Mode

FBD Pin Name	Count	Speed	Transparent Mode Signal Name	Comment
SN[0], $\overline{SN}$[0]	2	200 MHz	TCKE[1:0]	
SN[1], $\overline{SN}$[1]	2	200 MHz	TCS#[1:0]	
SN[2],	1	200 MHz	TODT	
$\overline{SN}$[2]	1	200 MHz	TRAS#	
SN[3],	1	200 MHz	TCAS#	
$\overline{SN}$[3]	1	200 MHz	TWE#	
SN[4], $\overline{SN}$[4] SN[5]	3	200 MHz	TBA[2:0]	
SN[13:6], [13:6]	16	200 MHz	TA[15:0]	
PS[8]	1	200 MHz	TDRV	
$\overline{PS}$[8]	1	200 MHz	TCMP	
PS[7:0]	8	200 MHz	TDQ[15:8]	early data
$\overline{PS}$[7:0]	8	200 MHz	TDQ[7:0]	late data
SS[8:0]	9	200 MHz	TPF[8:0]	Pass/Fail mode (TRANSCFG.ENDOUT =0)
PN[13:7], SS[8:0]	16	200 MHz	TDQO[15:0]	Data output mode (TRANSCFG.ENDOUT =1)
Total Pins				

6.1.4 Clock Frequency and Core Timing

The DDR2 DRAM clock frequency is 200 to 400 MHz but core timings require several clocks (or nS) to complete.

For example on DDR2 667:

- tCL, tRP and tRCD are 4 clocks or 12 ns
- tRC is 57 ns
- tRRD is 7.5 ns

DDR2 transactions are burst-oriented, reading or writing 4 or 8 words of data across 4 or 8 clock edges. Assuming a 4 bit burst, a x8 DRAM will transfer 32 bits on successive edges of 2 DRAM clock cycles. On the tester side of the interface the same 32 bits of data is transferred, 16 bits at a time, over two DRAM cycles.

Command, address and data edges should be reasonably close to the appropriate clock edge but with some margin of error. DRAM setup and hold times are 400 to 600pS, while the half cycle time is at least 1250pS. As long as the data is within ¼ cycle (625pS) of the clock edge it will not violate setup or hold. Since there will be other error terms (DIMM trace length matching, jitter etc.) it is recommended the tester be accurate to +/-300pS.

6.1.5 Transparent mode timing

Normally, transparent mode will use DDR2-400 timing even if the DRAM is rated for faster operation. Optionally an AMB may support operation at frequencies higher than 200MHz.

To set up transparent mode the appropriate AMB registers should be set to AL=0, CL=4 and CMD2DATA=4. Some AMBs may default to these values, in which case programming has no effect. These values establish an internal timing relationship as illustrated in the following figures. Optionally other register values may be supported for special test cases.

Actual placement of DRAM read/write or other commands is dependent on the incoming signals, not the AMB register values. Figure 6. shows an example of a write, read, write sequence using incoming signals that correspond to WL=4 and RL=5. The timing relationships in red (normal font) are fixed relationships (established by the AMB register settings above). These edges will move together. The relationships in green (italic font) are the DRAM timings, which are under control of the tester.

Timing may be changed on the fly (e.g., in the middle of a test pattern) by changing the placement of edges from the tester. DRAM mode registers can be programmed on the fly as needed by including (E)MRS commands in the tester data stream. There is no need to change AMB settings during a test. The only exception is that DRAM BL may be changed on the fly but the data logging logic may get confused if DRAM BL does not match the BL expected by the data logger. All other DRAM settings such as AL and CL may be changed at any time.

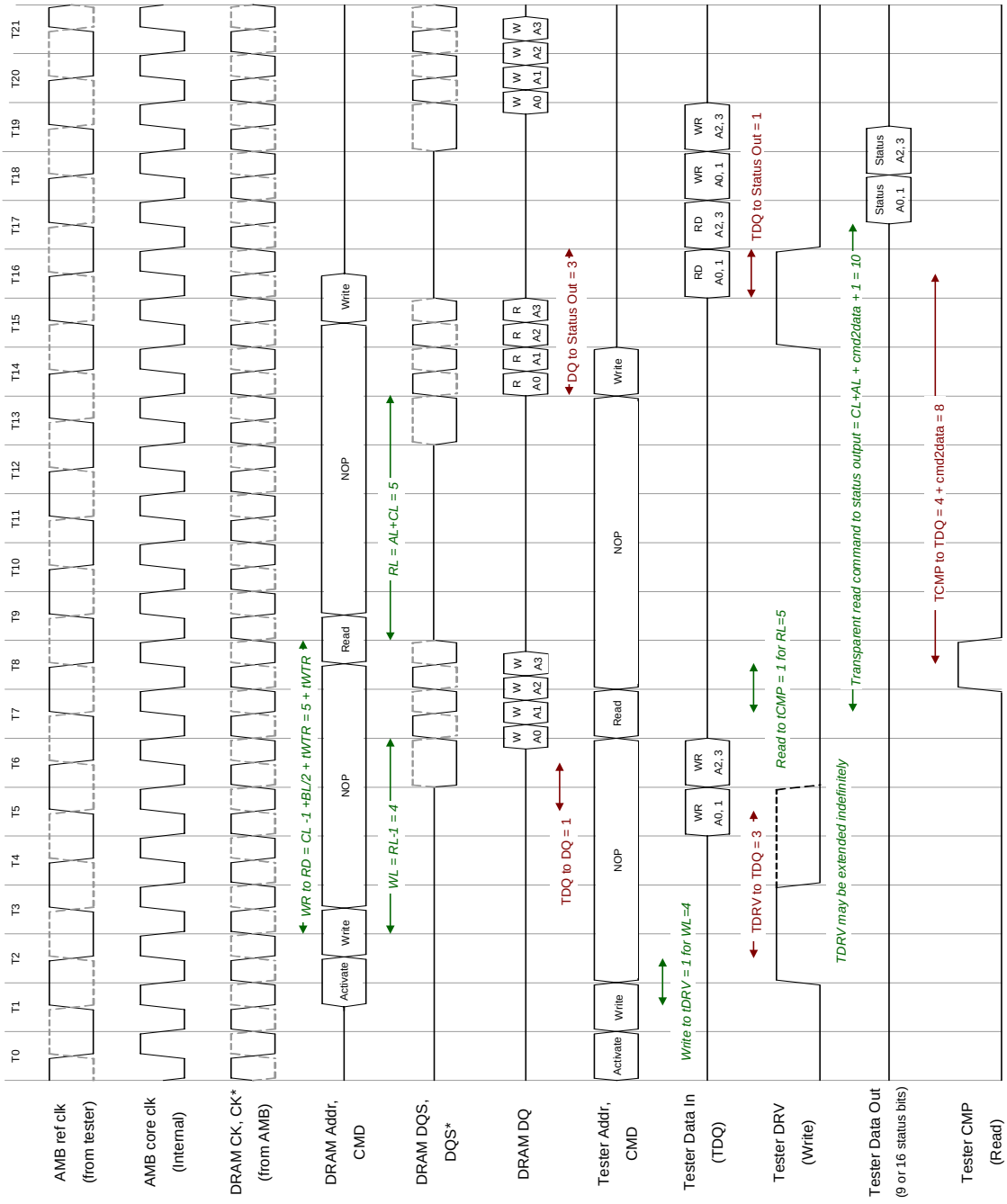


Figure 6.2 — Transparent Mode Timing

6.1.5.1 Write timing

Figure 6. illustrates write timing with the tester set to WL=3, 4, and 5. There is a constant offset of three cycles from TDRV to TDQ and one cycle from TDQ to DRAM DQ. The DRAM mode registers must, of course, be set to the appropriate timing to recognize the read. For BL=8 the TDRV pulse will be 4 clocks wide rather than 2.

6.1.5.2 Extended write timing

The TDRV pulse may be extended indefinitely in cases where it is necessary to apply constant data to the DRAM pins. As long as TDRV remains asserted the AMB will continuously propagate data from the tester TDQ inputs through to the DRAM DQ pins (delayed by 1 cycle) as indicated below.

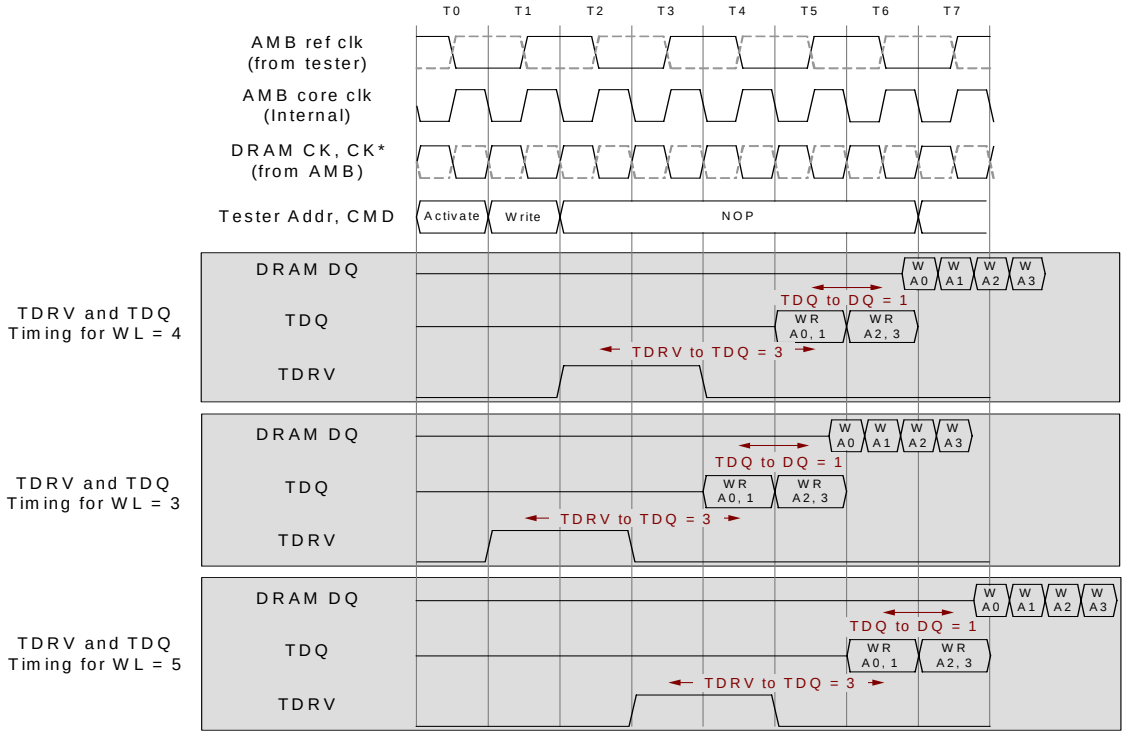


Figure 6.3 — Transparent mode write timing

6.1.5.3 Read timing

Figure 6. shows read timing with the tester set to RL=3 and RL=5. Due to complexities in the handling of read data in an AMB there is a latency of several cycles from the TDRV pulse to TDQ and test status outputs. Specifically there is a constant latency of four cycles plus the programmed CMD2DATA value from TDRV to TDQ (8 cycles total using the AMB settings above) and one cycle from TDQ to DRAM DQ. An AMB may support shorter latencies but this is not required.

TCMP is latched on the rising edge of core clock. This initiates the read inside the AMB. In most cases the AMB will latch DRAM read data slightly before TDQ data is needed. The reason is most AMBs will load DDR data into a queue in the DRAM domain and unload the data on a core clock edge. TDQ is typically not needed until the DRAM data is in the core. The comparison of actual and expected data and propagation back to the tester will occur on the next core clock edge.

The timings below are for BL=4. When testing BL=8 the TCMP pulse should be 3 clocks wide rather than 1. Tester DQ data, DRAM data and the status outputs will be extended appropriately to cover the burst length.

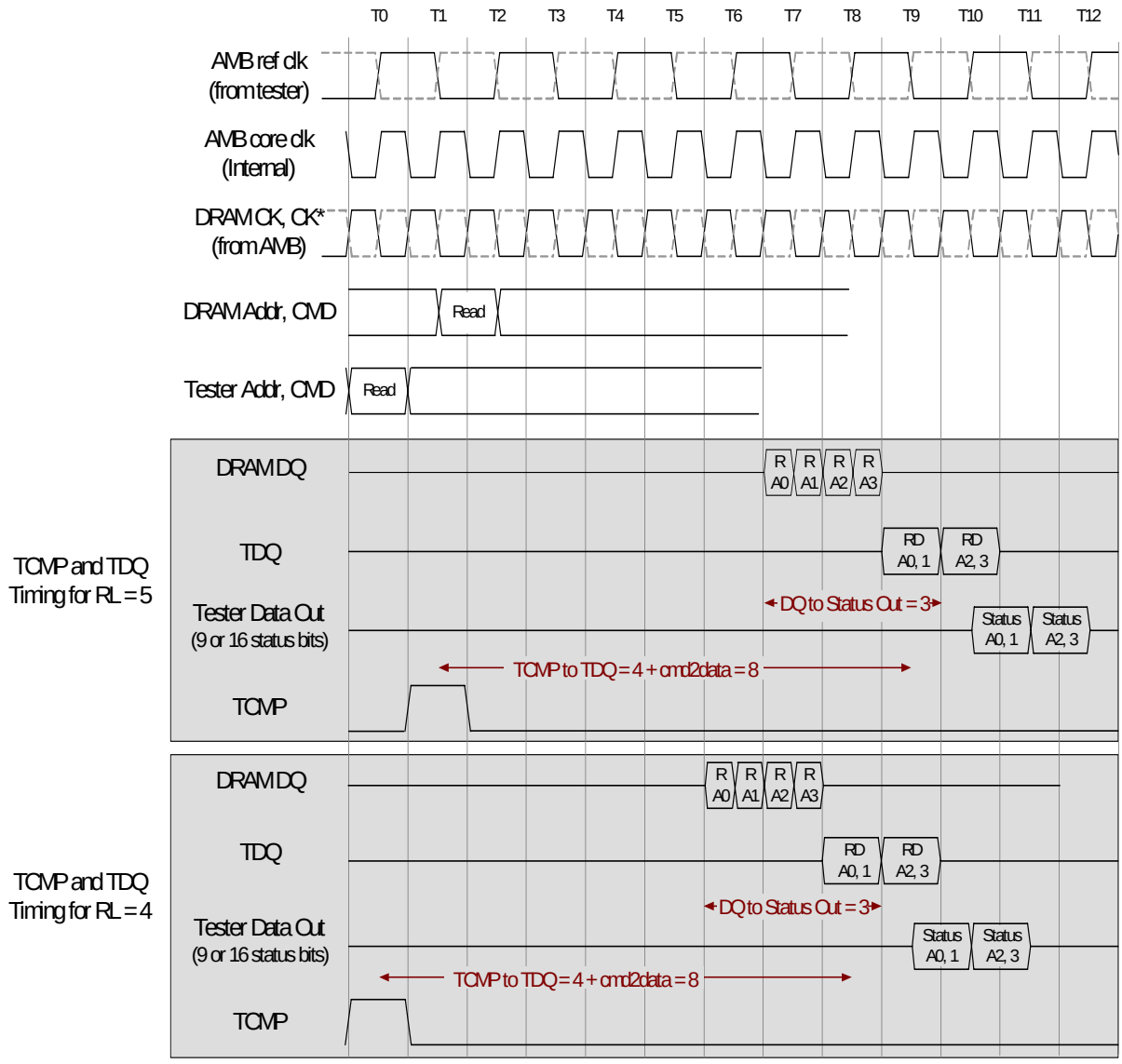


Figure 6.4 — Transparent mode read timing

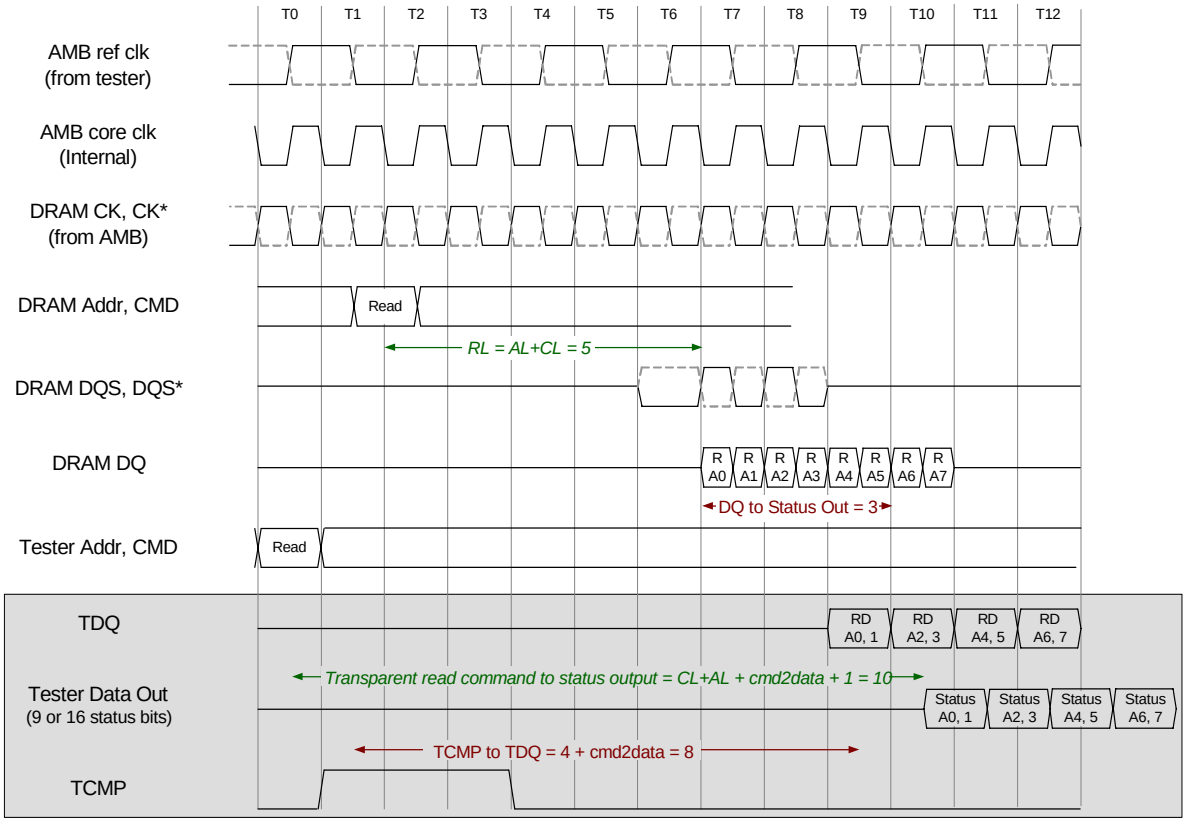


Figure 6.5 — BL=8 Read timing

6.1.6 Error reporting

By default the status pins will be the xor of actual data from the DRAM and expected data from the tester. The AMB also stores 144 bits of DQ data. If the LGFBITS control bit is cleared the 144 bits of data will be actual data read from the DRAM. Otherwise the result of the data compare is stored. In either case the tester must still provide expected data for the AMB to properly set the status pins.

Normally the test will stop when an error occurs. It is the responsibility of the tester or test program to track errors, read error registers and stop or continue as appropriate. This may require multiple iterations of the same test to execute, collect data and re-start the test.

6.1.6.1 Multiple failures

There are some implications if multiple failures occur in the same DRAM burst. Three control register bits determine how these failures should be captured. If the log first fail (LGFFAIL) bit is set, the AMB will record only the first failure in a burst. When the bit is cleared (default), the AMB will record the last failure at the burst position matching the burst position (BSTPOS) setting. If the LGFFAIL bit is set and an error is logged, no further logging will occur until the bit is cleared.

a) If a failure is detected only in one half of the burst (first and second or third and fourth data words), the error pins will indicate which DRAM or DRAMs failed. The error register will indicate which data lines failed and in which data words.

b) If a failure is detected in both halves of the burst (data word 1 or 2 and words 3 or 4), data from the second failure will overwrite data from the first failure. By default this is prevented by the log fail bit. The error pins will continue to operate correctly. If it is desired to collect data from a specific portion of the burst the burst position bits can be used to select an appropriate burst position to record. For a 4 bit burst it is possible to select data from the first or second half of the burst. For an 8 bit burst there are four positions to choose from. These mappings are illustrated in the following figure.

Table 6.3 — Mapping of burst position bits to error capture

Log First Fail	Burst Position		BL=4			
Bit0	Bit1	Bit0	1	2	3	4
1	x	x	144 bits*		or 144 bits*	
0	0	0	144 bits			
0	0	1			144 bits	

Log First Fail	Burst Position		BL=8							
Bit0	Bit1	Bit0	1	2	3	4	5	6	7	8
1	x	x	144 bits*		or 144 bits*		or 144 bits*		or 144 bits*	
0	0	0	144 bits							
0	0	1			144 bits					
0	1	0					144 bits			
0	1	1							144 bits	

* the first failure will be saved in whatever burst position it occurs

6.1.6.2 Direct Access - Testing of individual DRAMs

In certain cases it is desirable to test one or two DRAMs. Transparent mode allows direct access to a single x8 or two x4 DRAMs. In this mode 8 DDR DQ pins are demultiplexed onto 16 SDR status pins, providing16 bit input data path (on TDQ) and a 16 bit output data path on the status pins.

The transparent mode configuration register has one bit (ENDOUT) to enable this mode. On reads, the DRAMRD bits will select the bytes of DRAM data to be presented on the status pins. On writes the DRAMWR bits select a DRAM to receive data from the TDQ bus. A separate register holds 8 bits of default data to be applied to non-selected DRAMs in the early/even cycles and another 8 bits for late/odd cycles. The mapping of these bits to DQ selection is illustrated in the following table.

Table 6.4 — Selection of 8 bit data paths when ENDOUT is set

DRAM RD/WR	DQ	Early Data DQ Byte	Late Data DQ Byte
0xF (DRAM WR only)	all bytes		
8	71:64	8	17
7	63:56	7	16
6	55:48	6	15
5	47:40	5	14
4	39:32	4	13
3	31:24	3	12
2	23:16	2	11
1	15:8	1	10
0	7:0	0	9

DRAMWR is the byte of data bus selected to receive transparent write data, and byte of data bus to be compared against transparent read data. DRAMWR allows a setting of 0xF (all ones) which sends the TDQ input data to all DQ bytes. DRAMRD is the byte of data bus selected to be output on transparent data/status pins when ENDOUT bit is set.

6.1.7 Transparent mode IO specifications

Listed below are the specifcations for transparent mode input and output pins.

Table 6.5 — Transparent mode FB-DIMM interface signaling specifications

	Minimum	Maximum	Units
I/O voltage swing	0	500	mV
Input slew rate	2	-	V/ns
Input to refclk setup time	3000	-	ps
Input to refclk hold time	1000	-	ps
Status output valid to refclk time	-1000	+1000	ps
Vref	200	300	mV
Vil (DC)	-300	200	mV
Vil (AC)	-300	150	mV
Vih (DC)	300	900	mV
Vih (AC)	350	900	mV
Voh	400	-	mV
Vol	-	100	mV
Ioh	8	-	mA
Iol	12	-	mA
Ioh: current into a 50-ohm external load to ground, with on-die transmitter termination enabled Iol: current into a 50-ohm external load to 1.5V supply rail, with on-die transmitter termination enabled			

6.1.8 IO implementation guidelines

6.1.8.1 Dedicated receivers

Simple one-stage receivers for the transparent mode have been added in parallel to the existing high-speed sampling receivers. The latter can be turned off during transparent mode, as well as the DRC and the phase interpolator, to save power and avoid noise. An internal VREF set to 0.25V will be used, so the tester signals should oscillate between 0 and 0.5V. The transparent mode RX should be turned off during normal mode, so as to save power/avoid noise.

6.1.8.2 Common clock scheme

To avoid costly implementations using strobes and FIFOs, a common clock scheme is followed, implemented in the core, where the data capture flops reside. Since transparent mode data signals from the tester are all in phase with the 100MHz system clock, the clock used for the capture flops has to be aligned with the external system clock (or slightly delayed, to account for the propagation delay difference between data receivers and clock receiver).

Aligning core clock and external clock can be done using the HVM mode circuitry included in the PLL. The HVM clock tree will have to feed the capture flops, and one of its leaves has to be fed back to the PLL, in order to achieve adequate synchronization.

6.1.8.3 Tester interface clock and data routing

The following uncertainties have to be factored in:

- Tester board (TIU) trace mismatches
- Package trace mismatches
- FBD low speed RX propagation delay variations due to PVT
- Set up and hold of capture flops (typically <350ps depending on process, voltage and temperature)
- Clock synchronization mismatch, core clock PLL and tree jitter (approximately +/-200pS)

At 200MHz, there is a 5ns data window. The potential FBD low speed receiver variation is approximately 300ps propagation variation over process, voltage and temperature. Package and tester interface mismatches are not expected to exceed 200ps. Flop setup variation should also be less than 200pS. After removing 400ps for clock uncertainties leaves 3.9ns margin. While this is plenty of margin, some amount of trace matching should be done on the tester interface to minimize skew.

6.1.8.4 Outgoing control signals

Only the TX+ pin should connect to the tester. The data on TX- can be discarded (it will toggle at the same rate as TX+).

Terminating TX+ on the tester should be a given, as every tester offers this capability. Terminating TX- could be done on the tester, by having a TIU (tester board) with a route and a tester connection allocated for it. It may be cheaper to just have a 50 ohm resistor tied to ground on the TIU itself, from the TX- pins.

To avoid the crossing clock domains from core clock to FBD fast clocks, the transparent mode data flows directly through the Analog Front-end Unit of the TX.

6.1.8.5 Usage models

6.1.8.5.1 Host side usage

TX: The transmitters are set the same as in normal operation (bias on, enable termination, etc.).

RX: RX+ and RX- signals will be independent. Incoming data will free-flow through the I/O (no flops). The routing distance from transparent_rxout pins should be the same for all capture flops. All these flops should be clocked by the dedicated HVM clock.

6.1.8.5.2 Tester side usage

The tester interface should have trace-matched data signals, to avoid skews > 1ns. The tester should have 50 ohm terminations to ground for all TX pins in use (on-tester termination can be used where applicable). The tester should enable 50 ohm terminations to ground for all the signals sent to RX pins. This will guarantee reasonable signal integrity.

6.2 Transparent Mode Control and Status Registers

In transparent mode, CSRs will be accessed and programmed through SMBus. See Section 12, “Configuration Registers,” for register descriptions.

§

7 SMBus Interface

The Advanced Memory Buffer has configuration registers that provide flexibility and allow for testing and optimization of the chip. Upon system reset (RESET#), configuration registers are reset to predetermined default states, representing the minimum feature set required to successfully bring up a nominal channel. It is expected that the BIOS will properly determine and program the optimal configuration settings.

For all of these registers, the Advanced Memory Buffer supports register access mechanisms through SMBus as well as through in-band channel commands.

7.1 System Management Access

System Management software in the platform can initiate system management access to the configuration registers. This can be done through SMBus accesses.

The mechanism for the Server Management (SM) software to access configuration registers is through a *SMBus Specification*, Rev. 2.0-compliant slave port. Advanced Memory Buffer components contain this slave port and allow access to the configuration registers.

SMBus operations are made up of two major steps: (1) writing information to registers within each component and (2) reading configuration registers from each component. The following sections will describe the protocol for an SMBus master to access an Advanced Memory Buffer component's internal configuration registers. Refer to the *SMBus Specification*, Rev. 2.0 for the bus protocol, timings, and waveforms.

7.1.1 SMBus 2.0 Specification Compatibility

The principal requirement from the SMBus 2.0 specification is support of the "high power" bus electrical specifications described in the layer 1 (Physical layer) chapter.

For the simple register access requirements of FBD, no layer 2 (Link layer) or layer 3 (Network layer) extensions provided by the 2.0 specification are used. In particular, there is no support for Address Resolution Protocol (ARP) since FBD is using fixed addresses. Additionally, only a subset of the network packet protocols described in the specification are needed and these are described below.

AMB's are required to support read and write transactions without requiring clock stretching in order to simplify host controller requirements. For similar reasons, AMB's should not master SMBus transactions in normal operation.

7.1.2 Supported SMBus Commands

The Advanced Memory Buffer components SMBus Rev. 2.0 slave ports support register reads and writes built out of the following SMBus primitive commands:

Block Write Byte Write

Block Read Byte Read

The slave address for each primitive SMBus transaction are determined from the SA pins.

- For normal FBD DIMMs: ;
  - Slave Address[6:3] = 4'b1011
  - Slave Address[2:0] = SA[2:0]
- For repeaters or LAI AMBs: ;
  - Slave Address[6:3] = 4'b0011
  - Slave Address[2:0] = SA[2:0]

Each SMBus transaction has an 8-bit command driven by the master. The format for this command is illustrated in Table 7.1.

Table 7.1 — SMBus command Encoding

7	6	5	4	3:2	1:0
Begin	End	Rsvd	PEC_en	Internal Command: 00 - Read DWord 01 - Write Byte 10 - Write Word 11 - Write DWord	SMBus Command: 00 - Byte 01 - *Rsvd* 10 - Block 11 - *Rsvd*

The *Begin* bit indicates the first transaction of a read or write sequence.

The *End* bit indicates the last transaction of a read or write sequence.

The *PEC_en* bit enables the 8-bit PEC generation and checking logic.

The *Internal Command* field specifies the internal command to be issued by the SMBus slave logic. Note that the Internal Command must remain consistent (i.e. not change) during a sequence that accesses a configuration register. Operation cannot be guaranteed if it is not consistent when the command setup sequence is done.

The *SMBus Command* field specifies the SMBus command to be issued on the bus. This field is used as an indication of the length of transfer so the slave knows when to expect the PEC packet (if enabled).

Reserved bits should be written to zero to preserve future compatibility.

7.1.3 FBD AMB Register Access Protocols

Sequences of these basic commands will initiate internal accesses to the component's configuration registers.

Each configuration read or write first consists of an SMBus write sequence which initializes the register's address . The term sequence is used since these variables may be written with a single block write or multiple byte writes. Once these parameters are initialized, the SMBus master can initiate a read sequence (which performs a configuration read) or a write sequence (which performs a configuration write).

Table 7.2 — SMBus Protocol Addressing fields

Address Field Name	Bits	Description
Reserved	7:0	Reserved - AMB may alias all these addresses to 00h
Dev	4:0	Reserved - AMB may alias all these addresses to 00h
Function	2:0	Function Address
Reg_Num[15:]	7:0	Reserved - AMB may alias all these addresses to 00h
Reg_Num[7:0]	7:0	Register Address within Function

7.1.3.1 Configuration Register Read Protocol

Configuration reads are accomplished through an SMBus write(s) and later followed by an SMBus read. The write sequence is used to initialize the Bus Number, Device, Function, and Register Number for the configuration access. The writing of this information can be accomplished through any combination of the supported SMBus write commands (Block, Byte). The *Internal Command* field for each write should specify Read DWord.

After all the information is set up, the last write (*End* bit is set) initiates an internal configuration read. If an error occurs during the internal access, the last write command will receive a NACK. A status field indicates abnormal termination and contains status information such as target abort, master abort, and time-outs. The status field encoding is defined in the following table.

Table 7.3 — Status Field Encoding for SMBus Reads

Bit	Description
7	Reserved
6	Reserved
5	Reserved
4	Internal Target Abort
3:1	Reserved
0	Successful

Examples of configuration reads are illustrated below. All of these examples have PEC (Packet Error Code) enabled. If the master does not support PEC, then bit 4 of the command would be cleared and there would not be a PEC phase. For the definition of the diagram conventions below, refer to the *SMBus Specification*, Rev. 2.0. For SMBus read transactions, the last byte of data (or the PEC byte if enabled) is NACKed by the master to indicate the end of the transaction. For diagram compactness, “Register Number[]” is also sometimes referred to as “Reg Number” or “Reg Num”.

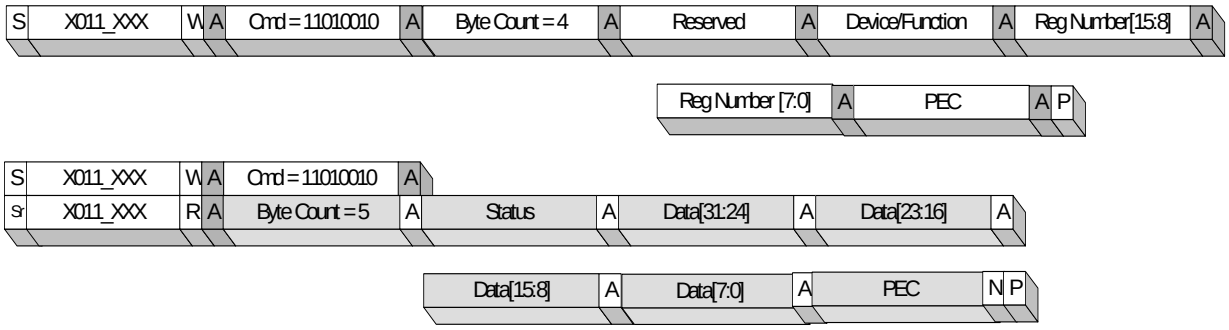


Figure 7.1 — SMBus Configuration Read (Block Write / Block Read, PEC enabled)

The following example uses byte reads.

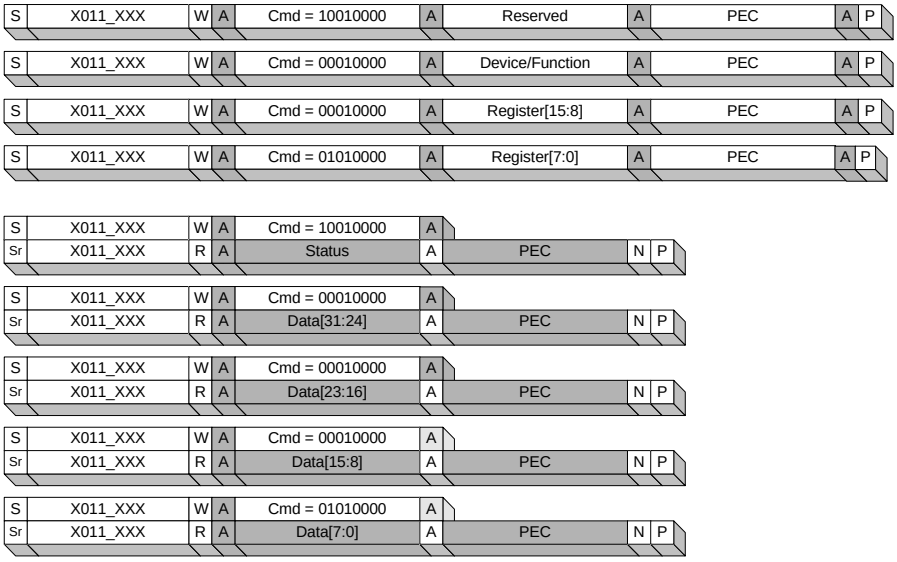


Figure 7.2 — SMBus Configuration Read (Write Bytes / Read Bytes, PEC enabled)

7.1.3.2 Configuration Register Write Protocol

Configuration writes are accomplished through a series of SMBus writes. As with configuration reads, a write sequence is first used to initialize the Bus Number, Device, Function, and Register Number for the configuration access. The writing of this information can be accomplished through any combination of the supported SMBus write commands (Block, Byte).

On SMBus, there is no concept of byte enables. Therefore, the Register Number written to the slave is assumed to be aligned to the length of the Internal Command. In other words, for a Write Byte internal command, the Register Number specifies the byte address. For a Write DWord internal command, the two least-significant bits of the Register Number are ignored. This is different from PCI where the byte enables are used to indicate the byte of interest.

After all the information is set up, the SMBus master initiates one or more writes which sets up the data to be written. The final write (*End* bit is set) initiates an internal configuration write. If an error occurred, the SMBus interface NACKs the last write operation just before the stop bit.

Examples of configuration writes are illustrated below. For the definition of the diagram conventions below, refer to the *SMBus Specification*, Rev. 2.0.

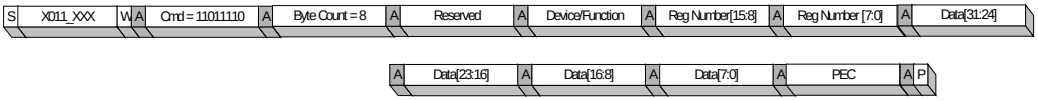


Figure 7.3 — SMBus Configuration Double Word Write (Block Write, PEC enabled)

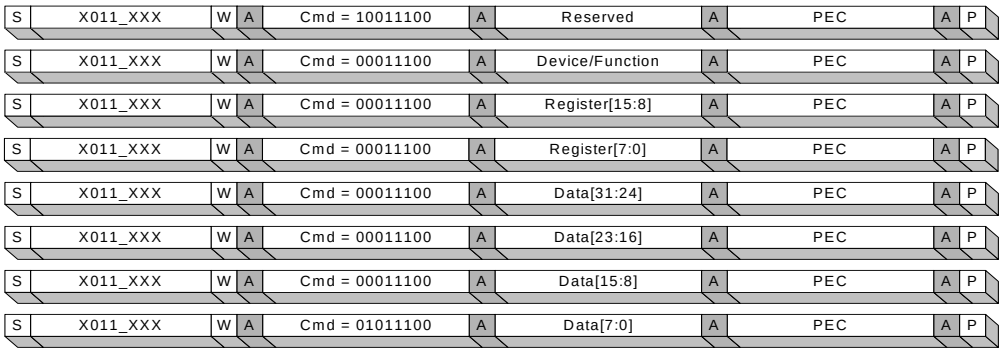


Figure 7.4 — SMBus Configuration Double Word Write (Write Bytes, PEC enabled)

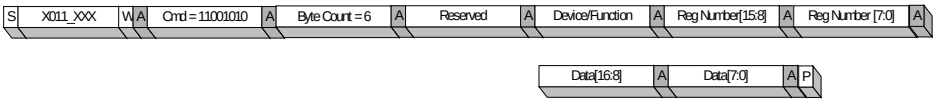


Figure 7.5 — SMBus Configuration Word Write (Block Write, PEC disabled)

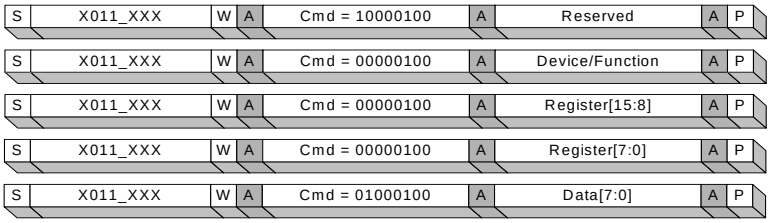


Figure 7.6 — SMBus Configuration Byte Write (Write Bytes, PEC disabled)

7.1.4 SMBus Error Handling

The SMBus slave interface handles two types of errors: internal and PEC. These errors manifest as a Not-Acknowledge (NACK) for the read command (*End* bit is set). If an internal error occurs during a configuration write, the final write command receives a NACK just before the stop bit. If the master receives a NACK, the entire configuration transaction should be reattempted.

If the master supports packet error checking (PEC) and the PEC_en bit in the command is set, then the PEC byte is checked in the slave interface. If the check indicates a failure, then the slave will NACK the PEC packet.

7.1.5 SMBus Resets

7.1.5.1 SMBus transactions during FBD Link Fast Reset

When the FBD link transitions into Electrical Idle (disable state) from an active state, this causes a “fast” reset of all non-sticky registers in the AMB. SMB transactions underway during a “fast” reset will not complete normally.

Generally, this is not a problem since SMBus accesses are only required prior to initial link turn-on or for diagnostic access when a link can not be initialized. It is the host’s responsibility to monitor for SMBus transactions during a fast reset and retry these transactions when the link is stable.

Generally, an interrupted transaction will result in the AMB as slave not properly acknowledging the Master. This protects write transactions. However, if a read transaction has proceeded to the point where the slave no longer acknowledges the master, read data can be lost when the SMBus state machine is reset. If PEC is enabled, this data loss will be detected as a PEC error.

The host restricting usage of SMBus to when the link is idle or monitoring “fast resets” and retrying transactions that are interrupted is the safest SMBus access method.

7.1.5.2 SMBus Interface State Machine Reset

The slave interface state machine can be reset by the master in two ways :

- The master holds SCL low for 25ms cumulative. Cumulative in this case means that all the “low time” for SCL is counted between the Start and Stop bit. If this totals 25ms before reaching the Stop bit, the interface is reset.
  - — Timing is set up to be 25ms for DDR2-800 and may scale up at lower frequencies
    * 30ms at DDR2-667
    * 37.5ms at DDR2-533
- The master holds SCL continuously high for 50us.
  - — Timing is set up to be 50us for DDR2-800 and may scale up at lower frequencies
    * 60us at DDR2-667
    * 75us at DDR2-533

7.1.5.3 SMBus transactions during hard reset

Since the configuration registers are affected by the reset pin, SMBus masters will NOT be able to access the internal registers while the system is reset.

8 Clocking

8.1 Advanced Memory Buffer Clock Domains

There are three main clock domains in the Advanced Memory Buffer. The FBD link domain is a 12x multiple of the core clock. The DDR data-rate domain is 2x the core clock. The core domain frequency equals the DDR command-rate, and is a 2x multiple of the external reference clock. The ratio between these domains remains fixed..

8.2 PLL Clocks

The PLL receives a reference clock at 1/2X, where X is the DDR command frequency. The PLL generates the internal clocks.

8.3 Reference Clock

A low-jitter differential reference clock (REFCLK) is routed to the host and each DIMM from a common clock source on the system board. This reference clock uses HCSL (High-Speed Current Steering Logic) signaling and its detailed requirements are documented in the FB-DIMM Draft Specification: High Speed Differential P2P Link at 1.5V[ref tbd]. The Advanced Memory Buffer uses the reference clock to generate internal buffer clocks and to generate the clocks to the DRAMs located on each DIMM. The frequency of the reference clocks (133 to 200 Mhz) is one half the frequency of the DRAM base clock (267 to 400 Mhz), i.e., it is one half the command-rate of the DRAM devices located behind the Advanced Memory Buffer. For example, for DDR2 667 DRAM devices the reference clock frequency would be 167 MHz. The reference clock is the basis for the various Core, FBD and DDR internal clocks.

It is a requirement for the FBD channel to operate in the presence of Spread Spectrum Clocking (SSC), which is commonly used to reduce EMI. The reference clocks for FBD have to meet a jitter specification.

The reference clocks to the host and each DIMM are mesochronous, i.e. they have an unknown but fixed phase relationship to each other or the memory channel. This simplifies PCB routing since no precise length matching is required. However an upper bound for the clock length mismatch is necessary since the maximum phase difference between the data sent out with the transmitter clock and the receiver clock needs to be limited in the presence of SSC. It is required that all the reference clocks for a given FBD channel originate from a single clock source, e.g. a common clock synthesizer or clock oscillator, and travel through the same jitter spectrum modifying components (e.g. PLL clock buffer) thereby ensuring that there is no frequency mismatch or frequency drift between FBD agents.

The PLL will also operate with the REFCLK at 100 MHz during special transparent mode testing. Since there is no high speed link operation, there can be looser requirements for jitter and no SSC.

8.4 FBD Lane Frame Clocks

Each FBD I/O lane also sources a frame clock at core frequency that is matched to the parallel data sourced by the lane. These are used during initialization to capture data in training sequences and to align data across the link.

8.5 Clock Ratios

The core, DDR and FBD link clock domains are fixed in a 1:2:12 ratio. The SMBus asynchronous subsystem need not scale. The supported clock ratios are shown in Table 8.1.

Table 8.1 — Advanced Memory Buffer Clock Ratios

FBD Link Data Rate	DDR Data Rate	Core Frequency	Ref Clk	FBD Link : Core	Core : DDR
3.2 Gb/s	533 Mb/s	266 MHz	133 MHz	12 : 1	1 : 2
4.0 Gb/s	666 Mb/s	333 MHz	167 MHz	12 : 1	1 : 2
4.8 Gb/s	800 Mb/s	400 MHz	200 MHz	12 : 1	1 : 2

Note: The clock tolerance for the reference clock is -5%, +0.05%. This is reflected in Table 3-1 of the “FB-DIMM Draft Specification: High Speed Differential PTP Link at 1.5V”. Because of this, the FBD Link Data Rate will support the same tolerance (i.e. -5% and +0.05%) as well.

8.6 DDR DRAM Clock Support

The DDR command clocks (CLK[3:0], $\overline{\text{CLK}}$[3:0]) are generated by the Advanced Memory Buffer. They operate at 1X the core frequency for DDR2.

The write strobes operate at the same frequency as the CLK/$\overline{\text{CLK}}$ signals. Write data and check bits are aligned to both the rising and falling edges of the write strobe.

The source-synchronous read strobes operate at the same rates as the write strobes. Each read strobe will be individually aligned with its portion of the data and check-bits.

8.7 Clock Pins

Table 8.2 — Clock Pins

Pin Name	Pin Description
SCK	Advanced Memory Buffer clock
SCK	Advanced Memory Buffer clock (Complement)
VCCAPLL	analog power supply for PLL
VSSAPLL	analog ground for PLL
SCL	SMBus clock
CKE[1:0]{A,B}	DDR clock enables
CLK[3:0]	DDR clocks
$\overline{\text{CLK}}$[3:0]	DDR clocks (Complements)
DQS[17:0]	DDR data/check-bit strobes
$\overline{\text{DQS}}$[17:0]	DDR data/check-bit strobes (Complements)

8.8 PLL Requirements

8.8.1 Jitter

See the FB-DIMM Draft Specification: High Speed Differential P2P Link at 1.5V[ref tbd] for more details.

8.8.2 PLL Bandwidth Requirements

See the FB-DIMM Draft Specification: High Speed Differential P2P Link at 1.5V[ref tbd] for more details.

8.8.3 External Reference

See the FB-DIMM Draft Specification: High Speed Differential P2P Link at 1.5V[ref tbd] for more details.

8.8.4 Spread Spectrum Support

See the FB-DIMM Draft Specification: High Speed Differential P2P Link at 1.5V[ref tbd] for more details.

8.9 Analog Power Supply Pins

Separate filtered power pins are available for use by a PLL if needed.

Warning: The filters are NOT to be connected to board Vss. The ground connection of the filters will be routed through the package and grounded to on-die Vss.

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9 Pin Descriptions

9.1 Pin Description

Table 9.1 — Buffer Signal Types

Buffer Direction	Description
I	Input signal
O	Output signal
A	Analog
I/O	Bidirectional (input/output) signal
NC	No Connect.

Table 9.2 — Pin Description (Sheet 1 of 3)

Signal	Type	Description
Channel Interface		
PN[13:0]	O	**Northbound Output Data:** High speed serial signal. Read path from AMB toward host on primary side of the DIMM connector.
$\overline{\text{PN}}$[13:0]	O	Northbound Output Data Complement
SN[13:0]	I	**Northbound Input Data:** High speed serial signal. Read path from the previous AMB toward this AMB on secondary side of the DIMM connector.
SN[13:0]	I	Northbound Input Data Complement
PS[9:0]	I	**Southbound Input Data:** High speed serial signal. Write path from host toward AMB on primary side of the DIMM connector.
PS[9:0]	I	Southbound Input Data Complement
SS[9:0]	O	**Southbound Output Data:** High speed serial signal. Write path from this AMB toward next AMB on secondary side of the DIMM connector. These output buffers are disabled for the last AMB on the channel.
SS[9:0]	O	Southbound Output Data Complement
FBDRES	A	External precision resistor connected to VCC. On-die termination calibrated against this resistor.
DRAM Interface		
CB[7:0]	I/O	Check bits
DQ[63:0]	I/O	Data
DQS[17:0]	I/O	**Data Strobe:** DDR2 data and check-bit strobe.
DQS[17:0]	I/O	**Data Strobe Complement:** DDR2 data and check-bit strobe complements.
A0A-A15A, A0B-A15B	O	**Address:** Used for providing multiplexed row and column address to SDRAM.

Table 9.2 — Pin Description (Sheet 2 of 3)

Signal	Type	Description
BA0A-BA2A, BA0B-BA2B	O	**Bank Active:** Used to select the bank within a rank.
$\overline{RAS}$A, $\overline{RAS}$B	O	**Row Address Strobe:** Used with $\overline{CS}$, $\overline{CAS}$, and $\overline{WE}$ to specify the SDRAM command.
$\overline{CAS}$A, $\overline{CAS}$B	O	**Column Address Strobe:** Used with $\overline{CS}$, $\overline{RAS}$, and $\overline{WE}$ to specify the SDRAM command.
$\overline{WE}$A, $\overline{WE}$B	O	**Write Enable:** Used with $\overline{CS}$, $\overline{CAS}$, and $\overline{RAS}$ to specify the SDRAM command.
$\overline{CS}$0A-$\overline{CS}$1A, $\overline{CS}$0B-$\overline{CS}$1B	O	**Chip Select:** Used with $\overline{CAS}$, $\overline{RAS}$, and $\overline{WE}$ to specify the SDRAM command. These signals are used for selecting one of two SDRAM ranks. $\overline{CS}$0 is used to select the first rank and $\overline{CS}$1 is used to select the second rank.
CKE0A-CKE1A, CKE0B-CKE1B	O	**Clock Enable:** DIMM command register enable.
ODT0A, ODT0B	O	**DIMM On-Die-Termination:** Dynamic ODT enables for each DIMM on the channel.
CLK[3:0]	O	**Clock:** Clocks to DRAMs. CLK0 and CLK1 are always used. CLK2 and CLK3 are optional and may be disabled when not required.
CLK[3:0]	O	**Clock Complement:** Clocks to DRAMs.
DDR Compensation		
DDRC_C14	A	**DDR Compensation Common:** Common return (ground) pin for DDRC_B18 and DDRC_C18
DDRC_B18	A	DDR Compensation Ball Resistor connected to Compensation Common above
DDRC_C18	A	DDR Compensation Ball Resistor connected to Compensation Common above
DDRC_B12	A	DDR Compensation Ball Resistor connected to VSS
DDRC_C12	A	**DDR Compensation Ball** Resistor connected to VDD
Clocking		
SCK	I	**AMB Clock:** This is one of the two differential reference clock inputs to the Phase Locked Loop in the AMB core. Phase Locked Loops in the AMB will shift this to all frequencies required by the core, DDR channels, and FBD Channel.
SCK	I	**AMB Clock Complement:** This is the other differential reference clock input to the Phase Locked Loop in the AMB core. Phase Locked Loops in the AMB will shift this to all frequencies required by the core, DDR channels, and FBD Channel.
PLLTSTO	O	PLL Clock Observability Output: This pin can be used to observe VCO, reference clock, core clock, etc. For system debug and design characterization.
VCCAPLL	A	**VCC:** PLL Analog Voltage for the core PLL
VSSAPLL	A	**VSS:** PLL Analog Voltage for the core PLL
System Management		
SCL	I/O	SMBus Clock
SDA	I/O	SMBus Address/Data
SA[2:0]		DIMM Select ID
Reset		

Table 9.2 — Pin Description (Sheet 3 of 3)

Signal	Type	Description
$\overline{\text{RESET}}$		Power Good Reset
Miscellaneous Test		
TEST (4 pins)	NC	Pin for debug and test. Must be floated on DIMM.
TESTLO (5 pins)	A	Pin for debug and test. Must be tied to Ground on DIMM
TESTLO_AB20	A	Pin for debug and test. Connected to two resistors. One resistor is connected to VCCFBD, the other resistor is connected to VSS.
TESTLO_AC20	A	Pin for debug and test. Connected to two resistors. One resistor is connected to VCCFBD, the other resistor is connected to VSS.
Power Supplies		
VCC (24 pins)	A	1.5V nominal supply for core IO
VCCFBD (8 pins)	A	1.5V nominal supply for FBD high speed IO
VDD (24 pins)	A	1.8V nominal supply for DDR IO
VSS (156 pins)	A	Ground
VDDSPD	A	3.3V nominal supply for SMB receivers and ESD diodes
Other Pins		
BFUNC	I	**Buffer Function Bit:** When BFUNC = 0, AMB is used as a regular buffer on FB-DIMM. When BFUNC = 1, AMB is used as either a repeater or a buffer for LAI function. On FB-DIMM, BFUNC is tied to Ground
RFU (18 pins)	NC	**Reserved for Future Use.** Must be floated on DIMM. RFU pins denoted by "a" are reserved for forwarded clocks in future AMB implementations.
Other No Connect Pins		
NC (129 pins)	NC	No Connect pins

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10 Reset

10.1 Introduction

This chapter describes aspects of hardware reset specific to the Advanced Memory Buffer.

10.2 Platform Reset Functionality

The FBD channel provides a RESET# signal to initialize all AMBs on the channel. The generation of this signal is platform dependent, and may be asynchronous to the clock. The platform will assert RESET# at power up. This signal may be asserted at other times, such as a warm boot (i.e., a 3 key reset, or machine restart).

It is possible that platform conditions cause RESET# to be asserted at any time, including in the middle of DRAM commands. This could occur during a warm boot. Under these conditions, the Advanced Memory Buffer will be reset and the contents of memory are not guaranteed. The state of the DRAMs must be guaranteed when reinitialized for proper response (refer to 3.5.1 in Section 3 DDR Interface).

10.2.1 Platform RESET# Requirements

RESET# must be asserted at power up, and may also be asserted at other times such as a warm boot.

- Asserting RESET# only at power up will allow error logging registers to be maintained through a warm boot cycle.
- Asserting RESET# at warm boot will clear all error logging registers.

There is no need to delay or lockout RESET# going to the FBD channel since the AMB will guarantee that the tDelay parameter is met. Reference Clocks must remain stable for at least 4 clock cycles after RESET# is asserted in order to allow the AMB to satisfy the tDelay requirement.

- RESET# must be asserted during power up, and for a minimum of 1mS after the FBD channel power and reference clocks SCK/$\overline{\text{SCK}}$are stable.
- RESET# must be asserted for a minimum of 100uS. This will only apply if RESET# is re-asserted while power and clocks remain stable.
- After initial power on , if the reference clock frequency is changed while RESET# is asserted, RESET# must not be deasserted until power and reference clocks SCK/$\overline{\text{SCK}}$ have been stable for at least 1 ms.

10.2.2 Advanced Memory Buffer RESET# Requirements

RESET# is asynchronously applied to all storage elements. Assertion of RESET# may or may not affect AMB PLL operation (depends on specific AMB PLL design).

Upon assertion of RESET#:

- DRAM CKE is driven low asynchronously with minimal delay (within 1 clock, asynch path from reset to CKE)
- DQ/DQS, and C/A are don’t care.
- DRAM CLK/$\overline{\text{CLK}}$ continue to run with no short pulses generated within the tDelay period specified in JESD79-2A Table 36 (timing diagram in Figure 60).
- DRAM CLK/$\overline{\text{CLK}}$ may be stopped after the tDelay has been satisfied.
- All internal register bits are set to their default values, including any error logging bits that are normally not reset by the channel reset.
- The initialization FSM is put into the disable state. All internal state machines are put in their default state.
- All southbound and northbound Tx outputs are put into electrical idle (EI) mode. All Tx outputs stay in EI mode until they are put into Training State (TS0) after deassertion of RESET#.

10.2.3 Power-Up and Suspend-to-RAM Considerations

In a suspend to RAM environment the DRAMs are put into self-refresh mode, and the FBD channel power may be removed. The DRAM power supply remains active. This supply is used by the AMB DRAM interface I/O circuits. The AMB must keep the CKE pins low, without glitches through this transition.

RESET# must be asserted before channel power goes away when entering S3.

DDR control and clock signals will be pulled low during initial power up. This may be done with a voltage detection circuit. CKE must be maintained low during this time without glitches to prevent the DRAMs from exiting self refresh mode. The RESET# signal will remain low during the power-up sequence, for at least 1mS after power and clocks are stable. The CKE signals must remain low until a command is received that takes the CKE signals high. This could be an exit self refresh command, or any of the DRAM CKE commands.

10.3 Reset Types

Types of reset:

- Hard resets occur when the RESET# signal is low. This usually occurs at power up.
- Fast resets occur when there is a reset event on the primary southbound FBD Link.
- SMBus resets affect only the SMBus interface.

10.4 Pads Controlling Reset

The Advanced Memory Buffer resets are controlled by the RESET# pad and the primary southbound FBD link pads. The RESET# pad resets the chip at power up. When the primary southbound FBD link pads indicate EI, a fast reset is started.

10.4.1 RESET# Pad

The RESET# pad is controlled by the platform until after power and SCK/$\overline{\text{SCK}}$ are stable. RESET# asynchronously resets most of the chip to a safe initial state. As the chip comes out of reset, the Primary South FBD Link is expected to be in a reset state. As the link sequences through the first initialization sequence after power up, the Advanced Memory Buffer will not generate any DRAM commands other than to maintain CKE low and enable DRAM clocks at the appropriate time.

10.4.2 Primary FBD Link

When an EI occurs on the primary southbound FBD link a fast reset is started. This starts a handshake procedure putting the DRAMs into self-refresh mode and resetting the Advanced Memory Buffer. Fast reset does not reset the PLL, and sticky registers.

10.5 Details

10.5.1 Cold Power-Up Reset Sequence

1. 1.5V, 1.8V and 3.3V power supplies comes up

- RESET# asserted low while power supplies are coming up
- CKE's are low upon 1.8V power up

2. BIOS queries SPD on all the FBDs on the channel to determine operating conditions
   — channel frequency, compatible DIMMs, DRAM and AMB parameters
3. Clocks up and stable at required frequency

- Reference Clocks should be stable for at least 1ms before RESET# deasserted
- DRAM clocks (CLK/$\overline{\text{CLK}}$) may be toggling at this time

4. RESET# deasserted high

- CKE's to DRAMs remain low

5. No in-band or SMBus transactions for at least 2 ms after RESET# deasserted
6. AMB parameters critical for robust link initialization are programmed via SMBus

- Architected link registers
  — LINKPARNXT: link frequency - Note: some AMBs may use this write to trigger PLL init
  After writing to LINKPARNXT, 200us is required prior to any in-band activity.
  Note: It is generally satisfied by additional SMBus activity.
  — FBDSBCFGNXT: SB transmitter drive strength, de-emphasis setting and pass-thru mode
  — FBDNBCFGNXT:NB transmitter drive strength, de-emphasis setting and pass-thru mode
- Personality Bytes from SPD needed for link inititalization
  — PERSBYTE[5:0]NXT:
  — remaining Personality bytes are not required for link init and may be loaded over the high speed FBD configuration register accesses
- These "Next" register values must be transferred to the matching "Current" registers before the FBD link leaves the DISABLE state
  — Updates may be done right after the NXT register is updated when link is in electrical idle. Updates must be complete before the beginning of training.

7. FBD Link is initialized including CALIBRATION state.
8. Remaining AMB configuration is loaded over high speed FBD channel

- CMD2DATA, remaining Personality bytes, other SPD parameters, DRAM parameters, Errors enabled, etc.

9. FBD Link goes through fast reset (no CALIBRATION) to establish the desired configuration
   DRAM clocks should be stable at this time (i.e. after link train).
10. DRAM interface can now be established
    a. MRS/EMRS setup using DCALCSR and DCALADDR
    b. DRAM interface calibrated using DCALCSR
    c. Optionally, Membist functionality can be used to test the DRAMs
    d. DRAM's can be initialized using MemBist
    e. AMB auto-refresh engine is enabled at this time.

11. Refresh must now be transfered to the host

- Option 1: Use fast reset on the link with DRAMs in self-refresh
  - clear DSREFTC:DISSREXIT to enable fast self refresh exit when link is re-established
  - put the link in disable state which automatically puts the DRAMs in self refresh.
  - Start the refresh engine on the host
  - bring up the link again
  - Host starts sending refresh commands as soon as L0 state reached
- Option 2: write control register to disable auto-refresh engine followed by
  - Clear DAREFTC:AREFEN to turn off auto-refresh
  - Host then immediately takes over sending refresh commands

12. Host now has complete control of the FBD Channel

10.6 Timing Diagrams

Timing diagrams will be released in a future revision of this document.

10.7 I/O Initialization

10.7.1 FBD Channel Initialization

Channel initialization states and uses of fast reset are described in the *FB-DIMM Architecture and Protocol Specification*.

11 Registers

This chapter defines the minimal subset of AMB configuration registers to support this version of the FBD protocol.

11.1 Access Mechanisms

The Advanced Memory Buffer (AMB) component supports PCI configuration space access as defined in the *PCI Local Bus Specification, Rev.2.2*. The internal registers of the AMB can be accessed in byte or double word (32-bit) quantities. All multi-byte numeric fields use “little-endian” ordering (i.e., lower addresses contain the least significant parts of the field). As a memory buffer (not a PCI device or bridge) the AMB is not fully compliant with this mechanism with respect to the standard registers (those with offsets 0-3Fh).

AMB will not be mapped into the host system's PCI Plug and Play hierarchy, but is accessed through a method that is host controller implementation specific.

Problems will occur if the host system maps the registers into the PCI PnP hierarchy.

Configuration accesses are transported on the FBD link as configuration read and write commands, which mimic the corresponding PCI commands.

11.1.1 Conflict Resolution and Usage Model Limitations

AMB accepts configuration register reads and writes through the FBD link and through SMBus transactions. In Logic Analyzer Interface (LAI) mode, registers are not accessible through the in-band FBD link configuration read/write commands.

Registers do not incur read side-effects.

11.1.2 FBD Data on Configuration Read Returns

FBD read return data from AMB is described in the *FB-DIMM Draft Specification: Architecture and Protocol*. Configuration reads are sent in northbound data frames. Only the bottom four bytes of this data are defined for a configuration access. The rest of the bytes in the read return are undefined. Legal CRCs are generated for these undefined inbound bytes.

11.1.3 Non-Existent Register Bits

To comply with the PCI specification, accesses to non-existent registers and bits will be treated as follows:

Table 11.1 — Access to “Non-existent” Register Bits

Access to	Writes	Reads
Registers in unimplemented functions	Have no effect	AMB returns -1
Registers not listed	Have no effect	AMB returns all zeroes
Reserved bits in registers	Software must read-modify-write to preserve the value	AMB returns implementation specific values

11.1.4 Register Attribute Definition

Table 11.2 — Register Attributes Definitions

Attribute	Abbrevi-ation	Description
Read Only	RO	The bit is set by the hardware only and software can only read the bit. Writes to the register have no effect.
Read/ Write	RW	The bit can be read or written by software.
Read/ Write / Clear	RWC	The bit can be either read or cleared by software. In order to clear a bit, the software must write a one to it. Writing a zero to an RWC bit will have no effect. Hardware will set this bit.
Read/ Write /Set	RWS	The bit can be either read or set by software. In order to set this RWS bit, the software must write a one to it. Writing a zero to an RWS bit will have no effect. Hardware will clear this bit.
Sticky	All of the above with "ST" appended to the end	The bit is "sticky" or unchanged by a link reset. These bits can only be defaulted by a power-up reset.
Reserved	RV	This bit is reserved for future expansion and must not be written. The *PCI Local Bus Specification*, Revision 2.2 requires that reserved bits must be preserved. Any software that modifies a register that contains a reserved bit is responsible for reading the register, modifying the desired bits, and writing back the result.

11.1.5 Binary Number Notation

When references are made to binary numbers, the following notation is used:

n'bXX

n - number of digits

b - indicates binary

XX - binary value

For example, 2'b01 is two binary digital of value "01".

11.1.6 Function Mapping

The following functions are described in this chapter:

0) PCI Standard Header Identification Registers
1) FBD Link Registers
2) Implementation Specific FBD Registers
3) DDR and Miscellaneous Registers
4) Implementation Specific DDR Initialization and Calibration Registers
5) DFX Registers
6)IBIST, Bring-up and Debug Registers
7) Implementation Specific

Table 11.3 — Function Mapping Legend

Fill	Description
RegName	Required Architected Register"RegName" in these bytes
Reserved	Reserved Register for future architecture in these bytes
RegName	Optional Architected Register"RegName" in these bytes • No Implementation Specific Registers usage recommended
	Unused Register location available for Implementation Specific use

Table 11.4 — Function 0: PCI Standard Header Identification Registers

DID		VID		00h				80h
				04h				84h
CCR			RID	08h				88h
	HDR			0Ch				8Ch
				10h				90h
				14h				94h
				18h				98h
				1Ch				9Ch
				20h				A0h
				24h				A4h
				28h				A8h
RESERVED				2Ch				ACh
				30h				B0h
				34h				B4h
				38h				B8h
				3Ch				BCh
				40h				C0h
				44h				C4h
				48h				C8h
				4Ch				CCh
				50h				D0h
				54h				D4h
				58h				D8h
				5Ch				DCh
				60h				E0h
				64h				E4h
				68h				E8h
				6Ch				ECh
				70h				F0h
				74h				F4h
				78h				F8h
				7Ch				FCh

Table 11.5 — Function 1: FBD Link Registers

RESERVED				00h	RESERVED				80h
RESERVED				04h	RESERVED				84h
RESERVED				08h	RESERVED			CBC	88h
RESERVED				0Ch	**EMASK**				8Ch
				10h	**FERR**				90h
				14h	**NERR**				94h
				18h	RESERVED		RECCFG		98h
				1Ch	RECFBD1		RECFBD0		9Ch
				20h	RECFBD3		RECFBD2		A0h
				24h	RECFBD5		RECFBD4		A4h
				28h	RECFBD7		RECFBD6		A8h
				2Ch	RECFBD9		RECFBD8		ACh
				30h	PERSBYTE3 NXT	PERSBYTE 2NXT	PERSBYTE 1NXT	PERSBYTE 0NXT	B0h
				34h	PERSBYTE7 NXT	PERSBYTE 6NXT	PERSBYTE 5NXT	PERSBYTE 4NXT	B4h
				38h	PERSBYTE1 1NXT	PERSBYTE 10NXT	PERSBYTE 9NXT	PERSBYTE 8NXT	B8h
				3Ch	RESERVED		PERSBYTE 13NXT	PERSBYTE 12NXT	BCh
FBDS3	FBDS2	FBDS1	FBDS0	40h	PERSBYTE3 CUR	PERSBYTE 2CUR	PERSBYTE 1CUR	PERSBYTE 0CUR	C0h
RESERVED				44h	PERSBYTE7 CUR	PERSBYTE 6CUR	PERSBYTE 5CUR	PERSBYTE 4CUR	C4h
RESERVED				48h	PERSBYTE1 1CUR	PERSBYTE 10CUR	PERSBYTE 9CUR	PERSBYTE 8CUR	C8h
RESERVED				4Ch	RESERVED		PERSBYTE 13CUR	PERSBYTE 12CUR	CCh
LINKPARCUR		FBDNBCFG CUR	FBDSBCFG CUR	50h					D0h
LINKPARNXT		FBDNBCFG NXT	FBDSBCFG NXT	54h					D4h
FBDNBCFG NXT (TMT)	FBDSBCFG NXT (TMT)	RESERVED		58h					D8h
RESERVED			MODES	5Ch					DCh
FEATURES				60h					E0h
FBDLIS				64h					E4h
RESERVED		FBDLOCKTO		68h	C2DINCRCUR	C2DINCRNXT	CMD2DATACUR	CMD2DATANXT	E8h
			FBDHAC	6Ch	RESERVED		C2DDECRCUR	C2DDECRNXT	ECh
			RECALDUR	70h					F0h
			L0SDUR	74h					F4h
			SYNCTRAINT	78h					F8h
NBCALSTATUS		SBCALSTATUS		7Ch					FCh

Table 11.6 — Function 2: Implementation Specific FBD Registers

RESERVED	00h	80h
RESERVED	04h	84h
RESERVED	08h	88h
RESERVED	0Ch	8Ch
	10h	90h
	14h	94h
	18h	98h
	1Ch	9Ch
	20h	A0h
	24h	A4h
	28h	A8h
	2Ch	ACh
	30h	B0h
	34h	B4h
	38h	B8h
	3Ch	BCh
	40h	C0h
	44h	C4h
	48h	C8h
	4Ch	CCh
	50h	D0h
	54h	D4h
	58h	D8h
	5Ch	DCh
	60h	E0h
	64h	E4h
	68h	E8h
	6Ch	ECh
	70h	F0h
	74h	F4h
	78h	F8h
	7Ch	FCh

Table 11.7 — Function 3: DDR and Miscellaneous Registers

RESERVED				00h	UPDATED	TEMPHI	TEMPMID	TEMPLO	80h
RESERVED				04h			TEMP	TEMPSTAT	84h
RESERVED				08h					88h
RESERVED				0Ch					8Ch
				10h					90h
				14h					94h
				18h					98h
				1Ch	**MB_START_ADDR**				9Ch
				20h	**MB_END_ADDR**				A0h
				24h	**MB_LFSR**				A4h
				28h	**MBFADDRPTR**				A8h
				2Ch	RESERVED				ACh
				30h	**MB_ERR_DATA00**				B0h
				34h	**MB_ERR_DATA01**				B4h
				38h	**MB_ERR_DATA02**				B8h
				3Ch	**MB_ERR_DATA03**				BCh
MBCSR				40h			MB_ERR_DATA04		C0h
MBADDR				44h					C4h
MBDATA0				48h					C8h
MBDATA1				4Ch					CCh
MBDATA2				50h					D0h
MBDATA3				54h					D4h
MBDATA4				58h					D8h
MBDATA5				5Ch					DCh
MBDATA6				60h					E0h
MBDATA7				64h					E4h
MBDATA8				68h					E8h
MBDATA9				6Ch					ECh
DAREFTC				70h					F0h
MTR	DSREFTC			74h					F4h
DRT				78h					F8h
DRC				7Ch					FCh

Table 11.8 — Function 4: Implementation Specific DDR Initialization and Calibration Registers

RESERVED				00h					80h
RESERVED				04h					84h
RESERVED				08h					88h
RESERVED				0Ch					8Ch
				10h					90h
				14h					94h
				18h					98h
				1Ch					9Ch
				20h					A0h
				24h	S3RESTORE0				A4h
				28h	S3RESTORE1				A8h
				2Ch	S3RESTORE2				ACh
				30h	S3RESTORE3				B0h
				34h	S3RESTORE4				B4h
				38h	S3RESTORE5				B8h
				3Ch	S3RESTORE6				BCh
DCALCSR				40h	S3RESTORE7				C0h
DCALADDR				44h	S3RESTORE8				C4h
				48h	S3RESTORE9				C8h
				4Ch	S3RESTORE10				CCh
				50h	S3RESTORE11				D0h
				54h	S3RESTORE12				D4h
				58h	S3RESTORE13				D8h
				5Ch	S3RESTORE14				DCh
				60h	S3RESTORE15				E0h
				64h					E4h
				68h					E8h
				6Ch					ECh
				70h					F0h
				74h					F4h
				78h					F8h
				7Ch				DDR2ODTC	FCh

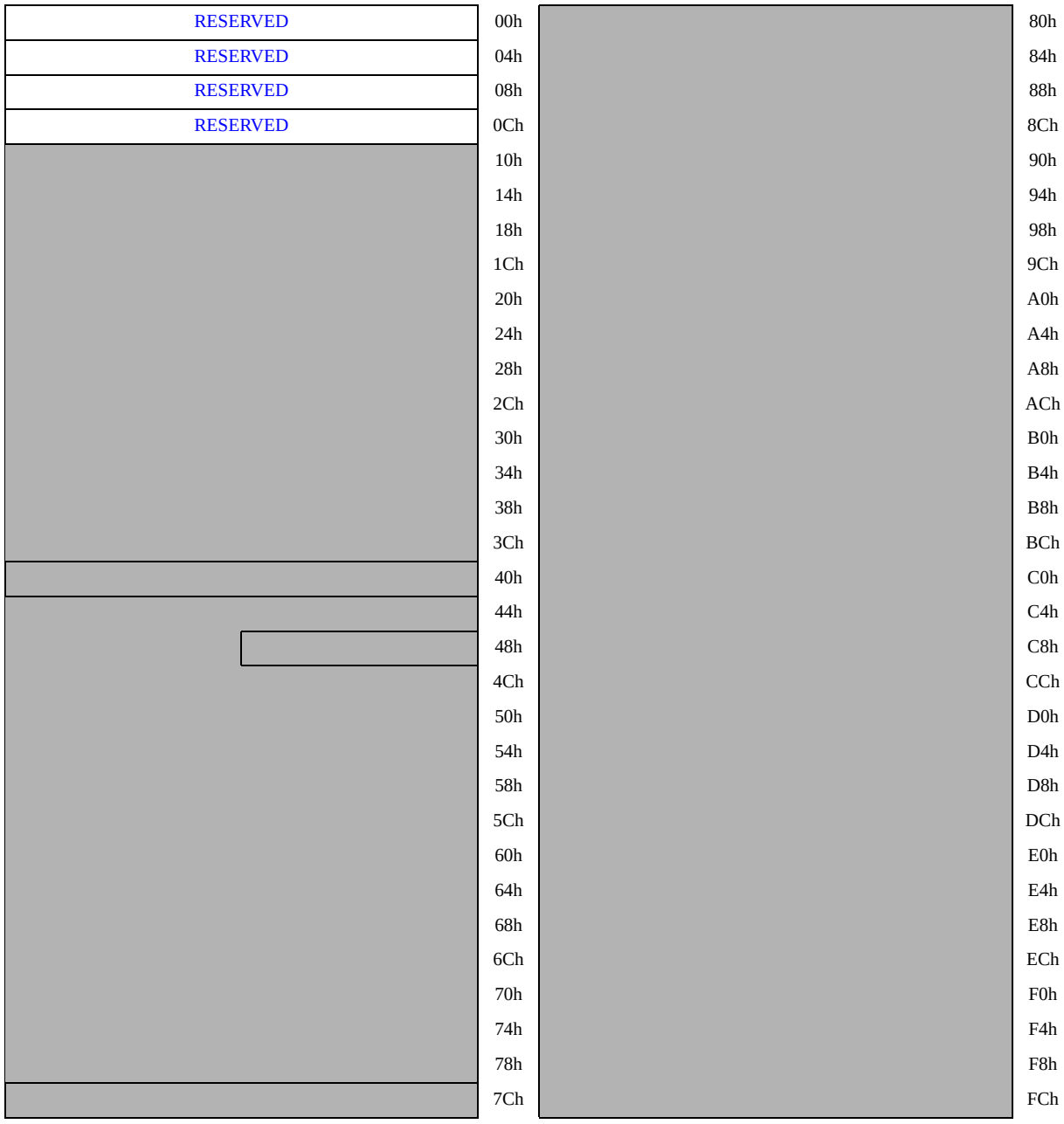
Table 11.9 — Function 5: DFX Registers

RESERVED		00h		TRANSCTRL	80h
RESERVED		04h			84h
RESERVED		08h			88h
RESERVED		0Ch			8Ch
		10h			90h
		14h			94h
		18h			98h
		1Ch			9Ch
		20h			A0h
		24h			A4h
		28h			A8h
		2Ch			ACh
		30h			B0h
		34h			B4h
		38h	LAI		B8h
TRANSCFG		3Ch	**SBMA**TCH**U**		BCh
TRANDERR1	TRANDERR0	40h	**SBMA**TCH**L0**		C0h
TRANDERR3	TRANDERR2	44h	SBMATCHL1		C4h
TRANDERR5	TRANDERR4	48h	SBMATCHL2		C8h
TRANDERR7	TRANDERR6	4Ch	**SBMASKU**		CCh
	TRANDERR8	50h	**SBMA**SKL0		D0h
		54h	SBMASKL1		D4h
		58h	SBMASKL2		D8h
		5Ch		MMEVENTSEL	DCh
		60h	**EVENTSEL0**		E0h
		64h	EVENTSEL1		E4h
		68h	EVENTSEL2		E8h
		6Ch			ECh
		70h	EVENT		F0h
		74h	EVBUS		F4h
		78h			F8h
		7Ch	STUCKL	EICNTL	FCh

Table 11.10 — Function 6: IBIST, Bring-up and Debug Registers

RESERVED	00h	**SBFIBPORTCTL**	80h
RESERVED	04h	**SBFIBPGCTL**	84h
RESERVED	08h	**SBFIBPATTBUF1**	88h
RESERVED	0Ch	**SBFIBTXMSK**	8Ch
	10h	**SBFIBRXMSK**	90h
	14h	**SBFIBTXSHFT**	94h
	18h	**SBFIBRXSHFT**	98h
	1Ch	**SBFIBRXLNERR**	9Ch
	20h	**SBFIBPATTBUF2**	A0h
	24h	SBFIBPATTBUF2EN	A4h
	28h		A8h
	2Ch		ACh
	30h	SBFIBINIT	B0h
	34h	SBIBISTMISC	B4h
	38h		B8h
	3Ch		BCh
	40h	**NBFIBPORTCTL**	C0h
	44h	**NBFIBPGCTL**	C4h
	48h	**NBFIBPATTBUF1**	C8h
	4Ch	**NBFIBTXMSK**	CCh
	50h	**NBFIBRXMSK**	D0h
	54h	**NBFIBTXSHFT**	D4h
	58h	**NBFIBRXSHFT**	D8h
	5Ch	**NBFIBRXLNERR**	DCh
	60h	**NBFIBPATTBUF2**	E0h
	64h	NBFIBPATTBUF2EN	E4h
	68h		E8h
	6Ch		ECh
	70h	NBFIBINIT	F0h
	74h	NBIBISTMISC	F4h
	78h		F8h
	7Ch		FCh

Table 11.11 — Functions 7: FBD DFX/Defeature Registers



11.2 PCI Standard Header Identification Registers (Function 0)

11.2.1 VID: Vendor Identification Register

This register identifies the manufacturer of the AMB.

Function: 0 Offset:00h			
Bit	**Attr**	**Default**	**Description**
15:0	RO	VID	**Vendor Identification Number** Manufacturer's PCI ID number

11.2.2 DID: Device Identification Register

These registers combined with the vendor identification register uniquely identifies the AMB Devices.

Function: 0 Offset:02h			
Bit	**Attr**	**Default**	**Description**
15:0	RO	DID	**Device Identification Number** Identifies each function of the AMB

11.2.3 RID: Revision Identification Register

This register contains the revision number of the AMB.

Function:0 Offset:08h			
Bit	**Attr**	**Default**	**Description**
7:0	RO	RID	**Revision Identification Number**: RID Identifies this revision of AMB

11.2.4 CCR: Class Code Register

This register contains the Class Code for the AMB, specifying the device function.

Function: 0 Offset:09h			
Bit	**Attr**	**Default**	**Description**
23:16	RO	05h	**Base Class**. This field indicates the general device category. For the AMB, this field is hardwired to 05h, indicating it is a "memory controller".
15:8	RO	00h	Sub-Class. This field qualifies the Base Class, providing a more detailed specification of the device function. For the AMB, this field is hardwired to 00h, indicating it is a "RAM".
7:0	RO	00h	Register-Level Programming Interface. This field identifies a specific programming interface (if any), that device independent software can use to interact with the device. There are no such interfaces defined for "memory controllers".

11.2.5 HDR: Header Type Register

This register identifies the header layout of the configuration space.

Function: 0 **Offset:0Eh**			
Bit	**Attr**	**Default**	**Description**
7	RO	1	Multi-function Device. Selects whether this is a multi-function device, that may have alternative configuration layouts. The AMB has more than the 256 bytes of configuration registers allotted to a single function. Therefore, the AMB is defined to be a multifunction device, and this bit is hardwired to 1.
6:0	RO	00h	Configuration Layout. This field identifies the format of the 10h through 3Fh space. The AMB uses header type “00”: these bits are hardwired to 00h.

11.3 FBD Link Registers (Function 1)

11.3.1 FBD Link Control and Status

11.3.1.1 FBDS0: FBD Status 0

This register contains copies of status bits returned by the AMB in the most recent northbound status frame when SYNC command R[1:0] field is 2’b00.

In the absence of SYNCs to this register, this register is not updated.

Function:1 **Offset:40h**			
Bit	**Attr**	**Default**	**Description**
7:5	RV	0h	Reserved
4	RO	0h	SP: Parity: This bit contains an odd parity bit that covers the S[3:0] field.
3	RO	0h	**S3: Northbound Debug Event** (1 = asserted, 0 = inactive): This bit is used to communicate debug events to the host.
2:1	RO	0h	**S[2:1]: Thermal Trip:** This field indicates various thermal conditions of the AMB as follows: • 00 – Below TEMPLO • 01 – Above TEMPLO • 10 – Above TEMPMID and falling • 11 – Above TEMPMID and rising The TEMPLO threshold is generally used to inform the host to accelerate refresh events. The TEMPMID threshold is generally used to inform the host that a thermal limit has been exceeded and that thermal throttling is needed. Refer to the RAS chapter for more details on thermal management.
0	RO	0h	S0: ERROR Asserted: This bit indicates an error has been detected by the AMB. Errors can be alert or other type.

11.3.1.2 FBDS1: FBD Status 1

This register contains copies of status bits returned by the AMB in the most recent northbound status frame when SYNC command R[1:0] field is 2'b01.

Function:1 Offset:41h			
Bit	**Attr**	**Default**	**Description**
7:5	RV	0h	Reserved
4	RO	0h	SP: Parity: This bit contains an odd parity bit that covers the S[3:0] field.
3:1	RV	0h	Reserved
0	RO	0h	S0: Data Merge Error: This bit indicates that the northbound data merge alignment logic of an intermediate AMB cannot met the timing required to merge its DRAM data into the northbound data stream when required. Refer to the initialization chapter for details.

11.3.1.3 FBDS2: FBD Status 2

This register contains copies of status bits returned by the AMB in the most recent northbound status frame when SYNC command R[1:0] field is 2'b10

Function:1 Offset:42h			
Bit	**Attr**	**Default**	**Description**
7:5	RV	0h	Reserved
4	RO	0h	SP: Parity: This bit contains an odd parity bit that covers the S[3:0] field.
3:0	RV	0h	Reserved

11.3.1.4 FBDS3: FBD Status 3

This register contains copies of bits that were returned by the AMB in the most recent northbound status frame when the SYNC command R[1:0] field is 2'b11. This can also be written with an override value that will be returned if selected during SYNC command.

Function:1 Offset:43h			
Bit	**Attr**	**Default**	**Description**
7:6	RV	0h	Reserved
5	RW	0h	OVREN: Use values written by user. Setting this bit causes the values specified in the lower 5 bits of this register returned as-is if requested by SYNC command.
4	RW	1h	USRPAR: User Specified parity for USRVAL
3:0	RW	0h	USRVAL: User Specified value

11.3.1.5 MODES: Operating Mode

This register contains overview configuration status of chip.

Function:1 Offset:5Ch			
Bit	**Attr**	**Default**	**Description**
7	RO	1	NORMAL: • 1 = Normal AMB Buffer
6	RO	0	LAI: • 1 = LAI
5	RO	0	REPEATER: • 1 = Repeater
4	RO	0	TRANSPARENT: • 1 = Transparent Test Mode
3:0	RV	0	Reserved

11.3.1.6 FEATURES: Capabilities

This register reports optional capabilities of this DIMM.

Function:1 **Offset:60h**			
Bit	**Attr**	**Default**	**Description**
31:15	RV	0h	Reserved
14:11	RO	Vendor Specific	DDRFREQ: DDR2 frequencies supported • 1XXX = reserved • X1XX = DDR2-800 • XX1X = DDR2-667 • XXX1 = DDR2-533
10	RO	Vendor Specific	VARLAT: Variable Read Latency Mode • 1 = Support Variable Read Latency on data returns • 0 = Not supported
9	RO	Vendor Specific	LAI: Logic Analyzer Interface Mode • 1 = Support remapping DDR interface as Logic Analyzer Interface • 0 = Not supported
8	RO	Vendor Specific	DMASK: Data Mask for non-ECC Write Data • 1 = Support data mask with non-ECC Write • 0 = Not supported
7	RO	Vendor Specific	L0S: Low Power Link State • 1 = Support L0s state • 0 = Not supported
6:2	RO	Vendor Specific	NBWC: Northbound Width Capability • 1XXXX = 14 bits NB width supported • X1XXX = 14bits fail over to 13 bits mode supported. • XX1XX = 13 bits NB width supported • XXX1X = 13 bits fail over to 12 bits mode supported. •
1:0	RO	Vendor Specific	SBWC: Southbound Width Capability • X1 = 10 SB bits: Device supports 10-bits and 10-bit fail-over to 9-bits. Both configurations deliver 72-bits of data payload frame. 1X = Reserved

11.3.1.7 FBDLIS: FBD Link Initialization Status

This register reports GB AMB FBD initialization status and is only valid when the link is up since it is not sticky.

Function:1
Offset:64h

Bit	Attr	Default	Description
31:20	RV	0	Reserved
19	RO	0	DATAMERGEERROR: NorthBound Data Merge Error • 1 = NB merge error
18	ROST	0	**NBMERGEDIS: NorthBound Merge Disable** Set by TS2 packet addressed to it • 1 = Disable NB merge • Note: state in AMB should be sticky through fast link reset until new TS2 resets bit or hard pin reset
17:12	RO	3Fh	NBWCFG: Northbound width configuration set by TS3 • See table in *FBD Channel Specification* for full decoding • [5:4] = Selects 14, 13 or 12 lane operation. • [3:0] - Selects none or one lane to map out
11:8	RO	Fh	SBWCFG: Southbound width capability set by TS3 • See Table in *FBD Channel Specification* for full decoding • [3:0] - Selects none or one lane to map out
7	RV	0	Reserved
6	RO	0	**TS2RESP:** Responded to a TS2 packet addressed to it 1: TS2 was addressed to this AMB • In polling mode - DS matches TS2 AMB_ID value • Undefined in other states
5	RO	0	SB2NBLBMAP: Specifies if upper or lower SB lanes are reflected in TS1 Valid only during testing phase (TS1) 1 = upper SB bit lanes 0 = lower SB lanes
4	RO	0	LASTAMBFLAG: Indicates if this AMB is acting like the last AMB • In Disable, Calibrate - always 0. • In training - Set if DS matches TS0 AMB_ID value • Retains value after training till next reset.
3:0	RO	0h	**LINITST: Link initialization state** Encoding is • 0000 - Disable • 0001 - Calibrate • 0010 - Training • 0011 - Testing • 0100 - Polling • 0101 - Config • 0110 - L0 • 0111 - L0s • 1000 - Recalibrate

11.3.1.8 FBDSBCFGNXT: FBD SB Link Electrical Configuration

This register contains next settings of control bits to set link electrical parameters to match link length and frequency characteristics.

Note: The Margin Drive Strength settings are not to be used during normal function mode, and therefore do not have a corresponding CUR register. New margin settings only take effect after the channel comes out of fast reset (channel Electrical Idle). Transmitters are not required to dynamically adjust drive strengths on the fly. Desired voltage margin settings are loaded into FBDSBCFGNXT, function 1, offsets 54h when SBTXDRVMAR is HIGH, and SB transmitters will be driven accordingly.

Function:1 **Offset:54h**			
Bit	**Attr**	**Default**	**Description**
7:6	RV	0h	Reserved
5	RWST	0h	**SBTXDRVMAR: SB TRANSMIT MARGIN** '1' = margin drive strength '0' (default) = no change to normal drive strength
4:3	RWST	00b	**SBTXDRVCUR: SB TRANSMIT DRIVE STRENGTH** Normal drive strengths: (SBTXDRVMAR == 0) ‘11’ = Small ‘10’ = reserved ‘01’ = Regular ‘00’ = Large **SBTXDRVCUR:** Margin test drive strengths: (SBTXDRVMAR == 1) ‘11’ = 160 mv minimum ‘10’ = 250 mv minimum ‘01’ = 340 mv minimum ‘00’ = 430 mv minimum
2:1	RWST	10b	**SBTXDEEMP:** 00 = 0 dB 01 = 3.5dB 10 = 6dB 11 = 9.5dB
0	RWST	1b	**SBRESYNCEN:** ‘1’ = SB pass-thru data is in Re-sync mode ‘0’ = SB pass-thru is in Re-sample mode.

Optional feature "Timing Margin Test"

Receivers are not required to dynamically adjust error offset on the fly. New margin settings only take effect after the channel comes out of fast reset. Receivers are not required to dynamically adjust timing margin on the fly. Desired timing margin settings are loaded into FBDSBCFGNXT and FBDNBCFGNXT, function 1, offsets 5Ah and 5Bh. Refer to FB-DIMM Design for Test, Design for Validation (DFx) Specification v1.0 section 7.3 for details.

Function:1 **Offset:5Ah**			
Bit	**Attr**	**Default**	**Description**
7	RWST	0h	**SBRXMARPOL: SOUTHBOUND RECEIVER TIMING MARGIN POLARITY** Sets the southbound receiver margin error polarity 0 = early 1 = late
6:0	RWST	0h	**SBRXMAROFF: SOUTHBOUND RECEIVER TIMING MARGIN OFFSET** This field sets the magnitude of the timing sampling error applied to the SB receiver. A minimum implementation requires 6:4 to be implemented. Specific implementations may choose to implement additional error offset granularity using some or all of bits 3:0. '1111111' = full error '0000000' = zero error all other values will provide binary monotonic error insertion between zero and full sampling error

11.3.1.9 FBDNBCFGNXT: FBD NB Link Electrical Configuration

This register contains next settings of control bits to set link electrical parameters to match link length and frequency characteristics.

Note: The Margin Drive Strength settings are not to be used during normal function mode, and therefore do not have a corresponding CUR register. New margin settings only take effect after the channel comes out of fast reset (channel Electrical Idle). Transmitters are not required to dynamically adjust drive strengths on the fly. Desired voltage margin settings are loaded into FBDNBCFGNXT, function 1, offsets 55h when NBTXDRVMAR is HIGH, and NB transmitters will be driven accordingly

Function:1 **Offset:55h**			
Bit	**Attr**	**Default**	**Description**
7:6	RV	0h	Reserved
5	RWST	0h	**NBTXDRVMAR: NB TRANSMIT MARGIN** '1' = margin drive strength '0' (default) = no change to normal drive strength
4:3	RWST	00b	**NBTXDRVCUR: NB TRANSMIT DRIVE STRENGTH** Normal drive strengths: (NBTXDRVMAR == 0) ‘11’ = Small ‘10’ = reserved ‘01’ = Regular ‘00’ = Large **NBTXDRVCUR:** Margin test drive strengths: (NBTXDRVMAR == 1) ‘11’ = 160 mv minimum ‘10’ = 250 mv minimum ‘01’ = 340 mv minimum ‘00’ = 430 mv minimum
2:1	RWST	10b	**NBTXDEEMP:** 00 = 0 dB 01 = 3.5dB 10 = 6dB 11 = 9.5dB
0	RWST	1b	**NBRESYNCEN:** ‘1’ = NB pass-thru data is in Re-sync mode ‘0’ = NB pass-thru is in Re-sample mode.

Optional feature "Timing Margin Test"

Receivers are not required to dynamically adjust error offset on the fly. New margin settings only take effect after the channel comes out of fast reset. Receivers are not required to dynamically adjust timing margin on the fly. Desired timing margin settings are loaded into FBDSBCFGNXT and FBDNBCFGNXT, function 1, offsets 5Ah and 5Bh. Refer to FB-DIMM Design for Test, Design for Validation (DFx) Specification v1.0 section 7.3 for details.

Function:1 **Offset:5Bh**			
Bit	**Attr**	**Default**	**Description**
7	RWST	0h	**NBRXMARPOL: NORTHBOUND RECEIVER TIMING MARGIN POLARITY** Sets the northbound receiver margin error polarity 0 = early 1 = late
6:0	RWST	0h	**NBRXMAROFF: NORTHBOUND RECEIVER TIMING MARGIN OFFSET** This field sets the magnitude of the timing sampling error applied to the NB receiver. A minimum implementation requires 6:4 to be implemented. Specific implementations may choose to implement additional error offset granularity using some or all of bits 3:0. '1111111' = full error '0000000' = zero error all other values will provide binary monotonic error insertion between zero and full sampling error

11.3.1.10 LINKPARNXT: FBD Link Frequency

This register contains current settings of control bits to set link electrical parameters to match link length and frequency characteristics.

Function:1 **Offset:56h**			
Bit	**Attr**	**Default**	**Description**
15:2	RV	0h	Reserved
1:0	RWST	00b¡@¡@	CFREQ: Current Link Frequency • 11 = DDR2-800 • 10 = DDR2-667 • 01 = DDR2-533 • 00 = Uninitialized

11.3.1.11 FBDSBCFGCUR: FBD SB Link Electrical Configuration

This register contains current settings of control bits to set link electrical parameters to match link length and frequency characteristics.

Function:1 **Offset:50h**			
Bit	**Attr**	**Default**	**Description**
7:5	RV	0h	Reserved
4:3	ROST	00b	**SBTXDRVCUR:** ‘11’ = Small ‘10’ = reserved ‘01’ = Regular ‘00’ = Large
2:1	ROST	10b	**SBTXDEEMP:** 00 = 0 dB 01 = 3.5dB 10 = 6dB 11 = 9.5dB
0	ROST	1	**SBRESYNCEN:** ‘1’ = SB pass-thru data is in Re-sync mode ‘0’ = SB pass-thru is in Re-sample mode.

11.3.1.12 FBDNBCFGCUR: FBD NB Link Electrical Configuration

This register contains current settings of control bits to set link electrical parameters to match link length and frequency characteristics.

Function:1 Offset:51h			
Bit	**Attr**	**Default**	**Description**
7:5	RV	0h	Reserved
4:3	ROST	00	**NBTXDRVCUR:** ‘11’ = Small ‘10’ = reserved ‘01’ = Regular ‘00’ = Large
2:1	ROST	10b	**NBTXDEEMP:** 00 = 0 dB 01 = 3.5dB 10 = 6dB 11 = 9.5dB
0	ROST	1	**NBRESYNCEN:** ‘1’ = NB pass-thru data is in Re-sync mode ‘0’ = NB pass-thru is in Re-sample mode.

11.3.1.13 LINKPARCUR: FBD Link Frequency

This register contains current settings of control bits to set link electrical parameters to match link length and frequency characteristics

Function:1 Offset:52h			
Bit	**Attr**	**Default**	**Description**
15:2	RV	0h	Reserved
1:0	ROST	01	CFREQ: Current Link Frequency • 11 = DDR2-800 • 10 = DDR2-667 • 01 = DDR2-533 • 00 = Reserved

11.3.1.14 FBDLOCKTO: FBD Bit Lock Time Out Register

This register contains .

Function:1 **Offset:68h**			
Bit	**Attr**	**Default**	**Description**
15:2	RWST	0594h	BLTOCNT: Bit Lock Time Out Counter default:: 1428 frames
1:0	RWST	0h	NBLINKCFG: Norht bound Link Config 00 = 14 lane 01 = 13 lane 10 = 12 lane 11 = reserved

11.3.1.15 FBDHAC: FBD Hot Add Control

This register contains control to aid in hot add functionality.

Function:1 **Offset:6Ch**			
Bit	**Attr**	**Default**	**Description**
7:2	RV	0	Reserved
1	RO	0	NB_DATA_ALL_ONES_FLAG: • 1 = Receiving ones on sufficient NB lanes to support init • 0 = Not receiving calibrate handshake on NB Rx
0	RW	0	DRIVE_ONES_SB: • 1 = Enable SB Tx Outputs and drive one's • 0 = Normal operation

11.3.1.16 RECALDUR: FBD Recalibrate Duration

This register determines the duration of the Recalibration state between 32 and 42 frames. During recalibration state all commands and CRC are ignored.

Function:1 Offset:70h			
Bit	**Attr**	**Default**	**Description**
7	RV	0	Reserved
6:1	RW	0h	Recalibrate_Duration: This field sets the duration of the Recalibrate state once a sync command with the ERC bit. set is received. Legal values are between 32 and 42. Functionality if set outside this range is undefined. • > ‘42d (101010b) = undefined • = ‘42d (101010b) = ignore for 42 frames after Sync • .... • = 32d (100000b) = ignore for 32 frames after Sync • <32d (100000b) = undefined
0	RV	0	Reserved

11.3.1.17 L0SDUR: FBD L0S State Duration

This register determines the duration of the L0s state between 32 and 42 frames.

Function:1 Offset:74h			
Bit	**Attr**	**Default**	**Description**
7	RV	0	Reserved
6:1	RW	0h	L0s_Duration: This field sets the duration of the L0s state once a sync command with the EL0s bit. set is received. Legal values are between 32 and 42. Functionality if set outside this range is undefined. • > ‘42d (101010b) = undefined • = ‘42d (101010b) = ignore for 42 frames after Sync • .... • = 32d (100000b) = ignore for 32 frames after Sync • <32d (100000b) = undefined
0	RW	0b	L0s_Enable: When 1 L0s mode is enabled

11.3.1.18 SYNCTRAININT: SYNC Train Interval register

This register sets the typical spacing of sync commands on the link.

Function:1 **Offset:78h**			
Bit	**Attr**	**Default**	**Description**
7:0	RWST	2Ah	SyncTrainInt: This field sets the min spacing for sync cmds default value 42d (101010b) min value 32, max value=255

11.3.1.19 SBCALSTATUS: Southbound Calibration Status

This register contains the pass/fail information of the last calibration on a per lane basis for the southbound. The AMB is expected to log the information when it is asked to go through calibration. The register is always cleared when entering the calibration state. This register will be used for debug purposes.

Function:1 **Offset:7Ch**			
Bit	**Attr**	**Default**	**Description**
15:10	RV	0h	Reserved
9:0	RWST	0h	CALSTATUS: Calibration status 0 - Pass 1 - Fail **Note**: Read/Write for firmware debug purposes ONLY

11.3.1.20 NBCALSTATUS: Northbound Calibration Status

This register contains the pass/fail information of the last calibration on a per lane basis for the southbound. The AMB is expected to log the information when it is asked to go through calibration. The register is always cleared when entering the calibration state. This register will be used for debug purposes.

Function:1 **Offset:7Eh**			
Bit	**Attr**	**Default**	**Description**
15:14	RV	0h	Reserved
13:0	RWST	0h	CALSTATUS: Calibration status 0 - Pass 1 - Fail **Note**: Read/Write for firmware debug purposes ONLY

11.3.2 Error Registers

11.3.2.1 EMASK: Error Mask

This register masks errors in the FERR and NERR registers as well as disabling some types of error detection. A ‘0’ in any field enables that error. A ‘1’ in any field masks (disables) that error. Multiple bits can be set in this register. An enabled error sets error status, updates error logs, and generates link signals. A masked error does not affect error status, error logs, or link signals.

.

Function:1 Offset:8Ch			
Bit	**Attr**	**Default**	**Description**
31:6	RV	0	Reserved
5	RWST	1	INJERR: Error Injection has sourced an injected error bit in the status return field (optional)
4	RWST	1	INJALERT: Error Injection has sourced an injected alert error (optional)
3	RWST	0	FEWEDGES: tClk Training Violation (no sync cmd for 2x SYNCTRAININT - typically 84 frames)
2	RWST	1	OVERTEMP: Temp > TEMPHI and temp enabled
1	RWST	1	UNIMPLCFG: Unimplemented Configuration Address
0	RWST	0	CMDCRCERR: SB CRC Error

11.3.2.2 FERR: First Error

This register contains bits specifying which errors occurred first as related to the FBD channel.

Function:1 Offset:90h			
Bit	**Attr**	**Default**	**Description**
31:6	RV	0	Reserved
5	RWCST	0	INJERR: Error Injection has sourced an injected error bit in the status return field (optional)
4	RWCST	0	INJALERT: Error Injection has sourced an injected alert error (optional)
3	RWCST	0	FEWEDGES: tClk Training Violation (no sync cmd for2x SYNCTRAININT - typically 84 frames) Logs in RECFBD registers. Sends Alerts NB. Triggers auto self refresh SM. .
2	RWCST	0	OVERTEMP: Temp > TEMPHI and temp enabled Fatal. AMB shuts down.

Function:1 Offset:90h			
Bit	**Attr**	**Default**	**Description**
1	RWCST	0	UNIMPLCFG: Unimplemented Configuration Address Correctable. Logs in RECCFG* registers. AMB drops the command.
0	RWCST	0	CMDCRCERR: SB CRC Error Correctable. Logs in RECFBD registers. AMB drops the current command and sources alerts

11.3.2.3 NERR: Successive Error

This register is used to report successive errors. More than two bits can be set in this register. This register contains bits specifying which errors occurred as related to the FBD channel.

A first error may also cause a successive error to be logged in the NERR.

Function:1 Offset:94h			
Bit	**Attr**	**Default**	**Description**
31:6	RV	0	Reserved
5	RWCST	0	INJERR: Error Injection has sourced an injected error bit in the status return field (optional)
4	RWCST	0	INJALERT: Error Injection has sourced an injected alert error (optional)
3	RWCST	0	FEWEDGES: tClkTraining Violation (no sync cmd for 2x SYNCTRAININT - typically 84 frames) Logs in RECFBD registers. Sends Alerts NB. Triggers auto self refresh SM. .
2	RWCST	0	OVERTEMP: Temp > TEMPHI and temp enabled Fatal. AMB shuts down.
1	RWCST	0	UNIMPLCFG: Unimplemented Configuration Address Correctable. Logs in RECCFG* registers. Drops the command.
0	RWCST	0	CMDCRCERR: SB CRC Error Correctable. Logs in RECFBD registers. Drops the current command and sources alerts.

11.3.2.4 RECCFG: Configuration Register Error Log

This register contains the received address for an unimplemented configuration register access error. The contents of this register are only valid when the error that set this register is logged in the FERR or NERR register.

Function:1 **Offset:98h**			
Bit	**Attr**	**Default**	**Description**
15:13	RV	0	Reserved
12:10	RWST	0h	function: **Note**: Read/Write for firmware debug purposes ONLY
9:8	RWST	0h	size: 00 = one byte 01 = two bytes 10 = three bytes 11 = four bytes **Note**: Read/Write for firmware debug purposes ONLY
7:0	RWST	0h	register address: **Note**: Read/Write for firmware debug purposes ONLY

11.3.2.5 RECFBD[9:0]: FBD Error Log

.This register contains FBD frame data received that matches the logged frame error.

Captures {BC} from frame N and A from frame N+1 where

[11:8] = A[n+1]

[7:4] = C[n] slot

[3:0] = B[n] slot

The contents of this register are only valid when one of the errors that set this register is logged in the FERR register. The contents of this register should not change until the error indication is cleared from the FERR register.

Function:1 **Offset:AEh, ACh, AAh, A8h, A6h, A4h, A2h, A0h, 9Eh, 9Ch**			
Bit	**Attr**	**Default**	**Description**
15:12	RV	0	Reserved
11:0	RWST	0	FRMDATA: Frame data for lane n **Note**: Read/Write for firmware debug purposes ONLY

11.3.3 PERSONALITY BYTES loaded from the SPD

These bytes allow for AMB implementation specific settings to be loaded in an architected way by BIOS without BIOS being aware of specific AMB requirements. Each AMB vendor defines how these bytes should be loaded for the specific DIMM being built. The values to be loaded into these bytes are stored in the SPD EEPROM on the DIMM.

The first six bytes are required to be loaded into the AMB via SMBus before link initialization to allow for configuration information needed for robust link operation.

The remaining 8 bytes must be loaded before the FBD begins normal operation.

Usage of these bytes can include

- DDR electrical parameters to optimize performance on a given DIMM
  - e.g. DLL delay settings, various IO driver slew settings,
- Enable/disable of various optimizations that may have been included in the design but can be turned off if they are not needed on this DIMM or they have unanticipated side effects - e.g. power save modes, alternate clock recovery algorithms, ..
- Temperature Sensor offsets
- Internal clock domain phase offsets

11.3.3.1 PERSBYTE[13:0]NXT: Personality Bytes

Function:1 **Offset:BDh:B0h**			
Bit	**Attr**	**Default**	**Description**
7:0	RWST	0	PData: Personality Data Byte Implementation specific registers

11.3.3.2 PERSBYTE[13:0]CUR: Personality Bytes

Function:1 **Offset:BDh:B0h**			
Bit	**Attr**	**Default**	**Description**
7:0	ROST	0	PData: Personality Data Byte Implementation specific registers

11.3.4 Advanced Memory Buffer Hardware Configuration Registers

11.3.4.1 CMD2DATANXT: Next Value of Command to Data Delay

This register has the next value of the command to data delay. This will be used after the next fast reset. Value comes from SPD.

Function:1 **Offset:E8h**			
Bit	**Attr**	**Default**	**Description**
7:4	RWST	0h	**DLYFRMS: Number of frames** This specifies full frame delay part of the command to data delay. 0 - 9: Valid delays 10 - 15: Reserved
3:0	RWST	0h	**DLYFRAC: Fractional delay of command to data** This specifies fractional frame delay part of the command to data delay. 0 - 11: Specifies the delay in 1UI increments 12 - 15: Reserved

11.3.4.2 CMD2DATACUR: Current Value of Command to Data Delay

This register has the current value of the command to data delay.

Function:1 **Offset:E9h**			
Bit	**Attr**	**Default**	**Description**
7:4	ROST	0h	**DLYFRMS: Number of frames** This specifies full frame delay part of the command to data delay. 0 - 9: Valid delays 10 - 15: Reserved
3:0	ROST	0h	**DLYFRAC: Fractional delay of command to data** This specifies fractional frame delay part of the command to data delay. 0 - 11: Specifies the delay in 1UI increments 12 - 15: Reserved

11.3.4.3 C2DINCRNXT: Next Value of Command to Data Delay Increment

This register has the next value of the command to data incremental delay. This will be used after the next fast reset. This will be used by the last AMB to delay driving the data beyond that specified in the command to data delay.

Function:1 Offset:EAh			
Bit	**Attr**	**Default**	**Description**
7:2	RV	0h	Reserved
1:0	RWST	0h	**INCRDLY: Incremental Delay for command to data** 0 - 3: Specifies the incremental delay in frames

11.3.4.4 C2DINCRCUR: Current Value of Command to Data Delay Increment

This register has the current value of the command to data incremental delay. This will be used by the last AMB to delay driving the data beyond that specified in

Function:1 Offset:EBh			
Bit	**Attr**	**Default**	**Description**
7:2	RV	0h	Reserved
1:0	ROST	0h	**INCRDLY: Incremental Delay for command to data** 0 - 3: Specifies the incremental delay in frames

11.3.4.5 C2DDECRNXT: Next Value of Command to Data Delay Decrement

This register has the next value of the command to data decrement delay. This will be used after the next fast reset. This will only be used by AMBs supporting Variable Read Delay.

Function:1 Offset:ECh			
Bit	**Attr**	**Default**	**Description**
7:4	RV	0h	Reserved
3:0	RWST	0h	**DECFRMS: Number of frames** This specifies full frame decrease in the command to data delay of this DIMM. 0- 15: number of frames

11.3.4.6 C2DDECRCUR: Current Value of Command to Data Delay Decrement

This register has the current value of the command to data decrement delay. This is only valid on AMBs supporting Variable Read Delay.

Function:1 Offset:EDh			
Bit	**Attr**	**Default**	**Description**
7:4	RV	0h	Reserved
3:0	ROST	0h	**DECFRMS: Number of frames** This specifies full frame decrease in the command to data delay of this DIMM. 0- 15: number of frames

11.4 Implementation Specific FBD Registers (Function 2)

These registers are implementation specific.

11.5 DDR and Miscellaneous Registers (Function 3)

11.5.1 Memory BIST Registers

11.5.1.1 MBCSR: MemBIST Control

Architected MemBIST control interface.

Function:3 Offset:40h			
Bit	**Attr**	**Default**	**Description**
31	RWS	0	START: Start operation: 1 => Set this bit to begin MemBIST execution. 0 => Hardware will clear this bit when MemBIST execution is completed.
30	RW	0	PF: Fail/Pass indicator: Write to 0 when start MemBIST. Hardware will set to 1 when a failure is detected. 0 => Pass 1 => Fail **Note**: Read/Write for firmware debug purposes ONLY
29	RW	0	HALT: Halt on Error 0 => Operation will not halt due to a detected error. 1 => Operation will halt after read-compare data error is detected. MemBIST will complete the current transaction before halting. This may result in multiple errors being logged.

Function:3 **Offset:40h**			
Bit	**Attr**	**Default**	**Description**
28	RW	0	ABORT: Membist test abort. When test abort bit is set, MBCSR bit 31 (Start operation, RWS) needs to be set to "0" at the same time to avoid restarting MemBIST. 0 => Normal operation. 1 => Need to abort the test during Membist operation. If there is any following membist test after the abort test, bit [28] needs to be cleared. The Write to set MBCSR.abort must occure at least tRFC after the Write to set MBCSR.start. Otherwise subsequent MemBIST operations may fail. tRFC value is set in DAREFTC.trfc (Function3, offset70h, bit field 23:16).
27	RW	0	SPARE:
26:24	RW	000	ALGO: Embedded Algorithm selection: When Embedded algorithm is applied, please program the following bits at the same time. • I/ Select bit[5:4] for the initial command execution mode. Except for the Data Retention stepII for selecting "10: read only with data comparison", program "01: write only without data comparison" for the rest of algorithms. • II/ Program MBCSR bit[11:10] to select FastX, FastY, FastXY • III/Program proper start/end address registers and correspondent MTR value for DIMM type.Do not leave start and end address register as default "00" or the same value. Algorithm did not support single address mode. • IV/ Program MBCSR bit 14 to select failure address logger or failure bits location accumulator. Embedded Algorithm selection: 000 => No embedded algorithm is selected. Normal command will be executed from the selection of MBCSR bits field [5:4] 001 => Scan: ^ (WD1); ^(RD2); ^ (WI3); ^ (RI4) 010 => Undefined 011 => Data Retention Write or Init: ^ (WD1); 100 => Data Retention Read : ^ (RD2); 101 => Mats +: ^(WD1); ^(RD2, WI3); v(RI4, WD5); 110 => March C-: ^(WD1); ^(RD2, WI3); ^(RI4, WD5); v(RD6, WI7); v(RI8, WD9); v(RD10); 111 => Undefined
23:22	RV	00	Reserved

Function:3 **Offset:40h**			
Bit	**Attr**	**Default**	**Description**
21:20	RW	00	CS: CS[1:0] selection in MemBIST mode 01: select Rank 0 10: select Rank 1 00: Reserved 11: Reserved
19	RW	0	INVERT: Invert data pattern when data is written out to DRAM.
18:16	RW	000	FIXED: Fixed data pattern selection for MemBIST operation 000 => 0 001 => F 010 => A 011 => 5 100 => C 101 => 3 110 => 9 111 => 6
15	RW	0	ENABLE288: Enable 288 bits user defined pattern for memory fill write only. There is no data comparison, error logger functions for 288 bits user defined data. 0 => 144 bits user defined data pattern when MBCSR[9:8] selects user defined data. 1 => 288 bits user defined data pattern when MBCSR[9:8] selects user defined data.
14	RW	0	MBDATA: Selects use of MBDATA for error log field for LFSR, Circular Shift and user defined data modes. This field has no effect on fixed data patterns. 0 => use MBDATA0/1/2/3/8 for failure data bit location accumulator. 1 => use MBDATA0/1/2/3/8 to log 5 failure addresses .
13	RW	0	ABAR: MemBIST output address compliment for FastX, FastY, and FastXY. Whenever this bit is enabled, Bank, Row, Column address will be inverted on alternate addresses as described in the MemBIST chapter. 0 => Regular addressing 1 => Dynamic address inversion (see more description in MemBIST Chapt).
12	RW	0	ADIR: Address decode direction for FastX, Fast Y, FastXY 0 => Address increments 1 => Address decrements

Function:3 **Offset:40h**			
Bit	**Attr**	**Default**	**Description**
11:10	RW	00	FAST: Address sequencing 00 => addressing with XZY toggling (column->bank->row) 01 => Fast Y with fixed bank 10 => Fast X with fixed bank 11 => Fast XY with fixed bank
9:8	RW	00	DTYPE: Data type selection: 00 => Fixed data pattern, selected by MBCSR bits 18:16 01 => 144 or 288 bits user defined data 10 => Circular shift data 11 => LFSR data, seeded from 32 bit LFSR seed register. Circular shift data and LFSR data type should not be used for single address operation (ATYPE = 01).
7:6	RW	00	ATYPE: Address type 00 => Reserved 01 => Single physical address operation, contained in MBADDR row/ column/bank. 10 => start/end physical address range defined in MB_START_ADDR & MB_END_ADDR registers. • In FastX, FastY and FastXY modes, only the bank specified in MB_START_ADDR will be exercised. 11 => full address range of the DIMM as defined in MTR register which specifys the number of banks, rows, and columns. • In FastX, FastY and FastXY modes, only the bank 0 will be exercised. Full address test supports XZY addressing (column->bank->row) and fastX/fastY/fastXY .
5:4	RW	00	CMD: Command execution: 00 => Read only without data comparison 01 => Write only without data comparison 10 => Read with data comparison 11 => Write followed by Read with data comparison
3:0	RV	0	Reserved

11.5.1.2 MBADDR: Memory Test Address

The register is used by MemBIST only when testing to a single memory location.

(MBCSR.atype = 2b‘01)

Function:3 **Offset:44h**			
Bit	**Attr**	**Default**	**Description**
31:16	RWST	0000h	ROW: Row Address 15:0
15	RWST	0	SPARE:
14:3	RWST	0000h	COL: Column Address BL8[14:3] <==> DRAM Column Address 15:11,9:3 BL4[14:3] <==> DRAM Column Address 14:11,9:2
2:0	RWST	000	BA: Bank Address 2:0

11.5.1.3 MBDATA[9:0]: Memory Test Data

Function:3 **Offset:6Ch, 68h, 64h, 60h,5Ch, 58h, 54h, 50h,4Ch, 48h**			
Bit	**Attr**	**Default**	**Description**
31:0	RWST	0000h	DATA: see functional description below for definition by mode and register

Table 11.12 — Functional mapping of MemBIST data fields by test mode

			Description by mode (note: MBCSR.dtype, MBCSR.mbdata and MBCSR.enable288 select mode)				
Reg	**Bit**	**Offset**	**Fixed Data Pattern**	**144 bit User Defined Pattern**	**Circular Shift**	**LFSR**	**288 bit User defined pattern**
MBDATA9	31:0	6Ch	5th Fail address	User defined Late data [71:64] & Early data [71:64]	Word4 Circular shift data	LFSR random Late data [71:64] & Early data [71:64]	User defined Late data [71:64] (2nd burst data) & Early data [71:64] (2nd burst data)
MBDATA8	31:0	68h	Late data [71:64] & Early data [71:64] Failure bit location accumulator	5th Fail address Or Late data [71:64] & Early data [71:64] Failure bit location accumulator	5th Fail address Or Late data [71:64] & Early data [71:64] Failure bit location accumulator	5th Fail address Or Late data [71:64] & Early data [71:64] Failure bit location accumulator	User defined Late data [71:64] (1st burst data) & Early data [71:64] (1st burst data)
MBDATA7	31:0	64h	Fail address 4	User defined Late data [63:32]	DW3 Circular shift data	LFSR random Late data [63:32]	User defined Late data [63:32] (2nd burst data)
MBDATA6	31:0	60h	Fail address 3	User defined Late data [31:0]	DW2 Circular shift data	LFSR random Late data [31:0]	User defined Late data [31:0] (2nd burst data)
MBDATA5	31:0	5Ch	Fail address 2	User defined Early data [63:32]	DW1 Circular shift data	LFSR random Early data [63:32]	User defined Early data [63:32] (2nd burst data)
MBDATA4	31:0	58h	Fail address 1	User defined Early data [31:0]	DW0 Circular shift data	LFSR random Early data [31:0]	User defined Early data [31:0] (2nd burst data)
MBDATA3	31:0	54h	Late data [63:32] Failure bit location accumulator	Fail address 4 Or Late data [63:32] Failure bit location accumulator	Fail address 4 Or Late data [63:32] Failure bit location accumulator	Fail address 4 Or Late data [63:32] Failure bit location accumulator	User defined Late data [63:32] (1st burst data)
MBDATA2	31:0	50h	Late data [31:0] Failure bit location accumulator	Fail address 3 Or Late data [31:0] Failure bit location accumulator	Fail address 3 Or Late data [31:0] Failure bit location accumulator	Fail address 3 Or Late data [31:0] Failure bit location accumulator	User defined Late data [31:0]] (1st burst data)
MBDATA1	31:0	4Ch	Early data [63:32] Failure bit location accumulator	Fail address 2 Or Early data [63:32] Failure bit location accumulator	Fail address 2 Or Early data [63:32] Failure bit location accumulator	Fail address 2 Or Early data [63:32] Failure bit location accumulator	User defined Early data [63:32] (1st burst data)
MBDATA0	31:0	48h	Early data [31:0] Failure bit location accumulator	Fail address 1 Or Early data [31:0] Failure bit location accumulator	Fail address 1 Or Early data [31:0] Failure bit location accumulator	Fail address 1 Or Early data [31:0] Failure bit location accumulator	User defined Early data [31:0] (1st burst data)

* In the later half part of data burst length 8 test, 144 bits or 288 bits user-defined data pattern will be repeat as the same sequence of burst length 4.

11.5.1.3.1 MBDATA failure address mapping

To compress the failure address into 32 bits, bits that are always zero are removed from the logging. These removed bits include AutoPrecharge Column address [10] and least significant bits assumed by burst length.

Table 11.13 — MBDATA Failure Address register correspondence to DRAM address

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
2	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	see description below												
Bank			Row																Column and Chunk												

BL4: 1 bit chunk indicates the location of 2 failure burst data chunks.

The above Column plus Chunk is equal to DRAM column address as the following:

Table 11.14 — BL4 Column and Chunk correspondence to DRAM address

Register Bit Location	12	11	10	9	8	7	6	5	4	3	2	1	0	
DRAM Col Address	14	13	12	11	9	8	7	6	5	4	3	2		
Data Chunk													1	X

- where the auto-precharge address bit 10 is assumed zero
- since data is logged in 144 bits (two chunks), address bit zero is not needed

BL8: 2 bit chunk indicates the location of 4 failure burst data chunks.

The above Column plus Chunk is equal to DRAM column address as the following:

Table 11.15 — BL8 Column and Chunk correspondence to DRAM address

Register Bit Location	12	11	10	9	8	7	6	5	4	3	2	1	0	
DRAM Col Address	14	13	12	11	9	8	7	6	5	4	3			
Data Chunk												2	1	X

- where the auto-precharge address bit 10 is assumed zero
- since data is logged in 144 bits (two chunks), Data chunk address bit zero is not needed

11.5.1.4 MB_START_ADDR: Memory Test Start Address

MB_END_ADDR row and column address must be larger than MB_START_ADDR row and column address in either increasing or deceasing address mode.

During FastX, FastY and FastXY operation, only one memory bank will be selected. User should only define the desired bank in MB_START_ADDR[2:0]. MB_END_ADDR[2:0] is ignored.

This register is only used when MBCSR.atype = 2b’10, and when MBCSR.algo is non-zero.

Function:3 Offset:9Ch			
Bit	**Attr**	**Default**	**Description**
31:16	RWST	0000h	ROW: MemBIST Start Row Address 15:0
15	RV	0	Reserved
14:3	RWST	0000h	COL: MemBIST Start Column Address BL8 [14:3] <==> Column Address 15:11, 9:3 BL4 [14:3] <==> Column Address 14:11, 9:2
2:0	RWST	000	BA: MemBIST Start Bank Address 2:0

11.5.1.5 MB_END_ADDR: Memory Test End Address

This register is only used when MBCSR.atype = 2b'10, and when MBCSR.algo is non-zero.

Function:3 Offset:A0h			
Bit	**Attr**	**Default**	**Description**
31:16	RWST	0000h	ROW: MemBIST End Row Address 15:0
15	RV	0	Reserved
14:3	RWST	0000h	COL: MemBIST End Column Address BL8 [14:3] <==> Column Address 15:11, 9:3 BL4 [14:3] <==> Column Address 14:11, 9:2
2:0	RWST	000	BA: MemBIST End Bank Address 2:0

11.5.1.6 MBLFSRSED: Memory Test Circular Shift and LFSR Seed

Function:3 Offset:A4h			
Bit	**Attr**	**Default**	**Description**
31:0	RWST	0000h	DMBLFSRSED:MemBIST LFSR Seed This 32 bit register will be used as the initial data seed for LFSR or Circular shift data pattern.

11.5.1.7 MBFADDRPTR: Memory Test failure address pointer register

Function:3 Offset:A8h			
Bit	**Attr**	**Default**	**Description**
31:0	RWST	0000h	DMBFADDRPTR: This 32 bit register designates which MemBIST failures to log in the available failure address locations. The default value of this register is zero. It means MemBIST always starts logging on the first failure address. If it is programmed to hex A (10 in decimal), MemBIST will log failure addresses starting from the11th failure. The corresponding MB_ERR_DATA0 register will log corrupted data in the first designated failure address. Note: this register does not affect the MBDATA failure bit location accumulators.

11.5.1.8 MB_ERR_DATA00: Memory Test Error Data 0 Bytes [3:0]

Stores the first 32 bits of the 1st 144 bit failure data

Function:3 Offset:B0h			
Bit	**Attr**	**Default**	**Description**
31:0	RWST	0000h	DATA: Early failure data [31:0] **Note**: Read/Write for firmware debug purposes ONLY

11.5.1.9 MB_ERR_DATA01: Memory Test Error Data 0 Bytes [7:4]

Stores the second 32 bits of the 1st 144 bit failure data

Function:3 Offset:B4h			
Bit	**Attr**	**Default**	**Description**
31:0	RWST	0000h	DATA: Early failure data [63:32] **Note**: Read/Write for firmware debug purposes ONLY

11.5.1.10 MB_ERR_DATA02: Memory Test Error Data 0 Bytes [11:8]

Stores the third 32 bits of the 1st 144 bit failure data

Function:3 **Offset:B8h**			
Bit	**Attr**	**Default**	**Description**
31:0	RWST	0000h	DATA: Late failure data [31:0] **Note**: Read/Write for firmware debug purposes ONLY

11.5.1.11 MB_ERR_DATA03: Memory Test Error Data 0 Bytes [15:12]

Stores the fourth 32 bits of the 1st 144 bit failure data

Function:3 **Offset:BCh**			
Bit	**Attr**	**Default**	**Description**
31:0	RWST	0000h	DATA: Late failure data [63:32] **Note**: Read/Write for firmware debug purposes ONLY

11.5.1.12 MB_ERR_DATA04: Memory Test Error Data 0 Bytes [17:16]

Stores the last 16 bits of the 1st 144 bit failure data

Function:3 **Offset:C0h**			
Bit	**Attr**	**Default**	**Description**
15:0	RWST	0000h	DATA: Late failure data [71:64] & Early failure data [71:64] **Note**: Read/Write for firmware debug purposes ONLY

11.5.2 Memory Registers

11.5.2.1 DAREFTC: DRAM Auto-Refresh Timing and Control

Function:3 **Offset:70h**			
Bit	**Attr**	**Default**	**Description**
31:24	RV	0	Reserved
23:16	RWST	4Eh	TRFC: DRAM refresh period

Function:3 Offset:70h			
Bit	**Attr**	**Default**	**Description**
15	RW	0	AREFEN: auto-refresh enable **Note:** This bit can also be cleared by the AMB self-refresh FSM as described in section 3.5.1
14:0	RWST	0C30h	TREFI: DRAM refresh interval

11.5.2.2 DSREFTC: DRAM Self-Refresh Timing and Control

Function:3 Offset:74h			
Bit	**Attr**	**Default**	**Description**
23:17	RV	0	Reserved
16	RWST	1	**DISSREXIT**: Disable DRAM Self-Refresh Exit when the link comes up
15:8	RWST	56h	**TXSNR**: DRAM Self-Refresh Exit to Non-Read Command Timing
7:4	RWST	Fh	TRP: DRAM Precharge Timing
3	RV	0	Reserved
2:0	RWST	7h	**TCKE**: DRAM Minimum CKE Pulse Width

11.5.2.3 MTR: Memory Technology Register

This register provides a local definition of the organization of DIMMs.

Note: These registers shall be copied from the SPD.

Function:3 Offset:77h			
Bit	**Attr**	**Default**	**Description**
7	RV	0	*Reserved*
6	RWST	0	WIDTH: Technology – DRAM data width Define the data width of SDRAMs within these DIMM's 0 = x4 (4 bits wide) 1 = x8 (8 bits wide)

Function:3 Offset:77h			
Bit	**Attr**	**Default**	**Description**
5	RWST	0	NUMRANK: Technology – Number of Ranks Define the number of ranks within these DIMM's 0 = single ranked 1 = double ranked
4	RWST	0	NUMBANK: Technology – Number of Banks Define the number of banks within these DIMM's 0 = 4 banks 1 = 8 banks
3:2	RWST	00	NUMROW: Technology – Number of Rows Define the number of rows within these DIMM's 00 = 8,192 01 = 16,384 10 = 32,768 11 = 65,536
1:0	RWST	00	NUMCOL: Technology – Number of Columns Define the number of columns within these DIMM's 00 = 1,024 01 = 2,048 10 = 4,096 11 = 8,192

11.5.2.4 DRT: DRAM Timing Control

Function:3 Offset:78h			
Bit	**Attr**	**Default**	**Description**
31	RV	0	*Reserved*
30:29	RWST	00	TRAS: DRAM tRAS minimum required delay from active command to precharge command. Delay cycles based on JEDEC DDRII spec 45 ns for DDRII 400/533/667. Based on the latest JEDEC spec (JESD79-2, Sept 2003) for DDRII 800 MHz min tRAS is not defined yet. tRASMIN clocks delay: 00 => 18 for DDRII 800 MHz 01 => 15 for DDRII 667 MHz 10 => 12 for DDRII 533 MHz 11 => Reserved

Function:3 **Offset:78h**			
Bit	**Attr**	**Default**	**Description**
28:27	RWST	00	TRTP: DRAM cell internal read to precharge command delay. tRTP clocks delay: 00 => 2 01 => 3 10 => 4 11 => 5
26:24	RWST	000	BBRW: Back to Back Read-Write turn around. This field determines the minimum number of CMDCLK between Read-Write commands. The purpose of these 3 bits are to control the turnaround time on the DQ bus. Regular setting will be based on BL/2 + 2 tCK. BL4: tR2W = 4 tCK BL8: tR2W = 6 tCK Command clocks apart based on the following encoding: 000 => 10 001 => 9 010 => 8 011 => 7 100 => 6 101 => 5 110 => 4 111 => 3 (stress mode, not recommended)
23	RV	0	Reserved
22:20	RWST	000	BBWR: Back to Back Write-Read turn around. This field determines the minimum number of CMDCLK between Write-Read commands. The purpose of these 3 bits are to control the turnaround time on the DQ bus. Regular setting will be based on (CL-1)+BL/2+tWTR. Command clocks apart based on the following encoding: 000 => 12 001 => 11 010 => 10 011 => 9 100 => 8 101 => 7 110 => 6 111 => 5 (stress mode, not recommended
19	RV	0	Reserved

Function:3 Offset:78h			
Bit	**Attr**	**Default**	**Description**
18:16	RWST	000	TWR: Twr DRAM Write Recovery delay Overall delay clocks will be (CL+AL-1) +BL/2 + tWR from write command to precharge command. 000 => 9 001 => 8 010 => 7 011 => 6 100 => 5 101 => 4 110 => 3 111 => 2
15:12	RWST	0000	TRC: Trc DRAM activate to another activate delay 0000 => 26 0001 => 25 0010 => 24 0011 => 23 0100 => 22 0101 => 21 0110 => 20 0111 => 19 1000 => 18 1001 => 17 1010 => 16 1011 => 15 1100 => 14 1101 => 13 1110 => 12 1111 => 11
11:10	RWST	00	TRCD: Trcd DRAM RAS# to CAS# delay 00 => 6 01 => 5 10 => 4 11 => 3 If AL >= Trcd, Read/Write command will be issued right after ACT cycle.

Function:3 Offset:78h			
Bit	**Attr**	**Default**	**Description**
9:8	RWST	00	TRP: Trp DRAM RAS# to Precharge delay 00 => 6 01 => 5 10 => 4 11 => 3
7:0	RWST	00h	NOPCNT: Programmable NOP insertion (Device Deselect actually). Number of Nops will be inserted between read/write commands to slow down MemBIST activities. Up to 255 clocks NOPs can be programmed to insert delay between read/write commands. If NOPs delay is programmable less than the required DRAM timing, Overall NOP delay from command to command will not be seen.

11.5.2.5 DRC: DRAM Controller Mode Register

This register controls the mode of the DRAM Controller.

Function:3 Offset:7Ch			
Bit	**Attr**	**Default**	**Description**
31:30	RV	00	Reserved
29	RW	0	**INITDONE: Initialization Complete.** This scratch bit communicates software state from the AMB to BIOS. BIOS sets this bit to 1 after initialization of the DRAM memory array is complete. This bit has no effect on AMB operation.
28	RV	0	Reserved
27:24	RWST	0	CLKDIS: clock[3:0] output disable
23	RWST	0	SEQADDR: When set to 1 turns off address balancing to support DRAMs programmed for Sequential Burst Type
19:22	RV	00	Reserved
18	RWST	1	**ODTZ: On-Die Termination Strength**. “0” Disabled “1” Enabled
17	RWST	0	**HLDDIS**: command/address hold disable
16	RWST	0	**BALDIS**: command/address balancing disable
15	RW	0	**CADIS**: command/address output disable
14	RW	0	**CSDIS**: chip select output disable

Function:3 Offset:7Ch			
Bit	**Attr**	**Default**	**Description**
13	RW	0	**ODTDIS**: ODT output disable
12	RWST	1	**CKEFRCLOW**: CKE Force Low Forces CKE low. Must be cleared to enable normal DDR functionality. This bit overrides the CKE1 and CKE0 fields described below, and also overrides all channel commands and other hardware fuctions that would otherwise affect the state of the CKE outputs.
11	RW	0	**CKEDIS**: CKE output disable
10	RWST	0	CKE1: CKE output 1 control and status. Software can write to this bit to change the state of the CKE 1 output. Hardware will update this bit with the current status of the CKE1 output two core cycles after a channel command or other hardware function changes the state of the CKE1 output. ‘1’ = CKE1 pads asserted. ‘0’ = CKE1 pads de-asserted.
9	RWST	0	CKE0: CKE output 0 control and status. Software can write to this bit to change the state of the CKE 0 output. Hardware will update this bit with the current status of the CKE 0 output two core cycles after a channel command or other hardware function changes the state of the CKE 0 output. ‘1’ = CKE0 pads asserted. ‘0’ = CKE0 pads de-asserted.
8	RWST	0	**BL**: DRAM burst length. ‘1’ = bl8 ‘0’ = bl4
7:4	RWST	2h	**AL**: DRAM Additive Latency [3:0]
3:0	RWST	3h	**CL**: DRAM CAS Latency [3:0]

11.5.3 Thermal Sensor Registers

11.5.3.1 TEMPLO: Temperature Low Trip Point

Low trip point.

Function:3 Offset:80h			
Bit	**Attr**	**Default**	**Description**
7:0	RWST	FFh	TEMPLO: Low threshold trip point

11.5.3.2 TEMPMID: Temperature Mid Trip Point

Mid trip point.

Function:3 Offset:81h			
Bit	**Attr**	**Default**	**Description**
7:0	RWST	FFh	TEMPMID: Mid threshold trip point

11.5.3.3 TEMPHI: Temperature High Trip Point

High trip point.

Function:3 Offset:82h			
Bit	**Attr**	**Default**	**Description**
7:0	RWST	FFh	TEMPHI: High threshold trip point

11.5.3.4 UPDATED: Update Temp Diff Bit

Take new temperature sample and update the temp diff bit (INCREASING).

Function:3 Offset:83h			
Bit	**Attr**	**Default**	**Description**
7:1	RV	00h	reserved
0	RWS	0	UPDATE: Write ‘1’ = latch current temperature (TEMP) and update INCREASING bit of TEMPSTAT register; Automatically clears this bit to ‘0’ after INCREASING bit is updated; Write ‘0’ - no effect

11.5.3.5 TEMPSTAT: Thermal Sensor Status Register

This register controls and reports temperature status.

Function:3 **Offset:84h**			
Bit	**Attr**	**Default**	**Description**
7:6	RV	0	Reserved
5	RWST	0	NoAutoUpdate '1' = turns off update of temp stat values so that forced values written in by firmware are not overwritten '0' = trip registers automatically updated as normal
4	RW	0	**INCREASING** '1' = Temperature has increased since the last time UPDATE bit was set in UPDATED register. '0' = Temperature has not increased since the last time UPDATE bit was set in UPDATED register. This is reflected as the Rising/Falling value in the Thermal Trip field of northbound FBD status 0.
3	RWST	0	**OVERTEMPHI** '1' = Temperature is above or equal to TEMPHI.TRIP '0' = Temperature is below TEMPHI.TRIP
2	RWST	0	**OVERTEMPMID** '1' = Temperature is above or equal to TEMPMID.TRIP '0' = Temperature is below TEMPMID.TRIP This is reflected in the Thermal Trip value of northbound FBD status 0
1	RWST	0	**OVERTEMPLO** '1' = Temperature is above or equal to TEMPLO.TRIP '0' = Temperature is below TEMPLO.TRIP This is reflected in the Thermal Trip value of northbound FBD status 0
0	RWST	0	**TEMPHIENABLE** '1' = Allow OVERTEMPHI=1 to shut down the DDR channel, drop DDR commands, log an error, and take FBD links to EI. '0' = OVERTEMPHI=1 only logs an error.

Notes:

1. The OVERTEMPLO, OVERTEMPMID and OVERTEMPHIGH bits of the TEMPSTAT register are refreshed whenever TEMP has a new value. This is independent of the UPDATE bit in the UPDATED register.
2. TEMPSTAT[3:1] = 000, when temperature is below TEMPLO.TRIP.
3. TEMPSTAT[3:1] = 001, when temperature is above or equal to TEMPLO.TRIP but below TEMPMID.TRIP.
4. TEMPSTAT[3:1] = 011, when temperature is above or equal to TEMPMID.TRIP but below TEMPHIGH.TRIP.
5. TEMPSTAT[3:1] = 111, when temperature is above or equal to TEMPHIGH.TRIP

11.5.3.6 TEMP: Temperature A/D

Current temperature reading. This- 8-bit with 0.5 degree resolution is continuously and automatically kept up to date

Function:3 **Offset:85h**			
Bit	**Attr**	**Default**	**Description**
7:0	RO	00h	DEGREES: Current temperature - binary encode 0 - 127 degrees C

by AMB hardware.

11.6 Implementation Specific DDR Initialization and Calibration Registers (Function 4)

11.6.1 DDR Calibration

11.6.1.1 DCALCSR: DCAL Control and Status

Function:4 **Offset:40h**			
Bit	**Attr**	**Default**	**Description**
31	RWS	0	**START: Start Operation** When set to 1 by software, the operation selected by the dcalcsr.opcode is initiated. Hardware clears this bit when the operation is complete.
30:28	RW	0	**FAIL: Completion Status** 1xx = Fail, 0xx = Pass **Note**: Read/Write for firmware debug purposes ONLY
27:23	RV	00	Reserved
22:21	RW	00	CS: Rank select This field corresponds to the chip select outputs: CS[1:0]. Setting a bit in this field will cause the corresponding CS pin to drive low when commands are issued on the DDR bus. This field Applies to NOP, Refresh, Precharge all, and MRS/EMRS commands.
20:15	RV	00	Reserved
14:4	RW	000h	**OPMODS:** Operation modifiers
3:0	RW	0h	**OPCODE:** “0000” = NOP “0001” = Refresh “0010” = Pre-Charge “0011” = MRS/EMRS “0101” = Automatic DQS Delay Calibration “1100” = Automatic Receive Enable Calibration “1101” = Self-Refresh Entry All other settings are reserved

11.6.1.2 DCALADDR: DCAL Address Register

Function:4 Offset:44h			
Bit	**Attr**	**Default**	**Description**
31:0	RW	0000_0000h	**DCALADDR: DCAL Address and Other Information Based on Opcode.**

Table 11.16 — Functional Characteristics of DCALADDR (Sheet 1 of 2)

Bit	NOP, Refresh, Pre-Charge, MRS/ EMRS, and Self-Refresh Entry Commands intiated by DCALCSR
31	DRAM Address Bus 15:0
30	
29	
28	
27	
26	
25	
24	
23	
22	
21	
20	
19	
18	
17	
16	
15	
14	
13	
12	
11	
10	
9	
8	
7	
6	
5	
4	
3	

Table 11.16 — Functional Characteristics of DCALADDR (Sheet 2 of 2)

Bit	NOP, Refresh, Pre-Charge, MRS/ EMRS, and Self-Refresh Entry Commands intiated by DCALCSR
2	DRAM Bank Address Bus 2:0
1	
0	

11.6.1.3 S3RESTORE [15:0] : DDR State Restore

These registers contain implementation dependent state needed to recover connections to DRAMs left in self refresh without destroying data in the DRAMs. For example, these may contain calibration information for DDR IO drivers. BIOS will copy these registers into some form of stable storage prior to system standby then restore these registers after system wakes up.

Note: The functionality of the AMB S3 restore registers is design dependent. Some of the S3 restore registers may or may not be implemented depending the AMB design.

Function:4 **Offset:E0h - A4h**			
Bit	**Attr**	**Default**	**Description**
31:0	RWST	00	S3STATE:

11.6.1.4 DDR2ODTC: DDR2 DRAM On-Die Termination Control

The DDR2ODTC controls the behavior of the ODT output (one ODT output per command bus copy). There is a separate field to control the behavior for reads to rank0, reads to rank1, writes to rank0, and writes to rank1. Only the lsb of each field is used, and the msb has no effect. When an lsb of a field is set to one, the ODT pins will drive high, at the appropriate time relative to data on the DDR bus, when the selected transaction (read or write) is issued to the selected rank (0 or 1.) If a field is set to 0, the ODT output continues to drive low during the transaction, as it does during idle cycles.

Function:4 **Offset:FCh**			
Bit	**Attr**	**Default**	**Description**
7:6	RWST	0h	R1ODTWR: ODT control during writes to CS1 x1: ODT pins will drive high x0: ODT pins remain driving low
5:4	RWST	0h	R1ODTRD: ODT control during reads to CS1
3:2	RWST	0h	R0ODTWR: ODT control during writes to CS0
1:0	RWST	0h	R0ODTRD: ODT control during reads to CS0

11.7 DFX Registers (Function 5)

11.7.1 Transparent Mode Registers

11.7.1.1 TRANSCFG: Transparent Mode Configuration

This register enables and controls FBD DFX transparent mode features.

Function:5 **Offset:3Ch**			
Bit	**Attr**	**Default**	**Description**
31:29	RV	0h	Reserved
28	RWST	0	ENDOUT: enable data output on transparent data/status pins when set, output status when clear
27	RWST	0	LGFBITS: log bits that fail the compare when set, log raw read data when clear.
26	RWST	0	LGFFAIL: log first failure in any burst position.
25:24	RWST	00	BSTPOS: burst position to log data/failed bits from when LGFFAIL bit is not set. 0 = first burst in bl4 or bl8 mode 1 = last burst of bl4, second burst of bl8 2 = third burst of bl8 3 = last burst of bl8
23:20	RWST	0h	DRAMRD: byte of data bus selected to be output on transparent data/status pins when ENDOUT bit is set. 8= DQS 17 and DQS 8 7= DQS 16 and DQS 7 ... 0 = DQS 9 and DQS 0
19:16	RWST	0h	DRAMWR: byte of data bus selected to receive transparent write data, and byte of data bus to be compared against transparent read data. Fh = all bytes 8= DQS 17 and DQS 8 7= DQS 16 and DQS 7 ... 0 = DQS 9 and DQS 0
15:0	RWST	0000h	DFTDATA: default data for bytes not selected by the DRAMWR field. This field has early/even data in the upper 8 bits, and late/odd data in the lower 8 bits.

11.7.1.2 TRANDERR[8:0]: Transparent Mode Data Error Logs

This register stores data returned from DRAM byte groups on failing transparent mode tests.

Function:5 **Offset:50h, 4Eh, 4Ch, 4Ah, 48h,46h, 44h, 42h, 40h**			
Bit	**Attr**	**Default**	**Description**
15:8	RWST	00h	LATE_DATA: **Note**: Read/Write for firmware debug purposes ONLY
7:0	RWST	00h	EARLY_DATA: **Note**: Read/Write for firmware debug purposes ONLY

11.7.1.3 TRANSCTRL: Transparent Mode Control

This register enables and controls FBD DFX transparent mode features.

Function:5 **Offset:80h**			
Bit	**Attr**	**Default**	**Description**
7:1	RV	00h	Reserved
0	RWST	0	ENTRNSPMODE: Transparency Mode Enable 1 - Enables Transparency Mod

11.7.2 Logic Analyzer Interface (LAI) Registers

This block of registers describe the optional LAI mode for AMBs.

11.7.2.1 LAI: LAI Operation Modes

This register controls and reports theAMBs LAI mode and Qual controls.

Function:5 Offset:B8h			
Bit	**Attr**	**Default**	**Description**
31:16	RV	0000h	Reserved
15	RWST	0	**RAWMODE: data connected to LAI** 0: LAI outputs contain initialization state information **prior to L0S then lane data after L0S** 1: LAI outputs connected to FBD data inputs even though valid timing is not present
14	RV	0	Reserved
13	RWST	0	QUALMODE: Assert Qual for all non-filtered frames, or only assert Qual for all non-filtered frames between start and stop events. 0: Ignore Qual start/stop events 1: Assert Qual after a start event, and deassert Qual after a stop events
12	RWST	0	FILTERSYNC: Filter the frame (do not assert Qual) if the frame is a sync. 0: Disable sync filtering 1: Enable sync filtering
11:6	RV	00h	Reserved
5:0	RWST	3Fh	QUALPERIOD: Additional number of frames Qual remains asserted Power-on default to 63

11.7.2.2 SBMATCHU: Upper Southbound Match Register

This register sets the upper 8 bits of data match for three southbound commands..

Function:5 Offset:BCh			
Bit	**Attr**	**Default**	**Description**
31:24	RV	00h	Reserved
23:16	RWST	00h	**CMD2:** Upper 8 bits [39:32] of southbound command 2
15:8	RWST	00h	**CMD1:** Upper 8 bits [39:32] of southbound command 1
7:0	RWST	00h	**CMD0:** Upper 8 bits [39:32] of southbound command 0

Match and Mask bit numbering of SB frames is as follows: -

- where N= 0 for slot A, 4 for slot B and 8 for slot C

Table 11.17 — Bit Locations for SB Match and Mask

Xfr\lane	9	8	7	6	5	4	3	2	1	0
0 + N	B36	B32	B28	B24	B20	B16	B12	B8	B4	B0
1 + N	B37	B33	B29	B25	B21	B17	B13	B9	B5	B1
2 + N	B38	B34	B30	B26	B22	B18	B14	B10	B6	B2
3 + N	B39	B35	B31	B27	B23	B19	B15	B11	B7	B3

11.7.2.3 SBMATCHL0: Lower Southbound Match Register 0

This register sets the lower 32 bits of data match for match southbound command 0.

Function:5 **Offset:C0h**			
Bit	**Attr**	**Default**	**Description**
31:0	RWST	00004000h	**CMD:** Lower 32bits [31:0] of southbound command power on default = match Synch

11.7.2.4 SBMATCHL1: Lower Southbound Match Register 1

This register sets the lower 32 bits of data match for match southbound command 1.

Function:5 **Offset:C4h**			
Bit	**Attr**	**Default**	**Description**
31:0	RWST	00100000h	**CMD:** Lower 32bits [31:0] of southbound command power on default = match Activate

11.7.2.5 SBMATCHL2: Lower Southbound Match Register 2

This register sets the lower 32 bits of data match for match southbound command 2.

Function:5 **Offset:C8h**			
Bit	**Attr**	**Default**	**Description**
31:0	RWST	00014000h	**CMD:** Lower 32bits [31:0] of southbound command power on default = match Write Config Reg

11.7.2.6 SBMASKU: Upper Southbound Mask Register

This register sets the upper 8 bits of data mask for three southbound commands.

Function:5 **Offset:CCh**			
Bit	**Attr**	**Default**	**Description**
31:24	RV	00h	Reserved
23:16	RWST	00h	**CMDMASK2:** Upper 8 bits [39:32] of southbound command 2 mask 0: Do not include this bit in match comparison 1: Include this bit in match comparison
15:8	RWST	00h	**CMDMASK1:** Upper 8 bits [39:32] of southbound command 1 mask 0: Do not include this bit in match comparison 1: Include this bit in match comparison
7:0	RWST	00h	**CMDMASK0:** Upper 8 bits [39:32] of southbound command 0 mask 0: Do not include this bit in match comparison 1: Include this bit in match comparison

11.7.2.7 SBMASKL0: Lower Southbound Mask Register 0

This register sets the lower 32 bits of data mask for match southbound command 0.

Function:5 **Offset:D0h**			
Bit	**Attr**	**Default**	**Description**
31:0	RWST	031FC000h	**CMDMASK:** Lower 32bits [31:0] of southbound command mask. 0: Do not include this bit in match comparison 1: Include this bit in match comparison power on default = match Sync

11.7.2.8 SBMASKL1: Lower Southbound Mask Register 1

This register sets the lower 32 bits of data mask for match southbound command 1.

Function:5 **Offset:D4h**			
Bit	**Attr**	**Default**	**Description**
31:0	RWST	00100000h	**CMDMASK:** Lower 32bits [31:0] of southbound command mask. 0: Do not include this bit in match comparison 1: Include this bit in match comparison power on default = match Activate

11.7.2.9 SBMASKL2: Lower Southbound Mask Register 2

This register sets the lower 32 bits of data mask for match southbound command 2.

Function:5 **Offset:D8h**			
Bit	**Attr**	**Default**	**Description**
31:0	RWST	001FC000h	**CMDMASK:** Lower 32bits [31:0] of southbound command mask. 0: Do not include this bit in match comparison 1: Include this bit in match comparison power on default = match Write Config Reg

11.7.2.10 MMEVENTSEL: Match/Mask Event Selection Register

Selects 1 of 13 local match events described below for promotion to local event select. Three local events MMEVENT[2:0] can be associated with one of these local match events..

Function:5 **Offset:DCh**			
Bit	**Attr**	**Default**	**Description**
15:12	RV	0h	Reserved
11:8	RWST	2h	MMEVENT2SEL: default: match pattern 0 to slot A only for sync
7:4	RWST	Ah	MMEVENT1SEL: default: match pattern 1 to slot A , B or C for activate
3:0	RWST	3h	MMEVENT0SEL: default: match pattern 2 to slot B only for write config reg

Table 11.18 — Local Mask and Match Events selected by MMEVENTnSEL fields

MM Event	Description
15:13	Reserved
12	**FRAMEMATCH** Bit pattern in slot A matches SBMATCH/SBMASK 0 **AND** Bit pattern in slot B matches SBMATCH/SBMASK 1 **AND** Bit pattern in slot C matches SBMATCH/SBMASK 2
11	**SLOTMATCH0** Command in slot A, B, or C matches SBMATCH/ SBMASK 0
10	**SLOTMATCH1** Command in slot A, B, or C matches SBMATCH/ SBMASK 1
9	**SLOTMATCH2** Command in slot A, B, or C matches SBMATCH/ SBMASK 2
8	**SLOTCMATCH0** Command in slot C matches SBMATCH/SBMASK 0
7	**SLOTCMATCH1** Command in slot C matches SBMATCH/SBMASK 1
6	**SLOTCMATCH2** Command in slot C matches SBMATCH/SBMASK 2
5	**SLOTBMATCH0** Command in slot B matches SBMATCH/SBMASK 0
4	**SLOTBMATCH1** Command in slot B matches SBMATCH/SBMASK 1
3	**SLOTBMATCH2** Command in slot B matches SBMATCH/SBMASK 2
2	**SLOTAMATCH0** Command in slot A matches SBMATCH/SBMASK 0
1	**SLOTAMATCH1** Command in slot A matches SBMATCH/SBMASK 1
0	**SLOTAMATCH2** Command in slot A matches SBMATCH/SBMASK 2

11.7.2.11 EVENTSEL0: Event Selection Register

·In LAI mode, selects 1 of 32 local events (see EVENT register) for 2 uses (Qual Start and Qual Stop) and sets programmable delay for QualStop. In Normal mode, selects local event for 2 uses (error injection and NB in-band event signaling) and sets programmable delay for error injection..

Function:5 **Offset:E0h**			
Bit	**Attr**	**Default**	**Description**
31:21	RV	00h	Reserved
20:15	RWST	3Fh	QUALSTOPDELAY: in LAI Mode Additional number of clocks QualStop is delayed before use (0 to 63) Power-on default to 63 INJERRORDELAY: in Normal Mode Additional number of clocks INJERROR is delayed before use (0 to 63) Power-on default to 63
14:10	RW	00h	INBAND: in LAI Mode No effect. Northbound in-band debug events can not be asserted in LAI mode INBAND: in Normal Mode If selected event occurs, assert the northbound in-band event bit in next sync status 0 return and in FBDS0.S3
9:5	RWST	00h	QUALSTART: in LAI Mode If selected event occurs, enable assertion of Qual until next QUALSTOP
4:0	RWST	00h	QUALSTOP: in LAI Mode • If selected event occurs, disable assertion of Qual until next QUALSTART INJERROR: in Normal Mode • If selected event occurs, inject error selected by EICNTL

11.7.2.12 EVENTSEL1: Event Selection Register

·Selects 1 of 32 local events (see EVENT register) for each of six events transmitted to the LAI interface (events[5:0]).

Function:5 **Offset:E4h**			
Bit	**Attr**	**Default**	**Description**
31:30	RV	00	Reserved
29:25	RWST	0Ah	LAITRIGGER5: Local event selected and transmitted to LAI as TRIGGER5 Default on power on to MM[1] event= Activate on any command
24:20	RWST	0Bh	LAITRIGGER4: Local event selected and transmitted to LAI as TRIGGER4 Default on power on to MM[2] event= Sync command in slot A
19:15	RWST	13h	LAITRIGGER3: Local event selected and transmitted to LAI as TRIGGER3 Default on power on to select in-band debug event 3
14:10	RWST	12h	LAITRIGGER2: Local event selected and transmitted to LAI as TRIGGER2 Default on power on to select in-band debug event 2
9:5	RWST	11h	LAITRIGGER1: Local event selected and transmitted to LAI as TRIGGER1 Default on power on to select in-band debug event 1
4:0	RWST	10h	LAITRIGGER0: Local event selected and transmitted to LAI as TRIGGER0 Default on power on to select in-band debug event 0

11.7.2.13 EVENTSEL2: Event Selection Register

Selects 1 of 32 local events (see EVENT register) for each of five events transmitted to the LAI interface (events[10:6]).

Function:5 **Offset:E8h**			
Bit	**Attr**	**Default**	**Description**
31:30	RV	00	Reserved
29:25	RV	00h	Reserved
24:20	RWST	04h	LAITRIGGER10: Local event selected and transmitted to LAI as TRIGGER10 Default on power on to SB Unit Testing State detect
19:15	RWST	1Ah	LAITRIGGER9: Local event selected and transmitted to LAI as TRIGGER9 Default on power on to SB CRC error detect
14:10	RWST	0Dh	LAITRIGGER8: Local event selected and transmitted to LAI as TRIGGER8 Default on power on to Event Bus[1] event
9:5	RWST	0Ch	LAITRIGGER7: Local event selected and transmitted to LAI as TRIGGER7 Default on power on to Event Bus[0] event
4:0	RWST	09h	LAITRIGGER6: Local event selected and transmitted to LAI as TRIGGER6 Default on power on to MM[0] event= Write Register in command slot B

11.7.2.14 EVENT: Local LAI Event Register

This register sets a bit if a local event is hit. Except for QUAL, event signal internal to theAMBwill only toggle one cycle when bit is set to avoid multiple triggers per event. The 5-bit encoding for the bit number is used by the EVENTSEL register to select the event corresponding to the bit number.

Function:5 **Offset:F0h**			
Bit	**Attr**	**Default**	**Description**
31	RWCST	0	Spare:
30:25	RWCST	00h	ERROR EVENTS: • SB/NB failover[25], when unmasked: • SB CRC error[26], • thermal overload[27], • clock training violation (< 6 transitions in 512 UI) [28], • unimplemented register access[29], • other implementation specific errors[30] set on event and cleared by writing
24	RWCST	0	QUALFLAG:
23:16	RWCST	00h	INBANDEV: SB link in-band EV[7:0] set on event and cleared by writing
15:12	RWCST	0h	EV: Event Bus EV[3:0] set on event and cleared by writing
11:9	RWCST	0h	MMEVENT: MMEVENT[2:0] selected by MMEVENTSEL set on event and cleared by writing
8:1	RWST	0h	LINKST: FBD Link State: Disable[1], calibrate[2], training[3], testing[4], pollling[5], config[6], l0[7], l0s or recalibrate[8] One hot encoding of FBD link state
0	RO	0	NULL: Null Event: Bit never set

11.7.2.15 EVBUS: Event Bus Control Register

EVBUS fields select 1 of 32 local events (see EVENT register) for output to the GBAMB event bus. EVTYPE sets up type of event for each event bus pin and EVT fields set event bus timing filters.

Function:5 **Offset:F4h**			
Bit	**Attr**	**Default**	**Description**
31:27	RWST	00h	EVBUS3: Local event selected for event bus [3]
26:22	RWST	00h	EVBUS2: Local event selected for event bus [2]
21:17	RWST	03h	EVBUS1: Local event selected for event bus [1] default on power-on = start of initialization as detected by Init Training State Event
16:12	RWST	17h	EVBUS0: Local event selected for event bus [0] default on power-on = In-band Debug Event 7 (23d)
11:8	RWST	0h	EVTYPE: 0 = pulse event 1 = level event bit 11 for EVBUS3 thru bit 8 for EVBUS0
7:0	RWST	0Fh	EVT1: Min delay after EVBus trigger out deasserted before next assertion allowed and same value is used for Pulse width used when asserting all EVBus outputs Power on default of 16 clks

11.7.3 Error Injection Registers

11.7.3.1 EICNTL: Error Injection Control

This register controls the AMBerror injection logic.

Function:5 Offset:FCh			
Bit	**Attr**	**Default**	**Description**
7	RW	0	**EIEN:Error Injection Enable** 1= Error Injection enabled 0= Error Injection disabled
6:4	RW	000	**EITYPE: Type of error injection** 111 = Reserved; 110 = Reserved 101 = Force NB Error bit on next Status return 100 = Force Alert on event 011 = Reserved 010 =Reserved 001= Corrupt NB CRC on event 000= No error injection
3:0	RV	0h	Reserved

11.7.3.2 STUCKL: Stuck “ON” FBD Lanes

This register selects FBD Lanes to be stuck at EI following next link reset.

Function:5 Offset:FEh			
Bit	**Attr**	**Default**	**Description**
7:4	RV	0h	Reserved
3:0	RWST	Fh	NBSTUCK: NB Lane to be driven to EI to simulate a failed lane • 0h = lane 0: Dh = lane 13 and > 13 = NOP

11.8 Bring-up and Debug Registers (Function 6)

11.8.1 Southbound FBD IBIST registers

11.8.1.1 SBFIBPORTCTL: Southbound FBD IBIST Port Control Register

This register controls the operation of the IBIST logic.

Device:NodeID
Function: 6
Offset:80h

Bit	Attr	Default	Description
31:24	RV	00h	Reserved
23	RWST	0	SBNBMAP: Loopback mapping bit This bit will be sent during TS1 to the slave to specify which lanes needs to be looped back. Actual lanes looped back is specified in the FBD Architecture Spec.
22	RWST	0	CMMSTR: Compliance Measurement Mode start This puts the IBIST logic in CMM mode and IBIST TX engine will start transmitting IBIST patterns.
21:12	RWCST	000h	ERRCNT: Error Counter Total number of errors encountered in this port.
11:8	ROST	0h	ERRLNNUM: Error Lane Number This points to the first lane that encountered an error. If more than one lane reports an error in a cycle, the most significant lane number that reported the error will be logged.
7:6	RWCST	00	ERRSTAT: Port Error Status When IBIST is started, status goes to 01 until first start delimiter is received and then goes to 00 until the end or to10 if an error occurs. 00: No error. 01: Did not receive first start delimiter. 10: Transmission error (first error). 11: Reserved for future use
5	RWST	0	AUTOINVSWPEN: Auto Inversion sweep enable This bit enables the inversion shift register to continuously rotate the pattern in the FIBTXSHFT and FIBRXSHFT registers. 0: Disable Auto-inversion 1: Enable Auto-inversions
4	RWST	0	STOPONERR: Stop IBIST on Error 0: Do not stop on error, only update error counter 1: Stop on error
3	RWST	0	LOOPCON: Loop forever 0: No looping 1: Loop forever
2	RWCST	0	COMPLETE: IBIST done flag 0: Not done 1: Done

Device:NodeID **Function: 6** **Offset:80h**			
Bit	**Attr**	**Default**	**Description**
1	RWST	0	MSTRMD: Master Mode Enable When this bit is set, during the next TS1 training set, IBIST will transmit patterns generated locally rather than looping back the incoming test data. 0: Disable Master mode. 1: Enable master mode.
0	RWST	0	IBISTR: IBIST Start When set, IBIST starts transmitting after the TS1 header is recognized during the next link initialization sequence. and **MSTRMD** bit is set.This bit also enables the receive engine to start looking for the start delimiter during TS1 training set. This bit is reset when IBIST is done. The IBIST transmitter can be stopped by setting this bit to 0. 0: Stop IBIST transmitter 1: Start IBIST transmitter

11.8.1.2 SBFIBPGCTL: SB IBIST Pattern Generator Control Register

This register contains bits to control the operation of the IBIST pattern generator. All counts are in 24 bit increments.

Device:NodeID **Function: 6** **Offset:84h**			
Bit	**Attr**	**Default**	**Description**
31:26	RWST	0Fh	OVRLOOPCNT: Overall Loop Count 0h: Reserved 1h:3Fh: Number of times to loop all the patterns.
25:21	RWST	00h	CNSTGENCNT: Constant Generator Loop Counter 00h: Disable constant generator output 01h: 1Fh The number of times the constant generator counter pattern should loop before going to the next component. Each count represents 24 bits of 1’s or 0’s.
20	RWST	0	CNSTGENSET: Constant Generator Setting 0: Generate 0 1: Generate 1
19:13	RWST	0Fh	MODLOOPCNT: Modulo-N Loop Counter Each count represents 24 bits of the pattern specified by **MODPERIOD**. 00h: Disable Pattern Output 01h: 7Fh The number of times the Pattern Buffer should loop before going to the next component.

Device:NodeID **Function: 6** **Offset:84h**			
Bit	**Attr**	**Default**	**Description**
12:10	RWST	001b	MODPERIOD: Period of the Modulo-N counter Each encoding transmits a 24-bit pattern as specified below. All other encodings are reserved. 001: L/2 - 0101_0101_0101_0101_0101_0101 010: L/4 - 0011_0011_0011_0011_0011_0011 011: L/6 - 0001_1100_0111_0001_1100_0111 100: L/8 - 0000_1111_0000_1111_0000_1111 110: L/24 - 0000_0000_0000_1111_1111_1111
9:3	RWST	0Fh	PATTLOOPCNT: Pattern Buffer Loop Counter 00h: Disable Pattern Output 01h: 7Fh The number of times the Pattern Buffer (**FIBPATTBUF1**) should be repeated before going to the next component.
2:0	RWST	000	PTGENORD: Pattern Generation Order 000: Pattern Store + Modulo N Cntr + Constant Generator 001: Pattern Store + Constant Generator + Modulo N Cntr 010: Modulo N Cntr + Pattern Store + Constant Generator 011: Modulo N Cntr + Constant Generator + Pattern Store 100: Constant Generator + Pattern Store + Modulo N Cntr 101: Constant Generator + Modulo N Cntr + Pattern Store 110: Reserved 111: Reserved

11.8.1.3 SBFIBPATTBUF1: SB IBIST Pattern Buffer 1 Register

This register contains the pattern bits used in IBIST operations. Only the least significant 24 bits are used.

Function: 6 **Offset:88h**			
Bit	**Attr**	**Default**	**Description**
31:24	RV	00h	Reserved
23:0	RWST	02ccfdh	IBPATBUF: IBIST Pattern Buffer Pattern buffer storing the default and the user programmable pattern. Default: 02ccfdh

11.8.1.4 SBFIBTXMSK: SB IBIST Transmitter Mask Register

This register enables IBIST operations for individual lanes. This mask only applies to transmitters and not receivers.

Function: 6 Offset:8Ch			
Bit	**Attr**	**Default**	**Description**
31:10	RV	000000h	Reserved
9:0	RWST	3FFh	TXMASK: Selects which channels to enable for testing.

11.8.1.5 SBFIBRXMSK: SB IBIST Receiver Mask Register

This register enables IBIST operations for individual lanes. This mask only applies to receivers and not transmitters.

Function: 6 Offset:90h			
Bit	**Attr**	**Default**	**Description**
31:10	RV	000000h	Reserved
9:0	RWST	3FFh	RXMASK: Selects which channels to enable for testing.

11.8.1.6 SBFIBTXSHFT: SB IBIST Transmitter Inversion Shift Register

Each bit in this register enables inverting the patterns that is driven on corresponding lanes. If AUTOINVSWPEN bit is set in port control register, the TXINVSHFT field is rotated left at the completion of each pattern buffer set.

Function: 6 Offset:94h			
Bit	**Attr**	**Default**	**Description**
31:10	RV	000000h	Reserved
9:0	RWST	3FFh	TXINVSHFT: Transmitter Inversion Shift Register.

11.8.1.7 SBFIBRXSHFT: SB IBIST Receiver Inversion Shift Register

Each bit in this register enables inverting the patterns that is received on corresponding lanes. If AUTOINVSWPEN bit is set in port control register, the RXINVSHFT field is rotated left at the completion of each pattern buffer set.

Function: 6 Offset:98h			
Bit	**Attr**	**Default**	**Description**
31:10	RV	000000h	Reserved
9:0	RWST	3FFh	RXINVSHFT: Receiver Inversion Shift Register.

11.8.1.8 SBFIBRXLNERR: SB IBIST Receiver Lane Error Status

This records the error status from each lane.

Function: 6 Offset:9Ch			
Bit	**Attr**	**Default**	**Description**
31:10	RV	000000h	Reserved
9:0	ROST	000h	RXERRSTAT: Receiver Error Status

11.8.1.9 SBFIBPATTBUF2: SB IBIST Pattern Buffer 2 Register

This register contains the pattern bits used in IBIST operations. Only the least significant 24 bits are used.

Function: 6 Offset:A0h			
Bit	**Attr**	**Default**	**Description**
31:24	RV	00h	Reserved
23:0	RWST	fd3302h	IBPATBUF2: IBIST Pattern Buffer 2 Pattern buffer storing the default and the user programmable pattern. Default: fd3302h

11.8.1.10 SBFIBPATT2EN: SB IBIST Pattern Buffer 2 Enable

This specifies which lanes will carry the pattern specified in SBFIBPATTBUFF2.

Function: 6 Offset:A4h			
Bit	**Attr**	**Default**	**Description**
31:10	RV	00h	Reserved
9:0	RWST	000h	SBFIBPATT2EN: IBIST Pattern Buffer 2 enable Per lane enable for driving pattern buffer 2.

11.8.1.11 SBFIBINIT: SB IBIST Initialization Register

This register control southbound IBIST Testing.

Function: 6 Offset:B0h			
Bit	**Attr**	**Default**	**Description**
31	RV	0	Reserved
30:21	RWST	0c8h	SBTS0CNT: Southbound TS0 Count Number of TS0 sequences to transmit.

20:13	RWST	01h	SBTS1CNT: Southbound TS1 Count Number of TS1 sequences to transmit.
12:3	RWST	100h	SBDISCNT: Southbound Disable State Count Number of cycles to remain in disable state.
2	RWST	1	SBCALIBEN: Southbound Calibration Enable 1 - Perform FBD Calibration.
1	RV	0	Reserved
0	RWST	0	SBIBISTINITEN: IBIST Initialization Enable 1 - Start IBIST Testing with Southbound Transmitter as the host.

11.8.1.12 SBIBISTMISC: SB IBIST Initialization Miscellaneous Register

This register control southbound IBIST Testing.

Function: 6 Offset:B4h			
Bit	**Attr**	**Default**	**Description**
31:24	RV	00h	Reserved
23:20	RWST	0h	AMBID: Value of the AMB ID field during TS0
19:0	RWST	61a80h	SBIBISTCALPERIOD: Number of cycles to drive 1 during Calibration

11.8.2 Northbound FBD IBIST registers

11.8.2.1 NBFIBPORTCTL: Northbound FBD IBIST Port Control Register

This register controls the operation of the IBIST logic.

Function: 6 Offset:C0h			
Bit	**Attr**	**Default**	**Description**
31:24	RV	00h	Reserved
23	RWST	0	SBNBMAP: Loopback mapping bit This bit will be sent during TS1 to specify to the slave which lanes needs to be looped back. Actual lanes looped back is specified in the FBD Architecture Spec.
22	RWST	0	CMMSTR: Compliance Measurement Mode start This puts the IBIST logic in CMM mode and IBIST TX engine will start transmitting IBIST patterns.
21:12	RWCST	000h	ERRCNT: Error Counter Total number of errors encountered in this port.

Function: 6 **Offset:C0h**			
Bit	**Attr**	**Default**	**Description**
11:8	ROST	0h	ERRLNNUM: Error Lane Number This points to the first lane that encountered an error. If more than one lane reports an error in a cycle, the most significant lane number that reported the error will be logged.
7:6	RWCST	00	ERRSTAT: Port Error Status When IBIST is started, status goes to 01 until first start delimiter is received and then goes to 00 until the end or to10 if an error occurs. 00: No error. 01: Did not receive first start delimiter. 10: Transmission error (first error). 11: Reserved
5	RWST	0	AUTOINVSWPEN: Auto Inversion sweep enable This bit enables the inversion shift register to continuously rotate the pattern in the FIBTXSHFT and FIBRXSHFT registers. 0: Disable Auto-inversion 1: Enable Auto-inversions
4	RWST	0	STOPONERR: Stop IBIST on Error 0: Do not stop on error, only update error counter 1: Stop on error
3	RWST	0	LOOPCON: Loop forever 0: No looping 1: Loop forever
2	RWCST	0	COMPLETE: IBIST done flag 0: Not done 1: Done
1	RWST	0	MSTRMD: Master Mode Enable When this bit is set, during the next TS1 training set, IBIST will transmit patterns generated locally rather than looping back the incoming test data. 0: Disable Master mode. 1: Enable master mode.
0	RWST	0	IBISTR: IBIST Start When set, IBIST starts transmitting after the TS1 header is recognized during the next link initialization sequence. and **MSTRMD** bit is set. This bit also enables the receive engine to start looking for the start delimiter during TS1 training set. This bit is reset when IBIST is done. The IBIST transmitter can be stopped by setting this bit to 0. 0: Stop IBIST transmitter 1: Start IBIST transmitter

11.8.2.2 NBFIBPGCTL: NB IBIST Pattern Generator Control Register

This register contains bits to control the operation of the IBIST pattern generator. All counts are in 24 bit increments.

Function: 6 Offset:C4h			
Bit	**Attr**	**Default**	**Description**
31:26	RWST	0Fh	OVRLOOPCNT: Overall Loop Count 0h: Reserved 1h-3Fh: Number of times to loop all the patterns.
25:21	RWST	00h	CNSTGENCNT: Constant Generator Loop Counter 00h: Disable constant generator output 01h: 1Fh The number of times the constant generator counter pattern should loop before going to the next component. Each count represents 24 bits of 1's or 0's.
20	RWST	0	CNSTGENSET: Constant Generator Setting 0: Generate 0 1: Generate 1
19:13	RWST	0Fh	MODLOOPCNT: Modulo-N Loop Counter Each count represents 24 bits of the pattern specified by **MODPERIOD**. 00h: Disable Pattern Output 01h: 7Fh The number of times the Pattern Buffer should loop before going to the next component.
12:10	RWST	001b	MODPERIOD: Period of the Modulo-N counter Each encoding transmits a 24-bit pattern as specified below. All other encodings are reserved. 001: L/2 - 0101_0101_0101_0101_0101_0101 010: L/4 - 0011_0011_0011_0011_0011_0011 011: L/6 - 0001_1100_0111_0001_1100_0111 100: L/8 - 0000_1111_0000_1111_0000_1111 110: L/24 - 0000_0000_0000_1111_1111_1111
9:3	RWST	0Fh	PATTLOOPCNT: Pattern Buffer Loop Counter 00h: Disable Pattern Output 01h: 7Fh The number of times the Pattern Buffer (**IBPATTBUF**) should be repeated before going to the next component.
2:0	RWST	000	PTGENORD: Pattern Generation Order 000: Pattern Store + Modulo N Cntr + Constant Generator 001: Pattern Store + Constant Generator + Modulo N Cntr 010: Modulo N Cntr + Pattern Store + Constant Generator 011: Modulo N Cntr + Constant Generator + Pattern Store 100: Constant Generator + Pattern Store + Modulo N Cntr 101: Constant Generator + Modulo N Cntr + Pattern Store 110: Reserved 111: Reserved

11.8.2.3 NBFIBPATTBUF1: NB IBIST Pattern Buffer 1 Register

This register contains the pattern bits used in IBIST operations. Only the least significant 24 bits are used.

Function: 6 **Offset:C8h**			
Bit	**Attr**	**Default**	**Description**
31:24	RV	00h	Reserved
23:0	RWST	02ccfdh	IBPATBUF: IBIST Pattern Buffer Pattern buffer storing the default and the user programmable pattern.

11.8.2.4 NBFIBTXMSK: NB IBIST Transmitter Mask Register

This register enables IBIST operations for individual lanes. This mask only applies to transmitters and not receivers.

Function: 6 **Offset:CCh**			
Bit	**Attr**	**Default**	**Description**
31:14	RV	00000h	Reserved
13:0	RWST	3FFFh	TXMASK: Selects which channels to enable for testing.

11.8.2.5 NBFIBRXMSK: NB IBIST Receiver Mask Register

This register enables IBIST operations for individual lanes. This mask only applies to receivers and not transmitters.

Function: 6 **Offset:D0h**			
Bit	**Attr**	**Default**	**Description**
31:14	RV	00000h	Reserved
13:0	RWST	3FFFh	RXMASK: Selects which channels to enable for testing.

11.8.2.6 NBFIBTXSHFT: NB IBIST Transmitter Inversion Shift Register

Each bit in this register enables inverting the patterns that is driven on corresponding lanes. If AUTOINVSWPEN bit is set in port control register, the TXINVSHFT field is rotated left at the completion of each pattern buffer set.

Function: 6 **Offset:D4h**			
Bit	**Attr**	**Default**	**Description**
31:14	RV	00000h	Reserved
13:0	RWST	3FFFh	TXINVSHFT: Transmitter Inversion Shift Register.

11.8.2.7 NBFIBRXSHFT: NB IBIST Receiver Inversion Shift Register

Each bit in this register enables inverting the patterns that is received on corresponding lanes. If AUTOINVSWPEN bit is set in port control register, the RXINVSHFT field is rotated left at the completion of each pattern buffer set.

Function: 6 Offset:D8h			
Bit	**Attr**	**Default**	**Description**
31:14	RV	00000h	Reserved
13:0	RWST	3FFFh	RXINVSHFT: Receiver Inversion Shift Register.

11.8.2.8 NBFIBRXLNERR: NB IBIST Receiver Lane Error Status

This records the error status from each lane.

Function: 6 Offset:DCh			
Bit	**Attr**	**Default**	**Description**
31:14	RV	00000h	Reserved
13:0	ROST	0000h	RXERRSTAT: Receiver Error Status

11.8.2.9 NBFIBPATTBUF2: NB IBIST Pattern Buffer 2Register

This register contains the pattern bits used in IBIST operations. Only the least significant 24 bits are used.

Function: 6 Offset:E0h			
Bit	**Attr**	**Default**	**Description**
31:24	RV	00h	Reserved
23:0	RWST	fd3302h	IBPATBUF2: IBIST Pattern Buffer 2 Pattern buffer storing the default and the user programmable pattern.

11.8.2.10 NBFIBPATT2EN: NB IBIST Pattern Buffer 2 Enable

This specifies which lanes will carry the pattern specified in NBFIBPATTBUFF2.

Function: 6 Offset:E4h			
Bit	**Attr**	**Default**	**Description**
15:14	RV	00	Reserved
13:0	RWST	0000h	IBPATBUF2EN: IBIST Pattern Buffer 2 enable Per lane enable for driving pattern buffer 2.

11.8.2.11 NBFIBINIT: NB IBIST Initialization Register

This register control northbound IBIST Testing.

Function: 6 Offset:F0h			
Bit	**Attr**	**Default**	**Description**
31	RWST	0	SBIDLE: SB Link is not active This is to enable the NB link to complete training when there is no activity on the SB side. Normally NB waits for SB init to complete before proceeding with its training. 0 - Wait for SB 1 - Do not wait for SB
30:21	RWST	0c8h	NBTS0CNT: Northbound TS0 Count Number of TS0 sequences to transmit.
20:13	RWST	01h	NBTS1CNT: Northbound TS1 Count Number of TS1 sequences to transmit.
12:3	RWST	100h	NBDISCNT: Northbound Disable State Count Number of cycles to remain in disable state.
2	RWST	1	NBCALIBEN: Northbound Calibrating Enable 1 - Perform FBD Calibration.
1	RV	0	Reserved
0	RWST	0	NBIBISTINITEN: IBIST Initialization Enable 1 - Start IBIST Testing with Northbound Transmitter as the host.

11.8.2.12 NBIBISTMISC: NB IBIST Initialization Miscellaneous Register

This register control northbound IBIST Testing.

Function: 6 Offset:F4h			
Bit	**Attr**	**Default**	**Description**
31:24	RV	0h	Reserved
23:20	RWST	0h	AMBID: Value of the AMB ID field during TS0
19:0	RWST	61a80h	NBIBISTCALPERIOD: Number of cycles to drive 1 during Calibration

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12 Ballout and Package Information

12.1 655-ball FBGA (23x29 Array, 19.5x24.5 mm Body Size, 0.8 mm Pitch, MO-261A Variation AA/BA) Pin configuration

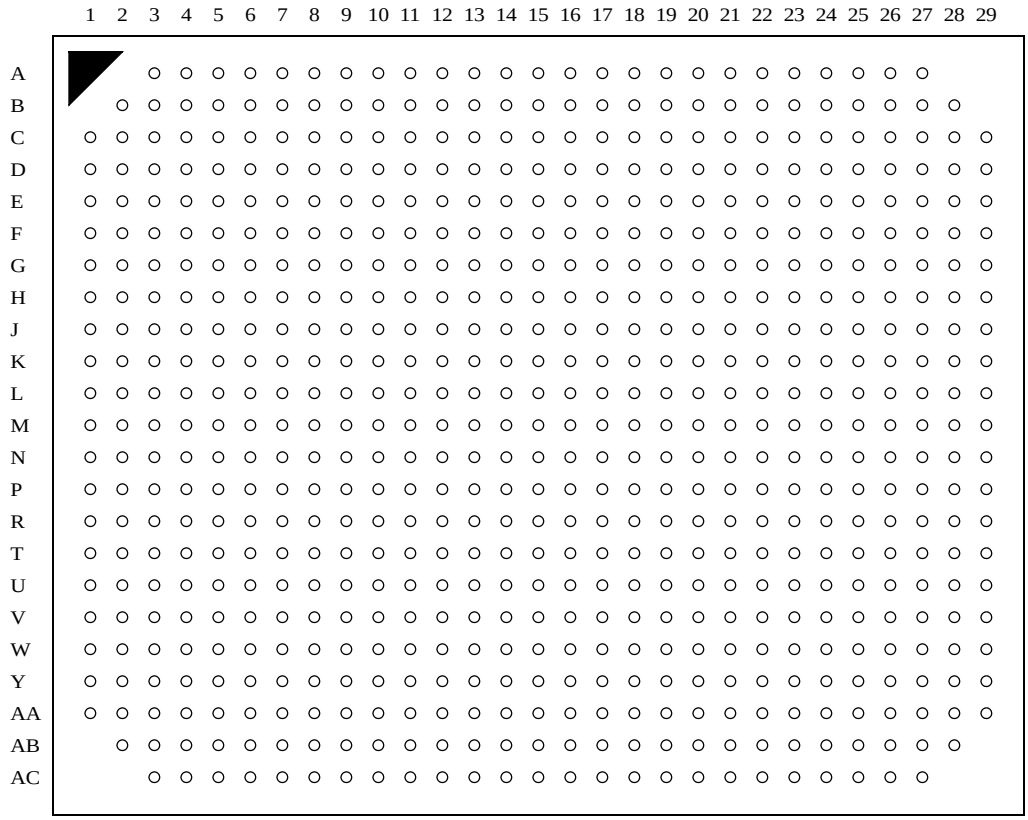


Figure 12.1 — Pinout Configuration

12.2 Pin Assignments for the Advanced Memory Buffer (AMB)

Table 12.1 — 655-Ball FBGA (23x29 Array, 19.5x24.5 mm Body Size, 0.8 mm Pitch, MO-261A Variation AA/BA) - Left Side

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
A			V_{SS}	DQ26	DQ12	V_{DD}	DQS10	DQ13	V_{DD}	$\overline{DQS}$1	DQ10	V_{DD}	TESTLO	V_{DD}	V_{DD}
B		V_{DD}	DQS3	$\overline{DQS}$3	V_{SS}	DQ14	$\overline{DQS}$10	V_{SS}	DQ11	DQS1	V_{SS}	DDRC	TESTLO	V_{DD}	V_{SS}
C	V_{SS}	DQS2	DQ18	V_{SS}	DQ4	$\overline{DQS}$9	V_{SS}	DQ15	DQ9	V_{SS}	DQ8	DDRC	V_{SS}	DDRC	DQS17
D	DQ19	$\overline{DQS}$2	V_{SS}	DQ16	DQ24	V_{SS}	DQS9	DQ7	V_{SS}	DQ3	DQS0	V_{SS}	$\overline{DQS}$8	DQS8	V_{DD}
E	DQ21	V_{SS}	DQ17	DQ29	V_{SS}	DQ25	DQ6	V_{SS}	DQ5	DQ1	V_{SS}	DQ0	CB1	V_{SS}	CB2
F	V_{SS}	DQ20	DQ23	V_{SS}	DQ31	DQ27	V_{SS}	TESTLO	TEST	V_{SS}	$\overline{DQS0}$	DQ2	V_{DD}	CB0	CB3
G	$\overline{DQS}$11	DQS11	NC	NC	NC	V_{SS}	DQS12	$\overline{DQS}$12	NC	NC	NC	BFUNC	RFU	RFU	RFU
H	DQ22	V_{SS}	NC	NC	NC	DQ28	DQ30	V_{SS}	NC	NC	NC	V_{SS}	V_{DD}	V_{SS}	V_{DD}
J	V_{SS}	CLK2	NC	NC	NC	BA1A	V_{SS}	CKE1A	NC	NC	NC	V_{DD}	V_{SS}	V_{DD}	V_{SS}
K	$\overline{CLK}$2	CLK0	NC	NC	NC	V_{SS}	$\overline{WE}$A	$\overline{RAS}$A	NC	NC	NC	V_{SS}	V_{CC}	V_{SS}	V_{CC}
L	$\overline{CLK}$0	V_{SS}	NC	NC	NC	A0A	CKE0A	V_{SS}	NC	NC	NC	V_{CC}	V_{SS}	V_{CC}	V_{SS}
M	ODT0A	RFU	NC	NC	NC	$\overline{CAS}$A	V_{SS}	BA2A	NC	NC	NC	V_{SS}	V_{CC}	V_{SS}	V_{CC}
N	$\overline{CS}$1A	$\overline{CS}$0A	NC	NC	NC	V_{SS}	BA0A	A10A	NC	NC	NC	V_{CC}	V_{SS}	V_{CC}	V_{SS}
P	A6A	V_{SS}	NC	NC	NC	A2A	A1A	A3A	NC	NC	NC	V_{SS}	V_{CC}	V_{SS}	V_{CC}
R	V_{SS}	A8A	NC	NC	NC	A11A	V_{SS}	A5A	NC	NC	NC	V_{CC}	V_{SS}	V_{CC}	V_{SS}
T	A4A	A13A	NC	NC	NC	V_{SS}	A9A	A7A	NC	NC	NC	V_{SS}	V_{CC}	V_{SS}	V_{CC}
U	PN0	$\overline{PN}$0	NC	NC	NC	A15A	A14A	A12A	NC	NC	NC	RFU	V_{CCFBD}	V_{SS}	V_{SS}
V	PN1	$\overline{PN}$1	V_{SS}	SN0	$\overline{SN}$0	V_{CCFBD}	V_{SS}	V_{CCFBD}	V_{SS}	RFU[a]	RFU[a]	V_{CCFBD}	V_{SS}	V_{SS}	V_{SS}
W	PN2	$\overline{PN}$2	V_{SS}	SN1	$\overline{SN}$1	$\overline{SN}$3	$\overline{SN}$4	$\overline{SN}$5	$\overline{SN}$13	$\overline{SN}$12	$\overline{SN}$6	$\overline{SN}$7	$\overline{SN}$8	$\overline{SN}$9	$\overline{SN}$10
Y	PN3	$\overline{PN}$3	V_{SS}	SN2	$\overline{SN}$2	SN3	SN4	SN5	SN13	SN12	SN6	SN7	SN8	SN9	SN10
AA	V_{SS}	PN4	$\overline{PN}$4	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}
AB		V_{SS}	$\overline{RESET}$	$\overline{PN}$5	$\overline{PN}$13	RFU[a]	$\overline{PN}$12	$\overline{PN}$6	$\overline{PN}$7	$\overline{PN}$8	$\overline{PN}$9	V_{SSAPLL}	V_{CCAPLL}	$\overline{PN}$10	$\overline{PN}$11
AC			V_{SS}	PN5	PN13	RFU[a]	PN12	PN6	PN7	PN8	PN9	FBDRES	PLLTSTO	PN10	PN11

[a] These pin positions are reserved for forward clocks to be used in future AMB implementations.

Table 12.2 — 655-Ball FBGA (23x29 Array, 19.5x24.5 mm Body Size, 0.8 mm Pitch, MO-261A Variation AA/BA) - Right Side

	16	17	18	19	20	21	22	23	24	25	26	27	28	29
A	V_{DD}	TEST	V_{DD}	DQ52	DQS15	V_{DD}	DQ49	$\overline{DQS}$6	V_{DD}	DQ48	DQ38	V_{DD}		
B	V_{DD}	TESTLO	DDRC	V_{SS}	$\overline{DQS}$15	DQ53	V_{SS}	DQS6	DQ50	V_{SS}	$\overline{DQS}$13	DQS13	V_{SS}	
C	$\overline{DQS}$17	V_{SS}	DDRC	DQ54	V_{SS}	DQ55	DQ51	V_{SS}	DQS7	DQ56	V_{SS}	DQ46	$\overline{DQS}$14	V_{DD}
D	CB6	CB7	V_{SS}	DQS16	DQ63	V_{SS}	DQ59	$\overline{DQS}$7	V_{SS}	DQ36	DQ44	V_{SS}	DQS14	DQ47
E	V_{SS}	CB5	$\overline{DQS}$16	V_{SS}	DQ61	DQ57	V_{SS}	DQ58	DQ39	V_{SS}	DQ33	DQ45	V_{SS}	DQ41
F	CB4	V_{DD}	DQ62	DQ60	V_{SS}	TEST	TEST	V_{SS}	DQ37	DQ35	V_{SS}	$\overline{DQS}$5	DQ43	V_{SS}
G	TESTLO	RFU	RFU	NC	NC	NC	DQS4	$\overline{DQS}$4	V_{SS}	NC	NC	NC	DQS5	DQ40
H	V_{SS}	V_{DD}	V_{SS}	NC	NC	NC	V_{SS}	DQ34	DQ32	NC	NC	NC	V_{SS}	DQ42
J	V_{DD}	V_{SS}	V_{DD}	NC	NC	NC	$\overline{RAS}$B	V_{SS}	RFU	NC	NC	NC	$\overline{CLK}$3	V_{SS}
K	V_{SS}	V_{CC}	V_{SS}	NC	NC	NC	ODT0B	$\overline{CS}$1B	V_{SS}	NC	NC	NC	$\overline{CLK}$1	CLK3
L	V_{CC}	V_{SS}	V_{CC}	NC	NC	NC	V_{SS}	$\overline{CAS}$B	$\overline{WE}$B	NC	NC	NC	V_{SS}	CLK1
M	V_{SS}	V_{CC}	V_{SS}	NC	NC	NC	$\overline{CS}$0B	V_{SS}	BA1B	NC	NC	NC	CKE0B	V_{SS}
N	V_{CC}	V_{SS}	V_{CC}	NC	NC	NC	A0B	A2B	V_{SS}	NC	NC	NC	BA0B	BA2B
P	V_{SS}	V_{CC}	V_{SS}	NC	NC	NC	V_{SS}	A4B	A1B	NC	NC	NC	V_{SS}	CKE1B
R	V_{CC}	V_{SS}	V_{CC}	NC	NC	NC	A6B	V_{SS}	A10B	NC	NC	NC	A3B	V_{SS}
T	V_{SS}	V_{CC}	V_{SS}	NC	NC	NC	A11B	A9B	V_{SS}	NC	NC	NC	A7B	A5B
U	V_{SS}	V_{CCFBD}	RFU	NC	NC	NC	A8B	A15B	A14B	SA0	SCL	SDA	$\overline{PS}$8	PS8
V	V_{CCFBD}	V_{SS}	V_{CCFBD}	V_{SS}	V_{CCFBD}	RFU[a]	RFU[a]	V_{SS}	A13B	A12 B	SA2	SA1	$\overline{PS}$7	PS7
W	V_{SS}	$\overline{SS}$0	$\overline{SS}$1	$\overline{SS}$2	$\overline{SS}$3	$\overline{SS}$4	$\overline{SS}$9	$\overline{SS}$5	$\overline{SS}$6	$\overline{SS}$7	$\overline{SS}$8	V_{SS}	$\overline{PS}$6	PS6
Y	V_{SS}	SS0	SS1	SS2	SS3	SS4	SS9	SS5	SS6	SS7	SS8	V_{SS}	$\overline{PS}$5	PS5
AA	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	$\overline{PS}$9	PS9	V_{SS}
AB	V_{SS}	$\overline{SN}$11	V_{SS}	SCK	TESTLO_AB20	$\overline{PS}$0	$\overline{PS}$1	$\overline{PS}$2	$\overline{PS}$3	$\overline{PS}$4	RFU[a]	V_{DDSPD}	V_{SS}	
AC	RFU	SN11	V_{SS}	$\overline{SCK}$	TESTLO_AC20	PS0	PS1	PS2	PS3	PS4	RFU[a]	V_{SS}		

[a] These pin positions are reserved for forward clocks to be used in future AMB implementations.

Table 12.3 — Advanced Memory Buffer Signals By Ball Number (Sheet 1 of 6)

Ball No.	Signal		Ball No.	Signal		Ball No.	Signal
A3	VSS		B15	VSS		C25	DQ56
A4	DQ26		B16	VDD		C26	VSS
A5	DQ12		B17	TESTLO		C27	DQ46
A6	VDD		B18	DDRC_B18		C28	$\overline{\text{DQS}}$14
A7	DQS10		B19	VSS		C29	VDD
A8	DQ13		B20	$\overline{\text{DQS}}$15		D1	DQ19
A9	VDD		B21	DQ53		D2	$\overline{\text{DQS}}$2
A10	$\overline{\text{DQS}}$1		B22	VSS		D3	VSS
A11	DQ10		B23	DQS6		D4	DQ16
A12	VDD		B24	DQ50		D5	DQ24
A13	TESTLO		B25	VSS		D6	VSS
A14	VDD		B26	$\overline{\text{DQS}}$13		D7	DQS9
A15	VDD		B27	DQS13		D8	DQ7
A16	VDD		B28	VSS		D9	VSS
A17	TEST		C1	VSS		D10	DQ3
A18	VDD		C2	DQS2		D11	DQS0
A19	DQ52		C3	DQ18		D12	VSS
A20	DQS15		C4	VSS		D13	$\overline{\text{DQS}}$8
A21	VDD		C5	DQ4		D14	DQS8
A22	DQ49		C6	$\overline{\text{DQS}}$9		D15	VDD
A23	$\overline{\text{DQS}}$6		C7	VSS		D16	CB6
A24	VDD		C8	DQ15		D17	CB7
A25	DQ48		C9	DQ9		D18	VSS
A26	DQ38		C10	VSS		D19	DQS16
A27	VDD		C11	DQ8		D20	DQ63
B2	VDD		C12	DDRC_C12		D21	VSS
B3	DQS3		C13	VSS		D22	DQ59
B4	$\overline{\text{DQS}}$3		C14	DDRC_C14		D23	$\overline{\text{DQS}}$7
B5	VSS		C15	DQS17		D24	VSS
B6	DQ14		C16	$\overline{\text{DQS}}$17		D25	DQ36
B7	$\overline{\text{DQS}}$10		C17	VSS		D26	DQ44
B8	VSS		C18	DDRC_C18		D27	VSS
B9	DQ11		C19	DQ54		D28	DQS14
B10	DQS1		C20	VSS		D29	DQ47
B11	VSS		C21	DQ55		E1	DQ21
B12	DDRC_B12		C22	DQ51		E2	VSS
B13	TESTLO		C23	VSS		E3	DQ17
B14	VDD		C24	DQS7		E4	DQ29

Table 12.3 — Advanced Memory Buffer Signals By Ball Number (Sheet 2 of 6)

Ball No.	Signal		Ball No.	Signal		Ball No.	Signal
E5	VSS		F14	CB0		G23	$\overline{\text{DQS}}$4
E6	DQ25		F15	CB3		G24	VSS
E7	DQ6		F16	CB4		G25	NC
E8	VSS		F17	VDD		G26	NC
E9	DQ5		F18	DQ62		G27	NC
E10	DQ1		F19	DQ60		G28	DQS5
E11	VSS		F20	VSS		G29	DQ40
E12	DQ0		F21	TEST		H1	DQ22
E13	CB1		F22	TEST		H2	VSS
E14	VSS		F23	VSS		H3	NC
E15	CB2		F24	DQ37		H4	NC
E16	VSS		F25	DQ35		H5	NC
E17	CB5		F26	VSS		H6	DQ28
E18	$\overline{\text{DQS}}$16		F27	$\overline{\text{DQS}}$5		H7	DQ30
E19	VSS		F28	DQ43		H8	VSS
E20	DQ61		F29	VSS		H9	NC
E21	DQ57		G1	$\overline{\text{DQS}}$11		H10	NC
E22	VSS		G2	DQS11		H11	NC
E23	DQ58		G3	NC		H12	VSS
E24	DQ39		G4	NC		H13	VDD
E25	VSS		G5	NC		H14	VSS
E26	DQ33		G6	VSS		H15	VDD
E27	DQ45		G7	DQS12		H16	VSS
E28	VSS		G8	$\overline{\text{DQS}}$12		H17	VDD
E29	DQ41		G9	NC		H18	VSS
F1	VSS		G10	NC		H19	NC
F2	DQ20		G11	NC		H20	NC
F3	DQ23		G12	BFUNC		H21	NC
F4	VSS		G13	RFU		H22	VSS
F5	DQ31		G14	RFU		H23	DQ34
F6	DQ27		G15	RFU		H24	DQ32
F7	VSS		G16	TESTLO		H25	NC
F8	TESTLO		G17	RFU		H26	NC
F9	TEST		G18	RFU		H27	NC
F10	VSS		G19	NC		H28	VSS
F11	$\overline{\text{DQS}}$0		G20	NC		H29	DQ42
F12	DQ2		G21	NC		J1	VSS
F13	VDD		G22	DQS4		J2	CLK2

Table 12.3 — Advanced Memory Buffer Signals By Ball Number (Sheet 3 of 6)

Ball No.	Signal		Ball No.	Signal		Ball No.	Signal
J3	NC		K12	VSS		L21	NC
J4	NC		K13	VCC		L22	VSS
J5	NC		K14	VSS		L23	$\overline{\text{CASB}}$
J6	BA1A		K15	VCC		L24	$\overline{\text{WEB}}$
J7	VSS		K16	VSS		L25	NC
J8	CKE1A		K17	VCC		L26	NC
J9	NC		K18	VSS		L27	NC
J10	NC		K19	NC		L28	VSS
J11	NC		K20	NC		L29	CLK1
J12	VDD		K21	NC		M1	ODT0A
J13	VSS		K22	ODT0B		M2	RFU
J14	VDD		K23	$\overline{\text{CS1}}$B		M3	NC
J15	VSS		K24	VSS		M4	NC
J16	VDD		K25	NC		M5	NC
J17	VSS		K26	NC		M6	$\overline{\text{CASA}}$
J18	VDD		K27	NC		M7	VSS
J19	NC		K28	$\overline{\text{CLK}}$1		M8	BA2A
J20	NC		K29	CLK3		M9	NC
J21	NC		L1	$\overline{\text{CLK}}$0		M10	NC
J22	$\overline{\text{RASB}}$		L2	VSS		M11	NC
J23	VSS		L3	NC		M12	VSS
J24	RFU		L4	NC		M13	VCC
J25	NC		L5	NC		M14	VSS
J26	NC		L6	A0A		M15	VCC
J27	NC		L7	CKE0A		M16	VSS
J28	$\overline{\text{CLK}}$3		L8	VSS		M17	VCC
J29	VSS		L9	NC		M18	VSS
K1	$\overline{\text{CLK}}$2		L10	NC		M19	NC
K2	CLK0		L11	NC		M20	NC
K3	NC		L12	VCC		M21	NC
K4	NC		L13	VSS		M22	$\overline{\text{CS0}}$B
K5	NC		L14	VCC		M23	VSS
K6	VSS		L15	VSS		M24	BA1B
K7	$\overline{\text{WEA}}$		L16	VCC		M25	NC
K8	$\overline{\text{RASA}}$		L17	VSS		M26	NC
K9	NC		L18	VCC		M27	NC
K10	NC		L19	NC		M28	CKE0B
K11	NC		L20	NC		M29	VSS

Table 12.3 — Advanced Memory Buffer Signals By Ball Number (Sheet 4 of 6)

Ball No.	Signal		Ball No.	Signal		Ball No.	Signal
N1	$\overline{CS1}$A		P10	NC		R19	NC
N2	$\overline{CS0}$A		P11	NC		R20	NC
N3	NC		P12	VSS		R21	NC
N4	NC		P13	VCC		R22	A6B
N5	NC		P14	VSS		R23	VSS
N6	VSS		P15	VCC		R24	A10B
N7	BA0A		P16	VSS		R25	NC
N8	A10A		P17	VCC		R26	NC
N9	NC		P18	VSS		R27	NC
N10	NC		P19	NC		R28	A3B
N11	NC		P20	NC		R29	VSS
N12	VCC		P21	NC		T1	A4A
N13	VSS		P22	VSS		T2	A13A
N14	VCC		P23	A4B		T3	NC
N15	VSS		P24	A1B		T4	NC
N16	VCC		P25	NC		T5	NC
N17	VSS		P26	NC		T6	VSS
N18	VCC		P27	NC		T7	A9A
N19	NC		P28	VSS		T8	A7A
N20	NC		P29	CKE1B		T9	NC
N21	NC		R1	VSS		T10	NC
N22	A0B		R2	A8A		T11	NC
N23	A2B		R3	NC		T12	VSS
N24	VSS		R4	NC		T13	VCC
N25	NC		R5	NC		T14	VSS
N26	NC		R6	A11A		T15	VCC
N27	NC		R7	VSS		T16	VSS
N28	BA0B		R8	A5A		T17	VCC
N29	BA2B		R9	NC		T18	VSS
P1	A6A		R10	NC		T19	NC
P2	VSS		R11	NC		T20	NC
P3	NC		R12	VCC		T21	NC
P4	NC		R13	VSS		T22	A11B
P5	NC		R14	VCC		T23	A9B
P6	A2A		R15	VSS		T24	VSS
P7	A1A		R16	VCC		T25	NC
P8	A3A		R17	VSS		T26	NC
P9	NC		R18	VCC		T27	NC

Table 12.3 — Advanced Memory Buffer Signals By Ball Number (Sheet 5 of 6)

Ball No.	Signal		Ball No.	Signal		Ball No.	Signal
T28	A7B		V8	VCCFBD		W17	$\overline{SS}$0
T29	A5B		V9	VSS		W18	$\overline{SS}$1
U1	PN0		V10	RFU[a]		W19	$\overline{SS}$2
U2	$\overline{PN}$0		V11	RFU[a]		W20	$\overline{SS}$3
U3	NC		V12	VCCFBD		W21	$\overline{SS}$4
U4	NC		V13	VSS		W22	$\overline{SS}$9
U5	NC		V14	VSS		W23	$\overline{SS}$5
U6	A15A		V15	VSS		W24	$\overline{SS}$6
U7	A14A		V16	VCCFBD		W25	$\overline{SS}$7
U8	A12A		V17	VSS		W26	$\overline{SS}$8
U9	NC		V18	VCCFBD		W27	VSS
U10	NC		V19	VSS		W28	$\overline{PS}$6
U11	NC		V20	VCCFBD		W29	PS6
U12	RFU		V21	RFU[a]		Y1	PN3
U13	VCCFBD		V22	RFU[a]		Y2	$\overline{PN}$3
U14	VSS		V23	VSS		Y3	VSS
U15	VSS		V24	A13B		Y4	SN2
U16	VSS		V25	A12B		Y5	$\overline{SN}$2
U17	VCCFBD		V26	SA2		Y6	SN3
U18	RFU		V27	SA1		Y7	SN4
U19	NC		V28	$\overline{PS}$7		Y8	SN5
U20	NC		V29	PS7		Y9	SN13
U21	NC		W1	PN2		Y10	SN12
U22	A8B		W2	$\overline{PN}$2		Y11	SN6
U23	A15B		W3	VSS		Y12	SN7
U24	A14B		W4	SN1		Y13	SN8
U25	SA0		W5	$\overline{SN}$1		Y14	SN9
U26	SCL		W6	$\overline{SN}$3		Y15	SN10
U27	SDA		W7	$\overline{SN}$4		Y16	VSS
U28	$\overline{PS}$8		W8	$\overline{SN}$5		Y17	SS0
U29	PS8		W9	$\overline{SN}$13		Y18	SS1
V1	PN1		W10	$\overline{SN}$12		Y19	SS2
V2	$\overline{PN}$1		W11	$\overline{SN}$6		Y20	SS3
V3	VSS		W12	$\overline{SN}$7		Y21	SS4
V4	SN0		W13	$\overline{SN}$8		Y22	SS9
V5	$\overline{SN}$0		W14	$\overline{SN}$9		Y23	SS5
V6	VCCFBD		W15	$\overline{SN}$10		Y24	SS6
V7	VSS		W16	VSS		Y25	SS7

[a] These pin positions are reserved for forward clocks to be used in future AMB implementations.

Table 12.3 — Advanced Memory Buffer Signals By Ball Number (Sheet 6 of 6)

Ball No.	Signal		Ball No.	Signal		Ball No.	Signal
Y26	SS8		AB7	$\overline{PN}$12		AC19	$\overline{SCK}$
Y27	VSS		AB8	$\overline{PN}$6		AC20	TESTLO_AC20
Y28	$\overline{PS}$5		AB9	$\overline{PN}$7		AC21	PS0
Y29	PS5		AB10	$\overline{PN}$8		AC22	PS1
AA1	VSS		AB11	$\overline{PN}$9		AC23	PS2
AA2	PN4		AB12	VSSAPLL		AC24	PS3
AA3	$\overline{PN}$4		AB13	VCCAPLL		AC25	PS4
AA4	VSS		AB14	$\overline{PN}$10		AC26	RFU[a]
AA5	VSS		AB15	$\overline{PN}$11		AC27	VSS
AA6	VSS		AB16	VSS			
AA7	VSS		AB17	$\overline{SN}$11			
AA8	VSS		AB18	VSS			
AA9	VSS		AB19	SCK			
AA10	VSS		AB20	TESTLO_AB20			
AA11	VSS		AB21	$\overline{PS}$0			
AA12	VSS		AB22	$\overline{PS}$1			
AA13	VSS		AB23	$\overline{PS}$2			
AA14	VSS		AB24	$\overline{PS}$3			
AA15	VSS		AB25	$\overline{PS}$4			
AA16	VSS		AB26	RFU[a]			
AA17	VSS		AB27	VDDSPD			
AA18	VSS		AB28	VSS			
AA19	VSS		AC3	VSS			
AA20	VSS		AC4	PN5			
AA21	VSS		AC5	PN13			
AA22	VSS		AC6	RFU[a]			
AA23	VSS		AC7	PN12			
AA24	VSS		AC8	PN6			
AA25	VSS		AC9	PN7			
AA26	VSS		AC10	PN8			
AA27	$\overline{PS}$9		AC11	PN9			
AA28	PS9		AC12	FBDRES			
AA29	VSS		AC13	PLLTSTO			
AB2	VSS		AC14	PN10			
AB3	$\overline{RESET}$		AC15	PN11			
AB4	$\overline{PN}$5		AC16	RFU			
AB5	$\overline{PN}$13		AC17	SN11			
AB6	RFU[a]		AC18	VSS			

[a] These pin positions are reserved for forward clocks to be used in future AMB implementations.

12.3 Package Information

Refer to Registered Outline MO-261A published by JC-11 committee for AMB package info.

Standard Improvement Form JEDEC JESD82-20

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1. I recommend changes to the following:

☐ Requirement, paragraph number _____

☐ Test method number _____ Paragraph number _____

The referenced paragraph number has proven to be:

☐ Unclear ☐ Too Rigid ☐ In Error

☐ Other _____

2. Recommendations for correction:

_____

_____

_____

_____

3. Other suggestions for document improvement:

_____

_____

_____

_____

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Company: _____ E-mail: _____

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Rev. 9/02



Exhibit B

JEDEC STANDARD

FBDIMM Specification:

DDR2 SDRAM Fully Buffered DIMM (FBDIMM) Design Specification

JESD205

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March 2007

JEDEC SOLID STATE TECHNOLOGY ASSOCIATION





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Product Description

This specification defines the electrical and mechanical requirements for 240-pin, PC2-4200/PC2-5300/ PC2-6400, 72 bit-wide, Fully Buffered Double Data Rate Synchronous DRAM Dual In-Line Memory Modules (DDR2 SDRAM FB-DIMMs).These SDRAM FB-DIMMs are intended for use as main memory when installed in systems such as servers and workstations. PC2-4200/PC2-5300/PC2-6400 refers to the DIMM naming convention in which PC2-4200/PC2-5300/PC2-6400 indicates a 240-pin DDR2 DIMM running at 266/333/400 MHz DRAM clock speed and offering 4266/5333/6400 MB/s bandwidth.

DIMM	DRAM	DRAM Clock	Single DIMM Bandwidth	Channel Clock	Channel Transfer Rate
PC2-4200	DDR2-533	266 MHz	4266 MB/s	133 MHz	3.2 GT/s
PC2-5300	DDR2-667	333 MHz	5333 MB/s	166 MHz	4.0 GT/s
PC2-6400	DDR2-800	400 MHz	6400 MB/s	200 MHz	4.8 GT/s

Reference design examples are included which provide an initial basis for Fully Buffered DIMM designs. Modifications to these reference designs may be required to meet all system timing, signal integrity, and thermal requirements for PC2-4200/PC2-5300/PC2-6400 support. All Fully Buffered DIMM implementations must use simulations and lab verification to ensure proper timing requirements and signal integrity in the design..

Product Family Attributes

DIMM organization	x72 ECC			
DIMM dimensions (nominal)	30.35mm (height) x 133.35mm (width) x 8.2 mm (max thickness) MO-256 variation AB 30.35mm (height) x 133.35mm (width) x 8.8 mm (max thickness) MO-256 variation BB			
Pin count	240			
SDRAMs supported	256Mb, 512Mb, 1Gb, 2Gb, 4Gb			
Capacity	256MB, 512MB, 1GB, 2GB, 4GB, 8GB, 16GB			
Serial PD	Consistent with JC 45			
Supply voltages (nominal)	min	typ	max	
	1.7	1.8	1.9	(DRAM V_{DD}/V_{DDQ}, AMB V_{DDQ})
	1.455[1]	1.5	1.575[1]	(AMB V_{CC}/V_{CCFBD})
	$0.453*V_{DD}$	$0.5*V_{DD}$	$0.547*V_{DD}$	(DRAM Interface V_{TT}) This supply should track as 0.5 * 1.8 volt supply
	3.0	3.3	3.6	(V_{DDSPD})
Buffer Interface	High-speed Differential Point-to-point Link at 1.5 volt			
DRAM Interface	SSTL_18			

Note 1: Approximate DC values, refer to AMB Component Specification for actual DC and AC values and conditions.
Note 2: Vtt range accomodates measurable offset due to complementary CA bus current paths. (See Vtt section)
An Unloaded system should supply Vtt of 0.48*Vdd/0.52*Vdd to Dimm socket

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The reference designs for the DIMM PCBs are called the “raw cards”, abbreviated R/C. After the designs have been verified in working systems, the JEDEC JC-45 committee will post registrations of these R/C designs to the JEDEC web site for use by the industry at large.

Product Family Raw Card Types

Raw Card	DRAM Data Width	# of Ranks	# of DRAM	Z-axis	Width x Height (mm)
A	x8	1	9	planar	133.35 x 30.35
B	x8	2	18	planar	133.35 x 30.35
C	x4	1	18	planar	133.35 x 30.35
D	x4	2	36	stacked / dual die	133.35 x 30.35
E	x4	2	36	planar	133.35 x 30.35
H	x4	2	36	planar	133.35 x 30.35
J	x4	2	36	stacked / dual die	133.35 x 30.35

Environmental Requirements

DDR2 SDRAM Fully Buffered DIMMs are intended for use in standard office environments that have limited capacity for heating and air conditioning.

Environmental Parameters

Symbol	Parameter	Rating	Units	Notes
T_{OPR}	Operating temperature	See Note		1
H_{OPR}	Operating humidity (relative)	10 to 90	%	2
T_{STG}	Storage temperature	-50 to +100	°C	2
H_{STG}	Storage humidity (without condensation)	5 to 95	%	2
P_{BAR}	Barometric pressure (operating & storage)	105 to 69	K Pascal	2

1. The designer must meet the case temperature specifications for individual module components.
2. Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

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Architecture

DIMM Connector Pin Description

Pin Name	Pin Description	Count
SCK	System Clock Input, positive line[1]	1
$\overline{SCK}$	System Clock Input, negative line[1]	1
PN[13:0]	Primary Northbound Data, positive lines	14
$\overline{PN}$[13:0]	Primary Northbound Data, negative lines	14
PS[9:0]	Primary Southbound Data, positive lines	10
$\overline{PS}$[9:0]	Primary Southbound Data, negative lines	10
SN[13:0]	Secondary Northbound Data, positive lines	14
$\overline{SN}$[13:0]	Secondary Northbound Data, negative lines	14
SS[9:0]	Secondary Southbound Data, positive lines	10
$\overline{SS}$[9:0]	Secondary Southbound Data, negative lines	10
SCL	Serial Presence Detect (SPD) Clock Input	1
SDA	SPD Data Input / Output	1
SA[2:0]	SPD Address Inputs, also used to select the DIMM number in the AMB	3
VID[1:0]	Voltage ID: These pins must be unconnected for DDR2-based Fully Buffered DIMMs VID[0] is V_{DD} value: OPEN = 1.8 V, GND = 1.5 V; VID[1] is V_{CC} value: OPEN = 1.5 V, GND = 1.2 V	2
$\overline{RESET}$	AMB reset signal	1
RFU	Reserved for Future Use[2]	16
V_{CC}	AMB Core Power and AMB Channel Interface Power (1.5 Volt)	8
V_{DD}	DRAM Power and AMB DRAM I/O Power (1.8 Volt)	24
V_{TT}	DRAM Address/Command/Clock Termination Power (V_{DD}/2)	4
V_{DDSPD}	SPD Power	1
V_{SS}	Ground	80
DNU/M_Test	The DNU/M_Test pin provides an external connection on R/Cs A-D for testing the margin of Vref which is produced by a voltage divider on the module. It is not intended to be used in normal system operation and must not be connected (DNU) in a system. This test pin may have other features on future card designs and if it does, will be included in this specification at that time. 1	1
	Total	240

1. System Clock Signals SCK and $\overline{SCK}$ switch at one half the DRAM CK/$\overline{CK}$ frequency
2. Eight pins reserved for forwarded clocks, eight pins reserved for future architecture flexibility

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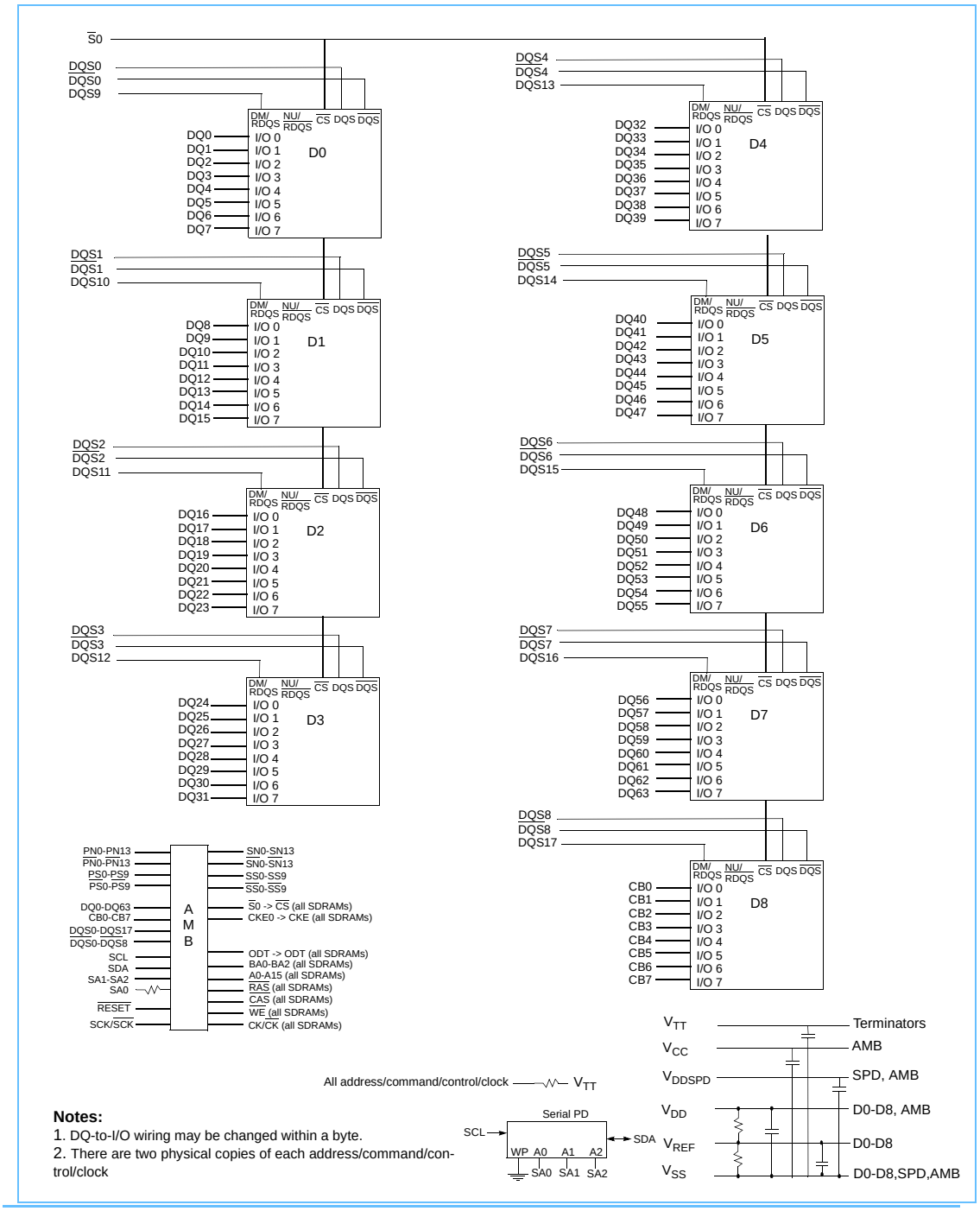
DDR2 240-pin FBDIMM Pinout

Pin #	Front Side	Pin #	Back Side	Pin #	Front Side	Pin #	Back Side	Pin #	Front Side	Pin #	Back Side	Pin #	Front Side	Pin #	Back Side
1	V_{DD}	121	V_{DD}	31	PN3	151	SN3	61	$\overline{PN9}$	181	$\overline{SN9}$	91	$\overline{PS9}$	211	$\overline{SS9}$
2	V_{DD}	122	V_{DD}	32	$\overline{PN3}$	152	$\overline{SN3}$	62	V_{SS}	182	V_{SS}	92	V_{SS}	212	V_{SS}
3	V_{DD}	123	V_{DD}	33	V_{SS}	153	V_{SS}	63	PN10	183	SN10	93	PS5	213	SS5
4	V_{SS}	124	V_{SS}	34	PN4	154	SN4	64	$\overline{PN10}$	184	$\overline{SN10}$	94	$\overline{PS5}$	214	$\overline{SS5}$
5	V_{DD}	125	V_{DD}	35	$\overline{PN4}$	155	$\overline{SN4}$	65	V_{SS}	185	V_{SS}	95	V_{SS}	215	V_{SS}
6	V_{DD}	126	V_{DD}	36	V_{SS}	156	V_{SS}	66	PN11	186	SN11	96	PS6	216	SS6
7	V_{DD}	127	V_{DD}	37	PN5	157	SN5	67	$\overline{PN11}$	187	$\overline{SN11}$	97	$\overline{PS6}$	217	$\overline{SS6}$
8	V_{SS}	128	V_{SS}	38	$\overline{PN5}$	158	$\overline{SN5}$	68	V_{SS}	188	V_{SS}	98	V_{SS}	218	V_{SS}
9	V_{CC}	129	V_{CC}	39	V_{SS}	159	V_{SS}	KEY				99	PS7	219	SS7
10	V_{CC}	130	V_{CC}	40	PN13	160	SN13	69	V_{SS}	189	V_{SS}	100	$\overline{PS7}$	220	$\overline{SS7}$
11	V_{SS}	131	V_{SS}	41	$\overline{PN13}$	161	$\overline{SN13}$	70	PS0	190	SS0	101	V_{SS}	221	V_{SS}
12	V_{CC}	132	V_{CC}	42	V_{SS}	162	V_{SS}	71	$\overline{PS0}$	191	$\overline{SS0}$	102	PS8	222	SS8
13	V_{CC}	133	V_{CC}	43	V_{SS}	163	V_{SS}	72	V_{SS}	192	V_{SS}	103	$\overline{PS8}$	223	$\overline{SS8}$
14	V_{SS}	134	V_{SS}	44	RFU*	164	RFU*	73	PS1	193	SS1	104	V_{SS}	224	V_{SS}
15	V_{TT}	135	V_{TT}	45	RFU*	165	RFU*	74	$\overline{PS1}$	194	$\overline{SS1}$	105	RFU**	225	RFU**
16	VID1	136	VID0	46	V_{SS}	166	V_{SS}	75	V_{SS}	195	V_{SS}	106	RFU**	226	RFU**
17	$\overline{RESET}$	137	DNU/M_Test	47	V_{SS}	167	V_{SS}	76	PS2	196	SS2	107	V_{SS}	227	V_{SS}
18	V_{SS}	138	V_{SS}	48	PN12	168	SN12	77	$\overline{PS2}$	197	$\overline{SS2}$	108	V_{DD}	228	SCK
19	RFU**	139	RFU**	49	$\overline{PN12}$	169	$\overline{SN12}$	78	V_{SS}	198	V_{SS}	109	V_{DD}	229	$\overline{SCK}$
20	RFU**	140	RFU**	50	V_{SS}	170	V_{SS}	79	PS3	199	SS3	110	V_{SS}	230	V_{SS}
21	V_{SS}	141	V_{SS}	51	PN6	171	SN6	80	$\overline{PS3}$	200	$\overline{SS3}$	111	V_{DD}	231	V_{DD}
22	PN0	142	SN0	52	$\overline{PN6}$	172	$\overline{SN6}$	81	V_{SS}	201	V_{SS}	112	V_{DD}	232	V_{DD}
23	$\overline{PN0}$	143	$\overline{SN0}$	53	V_{SS}	173	V_{SS}	82	PS4	202	SS4	113	V_{DD}	233	V_{DD}
24	V_{SS}	144	V_{SS}	54	PN7	174	SN7	83	$\overline{PS4}$	203	$\overline{SS4}$	114	V_{SS}	234	V_{SS}
25	PN1	145	SN1	55	$\overline{PN7}$	175	$\overline{SN7}$	84	V_{SS}	204	V_{SS}	115	V_{DD}	235	V_{DD}
26	$\overline{PN1}$	146	$\overline{SN1}$	56	V_{SS}	176	V_{SS}	85	V_{SS}	205	V_{SS}	116	V_{DD}	236	V_{DD}
27	V_{SS}	147	V_{SS}	57	PN8	177	SN8	86	RFU*	206	RFU*	117	V_{TT}	237	V_{TT}
28	PN2	148	SN2	58	$\overline{PN8}$	178	$\overline{SN8}$	87	RFU*	207	RFU*	118	SA2	238	VDDSPD
29	$\overline{PN2}$	149	$\overline{SN2}$	59	V_{SS}	179	V_{SS}	88	V_{SS}	208	V_{SS}	119	SDA	239	SA0
30	V_{SS}	150	V_{SS}	60	PN9	180	SN9	89	V_{SS}	209	V_{SS}	120	SCL	240	SA1
								90	PS9	210	SS9				

RFU = Reserved Future Use.
* These pin positions are reserved for forwarded clocks to be used in future module implementations
** These pin positions are reserved for future architecture flexibility
1) The following signals are CRC bits and thus appear out of the normal sequence: PN12/$\overline{PN12}$, SN12/$\overline{SN12}$, PN13/$\overline{PN13}$, SN13/$\overline{SN13}$, PS9/$\overline{PS9}$, SS9/$\overline{SS9}$

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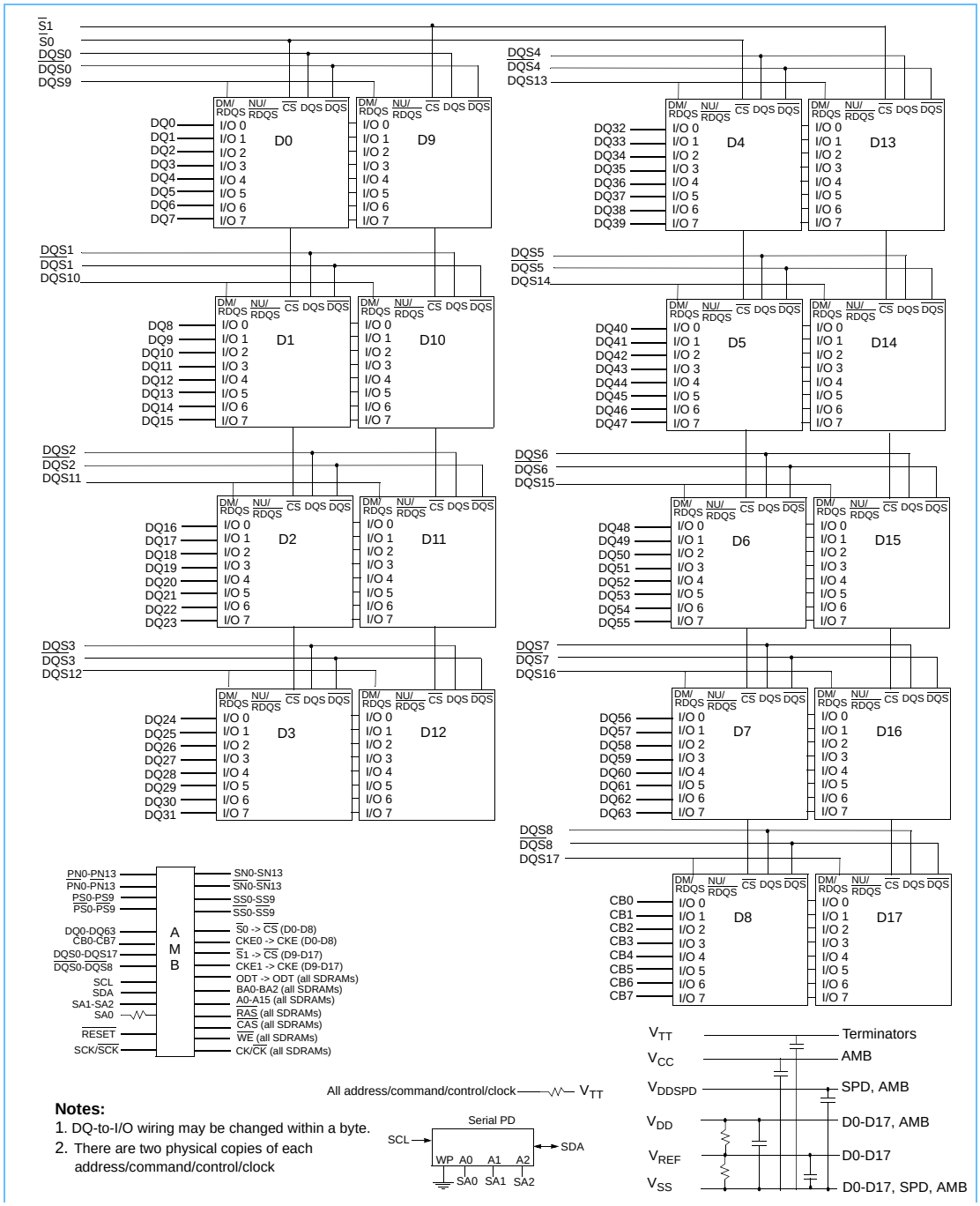
Block Diagram: Raw Card Version A (x72 ECC DIMM, one physical rank of x8 DDR2 SDRAMs)



Notes:

1. DQ-to-I/O wiring may be changed within a byte.
2. There are two physical copies of each address/command/control/clock

Block Diagram: Raw Card Version B (x72 ECC DIMMs, two physical ranks of x8 DDR2 SDRAMs)

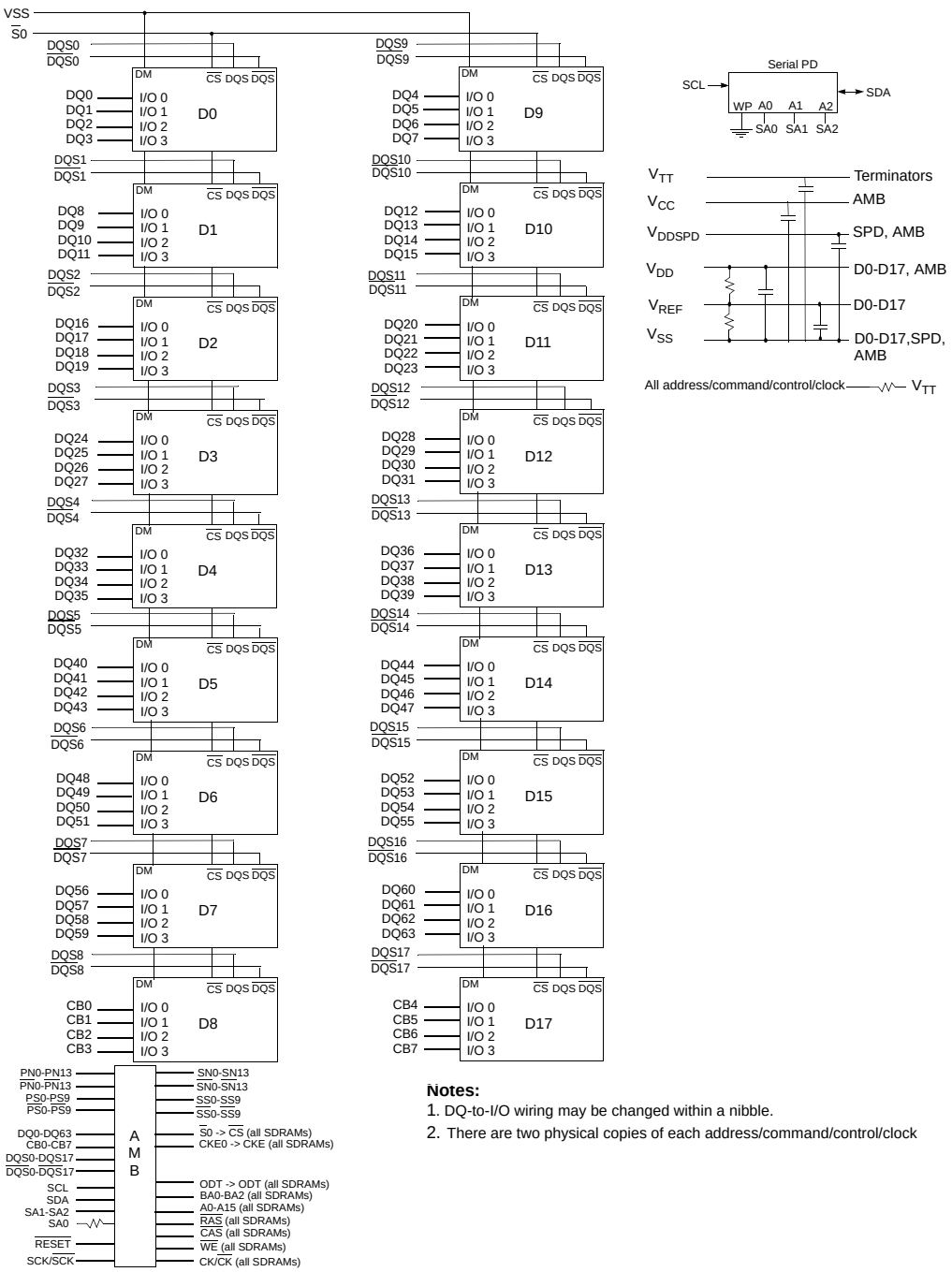


Notes:

1. DQ-to-I/O wiring may be changed within a byte.
2. There are two physical copies of each address/command/control/clock

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Block Diagram: Raw Card Version C (x72 ECC DIMM, one physical rank of x4 DDR2 SDRAMs)

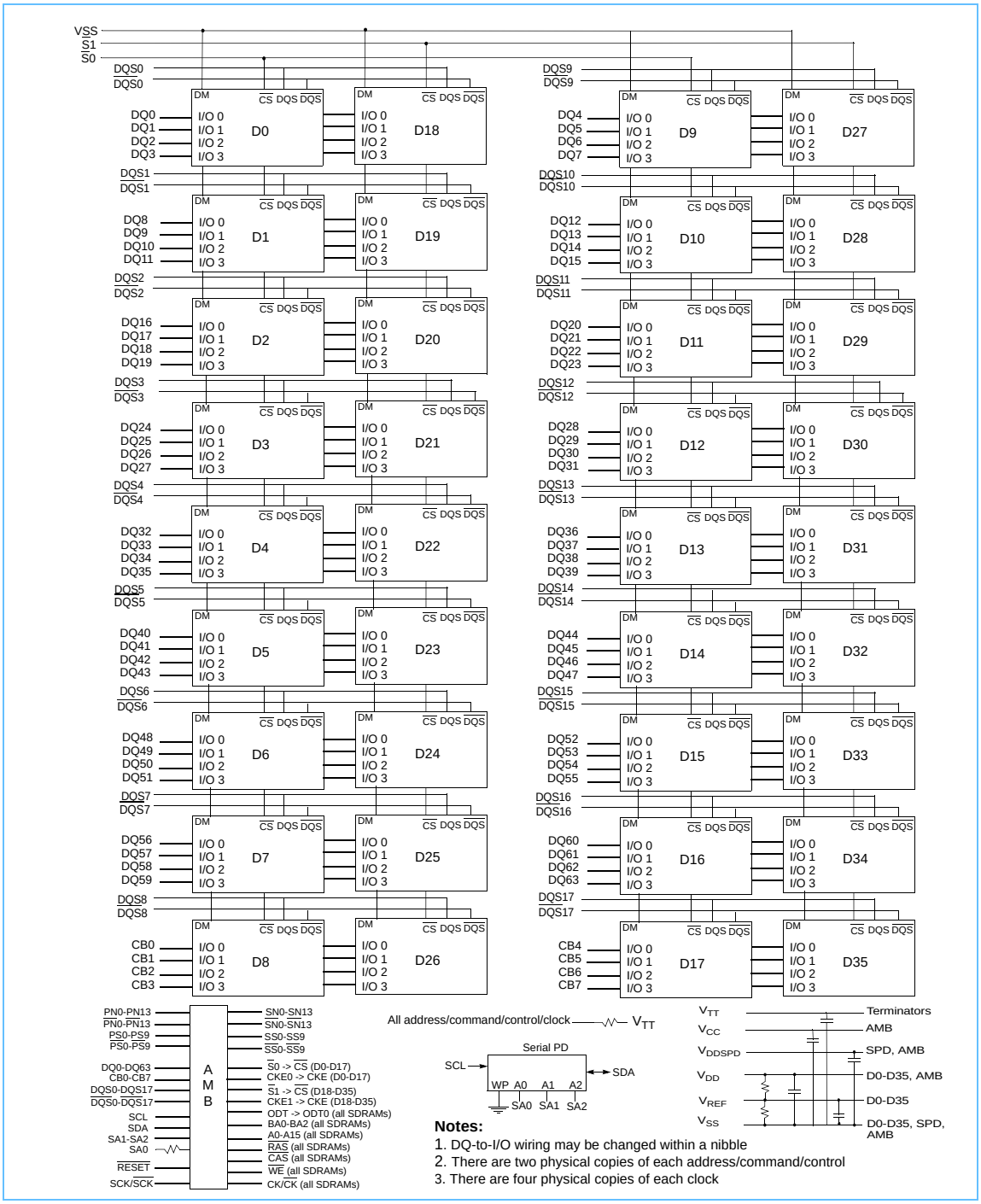


Notes:

1. DQ-to-I/O wiring may be changed within a nibble.
2. There are two physical copies of each address/command/control/clock

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Block Diagram: RC Versions D,E,H,J (x72 ECC DIMMs, 2 physical ranks of x4 DDR2 SDRAMs)



Notes:

1. DQ-to-I/O wiring may be changed within a nibble
2. There are two physical copies of each address/command/control
3. There are four physical copies of each clock

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Component Details:

DDR2 SDRAM, 256 Mb to 4 Gb

Raw cards A and B accommodate the x8 ballout with or without support balls, using the x8 common footprint. Raw card C accommodates the x4 ballout with or without support balls, using the x4 common footprint. Raw card D accommodates the stacked x4 ballout with or without support balls, using the stacked x4 common footprint. The tables on the next few pages may include blank rows above the first row with balls, so that all of the tables line up with the common footprints for x4, x8 and stacked x4.

Pin Assignments for x4 and x8 Ballouts without Support Balls (Top View)

(MO-207 variation DJ-z, 60 Balls FBGA 0.8mm x 0.8mm pitch)

x4 Ballout of DDR2 SDRAMs (Top view)

	1	2	3	7	8	9
A	VDD	NC	VSS	VSSQ	$\overline{\text{DQS}}$	VDDQ
B	NC	VSSQ	DM	DQS	VSSQ	NC
C	VDDQ	DQ1	VDDQ	VDDQ	DQ0	VDDQ
D	NC	VSSQ	DQ3	DQ2	VSSQ	NC
E	VDDL	VREF	VSS	VSSDL	CK	VDD
F		CKE	$\overline{\text{WE}}$	$\overline{\text{RAS}}$	$\overline{\text{CK}}$	ODT
G	BA2	BA0	BA1	$\overline{\text{CAS}}$	$\overline{\text{CS}}$	
H		A10	A1	A2	A0	VDD
J	VSS	A3	A5	A6	A4	
K		A7	A9	A11	A8	VSS
L	VDD	A12	A14,NC	A15,NC	A13,NC	

x8 Ballout of DDR2 SDRAMs (Top view)

	1	2	3	7	8	9
A	VDD	$\frac{\text{NU/}}{\text{RDQS}}$	VSS	VSSQ	$\overline{\text{DQS}}$	VDDQ
B	DQ6	VSSQ	DM/ RDQS	DQS	VSSQ	DQ7
C	VDDQ	DQ1	VDDQ	VDDQ	DQ0	VDDQ
D	DQ4	VSSQ	DQ3	DQ2	VSSQ	DQ5
E	VDDL	VREF	VSS	VSSDL	CK	VDD
F		CKE	$\overline{\text{WE}}$	$\overline{\text{RAS}}$	$\overline{\text{CK}}$	ODT
G	BA2	BA0	BA1	$\overline{\text{CAS}}$	$\overline{\text{CS}}$	
H		A10	A1	A2	A0	VDD
J	VSS	A3	A5	A6	A4	
K		A7	A9	A11	A8	VSS
L	VDD	A12	A14,NC	A15,NC	A13,NC	

1. The thick line area indicates the minimum ball out for x4 and x8 DDR2 SDRAMs.

2. Above coordinates of ball out corresponds to x4 and x8 PCB symbol.

3. NC balls will not be connected to anything on the DRAM. They will be either open or tied to VDD/VDDQ on the DIMM. Ball A2 (NU/$\overline{\text{RDQS}}$) will be open on the x8 based DIMMs.

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Pin Assignments for Stacked x4 Ballout without Support Balls (Top View)

(MO-242 variation AA, 63 Balls FBGA 0.8mm x 0.8mm pitch

x4 Ballout of DDR2 SDRAMs for Stacked DIMM (Top view)

	1	2	3		7	8	9
A	VDD	NC	VSS		VSSQ	$\overline{\text{DQS}}$	VDDQ
B	NC	VSSQ	DM		DQS	VSSQ	NC
C	VDDQ	DQ1	VDDQ		VDDQ	DQ0	VDDQ
D	NC	VSSQ	DQ3		DQ2	VSSQ	NC
E	VDDL	VREF	VSS		VSSDL	CK	VDD
F		CKE0	$\overline{\text{WE}}$		$\overline{\text{RAS}}$	$\overline{\text{CK}}$	ODT0
G	BA2	BA0	BA1		$\overline{\text{CAS}}$	$\overline{\text{CS0}}$	$\overline{\text{CS1}}$
H	CKE1	A10	A1		A2	A0	VDD
J	VSS	A3	A5		A6	A4	ODT1
K		A7	A9		A11	A8	VSS
L	VDD	A12	A14,NC		A15,NC	A13,NC	

1. The thick line area indicates the minimum ball out for x4 and x8 DDR2 SDRAMs.

2. Above coordinates of ball out corresponds to stacked x4 PCB symbol.

3. NC balls will not be connected to anything on the DRAM. They will be either open or tied to VDD/VDDQ on the DIMM.

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Pin Assignments for x4 and x8 Ballouts with Support Balls (Top View)

(MO-207 variation DM-z, 68 Balls FBGA 0.8mm x 0.8mm pitch)

x4 Ballout of DDR2 SDRAMs (Top view)

	1	2	3	7	8	9
A	NC	NC			NC	NC
B						
C						
D						
E	VDD	NC	VSS	VSSQ	$\overline{DQS}$	VDDQ
F	NC	VSSQ	DM	DQS	VSSQ	NC
G	VDDQ	DQ1	VDDQ	VDDQ	DQ0	VDDQ
H	NC	VSSQ	DQ3	DQ2	VSSQ	NC
J	VDDL	VREF	VSS	VSSDL	CK	VDD
K		CKE	$\overline{WE}$	$\overline{RAS}$	$\overline{CK}$	ODT
L	BA2	BA0	BA1	$\overline{CAS}$	$\overline{CS}$	
M		A10	A1	A2	A0	VDD
N	VSS	A3	A5	A6	A4	
P		A7	A9	A11	A8	VSS
L	VDD	A12	A14,NC	A15,NC	A13,NC	
T						
U						
V						
W	NC	NC			NC	NC

x8 Ballout of DDR2 SDRAMs (Top view)

	1	2	3	7	8	9
A	NC	NC			NC	NC
B						
C						
D						
E	VDD	$\overline{NU/RDQS}$	VSS	VSSQ	$\overline{DQS}$	VDDQ
F	DQ6	VSSQ	DM/ RDQS	DQS	VSSQ	DQ7
G	VDDQ	DQ1	VDDQ	VDDQ	DQ0	VDDQ
H	DQ4	VSSQ	DQ3	DQ2	VSSQ	DQ5
J	VDDL	VREF	VSS	VSSDL	CK	VDD
K		CKE	$\overline{WE}$	$\overline{RAS}$	$\overline{CK}$	ODT
L	BA2	BA0	BA1	$\overline{CAS}$	$\overline{CS}$	
M		A10	A1	A2	A0	VDD
N	VSS	A3	A5	A6	A4	
P		A7	A9	A11	A8	VSS
L	VDD	A12	A14,NC	A15,NC	A13,NC	
T						
U						
V						
W	NC	NC			NC	NC

1. The thick line area indicates the minimum ball out for x4 and x8 DDR2 SDRAMs.

2. Above coordinates of ball out corresponds to x4 and x8 PCB symbol.

3. NC balls will not be connected to anything on the DRAM. They will be either open or tied to VDD/VDDQ on the DIMM. Ball E2 (NU/$\overline{RDQS}$) will be open on the x8 based DIMMs.

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Pin Assignments for Stacked x4 Ballout with Support Balls (Top View)

(MO-242 variation AD, 71 Balls FBGA 0.8mm x 0.8mm pitch)

x4 Ballout of DDR2 SDRAMs for Stacked DIMM (Top view)

	1	2	3	7	8	9
A	NC	NC			NC	NC
B						
C						
D						
E	VDD	NC	VSS	VSSQ	$\overline{\text{DQS}}$	VDDQ
F	NC	VSSQ	DM	DQS	VSSQ	NC
G	VDDQ	DQ1	VDDQ	VDDQ	DQ0	VDDQ
H	NC	VSSQ	DQ3	DQ2	VSSQ	NC
J	VDDL	VREF	VSS	VSSDL	CK	VDD
K		CKE0	$\overline{\text{WE}}$	$\overline{\text{RAS}}$	$\overline{\text{CK}}$	ODT0
L	BA2	BA0	BA1	$\overline{\text{CAS}}$	$\overline{\text{CS0}}$	$\overline{\text{CS1}}$
M	CKE1	A10	A1	A2	A0	VDD
N	VSS	A3	A5	A6	A4	ODT1
P		A7	A9	A11	A8	VSS
L	VDD	A12	A14,NC	A15,NC	A13,NC	
T						
U						
V						
W	NC	NC			NC	NC

1. The thick line area indicates the minimum ball out for x4 and x8 DDR2 SDRAMs.

2. Above coordinates of ball out corresponds to stacked x4 PCB symbol.

3. NC balls will not be connected to anything on the DRAM. They will be either open or tied to VDD/VDDQ on the DIMM.

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Pin Assignments for x4 and x8 Ballouts with Support Balls (Top View)

(MO-207 variation DL-z, 92 Balls FBGA 0.8mm x 0.8mm pitch)

x4 Ballout of DDR2 SDRAMs (Top view)

	1	2	3	7	8	9
A	NC	NC			NC	NC
B						
C						
D	VDD	NC	VSS	VSS	NC	VDD
E	NC	NC	NC	NC	NC	NC
F	NC	NC	NC	NC	NC	NC
G	NC	NC	NC	NC	NC	NC
H	VDD	NC	VSS	VSS	$\overline{DQS}$	VDD
J	NC	VSS	DM	DQS	VSS	NC
K	VDD	DQ1	VDD	VDD	DQ0	VDD
L	NC	VSS	DQ3	DQ2	VSS	NC
M	VDD	VREF	VSS	VSS	CK	VDD
N		CKE	$\overline{WE}$	$\overline{RAS}$	$\overline{CK}$	ODT
P	BA2	BA0	BA1	$\overline{CAS}$	$\overline{CS}$	
R		A10/AP	A1	A2	A0	VDD
T	VSS	A3	A5	A6	A4	
U		A7	A9	A11	A8	VSS
V	VDD	A12	A14,NC	A15,NC	A13,NC	
W						
Y						
AA	NC	NC			NC	NC

x8 Ballout of DDR2 SDRAMs (Top view)

	1	2	3	7	8	9
A	NC	NC			NC	NC
B						
C						
D	VDD	NC	VSS	VSS	NC	VDD
E	NC	NC	NC	NC	NC	NC
F	NC	NC	NC	NC	NC	NC
G	NC	NC	NC	NC	NC	NC
H	VDD	$\frac{NU/}{RDQS}$	VSS	VSS	$\overline{DQS}$	VDDQ
J	DQ6	VSS	DM/ RDQS	DQS	VSS	DQ7
K	VDD	DQ1	VDD	VDD	DQ0	VDD
L	DQ4	VSSQ	DQ3	DQ2	VSS	DQ5
M	VDD	VREF	VSS	VSS	CK	VDD
N		CKE	$\overline{WE}$	$\overline{RAS}$	$\overline{CK}$	ODT
P	BA2	BA0	BA1	$\overline{CAS}$	$\overline{CS}$	
R		A10/AP	A1	A2	A0	VDD
T	VSS	A3	A5	A6	A4	
U		A7	A9	A11	A8	VSS
V	VDD	A12	A14,NC	A15,NC	A13,NC	
W						
Y						
AA	NC	NC			NC	NC

1. The thick line area indicates the minimum ball out for x4 and x8 DDR2 SDRAMs.

2. Above coordinates of ball out corresponds to x4 and x8 PCB Symbol.

3. NC balls will not be connected to anything on the DRAM. They will be either open or tied to VDD/VDDQ on the DIMM. Ball H2 (NU/$\overline{RDQS}$) will be open on the x8 based DIMMs.

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Pin Assignments for Stacked x4 with Support Balls (Top View)

(MO-242 variation AC, 95 Balls FBGA 0.8mm x 0.8mm pitch)

x4 Ballout of DDR2 SDRAMs for Stacked DIMM (Top view)

	1	2	3		7	8	9
A	NC	NC				NC	NC
B							
C							
D	VDD	NC	VSS		VSS	NC	VDD
E	NC	NC	NC		NC	NC	NC
F	NC	NC	NC		NC	NC	NC
G	NC	NC	NC		NC	NC	NC
H	VDD	NC	VSS		VSS	$\overline{\text{DQS}}$	VDD
J	NC	VSS	DM		DQS	VSS	NC
K	VDD	DQ1	VDD		VDD	DQ0	VDD
L	NC	VSS	DQ3		DQ2	VSS	NC
M	VDD	VREF	VSS		VSS	CK	VDD
N		CKE	$\overline{\text{WE}}$		$\overline{\text{RAS}}$	$\overline{\text{CK}}$	ODT0
P	BA2	BA0	BA1		$\overline{\text{CAS}}$	$\overline{\text{CS0}}$	$\overline{\text{CS1}}$
R		A10/AP	A1		A2	A0	VDD
T	VSS	A3	A5		A6	A4	ODT1
U		A7	A9		A11	A8	VSS
V	VDD	A12	A14,NC		A15,NC	A13,NC	
W							
Y							
AA	NC	NC				NC	NC

1. The thick line area indicates the minimum ball out for x4 and x8 DDR2 SDRAMs.

2. Above coordinates of ball out corresponds to stacked x4 PCB Symbol.

3. NC balls will not be connected to anything on the DRAM. They will be either open or tied to VDD/VDDQ on the DIMM.

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Component Details: **DDR2 SDRAM Fully Buffered DIMM Design Specification**

Pin Assignments for x4 and x8 Ballouts with Support Balls (Top View)

(MO-207 variation DK-z, 84 Balls FBGA 0.8mm x 0.8mm pitch)

x4 Ballout of DDR2 SDRAMs (Top view)

	1	2	3	7	8	9
A	VDD	NC	VSS	VSS	NC	VDD
B	NC	NC	NC	NC	NC	NC
C	NC	NC	NC	NC	NC	NC
D	NC	NC	NC	NC	NC	NC
E	VDD	NC	VSS	VSS	$\overline{DQS}$	VDD
F	NC	VSS	DM	DQS	VSS	NC
G	VDD	DQ1	VDD	VDD	DQ0	VDD
H	NC	VSS	DQ3	DQ2	VSS	NC
J	VDD	VREF	VSS	VSS	CK	VDD
K		CKE	$\overline{WE}$	$\overline{RAS}$	$\overline{CK}$	ODT
L	BA2	BA0	BA1	$\overline{CAS}$	$\overline{CS}$	
M		A10/AP	A1	A2	A0	VDD
N	VSS	A3	A5	A6	A4	
P		A7	A9	A11	A8	VSS
R	VDD	A12	A14,NC	A15,NC	A13,NC	

x8 Ballout of DDR2 SDRAMs (Top view)

	1	2	3	7	8	9
A	VDD	NC	VSS	VSS	NC	VDD
B	NC	NC	NC	NC	NC	NC
C	NC	NC	NC	NC	NC	NC
D	NC	NC	NC	NC	NC	NC
E	VDD	$\frac{NU/}{RDQS}$	VSS	VSS	$\overline{DQS}$	VDDQ
F	DQ6	VSS	DM/ RDQS	DQS	VSS	DQ7
G	VDD	DQ1	VDD	VDD	DQ0	VDD
H	DQ4	VSSQ	DQ3	DQ2	VSS	DQ5
J	VDD	VREF	VSS	VSS	CK	VDD
K		CKE	$\overline{WE}$	$\overline{RAS}$	$\overline{CK}$	ODT
L	BA2	BA0	BA1	$\overline{CAS}$	$\overline{CS}$	
M		A10/AP	A1	A2	A0	VDD
N	VSS	A3	A5	A6	A4	
P		A7	A9	A11	A8	VSS
R	VDD	A12	A14,NC	A15,NC	A13,NC	

1. The thick line area indicates the minimum ball out for x4 and x8 DDR2 SDRAMs.

2. Above coordinates of ball out corresponds to x4 and x8 PCB Symbol.

3. NC balls will not be connected to anything on the DRAM. They will be either open or tied to VDD/VDDQ on the DIMM. Ball E2 (NU/$\overline{RDQS}$) will be open on the x8 based DIMMs.

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Pin Assignments for Stacked x4 Ballouts with Support Balls (Top View)

(MO-242 variation AD, 87 Balls FBGA 0.8mm x 0.8mm pitch)

x4 Ballout of DDR2 SDRAMs for Stacked DIMM (Top view)

	1	2	3		7	8	9
A	VDD	NC	VSS		VSS	NC	VDD
B	NC	NC	NC		NC	NC	NC
C	NC	NC	NC		NC	NC	NC
D	NC	NC	NC		NC	NC	NC
E	VDD	NC	VSS		VSS	$\overline{\text{DQS}}$	VDD
F	NC	VSS	DM		DQS	VSS	NC
G	VDD	DQ1	VDD		VDD	DQ0	VDD
H	NC	VSS	DQ3		DQ2	VSS	NC
J	VDD	VREF	VSS		VSS	CK	VDD
K		CKE	$\overline{\text{WE}}$		$\overline{\text{RAS}}$	$\overline{\text{CK}}$	ODT0
L	BA2	BA0	BA1		$\overline{\text{CAS}}$	$\overline{\text{CS}}$	$\overline{\text{CS1}}$
M		A10/AP	A1		A2	A0	VDD
N	VSS	A3	A5		A6	A4	ODT1
P		A7	A9		A11	A8	VSS
R	VDD	A12	A14,NC		A15,NC	A13,NC	

1. The thick line area indicates the minimum ball out for x4 and x8 DDR2 SDRAMs.

2. Above coordinates of ball out corresponds to stacked x4 PCB Symbol on PCB

3. NC balls will not be connected to anything on the DRAM. They will be either open or tied to VDD/VDDQ on the DIMM.

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Pin Assignments for x4 and x8 PCB Symbol (Top View)

x4 Common Symbol on PCB (Top view)

	1	2	3	7	8	9
A	NU	NU			NU	NU
B						
C						
D	VDD	NU	VSS	VSS	NU	VDD
E	NU	NU	NU	NU	NU	NU
F	NU	NU	NU	NU	NU	NU
G	NU	NU	NU	NU	NU	NU
H	VDD	NU	VSS	VSS	$\overline{DQS}$	VDD
J	NU	VSS	DM	DQS	VSS	NU
K	VDD	DQ1	VDD	VDD	DQ0	VDD
L	NU	VSS	DQ3	DQ2	VSS	NU
M	VDD	VREF	VSS	VSS	CK	VDD
N		CKE	$\overline{WE}$	$\overline{RAS}$	$\overline{CK}$	ODT
P	BA2	BA0	BA1	$\overline{CAS}$	$\overline{CS}$	
R		A10/AP	A1	A2	A0	VDD
T	VSS	A3	A5	A6	A4	
U		A7	A9	A11	A8	VSS
V	VDD	A12	A14	A15	A13	
W						
Y						
AA	NU	NU			NU	NU
AB	NU	NU			NU	NU

x8 Common Symbol on PCB (Top view)

	1	2	3	7	8	9
A	NU	NU			NU	NU
B						
C						
D	VDD	NU	VSS	VSS	NU	VDD
E	NU	NU	NU	NU	NU	NU
F	NU	NU	NU	NU	NU	NU
G	NU	NU	NU	NU	NU	NU
H	VDD	NC	VSS	VSS	$\overline{DQS}$	VDDQ
J	DQ6	VSS	DM/ RDQS	DQS	VSS	DQ7
K	VDD	DQ1	VDD	VDD	DQ0	VDD
L	DQ4	VSSQ	DQ3	DQ2	VSS	DQ5
M	VDD	VREF	VSS	VSS	CK	VDD
N		CKE	$\overline{WE}$	$\overline{RAS}$	$\overline{CK}$	ODT
P	BA2	BA0	BA1	$\overline{CAS}$	$\overline{CS}$	
R		A10/AP	A1	A2	A0	VDD
T	VSS	A3	A5	A6	A4	
U		A7	A9	A11	A8	VSS
V	VDD	A12	A14	A15	A13	
W						
Y						
AA	NU	NU			NU	NU
AB	NU	NU			NU	NU

1. Above coordinates of symbol corresponds to x4 and x8 ballouts of the DDR2 SDRAMs.

2. “NC” means that a solder pad is present and is not connected to any signal on the PCB. NC solder pads may be mated with any of the balls of an SDRAM. On the FB-DIMM x8 symbol, only ball H2 is NC.

3. “NU” means that the solder pad is present and may or may not be electrically connected to an active signal on the PCB. NU solder pads may only be mated with the NC ball of an SDRAM. On FB-DIMM, the NU solder pads will be either open, or connected to Vdd/VddQ. The NU pad may be a continuation of a surface plane utilized for power delivery purposes, thus it must only mate to a NC ball on the SDRAM.

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Pin Assignments for Stacked x4 PCB Symbol (Top View)

x4 Common Symbol on PCB for Stacked DIMM (Top view)

	1	2	3	7	8	9
A	NU	NU			NU	NU
B						
C						
D	VDD	NU	VSS	VSS	NU	VDD
E	NU	NU	NU	NU	NU	NU
F	NU	NU	NU	NU	NU	NU
G	NU	NU	NU	NU	NU	NU
H	VDD	NU	VSS	VSS	$\overline{DQS}$	VDD
J	NU	VSS	DM	DQS	VSS	NU
K	VDD	DQ1	VDD	VDD	DQ0	VDD
L	NU	VSS	DQ3	DQ2	VSS	NU
M	VDD	VREF	VSS	VSS	CK	VDD
N		CKE0	$\overline{WE}$	$\overline{RAS}$	$\overline{CK}$	ODT0
P	BA2	BA0	BA1	$\overline{CAS}$	$\overline{CS0}$	$\overline{CS1}$
R	CKE1	A10/AP	A1	A2	A0	VDD
T	VSS	A3	A5	A6	A4	ODT1
U		A7	A9	A11	A8	VSS
V	VDD	A12	A14	A15	A13	
W						
Y						
AA	NU	NU			NU	NU
AB	NU	NU			NU	NU

1. Above coordinates of symbol corresponds to stacked x4 ballout of the DDR2 SDRAMs.

2. “NU” means that the solder pad is present and may or may not be electrically connected to an active signal on the PCB. NU solder pads may only be mated with the NC ball of an SDRAM. On FB-DIMM, the NU solder pads will be either open, or connected to Vdd/VddQ. The NU pad may be a continuation of a surface plane utilized for power delivery purposes, thus it must only mate to a NC ball on the SDRAM.

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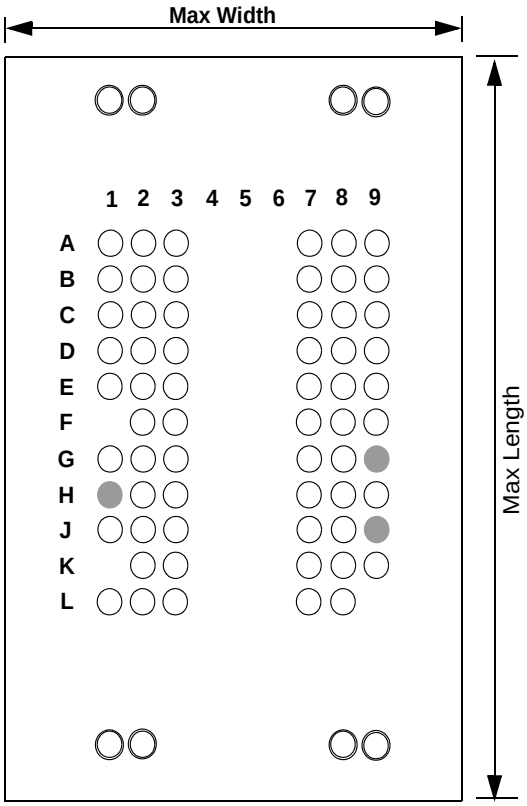
Component Details

Supported SDRAM Component Maximum size for 256Mb to 4Gb, DDR2 SDRAM

Raw Card	Package Type	Supported DRAM Outline (Width x Length) max. (mm)			
		MO-207 Variation			
		DJ-z (60 pins)	DM-z (68 pins)	DL-z (92 pins)	DK-z (84 pins)
A	Planar	12.4 x 15	12.4 x 18	12.4 x 21	12.4 x 21
B,C	Planar	11.4 [2] (12.4 [1,2]) x 15	11.4 [2] (12.4 [1,2]) x 18	11.4 [2] (12.4 [1,2]) x 21[3]	11.4 [2] (12.4 [1,2]) x 21
E	Planar	11 x 11.5	--	--	--
H	Planar	12[4] x 11	--	--	--
		MO-242 Variation			
		AA (63 pins)	AD (71 pins)	AC (95 pins)	AB (87 pins)
D,J	Stacked	11.4 [2] (12.4 [1,2]) x 15	11.4 [2] (12.4 [1,2]) x 18	11.4 [2] (12.4 [1,2]) x 21[3]	11.4 [2] (12.4 [1,2]) x 21

1. supported only if no-decoupling capacitor are placed in between the DRAMs
2. 0.4 mm DRAM to DRAM spacing
3 Heat sink attachment may modify the max DRAM length that will fit to 18.6mm
4. Heat sink attachment may modify the max DRAM width that will fit to 11.5mm

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Note: Double circles indicate the location of support balls of Variation DM-z
Gray circles indicate the balls for stacked only

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Architecture

Advanced Memory Buffer Pin Description

Pin Name	Pin Description	Count
FB-DIMM Channel Signals		**99**
SCK	System Clock Input, positive line	1
$\overline{\text{SCK}}$	System Clock Input, negative line	1
PN[13:0]	Primary Northbound Data, positive lines	14
$\overline{\text{PN}}$[13:0]	Primary Northbound Data, negative lines	14
PS[9:0]	Primary Southbound Data, positive lines	10
$\overline{\text{PS}}$[9:0]	Primary Southbound Data, negative lines	10
SN[13:0]	Secondary Northbound Data, positive lines	14
$\overline{\text{SN}}$[13:0]	Secondary Northbound Data, negative lines	14
SS[9:0]	Secondary Southbound Data, positive lines	10
$\overline{\text{SS}}$[9:0]	Secondary Southbound Data, negative lines	10
FBDRES	To an external precision calibration resistor connected to Vcc	1
DDR2 Interface Signals		**175**
DQS[8:0]	Data Strobes, positive lines	9
$\overline{\text{DQS}}$[8:0]	Data Strobes, negative lines	9
DQS[17:9]/DM[8:0]	Data Strobes (x4 DRAM only), positive lines. These signals are driven low to x8 DRAM on writes.	9
$\overline{\text{DQS}}$[17:9]	Data Strobes (x4 DRAM only), negative lines	9
DQ[63:0]	Data	64
CB[7:0]	Checkbits	8
A[15:0]A, A[15:0]B	Addresses. A10 is part of the pre-charge command	32
BA[2:0]A, BA[2:0]B	Bank Addresses	6
$\overline{\text{RAS}}$A, $\overline{\text{RAS}}$B	Part of command, with $\overline{\text{CAS}}$, $\overline{\text{WE}}$, and $\overline{\text{CS}}$[1:0].	2
$\overline{\text{CAS}}$A, $\overline{\text{CAS}}$B	Part of command, with $\overline{\text{RAS}}$, $\overline{\text{WE}}$, and $\overline{\text{CS}}$[1:0].	2
$\overline{\text{WE}}$A, $\overline{\text{WE}}$B	Part of command, with $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, and $\overline{\text{CS}}$[1:0].	2
ODTA, ODTB	On-die Termination Enable	2
CKE[1:0]A, CKE[1:0]B	Clock Enable (one per rank)	4
$\overline{\text{CS}}$[1:0]A, $\overline{\text{CS}}$[1:0]B	Chip Select (one per rank)	4
CLK[3:0]	CLK[1:0] used on 9 and 18 device DIMMs, CLK[3:0] used on 36 device DIMMs. CLK[3:2] should be output disabled when not in use.	4
$\overline{\text{CLK}}$[3:0]	Negative lines for CLK[3:0]	4
DDRC_C14	DDR Compensation: Common return pin for DDRC_B18 and DDRC_C18.	1
DDRC_B18	DDR Compensation: Resistor connected to common return pin DDRC_C14	1
DDRC_C18	DDR Compensation: Resistor connected to common return pin DDRC_C14	1
DDRC_B12	DDR Compensation: Resistor connected to V_{SS}	1
DDRC_C12	DDR Compensation: Resistor connected to V_{DD}	1

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Advanced Memory Buffer Pin Description

SPD Bus Interface Signals		**5**
SCL	Serial Presence Detect (SPD) Clock Input	1
SDA	SPD Data Input / Output	1
SA[2:0]	SPD Address Inputs, also used to select the DIMM number in the AMB	3
Miscellaneous Signals		**163**
PLLTSTO	PLL Clock Observability Output	1
VCCAPLL	Analog VCC for the PLL. Tied with low pass filter to VCC.	1
VSSAPLL	Analog VSS for the PLL. Tied to ground on the AMB die. Do not tie to ground on the DIMM.	1
TEST_pin#	Leave floating on the DIMM	6
TESTLO_pin#	Tie to ground on the DIMM[2]	5
BFUNC	Tie to ground to set functionality as “buffer on DIMM.”	1
$\overline{\text{RESET}}$	AMB reset signal	1
NC	No connect. Many NC are connected to VDD on the DIMM, to lower the impedance of the VDD power islands.	129
RFU	Reserved for Future Use	18
Power/Ground Signals		**213**
V_{CC}	AMB Core Power (1.5 Volt)	24
V_{CCFBD}	AMB Channel I/O Power (1.5 Volt)	8
V_{DD}	AMB DRAM I/O Power (1.8 Volt)	24
V_{DDSPD}	SPD Power (3.3 Volt)	1
V_{SS}	Ground	156
	Total	**655**

1. System Clock Signals SCK and $\overline{\text{SCK}}$ switch at one half the DRAM CK/$\overline{\text{CK}}$ frequency.
2. TESTLO_AB20 and TESTLO_AC20 should be configured for debug purposes on prototype DIMMs: each pin should have a zero ohm resistor pulldown to ground, and an unpopulated resistor pullup to VCC. These resistors can be replaced on production DIMMs with a direct connection to ground.

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Pin Assignments for the Advanced Memory Buffer (AMB) (Top View)

655-Ball LFBGA 0.8 mm x 0.8 mm pitch [MO-TBD]

Left Side

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
A			V_{SS}	DQ26	DQ12	V_{DD}	DQS10	DQ13	V_{DD}	$\overline{DQS1}$	DQ10	V_{DD}	TEST	V_{DD}	V_{DD}
B		V_{DD}	DQS3	$\overline{DQS3}$	V_{SS}	DQ14	$\overline{DQS10}$	V_{SS}	DQ11	DQS1	V_{SS}	DDRC	TESTLO	V_{DD}	V_{SS}
C	V_{SS}	DQS2	DQ18	V_{SS}	DQ4	$\overline{DQS9}$	V_{SS}	DQ15	DQ9	V_{SS}	DQ8	DDRC	V_{SS}	DDRC	DQS17
D	DQ19	$\overline{DQS2}$	V_{SS}	DQ16	DQ24	V_{SS}	DQS9	DQ7	V_{SS}	DQ3	DQS0	V_{SS}	$\overline{DQS8}$	DQS8	V_{DD}
E	DQ21	V_{SS}	DQ17	DQ29	V_{SS}	DQ25	DQ6	V_{SS}	DQ5	DQ1	V_{SS}	DQ0	CB1	V_{SS}	CB2
F	V_{SS}	DQ20	DQ23	V_{SS}	DQ31	DQ27	V_{SS}	TESTLO	TEST	V_{SS}	$\overline{DQS0}$	DQ2	V_{DD}	CB0	CB3
G	$\overline{DQS11}$	DQS11	NC	NC	NC	V_{SS}	DQS12	$\overline{DQS12}$	NC	NC	NC	BFUNC	RFU	RFU	RFU
H	DQ22	V_{SS}	NC	NC	NC	DQ28	DQ30	V_{SS}	NC	NC	NC	V_{SS}	V_{DD}	V_{SS}	V_{DD}
J	V_{SS}	CLK2	NC	NC	NC	BA1A	V_{SS}	CKE1A	NC	NC	NC	V_{DD}	V_{SS}	V_{DD}	V_{SS}
K	$\overline{CLK2}$	CLK0	NC	NC	NC	V_{SS}	$\overline{WEA}$	$\overline{RASA}$	NC	NC	NC	V_{SS}	V_{CC}	V_{SS}	V_{CC}
L	$\overline{CLK0}$	V_{SS}	NC	NC	NC	A0A	CKE0A	V_{SS}	NC	NC	NC	V_{CC}	V_{SS}	V_{CC}	V_{SS}
M	ODT0A	RFU	NC	NC	NC	$\overline{CASA}$	V_{SS}	BA2A	NC	NC	NC	V_{SS}	V_{CC}	V_{SS}	V_{CC}
N	$\overline{CS1A}$	$\overline{CS0A}$	NC	NC	NC	V_{SS}	BA0A	A10A	NC	NC	NC	V_{CC}	V_{SS}	V_{CC}	V_{SS}
P	A6A	V_{SS}	NC	NC	NC	A2A	A1A	A3A	NC	NC	NC	V_{SS}	V_{CC}	V_{SS}	V_{CC}
R	V_{SS}	A8A	NC	NC	NC	A11A	V_{SS}	A5A	NC	NC	NC	V_{CC}	V_{SS}	V_{CC}	V_{SS}
T	A4A	A13A	NC	NC	NC	V_{SS}	A9A	A7A	NC	NC	NC	V_{SS}	V_{CC}	V_{SS}	V_{CC}
U	PN0	$\overline{PN0}$	NC	NC	NC	A15A	A14A	A12A	NC	NC	NC	RFU	V_{CCFBD}	V_{SS}	V_{SS}
V	PN1	$\overline{PN1}$	V_{SS}	SN0	$\overline{SN0}$	V_{CCFBD}	V_{SS}	V_{CCFBD}	V_{SS}	RFU[a]	RFU[a]	V_{CCFBD}	V_{SS}	V_{SS}	V_{SS}
W	PN2	$\overline{PN2}$	V_{SS}	SN1	$\overline{SN1}$	$\overline{SN3}$	$\overline{SN4}$	$\overline{SN5}$	$\overline{SN13}$	$\overline{SN12}$	$\overline{SN6}$	$\overline{SN7}$	$\overline{SN8}$	$\overline{SN9}$	$\overline{SN10}$
Y	PN3	$\overline{PN3}$	V_{SS}	SN2	$\overline{SN2}$	SN3	SN4	SN5	SN13	SN12	SN6	SN7	SN8	SN9	SN10
AA	V_{SS}	PN4	$\overline{PN4}$	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}
AB		V_{SS}	$\overline{RESET}$	$\overline{PN5}$	$\overline{PN13}$	RFU[a]	$\overline{PN12}$	$\overline{PN6}$	$\overline{PN7}$	$\overline{PN8}$	$\overline{PN9}$	V_{SSAPLL}	V_{CCAPLL}	$\overline{PN10}$	$\overline{PN11}$
AC			V_{SS}	PN5	PN13	RFU[a]	PN12	PN6	PN7	PN8	PN9	FBDRES	PLL TSTO	PN10	PN11
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15

a. These pin positions are reserved for forwarded clocks to be used in future AMB implementations

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Right Side

	16	17	18	19	20	21	22	23	24	25	26	27	28	29
A	V_{DD}	TEST	V_{DD}	DQ52	DQS15	V_{DD}	DQ49	$\overline{DQS}$6	V_{DD}	DQ48	DQ38	V_{DD}		
B	V_{DD}	TEST	DDRC	V_{SS}	$\overline{DQS}$15	DQ53	V_{SS}	DQS6	DQ50	V_{SS}	$\overline{DQS}$13	DQS13	V_{SS}	
C	$\overline{DQS}$17	V_{SS}	DDRC	DQ54	V_{SS}	DQ55	DQ51	V_{SS}	DQS7	DQ56	V_{SS}	DQ46	$\overline{DQS}$14	V_{DD}
D	CB6	CB7	V_{SS}	DQS16	DQ63	V_{SS}	DQ59	$\overline{DQS}$7	V_{SS}	DQ36	DQ44	V_{SS}	DQS14	DQ47
E	V_{SS}	CB5	$\overline{DQS}$16	V_{SS}	DQ61	DQ57	V_{SS}	DQ58	DQ39	V_{SS}	DQ33	DQ45	V_{SS}	DQ41
F	CB4	V_{DD}	DQ62	DQ60	V_{SS}	TEST	TEST	V_{SS}	DQ37	DQ35	V_{SS}	$\overline{DQS}$5	DQ43	V_{SS}
G	TESTLO	RFU	RFU	NC	NC	NC	DQS4	$\overline{DQS}$4	V_{SS}	NC	NC	NC	DQS5	DQ40
H	V_{SS}	V_{DD}	V_{SS}	NC	NC	NC	V_{SS}	DQ34	DQ32	NC	NC	NC	V_{SS}	DQ42
J	V_{DD}	V_{SS}	V_{DD}	NC	NC	NC	$\overline{RAS}$B	V_{SS}	RFU	NC	NC	NC	$\overline{CLK}$3	V_{SS}
K	V_{SS}	V_{CC}	V_{SS}	NC	NC	NC	ODT0B	$\overline{CS}$1B	V_{SS}	NC	NC	NC	$\overline{CLK}$1	CLK3
L	V_{CC}	V_{SS}	V_{CC}	NC	NC	NC	V_{SS}	$\overline{CAS}$B	$\overline{WE}$B	NC	NC	NC	V_{SS}	CLK1
M	V_{SS}	V_{CC}	V_{SS}	NC	NC	NC	$\overline{CS}$0B	V_{SS}	BA1B	NC	NC	NC	CKE0B	V_{SS}
N	V_{CC}	V_{SS}	V_{CC}	NC	NC	NC	A0B	A2B	V_{SS}	NC	NC	NC	BA0B	BA2B
P	V_{SS}	V_{CC}	V_{SS}	NC	NC	NC	V_{SS}	A4B	A1B	NC	NC	NC	V_{SS}	CKE1B
R	V_{CC}	V_{SS}	V_{CC}	NC	NC	NC	A6B	V_{SS}	A10B	NC	NC	NC	A3B	V_{SS}
T	V_{SS}	V_{CC}	V_{SS}	NC	NC	NC	A11B	A9B	V_{SS}	NC	NC	NC	A7B	A5B
U	V_{SS}	V_{CCFBD}	RFU	NC	NC	NC	A8B	A15B	A14B	SA0	SCL	SDA	$\overline{PS}$8	PS8
V	V_{CCFBD}	V_{SS}	V_{CCFBD}	V_{SS}	V_{CCFBD}	RFU[a]	RFU[a]	V_{SS}	A13B	A12 B	SA2	SA1	$\overline{PS}$7	PS7
W	V_{SS}	$\overline{SS}$0	$\overline{SS}$1	$\overline{SS}$2	$\overline{SS}$3	$\overline{SS}$4	$\overline{SS}$9	$\overline{SS}$5	$\overline{SS}$6	$\overline{SS}$7	$\overline{SS}$8	V_{SS}	$\overline{PS}$6	PS6
Y	V_{SS}	SS0	SS1	SS2	SS3	SS4	SS9	SS5	SS6	SS7	SS8	V_{SS}	$\overline{PS}$5	PS5
AA	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	$\overline{PS}$9	PS9	V_{SS}
AB	V_{SS}	$\overline{SN}$11	V_{SS}	SCK	TESTLO	$\overline{PS}$0	$\overline{PS}$1	$\overline{PS}$2	$\overline{PS}$3	$\overline{PS}$4	RFU[a]	V_{DDSPD}	V_{SS}	
AC	RFU	SN11	V_{SS}	$\overline{SCK}$	TESTLO	PS0	PS1	PS2	PS3	PS4	RFU[a]	V_{SS}		
	16	17	18	19	20	21	22	23	24	25	26	27	28	29

a. These pin positions are reserved for forwarded clocks to be used in future AMB implementations

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Advanced Memory Buffer (AMB) DRAM Interface Specifications

Please refer to the AMB Specification for all technical requirements.

The following specifications for the AMB constitute the subset which is critical for proper operation of the DDR2 SDRAM interface..

Critical AMB Specifications

Symbol	Parameter	Type	V_{DDQ} = 1.8 V ± 0.1 V		Units	Notes
			Min	Max		
t_{SU}	DQ to DQS/$\overline{DQS}$ setup time (read)	Input		-425	ps	1
t_H	DQ to DQS/$\overline{DQS}$ hold time (read)	Input		825	ps	1
tDVBamb	AMB Data Valid Before DQS	Output	470		ps	1
tDVAamb	AMB Data Valid After DQS	Output	470		ps	1
tCVBamb	C/A/CNTL Valid Before Clock	Output	1030		ps	1
tCVAamb	C/A/CNTL Valid After Clock	Output	890		ps	1
$t_{DQSCKamb}$	DQS/$\overline{DQS}$-to-CK/$\overline{CK}$ output skew	Output	-190	190	ps	1
C_{IN}	Input Capacitance (DQ/DQS/$\overline{DQS}$)		2.0	2.5	pF	1

Note 1: The timing numbers are for example only. Design should be based on the latest AMB component specifications

AMB Sourcing

This document is not intended to be an approved vendor list for support components. Although it is recommended that all DDR2 SDRAM FBDIMM AMBs meet the specifications documented above, it is up to each DIMM producer to select the AMB and AMB vendors which meet these requirements.

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DDR2 Fully Buffered DIMM Details

DDR2 SDRAM Module Configurations (Reference Designs)

Raw Card Version	DIMM		SDRAM		# of SDRAMs	SDRAM Package Type	# of Ranks	# of Banks in SDRAM	# of Address bits row/col/Bank
	Capacity	Organization	Density	Organization					
A	256MB	32Mx72	256Mbit	32Mx8	9	60 Ball FBGA	1	4	13/10/2
	512MB	64Mx72	512Mbit	64Mx8	9	60 Ball FBGA	1	4	14/10/2
	1GB	128Mx72	1Gbit	128Mx8	9	60 Ball FBGA	1	8	14/10/3
	2GB	256Mx72	2Gbit	256Mx8	9	60 Ball FBGA	1	8	15/10/3
	4GB	512Mx72	4Gbit	512Mx8	9	60 Ball FBGA	1	8	16/10/3
B	512MB	64Mx72	256Mbit	32Mx8	18	60 Ball FBGA	2	4	13/10/2
	1GB	128Mx72	512Mbit	64Mx8	18	60 Ball FBGA	2	4	14/10/2
	2GB	256Mx72	1Gbit	128Mx8	18	60 Ball FBGA	2	8	14/10/3
	4GB	512Mx72	2Gbit	256Mx8	18	60 Ball FBGA	2	8	15/10/3
	8GB	1Gx72	4Gbit	512Mx8	18	60 Ball FBGA	2	8	16/10/3
C	512MB	64Mx72	256Mbit	64Mx4	18	60 Ball FBGA	1	4	13/11/2
	1GB	128Mx72	512Mbit	128Mx4	18	60 Ball FBGA	1	4	14/11/2
	2GB	256Mx72	1Gbit	256Mx4	18	60 Ball FBGA	1	8	14/11/3
	4GB	512Mx72	2Gbit	512Mx4	18	60 Ball FBGA	1	8	15/11/3
	8GB	1Gx72	4Gbit	1Gbx4	18	60 Ball FBGA	1	8	16/11/3
D, J, E, H	1GB	64Mx72	256Mbit	64Mx4	36	63 Ball FBGA	2	4	13/11/2
	2GB	128Mx72	512Mbit	128Mx4	36	63 Ball FBGA	2	4	14/11/2
	4GB	256Mx72	1Gbit	256Mx4	36	63 Ball FBGA	2	8	14/11/3
	8GB	512Mx72	2Gbit	512Mx4	36	63 Ball FBGA	2	8	15/11/3
	16GB	1Gx72	4Gbit	1Gbx4	36	63 Ball FBGA	2	8	16/11/3

DDR2 Fully Buffered DIMM Design File Releases

‘Reference’ design file updates will be released as needed. This Fully Buffered DIMM specification will reflect the most recent design files, but may also be updated to reflect clarifications to the specification only; in these cases the design files will not be updated. The following table outlines the most recent design file releases.

Raw Card Version	Specification Revision	Applicable Design File	Notes
A	0.5	TBD	TBD
B	0.5	TBD	TBD
C	0.4	TBD	TBD
D	0.4	TBD	TBD
E	0.41	TBD	TBD
H	0.5	TBD	TBD

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Raw Card Version	Specification Revision	Applicable Design File	Notes
J	0.3	TBD	TBD

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Component Types and Placement

Components shall be surface mounted on one or both sides of the PCB and positioned on the PCB to meet the minimum and maximum trace lengths required for DDR2 SDRAM signals. Bypass capacitors for DDR2 SDRAM devices must be located near the device power pins.

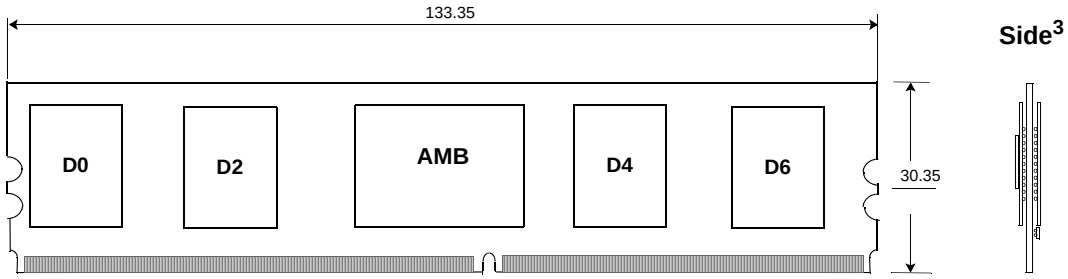
The following layouts suggest placement for the Raw Cards. Exact spacing is not provided, but should be based on manufacturing constraints and signal routing constraints imposed by this design guide.

This example is for reference only; please refer to JEDEC standard MO-256 for details.

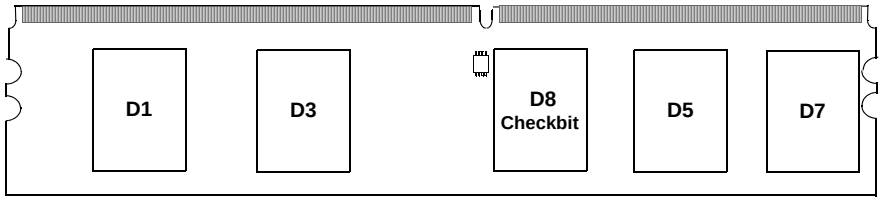
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Raw Card A

Front



Back

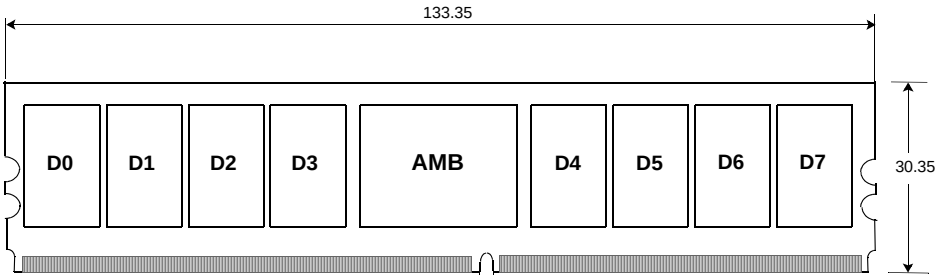


Note 1: All dimensions (in mm) are typical unless otherwise stated.
Note 2: Support for 16.5 mm wide by 21.9 mm tall DRAM footprint.
Note 3: Heat Spreader Assembly not shown, refer to MO-256 for thickness dimensions.

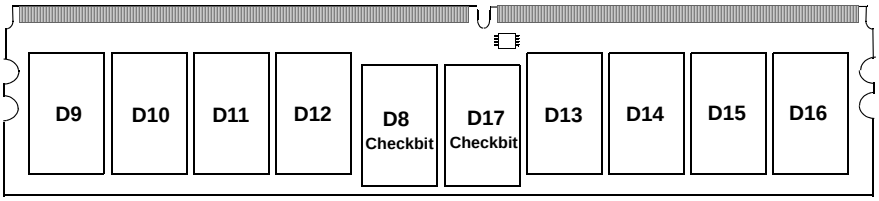
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Raw Cards B and C

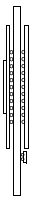
Front



Back



Side[2]



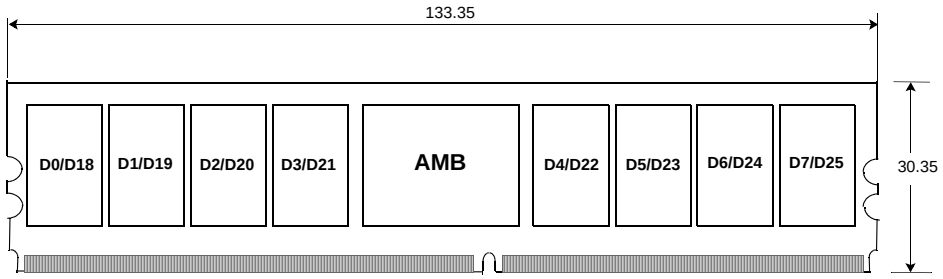
Note 1: All dimensions (in mm) are typical unless otherwise stated.

Note 2: Heat Spreader Assembly not shown, refer to MO-256 for thickness dimensions.

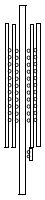
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Raw Cards D and J

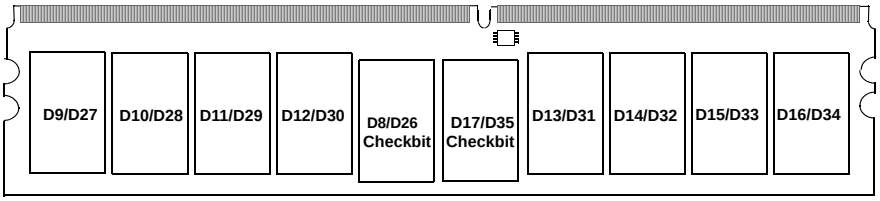
Front



Side[2]



Back

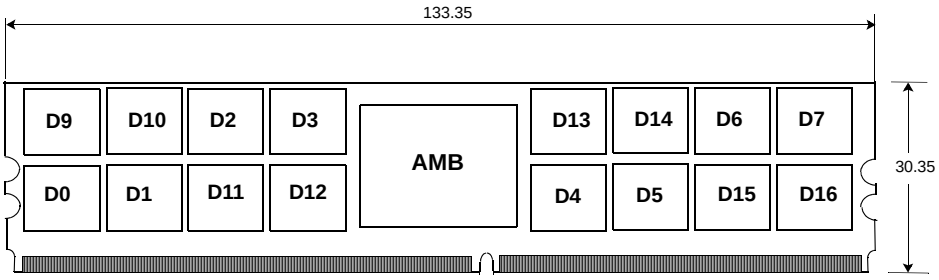


Note 1: All dimensions (in mm) are typical unless otherwise stated.
Note 2: Heat Spreader Assembly not shown, refer to MO-256 for thickness dimensions.

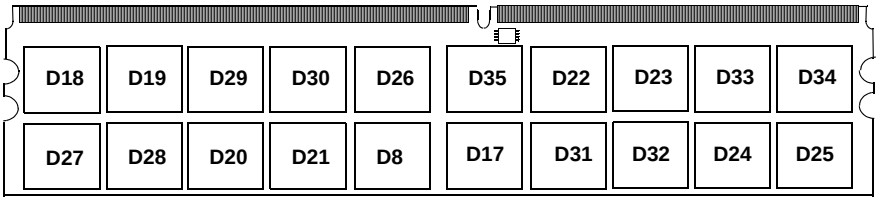
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Raw Cards E and H

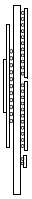
Front



Back



Side[2]



Note 1: All dimensions (in mm) are typical unless otherwise stated.

Note 2: Heat Spreader Assembly not shown, refer to MO-256 for thickness dimensions.

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DDR2 Fully Buffered DIMM Biasing Details

Common AMB Bias Detail

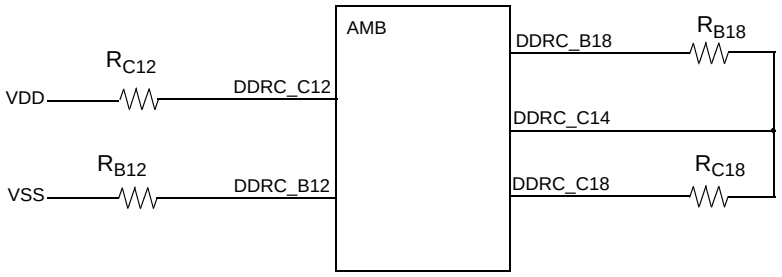
This specification documents the common biasing circuit topology for AMB devices as used on FB-DIMMs. While specific component values are not documented, the circuit topologies are included.

AMBs from different vendors may have specific requirements for BIAS inputs. It is incumbent on users to select correct components to ensure AMB specific requirements are met.

Diagrams are separated by functional groups DDR, PLL, Miscellaneous Explanation of Bias Diagrams.

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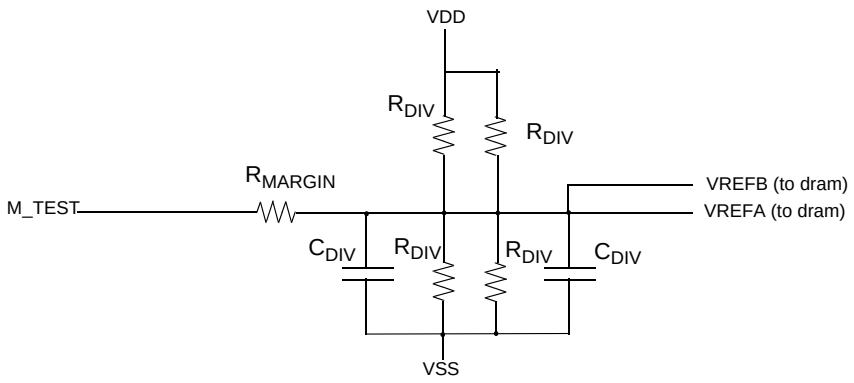
DDR Bias



DDR Bias is composed of compensation resistors that implement compensation control of AMB DDR interface. AMB internal implementation details and component values may vary but the topology shown is sufficient for all AMB devices. Some AMB's may not require these components. See following table of Vendor reference material.

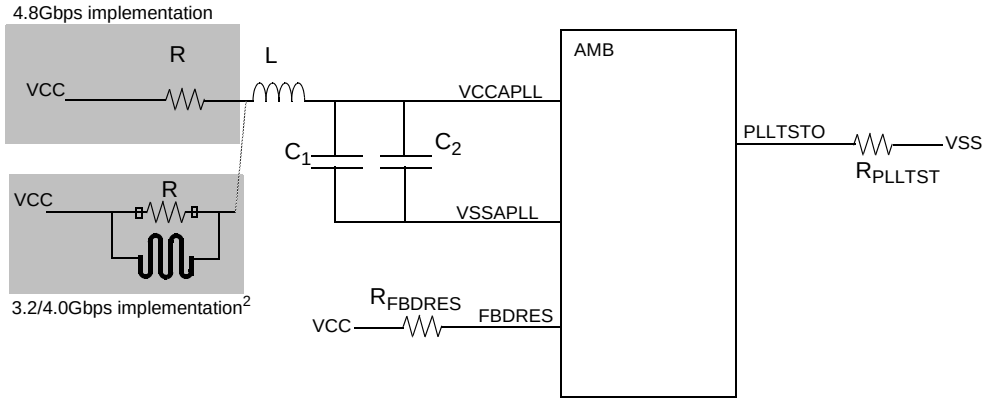
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DDR VREF BIAS



Dram devices require a VREF that tracks VDD/2, Raw Cards generates a trace for each side of the DIMM. Additionally, a test feature M_TEST implements a margin capability to slightly vary VREF for test purposes. While DIMM vendors may utilize their own values, it is recommended that the ratio of Rmargin to Rdiv be 0.015.

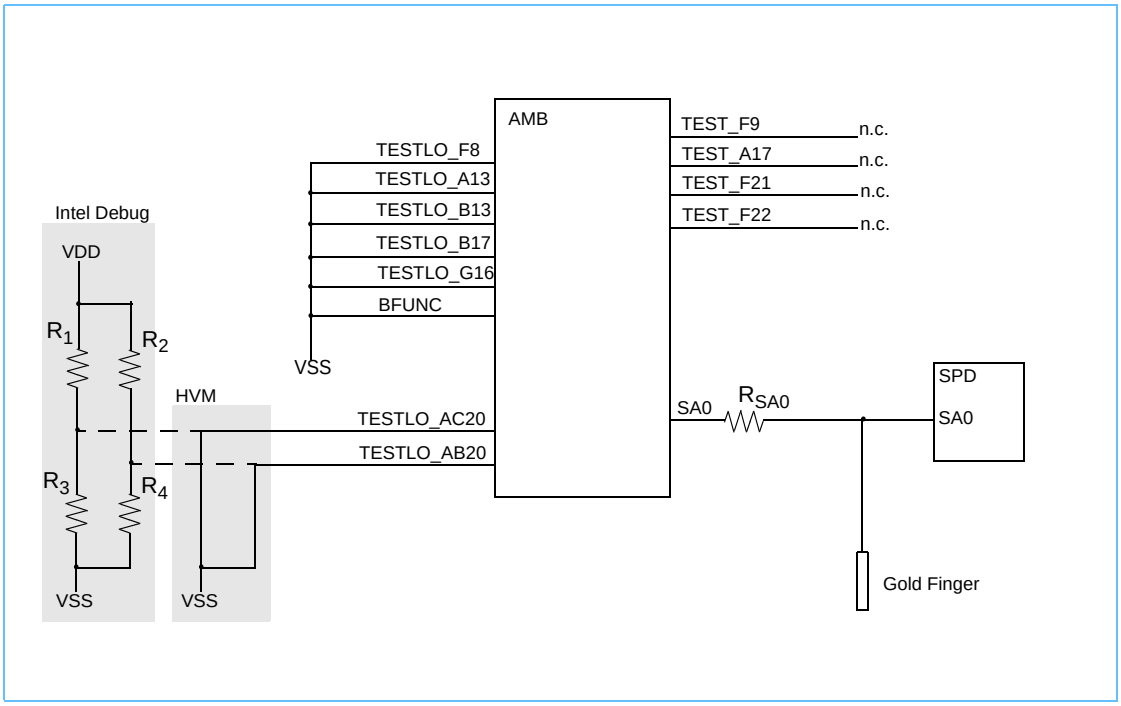
PLL and Channel Bias



NOTE 1: There is no connection to ground from VSSAPLL.
NOTE 2: Users must ensure AMB requirements are met by their implementation. Example, in VCCAPLL network, R implemented as copper trace serpentine may not achieve acceptable tolerances for all AMBs.
NOTE 3: VCC power delivery requirements (as specified for VCC balls) are assumed to be met at inputs of VCCAPLL and FBDRES networks, not at VCCAPLL and FBDRES balls.

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Miscellaneous Bias



NOTE 1: Intel Debug circuit is optional for proprietary development purposes; Production should use HVM option.

NOTE 2: R_{SA0} protects AMB from overvoltage during SPD programing.

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BIAS Components

Diagram	RefDes	Notes	Value
DDR Bias	R1		reference AMB vendor design guide
	R2,		
	R3		
	R4		
DDR VREF Bias	R_{MARGIN}		reference AMB vendor design guide
	R_{DIV}		
	C_{DIV}		
PLL and Channel	R		reference AMB vendor design guide
	L		
	C_1		
	C_2		
	R_{PLLTST}		
	R_{FBDRES}		
Miscellaneous	R_1		reference AMB vendor design guide
	R_2		
	R_3		
	R_4		
	R_{SA0}		

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DDR2 Fully Buffered DIMM Wiring Details

Signal Groups

This specification categorizes DDR SDRAM timing-critical signals into four groups. The signals for the high-speed system and SPD interfaces are also included. The following table summarizes the signals contained in each group.

Signal Group	Signals In Group	Raw Card Version	Notes
System Clock	SCK, $\overline{\text{SCK}}$	A, B, C, D, E, H, J	
System Data Channels	PN[13:0], $\overline{\text{PN}}$[13:0], SN[13:0], $\overline{\text{SN}}$[13:0], PS[9:0], $\overline{\text{PS}}$[9:0], SS[9:0], $\overline{\text{SS}}$[9:0]	A, B, C, D, E, H, J	
DRAM Data, DQS, $\overline{\text{DQS}}$, DM	DQ[63:0],CB[7:0],DQS[17:0],$\overline{\text{DQS}}$[17:0]	A, B, C, D, E, H, J	$\overline{\text{DQS}}$[17:9] not used on R/C A, B $\overline{\text{DQS}}$[8:0] are DM on R/C A, B
DRAM Clock	CK[3:0], $\overline{\text{CK}}$[3:0]	A[1:0], B[1:0], C[1:0], D[3:0], E[3:0], H[3:0], J[3:0]	CK0, CK2 on left CK1, CK3 on right
DRAM Address and Command	A[15:0], BA[2:0], $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$, ODT	A, B, C, D, E, H, J	Two sets, one set for left and one set for right
DRAM Control	$\overline{\text{CS}}$[1:0], CKE[1:0]	A (0), B (1:0) C (0), D (1:0), E[1:0], H[1:0], J[1:0]	Two sets, one set for left and one set for right
SPD	SCL, SDA	A, B, C, D, E, H, J	

General Net Structure Routing Guidelines

Net structures and lengths must satisfy signal quality and setup/hold time requirements for the memory interface. Net structure diagrams for each signal group are shown in the following sections. Each diagram is accompanied by a trace length table that lists the minimum and maximum allowable lengths for each trace segment and/or net.

The general routing requirements are as follows:

- Signals are referenced to Vss layers only

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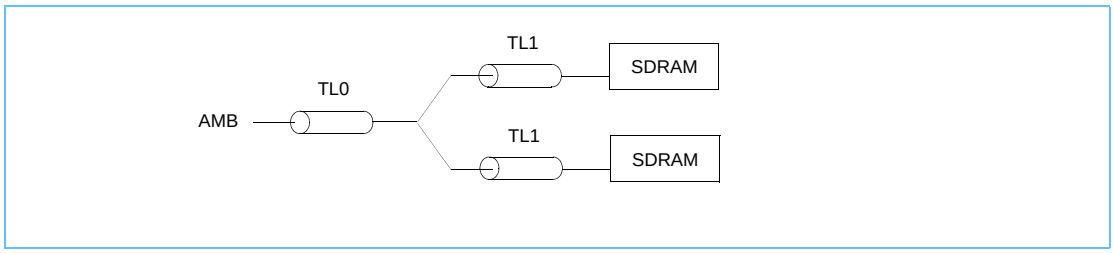
Explanation of Net Structure Diagrams

The net structure routing diagrams provide a reference design example for each raw card version. These designs provide an initial basis for Fully Buffered DIMM designs. The diagrams should be used to determine individual signal wiring on a DIMM for any supported configuration. Only transmission lines (represented as cylinders and labeled with trace length designators “TL”) represent physical trace segments. All other lines are zero in length. To verify DIMM functionality, a full simulation of all signal integrity and timing is required. **The given net structures and trace lengths are not inclusive for all solutions.**

Once the net structure has been determined, the permitted trace lengths for the net structure can be read from the table below each net structure routing diagram. Some configurations require the use of multiple net structure routing diagrams to account for varying load quantities on the same signal. All diagrams define one load as one SDRAM input. **It is highly recommended that the net structure routing data in this document be simulated by the user.**

Net Structure Example

A 1GB dual-rank x72 DIMM using 512Mbit, 64Mx8 SDRAM devices would have a data net structure as shown in the following diagram.



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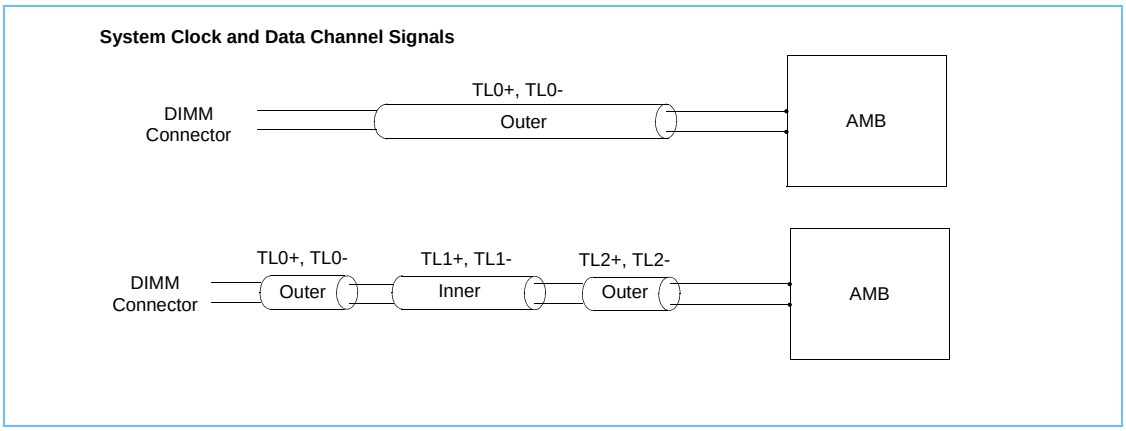
System Clock and Data Channel Net Structures

SCK, $\overline{\text{SCK}}$, PN[13:0], $\overline{\text{PN}}$[13:0], SN[13:0], $\overline{\text{SN}}$[13:0], PS[9:0], $\overline{\text{PS}}$[9:0], SS[9:0], $\overline{\text{SS}}$[9:0]

System Clock and Data Channel traces must be carefully routed to meet the following requirements:

- Signal quality
- Signal loss
- Minimal crosstalk
- Differential signal crosspoint

Net Structure Routing for System Data Channel



Trace Lengths for System Clock Net Structure (SCK, $\overline{\text{SCK}}$)

Raw Card	TL0+/TL0-		TL1+/TL1-		TL2+/TL2-		Sum(TL+)/ Sum(TL-)		Notes
	Min	Max	Min	Max	Min	Max	Min	Max	
A, B	1.9		50.3	51.0	0.6		52.8	53.5	1, 2
C	1.9		50.3	51.0	0.6		52.8	53.5	1, 2
D, J	1.9		50.3	51.0	0.6		52.8	53.5	1, 2
E	1.8	1.9	50.9		0.5	0.6	53.2	53.3	1, 2
H	1.8	2.2	50.6	51.0	0.5	0.6	52.8	53.5	1, 2

1. All trace distances are given in millimeters.
2. TL0+, TL1+ and TL2+ are the lengths of the positive signal of the differential pair. TL0-, TL1- and TL2- are the lengths of the negative signal of the differential pair. The sum of the TL+ and the sum of the TL- must match within +/- 0.1 mm.

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Trace Lengths for Primary Northbound Channel (PN[13:0], $\overline{PN}$[13:0])

Raw Card	TL0+/TL0-		TL1+/TL1-		TL2+/TL2-		Sum(TL+)/ Sum(TL-)		Notes
	Min	Max	Min	Max	Min	Max	Min	Max	
A, B, C	8.1	34.4	NA		NA		8.1	34.4	1, 2
D, J	8.1	34.4	NA		NA		8.1	34.4	1, 2
E	1.6	34.4	0.0	23.6	0.0	0.6	9.2	34.4	1, 2
H	1.6	35.2	0.0	20.5	0.0	3.4	9.2	35.2	1, 2

1. All trace distances are given in millimeters.
2. TL0+, TL1+ and TL2+ are the lengths of the positive signal of the differential pair. TL0-, TL1- and TL2- are the lengths of the negative signal of the differential pair. For sum of TL shorter than 12 mm, the sum of the TL+ and the sum of the TL- must match within +/- 0.5 mm. For sum of TL longer than 12 mm, the sum of the TL+ and the sum of the TL- must match within +/- 0.1 mm.

Trace Lengths for Secondary Northbound Channel (SN[13:0], $\overline{SN}$[13:0])

Raw Card	TL0+/TL0-		TL1+/TL1-		TL2+/TL2-		Sum(TL+)/ Sum(TL-)		Notes
	Min	Max	Min	Max	Min	Max	Min	Max	
A, B, C	1.8		9.1	34.6	0.6		11.5	37.0	1, 2
D, J	1.8		9.1	34.6	0.6		11.5	37.0	1, 2
E	1.5	2.3	9.1	34.3	0.5	0.6	11.7	37.0	1, 2
H	1.5	2.4	9.1	35.2	0.5	0.6	11.7	37.7	1, 2

1. All trace distances are given in millimeters.
2. TL0+, TL1+ and TL2+ are the lengths of the positive signal of the differential pair. TL0-, TL1- and TL2- are the lengths of the negative signal of the differential pair. For sum of TL shorter than 16 mm, the sum of the TL+ and the sum of the TL- must match within +/- 0.5 mm. For sum of TL longer than 16 mm, the sum of the TL+ and the sum of the TL- must match within +/- 0.1 mm.

Trace Lengths for Primary Southbound Channel (PS[9:0], $\overline{PS}$[9:0])

Raw Card	TL0+/TL0-		TL1+/TL1-		TL2+/TL2-		Sum(TL+)/ Sum(TL-)		Notes
	Min	Max	Min	Max	Min	Max	Min	Max	
A, B, C	12.4	40.1	NA		NA		12.4	40.1	1, 2
D, J	12.4	40.1	NA		NA		12.4	40.1	1, 2
E	5.8	40.5	0.0	23.5	0.0	2.4	12.7	40.5	1, 2
H	1.6	41.3	0	24	0.0	4.5	12.4	41.3	1, 2

1. All trace distances are given in millimeters.
2. TL0+, TL1+ and TL2+ are the lengths of the positive signal of the differential pair. TL0-, TL1- and TL2- are the lengths of the negative signal of the differential pair. The sum of the TL+ and the sum of the TL- must match within +/- 0.1 mm.

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Trace Lengths for Secondary Southbound Channel (SS[9:0], SS[9:0])

Raw Card	TL0+		TL1+		TL2+		Sum(TL+) / Sum(TL-)		Notes
	Min	Max	Min	Max	Min	Max	Min	Max	
A, B, C	1.8	2.0	17.1	39.1	0.6	1.4	19.5	42.3	1, 2
D, J	1.8	2.0	17.1	39.1	0.6	1.4	19.5	42.3	1, 2
E	1.6	2.0	19.0	40.1	0.5	0.6	21.4	42.3	1, 2
H	1.6	2.1	17.1	40.1	0.5	0.6	21.4	42.3	1, 2

1. All trace distances are given in millimeters.
2. TL0+, TL1+ and TL2+ are the lengths of the positive signal of the differential pair. TL0-, TL1- and TL2- are the lengths of the negative signal of the differential pair. The sum of the TL+ and the sum of the TL- must match within +/- 0.1 mm.

Pair-to-Pair Spacing Rules for System Data Channel Nets

Net Type	Net Length	Minimum Pair-to-Pair Separation	Notes
Microstrip (outer)	< 20 mm	4.25 x Height	1, 2, 3, 4
Microstrip (outer)	> 20 mm	5.25 x Height	1, 2, 3, 4
Stripline (inner)		3.7 x Height	1, 2, 3, 4

1. Pair-to-pair spacing rules are required to guarantee the crosstalk characteristics of the channel.
2. Separation is defined as a multiple of the dielectric height.
3. Separation between two differential pairs is measured between the closest traces, from the center of one trace to the center of the other trace.
4. For traces with a fine serpentine routing (for length matching) the spacing is measured from the average position of the center of the trace.

Minimum Trace Widths for System Data Channel Nets

Net Type	Absolute Minimum Width	Notes
Microstrip (outer)	0.102 mm	1
Stripline (inner)	0.127 mm	1

1. Minimum trace width is required to guarantee the loss characteristics of the channel.

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Recommended Minimum Trace and Shape Separation Rules

The following table describes recommended minimum spacing for signals, buses and power isles.

Spacing is represented as ratio AG/D where AG is the air gap measurement from feature edge to feature edge and D is the distance between the signal layer and its reference plane. Ratios are calculated based on values from “Example Six Layer Stackup” section.

Design physical constraints (such as limited routing space in fan-out regions etc.) can cause exceptions. These exceptions should be minimized as much as possible since they can put at risk design integrity.

As table below contains recommended minimum values, designer should try to maximize separation whenever possible. As an example, on 10 layers R/C D designer was able to increase DQ to DQ spacing to 3.3 x dielectric height.

Number represent air gap to dielectric height ratio #1		To:						
		DQ	DQS/$\overline{\text{DQS}}$	CK	C/A	Power Island	NB Channel	SB Channel
From:	DQ	2.0	2.0	2.4	2.0	2.0	non adj.	non adj.
	DQS/$\overline{\text{DQS}}$	na	note #2	non adj.	2.5	non adj.	non adj.	non adj.
	CK	na	na	note #2	2.0	2.0	non adj.	non adj.
	C/A	na	na	na	2.0	2.0	note #4	note #4
	Power Island	na	na	na	na	2.0	3.0	3.0
	NB Channel	na	na	na	na	na	note #2	note #3
	SB Channel	na	na	na	na	na	na	note #2

Notes:
#1 Values in the table represent recommended minimum ratio AG/D where AG is the air gap measurement from feature edge to feature edge and D is the distance between the signal layer and its reference plane. For simplicity, only “From => To” values are shown since the shaded fields contain duplicate values. “non adj.” means that busses are not adjacent on FBDIMM.
#2 For DQS/DQS#, CK and channel information see “Example Trace Geometries” section of this document.
#3 For information see “Pair-to-Pair Spacing Rules for System Data Channel Nets” section.
#4 Primary NB (micro-strip Tx) 5.0 (less or equal than 3.0 is OK for < 2.5 mm parallel run)
Primary SB (micro-strip Rx) 5.0
Secondary SB (strip-line, Tx) 3.0
Secondary NB (strip-line, Rx) 5.0

Example calculations

If the distance between the signal layer and its reference plane (dielectric height) is D=0.127um,
the recommended minimum air gap between DQ and DQS/DQS# is: 2.0x0.127=0.254um

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Dual Strip-line Differential Pairs Spacing

Noise can be coupled onto to a differential pair from a close-by differential pair running in parallel if a certain width to height ratio is not maintained. This spacing rule provides routing guidelines in the case when two strip-line differential signal pairs are routed in parallel on adjacent strip-line layers. The intra-pair coupling could adversely impact the proper termination and hence spacing rule(s) has to be taken to prevent reflection at the far end of the pairs.

The rules are as follows based on dimensions given in figure below (rules are based on nominal dimensions.)

1.For differential pairs, where signals are opposite direction (RX to TX)

(Xdiff + Ydiff) > 1.7 (S+H)

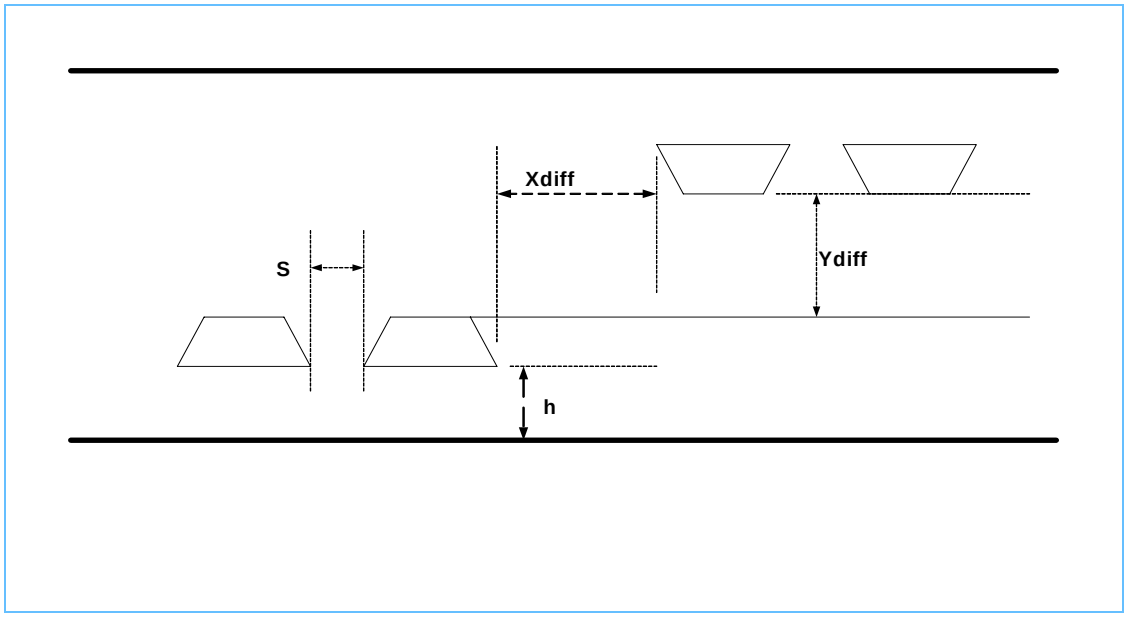
This 1.7 Rule is a MIN spacing requirement for parallel trace segments. While there are no rules precluding pair crossing segments (areas where a pair on one layer crosses over another pair on an adjacent layer), best layout practice should avoid pair crossings whenever possible in order to minimize all forms of crosstalk. Pair crossings should be perpendicular (90 degree intersect), else pair crossings must acheive at least 45 degree intersects.

2.For differential pairs, where signals are same direction (RX to RX or TX to TX)

(Xdiff + Ydiff) > 1.3 (S+H)

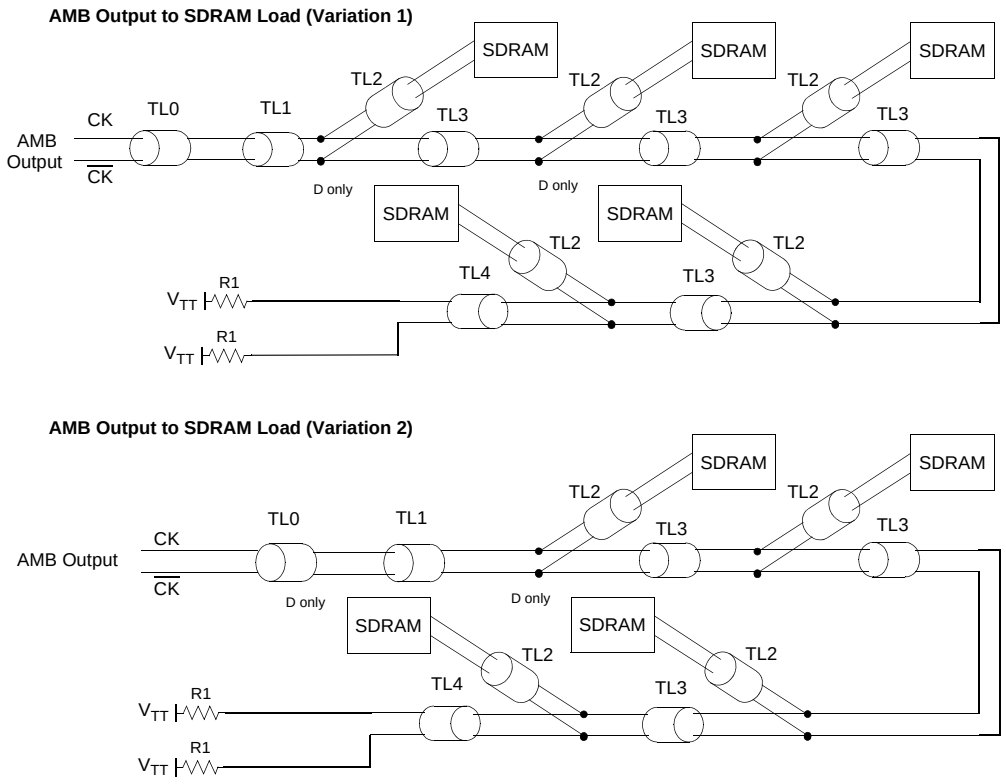
This 1.3 Rule is a MIN spacing requirement applied in case the signal lines are parallel to possible agressors, and the total length of net segments for that signal is more than 6mm and the aggressor signals run in the same direction. these nets may have some segments with spacing violations and that violation is acceptable so long as the sum of the violating segments is less that 6mm in length.

Dual-strip-line Differential Pairs



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Net Structure Routing for AMB Clock Output to SDRAM (Raw Card A)



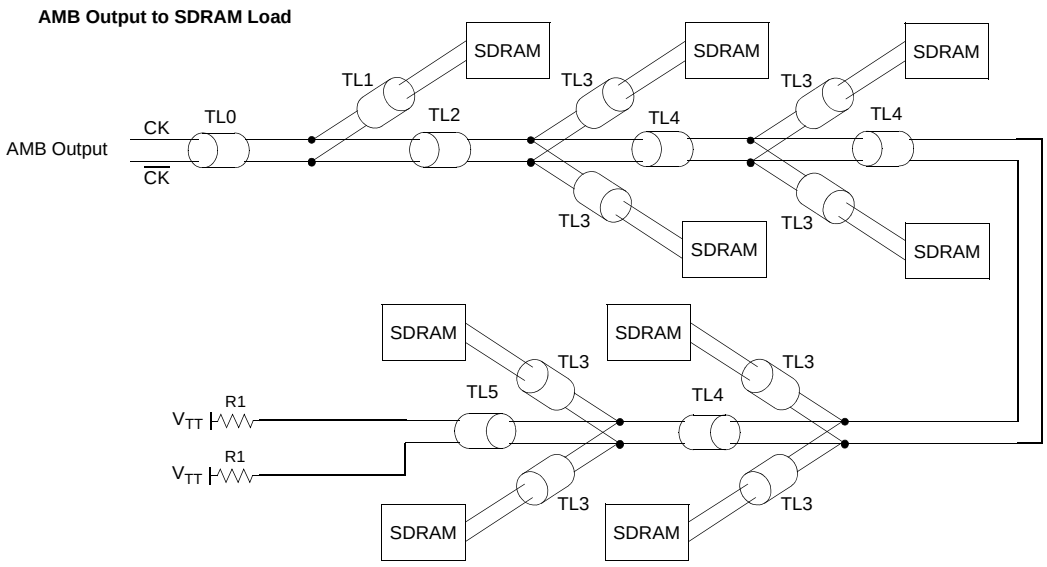
Trace Lengths for AMB Clock Output to SDRAM Net Structure (Raw Card A)

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Raw Card	Variation	TL0		TL1		TL2		TL3		TL4		R1 Ohms	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
A	1	0.6	0.6	10.0	10.1	2.8	2.8	10.0	10.0	17.6	19.7	30	1, 2, 3, 4
	2	0.6	0.6	14.7	15.0	2.8	2.8	10.0	10.0	19.8	20.3	30	1, 2, 3, 4

1. All distances are given in millimeters.
2. Trace length difference between the two elements of a differential pair, measured from the AMB to any DRAM, must not exceed 0.50 mm.
3. TL1 and TL3 segments are routed on inner layers only. TL4 is routed on inner layer except for the final 0.9-1.9 mm.
4. On Raw Card A, variation 1 is CK1/$\overline{CK1}$, variation 2 is CK0/$\overline{CK0}$.

Net Structure Routing for AMB Clock Output to SDRAM (Raw Cards B,C)



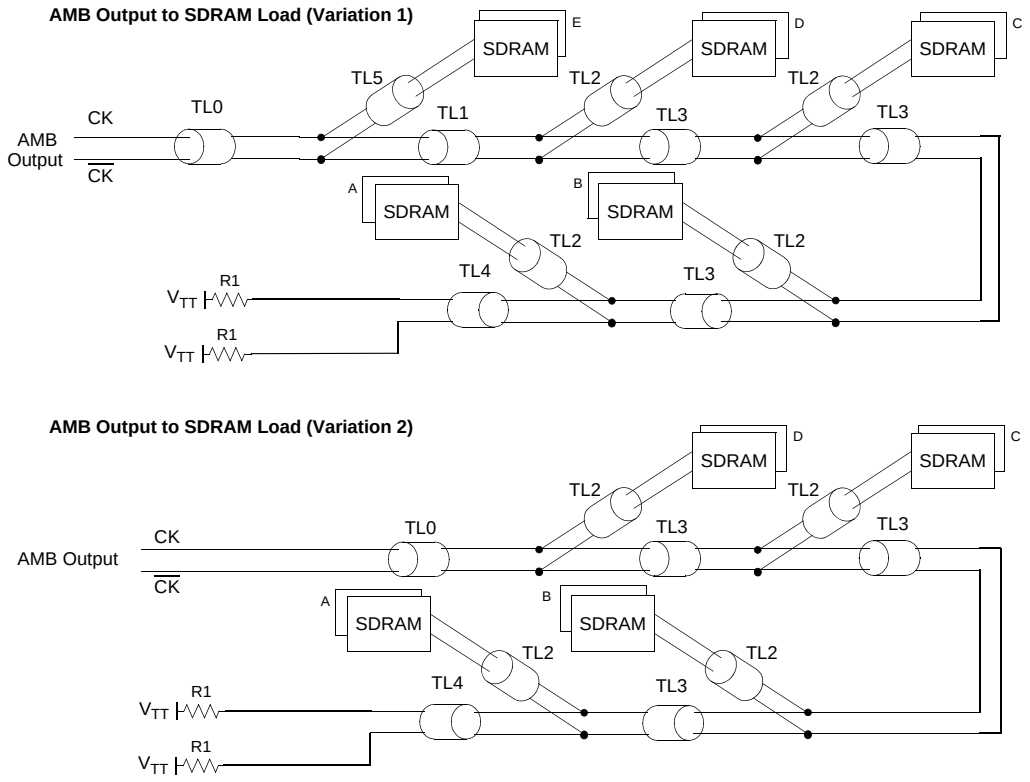
Trace Lengths for AMB Clock Output to SDRAM Net Structure

Raw Card	TL0		TL1		TL2		TL3		TL4		TL5		R1 Ohms	Notes
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
B CK0/$\overline{CK0}$	0.6	1.5	2.1	2.5	12.1	12.2	0.6	4.4	13.3	14.9	16.1	20.8	39	1, 2, 3
B CK1/$\overline{CK1}$	0.6	1.5	8.6	9.9	7.8	9.3	0.6	3.7						
C CK0/$\overline{CK0}$	0.6	1.5	2.1	2.5	11.1	11.2	3.1	3.2	13.3	14.9	16.1	20.8	39	1, 2, 3
C CK1/$\overline{CK1}$	0.6	1.5	9.7	9.9	7.8	9.3	3.1	3.2						

1. CK0/$\overline{CK0}$ is for the left half of the DIMM, CK1/$\overline{CK1}$ is for the right half of the DIMM.
2. Trace length difference between the two elements of a differential pair, measured from the AMB to any DRAM, must not exceed 0.5 mm.
3. TL2 and TL4 segments are routed on inner layers only, TL5 is routed on inner layer except for the final 0.9-1.9 mm.

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Net Structure Routing for AMB Clock Output to SDRAM (Raw Card D)



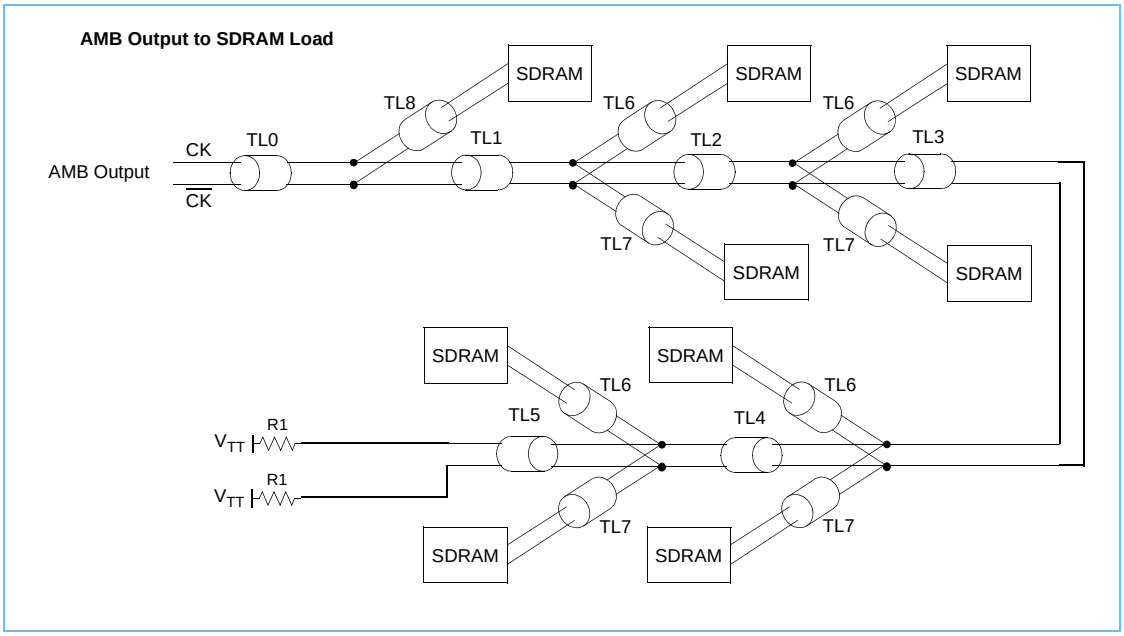
Trace Lengths for AMB Clock Output to SDRAM Net Structure (Raw Card D)

Raw Card	Variation	TL0		TL1		TL2		TL3		TL4		TL5		R1 Ohms	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
D	1	0.6	0.6	12.2	12.4	0.6	0.6	15.2	15.4	20.3	20.8	8.2	8.4	33	1, 2, 3, 4
	2	21.2	21.4	NA		0.6	0.6	15.2	15.4	20.3	20.7	NA		33	1, 2, 3, 4

1. All distances are given in millimeters.
2. Trace length difference between the two elements of a differential pair, measured from the AMB to any DRAM, must not exceed 0.50 mm.
3. TL1 and TL3 segments are routed on inner layers only, TL4 is routed on inner layer except for the final 0.9-1.9 mm.
4. On Raw Card D, variation 1 is CK0/$\overline{\text{CK0}}$ and CK1/$\overline{\text{CK1}}$, variation 2 is CK2/$\overline{\text{CK2}}$ and CK3/$\overline{\text{CK3}}$.

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Net Structure Routing for AMB Clock Output to SDRAM (Raw Card E, H)



Trace Lengths for AMB Clock Output to SDRAM Net Structure (Raw Card E, H)

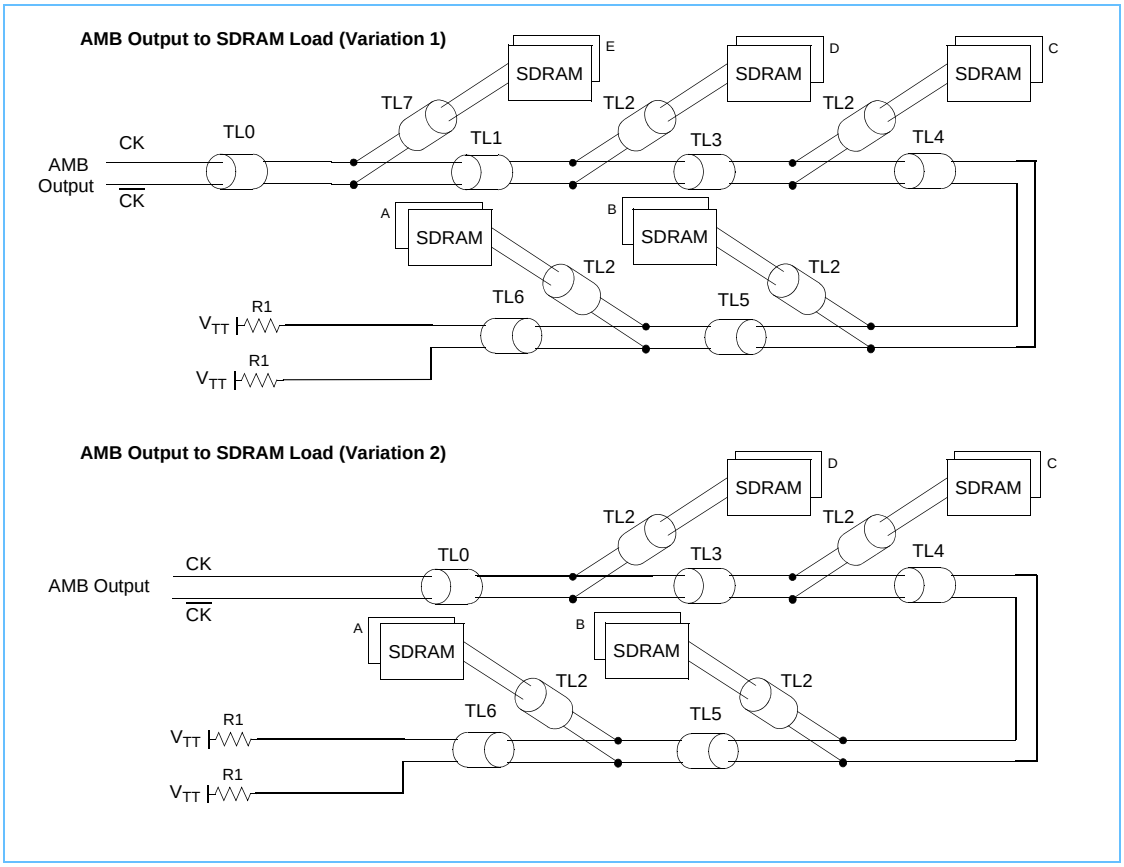
Raw Card	TL0		TL1		TL2		TL3		TL4		TL5		TL6		TL7		TL8		R1 Ohms	Notes
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
E	0.5	10.2	7.5	17.2	13.3	13.6	13.3	13.6	13.3	13.6	17.0	17.6	3.8	3.9	3.8	3.9	10.0	19.6	39	1,2,3
H	0.57	10.1	7.7	17.2	13.3	13.6	13.3	13.6	13.3	13.6	17.0	17.6	3.84	3.86	3.84	3.86	10.6	13.8	39	1,2,3

1. CK0/$\overline{\text{CK0}}$ is for the left half of the DIMM, CK1/$\overline{\text{CK1}}$ is for the right half of the DIMM.
2. Trace length difference between the two elements of a differential pair, measured from the AMB to any DRAM, must not exceed 0.5 mm.
3. Segments TL0 and TL6 are routed on top layer. Segments TL1, TL2, TL3, TL4 and TL5 are routed on layer S8. Segments TL7 and TL8 are routed on bottom layer.

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Net Structure Routing for AMB Clock Output to SDRAM (Raw Card J)



Trace Lengths for AMB Clock Output to SDRAM Net Structure (Raw Card J)

Raw Card	Variation	TL0		TL1		TL2		TL3		TL4		TL5		TL6		TL7	R1 Ohms	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max			
J	1	0.6	0.6	12.1	12.5	0.6	0.6	19.2	19.3	22.1	22.1	20.7	20.8	20.8	20.9	10.0	30	1, 2, 3, 4
	2	0.6	0.6	12.3	12.5	0.6	0.6	32.6	32.7	23.6	23.7	23.6	23.7	21.8	21.8	--	30	1, 2, 3, 4

1. All distances are given in millimeters.
2. Trace length difference between the two elements of a differential pair, measured from the AMB to any DRAM, must not exceed 0.50 mm.
3. TL1, TL3, TL4 and TL5 segments are routed on inner layers only, TL6 is routed on inner layer except for the final 0.9-2.5 mm.
4. On Raw Card J, variation 1 is CK0/$\overline{\text{CK0}}$ and CK1/$\overline{\text{CK1}}$, variation 2 is CK2/$\overline{\text{CK2}}$ and CK3/$\overline{\text{CK3}}$.

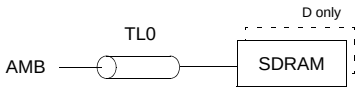
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Data Net Structures

DQ[63:0], CB[7:0], DQS[17:0], $\overline{\text{DQS}}$[17:0]

Special attention must be paid to balancing data nets (including check bits) within a byte lane (Raw Cards A and B) or nibble lane (Raw Cards C and D). Data nets have been placed in order to bound the data strobe nets. Because data travels with the data strobe, the placement of the strobe in the middle of the narrow window aids in data timing.

Net Structure Routing for DQ, CB, DQS, $\overline{\text{DQS}}$ (Raw Cards A, D, J)



Trace Lengths for DQ, CB, DQS, $\overline{\text{DQS}}$ Net Structure (Raw Cards A, D, J)

Raw Card	DRAM Position	TL0		Notes
		Min	Max	
A	3,8	21.7	25.3	1, 2, 3, 4
	2,4	30.1	30.5	1, 2, 3, 4
	1,5	40.5	51.6	1, 2, 3, 4
	0,6	57.5	61.7	1, 2, 3, 4
	7	76.8	76.9	1, 2, 3, 4
D (DQ)	8,17	11.9	12.1	1, 2, 3, 4
	3,4,12,13	21.4	21.6	1, 2, 3, 4
	2,5,11,14	37.9	38.1	1, 2, 3, 4
	1,6,10,15	60.9	61.1	1, 2, 3, 4
	0,7,9,16	82.9	83.1	1, 2, 3, 4
D (DQS/$\overline{\text{DQS}}$)	8,17	11.9	12.1	1, 2, 3, 4
	3,4,12,13	21.4	21.6	1, 2, 3, 4
	2,5,11,14	46.9	47.1	1, 2, 3, 4
	1,6,10,15	69.9	70.1	1, 2, 3, 4
	0,7,9,16	91.9	92.1	1, 2, 3, 4
J (DQ)	8,17	12.0	14.2	1, 2, 3, 4
	3,4,12,13	17.5	17.5	1, 2, 3, 4
	2,5,11,14	40.0	40.0	1, 2, 3, 4
	1,6,10,15	80.5	80.5	1, 2, 3, 4
	0,7,9,16	110.0	110.0	1, 2, 3, 4
J (DQS/$\overline{\text{DQS}}$)	8,17	11.7	12.0	1, 2, 3, 4
	3,4,12,13	17.5	17.6	1, 2, 3, 4
	2,5,11,14	41.0	41.2	1, 2, 3, 4
	1,6,10,15	82.5	82.5	1, 2, 3, 4
	0,7,9,16	112.9	113.1	1, 2, 3, 4

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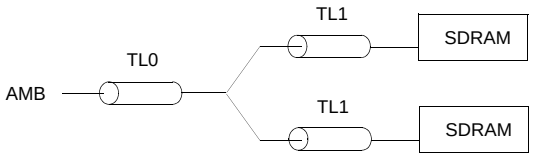
Trace Lengths for DQ, CB, DQS, DQS Net Structure (Raw Cards A, D, J)

Raw Card	DRAM Position	TL0		Notes
		Min	Max	

1. All trace distances are given in millimeters.
2. Trace length difference between the two elements of a differential pair (DQS/$\overline{\text{DQS}}$) must not exceed 0.25 mm.
3. Trace length difference between the DQS/$\overline{\text{DQS}}$ traces and the DQ traces of a given byte (Raw Card A) or nibble (Raw Cards C, D) must not exceed 0.5 mm, unless up to 5 mm of additional trace is added to DQS/DQS# to improve write setup margin, in which case, the spread across the DQ signals must not exceed 1 mm. DRAM positions TBD have TBD additional trace on DQS/DQS#.
4. The designations in the “DRAM Position” column refer to the assignments made in the example diagrams.from “Component Types and Placement” section.

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Net Structure Routing for DQ, CB, DQS, $\overline{\text{DQS}}$ (Raw Card B)



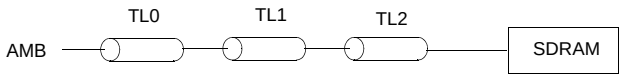
Trace Lengths for DQ, CB, DQS, $\overline{\text{DQS}}$ Net Structure (Raw Card B)

Raw Card	DRAM	TL0		TL1		TL0 + TL1		Notes
		Min	Max	Min	Max	Min	Max	
B (DQ/CB)	8,17	0.6		14.0	14.2	14.6	14.7	1, 2, 3, 4
	3,4,12,13	19.7	24.1	0.6	1.9	21.4	24.7	1, 2, 3, 4
	2,5,11,14	31.0	34.5	0.6	2.7	33,4	35.2	1, 2, 3, 4
	1,6,10,15	56.3	58.1	0.6	1.9	58.0	58.7	1, 2, 3, 4
	0,7,9,16	71.1	75.6	0.6	1.9	73.0	76.2	1, 2, 3, 4
B (DQS/$\overline{\text{DQS}}$)	8,17	0.6		14.0	14.2	14.6	14.7	1, 2, 3, 4
	3,4,12,13	19.7	24.1	0.6	1.9	21.4	24.7	1, 2, 3, 4
	2,5,11,14	31.0	38.5	0.6	2.7	33,4	39.2	1, 2, 3, 4
	1,6,10,15	56.3	61.1	0.6	1.9	58.0	61.7	1, 2, 3, 4
	0,7,9,16	71.1	77.6	0.6	1.9	73.0	78.2	1, 2, 3, 4

1. All trace distances are given in millimeters.
2. Trace length difference between the two elements of a differential pair (DQS/$\overline{\text{DQS}}$) must not exceed 0.25 mm.
3. Total trace length difference (TL0 + TL1) between the DQS/$\overline{\text{DQS}}$ traces and the DQ traces of a given byte must not exceed 0.5 mm, unless up to 5 mm of additional trace is added to DQS/DQS# to improve write setup margin, in which case, the spread across the DQ signals must not exceed 1 mm.
4. The designations in the “DRAM Position” column refer to the assignments made in the example diagrams.from “Component Types and Placement” section.

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Net Structure Routing for DQ, CB, DQS, $\overline{DQS}$ (Raw Card C)



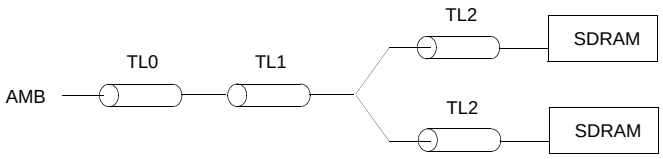
Trace Lengths for DQ, CB, DQS, $\overline{DQS}$ Net Structure (Raw Card C)

Raw Card	DRAM	TL0		TL1		TL2		TL0+TL1+TL2		Notes
		Min	Max	Min	Max	Min	Max	Min	Max	
C	8,17	0.6	0.6	13.4	13.6	0.6	0.6	14.6	14.7	1,2,4
	3,4,12,13	0.6	0.6	16.1	19.6	0.6	5.5	21.4	21.7	1,2,4
	2,5,11,14	0.6	0.6	28.0	32.5	0.6	5.5	33,4	35.4	1-4
	1,6,10,15	0.6	0.6	52.0	58.5	0.6	5.5	58.0	58.7	1-4
	0,7,9,16	0.6	0.6	69.0	73.5	0.6	5.5	73.0	76.2	1-4

1. All trace distances are given in millimeters.
2. Trace length difference between the two elements of a differential pair (DQS/$\overline{DQS}$) must not exceed 0.25 mm.
3. DRAM positions 2,5,11,14 must have 2mm additional trace on DQS/DQS#.
   DRAM positions 1,6,10,15 must have 3mm additional trace on DQS/DQS#.
   DRAM positions 0,7,9,16 must have 2mm additional trace on DQS/DQS#.
4. The designations in the “DRAM Position” column refer to the assignments made in the example diagrams.from “Component Types and Placement” section.

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Net Structure Routing for DQ, DQS, $\overline{\text{DQS}}$ (Raw Cards E, H; excluding DQS8/17, DQS8/17)



Trace Lengths for DQ, DQS, $\overline{\text{DQS}}$ Net Structure (Raw Card E; excluding DQS8/17, DQS8/17)

Raw Card	DRAM	TL0		TL1		TL2		TL0 + TL1 + TL2		Notes
		Min	Max	Min	Max	Min	Max	Min	Max	
E	3, 4, 12, 13, 21, 22, 30, 31	0.5	1.4	19.1	20.7	2.1	3.3	22.9	24.2	1-5
	2, 5, 11, 14, 20, 23, 29, 32	0.5	0.6	31.1	34.9	2.1	3.3	33.9	38.8	1-5
	1, 6, 10, 15, 19, 24, 28, 33	0.5	1.4	54.8	58.0	0.5	3.3	57.5	61.9	1-5
	0, 7, 9, 16, 18, 25, 27, 34	0.5	0.6	71.7	73.7	1.3	3.3	74.8	77.6	1-5

1. All trace distances are given in millimeters.
2. Trace length difference between the two elements of a differential pair (DQS/$\overline{\text{DQS}}$) must not exceed 0.25 mm.
3. Total trace length difference (TL0 + TL1 + TL2) between the DQS/$\overline{\text{DQS}}$ traces and the DQ traces of a given byte must not exceed 0.5 mm, unless up to 5 mm of additional trace is added to DQS/DQS# to improve write setup margin, in which case, the spread across the DQ signals must not exceed 1 mm.
4. The designations in the “DRAM Position” column refer to the assignments made in the example diagrams.from “Component Types and Placement” section.
5. Segment TL0 is routed on top layer only. Segment TL1 is routed on layers S3 or S5. Segment TL2 is routed on top or bottom layers..

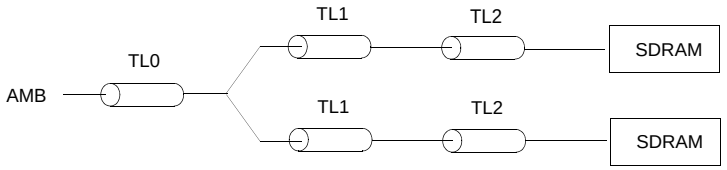
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Trace Lengths for DQ, DQS, $\overline{\text{DQS}}$ Net Structure (Raw Card H; excluding DQS8/17, $\overline{\text{DQS8/17}}$)

Raw Card	DRAM	Nets	TL0		TL0 + TL1		TL2		TL0 + TL1 + TL2		Notes
			Min	Max	Min	Max	Min	Max	Min	Max	
H	0, 7, 9, 16, 18, 25, 27, 34	DQ0 - DQ7, DQ56 - DQ63	0.57	1.37	71.1	75.6	0.6	2.7	73	76.2	1-5
		DQS 0, DQS 9, DQS 7, DQS 16	0.57	1.37	73.1	77.6	2.5	3.3	75	78.2	1-5
	1, 6, 10, 15, 19, 24, 28, 33	DQ8 - DQ15, DQ48 - DQ55	0.57	1.37	56.3	58.1	0.6	2.7	58	58.7	1-5
		DQS 1, DQS 10, DQS 6, DQS 15	0.57	1.37	58.3	61.1	2.5	3.3	61	61.7	1-5
	2, 5, 11, 14, 20, 23, 29, 32	DQ16 - DQ23, DQ40 - DQ47	0.57	1.37	31	35.5	0.6	2.7	33.4	35.2	1-5
		DQS 2, DQS 11, DQS 5, DQS 14	0.57	1.37	35	38.5	2.5	3.3	37.4	39.2	1-5
	3, 4, 12, 13, 21, 22, 30, 31	DQ24 - DQ39	0.57	1.37	19.7	24.1	0.6	2.7	21.4	24.7	1-5
		DQS 3, DQS 12, DQS 4, DQS 13	0.57	1.37	19.7	24.1	2.5	3.3	19.7	24.1	1-5

1. All trace distances are given in millimeters.
2. Trace length difference between the two elements of a differential pair (DQS/$\overline{\text{DQS}}$) must not exceed 0.25 mm.
3. Total trace length difference (TL0 + TL1 + TL2) between the DQS/$\overline{\text{DQS}}$ traces and the DQ traces of a given byte must not exceed 0.5 mm, unless up to 5 mm of additional trace is added to DQS/$\overline{\text{DQS}}$# to improve write setup margin, in which case, the spread across the DQ signals must not exceed 1 mm.
4. The designations in the “DRAM Position” column refer to the assignments made in the example diagrams.from “Component Types and Placement” section.
5. Segment TL0 is routed on top layer only. Segment TL1 is routed on layers S3 or S5. Segment TL2 is routed on top or bottom layers..

Net Structure Routing for CB, DQS8/17, $\overline{\text{DQS8/17}}$ (Raw Cards E, H)



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Trace Lengths for CB, DQS8/17, $\overline{\text{DQS8/17}}$ (Raw Card E)

Raw Card	DRAM	TL0		TL1		TL2		TL0 + TL1 + TL2		Notes
		Min	Max	Min	Max	Min	Max	Min	Max	
E	8, 17, 26, 35	0.5	1.4	17.8	19.2	0.5	1.9	20.2	21.1	1, 2, 3, 4, 5

1. All trace distances are given in millimeters.
2. Trace length difference between the two elements of a differential pair (DQS/$\overline{\text{DQS}}$) must not exceed 0.25 mm.
3. Total trace length difference (TL0 + TL1) between the DQS/$\overline{\text{DQS}}$ traces and the DQ traces of a given byte must not exceed 0.5 mm, unless up to 5 mm of additional trace is added to DQS/DQS# to improve write setup margin, in which case, the spread across the DQ signals must not exceed 1 mm.
4. The designations in the “DRAM Position” column refer to the assignments made in the example diagrams.from “Component Types and Placement” section.
5. Segment TL0 is routed on top layer only. Segments TL1 and TL2 are routed on top or bottom layers..

Trace Lengths for CB, DQS8/17, $\overline{\text{DQS8/17}}$ (Raw Card H)

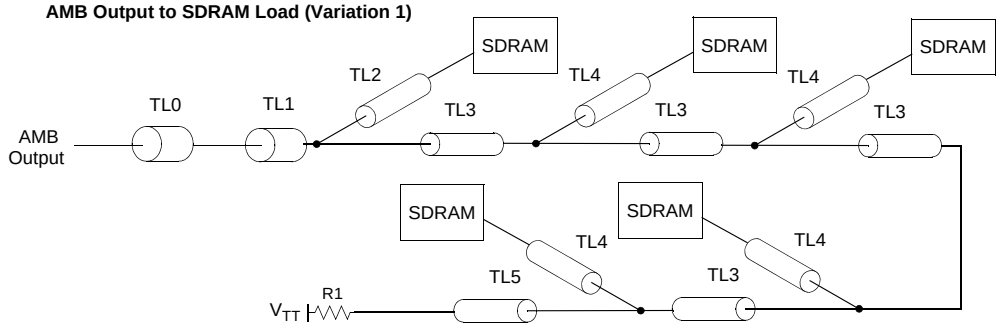
Raw Card	DRAM	Nets	TL0		TL0 + TL1		TL2		TL0 + TL1 + TL2		Notes
			Min	Max	Min	Max	Min	Max	Min	Max	
H	8, 17, 26, 35	CB 0 - CB 7	0.57	0.58	19.6	19.8	0.56	1.6	20.1	20.4	1-5
		DQS 8 , DQS 17	0.58	0.58	19.6	19.8	0.58	2.1	20.1	21.7	1-5

1. All trace distances are given in millimeters.
2. Trace length difference between the two elements of a differential pair (DQS/$\overline{\text{DQS}}$) must not exceed 0.25 mm.
3. Total trace length difference (TL0 + TL1) between the DQS/$\overline{\text{DQS}}$ traces and the DQ traces of a given byte must not exceed 0.5 mm, unless up to 5 mm of additional trace is added to DQS/DQS# to improve write setup margin, in which case, the spread across the DQ signals must not exceed 1 mm.
4. The designations in the “DRAM Position” column refer to the assignments made in the example diagrams.from “Component Types and Placement” section.
5. Segment TL0 is routed on top layer only. Segments TL1 and TL2 are routed on top or bottom layers..

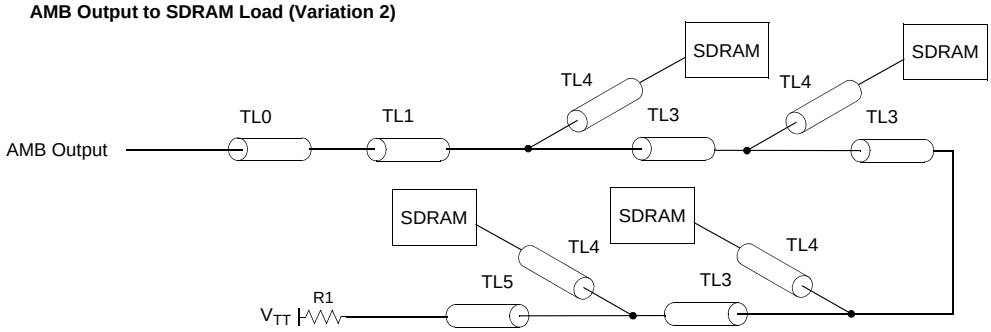
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Net Structure Routing for Address/Command to SDRAM (Raw Card A)

AMB Output to SDRAM Load (Variation 1)



AMB Output to SDRAM Load (Variation 2)



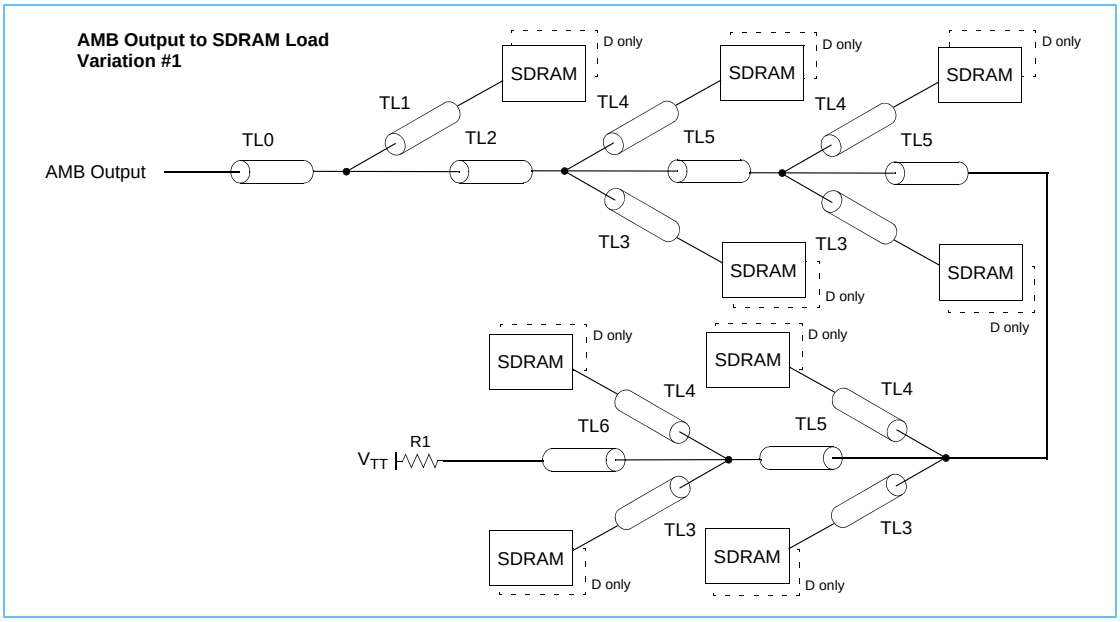
Trace Lengths for Address/Command Net Structure (Raw Card A)

Raw Card	Variation	TL0		TL1		TL2		TL3		TL4		TL5		End-to-End		R1 Ohms	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
A	1	0.6	2.0	7.9	16.6	0.6	2.3	1.9	17.4	0.6	2.3	11.7	20.9	74.9	95.9	39	1, 2, 3, 4
	2	0.6	2.0	13.5	21.1	N/A	N/A	2.3	18.7	0.6	2.3	7.0	21.4	52.0	67.3	39	1, 2, 3, 4

1. All distances are given in millimeters.
2. TL1, TL3, and TL5 segments are routed on inner layers only (except for last 0.9-1.9 mm of TL5).
3. End-to-End is the sum of TL0, TL1, all TL3 segments, and TL5, from the AMB output to the pad of the VTT R-pack.
4. Any two adjacent TL3 segments have a sum of between 18.4 and 21.2 mm.

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Net Structure Routing for Address/Command to SDRAM (Raw Cards B, C)



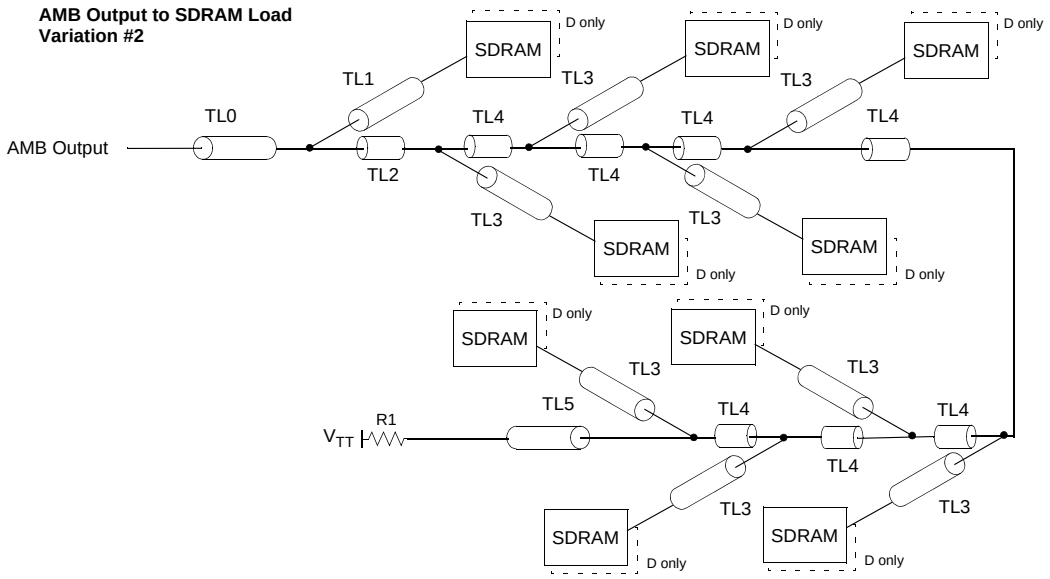
Trace Lengths for Address/Command Net Structure (Raw Cards B, C)

Raw Card	TL0		TL1		TL2		TL3		TL4		TL5		TL6		End-to-End		R1 Ohms	Notes
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
B	0.6	4.8	0.6	5.1	8.2	22.1	0.9	4.2	0.9	4.8	13.3	15.5	10.4	23.4	67.2	80.8	39	1-4
C	0.6	4.8	0.6	4.4	8.3	22.1	0.9	3.7	0.9	4.8	13.4	15.3	10.8	23.4	67.2	80.8	39	1-4

1. All distances are given in millimeters.
2. TL2, TL5, and TL6 segments are routed on inner layers only (except for last 0.9-1.9 mm of TL6).
3. On Raw Card B & C, all address and command are variation #1, except for A4, A7, A10, BA0, BA2 and ODT.
4. End-to-End is the sum of TL0, TL2, three TL5 segments, and TL6, from the AMB output to the pad of the VTT R-pack.

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Net Structure Routing for Address/Command to SDRAM (Raw Cards B, C)



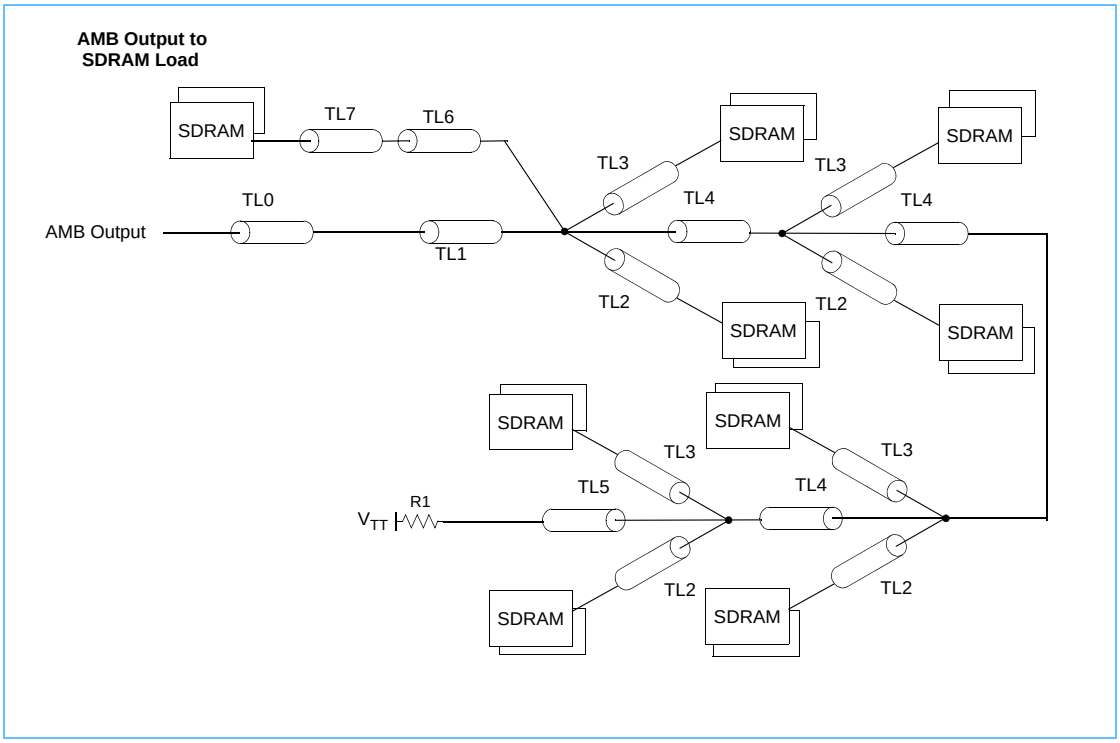
Trace Lengths for Address/Command Net Structure (Raw Cards B, C)

Raw Card	TL0		TL1		TL2		TL3		TL4		TL5		End-to-end		R1 Ohms	Notes
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
B	0.6	3.5	0.6	4.8	5.1	14.4	0.6	3.1	3.7	10.9	12.5	22.3	69.9	80.2	39	1-5
C	0.6	3.5	0.6	4.8	5.1	14.0	0.6	3.1	5.3	8.9	12.5	22.3	69.9	80.2	39	1-5

1. All distances are given in millimeters and must be kept within a tolerance of ± 0.8 millimeter.
2. TL2, TL4 and TL5 segments are routed on inner layers only (except for the last 0.9-1.9 mm of TL5 segments).
3. On Raw Card B & C, A4, A7, A10, BA0, BA2 and ODT are variation #2.
4. On Raw Card B & C, any two adjacent TL4 segments have a sum of between 11.7 and 16.8 mm.
5. End-to-End is the sum of TL0, TL2, seven TL4 segments, and TL5.

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Net Structure Routing for Address/Command to SDRAM (Raw Card D)



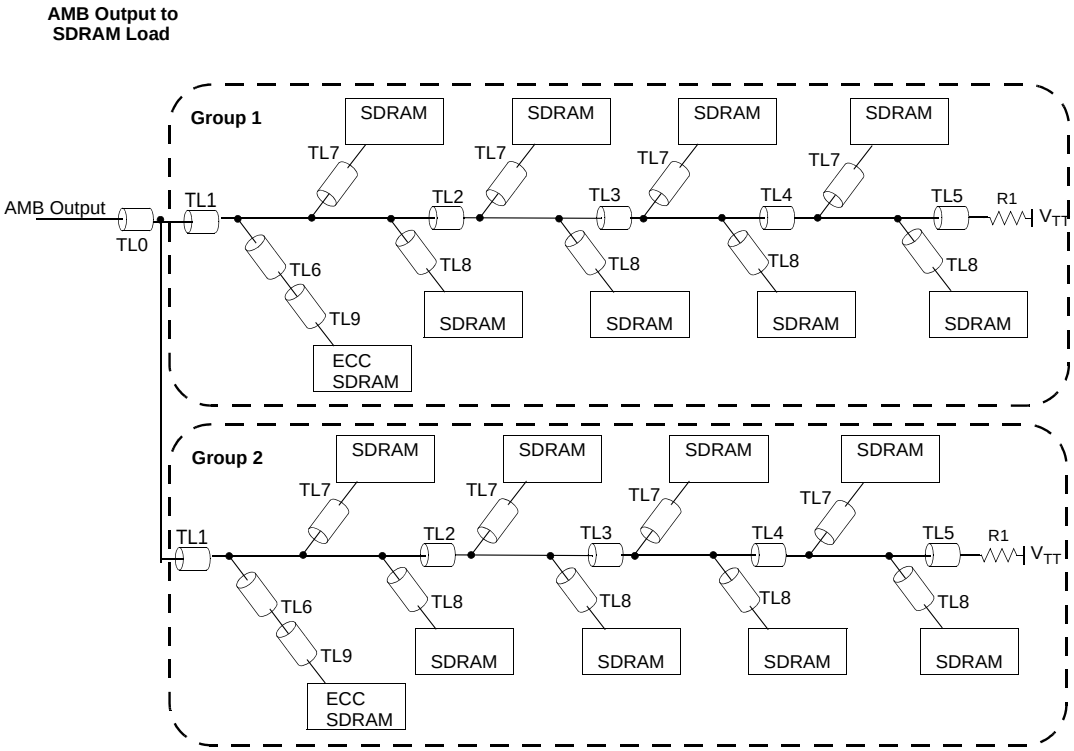
Trace Lengths for Address/Command Net Structure (Raw Card D)

Raw Card	TL0		TL1		TL2		TL3		TL4		TL5		TL6		TL7		R1 Ohms	Notes
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
D (less ODT)	0.6	1.4	26.0	26.1	1.4	6.3	1.0	6.6	13.5	15.1	17.0	18.0	18.2	19.5	0.6	0.6	20	1, 2, 3

1. All distances are given in millimeters.
2. ALL ADDR.CMD except ODT (see separate R/C D ODT wiring detail.
3. 533 MT/s operation can use Normal or Early timing.
   667 MT/s operation requires Early timing.
   800 MT/s operation requires Early timing.

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Net Structure Routing for Address/Command to SDRAM (Raw Cards E, H; excluding A4, A7, A10, BA0, BA2 and ODT)



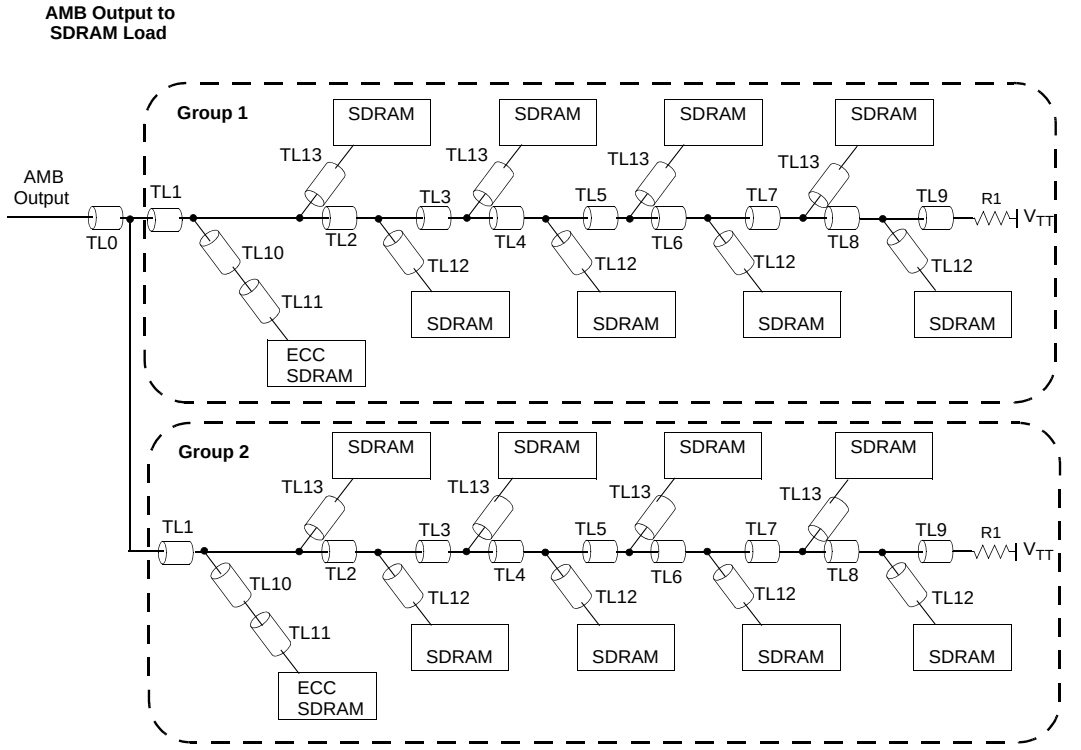
Trace Lengths for Address/Command Net Structure (Raw Cards E, H; excluding A4, A7, A10, BA0, BA2 and ODT)

Raw Card	TL0		TL1		TL2		TL3		TL4		TL5		TL6		TL7		TL8		TL9		R1 Ohms	Notes
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
E Group 1	0.5	4.3	11.8	23	13.3	15.1	12.9	15.3	13.0	15.3	11.4	16.1	7.2	17.1	1.1	4.6	1.0	5.2	0.5	8.0	33	1, 2
E Group 2	0.5	4.3	12.8	22.3	12.9	14.4	13.4	15.3	13.3	14.7	11.5	17.9	9.3	17.4	1.1	4.9	1.0	5.4	0.5	3.9	33	1, 3
H Group 1	0.56	3.6	12.3	22.5	13	15.25	12.9	15.5	13	15.5	11.4	16.2	7.5	18	1	4.6	1	5.3	0.57	9.3	33	1, 2
H Group 2	0.56	3.6	12.3	22.5	12.48	14.35	12.12	15.45	13.15	14.01	11.96	18.04	10.06	16.55	1	4.6	1	5.5	0.59	4.05	33	1, 3

1. All distances are given in millimeters.
2. For R/C E and R/C H, Group 1:TL0 and TL7 are routed on top layer; TL1, TL2, TL3, TL4, TL5 and TL6 are routed on layer S6; TL8 and TL9 are routed on bottom layer.
3. For R/C E and R/C H, Group 2:TL0 and TL7 are routed on top layer; TL1, TL2, TL3, TL4, and TL5 are routed on layer S8; TL6 is routed on layer S6; TL8 and TL9 are routed on bottom layer.

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Net Structure Routing for A4, A7, A10, BA0, BA2, ODT to SDRAM (Raw Cards E, H)



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Trace Lengths for A4, A7, A10, BA0, BA2 Net Structure (Raw Cards E, H)

Raw Card	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	R1 [Ohm]	Notes
E Group 1	TL0		TL1		TL2		TL3		TL4		TL5		TL6		33	1, 2
	0.5	3.5	9.9	19.2	6.0	8.7	5.2	7.7	6.2	8.2	5.3	7.8	6.2	8.1		
	TL7		TL8		TL9		TL10		TL11		TL12		TL13			
	5.3	7.8	6.0	8.2	12.6	14.7	4.2	14.5	0.5	3.3	0.5	1.4	0.5	2.8		
E Group 2	TL0		TL1		TL2		TL3		TL4		TL5		TL6		33	1, 3
	0.5	3.5	6.3	19.6	5.9	8.6	5.2	11.5	6.1	8.1	5.3	7.7	6.2	8.1		
	TL7		TL8		TL9		TL10		TL11		TL12		TL13			
	5.3	7.6	5.8	8.1	12.5	18.9	0.0	14.7	0.5	9.4	0.5	1.3	0.5	3.1		
H Group 1	TL0		TL1		TL2		TL3		TL4		TL5		TL6		33	1, 2
	0.57	3.6	8.47	19.44	5.94	8.61	5.3	7.66	6.23	8.14	5.29	7.74	6.21	8.09		
	TL7		TL8		TL9		TL10		TL11		TL12		TL13			
	5.29	7.33	6.1	8.14	12.68	15.58	4.27	14.78	0.57	3.27	0.54	0.58	0.55	3.0		
H Group 2	TL0		TL1		TL2		TL3		TL4		TL5		TL6		33	1, 3
	0.57	3.6	5.94	19.4	5.67	8.65	5.24	7.62	6.18	8.39	5.35	7.7	6.23	8.21		
	TL7		TL8		TL9		TL10		TL11		TL12		TL13			
	5.18	8.35	5.83	8.09	12.49	15.21	7.07	14.51	0.57	2.25	0.55	1.37	0.56	3.0		

1. All distances are given in millimeters.
2. For R/C E and R/C H, Group 1:TL0 and TL13 are routed on top layer; TL1 is routed on layer S6; TL2 - TL10 are routed on layer.S8; TL11 and TL12 are routed on bottom layer.
3. For R/C E and R/C H, Group 2:TL0 and TL13 are routed on top layer; TL1 is routed on layer S8; TL2 - TL10 are routed on layer.S6; TL11 and TL12 are routed on bottom layer.

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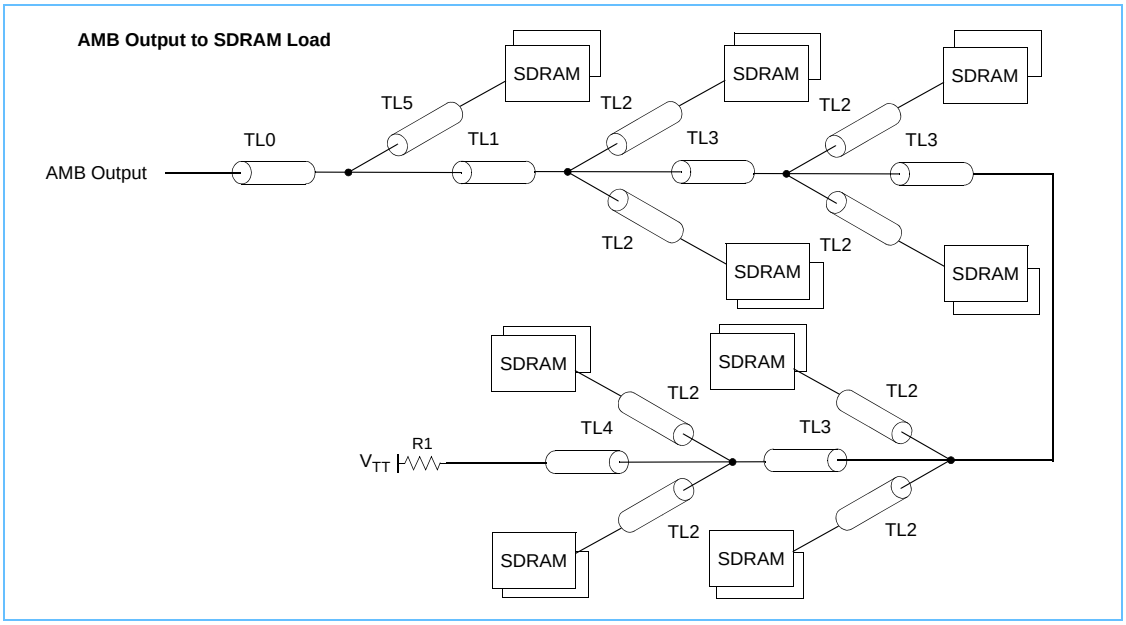
Trace Lengths for ODT Net Structure (Raw Cards E, H)

Raw Card	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	R1 [Ohm]	Notes
E Group 1	TL0		TL1		TL2		TL3		TL4		TL5		TL6		33	1, 2
	0.5	0.9	13.3	16.6	9.7	9.9	3.9	4.2	8.8	8.9	4.2	4.3	8.8	8.9		
	TL7		TL8		TL9		TL10		TL11		TL12		TL13			
	4.2	4.3	8.7	8.9	14.0	14.7	0.0	11.9	0.5	5.1	1.3	2.0	1.0	1.5		
E Group 2	TL0		TL1		TL2		TL3		TL4		TL5		TL6		33	1, 3
	0.5	0.9	6.9	16.2	9.5	10.0	4.2	5.6	8.7	8.9	4.2	5.8	8.8	8.9		
	TL7		TL8		TL9		TL10		TL11		TL12		TL13			
	4.2	5.7	8.8	8.9	12.3	16.0	0.0	15.0	2.2	4.8	1.3	2.0	1.0	1.6		
H Group 1	TL0		TL1		TL2		TL3		TL4		TL5		TL6		33	1, 2
	0.57	0.81	13.62	17.56	9.73	9.85	3.94	4.11	8.87	8.89	4.25	4.25	8.89	8.98		
	TL7		TL8		TL9		TL10		TL11		TL12		TL13			
	4.25	4.25	8.76	8.85	14.37	14.59	5.06	14.09	0.0	0.6	1.38	1.78	0.55	3.0		
H Group 2	TL0		TL1		TL2		TL3		TL4		TL5		TL6		33	1, 3
	0.57	0.81	7.0	17.53	9.71	9.96	4.23	5.57	8.85	8.87	4.28	5.73	8.86	8.86		
	TL7		TL8		TL9		TL10		TL11		TL12		TL13			
	4.34	5.61	8.78	8.87	11.95	15.79	4.72	14.72	0.0	1.94	1.42	1.73	0.56	3.0		

1. All distances are given in millimeters.
2. For R/C E and H, Group 1:TL0 and TL13 are routed on top layer; TL1 is routed on layer S6; TL2 - TL10 are routed on layer.S8; TL11 and TL12 are routed on bottom layer.
3. For R/C E and H, Group 2:TL0 and TL13 are routed on top layer; TL1 is routed on layer S8; TL2 - TL10 are routed on layer.S6; TL11 and TL12 are routed on bottom layer.

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Net Structure Routing for Address/Command to SDRAM (Raw Card J; excluding ODT)



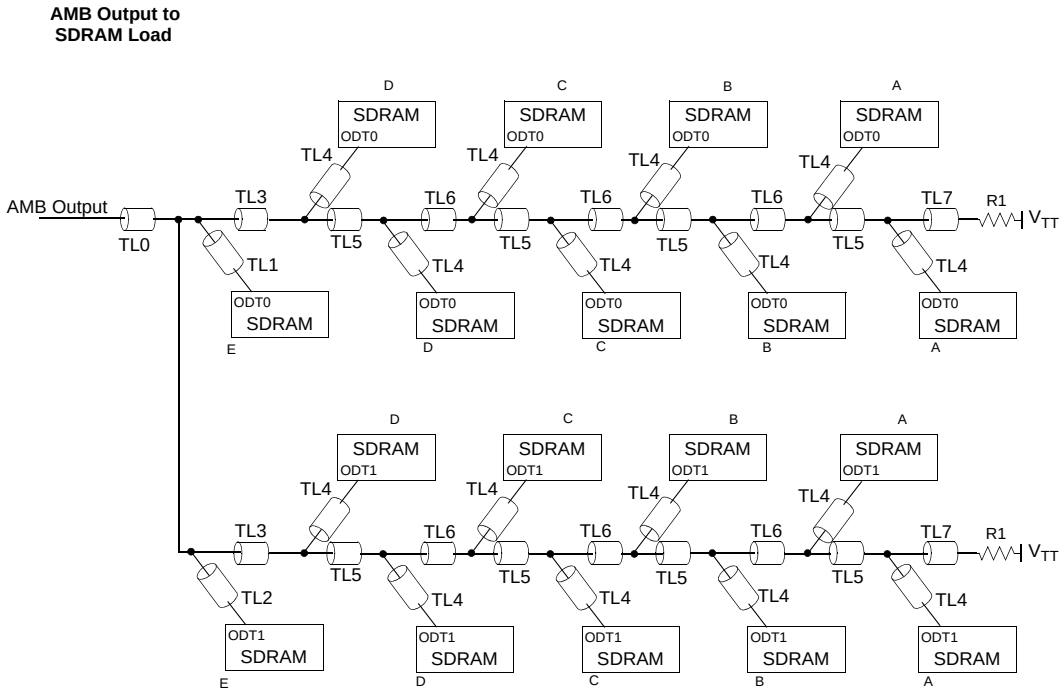
Trace Lengths for Address/Command Net Structure (Raw Card J; excluding ODT)

Raw Card	TL0		TL1		TL2		TL3		TL4		TL5		End-to-End		R1 Ohms	Notes
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
J	11.2	12.4	14.7	16.0	1.7	6.6	13.3	17.6	12.9	17.1	15.2	16.9	71.5	71.9	20	1, 2, 3

1. All distances are given in millimeters.
2. All Address and Command signals, except ODT (see separate R/C D ODT wiring detail)).
3. No early timing required
4. End-to-End is the sum of TL0, TL1, three TL3 segments, and TL4

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Net Structure Routing for ODT to SDRAM (Raw Card D)



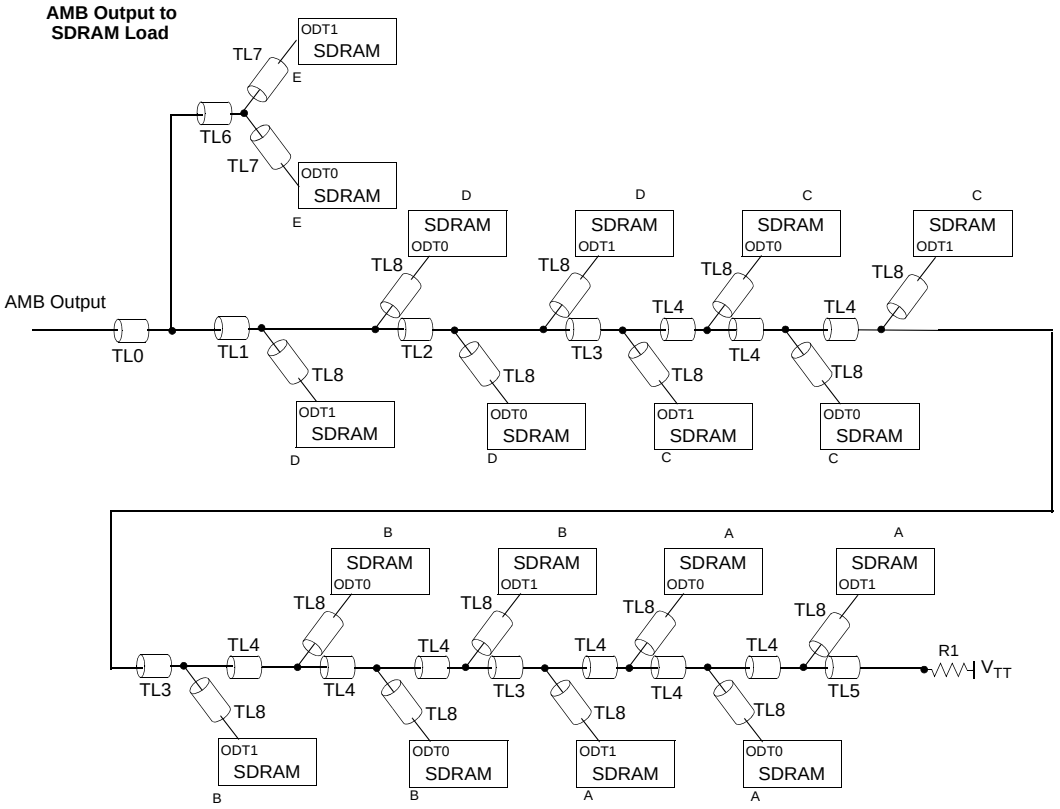
Trace Lengths for ODT Net Structure (Raw Card D)

Raw Card	TL0		TL1		TL2		TL3		TL4		TL5		TL6		TL7		R1 Ohms	Notes
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
ODT	2.3	3.2	4.0	4.1	5.5	5.6	9.9	10.1	1.4	1.5	10.1	10.3	4.2	4.4	13.5	14.5	24	1, 2

1. All distances are given in millimeters.
2. 533 MT/s operation can use Normal or Early timing.
   667 MT/s operation can use Normal or Early timing.
   800 MT/s operation requires Normal timing.

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Net Structure Routing for ODT to SDRAM (Raw Card J)



Trace Lengths for ODT Net Structure (Raw Card J)

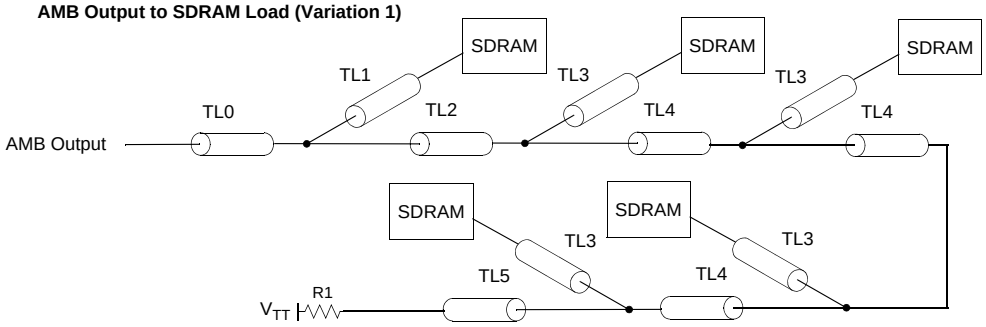
Raw Card	TL0		TL1		TL2		TL3		TL4		TL5		TL6		TL7		TL8		R1 Ohms	Notes
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
J	12.1	13.0	3.8	6.2	2.1	2.6	12.2	12.5	0.2	0.7	10.9	11.5	8.4	10.6	1.7	3.8	3.3	5.5	20	1, 2, 3, 4

1. All distances are given in millimeters.
2. Early timing not required.
3. Segment TL6 is a 0.2 mm wide trace where possible.
4. TL6 + TL7 = 11.7 to 12.2.

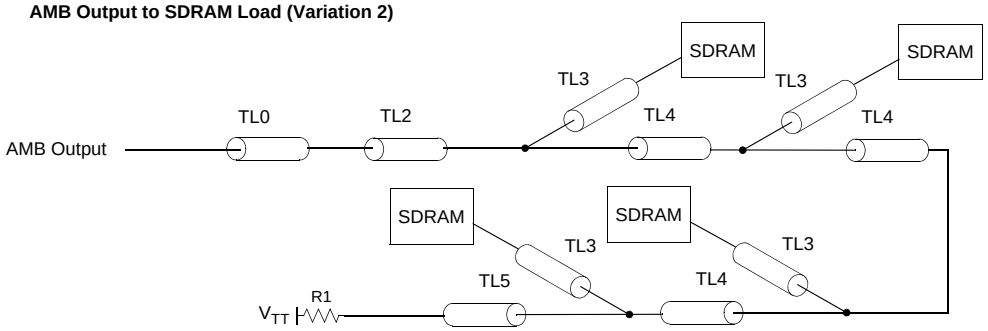
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Net Structure Routing for Control to SDRAM (Raw Cards A, B)

AMB Output to SDRAM Load (Variation 1)



AMB Output to SDRAM Load (Variation 2)



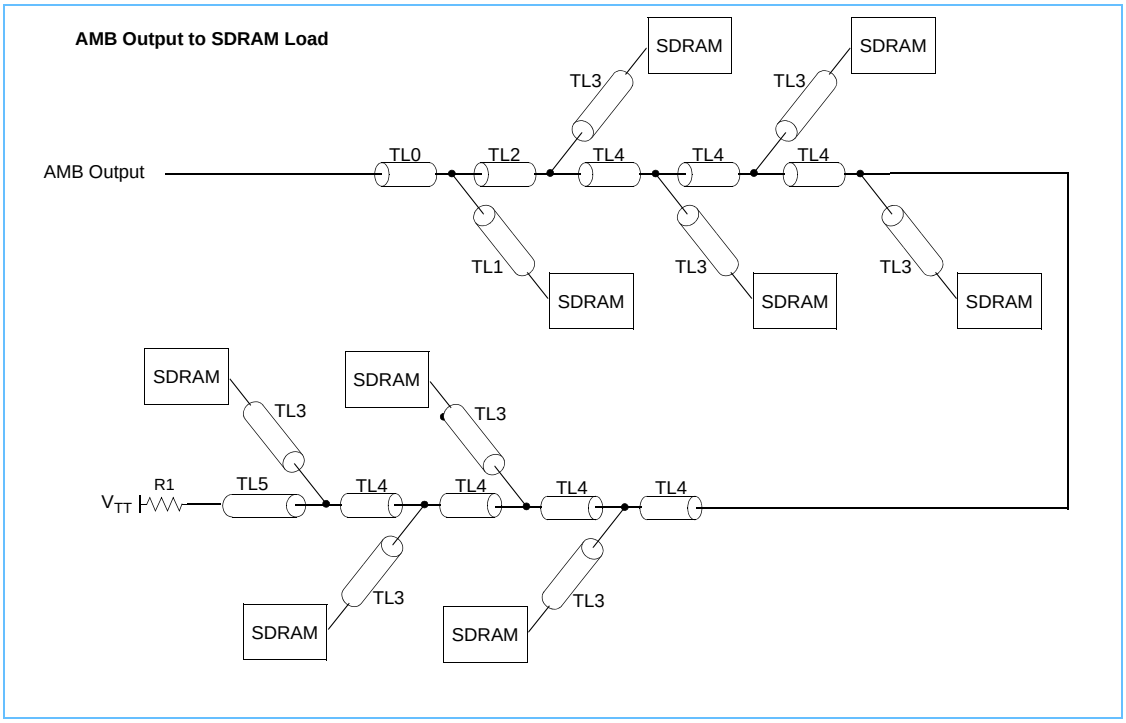
Trace Lengths for Control Net Structure (Raw Cards A, B)

Raw Card	Variation	TL0		TL1		TL2		TL3		TL4		TL5		End-to-end		R1 Ohms	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
A	1	11.9	12.7	0.6	0.6	4.6	17.1	0.6	0.6	3.1	16.8	15.3	20.9	81.6	90.5	39	1, 2, 3, 4, 6
	2	0.6	0.6	N/A	N/A	16.2	16.8	0.6	0.6	3.1	16.3	16.9	20.7	58.1	65.8	39	1, 2, 3, 4, 6
B	1	0.6	2.2	0.6	3.2	5.5	21.7	0.6	3.9	3.4	23.9	16.2	31.5	73.4	87.0	47	1, 2, 3, 5, 7
	2	0.6	1.9	N/A	N/A	9.2	14.4	0.6	2.6	3.5	23.9	16.0	26.7	78.3	96.8	47	1, 2, 3, 5, 7

1. All distances are given in millimeters.
2. TL2, TL4, and TL5 segments are routed on inner layers only (except for the last 0.9-1.9 mm of TL5).
3. End-to-end is the sum of segments TL0, TL2, three TL4 segments, and TL5.
4. For Raw Card A, variation 1 is for $\overline{CS}$0B and CKE0B, variation 2 is for $\overline{CS}$0A, CKE0A.
5. For Raw Card B, variation 1 is for $\overline{CS}$1A, CKE1A, $\overline{CS}$0B and CKE0B, variation 2 is for $\overline{CS}$0A, CKE0A, $\overline{CS}$1B and CKE1B.
6. On Raw Card A, any two adjacent TL4 segments have a sum of between 19.1 and 19.7 mm.
7. On Raw Card B, any two adjacent TL4 segments have a sum of between 27.0 and 32.3 mm.

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Net Structure Routing for Control to SDRAM (Raw Cards C)



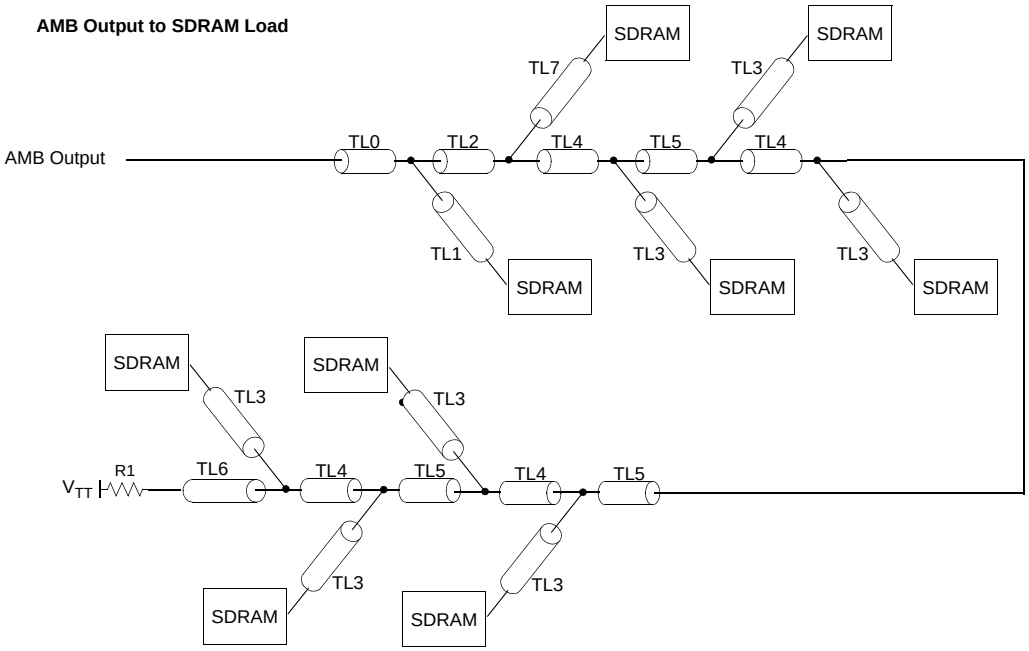
Trace Lengths for Control Net Structure (Raw Cards C)

Raw Card	TL0		TL1		TL2		TL3		TL4		TL5		End-to-end		R1 Ohms	Notes
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
C	0.6	2.2	0.6	2.2	8.6	13.7	0.6	1.4	5.2	8.7	12.1	15.8	70.6	78.0	39	1-4

1. All distances are given in millimeters.
2. TL2, TL4, and TL5 segments are routed on inner layers only (except for the last 0.9-1.9 mm of TL5).
3. End-to-end is the sum of segments TL0, TL2, seven TL4 segments, and TL5.
4. Control nets are CKE(1:0) and $\overline{CS}$(1:0).

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Net Structure Routing for Control to SDRAM (Raw Cards D, J)



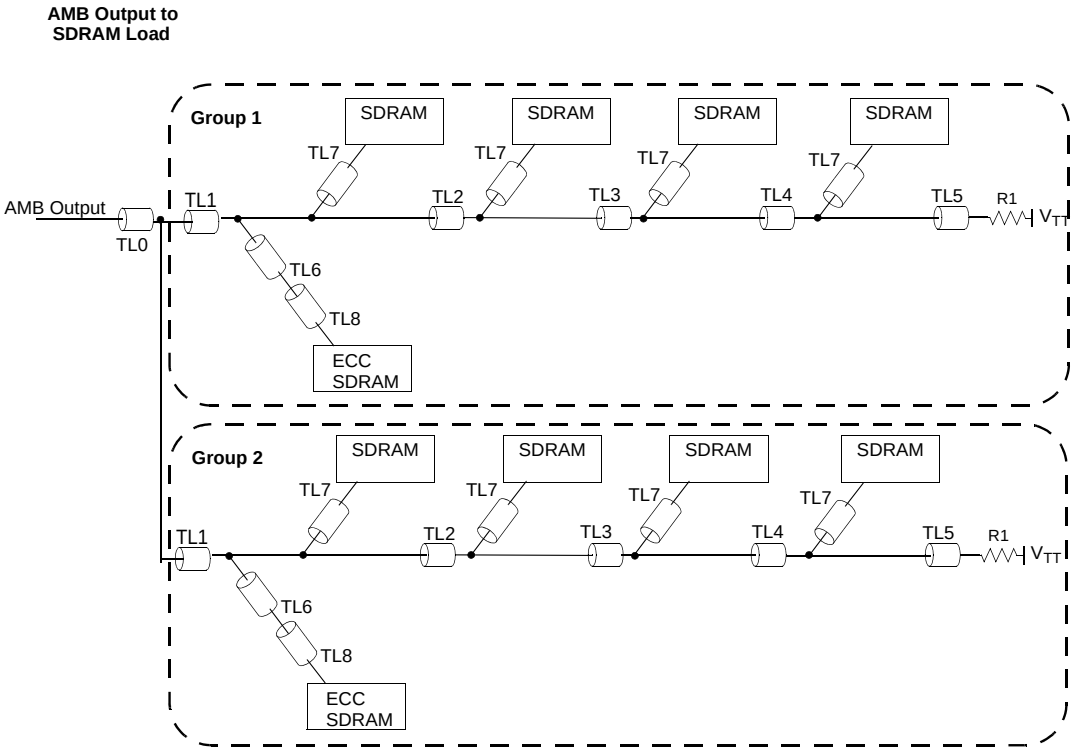
Trace Lengths for Control Net Structure (Raw Cards D, J)

Raw Card	TL0		TL1		TL2		TL3		TL4		TL5		TL6		TL7		End-to-end		R1 Ohms	Notes
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
D	0.6	3.5	0.6	6.8	7.0	14.4	0.6	0.6	4.7	8.0	5.6	9.4	17.7	18.3	0.6	0.6	72.5	82.5	24	1, 2, 3, 4, 5
J	13.8	14.1	8.6	8.8	15.6	21.1	3.7	3.8	1.9	2.3	20.0	22.1	15.9	18.8	5.1	5.4	92.5	116.3	20	1, 2, 3, 4, 6, 7

1. All distances are given in millimeters.
2. TL2, TL5, and TL6 segments are routed on inner layers only (except for the last 0.9-1.9 mm of TL6).
3. End-to-end is the sum of segments TL0, TL2, four TL4 segments, three TL5 segments and TL6.
4. Control nets are CKE(1:0) and $\overline{CS}$(1:0).
5. 533 MT/s operation can use Normal or Early timing.
   667 MT/s operation can use Normal or Early timing.
   800 MT/s operation requires Normal timing.
6. No early timing required
7. TL4 segment is routed on inner layers only

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Net Structure Routing for Control to SDRAM (Raw Card E; excluding S0L and CKE1R)



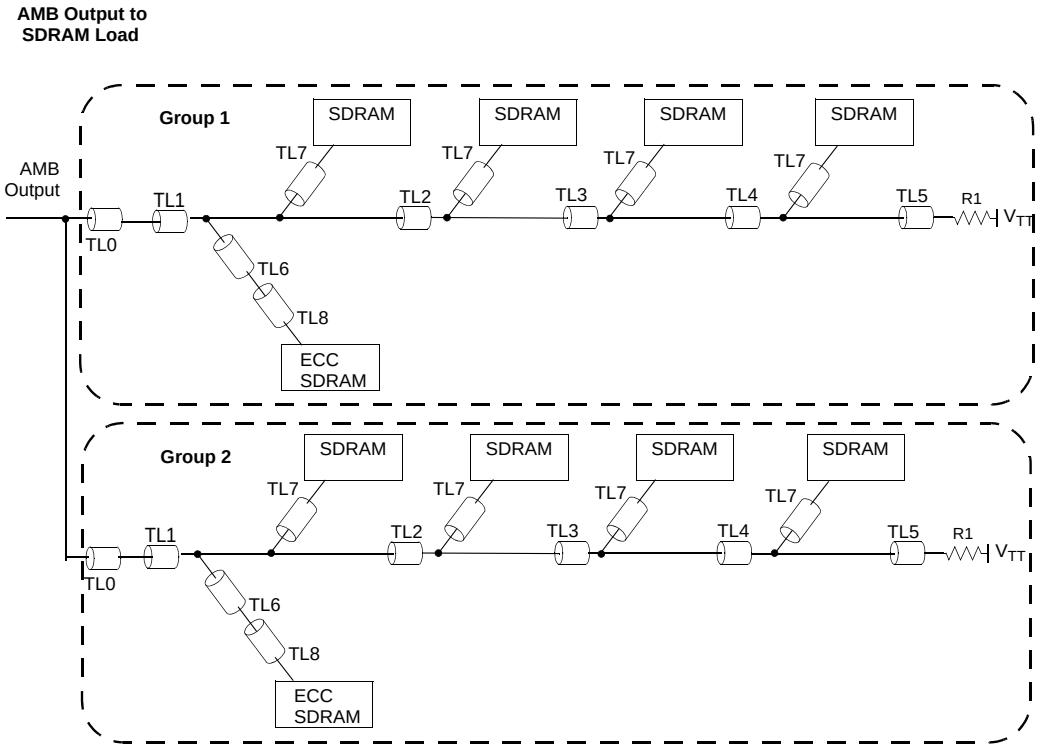
Trace Lengths for Control Net Structure (Raw Card E; excluding S0L and CKE1R)

Raw Card	TL0		TL1		TL2		TL3		TL4		TL5		TL6		TL7		TL8		R1 Ohms	Notes
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
E Group 1	0.5	11.4	9.0	21.9	12.8	14.4	14.1	14.4	14.1	14.5	17.9	19.2	4.5	21.1	0.5	3.0	0.5	2.3	39	1, 2, 4
E Group 2	0.5	1.4	10.1	22.9	12.1	15.8	14.1	15.5	14.0	16.5	17.3	18.6	11.0	14.1	0.5	3.2	0.5	4.7	39	1, 3, 5

1. All distances are given in millimeters.
2. For R/C E Group 1:TL0 and TL7 are routed on top layer; TL1 is routed on layer S6; TL2, TL3, TL4, TL5 and TL6 are routed on layer S8; TL8 is routed on bottom layer.
3. For R/C E Group 2:TL0, TL6 and TL7 are routed on top layer; TL1 is routed on layer S8; TL2, TL3, TL4 are routed on layer S6; TL5 is routed on layer S3; TL8 is routed on bottom layer.
4. R/C E Group 1 ECC SDRAM with TL6 and TL8 is only for S0R, CKE0R and CKE0L.
5. R/C E Group 2 ECC SDRAM with TL6 and TL8 is only for S1L, S1R and CKE1L.

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Net Structure Routing for S0L and CKE1R to SDRAM (Raw Card E)



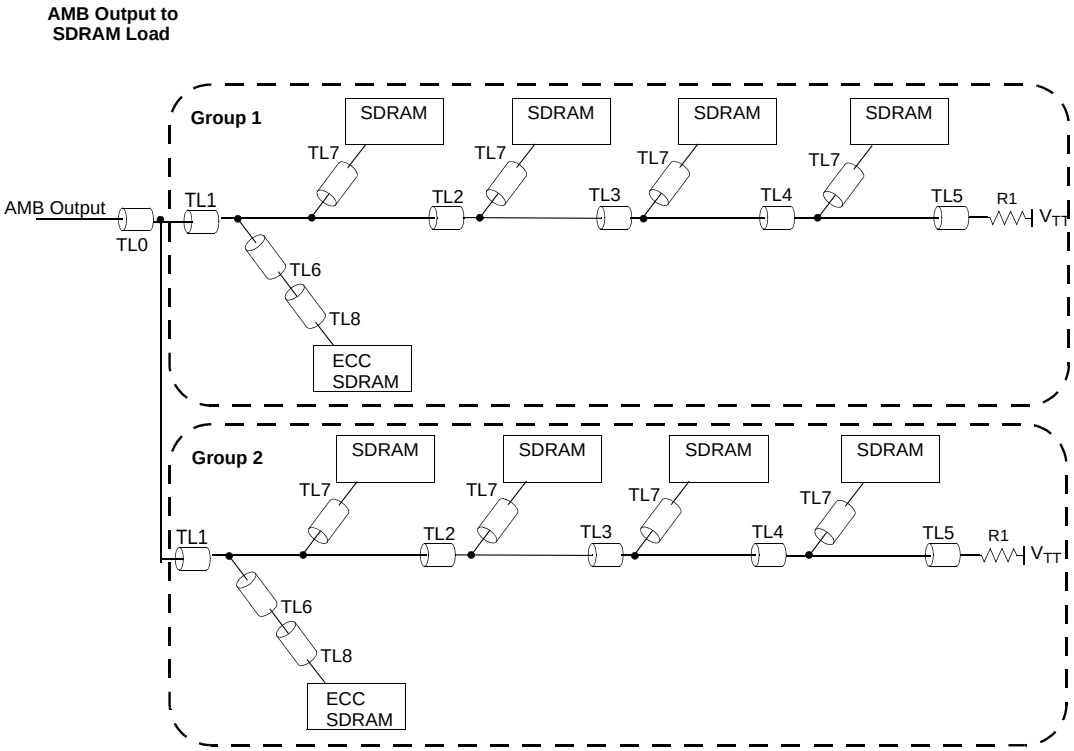
Trace Lengths for S0L and CKE1R Net Structure (Raw Card E)

Raw Card	TL0		TL1		TL2		TL3		TL4		TL5		TL6		TL7		TL8		R1 Ohms	Notes
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
E Group 1	10.1	12.6	3.6	9.9	13.1	14.3	14.1	14.2	14.0	14.3	16.6	18.0	0.0	0.0	0.5	2.3	8.2	8.2	39	1, 2, 4
E Group 2	5.3	8.3	4.0	11.3	14.0	15.6	14.0	15.0	14.2	15.5	17.1	17.4	7.8	7.8	0.5	2.3	7.6	7.6	39	1, 3, 5

1. All distances are given in millimeters.
2. For R/C E Group 1:TL0 and TL7 are routed on top layer; TL1 is routed on layer S6; TL2, TL3, TL4, TL5 and TL6 are routed on layer S8; TL8 is routed on bottom layer.
3. For R/C E Group 2:TL0, TL6 and TL7 are routed on top layer; TL1 is routed on layer S8; TL2, TL3, TL4 are routed on layer S6; TL5 is routed on layer S3; TL8 is routed on bottom layer.
4. R/C E Group 1 ECC SDRAM with TL6 and TL8 is only for S0L.
5. R/C E Group 2 ECC SDRAM with TL6 and TL8 is only for CKE1R.

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Net Structure Routing for Control to SDRAM (Raw Card H; excluding S0L, S1L and CKE1R)



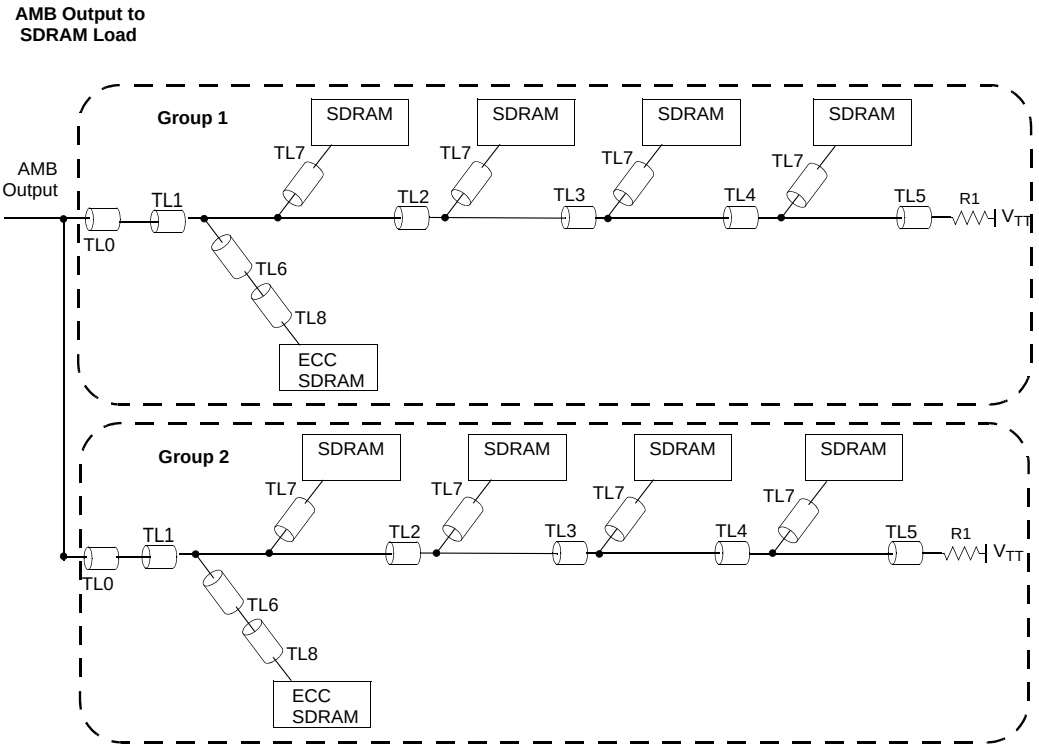
Trace Lengths for Control Net Structure (Raw Card H; excluding S0L, S1L and CKE1R)

Raw Card	TL0		TL1		TL2		TL3		TL4		TL5		TL6		TL7		TL8		R1 Ohms	Notes
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
H Group 1	0.57	11.85	3.7	21.83	12.75	14.37	14.13	14.31	14.09	14.43	15.92	18.73	4.51	21.22	0.56	2.9	0.0	2.3	39	1, 2, 4, 6
H Group 2	0.57	7.28	5.2	22.88	13.69	15.77	13.56	15.47	13.6	16.51	16.67	18.51	8.2	13.79	0.56	3.67	0.57	7.64	39	1, 3, 5

1. All distances are given in millimeters.
2. For R/C H Group 1:TL0 and TL7 are routed on top layer; TL1 is routed on layer S6; TL2, TL3, TL4, TL5 and TL6 are routed on layer S8; TL8 is routed on bottom layer.
3. For R/C H Group 2:TL0, TL6 and TL7 are routed on top layer; TL1 is routed on layer S8; TL2, TL3, TL4 are routed on layer S6; TL5 is routed on layer S3; TL8 is routed on bottom layer.
4. R/C H Group 1 ECC SDRAM with TL6 and TL8 is only for S0R, CKE0R and CKE0L.
5. R/C H Group 2 ECC SDRAM with TL6 and TL8 is only for S1R and CKE1L.
6. Group #1 TL6 is directly connected to the DRAM when TL8 = 0.

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Net Structure Routing for S0L, S1L and CKE1R to SDRAM (Raw Card H)



Trace Lengths for S0L, S1L and CKE1R Net Structure (Raw Card H)

Raw Card	TL0		TL1		TL2		TL3		TL4		TL5		TL6		TL7		TL8		R1 Ohms	Notes
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
H Group 1	0.57	11.85	3.7	21.83	12.75	14.37	14.13	14.31	14.09	14.43	15.92	18.73	4.51	21.22	0.56	2.9	0.0	2.3	39	1, 2, 4, 6
H Group 2	0.57	7.28	5.2	22.88	13.69	15.77	13.56	15.47	13.6	16.51	16.67	18.51	8.2	13.79	0.56	3.67	0.57	7.64	39	1, 3, 5

1. All distances are given in millimeters.
2. For R/C H Group 1:TL0 and TL7 are routed on top layer; TL1 is routed on layer S6; TL2, TL3, TL4, TL5 and TL6 are routed on layer S8; TL8 is routed on bottom layer.
3. For R/C H Group 2:TL0, TL6 and TL7 are routed on top layer; TL1 is routed on layer S8; TL2, TL3, TL4 are routed on layer S6; TL5 is routed on layer S3; TL8 is routed on bottom layer.
4. R/C H Group 1 ECC SDRAM with TL6 and TL8 is only for S0L.
5. R/C H Group 2 ECC SDRAM with TL6 and TL8 is only for S1L and CKE1R.
6. Group #1 TL6 is directly connected to the DRAM when TL8 = 0.

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Cross Section Recommendation

The DIMM printed circuit board design uses six, eight or ten layers of glass epoxy material. PCBs should contain solid ground planes. The outside layers typically supply VDD. The inner signal layers supply VDD and VCC.

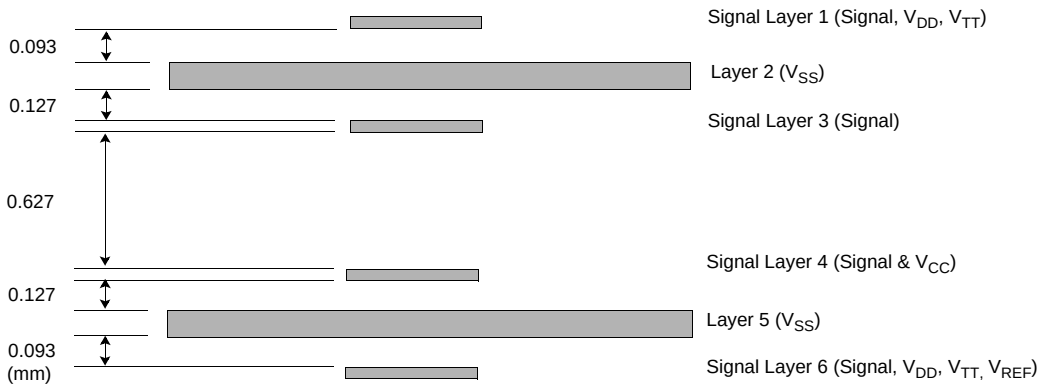
R/C reference design gerber registration collaterial must include stack-up assumptions used to develop the respective gerber. The furnished stack-up information must include core and pre-preg constructions information with dimensional and tolerance details.

Note: The PCB edge connector contacts shall be gold-plated.

PCB Electrical Specifications

Parameter	Min	Nominal	Max	Units
Trace velocity: S0 (outer layers)	5.5		6.7	ps/mm
Trace velocity: S0 (inner layers)	6.5		7.6	ps/mm
Trace impedance: Z_0 (Component break-out pad to via, outer layers)	54	60	66	Ohms
Trace impedance: Z_0 (DQ, inner layer)	50	56	62	Ohms
Trace impedance: Z_0 (Address/Command/Control, inner layer)	56	62	68	Ohms
Differential impedance: Z_{diff} (System Clock)	85	100	115	Ohms
Differential impedance: Z_{diff} (System Data Channel)	72	85	98	Ohms
Differential impedance: Z_{diff} (DRAM Clocks and DRAM DQS/$\overline{DQS}$)	85	100	115	Ohms

Example Six Layer Stackup



Note: This diagram is intended as an example only. Each DIMM manufacturer can determine the thickness of their layers based on their own impedance calculations.

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Example Trace Geometries, Single Ended

Location	Nominal Z_0	Nominal Trace Width
Outer Layers	60 ohms	0.102 mm
Inner Layers	56 ohms	0.127 mm
	62 ohms	0.102 mm

1.) Trace dimensions assume the example six-layer stackup in the previous diagram.
2.) The designer should maximize trace-to-trace air-gap separation (measuring from trace edge to trace edge) of single-ended signals to reduce signaling noise due to crosstalk.

Example Trace Geometries, Differential

Location	Nominal Z_{diff}	Nominal Trace Width	Nominal Trace Separation [3]
Outer Layers	85	0.127	0.127
Inner Layers	85	0.153	0.127
	100	0.102	0.127

1.) Trace dimensions assume the example six-layer stackup in the previous diagram.
2.) The designer should maximize trace-to-trace air-gap separation between the differential pair and its neighbors (measuring from pair trace edge to neighbor trace edge) to reduce signaling noise due to crosstalk.
3.) Values for Nominal Trace Separation are air-gap distances measuring from pair trace edge to neighbor trace edge.

Impedance Measurement Coupons

In order to allow DIMM card manufacturers to verify and monitor the trace impedances (Z_0 and Z_{diff}) listed above, measurement coupons have been added to the panels only (not the DIMM raw cards). A Time Domain Reflectometer (TDR) should be used to perform these measurements before DIMM assembly.

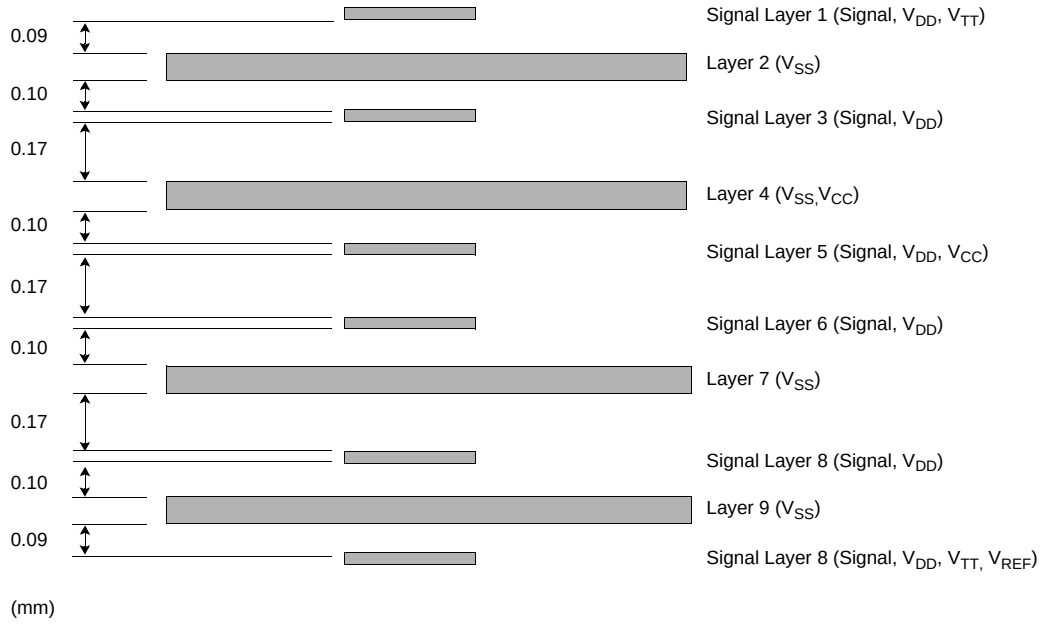
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Example Eight Layer Stackup



Note: This diagram is intended as an example only. Each DIMM manufacturer can determine the thickness of their layers based on their own impedance calculations.

Example Ten Layer Stackup



Note: This diagram is intended as an example only. Each DIMM manufacturer can determine the thickness of their layers based on their own impedance calculations.

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Example Timing Budget

The post-AMB timings on the Fully Buffered DIMMs are critical. The following tables describes a preliminary post-AMB timing budget for a typical DDR2 PC2-4200/PC2-5300/PC2-6400 Fully Buffered DIMM. Timing analysis is provided for read and write source synchronous data-to-strobe, strobe-to-clock, and address/command-to-clock. All skew budgets shall include the effects of trace length mismatch, crosstalk, inter-symbol interference (ISI) and VREF uncertainty.

The timing numbers used in the tables below are for example only - intention is to illustrate calculation method. Actual timing values should come from respective component specifications and calculated skew budget will differ accordingly.

Example DIMM Post-AMB Read Timing (PC2-4200/PC2-5300/PC2-6400)[1]

Parameter	Definition	Time (ps) PC2-4200	Time (ps) PC2-5300	Time (ps) PC2-6400	Notes
tCLK	Clock Cycle Time	3750	3000	2500	1
tHPmin	Minimum Clock Half Period at DRAM; tHPmin=min(tCL,tCH); tCL=CK low-level width; tCH=CK low-level width	1688	1315	1100	1
tDQSQ (dram)	DRAM DQS-to-DQ Skew	300	240	200	1
tQHS (dram)	DRAM Hold Skew Factor	400	340	300	1
tVALIDout (dram)	Data valid window at DRAM output tVALIDout = tHP - tDQSQ - tQHS	988	735	600	1
tSU (amb)	DQ and CB Input Setup TIme to DQS Crossing	-700	-530	-425	1
tHD (amb)	DQ and CB Input Hold TIme to DQS Crossing	1180	970	825	1
tSU + tHD (amb)	Sum of AMB Setup and Hold	480	440	400	1
DIMM Skew Budget	System Budget for DQ-to-DQS Skew (setup plus hold combined) = tVALIDout - (tSU + tHD)	508	295	200	1

Note 1: The timing numbers are for example only. Design should be based on the latest component specifications, FB-DIMM AMB and JESD 79-2 DRAM.

Example DIMM Post-AMB Write Setup Timing (PC2-4200/PC2-5300/PC2-6400)[1]

Parameter	Definition	Time (ps) PC2-4200	Time (ps) PC2-5300	Time (ps) PC2-6400	Notes
tDVB (amb)	AMB Data Valid Before DQS	750	575	470	1
tDS (dram)	DRAM Data Setup Time	350	300	250	1
Skew Budget	System DQ-to-DQS Setup Skew = tDVB - tDS	400	275	220	1

Note 1:The timing numbers are for example only. Design should be based on the latest component specifications, FB-DIMM AMB and JESD 79-2 DRAM.

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Example DIMM Post-AMB Write Hold Timing (PC2-4200/PC2-5300/PC2-6400)[1]

Parameter	Definition	Time (ps) PC2-4200	Time (ps) PC2-5300	Time (ps) PC2-6400	Notes
tDVA (amb)	AMB Data Valid After DQS	750	575	470	1
tDH (dram)	DRAM Data Hold Time	350	300	250	1
Skew Budget	System Budget for DQ-to-DQS Hold Skew = tDVA - tDH	400	275	220	1

Note 1: The timing numbers are for example only. Design should be based on the latest component specifications, FB-DIMM AMB and JESD 79-2 DRAM.

Example DIMM Post-AMB CK-to-DQS Timing (PC2-4200/PC2-5300/PC2-6400)[2]

Parameter	Definition	Time (ps) PC2-4200	Time (ps) PC2-5300	Time (ps) PC2-6400	Notes
tCLK	Clock Cycle Time	3750	3000	2500	2
tDQSCKamb	Clock/DQS Skew at AMB	210	200	190	1, 2
tDQSSmax	tCLK * 1.25	4688	3750	3125	2
tDQSSmin	tCLK * 0.75	2813	2250	1875	2
Skew Budget	System CK-to-DQS Delay Skew (tDQSSmax) = tDQSSmin/max - tCK - tDQSCK	728	550	435	2

Note 1: tDQSCKamb includes allowance for clock output jitter
Note 2: The timing numbers are for example only. Design should be based on the latest component specifications, FB-DIMM AMB and JESD 79-2 DRAM.

Example DIMM Post-AMB CK-to-C/A/Control Setup Timing (PC2-4200/PC2-5300/PC2-6400)[1]

Parameter	Definition	Time (ps) PC2-4200	Time (ps) PC2-5300	Time (ps) PC2-6400	Notes
tCVB (amb)	C/A/CNTL Valid before Clock	1615	1260	1030	1
tIS (dram)	DRAM Command/Address/Control Setup	500	400	375	1
Skew Budget	System Budget for DQ-to-C/A/Control Setup Skew (Setup) = tCVB - tIS	1115	860	655	1

Note 1:The timing numbers are for example only. Design should be based on the latest component specifications, FB-DIMM AMB and JESD 79-2 DRAM.

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Example DIMM Post-AMB CK-to-C/A/Control Hold Timing (PC2-4200/PC2-5300/PC2-6400)[1]

Parameter	Definition	Time (ps) PC2-4200	Time (ps) PC2-5300	Time (ps) PC2-6400	Notes
tCVA (amb)	C/A/CNTL Valid after Clock	1475	1120	890	1
tIH (dram)	DRAM Command/Address/Control Hold	500	400	375	1
Skew Budget	System Budget for DQ-to-C/A/Control Hold Skew (Hold) = tCVA - t IH	975	720	515	1

Note 1:The timing numbers are for example only. Design should be based on the latest component specifications, FB-DIMM AMB and JESD 79-2 DRAM.

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Design collateral for specific Raw Cards

Some usage and design information is specific to an individual raw card design. This specification captures collateral information by raw card design.

ODT provides termination to DQ/CB signals and has programmable values that are dynamically turned on in response to ODT signals provided by the AMB. DDR values are programmed via MRS/EMRS settings.

ODT values

Card	Speed	Transaction	AMB[1]	Rank 0 ODT[1]	Rank 1 ODT[1]
R/C A	533/667	Write	OFF	75	N/A
		Read	65	OFF	N/A
	800	Write	OFF	75	N/A
		Read	65	OFF	N/A
R/C B, E, H	533/667	Write	OFF	150	150
		Read	65	OFF	OFF
	800	Write	OFF	75	150
		Read	65	OFF	OFF
R/C C	533/667	Write	OFF	75	N/A
		Read	65	OFF	N/A
	800	Write	OFF	75	N/A
		Read	65	OFF	N/A
R/C D, J	533/667	Write	OFF	150	75
		Read	65	OFF	OFF
	800	Write	OFF	OFF	50
		Read	65	OFF	OFF

Note 1: Recommended values.

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Test Mode collateral

AMB devices support a mode that allows transparent access to DRAM interface directly with some special handling to accommodate double data rate data transfers. Details of operation in this mode are available in FB-DIMM AMB DFT Specification. The table documents the transparent DRAM interface signal mapping to the module pinout.

Transparent Mode Pinout

pin	Transparent Mode Signal	pin	Transparent Mode Signal	pin	Transparent Mode Signal
142	CKE[1]	181	A[3]	222	TPF[8]
143	CKE[0]	178	A[2]	219	TPF[7]
145	CS[1]	175	A[1]	216	TPF[6]
146	CS[0]	172	A[0]	213	TPF[5]
148	ODT	102	TDRV	202	TPF[4]
149	RAS#	103	TCMP	199	TPF[3]
151	CAS#	99	TDQ[15]	196	TPF[2]
152	WE#	96	TDQ[14]	193	TPF[1]
154	BA[2]	93	TDQ[13]	190	TPF[0]
155	BA[1]	82	TDQ[12]	40	TDQO[15]
157	BA[0]	79	TDQ[11]	48	TDQO[14]
160	A[15]	76	TDQ[10]	66	TDQO[13]
168	A[14]	73	TDQ[9]	63	TDQO[12]
186	A[13]	70	TDQ[8]	60	TDQO[11]
183	A[12]	100	TDQ[7]	57	TDQO[10]
180	A[11]	97	TDQ[6]	54	TDQO[9]
177	A[10]	94	TDQ[5]	222	TDQO[8]
174	A[9]	83	TDQ[4]	219	TDQO[7]
171	A[8]	80	TDQ[3]	216	TDQO[6]
161	A[7]	77	TDQ[2]	213	TDQO[5]
169	A[6]	74	TDQ[1]	202	TDQO[4]
187	A[5]	71	TDQ[0]	199	TDQO[3]
184	A[4]	--	--	196	TDQO[2]
--	--	--	--	193	TDQO[1]
--	--	--	--	190	TDQO[0]

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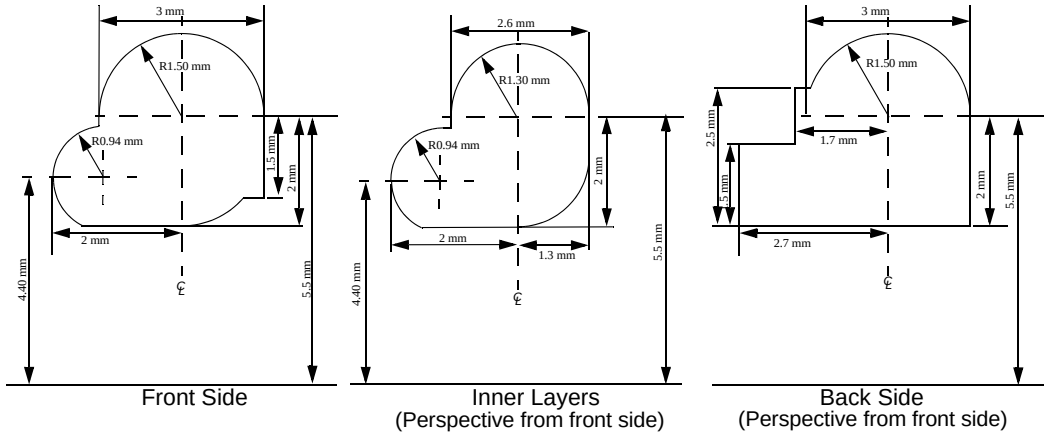
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Recommended trace keepout

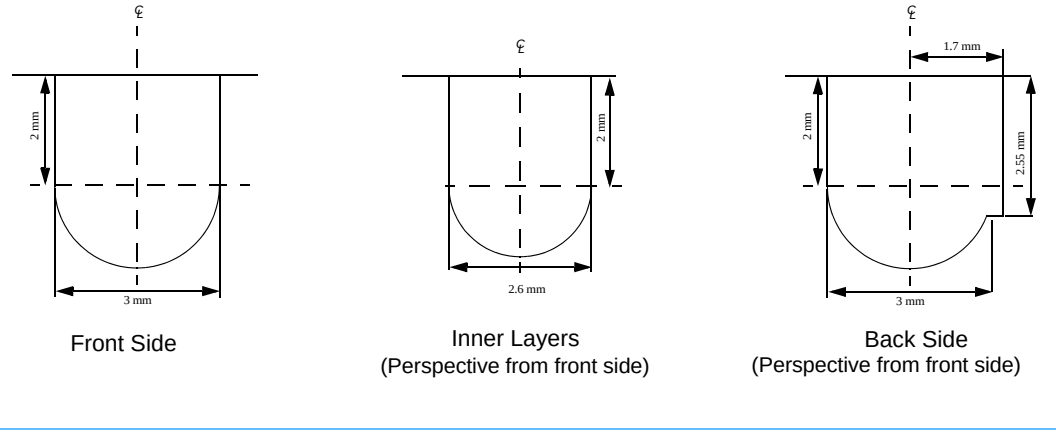
AMB components may require some thermal solution that includes a heat spreader attached to AMB device. Heat Spreader attachment methods may require holes or notches for heat spreader retention features.

Below are recommended trace keep out regions that provide for a common keep out area that corresponds to component keep out regions documented in MO-256 details.
Keep-out areas are intended generally for use by AMB buffer Heat Spreader retention features; details are applicable to MO variations AA,AB,AC, BA,BB and BC. Through-holes, notches or associated retention features may be located in these areas.

Trace keep out area in connector area



Trace keep out area in module top edge area



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Vcc Power Delivery

Robust Vcc DC power delivery must be ensured by the FB-DIMM designs. System designers should ensure AMB voltage tolerance is met when these dimm requirements are included in a system analysis.

For purposes of design FB-DIMM designs should target 4.75 mOhm nominal impedance for Vcc DC resistance. Some variation among raw card designs is allowed via a design tolerance.
Additionally, manufactured modules will have some variations and is represented in a manufacturing tolerance. Manufactured modules **should** meet **the** resistance range that incorporates design tolerance and manufacturing tolerances. **Qualification of a design should be by direct resistance measurement. During HVM manufacture, power delivery quality can be verified indirectly by functional tests.**

Effective Resistance Target 4.75 mOhm Nominal @ 23C(room temp)

Tolerance	Min	Max	Min resistance	Max Resistance	Comment
Design	-5%	+5%	4.51	4.99	Design Analysis must meet this range
Manufacturing	-15% Total (Design Min -10%)	+22% Total (Design Max +15%)	4.06	5.74	All manufactured modules must meet this range

Effective Resistance is the Vcc-to-Vss path resistance seen from the module edge fingers, it is comprised of two components: Reffective = Rvcc + Rvss.

Measurement of the effective path resistance is impractical due to multiple paths involved;

A satisfactory approximation is Reffective = Rkelvin + 0.70 mOhm;
where:
Rkelvin is a specific measurable path,
0.70 mOhm accounts for Rvss and residual Rvcc elements not included in Rkelvin path

For purposes of standard analysis and measurement, the following measurement points shall be used for measuring Vcc DC resistance in a Kelvin 4-wire measurement. Deriving Vcc Resistance from measurement:

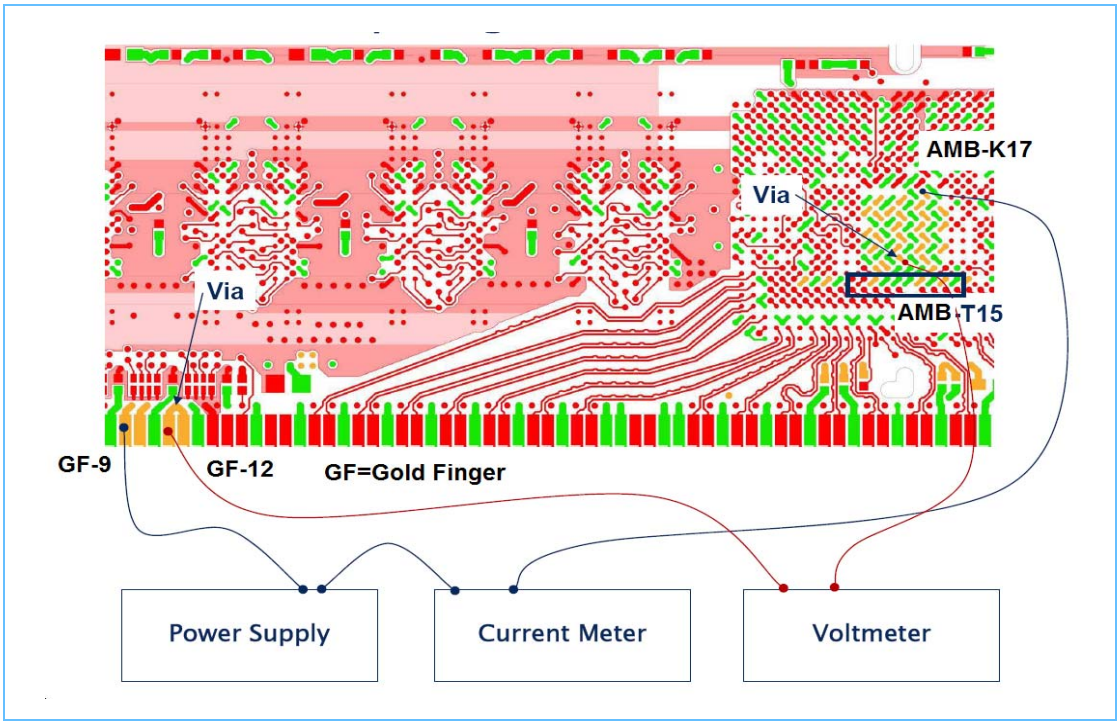
Rkelvin = |Vsense/Isource|

Kelvin Measurement Ports

Port	Adjacent Via of Edge Finger	Adjacent Via of AMB Ball	Function	Comment
A	9	--	Source HI	Current Source
B	12	--	Sense HI	Voltage Sense +
C	--	T15	Sense LO	Voltage Sense -
D	--	K17	Source LO	Current Source return

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Rkelvin Measurement Diagram



Injecting 100mA of current with a well regulated power supply, actual current and voltage can be measured with precision to derive Rkelvin.

Suggested equipment requirements for measurements

Equipment	Measurement Range	Minimum Resolution	Comment
Power Supply	100mA		current limit set point
Digital Meter	100mA	see note 1	Isource
Digital Meter	20mV	see note 1	Vsense

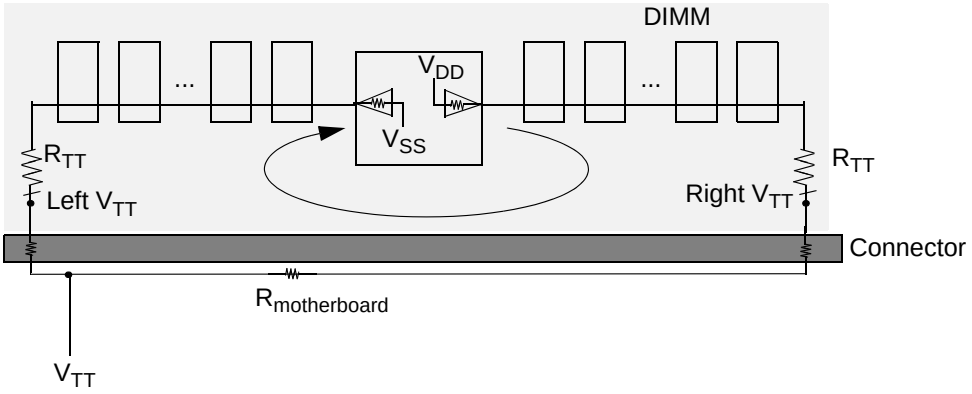
Note 1: Required tolerance is 1% or better. Designers should ensure analysis method accuracy through correlation to kelvin measurement results. Example analysis:
Rkelvin = 5mOhm; Accuracy 1% (50uOhm); Current set point: Isource = 100mA
Minimum Volt-meter resolution: 100mA x 50uOhm = 5uV
Minimum Current-meter resolution:5uV / 5mOhm = 1mA

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V_{TT} Provisions

AMB buffers provide complementary CA bus (between left CA bus and right CA bus). Complementary drivers generate current that travels through the R_{TT} network between the left and right CA buses.

Example Complementary CA Bus Current Path



$I_{left} = 0.9V/(R_{driver} + R_{TT} + R_{connector})$

$I_{right} = 0.9V/(R_{driver} + R_{TT} + R_{connector} + R_{motherboard})$

$Delta = M(I_{left} \times R_{connector}) + M(I_{right} \times R_{connector}) + MN(I_{right} \times R_{motherboard})$

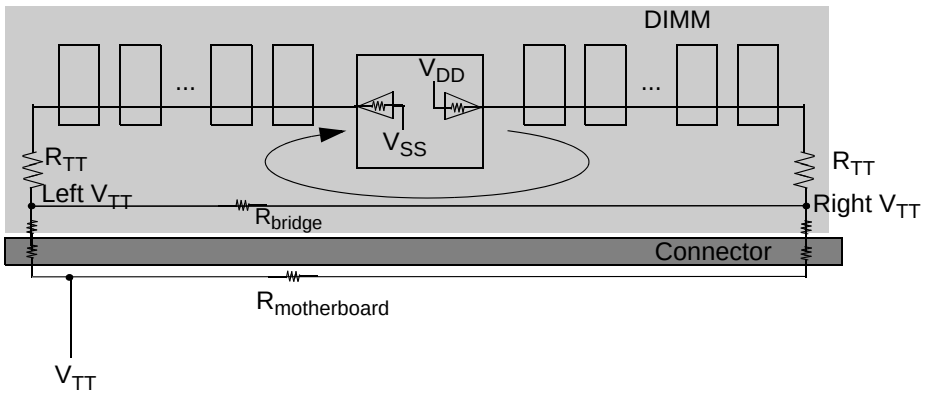
where: Delta is difference between Left V_{TT} and Right V_{TT},
N=number of dimms installed in system,
M=number of complementary CA signals

(Complete analysis requires complex summations not shown here)

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For purposes to limit V_{TT} voltage difference between left and right R_{TT} networks (due to voltage drop of connector and motherboard) some FB-DIMM designs should provide a connection on the dimm between left and right V_{TT} rails. Requirements of connection are dependent on R_{TT} values and subsequent analysis with system assumptions (complex summations). .

Example FB-DIMM bridge connection requirement



(Complete analysis requires complex summations not shown here)

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Based on analysis, the following resistance design requirements were developed to ensure V_{TT} tolerance range is met when complementary CA bus operation is considered. Effort should be spent to minimize effective resistance as low as is feasible. Meeting the max values shown in the table will ensure that induced offset on V_{TT} supply is controlled. System designers need to ensure that baseboard contributions in conjunction with these DIMM assumptions limit induced offset to values shown in Product Family Attributes table earlier in this document.

Effective Resistance (mOhm) Max @ $23°C$ (room temp) for 533/667 FB-DIMMs

Module	Edge Finger to Rtt network	R bridge	Comment
R/C A	6	N/A	No left/right connection needed
R/C B	6	N/A	No left/right connection needed
R/C C	6	N/A	No left/right connection needed
R/C D	10	50	
R/C E	7	52	
R/C H	7	52	
R/C J	10	50	

Effective edge finger to R_{TT} network Resistance is the average path resistance seen from the module edge fingers to local R_{TT} network.

Measurement of the effective path resistance is impractical due to multiple paths involved;

A satisfactory approximation is Reffective = Rkelvin ;

where:

Rkelvin is a specific measurable path representative of the median path,

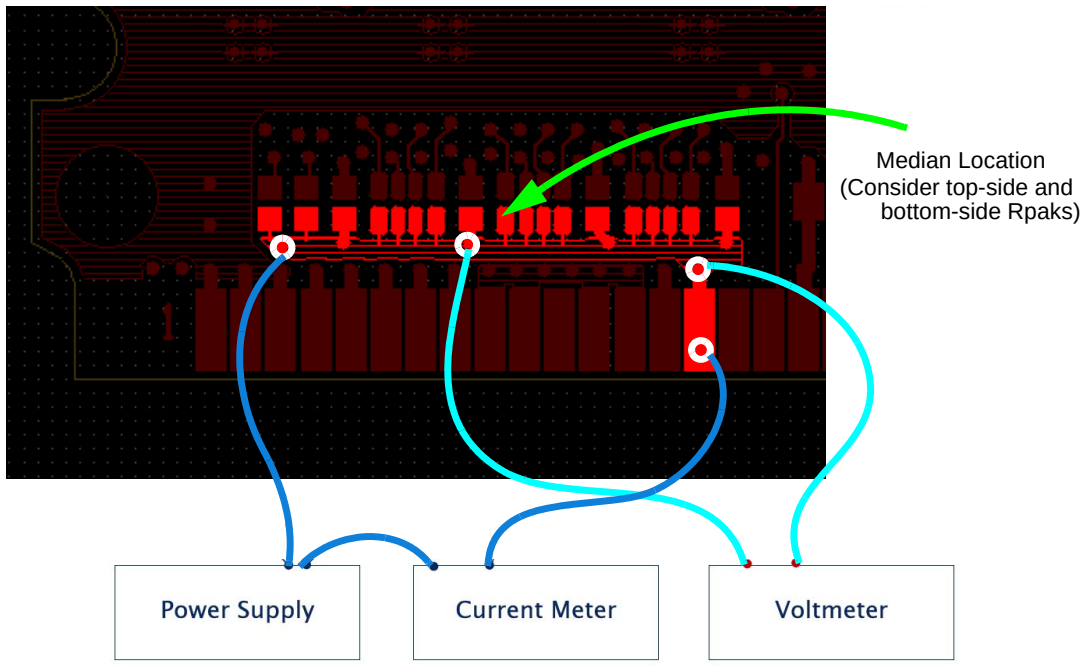
For purposes of standard analysis and measurement, the following measurement points shall be used for measuring V_{TT} DC resistance in a Kelvin 4-wire measurement. Deriving V_{TT} Resistance from measurement:

Rkelvin = |Vsense/Isource|

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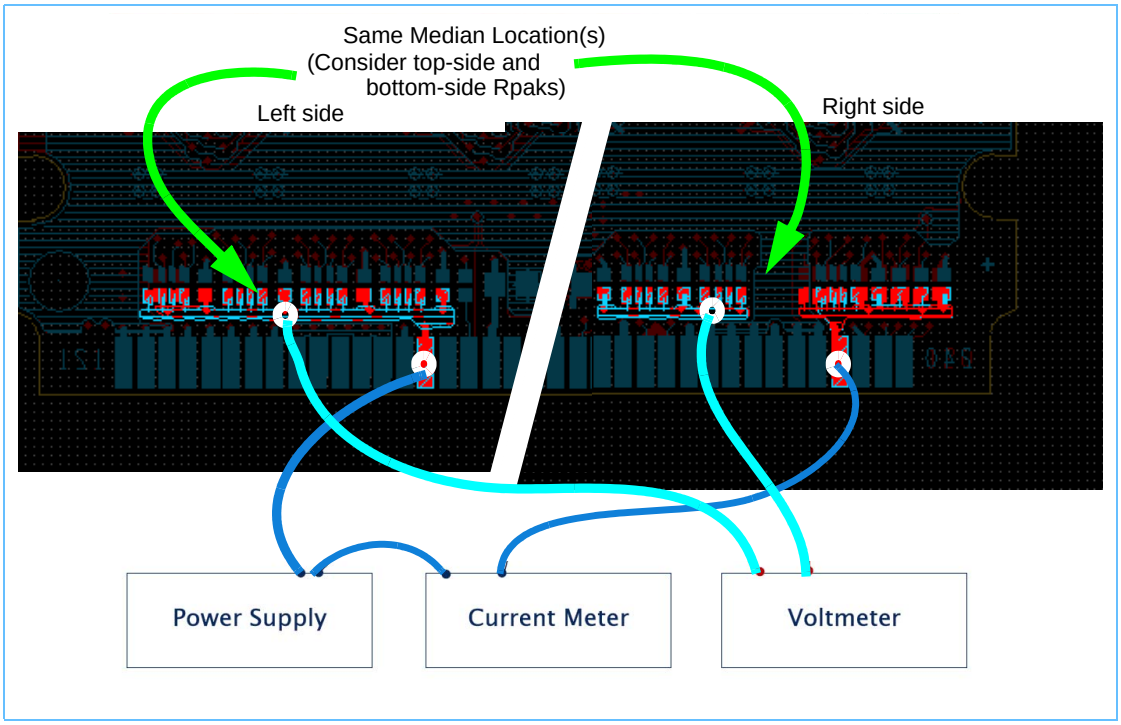
Typical Rkelvin Ports

(Shows typical Left Edge finger to R_{TT}network, use similar ports for right side)



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Typical Rkelvin Ports (Shows example R bridge measurement)



Injecting 100mA of current with a well regulated power supply, actual current and voltage can be measured with precision to derive Rkelvin;

Equiment considerations are the same as those specified in Vcc Resistance measurement.

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Serial Presence Detect Definition

The Serial Presence Detect (SPD) function MUST be implemented on the PC2-4200/PC2-5300/PC2-6400 DDR2 SDRAM FB-DIMM. The component used and the data contents must adhere to the most recent version of the JEDEC FB-DIMM SPD Specifications. Please refer to this document for all technical specifications and requirements of the serial presence detect devices. Please refer to this document for all technical specifications and requirements of the Serial Presence Detect devices (Refer to JEDEC ballot JC-45... for SPD field definitions)

The following table is intended to be an **example** of a fast bin PC2-6400 DIMM. SPD values indicating different DIMM characteristics will be utilized based on specific characteristics of the DIMMs. This example assumes:

- Module Organization: 512MB (64Mx72)
- Device Composition: 64Mx8
- Device Package: FBGA
- Module Physical Ranks: 1
- CAS latency: 4

(Editor Note: Table Below is subject to review in SPD TG)

Example 512Mb 1 rank 533 4-4-4 SPD image

Byte #	Function Description	SPD Entry Value	SPD BYTE (Hex)	Notes
0	Number of Serial PD Bytes in CRC	size=256; CRC = 116; used bytes=128	0x92	
1	SPD Revision	rev 1.0	0x10	
2	Key Byte/ DRAM Device Type	DDR2 FB-DIMM	0x09	
3	Voltage levels of this Assembly	Dram=1.8V; channel=1.5V	0x12	
4	SDRAM Addressing	row=14 col=10 bank=4	0x44	
5	Module Physical Attribues	30~35mm height 8~9mm thick	0x24	
6	Module Type	FB-DIMM 133.35mm nom	0x07	
7	Module Organization	1 rank x8 device width	0x09	
8	Fine Timebase Divend and Divisor	5ps	0x51	
9	Medim Timebase Divident	1(0.25ns)	0x01	
10	Medium Timebase Divisor	4(0.25ns)	0x04	
11	SDRAM Min Cycle TIme (tCKmin)	3.75ns(266MHz)	0x0f	
12	SDRAM Max Cycle Time (tCKmax)	8ns(125MHz)	0x20	
13	SDRAM CAS Latencies Supported	CL=3,4	0x23	
14	SDRAM Min CAS Latency (tAA)	15ns	0x3c	
15	SDRAM Write Recovery Times Supported	WR=3,4	0x23	

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Example 512Mb 1 rank 533 4-4-4 SPD image

Byte #	Function Description	SPD Entry Value	SPD BYTE (Hex)	Notes
16	SDRAM Write Recivery Time (tWR)	15ns	0x3c	
17	SDRAM Write Latencies Supported	WL=4,5,6	0x34	
18	SDRAM Additive Latencies Supported	AL=0,1,2,3	0x40	**
19	SDRAM Min RAS to CAS Delay (tRCD)	15ns	0x3c	
20	SDRAM Min Row Active to Row Active Delay (tRDD)	7.5ns	0x1e	
21	SDRAM Minimum Row Precharge Time (tRP)	15ns	0x3c	
22	SDRAM Upper Nibbles for tRAS and tRC	0	0x00	
23	SDRAM Minimum Active to Precharge Time (tRAS)	45ns	0xb4	
24	SDRAM Minimum Auto-Refresh to Active/Auto-Refresh Time (tRC)	55ns	0xdc	
25	DRAM Minimum Auto-Refresh to Active/Auto-Refresh Command (tRFC)	105ns	0xa4	
26			0x01	
27	SDRAM Internal Write to Read Command Delay (tWTR)	7.5ns	0x1e	
28	SDRAM Internal Read to Precharge Command Delay (tRTP)	7.5ns	0x1e	
29	SDRAM Burst Lengths Supported	BL8,BL4	0x03	
30	SDRAM Terminations Supported	75/150	0x03	
31	SDRAM Weak Drivers Supported	supported	0x01	
32	SDRAM Average Refresh Interval (tREFI) / Double Refresh t / High Temp self-refresh rate support indication	7.8us, 1x hot refresh, no hot self-refresh	0x02	see byte 33
33	Bits 7:4: Tcasemax Delta Bits 3:0: DT4R4W Delta (	Tcasemax=85C DT4R4W case rise=0.8C	0x02	
34	Thermal resistance of SDRAM device package from top (case) to ambient (Psi T-A SDRAM) at still air condition based on JESD51-2 standard.	32C/W	0x40	
35	DT0: Case temperature rise from ambient due to IDD0/activate-precharge operation minus 2.8 ◦C offset temperature.	3.7C	0x20	
36	DT2N/DT2Q: Case temperature rise IDD2N/precharge standby operation and IDD2Q/precharge quiet standby operation	1.6C	0x10	
37	DT2P: Case temperature rise IDD2P/precharge power-down operation.	0.24C	0x10	
38	DT3N: Case temperature rise IDD3N/active standby operation.	2.4C	0x10	
39	DT4R/Mode Bit: Bits 7:1: Case temperature rise IDD4R Bit 0: Mode bit to specify if DT4W is greater or less than DT4R.	9.6C 4W > 4R	0x30	
40	DT5B: Case temperature rise IDD5B/burst refresh operation.	10.5C	0x15	
41	DT7: Case temperature rise IDD7/bank interleave read mode operation.	16C	0x20	
42..59	Reserved		0x00	
60..80	Reserved		0x00	

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Example 512Mb 1 rank 533 4-4-4 SPD image

Byte #	Function Description	SPD Entry Value	SPD BYTE (Hex)	Notes
81	FB-DIMM Channel Protocols Supported	ECC Only	0x02	
82			0x00	
83	additional Back-to-Back Access Turnaround Time	r/w 2clk w/r 1clk r/r 1clk	0x25	
84	AMB Read Access Time for DDR2-800 (AMB.LINKPARNXT[1:0] = 11)	(5 + 6/12)* tCK	0x56	
85	AMB Read Access Time for DDR2-667 (AMB.LINKPARNXT[1:0] = 10)	(4 + 4/12)* tCK	0x44	
86	AMB Read Access Time for DDR2-533 (AMB.LINKPARNXT[1:0] = 01)	(3 + 10/12)* tCK	0x3a	
87	Thermal Resistance of AMB Package from top (case) to ambient (Psi T-A SDRAM) at still air condition based on JESD51-2 standard.	24C/W	0x30	
88	AMB DT Idle_0	53C	0x35	
89	AMB DT Idle_1	77C	0x4d	
90	AMB DT Idle_2	71C	0x47	
91	AMB DT Active_1	98C	0x62	
92	AMB DT Active_2	77C	0x4d	
93	AMB DT L0s	not supported	0x00	
94	Reserved		0x00	
95	Reserved		0x00	
96	Reserved		0x00	
97	Reserved		0x00	
98	Reserved		0x00	
99	Reserved		0x00	
100	Reserved		0x00	
101	AMB Personality Bytes: Pre-Init	GB (rev 0.3)	0xc0	
102			0x00	
103			0x00	
104			0x44	
105			0x00	
106			0x00	

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Example 512Mb 1 rank 533 4-4-4 SPD image

Byte #	Function Description	SPD Entry Value	SPD BYTE (Hex)	Notes
107	AMB Personality Bytes: Post-Init	GB (rev 0.3)	0x40	
108			0x43	
109			0x00	
110			0x00	
111			0x6d	
112			0x04	
113			0x00	
114			0x05	
115	AMB Manufacturer's JEDEC ID Code	Intel ID	0x80	
116			0x89	
117	Module ID: Module Manufacturer's JEDEC ID Code	(TBD)	0x00	
118			0x00	
119	Module ID: Module Manufacturing Location		0x01	
120	Module ID: Module Manufacturing Date	year (2004)	0x04	
121		(week)	0x52	
122	Module ID: Module Serial Number	(TBD)	0x84	
123			0x00	
124			0x03	
125			0xc1	
126	Cyclical Redundancy Code	(TBD)	0x56	
127			0xc3	
128..145	Module Part Number	alpha string(TBD)	0x20	
146	Module Revision Code		0x00	
147			0x01	
148	SDRAM Manufacturer's JEDEC ID Code		0x00	
149			0x2c	
150	Manufacturer's Specific Data	GB SPD rev	0x00	GB SPD rev is example usage
151			0x03	
152..175			0xff	
176..255	Customer Use		0xff	

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FBDIMM Label Format

The following label shall be applied to all DDR2 memory modules to fully describe the key attributes of the module. The label can be in the form of a stick-on label, silk screened onto the assembly, or marked using an alternate customer-readable format. A minimum font size of 8 points should be used, and the number can be printed in one or more rows on the label. Hyphens may be dropped when lines are split, or when font changes sufficiently separate fields.

ggggg eRxff PC2-wwwwm-abc-dd-ef

Where:

ggggg = Module total capacity, in bytes
- 256MB, 512MB, 1GB, 2GB, 4GB, etc.

eR = Number of ranks of memory installed
- 1R = 1 rank of DDR2 SDRAM installed
- 2R = 2 ranks

xff = Device organization (bit width) of DDR2 SDRAMs used on this assembly
- x4 = x4 organization (4 DQ lines per SDRAM)
- x8 = x8 organization
- x16 = x16 organization

wwww = Module bandwidth in MB/s
- 3200 = 3.20 GB/s
- 4200 = 4.26 GB/s
- 5300 = 5.33 GB/s
- 6400 = 6.40 GB/s

m = Module Type
- E = Unbuffered DIMM ("UDIMM"), with ECC (x72 bit module data bus)
- F = Fully Buffered DIMM ("FB-DIMM")
- M = Micro-DIMM
- N = Mini-Registered DIMM ("Mini-RDIMM"), no address/command parity function
- P = Registered DIMM ("RDIMM"), with address/command parity function
- R = RDIMM, no address/command parity function
- S = Small Outline DIMM ("SO-DIMM")
- U = Unbuffered DIMM ("UDIMM"), no ECC (x64 bit module data bus)

a = DDR2 SDRAM CAS Latency, in clocks at maximum operating frequency

b = DDR2 SDRAM minimum tRCD specification, in clocks at maximum operating frequency

c = DDR2 SDRAM minimum tRP specification, in clocks at maximum operating frequency

dd = JEDEC SPD Revision Encoding and Additions level used on this DIMM

e = Reference design file used for this design (if applicable)
- A = Reference design for raw card A is used for this assembly
- B = Reference design for raw card B is used for this assembly
- Z = None of the reference designs were used for this assembly

f = Revision number of the reference design used
- 0 = Initial release
- 1 = First revision
- 2 = Second revision
- P = Pre-release or Engineering sample
- Z = To be used when field e = Z

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Examples, single font:

1GB 1Rx4 PC2-3200F-333-10-C0

is a 1GB DDR2 Fully Buffered DIMM, using 1 rank of x4 SDRAMs operational to PC2-3200 performance with CAS Latency = 3, t_{RCD} = 3, t_{RP} = 3, using JEDEC SPD revision 1.0 (encoding type FB-DIMM), raw card reference design file C initial release used for the assembly

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DIMM Mechanical Specifications

JEDEC has standardized detailed mechanical information for the 240Pin DIMM family. This information can be accessed on the worldwide web as follows:

1. Go to JEDEC official site; http://www.jedec.org.

2. Click on ‘Free Standards ’ and enter the free download area.

3. Search by document number: ‘MO-256’ and download the PDF for this product family.

4. Or search by ‘JEP95’;‘JEDEC Publication 95.’ and open entire document,scroll down and select ‘MO-256’ to download the PDF for this product family.

Within MO-256, several DIMM thickness variations are defined. Variations are denoted by a two letter reference “XX”. The first (MSB) letter position encodes dimm thickness and height attributes . The second(LSB) letter position encodes keying position, three positions are defined(--A,--B,--C)

Note: Maximum DIMM thickness/height can be a measured maximum value, or can be calculated using the maximum component, card, label, and assembly process adders.

FB-DIMMs utilize a single keying position (--B) and can utilize any of the thickness/height variations.
Note: Some system platforms may be designed for a subset of specific variations.

To enable systems to electronically detect DIMM thickness, SPD byte 5 is encoded with the FB-DIMM thickness and height values. When used, in conjunction with other SPD bytes, system operating conditions can be adjusted based on installed modules and projected power consumption.

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Supporting Hardware:

Summary of FB-DIMM Support/Development Hardware

Vendor	name	p/n
Agilent Customer Contact Center 800-829-4444 http://www.agilent.com/find/fbd us@agilent.com Agilent Technologies / Perry Keller 1900 Garden of the Gods Rd. Colorado Springs, CO, 80907 perry_keller@agilent.com (719) 590-5651 FuturePlus Systems Corp. / Bill Furch (719) 278-3540 http://www.futureplus.com	4x Resistor Pack Flying Lead Probe	N4234A
	4x/8x BGA DRAM Interposer Probe	N4237A
	Interposer Channel Analysis Probe	FSI-60105 / FS2343
	DIMM Parametric Test Fixture	N4236A
	Slot Channel Analysis Probe	FSI-60097 / FS2338
	Slot Parametric Probe	N4238A
	AMB Parametric Test Fixture	N4235A
	RC/B Validation DIMM Logic Analysis Probe	FSI-60099 / FS2340
Tektronix Customer Support Center 800-833-9200 x3 503-627-2400 Fax: 503-627-5695 www.tek.com/memory Tektronix, Inc. David Haworth PO Box 500, M/S 39-345 Beaverton, OR 97077-0001 503-627-3127 David.A.Haworth@tek.com Nexus Technology, Inc. Bruce Krobusek 877-595-8116 x803 brucekro@busboards.com	12.5GHz Z-Active Differential Probe	P7313
	Serial Data Compliance and Analysis Software	TDSRT-EyeTM v2
	Jitter and Timing Analysis Software	TDSJIT3 v2
	FB-DIMM Interposer Probe & Analysis Software	NEX-FBD-LAI
	FBD Oscilloscope Probing Kit	NEX-TDSFBDP
	FB-DIMM AMB to DDR2 Analysis Probe & Software	NEX-FBD-NEXVu

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Summary of FB-DIMM Support/Development Hardware

Vendor	name	p/n
King Tiger Technology Inc., David Jaime 9601 Amberglen Blvd., Suite 120, Austin, TX 78729 512-401-8775 http://www.kingtigertech.com	King Tiger KT-2Pro DIMM Tester	King Tiger KT-2Pro DIMM Tester
Pycon Inc 3301 Leonard Court Santa Clara, CA 05054 Rob Ortega (408) 450-5609 rortega@pycon.com	Channel Test Card (CTC)	FB-DIMM Channel Test Card

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Diagnostic Sense Line

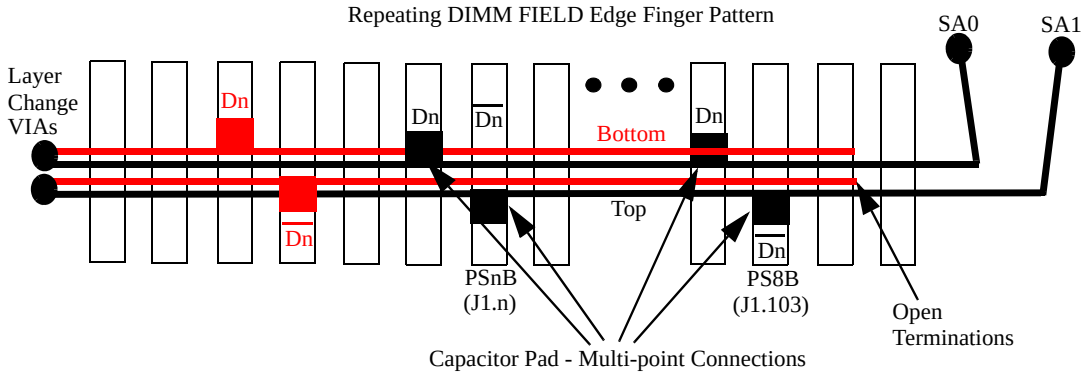
FBDIMM - Diagnostic Sense Line Specification, Introduction

FBDIMM Diagnostic sense lines are by design, ground referenced transmission lines, with specifically placed, routine and regular, capacitor pad multi-point connections. These sense lines couple to the "True" and "Compliment" high speed differential data card edge fingers, by means of proximity capacitive interconnect technology.

In a system that implements sense lines, the connection from the Memory Controller Unit (MCU) to the FBDIMM Hub chip now becomes a multipoint connection connecting the MCU to the Advanced Memory Buffer (AMB) and with diagnostic sense line connections to the Instrumentation Chip. The Instrumentation Chip serves as the diagnostic detection chip, to sense the signal activity or lack of signal activity on the High Speed Link. It does this one side of a differential pair at a time, and thus is capable of diagnosing the electrical continuity between the MCU and the AMB.

Diagnostic sense lines are routed just under the card edge fingers and begin at one end of the DIMM finger field pattern, then travel perpendicularly across the DIMM finger field down to the other end of the DIMM. The test traces then cross over to the other side of the PCB through a pair of layer change VIAs. They then travel back towards the point of origination in the same fashion with an open termination at the end of the line. See General Concept below.

General Concept



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Implementation Details

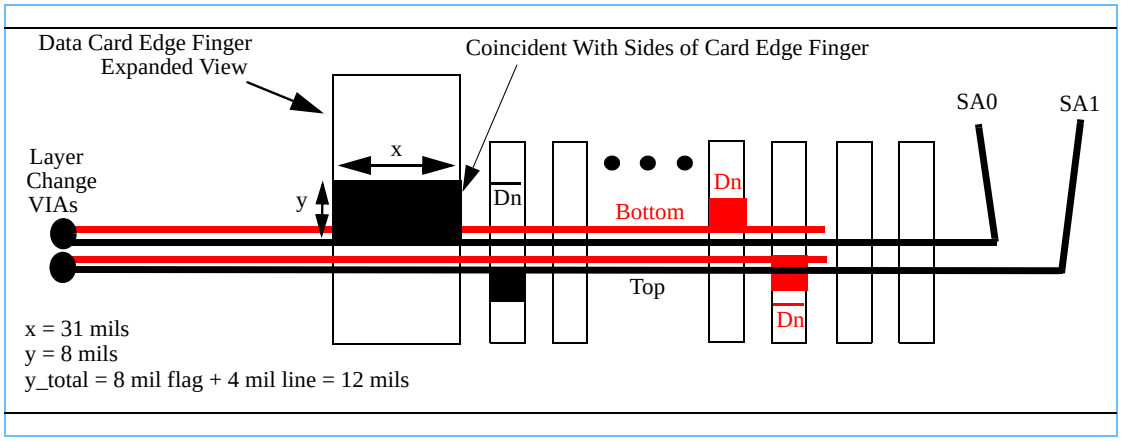
Capacitor Pad Connection Concept

There are one pair of sense line capacitor pad traces per DIMM. Each sense line shall originate at the right side of the DIMM (oriented card edge finger down and top side up). One sense line capacitor pad capacitively connects to the North and Southbound high-speed TX/RX "True" card edge fingers starting at PS8 (J1.102) then, PS7 (J1.99), then PS6 (J1.96), and continuing on. The other capacitively connects to the corresponding North and Southbound high-speed TX/RX "Compliment" card edge fingers starting at PS8B (J1.103) then, PS7B (J1.100), then PS6B (J1.97), and continuing on. See General Concept.

Capacitor Connection Pad Size and Placement

The capacitor connection pad is designed to be 31 mils x 12 mils. Each Flag extends off of the transmission line width is 8 mils. Adding the transmission line width (4 mils) results in the 12 mil pad height. The pads are placed as shown below.

Capacitor Connection Pad



Diagnostic Sense Line Routing Line Width and Spacing

Diagnostic sense lines shall have a line width of 4 mils and a edge to edge spacing of 4 mils.

Diagnostic Sense Line Same Layer Isolation

Diagnostic sense lines shall be isolated from any other active route or shape on the same layer by greater than or equal to 20 mils.

Diagnostic Sense Line Adjacent Layer Isolation

Diagnostic sense lines shall be isolated from any other active route or shape on the adjacent signal layer by greater than or equal to 20 mils. Crossing the diagnostic sense lines in any way with routes or shapes on the adjacent signal layers is not allowed.

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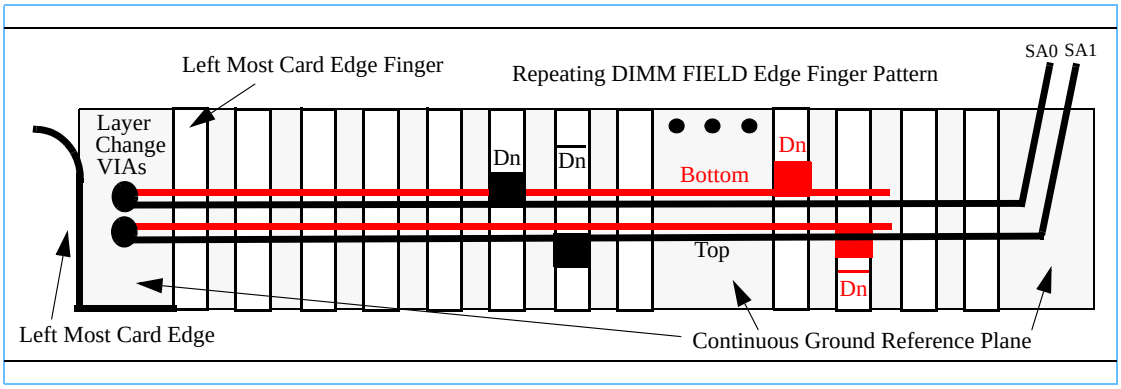
Diagnostic Sense Line Reference Planes

Diagnostic sense lines shall be referenced to ground. Ground shapes shall be placed on layers 3 and 4, or 3 and 6, or 3 and 8 of a 6, 8, or 10 layer board respectively. They shall shadow the card edge finger field all along the card edge of the DIMM. The width of the shape is essentially set to be the height of the rectangular card edge finger shape height.

There are two approved topologies shown in **Diagnostic Sense Line Topologies, Segment Lengths, and Terminations** section later in this text. Both of these topologies must be implemented with a uniform and continuous ground reference plane. See example of preferred topology with a uniform and continuous ground reference plane shown in the figure below.

Note – Uniform and continuous ground plane is required to follow the sense line routes around the notch. This is not shown in figure below but is implied.

Diagnostic Sense Line Reference Plane Shape and Location



Layer change transition VIAs are designed with the following parameters:

1. VIA Type = Plated Through Hole
2. VIA Drill Hole Size = 12 mils +0.002/-0.006
3. VIA Land (Internal) = 18 mils
4. VIA Land (Outer) = 20 mils
5. VIA Antipad (Internal) = 30 mils
6. VIA Finished Hole Size = 12 mils

Note – Remove the pads from unconnected layers

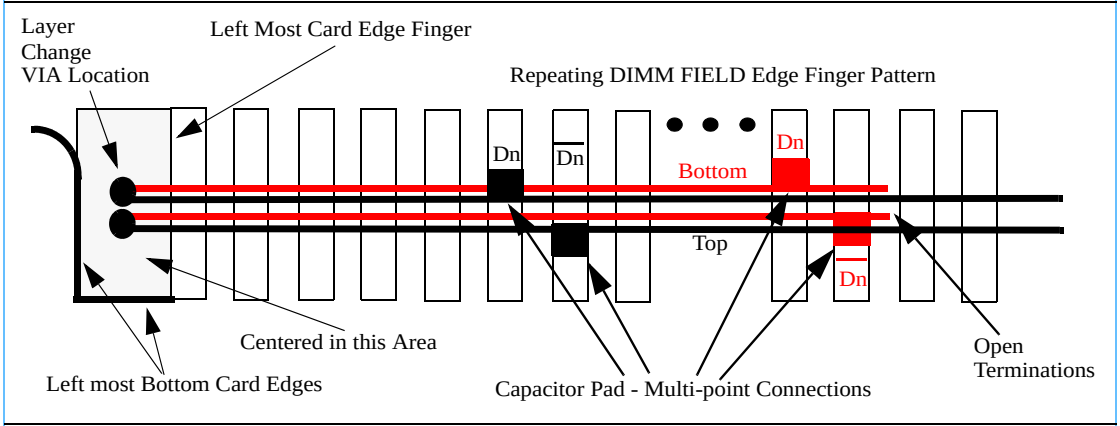
Diagnostic Sense Line Layer Change VIA location

Layer change transition VIAs are to be placed at the left side of the board and centered in the region bounded in the "X" direction by the left card edge and the left most edge of the last card edge finger. They are bounded in "Y" direction by the bottom card edge and the top of the card edge finger shape. See figure below.

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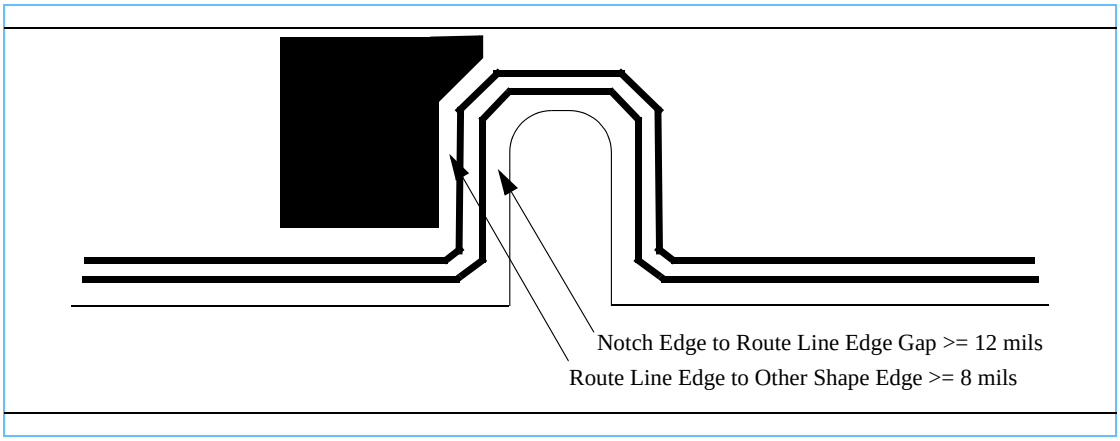
Routing around the DIMM Key Notch

Layer Change Transition VIA Location



When routing around the DIMM key notch, care must be taken to maintain the 4 mil line width and 4 mil spacing. Use 45 degree angle turns as shown below.

Routing Around the DIMM Key Notch



Diagnostic Sense Line Topologies, Segment Lengths, and Terminations

There are two acceptable diagnostic sense line topologies. The first is the preferred topology. The second is a less than optimal alternate, but approved topology.

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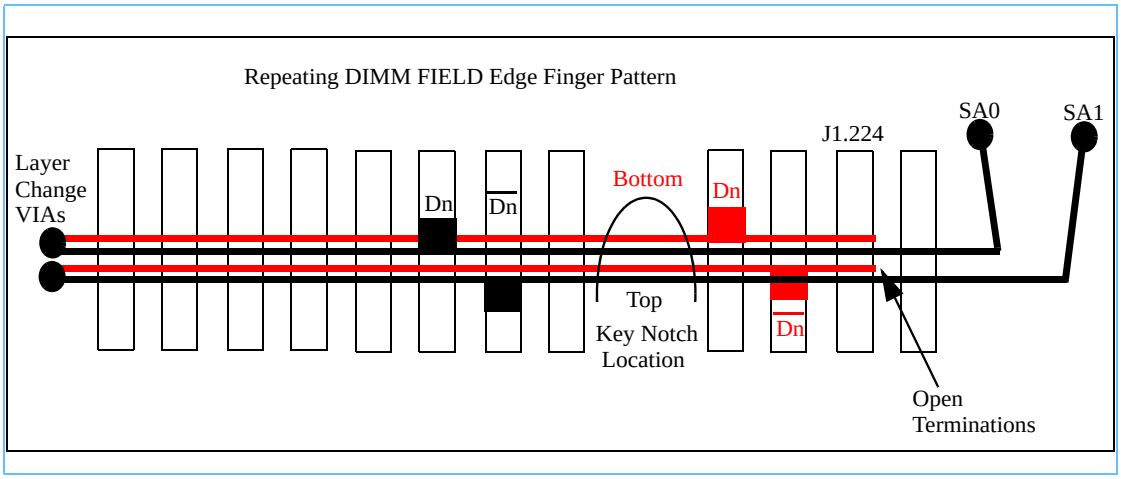
Preferred Topology

A pair of diagnostic sense lines shall travel from the right side of the card (oriented card edge finger down and top side up). They originate at a pair of VIAs connected to address bits SA0 and SA1. They run horizontally under the card edge fingers towards the left side of the card. The route travels on layer 2 of either a 6, 8, or 10 layer board. This leg of the sense line route is to be approximately 5.2 inches long.

The sense line pair then crosses over to the opposite side of the PCB through a pair of layer change vias. Once on the opposite side, they are to travel back towards the point of origination on layer 5, 7, or 9 of a 6, 8, or 10 layer board respectively.

The route is to then terminate at the right most edge of card edge finger J1.224 as an open termination at the end of the line. This leg of the route is to be approximately 4.5 inches long. See Preferred Topology shown below.

Diagnostic Sense Line - Preferred Topology



Alternate Topology (Forked Topology)

A pair of diagnostic sense lines shall travel from the right side of the card (oriented card edge finger down and top side up). They originate at a pair of VIAs connected to address bits SA0 and SA1. They run horizontally under the card edge fingers towards the left side of the card. The route travels on layer 2 of a 6, 8, or 10 layer board. This leg of the sense line route is to be approximately 5.2 inches long.

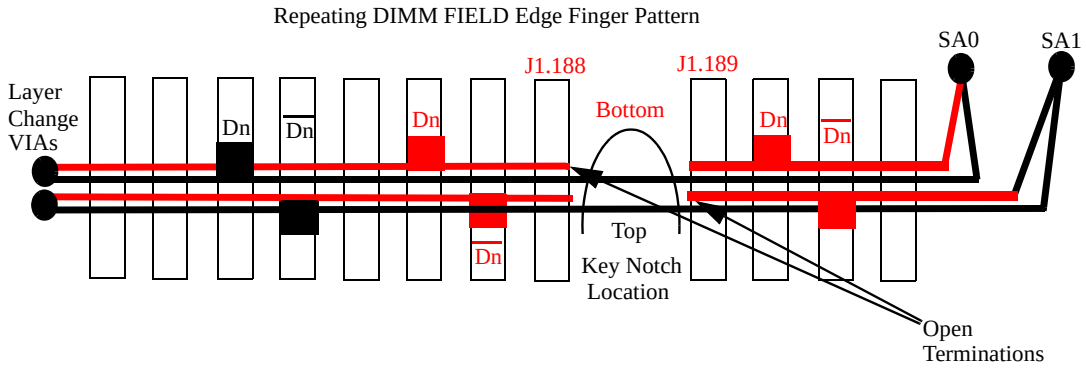
The sense line pair then crosses over to the opposite side of the PCB through a pair of layer change vias. Once on the opposite side, they travel back towards the point of origination on layer 5, 7, or 9 of a 6, 8, or 10 layer board respectively.

This back side segment terminates at the right most edge of card edge finger J1.188 as an open termination at the end of this line segment. This leg of the route is to be approximately 2.7 inches long.

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A second back side sense line segment originates and forks off of the same VIAs connected to address bits SA0 and SA1 (right side of the card) and then travels right to left on layer 5, 7, or 9 of a 6, 8, or 10 layer board respectively. This back side segment terminates at the left most edge of card edge finger J1.189 as an open termination at the end of this line segment. This leg of the route is to be approximately 2.2 inches long. See Alternate Topology below.

Diagnostic Sense Line - Alternate Topology



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Conclusion

While both the Alternate and the Preferred Topologies are designed to provide adequate diagnostic sense line signal strength to the input of the Instrumentation Chip, the implementation of the Preferred Topology will produce the highest signal power possible for any given system implementation.

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Revision Log

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Revision	Pages	Changes
Intel 0.55b	all	Initial content
Intel 0.60a		Removed all references to raw cards E and F Updated net topologies and lengths for channel Added pair-to-pair spacing rules for channel Updated net lengths for DRAM data Added pin descriptions and pinout for AMB Showed DM connection on x8 DIMMs Changed AMB on block diagram to show channel flow through NC pins on DRAM may be connected to VDD on DIMM Updated R/C A picture to show support for wider DRAM Removed example SPD values
	all	Added "JEDEC Confidential -- For Internal Use Only"
	5	Removed "also used to select DIMM number in AMB" from SDA, really belongs on SA(2:0)
	18	Added note 2, TESTLO_AB20 and TESTLO_AC20 should be configured for debug purposes
	23	Added note on DRAM size for R/C A
	30	For pair-to-pair spacings, separation is a multiple of dielectric height only
	32	Updated clock trace lengths
	34	Replaced "byte spread" with |DQ - DQS|
Intel 0.60b	5	Added "also used to select DIMM number in AMB" to SA(2:0)‘
	6	Changed pin 117, 237 to VTT
	8,10	Removed ‘s’
	9,10	changed ‘byte’ to ‘nibble’
	11-14	changed notes concerning NC pins
	15-16	added language on footprint NC/NU pins from registered DIMM spec
	18	added ‘also used to select DIMM number in AMB” to SA[2:0]
	24	added side view
	32	add note about CK0 on left, CK1 on right
	43	change FB- to PC2-
Intel 0.60c	3	Added table including channel clock and transfer rate, added "DRAM" to clock in text
	4	Added Introductory table of raw cards. Re-ordered notes on environmental table
	5	Added "DIMM connector" to title.

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Revision Log **DDR2 SDRAM Fully Buffered DIMM Design Specification**

	11	Added introduction to the DRAM component and common footprint details
	28-39	Removed references to trace impedance, Removed offset skew in AMB package and DIMM, increased max on SB signals by 2.2 mm Updated R/C B Command/Address bus trace lengths, renumbered segments Updated R/C B Control bus trace lengths, renumbered segments
	40	Indicated that power is typically delivered on outer layer power islands
	42	Re-calculated timing budgets using skew budgets, instead of margins
	43	Added calculations for CK-to-DQS and CK-to-C/A/Control
	44	Added note that table is temporarily removed
Intel 0.60d	12,14	changed 60 to 63 balls
	13	changed A1 reference to E2
	15	Changed A2 reference to H2. Changed H2, L1 and L9 in x4 package from NC to NU
	16	Changed 68 to 71 balls. Changed H2, L1 and L9 in stacked x4 package from NC to NU
	28-30	Replaced TL1 with TL- in the notes
	29	Changed 8.4 to 9.1 mm. For matching tolerance on northbound primary channel, distinguish between nets shorter and longer than 12 mm (this is especially for PN10/PN10#)
	38	Organized control into variation 1 and 2, updated lengths, changed R1 back to TBD
	40	Clarified component breakout, changed 0.100 to 0.102
0.20a		Changed to JEDEC rev 0.20 from Intel rev 0.60e
	5	non-stacked variations called out as MO-256 variation AB stated variations called out as MO-256 variation BB
	7	RFU pin count was reduced DNU/M_Test was added Note 2 was updated to reflect correct RFO accounting
	8	FBDIMM Pinout diagram updated for DNU/M_Test
	9~12	Power connectivity adjusted to include SPD
	24	Module Configuration table updated to reflect 4Gb page size change to be the same as 1Gb and 2Gb page sizes
	25~27	updated component placement diagrams and associated side-views
	29	added notes to indicate $\overline{\text{DQS}}$ usage on R/C's A & B added noes to indicate left and right copies of DRAM Addr/cmd/ctrl
	31	added R/C's A & C to trace length table TL1 and SUM changed to unique min and max values
	32	added R/C's A & C to trace length tables PN TL1 and SUM Max values changed to 34.4 SN TL1 max changed to 34.6; SUM max changed to 37.0 Notes updated short pair matching from TBD to +/- 0.5 mm

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	33	SS TL1 max changed to 39.1 SS SUM max changed to 42.3 Pair-to-Pair changes: microstrip outer < 20mm changed to 4.25xheight microstrip outer > 20mm changed to 5.25xheight stripline changed to 3.7xheight added 4 notes Added Minimum Trace Widths table for System Data Channel Nets
	34	changed “Copy A” to “Variation 1” In variation 1, changed TL1 segment to TL3, added new TL1 in series with TL0 added specific values to trace length table for R/C A split note 1 into notes 1 & 2 added note 4
	35	changed B CK1 TL1 min to 8.6 changed note 2 to “Trace length difference between the two elements of a differential pair, measured from the AMB to any DRAM, must not exceed 0.5 mm”
	36	R/C A DQ/CB/DQS/$\overline{\text{DQS}}$ TL0 updated separate min/max values Note 1 dropped tolerance reference Note 3 changed to “Trace length difference between the DQS/DQS traces and the DQ traces of a given byte (Raw Card A) or nibble (Raw Cards C, D) must not exceed 0.5 mm, unless up to 5 mm of additional trace is added to DQS/DQS# to improve write setup margin, in which case, the spread across the DQ signals must not exceed 1 mm. DRAM positions TBD have TBD additional trace on DQS/DQS#
	37	In DQ diagram changed “DIMM Connector” to “AMB” Note 3 changed to “Trace length difference between the DQS/DQS traces and the DQ traces of a given byte (Raw Card A) or nibble (Raw Cards C, D) must not exceed 0.5 mm, unless up to 5 mm of additional trace is added to DQS/DQS# to improve write setup margin, in which case, the spread across the DQ signals must not exceed 1 mm. DRAM positions TBD have TBD additional trace on DQS/DQS#
	38	added separate R/C C DQ diagram and table
	39	added separate R/C A Address/Command diagram and table
	40	updated R/C B and C Address/Command Trace lengths added R1 value of 39 ohms Note 5 dropped “from the AMB output to the pad of the VTT R-pack”
	41	added R/C A Control Trace Lengths added R/C A R1 value of 39 added R/C B R1 value of 47 changed notes 4~6 to: 4. For Raw Card A, variation 1 is for CS0B and CKE0B, variation 2 is for CS0A, CKE0A. 5. For Raw Card B, variation 1 is for CS1A, CKE1A, CS0B and CKE0B, variation 2 is for CS0A, CKE0A, CS1B and CKE1B. 6. On Raw Card A, any two adjacent TL4 segments have a sum of between 19.1 and 19.7 mm. 7. On Raw Card B, any two adjacent TL4 segments have a sum of between 27.0 and 32.3 mm.
	42	added R/C C Control diagram and table
	45	On Cross Section Recommendation, Note in edge connector dropped “and not chamfered” PCB Electrical Specs changed to include nom 60 Ohm for single ended, w/adjustments to min/max nom 85 for Zdiff DRAM clocks and DQS/DQS# w/adjustments to min/max
	46	added trace geometry examples to single-ended table removed 100 Ohm example from outer layer differential example.

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Revision Log **DDR2 SDRAM Fully Buffered DIMM Design Specification**

	47~48	Footnoted unofficial AMB/DRAM timing values as unapproved estimates.
	51	changed 4.26 GB/sec to 4.27 GB/sec changed 5.34 GB/sec to 5.33 GB/sec
0.21	global	changed PC2-4300 to PC2-4200
	5	added min/max values 1.7/1.9 for DRAM added min/max values 1.46/1.54 fro AMB; footnoted as estimate added min/max values 0.48*VDD/0.52*VDD for VTT added min/max values 3.0/3.6 for VDDSPD
	7	updated editorial wording of M_test description
	9~12	added “control” to Rtt terminated groups in block diagrams changed ‘banks’ to ‘ranks’ in R/C Block Diagram titles page 11: changed ‘72’ to ‘x72’ in diagram title
	19	(new page) added Early 2Gb x4 and x8 Ballout with support balls; note calls out x4 differences
	27~29	updated side-view dimensions to reflect proposed JC-11 MO-256 base values w/o HS
	31	changed Dram Address/Command/Control Notes: “one set for left, one set for right”
	33	updated R/C C System Clock Trace Lengths as per Infineon: TL0 1.9; TL2 0.6;
	36	updated R/C A AMB CLK Output to SDRAM Trace Lengths: R/C A Variation 2 TL1min from 14.6 to 14.7; TL4min/max from 18.2/18.4 to 19.8/20.2 R/C A Variation 1 TL3max from 10.7 to 10.0; TL4min form 18.5 to 18.4
	37	added AMB Clock Output to SDRAM Trace Lengths for R/C C values as per Infineon
	40	(new page) added unique R/C C DQ/C/DQS/DQS# diagram and table
	41	added unique R/C C to Address/Command diagram (R/C B,C,D; variation #1) and table
	42	added unique R/C C to Address/Command diagram (R/C B,C,D; variation #2) and table
	45	updated R/C C Control Net Trace Length: TL0max fro m2.7 to 2.2; End-to-End max from 79.8 to 78.0 removed reference to R/C F
	49	(new page) added Example Eight layer Stackup diagram
	53	changed ‘Module Physical Banks’ to ‘Module Physical Ranks’
	55	In labeling spec, changed 4300 to 4200 for module bandwidth
0.5	global	removed multiple footer references to approved/passed ballots as well as bars that indicate changes to previous document revisions
	6	clarified explanation of R/C
	25	timing parameters in table were changed to be consistent with the rest of document added note 1
	26	added the latest specification numbers
	34, 35, 36	updated trace lengths for R/C A, B and C added trace lengths for R/C D
	39	added diagram for R/C D net structure routing for AMB Clock Output to SDRAM added table with trace lengths for AMB Clock Output to SDRAM net structure

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	40	added R/C D trace lengths for DQ, CB, DQS, DQS# net structure and changed note 4
	41	updated R/C B DQS/DQS# trace lengths and changed note 4
	42	changed note 4
	46	added diagram that describes R/C D net structure routing for Address/Command to SDRAM added table with R/C D trace lengths for Address/Command net structure
	47	added diagram that describes R/C D net structure routing for ODT to SDRAM added table with R/C D trace lengths for ODT net structure
	50	added diagram that describes R/C D net structure routing for Control to SDRAM added table with R/C D trace lengths for Control net structure
	51-54	added chapter DDR2 Fully Buffered DIMM Biasing Details with diagrams/tables
	55	clarified cross-section recommendation
	57	added example 10 layer stackup
	59, 60, 61	multiple changes in paragraphs/tables: clarified that timing numbers used in the timing tables are for example only; multiple changes in description column and in timing values; added note 1
	63	added chapter “Design collateral for specific Raw Cards” including table with ODT values
	65	added “Test Mode collateral” chapter with table that describes transparent mode pinout
	69-70	label format updated
1.0	65	added trace KO page
	44,45,48	modified R/C B net lengths/Rterm as per review in TG
	23,58,59, 60	updated example timing values for amb and dram contributions
	37,40,45, 48	modified R/C A net lengths as per review in TG
	9,10,11,12	added SA0 resistors
	25	strike out TBD Note for additional ctritical AMB params; clarified table footnote to reference AMB spec
	74	Lifted Mechanical wording from RDIMM Spec.
	67..70	added SPD table
	75	added Supporting Hardware information
	25,26,27	on R/C A device placement drawing adjusted position of SPD device to match gerber; removed thickness dimensions, added reference to MO-256
	17,18	replaced “footprint” with “landing pattern”
1.0 BoD	8	PBAR param consistent with RDIMM Spec.
	16,18,19, 20	corrected reference to DRAM MO-XXX for ballouts with support balls
	15-20	made terminology consistent to “landing pattern” (table titles and notes)

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	17,18	corrected actual ball counts
	21	added Dram max outline by raw card
	79	revised HW List
2.0	Global	Introduced R/C E, H and J to spec. Multiple addition in different sections, mostly focusing on topologies
3.0	7	Product Faminly Attributes table was updated (MO256 variations; AMB Vcc voltage)
	15~25	SDRAM Component details and Dram Size Table updated
	97~98	Vcc power delivery section added
	65~68	R/C E and H CA termination value change.
	91	ODT Table corrected typographiocal error by numbering rank 0,1 (was numbered rank1,2)
	99~104	Vtt delivery
	47	dual stripline rule
	53~55,69, 70,73	R/C J adjustments
	80	VCC PLL Filter figure updated

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Exhibit C

The Wayback Machine - http://web.archive.org/web/20071021053839/http://www.jedec.org:80/Catalog/display.cfm

JEDEC CATALOGUE

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[Document type-|- Committees-|-Keywords-|-Revision Status]

Document Type

NUMBER	JEDEC Engineering Bulletins (JEB)	PRICE
JEB 5-A	METHODS OF MEASUREMENT FOR SEMICONDUCTOR LOGIC GATING MICROCIRCUITS: The purpose of this bulletin is to recommend for use in the rating of semiconductor logic gating microcircuits which use the binary states to represent and process logic information. Both static and dynamic measurements are covered. January 1970; Reaffirmed February 1984 /JEDEC Committee	$63.00
JEB 6	STANDARD MEASURMENTS OF THE ELECTRICAL CHARACTERISTICS OF SEMICONDUCTOR INTEGRATED CIRCUITS December 1966; Rescinded October 1984 / Committee!33JCJEDC	
JEB 15	TERMINOLOGY AND METHODS OF MEASUREMENT FOR BISTABLE SEMICONDUCTOR MICROCIRCUITS: This bulletin explains the terminology and methods of measurement for bistable semiconductor microcircuits. It is also intended to be used with the EIA Registration Data Format for semiconductor integrated bistable logic circuits. November 1969 /JC-40 Committee	$109.00
JEB 16	USER GUIDE FOR MICROCIRCUIT FAILURE ANALYSIS: This guide defines generalized procedures for the failure analysis of monolithic integrated microelectronic circuits. Although the generalized procedural steps may apply to all microelectronic circuits, additional analysis steps unique to thin/thick film hybrid devices are not covered. July 1970; Rescinded November 2004 September 2003 /JC-14 Committee	$41.00
JEB 17	USER GUIDELINES FOR QUALITY AND RELIABILITY ASSURANCE OF LSI COMPONENTS November 1970; Rescinded April 1987 April 1987	
JEB 19	RECOMMENDED CHARACTERIZATION OF MOS SHIFT REGISTERS: This recommendation applies to MOS Shift Registers. Definitions are	

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given for P-channel registers but are applicable to all CMOS and N-channel with changes in power supply notation.

November 1972 /JC-40 Committee $40.00

JEB 20 **ACCEPTED PRACTICES FOR MAKING MICROELECTRONIC DEVICE THERMAL CHARACTERISTICS TESTS**

January 1975; Rescinded November 1988 /JC-11 Committee

NUMBER Tentative Standards (TENTSTD) PRICE

TENTSTD 11 **HANDLING AND INSTALLATION OF POWER SEMICONDUCTORS IN DISC TYPE PACKAGES: Included in JESD282 and EIA397.**

July 1973; Rescinded June 1992 June 1992 /JC-22.2 Subcommittee

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TENTSTD 12 **STANDARD FOR SELENIUM SURGE SUPPRESSORS:** The suppresser furnished under this standard shall be a product that has been tested and meets the definitions and minimum requirements specified herein.

November 1973 /JC-22.5 Subcommittee $49.00

NUMBER JEDEC Specifications (JES) PRICE

JES 2 **TRANSISTOR, GALLIUM ARSENIDE POWER FET, GENERIC SPECIFICATION:** Establishes guideline requirements and quality assurance provisions for gallium arsenide power field-effect transistors (FETs, also know as MESFETs) designed for use in high-reliability space application such as spacecraft communications transmitters. Identifies the electrical parameters, wafer acceptance tests, screening tests, qualification tests, and lot acceptance tests pertinent to power GaAs FETs. Applicable to packaged and chip-carrier parts; portions may not be applicable to unpackaged and unmounted chips.

July 1992 /JC-14.7 Subcommittee $71.00

NUMBER JEDEC Standards (JESD) PRICE

JESD 1 **LEADLESS CHIP CARRIER PINOUTS STANDARDIZED FOR LINEARS:** This standard shows how to convert existing DIP pinouts for op-amps, comparators, and D/A converters, to chip carrier packages.

April 1982 / Committee!33JC41 $41.00

JESD 2 **DIGITAL BIPOLAR LOGIC PINOUTS FOR CHIP CARRIERS:** This standard provides a chip carrier format for digital devices by defining pin functions and locations for 20, 38, 44, 52, and 68-terminal devices.

December 1982 /JC-40.1 Subcommittee $41.00

JESD 3-C **STANDARD DATA TRANSFER FORMAT BETWEEN DATA PREPARATION**

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	SYSTEM AND PROGRAMMABLE LOGIC DEVICE PROGRAMMER: This standard was developed to prevent the proliferation of data transfer formats that occurred with microprocessor development systems. The focus of the standard is on field programmable devices and their support tools. It is not intended for other types of semicustom logic devices or other types of fabrication or testing equipment. June 1994 / Committee!33JC421	$61.00
JESD 4	**DEFINITION OF EXTERNAL CLEARANCE AND CREEPAGE DISTANCES OF DISCRETE SEMICONDUCTOR PACKAGES FOR THYRISTORS AND RECTIFIER DIODES:** This standard defines reference distances between terminals of the device and the external package at specific voltages. November 1983; Reaffirmed January 1991, April 1999, April 2002 April 2002 /JC-22.2 Subcommittee	$38.00
JESD 5	**MEASUREMENT OF TEMPERATURE COEFFICIENT OF VOLTAGE REGULATOR DIODES:** This standard is designed to define voltage-temperature characteristic measurement techniques and a method of calculation. Although many methods could be defined, this method provides a desired uniformity and lends itself to production testing. Formerly JEDEC Suggested Standard No. 5A February 1982; Reaffirmed April 1999, April 2002 April 2002 /JC-22.4 Subcommittee	$38.00
JESD 6	**MEASUREMENT OF SMALL VALUES OF TRANSISTOR CAPACITANCE:** This standard gives a test method for measuring transistor capacitance using a three-terminal bridge which employs a guard-circuit that eliminates the effect of extraneous capacitance. February 1967; Reaffirmed September 1981, April 1999, October 2002 /JC-25 Committee	$47.00
JESD 7-A	**STANDARD FOR DESCRIPTION OF 54/74HCXXXX AND 54/74HCTXXXX HIGH SPEED CMOS DEVICES:** This standard provides uniformity, multiplicity of sources, eliminate confusion, and ease of device specification and design by users for HC, and HCT CMOS devices. This standard specifies electrical parameters. It also includes appendices listing part numbers. August 1986 / Committee!33JC402	$109.00
JESD 8- 1	**ADDENDUM No. 1 to JESD8: INTERFACE STANDARD FOR LOW VOLTAGE TTL-COMPATIBLE (LVTTL) VLSI DIGITAL CIRCUITS** June 1994; Incorporated into JESD8-A, June 1994. JESD8-A was replaced by JESD8-B, September 1999. /JC-16 Committee	
JESD 8- 1-A	**INTERFACE STANDARD FOR NOMINAL 0.3 V/3.3 V SUPPLY DIGITAL INTEGRATED CIRCUITS**	

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June 1994; Incorporated into JESD8-A, June 1994. JESD8-A was replaced by JESD8-B, September 1999. /JC-16 Committee

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JESD 8- 2 **ADDENDUM No. 2 to JESD8 - STANDARD FOR OPERATING VOLTAGES AND INTERFACE LEVELS FOR LOW VOLTAGE EMITTER-COUPLED LOGIC (ECL) INTEGRATED CIRCUITS:** This Addendum No. 2 to JEDEC Standard No. 8 provides standard operating voltage and interface levels that can be used by designers and application engineers as they develop and introduce new products. Covers the ECL logic family designated 300K ECL. The 300K ECL family is Voltage and Temperature Compensated, with I/O interface levels compatible with the existing 100K ECL and 101K ECl families.

March 1993 /JC-16 Committee $40.00

JESD 8- 3A **ADDENDUM No. 3A to JESD8 - GUNNING TRANSCEIVER LOGIC (GTL) LOW-LEVEL, HIGH-SPEED INTERFACE STANDARD FOR DIGITAL INTEGRATED CIRCUITS:** This Addendum No. 3 to JEDEC Standard No. 8 defines the dc input and output specifications for a low-level, high-speed interface for integrated devices.

May 2007 December 2006 /JC-16 Committee $40.00

JESD 8- 4 **ADDENDUM No. 4 to JESD8 - CENTER-TAP-TERMINATED (CTT) INTERFACE LOW-LEVEL, HIGH-SPEED INTERFACE STANDARD FOR DIGITAL INTEGRATED CIRCUITS:** This Addendum No. 4 to JEDEC Standard No. 8 defines the dc input and output specifications for a low-level, high-speed interface for integrated devices that can be a super-set of LVCMOS and LVTTL.

November 1993 /JC-16 Committee $38.00

JESD 8-5A.01 **ADDENDUM No. 5 to JESD8 - 2.5 V 0.2 V (NORMAL RANGE), AND 1.8 V TO 2.7 V (WIDE RANGE) POWER SUPPLY VOLTAGE AND INTERFACE STANDARD FOR NONTERMINATED DIGITAL INTEGRATED CIRCUIT:** This standard defines power supply voltage ranges, dc interface parameters for a high speed, low voltage family of non-terminated digital circuits driving/driven by parts of the same family. The specifications in this standard represent a minimum set of 'base line' set of interface specifications for CMOS-compatible circuits.

September 2007 September 2004 /JC-16 Committee $43.00

JESD 8- 6 **ADDENDUM No. 6 to JESD8 - HIGH SPEED TRANSCEIVER LOGIC (HSTL)- A 1.5 V OUTPUT BUFFER SUPPLY VOLTAGE BASED INTERFACE STANDARD FOR DIGITAL INTEGRATED CIRCUITS:** This standard is a 1.5 volt high performance CMOS-based interface document suitable for high I/O count CMOS and BiCMOS devices operating at frequencies in excess of 200 Mhz.

August 1995 /JC-16 Committee $48.00

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JESD 8- 7A **ADDENDUM No. 7 to JESD8 - 1.8 V + -0.15 V (NORMAL RANGE), AND 1.2 V - 1.95 V (WIDE RANGE) POWER SUPPLY VOLTAGE AND INTERFACE STANDARD FOR NONTERMINATED DIGITAL INTEGRATED CIRCUIT:** This standard continues the voltage specification migration to the next level beyond the 2.5 V specification already established. Since this migration is driven by both process changes and performance/power, more entries can be expected in supporting required voltage levels. The rapidity of this evolution is expecting to increase because of the same feature sizes expected.

June 2006 June 2004 /JC-16 Committee $43.00

JESD 8- 8 **ADDENDUM No. 8 to JESD8 - STUB SERIES TERMINATED LOGIC FOR 3.3 VOLTS (SSTL_3) A 3.3 V VOLTAGE BASED INTERFACE STANDARD FOR DIGITAL INTEGRATED CIRCUITS:** This standard is a result of a major effort by the JC-16 Committee to develop a high performance CMOS-based interface suitable for high speed main memory applications in excess of 125 MHz.

August 1996 /JC-16 Committee $47.00

JESD 8- 9B **ADDENDUM No. 9B to JESD8 - STUB SERIES TERMINATED LOGIC FOR 2.5 VOLTS (SSTL_2): Includes Errata and Corrected Page 7 as of October 18, 2002.** This standard defines the input, output specifications and ac test conditions for devices that are designed to operate in the SSTL_2 logic switching range, nominally 0 V to 2.5 V. The standard may be applied to ICs operating with separate VDD and VDDQ supply voltages. This standard has been developed particularly with the objective of providing a relatively simple upgrade path from MOS push-pull interface designs. The standard is particularly intended to improve operation in situations where busses must be isolated from relatively large stubs.

May 2002 /JC-16 Committee $55.00

JESD 8- 11A.01 **ADDENDUM No. 11A.01 to JESD8 - 1.5 V +/- 0.1 V (NORMAL RANGE) AND 0.9 - 1.6 V (WIDE RANGE) POWER SUPPLY VOLTAGE AND INTERFACE STANDARD FOR NONTERMINATED DIGITAL INTEGRATED CIRCUITS:** This new standard provides specifications that will be used by several companies in new 1.5 V products designed in 0.12-0.15 um CMOS technologies, and in components that interface with them. The specifications allow limited interoperability with products using the existing JEDEC HSTL specification (JESD8-6). This version is a minor editorial revision as noted in Annex A.

September 2007 June 2004 /JC-16 Committee $41.00

JESD 8- 12A.01 **1.2 V +/- 0.1 V (NORMAL RANGE) AND 0.8 - 1.3 V (WIDE RANGE) POWER SUPPLY VOLTAGE AND INTERFACE STANDARD FOR NONTERMINATED DIGITAL INTEGRATED CIRCUITS:** This standard defines power supply voltage ranges, dc interface and switching

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parameters for a high speed, low voltage family of nonterminated digital circuits driving/driven by parts of the same family, or mixed families which comply with the input receiver specifications. The specifications in this standard represent a minimum set of interface specifications for CMOS compatible circuits.

September 2007 June 2004 /JC-16 Committee $41.00

JESD 8-13

SCALABLE LOW-VOLTAGE SIGNALING FOR 400 MV (SLVS-400): This standard defines the input, output, and termination specifications for differential signaling in the SLVS-400 environment, nominally between 0 and 400 mV. Power supplies other than the nominal 800 mV power for the SLVS interface are not specified.

October 2001 /JC-16 Committee $41.00

JESD 8-14A.01 

1.0 V +/- 0.1 V (NORMAL RANGE) AND 0.7 V - 1.1 V (WIDE RANGE) POWER SUPPLY VOLTAGE AND INTERFACE STANDARD FOR NONTERMINATED DIGITAL INTEGRATED CIRCUITS: This new standard provides specifications that will be used by several companies in new 1.0 V products designed in 0.10-0.12 um CMOS technologies, and in components that interface with them. This standard defines power supply voltage ranges, dc interface and switching parameters for a high speed, low voltage family of nonterminated digital circuits driving/driven by parts of the same family, or mixed families which comply with the input receiver specifications. The specifications in this standard represent a minimum set of interface specifications for CMOS compatible circuits. This version is a minor editorial revision as noted in Annex A.

September 2007 June 2004 /JC-16 Committee $41.00

JESD 8-15A

STUB SERIES TERMINATED LOGIC FOR 1.8 V (SSTL_18): This standard defines the input, output specifications and ac test conditions for devices that are designed to operate in the SSTL_18 logic switching range, nominally 0 V to 1.8 V. The standard may be applied to ICs operating with separate VDD and VDDQ supply voltages. The VDD value is not specified in this standard; however VDD and VDDQ will have the same voltage level in many cases.

September 2003 /JC-16 Committee $49.00

JESD 8-17

DRIVER SPECIFICATIONS FOR 1.8 V POWER SUPPLY POINT-TO-POINT DRIVERS This material is intended to be reflected in supplier specifications for point to point DDR devices ranging from 400 Mb/s to 800 Mb/s operation. It is a method to specify driver impedance with something other than a number that does not nec-essarily define how it operates in a real net This standard addresses this issue using net lengths and specifies how much uncertainty can exist in the data for each speed supported.

November 2004 May 2002 /JC-16 Committee $40.00

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JESD 8-18 **FBDIMM SPECIFICATION: HIGH SPEED DIFFERENTIAL PTP LINK AT 1.5 V** This specification is a JEDEC standard for the point-to-point link for the Fully Buffered DIMM.It is the result of a large amount of work from many people and is derived from prior internal specifications used at Intel Corporation with feedback from external vendors and the JEDECFully-Buffered DIMM Link Signaling Task Group.

September 2006 /JC-16 Committee $71.00

JESD 8C.01 **INTERFACE STANDARD FOR NOMINAL 3.0 V/3.3 V SUPPLY DIGITAL INTEGRATED CIRCUITS:** This standard (a replacement of JEDEC Standards No. 8, 8-1, 8-1-A, and 8-A) defines dc interface parameters for a family of digital circuits operating from a power supply of nominal 3.0 V/3.3. V and driving/driven by parts of the same family. The specifications in this standard represent a minimum set of 'base line' set of interface specifications for LVTTL-compatible and LVCMOS-compatible circuits.

September 2007 June 2004 /JC-16 Committee $45.00

JESD 9-A **METAL PACKAGE SPECIFICATION FOR MICROELECTRONIC PACKAGES AND COVERS:** This standard establishes the general requirements and quality assurance provisions that can be specified and met in procuring microelectronics packages and covers, manufactured from matched seal with and without high thermal conductivity base materials, intended for use in fabricating hybrid microelectronics circuits. This document details those minimum requirements necessary for metal packages' use exclusively.

April 1987; Under Revision /JC-13.5 Subcommittee $71.00

JESD 10 **LOW FREQUENCY POWER TRANSISTORS:** This standard consists of a listing of letter symbols, terms, and definitions that are used in power transistors. It also includes information on JEDEC registration procedures, verification tests, and thermal characteristics.

January 1976; Reaffirmed September 1981, October 2002 April 1999 /JC-25 Committee $147.00

JESD 11 **CHIP CARRIER PINOUTS STANDARDIZED FOR CMOS 4000, HC AND HCT SERIES OF LOGIC CIRCUITS:** This standard indicates the procedures used to convert existing DIP and flat packages for digital parts (SSI & MSI) to chip carrier packages.

December 1984 / Committee!33JC402 $41.00

JESD 12 **SEMICUSTOM INTEGRATED CIRCUITS (FORMERLY PUBLISHED AS STANDARD FOR GATE ARRAY BENCHMARK SET):** The purpose of these benchmarks is to provide a common set of high level functions which serve as vehicles for comparing the performance of gate arrays implemented in any technology using any internal

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structure. These benchmarks effectively provide an unbiased measure of gate array vendors' ability to implement a desired complex function on a particular gate array at a known level of performance.

June 1985 / Committee!33JC44 $43.00

JESD 12-1B **ADDENDUM No. 1 to JESD12 - TERMS AND DEFINITIONS FOR GATE ARRAYS AND CELL-BASED INTEGRATED CIRCUITS:** The purpose of this standard is to promote the uniform use of abbreviations, terms, and definitions throughout the semiconductor industry. It is a useful guide for users, manufactures, educators, technical writers, and others interested in the characterization, nomenclature, and classification of semicustom integrated circuits.

August 1993 / Committee!33JC44 $48.00

JESD 12-2 **ADDENDUM No. 2 to JESD12 - STANDARD FOR CELL-BASED INTEGRATED CIRCUIT BENCHMARK SET:** The purpose of these benchmarks is to provide a common set of high level functions that serve as vehicles for comparing the performance of cell-based ICs implemented in any technology using any internal structure. JESD12-2 extends the gate array benchmark set (JESD12) to cell-based ICs.

February 1986 / Committee!33JC44 $61.00

JESD 12-3 **ADDENDUM No. 3 to JESD12 - CMOS GATE ARRAY MACROCELL STANDARD:** This standard defines a minimum set of macro cell standards for CMOS gate arrays. A total of 41 macro cell types are addressed, all of which are commonly used by gate array designers to implement Application Specific Integrated Circuits.

June 1986 / Committee!33JC44 $47.00

JESD 12-4 **ADDENDUM No. 4 to JESD12 - METHOD OF SPECIFICATION OF PERFORMANCE PARAMETERS FOR CMOS SEMICUSTOM INTEGRATED CIRCUITS:** This standard defines how to specify various performance parameters of semicustom ICs, including cell and interconnect propagation delays, input/output levels and capacitance, and power dissipation.

April 1987 / Committee!33JC44 $48.00

JESD 12-5 **ADDENDUM No. 5 to JESD12 - DESIGN FOR TESTABILITY GUIDELINES:** This standard is intended to provide circuit designers with the information needed to develop complex integrated circuits that can be reliably and economically tested without compromising flexibility.

August 1988 / Committee!33JC44 $109.00

JESD 12-6 **ADDENDUM No. 6 to JESD12 - INTERFACE STANDARD FOR SEMICUSTOM INTEGRATED CIRCUITS:** This standard defines logic

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interface levels for CMOS, TTL, ECL, and BiCC inputs and outputs. This standard is intended to provide an industry-wide set of specifications, for Application Specific Integrated Circuit (ASIC) signal inputs and outputs, both necessary and sufficient to define a circuits electrical interfacing with the external environment. JESD12-6 is intended to provide the ASIC manufacturer and user with a common set of signal interface levels. The standard defines interface levels for 5 volt operation.

March 1991 / Committee!33JC44 $43.00

JESD 13-B

STANDARD SPECIFICATION FOR DESCRIPTION OF B SERIES CMOS DEVICES: This standard provides for uniformity, multiplicity of sources, elimination of confusion, and ease of device specifications and system design by users. It gives electrical levels and timing diagrams for B Series CMOS devices.

May 1980 / Committee!33JC402 $63.00

JESD 14

SEMICONDUCTOR POWER CONTROL MODULES: Semiconductor Power Control Modules (SPCM) are modules consisting of thyristors or transistors, or both, as the primary controlling elements. Methods of manufacture of semiconductor power control modules include the assembling of individual components and the use of semiconductor hybrids or monolithic processing technologies, or both.

November 1986; Reaffirmed June 1992, April 1999, April 2002 April 2002 /JC-22.2 Subcommittee $47.00

JESD 16-A

ASSESSMENT OF AVERAGE OUTGOING QUALITY LEVELS IN PARTS PER MILLION (PPM): This standard was revised to clarify assumptions necessary to estimate AOQ, revise the minimum sample size algorithm, address small sample size concerns, and provide methods for combining groups for AOQ estimation. Derivation of any new methods for combing groups for AOQ estimation. Derivation of any new methods introduced into this document have been provided in annexes. A statistical method is based on confidence interval statistics. A procedure was established for reporting AOQ when the minimum sample size criterion is not met.

April 1995 /JC-13 Committee $61.00

JESD 17

LATCH-UP IN CMOS INTEGRATED CIRCUITS - SUPERSEDED BY JESD78, February 1999

August 1988; Rescinded February 1999 February 1999 / Committee!33JC402

JESD 18-A

STANDARD FOR DESCRIPTION OF FAST CMOS TTL COMPATIBLE LOGIC: The purpose of this standard is to provide for uniformity, multiplicity of sources, elimination of confusion, and ease of device specification and design by users. The standard covers

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specifications for description of '54/74FCTXXXX' series fast CMOS TTL compatible devices.

January 1993 / Committee!33JC402 $63.00

JESD 19 **GENERAL STANDARD FOR STATISTICAL PROCESS CONTROL (SPC) - SUPERSEDED by EIA-557-A**

July 1988; Rescinded July 1995 /JC-13 Committee

JESD 20 **STANDARD FOR DESCRIPTION OF 54/74ACXXXXX AND 54/74ACTXXXXX ADVANCED HIGH-SPEED CMOS DEVICES:** This standard describes electrical parameters for this class of CMOS devices.

September 1990 / Committee!33JC402 $147.00

JESD 21-C **CONFIGURATIONS FOR SOLID STATE MEMORIES:** This revision of JESD21 is substantially different from previous issues because it reflects advancement in semiconductor technology and computer design needs. A new class of memory devices, the multiport DRAM (MPDRAM) C also know as 'Video Ram' because of the most common application for the devices C is represented. A new family of SRAMs which addresses the increasing need for high speed is introduced. Additional families of devices in the SOJ and Zip packages are included. The material in this revision is organized primarily by function (ROM, EPROM, SRAM, DRAM, etc.) rather than by technology and word length. Pinouts for SIMM and DIMM are included along with presence detect schemes. A current set of terms has also been included. JESD21-C is a compilation of all memory device standards that have been developed by the JC-42 Committee and approved by the JEDEC BoD from September 1989 to present. This latest issue has changed to a loose-leaf format and comes in a three-ring binder so that new drawings can be added without requiring a new publication. Time of publication of the material is identified by release number, i.e., if marked Release 8, this item was approved and released in 1998, if marked Release 13, this item was approved and released in 2003.

May 2003; Under Revision Sections in this document may be under revision at any time. /JC-42 Committee $150.00

JESD 21-C AUS **ANNUAL UPDATING SERVICE:** The JEDEC Office has generated a mailing list for those who wish to subscribe to updates of this publication. A payment is required for subscription to this updating service.

January 2004 /JC-42 Committee $50.00

JESD 22-A100-B **CYCLED TEMPERATURE HUMIDITY BIAS LIFE TEST:** The Cycled Temperature-humidity-bias Life Test is performed for the purpose of evaluating the reliability of nonhermetic packaged solid state devices in humid environments. It employs conditions of

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temperature cycling, humidity, and bias that accelerate the penetration of moisture through the external protective material (encapsulant or seal) or along the interface between the external protective material and the metallic conductors that pass through it. The Cycled Temperature-Humidity-Bias Life Test is typically performed on cavity packages (e.g., MQUADs, lidded ceramic pin grid arrays, etc.) as an alternative to JESD22-A101 or JESD22-A110.

April 2000 /JC-14.1 Subcommittee $40.00

JESD 22-A101-B

STEADY-STATE TEMPERATURE HUMIDITY BIAS LIFE TEST: This standard establishes a defined method and conditions for performing a temperature humidity life test with bias applied. The test is used to evaluate the reliability of non-hermetic packaged solid state devices in humid environments. It employs high temperature and humidity conditions to accelerate the penetration of moisture through external protective material or along interfaces between the external protective coating and conductors or other features which pass through it. This revision enhances the ability to perform this test on a device which cannot be biased to achieve very low power dissipation.

April 1997 /JC-14.1 Subcommittee $40.00

JESD 22-A102-C

ACCELERATED MOISTURE RESISTANCE - UNBIASED AUTOCLAVE: This test allows the user to evaluate the moisture resistance of nonhermetic packaged solid state devices. The Unbiased Autoclave Test is performed to evaluate the moisture resistance integrity of non-hermetic packaged solid state devices using moisture condensing or moisture saturated steam environments. It is a highly accelerated test which employs conditions of pressure, humidity and temperature under condensing conditions to accelerate moisture penetration through the external protective material (encapsulant or seal) or along the interface between the external protective material and the metallic conductors passing through it. This test is used to identify failure mechanisms internal to the package and is destructive.

December 2000 /JC-14.1 Subcommittee $38.00

JESD 22-A103C

HIGH TEMPERATURE STORAGE LIFE: The test is applicable for evaluation, screening, monitoring, and/or qualification of all solid state devices. High Temperature storage test is typically used to determine the effect of time and temperature, understorage conditions, for thermally activated failure mechanisms of solid state electronic devices, includingnonvolatile memory devices (data retention failure mechanisms). During the test elevated temperatures(accelerated test conditions) are used without electrical stress applied. This test may be destructive,depending on Time, Temperature and Packaging (if any).

November 2004 June 2004 /JC-14.1 Subcommittee $40.00

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JESD 22-A104C	**TEMPERATURE CYCLING:** This standard provides a method for determining solid state devices capability to withstand extreme temperature cycling. Changes in this revision include requirements that the worst-case load temperature must reach the specific extremes rather than just requiring that the chamber ambient temperature reach the extremes. This ensures that the test specimens will reach the specified temperature extremes regardless of chamber loading. Definitions are provided for Load, Monitoring Sensor, Worst-Case Load Temperature, and Working Zone. The transfer time has been tightened from 5 minutes to 1 minute. Five new test conditions have been added as well as a caution on test conditions which exceed the glass transition temperature of plastic package solid devices. May 2005 January 2005 /JC-14.1 Subcommittee	$45.00
JESD 22-A105C	**POWER AND TEMPERATURE CYCLING:** The power and temperature cycling test is performed to determine the ability of a device to withstand alternate exposures at high and low temperature extremes and simultaneously the operating biases are periodically applied and removed. It is intended to simulate worst case conditions encountered in application environments. The power and temperature cycling test is considered destructive and is only intended for device qualification. This test method applies to semiconductor devices that are subjected to temperature excursions and required to power on and off during all temperatures. January 2004 June 2003 /JC-14.1 Subcommittee	$40.00
JESD 22-A106B	**THERMAL SHOCK:** This test is conducted to determine the resistance of a part to sudden exposure to extreme changes in temperature and to the effect of alternate exposures to these extremes. June 2004 January 2003 /JC-14.1 Subcommittee	$40.00
JESD 22-A107B	**SALT ATMOSPHERE:** This salt Atmosphere test is conducted to determine the resistance of solid state devices to corrosion. It is an accelerated test that simulates the effects of severe seacoast atmosphere on all exposed surfaces. The salt atmosphere test is considered destructive. It is intended for lot acceptance, process monitor, and qualification testing. January 2004 January 2003 /JC-14.1 Subcommittee	$38.00
JESD 22-A108C	**TEMPERATURE, BIAS, AND OPERATING LIFE:** A revised method for determining the effects of bias conditions and temperature, over time, on solid state devices is now available. Revision B of A108 includes low temperature operating life (LTOL) and high temperature gate bias (HTGB) stress conditions, revised cool down requirements for high temperature stress, and a procedure to follow if parts are not tested within the allowed time window.	

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	June 2005 March 2004 /JC-14.1 Subcommittee	$43.00
JESD 22-A109-A	**HERMETICITY:** This revised test method establishes a standard procedure for determining the effectiveness of the seal of hermetically sealed solid state devices. The objective of this revision was to modify the test parameters to reflect current practice and to eliminate the specification of fluorocarbons, banned from use due to environmental concerns. July 2001 /JC-14.1 Subcommittee	$43.00
JESD 22-A110-B	**HIGHLY ACCELERATED TEMPERATURE AND HUMIDITY STRESS TEST (HAST)** The purpose of this new test method is to evaluate the reliability of nonhermetic packaged solid state devices in humid environments. It employs severe conditions of temperature, humidity, and bias that accelerate the penetration of moisture through the external protective material (encapsulant or seal) or along the interface between the external protective material and the metallic conductors which pass through it. February 1999 /JC-14.1 Subcommittee	$40.00
JESD 22-A111	**EVALUATION PROCEDURE FOR DETERMINING CAPABILITY TO BOTTOM SIDE BOARD ATTACH BY FULL BODY SOLDER IMMERSION OF SMALL SURFACE MOUNT SOLID STATE DEVICES:** The purpose of this test method is to identify the potential wave solder classification level of small plastic Surface Mount Devices (SMDs) that are sensitive to moisture-induced stress so that they can be properly packaged, stored, and handled to avoid subsequent mechanical damage during the assembly wave solder attachment and/or repair operations. This test method also provides a reliability preconditioning sequence for small SMDs that are wave soldered using full body immersion. This test method, may be used by users to determine what classification level should be used for initial board level reliability qualification. May 2004 June 2000 /JC-14.1 Subcommittee	$47.00
JESD 22-A112-A	**MOISTURE-INDUCED STRESS SENSITIVITY FOR PLASTIC SURFACE MOUNT DEVICES - SUPERSEDED BY J-STD-020A, April 1999.** J-STD-020 is now on revision D. November 1995; Rescinded May 2000 May 2000 /JC-14.1 Subcommittee	
JESD 22-A113E	**PRECONDITIONING OF PLASTIC SURFACE MOUNT DEVICES PRIOR TO RELIABILITY TESTING:** This Test Method establishes an industry standard preconditioning flow for nonhermetic solid state SMDs (surface mount devices) that is representative of a typical industry multiple solder reflow operation. These SMDs should be subjected to the appropriate preconditioning sequence of this document by the semiconductor manufacturer prior to being submitted to specific in-house reliability testing (qualification and	

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	reliability monitoring) to evaluate long term reliability (which might be impacted by solder reflow). March 2006 October 2005 /JC-14.1 Subcommittee	$47.00
JESD 22-A114E	**ELECTROSTATIC DISCHARGE (ESD) SENSITIVITY TESTING HUMAN BODY MODEL (HBM):** This test method establishes a standard procedure for testing and classifying microcircuits according to their susceptibility to damage or degradation by exposure to a defined electrostatic Human Body Model (HBM) discharge (ESD). The objective is to provide reliable, repeatable HBM ESD test results so that accurate classifications can be performed. January 2007 October 2005 /JC-14.1 Subcommittee	$49.00
JESD 22-A115-A	**ELECTROSTATIC DISCHARGE (ESD) SENSITIVITY TESTING MACHINE MODEL (MM):** This method establishes a standard procedure for testing and classifying microcircuits according to their susceptibility to damage or degradation by exposure to a defined Machine Model (MM) electrostatic discharge (ESD). The objective is to provide reliable, repeatable MM ESD test results so that accurate classifications can be performed. October 1997 This is a valid test method, however it is not currently being used in the industry, the preferred industry test methods are JESD22A114 or JESD22C101. /JC-14.1 Subcommittee	$45.00
JESD 22-A117A	**ELECTRICALLY ERASABLE PROGRAMMABLE ROM (EEPROM) PROGRAM/ERASE ENDURANCE AND DATA RETENTION TEST:** This method establishes a standard procedure for determining the data cycling endurance and data retention capability of non-volatile memory cells. It is intended as a qualification and monitor test procedure. This test is also applicable to FLASH EEPROM integrated circuits and Erasable Programmable Logic Devices (EPLD) with embedded EEPROM or FLASH memory. March 2006 June 2005 /JC-14.3 Subcommittee	$45.00
JESD 22-A118	**ACCELERATED MOISTURE RESISTANCE - UNBIASED HAST:** The Unbiased HAST is performed for the purpose of evaluating the reliability of non-hermetic packaged solid-state devices in humid environments. It is a highly accelerated test which employs temperature and humidity under non-condensing conditions to accelerate the penetration of moisture through the external protective material (encapsulant or seal) or along the interface between the external protective material and the metallic conductors which pass through it. Bias is not applied in this test to ensure the failure mechanisms potentially overshadowed by bias can be uncovered (e.g. galvanic corrosion). This test is used to identify failure mechanisms internal to the package and is destructive. December 2000 /JC-14.1 Subcommittee	$41.00

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JESD 22-A119	**LOW TEMPERATURE STORAGE LIFE** The test is applicable for evaluation, screening, monitoring, and/or qualification of all solid state devices. Low Temperature storage test is typically used to determine the effect of time and temperature, under storage conditions, for thermally activated failure mechanisms of solid state electronic devices, including nonvolatile memory devices (data retention failure mechanisms). During the test reduced temperatures (test conditions) are used without electrical stress applied. This test may be destructive, depending on Time, Temperature and Packaging (if any). November 2004 June 2004 /JC-14.1 Subcommittee	$40.00
JESD 22-A120	**TEST METHOD FOR THE MEASUREMENT OF MOISTURE DIFFUSIVITY AND WATER SOLUBILITY IN ORGANIC MATERIALS USED IN INTEGRATED CIRCUITS:** This specification details the procedures for the measurement of characteristic bulk material properties of moisture diffusivity and water solubility in organic materials used in the packaging of IC components. These two material properties are important parameters for the effective reliability performance of plastic packaged ICs after exposure to moisture and subjected to high temperature solder reflow. June 2001 /JC-14.1 Subcommittee	$41.00
JESD 22-A121.01	**Measuring Whisker Growth on Tin and Tin Alloy Surface Finishes** The predominant terminal finishes on electronic components have been Sn-Pb alloys. As the industry moves toward Pb-free components and assembly processes, the predominant terminal finish materials will be pure Sn and alloys of Sn, including Sn-Bi and Sn-Ag. Pure Sn and Sn-based alloy electrodeposits and solder-dipped finishes may grow tin whiskers, which could electrically short across component terminals or break off the component and degrade the performance of electrical or mechanical parts. October 2005 October 2004 /JC-14 Committee	$59.00
JESD 22-B100B	**PHYSICAL DIMENSION:** The standard provides a method for determining whether the external physical dimensions of the device are in accordance with the applicable procurement document. This revision includes a change in details to be specified by the procurement document. June 2003; Reaffirmed June 2006 September 2002 /JC-14.1 Subcommittee	$38.00
JESD 22-B101A	**EXTERNAL VISUAL:** The purpose of this inspection is to verify that the materials, design, construction, markings, and workmanship of the device are in accordance with the applicable procurement document. External visual is a nondestructive test and applicable for all package types. The test is useful for qualification, process monitor, or lot acceptance.	

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	October 2004 January 2004 /JC-14.1 Subcommittee	$43.00
JESD 22-B102E	**SOLDERABILITY:** This test method provides optional conditions for preconditioning and soldering for the purpose of assessing the solderability of device package terminations. It provides procedures for dip & look solderability testing of through hole, axial and surface mount devices and a surface mount process simulation test for surface mount packages. The purpose of this test method is to provide a means of determining the solderability of device package terminations that are intended to be joined to another surface using lead (Pb) containing or Pb-free solder for the attachment. October 2007 January 2007 /JC-14.1 Subcommittee	$62.00
JESD 22-B103B	**VIBRATION, VARIABLE FREQUENCY:** The Vibration, Variable Frequency Test Method is intended to determine the ability of component(s) to withstand moderate to severe vibration as a result of motion produced by transportation or filed operation of electrical equipment. This is a destructive test that is intended forcomponent qualification. June 2002; Reaffirmed June 2006 /JC-14.1 Subcommittee	$43.00
JESD 22-B104C	**MECHANICAL SHOCK:** This test is intended to determine the suitability of component parts for use in electronic equipment that may be subjected to moderately severe shocks as a result of suddenly applied forces or abrupt changes in motion produced by rough handling, transportation, or field operation. Shock of this type may disturb operating characteristics, particularly if the shock pulses are repetitive. This is a destructive test intended for device qualification. It is normally applicable to cavity-type packages. November 2004 - Typo found on pg.1 in title, a new version dated December 2004 has been posted. if you downloaded between 11/10/04 & 12/10/04, please download againJanuary 2004 /JC-14.1 Subcommittee	$41.00
JESD 22-B105C	**LEAD INTEGRITY:** This test method provides various tests for determining the integrity lead/package interface and the lead itself when the lead(s) are bent due to faulty board assembly followed by rework of the part for reassembly. For hermetic packages it is rececommend that this test be followed by hermeticity tests in accordance with Test Method A109 to determine if there are any adverse effects from the stresses applied to the seals as well as to the leads. These tests, including each of its test conditions, is considered destructive and is only recommended for qualification testing. This test is applicable to all through-hole devices and surface-mount devices requiring lead forming by the user. May 2003; Reaffirmed June 2006 /JC-14.1 Subcommittee	$48.00
JESD 22-B106C	**RESISTANCE TO SOLDERING TEMPERATURE FOR THROUGH-HOLE MOUNTED DEVICES:** This method established a standard procedure	

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	for determining whether through-hole solid state devices can withstand the effects of the temperature to which they will be subject during soldering of their leads. This revision updates the references to currently military standards. February 2005 September 2004 /JC-14.1 Subcommittee	$40.00
JESD 22-B107C	**MARKING PERMANENCY:** This test method provides two tests for determining the marking permanency of ink marked integrated circuits. A new non-destructive tape test method is introduced to quickly determine marking integrity. The test method also specifies a resistance to solvents method based upon MIL Std 883 Method 2015. September 2004 October 2002 /JC-14.1 Subcommittee	$43.00
JESD 22-B108A	**COPLANARITY TEST FOR SURFACE-MOUNT SEMICONDUCTOR DEVICES:** The purpose of this test is to measure the deviation of the terminals (leads or solder balls) from coplanarity for surface-mount semiconductor devices. January 2003 /JC-14.1 Subcommittee	$41.00
JESD 22-B109	**FLIP CHIP TENSILE PULL:** The Flip Chip Tensile Pull Test Method is performed to determine the fracture mode and strength of the solder bump interconnection between the flip chip die and the substrate. It should be used to assess the consistency of the chip join process. This test method is a destructive test. June 2002 /JC-14.1 Subcommittee	$41.00
JESD 22-B110A	**SUBASSEMBLY MECHANICAL SHOCK:** The new test method JESD22-B110 provides guidance for in-situ testing of mechanical shock resistance of components as mounted in a subassembly. Using terms, procedures, and test levels in common with JESD22-B104B, this test method provides a range of test level options to improve test applicability and compatibility with fragility test procedures. Test procedures are detailed, including test card and fixture needs, test tolerances, test documentation, component preparation, and definition of terms. November 2004 January 2004 /JC-14.1 Subcommittee	$45.00
JESD 22-B111	**BOARD LEVEL DROP TEST METHOD OF COMPONENTS FOR HANDHELD ELECTRONIC PRODUCTS:** This Board Level Drop Test Method is intended to evaluate and compare drop performance of surface mount electronic components for handheld electronic product applications in an accelerated test environment, where excessive flexure of a circuit board causes product failure. The purpose is to standardize the test board and test methodology to provide a reproducible assessment of the drop test performance of surface mounted components while duplicating the failure modes normally observed during product level test.	

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	July 2003 /JC-14.1 Subcommittee	$48.00
JESD 22-B112	**High Temperature Package Warpage Measurement Methodology** The purpose of this test method is to measure the deviation from uniform flatness of an integrated circuit package body for the range of environmental conditions experienced during the surface-mount soldering operation.	
	May 2005 October 2004 /JC-14.1 Subcommittee	$49.00
JESD 22-B113	**BOARD LEVEL CYCLIC BEND TEST METHOD FOR INTERCONNECT RELIABILITY CHARACTERIZATION OF COMPONENTS FOR HANDHELD ELECTRONIC PRODUCTS** The Board Level Cyclic Bend Test Method is intended to evaluate and compare the performance of surface mount electronic components in an accelerated test environment for handheld electronic products applications. The purpose is to standardize the test methodology to provide a reproducible performance assessment of surface mounted components while duplicating the failure modes normally observed during product level test. This is not a component qualification test and is not meant to replace any product level test that may be needed to qualify a specific product and assembly.	
	March 2006 October 2005 /JC-14.1 Subcommittee	$49.00
JESD 22-B115	**SOLDER BALL PULL** This document describes a test method only; acceptance criteria and qualification requirements are not defined. This test method applies to solder ball pull force testing prior to end-use attachment. Solder balls are pulled individually using mechanical jaws; force and failure mode data are collected and analyzed. Other specialized solder ball pull methods using a heated thermode, gang pulling of multiple solder joints, etc., are outside the scope of this document. Both low and high speed testing are covered by this document.	
	May 2007 September 2006 /JC-14.1 Subcommittee	$49.00
JESD 22-B116	**WIRE BOND SHEAR TEST:** This test method establishes a standard procedure for determining the strength of an integrated circuit wire bond by shearing the wire from the surface it is bonded to and measuring the force required. This method serves as an alternative to pulling the wire vertically until the wire separates from one of it's two bonded surfaces. It also provides guidelines for determining an appropriate minimum shear force for gold balls on aluminum alloy bonding surfaces.	
	July 1998 /JC-14.1 Subcommittee	$45.00
JESD 22-B117A	**SOLDER BALL SHEAR:** The purpose of this test is conducted to assess the ability of solder balls to withstand mechanical shear forces that may be applied during device manufacturing, handling, test, shipment and end-use conditions. Solder ball shear is a destructive test.	

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	October 2006 January 2006 /JC-14.1 Subcommittee	$45.00
JESD 22-C100-A	**HIGH TEMPERATURE CONTINUITY - RESCINDED, November 1999** April 1990; Rescinded November 1999 /JC-14.1 Subcommittee	
JESD 22-C101C	**FIELD-INDUCED CHARGED-DEVICE MODEL TEST METHOD FOR ELECTROSTATIC DISCHARGE WITHSTAND THRESHOLDS OF MICROELECTRONIC COMPONENTS:** This new test method describes a uniform method for establishing charged-device model electrostatic discharge withstand thresholds. The charged-device-model simulates charging/discharging events that occur in production equipment and processes. Potential for CDM ESD events occurs whenever there is metal-to-metal contact in manufacturing. One of many examples is a device sliding down a shipping tube hitting a metal surface. Discharges to devices on unterminated circuit assemblies are also well-modeled by the CDM test. DM ESD events not only reduce assembly yields but can also produce device damage that goes undetected by factory test and later is the cause of a latent failure. December 2004 June 2004 /JC-14.1 Subcommittee	$47.00
JESD 23	**TEST METHODS AND CHARACTER DESIGNATION FOR LIQUID CRYSTAL DEVICES:** This standard specifies a collection of procedures for testing and character designation of liquid crystal devices. May 1982	$57.00
JESD 24	**POWER MOSFETS:** This standard contains a listing of terms and definitions and letter symbols; a description of established procedures that are followed in the assignment of semiconductor-industry-type designations to power transistors; electrical verification test; thermal characteristics; and a user's guide. July 1985 /JC-25 Committee	$71.00
JESD 24-1	**ADDENDUM No. 1 to JESD24 - METHOD FOR MEASUREMENT OF POWER DEVICE TURN-OFF SWITCHING LOSS:** Describes the method of a typical oscilloscope waveform and the basic test circuit employed in the measurement of turn off loss for bipolar, IGBT and MOSFET power semiconductors. This method can be used as a standard for evaluating power semiconductor turn-off switching loss capability and defines standard terminology that should be referenced within the electronic industry. October 1989; Reaffirmed April 1999, October 2002 /JC-25 Committee	$41.00
JESD 24-2	**ADDENDUM No. 2 to JESD24 - GATE CHARGE TEST METHOD:** This addendum establishes a method for measuring power device gate	

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charge. A gate charge test is performed by driving the device gate with a constant current and measuring the resulting gate voltage response. Constant gate current scales the gate voltage, a function of time, to a function of coulombs. The slope of the generated response reflects the active device capacitance as it varies during the switching transition . Gate charge measurements are useful for characterizing the large signal switching performance of power MOS and IGBT devices. Developed over a four year span by the JEDEC JC-25 Committee, the method defines a repeatable means of measuring the widely published Qgd charge values.

January 1991; Reaffirmed October 2002 April 1999 /JC-25 Committee — $41.00

JESD 24- 3 

ADDENDUM No. 3 to JESD24 - THERMAL IMPEDANCE MEASUREMENTS FOR VERTICAL POWER MOSFETS (DELTA SOURCE-DRAIN VOLTAGE METHOD): The purpose of this test method is to measure the thermal impedance of the MOSFET under the specified conditions of applied voltage, current and pulse duration. The temperature sensitivity if the forward voltage drop of the source-drain is used as the junction temperature indicator. This method is particularly suitable to enhancement mode, power MOSFETs having relatively long thermal response times. This test method may be used to measure the thermal response of junction to a heating pulse, to ensure proper die mountdown to its case, or the dc thermal resistance, by the proper choice of the pulse duration and magnitude if the heating pulse.

November 1990; Reaffirmed April 1999 /JC-25 Committee — $47.00

JESD 24- 4 

ADDENDUM No. 4 to JESD24 - THERMAL IMPEDANCE MEASUREMENTS FOR BIPOLAR TRANSISTORS (DELTA BASE-EMITTER VOLTAGE METHOD): The purpose of this test method is to measure the thermal impedance of the Bipolar Transistor under the specified conditions of applied voltage, current and pulse duration. The temperature sensitivity of the base-emitter voltage is used as the junction temperature indicator. This test method is used to measure the thermal response of the junction to a heating pulse. Specifically, the test may be used to measure dc thermal resistance, and to ensure proper die mountdown to its case. This is accomplished through the appropriate choice of pulse duration and heating power magnitude.

November 1990; Reaffirmed October 2002 April 1999 /JC-25 Committee — $47.00

JESD 24- 5 

ADDENDUM No. 5 to JESD24 - SINGLE PULSE UNCLAMPED INDUCTIVE SWITCHING (UIS) AVALANCHE TEST METHOD: This method describes a means for testing the ability of a power switching device to withstand avalanche breakdown.

August 1990; Reaffirmed october 2002 April 1999 /JC-25 Committee — $38.00

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JESD 24- 6	**ADDENDUM No. 6 to JESD24 - THERMAL IMPEDANCE MEASUREMENTS FOR INSULATED GATE BIPOLAR TRANSISTORS:** This standard describes in detail the method for thermal measurements of Insulated Gate Bipolar Transistors (IGBTs) and is suitable for use both in manufacturing and application of the devices. The method covers both thermal transient and thermal equilibrium measurements for manufacturing process control and device characterization purposes. Properly implemented, JESD24-6 provides a basis for obtaining realistic thermal parametric values that will benefit supplier's internal effectiveness and will be useful to the design and manufacturer of reliable IGBT circuits. October 1991; Reaffirmed October 2002 April 1999 /JC-25 Committee	$47.00
JESD 24- 7	**ADDENDUM No. 7 to JESD24 - COMMUTATING DIODE SAFE OPERATING AREA TEST PROCEDURE FOR MEASURING dv/dt DURING REVERSE RECOVERY OF POWER TRANSISTORS:** Defines methods for verifying the diode recovery stress capability of power transistors. August 1982; Reaffirmed October 2002 April 1999 /JC-25 Committee	$40.00
JESD 24- 8	**ADDENDUM No. 8 to JESD24 - METHOD FOR REPETITIVE INDUCTIVE LOAD AVALANCHE SWITCHING:** Determines the repetitive inductive avalanche switching capability of power switching transistors. August 1992; Reaffirmed October 2002 April 1999 /JC-25 Committee	$40.00
JESD 24- 9	**ADDENDUM No. 9 to JESD24 - SHORT CIRCUIT WITHSTAND TIME TEST METHOD:** Test method to determine how long a device can survive a short circuit condition with a given drive level. August 1992; Reaffirmed October 2002 April 1999 /JC-25 Committee	$40.00
JESD 24-10	**ADDENDUM No. 10 to JESD24 - TEST METHOD FOR MEASUREMENT OF REVERSE RECOVERY TIME trr FOR POWER MOSFET DRAIN-SOURCE DIODES:** Test method to measure the reverse recovery characteristics of the drain source diode of a power MOSFET. August 1994; Reaffirmed October 2002 April 1999 /JC-25 Committee	$41.00
JESD 24-11	**ADDENDUM No. 11 to JESD24 - POWER MOSFET EQUIVALENT SERIES GATE RESISTANCE TEST METHOD:** Test method to measure the equivalent resistance of the gate to source of a power MOSFET. August 1996; Reaffirmed March 2001, October 2002 March 2001 /JC-25 Committee	$38.00
JESD 24-12	**Thermal Impedance Measurement for Insulated Gate Bipolar**	

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Transistors - (Delta VCE(on) Method) The purpose of this test method is to measure the thermal impedance of the IGBT (Insulated Gate Bipolar Transistor) under the specified conditions of applied voltage, current and pulse duration. The temperature sensitivity of the collector-emitter on voltage, VCE(on), is used as the junction temperature indicator. This is an alternative method to JEDEC Standard No. 24-6.

June 2004 September 2002 /JC-25 Committee $45.00

JESD 25



MEASUREMENT OF SMALL-SIGNAL TRANSISTOR SCATTERING PARAMETERS: This standard provides a test method and definition for small-signal conditions at microwave frequencies.

November 1972; Reaffirmed September 1981, April 2000, October 2002 /JC-25 Committee $57.00

JESD 26-A



GENERAL SPECIFICATION FOR PLASTIC ENCAPSULATED MICROCIRCUITS FOR USE IN RUGGED APPLICATIONS - RESCINDED, July 2001

April 1990; Rescinded July 2001 /JC-13.2 Subcommittee

JESD 27



CERAMIC PACKAGE SPECIFICATION FOR MICROELECTRONIC PACKAGES: The intent of this standard is to be a guide in the manufacture and procurement of ceramic packages, especially for the hybrid industry. Manufacturers or ceramic packages and procuring activities for these packages will now be able to use this document as the means for agreement in the imposition of minimum requirements in qualification, screening, and quality conformance.

August 1993; Under Revision , will be merged with JESD9-A /JC-13.5 Subcommittee $67.00

JESD 28-1



N-CHANNEL MOSFET HOT CARRIER DATA ANALYSIS: This addendum provides data analysis examples useful in analyzing MOSFET n-channel hot-carrier-induced degradation data. This addendum to JESD28 (Hot carrier n-channel testing standard) suggests hot-carrier data analysis techniques.

September 2001 /JC-14.2 Subcommittee $43.00

JESD 28-A



A PROCEDURE FOR MEASURING N-CHANNEL MOSFET HOT-CARRIER-INDUCED DEGRADATION UNDER DC STRESS: This document describes an accelerated test for measuring the hot-carrier-induced degradation of a single n-channel MOSFET using dc bias. The purpose of this document is to specify a minimum set of measurements so that valid comparisons can be made between different technologies, IC processes, and process variations in a simple, consistent and controlled way. The measurements specified should be viewed as a starting point in the characterization and benchmarking of the transistor manufacturing process.

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December 2001 /JC-14.2 Subcommittee $47.00

JESD 29-A **FAILURE-MECHANISM-DRIVEN RELIABILITY MONITORING - SUPERSEDED BY EIA/ANSI-659, July 1996.**

July 1996; Superseded July 1996 /JC-14.3 Subcommittee

JESD 30D **DESCRIPTIVE DESIGNATION SYSTEM FOR SEMICONDUCTOR-DEVICE PACKAGES:** This standard describes a systematic method for generating universal descriptive designators for semiconductor-device packages. The descriptive designator is intended to provide a useful communication tool but has no implied control for assuring package interchangeability.

July 2006 July 2004 /JC-11 Committee $55.00

JESD 31C **GENERAL REQUIREMENTS FOR DISTRIBUTORS OF COMMERCIAL AND MILITARY SEMICONDUCTOR DEVICES:** This publication identifies the general requirements for Distributors that supply Commercial and Military products. This document identifies the general requirements for Distributors that supply Commercial and Military products. Now updated to provide clarification, these requirements apply to all discrete semiconductors, integrated circuits and hybrids, whether packaged or in wafer/die form, manufactured by all component Manufacturers. This revision was incorporated to better define the requirements for the handling of moisture-sensitive devices in distribution. The addition of IPC/JEDEC J-STD-020 and IPC/JEDEC J-STD-033 ensure consistent requirements throughout the distribution channel.

September 2003 January 2003 /JC-14.4 Subcommittee $52.00

JESD 32 **STANDARD FOR CHAIN DESCRIPTION FILE:** This document provides a standard for describing an ISP device chain, opening up the possibility for third-party companies to provide value-added ISP software. The purpose of the Chain Description File is to describe the configuration of a programming chain made up of devices that can be connected in some serial fashion. No assumptions are made about how data is used by the device, nor about the nature or configuration of the control signals that affect programming. It will support devices configured using electrically-erasable(EE), Flash, SRAM, or any other reconfigurable cell. For devices programmed via an IEEE programmable devices in the same chain.

June 1996 / Committee!33JC421 $47.00

JESD 33-B **STANDARD METHOD FOR MEASURING AND USING THE TEMPERATURE COEFFICIENT OF RESISTANCE TO DETERMINE THE TEMPERATURE OF A METALLIZATION LINE:** This newly revised test method provides a procedure for measuring the temperature coefficient of resistance, TCR(T), of thin-film metallizations used in microelectronic circuits and devices. Procedures are also provided to use the TCR(T) to determine the temperature of a metallization

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	line under Joule-heating conditions and to determine the ambient temperature where the metallization line is used as a temperature sensor. Originally, the method was intended only for aluminum-based metallizations and for other metallizations that satisfy the linear dependence and stability stipulations of the method. The method has been revised to make it explicitly applicable to copper-based metallizations, as well, and at temperatures beyond where the resistivity of copper is no longer linearly dependent on temperature (beyond approximately 200 °C). Using the TCR(T) measured for copper in the linear-dependent region, a factor is used to correct the calculated temperature at these higher temperatures. February 2004 April 2003 /JC-14.2 Subcommittee	$61.00
JESD 34	**FAILURE-MECHANISM-DRIVEN RELIABILITY QUALIFICATION OF SILICON DEVICES:** This document applies to the reliability qualification of new or changed silicon devices, and their materials or manufacturing processes. Does not address qualification of product quality or functionality. Provides an alternative to traditional stress-driven qualification. March 1993; Rescinded November 2004 June 2004 /JC-14.2 Subcommittee	$43.00
JESD 35-1	**ADDENDUM No. 1 to JESD35 - GENERAL GUIDELINES FOR DESIGNING TEST STRUCTURES FOR THE WAFER-LEVEL TESTING OF THIN DIELECTRICS:** This addendum expands the usefulness of the Standard 35 (JESD35) by detailing the various sources of measurement error that could effect the test results obtained by the ramped tests described in JESD35. Each source of error is described and its implications on test structure design is noted. This addendum can be used as a guide when designing test structures for the qualification and characterization of thin oxide reliability, specifically, by implementing accelerated voltage or current ramp tests. September 1995 /JC-14.2 Subcommittee	$52.00
JESD 35-2	**ADDENDUM No. 2 to JESD35 - TEST CRITERIA FOR THE WAFER-LEVEL TESTING OF THIN DIELECTRICS:** This addendum includes test criteria to supplement JESD35. JESD35 describes procedures developed for estimating the overall integrity of thin oxides in the MOS Integrated Circuit manufacturing industry. Two test procedures are included in JESD35: a Voltage-Ramp (V-Ramp) and a Current-Ramp (J-Ramp). As JESD35 became implemented into production facilities on a variety of test structures and oxide attributes, a need arose to clarify end point determination and point out some of the obstacles that could be overcome by careful characterization of the equipment and test structures. February 1996 /JC-14.2 Subcommittee	$43.00

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JESD 35-A **PROCEDURE FOR WAFER-LEVEL-TESTING OF THIN DIELECTRICS:**
The revised JESD35 is intended for use in the MOS Integrated Circuit manufacturing industry. It describes procedures developed for estimating the overall integrity and reliability of thin gate oxides. Three basic test procedures are described, the Voltage-Ramp (V-Ramp), the Current-Ramp (J-Ramp) and the new Constant Current (Bounded J-Ramp) test. Each test is designed for simplicity, speed and ease of use. The standard has been updated to include breakdown criteria that are more robust in detecting breakdown in thinner gate oxides that may not experience hard thermal breakdown.

April 2001 /JC-14.2 Subcommittee $67.00

JESD 36 **STANDARD DESCRIPTION OF LOW-VOLTAGE TTL-COMPATIBLE, 5 V TOLERANT CMOS LOGIC DEVICES:** This standard outlines the standard dc specifications, test conditions, and test loading for logic products that are designed to tolerate input and output voltages which exceed the device's power supply. More specifically this standardizes 5 V - tolerant logic prducts that run from 'low voltage' (2.7 V to 3.6 V) power supplies. Products that meet this standard can be used to effectively interface between LVCMOS/LVTTL and 5 V TTL buses, bridging the gap between low-voltage and 5 V TTL busses.

June 1996 /JC-40 Committee $45.00

JESD 37 **STANDARD LOGNORMAL ANALYSIS OF UNCENSORED DATA, AND OF SINGLY RIGHT -CENSORED DATA UTILIZING THE PERSSON AND ROOTZEN METHOD:** This standard details techniques for estimating the values of a two parameter lognormal distribution from complete lifetime data (all samples in an experiment have failed) or singly right-censored lifetime data (the experiment have failed) or singly right-censored lifetime data gathered from rapid stress test; however, not all types of failure data can be analyzed with these techniques.

October 1992 /JC-14.2 Subcommittee $59.00

JESD 38 **STANDARD FOR FAILURE ANALYSIS REPORT FORMAT:** This standard is to promote unification of content and format of semiconductor device failure-analysis reports so that reports from diverse laboratories may be easily read, compared, and understood by customers. Additional objectives are to ensure that reports can be easily ready by users, satisfactorily reproduced on copying machines, adequately transmitted by telefax, and conveniently stored in standard filing cabinets.

December 1995 /JC-14.6 Subcommittee $43.00

JESD 39-A **QUALITY SYSTEM ASSESSMENT - SUPERSEDED BY ANSI/EIA-670, June 1997.**

June 1997; Superseded /JC-14.4 Subcommittee

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JESD 40 **PROCUREMENT QUALITY OF SOLID STATE COMPONENTS BY GOVERNMENT CONTRACTORS - SUPERSEDED BY EIA-623, July 1994**

July 1994; Superseded /JC-13 Committee

JESD 41 **REVERSE RECOVERY CHARACTERISTICS OF SILICON DIODES: Rescinded June 2002.**

May 1995; Rescinded June 2002 /JC-22.1 Subcommittee

JESD 42 **REQUIREMENTS FOR HANDLING ELECTROSTATIC-DISCHARGE-SENSITIVE (ESDS) DEVICES - SUPERSEDED BY EIA-625, November 1994.**

March 1994; Superseded /JC-13 Committee

JESD 43 **COMPONENT PROBLEM ANALYSIS AND CORRECTIVE ACTION REQUIREMENTS - SUPERSEDED BY EIA-671, November 1996.**

November 1996; Superseded /JC-14.4 Subcommittee

JESD 45 **MEASUREMENT METHOD FOR THERMAL RESISTANCE OF BRIDGE RECTIFIER ASSEMBLIES: RESCINDED, June 2002. Replaced by JESD282-B.**

December 1994; Rescinded June 2002 June 2002 /JC-22.2 Subcommittee

JESD 46C **CUSTOMER NOTIFICATION OF PRODUCT/PROCESS CHANGES BY SEMICONDUCTOR SUPPLIERS:** This standard establishes procedures to notify customers of semiconductor product and process changes. Requirements include: documentation; procedures for classification, notification and customer response; content; and records.Documentation of a suppliers change notification system should set clear and understandable expectations for both the originators of the change and their end customers.

October 2006 January 2006 /JC-14.4 Subcommittee $41.00

JESD 47E **STRESS-TEST-DRIVEN QUALIFICATION OF INTEGRATED CIRCUITS:** This standard describes a baseline set of acceptance tests for use in qualifying electronic components as new products, a product family, or as products in a process which is being changed.

January 2007 January 2006 /JC-14.3 Subcommittee $52.00

JESD 48B **PRODUCT DISCONTINUANCE:** This standard establishes the requirements for timely customer notification of planned productdiscontinuance, which will assist customers in managing end-of-life supply, or to transition on-goingrequirements to alternate products.

May 2005 January 2005 /JC-14.4 Subcommittee $40.00

JESD 49A **PROCUREMENT STANDARD FOR KNOWN GOOD DIE (KGD):** This standard was created to facilitate the procurement and use of high

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reliability semiconductor microcircuits or discrete devices provided in bare die form, commonly known as Known Good Die (KGD).

September 2005 January 2005 /JC-13 Committee $48.00

JESD 50A **SPECIAL REQUIREMENTS FOR MAVERICK PRODUCT ELIMINATION:** This standard applies to the identification and control of Maverick Product that can occur during fabrication, assembly, packaging, or test of any electronic component. It can be implemented for an entire product line or to segregate product that has a higher probability of adversely impacting quality or reliability.

December 2004 June 2004 /JC-14.3 Subcommittee $40.00

JESD 51 **METHODOLOGY FOR THE THERMAL MEASUREMENT OF COMPONENT PACKAGES (SINGLE SEMICONDUCTOR DEVICE)** This standard and its subsequent addendum's, provides a standard for thermal measurement that, if followed fully, will provide correct and meaningful data that will allow for determination of junction temperature for specific conditions. The data can be used for package design evaluation, device characterization and reliability predictions.

December 1995 /JC-15.1 Subcommittee $40.00

JESD 51- 1 **INTEGRATED CIRCUIT THERMAL MEASUREMENT METHOD - ELECTRICAL TEST METHOD (SINGLE SEMICONDUCTOR DEVICE):** The purpose of this test method is to define a standard Electrical Test Method (ETM) that can be used to determine the thermal characteristics of single integrated circuit devices housed in some form of electrical package. This method will provide a basis for comparison of different devices housed in the same electronic package or similar devices housed in different electronic packages.

December 1995 /JC-15.1 Subcommittee $61.00

JESD 51- 2 **INTEGRATED CIRCUITS THERMAL TEST METHOD ENVIRONMENTAL CONDITIONS - NATURAL CONVECTION (STILL AIR):** This document outlines the environmental conditions necessary to ensure accuracy and repeatability for a standard junction-to-ambient thermal resistance measurement in natural convection.

December 1995 /JC-15.1 Subcommittee $47.00

JESD 51- 3 **LOW EFFECTIVE THERMAL CONDUCTIVITY TEST BOARD FOR LEADED SURFACE MOUNT PACKAGES:** This standard describes design requirements for a single layer, leaded surface mount integrated circuit package thermal test board. The standard describes board material and geometry requirements, minimum trace lenghts, trace thickness, and routing considerations. Application includes still air and moving air thermal tests.

August 1996 /JC-15.1 Subcommittee $41.00

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JESD 51- 4 **THERMAL TEST CHIP GUIDELINE (WIRE BOND TYPE CHIP):** This guideline describes design requirements for wire bond type semiconductor chips to be used for thermal resistance listing of IC packages. This document provides specific guidelines for chip design but allows flexibility in the materials and layout requirements.

February 1997 /JC-15.1 Subcommittee $45.00

JESD 51- 5 **EXTENSION OF THERMAL TEST BOARD STANDARDS FOR PACKAGES WITH DIRECT THERMAL ATTACHMENT MECHANISMS:** This extension of the thermal standards provides a standard fixture for direct attach type packages such as deep-downset of thermally tabbed packages. This specification provides additional design detail for use in developing thermal test boards with application to these package types. This document is in addition to and not replacement for the design specifications in other standards.

February 1999 /JC-15.1 Subcommittee $38.00

JESD 51- 6 **INTEGRATED CIRCUIT THERMAL TEST METHOD ENVIRONMENTAL CONDITIONS - FORCED CONVECTION (MOVING AIR):** This standard specifies the environmental conditions for determining thermal performance of an integrated circuit device in a forced convection environment when mounted on a standard thermal test board.

March 1999 /JC-15.1 Subcommittee $38.00

JESD 51- 7 **HIGH EFFECTIVE THERMAL CONDUCTIVITY TEST BOARD FOR LEADED SURFACE MOUNT PACKAGES:** This fixturing further defines the environment for thermal test of packaged microelectronic devices. Its function is to provide an alternate mounting surface for the analysis of heat flow in electronic components. The objective of the standard is to provide a high effective thermal conductivity mounting surface that can be compared equally against standard tests done in different laboratories with typical variations of less than or equal to 10%.

February 1999 /JC-15.1 Subcommittee $41.00

JESD 51- 8 **INTEGRATED CIRCUIT THERMAL TEST METHOD ENVIRONMENTAL CONDITIONS - JUNCTION-TO-BOARD:** This specification should be used in conjunction with the overview document JESD51, Methodology for the Thermal Measurement of Component Packages (Single Semiconductor Device) [1] and the electrical test procedures described in JESD51-1, 'Integrated Circuit Thermal Measurement Method (Single Semiconductor Device' [2. The environmental conditions described in this document are specifically designed for testing of integrated circuit devices that are mounted on standard test boards with two internal copper planes [3]. This standard is not applicable to packages that have asymmetric heat flow paths to the printed board caused by such thermal enhancements as fused leads (leads connected to the die

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pad) or power style packages with the exposed heat slug on one side of the package.

October 1999 /JC-15.1 Subcommittee $45.00

JESD 51- 9 **TEST BOARDS FOR AREA ARRAY SURFACE MOUNT PACKAGE THERMAL MEASUREMENTS:** This standard covers the design of printed circuit boards (PCBs) used in the thermal characterization of ball grid array (BGA) and land grid array (LGA) packages. It is intended to be used in conjunction with the JESD51 series of standards that cover the test methods and test environments. JESD51-9 was developed to give a figure-of-merit of thermal performance that allows for accurate comparisons of packages from different suppliers. It can be used to give a first order approximation of system performance and, in conjunction with the other JESD51 PCB standards, allows for comparisons of the various package families.

July 2000 /JC-15.1 Subcommittee $48.00

JESD 51-10 **TEST BOARDS FOR THROUGH-HOLE PERIMETER LEADED PACKAGE THERMAL MEASUREMENTS:** This standard covers the design of printed circuit boards (PCBs) used in the thermal characterization of Dual-Inline Packages (DIP) and Single-Inline Packages (SIP). It is intended to be used in conjunction with the JESD51 series of standards that cover the test methods and test environments. JESD51-10 was developed to give a figure-of-merit of thermal performance that allows for accurate comparisons of packages from different suppliers. It can be used to give a first order approximation of system performance and, in conjunction with the other JESD51 PCB standards, allows for comparisons of the various package families.

July 2000 /JC-15.1 Subcommittee $45.00

JESD 51-11 **TEST BOARDS FOR THROUGH-HOLE AREA ARRAY LEADED PACKAGE THERMAL MEASUREMENT:** This standard covers the design of printed circuit boards (PCBs) used in the thermal characterization of Pin Grid Array (PGA) packages. It is intended to be used in conjunction with the JESD51 series of standards that cover the test methods and test environments. JESD51-11 was developed to give a figure-of-merit of thermal performance that allows for accurate comparisons of packages from different suppliers. It can be used to give a first order approximation of system performance and, in conjunction with the other JESD51 PCB standards, allows for comparisons of the various package families.

June 2001 /JC-15.1 Subcommittee $47.00

JESD 52 **STANDARD FOR DESCRIPTION OF LOW VOLTAGE TTL-COMPATIBLE CMOS LOGIC DEVICES:** This standard describes dc interface specifications and test environment for these devices that operate with 2.7 V to 3.6 V power supplies. The goal is to provide a

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consistent set of dc specifications for reference by logic suppliers and users alike.

November 1995 /JC-40 Committee $45.00

JESD 53 **MANAGEMENT OF COMPONENT OBSOLESCENCE BY GOVERNMENT CONTRACTORS: RESCINDED, October 2002**

January 1996; Rescinded October 2002 October 2002 /JC-13.2 Subcommittee

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JESD 54 **STANDARD FOR DESCRIPTION OF 54/74ABTXXX AND 74BCXXX TTL-COMPATIBLE BiCMOS LOGIC DEVICES:** The purpose is to provide a standard of BiCMOS Logic series specifications to provide for uniformity, multiplicity of sources, elimination of confusion, and ease of device specification and design by users.

February 1996 /JC-40 Committee $61.00

JESD 55 **STANDARD FOR DESCRIPTION OF LOW-VOLTAGE TTL-COMPATIBLE BiCMOS LOGIC DEVICES:** The purpose is to provide a standard of BiCMOS Logic series specifications for uniformity, multiplicity of sources, elimination of confusion, and ease of device specification and design by users.

May 1996 /JC-40 Committee $49.00

JESD 57 **TEST PROCEDURE FOR THE MANAGEMENT OF SINGLE-EVENT EFFECTS IN SEMICONDUCTOR DEVICES FROM HEAVY ION IRRADIATION:** This test method defines requirements and procedures for ground simulation and single event effects (SEE) and implementation of the method in testing integrated circuits. This standard is valid when using a cyclotron or Van de Graaff accelerator. Microcircuits under test must be delidded. The ions used at the facilities have an atomic number Z > 2. It does not apply to SEE testing that uses protons, neutrons, or other lighter particles. This standard is designed to eliminate any misunderstanding between users of the method and test facilities, to minimize delays, and to promote standardization of testing and test data.

December 1996; Under Revision September 2003 /JC-13.4 Subcommittee $67.00

JESD 59 **BOND WIRE MODELING STANDARD:** This standard describes the modeling of a bond wire from an integrated circuit (IC) die to a package lead in a ball or wedge type wire bond configuration.

June 1997 /JC-15.2 Subcommittee $45.00

JESD 60A **A PROCEDURE FOR MEASURING P-CHANNEL MOSFET HOT-CARRIER-INDUCED DEGRADATION AT MAXIMUM GATE CURRENT UNDER DC STRESS:** This method establishes a standard procedure for accelerated testing of the hot-carrier-induced change of a p-channel MOSFET. The objective is to provide a minimum set of

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measurements so that accurate comparisons can be made between different technologies. The measurements specified should be viewed as a starting pint in the characterization and benchmarking of the trasistor manufacturing process.

September 2004 August 2002 /JC-14.2 Subcommittee $52.00

JESD 61A

ISOTHERMAL ELECTROMIGRATION TEST PROCEDURE: This standard describes an algorithm for the execution of the isothermal test, using computer-controlled instrumentation. The primary use of this test is for the monitoring of microelectronic metallization lines at water level (1) in process development, to evaluate process options, (2) in manufacturing, to monitor metallization reliability and (3) to monitor/evaluate process equipment. While it is developed as a fast WLR test, it can also be an effective tool for controlling the uniformity of stress applied during the standard package level electromigration test.

May 2007 June 2006 /JC-14.2 Subcommittee $67.00

JESD 62-A

OUTLIER IDENTIFICATION AND MANAGEMENT SYSTEM FOR ELECTRONIC COMPONENTS: This revision incorporates recommended tests and an example of a statistics-based method for identifying and removing outliers, i.e., parts that meet supplier specifications and end-user requirements but lie outside typical distribution limits. Outlier product can occur during fabrication, assembly, packaging, or test of any electronic components.

May 2002 /JC-14.3 Subcommittee $45.00

JESD 63

STANDARD METHOD FOR CALCULATING THE ELECTROMIGRATION MODEL PARAMETERS FOR CURRENT DENSITY AND TEMPERATURE: This method provides procedures to calculate sample estimates and their confidence intervals for the electromigration model parameters of current density and temperature. The model parameter for current density is the exponent (n) to which the current density is raised in Black's equation. The parameter for temperature is the activation energy for the electromigration failure process.

February 1998 /JC-14.2 Subcommittee $61.00

JESD 64-A

STANDARD FOR DESCRIPTION OF 2.5 V CMOS LOGIC DEVICES WITH 3.6 V CMOS TOLERANT INPUTS AND OUTPUTS: The purpose is to provide a standard for 2.5 V nominal supply voltage logic devices for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use. This specification provides for compatibility between devices operating between either the Standard Range of 1.8 V to 2.7 V or the optional Extended Range of 1.65 V to 2.7 V supply voltages, as well as over-voltage tolerance with devices operating at 3.6 V.

October 2000 /JC-40 Committee $40.00

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JESD 65B 

DEFINITION OF SKEW SPECIFICATIONS FOR STANDARD LOGIC DEVICES: This standard defines skew specifications and skew testing for standard logic devices. The purpose is to provide a standard for specifications to achieve uniformity, multiplicity of sources, elimination of confusion, and ease of device specification and design by users.

September 2003 /JC-40 Committee $48.00

JESD 66 

TRANSIENT VOLTAGE SUPPRESSOR STANDARD FOR THYRISTOR SURGE PROTECTIVE DEVICE: This standard is applicable to Thyristor Surge Protective Devices. It describes terms and definitions and explains methods for verifying device ratings and measuring device characteristics. The intended users of this standard are those interested in Thyristor Surge Protective Device characterization and rating verification. These devices are used primarily by the telecommunications industry to protect circuits from harmful overvoltages. The Thyristor Surge Protective Device (TSPD) is a semiconductor device that is finding widespread application in the telecommunication industry. The intent of this stand is to provide information on test methods that will reduce the possibility of disagreement and misunderstanding between TSPD vendors and users, and facilitate the determination of device interchangeability.

November 1999 /JC-22.5 Subcommittee $91.00

JESD 67 

I/O DRIVERS AND RECEIVERS WITH CONFIGURABLE COMMUNICATION VOLTAGE, IMPEDANCE, AND RECEIVER THRESHOLD: This standard attempts to aid in the design of electronic systems comprised of components that operate at several different supply voltages. This document covers respectively configurable I/O voltage, receiver type and switchpoint, and driver impedance.

February 1999 /JC-16 Committee $45.00

JESD 68.01 

COMMON FLASH INTERFACE (CFI): The Common Flash Interface (CFI) specification outlines a device and host system software interrogation handshake that allows specific software algorithms to be used for entire families of devices. This allows device-independent, JEDEC ID-independent, and forward- and backward-compatible software support for the specific flash families. It allows flash vendors to standardize their existing interfaces for long-term compatibility. The changes for this minor revision are indicated in Annex A on page 11.

September 2003 December 2002 /JC-42.4 Subcommittee $48.00

JESD 69A 

INFORMATION REQUIREMENTS FOR THE QUALIFICATION OF SILICON DEVICES: This standard establishes the information required by semiconductor users from IC manufacturers and distributors in order to judge whether a semiconductor component is fit for use in their particular application. It establishes a set of data elements that describes the component and defines what each element

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means. It does not define the quality and reliability requirements that the component must satisfy. This standard can be used in conjunction with other reliability qualification standards, such as JESD34 'Failure Mechanism-Driven Reliability Qualification of Silicon Devices' and JESD47 'Stress Test Driven Qualification of Integrated Circuits'.

October 2006 January 2006 /JC-14.3 Subcommittee $43.00

JESD 70

2.5 V BiCMOS LOGIC DEVICE FAMILY SPECIFICATION WITH 5 V TOLERANT INPUTS AND OUTPUTS: The purpose is to provide a standard for 2.5 V nominal supply voltage logic devices, for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use, thus providing compatibility between devices operating between 2.3 V and 2.7 V supply voltages, as well as overvoltage tolerance with devices operating at 3.3 V, or 5 V.

June 1999 /JC-40 Committee $41.00

JESD 71

STANDARD TEST AND PROGRAMMING LANGUAGE (STAPL): STAPL is a vendor- and platform-independent language for programming and testing devices via the IEEE standard 1149.1 interface, commonly known as JTAG. STAPL enables programming of designs into programmable logic devices (PLDs) offered by a variety of PLD vendors. STAPL is also suitable for testing 1149.1-compliant devices.

August 1999 / Committee!33JC421 $67.00

JESD 72

TEST METHODS AND ACCEPTANCE PROCEDURES FOR THE EVALUATION OF POLYMERIC MATERIALS: This Test Method covers the minimum requirements that should be in effect for the evaluation and acceptance of polymeric materials for use in industrial, military, space, and other special-condition products which may require capabilities beyond standard commercial microelectronics applications. It is not the intent of this Publication to specify a material, but to evaluate the material to assure that the quality and reliability of the microelectronic devices are not compromised. This document replaces JEP105, JEP107 and JEP112.

June 2001 January 2001 /JC-13.5 Subcommittee $52.00

JESD 73

DESCRIPTION OF 5 V BUS SWITCH WITH TTL-COMPATIBLE CONTROL INPUTS: This standard covers specifications for a family of 5 V NMOS FET bus switch devices with 5 V TTL compatible control inputs. Not included in this document are device-specific parameters and performance levels that the vendor must also apply for full device description.

June 1999 /JC-40 Committee $40.00

JESD 73-1 **STANDARD FOR DESCRIPTION OF 3.3 V NFET BUS SWITCH**

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DEVICES: This standard covers specifications for a family of 3.3 V NMOS FET bus switch devices. Not included in this document are device specific parameters and performance levels that the vendor must also supply for full device description. The purpose of this document is to provide a set of uniform data sheet parameters for the description of bus switch devices. This standard includes required parameters, test conditions, test levels, and measurement methods for data sheet descriptions of bus switch devices.

August 2001 /JC-40 Committee $40.00

JESD 73-2 **STANDARD FOR DESCRIPTION OF 3.3 V NFET BUS SWITCH DEVICES WITH INTEGRATED CHARGE PUMPS:** This standard covers specifications for a family of 3.3 V NMOS FET bus switch devices with integrated charge pumps. Not included in this document are device specific parameters and performance levels that the vendor must also supply for full device description. The purpose of this standard is to provide a set of uniform data sheet parameters for the description of bus switch devices. This standard includes required parameters, test conditions, test levels, and measurement methods for data sheet descriptions of bus switch devices.

August 2001 /JC-40 Committee $40.00

JESD 73-3 **STANDARD FOR DESCRIPTION OF 3867 - 2.5 V, SINGLE 10-BIT, 2-PORT, DDR FET SWITCH:** This standard provides a set of uniform data sheet parameters for the description of a single 10-bit, 2.5 V FET transmission-gate bus switch device for DDR memory module and motherboard applications. This bus switch device has a low ON resistance allowing inputs to be connected directly to outputs, with near zero propagation delay.

November 2001 / Committee!33JC402 $40.00

JESD 73-4 **STANDARD FOR DESCRIPTION OF 3877 - 2.5 V, DUAL 5-BIT, 2-PORT, DDR FET SWITCH:** This standard provides a set of uniform data sheet parameters for the description of a dual 5-bit, 2.5 V FET transmission-gate bus switch device for DDR memory module and motherboard applications. This bus switch device has a low ON resistance allowing inputs to be connected directly to outputs, with near zero propagation delay.

November 2001 / Committee!33JC402 $40.00

JESD 74A **EARLY LIFE FAILURE RATE CALCULATION PROCEDURE FOR SEMICONDUCTOR COMPONENTS:** This standard defines methods for calculating the early life failure rate of a product, using accelerated testing, whose failure rate is constant or decreasing over time. For technologies where there is adequate field failure data, alternative methods may be used to establish the early life failure rate. The purpose of this standard is to define a procedure for performing measurement and calculation of early life failure rates. Projections can be used to compare reliability performance with objectives,

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provide line feedback, support service cost estimates, and set product test and screen strategies to ensure that the ELFR meets customers' requirements.

February 2007 September 2006 /JC-14.3 Subcommittee $61.00

JESD 75 

BALL GRID ARRAY PINOUTS STANDARDIZED FOR 32-BIT LOGIC FUNCTIONS: The purpose of this standard is to provide a pinout standard for dual-die 32-bit logic devices offered in a 96- and 144-ball grid array package for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease use. This standard defines device output for 32-bit wide buffer, driver and transceiver functions. This pinout specifically applies to the conversion of DIP-packaged 16-bit logic devices to LFBGA-packaged dual-die 32-bit logic devices.

November 1999 /JC-40 Committee $38.00

JESD 75-1 

BALL GRID ARRAY PINOUTS STANDARDIZED FOR 16, 18, AND 20-BIT LOGIC FUNCTIONS USING A 54 BALL PACKAGE: This standard establishes a 54 Ball Grid Array pinout for 16, 18 and 20-bit standard logic devices that are currently being produced in 48 and 56 Pin SSOP and TSSOP packages. The 54 Ball Grid Array Package is organized as a 6 x 9 array with balls on a .8mm x .8mm grid pitch.

October 2001 /JC-40 Committee $38.00

JESD 75-2 

BALL GRID ARRAY PINOUTS STANDARDIZED FOR 16-BIT LOGIC FUNCTIONS: This standard provides a pinout standard for 16-bit wide logic devices offered in a 56-ball areagrid array package to provide for uniformity, multiplicity of sources, elimination of confusion,ease of device specification, and ease of use.

July 2001 /JC-40 Committee $38.00

JESD 75-3 

BALL GRID ARRAY PINOUTS STANDARDIZED FOR 8-BIT LOGIC FUNCTIONS: This standard provides a pinout standard for 8-bit logic devices offered in a 20-ball area gridarray package to provide for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use.

July 2001 /JC-40 Committee $37.00

JESD 75-4 

Ball Grid Array Pinout for 1-, 2-, and 3-Bit Logic Functions This standard defines device pinout for 1-, 2- and 3-bit wide logic functions. This pinout specifically applies to the conversion of Dual-Inline-Packaged (DIP) 1-, 2- and 3-bit logic devices to DSBGA-packaged 1-, 2- and 3-bit logic devices.

March 2004 June 2003 /JC-40 Committee $41.00

JESD 75-5 

SON/QFN PACKAGE PINOUTS STANDARDIZED FOR 1-, 2-, AND 3-BIT LOGIC FUNCTIONS This standard defines device pinout for 1-,

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2- and 3-bit wide logic functions. This pinout specifically applies to the conversion of Dual-Inline-Packaged (DIP) 1-, 2- and 3-bit logic devices to SON/QFN packaged 1-, 2- and 3-bit logic devices. The purpose of this document is to provide a pinout standard for 1-, 2- and 3-bit logic devices offered in 5-, 6- or 8-land SON/QFN packages for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use.

July 2004 December 2003 /JC-40.1 Subcommittee $41.00

JESD 75-6 **PSO-N/PQFN Pinouts Standardized for 14-, 16-, 20-, and 24-Lead Logic Functions** This standard defines device pinouts for 14-, 16-, 20-, and 24-lead logic functions. This pinout standard specifically applies to the conversion of DIP-packaged logic devices to PSO-N/PQFN packages logic devices. The purpose of this standard is to provide a pinout standard for 14-, 16-, 20-, and 24-lead logic devices offered in 14-, 16-, 20-, and 24-lead PSO-N/PQFN packages for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use.

March 2006 September 2005 /JC-40.1 Subcommittee $41.00

JESD 76 **DESCRIPTION OF 1.8 V CMOS LOGIC DEVICES:** This standard continues the voltage specification migration to the next level beyond the 2.5 V specification already established in JESD80. In this standard, the input and output conditions are described for CMOS Logic products in a 1.8 V (Normal Range) application.

April 2000 /JC-40.1 Subcommittee $38.00

JESD 76-1 **STANDARD DESCRIPTION OF 1.2 V CMOS LOGIC DEVICES (WIDE RANGE OPERATION):** This standard defines dc interface, switching parameters and test loading for digital logic devices based on 1.2 V (nominal) power supply levels. The purpose is to provide a standard specification for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use.

June 2001 /JC-40 Committee $38.00

JESD 76-2 **STANDARD DESCRIPTION OF 1.2 V CMOS LOGIC DEVICES (NORMAL RANGE OPERATION):** This standard defines dc interface, switching parameters and test loading for digital logic devices based on 1.2 V (normal range) power supply levels. The purpose is to provide a standard specification for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use.

June 2001 /JC-40 Committee $38.00

JESD 76-3 **STANDARD DESCRIPTION OF 1.5 V CMOS LOGIC DEVICES:** This standard continues the voltage specification migration to the next level beyond the 1.8 V specification already established. The

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purpose is to provide a standard for 1.5 V nominal supply voltage CMOS logic devices, for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use.

August 2001 /JC-40.1 Subcommittee $38.00

JESD 77B.01

TERMS, DEFINITIONS, AND LETTER SYMBOLS FOR DISCRETE SEMICONDUCTOR AND OPTOELECTRONIC DEVICES: A revised and significantly expanded reference for technical writers and educators, manufacturers, buyers and users of discrete semiconductor and optoelectronic devices, is now available. Revision B of JEDEC Standard No. 77 includes extensive information on: letter symbol conventions; diodes and rectifiers (including signal, rectifier, microwave, tunnel and backward, voltage-regulator, voltage-reference, current regulator, and varactor diodes); transistors (including FETs, JFETs, and IGBTs); photosensitive devices, photoemitters, and optocouplers; thyristors and PUTs; and transient voltage suppressors. Terms and symbols, with their definitions, are arranged alphabetically by product type. Where applicable, graphical symbols are also included.

July 2006 /JC-10 Committee $162.00

JESD 78A

IC LATCH-UP TEST: This standard has been adopted by the Defense Logistics Agency (DLA) as project 5962-1880. This standard establishes a defined method for latch-up testing of ICs. It defines Classes and Levels for a device's latch-up capability so that both the user and supplier understand a device's latch-up capabilities. It is applicable to NMOS, CMOS, Bipolar, and all variations and combinations of these technologies. Latch-up is an extremely important factor in determining product reliability. This document contains the corrected figure 4 to include T6 on page 12, this change was made in January 1998.

February 2006 January 2005 /JC-14.1 Subcommittee $55.00

JESD 79-2C

DDR2 SDRAM SPECIFICATION This comprehensive standard defines all required aspects of 256Mb through 4Gb DDR2 SDRAMs with x4/x8/x16 data interfaces, including pinout, addressing, functional description, features, ac and dc parametrics, truth tables, and packages. Standard JESD79-2 uses a SSTL_18 interface, which is described in another JEDEC standard called JESD8-15. The purpose of this Standard is to define the minimum set of requirements for compliant devices 256Mb through 4Gb, x4/x8/x16 DDR2 SDRAMs. System designs based on the required aspects of this specification will be supported by all DDR2 SDRAM vendors providing compliant devices. Changes between versions is indicated in Annex A.

May 2006 September 2005 /JC-42.3 Subcommittee $127.00

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JESD 79-3A DDR3 SDRAM Standard - Reposted 09/25/2007 correctly.

This document defines the DDR3 SDRAM specification, including features, functionalities, AC and DC characteristics, packages, and ball/signal assignments. The purpose of this Specification is to define the minimum set of requirements for JEDEC compliant 512 Mb through 8 Gb for x4, x8, and x16 DDR3 SDRAM devices. This specification was created based on the DDR2 specification (JESD79-2) and some aspects of the DDR specification (JESD79). Each aspect of the changes for DDR3 SDRAM operation were considered and approved by committee ballots). The accumulation of these ballots were then incorporated to prepare this JESD79-3 specification, replacing whole sections and incorporating the changes into Functional Description and Operation.

September 2007 June 2006 /JC-42.3 Subcommittee $177.00

JESD 79E **DOUBLE DATA RATE (DDR) SDRAM SPECIFICATION:** This comprehensive standard defines all required aspects of 64Mb through 1Gb DDR SDRAMs with X4/X8/X16 data interfaces, including features, functionality, ac and dc parametrics, packages and pin assignments. This scope will subsequently be expanded to formally apply to x32 devices, and higher density devices as well. The purpose of this Standard is to define the minimum set of requirements for JEDEC compliant 64Mb through 1Gb, X4/X8/X16 DDR SDRAMs. System designs based on the required aspects of this specification will be supported by all DDR SDRAM vendors providing JEDEC compliant devices.

May 2005 /JC-42.3 Subcommittee $109.00

JESD 8-16A **BUS INTERCONNECT LOGIC (BIC) FOR 1.2 V** This standard defines the electrical parameters for high-speed interfaces for use in the 1.2V electrical environment. Included in the standard are a single ended signaling interface suitable for parallel busses, and a differential signaling interface suitable for clock applications or parallel differential buses. JEDEC ?BIC? Standard JESD8-16A continues the tradition of the JESD8-xx standards, defining electrical interfaces for the industry as new technologies and bus requirements develop. Previously, JEDEC defined standard JESD8-6, the ?HSTL? standard, for use in 1.5V electrical environments. BIC is similar to HSTL, except the power supply voltage has dropped from 1.5V to 1.2V, and interface requirements are tightened to allow much higher speeds.

November 2004 June 2004 /JC-16 Committee $52.00

JESD 80 **STANDARD FOR DESCRIPTION OF 2.5 V CMOS LOGIC DEVICES:** The purpose of this standard is to provide a standard for 2.5 V nominal supply-voltage CMOS logic devices, for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use. This standard defines dc interface parameters and test loading for CMOS digital logic family based on 2.5 V (nominal) power supply levels at 2.5 V input tolerance.

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November 1999 /JC-40 Committee $38.00

JESD 82 

DEFINITION OF CDCV857 PLL CLOCK DRIVER FOR REGISTERED DDR DIMM APPLICATIONS: This specification is a reference for Registered DDR DIMM designers. JESD82 defines the physical, electrical, interface and timing requirements of a 1:10 PLL clock driver for DDR Registered DIMMs from DDR200 to DDR266 as refined in revision C of JEDEC Standard 21-C (JESD21-C). JESD82 was also written to meet the future performance requirements of Registered DIMMs for DDR300 and DDR333.

July 2000 /JC-40 Committee $47.00

JESD 82-10A 

DEFINITION OF THE SSTU32866 1.8 V CONFIGURABLE REGISTERED BUFFER WITH PARITY FOR DDR2 RDIMM APPLICATIONS This standard defines standard specifications of dc interface parameters, switching parameters, and test loading for definition of the SSTU32866 registered buffer with parity test for DDR2 RDIMM applications. The purpose is to provide a standard for the SSTU32866 (see Note) logic device, for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use.

May 2007 September 2006 /JC-40.4 Subcommittee $63.00

JESD 82-11 

DEFINITION OF 'CU878 PLL CLOCK DRIVER FOR REGISTERED DDR2 DIMM APPLICATIONS This standard defines standard specifications of dc interface parameters, switching parameters, and test loading for definition of a ?CU878 PLL clock device for registered DDR2 DIMM applications. The purpose is to provide a standard for a ?CU878 PLL clock device, for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use.

September 2004 February 2004 /JC-40.3 Subcommittee $48.00

JESD 82-12A 

DEFINITION OF THE SSTU32S869 & SSTU32D869 REGISTERED BUFFER WITH PARITY FOR DDR2 RDIMM APPLICATIONS This standard defines standard specifications of DC interface parameters, switching parameters, and test loading for definition of the SSTU32S869 and SSTU32D869 registered buffer with parity for driving heavy load on high-density DDR2 RDIMM applications. A typical application would be a 36 SDRAM planar DIMM. The purpose is to provide a standard for the SSTU32S869 and SSTU32D869 logic devices, for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use.

April 2007 September 2006 /JC-40 Committee $57.00

JESD 82-13A 

DEFINITION OF THE SSTVN16859 2.5-2.6 V 13-BIT TO 26-BIT SSTL_2 REGISTERED BUFFER FOR PC1600, PC2100, PC2700 AND PC3200 DDR DIMM APPLICATIONS This standard defines standard

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specifications of dc interface parameters, switching parameters, and test loading for definition of the SSTVN16859 13-bit to 26-bit SSTL_2 registered buffer for PC1600, PC2100, PC2700 and PC3200 DDR DIMM applications. The SSTVN16859 is a speed upgrade of the SSTV16859 (JESD82-4) for use in PC3200 DDR DIMMs. It is fully backward compatible with SSTV16859 for all speed grades.

May 2005 September 2004 /JC-40 Committee $48.00

JESD 82-14A **DEFINITION OF THE SSTUB32868 1.8 V CONFIGURABLE REGISTERED BUFFER WITH PARITY FOR DDR2 RDIMM APPLICATIONS**

This standard defines standard specifications of dc interface parameters, switching parameters, and test loading for definition of the SSTUB32868 registered buffer with parity test for DDR2 RDIMM applications. SSTU32S2868 denotes a single-die implementation and SSTU32D868 denotes a dual-die implementation.

October 2006 June 2005 /JC-40 Committee $57.00

JESD 82-15 **STANDARD FOR DEFINITION OF CUA878 PLL CLOCK DRIVER FOR REGISTERED DDR2 DIMM APPLICATIONS** This standard defines standard specifications of dc interface parameters, switching parameters, and test loading for definition of a CUA878 PLL clock device for registered DDR2 DIMM applications. The purpose is to provide a standard for a CUA878 PLL clock device, for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use.

November 2005 September 2004 /JC-40 Committee $49.00

JESD 82-16A **DEFINITION OF THE SSTUA32866 1.8 V CONFIGURABLE REGISTERED BUFFER WITH PARITY TEST FOR DDR2 RDIMM APPLICATIONS** This standard defines standard specifications of dc interface parameters, switching parameters, and test loading for definition of the SSTUA32866 registered buffer with parity test for DDR2 RDIMM applications. The purpose is to provide a standard for the SSTUA32866 (see Note) logic device, for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use.

May 2007 June 2006 /JC-40 Committee $63.00

JESD 82-17 **DEFINITION OF THE SSTUA32S868 AND SSTUA32D868 REGISTERED BUFFER WITH PARITY FOR 2R X 4 DDR2 RDIMM APPLICATIONS**

This standard defines standard specifications of dc interface parameters, switching parameters, and test loading for definition of the SSTUA32S868 and SSTUA32D868 registered buffer with parity test for DDR2 RDIMM applications.

November 2005 June 2004 /JC-40.3 Subcommittee $57.00

JESD 82-18A **STANDARD FOR DEFINITION OF THE CUA877 AND CU2A877 PLL CLOCK DRIVERSFOR REGISTERED DDR2 DIMM APPLICATIONS** This standard defines standard specifications of dc interface parameters,

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switching parameters, and test loading for definition of the CUA877 and CU2A877 PLL clock devices for registered DDR2 DIMM applications.The purpose is to provide a standard for the CUA877 and CU2A877 PLL clock devices, for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use.

January 2007 June 2006 /JC-40 Committee $49.00

JESD 82-19A **DEFINITION OF THE SSTUA32S865 AND SSTUA32D865 28-BIT 1:2 REGISTERED BUFFER WITH PARITY FOR DDR2 RDIMM APPLICATIONS** This standard defines standard specifications of dc interface parameters, switching parameters, and test loading for definition of the SSTUA32S865 and SSTUA32D865 registered buffer with parity for 2 rank by 4 or similar high-density DDR2 RDIMM applications.

May 2007 June 2006 /JC-40 Committee $55.00

JESD 82-1A **DEFINITION OF CVF857 PLL CLOCK DRIVER FOR REGISTERED PC1600, PC2100, PC2700, AND PC3200 DIMM APPLICATIONS:** This standard defines standard specifications of dc interface parameters, switching parameters, and test loading for definition of a CV857 PLL clock device for registered PC1600, PC2100, PC2700 and PC3200 DIMM applications. The purpose is to provide a standard for a CV857 PLL clock device, for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use.

May 2004 /JC-40 Committee $52.00

JESD 82-2 **STANDARD FOR DESCRIPTION OF A 3.3 V, 18-BIT, LVTTL I/O REGISTER FOR PC133 REGISTERED DIMM APPLICATIONS:** This standard defines the register support devices needed for standard height and low profile registered PC133 SDRAM DIMM modules. The objective of the standard is to clearly define the functionality, pinout and electrical characteristics required for this type of SDRAM module.

July 2001 /JC-40 Committee $45.00

JESD 82-20 **FBDIMM: Advanced Memory Buffer (AMB)** This document is a core specification for a Fully Buffered DIMM (FBD) memory system. This document, along with the other core specifications, must be treated as a whole. Information critical to a Advanced Memory Buffer design appears in the other specifications, with specific cross-references provided.

March 2007 March 2006 /JC-40 Committee $177.00

JESD 82-21 **STANDARD FOR DEFINITION OF CUA845 PLL CLOCK DRIVER FOR REGISTERED DDR2 DIMM APPLICATIONS** This standard defines standard specifications of dc interface parameters, switching parameters, and test loading for definition of a CUA845 PLL clock

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device for registered DDR2 DIMM applications.The purpose is to provide a standard for a CUA845 PLL clock device, for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use.

January 2007 March 2006 /JC-40 Committee $48.00

JESD 82-22 INSTRUMENTATION CHIP DATA SHEET FOR FBDIMM DIAGNOSTIC SENSELINES This device is a one-chip spectrum analyzer that operates in the frequency range from 1 to 2 GHz. It requires no external components except some filtering of the voltage supply (one inductor, one bypass capacitor). The frequency of the VCO is adjusted by an internal DAC. No PLL loop is used to lock the VCO to a reference frequency. A counter is used to determine the VCO frequency. The device has a serial I2C data interface. The device is available in a 28 pin TQFN package and is specified over the extended industrial (-40 C to +85 C) temperature range.

November 2006 March 2006 /JC-40.4 Subcommittee $47.00

JESD 82-23 DEFINITION OF the SSTUA32S869 AND SSTUA32D869 REGISTERED BUFFER WITH PARITY FOR DDR2 RDIMM APPLICATIONS This standard defines standard specifications of DC interface parameters, switching parameters, and test loading for definition of the SSTUA32S869 and SSTUA32D869 registered buffer with parity for driving heavy load on high-density DDR2 RDIMM applications. A typical application would be a 36 SDRAM planar DIMM. The SSTUA32S869 and SSTUA32D869 are identical in functionality to the SSTU32S869 and SSTU32D869 devices respectively but specify tighter timing characteristics and a higher application frequency of up to 410MHz.

May 2007 June 2006 /JC-40 Committee $59.00

JESD 82-24 DEFINITION OF the SSTUB32865 28-bit 1:2 REGISTERED BUFFER WITH PARITY FOR DDR2 RDIMM APPLICATIONS This standard defines standard specifications of dc interface parameters, switching parameters, and test loading for definition of the SSTUB32865 registered buffer with parity for 2 rank by 4 or similar high-density DDR2 RDIMM applications. The SSTUB32865 is identical in functionality to the SSTU32865 but specifies tighter timing characteristics and a higher application frequency of up to 410MHz.

May 2007 September 2006 /JC-40 Committee $55.00

JESD 82-25 DEFINITION OF the SSTUB32866 1.8 V CONFIGURABLE REGISTERED BUFFER WITH PARITY FOR DDR2 RDIMM APPLICATIONS This standard defines standard specifications of dc interface parameters, switching parameters, and test loading for definition of the SSTUB32866 registered buffer with parity test for DDR2 RDIMM applications.

May 2007 September 2006 /JC-40 Committee $63.00

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JESD 82-26 **DEFINITION OF THE SSTUB32868 REGISTERED BUFFER WITH PARITY FOR 2R x 4 DDR2 RDIMM APPLICATIONS** This standard defines standard specifications of dc interface parameters, switching parameters, and test loading for definition of the SSTUB32868 registered buffer with parity test for DDR2 RDIMM applications.

May 2007 September 2006 /JC-40 Committee $57.00

JESD 82-27 **Definition of the SSTUB32869 Registered Buffer with Parity for DDR2 RDIMM Applications** This standard defines standard specifications of DC interface parameters, switching parameters, and test loading for definition of the SSTUB32869 registered buffer with parity for driving heavy load on high-density DDR2 RDIMM applications. A typical application would be a 36 SDRAM planar DIMM.

May 2007 September 2006 /JC-40 Committee $59.00

JESD 82-3B **DEFINITION OF THE SSTV16857 2.5 V, 14-BIT SSTL_2 REGISTERED BUFFER FOR DDR DIMM APPLICATIONS:** This standard defines standard specifications of dc interface parameters, switching parameters, and test loading for definition of the SSTV16857 14-bit SSTL_2 registered buffer for DDR DIMM applications.The purpose is to provide a standard for the SSTV16857 logic device, for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use.

November 2004 December 2003 JC-40.3 $48.00

JESD 82-4B **STANDARD FOR DEFINITION OF THE SSTV16859 2.5 V, 13-BIT TO 26-BIT SSTL_2 REGISTERED BUFFER FOR STACKED DDR DIMM APPLICATIONS:** This standard defines standard specifications of dc interface parameters, switching parameters, and test loading for definition of the SSTV16859 13-bit to 26-bit SSTL_2 registered buffer for stacked DDR DIMM applications. The purpose is to provide a standard for the SSTV16859 logic device, for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use.

May 2003 /JC-40 Committee $47.00

JESD 82-5 **STANDARD FOR DESCRIPTION OF A 3.3 V, ZERO DELAY CLOCK DISTRIBUTION DEVICE COMPLIANT WITH THE JESD21-C PC133 REGISTERED DIMM SPECIFICATION** This standard defines the PLL support devices required for standard height and low profile registered PC133 SDRAM DIMM modules. The objective of the standard is to clearly define the functionality, pinout and electrical characteristics of the PLL used on JEDEC standard modules.JESD82-5 is the latest specification to be added to the JESD82 family of specifications for memory module support

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devices. Additional specifications are currently under development for DDR2 support devices.

July 2002 /JC-40 Committee $43.00

JESD 82-6A **DEFINITION OF THE SSTV32852 2.5 V 24-BIT TO 48-BIT SSTL_2 REGISTERED BUFFER FOR 1U STACKED DDR DIMM APPLICATIONS:** This standard defines standard specifications of dc interface parameters, switching parameters, and test loading for definition of the SSTV32852 24-bit to 48-bit SSTL_2 registered buffer for stacked DDR DIMM applications. The purpose is to provide a standard for the SSTV32852 logic device, for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use.

November 2004 December 2003 /JC-40 Committee $47.00

JESD 82-7A **DEFINITION OF THE SSTU32864 1.8-V CONFIGURABLE REGISTERED BUFFER FOR DDR2 RDIMM APPLICATIONS:** This standard defines standard specifications of dc interface parameters, switching parameters, and test loading for definition of the SSTU32864 configurable registered buffer for DDR2 RDIMM applications. The purpose is to provide a standard for the SSTU32864 logic device, for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use.

October 2004 /JC-40.4 Subcommittee $47.00

JESD 82-9B **DEFINITION OF SSTU32865 REGISTERED BUFFER WITH PARITY FOR 2R x 4 DDR2 RDIMM APPLICATIONS** This standard provides the functional definition, ball-out configuration and package outline, signal definitions and input/output characteristics for a 28-bit 1:2 registered driver with parity suitable for use on DDR2 RDIMMs. The SSTU32865 integrates the functional equivalent of two SSTU32864 devices (as defined in JESD82-7) into a single device, thereby easing layout and board design constraints especially on high density RDIMMs such as dual rank, by four configurations. Moreover, the optional use of a parity function is provided for, permitting detection and reporting of parity errors across its 22 data inputs. JESD82-9 specifies a 160-pin Thin-profile, fine-pitch ball-grid array (TFBGA) package.

May 2007 September 2006 /JC-40.4 Subcommittee $52.00

JESD 84-A41 **EMBEDDED MULTIMEDIACARD (eMMC) PRODUCT STANDARD, STANDARD CAPACITY** This document provides a definition of the Embedded MultiMediaCard product, its environment, and handling. It also provides design guidelines and defines a tool box of macro functions and algorithms intended to reduce design-in costs.

July 2007 If you downloaded this file prior to 8/23/07 please download again. May 2007 /JC-64 Committee $55.00

JESD 84- **EMBEDDED MULTIMEDIACARD (eMMC) PRODUCT STANDARD, HIGH**

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A42 	**CAPACITY** This document provides a definition of the Embedded MultiMediaCard product, its environment, and handling. It also provides design guidelines and defines a tool box of macro functions and algorithms intended to reduce design-in costs. July 2007 If you downloaded this file prior to 8/23/07 please download again. June 2007 /JC-64 Committee	$57.00
JESD 84-B41 	**MULTIMEDIACARD (MMC) ELECTRICAL STANDARD, STANDARD CAPACITY (MMCA, 4.1)** This document provides a comprehensive definition of the MultiMediaCard, its environment, and handling. It also provides design guidelines and defines a tool box of macro functions and algorithms intended to reduce design-in costs. June 2007 June 2007 /JC-64.1 Subcommittee	$162.00
JESD 84-B42 	**MultiMediaCard (MMC) Electrical Standard, High Capacity (MMCA, 4.2)** The purpose of the specification is the definition of the eMMC, its environment and handling. It provides guidelines for systems designers. The specification also defines a tool box (a set of macro functions and algorithms) that contributes to reducing design-in costs. July 2007 March 2007 /JC-64.1 Subcommittee	$162.00
JESD 85 	**METHODS FOR CALCULATING FAILURE RATES IN UNITS OF FITS:** This standard establishes methods for calculating failure rates in units of FITs by using data in varying degrees of detail such that results can be obtained from almost any data set. The objective is to provide a reference to the way failure rates are calculated. July 2001 /JC-14.3 Subcommittee	$55.00
JESD 86 	**ELECTRICAL PARAMETERS ASSESSMENT:** This standard is intended to describe various methods for obtaining electrical variate data on devices currently produced on the manufacturing and testing process to be qualified. The intent is to assess the device?s capability to function within the specification parameters over time and the application environment (operating range of temperature, voltage, humidity, input/output levels, noise, power supply stability etc.). August 2001 /JC-14.3 Subcommittee	$38.00
JESD 87 	**STANDARD TEST STRUCTURE FOR RELIABILITY ASSESSMENT OF AlCu METALLIZATIONS WITH BARRIER MATERIALS** This document describes design of test structures needed to assess the reliability of aluminum-copper, refractory metal barrier interconnect systems. This includes any metal interconnect system where a refractory metal barrier or other barrier material prevents the flow of aluminum and/or copper metal ions from moving between interconnect layers. This document is not intended to show design of test structures to assess aluminum or aluminum-copper alloy	

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systems, without barriers to Al and Cu ion movement, nor for Cu only metal systems. Some total interconnect systems might not include barrier materials on all metal layers. The structures in this standard are designed for cases where a barrier material separates two Al or Al alloy metal layers. The purpose of this document is to describe the design of test structures needed to assess electromigration (EM) and stress-induced-void (SIV) reliability of AlCu barrier metal systems.

July 2001 /JC-14.2 Subcommittee $43.00

JESD 88C **DICTIONARY OF TERMS FOR SOLID STATE TECHNOLOGY, Fourth Edition:** This reference for technical writers and educators, manufacturers, and buyers and users of discrete solid state devices is now available. It should aid the technical committees of JEDEC in the avoidance of multiple definitions and reduce the proliferation of redundant definitions. The long-term goal is to include definitions from all JEDEC publications and standards. Even in this fourth edition, that goal has been largely met. Each of the approximately two thousand entries is referenced to its source publication, and an annex listing the names of the source publications and their releases dates is included. All entries were reviewed for punctuation, grammar, and clarity, as well as accuracy, and reworded if such was considered warranted. The purpose of this dictionary is to promote the uniform use of terms, definitions, abbreviations, and symbols throughout the solid state industry.

July 2007 /JC-10 Committee $150.00

JESD 89-1 **SYSTEM SOFT ERROR RATE (SSER) TEST METHOD** This method describes a standard procedure for collecting life test data with respect to soft errors. JESD89-1 is published as an addendum to the existing overall technical content of JESD89. JESD89-1 provides a concise procedure for those in need of collecting system soft error test data for comparative purposes.

June 2004 September 2003 /JC-14.1 Subcommittee $41.00

JESD 89-2 **ADDENDUM NO. 2 to JESD89 - TEST METHOD FOR ALPHA SOURCE ACCELERATED SOFT ERROR RATE (SER)** This method describes a concise, standard procedure for collecting soft error test data on components under exposure to an accelerated source of alpha particles. JESD89-2 is published as an addendum to the existing overall technical content of JESD89.

November 2004 January 2004 /JC-14.1 Subcommittee $43.00

JESD 89-3 **TEST METHOD FOR BEAM ACCELERATED SOFT ERROR RATE** This test is used to determine the terrestrial cosmic ray Soft Error Rate (SER) sensitivity of solid state volatile memory arrays and bistable logic elements (e.g. flip-flops) by measuring the error rate while the device is irradiated in a neutron or proton beam of known flux.

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The results of this accelerated test can be used to estimate the terrestrial cosmic ray induced SER for a given terrestrial cosmic ray radiation environment. This test cannot be used to project alpha-particleinduced SER.

September 2005 January 2005 /JC-14.1 Subcommittee $40.00

JESD 89A **MEASUREMENT AND REPORTING OF ALPHA PARTICLE AND TERRESTRIAL COSMIC RAY INDUCED SOFT ERRORS IN SEMICONDUCTOR DEVICES:** This specification defines the standard requirements and procedures for terrestrial soft-error-rate (SER)testing of integrated circuits and reporting of results. Both real-time (unaccelerated) and acceleratedtesting procedures are described. At terrestrial, Earth-based altitudes, the predominant sources of radiation include both cosmic-ray radiation and alpha-particle radiation from radioisotopic impurities in the package and chip materials. An overall assessment of a device?s SER is complete, only when an unaccelerated test is done, or accelerated SER data for the alpha-particle component and the cosmic-radiation component has been obtained.

October 2006 January 2006 /JC-13.4 Subcommittee $109.00

JESD 90 **A PROCEDURE FOR MEASURING P-CHANNEL MOSFET NEGATIVE BIAS TEMPERATURE INSTABILITIES** This document describes an accelerated stress and test methodology for measuring device parameter changes of a single p-channel MOSFET after Negative Bias Temperature Instability (NBTI) stress at dc bias conditions. This document gives a procedure to investigate NBTI stress in a symmetric voltage condition with the channel inverted (VGS < 0) and no channel conduction (VDS = 0).There can be NBTI degradation during channel conduction (VGS < 0, VDS < 0), however, this document does not cover this phenomena.

November 2004 August 2002 /JC-14.2 Subcommittee $48.00

JESD 91-A **METHOD FOR DEVELOPING ACCELERATION MODELS FOR ELECTRONIC COMPONENT FAILURE MECHANISMS:** The method described in this document applies to all reliability mechanisms associated with electronic components.The purpose of this standard is to provide a reference for developing acceleration models for defect-related and wear-out mechanisms in electronic components.

August 2003 /JC-14.3 Subcommittee $49.00

JESD 92 **PROCEDURE FOR CHARACTERIZING TIME-DEPENDENT DIELECTRIC BREAKDOWN OF ULTRA-THIN GATE DIELECTRICS:** This document defines a constant voltage stress test procedure for characterizing time-dependent dielectric breakdown or ?wear-out? of thin gate dielectrics used in integrated circuit technologies. The test is designed to obtain voltage and temperature acceleration parameters required to estimate oxide life at use conditions. The test procedure includes sophisticated techniques to detect

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breakdown in ultra-thin films that typically exhibit large tunneling currents and soft or noisy breakdown characteristics. This document includes an annex that discusses test structure design, methods to determine the oxide electric field in ultra-thin films, statistical models, extrapolation models, and example failure-rate calculations.

August 2003 July 2002 /JC-14.2 Subcommittee $57.00

JESD 94.01 **APPLICATION SPECIFIC QUALIFICATION USING KNOWLEDGE BASED TEST METHODOLOGY:** The method described in this document applies to all application specific reliability testing for solid state components with known failure mechanisms where the test duration and conditions vary based on application variables. This document does not cover reliability tests that are characterization based or essentially go / no-go type tests, for example, ESD, latch-up, or electrical over stress. Also, it does not attempt to cover every failure mechanism or test environment, but does provide a methodology that can be extended to other failure mechanisms and test environments.

May 2007 This document contains minor editorial changes listed in Annex B. June 2003 /JC-14.3 Subcommittee $49.00

JESD 95-1 **DESIGN REQUIRMENTS FOR OUTLINES OF SOLID STATE AND RELATED PRODUCTS: DISCONTINUED AS A SEPARATE ITEM CONTAINED IN JEP95, BOOK 1, SECTION 4.**

September 2000; Incorporated /JC-11 Committee

JESD 96A **RADIO FRONT END - BASEBAND (RF-BB) INTERFACE** The normative information in this standard is intended to provide a technical design team to construct the interface on a FED and a BED such that they will operate correctly with each other (at the interface level), when designed to this specification. Additional informative information is provided in the appendices to help illustrate the normative material. This document addresses the following interface topics: 1) RF-BB Electrical layer: time and amplitude specifications for lines, drivers, receivers, clocks; 2)RF-BB Link layer: bits, clock-data synchronization, power modes; 3) RF-BB Transport layer: data types, data framing, data bandwidth, connection to core IC; 4) RF-BB Interface Registers. This document defines a high-speed serial link that enables the bi-directional transfer of data and control information between the FED and BED. The document does not mandate the use of specific signaling, standard framing or standard messaging needed to make this an interoperable interface standard for RF devices or BB devices.

February 2006 February 2005 /JC-61 Committee $71.00

JESD 97 **MARKING, SYMBOLS, AND LABELS FOR IDENTIFICATION OF LEAD (Pb) FREE ASSEMBLIES, COMPONENTS, AND DEVICES - SUPERSEDED BY J-STD-609, August 2007**

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May 2004; Superseded by J-STD-609, August 2007 June 2003 /JC-14.1 Subcommittee $45.00

JESD 99-1 **ADDENDUM No. 1 to JESD99 - TERMS, DEFINITIONS, AND LETTER SYMBOLS FOR ANALOG-TO-DIGITAL AND DIGITAL-TO-ANALOG CONVERTERS:** This addendum has now been incorporated into JESD99.

July 1989; Incorporated into JESD99-A, May 2000 /JC-10 Committee

JESD 99B **TERMS, DEFINITIONS, AND LETTER SYMBOLS FOR MICROELECTRONIC DEVICES:** This standard will be useful to users, manufacturers, educators, technical writers, and others interested in the characterization, nomenclature, and classification of microelectronics devices. There are general guidelines for both letter symbols and abbreviations applicable to all integrated circuits, and detailed sections for digital ICs, linear (analog) ICs, interface ICs (including D/A and A/D converters), voltage regulators, charge-transfer devices. The standard lists and defines more than 400 of the most common physical and electrical terms applicable to these devices and shows the industry-standard symbol and abbreviations that have been established for such terms.

May 2007 /JC-10 Committee $127.00

JESD 100B.01 **TERMS, DEFINITIONS, AND LETTER SYMBOLS FOR MICROCOMPUTERS, MICROPROCESSORS, AND MEMORY INTEGRATED CIRCUITS:** A revised reference for technical writers and educators, manufacturers, buyers and users of microprocessors, microcomputers, mircocontrollers, memory ICs, and other complex devices. The terms and their definitions in this standard have been updated and are in general agreement with the latest publications of the IEEE and the IEC. The companion standard for other integrated circuits is JESD99A. Also included is a system for generating symbols for time intervals found in complex sequential circuits, including memories. JESD100B.01 is the first minor revision of JESD100-B, December 1999. Annex A briefly shows entries that have changed.

December 2002 /JC-10 Committee $71.00

JESD 201 **Environmental Acceptance Requirements for Tin Whisker Susceptibility of Tin and Tin Alloy Surface Finished** The methodology described in this document is applicable for environmental acceptance testing of tin based surface finishes and mitigation practices for tin whiskers. This methodology may not be sufficient for applications with special requirements, (i.e., military, aerospace, etc.). Additional requirements may be specified in the appropriate requirements (procurement) documentation.

March 2006 June 2005 /JC-14.3 Subcommittee $55.00

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JESD 202 **Method for Characterizing the Electromigration Failure Time Distribution of Interconnects Under Constant-Current and Temperature Stress** This is an accelerated stress test method for determining sample estimates and their confidence limits of the median-time-to-failure, sigma, and early percentile of a log-Normal distribution, which are used to characterize the electromigration failure-time distribution of equivalent metal lines subjected to a constant current-density and temperature stress. Failure is defined as some pre-selected fractional increase in the resistance of the line under test. Analysis procedures are provided to analyze complete and singly, right-censored failure-time data. Sample calculations for complete and right-censored data are provided in Annex A. The analyses are not intended for the case when the failure distribution cannot be characterized by a single log-Normal distribution.

March 2006 June 2004 /JC-14.2 Subcommittee $61.00

JESD 203 **STANDARD TEST LOADS FOR DUAL-SUPPLY LEVEL TRANSLATION DEVICES** This standard defines ac test loads for dual-supply level translation devices. Uniform test loads enable easy comparison of electrical parameters of dual-supply level translation devices across functions, logic families and IC suppliers. This standard is only intended to apply to devices released subsequent to the publication of this document.

November 2005 June 2004 /JC-40.1 Subcommittee $40.00

JESD 204 **Serial Interface for Data Converters** This specification describes a serialized interface between data converters and logic devices. It contains normative information to enable designers to implement devices that communicate with other devices covered by this specification. Informative sections are included to clarify and exemplify the specification.

April 2006 March 2005 /JC-16 Committee $63.00

JESD 205 **FBDIMM Standard: DDR2 SDRAM Fully Buffered DIMM (FBDIMM) Design Specification** This specification defines the electrical and mechanical requirements for 240-pin, PC2-4200/PC2-5300/PC2-6400, 72 bit-wide, Fully Buffered Double Data Rate Synchronous DRAM Dual In-Line Memory Modules (DDR2 SDRAM FB-DIMMs).These SDRAM FB-DIMMs are intended for use as main memory when installed in systems such as servers and workstations. PC2-4200/PC2-5300/PC2-6400 refers to the DIMM naming convention in which PC2-4200/PC2-5300/PC2-6400 indicates a 240-pin DDR2 DIMM running at 266/333/400 MHz DRAM clock speed and offering 4266/5333/6400 MB/s bandwidth.

March 2007 March 2006 /JC-45.4 Subcommittee $147.00

JESD 206 **FBDIMM Architecture and Protocol**

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January 2007 March 2006 /JC-40 Committee $147.00

JESD 209 **Low Power Double Data Rate (LPDDR) SDRAM Specification**

This document was numbered as JESD79-4 May 2006 to August 2007. The document number has been corrected to JESD209 09/17/2007. The purpose of this Specification is to define the minimum set of requirements for JEDEC compliant 128 Mb through 1 Gb for x16 and x32 Low Power Double Data Rate SDRAM devices. System designs based on the required aspects of this specification will be supported by all LPDDR SDRAM vendors providing compliant devices.

August 2007 June 2005 /JC-42.3 Subcommittee $83.00

JESD 22-A122

POWER CYCLING This Test Method establishes a uniform method for performing component package power cycling stress test. This specification covers power induced temperature cycling of a packaged component, simulating the non-uniform temperature distribution resulting from a device powering on and off in the application.

August 2007 January 2007 /JC-14.1 Subcommittee $47.00

JESD 282B.01

SILICON RECTIFIER DIODES: This standard provided definitions, electrical characteristics circuit technology, letter symbols and registration format for diodes and stacks. It also covers rating and characteristics, manufacturing and performance as well as test practices to demonstrate the performance of semiconductor rectifier diodes and rectifier stacks used for the conversion and/or control of electric power. This version contains minor revisions to JESD282-B, April 2000.

November 2002 /JC-22.2 Subcommittee $177.00

JESD 284-A **TEST METHODS FOR THE COLLECTOR-BASE TIME CONSTANT AND FOR THE RESISTIVE PART OF THE COMMON-EMITTER INPUT IMPEDANCE:** The test methods described in this Standard are generally applicable to alloy-like devices for which the usual simplified equivalent circuits can be employed.


November 1963; Reaffirmed November 1963, June 1972, April 1981, April 1999, October 2002 /JC-25 Committee $38.00

JESD 286-B **STANDARD FOR MEASURING FORWARD SWITCHING CHARACTERISTICS OF SEMICONDUCTOR DIODES:** This method updates the standard procedure for characterizing the switching of signal or switching diodes when a step function of forward current is applied. The objective is to provide a standard so that accurate comparisons can be made.

February 2000 /JC-22.4 Subcommittee $40.00

JESD 307 **VOLTAGE REGULATOR DIODE NOISE VOLTAGE MEASUREMENT:** This


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standard is intended to cover the measurement of noise voltage in voltage regulator diodes in the reverse breakdown region. It describes noise voltage measurements at specified conditions, but may be used as a guide for making such measurements at other than specified conditions.(Formerly EIA-307)

May 1965; Reaffirmed January 1992, April 1999, April 2002 April 2002 /JC-22.4 Subcommittee $38.00

JESD 313-B **THERMAL RESISTANCE MEASUREMENTS OF CONDUCTION COOLED POWER TRANSISTORS:** This standard provides a test method for measuring thermal resistance for conduction cooled power transistors.

October 1975; Reaffirmed April 1981, April 2001 /JC-25 Committee $45.00

JESD 320-A **CONDITIONS FOR MEASUREMENT OF DIODE STATIC PARAMETERS:** This standard provides guidance for achieving equilibrium when measuring temperature sensitive static parameters of signal diodes. (Formerly EIA-302-A)

December 1992; Reaffirmed April 1999, April 2002 (Original publication July 1965) /JC-22.4 Subcommittee $37.00

JESD 381-A **METHOD OF DIODE Q MEASUREMENT:** This standard was updated and revised for the purpose of clarifying the method used to measure Q of a Voltage-Variable-Capacitance Diode in the low VHF range using an RF admittance bridge. Originally published November 1981. Approved as ANSI/EIA-381-A-1992, July 1992. Became JESD381-A after ANSI expiration July 2002.

November 1981; Reaffirmed April 1999, April 2002 April 1999 /JC-22.4 Subcommittee $48.00

JESD 419-A **STANDARD LIST OF VALUES TO BE USED IN SEMICONDUCTOR DEVICE SPECIFICATIONS AND REGISTRATION FORMAT:** This document contains standard lists of values which are recommended for use in semiconductor device specification and JEDEC Registration Formats. Good reasons should exist in those cases where values are used that are not included in these lists.

October 1980; Reaffirmed March 2001 /JC-25 Committee $37.00

JESD 482-A **LIST OF PREFERRED VALUES FOR USE ON VARIOUS TYPES OF SMALL SIGNAL AND REGULATOR DIODES:** This standard specifies preferred values to be used on signal and regulator diodes. It will facilitate the standardization for nominal values used on small signal regulator diodes previously established in JEDEC Suggested Standard No. 2. (Formerly EIA-482-A)

August 1984; Reaffirmed April 1999, April 2002 April 2002 /JC-22.4 Subcommittee $38.00

JESD 51-12 **Guidelines for Reporting and Using Electronic Package**

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Thermal Information This document provides guidelines for both reporting and using electronic package thermal information generated using JEDEC JESD51 standards. By addressing these two areas, this document can be used as the common basis for discussion between electronic package thermal information suppliers and users.

May 2005 October 2004 /JC-15.1 Subcommittee $49.00

JESD 531 **THERMAL RESISTANCE TEST METHOD FOR SIGNAL AND REGULATOR DIODES (FORWARD VOLTAGE, SWITCHING METHOD):** This standard describes a test method for measuring the thermal resistance of signal and regulator diodes. The need for modification of this test method arose out of the limited description that existed earlier for both signal and regulator diode applications in testing for thermal resistance. Previously published as ID-13. ANSI/EIA-531-1986 (July) expired June 1996. Became JESD531 after reaffirmation April 2002.

July 1986; Reaffirmed April 1999, April 2002 April 1999 /JC-22.4 Subcommittee $47.00

JESD 625-A **REQUIREMENTS FOR HANDLING ELECTROSTATIC-DISCHARGE-SENSITIVE (ESDS) DEVICES:** This standard establishes the minimum requirements for Electrostatic Discharge (ESD) control methods and materials used to protect electronic devices that are susceptible to damage or degradation from electrostatic discharge (ESD). The passage of a static charge through an electrostatic-discharge-sensitive (ESDS) device can result in catastrophic failure or performance degradation of the part. Device sensitivity to ESD is determined by test methods such as EIA/JESD22-A114. ESDS devices with human body model sensitivities of less than +200 volts may need additional protective measures beyond those specified in this standard.

December 1999 /JC-14.1 Subcommittee $55.00

JESD 659B **FAILURE-MECHANISM-DRIVEN RELIABILITY MONITORING:** This method establishes requirements for application of Statistical Reliability Monitoring 'SRM' technology to monitor and improve the reliability of electronic components and subassemblies. The standard also describes the condition under with a monitor may be replaced or eliminated.

February 2007 September 2006 /JC-14.3 Subcommittee $45.00

JESD 671-A **COMPONENT QUALITY PROBLEM ANALYSIS AND CORRECTIVE ACTION REQUIREMENTS (INCLUDING ADMINISTRATIVE QUALITY PROBLEMS):** This revision now encompasses administrative quality problems, in addition to the electrical and visual/mechanical quality problems that were addressed in the original release. A standard set of problem categories for each of these three types of component problems is presented for tracking and reporting purposes. A

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common set of customer and supplier expectations and requirements are set forth to help facilitate the successful problem analysis and corrective action of any type of component quality problem.

December 1999 /JC-14.4 Subcommittee $43.00

JESD 8-19 **POD18 - 1.8 V Pseudo Open Drain I/O** This standard defines the dc and ac single-ended (data) and differential (clock) operating conditions, I/O impedances, and the termination and calibration scheme for 1.8 V Pseudo Open Drain I/Os. The 1.8 V Pseudo Open Drain interface, also known as POD18, is primarily used to communicate with GDDR3 SGRAM devices.

December 2006 December 2003 /JC-16 Committee $43.00

JESD 8-20 **POD15 - 1.5 V Pseudo Open Drain I/O** This standard defines the dc and ac single-ended (data) and differential (clock) operating conditions, I/O impedances, and the termination and calibration scheme for 1.5 V Pseudo Open Drain I/Os. The 1.5 V Pseudo Open Drain interface, also known as POD15, is primarily used to communicate with GDDR4 SGRAM devices.

December 2006 March 2006 /JC-16 Committee $43.00

JESD 82-8.01 **STANDARD FOR DEFINITION OF ?CU877 PLL CLOCK DRIVER FOR REGISTERED DDR2 DIMM APPLICATIONS** This standard defines standard specifications of dc interface parameters, switching parameters, and test loading for definition of a ?CU877 PLL clock device for registered DDR2 DIMM applications. The purpose is to provide a standard for a ?CU877 PLL clock device, for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use. This document includes minor editorial changes as noted in Annex A, page 16.

February 2004 /JC-40 Committee $49.00

JESD 93 **Hybrids/MCM** This specification establishes the general requirements for hybrid microcircuits, RF/microwave hybrid microcircuits and MCMs (hereafter referred to as devices). Detailed performance requirements for a specific device are specified in the applicable device acquisition document. In the event of a conflict between this document and the device acquisition document, the device acquisition document will take precedence.

September 2005 May 2002 /JC-13.5 Subcommittee $49.00

JESD 96A-1 **Addendum 1 to JESD96A - INTEROPERABILITY AND COMPLIANCE TECHNICAL REQUIREMENTS FOR JEDEC STANDARD JESD96A - RECOMMENDED PRACTICE FOR USE WITH IEEE 802.11N** The normative information in this publication is intended to provide a technical design team to construct the interface on a FED and a

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BED such that they will operate correctly with each other (at the interface level), when designed to JESD96A.

January 2007 March 2006 /JC-61 Committee $45.00

JESD JIG-101

Material Composition Declaration Guide for Electronic Products The purpose of this guide establishes the materials and substances to be disclosed by suppliers when those materials and substances are present in products and subparts that are incorporated into EEE. It benefits suppliers and their commercial customers by providing consistency and efficiency to the material declaration process. It promotes the development of consistent data exchange formats and tools that will facilitate and improve data transfer along the entire global supply chain.

June 2005 January 2003 /JC-14 Committee

NUMBER Joint IPC/JEDEC Standards (J-STD-) PRICE

J-STD-002B

SOLDERABILITY TESTS FOR COMPONENT LEADS, TERMINATIONS, LUGS, TERMINALS AND WIRES: At the request of IPC, J-STD-002B has been temporarily removed from the free download area until such time when it is revised to include lead-free. In its place, JEDEC's Test Method B102-D, Solderability, which includes lead-free, is available for free downloading.

February 2003 Removed 01/21/04 /JC-14.1 Subcommittee

J-STD-020D

JOINT IPC/JEDEC STANDARD FOR MOISTURE/REFLOW SENSITIVITY CLASSIFICATION FOR NONHERMETIC SOLID STATE SURFACE-MOUNT DEVICES: This document identifies the classification level of nonhermetic solid-state surface mount devices (SMDs) that are sensitive to moisture-induced stress. It is used to determine what classification level should be used for initial reliability qualification. Once identified, the SMDs can be properly packaged, stored and handled to avoid subsequent thermal and mechanical damage during the assembly solder reflow attachment and/or repair operation. This revision now covers components to be processed at higher temperatures for lead-free assembly. A hard cop version is available for $20 each for IPC/JEDEC members and $40 for nonmembers.

June 2007; Under Revision This document has some minor editorial changes, some notes are misplaced and will be relocated by 08/24/2007. September 2006 /JC-14.1 Subcommittee

J-STD-033B.1

JOINT IPC/JEDEC STANDARD FOR HANDLING, PACKING, SHIPPING AND USE OF MOISTURE/REFLOW SENSITIVE SURFACE-MOUNT DEVICES: NOTE - The Moisture Sensitive Caution Label (figure 3-4) has been editorially revised since originally posted 11/04/05, if you downloaded this file prior to 12/14/05 please download this revised version. This document provides SMD manufacturers and users with standardized methods for handling, packing, shipping and use of moisture/reflow sensitive SMDs. Now updated to support components that may need

to be processed at higher temperatures, such as lead-free processes, these methods help avoid damage from moisture absorption and exposure to solder reflow temperatures that can result in yield and reliability degradation. IPC/JEDEC J-STD-033B helps achieve safe and damage-free reflow with the dry packing process and provides a minimum shelf life of 12 months from the seal date when using sealed dry bags.

January 2007 October 2004 /JC-14.1 Subcommittee

J-STD- 035 JOINT IPC/JEDEC STANDARD FOR ACOUSTIC MICROSCOPY FOR NONHERMETRIC ENCAPSULATED ELECTRONIC COMPONENTS: This test method defines the procedures for performing acoustic microscopy on non-hermetic encapsulated electronic components. This method provides users with an acoustic microscopy process reflow for detecting defects non-destructively in plastic packages while achieving reproducibility.

May 1999; Under Revision /JC-14.1 Subcommittee $35.00

J-STD- 609 MARKING AND LABELING OF COMPONENTS, PCBs AND PCBAs TO IDENTIFY LEAD (Pb), Pb-FREE AND OTHER ATTRIBUTES This standard applies to boards/assemblies, to identify the type of Pb-free or Pb-containing solder used. This standard documents a method for identifying board surface finishes and Printed Circuit Board (PCB) resin systems. This standard applies to PCB base materials and for marking the type of conformal coating utilized on Printed Circuit Board Assemblies (PCBAs). Material and their containers previously marked or labeled according to JESD 97 or IPC-1066 need not be remarked unless agreed upon by the supplier and customer.

May 2007 January 2007 /JC-14.4 Subcommittee

NUMBER Joint Publication (JP) PRICE

JP 001.01 FOUNDRY PROCESS QUALIFICATION GUIDELINES (Wafer Fabrication Manufacturing Sites) This document provides a guideline for the minimum set of measurements to qualify a new semiconductor wafer process. It is written with particular reference to a generic silicon based CMOS logic technology. While it may be applicable to other technologies (e.g. analog CMOS, bipolar, BICMOS, GaAs, etc.), some sections apply specifically to CMOS. No effort was made in the present document to cover all the qualification requirements for specific other technologies, e.g. Cu/Low K interconnects or ultra thin gate oxide. This publication, is co-sponsored by JEDEC JC-14.2 and the FSA (Fabless Semiconductor Association). It originated at the FSA as a technology specific document, and has evolved into a generic set of qualification requirements.

May 2004 /JC-14.2 Subcommittee $67.00

JP 002 CURRENT TIN WHISKERS THEORY AND MITIGATION PRACTICES

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GUIDELINE This document will provide insight into the theory behind tin whisker formation as it is known today and, based on this knowledge, potential mitigation practices that may delay the onset of, or prevent tin whisker formation. The potential effectiveness of various mitigation practices will also be briefly discussed. References behind each of the theories and mitigation practices are provided.

March 2006 June 2005 /JC-14.1 Subcommittee $55.00

NUMBER	Joint Standard (JS)	PRICE

JS 9702 **MONOTONIC BEND CHARACTERIZATION OF BOARD-LEVEL INTERCONNECTS (IPC/JEDEC-9702)** This publication specifies a common method of establishing the fracture resistance of board-level device interconnects to flexural loading during non-cyclic board assembly and test operations. Monotonic bend test qualification pass/fail requirements are typically specific to each device application and are outside the scope of this document.

June 2004 September 2003 /JC-14.1 Subcommittee

JS 9704 **Printed Wiring Board (PWB) Strain Gage Test Guideline** This document describes specific guidelines for strain gage testing for Printed Wiring Board (PWB)assemblies. The suggested procedures enables board manufacturers to conduct required strain gage testing independently, and provides a quantitative method for measuring board flexure, and assessing risk levels. The topics covered include: Test setup and equipment; requirements; Strain measurement; Report format

June 2005 January 2005 /JC-14.1 Subcommittee

NUMBER	JEDEC Publications (JEP)	PRICE

JEP 64 **SOLID STATE PRODUCTS REGISTRATION LIST(ORDER FROM TYPE ADMINISTRATION OFFICE):** This publication includes addenda from 1976 to August 1986. The purpose of this list is to determine release numbers (file numbers) for JEDEC Type Designations. (See page 6 for more information.)

September 1986; Reaffirmed November 2002 / Committee!33JCJEDC $162.00

JEP 65 **TEST PROCEDURES FOR VERIFICATION OF MAXIMUM RATINGS OF POWER TRANSISTORS:** This publication describes tests which are intended to represent the verification of maximum ratings for data sheets; they are not tests for performance or quality level. This material is to be used in conjunction with formats developed for device registration and defining data.

December 1967; Reaffirmed September 1981, April 1999 /JC-25 Committee $52.00

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JEP 69-B **PREFERRED LEAD CONFIGURATION FOR FIELD-EFFECT TRANSISTORS:** This publication indicates preferred pinouts for FETs in various package designs.

November 1973; Reaffirmed September 1981, April 1999 /JC-25 Committee $38.00

JEP 70-B **QUALITY AND RELIABILITY STANDARDS AND PUBLICATIONS:** Contains a listing and description of commonly used quality and reliability related standards and publications that are applicable to the semiconductor industry. It is intended to be a reference aid in finding available standards and obtaining a copy from the source of the standard. It is not intended to recommend or imply the applicability of any standard for a specific purpose. This revision has been updated to include recent releases as well as revisions, in addition, URLs have been added to the

October 1999 /JC-14.4 Subcommittee $57.00

JEP 74 **STANDARD LIST OF VALUES TO BE USED IN POWER TRANSISTOR DEVICE REGISTRATION AND MINIMUM DIFFERENCES FOR DISCRETENESS OF REGISTRATIONS - SUPERSEDED BY EIA-419-A, February 1996.**

July 1969; Rescinded February 1996 /JC-25 Committee $38.00

JEP 75 **LETTER SYMBOLS USED WITH INFRARED DEVICES - INCORPORATED INTO JESD77-A.**

August 1984; Rescinded August 1984 /JC-10 Committee

JEP 78 **RELATIVE SPECTRAL RESPONSE CURVES FOR SEMICONDUCTOR INFRARED DETECTORS:** The intent of this publication is to facilitate the specification of infrared detector diodes, particularly in conjunction with the preparation of data for JEDEC type registration.

October 1969 /JEDEC Committee $52.00

JEP 79 **LIFE TEST METHODS FOR PHOTOCONDUCTIVE CELLS:** This publication is for photoconductive cells sensitive primarily in the visible and near infrared region.

September 1969 $52.00

JEP 84A **RECOMMENDED PRACTICE FOR MEASUREMENT OF TRANSISTOR LEAD TEMPERATURE:** This publication covers recommended methods for measurement of transistor lead temperatures under various load conditions. The techniques described are sufficiently accurate for most applications.

June 2004 September 2002 /JC-25 Committee $41.00

JEP 86-A **RECOMMENDED PRACTICE FOR DUAL DIMENSIONING**

May 1976; Rescinded November 1999 /JC-11 Committee

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JEP 87 **FORWARD TURN-ON TIME MEASUREMENT ON SEMI-DIODES - INCORPORATED INTO EIA-282-A.**

June 1992; Rescinded June 1985 /JC-22.2 Subcommittee

JEP 88 **THERMAL RESISTANCE AND THERMAL IMPEDANCE TEST METHODS FOR STUD AND BASE-MOUNTED RECTIFIER DIODES AND THYRISTORS**

January 1974; Rescinded June 1992 /JC-22.1 Subcommittee

JEP 90 **THERMAL RESISTANCE FOR TEST METHODS FOR SIGNAL DIODES - SUPERSEDED BY EIA-531, July 1986. See JESD531, April 2002.**

September 1983; Rescinded September 1986 /JC-22.4 Subcommittee

JEP 93 **MICROELECTRONIC DEVICE TYPE ASSIGNMENTS**

August 1975; Rescinded June 1992 June 1992 / Committee!33JCJEDC

JEP 95 **JEDEC REGISTERED AND STANDARD OUTLINES FOR SOLID STATE AND RELATED PRODUCTS:** This publication is a compilation of some 1800 pages of outline drawings for microelectronic packages including transistors, diodes, DIPS, chip carriers and package interface BGA outlines in both inch and metric versions.

January 2000 /JC-11 Committee $350.00

JEP 95 AUS **ANNUAL UPDATING SERVICE:** Subscription to this updating service is available from the JEDEC Office. New outlines are shipped to subscribers for insertion into the appropriate sections of Publication No. 95. JEP95 and Updating Service can be ordered through JEDEC at (703)907-7540 or ptanner@jedec.org.

January 2000 /JC-11 Committee $110.00

JEP 96 **GUIDELINES FOR NONDESTRUCTIVE PULL TESTING OF WIRE BONDS ON HYBRID DEVICES**

March 1977; Rescinded April 2000 /JC-13.5 Subcommittee

JEP 99 **GLOSSARY OF MICROELECTRONIC TERMS, DEFINITIONS, AND SYMBOLS: ELEVATED TO JESD99, June 1985.**

July 1977; Rescinded June 1985 /JC-10 Committee

JEP 100 **TERMS, DEFINTIONS, AND LETTER SYMBOLS FOR MICROCOMPUTERS AND MEMORY INTEGRATED CIRCUITS: ELEVATED TO JESD100, August 1993.**

September 1979; Rescinded October 1983 /JC-10 Committee

JEP 101-C **JEDEC REQUIREMENTS FOR CLASS B MICROCIRCUITS: RESCINDED, May 2006**

November 1995; Rescinded May 2006 /JC-13.2 Subcommittee $38.00

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JEP 102 **STANDARD FOR 64K x 1 DYNAMIC RAM - SUPERSEDED BY JESD21-C.**

September 1978; Rescinded April 1985 April 1985 /JC-42 Committee

JEP 103A **SUGGESTED PRODUCT-DOCUMENTATION, CLASSIFICATIONS, AND DISCLAIMERS** In order to improve understanding between manufacturers and users, a consistent set of product-documentation classifications associated with the stages of product development.

July 1996; Reaffirmed November 1999, May 2003 /JC-10 Committee $38.00

JEP 104C.01 **REFERENCE GUIDE TO LETTER SYMBOLS FOR SEMICONDUCTOR DEVICES:** This publication provides a quick reference to the letter symbols and corresponding terms that are defined in JESD77-B, Terms, Definitions, and Letter Symbols for Discrete Semiconductor and Optoelectronic Devices; JESD99-A, Terms, Definitions, and Letter Symbols for Microelectronic Devices, and JESD100-B, Terms, Definitions, and Letter Symbols for Microcomputers, Microprocessors, and Memory Integrated Circuits. It is intended to simplify interpretation of data sheets and specifications and to promote the uniform use of these symbols. The symbols relate to ratings and characteristics found in data sheets and other specifications. Some abbreviations used in lieu of symbols are also included. The newly added Annex B is provided as an aid to determining what symbol should be used and is organized by term, whereas the main body of the publication is organized by symbol or abbreviation as in previous versions. This version contains minor revisions.

May 2003 /JC-10 Committee $91.00

JEP 105 **JEDEC GUIDELINE FOR THE CHARACTERIZATION OF HYBRID POLYMERIC MATERIALS - SUPERSEDED BY JESD72, June 2001**

April 1983; Rescinded June 2001 /JC-13.5 Subcommittee

JEP 106W **STANDARD MANUFACTURERS IDENTIFICATION CODE:** The manufacturers identification code is defined by one or more 8 bit fields, each consisting of 7 data bits plus 1 odd parity bit. The manufacturers identification code is assigned, maintained and updated by the JEDEC Office. The intent of this identification code is that it may be used whenever a digital field is required, e.g., hardware, software, documentation, etc. To make a request for an ID Code please go to http://www.jedec.org/Home/MIDCODE_request.cfm

May 2007 NOTE: JEP106U was in error starting with bank two an additional continuation code was added. This has been corrected, JEP106U should be discarded. /JC-42.3 Subcommittee $52.00

JEP 107 **TEST METHOD FOR QUALIFICATION AND ACCEPTANCE OF PARTICLE GETTERS FOR USE IN HYBRID MICROELECTRONIC APPLICATIONS -**

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SUPERSEDED BY JESD72, June 2001

April 1985; Rescinded June 2001 /JC-13.5 Subcommittee

JEP 108-B **DISTRIBUTOR REQUIREMENTS FOR HANDLING ELECTROSTATIC - DISCHARGE SENSITIVE (ESDS) DEVICES: SUPERSEDED BY JESD42, March 1994.**

April 1991; Superseded /JC-14.1 Subcommittee

JEP 109-C **GENERAL REQUIREMENTS FOR DISTRIBUTORS OF MILITARY SEMICONDUCTOR DEVICES:** Superseded by JESD31-A, June 2001.

March 1995; Rescinded November 2001 /JC-13 Committee

JEP 110 **GUIDELINES FOR THE MEASUREMENT OF THERMAL RESISTANCE OF GaAs FETS:** This publication is intended for power GaAs FET applications requiring high reliability. An accurate measurement of thermal resistance is extremely important to provide the user with knowledge of the FETs operating temperature so that more accurate life estimates can be made. FET failure mechanisms and failure rates have, in general, an exponential dependence on temperature (which is why temperature-accelerated testing is successful). Because of the exponential relationship of failure rate with temperature, the thermal resistance should be referenced to the hottest part of the FET.

July 1988 /JC-14.7 Subcommittee $43.00

JEP 111 **TEST PROCEDURES FOR CUSTOM MONOLITHIC MICROCIRCUITS - SUPERSEDED BY MIL-PRF-38535C.**

July 1986; Rescinded June 1996 June 1996 /JC-13.2 Subcommittee

JEP 112 **TEST METHOD FOR QUALIFICATION AND ACCEPTANCE OF CIRCUIT SUPPORT FILMS FOR USE IN MICROELECTRONIC APPLICATIONS - SUPERSEDED BY JESD72, June 2001**

June 1987; Rescinded June 2001 /JC-13 Committee $52.00

JEP 113-B **SYMBOL AND LABELS FOR MOISTURE-SENSITIVE DEVICES:** Certain PSMC (Plastic Surface-mount Components) are subject to permanent damage due to moisture-induced failures encountered during high-temperature surface-mount processing unless appropriate precautions are observed. The purpose of this publication is to provide a distinctive symbol and labels to be used to identify those devices that require special packing and handling precautions.

May 1999 /JC-14.1 Subcommittee $45.00

JEP 114 **GUIDELINES FOR PARTICLE IMPACT NOISE DETECTION (PIND) TESTING, OPERATOR TRAINING, AND CERTIFICATION:** This publication was developed to help the user of this test methodology avoid common interferenceÆs to successful application. The guide

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contains sections on typical specification requirements, sources of particles, PIND test systems, calibration, maintenance, test interference's, operator training, particle recovery and failure analysis. Application of the information contained in the guide will improve the quality and affectivity for any PIND testing operation.

December 1989; Under Revision /JC-13 Committee $61.00

JEP 115

POWER MOSFET ELECTRICAL DOSE RATE TEST METHOD: The purpose of this Test Method is to establish electrical criteria for comparing and specifying power MOSFET performance under high dose rate radiation.

August 1989; Reaffirmed April 1999 /JC-25 Committee $41.00

JEP 116

CMOS SEMICUSTOM DESIGN GUIDELINES: The design of ASIC circuits is becoming a significant part of system or product design, yet many problems continue to exist in current design practice. The guidelines in this document provide an explanation of common ASIC design problems and concerns and where possible offer solutions.

November 1991 / Committee!33JC44 $109.00

JEP 117

GUIDELINES FOR USER NOTIFICATION OF PRODUCT/PROCESS CHANGES BY SEMICONDUCTOR SUPPLIERS - SUPERSEDED BY JESD46, August 1997.

April 1994; Rescinded July 1994 /JC-14.4 Subcommittee

JEP 118

GUIDELINES FOR GaAs MMIC AND FET LIFE TESTING: These guidelines apply to monolithic microwave GaAs integrated circuits (MMICs) and their individual component building blocks, such as GaAs field effect transistors (FETs), resistors, and capacitors. The purpose of this document is to define a standard approach for evaluating the expected live of GaAs MMICs so that results from different life tests can be compared and so that wording of this document that the MMIC contains at least one FET, but the use of this document has no such limitation.

January 1993 /JC-14.7 Subcommittee $48.00

JEP 119A

A PROCEDURE FOR EXECUTING SWEAT: This document describes an algorithm for performing the Standard Wafer Level Electromigration Accelerated Test (SWEAT) method with computer controlled instrumentation. The algorithm requires a separate iterative technique (not provided) to calculate the force current for a given target time to failure. This document does not specify what test structure to use with this procedure. However, users of this algorithm report its effectiveness on both straight-lines and via-terminated test structures. Some test-structures design features are provided in JESD87 and in ASTM 1259M - 96.

August 2003 /JC-14.2 Subcommittee $57.00

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JEP 120-A **INDEX OF TERMS DEFINED IN JEDEC PUBLICATIONS:** This publication provides an index to terms that are defined in certain JEDEC publications. It is intended to promote the uniform use of these terms and their definitions while reducing the proliferation of new definitions for old terms.

May 2000 /JC-10 Committee $109.00

JEP 121A **REQUIREMENTS FOR MICROELECTRONIC SCREENING AND TEST OPTIMIZATION:** The purpose of this document provides the basis for the optimization of 100% screening/stress operations and sample inspection test activities. This document is designed to assist the manufacturer in optimizing the test flow while maintaining and/or improving assurance of providing high quality and reliable product in an efficient manner. This will allow for optimization of testing that is not adding value, hence, reducing cycle time and costs.

October 2006 May 2006 /JC-13.2 Subcommittee $59.00

JEP 122C **FAILURE MECHANISMS AND MODELS FOR SILICON SEMICONDUCTOR DEVICES:** This publication provides a list of failure mechanisms and their associated activation energies or acceleration factors that may be used in making system failure rate estimations when the only available data is based on tests performed at accelerated stress test conditions. The method to be used is the Sum of the Failure Rates method.

March 2006 June 2005 /JC-14.1 Subcommittee $63.00

JEP 123 **GUIDELINE FOR MEASUREMENT OF ELECTRONIC PACKAGE INDUCTANCE AND CAPACITANCE MODEL PARAMETERS:** The need for this guideline arose from widespread lack of consistency in characterizing electrical parameters of electronic packages, which existed in the industry until the early 1990s. Then, the JEDEC Committee JC-15 provided the forum where various methods were discussed and commonality in approach emerged. The result is that today we have relatively consistent results in measuring and reporting electrical package parameters, as well as specialized tools (e.g., the IPA-510, the interconnect parameter analyzer) which were developed to support the methodology.

October 1995 /JC-15.2 Subcommittee $49.00

JEP 124 **GUIDELINES FOR THE PACKING, HANDLING, AND REPACKING OF MOISTURE-SENSITIVE COMPONENTS - SUPERSEDED BY J-STD-033, May 1999.**

December 1995; Rescinded November 1999 November 1999 /JC-14.4 Subcommittee

JEP 126 **GUIDELINE FOR DEVELOPING AND DOCUMENTING PACKAGE ELECTRICAL MODELS DERIVED FROM COMPUTATIONAL ANALYSIS:** This publication provides a guideline to suppliers of IC components

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with a template for documenting the numerical simulation assumptions. In addition this guideline also suggests a model environment to reference when comparing various packages or component suppliers. This publication should improve the communication between the package model suppliers. This publication should improve the communication between the package model supplier and the end user.

May 1996 /JC-15.2 Subcommittee $38.00

JEP 128 **GUIDE FOR STANDARD PROBE PAD SIZES AND LAYOUTS FOR WAFER LEVEL ELECTRICAL TESTING:** This guide was developed to expedite inter-laboratory experiments used to evaluate or develop standard test methods that involve test-structure measurements or tests. It also facilitates, generally, any electrical tests that require wafer-probe card to make electrical contact to test structures. Widespread use of this guide will afford the efficient and cost-effective use of water-probe test stations because of the need for fewer probe cards and probe-card changes to accommodate the various test structures that may need to be tested.

November 1996 /JC-14.2 Subcommittee $40.00

JEP 129 **THERMAL TEST CHIP GUIDELINE (WIRE BOND TYPE CHIP)- SUPERSEDED BY JESD51-4, September 1997.**

February 1997; Elevated September 1997 /JC-15.1 Subcommittee

JEP 130A **GUIDELINES FOR PACKING AND LABELING OF INTEGRATED CIRCUITS IN UNIT CONTAINER PACKING:** This document establishes guidelines for integrated circuit unit container and the next level (intermediate) container packing and labeling. The guidelines include tube/rail standardization, intermediate packing, date codes, tube labeling, intermediate container and shipping labels, and standardize tube quantities. Future revisions of this document will also include tray and reel guidelines. The objective of this publication is to promote the standardization of practices between manufacturers and distributors resulting in improved efficiency, profitability, and product quality.

February 2006 January 2005 /JC-14.4 Subcommittee $43.00

JEP 131A **PROCESS FAILURE MODE AND EFFECTS ANALYSIS (FMEA):** This publication was created in response to the need for a straight forward FMEA procedure. The objective is to provide a guideline for the application of FMEA techniques to improve quality, reliability and/or consistency of electronic components and subassemblies by continually evaluating processes/products against potential failure modes.

May 2005 October 2004 /JC-15.1 Subcommittee $55.00

JEP 132 **PROCESS CHARACTERIZATION GUIDELINE:** This guideline provides a methodology to characterize a new or existing process and is

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applicable to any manufacturing or service process. It describes when to use specific tools such as failure mode effects analysis (FEMA), design or experiments (DOE), measurement system evaluation (MSE), capability analysis (CpK), statistical process control (SPC), and problem solving tools. It also provides a brief description of each tool. In December 2004 the document was renumbered to conform with JM7, JEDEC Style Manual.

July 1998; Reaffirmed September 2003 /JC-13 Committee $59.00

JEP 133B 

GUIDE FOR THE PRODUCTION AND ACQUISITION OF RADIATION-HARDNESS ASSURED MULTICHIP MODULES AND HYBRID MICROCIRCUITS: A revised and expanded publication for suppliers and users of radiation hardness assured (RHA) multichip modules (MCMs) and hybrid microcircuits, is now available. Revision A of JEP133 includes modifications to the introduction, clarification of a definition and clarification of several technical issues within the document. In addition, the Bibliography section was updated to include added references. The document provides guidance as to how to achieve, maintain and ensure required levels of radiation-hardness given the fact that the constituent dice can have different levels of hardness assurance. It also describes how to deal with the various radiation hardness situations that an MCM/Hybrid developer, procuring activity or user will encounter. The guide is intended to supplement three relevant performance specifications: MIL-PRF-38534, MIL-PRF-38535 and MIL-PRF-19500.

March 2005 September 2003 /JC-13.5 Subcommittee $59.00

JEP 134 

GUIDELINES FOR PREPARING CUSTOMER-SUPPLIED BACKGROUND INFORMATION RELATING TO A SEMICONDUCTOR-DEVICE FAILURE ANALYSIS: The purpose of this Guideline is to provide a vehicle for acquiring and transmitting the necessary information in a concise, organized, and consistent format. Included in the Guideline is a sample form that facilitates transferring the maximum amount of background data to the failure analyst in a readily interpretable format. Immediate availability of this key information assists that analyst in completing a timely and accurate failure analysis.

September 1998 /JC-14.6 Subcommittee $45.00

JEP 136 

SIGNATURE ANALYSIS: Signature Analysis is a method to reduce the number of comprehensive physical failure analyses by the application of statistical inference techniques. The purpose of this document is to promote a common definition of Signature Analysis by inference, using the same statistical techniques, and to recognize that it is formal means of doing failure analysis.

July 1999 /JC-14.6 Subcommittee $47.00

JEP 137B 

COMMON FLASH INTERFACE (CFI) IDENTIFICATION CODES: This publication is a companion document to the Common Flash Interface (CFI) standard, JESD68, which outlines the device and

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host system software interrogation handshake. JEP137 documents ID Code assignments for: 1)) the Algorithm-specific Command Set and Control Interfaces and 2) the Device Interfaces. It is published as needed when additions are made to either of these lists of codes. To make a request for an ID Code please contact the JEDEC Office at (703)907-7558.

May 2004 /JC-42.4 Subcommittee $41.00

JEP 138 **USER GUIDELINES FOR IR THERMAL IMAGING DETERMINATION OF DIE TEMPERATURE:** The purpose of these user guidelines is to provide background and an example for the use of an infrared (IR) microscope to determine die temperature of electronic devices for calculations such as thermal resistance.

September 1999 /JC-25 Committee $41.00

JEP 139 **GUIDELINE FOR CONSTANT TEMPERATURE AGING TO CHARACTERIZE ALUMINUM INTERCONNECT METALLIZATIONS FOR STRESS-INDUCED VOIDING:** This document describes a constant temperature (isothermal) aging method for testing aluminum (Al) metallization test structures on microelectronics wafers for susceptibility to stress-induced voiding. This method is valid for metallization/dielectric systems in which the dielectric is deposited onto the metallization at a temperature considerably above the intended use temperature, and above or equal to the deposition temperature of the metal. Although this is a wafer test, it is not a fast (less than 5 minutes per probe) test. It is intended to be used for lifetime prediction and failure analysis, not for production Go-NoGo lot checking.

December 2000 /JC-14.2 Subcommittee $47.00

JEP 140 **BEADED THERMOCOUPLE TEMPERATURE MEASUREMENT OF SEMICONDUCTOR PACKAGES:** The beaded thermocouple temperature measurement guideline provides a procedure to accurately and consistently measure the temperature of semiconductor packages during exposure to thermal excursions. The guideline applications can include, but not limited to, temperature profile measurement in reliability test chambers and solder reflow operations that are associated with component assembly to printed wiring boards.

June 2002; Reaffirmed June 2006 /JC-14.1 Subcommittee $43.00

JEP 142 **GUIDELINE FOR OBTAINING AND ACCEPTING MATERIAL FOR USE IN HYBRID / MCM PRODUCTS:** This document provides guidance regarding design considerations, material assessment techniques, and recommendations for material acceptance prior to use in Hybrid / MCM Products. As part of the risk assessment process, both technical requirements and cost should be carefully considered with regard to testing / evaluating the elements of a hybrid microcircuit or Multi-chip Module (MCM) prior to material release for assembly. The intent of this document is to highlight

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various options that are available to the Hybrid / MCM manufacturer and provide associated guidance, not to impose a specific set of tests.

May 2002 /JC-13.5 Subcommittee $55.00

JEP 143A **SOLID STATE RELIABILITY ASSESSMENT QUALIFICATION METHODOLOGIES:** The purpose of this publication is to provide an overview of some of the most commonly used systems and test methods historically performed by manufacturers to assess and qualify the reliability of solid state products. The appropriate references to existing and proposed JEDEC (or EIA) standards and publications are cited. This document is also intended to provide an educational background and overview of some of the technical and economic factors associated with assessing and qualifying microcircuit reliability.

May 2004 /JC-14.3 Subcommittee $52.00

JEP 144 **GUIDELINE FOR RESIDUAL GAS ANALYSIS (RGA) FOR MICROELECTRONIC PACKAGES** The intent of this document is to give guidance on the Residual Gas Analysis (RGA) process and surrounding issues. The guideline describes how to select a suitable test lab and includes RGA history, measurement methodology, and issues that arise with the test. Interpreting the lab results along with common failure mechanisms are discussed at length along with process controls and alternative test techniques for measuring the moisture content within packages.

July 2002 /JC-13 Committee $57.00

JEP 145 **GUIDELINE FOR ASSESSING THE CURRENT-CARRYING CAPABILITY OF THE LEADS IN A POWER PACKAGE SYSTEM:** This publication is intended as a guideline to establish procedures, consideration and common practices that will allow a manufacturer, an application entity, a system designer and other interested parties to define current capability limitations in the leads of components and power systems with semiconductor components. This is a guideline, not a standardized method, it was developed over several years to clarify questions that had been posed to committee members in their respective engineering functions.

February 2003 /JC-25 Committee $41.00

JEP 146 **GUIDELINES FOR SUPPLIER PERFORMANCE RATING:** The intent of this document is to establish guidelines and provide examples by which customers can measure their suppliers based on mutually agreed upon objective criteria. These results can then be used to improve communications between customers and suppliers.

June 2003 September 2002 /JC-14.4 Subcommittee $47.00

JEP 147 **PROCEDURE FOR MEASURING INPUT CAPACITANCE USING A VECTOR**

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NETWORK ANALYZER (VNA): This procedure describes a recommended way to measure pin capacitance of devices with SSTL (Stub Series Terminated Logic) interface pins by use of a Vector Network Analyzer. One purpose of this standard procedure is to reduce the lengthy and often inaccurate footnote - usually found around the specification of pin parasitics - to a simple reference to this document. In special cases modifying statements may adjust this procedure to the special needs of certain component.

October 2003 December 2002 / Committee!33JC162 $41.00

JEP 148

Reliability Qualification of Semiconductor Devices Based on Physics of Failure Risk and Opportunity Assessment A concept is outlined, which proactively integrates qualification into the development process and provides a systematic procedure as support tool to development and gives early focus on required activities. It converts requirements for a product into measures of development and qualification in combination with a risk and opportunity assessment step and accompanies the development process as guiding and recording tool for advanced quality planning and confirmation. The collected data enlarge the knowledge database for DFR / BIR (design for reliability / building-in reliability) to be used for future projects. The procedure challenges and promotes teamwork of all involved disciplines. Based on the Physics-of-Failure (PoF) concept the reliability qualification methodology is re-arranged with regard to the relationships between design, technology, manufacturing and the different product life phases at use conditions. It makes use of the Physics-of-Failure concept by considering the potential individual failure mechanisms and relates most of the reliability aspects to the technology rather than to the individual product design. Evaluation of complex products using common reliability models and definition of sample sizes with respect to systematic inherent product properties and fractions of defects are discussed.

April 2004 January 2003 /JC-14.3 Subcommittee $63.00

JEP 149

APPLICATION THERMAL DERATING METHODOLOGIES: This publication applies to the application of integrated circuits and their associated packages in end use designs. It summarizes the methodology of thermal derating and the suitability of such methodologies.

November 2004 June 2004 /JC-14.3 Subcommittee $47.00

JEP 150

Stress-Test-Driven Qualification of and Failure Mechanisms Associated with Assembled Solid State Surface-Mount Components This publication contains a set of frequently recommended and accepted JEDEC reliability stress tests. These tests are used for qualifying new and modified technology/ process/ product families, as well as individual solid state surface-mount products, in particular leadless chip carriers, ball grid array

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(BGA) packages, direct chip attach die and packages with exposed pads that are attached to the PWB for thermal considerations. Assembly level testing may not be a prerequisite for device qualification; however, if the effect of assembly conditions on the component is not known, there could be reliability concerns for that component that are not evident in component level testing. As such, it is recommended that assembly level testing be performed to determine if there are any adverse effects on that component due to its assembly to a PWB.

May 2005 October 2004 /JC-14.3 Subcommittee $48.00

JEP 152 **DDR2 DIMM CLOCK SKEW MEASUREMENT PROCEDURE USING A CLOCK REFERENCE BOARD** This document is the work product of the JC-45.1 DDR2 DIMM Clock Skew Measurement task group.The purpose of this document is to define procedures to measure clock parameters on registered DIMMs using the DDR2 Clock Reference Board. It is NOT the intent of this document to set specification values or validation requirements.

May 2007 February 2004 /JC-45.1 Subcommittee $55.00

JEP 179 **DDR2 SPD Interpretation of Temperature Range and (Self-) Refresh Operation** The purpose of this document is to explain the meaning of SPD setting (JESD21 SPD section) for DDR2 SDRAM (JESD79-2) in normal and extended temperature operationy67.

June 2006 March 2005 /JC-42.3 Subcommittee $40.00

NUMBER EIA Standards (EIA) PRICE

EIA 236-C **COLOR CODING OF DISCRETE SEMICONDUCTOR DEVICES:** This standard details the methods to be followed if color coding is used to identify JEDEC-assigned type numbers or for cathode identification of discrete semiconductor devices. ANSI/EIA-236-C-1986.

March 1986; Reaffirmed November 1999 /JC-10 Committee $38.00

EIA 282-A **STANDARD FOR SILICON RECTIFIER DIODES: SEE JESD282-B** ANSI/EIA-282-A-1989

February 1990; Elevated Became JESD282-B after revision April 2000 /JC-22.2 Subcommittee

EIA 283 **TEST METHOD FOR TRANSISTOR NOISE FIGURE MEASUREMENTS AT MEDIUM FREQUENCIES - SUPERSEDED BY EIA-311-A.**

November 1963; Rescinded November 1981 November 1981 /JC-25 Committee

EIA 284-A **TEST METHODS FOR THE COLLECTOR-BASE TIME CONSTANT AND FOR THE RESISTIVE PART OF THE COMMON-EMITTER INPUT IMPEDANCE:**

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SEE JESD284A. EIA-284-A became JESD284A after reaffirmation in October 2002.

November 1963; Reaffirmed /JC-25 Committee

EIA 286-A **STANDARD FOR MEASURING FORWARD SWITCHING CHARACTERISTICS OF SEMICONDUCTOR DIODES: SEE JESD286-B.** ANSI/EIA-286-A-1991.

February 1991; Elevated Became JESD286-B after revision February 2000 /JC-22.4 Subcommittee

EIA 302 **RANGES AND CONDITIONS FOR SPECIFYING BETA FOR LOW POWER, AUDIO FREQUENCY TRANSISTORS FOR ENTERTAINMENT SERVICE:** This standard establishes the preferred rating ranges and conditions for specifying beta for low power, audio frequency transistors intended for entertainment service.

January 1965; Reaffirmed April 1981, April 1999 /JC-25 Committee $37.00

EIA 306 **MEASUREMENT OF SMALL SIGNAL HF, VHF, AND UHF POWER GAIN OF TRANSISTORS:** This standard provides a method of measurement for small-signal HF, VHF, and UHF power gain of low power transistors.

May 1965; Reaffirmed April 1981, April 1999 /JC-25 Committee $38.00

EIA 308-A **PREPARATION OF OUTLINE DRAWINGS OF SOLID-STATE PRODUCTS FOR JEDEC TYPE REGISTRATION:** This standard is intended to serve as a guide to manufacturers of solid state products for the preparation of outline drawings of solid state product packages for JEDEC type registration.

August 1981 /JC-11 Committee $38.00

EIA 311-A **MEASUREMENT OF TRANSISTOR NOISE FIGURE AT MF, HF, AND VHF:** This standard describes a test method for measurement of transistor noise figure and effective input noise temperature at MF, HF, and VHF. This standard also adds the necessary information to make 'effective input noise temperature measurements'. This method is a revision of EIA-311 and incorporates material previously found in EIA-283.

November 1981; Reaffirmed April 1999 /JC-25 Committee $48.00

EIA 318-B **MEASUREMENT OF REVERSE RECOVERY TIME FOR SEMICONDUCTOR SIGNAL DIODES:** This standard describes the measurement of signal diodes (I_F <=500mA dc) reverse recovery times of less than 300 ns duration. It may, however, also be used for the measurement of longer recovery times. This standard is also intended to establish a method which to characterize the test fixture used for this measurement.

July 1996; Reaffirmed April 1999 /JC-22.4 Subcommittee $47.00

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EIA 321-C **NUMBERING OF LIKE-NAMED TERMINAL FUNCTIONS IN SEMICONDUCTOR DEVICES AND DESIGNATION OF UNITS IN MULTIPLE-UNIT SEMICONDUCTOR DEVICES:** This standard gives the system for numbering like-named electrodes or terminal functions in semiconductor devices and for assigning numerical designations to units of multiple-unit semiconductor devices. It applies to both integrated circuits and discrete devices. ANSI/EIA-321-C-1987

February 1987; Reaffirmed November 1995 November 1995 /JC-10 Committee $41.00

EIA 323 **AIR-CONVECTION-COOLED, LIFE TEST ENVIRONMENT FOR LEAD-MOUNTED SEMICONDUCTOR DEVICES:** This standard is applicable to life testing of lead-mounted semiconductor devices intended for applications in a natural air-cooled environment where most of the power dissipation is obtained by convection and radiation losses from the body to the device.

March 1966; Reaffirmed February 1972, November 2002 November 2002 /JC-22.1 Subcommittee $40.00

EIA 340 **STANDARD FOR THE MEASUREMENT OF CRE:** This standard offers an easily measured parameter which is one of the significant characteristics in determining the stability of a transistor intended for small-signal operation. The measurement technique allows rapid testing. Its correlation to AC stability will help to establish the interchangeability of a device.

November 1967; Reaffirmed April 1981, April 1999 /JC-25 Committee $43.00

EIA 353 **THE MEASUREMENT OF TRANSISTOR NOISE FIGURE AT FREQUENCIES UP TO 20 kHz BY SINUSOIDAL SIGNAL-GENERATOR METHOD:** This noise measurement method applies to transistors whose noise has a Gaussian power distribution, to transistors whose noise has a flat (white) power distribution, and to transistors whose noise has a l/f (power inversely proportional to frequency) power distribution.

April 1968; Reaffirmed April 1981, April 1999 /JC-25 Committee $40.00

EIA 354 **THE MEASUREMENT OF TRANSISTOR EQUIVALENT NOISE VOLTAGE AND EQUIVALENT NOISE CURRENT AT FREQUENCIES OF UP TO 20 kHz:** This standard provides a method for determining values, for device registration purposes, for transistor equivalent noise voltage and equivalent noise current at frequencies up to 20 kHz. This method is applicable to transistors whose noise has a Gaussian, flat (white) or I/f power distribution.

April 1968; Reaffirmed April 1981, April 1999 /JC-25 Committee $40.00

EIA 365 **PERFORMANCE TEST PROCEDURE FOR SOLAR CELLS AND CALIBRATION PROCEDURE FOR SOLAR CELL STANDARDS FOR SPACE VEHICLE SERVICE:** The purpose of this standard is to classify the

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output of solar cells for space vehicle service in accordance with requirements of EIA Format JS4-RDF4.

November 1969; Reaffirmed February 1984 / Committee!33JC231 $47.00

EIA 371 **THE MEASUREMENT OF SMALL-SIGNAL VHF-UHF TRANSISTOR SHORT-CIRCUIT FORWARD CURRENT TRANSFER RATIO:** This standard describes the method to be used for the measurement of small-signal VHF-UHF transistor short-circuit forward current transfer ratio, in preparing data sheets for JEDEC registration of low power transistors.

February 1970; Reaffirmed April 1981, April 1999 /JC-25 Committee $41.00

EIA 372 **THE MEASUREMENT OF SMALL-SIGNAL VHF-UHF TRANSISTOR ADMITTANCE PARAMETERS:** This standard describes the method to be used for the measurement of small-signal VHF-UHF transistor admittance parameters, in preparing data sheets for JEDEC registration of low power transistors.

May 1970; Reaffirmed April 1981, April 1999 /JC-25 Committee $43.00

EIA 397 **RECOMMENDED STANDARD FOR THYRISTORS:** One section of this standard presents a thorough explanation of thyristor principals, defining thedifferent classes of these devices, their Physical structure and detailing the numerous test methods and ratings required in their application to electronic and power circuitry. Another section presents a universally accepted listing of letter symbols. Considerable effort is devoted to the use of JEDEC Type Registration System as related to thyristors. This will permit the device manufacturer to employ a uniform procedure in the development of maximum rating and presentation of performance data.

June 1972 /JC-22.1 Subcommittee $177.00

EIA 397-1 **ADDENDUM No. 1 TO EIA-397:** A compilation of 12 new or revised thyristor test methods which have been adopted since the original standard was issued in 1972.

July 1980 /JC-22.1 Subcommittee $83.00

EIA 398 **MEASUREMENT OF SMALL VALUES OF TRANSISTOR CAPACITANCE:** This standard contains a three-terminal procedure for capacitance measurement with due precautions for shielding of extraneous effects due to terminal leads and metal enclosures.

July 1972; Reaffirmed April 1981, April 1999 /JC-25 Committee $43.00

EIA 428-A **TYPE DESIGNATION SYSTEM FOR MICROELECTRONIC DEVICES**

October 1988; Rescinded September 1993 September 1993 /JC-10 Committee

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EIA 435 **STANDARD FOR THE MEASUREMENT OF SMALL-SIGNAL TRANSISTOR SCATTERING PARAMETERS:** This standard specifies the standard for the measurement of small-signal transistor scattering parameters.

June 1976; Reaffirmed April 1999 /JC-25 Committee $49.00

EIA 471 **SYMBOL AND LABEL FOR ELECTROSTATIC SENSITIVE DEVICES:** This standard will be useful to anyone engaged in handling semiconductor devices and integrated circuits that are subject to permanent damage due to electrostatic potentials. The standard establishes a symbol and label that will gain the attention of those persons who might inflict electrostatic damage to the device. The label which is placed on the lowest practical level of packaging contains the words 'ATTENTION - OBSERVE PRECAUTIONS FOR HANDLING ELECTROSTATIC SENSITIVE DEVICES'. The symbol contained in this label, which may be used on the device itself, shows a hand in a triangle with a bar through it.

February 1980; Reaffirmed October 1988, September 1996, November 1996 /JC-10 Committee $38.00

EIA 554A **Method Selection for Assessment of Nonconforming Levels in Parts Per Million (PPM)** This standard is intended to provide guidance for the selection of a method for estimating and reporting th proportion nonconforming. The PPM philosophy applies to the average quality level of a product, not to acceptance plans.

July 1996; Reaffirmed September 5, 2002 January 2006 /JC-13.2 Subcommittee $IHS

EIA 557B **STATISTICAL PROCESS CONTROL SYSTEMS:** SPC embraces a management philosophy of continuous process improvement that has a primary focus on prevention of defects. After a process has been characterized using statistical techniques (i.e., design experiments (DOE), capability studies, etc.), SPC is a tool that can be applied to control and optimize the process and reduce variability. An acceptable approach toward an SPC system involves the use of 'end-of-process' data to control the process through the application of SPC techniques. However, the intent of this standard is to emphasize the use of in-process data in order to better control and forecast system quality. This proactive use of SPC in conjunction with other techniques and the appropriate responsiveness to out-of-control situations serves to make SPC techniques critical in continuous process improvement and achieving excellence.

February 2006 /JC-13.5 Subcommittee $IHS

EIA 599-A **NATIONAL ELECTRONIC PROCESS CERTIFICATION STANDARD; GOVERNMENT CONTRACTORS:** Due to notification from the JC-14.4 subcommittee that the material contained in EIA599 has been replaced by the ISO 9000 series, the JEDEC Board of Directors, at its August 2003 meeting, approved to remove this standard from the JEDEC Free Download Area.

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June 1998; Rescinded August 25, 2003 August 2003 /JC-14.4 Subcommittee

EIA 623 **PROCUREMENT QUALITY OF SOLID STATE COMPONENTS BY GOVERNMENT CONTRACTORS: RESCINDED, May 2006**

July 1994; Rescinded May 2006 January 2004 /JC-13 Committee $40.00

EIA 625 **REQUIREMENTS FOR HANDLING ELECTROSTATIC-DISCHARGE-SENSITIVE (ESDS) DEVICES (SUPERSEDES JEP108-B): SEE JESD625-A.**

November 1994; Elevated Became JESD625A after Revision December 1999 /JC-13 Committee

EIA 659 **FAILURE-MECHANISM-DRIVEN RELIABILITY MONITORING (SUPERSEDES JESD29-A): SEE JESD659-A.**

July 1996; Elevated Became JESD659A after Revision September 1999 /JC-14.3 Subcommittee

EIA 670 **QUALITY SYSTEM ASSESSMENT (SUPERSEDES JESD39-A):** This standard is used by the electronic industry for preparation of audit checklists for assessing compliance of quality systems to the requirements of ANSI/ASQC Q9001 (ISO9001), ANSI/ASQC Q9002 (ISO9002), ANSI/ASQC Q9003 (ISO9003), and ANSI/EIA599, National Electronic Process Certification Standard. It also provides a tool for quality system evaluation in accordance with the guidelines of ANSI/ASQC Q9004 (ISO9004) and the Malcolm Baldrige National Quality Award Criteria.

June 1997 /JC-14.4 Subcommittee $63.00

EIA 671 **COMPONENT PROBLEM ANALYSIS AND CORRECTIVE ACTION REQUIREMENTS: SEE JESD671-A.**

November 1996; Elevated Became JESD671A after revision December 1999 /JC-14.4 Subcommittee

JESD 370B **DESIGNATION SYSTEM FOR SEMICONDUCTOR DEVICES:** This standard includes several new items and has been completely rewritten from the original EIA-370. The first is a new letter symbol C so that a JEDEC type designation may now be 2C1234, to indicate that a chip is being designated that if it were properly mounted on the package registered for the 2N1234, it would display characteristics similar to those of the 2N1234. The second major addition is the method for assigning the first numeric symbol for type designations of optoelectronic devices. ANSI/EIA-370-B-1992.

February 1982; Reaffirmed November 1995, November 1999, May 2003 /JC-10 Committee $43.00

JESD 390-A **STANDARD TEST PROCEDURE FOR NOISE MARGIN MEASUREMENTS FOR SEMICONDUCTOR LOGIC GATING MICROCIRCUITS:** The purpose of

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this standard is to define the dc (Steady-State) noise margin and the ac (Transient) Noise Margin in Semiconductor Logic Gating Microcircuits, and to describe the procedures used to measure these parameters. The standardization of the definitions and test procedures is intended to improve the ability to ensure interchangeability of elements by test specification, and to eliminate misunderstandings between manufacturers and users.

February 1981; Reaffirmed September 2003 /JC-13 Committee $43.00

NUMBER	Joint Industry Guide (JIG)	PRICE
JIG 101	**Material Composition Declaration for Electronic Products** This document has been worked on for more than three years by member companies of EICTA (Europe), JGPSSI (Japan), EIA (USA) and JEDEC (USA). The purpose of this guide establishes the materials and substances to be disclosed by suppliers when those materials and substances are present in products and subparts that are incorporated into EEE. It benefits suppliers and their commercial customers by providing consistency and efficiency to the material declaration process. It promotes the development of consistent data exchange formats and tools that will facilitate and improve data transfer along the entire global supply chain. May 2005 January 2002 /JC-14 Committee	$0.00-TBD

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EIA 236-C	COLOR CODING OF DISCRETE SEMICONDUCTOR DEVICES:
EIA 321-C	NUMBERING OF LIKE-NAMED TERMINAL FUNCTIONS IN SEMICONDUCTOR DEVICES AND DESIGNATION OF UNITS IN MULTIPLE-UNIT SEMICONDUCTOR DEVICES:
JESD 370B	DESIGNATION SYSTEM FOR SEMICONDUCTOR DEVICES:
EIA 428-A	TYPE DESIGNATION SYSTEM FOR MICROELECTRONIC DEVICES
EIA 471	SYMBOL AND LABEL FOR ELECTROSTATIC SENSITIVE DEVICES:
JEP 100	TERMS, DEFINTIONS, AND LETTER SYMBOLS FOR MICROCOMPUTERS AND MEMORY INTEGRATED CIRCUITS: ELEVATED TO JESD100, August 1993.
JEP 103A	SUGGESTED PRODUCT-DOCUMENTATION, CLASSIFICATIONS, AND DISCLAIMERS

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JEP 120-A	INDEX OF TERMS DEFINED IN JEDEC PUBLICATIONS:
JEP 75	LETTER SYMBOLS USED WITH INFRARED DEVICES - INCORPORATED INTO JESD77-A.
JEP 99	GLOSSARY OF MICROELECTRONIC TERMS, DEFINITIONS, AND SYMBOLS: ELEVATED TO JESD99, June 1985.
JESD 100B.01	TERMS, DEFINITIONS, AND LETTER SYMBOLS FOR MICROCOMPUTERS, MICROPROCESSORS, AND MEMORY INTEGRATED CIRCUITS:
JESD 99B	TERMS, DEFINITIONS, AND LETTER SYMBOLS FOR MICROELECTRONIC DEVICES:
JESD 99-1	ADDENDUM No. 1 to JESD99 - TERMS, DEFINITIONS, AND LETTER SYMBOLS FOR ANALOG-TO-DIGITAL AND DIGITAL-TO-ANALOG CONVERTERS:
JEP 104C.01	REFERENCE GUIDE TO LETTER SYMBOLS FOR SEMICONDUCTOR DEVICES:
JESD 77B.01	TERMS, DEFINITIONS, AND LETTER SYMBOLS FOR DISCRETE SEMICONDUCTOR AND OPTOELECTRONIC DEVICES:
JESD 88C	DICTIONARY OF TERMS FOR SOLID STATE TECHNOLOGY, Fourth Edition:

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JESD 95-1	DESIGN REQUIRMENTS FOR OUTLINES OF SOLID STATE AND RELATED PRODUCTS: DISCONTINUED AS A SEPARATE ITEM CONTAINED IN JEP95, BOOK 1, SECTION 4.
JESD 30D	DESCRIPTIVE DESIGNATION SYSTEM FOR SEMICONDUCTOR-DEVICE PACKAGES:
JEP 86-A	RECOMMENDED PRACTICE FOR DUAL DIMENSIONING
JEP 95 AUS	ANNUAL UPDATING SERVICE:
JEP 95	JEDEC REGISTERED AND STANDARD OUTLINES FOR SOLID STATE AND RELATED PRODUCTS:
JEB 20	ACCEPTED PRACTICES FOR MAKING MICROELECTRONIC DEVICE THERMAL CHARACTERISTICS TESTS
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JEP 109-C	GENERAL REQUIREMENTS FOR DISTRIBUTORS OF MILITARY SEMICONDUCTOR DEVICES:
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JESD 390-A	STANDARD TEST PROCEDURE FOR NOISE MARGIN MEASUREMENTS FOR SEMICONDUCTOR LOGIC GATING MICROCIRCUITS:
EIA 623	PROCUREMENT QUALITY OF SOLID STATE COMPONENTS BY GOVERNMENT CONTRACTORS: RESCINDED, May 2006
EIA 625	REQUIREMENTS FOR HANDLING ELECTROSTATIC-DISCHARGE-SENSITIVE (ESDS) DEVICES (SUPERSEDES JEP108-B): SEE JESD625-A.
JEP 132	PROCESS CHARACTERIZATION GUIDELINE:
JEP 114	GUIDELINES FOR PARTICLE IMPACT NOISE DETECTION (PIND) TESTING, OPERATOR TRAINING, AND CERTIFICATION:
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JESD 40	PROCUREMENT QUALITY OF SOLID STATE COMPONENTS BY GOVERNMENT CONTRACTORS - SUPERSEDED BY EIA-623, July 1994
JESD 42	REQUIREMENTS FOR HANDLING ELECTROSTATIC-DISCHARGE-SENSITIVE (ESDS) DEVICES - SUPERSEDED BY EIA-625, November 1994.
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JEP 121A	REQUIREMENTS FOR MICROELECTRONIC SCREENING AND TEST OPTIMIZATION:
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JEP 101-C	JEDEC REQUIREMENTS FOR CLASS B MICROCIRCUITS: RESCINDED, May 2006
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JEP 133B	GUIDE FOR THE PRODUCTION AND ACQUISITION OF RADIATION-HARDNESS ASSURED MULTICHIP MODULES AND HYBRID MICROCIRCUITS:
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Metric	**Design 4.13**
Metrication	**SPP 003C**
Mezzanine	**SO 004A** **MO 260C**
Micro	**MO 214-B** **MO 260C**

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Micro DIMM	**SO 004A**
Micro Size	**MO 279A**
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Mini DIMM	**MO 244-B** **SO 002A**
Mini Tray	**CO 030-A** **CO 031-A**
MiniDIMM	**MO 258-A** **MODULE 4_20_14**
MiniRDIMM	**MO 258-A**
Mitigation	**JP 002**
MM	**JESD 22-A115-A**
MMC	**JESD 84-B41** **JESD 84-B42** **JESD 84-A42** **MO 277A** **MO 278A** **MO 279A**
MMCA	**JESD 84-B41** **JESD 84-B42** **JESD 84-A42**
MMCmicro	**MO 279A**
MMCmobile	**MO 278A**
MMCplus	**MO 277A**
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Mode	**JESD 22-B115**
Model Development	**JESD 91-A**
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Moisture-Induced	**JESD 22-A112-A**
Mold Flash	**MS 012E** **MS 013E** **SPP 014**
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Monotonic	**JS 9702**
Mos	**SRAM 3_07_08**

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MOSFET	**JESD 28-1** **JESD 90**
MOSFETs	**JESD 24- 3** **JESD 60A**
MPDRAM	**MODULE 4_4_6**
MQFP	**CS 004-B**
Multi Chip Module	**JEP 142**
Multi Media	**JESD 84-A41**
Multi Media Card	**MO 277A** **MO 278A** **MO 279A**
Multi-row	**MO 247D** **Design 4.19D**
Multibus	**PR N07-SM2**
Multichip	**MCP 3_12_01**
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N-Channel MOSFET	**JESD 28-A**
NAND	**PR N07-SM2** **MO 259-A**
National Electronic Process Certification	EIA 599-A
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NBTI	**JESD 90**
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NFET Switch	**JESD 73-1** **JESD 73-2**
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NMOS FET	**JESD 73**
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Optional Features	**DRAM 3_09_05**
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Outlier Identification	**JESD 62-A**
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Package Height	**SDRAM 3_11_05_08**
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Package-on-Package	**MCP 3_12_02** **PR N07-SM2** **Design 4.22A**
Packages - Semiconductor Devices	**JESD 30D**
Packing	**J-STD- 033B.1**
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Parity	**JESD 82-23** **JESD 82-12A** **JESD 82-14A** **JESD 82-17**
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PB-Free	**J-STD- 609**
PBGA	**MS 034-D**
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PC1600	**MODULE 4_20_05** **MODULE 4_20_04** **JESD 82-1A** **JESD 82-13A**
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PC2-4200	**MODULE 4_20_10** **MODULE 4_20_13** **MODULE 4_20_11**
PC2-5300	**MODULE 4_20_10** **MODULE 4_20_13** **MODULE 4_20_11**
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PC200	**JESD 79E**
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PC2700/PC3200	**MODULE 4_20_07**
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Plasma-Process	**JP 001.01**
Plastic	**MO 287-A** **MO 288-A** **TO 279A** **DO 221A** **DO 222A** **MO 283A** **CO 033-A** **CS 002-A** **DO 214-D** **DO 215-D** **MO 059-B** **MO 153-F** **MO 204-B** **MO 208-C** **MS 012E** **MS 013E** **MS 034-D** **TO 263-E** **TO 273-B** **MO 230-A** **MO 232-A** **DO 219-B** **MO 187-E** **MO 235-B** **TO 261-C** **MO 137-C** **MO 240-A** **MO 236-B**

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	MO 220K
	MO 248E
	MO 247D
	MO 250-A
	Design 4.19D
	MO 249-A
	MO 251-A
	MO 254-A
	DO 220-B
	MO 252-C
	MO 255-B
	MO 257-B
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	MO 272A
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PLL Clock Driver	**JESD 82**
PMOS	**JESD 60A**
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POD	**JESD 8-19**
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Punch-Singulated	**MO 267B** **Design 4.23A**

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QFP	**CO 011-B** **CO 012-C** **MO 239-B**
Quad	**MO 288-A** **MO 134-A** **MO 148-A** **MO 208-C** **MO 217-B** **Design 4.4A** **MO 220-D** **Design 4.8C** **MO 220K** **MO 248E** **MO 250-A** **Design 4.19D** **MO 254-A**

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Quad Flat	**MO 243-A** **MO 251-A** **MO 255-B**
Quad Flat Pack	**CO 011-B** **CO 012-C**
Qual Flatpack	**CS 002-A**
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Receiving Inspection	**EIA 623**
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Rectangular Die-Size	**MO 242B**
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Refresh Control	**DRAM 3_09_05**
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ROM DIMM	MODULE 4_4_8
Round Lead	DO 204B-D
RT-PLGA	MO 279A
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S-PBGA	MS 034-D
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SDRAM	JESD 79-3A MODULE 4_20_10 MODULE 4_20_12 SDRAM 3_11_02 SDRAM 3_11_03 SDRAM 3_11_04 SDRAM 3_11_05TOC SPD 4_01_02_04 SPD 4_01_02_09 MODULE 4_4_8 MODULE 4_5_2 MODULE 4_5_6 MODULE 4_05_10 MODULE 4_5_11 MODULE 4_5_13 MODULE 4_5_07 JESD 79E MODULE 4_20_06 JESD 82-6A MO 237F SO 001B MODULE 4_05_14 MODULE 4_20_08 PR N06-DR7 JESD 79-2C MODULE 4_20_09 SPD 4_01_02_10 JESD 8-17 JESD 209

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	SDRAM 3_11_05_05
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	SDRAM 3_11_05_02
	SDRAM 3_11_05_03
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	JESD 22-A115-A
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Serial Data	DRAM 3_09_05
Serial Interface	JESD 204
Serial Presence	SPD 4_01_02_09
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	PR N06-DR8
	SDRAM 3_11_05_08
	SDRAM 3_11_05_06
	SDRAM 3_11_05_07
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	JESD 8-20
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Shear	JESD 22-B117A
Shelf life	J-STD- 033B.1
Shipping	J-STD- 033B.1
	CO 010-E

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Shrink	GS 003C MO 137-C
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SLVS	JESD 8-13
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	MO 271A
	DO 215-D
	MO 059-B
	Design 4.15B
	MS 024H
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	DO 220-B
	MO 259-A
	MO 274A
Small Outline	**DO 221A**
	DO 222A
	SO 008A
	CO 032-A
	MS 012E
	MS 013E
	MO 230-A
	MO 187-E
	MO 249-A
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	MO 255-B
	TO 278B
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SO-004	**MO 260C**
SO-CDIMM	**JESD 82-21**
SO-DIMM	**SO 008A**
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	MODULE 4_5_5
	MODULE 4_5_6
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SODIMM	**MO 224E** **MO 274A** **MODULE 4_20_16** **MO 268B** **MODULE 4_20_11**
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SOJ	**CO 032-A** **Design 4.13**
Solar Cells	**EIA 365**
Solder	**JESD 22-B115** **JESD 22-B117A**
Solder Reflow Operations	**JEP 140**
Solderability	**J-STD- 002B**
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	MO 259-A
SOT	**TO 261-C**
Space Vehicle Service	**EIA 365**
SPC System	**EIA 557B**
SPD	**SPD 4_01_TOC**
	SPD 4_01_02
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	MO 228-A
	Design 4.8C
	Design 4.20C
	MO 275-A
	MO 267B
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	Design 4.22A
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	SRAM 3_7_1
	SRAM 3_7_4
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	MCP 3_12_01
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SSOP	**MO 153-F**
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SSTL - SSTL_2	**JESD 8- 9B**
SSTL_18	**JESD 8-15A**
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SSTU	JESD 82-26 JESD 82-23 JESD 82-25 JESD 82-7A JESD 82-9B JESD 82-24 JESD 82-19A JESD 82-12A JESD 82-14A JESD 82-16A
SSTU32864	JESD 82-7A
SSTU32865	JESD 82-9B JESD 82-19A
SSTU32866	JESD 82-10A
SSTU32D868	JESD 82-14A
SSTU32D869	JESD 82-12A
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SSTUA	JESD 82-23
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SSTUA32866	JESD 82-16A
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SSTVN16859	JESD 82-13A
Stackable	MO 266B
Stacked	JESD 82-6A MO 238-A

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Stacking Module	**Design 4.21A**
Staggered	**MO 247D** **Design 4.19D** **MO 257-B** **MO 267B**
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Status Register	**PR N07-DR3**
Storage Life	**JESD 22-A103C** **JESD 22-A119**
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Very Thick	**MO 261A**
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1.2 V	JESD 76-1 JESD 8-16A
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240-Pin	MODULE 4_05_14
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54 Ball Package	**JESD 75-1**
64 pin	**MODULE 4_4_1**
72 pin	**MODULE 4_4_1** **MODULE 4_4_2** **MODULE 4_4_4**
8 lead	**MO 240-A**
8-Bit	**JESD 75-3**
8.89 mm Body	
80 Pin	**MODULE 4_4_7**

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EIA 283
TEST METHOD FOR TRANSISTOR NOISE FIGURE MEASUREMENTS AT MEDIUM FREQUENCIES - SUPERSEDED BY EIA-311-A.
November 1963; Rescinded November 1981

EIA 318-1
ADDENDUM No. 1 to EIA-318 - CHARACTERIZATION OF A REVERSE TEST FIXTURE: SUPERSEDED BY EIA-318-B, July 1996.
February 1981; Rescinded

EIA 428-A
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October 1988; Rescinded September 1993

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NATIONAL ELECTRONIC PROCESS CERTIFICATION STANDARD; GOVERNMENT CONTRACTORS:
June 1998; Rescinded August 2003

EIA 623
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July 1994; Rescinded January 2004

JEB 16
USER GUIDE FOR MICROCIRCUIT FAILURE ANALYSIS:
July 1970; Rescinded September 2003

JEB 17
USER GUIDELINES FOR QUALITY AND RELIABILITY ASSURANCE OF LSI COMPONENTS
November 1970; Rescinded April 1987

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JEB 20 ACCEPTED PRACTICES FOR MAKING MICROELECTRONIC DEVICE THERMAL CHARACTERISTICS TESTS
January 1975; Rescinded November 1988

JEB 6 STANDARD MEASURMENTS OF THE ELECTRICAL CHARACTERISTICS OF SEMICONDUCTOR INTEGRATED CIRCUITS
December 1966; Rescinded

JEP 100 TERMS, DEFINTIONS, AND LETTER SYMBOLS FOR MICROCOMPUTERS AND MEMORY INTEGRATED CIRCUITS: ELEVATED TO JESD100, August 1993.
September 1979; Rescinded October 1983

JEP 101-C JEDEC REQUIREMENTS FOR CLASS B MICROCIRCUITS: RESCINDED, May 2006
November 1995; Rescinded

JEP 102 STANDARD FOR 64K x 1 DYNAMIC RAM - SUPERSEDED BY JESD21-C.
September 1978; Rescinded April 1985

JEP 105 JEDEC GUIDELINE FOR THE CHARACTERIZATION OF HYBRID POLYMERIC MATERIALS - SUPERSEDED BY JESD72, June 2001
April 1983; Rescinded June 2001

JEP 107 TEST METHOD FOR QUALIFICATION AND ACCEPTANCE OF PARTICLE GETTERS FOR USE IN HYBRID MICROELECTRONIC APPLICATIONS - SUPERSEDED BY JESD72, June 2001
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JEP 108-B DISTRIBUTOR REQUIREMENTS FOR HANDLING ELECTROSTATIC - DISCHARGE SENSITIVE (ESDS) DEVICES: SUPERSEDED BY JESD42, March 1994.
April 1991; Superseded

JEP 109-C GENERAL REQUIREMENTS FOR DISTRIBUTORS OF MILITARY SEMICONDUCTOR DEVICES:
March 1995; Rescinded November 2001

JEP 111 TEST PROCEDURES FOR CUSTOM MONOLITHIC MICROCIRCUITS - SUPERSEDED BY MIL-PRF-38535C.
July 1986; Rescinded June 1996

JEP 112 TEST METHOD FOR QUALIFICATION AND ACCEPTANCE OF CIRCUIT SUPPORT FILMS FOR USE IN MICROELECTRONIC APPLICATIONS - SUPERSEDED BY JESD72, June 2001
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JEP 117 GUIDELINES FOR USER NOTIFICATION OF PRODUCT/PROCESS CHANGES BY SEMICONDUCTOR SUPPLIERS - SUPERSEDED BY JESD46,

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June 1992; Rescinded June 1985

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July 1977; Rescinded June 1985

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March 1993; Rescinded June 2004

JESD 39-A QUALITY SYSTEM ASSESSMENT - SUPERSEDED BY ANSI/EIA-670, June 1997.
June 1997; Superseded

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July 1994; Superseded

JESD 41 REVERSE RECOVERY CHARACTERISTICS OF SILICON DIODES: Rescinded June 2002.
May 1995; Rescinded June 2002

JESD 42 REQUIREMENTS FOR HANDLING ELECTROSTATIC-DISCHARGE-SENSITIVE (ESDS) DEVICES - SUPERSEDED BY EIA-625, November 1994.
March 1994; Superseded

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November 1996; Superseded

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