US006856556B1

(12) **United States Patent**
Hajeck

(10) **Patent No.: US 6,856,556 B1**
(45) **Date of Patent: Feb. 15, 2005**

(54) **STORAGE SUBSYSTEM WITH EMBEDDED CIRCUIT FOR PROTECTING AGAINST ANOMALIES IN POWER SIGNAL FROM HOST**

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(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 1 day.

(21) Appl. No.: **10/406,805**

(22) Filed: **Apr. 3, 2003**

(51) **Int. Cl.**[7] **G11C 7/00**
(52) **U.S. Cl.** **365/189.11**; 365/191; 365/226
(58) **Field of Search** 365/189.11, 191, 365/226, 189.01, 229, 185.33, 212, 200, 189.07, 225.7, 203, 189.08, 158, 171; 307/43–46, 48, 64, 66, 85–87

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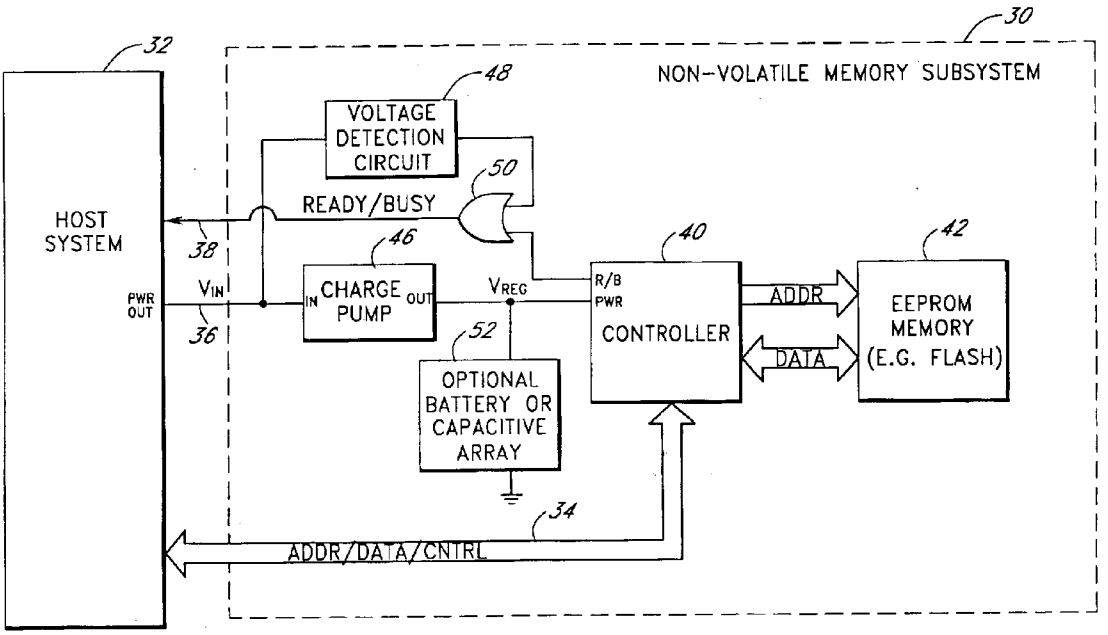
(57) **ABSTRACT**

A storage subsystem, such as a flash memory card, includes a charge pump that receives a power signal from a host system, and generates a regulated power signal that is provided to the storage subsystem's controller. When the power signal from the host is interrupted, the charge pump additionally acts as a backup power supply such that the storage subsystem can continue to operate temporarily. The storage subsystem also includes a voltage detection circuit that monitors the power signal from the host system to detect anomalies therein. The voltage detection circuit responds to detection of an anomaly by asserting a busy signal to block the host system from performing write operations to the storage subsystem. By asserting the busy signal, the voltage detection circuit substantially ensures that the backup, regulated power provided by the charge pump will be sufficient for the controller to complete all outstanding operations.

38 Claims, 2 Drawing Sheets



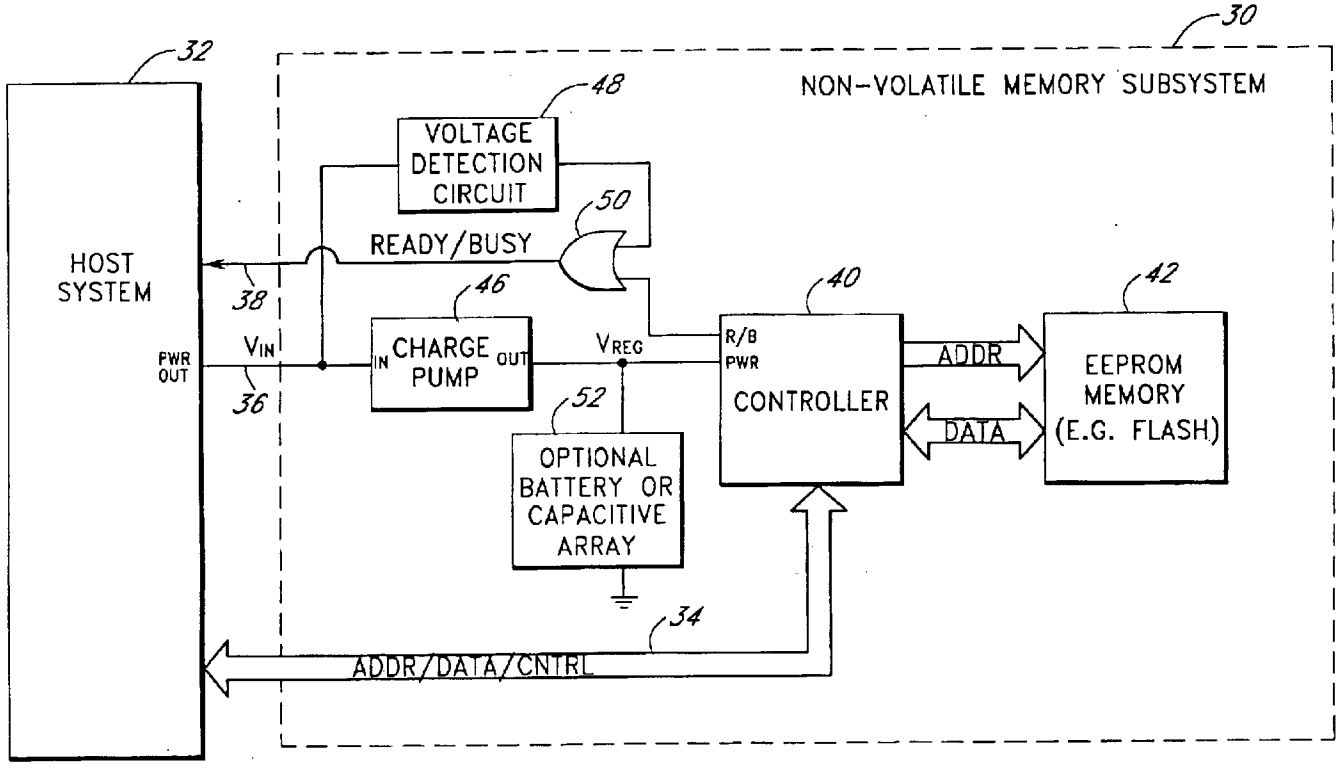

30
32
NON-VOLATILE MEMORY SUBSYSTEM
48
VOLTAGE DETECTION CIRCUIT
50
READY/BUSY
HOST SYSTEM
38
46
40
42
PWR OUT
VIN
IN
CHARGE PUMP
OUT
VREG
R/B
PWR
CONTROLLER
ADDR
EEPROM MEMORY (E.G. FLASH)
36
52
DATA
OPTIONAL BATTERY OR CAPACITIVE ARRAY
34
ADDR/DATA/CNTRL

FIG. 1

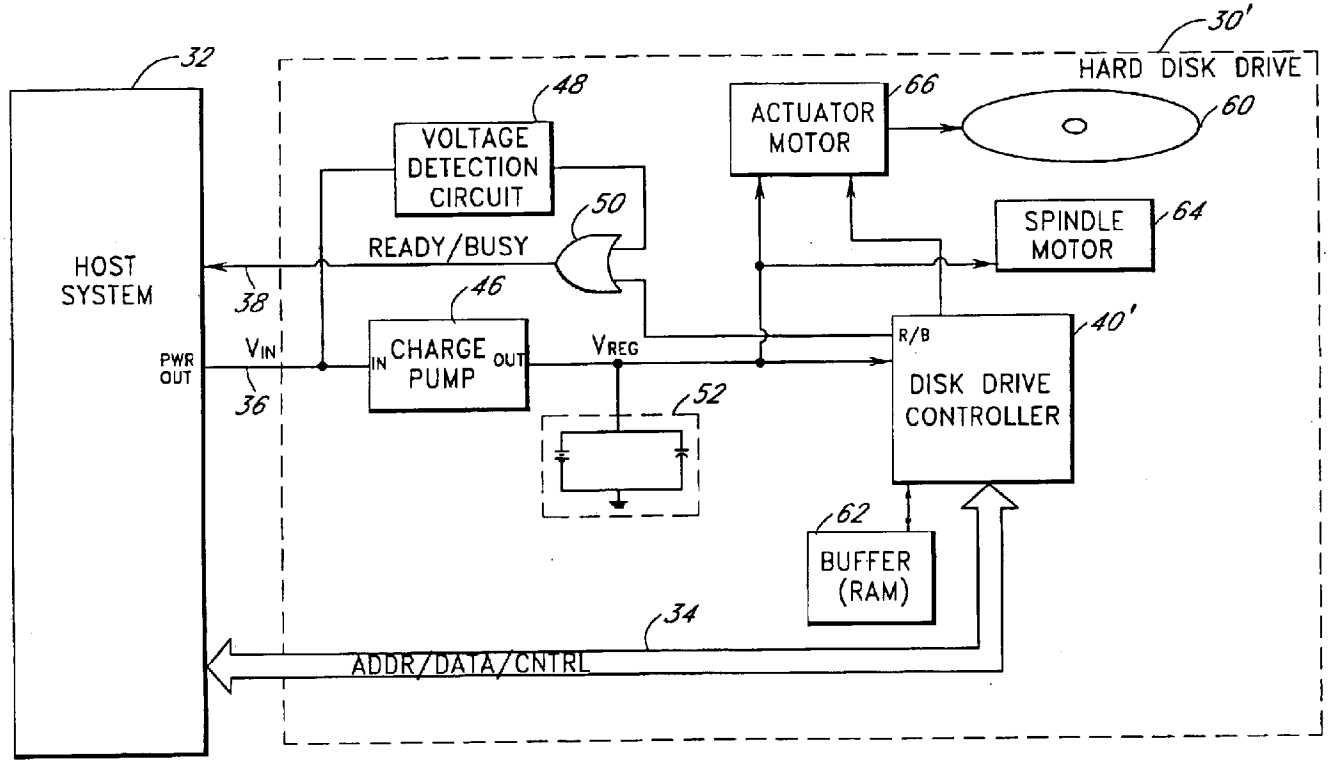

32
HOST SYSTEM
PWR OUT
38
36
V_{IN}
30'
HARD DISK DRIVE
48
VOLTAGE DETECTION CIRCUIT
50
READY/BUSY
46
CHARGE PUMP
IN
OUT
V_{REG}
52
66
ACTUATOR MOTOR
60
64
SPINDLE MOTOR
40'
R/B
DISK DRIVE CONTROLLER
62
BUFFER (RAM)
34
ADDR/DATA/CNTRL

FIG. 2

STORAGE SUBSYSTEM WITH EMBEDDED CIRCUIT FOR PROTECTING AGAINST ANOMALIES IN POWER SIGNAL FROM HOST

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to circuits from protecting storage subsystems, such as but not limited to flash memory cards, from damage and data loss caused by irregularities in a power signal provided by a host.

2. Description of the Related Art

A significant problem in the area of storage subsystems relates to data loss, data corruption, and circuitry damage caused by interruptions and other irregularities in the power signal supplied by the host system. For example, in the context of a flash memory subsystem, an unexpected power loss can cause a sector write operation to terminate prematurely, resulting in a mismatch between a sector's data and ECC portions. In addition to losing the write data, the memory subsystem's controller may thereafter respond to the ECC mismatch condition by treating the sector as defective, and unnecessarily replacing the sector with a spare sector. Incomplete sector write operations can also result in data loss and sector replacement in disk drives that store data on a rotating medium. Other types of power signal anomalies, such as power surges and spikes, can additionally cause permanent damage to the circuitry of the storage subsystem.

SUMMARY OF THE INVENTION

The present invention provides a circuit and associated method for protecting a storage subsystem from irregularities in a power signal supplied by a host system. The invention may be embodied within a variety of different types of storage subsystems, including but not limited to non-volatile solid state memory cards (such as but not limited to those that comply with the CompactFlash, PCMCIA, SmartMedia, MultiMediaCard, SecureDigital and Memory Stick card specifications), volatile and non-volatile solid-state storage products in disk drive form factors, electro-mechanical disk drives, and volatile and non-volatile solid-state storage products in a variety of industry standard and custom form factors. No modifications are needed to the host system.

In one embodiment, the storage subsystem includes a charge pump circuit that receives the power signal from a host system, and generates a regulated power signal that is provided to the storage subsystem's controller (and possibly to other active components of the storage subsystem). When the power signal from the host is interrupted, the charge pump circuit acts as a backup power source such that the storage subsystem can continue to operate temporarily. A rechargeable battery and/or a capacitive array may also be provided as additional sources of backup power. In addition to providing backup power, the charge pump circuit protects the controller from potential damage caused by power surges and spikes.

The storage subsystem in the preferred embodiment also includes a voltage detection circuit that monitors the power signal from the host system to detect anomalies. The voltage detection circuit responds to detection of a power signal anomaly by asserting a busy signal to block the host system from performing write operations to the storage subsystem.

By asserting the busy signal, the voltage detection circuit substantially ensures that backup power provided by the charge pump (and by the battery and/or capacitive array, if provided) will be sufficient for the controller to complete all outstanding operations. The likelihood that data will be lost as the result of the power signal anomaly is therefore significantly reduced.

BRIEF DESCRIPTION OF THE DRAWINGS

Specific embodiments of the invention will now be described with reference to the following drawings, which are intended to illustrate and not limit the invention:

FIG. **1** illustrates the design of a non-volatile solid state memory subsystem according to one embodiment of the invention; and

FIG. **2** illustrates the design of a hard disk drive subsystem according to another embodiment of the invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

FIG. **1** illustrates a solid state memory subsystem **30** according to one embodiment of the invention. The memory subsystem **30** may, for example, be a flash memory card that conforms to one of the aforementioned card specifications, although the invention is not so limited. The memory subsystem plugs into a slot of, or otherwise attaches to, a host system **32** (hereinafter "host"). The host may be any type of conventional system or device that accepts the memory subsystem, and need not include any special hardware or software for implementing the present invention.

The interface between the memory subsystem **30** and the host **32** includes the following conventional signal lines: a set of address/data/control lines **34** for transferring data; at least one power line **36** over which the host provides a power signal to the memory subsystem; and a ready/busy signal line **38** that is driven by the memory subsystem to notify the host of the subsystem's current status. In implementations in which the particular interface does not include an actual "ready/busy" signal, a different signal or combination of signals may be used to notify the host of the memory subsystem's ready/busy status.

As is conventional, the memory subsystem **30** includes a controller **40** that controls, an array of solid state, non-volatile memory **42**, which may be flash memory or another type of EEPROM memory. A conventional flash memory controller **40** may be used, as no special controller circuitry or functionality is needed in the illustrated embodiment. In accordance with the invention, the memory subsystem **30** also includes the following components to protect against anomalies in the power signal supplied by the host: a charge pump circuit **46**, a voltage detection circuit **48**, and a logic gate or switch **50**. The switch is shown for illustrative purposes as an OR gate, although other types of gates and switches may be used. The charge pump circuit **46** ("charge pump"), voltage detection circuit **48**, and switch **50** may be integrated within a single analog ASIC (application specific integrated circuit), possibly together with other components of the memory subsystem. As depicted by block **52** in the drawing, an optional battery or capacitive array may also be included to provide an additional level of protection against power anomalies.

As illustrated in FIG. **1**, the charge pump **46** receives the power signal V_{IN} from the host **32**, and supplies a regulated, substantially-constant power signal V_{REG} to the controller **40**— and possibly to other active components of the

memory subsystem, such as a volatile memory used as a buffer (not shown). Preferably, the charge pump is designed such that the voltage V_{REG} supplied to the controller **40** is maintained at the ideal level (e.g., 5.4 volts) in the event of a brief interruption, drop, increase, or spike in the voltage V_{IN} supplied by the host **32**. In addition, the charge pump is preferably designed to protect against sustained voltage drops; for example, in one embodiment, the charge pump is capable of maintaining V_{REG} at 5.4 volts indefinitely as long as V_{IN} exceeds 0.7 volts. The charge pump **46** thus allows the memory subsystem **30** to continue to operate during certain types of power anomalies, including brief power interruptions, spikes and sustained voltage drops. In addition, the charge pump **46** protects the controller **40** from being damaged by spikes and surges in the power signal provided by the host.

The charge pump **46** preferably is or comprises a DC-to-DC step-up/step-down converter. Examples of commercially available charge pump devices that may be used include the ILC6363CIR50 and ILC6383CIRADJ from Fairchild and the MAX849, MAX1705 from Maxim. As is known in the art, the charge pump may optionally include or be followed by a low drop-out (LDO) voltage regulator (not shown) to provide greater output voltage stability. This LDO voltage regulator may be provided in-line between the charge pump's output and the controller's power input, downstream from the optional battery or capacitive array **52** if provided. One example of a voltage regulator device that may be used is a Seiko Epson S80827C.

The voltage detection circuit **48** is responsible for detecting anomalies in the power signal V_{IN} supplied by the host on line **36**, and for driving the ready/busy signal to the "busy" state when such anomalies are detected. A conventional voltage detection circuit may be used. The voltage detection circuit **48** may be designed to generate a "busy" signal whenever V_{IN} falls below a certain level, such as 2.6 or 2.7 volts. The voltage detection circuit may also be designed to generate a busy signal when the voltage exceeds a certain level, and/or when other types of anomalies are detected. To inhibit rapid transitions between the "ready" and "busy" states, the voltage detection circuit may be designed to provide a degree of hysteresis, and/or to hold its output for a particular time period after a state transition.

The logic switch **50** logically combines (e.g., ORs) the ready/busy signals generated by the voltage detection circuit **48** and the controller **40** to generate the ready/busy signal provided to the host **32** on line **38**. Specifically, if a busy signal is generated by the voltage detection circuit **48**, the controller **40**, or both the voltage detection and the controller, a busy signal is provided to the host **32**. As is known in the art and defined by various interface specifications, the host will not perform new write operations to the memory subsystem when the "busy" state is asserted. Thus, the host **32** is prevented from performing write operations to the memory subsystem when voltage anomalies are detected and signaled by the voltage detection circuit **48**. As mentioned above, in implementations in which the particular host-subsystem interface does not include a "ready/busy" signal, the ready/busy status of the memory subsystem **30** may be communicated to the host using a different signal line or combination of signal lines.

The illustrated memory subsystem **30** responds to power signal anomalies generally as follows. Upon detecting the anomaly, the voltage detection circuit **48** generates a busy signal on line **36**, causing the host to refrain from writing or reading data to/from the memory subsystem **30**. Despite the anomaly in the power input signal, the charge pump **46** continues to provide a near-constant voltage V_{REG} to the controller **40** (for at least a minimum time period T_{VREG}, as described below). Because new write operations are inhibited, and because the charge pump continues to provide a regulated power signal to the controller **40**, the possibility of data corruption (e.g., as the result of incomplete write operations) is significantly reduced. The charge pump also serves to protect the controller **40** and other circuitry from damage caused by voltage surges and spikes.

Even if the anomaly is in the form of a complete interruption or termination of power from the host **32**, the charge pump **46** continues to provide power to the controller **40** (and possibly to other active components, as mentioned above) for at least the minimum time period, T_{VREG}, needed to complete all outstanding operations. For example, if a write operation is in progress and the memory subsystem **30** has write data stored in its volatile RAM buffer (not shown), backup power will be provided for a time period sufficient for the controller **40** to finish writing this data to the EEPROM memory **42**, and if necessary, to back up any configuration data stored in volatile memory. The memory subsystem **30** may also use the backup power to perform a shut down sequence. The value of T_{VREG} needed to protect against data loss will typically be in the range of several milliseconds to several seconds, depending upon the design and type of the memory subsystem **30**.

As depicted by block **52** in FIG. **1**, a battery or a capacitive array may be connected between ground and the output of the charge pump **46** to extend the time duration for which backup power is provided. If a battery is used, the battery may be a small, rechargeable, watch-type battery that is embedded within the memory subsystem's housing. Typically, a battery of this type can provide several minutes of backup power to the controller **40**. If a capacitive array is provided, the capacitive array may consist of a bank or array of capacitors, and may provide tens to thousands of microfarads of capacitance. The battery or capacitive array, if provided, is connected so as to become or remain charged from the output of the charge pump **46**.

The protection circuitry illustrated in FIG. **1** is particularly useful for protecting against power interruptions caused by the removal or movement of the memory subsystem **30** by the user. The protection circuitry also protects against power anomalies emanating from or experienced by the host, and may therefore also find utility in memory subsystems that are not intended to be removed by the user.

FIG. **2** illustrates an embodiment in which the power anomaly protection circuitry is included within a hard disk drive subsystem **30**, such as an ATA, Serial ATA, SCSI, or Serial-Attached SCSI disk drive. In this embodiment, the controller **40** is a conventional disk drive controller that controls reads and writes of data to/from a rotating magnetic disk **60**. In the illustrated embodiment, the controller **40'** accesses a buffer or cache **62** formed from volatile solid state RAM. The design and operation of the power anomaly protection circuitry in this disk drive embodiment may be substantially the same as described with reference to FIG. **1**, except that the charge pump (and the optional battery or capacitive array **52**) also provide backup power to the spindle and actuator motors **64**, **66** of the disk drive **30'**.

The protection circuitry and methods of the present invention may also be incorporated into other types of storage subsystems, including volatile storage subsystems that store data within DRAM or SRAM.

Although this invention has been described in terms of certain preferred embodiments and applications, other

embodiments and applications that are apparent to those of ordinary skill in the art, including embodiments which do not provide all of the features and advantages set forth herein, are also within the scope of this invention. Accordingly, the scope of the present invention is intended to be defined only by reference to the appended claims.

What is claimed is:

1. A storage subsystem, comprising:

a controller that writes data to, and reads data from, a non-volatile storage medium;

a charge pump circuit that receives a power signal from a host system, and generates a regulated power signal that is provided to the controller, wherein the charge pump circuit is capable of maintaining the regulated power signal to the controller when the power signal from the host system is interrupted, such that the charge pump circuit acts as a backup power supply when power from the host system is interrupted; and

a voltage detection circuit that monitors the power signal from the host system to detect anomalies therein, and responds to detection of such an anomaly by asserting a signal to the host system to block the host system from performing write operations to the storage subsystem.

2. The storage subsystem as in claim **1**, wherein the voltage detection circuit, by asserting the signal to block the host system, substantially ensures that backup power provided by the charge pump circuit will be sufficient for the controller to complete all outstanding operations.

3. The storage subsystem as in claim **1**, further comprising a logic circuit that generates the signal to the host system when either or both of the following occur: (a) a busy signal is generated by the voltage detection circuit; (b) a busy signal is generated by the controller.

4. The storage subsystem as in claim **1**, further comprising a rechargeable battery that acts as an additional source of backup power to the controller, said battery coupled to the charge pump such that the battery is charged when power is supplied by the host system.

5. The storage subsystem as in claim **1**, further comprising a capacitive array that acts as an additional source of backup power to the controller, said capacitive array coupled to the charge pump such that the capacitive array is charged when power is supplied by the host system.

6. The storage subsystem as in claim **1**, wherein the non-volatile storage medium comprises flash memory.

7. The storage subsystem as in claim **1**, wherein the non-volatile storage medium comprises a magnetic medium.

8. The storage subsystem as in claim **1**, wherein the storage subsystem is a flash memory card.

9. The storage subsystem as in claim **1**, wherein the charge pump and the voltage detection circuit are integrated within a common analog application-specific integrated circuit (ASIC).

10. The storage subsystem as in claim **1**, wherein the charge pump circuit comprises a step-up/step-down DC-to-DC converter.

11. The storage subsystem as in claim **1**, further comprising a voltage regulator connected between the charge pump circuit and the controller to further regulate the regulated power signal provided to the controller.

12. A method of responding to an anomaly in a power signal provided by a host system to a storage subsystem, the method comprising, within the storage subsystem:

receiving the power signal from the host system, said host system being separate from the storage subsystem and pluggably connecting to the storage subsystem;

detecting the anomaly in the power signal with a detection circuit of the storage subsystem;

while the anomaly is detected by the detection circuit, asserting a signal to the host system to inhibit the host system from writing data to the storage subsystem; and

during the anomaly, providing power to a controller of the storage subsystem from at least one source of backup power contained within storage subsystem, to allow the storage subsystem to complete operations that were in progress when the anomaly was detected.

13. The method of claim **12**, wherein the at least one source of backup power comprises a charge pump circuit.

14. The method of claim **12**, wherein the at least one source of backup power further comprises a rechargeable battery embedded within the storage subsystem.

15. The method of claim **12**, wherein the at least one source of backup power further comprises a capacitive array embedded within the storage subsystem.

16. The method of claim **12**, wherein the charge pump circuit comprises a step-up/step-down DC-to-DC converter.

17. The method of claim **12**, wherein the step of providing power to a controller of the storage subsystem from at least one source of backup power is performed for a sufficient time period to substantially ensure that the storage subsystem will complete all outstanding operations.

18. The method of claim **12**, wherein the storage subsystem is a solid state nonvolatile memory card.

19. The method of claim **12**, wherein the storage subsystem is a disk drive.

20. The method of claim **12**, wherein the signal is a busy signal used to notify the host system that the storage subsystem is currently in a busy state.

21. The method of claim **12**, wherein the signal is provided to the host system on a ready/busy signal line of a standard card interface that interconnects the host system and the storage subsystem.

22. The method of claim **12**, wherein the signal is generated by a logic circuit that generates the signal when either or both of the following occur: (a) a busy signal is generated by the detection circuit; (b) a busy signal is generated by the controller.

23. The method of claim **12**, wherein the anomaly is a termination of power from the host system.

24. The method of claim **23**, wherein the method further comprises the storage subsystem using the power from the at least one source of backup power to perform a shut down sequence following completion of said operations.

25. The method of claim **12**, wherein, by asserting the signal to the host system, the storage subsystem additionally inhibits the host system from reading data from the storage subsystem.

26. The storage subsystem as in claim **1**, wherein the charge pump circuit is responsive to termination of the power signal from the host system by continuing to provide power to the controller for at least a time period needed to complete all outstanding operations.

27. The storage subsystem as in claim **1**, wherein the storage subsystem is responsive to termination of the power signal from the host system by using backup power provided by the charge pump circuit to, at least, complete an outstanding write operation.

28. The storage subsystem as in claim **1**, wherein the storage subsystem is responsive to termination of the power signal from the host system by using backup power provided by the charge pump circuit to, at least, perform a shut down sequence.

29. The storage subsystem as in claim **1**, wherein the storage subsystem is a solidstate memory card that plugs into a slot of the host system.

30. The storage subsystem as in claim **29**, wherein the controller writes data to, and reads data from, the non-volatile storage medium in response to commands received from the host system.

31. The storage subsystem as in claim **29**, wherein the memory card complies with at least one of the following card specifications: CompactFlash, PCMCIA, SmartMedia, MultiMediaCard, SecureDigital, Memory Stick.

32. The storage subsystem as in claim **1**, wherein the signal asserted by the voltage detection circuit is provided on a ready/busy signal line used to inform the host system of whether the storage subsystem in ready to receive a next command.

33. A solid state memory subsystem, comprising:

a solid state, non-volatile memory array;

a controller that writes data to, and reads data from, the non-volatile memory array in response to operations initiated by a host system;

a power regulation circuit that receives a power signal from the host system and generates a regulated power signal that is provided to the controller, wherein the power regulation circuit is capable of maintaining the regulated power signal to the controller when the power signal from the host system is interrupted, such that the power regulation circuit acts as a backup power supply when power from the host system is interrupted;

a voltage detection circuit that monitors the power signal from the host system to detect anomalies therein; and

a signal generation circuit that generates a busy signal to the host system when either or both of the following occur: (a) an anomaly is detected by the voltage detection circuit, (b) the controller is in a busy state.

34. The solid state memory subsystem as in claim **33**, wherein the busy signal is a signal that, when asserted, stops the host system from instructing the memory subsystem to perform memory access operations.

35. The solid state memory subsystem as in claim **33**, further comprising a housing that houses the non-volatile memory array, the controller, the power regulation circuit, the voltage detection circuit, and the signal generation circuit, said housing configured for insertion into a slot of the host system.

36. The solid state memory subsystem as in claim **33**, wherein the memory subsystem is a memory card that complies with a CompactFlash, PCMCIA, SmartMedia, MultiMediaCard, SecureDigital or Memory Stick card specification.

37. The solid state memory subsystem as in claim **33**, wherein the power regulation circuit comprises a charge pump circuit.

38. The solid state memory subsystem as in claim **33**, wherein the busy signal is provided to the host system on a ready/busy signal line of an industry-standard interface.

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