

FORWARD ERROR CORRECTION FOR MEMORIES

CROSS-REFERENCES TO RELATED APPLICATIONS

[0001] This application claims priority from co-pending U.S. Provisional Patent Application No. 61/234,911, filed August 18, 2009, entitled "FORWARD ERROR CORRECTION FOR FLASH MEMORIES" (Attorney Docket No. 026258-003700US), which is hereby incorporated by reference, as if set forth in full in this document, for all purposes.

BACKGROUND

[0002] The present invention relates to forward error correction (FEC) in general and, in particular, to FEC for flash memory. The advancements of flash memory technology in recent years has dramatically increased storage capacity and decreased the cost of non-volatile semiconductor memory. This has made Solid State Drives (SSDs) (typically a flash memory-based non-volatile memory system) an emerging substitute for magnetic Hard Disk Drive (HDD).

[0003] The use of FEC to enhance the reliability and longevity of flash memory is one of the challenges for making SSDs perform on par with HDDs.

SUMMARY

[0004] Methods, systems, and devices are described for forward error correction for flash memory. Encoded data from flash memory may be retrieved to generate a number of data streams (which may, but need not be, partially decoded). At each of a number of error detection sub-modules operating in parallel, a different one of the data streams is processed. Each error detection sub-module may detect whether a portion of the respective received stream contains an error, and forward the portion of the respective stream containing an error to an error correction module. An error correction module, physically separate from the error detection sub-modules, may correct the forwarded portions of the respective streams.

[0005] The age and error rate associated with the flash memory may be monitored, and a coding rate may be dynamically adapted to account for these factors. The error rate may be monitored on a per-sector basis and, therefore, the coding rate may be adapted on a per-sector

(or per-set of sectors) basis. As the error rate increases in certain sets of sectors, additional error-correction sub-modules assigned to those sectors may be powered-up to handle the increased error rate. In one example, there are fewer error correction sub-modules than error detection sub-modules; each error correction sub-module may be time-shared by a number of error detection sub-modules. Also, it is worth noting that the associations between flash memory sectors, error detection sub-modules, and error correction sub-modules may be changed dynamically in response to age and error rates, as well.

BRIEF DESCRIPTION OF THE DRAWINGS

[0006] A further understanding of the nature and advantages of the present invention may be realized by reference to the following drawings. In the appended figures, similar components or features may have the same reference label. Further, various components of the same type may be distinguished by following the reference label by a dash and a second label that distinguishes among the similar components. If only the first reference label is used in the specification, the description is applicable to any one of the similar components having the same first reference label irrespective of the second reference label.

[0007] FIG. 1 is a block diagram of a flash memory decoder system according to various embodiments of the invention.

[0008] FIG. 2 is a block diagram of a flash memory decoder according to various embodiments of the invention.

[0009] FIG. 3 is a block diagram of a flash memory decoder system illustrating error detection and correction sub-modules according to various embodiments of the invention.

[0010] FIG. 4 is a block diagram of a flash memory decoder system illustrating an architecture for a decoder controller according to various embodiments of the invention.

[0011] FIG. 5 is a flowchart illustrating a method of decoding data from a flash memory according to various embodiments of the invention.

[0012] FIG. 6 is a flowchart illustrating a method of age responsive decoding of data from a flash memory according to various embodiments of the invention.

[0013] FIG. 7 is a flowchart illustrating a method of decoding data from a flash memory responsive to error rate according to various embodiments of the invention.

DETAILED DESCRIPTION

[0014] Methods, systems, and devices are described for forward error correction for flash memory. Encoded data from flash memory may be processed to generate a number of data streams. At each of a number of error detection sub-modules operating in parallel, a different
5 one of the data streams is processed. Each error detection sub-module may detect whether a portion of the respective received stream contains an error, and forward the portion to an error correction module. An error correction module, physically separate from the error detection sub-modules, may correct the forwarded portions. The age and error rate associated with the flash memory may be monitored, and a coding rate or other aspects may be
10 dynamically adapted to account for these factors.

[0015] This description provides example embodiments only, and is not intended to limit the scope, applicability, or configuration of the invention. Rather, the ensuing description of the embodiments will provide those skilled in the art with an enabling description for implementing embodiments of the invention. Various changes may be made in the function
15 and arrangement of elements without departing from the spirit and scope of the invention.

[0016] Thus, various embodiments may omit, substitute, or add various procedures or components as appropriate. For instance, it should be appreciated that in alternative embodiments the methods may be performed in an order different from that described, and that various steps may be added, omitted, or combined. Also, features described with respect
20 to certain embodiments may be combined in various other embodiments. Different aspects and elements of the embodiments may be combined in a similar manner.

[0017] It should also be appreciated that the following systems, methods, and software may individually or collectively be components of a larger system, wherein other procedures may take precedence over or otherwise modify their application. Also, a number of steps may be
25 required before, after, or concurrently with the following embodiments.

[0018] Although much of the following discussion relates specifically to flash memory, aspects of the inventions are applicable to other forms of solid state memory. Generally, there are two predominant types of flash memory architectures: NOR and NAND. For the purposes of this disclosure, much discussion is directed to NAND-type flash, while again
30 noting that principles set forth herein have wider applicability.

[0019] There are two primary NAND flash technologies. The earlier versions of NAND flash were Single-Level Cell (SLC). With SLC Flash, there is only one programmed state in addition to the erased state. The total of two states allows a single data bit to be stored in the

memory cell. The desire for higher density led to the more advanced Multiple-Level Cell (MLC). With MLC flash, there are multiple programmed states in addition to the erased state which allows multiple bits to be stored per memory cell.

5 [0020] Because of this increase in density and the related issues in manufacturing, one of the challenges for flash memory is to maintain high reliability and longevity. The deterioration of the oxide over time, and the disruptions from neighboring memory pages, can lead to data retention and corruption issues translating into bit errors. While the chances of any given data bit being corrupted is quite small, the vast number of data bits in a storage system makes the likelihood of data corruption a very real possibility. FEC may be one of
10 the tools used to address these bit errors to improve the reliability and lifespan of flash memory.

[0021] Systems, devices, methods, and software are described for FEC for flash memory. Turning first to **FIG. 1**, a flash memory system 100 is illustrated. The system includes an encoder 105, flash memory 110, a decoder 115, and a controller 120. This flash memory
15 system 100 may be a stand-alone device, or may be integrated (in whole or in part) with a computer, server, phone or mobile device, tablet, television, or any other computing device.

[0022] Each of these system 100 components may be in communication with each other. The encoder 105, decoder 115, and controller 120 may, individually or collectively, be implemented with one or more Application Specific Integrated Circuits (ASICs) adapted to
20 perform some or all of the applicable functions in hardware. Alternatively, the functions may be performed by one or more other processing units (or cores), on one or more integrated circuits. In other embodiments, other types of integrated circuits may be used (e.g., Structured/Platform ASICs, Field Programmable Gate Arrays (FPGAs), and other Semi-Custom ICs), which may be programmed in any manner known in the art. The functions of
25 each unit may also be implemented, in whole or in part, with instructions embodied in a memory, formatted to be executed by one or more general or application-specific processors.

[0023] The encoder 105 may receive data to be stored, and encode the data (e.g., adding parity information) for storage in the flash memory 110 as encoded data. The decoder 115 may include a number of sub-components (not shown). An embodiment of the decoder 115
30 includes an error correction module in communication with and physically separate from an error detection module. The decoder 115 may process the encoded data to generate a number of data streams (which may, but need not be, decoded in whole or in part). The decoder 115 may process each stream at a different error detection sub-module operating in parallel in the

decoder 115. Each error detection sub-module may detect whether a portion of the respective received stream contains an error, and then forward the portion of the respective received stream containing an error to the error correction module. The error correction module may correct the forwarded portions of the respective received streams containing an error.

5 **[0024]** There are a number of different FEC schemes and codes that may be used in the flash memory system 100 introduced above. The system 100 functionality may be also be leveraged in a number of ways. For example, the error detection module may detect and flag bit errors, and this may allow sectors of memory with errors exceeding a threshold amount to be avoided by replacing such sectors with other sectors from a pool of available substitutes.

10 The encoder 105 may, also or alternatively, change the code rate for the error-laden sections. As flash become more dense, the inherent bit error probability becomes higher.

[0025] Some simple FEC coding may be used to clean up these errors. The Hamming Code, with correction capacity of 1 bit and detection capability of 2, may be used with flash memory 110. With the desire for improving the performance, as well as the increased
15 probability of inherent bit errors because of the denser memories, Bose Chaudhuri Hocqunghem (BCH) codes may be used, including the binary BCH and non-binary BCH (Reed Solomon (RS)) codes. These codes offer a higher correction capacity in comparison to the Hamming Code.

[0026] BCH encoding/decoding architectures may be the foundation of error correction in
20 flash memory. However, there are more advanced coding options that may in some instances provide better performance than BCH codes. These codes may be used in flash memory 110, particularly for higher density flash and in applications where performance demands increase. Convolutional Turbo Codes (CTCs), Turbo Product Codes (TPCs), and low density parity check codes (LDPCs) are examples of the coding schemes that may be used. These state-of-
25 the-art codes perform very close to the theoretical limits (Shannon Limits) of error correction, providing very high coding gain and improvement in Bit Error Rate (BER) performance for a given amount of redundancy.

[0027] Flash memory does have an inherent probability of error. Depending on the flash technology, this error rate may typically be somewhere between $1e-5$ and $1e-8$. To be able to
30 match an HDD read/write bit error rate of $1e-15$, a FEC scheme may be used. The measure of how good a job a code can perform in increasing the reliability depends upon its correction capacity. If the probability of bit error for flash memory 110 is p and the correction capacity

of the code is t bits over a codeword length of n bits, the probability of making an error may be expressed as:

$$P_{\text{decoded}} = \sum_{i=t+1}^n p^i * (1-p)^{n-i} \quad (1)$$

5 **[0028]** From equation (1), for a given p the higher the correction capacity of the code, the smaller the probability of error after the decoding will be. The correction capacity can be expressed as the number of bits a code can correct over a codeword length, or an input BER, or probability of error that it can take down to a certain target decoded BER. The advanced codes may correct more errors over a certain length, or take a higher input BER to create the same decoded BER.

10 **[0029]** There is incentive to use advanced codes for flash memory 110 even with not so dense memories. If the inherent error performance of flash memory 110 stayed at a certain low level, there would probably be decreased need for advanced codes. But, in practice, flash memory 110 performance tends to degrade over time. This means that even with an advanced code to help improve the reliability of a flash memory 110, over time the flash
15 memory 110 may become lossy and, once the error rate is high enough, it may be beyond repair by the code being used.

[0030] In one example, the rate of errors or age of the flash memory 110 may be monitored, and the coding rate for data to be stored on the flash memory 110 may be modified in response thereto. Thus, a more robust coding rate may be used as the decoded
20 error rate increases. The error monitoring may take place on a per-sector basis, and the code rate modification may similarly take place on a per-sector basis. In another example, the rate of errors or age of the flash memory 110 may be monitored, and error correction sub-modules may be powered-up in response thereto. Power savings may be achieved by keeping certain error correction sub-modules in an inactive mode until the flash memory reaches a certain
25 age.

[0031] As noted, the flash memory 110 may be partitioned into a pool of small fixed-size sectors, and FEC may be applied on a sector-by-sector basis. The flash memory 110 size may be defined by the number of sectors that it contains. As there is a chance of sectors going bad over time, there may be a reserve/spare sector pool that allows the controller to
30 replace the bad sectors by the spares as needed to extend the life of the flash. The error detection sub-module and error correction sub-modules may be dynamically assigned to various sectors, and the number powered-on may be increased or decreased.

[0032] A wear leveling technique may be used to make sure that various areas/sectors of the Flash “age” at a similar rate. Instead of the same sector being used over and over again, the read/writes are spread over much or the entire flash. And this translates into the probability of any sector being good (p_{good}) may be substantially the same for the various sectors in flash memory 110. If the size of the flash is N sectors and there are Δ spare sectors, the probability that the flash is still usable after time t is:

$$P_{usable} = \sum_{i=N}^{N+\Delta} (C_i^{N+\Delta} * (p_{good})^i * (1 - p_{good})^{N+\Delta-i}) \quad (2)$$

[0033] p_{good} may be a function of use time for the flash memory 110 sector. This is a component that is dependent upon the correction capacity of the code used. Thus, even with the spare sectors and the wear-leveling technique, the codes may play a key role in the flash being usable after a certain use time.

[0034] One of the concerns regarding advanced codes is how they fit into the sector sizes and overhead requirements of some flash memory architectures. TPC and LDPC codes offer an excellent degree of freedom in selecting the various code parameters like information block size, coded block size, and correction capacity, and would allow customization to suit any number of flash configurations.

[0035] FIG. 2 is a block diagram 200 of a flash memory decoder 115-a according to various embodiments of the invention. The flash memory decoder 115-a may, for example, be the decoder 115 of FIG. 1, although flash memory decoder 115-a may be implemented in a number of other systems and devices, as well. The flash memory decoder 115-a includes a decoder module 205, an error detection module 210, and an error correction module 215, and each of may be in communication with each other. In one example, the error detection module 210 includes a number of sub-modules configured to detect errors on decoded streams of data. The error correction module 215 may be physically separate from each error detection sub-module, and may also include a number of sub-modules (each of which may be time-shared by a number of error detection sub-modules).

[0036] These components and sub-modules therein may, individually or collectively, be implemented with one or more Application Specific Integrated Circuits (ASICs) adapted to perform some or all of the applicable functions in hardware. Alternatively, the functions may be performed by one or more other processing units (or cores), on one or more integrated circuits. In other embodiments, other types of integrated circuits may be used (e.g., Structured/Platform ASICs, Field Programmable Gate Arrays (FPGAs), and other Semi-

Custom ICs), which may be programmed in any manner known in the art. The functions of each unit may also be implemented, in whole or in part, with instructions embodied in a memory, formatted to be executed by one or more general or application-specific processors.

5 **[0037]** The decoder module 205 may receive encoded data from flash memory, and process the received encoded data to generate a number of data streams. In one embodiment, the decoder module processor may buffer, de-interleave, or perform certain aspects of the decoding process, and thereby generate decoded (or partially decoded) data streams. As noted, the error detection module 210 may include a number of error detection sub-modules operating in parallel. Each (or a subset) of the error detection sub-modules may receive a
10 different one of the data streams, and evaluate the respective stream to determine whether a portion of the stream contains an error. Each error detection sub-module may forward the portion of the respective received stream containing an error to the error correction module 215 (bypassing the error correction module 215 with the error-free portions). The error correction module 215 corrects the received portions of the respective received streams
15 containing an error. As noted above, the error correction module 215 may include a number of sub-modules (each of which may be time-shared by a number of error detection sub-modules).

20 **[0038]** FIG. 3 is a block diagram illustrating an example of an architecture for a flash memory decoder system 300 more particularly illustrating error detection and correction sub-modules. The flash memory decoder system 300 may, for example, be the system 100 of FIG. 1. The flash memory decoder system 300 includes flash memory 110-a, a decoder module 205-a, an error detection module 210-a, an error correction module 215-a, a controller 120-a, and an encoder 105-a. Each of these components may be in communication with each other.

25 **[0039]** The flash memory 110-a includes a number of different sets of one or more active sectors 305. The decoder module 205-a includes a number of decoder sub-modules 310, and each decoder sub-module 310 may be associated with a different set of sectors 305. The error detection module 210-a includes a number of error detection sub-modules 315, and each decoder sub-module 310 may be associated with a different set of sectors 305. Thus,
30 encoded data may be read from a set of one or more of sectors 305 (e.g., sector(s) 305-a) by a decoder sub-module 310 (e.g., decoder sub-module 310-a), and processed (e.g., buffered, de-interleaved, decoded to some extent, etc.) to generate a data stream. The data stream may be forwarded to an error detection sub-module 315 (error detection sub-module 315-a). Thus, encoded data from a set of one or more of sectors 305-a may be sent to an error detection

sub-module 315-a. Different sets of sectors 305 may each send their respective data via different decoder sub-modules 310, as illustrated. In one embodiment, each error detection sub-module 315 is distinct from each other. In other embodiments, the decoder sub-module 310 and error detection sub-module 315 may be integrated to varying degrees.

5 **[0040]** Each error detection sub-module 315 may evaluate the respective stream to determine whether a portion of the stream contains an error. Each error detection sub-module 315 may forward the portion of the respective received stream containing an error to the error correction module 215-a (bypassing the error correction module 215 with the error-free portions). The error correction module 215-a includes a number of error correction sub-
10 modules 320, each error correction sub-module 320 responsible for handling the errors from a number of error detection sub-modules 315 (e.g., error correction sub-module 320 may correct errors from error detection sub-modules 315-a, -b, and -c). Error correction sub-modules 320 may correct the received portions of the respective received streams containing an error. Each error correction sub-module 320 may receive portions of streams with errors,
15 and these portion may have been detected in parallel.

[0041] Controller 120-a may perform a number of functions in the decoder process. Controller 120-a may dynamically modify the error detection sub-modules 315 and the error correction sub-modules 320 assigned to sectors 305 of flash memory 110-a. The controller 120-a may selectively power-up one or more of the error correction sub-modules 320
20 responsive to a monitored age or error rate associated with the flash memory 110-a. The controller 120-a may perform this monitoring on a per-sector basis, and the error correction sub-modules 320 may be powered-up to serve the sectors 305 where the error rates exceed a threshold. The controller 120-a may adapt the coding rate to be used by the encoder responsive to a monitored age or error rate associated with the flash memory 110-a. The
25 controller 120-a may perform this monitoring on a per-sector basis, and the controller 120-a may adapt the coding rate on a per sector basis.

[0042] **FIG. 4** is a block diagram of a flash memory decoder system 400 illustrating certain controller functionality according to various embodiments of the invention. The system 400 includes an encoder 105-b, flash memory 110-b, a decoder 115-b, and a controller 120-b.
30 This system 400 may be an example of the system 100 of FIG. 1, and a component of this system 400 may have the same functionality as the counterpart component from FIG. 1 This flash memory system 400 may be a stand-alone device, or may be integrated (in whole or in part) with a computer, server, phone, mobile device, tablet, television, or any other computing device.

[0043] The controller 120-b includes an adaptive encoding rate controller 405, a power controller 410, a write controller 415, a read controller 420, an age monitoring module 425, and an error monitoring module 430. The age monitoring module 425 may monitor an age associated with the flash memory 110-b. This may be a time since manufacture, a time since first use, an amount of use, or any other metric which corresponds to the aging of the flash memory 110-b. This monitoring may involve direct monitoring of the flash memory 110-b itself, or may be based on reports from the encoder 105-b, decoder 115-b, or other components of the system.

[0044] The error monitoring module 430 may monitor an amount of errors associated with the flash memory 110-b. This monitoring may measure errors over a variety of time periods and metrics, and may be translated into an error rate. The monitoring may be performed on a per-sector (or per set of sectors) basis. A number of sampling and averaging techniques may be used. This monitoring may involve direct monitoring of the decoder 115-b itself, or may be based on reports from the decoder 115-b or other components of the system.

[0045] The adaptive encoding rate controller 405 may receive information on the rate and/or amount of errors from the error monitoring module 430. The adaptive encoding rate controller 405 may modify a coding rate to be used by the encoder 105-b when the monitored rate and/or amount of errors exceeds a threshold. The monitoring of errors may be performed on a per-sector, per set of sectors, or other regional basis. Thus, the coding rate to be used by the encoder 105-b may be modified when the monitored rate of errors for the applicable region exceeds a threshold. In some embodiments, the coding rate may be adapted to be more, or less, robust; in other embodiments, the adaptation is only to make the coding rate more robust. The adaptive encoding rate controller 405 may receive information on the age of the flash memory 110-b from the age monitoring module 425. The adaptive encoding rate controller 405 may adapt the coding rate based on this monitoring (e.g., implementing a more robust coding rate for one or more sectors of the flash memory 110-b when the age exceeds a threshold). There may be a number of different coding rate change thresholds related both to age and error rate. Moreover, these threshold may be adaptive to the amount of flash memory 110-b that remains available (e.g., the margin may be increased when the flash memory is utilized below a threshold amount).

[0046] As noted above, an decoder module 115 may include a number of error correction sub-modules. The power controller 410 may receive information on the age of the flash memory 100-b from the age monitoring module 425. The power controller 410 may selectively power-up (or power-down) one or more of the error correction sub-modules

responsive to an age of the flash memory 110-b. The power controller 410 may receive information on the rate and/or amount of errors from the error monitoring module 430. The power controller 410 may power-up (or power-down) one or more of the error correction sub-modules (e.g., when the monitored rate and/or amount of errors exceeds a threshold). The monitoring of errors may be performed on a per-sector, per set of sectors, or other regional basis. Thus, the power-up or power-down may be specific to a particular error correction sub-module for a given region of flash memory 110-b.

[0047] The write controller 415 may change the sectors of flash memory 110-b to be written to. These changes may be made in response to information from the age monitoring module 425 and error monitoring module 430. The read controller 420 may dynamically change the components of the decoder 115-b to be used to read different sectors of flash memory 110-b (e.g., in FIG. 3, the assignments of the decoder sub-modules 310, error detection sub-modules 315, and error correction sub-modules 320 may be changed in response to code rate modifications, increased errors, or age).

[0048] FIG. 5 is a flowchart illustrating a method 500 of decoding data from a flash memory according to various embodiments of the invention. The method 500 may, for example, be performed in whole or in part by the system 100, 300, or 400 of FIG. 1, 3, or 4 or, more specifically, by the decoder 115 of FIG. 1, 2, or 4.

[0049] At block 505, encoded data from a flash memory is received. At block 510, the received encoded data is processed to generate a number of data streams. The information for each data stream may be a wholly or partially decoded before being forwarded to respective error correction sub-modules. At block 515, at each of a number of error detection sub-modules operating in parallel, a different one of the data streams is processed. Each error detection sub-module is configured to: detect whether a portion of the respective received stream contains an error, and forward the portion of the respective received stream containing an error to an error correction module. At block 520, at the error correction module physically separate from the error detection sub-modules, the forwarded portions of the respective received streams containing an error are corrected.

[0050] FIG. 6 is a flowchart illustrating a method of age responsive decoding of data from a flash memory according to various embodiments of the invention. The method 600 may, for example, be performed in whole or in part by the system 100, 300, or 400 of FIG. 1, 3, or 4. The method 600 may be an example of the method 500 of FIG. 5.

[0051] At block 605, an age of a flash memory is monitored. At block 610, the coding rate for data to be encoded and stored in the flash memory is modified responsive to a first age threshold of the flash memory. At block 615, data is encoded at the modified rate, and the encoded data is stored on the flash memory. At block 620, one or more error correction sub-modules of an error correction module are powered-up from an inactive mode responsive to a second age threshold of the flash memory.

[0052] At block 625, the encoded data from the flash memory is processed to generate a number of partially decoded data streams. At block 630, at each of a number of error detection sub-modules operating in parallel, a different one of the data streams is processed. At block 635, a determination is made at each error detection sub-module whether a portion of the respective received stream contains an error. At block 640, error detection sub-modules forward those portions of the respective streams containing an error to the error correction module physically separate from the error detection sub-modules. At block 645, the error-free portions are forwarded to bypass the error correction module. At block 650, the portions of the respective received streams containing an error are corrected with the powered-up error correction modules and additional error correction modules.

[0053] FIG. 7 is a flowchart illustrating a method of decoding data from a flash memory responsive to error rate according to various embodiments of the invention. The method 700 may, for example, be performed in whole or in part by the system 100, 300, or 400 of FIG. 1, 3, or 4. The method 700 may be an example of the method 500 of FIG. 5 or the method 600 of FIG. 6.

[0054] At block 705, a rate of errors from an error detection module is monitored for each of a number of sectors of the flash memory. At block 710, the coding rate for data to be encoded and stored in one or more sectors is modified responsive to the monitoring of first error rate threshold for the one or more sectors. At block 715, data is encoded at the modified rate and stored in the one or more sectors.

[0055] At block 720, an error correction sub-module assigned to the one or more sectors are powered-up from an inactive mode responsive to the monitoring of a second error rate threshold for the one or more sectors. At block 725, the encoded data from the one or more sectors is decoded to generate a decoded data stream. At block 730, at one of a number of error detection sub-modules operating in parallel, the decoded data stream is processed. At block 735, a determination is made by the error detection sub-module that a portion of the respective received stream contains an error. At block 740, the portion of the received stream

containing an error is forwarded to the powered-up error correction sub-module. At block 745, the forwarded portion is corrected with the powered-up error correction sub-module.

[0056] It should be noted that the methods, systems, and devices discussed above are intended merely to be examples. It must be stressed that various embodiments may omit, substitute, or add various procedures or components as appropriate. For instance, it should be appreciated that, in alternative embodiments, the methods may be performed in an order different from that described, and that various steps may be added, omitted, or combined. Also, features described with respect to certain embodiments may be combined in various other embodiments. Different aspects and elements of the embodiments may be combined in a similar manner. Also, it should be emphasized that technology evolves and, thus, many of the elements are examples and should not be interpreted to limit the scope of the invention.

[0057] Specific details are given in the description to provide a thorough understanding of the embodiments. However, it will be understood by one of ordinary skill in the art that the embodiments may be practiced without these specific details. For example, well-known circuits, processes, algorithms, structures, and techniques have been shown without unnecessary detail in order to avoid obscuring the embodiments.

[0058] Also, it is noted that the embodiments may be described as a process which is depicted as a flow diagram or block diagram. Although each may describe the operations as a sequential process, many of the operations can be performed in parallel or concurrently. In addition, the order of the operations may be rearranged. A process may have additional steps not included in the figure.

[0059] Moreover, as disclosed herein, the term "memory" or "memory unit" may represent one or more devices for storing data, including read-only memory (ROM), random access memory (RAM), magnetic RAM, core memory, magnetic disk storage mediums, optical storage mediums, flash memory devices, or other computer-readable mediums for storing information. The term "computer-readable medium" includes, but is not limited to, portable or fixed storage devices, optical storage devices, wireless channels, a sim card, other smart cards, and various other mediums capable of storing, containing, or carrying instructions or data.

[0060] Furthermore, embodiments may be implemented by hardware, software, firmware, middleware, microcode, hardware description languages, or any combination thereof. When implemented in software, firmware, middleware, or microcode, the program code or code

segments to perform the necessary tasks may be stored in a computer-readable medium such as a storage medium. Processors may perform the necessary tasks.

5 [0061] Having described several embodiments, it will be recognized by those of skill in the art that various modifications, alternative constructions, and equivalents may be used without departing from the spirit of the invention. For example, the above elements may merely be a component of a larger system, wherein other rules may take precedence over or otherwise modify the application of the invention. Also, a number of steps may be undertaken before, during, or after the above elements are considered. Accordingly, the above description should not be taken as limiting the scope of the invention.

WHAT IS CLAIMED IS:

- 1 1. A flash memory decoder comprising:
2 a decoding module configured to:
3 receive encoded data from the flash memory; and
4 decode the received encoded data to generate a plurality of partially
5 decoded data streams;
6 an error detection module communicatively coupled with the decoding
7 module, and comprising a plurality of error detection sub-modules operating in parallel, each
8 error detection sub-module configured to:
9 receive a different one of the plurality of partially decoded data
10 streams;
11 detect whether a portion of the respective received stream contains an
12 error; and
13 forward the portion of the respective received stream containing an
14 error to an error correction module; and
15 an error correction module, communicatively coupled with and physically
16 separate from the error detection module, and configured to correct the received portions of
17 the respective received streams containing an error.
- 1 2. The flash memory decoder of claim 1, wherein each of the error
2 detection sub-modules is configured to read data from a set of one or sectors of flash memory
3 different from other of the error detection sub-modules.
- 1 3. The flash memory decoder of claim 2, further comprising a read
2 controller configured to dynamically modify the error detection sub-modules assigned to at
3 least a subset of the sectors of flash memory.
- 1 4. The flash memory decoder of claim 1, wherein the error correction
2 module comprises a plurality of error correction sub-modules operating in parallel and fewer
3 in number than the error detection sub-modules.
- 1 5. The flash memory decoder of claim 4, further comprising a power
2 controller configured to selectively power-up one or more of the error correction sub-modules
3 responsive to an age of the flash memory.
- 1 6. The flash memory decoder of claim 4, further comprising:

2 an error monitoring module, communicatively coupled with the error detection
3 module, and configured to monitor a rate of errors from the error detection module,
4 wherein the power controller is configured to selectively power-up one or
5 more of the error correction sub-modules when the monitored rate of errors exceeds a
6 threshold.

1 7. The flash memory decoder of claim 4, further comprising:
2 an error monitoring module, communicatively coupled with the error detection
3 module, and configured to monitor a rate of errors from the error detection module for each
4 of a plurality of sectors of the flash memory,
5 wherein a power controller is configured to selectively power-up an error
6 correction sub-module for assignment to a set of one or more of the monitored sectors when
7 the monitored rate of errors for the set exceeds a threshold.

1 8. The flash memory decoder of claim 4, wherein,
2 each error correction sub-module is assigned a set of two or more error
3 detection sub-modules different from error detection sub-modules associated with other of
4 the error correction sub-modules; and
5 each error correction sub-module is configured to receive portions of the
6 respective received streams containing an error detected in parallel by the set of two or more
7 error detection sub-modules assigned to the respective error correction sub-module.

1 9. The flash memory decoder of claim 1, further comprising a read
2 controller configured to selectively power-down one or more subsets of the error detection
3 sub-modules.

1 10. The flash memory decoder of claim 1, further comprising:
2 the flash memory, communicatively coupled with the decoding module;
3 an encoder, communicatively coupled with the flash memory, and configured
4 to encode data at a coding rate for storage as the encoded data on the flash memory; and
5 an adaptive encoding rate controller configured to modify the coding rate
6 responsive to an age of the flash memory.

1 11. The flash memory decoder of claim 1, further comprising:
2 an error monitoring module, communicatively coupled with the error detection
3 module, and configured to monitor a rate of errors from the error detection module; and

4 an adaptive encoding rate controller configured to modify a coding rate for a
5 flash memory encoding module when the monitored rate of errors exceeds a threshold.

1 12. The flash memory decoder of claim 1, further comprising:
2 an error monitoring module, communicatively coupled with the error detection
3 module, and configured to monitor a rate of errors from the error detection module for each
4 of a plurality of sectors of the flash memory; and
5 an adaptive encoding rate controller configured to modify a coding rate of a
6 set of one or more of the monitored sectors when the monitored rate of errors for the set
7 exceeds a threshold.

1 13. The flash memory decoder of claim 1, wherein each error detection
2 sub-module is configured to direct error-free portions of the respective received streams to
3 bypass the error correction module.

1 14. The flash memory decoder of claim 1, wherein,
2 the error detection module comprises the decoding module; and
3 the encoded data is encoded with a Hamming code, a BCH code, a Turbo
4 code, or a low-density parity check code.

1 15. A system comprising:
2 an encoder configured to encode data for storage on a flash memory;
3 the flash memory, communicatively coupled with the encoding module, and
4 configured to store the encoded data; and
5 a decoder, communicatively coupled with the flash memory, and configured
6 to:
7 retrieve the encoded data from flash memory to generate a plurality of
8 data streams; and
9 process, at each of a plurality of error detection sub-modules of the
10 decoder operating in parallel, a different one of the plurality of data streams, wherein each
11 error detection sub-module is configured to:
12 detect whether a portion of the respective received stream
13 contains an error; and
14 forward the portion of the respective received stream
15 containing an error to an error correction module of the decoder; and

16 correct, with the error correction module physically separate from the
17 error detection module, the forwarded portions of the respective received streams containing
18 an error.

1 16. The system of claim 15, wherein the encoder is further configured to
2 adaptively modify the coding rate responsive to an age of the flash memory or a rate of errors
3 associated with the decoded data.

1 17. A method comprising:
2 receiving encoded data from a flash memory comprising a plurality of data
3 streams;
4 processing, at each of a plurality of error detection sub-modules operating in
5 parallel, a different one of the plurality of data streams, wherein each error detection sub-
6 module is configured to:
7 detect whether a portion of the respective received stream contains an
8 error; and
9 forward the portion of the respective received stream containing an
10 error to an error correction module; and
11 correcting, with the error correction module physically separate from an error
12 detection module, the forwarded portions of the respective received streams containing an
13 error.

1 18. The method of claim 17, further comprising:
2 dynamically modifying the error detection sub-modules assigned to receive
3 data from respective sectors of flash memory.

1 19. The method of claim 17, wherein the error correction module
2 comprises a plurality of error correction sub-modules operating in parallel and fewer in
3 number than the error detection sub-modules.

1 20. The method of claim 19, further comprising:
2 powering-up, from an inactive mode, one or more of the error correction sub-
3 modules responsive to an age of the flash memory.

1 21. The method of claim 19, further comprising:
2 monitoring a rate of errors from the error detection module; and

3 powering-up one or more of the error correction sub-modules when the
4 monitored rate of errors exceeds a threshold.

1 22. The method of claim 19, further comprising:
2 monitoring a rate of errors from the error detection module for each of a
3 plurality of sectors of the flash memory; and
4 powering-up an error correction sub-module for assignment to a set of one or
5 more of the monitored sectors when the monitored rate of errors for the set exceeds a
6 threshold.

1 23. The method of claim 17, further comprising:
2 modifying a coding rate for data to be stored as the encoded data on the flash
3 memory responsive to an age of the flash memory.

1 24. The method of claim 17, further comprising:
2 monitoring a rate of errors from the error detection module; and
3 modifying a coding rate for data to be stored as the encoded data on the flash
4 memory when the monitored rate of errors exceeds a threshold.

1 25. The method of claim 17, further comprising:
2 monitoring a rate of errors from the error detection module for each of a
3 plurality of sectors of the flash memory; and
4 modifying a coding rate for data to be stored as the encoded data on the flash
5 memory when the monitored rate of errors for the set exceeds a threshold.

ABSTRACT OF THE DISCLOSURE

Methods, systems, and devices are described for forward error correction for flash memory. Encoded data from flash memory may be used to generate a number of data streams. At each of a number of error detection sub-modules operating in parallel, a different one of the data streams is processed. Each error detection sub-module may detect whether a portion of the respective received stream contains an error, and forward the portion to an error correction module. The error correction module, physically separate from the error detection sub-modules, may correct the forwarded portions of the respective received streams containing an error. The age and error rate associated with the flash memory may be monitored, and a coding rate or other aspects may be dynamically adapted to account for these factors.

62790421 v1

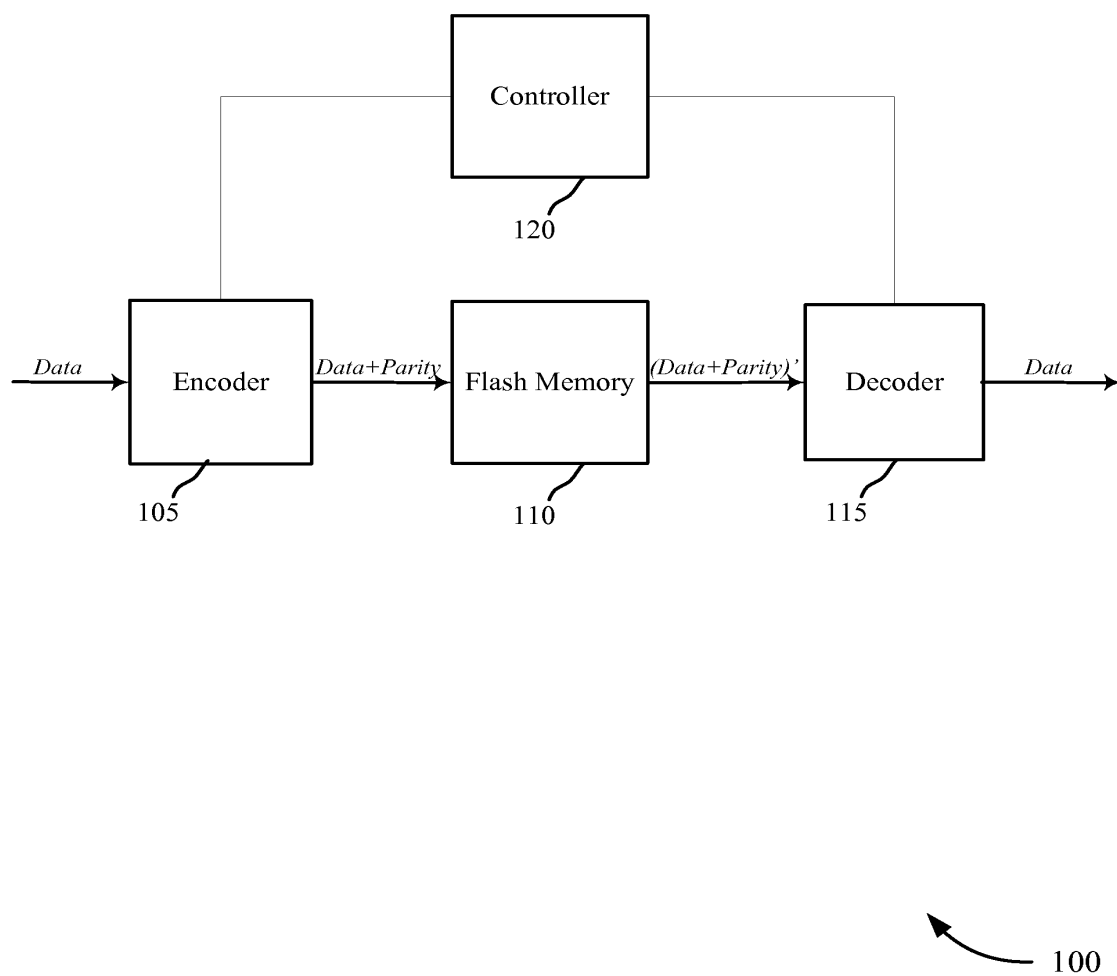


FIG. 1

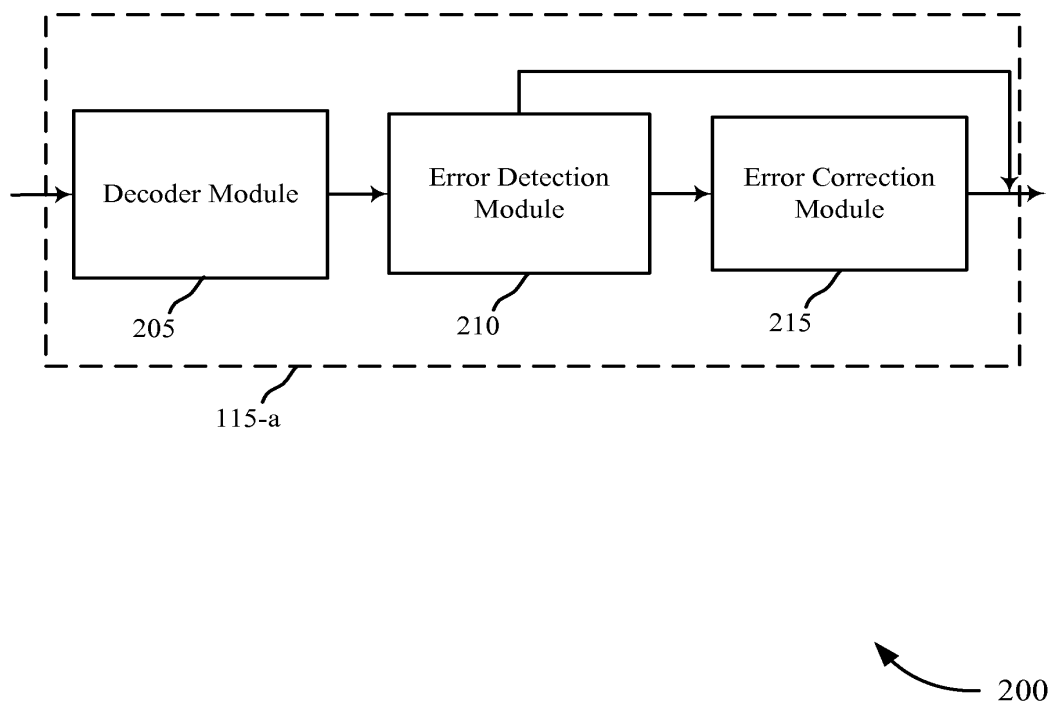


FIG. 2

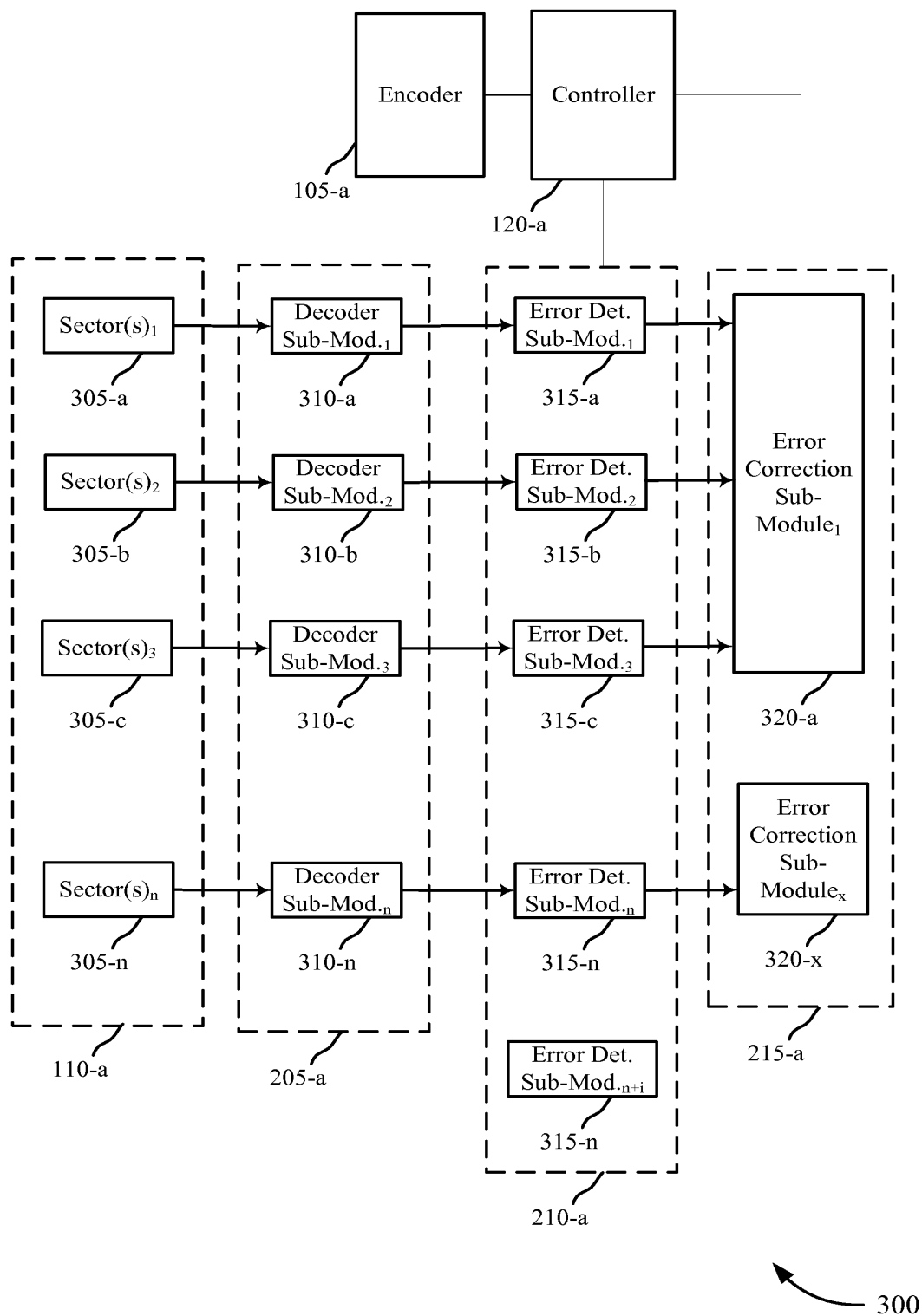
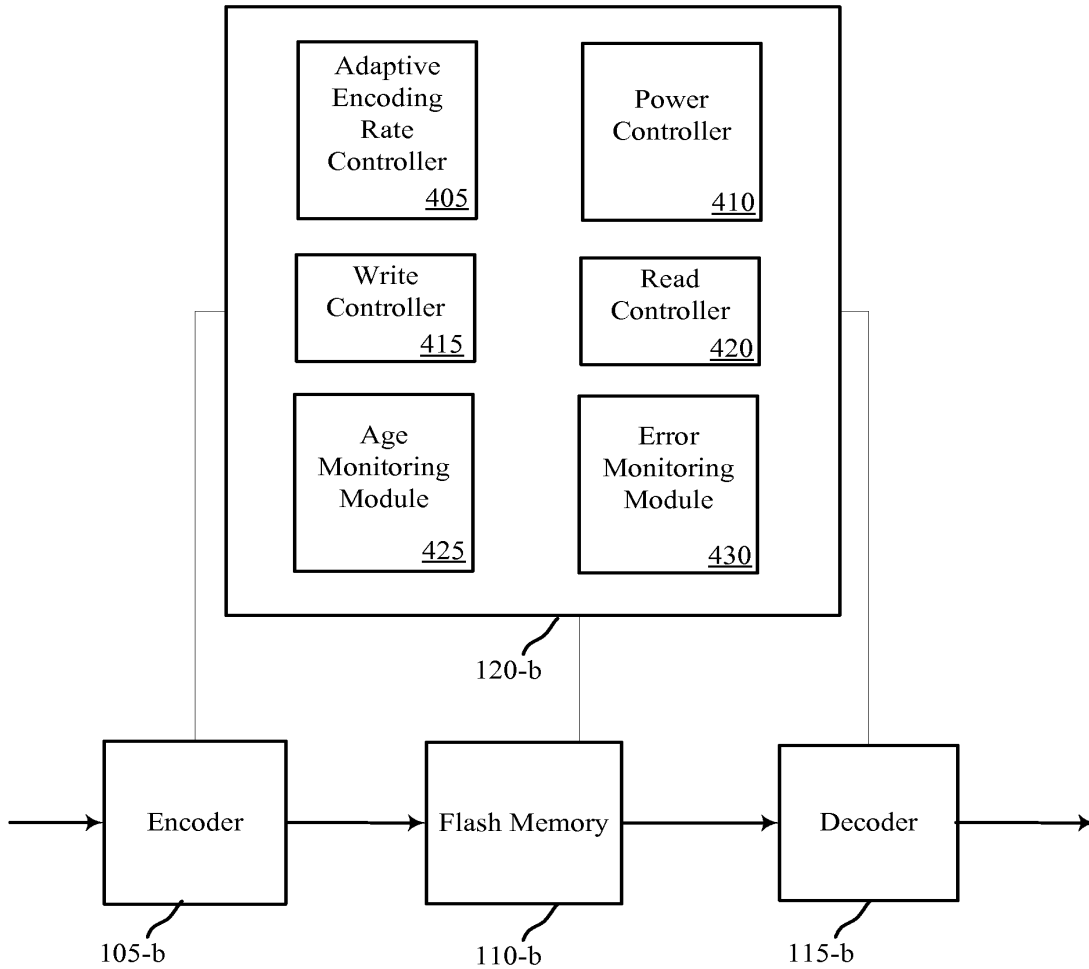


FIG. 3



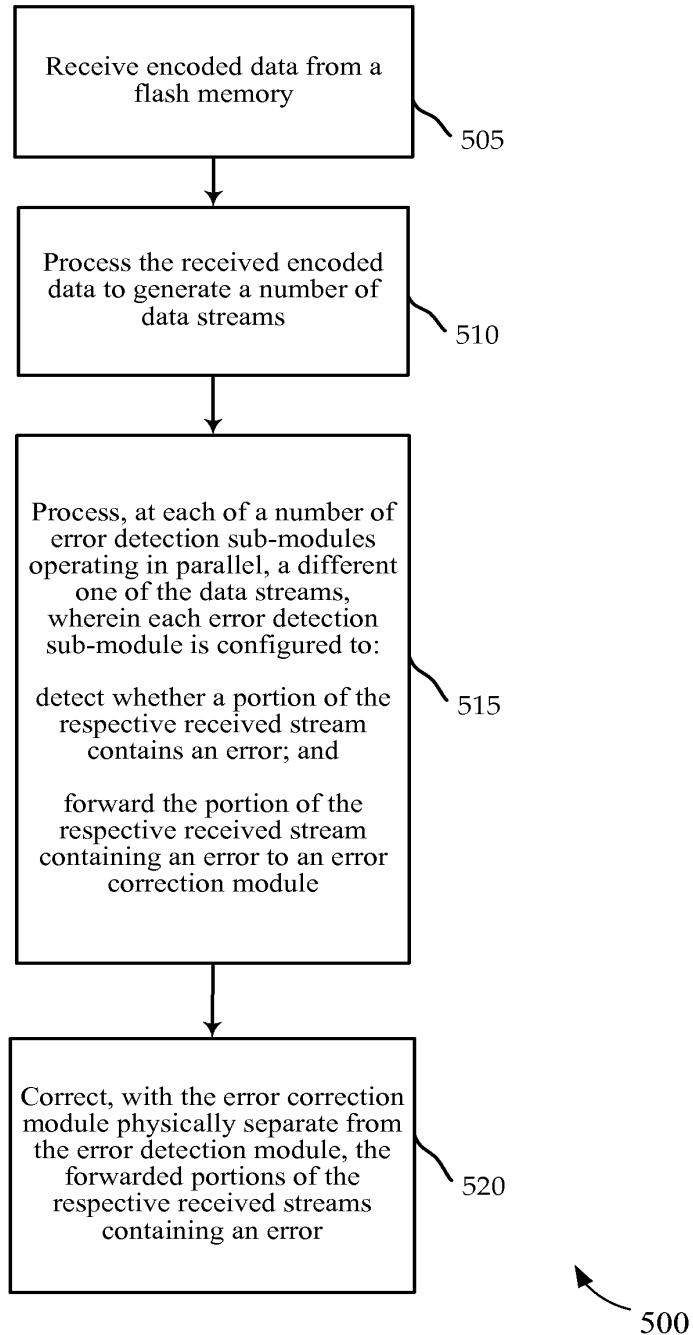


FIG. 5

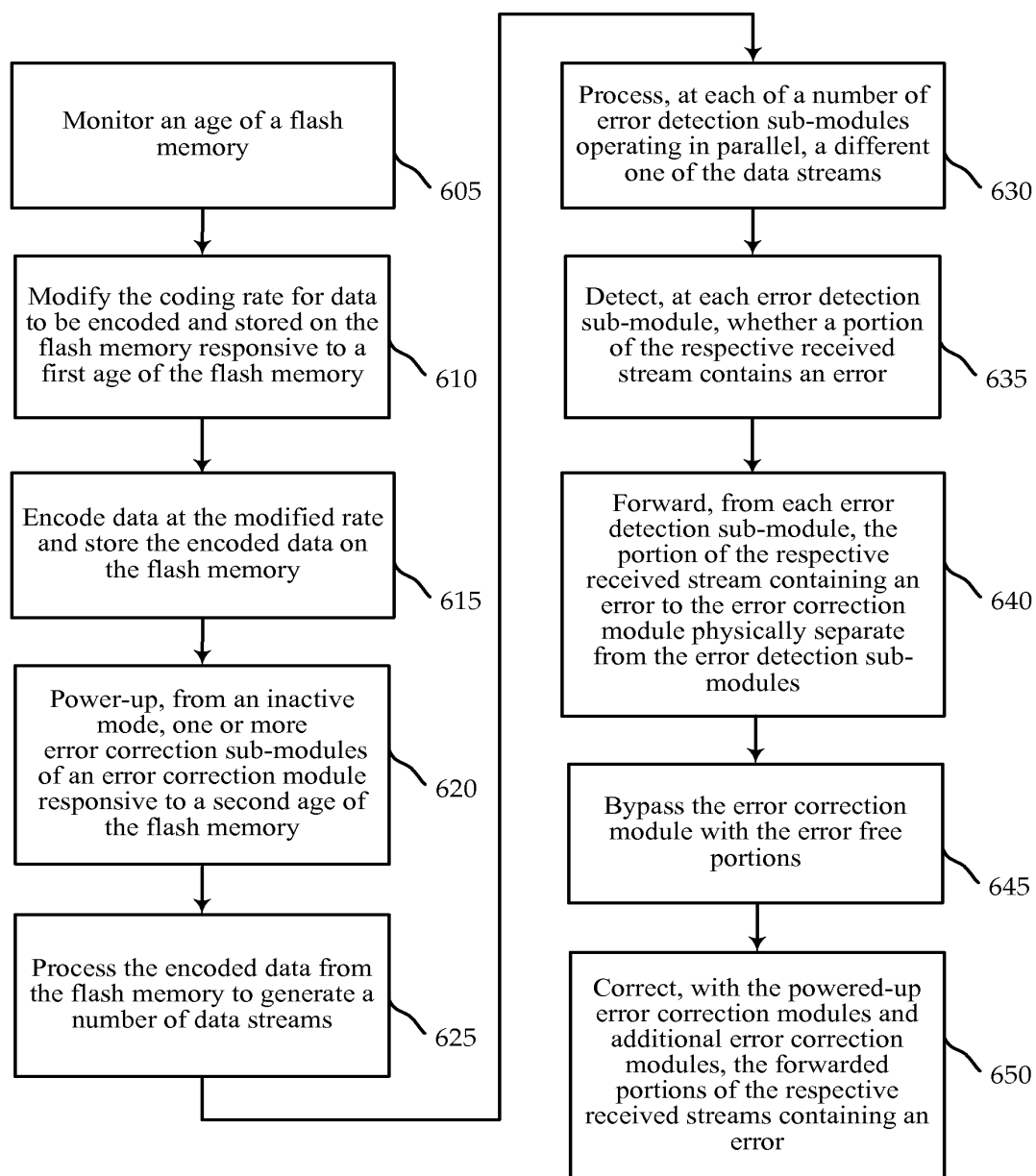


FIG. 6

600

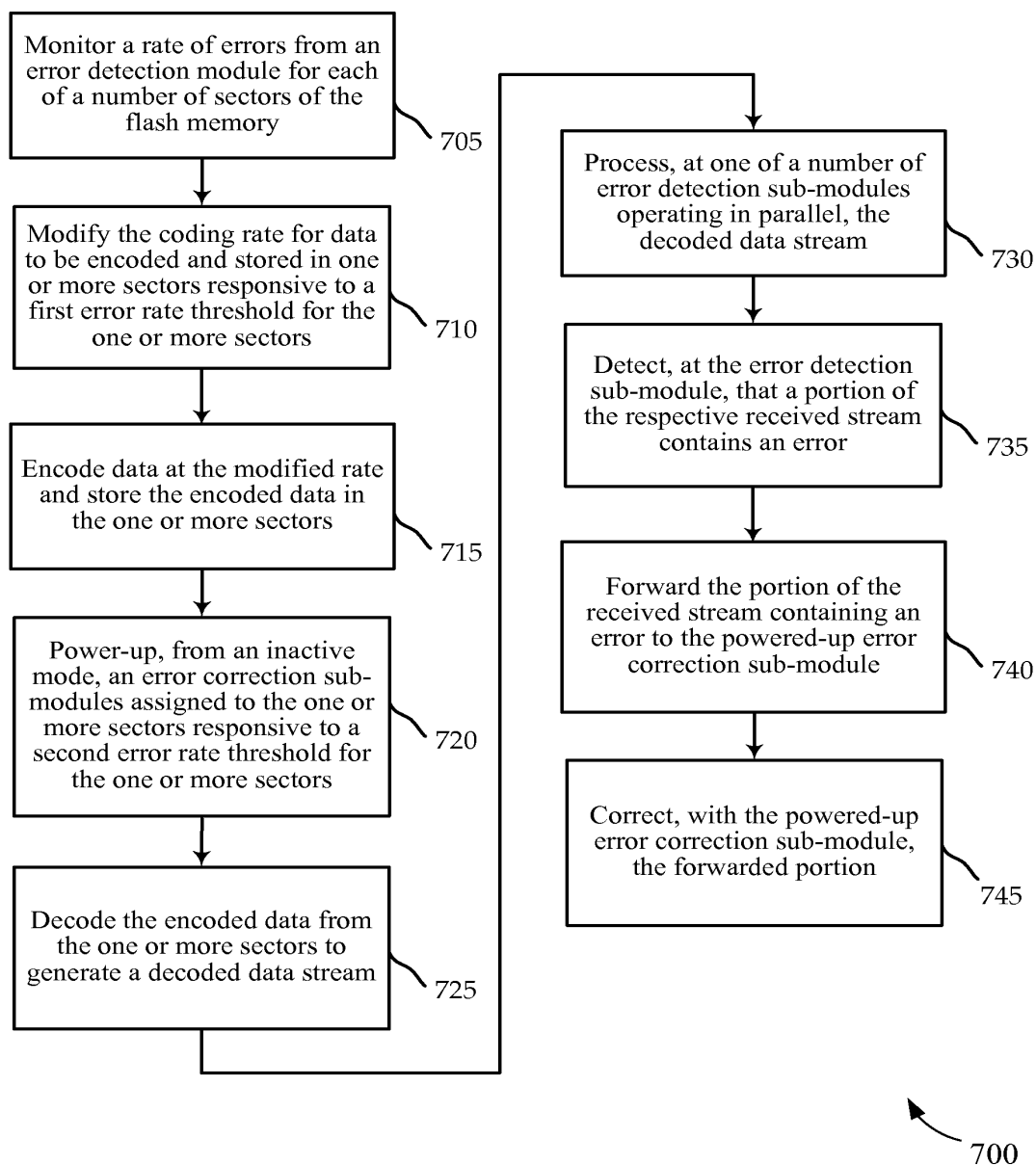


FIG. 7

Application Data Sheet

Application Information

Application number::
Filing Date:: 08/18/10
Application Type:: Regular
Subject Matter:: Utility
Title:: FORWARD ERROR CORRECTION FOR
MEMORIES
Attorney Docket Number:: 026258-003710US
Request for Early Publication:: No
Request for Non-Publication:: No
Suggested Drawing Figure:: 4
Total Drawing Sheets:: 7
Small Entity?: No
Petition included?: No
Secrecy Order in Parent Appl.: No

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Correspondence Information

Correspondence Customer Number:: 61668

Representative Information

Representative Number:: 61668

Domestic Priority Information

Application::	Continuity Type::	Parent Application::	Parent Filing Date::
This Application	An Appn claiming benefit under 35 USC 119(e) of	61/234,911	08/18/09

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City of mailing address::	Carlsbad
State or Province of mailing address::	CA
Country of mailing address::	US
Postal or Zip Code of mailing address::	92009

Electronic Acknowledgement Receipt	
EFS ID:	8240360
Application Number:	12858510
International Application Number:	
Confirmation Number:	6028
Title of Invention:	FORWARD ERROR CORRECTION FOR MEMORIES
First Named Inventor/Applicant Name:	Sameep Dave
Customer Number:	61668
Filer:	Michael L. Drapkin/Stephanie Klepp
Filer Authorized By:	Michael L. Drapkin
Attorney Docket Number:	026258-003710US
Receipt Date:	18-AUG-2010
Filing Date:	
Time Stamp:	10:49:15
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		026258_003710US_Application.pdf	142648 09c88e46d779f15a75fec52e4eab4e90f4d018b	yes	20

	Multipart Description/PDF files in .zip description								
	Document Description		Start	End					
	Specification		1	14					
	Claims		15	19					
	Abstract		20	20					
Warnings:									
Information:									
2	Drawings-only black and white line drawings	026258_003710US_Drawings.pdf	82279 4f8eca6e3f114afdcfb7ea5f8912cfaa1c103cf	no	7				
Warnings:									
Information:									
3	Application Data Sheet	026258_003710US_ADS.pdf	56087 1361a872b9c4123c5106f91b79ee6b5554946ee6	no	4				
Warnings:									
Information:									
This is not an USPTO supplied ADS fillable form									
Total Files Size (in bytes):			281014						
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Date: 08/18/10

PTO/SB/06 (12-04)

Approved for use through 7/31/2006. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875					Application or Docket Number 12/858,510		
APPLICATION AS FILED – PART I							
(Column 1)		(Column 2)		SMALL ENTITY		OR	
OTHER THAN SMALL ENTITY							
FOR	NUMBER FILED	NUMBER EXTRA	RATE (\$)	FEE (\$)	RATE (\$)	FEE (\$)	
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A		N/A	330	
SEARCH FEE (37 CFR 1.16(k), (l), or (m))	N/A	N/A	N/A		N/A	540	
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A		N/A	220	
TOTAL CLAIMS (37 CFR 1.16(i))	25	minus 20 = 5	x\$26		x\$52	260	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	3	minus 3 = *	x\$110		x\$220		
APPLICATION SIZE FEE (37 CFR 1.16(s))			If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$270 (\$135 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR				
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))			195		390		
			TOTAL		TOTAL	1350	
* If the difference in column 1 is less than zero, enter "0" in column 2.							
APPLICATION AS AMENDED – PART II							
(Column 1)		(Column 2)		(Column 3)			
AMENDMENT A	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)	RATE (\$)	ADDITIONAL FEE (\$)
	Total (37 CFR 1.16(i))	Minus **	=	X =		X =	
	Independent (37 CFR 1.16(h))	Minus ***	=	X =		X =	
	Application Size Fee (37 CFR 1.16(s))			N/A		N/A	
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))			TOTAL ADD'T FEE		TOTAL ADD'T FEE	
(Column 1)		(Column 2)		(Column 3)			
AMENDMENT B	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)	RATE (\$)	ADDITIONAL FEE (\$)
	Total (37 CFR 1.16(i))	Minus **	=	X =		X =	
	Independent (37 CFR 1.16(h))	Minus ***	=	X =		X =	
	Application Size Fee (37 CFR 1.16(s))			N/A		N/A	
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))			TOTAL ADD'T FEE		TOTAL ADD'T FEE	
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3. ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20". *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3". The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.							

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
12/858,510	08/18/2010	Sameep Dave	026258-003710US

CONFIRMATION NO. 6028

FORMALITIES LETTER



OC000000043259232

61668
TOWNSEND AND TOWNSEND AND CREW LLP
VIASAT, INC. (CLIENT #017018)
TWO EMBARCADERO CENTER
8TH FLOOR
SAN FRANCISCO, CA 94111

Date Mailed: 08/31/2010

NOTICE TO FILE MISSING PARTS OF NONPROVISIONAL APPLICATION

FILED UNDER 37 CFR 1.53(b)

Filing Date Granted

Items Required To Avoid Abandonment:

An application number and filing date have been accorded to this application. The item(s) indicated below, however, are missing. Applicant is given **TWO MONTHS** from the date of this Notice within which to file all required items and pay any fees required below to avoid abandonment. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a).

- The statutory basic filing fee is missing.
Applicant must submit \$330 to complete the basic filing fee for a non-small entity. If appropriate, applicant may make a written assertion of entitlement to small entity status and pay the small entity filing fee (37 CFR 1.27).
- The oath or declaration is missing.
A properly signed oath or declaration in compliance with 37 CFR 1.63, identifying the application by the above Application Number and Filing Date, is required.
Note: If a petition under 37 CFR 1.47 is being filed, an oath or declaration in compliance with 37 CFR 1.63 signed by all available joint inventors, or if no inventor is available by a party with sufficient proprietary interest, is required.

The application is informal since it does not comply with the regulations for the reason(s) indicated below.

The required item(s) identified below must be timely submitted to avoid abandonment:

- Replacement drawings in compliance with 37 CFR 1.84 and 37 CFR 1.121(d) are required. The drawings submitted are not acceptable because:
 - More than one figure is present and each figure is not labeled "Fig." with a consecutive Arabic numeral (1, 2, etc.) or an Arabic numeral and capital letter in the English alphabet (A, B, etc.)(see 37 CFR 1.84(u)(1)). See Figure(s) 4. A brief description of the several views of the drawings (see 37 CFR 1.74) should be added or amended to correspond to the corrected numbering of the figures. See also 37 CFR 1.77(b)(7).

Applicant is cautioned that correction of the above items may cause the specification and drawings page count to exceed 100 pages. If the specification and drawings exceed 100 pages, applicant will need to submit the required application size fee.

The applicant needs to satisfy supplemental fees problems indicated below.

The required item(s) identified below must be timely submitted to avoid abandonment:

page 1 of 2

- Additional claim fees of **\$260** as a non-small entity, including any required multiple dependent claim fee, are required. Applicant must submit the additional claim fees or cancel the additional claims for which fees are due.
- To avoid abandonment, a surcharge (for late submission of filing fee, search fee, examination fee or oath or declaration) as set forth in 37 CFR 1.16(f) of **\$130** for a non-small entity, must be submitted with the missing items identified in this notice.

SUMMARY OF FEES DUE:

Total additional fee(s) required for this application is **\$1480** for a non-small entity

- **\$330** Statutory basic filing fee.
- **\$130** Surcharge.
- The application search fee has not been paid. Applicant must submit **\$540** to complete the search fee.
- The application examination fee has not been paid. Applicant must submit **\$220** to complete the examination fee for a non-small entity.
- Total additional claim fee(s) for this application is **\$260**
 - **\$260** for **5** total claims over 20.

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Commissioner for Patents
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Alexandria VA 22313-1450

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/jmilani/

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101



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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY. DOCKET NO	TOT CLAIMS	IND CLAIMS
12/858,510	08/18/2010	2827	0.00	026258-003710US	25	3

CONFIRMATION NO. 6028

FILING RECEIPT



OC000000043259231

61668
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Date Mailed: 08/31/2010

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Applicant(s)

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Assignment For Published Patent Application

ViaSat, Inc., Carlsbad, CA

Power of Attorney: None

Domestic Priority data as claimed by applicant

This appln claims benefit of 61/234,911 08/18/2009

Foreign Applications

If Required, Foreign Filing License Granted: 08/27/2010

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 12/858,510**

Projected Publication Date: To Be Determined - pending completion of Missing Parts

Non-Publication Request: No

Early Publication Request: No

Title

FORWARD ERROR CORRECTION FOR MEMORIES

Preliminary Class

365

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

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page 2 of 3

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This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign Assets Control, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

Substitute for form 1449/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(Use as many sheets as necessary)</i>				Complete if Known	
				Application Number	12/858,510
				Filing Date	August 18, 2010
				First Named Inventor	Dave, Sameep
				Art Unit	
Examiner Name					
Attorney Docket Number	026258-003710US				
Sheet	1	of	3		

U.S. PATENT DOCUMENTS					
Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number Kind Code ² (if known)			
	AA	US-7,203,874	04-10-2007	Roohparvar	
	AB	US-7,296,213	11-13-2007	Vainsencher et al.	
	AC	US-7,394,689	07-01-2008	Ryu	
	AD	US-7,356,755	04-08-2008	Fackenthal	
	AE	US-6,751,766	06-15-2004	Guterman et al.	
	AF	US-2007/0204206	08-30-2007	Lee et al.	
	AG	US-2004/0083334	04-29-2004	Chang et al.	
	AH	US-2008/0244362	10-02-2008	Liu et al.	
	AI	US-2008/0072120	03-20-2008	Radke	
	AJ	US-2007/0266295	11-15-2007	Conley	
	AK	US-2008/0244370	10-02-2008	Lam	
	AL	US-2008/0163028	07-03-2008	Mokhlesi	
	AM	US-2007/0283428	12-06-2007	Ma et al.	
	AN	US-7,231,585	06-12-2007	Vainsencher et al.	
	AO	US-7,333,364	02-19-2008	Yu et al.	
	AP	US-2008/0148132	06-19-2008	Mavila	
	AQ	US-2003/0041299	02-27-2003	Kanazawa et al.	
	AR	US-2008/0270680	10-30-2008	Chang	
	AS	US-2007/0271494	11-22-2007	Gorobets	
	AT	US-2008/0130341	06-05-2008	Shalvi et al.	
	AU	US-2008/0184094	07-31-2008	Murray et al.	
	AV	US-2007/0266296	11-15-2007	Conley	
	AW	US-2006/0059406	03-16-2006	Michelsoni et al.	
	AX	US-7,360,136	04-15-2008	Guterman et al.	
	AY	US-2007/0223277	09-27-2007	Tanaka et al.	
	AZ	US-7,304,893	12-04-2007	Hemink	
	BA	US-2008/0212371	09-04-2008	Roohparvar	
	BB	US-6,684,353	01-27-2004	Parker et al.	
	BC	US-2007/0171730	07-26-2007	Ramamoorthy et al.	
	BD	US-2008/0282128	11-13-2008	Lee et al.	
	BE	US-7,305,596	12-04-2007	Noda et al.	
	BF	US-2008/0109703	05-08-2008	Brandman	
	BG	US-2008/0168320	07-10-2008	Cassuto et al.	
	BH	US-2008/0276150	11-06-2008	Kong et al.	
	BI	US-2008/0301526	12-04-2008	Kohler et al.	

Examiner Signature		Date Considered	
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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. ¹ Applicant's unique citation designation number (optional). ² See Kind Codes of U.S. Patent Documents at www.uspto.gov or MPEP 901.04. ³ Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). ⁴ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁵ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. ⁶ Applicant is to place a check mark here if English language Translation is attached.

62860401 v1

Substitute for form 1449/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(Use as many sheets as necessary)</i>				Complete if Known	
				Application Number	12/858,510
				Filing Date	August 18, 2010
				First Named Inventor	Dave, Sameep
				Art Unit	
Examiner Name					
Sheet	2	of	3	Attorney Docket Number	026258-003710US

U.S. PATENT DOCUMENTS					
Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number Kind Code ² (if known)			
	BJ	US-2008/0313493	12-18-2008	Roohparvar et al.	
	BK	US-2009/0013234	01-08-2009	Radke	

FOREIGN PATENT DOCUMENTS								
Examiner Initials*	Cite No. ¹	Foreign Patent Document			Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ⁶
		Country Code ³	Number ⁴	Kind Code ⁵ (if known)				
								☐
								☐
								☐
								☐
								☐

Examiner Signature		Date Considered	
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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. ¹ Applicant's unique citation designation number (optional). ² See Kind Codes of U.S. Patent Documents at www.uspto.gov or MPEP 901.04. ³ Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). ⁴ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁵ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. ⁶ Applicant is to place a check mark here if English language Translation is attached.

Substitute for form 1449/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(Use as many sheets as necessary)</i>				Complete if Known	
				Application Number	12/858,510
				Filing Date	August 18, 2010
				First Named Inventor	Dave, Sameep
				Art Unit	
				Examiner Name	
Sheet	3	of	3	Attorney Docket Number	026258-003710US

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials *	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
	BA	STMicroelectronics, "Error Correction Code in NAND Flash Memories", http://www.eetasia.com/ARTICLES/2004NOV29MEM_AN10.PDF?SOURCES=DOWNLOAD , May 11, 2004.	☐
	BB	Numonyx, "Error Correction Code in Single Level Cell NAND Flash Memories", http://www.numonyx.com/Documents/Application%20Notes/AN1823.pdf , May 26, 2008.	☐
	BC	Micron Technology, Inc., "ECC Module for Xilinx Spartan-3", http://download.micron.com/pdf/technotes/nand/tn2905.pdf , May 1, 2007.	☐
	BD	Micron Technology, Inc., "Hamming Codes for NAND Flash Memory Devices", http://download.micron.com/pdf/technotes/nand/tn2908.pdf , May 1, 2007.	☐
	BE	Sun et al., "Multilevel Flash Memory On-Chip Error Correction Based on Trellis Coded Modulation", http://www.ecse.rpi.edu/homepages/tzhang/pub/FLASHISCAS06.pdf .	☐
	BF	Micron Technology, Inc., "NAND Flash Design and Use Considerations", http://download.micron.com/pdf/technotes/nand/tn2917.pdf , August 1, 2006.	☐
	BG	Micron Technology, Inc., "Using COPYBACK Operations in NAND Flash Devices," http://download.micron.com/pdf/technotes/nand/tn2941_idm_copyback.pdf , October 1, 2008.	☐
	BH	Micron Technology, Inc., "NAND Flash Internal Data Move", http://download.micron.com/pdf/technotes/nand/tn2915.pdf , June 1, 2007.	☐
	BI	Micron Technology, Inc., "Wear-Leveling Techniques in NAND Flash Devices", http://download.micron.com/pdf/technotes/nand/tn2942_nand_wear_leveling.pdf , October 1, 2008.	☐
	BJ	Chen, et al., "Error Correction for Multi-Level NAND Flash Memory Using Reed-Solomon Codes", http://www.csie.ntu.edu.tw/~f95070/Flash%20Paper%20Collection/ERROR%20CORRECTION%20FOR%20MULTI-LEVEL%20NAND%20FLASH%20MEMORY%20USING%20REED-SOLOMON%20CODES.pdf , November 26, 2008.	

Examiner Signature		Date Considered	
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* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

¹ Applicant's unique citation designation number (optional). ² Applicant is to place a check mark here if English language Translation is attached.

Electronic Acknowledgement Receipt	
EFS ID:	8344163
Application Number:	12858510
International Application Number:	
Confirmation Number:	6028
Title of Invention:	FORWARD ERROR CORRECTION FOR MEMORIES
First Named Inventor/Applicant Name:	Sameep Dave
Customer Number:	61668
Filer:	Michael L. Drapkin/Stephanie Klepp
Filer Authorized By:	Michael L. Drapkin
Attorney Docket Number:	026258-003710US
Receipt Date:	02-SEP-2010
Filing Date:	18-AUG-2010
Time Stamp:	13:10:24
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		026258_003710US_IDS_2_Sept_2010.pdf	251294 20f5f752455093ef258c40aa92e850ecce166d8e	yes	5

	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Transmittal Letter		1	2	
	Information Disclosure Statement (IDS) Filed (SB/08)		3	5	
Warnings:					
Information:					
2	NPL Documents	026258_003710US_STMicroelectronics.pdf	459226 78ab667242644f4b0023e869e1b30b3f88332e6f	no	14
Warnings:					
Information:					
3	NPL Documents	026258_003710US_Numonyx.pdf	473938 6255502567f327db7ea011c3e8424b54b87aa47b	no	19
Warnings:					
Information:					
4	NPL Documents	026258_003710US_MicronXilinx.pdf	2116178 6885d03a70e0db87f1f106bfd4655f21c587519e7	no	21
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Information:					
5	NPL Documents	026258_003710US_MicronHamingCodes.pdf	1273117 243c2a4a72de59186ae866919abfc9891f1bd792	no	7
Warnings:					
Information:					
6	NPL Documents	026258_003710US_Sun.pdf	336724 e8168c853cf1bededef2bb0b2f0ef87ee1fa9982	no	4
Warnings:					
Information:					
7	NPL Documents	026258_003710US_MicronUseConsiderations.pdf	598083 5ff4060389bf7b09fb4033e58b32e77c780db4e6	no	8
Warnings:					
Information:					
8	NPL Documents	026258_003710US_MicronCopyback.pdf	192477 91ce55d90956498da4afa829a34c10c75471a00c	no	4
Warnings:					
Information:					

9	NPL Documents	026258_003710US_MicronInternalMove.pdf	710209 0125e9fd4405d36d1e7be11f44974103fb4bde	no	7
Warnings:					
Information:					
10	NPL Documents	026258_003710US_MicronWeatherLeveling.pdf	594137 41b99a6cbb5957d21efde39a3e5357d001babcb	no	8
Warnings:					
Information:					
11	NPL Documents	026258_003710US_Chen.pdf	695283 864bd3aeea299d48f924f36c92008edc943cb52	no	11
Warnings:					
Information:					
Total Files Size (in bytes):			7700666		
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					

I hereby certify that this correspondence is being filed via
EFS-Web with the United States Patent and Trademark Office
on September 2, 2010

PATENT
Attorney Docket No.: 026258-003710US
Client Reference No.: ECC-0407-US-2

TOWNSEND and TOWNSEND and CREW LLP

By: /Stephanie Klepp/
Stephanie Klepp

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

Russell Fuerst et al.

Application No.: 12/858,510

Filed: August 18, 2010

For: FORWARD ERROR
CORRECTION FOR MEMORIES

Customer No.: 61668

Confirmation No.: 6028

Examiner:

Art Unit:

INFORMATION DISCLOSURE
STATEMENT UNDER 37 CFR §1.97 and
§1.98

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Commissioner:

The references cited on attached form PTO/SB/08A and PTO/SB/08B are being called to the attention of the Examiner. Copies of the references in compliance with the requirements of 37 CFR §1.98(a)(2) are enclosed. It is respectfully requested that the cited references be expressly considered during the prosecution of this application, and the references be made of record therein and appear among the "references cited" on any patent to issue therefrom.

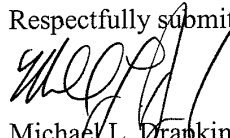
As provided for by 37 CFR §1.97(g) and (h), no inference should be made that the information and references cited are prior art merely because they are in this statement and no

representation is being made that a search has been conducted or that this statement encompasses all the possible relevant information.

Applicants believes that no fee is required for submission of this statement.

However, if a fee is required, the Commissioner is authorized to deduct such fee from the undersigned's Deposit Account No. 20-1430. Please deduct any additional fees from, or credit any overpayment to, the above-noted Deposit Account.

Respectfully submitted,



Michael L. Drapkin
Reg. No. 55,127

TOWNSEND and TOWNSEND and CREW LLP
Two Embarcadero Center, Eighth Floor
San Francisco, California 94111-3834
Tel: 303-571-4000
Fax: 303-571-4321
MLD:s5k
62860401 v1

I hereby certify that this correspondence is being filed via
EFS-Web with the United States Patent and Trademark Office
on September 30, 2010

PATENT
Docket No.: 026258-003710US
Client Reference No. ECC-0407-US-2

TOWNSEND and TOWNSEND and CREW LLP

By: / Stephanie Klepp /
Stephanie Klepp

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

Sameep Dave et al.

Application No.: 12/858,510

Filed: August 18, 2010

For: FORWARD ERROR
CORRECTION FOR MEMORIES

Confirmation No.: 6028

Examiner: Not Assigned

Art Unit: 2827

REQUEST FOR CORRECTION OF
FILING RECEIPT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Attached is a copy of the official Filing Receipt received from the Patent and Trademark Office in the above-noted application for which issuance of a corrected filing receipt is respectfully requested.

There is an error in that the fourth-named inventor's address is incorrect and should read as follows:

Jim Keszenheimer, Chagrin Falls, OH

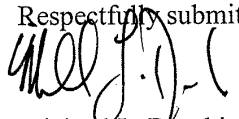
The Application Data Sheet is also attached which reflects the correct address.

Sameep Dave et al.
Application No.: 12/858,510
Page 2

PATENT

Applicants believe no fee is due as the correct information was included in the Application Data Sheet. However, if a fee is due, the Commissioner is hereby authorized to charge any additional fees associated with this paper to Deposit Account No. 20-1430.

Respectfully submitted,



Michael L. Drapkin
Reg. No. 55,127

TOWNSEND and TOWNSEND and CREW LLP
Two Embarcadero Center, Eighth Floor
San Francisco, California 94111-3834
Tel: (303) 571-4000
Fax: (415) 576-0300
MLD:sk
62863672 v1



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY DOCKET NO	TOT CLAIMS	IND CLAIMS
12/858,510	08/18/2010	2827	0.00	026258-003710US	25	3

CONFIRMATION NO. 6028

61668
TOWNSEND AND TOWNSEND AND CREW LLP
VIASAT, INC. (CLIENT #017018)
TWO EMBARCADERO CENTER
8TH FLOOR
SAN FRANCISCO, CA 94111

FILING RECEIPT



0000000043259231

Date Mailed: 08/31/2010

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Applicant(s)

Sameep Dave, Stow, OH;
Russell Fuerst, Mentor, OH;
Mark Kohoot, Cleveland Heights, OH;
Jim Keszenheimer, Chargin Falls, OH; **Chargin**
William H. Thesling, Hudson, OH;

Assignment For Published Patent Application

ViaSat, Inc., Carlsbad, CA

Power of Attorney: None

Domestic Priority data as claimed by applicant

This appln claims benefit of 61/234,911 08/18/2009

Foreign Applications

If Required, Foreign Filing License Granted: 08/27/2010

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 12/858,510**

Projected Publication Date: To Be Determined - pending completion of Missing Parts

Non-Publication Request: No

Early Publication Request: No

Title

FORWARD ERROR CORRECTION FOR MEMORIES

Preliminary Class

365

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at <http://www.uspto.gov/web/offices/pac/doc/general/index.html>.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, <http://www.stopfakes.gov>. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4158).

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page 2 of 3

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This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign Assets Control, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

Application Data Sheet

Application Information

Application number::
Filing Date:: 08/18/10
Application Type:: Regular
Subject Matter:: Utility
Title:: FORWARD ERROR CORRECTION FOR
MEMORIES
Attorney Docket Number:: 026258-003710US
Request for Early Publication:: No
Request for Non-Publication:: No
Suggested Drawing Figure:: 4
Total Drawing Sheets:: 7
Small Entity?:: No
Petition included?:: No
Secrecy Order in Parent Appl.: No

Applicant Information

Applicant Authority Type:: Inventor
Primary Citizenship Country:: India
Status:: Full Capacity
Given Name:: Sameep
Family Name:: Dave
City of Residence:: Stow
State or Province of Residence:: OH
Country of Residence:: US
Street of Mailing Address:: 4869 Concord Drive
City of Mailing Address:: Stow
State or Province of mailing address:: OH

Country of mailing address:: US
Postal or Zip Code of mailing address:: 44224

Applicant Authority Type:: Inventor
Primary Citizenship Country:: US
Status:: Full Capacity
Given Name:: Russell
Family Name:: Fuerst
City of Residence:: Mentor
State or Province of Residence:: OH
Country of Residence:: US
Street of Mailing Address:: 8475 Mansion Boulevard
City of Mailing Address:: Mentor
State or Province of mailing address:: OH
Country of mailing address:: US
Postal or Zip Code of mailing address:: 44060

Applicant Authority Type:: Inventor
Primary Citizenship Country:: US
Status:: Full Capacity
Given Name:: Mark
Family Name:: Kohoot
City of Residence:: Cleveland Heights
State or Province of Residence:: OH
Country of Residence:: US
Street of Mailing Address:: 2748 Lancashire Road
City of Mailing Address:: Cleveland Heights
State or Province of mailing address:: OH
Country of mailing address:: US
Postal or Zip Code of mailing address:: 44106

Applicant Authority Type:: Inventor
Primary Citizenship Country:: US
Status:: Full Capacity
Given Name:: Jim
Family Name:: Keszenheimer
City of Residence:: Chagrin Falls
State or Province of Residence:: OH
Country of Residence:: US
Street of Mailing Address:: 8025 Bainbrook
City of Mailing Address:: Chagrin Falls
State or Province of mailing address:: OH
Country of mailing address:: US
Postal or Zip Code of mailing address:: 44023

Applicant Authority Type:: Inventor
Primary Citizenship Country:: US
Status:: Full Capacity
Given Name:: William
Middle Name:: H.
Family Name:: Thesling
City of Residence:: Hudson
State or Province of Residence:: OH
Country of Residence:: US
Street of Mailing Address:: 7332 E. Firelands Drive
City of Mailing Address:: Hudson
State or Province of mailing address:: OH
Country of mailing address:: US
Postal or Zip Code of mailing address:: 44236

Correspondence Information

Correspondence Customer Number:: 61668

Representative Information

Representative Number:: 61668

Domestic Priority Information

Application::	Continuity Type::	Parent Application::	Parent Filing Date::
This Application	An Appn claiming benefit under 35 USC 119(e) of	61/234,911	08/18/09

Assignee Information

Assignee Name:: ViaSat, Inc.
Street of mailing address:: 6155 El Camino Real
City of mailing address:: Carlsbad
State or Province of mailing address:: CA
Country of mailing address:: US
Postal or Zip Code of mailing address:: 92009

Electronic Acknowledgement Receipt	
EFS ID:	8532514
Application Number:	12858510
International Application Number:	
Confirmation Number:	6028
Title of Invention:	FORWARD ERROR CORRECTION FOR MEMORIES
First Named Inventor/Applicant Name:	Sameep Dave
Customer Number:	61668
Filer:	Michael L. Drapkin/Stephanie Klepp
Filer Authorized By:	Michael L. Drapkin
Attorney Docket Number:	026258-003710US
Receipt Date:	30-SEP-2010
Filing Date:	18-AUG-2010
Time Stamp:	12:55:40
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Request for Corrected Filing Receipt	026258_0003710US_ReqCorrectedFilingReceipt.pdf	307680 d530f1fca803bd7c4e004da2ec0890bda1b63fc	no	9

Warnings:

Information:

Total Files Size (in bytes):	307680
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.	

I hereby certify that this correspondence is being filed via
EFS-Web with the United States Patent and Trademark Office
on September 30, 2010

PATENT
Attorney Docket No.: 026258-003710US
Client Reference No.: ECC-0407-US-2

TOWNSEND and TOWNSEND and CREW LLP

By: /Stephanie Klepp/
Stephanie Klepp

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

Russell Fuerst et al.

Application No.: 12/858,510

Filed: August 18, 2010

For: FORWARD ERROR
CORRECTION FOR MEMORIES

Customer No.: 61668

Confirmation No.: 6028

Examiner:

Art Unit: 2827

TRANSMITTAL LETTER –
RESPONSE TO NOTICE OF MISSING
PARTS

Mail Stop Missing Parts
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Commissioner:

Pursuant to the Notice to File Missing Parts of Nonprovisional Application, dated
August 31, 2010, enclosed are the following to be made of record in the above-identified
application:

- 1) Executed Declaration
- 2) Power of Attorney and Certificate of Assignee Under 37 C.F.R. § 3.73(b)
- 3) Replacement Sheet Figure 4. Please use this Replacement Sheet in place
of the original sheet including Figure 4.

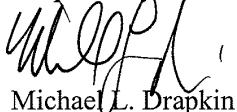
Please charge Deposit Account No. 20-1430 for the following fees:

Large Entity: (a) Utility Filing Fee \$330

(b)	Utility Search Fee	\$540
(c)	Utility Examination Fee	\$220
(d)	Application Size Fee	\$0
(e)	Excess Claims Fees (§ 1.16(b), (c)):	
	25 - 20 = 5 x \$52 =	\$260
	3 - 3 = 0 x \$220 =	\$0
(f)	Multiple Dependent Claims	
(g)	Missing Parts Surcharge	\$130
	TOTAL FEES TO BE CHARGED	\$1480

The Commissioner is hereby authorized to charge any additional fees associated with this paper or during the pendency of this application, or credit any overpayment, to Deposit Account No. 20-1430.

Respectfully submitted,


Michael L. Drapkin
Reg. No. 55,127

Customer No. 61668

TOWNSEND and TOWNSEND and CREW LLP
Two Embarcadero Center, Eighth Floor
San Francisco, California 94111-3834
Tel: 303-571-4000
Fax: 415 576-0300
MLD:s5k

62910844 v1

DECLARATION

As a below named inventor, I declare that:

My residence, post office address and citizenship are as stated below next to my name; I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural inventors are named below) of the subject matter which is claimed and for which a patent is sought on the invention entitled: FORWARD ERROR CORRECTION FOR MEMORIES the specification of which was filed on August 18, 2010 as Application No. 12/858,510.

I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above. I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56. I claim foreign priority benefits under Title 35, United States Code, Section 119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s)

Country	Application No.	Date of Filing	Priority Claimed Under 35 USC 119

I hereby claim the benefit under Title 35, United States Code § 119(e) of any United States provisional application(s) listed below:

Application No.	Filing Date
61/234,911	August 18, 2009

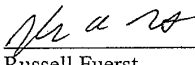
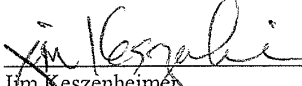
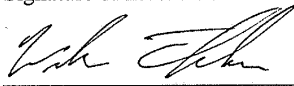
I claim the benefit under Title 35, United States Code, Section 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, Section 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, Section 1.56 which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

Application No.	Date of Filing	Status

Full Name of Inventor 1:	Last Name: DAVE	Suffix:	First Name: SAMEEP	Middle Name or Initial:
Residence & Citizenship:	City: Stow		State/Foreign Country: Ohio	Country of Citizenship: India
Post Office Address:	Post Office Address: 4869 Concord Drive		City: Stow	State/Country: Ohio
				Postal Code: 44224
Full Name of Inventor 2:	Last Name: FUERST	Suffix:	First Name: RUSSELL	Middle Name or Initial:
Residence & Citizenship:	City: Mentor		State/Foreign Country: Ohio	Country of Citizenship: United States
Post Office Address:	Post Office Address: 8475 Mansion Boulevard		City: Mentor	State/Country: Ohio
				Postal Code: 44060

Full Name of Inventor 3:	Last Name: KOHOOT	Suffix:	First Name: MARK	Middle Name or Initial:	
Residence & Citizenship:	City: Cleveland Heights		State/Foreign Country: Ohio	Country of Citizenship: United States	
Post Office Address:	Post Office Address: 2748 Lancashire Road		City: Cleveland Heights	State/Country: Ohio	Postal Code: 44106
Full Name of Inventor 4:	Last Name: KESZENHEIMER	Suffix:	First Name: JIM	Middle Name or Initial:	
Residence & Citizenship:	City: Chagrin Falls		State/Foreign Country: Ohio	Country of Citizenship: United States	
Post Office Address:	Post Office Address: 8025 Bainbrook		City: Chagrin Falls	State/Country: Ohio	Postal Code: 44023
Full Name of Inventor 5:	Last Name: THESLING	Suffix:	First Name: WILLIAM	Middle Name or Initial: H.	
Residence & Citizenship:	City: Hudson		State/Foreign Country: Ohio	Country of Citizenship: United States	
Post Office Address:	Post Office Address: 7332 E. Firelands Drive		City: Hudson	State/Country: Ohio	Postal Code: 44236

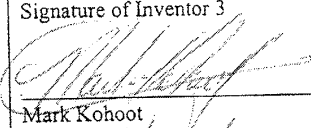
I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Signature of Inventor 1  Sameep Dave Date 8/20/2010	Signature of Inventor 2  Russell Fuerst Date 8/26/10	Signature of Inventor 3 Mark Kohoot Date
Signature of Inventor 4  Jim Keszenheimer Date 8/29/2010	Signature of Inventor 5  William H. Thesling Date 8-24-2010	

62836728 v1

Full Name of Inventor 3:	Last Name: KOHOOT	Suffix:	First Name: MARK	Middle Name or Initial:
Residence & Citizenship:	City: Cleveland Heights		State/Foreign Country: Ohio	Country of Citizenship: United States
Post Office Address:	Post Office Address: 2748 Lancashire Road		City: Cleveland Heights	State/Country: Ohio Postal Code: 44106
Full Name of Inventor 4:	Last Name: KESZENHEIMER	Suffix:	First Name: JIM	Middle Name or Initial:
Residence & Citizenship:	City: Chagrin Falls		State/Foreign Country: Ohio	Country of Citizenship: United States
Post Office Address:	Post Office Address: 8025 Bainbrook		City: Chagrin Falls	State/Country: Ohio Postal Code: 44023
Full Name of Inventor 5:	Last Name: THESLING	Suffix:	First Name: WILLIAM	Middle Name or Initial: H.
Residence & Citizenship:	City: Hudson		State/Foreign Country: Ohio	Country of Citizenship: United States
Post Office Address:	Post Office Address: 7332 E. Firelands Drive		City: Hudson	State/Country: Ohio Postal Code: 44236

I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Signature of Inventor 1 Sameep Dave Date	Signature of Inventor 2 Russell Fuerst Date	Signature of Inventor 3  Mark Kohoot Date 4/29/2010
Signature of Inventor 4 Jim Keszenheimer Date	Signature of Inventor 5 William H. Thesling Date	

62836728 v1

POWER OF ATTORNEY TO PROSECUTE APPLICATIONS BEFORE THE USPTO

I hereby revoke all previous powers of attorney given in the application identified in the attached statement under 37 CFR 3.73(b).

I hereby appoint:

☒ Practitioners associated with the Customer Number:

61668

OR

☐ Practitioner(s) named below (if more than ten patent practitioners are to be named, then a customer number must be used):

Name	Registration Number	Name	Registration Number

as attorney(s) or agent(s) to represent the undersigned before the United States Patent and Trademark Office (USPTO) in connection with any and all patent applications assigned only to the undersigned according to the USPTO assignment records or assignment documents attached to this form in accordance with 37 CFR 3.73(b). I further authorize any of the above-identified practitioners to execute a Statement Under 37 CFR 3.73(b) on the undersigned's behalf to certify the chain of title and establish the undersigned's ownership in any and all patent applications in which rights have been assigned to the undersigned.

Please change the correspondence address for the application identified in the attached statement under 37 CFR 3.73(b) to:

☒ The address associated with Customer Number:

61668

OR

☐ Firm or Individual Name

Address

City

State

Zip

Country

Telephone

Email

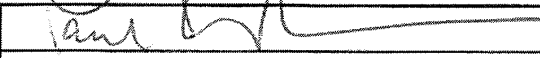
Assignee Name and Address:

ViaSat, Inc.
6155 El Camino Real
Carlsbad, California 92009

A copy of this form, together with a statement under 37 CFR 3.73(b) (Form PTO/SB/96 or equivalent) is required to be filed in each application in which this form is used. The statement under 37 CFR 3.73(b) may be completed by one of the practitioners appointed in this form if the appointed practitioner is authorized to act on behalf of the assignee, and must identify the application in which this Power of Attorney is to be filed.

SIGNATURE of Assignee of Record

The individual whose signature and title is supplied below is authorized to act on behalf of the assignee

Signature		Date	7 Sept 2010
Name	Paul Konopka	Telephone	760-476-2867
Title	Associate General Counsel		

Attorney Docket No. 026258-003710US

STATEMENT UNDER 37 CFR 3.73(b)Applicant/Patent Owner: Russell Fuerst et al.Application No./Patent No.: 12/858,510 Filed/Issue Date: August 18, 2010Titled: FORWARD ERROR CORRECTION FOR MEMORIES

ViaSat, Inc., a corporation
 (Name of Assignee) (Type of Assignee: corporation, partnership, university, government agency, etc.)

states that it is:

1. ☒ the assignee of the entire right, title, and interest in;
2. ☐ an assignee of less than the entire right, title, and interest in
 (The extent (by percentage) of its ownership interest is _____ %); or
3. ☐ the assignee of an undivided interest in the entirety of (a complete assignment from one of the joint inventors was made)

the patent application/patent identified above, by virtue of either:

- A. ☒ An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel 025064, Frame 0323, or for which a copy thereof is attached.

OR

- B. ☐ A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as follows:

1. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

2. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

3. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

☐ Additional documents in the chain of title are listed on a supplemental sheet (s).

- ☐ As required by 37 CFR 3.73(b)(1)(i), the documentary evidence of the chain of title from the original owner to the assignee was, or concurrently is being, submitted for recordation pursuant to 37 CFR 3.11.

[NOTE: A separate copy (i.e., a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, to record the assignment in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

Signature

September 30, 2010

Date

Michael L. Drapkin, Reg. No. 55,127

Printed or Typed Name

Attorney

Title

Replacement Sheet

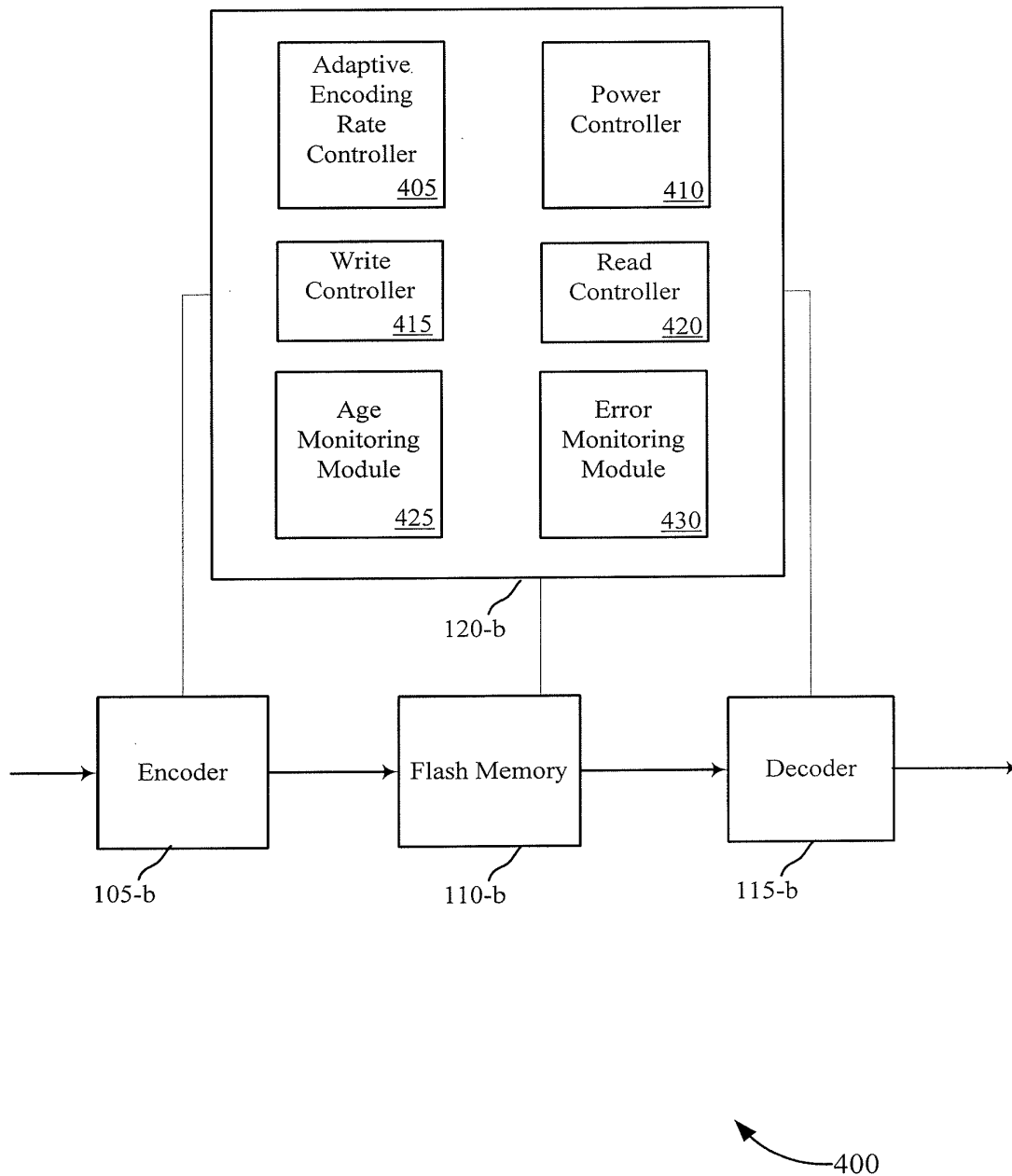


FIG. 4

Electronic Patent Application Fee Transmittal				
Application Number:	12858510			
Filing Date:	18-Aug-2010			
Title of Invention:	FORWARD ERROR CORRECTION FOR MEMORIES			
First Named Inventor/Applicant Name:	Sameep Dave			
Filer:	Michael L. Drapkin/Stephanie Klepp			
Attorney Docket Number:	026258-003710US			
Filed as Large Entity				
Utility under 35 USC 111(a) Filing Fees				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Utility application filing	1011	1	330	330
Utility Search Fee	1111	1	540	540
Utility Examination Fee	1311	1	220	220
Pages:				
Claims:				
Claims in excess of 20	1202	5	52	260
Miscellaneous-Filing:				
Late filing fee for oath or declaration	1051	1	130	130

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				1480

Electronic Acknowledgement Receipt	
EFS ID:	8532592
Application Number:	12858510
International Application Number:	
Confirmation Number:	6028
Title of Invention:	FORWARD ERROR CORRECTION FOR MEMORIES
First Named Inventor/Applicant Name:	Sameep Dave
Customer Number:	61668
Filer:	Michael L. Drapkin/Stephanie Klepp
Filer Authorized By:	Michael L. Drapkin
Attorney Docket Number:	026258-003710US
Receipt Date:	30-SEP-2010
Filing Date:	18-AUG-2010
Time Stamp:	13:01:13
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	\$ 1480
RAM confirmation Number	2112
Deposit Account	201430
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees) Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)	

Charge any Additional Fees required under 37 C.F.R. Section 1.19 (Document supply fees)					
Charge any Additional Fees required under 37 C.F.R. Section 1.20 (Post Issuance fees)					
Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)					
File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		026258_0003710US_Response MissingParts.pdf	402428 290c84cdee1daa7d0c497837a565cae7ed8453b9	yes	7
	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Applicant Response to Pre-Exam Formalities Notice		1	2	
	Oath or Declaration filed		3	5	
	Power of Attorney		6	6	
	Assignee showing of ownership per 37 CFR 3.73(b).		7	7	
Warnings:					
Information:					
2	Drawings-only black and white line drawings	026258_0003710US_ReplacementDrawing.pdf	20981 913e061cdf42641d7ba7e685432c729398749b2c	no	1
Warnings:					
Information:					
3	Fee Worksheet (PTO-875)	fee-info.pdf	38172 969016dd31e34c7ff74a5e45842b614595aa245b	no	2
Warnings:					
Information:					
Total Files Size (in bytes):			461581		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY. DOCKET NO	TOT CLAIMS	IND CLAIMS
12/858,510	08/18/2010	2827	1480	026258-003710US	25	3

CONFIRMATION NO. 6028

UPDATED FILING RECEIPT

61668
TOWNSEND AND TOWNSEND AND CREW LLP
VIASAT, INC. (CLIENT #017018)
TWO EMBARCADERO CENTER
8TH FLOOR
SAN FRANCISCO, CA 94111



OC000000043839551

Date Mailed: 10/07/2010

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Applicant(s)

Sameep Dave, Stow, OH;
Russell Fuerst, Mentor, OH;
Mark Kohoot, Cleveland Heights, OH;
Jim Keszenheimer, Chagrin Falls, OH;
William H. Thesling, Hudson, OH;

Assignment For Published Patent Application

ViaSat, Inc., Carlsbad, CA

Power of Attorney: The patent practitioners associated with Customer Number 61668

Domestic Priority data as claimed by applicant

This appln claims benefit of 61/234,911 08/18/2009

Foreign Applications

If Required, Foreign Filing License Granted: 08/27/2010

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 12/858,510**

Projected Publication Date: 02/24/2011

Non-Publication Request: No

Early Publication Request: No

Title

FORWARD ERROR CORRECTION FOR MEMORIES

Preliminary Class

365

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at <http://www.uspto.gov/web/offices/pac/doc/general/index.html>.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, <http://www.stopfakes.gov>. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4158).

LICENSE FOR FOREIGN FILING UNDER**Title 35, United States Code, Section 184****Title 37, Code of Federal Regulations, 5.11 & 5.15****GRANTED**

The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where the conditions for issuance of a license have been met, regardless of whether or not a license may be required as

page 2 of 3

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61668
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Date Mailed: 10/07/2010

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 09/30/2010.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

/llam/

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VIASAT, INC. (CLIENT #017018)
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Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number Kind Code ² (if known)			
	1	US-2003-037299 A1	02-20-2003	Smith, Kenneth Kay	
	2	US-2004-243906 A1	12-2-2004	Huang, Che-Chi	
	3	US-2005-172179 A1	08-04-2005	Brandenberger, Sarah H.	
	4	US-2008-052564 A1	02-28-2008	Yim, Yong-Tae	

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		Country Code ³	Number ⁴	Kind Code ⁵ (if known)				
	5	EP	1 612 950	A1	01-04-2006	St. Microelectronics SRL		☐
	6	EP	2 299 362	A2	05-04-2001	ViaSat, Inc.		☐
	7	WO	2006/013529	A1	02-09-2006	Koninkl Philipps Electronics NV		☐

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	8	European Search Report and Search Opinion of April 5, 2011 for European Application No. EP 2299362.	☐	

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3	Non Patent Literature	EP_2299362_Search_Report.pdf	780372 c0614b8cd91e641268c9f116a0a010d79f5923d	no	7
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4	Foreign Reference	EP2299362A2.pdf	494343 7bb416d517b390a85332d7261dba38acfca6d18	no	18
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(54) **Method and system for correcting errors during read and write to non volatile memories**

(57) The invention relates to a method and system for correcting errors in multilevel memories, both of the NAND and of the NOR type. The method provides the use of a BCH correction code made parallel by means of a coding and decoding architecture allowing the laten-

cy limits of prior art sequential solutions to be overcome. Two possible solutions are shown.

The parallelism being used for blocks C, 1 and 3 can be chosen in order to optimise the system performances in terms of latency and device area.

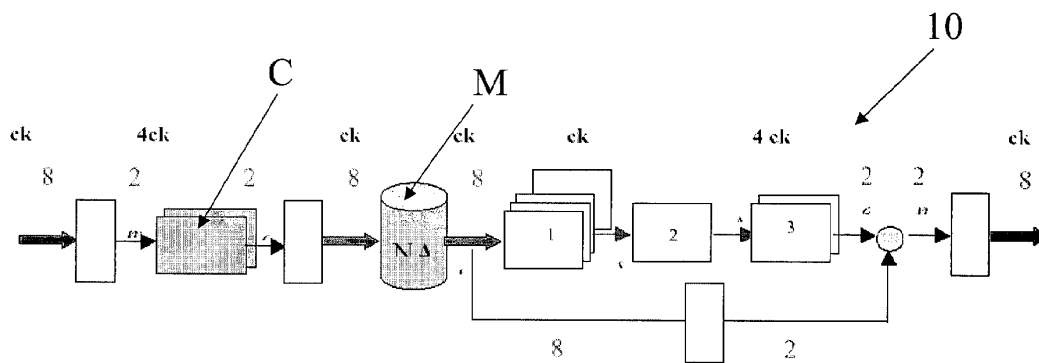


FIG. 20

EP 1 612 950 A1

DescriptionField of application

5 **[0001]** The present invention relates to a method and system for correcting low latency errors in read and write non volatile memories, particularly electronic Flash memories.

[0002] The invention particularly relates to read and write memories having a NAND structure and the following description is made with reference to this specific field of application for convenience of illustration only, since the invention can be also applied to memories with NOR structure, provided that they are equipped with an error correction system.

10 **[0003]** Even more particularly, the invention relates to a method and system for correcting errors in electronic read and write non volatile memory devices, particularly Flash memories, of the type providing at least the use of a BCH binary error correction code for the information data to be stored.

Prior art

15 **[0004]** As it is well known in this specific technical field, two-level and multilevel NAND memories have such a Bit Error Rate (BER) as to require an Error Correction system (ECC) in order to allow them to be used as reliably as possible.

[0005] Among the innumerable present ECC correction methods a particular interest is assumed by the so-called cyclical correction codes; particularly binary BCH and Reed-Solomon codes.

20 **[0006]** The main features concerning these two codes are quoted hereafter by way of comparison.

[0007] The code will be examined first:

1) Binary BCH.

25 **[0008]** This code operates on a block of binary symbols. If N ($4096 + 128$) is the block size, the number of parity bits is P (assuming to correct 4 bits, P is equal to 52bits).

[0009] As it will be seen hereafter, the code operates on a considerably lower number of bits with respect to the Reed-Solomon code.

30 **[0010]** The canonical coding and decoding structures process the data block by means of sequential operations on the bits to be coded or decoded.

[0011] The latency to code and decode data blocks is higher than the Reed-Solomon code latency since it operates on symbols.

35 **[0012]** The arithmetic operators (sum, multiplication, inversion) in $GF(2)$, and thus those necessary for this kind of code, are extremely simple (XOR, AND, NOT).

[0013] The code corrects K bits.

[0014] The other code will now be seen:

2) Reed Solomon

40 **[0015]** It operates on a block of symbols composed by a plurality of bits.

[0016] If N ($(4096 + 128) / 9$) is the symbol block size, the number of parity symbols is P (assuming to correct 4 errors, P is equal to 8 symbols formed by 9-bit, i.e. 72 bits).

45 **[0017]** The canonical coding and decoding structures process the data block by means of sequential operations on the symbols to be coded or decoded.

[0018] In this case, the latency to code and decode data blocks is lower than the BCH binary code latency since it operates on symbols rather than bits ($1/9$).

[0019] Another difference is due to the fact that the arithmetic operators (sum, multiplication, inversion) in $GF(2^m)$ are in this case complex operators with respect to the BCH code.

50 **[0020]** The code corrects K symbols. This is very useful in communication systems such as: Hard disks, Tape Recorders, CD-ROMs etc. wherein sequential errors are very probable. This latter feature cannot be fully used in NAND memories.

55 **[0021]** For a better understanding of all the aspects of the present invention, the structure of the error correction systems using a BCH coding and decoding will be analysed hereafter, the structure of Reed Solomon correction systems will be analysed afterwards.

The BCH structure

[0022] The typical structure of a BCH code is shown in the attached figure 1 wherein the block indicated with C represents the coding step while the other blocks 1, 2 and 3 are active during the decoding and they refer to the syndrome calculation, to the error detection polynomial calculation (for example by means of the known Berlekamp-Massey algorithm) and to the error detection, respectively. The block M indicates a storage and/or transfer medium of the coded data.

[0023] Blocks C, 1 and 3 can be realised by means of known structures, (for example according to what has been described by: Shu Lin, Daniel Costello - "Error Control Coding: Fundamentals and Applications") operating in a serial way and thus having a latency being proportional to the length of the message to be stored.

[0024] In particular:

BLOCK C: the block latency is equal to the message to be stored (4096 bits);

BLOCK 1: the block latency is equal to the coded message (for a four-error-corrector code $4096+52$);

BLOCK 3: the block latency is equal to the coded message (for a four-error-corrector code $4096+52$).

[0025] Figure 2 shows the flow that the data being written and read by a memory must follow in order to be coded and decoded by means of a BCH coding system. Bits traditionally arrive to the coder of the block C in groups of eight, while the traditional BCH coder processes one bit at a time. Similarly, bits are traditionally stored and read in groups of eight, while the traditional BCH decoder (1 and 3) processes them in a serial way.

[0026] Blocks (2.1) grouping or decomposing the bits to satisfy said requirements are thus required in the architecture.

[0027] Consequently, in order not to slow the data flow down, it is required that the coder and the decoder operate with a clock time being eight times higher than the clock of the data storage and reading step.

[0028] The other correction mode of the Reed Solomon type will now be examined.

The Reed Solomon structure (RS)

[0029] Reed - Solomon codes do not operate on bits but on symbols. As shown in figure 3, the code word is composed of N symbols. In the example each symbol is composed of 4 bits. The information field is composed of K symbols while the remaining N-K symbols are used as parity symbols.

[0030] The coding block C and the syndrome calculation block 1 are similar to the ones used for BCH codes with the only difference that they operate on symbols. The error detector block 3 must determine, besides the error position, also the correction symbol to be applied to the wrong symbol.

[0031] Since the code RS operates on symbols, a clearly lower latency is obtained paying a higher hardware complexity due to the fact that operators are no more binary.

BLOCK C: the block latency is equal to the number of symbols in the message to be coded (462);

BLOCK 1: the block latency is equal to the number of symbols in the coded message (470);

BLOCK 3: the block latency is equal to the number of symbols in the coded message (470);

[0032] Also in this case the same conditions about the bit grouping and decomposition occur. This time however the Reed-Solomon code does not operate in a sequential way on bits but on s-bit symbols.

[0033] Also in this case structures for grouping bits are required, but to ensure a continuous data flow the clock time must be $8/s$. It must be observed that in the case $s = 8$ these architectures are not required.

[0034] In this way the latency problem is solved, but, by comparing the number of parity bits required by BCH and Reed-Solomon, it can be seen that Reed-Solomon is much more expensive.

[0035] In the case being considered by way of example, i.e. 4224 ($4096+128$) data bits for correcting four errors, Reed - Solomon codes require twenty parity bits more than BCH binary codes.

[0036] Although advantageous under several aspects, known systems do not allow the latency due to the sequential bit processing to be reduced by keeping a number of parity bits yet, and thus an area, close to the theoretical minimum.

[0037] In substance, the advantages of the code RS low latency are accompanied by a high demand of parity bits and a higher system structural complexity.

[0038] The technical problem underlying the present invention is that of devising an error correction method and system having respective functional and structural features such as to allow the coding and decoding burdens to be reduced, reducing both the latency and the system structural complexity, thus overcoming the drawbacks of the solutions provided by the prior art.

Summary of the invention

[0039] The solution idea underlying the invention is to obtain for each coding and decoding block a good compromise between the speed and the occupied circuit area by applying a BCH code of the parallel type requiring a low number of parity bits and having a low latency.

[0040] By using this circuit solution it is possible to use for each coding and decoding block the most convenient parallelism and thus latency degree, taken into account that, in the Flash memory, the coding block is only involved in writing operations (only once since it is a non volatile memory), the first decoding block is involved in all reading operations (and it is the block requiring the greatest parallelism), while correction blocks are only called on in case of error and thus not very often.

[0041] In this way it is possible to optimise the system speed reducing in the meantime the circuit area occupied by the memory device.

[0042] On the basis of this solution idea, the technical problem is solved by a method as previously indicated and defined in claim 1.

[0043] The problem is also solved by a system as previously indicated and defined in claim 4.

[0044] The features and advantages of the methods and systems according to the invention will be apparent from the following description of an embodiment thereof given by way of indicative and non limiting example with reference to the attached drawings.

[0045] In these drawings:

Brief description of the drawings

[0046]

Figure 1 is a schematic block view of a BCH coding and decoding system;

Figure 2 is a schematic block view of the system of figure 1 emphasising some blocks being responsible for grouping and decomposing bits;

Figure 3 shows how the Reed-Solomon code, coding symbols rather than coding bits, operates;

Figure 4 shows how the parity calculation block operates for a traditional BCH code;

Figure 5 is a schematic view of a base block for calculating the parity in the case of the first parallelization type;

Figure 6 shows the block being responsible for calculating the parity as taught by the first parallelization method for a particular case;

Figure 8 is a schematic view of the block being responsible for searching the roots of the error detector polynomial through the Chien method by using a traditional BCH code;

Figure 9 specifies what the test required by the Chien algorithm means, particularly what summing the content of all the registers and the constant 1 involves;

Figure 10 shows what multiplying the content of a register by a power of α as required by the Chien algorithm involves;

Figure 11 is a schematic view of the architecture of an algorithm for searching the roots of an error detector polynomial in the case of a parallel BCH coding according to the first parallelization method;

Figure 12 specifies Figure 11 in greater detail, i.e. it shows for which powers of α it is necessary to multiply the register content in the case of the first by-four parallelization;

Figure 13 is a schematic view of a base block for calculating the parity according to the traditional BCH method;

Figure 14 is a schematic view of a circuit being responsible for calculating in parallel the parity according to the second method and by parallelizing twice;

Figure 15 is a schematic view of a circuit for calculating the parity by parallelizing q times according to the second

method;

Figure 16 is a schematic view of a circuit block being responsible for calculating the "syndrome" of a BCH binary code;

5 Figure 17 is a schematic view of a circuit block being responsible for calculating the "syndrome" for a parallelized code according to the second method of the present invention;

Figure 18 is a schematic view of the architecture of an algorithm for searching the roots of an error detector polynomial in the case of a known serial BCH code;

10 Figure 19 is a schematic view of the architecture of an algorithm for searching the roots of an error detector polynomial in the case of a parallel BCH coding according to the second method of the present invention;

Figure 20 is a schematic block view of the system of a further embodiment of the error correction system according to the invention, emphasising some blocks being responsible for grouping and decomposing bits in parallel;

Detailed description

20 **[0047]** With reference to the figures of the attached drawings, and particularly to the example of figure 20, an error correction system realised according to the present invention for information data to be stored in electronic non volatile memory devices, particularly multilevel reading and writing memories, is globally and schematically indicated with 10.

[0048] The system 10 comprises a block indicated with C representing the coding step; a block M indicating the electronic memory device and a group of blocks 1, 2 and 3 which are active during the decoding step. In particular, the block 1 is responsible for calculating the so-called code syndrome; the block 2 is a calculation block, while the block 3 is responsible for detecting the error by means of the Chien wrong position search algorithm.

25 **[0049]** The blocks indicated with 20.1 represent the parallelism conversion blocks on the data flow.

[0050] The invention is particularly suitable for the use in a Flash EEPROM memory M having a NAND structure; nevertheless nothing prevents the invention from being also applied to memories with NOR structure, provided that they are equipped with an error correction system.

30 **[0051]** Advantageously, the method and system according to the invention is based on an information data processing by means of a BCH code set parallel in the coding step and/or in the decoding step in order to obtain a low latency. The parallelism being used for blocks C, 1 and 3 is selected to optimise the system performance in terms of latency and device area.

[0052] Two different methods to make a BCH binary code parallel are provided.

35 **[0053]** In substance, the parallel scanning can be performed in any phase of the data processing flow according to the application requirements.

[0054] The mathematical basics whereon the two parallelization methods of a BCH code according to the invention are based will be described hereafter.

40 First parallelization method:

Coding (block C) and syndrome calculation (block 1)

[0055] The structures for the syndrome coding and calculation are very similar since both involve a polynomial division.

45 **[0056]** With reference to figure 4, the traditional BCH coding structure (prior art) is composed of b_i representing memory elements, by adders being simple binary xors and g_i can be either 1 or 0, i.e. the dividend coefficients, this means to say that either there is the connection (and consequently the adder) or such a connection does not exist.

[0057] The message to be coded enters the circuit performing the division and it simultaneously goes out being so shifted that in the end the coded message is composed of the initial data message and of the parity being calculated in the circuit.

50 **[0058]** The method intends to parallelize the division calculating the parity of the data to be written in the memory.

[0059] The structure being proposed, in the case of n input data, is represented in figure 5.

[0060] Registers 5.1 are initially reset. The words to be coded are applied to the logic network 5.2 in succession. After a word has been applied to the logic network 5.2, the outputs of the logic network 5.2 are stored in the registers 5.1. Once the message last word is applied, registers 5.1 will comprise the parity bits to be added to the data message.

55 **[0061]** It must be observed that the number of adders depends on the number one of the code generator polynomial.

[0062] The example of a BCH [15,11] code with generator polynomial $g(x) = 11011$ is to be seen, in the illustrative case of two input data (Figure 6). Hatched adders are not present since over there $g(x)$ is zero.

[0063] The syndrome calculation structure is absolutely similar to the coding structure. Each syndrome is calculated by dividing the datum being read from the memory for convenient polynomial factors of the code generator polynomial (prior art) and in the end the register content will be valued at α , α^3 , α^5 ed α^7 by means of a matrix up to obtaining the syndromes. The method being shown for parallelizing the parity calculation can thus be similarly used for the syndrome calculation.

Search for the error detection polynomial Fast BCH.

[0064] This block is unchanged with respect to the traditional BCH, but it must be observed that, although it is more complex than the decoding algorithm, it is the one requiring less time.

Search for error detection numbers

[0065] The syndromes being known, the error detection polynomial is searched, whose roots are the inverse of the wrong positions. This polynomial being known, it is thus necessary to find the roots. This search is performed by means of the Chien algorithm (prior art).

[0066] The algorithm carries out a test for all the field elements in order to check if they are the roots of the error detection polynomial.

[0067] If α^i is a root of the error detection polynomial, then the position n-i is wrong, where n is the code length.

[0068] Figure 8 is a schematic view of this structure, where registers L comprise the error detection polynomial coefficients, they are thus m-bit registers when operation occurs in a field GF(2^m) (in the case being taken as an example m=13).

[0069] At this point, for each field element, it must be seen if this is a root of the error detection polynomial, i.e. to check if the following equation is valid for some j.

$$1 + l_1 \alpha^j + \dots + l_i \alpha^{ji} = 0 \quad j = 0, 1, \dots, n-1$$

[0070] Consequently, a total sum is performed of all the register contents and the field element '1' as shown in figure 9. Multiplication blocks ($\times \alpha$, $\times \alpha^2$, ...) serve to generate all the field elements and they are performed by means of a logic network being described by means of a matrix whose input is an m-bit vector and whose output is an m-bit vector, as schematically shown in figure 10.

[0071] With reference to figure 11 parallelizing the algorithm means simultaneously carrying out several tests, and consequently checking several wrong positions. Each block represents a test and the content at the end of the last block is carried into the registers containing the error detection polynomial. In the figure case, four tests are simultaneously carried out so that with a single clock stroke it is possible to know if α^i , α^{i+1} , α^{i+2} o α^{i+3} are the roots of the error detection polynomial.

[0072] Figure 12 shows in greater detail the block composition, a four-step parallelism is used, where after every four steps the values return into the registers containing the four lambda coefficients. Also in this case there will be 52 registers (4 registers having 13 bits each).

Second parallelization method:

[0073] The structure of the system 10 according to the invention, incorporating coding and decoding blocks, is similar to the structure of an error correction system having a traditional BCH binary code; nevertheless, the internal structure of each block changes.

[0074] According to the invention it is provided to break the initial information message n times and to operate autonomously on each block. The possibility to break the initial information block into two blocks is considered by way of example; there will be thus bits in the even position and bits in the odd position so that two bits enter at a time in the circuit and the speed doubles.

[0075] Generally, parity bits are calculated according to the following relation (1), shown in figure 13:

$$par = x^{n-k} m(x) \bmod g(x) \quad (1)$$

where $m(x)$ is the data message and $g(x)$ is the code generator polynomial.

[0076] Operating in parallel, parity bits $par1$ and $par2$ are calculated according to these relations:

$$\begin{aligned}
 par &= par1 + par2 \quad \text{where:} \\
 par1 &= [(x^{n-k} m(x))_{\text{even}} \bmod g(x)] \text{ estimated in } \alpha^2 \\
 par2 &= \alpha \times [(x^{n-k} m(x))_{\text{odd}} \bmod g(x)] \text{ estimated in } \alpha^2
 \end{aligned}
 \tag{2}$$

[0077] An example of known circuit allowing the coding (1) to be realised is shown in figure 13.

[0078] Figure 13 thus schematically shows a base block being responsible for calculating the parity by sequentially operating on bits.

[0079] On the contrary, for calculating the parity in the double parallelization case the structure of figure 14 can be used.

[0080] The blocks indicated with "cod" perform both the division as in the traditional algorithm and the estimate in α^2 . This estimate can be carried out by means of a logic network being described by a matrix.

[0081] As regards odd bits, it is then necessary to multiply the results by α , following the modes being already described.

[0082] If the circuit is to be further parallelized in a plurality of q blocks, reference can be made to the example of figure 15 wherein the outputs of the multiple blocks converge in a single adder node producing the parity.

[0083] In the case of the traditional serial BCH binary coding it is possible to calculate the so-called code syndromes by means of the following calculation formula (3), corresponding to the circuit block diagram of figure 16, in the particular case of a BCH code [15,7]:

$$S_j = \sum_{i=0}^{n-1} \alpha^{ij} r_i \quad j = 0, 1, \dots, 2t - 1$$

[0084] On the contrary, according to the present invention, the syndrome calculation is set out on the basis of the following formulas (4):

$$\begin{aligned}
 S_j &= S1_j + S2_j \quad \text{where:} \\
 S1_j &= \sum_{l=0}^{\frac{n-1}{2}} \alpha^{2lj} r_{2l} \\
 S2_j &= \alpha^j \times \sum_{l=0}^{\frac{n-1}{2}} \alpha^{2lj} r_{2l+1}
 \end{aligned}$$

[0085] A possible implementation of the syndrome calculation according to the prior art is shown in figure 16 wherein two errors in a fifteen-long message are supposed to be corrected.

[0086] Consequently, a division is performed similarly to the coding in order to obtain the remainder in the registers marked with $s0, s1, \dots$. This remainder (seen as a polynomial) must then be valued in $\alpha, \alpha^2, \alpha^3, \alpha^4$ as above described, for example by using a logic network being described by matrixes.

[0087] The structure of figure 17 represents a simple parallelization obtained for calculating the syndromes for the code taken as an example according to the parallel structure proposed by the present invention and described by the previous formulas.

[0088] The blocks shown in figure 17 are substantially unchanged with respect to a traditional serial BCH binary coding; nevertheless, it is worth observing that the corresponding decoding algorithm is more complex, but it requires less latency.

[0089] In particular, two bits are analysed simultaneously, the evens and the odds and a structure similar to the traditional syndrome calculation occurs for both.

[0090] In fact, both for the evens and for the odds, there is a block calculating the remainder of the division of the input message with a polynomial, a factor of the code generator polynomial.

[0091] These remainders must be now valued in precise α powers, but differently from the traditional syndrome calculation, this time they are valued in α^2 , α^4 , α^6 and in α^8 .

[0092] In the case of odd bits, a multiplication for different α powers must be also performed.

[0093] The results of the even block and of the odd block will be then added in order to obtain the final syndromes.

[0094] Now, according to the prior art, a search algorithm of the roots of the error detection polynomial is located in block 3 and it provides the replacement of all the field elements in the polynomial

[0095] In substance, in the case of a serial BCH code, a test is performed for all the elements of the following field, according to the following formula:

$$1 + l_1 \alpha^j + \dots + l_t \alpha^{jt} = 0 \quad j = 0, 1, \dots, n-1 \quad (5)$$

[0096] In the traditional serial BCH code, always assuming to correct two errors, a circuit structure like the one of figure 18 would be obtained, corresponding to the previous formula (5).

[0097] According to the invention, and assuming to parallelize only once, two circuits are obtained, checking each half of the field elements and thus two different tests TEST1 e TEST2:

$$TEST1) 1 + l_1 \alpha^{2j} + \dots + l_t \alpha^{2jt} = 0 \quad j = 0, 1, \dots, \frac{n-1}{2}$$

$$TEST2) 1 + l_1 \alpha^{2j+1} + \dots + l_t \alpha^{(2j+1)t} = 0 \quad j = 0, 1, \dots, \frac{n-1}{2}$$

[0098] Consequently, parallelizing this portion means having several circuits replacing different field elements in the error detection polynomial. In particular, by parallelizing twice the diagram of figure 19 is obtained, which is reiterated twice, considering that for the second time registers are initialised by multiplying by α , expressly corresponding to the formulation of the two tests TEST1 e TEST2.

[0099] The first circuit performs the first test, i.e. it checks if the field elements being even α powers are the roots of the error detection polynomial, while the second checks if the odd α powers are the roots of the error detection polynomial.

[0100] The previous description has shown how to realise parallel structures for coding blocks C, syndrome calculation blocks 1 and error correction blocks 3.

[0101] It will be proved hereafter how, no correlation existing between the parallelism of one block and the parallelism of another block, it is very advantageous to structure the coding and decoding system 10 architecture in a structure having a hybrid parallelism, and thus a hybrid latency.

[0102] Specific reference will be made to the example of figure 20 showing a hybrid-parallelism coding and decoding system 11.

[0103] The coding and decoding example of figure 20 always concerns an application for multilevel NAND structure memory devices.

[0104] Assuming an error probability of 10^{-5} on a single bit for the NAND memory M, since the protection code operates on a package of 4096 bits, the probability that the package is wrong is 1 out of 50.

[0105] In order to understand if the message is correct, the syndrome calculation in block 1 must always be performed. For this reason for block 1 it is suitable to use a high parallelism in order to reduce the overall average latency.

[0106] The Chien circuit (block 3) performing the correction must be called on only in case of error (1 out of 50), it is thus suitable, for an area reduction, to use a low-parallelism structure for this single block 3 circuit.

[0107] For the coding block C it is possible to choose the most suitable parallelism for the application in order to optimise the coding speed or the overall system area.

[0108] The solution of the present invention allows the coding and decoding time to be reduced by varying the parallelism at will.

[0109] Another advantage is given by the fact that the independency of the parallelism of each block being involved in coding and decoding operations allows the performances and the system 10 or 11 area to be optimised according to the applications.

Claims

- 5 1. A method for correcting errors in read and write non volatile memory electronic devices, particularly Flash memories, of the type providing, for the information data to be stored, at least the use of a BCH binary error correction code, **characterised in that** it provides a processing with a first predetermined parallelism for the coding step, a processing with a second predetermined parallelism for the syndrome calculation and a processing with a third predetermined parallelism for calculating the error position, each parallelism being defined by a respective integer number being independent from the others.
- 10 2. A method according to claim 1, **characterised in that** it provides a parallel polynomial division for the coding and syndrome calculation.
- 15 3. A method according to claim 1, **characterised in that** the integer numbers concerning the first, second and third parallelism are different from each other.
- 20 4. A system for correcting errors in read and write non volatile electronic memory devices, particularly Flash memories, of the type providing the use of a coding block (C) having a BCH binary correction code and a cascade of decoding blocks (1, 2, 3) wherein a first block (1) is responsible for the code syndrome calculation, a second calculation block (2) and a third block (3) being responsible for the error detection, **characterised in that** it comprises a parallel division of at least one of said blocks in the coding and/or decoding step.
- 25 5. A system according to claim 4, **characterised in that** said parallel division provides the parallel multiplication of the structure of a given block and the association of bit composition and decomposition architectures.
- 30 6. A system according to claim 4, **characterised in that** said parallel division concerns coding (C), syndrome calculation (1) and error detection (3) blocks.
7. A system according to claim 4, **characterised in that** parity bits in the error correction are calculated according to the following relation:

$$par = x^{n-k} m(x) \bmod g(x)$$

35 where $m(x)$ is the data message and $g(x)$ is the code generator polynomial and **in that** in the parallel scanning parity bits (par1, par2) are calculated according to these relations:

40
$$par = par1 + par2 \quad \text{where:}$$

45
$$par1 = [(x^{n-k} m(x))_{\text{even}} \bmod g(x)] \text{ estimated in } \alpha^2$$

$$par2 = \alpha \times [(x^{n-k} m(x))_{\text{odd}} \bmod g(x)] \text{ estimated in } \alpha^2$$

50

55

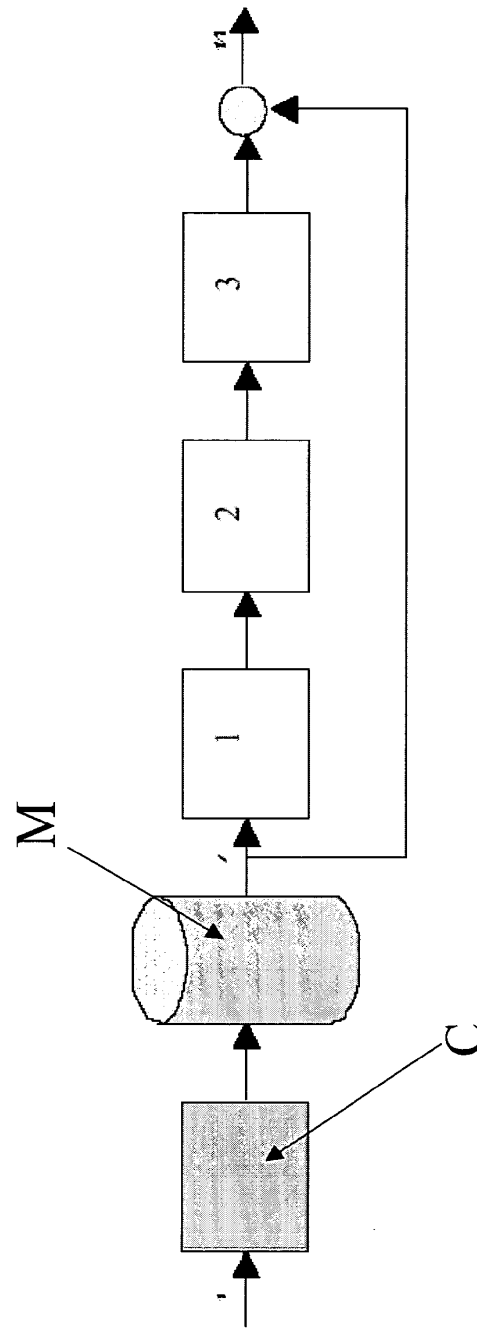
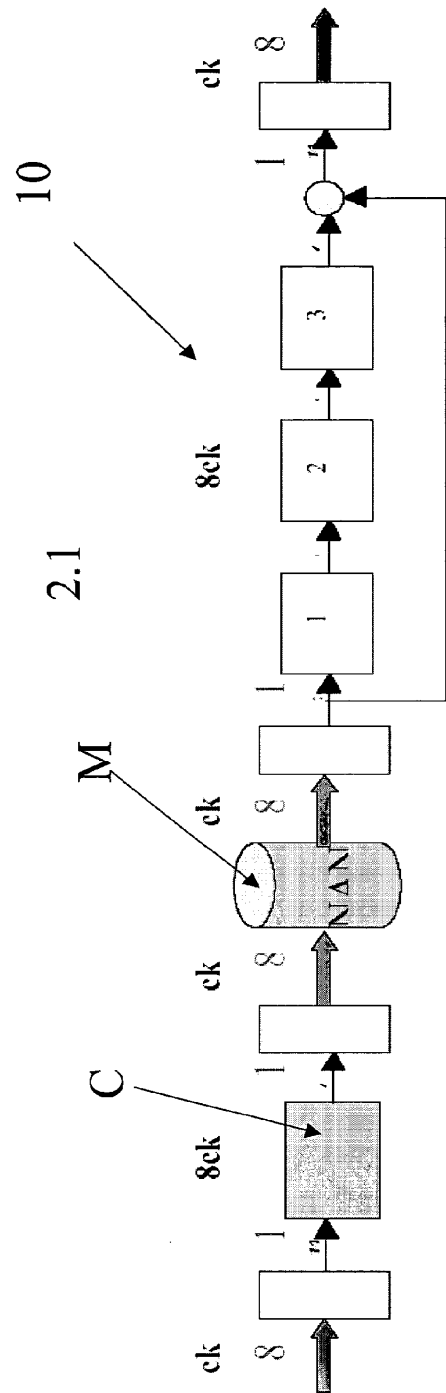
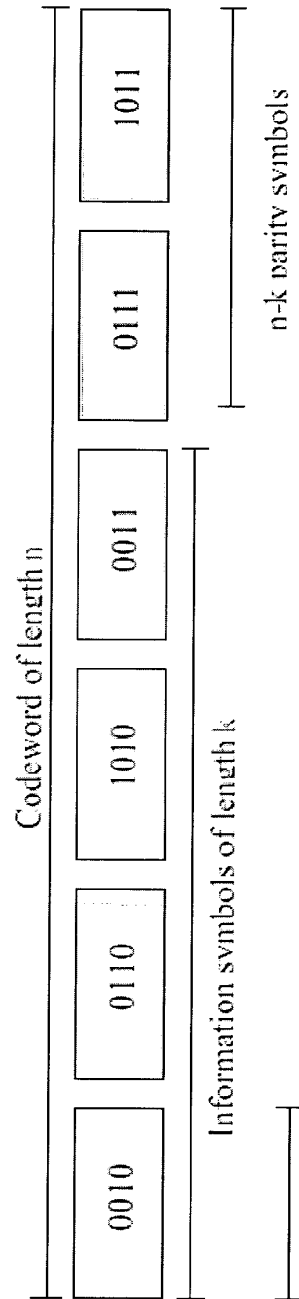


FIG. 1 PRIOR ART



2.1 2.1 2.1 FIG. 2

FIG. 3 PRIOR ART



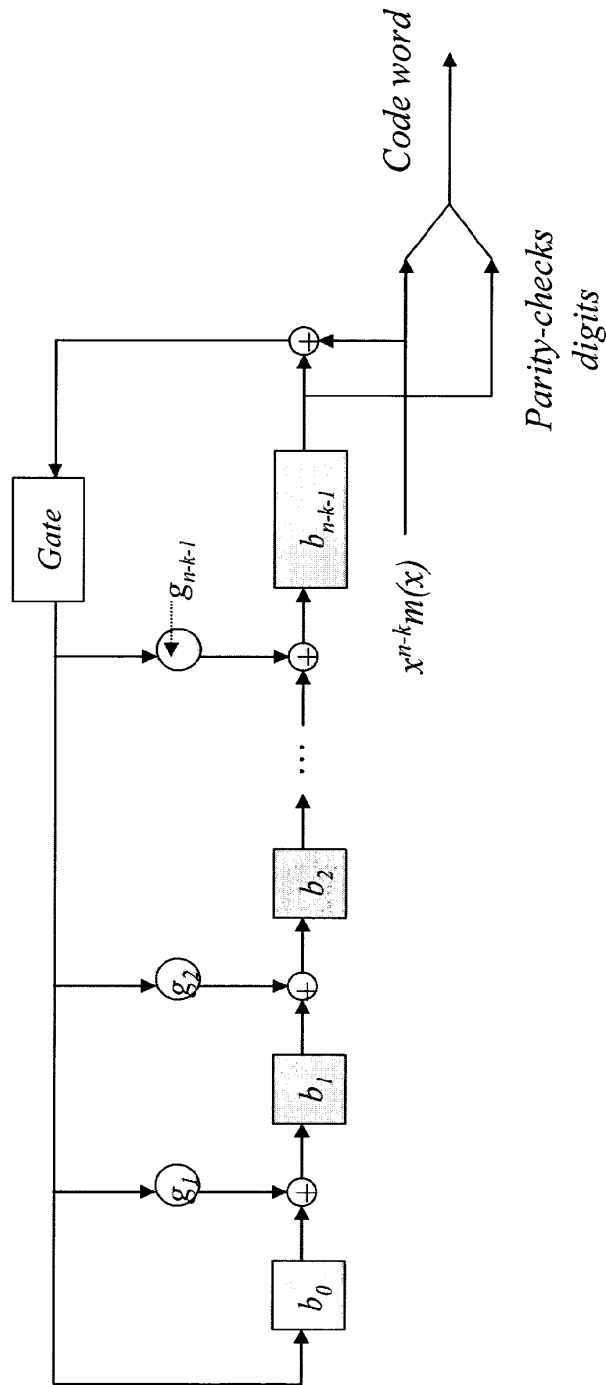


FIG. 4 PRIOR ART

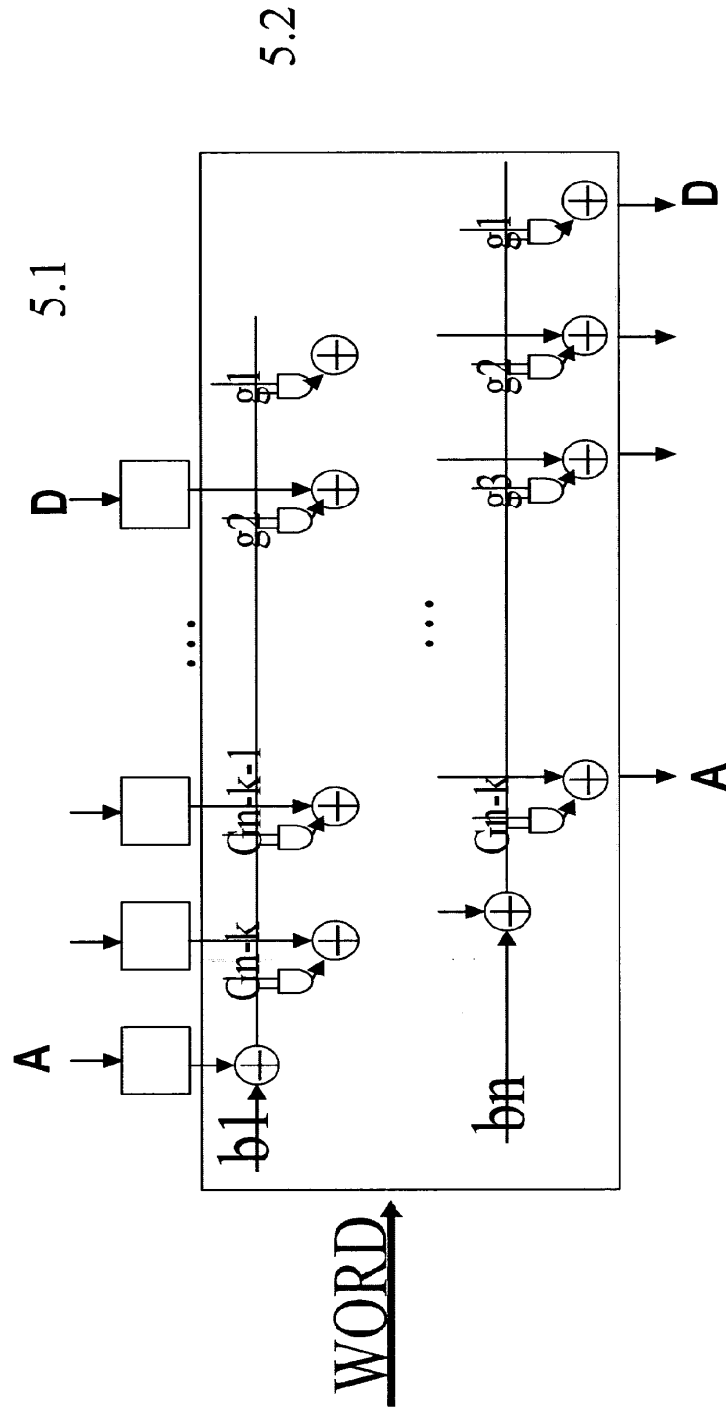
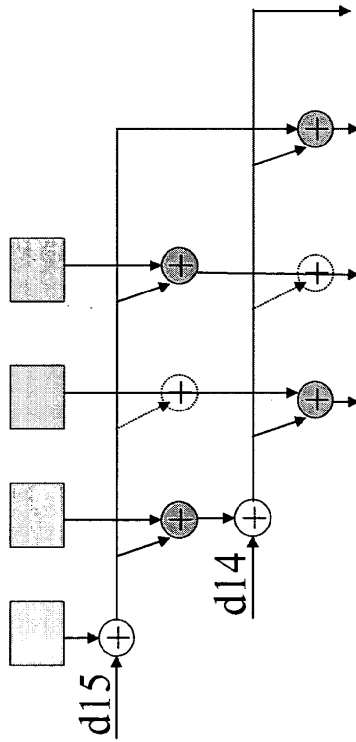


FIG. 5

FIG. 6



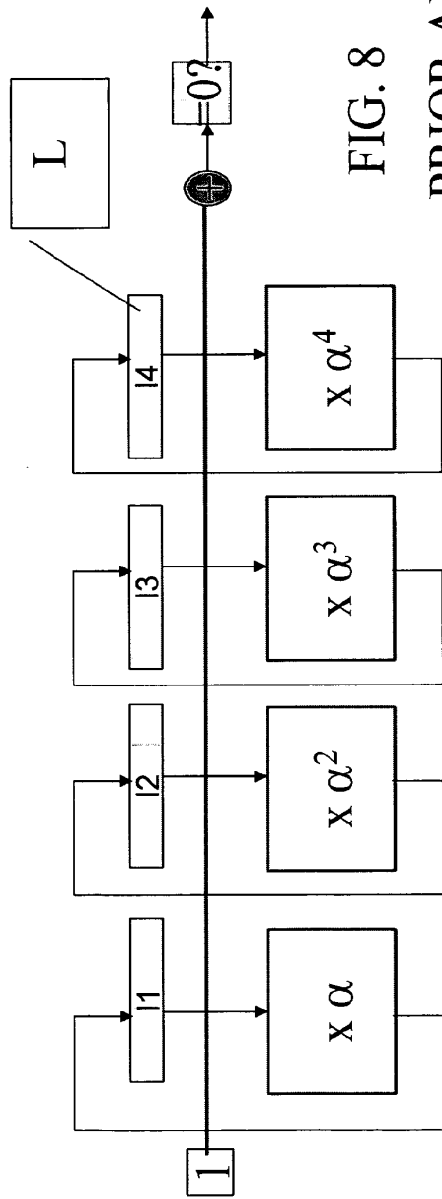


FIG. 8
PRIOR ART

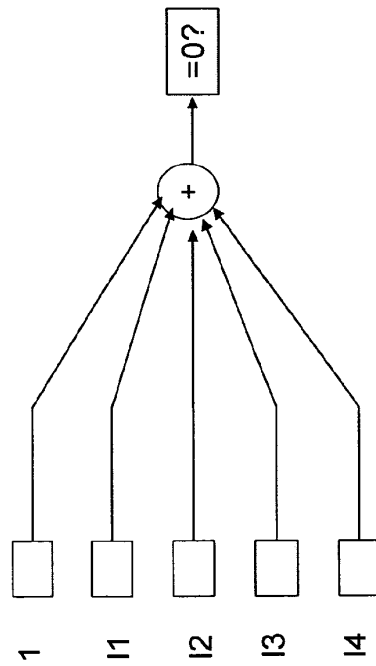
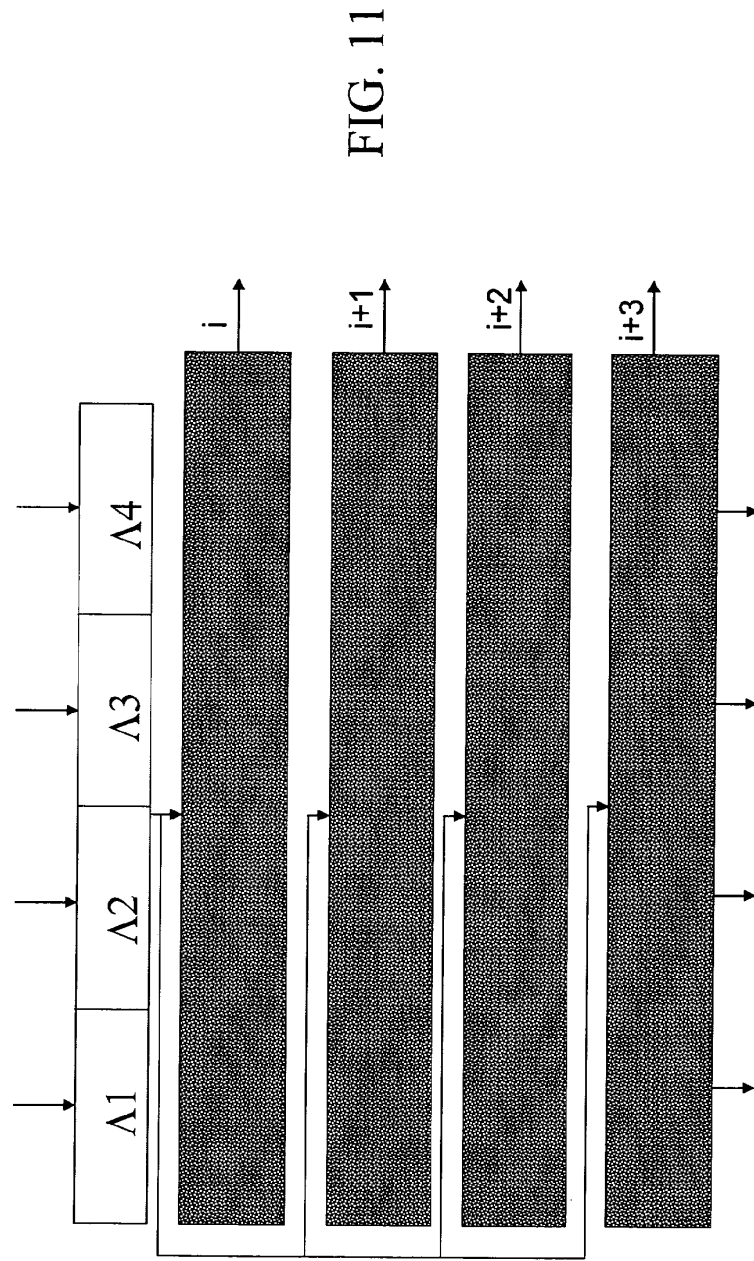
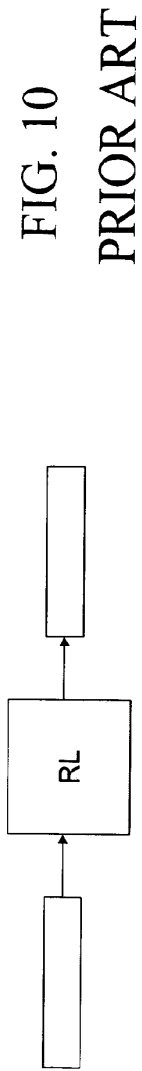


FIG. 9
PRIOR ART



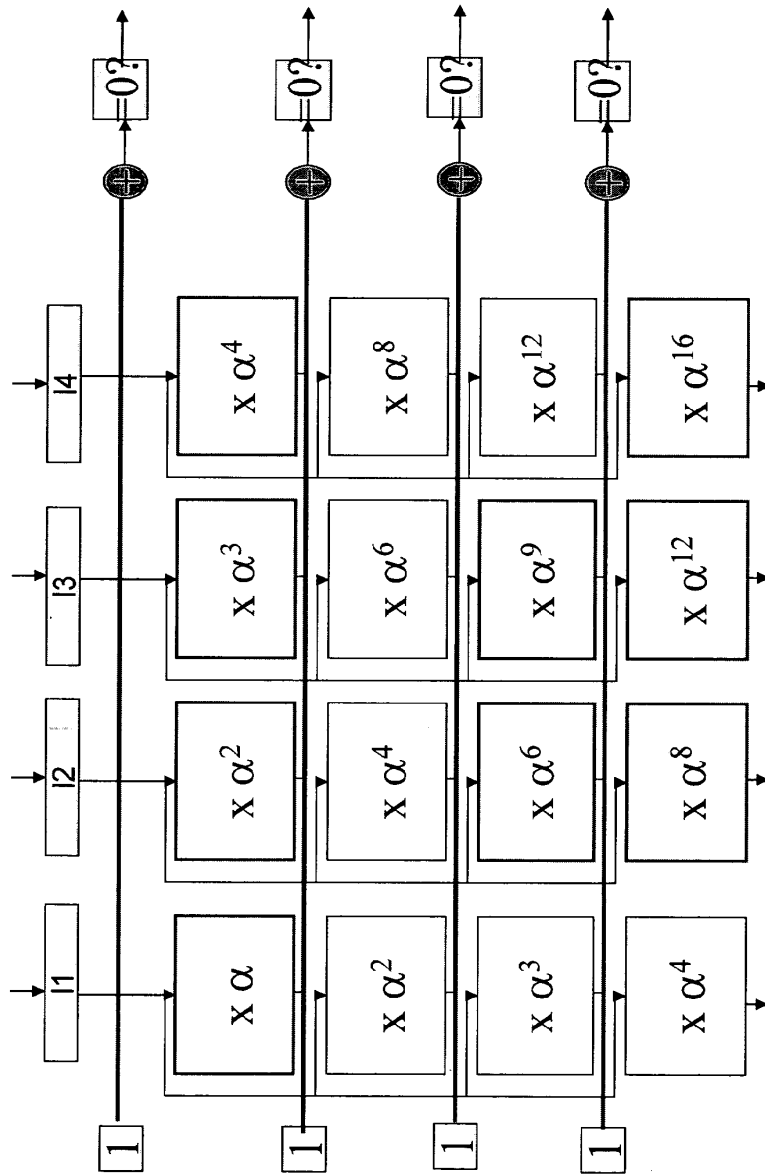


FIG. 12

FIG. 13
PRIOR ART

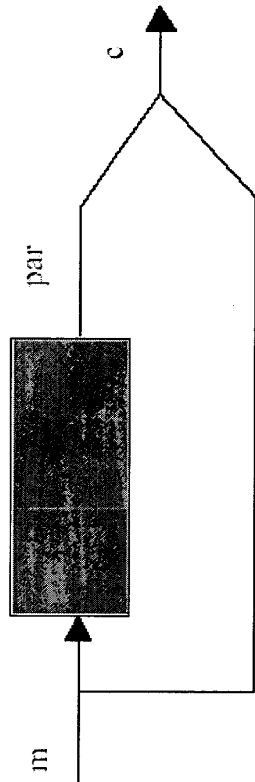


FIG. 14

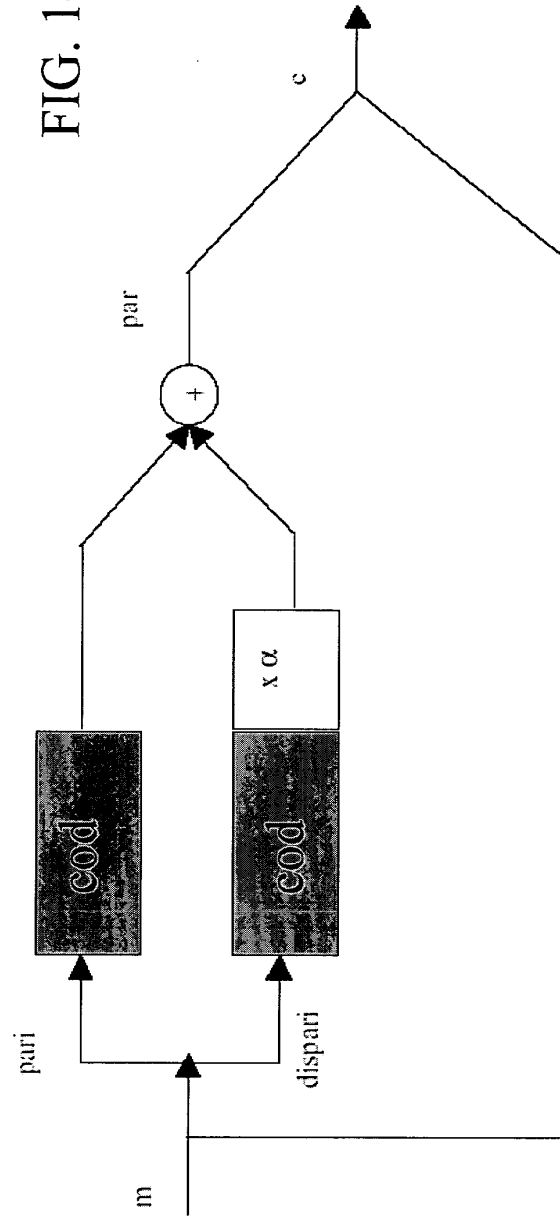
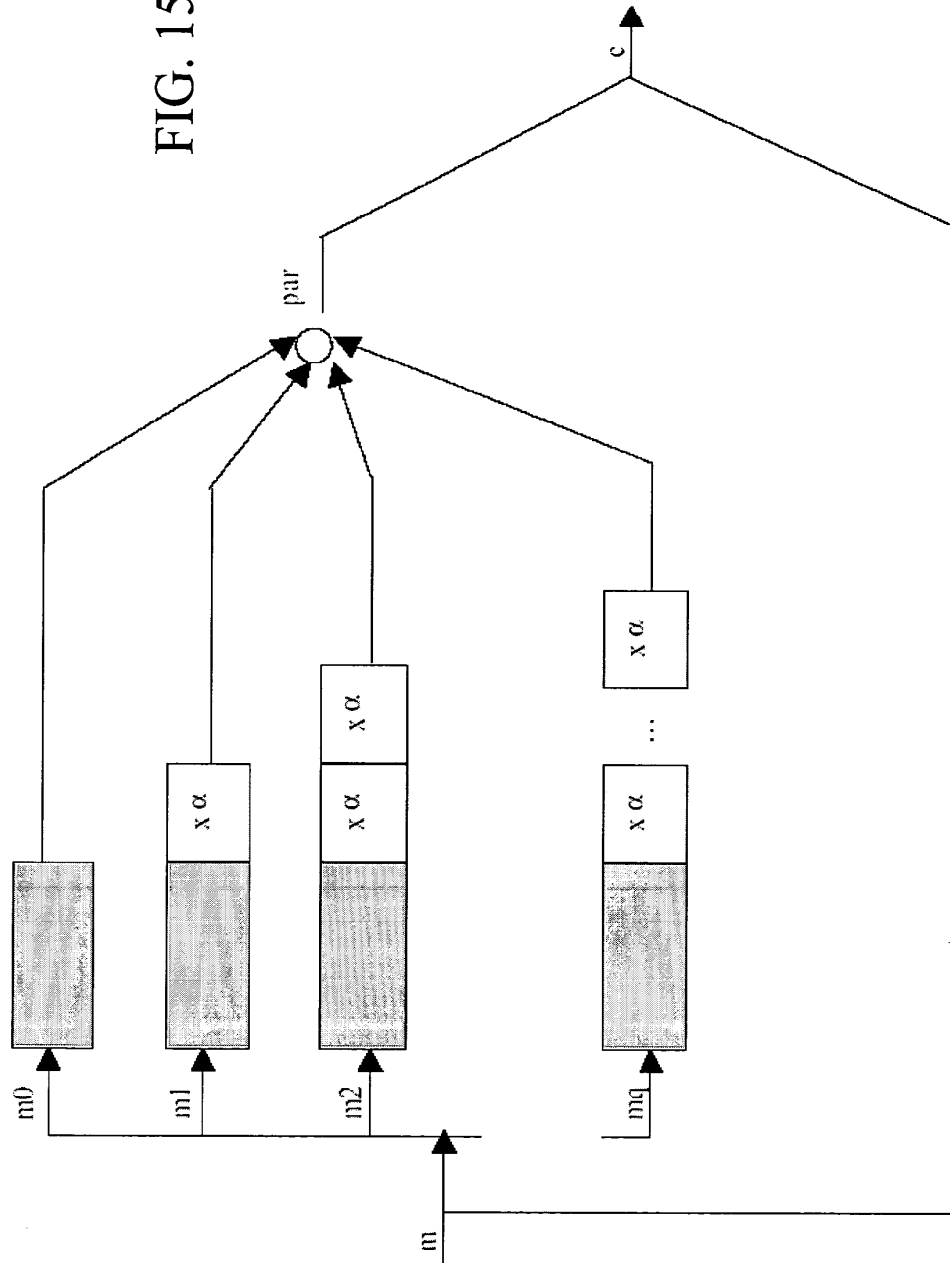


FIG. 15



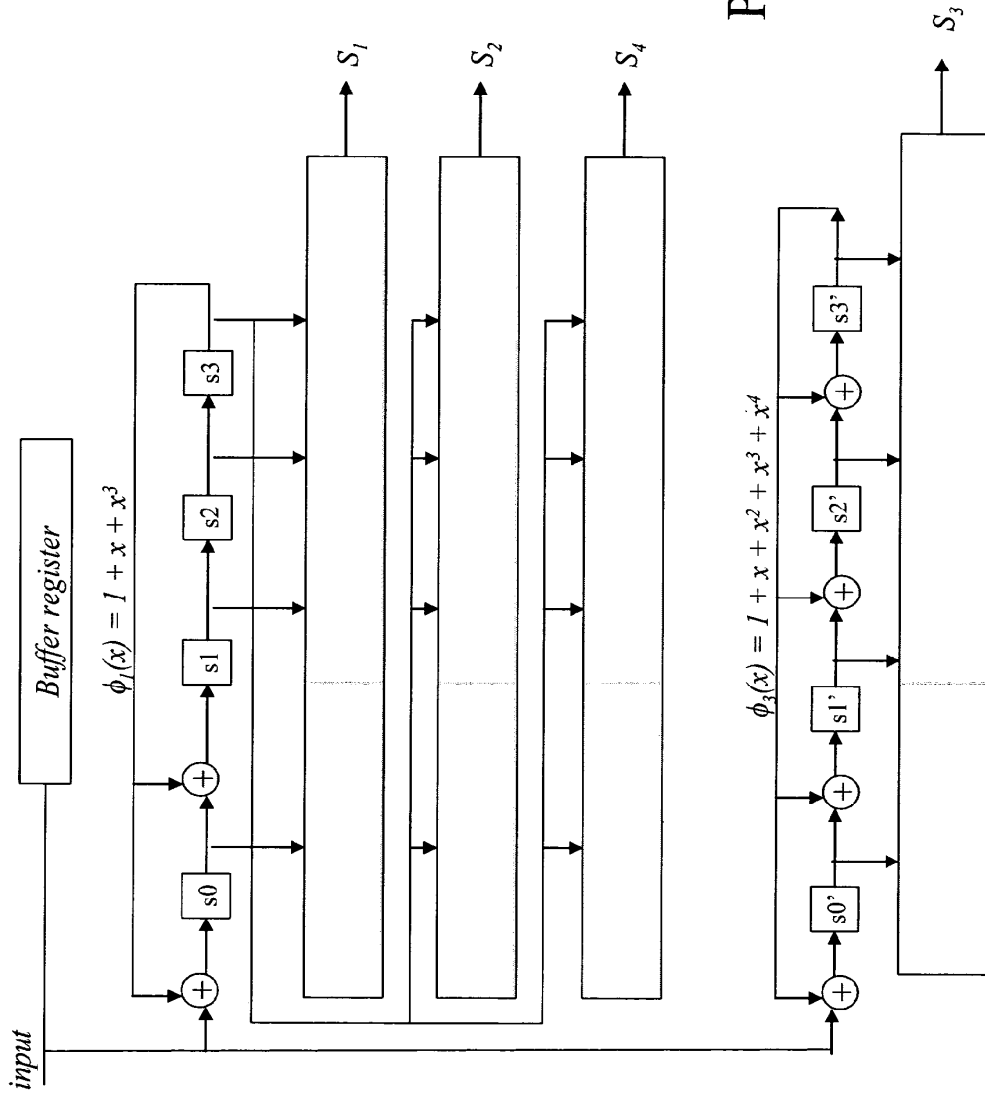


FIG. 16
PRIOR ART

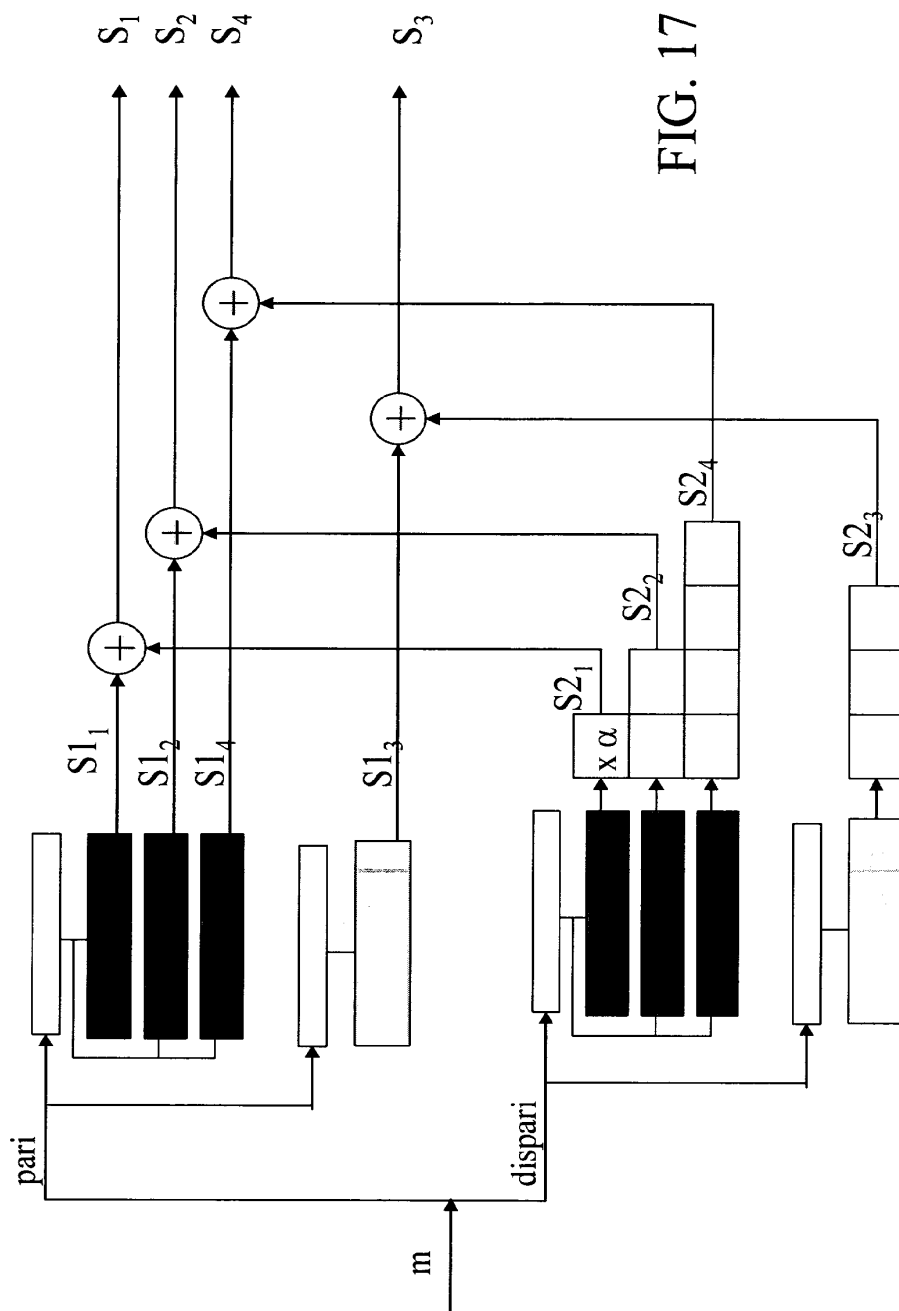
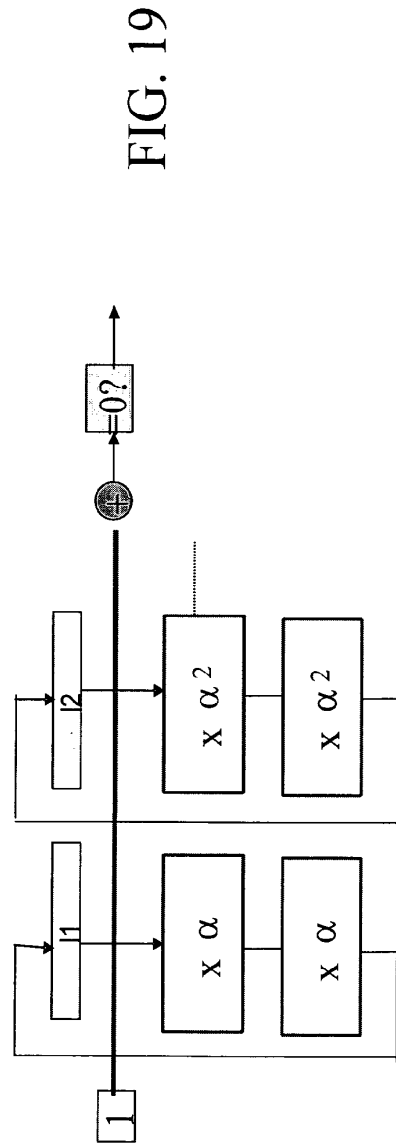
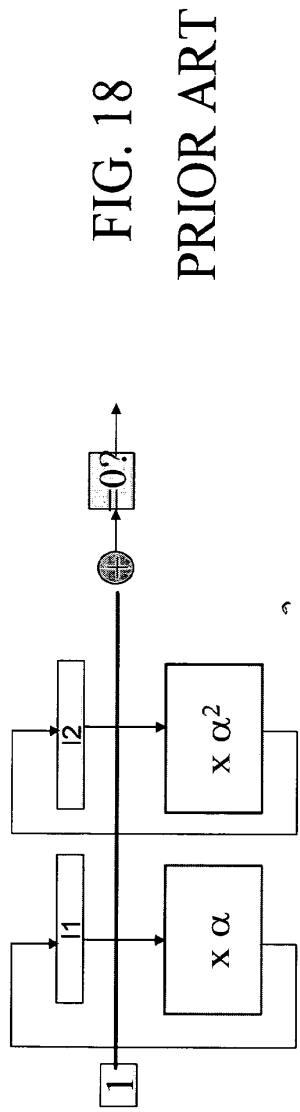
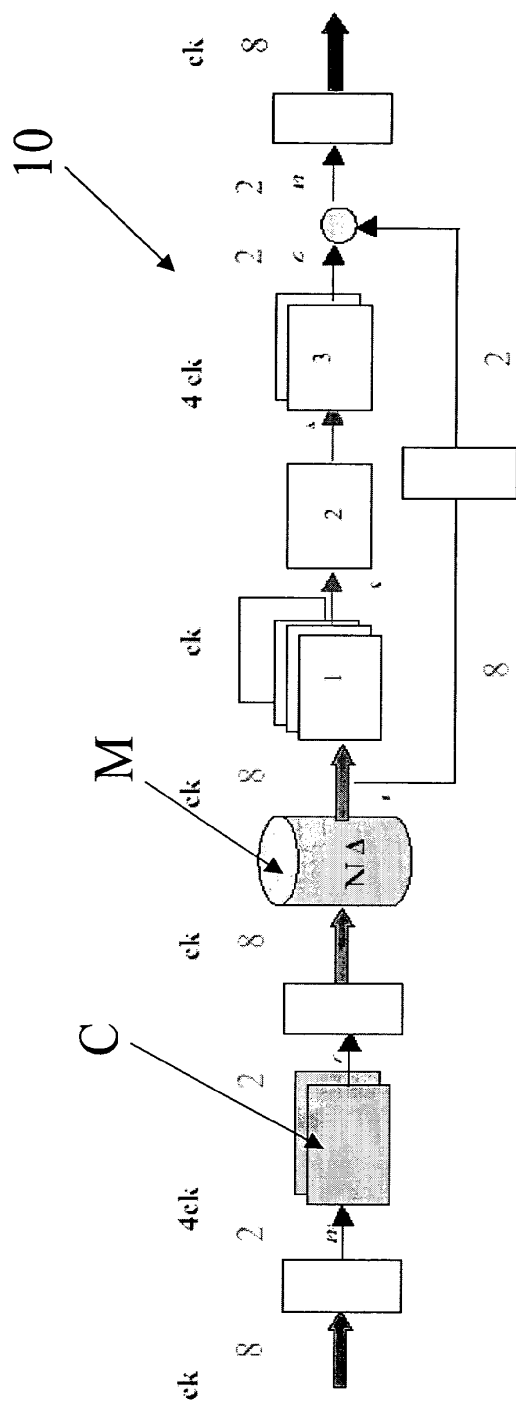


FIG. 17





20.1



European Patent
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EUROPEAN SEARCH REPORT

Application Number
EP 04 42 5486

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Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
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The present search report has been drawn up for all claims			
Place of search Munich		Date of completion of the search 27 April 2005	Examiner Bauer, R
CATEGORY OF CITED DOCUMENTS X: particularly relevant if taken alone Y: particularly relevant if combined with another document of the same category A: technological background O: non-written disclosure P: intermediate document T: theory or principle underlying the invention E: earlier patent document, but published on, or after the filing date D: document cited in the application L: document cited for other reasons &: member of the same patent family, corresponding document			

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For more details about this annex : see Official Journal of the European Patent Office, No. 12/82

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M., G. [NL/NL]; c/o Prof. Holstlaan 6, NL-5656 AA Eindhoven (NL). **BLUM, Martinus, W.** [NL/NL]; c/o Prof. Holstlaan 6, NL-5656 AA Eindhoven (NL).

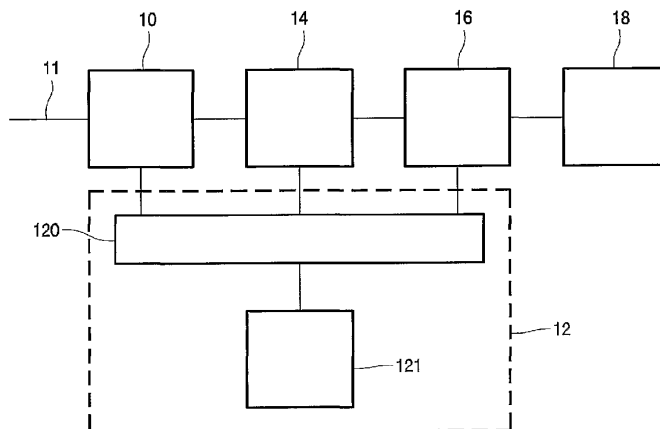
(74) Agents: **DE JONG, Durk, J.** et al.; Prof. Holstlaan 6, NL-5656 AA Eindhoven (NL).

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[Continued on next page]

(54) Title: DATA STORAGE AND REPLAY APPARATUS



(57) Abstract: A data storage and replay device uses measurements of the evolution of performance of the storage medium (typically a flash memory circuit) to predict an error rate of retrieval from a region of the storage medium. The prediction is used as a basis for dynamically selecting an ECC for encoding the data prior to storage of the data. The ECC is selected from a plurality of available ECC's so that a fastest encodable ECC is selected that is predicted to produce no more than a predetermined post-decoding error rate given said information. In this way the speed of transmission of data to the device can be maximized while keeping the error rate below an acceptable level in the predicted future after decoding. On decoding the data, which is typically audio or video data, is decoded and replayed at a predetermined speed. In another embodiment, the data stored using a plurality of ECC's together and an ECC is selected dynamically for decoding, so that an output data rate can be maximized or power consumption on replay can be minimized.

WO 2006/013529 A1

**Declaration under Rule 4.17:**

— as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii)) for the following designations AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HN, HU, ID, IL, IN, IS, JP, KE, KG, KM, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SM, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, UZ, VC, VN, YU, ZA, ZM, ZW, ARIPO patent (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR,

GB, GR, HU, IE, IS, IT, LT, LU, LV, MC, NL, PL, PT, RO, SE, SI, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG)

Published:

— with international search report
— before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

Data storage and replay apparatus

The invention relates to a device and method for storing and replaying data to and from a storage medium such as, in particular, a flash memory. Preferably the invention relates to storage and replay of real-time replayable data, such as audio or video streams.

US patent application No 2003/0217323 addresses the problems associated with deterioration of flash memory. As is well known flash memory and other storage media may suffer from bit errors. A conventional way of dealing with these bit errors is to store data using an error correcting code (ECC) and to use the ECC to correct errors on reading the data. However, the bit error rate of flash memory increases with time as the memory wears out. As a result error correction may eventually become impossible. US patent application No 2003/0217323 describes how detection of weak cells can initially be used to supply the error correction circuitry with information about bits that should be treated as unreliable. Ultimately detection of too many weak bits is used to trigger rewriting or even moving of a data block to a better memory area. US 2003/0033567 and US2003/0043647 similarly disclose moving of data in flash memory to better memory areas upon detection of too many errors. Thus weak memory areas are effectively abandoned.

The average elapsed service life before a memory area has to be abandoned depends on the quality of the ECC. A simple ECC like a Hamming code requires a memory area to be abandoned sooner than a more complex ECC like a Reed Solomon code. To retain as much useful memory for as long as possible it is therefore desirable to use the strongest possible ECC. A strong ECC, however, requires a considerable computational overhead both for encoding and decoding. For typical real-time replayable data, such as audio or video data (e.g. MP3 data), where no more than a predetermined reading speed is needed, reading speed limitations due to ECC decoding speed usually do not affect replay speed. In this case one can therefore use a strong ECC to maximize available memory space. The same goes for encoding during real time recording. However, even for this type of data use of the selection of the ECC involves a trade-off because encoding during downloading of prerecorded data, or decoding during transmission for a download limits downloading speed. Also, uses of a computationally intensive ECC increases power consumption.

Using such a trade-off to select a specific ECC for the entire useful life of the storage medium unnecessarily sacrifices speed and/or power consumption during the early life of the medium. The error rate of the storage medium like flash memory deteriorates during its useful life. Therefore, an ECC that makes a given amount of memory available at one stage during the useful life is unnecessarily complex to make the same amount of memory available earlier in the life of the medium.

Among others it is an object of the invention to make efficient use of a storage medium, particularly of a flash memory, whose error rate changes during its useful life, while permitting a high access speed to the medium.

Among others it is an object of the invention to maximize downloading speed for such a storage medium subject to efficient memory use, particularly for storing real-time replayable media data.

It is another object of the invention to reduce power consumption in a storage and replay apparatus, particularly in a battery operated apparatus.

A data storage and replay device according to the invention is set forth in Claim 1. According to the invention the device uses measurements of the evolution of the performance of the storage medium (typically a flash memory circuit) to predict an error rate of retrieval from a region of the storage medium. The prediction is used as a basis for selecting an ECC from a plurality of available ECC's for encoding the data prior to storage of the data. It may be noted that "encoding into an ECC" typically involves systematic encoding wherein the data is copied and parity symbols are added, in which case encoding before writing means determining the parity symbols from received data, not from data that has been retrieved from the memory region involved. This does not exclude later encoding of retrieved (and if necessarily corrected) data using other ECC's. However, it will be understood that encoding also encompasses non-systematic encoding, wherein data units are translated into codeword without always copying the data into the codeword. Preferably the ECC is selected from a plurality of available ECC's so that a fastest encodable ECC is selected that is predicted to produce no more than a predetermined post-decoding error rate given said information. In this way the speed of transmission of data to the device can be maximized while keeping the error rate below an acceptable level in the predicted future after decoding. In addition, use of such an ECC that requires a minimum of computation also reduces power consumption needed for the computation. This reduces overall power consumption, which may be an important factor in battery operated equipment.

Preferably a decoder circuit is provided that is arranged to read the data from said region as well as information that is indicative of the selected ECC for the region and to decode the data from the region according to the indicated ECC. Thus no further encoding is needed. However, in another embodiment the data may later be encoded according to a plurality of ECC's. If this happens once the data has been stored in the storage medium the further encoding does not compromise the speed of reception. In this case, the decoder may select to decode according to any ECC, for example the least error prone ECC. If the decoded data is used for real time signal rendering (e.g. audio and/or video signal rendering) in this case, any ECC may be selected that does not compromise rendering speed.

The decoder circuit may also select an ECC from a plurality of ECC's in which the data has been encoded, so as to decode the data according to the selected ECC. The ECC may be selected dependent on the information about the predicted error rate. In this case a variable speed of transmission of data from the device can be maximized while keeping the error rate below an acceptable level. This may be applied also if the data has not originally been written with an adaptively selected ECC, for example if the data has been written during real-time recording when the computational overhead for encoding is not critical so that a strong ECC may be used. Encoding information (e.g. parity symbols) according to different ECC's may then be added during recording or later.

Preferably respective information about the predicted error rate is determined for respective regions of the storage medium and the ECC is selected adaptively for each region independently. In this way differences between the quality of different regions, which may be due for example to more and less intensive prior use can be exploited to achieve higher access speed.

These and other objects and advantageous aspects will be described for examples of embodiments of the invention, using the following figure.

Figure 1 shows a store and replay apparatus

Figure 2 shows a further store and replay apparatus

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Figure 1 shows a store and replay apparatus comprising an input/encoder circuit 10, a flash memory circuit 12, an error rate assessment circuit 14, a read/decoder circuit 16 and an output circuit 18. Input/encoder circuit 10 has an input 11 which may be

coupled to the Internet, for example, for receiving download data. Optionally input/encoder circuit 10 may have a further input (not shown) for receiving real time audio and/or video data, for a microphone or camera for example. Input/encoder circuit 10 has an output coupled to flash memory circuit 12 and an interface coupled to assessment circuit 14. Read/decoder circuit 16 has an interface coupled to flash memory circuit 12 and assessment circuit 14 and an output coupled to output circuit 18. Output circuit 18 contains for example a display screen (not shown separately) and/or a loudspeaker (not shown separately) for rendering a video and/or audio signal that is encoded by data stored in flash memory circuit 12. Optionally, read/decoder circuit 16 may have a further output (not shown) for transmitting retrieved data to other devices (not shown) at a higher rate than to output circuit 18. Flash memory circuit 12 contains a memory proper 122 and a multiplexer 120 to give all of input/encoder circuit 10, assessment circuit 14 and read/decoder circuit 16 access to the same memory 122.

In operation read/decoder circuit 16 is used to read data from flash memory circuit 12 and to convert the data into signals that determine e.g. audio and/or video signals that are rendered by output circuit 18. Read/decoder circuit 16 performs correction of errors in the data from flash memory circuit 12 by decoding according to an ECC (Error Correcting Code). Typically, data encoded in an ECC comprises a copy of the actual data plus additional parity symbols. In this case, error correcting decoding involves determining whether the combination of the data and parity symbols is a code word of the ECC and, if not, determining a closest codeword from the ECC, in which case the data from that closest codeword is used. In this decoding process the closest codeword is determined for example by computing a number of syndromes from the retrieved combination of the data and parity symbols and generating corrections as a function of the computed syndromes. However, without deviating from the invention other types of decoding may be used, for example for decoding of non-systematic codes wherein the codeword does not contain a copy of the data.

Input/encoder circuit 10 writes the data into flash memory circuit 12 for later reading. Typically, the data is downloaded from another storage device, e.g. via the Internet, at a much higher data rate than needed for replay at output circuit 18. Input/encoder circuit 10 encodes the data into the ECC, typically by computing and adding parity symbols for the received data. Input/encoder circuit 10 writes the encoded data (e.g. the original data plus parity symbols) into flash memory circuit 12 for later reading. However, without deviating from the invention other types of encoding may be used, using non-systematic codes for

example which are not limited to adding redundant parity symbols, but include mapping data to codewords which do not necessarily contain a copy of the data.

The ECC used for writing and reading from flash memory circuit 12 is selected dynamically as a function of memory quality. The number of bit errors on reading block of data typically increases as a function of time as the memory wears out. The predicted number of bit errors is used to select which of a number of different available ECC's will be used. The more errors are predicted, the "heavier" the ECC that is selected, i.e. higher the ratio between correction capacity and required computation time of the ECC.

Assessment circuit 14 may use any convenient way to provide a prediction of the number of errors. In one embodiment for example assessment circuit 14 periodically reads data from flash memory circuit 12 (or monitors data read by read/decoder circuit 16) and uses the results of ECC decoding to detect errors, the frequency of detected errors being used as a prediction of the future error rate. In another embodiment, assessment unit 14 may measure the analog level of output signals from memory cells with higher accuracy than necessary for bit reading so as to determine the likelihood of erroneous bit reading. Combinations of these techniques and other techniques may be used as well. Typically, assessment unit 14 makes respective predictions for respective different regions of the memory (herein regions are e.g. rows of the memory matrix, or blocks of cells that can only be erased together), since the error rate may depend on the previous use of each region concerned. Assessment circuit 14 performs repeated quality assessments, typically periodically, but for each particular region preferably at least before the particular region is made available for writing downloaded data.

Input/encoder circuit 10 is typically arranged to perform encoding according to a selectable one of a number of different ECC's. Known ECC's may be used such as for example versions of a Hamming code or a Solomon code, possibly using multiple versions of these types of code with mutually different word sizes or number of parity bits, or product codes using any ECC for rows and columns. A choice may also be made between different versions of Reed Solomon codes with mutually different parameters, and/or between different versions of Hamming codes whereby the amount of computations and the robustness against errors can also be varied. Reed Solomon codes typically can correct more errors than Hamming codes, but also require more computations to encode the data (to determine parity symbols) and/or to decode the data (to determine syndromes and the associated corrections). Input/encoder circuit 10 ranks the available ECCs according to increasing computational requirements (the ECC's in the ranking being selected so that each ECC with higher

computational requirement in the ranking also has higher error correction capacity). Before reading input/encoder circuit 10 retrieves information about the predicted error rate from assessment circuit 14 and selects the ECC that will be used for encoding as a function of this information. Effectively, the range of possible predicted error rates is divided into successive sub-ranges, which are each associated with a respective ECC from the ranking, so that higher ranked (more computationally intensive) ECC are associated with higher predicted error rate. Input/encoder circuit 10 encodes the incoming data according to the ECC associated with the predicted error rate. Thus, a more computationally intensive ECC will be used when the predicted error rate is higher. Input/encoder circuit 10 stores information that identifies the ECC that has been used for later use during decoding. Typically, this information is stored in memory circuit 12 in association with the memory region where the data is stored (protected against errors, for example by use of some predetermined heavy ECC), or in a separate memory (not shown).

Typically information about different predicted error rates for different regions of memory circuit 12 is available. In this case input/encoder circuit 10 preferably adapt the ECC on a region by region basis, selecting the least heavy ECC allowed for each region (herein regions are for example respective lines of the memory matrix or blocks of memory cells that are erased together).

In the case of a high-speed download of the data, the ECC that is selected affects the download speed. On average successive data blocks can only be sent at a rate that allows for the computation of the ECC encoded data. Preferably, input/decoder circuit 10 has some mechanism to slow down the source of the data dependent on its readiness to perform encoding of a next block of data. A request/acknowledge handshake mechanism or a request for retry mechanism may be used for example. To a certain extent this need to slow down download speed can be mitigated by buffering the incoming data in a low error buffer memory (not shown) before writing the ECC encoded data into the more error prone memory circuit 122. A separate buffer such as an SRAM or DRAM memory, or a part of memory 122 that has low predicted error rate may be used. But when long download files typical for audio or video data are involved this approach is limited by the feasible buffer size. The average speed of incoming data has to match the ECC encoding speed.

It should be appreciated that the encoding according to the selected ECC (e.g. the computation of the parity symbols) cannot be performed on data that is stored in its eventual region of memory circuit 122 and later retrieved. After retrieval the data is prone to errors. Therefore encoding must take place essentially when the data is received. It should

also be appreciated that, of course, the disclosed embodiment is merely an example and that many alternatives exist. For example, without deviating from the invention the stored ECC encoded data may later be retrieved and encoded using a "heavier" ECC. As long as the original ECC is sufficiently strong to correct the expected number of errors this can be done without much risk of error. In this way, the stronger ECC may be used for reading, which protects against later wear of the memory. If all used ECC's provide for copies of the data plus parity symbols a number of ECC's may thus be used in parallel. As another example, assessment circuit 14 may be designed to test a region of memory circuit 122 and to predict its error rate in response to a request from input/encoder circuit 10 that is issued prior to writing into the region. In this case no information about the assessment need be stored for later use at an undetermined time. The information about the error rate may take the form of a number that is proportional to the error rate, but instead assessment unit may effectively select the ECC by using information that classifies the error rate according to required ECC.

Furthermore, although the example of selection of ECC's for high speed downloading has been used, it should be appreciated that it may also make sense to select the ECC at lower speed recording (e.g. of "live" audio and/or video data). Although the computation time for encoding may not be relevant in this case, it may be useful to use as light an ECC as consistent with the predicted error rate, so that high speed reading from memory circuit 122 for upload purposes is facilitated. This may also be advantageous even if the data rate is fixed, because use of the the least computationally intensive ECC minimizes power consumption, extending battery life of portable audio and/or video equipment. In an alternative embodiment, that data is stored using a plurality of ECC's for the same data, so that read/decoder circuit 16 will be able to select the most convenient ECC for decoding. Preferably input/encoder circuit 10 divides data in blocks of a predetermined size and writes each data block into a memory unit of a predetermined size, where the block leaves sufficient room for the maximum amount of additional data (e.g. parity symbols) due to any ECC, so that the memory unit size is independent of the ECC that is actually used. In this way addressing on retrieval can be performed independent of the selected ECC and optionally the ECC can later be changed without moving the data blocks.

On replay, read/decoder circuit 16 reads the information that identifies the ECC that has been used for encoding, reads the data from memory circuit 12 and decodes the data according to the identified ECC. Typically, the replay speed is so slow that the computational overhead for decoding poses no problem for the replay speed. In a further embodiment, wherein the stored data is later re-encoded with a heavier ECC, read/decoder

circuit 16 uses the heavier ECC. In this case the dynamically selected ECC is only used when the data is read before re-encoding has taken place.

In certain applications, a read/decoder circuit 16 may also be used to transmit data at high speed, for example during a further download wherein memory circuit 122 functions as source of the data. In this case the ECC that is used for decoding may limit the download speed. When the data has been written encoded by input/encoder circuit with one selected ECC (preferably one ECC per memory region), read/decoder circuit 16 accesses information that identifies this ECC and the identified ECC is used. In this case this ECC may affect download speed. Alternatively, when the data has been stored in memory circuit 122 encoded in a plurality of ECC's, read/decoder circuit 16 may query assessment circuit 14 to obtain information about a latest predicted error rate and to select the least computationally ECC that is able to correct errors at this rate. This may be done on a region by region basis, so that different ECC's may be used for different memory regions. The selected ECC's are used to decode the data. In this way a maximum download speed can be realized.

It should be appreciated that ECC decoding does not guarantee error free decoding. Accordingly, the selected ECCs are not selected according to a requirement that no errors should occur. Rather, the criterion is preferably that the fastest implementable ECC should be used that produces no more than a predetermined post-decoding error rate given the predicted error rate of the region of memory circuit 12 where the data is stored. Under exceptional circumstances the decoder or encoder may even switch to a faster ECC if overruling speed considerations prevent the use of a heavy ECC.

Although a separate input/encoder circuit 10, assessment circuit 14 and read/decoder circuit 16 have been shown, it should be understood that these functions may in practice be implemented using one circuit or distributed over different circuits in a different way. Suitably programmed programmable processors may be used for encoding and decoding, or a single suitably programmed processor for both encoding and decoding may be used for example. Similarly assessment circuit 14 may be a suitably programmed processor, possibly the same as used for encoding and/or decoding. The program or programs may be fixedly programmed or loaded using a computer program product such as a disk or an Internet signal. Figure 2 shows an example of a circuit wherein a programmable processor 20 is provided to execute a program from a program memory 22 to perform the functions of assessment, selection of the ECC, encoding and decoding.

CLAIMS:

1. A data storage and replay device, comprising
 - a storage medium (122);
 - an error rate assessment unit (14), arranged to generate information about a prediction of an error rate of retrieval from a region of the storage medium (122), based on
5 measurements of performance of the storage medium (122) during use;
 - an encoder (10) for performing encoding of received data into an ECC before storage of the encoded received data into the region, the encoder (10) selecting the ECC adaptively dependent on said information from the error rate assessment unit (14).
- 10 2. A data storage and replay device according to Claim 1, having an input circuit (10) that is arranged to adapt a rate of reception of the received data dependent on the selected ECC.
3. A data storage and replay device according to Claim 1, wherein the ECC is
15 selected from a plurality of available ECC's so that a fastest encodable ECC is selected that is predicted to produce no more than a predetermined post-decoding error rate given said information.
4. A data storage and replay device according to Claim 1, comprising a decoder
20 circuit (16) arranged to read the data from said region as well as information that is indicative of the selected ECC for the region and to decode the data from the region according to the indicated ECC.
5. A data storage and replay device according to Claim 4, having an output (18)
25 for outputting decoded data at least at a predetermined replay rate for use in audio and/or video replay.
6. A data storage and replay device according to Claim 1, wherein the storage medium (122) comprises a plurality of regions, the error rate assessment unit (14) assessing

respective information for respective ones of the regions, the encoder (10) selecting the ECC for each region particular dependent on the information for the particular region.

7. A data storage and replay device according to Claim 1, wherein the storage
5 medium is a flash memory circuit (122).
8. A data storage and transmission device, comprising
- a storage medium (122);
 - an error rate assessment unit (14), arranged to generate information about a
10 prediction of an error rate of retrieval from a region of the storage medium (122), based on measurements of performance of the storage medium (122) during use;
 - a decoder (16) for performing decoding of data, which is retrieved from a region of the storage medium (122), according to an ECC, the decoder (16) selecting the ECC from a plurality of available ECC's dependent on said information from the error rate
15 assessment unit (14).
9. A data storage and transmission device according to Claim 8, having an output circuit (16) that is arranged to adapt a rate of transmission of the retrieved and decoded data dependent on the selected ECC.
20
10. A data storage and transmission device according to Claim 8, comprising an encoder circuit (10) arranged to store the data initially encoded according to a selected one of the ECCs, which is selected adaptively dependent on said information from the error rate assessment unit (14).
25
11. A data storage and transmission device according to Claim 8, comprising an encoder circuit (10) arranged to store the data for retrieval and decoding so that the same data is encoded according to all of said plurality of ECC's.
12. A data storage and transmission device according to Claim 8, wherein the
30 storage medium is a flash memory circuit (122).
13. A method of writing data into a storage medium (122), the method comprising
- gathering measurements of performance of the storage medium (122) during

use;

- generating information about a prediction of an error rate of retrieval from a region of the storage medium (122), based on the measurements;
 - selecting an ECC from a plurality of ECC that are supported by an encoder
- 5 (10), the selection being adaptive in response to the generated information.
- encoding received data into the selected ECC with the encoder (10) before storage of the encoded received data into the region.

14. A method of reading data from a storage medium, the method comprising
- 10 - gathering measurements of performance of the storage medium (122) during use;
- generating information about a prediction of an error rate of retrieval from a region of the storage medium (122), based on the measurements;
 - selecting an ECC from a plurality of ECC that are supported by a decoder
- 15 (16), the selection being adaptive in response to the generated information.
- decoding received data with the decoder (16) according to the selected ECC before storage of the encoded received data into the region.

15. A computer program product comprising machine instructions which, when
- 20 loaded into a programmable computer (20, 22) make the computer (20, 22) perform the method according to claim 13 and/or 14.

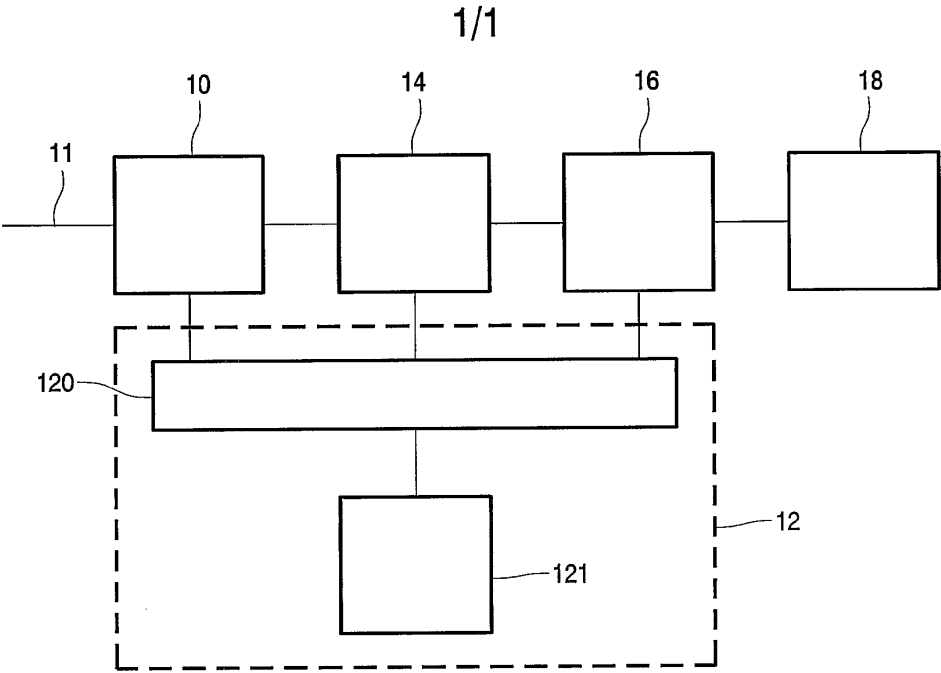


FIG. 1

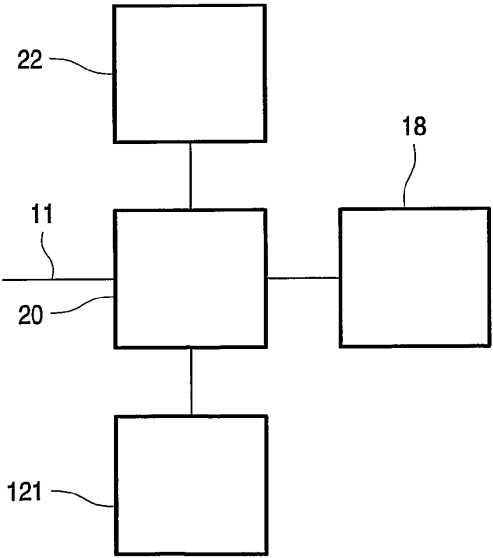


FIG. 2

INTERNATIONAL SEARCH REPORT

International Application No
PCT/IB2005/052475

A. CLASSIFICATION OF SUBJECT MATTER G11B20/18 G11C29/42 H03M13/35		
According to International Patent Classification (IPC) or to both national classification and IPC		
B. FIELDS SEARCHED Minimum documentation searched (classification system followed by classification symbols) G11B H03M G11C H04L		
Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched		
Electronic data base consulted during the international search (name of data base and, where practical, search terms used) EPO-Internal, PAJ, WPI Data, INSPEC		
C. DOCUMENTS CONSIDERED TO BE RELEVANT		
Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X A E	US 2003/037299 A1 (SMITH KENNETH KAY) 20 February 2003 (2003-02-20) paragraph '0002! - paragraph '0012! paragraph '0038! - paragraph '0042! paragraph '0050! - paragraph '0051! ----- US 2005/172179 A1 (BRANDENBERGER SARAH M ET AL) 4 August 2005 (2005-08-04) paragraph '0006! - paragraph '0008! paragraph '0018! paragraph '0029! paragraph '0047! - paragraph '0054! ----- -/--	1-7, 13, 15 8-10, 12, 14 1, 7, 13, 15
☒ Further documents are listed in the continuation of box C. ☒ Patent family members are listed in annex.		
* Special categories of cited documents : *A* document defining the general state of the art which is not considered to be of particular relevance *E* earlier document but published on or after the international filing date *L* document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified) *O* document referring to an oral disclosure, use, exhibition or other means *P* document published prior to the international filing date but later than the priority date claimed *T* later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention *X* document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone *Y* document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art. *G* document member of the same patent family		
Date of the actual completion of the international search 30 November 2005		Date of mailing of the international search report 22/12/2005
Name and mailing address of the ISA European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016		Authorized officer Ogor, M

Form PCT/ISA/210 (second sheet) (January 2004)

INTERNATIONAL SEARCH REPORT

International Application No
PCT/IB2005/052475

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT		
Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 4 701 923 A (FUKASAWA ET AL) 20 October 1987 (1987-10-20) column 1, line 64 - column 2, line 25 column 3, line 28 - column 5, line 14; figure 1 -----	1,4,5, 7-10,12, 14,15
X A	US 5 982 766 A (NYSTROEM ET AL) 9 November 1999 (1999-11-09) figures 5,6 column 3, line 5 - line 14 column 3, line 33 - column 4, line 67 -----	1,4,13, 15 8,10
X	US 2002/178421 A1 (HASSNER MARTIN AURELIANO ET AL) 28 November 2002 (2002-11-28) paragraph '0004! - paragraph '0006! paragraph '0011! paragraph '0058! -----	1,6,7, 13,15
X	US 2003/041298 A1 (BRUNER NIKKI M ET AL) 27 February 2003 (2003-02-27) paragraph '0011! - paragraph '0015! -----	1,13,15

Form PCT/ISA/210 (continuation of second sheet) (January 2004)

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Information on patent family members

International Application No
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US 5982766 A	09-11-1999	AU 2717597 A AU 2717697 A AU 721688 B2 AU 2717797 A AU 720308 B2 AU 2717897 A CA 2252693 A1 CN 1216652 A DE 19781710 T0 DE 19781715 T0 DE 69717443 D1 EP 0907950 A1 FI 982316 A FI 982317 A FI 982318 A WO 9741662 A1 WO 9741663 A1 WO 9741641 A2 WO 9741549 A1 TW 389014 B US 6195337 B1 US 5987319 A US 6163577 A	19-11-1997 19-11-1997 13-07-2000 19-11-1997 25-05-2000 19-11-1997 06-11-1997 12-05-1999 29-04-1999 29-04-1999 09-01-2003 14-04-1999 26-10-1998 26-10-1998 26-10-1998 06-11-1997 06-11-1997 06-11-1997 06-11-1997 01-05-2000 27-02-2001 16-11-1999 19-12-2000
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US 2003041298 A1	27-02-2003	NONE	

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(54) Forward error correction for memories

(57) The invention provides for methods, systems, and devices for forward error correction for flash memory and wherein encoded data from flash memory may be used to generate a number of data streams. At each of a number of error detection sub-modules operating in parallel, a different one of the data streams is processed. Each error detection sub-module may detect whether a portion of the respective received stream contains an error, and forward the portion to an error correction module. The error correction module, physically separate from the error detection sub-modules, may correct the forwarded portions of the respective received streams containing an error. The age and error rate associated with the flash memory may be monitored, and a coding rate or other aspects may be dynamically adapted to account for these factors.

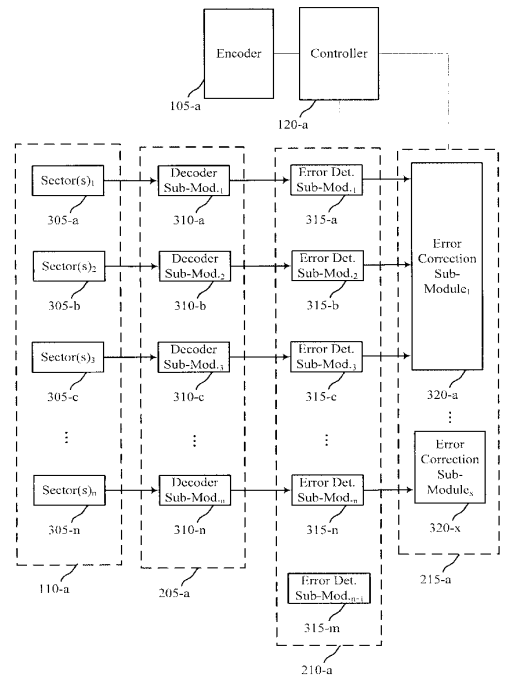


FIG. 3

Description

[0001] This application claims priority from co-pending U.S. Provisional Patent Application No. 61/234,911, filed August 18, 2009, entitled "FORWARD ERROR CORRECTION FOR FLASH MEMORIES" (Attorney Docket No. 026258-003700US), which is hereby incorporated by reference, as if set forth in full in this document, for all purposes.

[0002] The present invention relates to forward error correction (FEC) in general and, in particular, to FEC for flash memory. The advancements of flash memory technology in recent years has dramatically increased storage capacity and decreased the cost of non-volatile semiconductor memory. This has made Solid State Drives (SSDs) (typically a flash memory-based non-volatile memory system) an emerging substitute for magnetic Hard Disk Drive (HDD).

[0003] The use of FEC to enhance the reliability and longevity of flash memory is one of the challenges for making SSDs perform on par with HDDs. The present invention seeks to provide for forward error correction methods, decoders and systems having advantages over currently known such methods, decoders and systems.

[0004] Methods, systems, and devices are described for forward error correction for flash memory. Encoded data from flash memory may be retrieved to generate a number of data streams (which may, but need not be, partially decoded). At each of a number of error detection sub-modules operating in parallel, a different one of the data streams is processed. Each error detection sub-module may detect whether a portion of the respective received stream contains an error, and forward the portion of the respective stream containing an error to an error correction module. An error correction module, physically separate from the error detection sub-modules, may correct the forwarded portions of the respective streams.

[0005] The age and error rate associated with the flash memory may be monitored, and a coding rate may be dynamically adapted to account for these factors. The error rate may be monitored on a per-sector basis and, therefore, the coding rate may be adapted on a per-sector (or per-set of sectors) basis. As the error rate increases in certain sets of sectors, additional error-correction sub-modules assigned to those sectors may be powered-up to handle the increased error rate. In one example, there are fewer error correction sub-modules than error detection sub-modules; each error correction sub-module may be time-shared by a number of error detection sub-modules. Also, it is worth noting that the associations between flash memory sectors, error detection sub-modules, and error correction sub-modules may be changed dynamically in response to age and error rates, as well.

[0006] An example of a method includes: receiving encoded data from a flash memory comprising a plurality of data streams; processing, at each of a plurality of error detection sub-modules operating in parallel, a different one of the plurality of data streams, wherein each error detection sub-module is configured to: detect whether a portion of the respective received stream contains an error and forward the portion of the respective received stream containing an error to an error correction module; and correcting, with the error correction module separate from an error detection module, the forwarded portions of the respective received streams containing an error.

[0007] The method may include: dynamically modifying the error detection sub-modules assigned to receive data from respective sectors of flash memory; or powering-up, from an inactive mode, one or more of the error correction sub-modules responsive to an age of the flash memory. The powering-up may include: monitoring a rate of errors from the error detection module and powering-up one or more of the error correction sub-modules when the monitored rate of errors exceeds a threshold; or monitoring a rate of errors from the error detection module for each of a plurality of sectors of the flash memory and powering-up an error correction sub-module for assignment to a set of one or more of the monitored sectors when the monitored rate of errors for the set exceeds a threshold.

[0008] The method may also or alternatively include: modifying a coding rate for data to be stored as the encoded data on the flash memory responsive to an age of the flash memory. The modifying may include: monitoring a rate of errors from the error detection module and modifying a coding rate for data to be stored as the encoded data on the flash memory when the monitored rate of errors exceeds a threshold; or monitoring a rate of errors from the error detection module for each of a plurality of sectors of the flash memory and modifying a coding rate for data to be stored as the encoded data on the flash memory when the monitored rate of errors for the set exceeds a threshold.

[0009] An example of a flash memory decoder includes: a decoding module configured to receive encoded data from the flash memory and decode the received encoded data to generate a plurality of at least partially decoded data streams; an error detection module comprising a plurality of error detection sub-modules operating in parallel, each error detection sub-module configured to receive a different one of the plurality of at least partially decoded data streams, detect whether a portion of the respective received stream contains an error, and forward the portion of the respective received stream containing an error to an error correction module; and an error correction module separate from the error detection module and configured to correct the received portions of the respective received streams containing an error.

[0010] The flash memory decoder may include a power controller configured to selectively power-up one or more of the error correction sub-modules responsive to an age of or read error rate from the flash memory. The flash memory decoder may include an error monitoring module configured to monitor a rate of errors from the error detection module, and an adaptive encoding rate controller configured to modify a coding rate for a flash memory encoding module when the monitored rate of errors exceeds a threshold. The flash memory decoder may include the flash memory; an encoder

configured to encode data at a coding rate for storage as the encoded data on the flash memory; and an adaptive encoding rate controller configured to modify the coding rate responsive to an age of the flash memory. Each of the error detection sub-modules may read data from a set of one or sectors of flash memory different from other of the error detection sub-modules; the error correction module may include error correction sub-modules operating in parallel and fewer in number than the error detection sub-modules; each error detection sub-module may direct error-free portions of the respective received streams to bypass the error correction module; the error detection module may include the decoding module; and the encoded data may be encoded with a Hamming code, a BCH code, a Turbo code, or a low-density parity check code.

[0011] An example of a system includes an encoder configured to encode data for storage on a flash memory; the flash memory configured to store the encoded data; and a decoder configured to: retrieve the encoded data from flash memory to generate a plurality of data streams and process, at each of a plurality of error detection sub-modules of the decoder operating in parallel, a different one of the plurality of data streams. Each error detection sub-module may detect whether a portion of the respective received stream contains an error, forward the portion of the respective received stream containing an error to an error correction module of the decoder, and correct, with the error correction module separate from the error detection module, the forwarded portions of the respective received streams containing an error. The encoder may adaptively modify the coding rate responsive to an age of the flash memory or a rate of errors associated with the decoded data.

[0012] A further understanding of the nature and advantages of the present invention may be realized by reference to the following drawings illustrating, by way of example only, embodiments of the present invention. In the appended figures, similar components or features may have the same reference label. Further, various components of the same type may be distinguished by following the reference label by a dash and a second label that distinguishes among the similar components. If only the first reference label is used in the specification, the description is applicable to any one of the similar components having the same first reference label irrespective of the second reference label.

[0013] FIG. 1 is a block diagram of a flash memory decoder system according to various embodiments of the invention.

[0014] FIG. 2 is a block diagram of a flash memory decoder according to various embodiments of the invention.

[0015] FIG. 3 is a block diagram of a flash memory decoder system illustrating error detection and correction sub-modules according to various embodiments of the invention.

[0016] FIG. 4 is a block diagram of a flash memory decoder system illustrating an architecture for a decoder controller according to various embodiments of the invention.

[0017] FIG. 5 is a flowchart illustrating a method of decoding data from a flash memory according to various embodiments of the invention.

[0018] FIG. 6 is a flowchart illustrating a method of age responsive decoding of data from a flash memory according to various embodiments of the invention.

[0019] FIG. 7 is a flowchart illustrating a method of decoding data from a flash memory responsive to error rate according to various embodiments of the invention.

[0020] Methods, systems, and devices are described for forward error correction for flash memory. Encoded data from flash memory may be processed to generate a number of data streams. At each of a number of error detection sub-modules operating in parallel, a different one of the data streams is processed. Each error detection sub-module may detect whether a portion of the respective received stream contains an error, and forward the portion to an error correction module. An error correction module, physically separate from the error detection sub-modules, may correct the forwarded portions. The age and error rate associated with the flash memory may be monitored, and a coding rate or other aspects may be dynamically adapted to account for these factors.

[0021] This description provides example embodiments only, and is not intended to limit the scope, applicability, or configuration of the invention. Rather, the ensuing description of the embodiments will provide those skilled in the art with an enabling description for implementing embodiments of the invention. Various changes may be made in the function and arrangement of elements without departing from the spirit and scope of the invention.

[0022] Thus, various embodiments may omit, substitute, or add various procedures or components as appropriate. For instance, it should be appreciated that in alternative embodiments the methods may be performed in an order different from that described, and that various steps may be added, omitted, or combined. Also, features described with respect to certain embodiments may be combined in various other embodiments. Different aspects and elements of the embodiments may be combined in a similar manner.

[0023] It should also be appreciated that the following systems, methods, and software may individually or collectively be components of a larger system, wherein other procedures may take precedence over or otherwise modify their application. Also, a number of steps may be required before, after, or concurrently with the following embodiments.

[0024] Although much of the following discussion relates specifically to flash memory, aspects of the inventions are applicable to other forms of solid state memory. Generally, there are two predominant types of flash memory architectures: NOR and NAND. For the purposes of this disclosure, much discussion is directed to NAND-type flash, while again noting that principles set forth herein have wider applicability.

[0025] There are two primary NAND flash technologies. The earlier versions of NAND flash were Single-Level Cell (SLC). With SLC Flash, there is only one programmed state in addition to the erased state. The total of two states allows a single data bit to be stored in the memory cell. The desire for higher density led to the more advanced Multiple-Level Cell (MLC). With MLC flash, there are multiple programmed states in addition to the erased state which allows multiple bits to be stored per memory cell.

[0026] Because of this increase in density and the related issues in manufacturing, one of the challenges for flash memory is to maintain high reliability and longevity. The deterioration of the oxide over time, and the disruptions from neighboring memory pages, can lead to data retention and corruption issues translating into bit errors. While the chances of any given data bit being corrupted is quite small, the vast number of data bits in a storage system makes the likelihood of data corruption a very real possibility. FEC may be one of the tools used to address these bit errors to improve the reliability and lifespan of flash memory.

[0027] Systems, devices, methods, and software are described for FEC for flash memory. Turning first to **FIG. 1**, a flash memory system 100 is illustrated. The system includes an encoder 105, flash memory 110, a decoder 115, and a controller 120. This flash memory system 100 may be a stand-alone device, or may be integrated (in whole or in part) with a computer, server, phone or mobile device, tablet, television, or any other computing device.

[0028] Each of these system 100 components may be in communication with each other. The encoder 105, decoder 115, and controller 120 may, individually or collectively, be implemented with one or more Application Specific Integrated Circuits (ASICs) adapted to perform some or all of the applicable functions in hardware. Alternatively, the functions may be performed by one or more other processing units (or cores), on one or more integrated circuits. In other embodiments, other types of integrated circuits may be used (e.g., Structured/Platform ASICs, Field Programmable Gate Arrays (FPGAs), and other Semi-Custom ICs), which may be programmed in any manner known in the art. The functions of each unit may also be implemented, in whole or in part, with instructions embodied in a memory, formatted to be executed by one or more general or application-specific processors.

[0029] The encoder 105 may receive data to be stored, and encode the data (e.g., adding parity information) for storage in the flash memory 110 as encoded data. The decoder 115 may include a number of sub-components (not shown). An embodiment of the decoder 115 includes an error correction module in communication with and physically separate from an error detection module. The decoder 115 may process the encoded data to generate a number of data streams (which may, but need not be, decoded in whole or in part). The decoder 115 may process each stream at a different error detection sub-module operating in parallel in the decoder 115. Each error detection sub-module may detect whether a portion of the respective received stream contains an error, and then forward the portion of the respective received stream containing an error to the error correction module. The error correction module may correct the forwarded portions of the respective received streams containing an error.

[0030] There are a number of different FEC schemes and codes that may be used in the flash memory system 100 introduced above. The system 100 functionality may be also be leveraged in a number of ways. For example, the error detection module may detect and flag bit errors, and this may allow sectors of memory with errors exceeding a threshold amount to be avoided by replacing such sectors with other sectors from a pool of available substitutes. The encoder 105 may, also or alternatively, change the code rate for the error-laden sections. As flash become more dense, the inherent bit error probability becomes higher.

[0031] Some simple FEC coding may be used to clean up these errors. The Hamming Code, with correction capacity of 1 bit and detection capability of 2, may be used with flash memory 110. With the desire for improving the performance, as well as the increased probability of inherent bit errors because of the denser memories, Bose Chaudhuri Hocqunghem (BCH) codes may be used, including the binary BCH and non-binary BCH (Reed Solomon (RS)) codes. These codes offer a higher correction capacity in comparison to the Hamming Code.

[0032] BCH encoding/decoding architectures may be the foundation of error correction in flash memory. However, there are more advanced coding options that may in some instances provide better performance than BCH codes. These codes may be used in flash memory 110, particularly for higher density flash and in applications where performance demands increase. Convolutional Turbo Codes (CTCs), Turbo Product Codes (TPCs), and low density parity check codes (LDPCs) are examples of the coding schemes that may be used. These state-of-the-art codes perform very close to the theoretical limits (Shannon Limits) of error correction, providing very high coding gain and improvement in Bit Error Rate (BER) performance for a given amount of redundancy.

[0033] Flash memory does have an inherent probability of error. Depending on the flash technology, this error rate may typically be somewhere between $1e-5$ and $1e-8$. To be able to match an HDD read/write bit error rate of $1e-15$, a FEC scheme may be used. The measure of how good a job a code can perform in increasing the reliability depends upon its correction capacity. If the probability of bit error for flash memory 110 is p and the correction capacity of the code is t bits over a codeword length of n bits, the probability of making an error may be expressed as:

$$P_{\text{decoded}} = \sum_{i=t+1}^n p^i * (1-p)^{n-i} \quad (1)$$

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[0034] From equation (1), for a given p the higher the correction capacity of the code, the smaller the probability of error after the decoding will be. The correction capacity can be expressed as the number of bits a code can correct over a codeword length, or an input BER, or probability of error that it can take down to a certain target decoded BER. The advanced codes may correct more errors over a certain length, or take a higher input BER to create the same decoded BER.

[0035] There is incentive to use advanced codes for flash memory 110 even with not so dense memories. If the inherent error performance of flash memory 110 stayed at a certain low level, there would probably be decreased need for advanced codes. But, in practice, flash memory 110 performance tends to degrade over time. This means that even with an advanced code to help improve the reliability of a flash memory 110, over time the flash memory 110 may become lossy and, once the error rate is high enough, it may be beyond repair by the code being used.

[0036] In one example, the rate of errors or age of the flash memory 110 may be monitored, and the coding rate for data to be stored on the flash memory 110 may be modified in response thereto. Thus, a more robust coding rate may be used as the decoded error rate increases. The error monitoring may take place on a per-sector basis, and the code rate modification may similarly take place on a per-sector basis. In another example, the rate of errors or age of the flash memory 110 may be monitored, and error correction sub-modules may be powered-up in response thereto. Power savings may be achieved by keeping certain error correction sub-modules in an inactive mode until the flash memory reaches a certain age.

[0037] As noted, the flash memory 110 may be partitioned into a pool of small fixed-size sectors, and FEC may be applied on a sector-by-sector basis. The flash memory 110 size may be defined by the number of sectors that it contains. As there is a chance of sectors going bad over time, there may be a reserve/spare sector pool that allows the controller to replace the bad sectors by the spares as needed to extend the life of the flash. The error detection sub-module and error correction sub-modules may be dynamically assigned to various sectors, and the number powered-on may be increased or decreased.

[0038] A wear leveling technique may be used to make sure that various areas/sectors of the Flash "age" at a similar rate. Instead of the same sector being used over and over again, the read/writes are spread over much or the entire flash. And this translates into the probability of any sector being good (p_{good}) may be substantially the same for the various sectors in flash memory 110. If the size of the flash is N sectors and there are Δ spare sectors, the probability that the flash is still usable after time is:

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$$P_{\text{usable}} = \sum_{i=N}^{N+\Delta} (c_i^{N+\Delta} * (p_{\text{good}})^i * (1-p_{\text{good}})^{N+\Delta-i}) \quad (2)$$

40

[0039] p_{good} may be a function of use time for the flash memory 110 sector. This is a component that is dependent upon the correction capacity of the code used. Thus, even with the spare sectors and the wear-leveling technique, the codes may play a key role in the flash being usable after a certain use time.

[0040] One of the concerns regarding advanced codes is how they fit into the sector sizes and overhead requirements of some flash memory architectures. TPC and LDPC codes offer an excellent degree of freedom in selecting the various code parameters like information block size, coded block size, and correction capacity, and would allow customization to suit any number of flash configurations.

[0041] FIG. 2 is a block diagram 200 of a flash memory decoder 115-a according to various embodiments of the invention. The flash memory decoder 115-a may, for example, be the decoder 115 of FIG. 1, although flash memory decoder 115-a may be implemented in a number of other systems and devices, as well. The flash memory decoder 115-a includes a decoder module 205, an error detection module 210, and an error correction module 215, and each of may be in communication with each other. In one example, the error detection module 210 includes a number of sub-modules configured to detect errors on decoded streams of data. The error correction module 215 may be physically separate from each error detection sub-module, and may also include a number of sub-modules (each of which may be time-shared by a number of error detection sub-modules).

[0042] These components and sub-modules therein may, individually or collectively, be implemented with one or more Application Specific Integrated Circuits (ASICs) adapted to perform some or all of the applicable functions in hardware.

Alternatively, the functions may be performed by one or more other processing units (or cores), on one or more integrated circuits. In other embodiments, other types of integrated circuits may be used (e.g., Structured/Platform ASICs, Field Programmable Gate Arrays (FPGAs), and other Semi-Custom ICs), which may be programmed in any manner known in the art. The functions of each unit may also be implemented, in whole or in part, with instructions embodied in a memory, formatted to be executed by one or more general or application-specific processors.

[0043] The decoder module 205 may receive encoded data from flash memory, and process the received encoded data to generate a number of data streams. In one embodiment, the decoder module processor may buffer, de-interleave, or perform certain aspects of the decoding process, and thereby generate decoded (or partially decoded) data streams. As noted, the error detection module 210 may include a number of error detection sub-modules operating in parallel. Each (or a subset) of the error detection sub-modules may receive a different one of the data streams, and evaluate the respective stream to determine whether a portion of the stream contains an error. Each error detection sub-module may forward the portion of the respective received stream containing an error to the error correction module 215 (bypassing the error correction module 215 with the error-free portions). The error correction module 215 corrects the received portions of the respective received streams containing an error. As noted above, the error correction module 215 may include a number of sub-modules (each of which may be time-shared by a number of error detection sub-modules).

[0044] FIG. 3 is a block diagram illustrating an example of an architecture for a flash memory decoder system 300 more particularly illustrating error detection and correction sub-modules. The flash memory decoder system 300 may, for example, be the system 100 of FIG. 1. The flash memory decoder system 300 includes flash memory 110-a, a decoder module 205-a, an error detection module 210-a, an error correction module 215-a, a controller 120-a, and an encoder 105-a. Each of these components may be in communication with each other.

[0045] The flash memory 110-a includes a number of different sets of one or more active sectors 305. The decoder module 205-a includes a number of decoder sub-modules 310, and each decoder sub-module 310 may be associated with a different set of sectors 305. The error detection module 210-a includes a number of error detection sub-modules 315, and each decoder sub-module 310 may be associated with a different set of sectors 305. Thus, encoded data may be read from a set of one or more of sectors 305 (e.g., sector(s) 305-a) by a decoder sub-module 310 (e.g., decoder sub-module 310-a), and processed (e.g., buffered, de-interleaved, decoded to some extent, etc.) to generate a data stream. The data stream may be forwarded to an error detection sub-module 315 (error detection sub-module 315-a). Thus, encoded data from a set of one or more of sectors 305-a may be sent to an error detection sub-module 315-a. Different sets of sectors 305 may each send their respective data via different decoder sub-modules 310, as illustrated. In one embodiment, each error detection sub-module 315 is distinct from each other. In other embodiments, the decoder sub-module 310 and error detection sub-module 315 may be integrated to varying degrees.

[0046] Each error detection sub-module 315 may evaluate the respective stream to determine whether a portion of the stream contains an error. Each error detection sub-module 315 may forward the portion of the respective received stream containing an error to the error correction module 215-a (bypassing the error correction module 215 with the error-free portions). The error correction module 215-a includes a number of error correction sub-modules 320, each error correction sub-module 320 responsible for handling the errors from a number of error detection sub-modules 315 (e.g., error correction sub-module 320 may correct errors from error detection sub-modules 315-a, -b, and -c). Error correction sub-modules 320 may correct the received portions of the respective received streams containing an error. Each error correction sub-module 320 may receive portions of streams with errors, and these portion may have been detected in parallel.

[0047] Controller 120-a may perform a number of functions in the decoder process. Controller 120-a may dynamically modify the error detection sub-modules 315 and the error correction sub-modules 320 assigned to sectors 305 of flash memory 110-a. The controller 120-a may selectively power-up one or more of the error correction sub-modules 320 responsive to a monitored age or error rate associated with the flash memory 110-a. The controller 120-a may perform this monitoring on a per-sector basis, and the error correction sub-modules 320 may be powered-up to serve the sectors 305 where the error rates exceed a threshold. The controller 120-a may adapt the coding rate to be used by the encoder responsive to a monitored age or error rate associated with the flash memory 110-a. The controller 120-a may perform this monitoring on a per-sector basis, and the controller 120-a may adapt the coding rate on a per sector basis.

[0048] FIG. 4 is a block diagram of a flash memory decoder system 400 illustrating certain controller functionality according to various embodiments of the invention. The system 400 includes an encoder 105-b, flash memory 110-b, a decoder 115-b, and a controller 120-b. This system 400 may be an example of the system 100 of FIG. 1, and a component of this system 400 may have the same functionality as the counterpart component from FIG. 1. This flash memory system 400 may be a stand-alone device, or may be integrated (in whole or in part) with a computer, server, phone, mobile device, tablet, television, or any other computing device.

[0049] The controller 120-b includes an adaptive encoding rate controller 405, a power controller 410, a write controller 415, a read controller 420, an age monitoring module 425, and an error monitoring module 430. The age monitoring module 425 may monitor an age associated with the flash memory 110-b. This may be a time since manufacture, a time since first use, an amount of use, or any other metric which corresponds to the aging of the flash memory 110-b. This

monitoring may involve direct monitoring of the flash memory 110-b itself, or may be based on reports from the encoder 105-b, decoder 115-b, or other components of the system.

[0050] The error monitoring module 430 may monitor an amount of errors associated with the flash memory 110-b. This monitoring may measure errors over a variety of time periods and metrics, and may be translated into an error rate. The monitoring may be performed on a per-sector (or per set of sectors) basis. A number of sampling and averaging techniques may be used. This monitoring may involve direct monitoring of the decoder 115-b itself, or may be based on reports from the decoder 115-b or other components of the system.

[0051] The adaptive encoding rate controller 405 may receive information on the rate and/or amount of errors from the error monitoring module 430. The adaptive encoding rate controller 405 may modify a coding rate to be used by the encoder 105-b when the monitored rate and/or amount of errors exceeds a threshold. The monitoring of errors may be performed on a per-sector, per set of sectors, or other regional basis. Thus, the coding rate to be used by the encoder 105-b may be modified when the monitored rate of errors for the applicable region exceeds a threshold. In some embodiments, the coding rate may be adapted to be more, or less, robust; in other embodiments, the adaptation is only to make the coding rate more robust. The adaptive encoding rate controller 405 may receive information on the age of the flash memory 110-b from the age monitoring module 425. The adaptive encoding rate controller 405 may adapt the coding rate based on this monitoring (e.g., implementing a more robust coding rate for one or more sectors of the flash memory 110-b when the age exceeds a threshold). There may be a number of different coding rate change thresholds related both to age and error rate. Moreover, these threshold may be adaptive to the amount of flash memory 110-b that remains available (e.g., the margin may be increased when the flash memory is utilized below a threshold amount).

[0052] As noted above, an decoder module 115 may include a number of error correction sub-modules. The power controller 410 may receive information on the age of the flash memory 100-b from the age monitoring module 425. The power controller 410 may selectively power-up (or power-down) one or more of the error correction sub-modules responsive to an age of the flash memory 110-b. The power controller 410 may receive information on the rate and/or amount of errors from the error monitoring module 430. The power controller 410 may power-up (or power-down) one or more of the error correction sub-modules (e.g., when the monitored rate and/or amount of errors exceeds a threshold). The monitoring of errors may be performed on a per-sector, per set of sectors, or other regional basis. Thus, the power-up or power-down may be specific to a particular error correction sub-module for a given region of flash memory 110-b.

[0053] The write controller 415 may change the sectors of flash memory 110-b to be written to. These changes may be made in response to information from the age monitoring module 425 and error monitoring module 430. The read controller 420 may dynamically change the components of the decoder 115-b to be used to read different sectors of flash memory 110-b (e.g., in FIG. 3, the assignments of the decoder sub-modules 310, error detection sub-modules 315, and error correction sub-modules 320 may be changed in response to code rate modifications, increased errors, or age).

[0054] FIG. 5 is a flowchart illustrating a method 500 of decoding data from a flash memory according to various embodiments of the invention. The method 500 may, for example, be performed in whole or in part by the system 100, 300, or 400 of FIG. 1, 3, or 4 or, more specifically, by the decoder 115 of FIG. 1, 2, or 4.

[0055] At block 505, encoded data from a flash memory is received. At block 510, the received encoded data is processed to generate a number of data streams. The information for each data stream may be a wholly or partially decoded before being forwarded to respective error correction sub-modules. At block 515, at each of a number of error detection sub-modules operating in parallel, a different one of the data streams is processed. Each error detection sub-module is configured to: detect whether a portion of the respective received stream contains an error, and forward the portion of the respective received stream containing an error to an error correction module. At block 520, at the error correction module physically separate from the error detection sub-modules, the forwarded portions of the respective received streams containing an error are corrected.

[0056] FIG. 6 is a flowchart illustrating a method of age responsive decoding of data from a flash memory according to various embodiments of the invention. The method 600 may, for example, be performed in whole or in part by the system 100, 300, or 400 of FIG. 1, 3, or 4. The method 600 may be an example of the method 500 of FIG. 5.

[0057] At block 605, an age of a flash memory is monitored. At block 610, the coding rate for data to be encoded and stored in the flash memory is modified responsive to a first age threshold of the flash memory. At block 615, data is encoded at the modified rate, and the encoded data is stored on the flash memory. At block 620, one or more error correction sub-modules of an error correction module are powered-up from an inactive mode responsive to a second age threshold of the flash memory.

[0058] At block 625, the encoded data from the flash memory is processed to generate a number of partially decoded data streams. At block 630, at each of a number of error detection sub-modules operating in parallel, a different one of the data streams is processed. At block 635, a determination is made at each error detection sub-module whether a portion of the respective received stream contains an error. At block 640, error detection sub-modules forward those portions of the respective streams containing an error to the error correction module physically separate from the error detection sub-modules. At block 645, the error-free portions are forwarded to bypass the error correction module. At

block 650, the portions of the respective received streams containing an error are corrected with the powered-up error correction modules and additional error correction modules.

[0059] FIG. 7 is a flowchart illustrating a method of decoding data from a flash memory responsive to error rate according to various embodiments of the invention. The method 700 may, for example, be performed in whole or in part by the system 100, 300, or 400 of FIG. 1, 3, or 4. The method 700 may be an example of the method 500 of FIG. 5 or the method 600 of FIG. 6.

[0060] At block 705, a rate of errors from an error detection module is monitored for each of a number of sectors of the flash memory. At block 710, the coding rate for data to be encoded and stored in one or more sectors is modified responsive to the monitoring of first error rate threshold for the one or more sectors. At block 715, data is encoded at the modified rate and stored in the one or more sectors.

[0061] At block 720, an error correction sub-module assigned to the one or more sectors are powered-up from an inactive mode responsive to the monitoring of a second error rate threshold for the one or more sectors. At block 725, the encoded data from the one or more sectors is decoded to generate a decoded data stream. At block 730, at one of a number of error detection sub-modules operating in parallel, the decoded data stream is processed. At block 735, a determination is made by the error detection sub-module that a portion of the respective received stream contains an error. At block 740, the portion of the received stream containing an error is forwarded to the powered-up error correction sub-module. At block 745, the forwarded portion is corrected with the powered-up error correction sub-module.

[0062] It should be noted that the methods, systems, and devices discussed above are intended merely to be examples. It must be stressed that various embodiments may omit, substitute, or add various procedures or components as appropriate. For instance, it should be appreciated that, in alternative embodiments, the methods may be performed in an order different from that described, and that various steps may be added, omitted, or combined. Also, features described with respect to certain embodiments may be combined in various other embodiments. Different aspects and elements of the embodiments may be combined in a similar manner. Also, it should be emphasized that technology evolves and, thus, many of the elements are examples and should not be interpreted to limit the scope of the invention.

[0063] Specific details are given in the description to provide a thorough understanding of the embodiments. However, it will be understood by one of ordinary skill in the art that the embodiments may be practiced without these specific details. For example, well-known circuits, processes, algorithms, structures, and techniques have been shown without unnecessary detail in order to avoid obscuring the embodiments.

[0064] Also, it is noted that the embodiments may be described as a process which is depicted as a flow diagram or block diagram. Although each may describe the operations as a sequential process, many of the operations can be performed in parallel or concurrently. In addition, the order of the operations may be rearranged. A process may have additional steps not included in the figure.

[0065] Moreover, as disclosed herein, the term "memory" or "memory unit" may represent one or more devices for storing data, including read-only memory (ROM), random access memory (RAM), magnetic RAM, core memory, magnetic disk storage mediums, optical storage mediums, flash memory devices, or other computer-readable mediums for storing information. The term "computer-readable medium" includes, but is not limited to, portable or fixed storage devices, optical storage devices, wireless channels, a sim card, other smart cards, and various other mediums capable of storing, containing, or carrying instructions or data.

[0066] Furthermore, embodiments may be implemented by hardware, software, firmware, middleware, microcode, hardware description languages, or any combination thereof. When implemented in software, firmware, middleware, or microcode, the program code or code segments to perform the necessary tasks may be stored in a computer-readable medium such as a storage medium. Processors may perform the necessary tasks.

[0067] Having described several embodiments, it will be recognized by those of skill in the art that various modifications, alternative constructions, and equivalents may be used without departing from the spirit of the invention. For example, the above elements may merely be a component of a larger system, wherein other rules may take precedence over or otherwise modify the application of the invention. Also, a number of steps may be undertaken before, during, or after the above elements are considered. Accordingly, the above description should not be taken as limiting the scope of the invention.

Claims

1. A method comprising:

receiving encoded data from a flash memory comprising a plurality of data streams;
processing, at each of a plurality of error detection sub-modules operating in parallel, a different one of the plurality of data streams, wherein each error detection sub-module is configured to:

detect whether a portion of the respective received stream contains an error; and
forward the portion of the respective received stream containing an error to an error correction module; and

correcting, with the error correction module physically separate from an error detection module, the forwarded
portions of the respective received streams containing an error.

2. The method of claim 1, further comprising:

dynamically modifying the error detection sub-modules assigned to receive data from respective sectors of flash
memory.

3. The method of claim 1 or 2, wherein the error correction module comprises a plurality of error correction sub-modules
operating in parallel and fewer in number than the error detection sub-modules.

4. The method of claim 3, further comprising:

powering-up, from an inactive mode, one or more of the error correction sub-modules responsive to an age of
the flash memory.

5. The method of claim 3, further comprising:

monitoring a rate of errors from the error detection module; and
powering-up one or more of the error correction sub-modules when the monitored rate of errors exceeds a
threshold.

6. The method of claim 3, further comprising:

monitoring a rate of errors from the error detection module for each of a plurality of sectors of the flash memory;
and
powering-up an error correction sub-module for assignment to a set of one or more of the monitored sectors
when the monitored rate of errors for the set exceeds a threshold.

7. The method of any one or more of the preceding claims, further comprising:

modifying a coding rate for data to be stored as the encoded data on the flash memory responsive to an age
of the flash memory.

8. The method of any one or more of the preceding claims, further comprising:

monitoring a rate of errors from the error detection module; and
modifying a coding rate for data to be stored as the encoded data on the flash memory when the monitored
rate of errors exceeds a threshold.

9. The method of any one or more of the preceding claims, further comprising:

monitoring a rate of errors from the error detection module for each of a plurality of sectors of the flash memory;
and
modifying a coding rate for data to be stored as the encoded data on the flash memory when the monitored
rate of errors for the set exceeds a threshold.

10. A flash memory decoder comprising:

a decoding module configured to:

receive encoded data from the flash memory; and
decode the received encoded data to generate a plurality of partially decoded data streams;

an error detection module communicatively coupled with the decoding module, and comprising a plurality of

error detection sub-modules operating in parallel, each error detection sub-module configured to:

receive a different one of the plurality of partially decoded data streams;
 detect whether a portion of the respective received stream contains an error; and
 forward the portion of the respective received stream containing an error to an error correction module; and

an error correction module, communicatively coupled with and physically separate from the error detection module, and configured to correct the received portions of the respective received streams containing an error.

11. The flash memory decoder of claim 10, further comprising a power controller configured to selectively power-up one or more of the error correction sub-modules responsive to an age of or read error rate from the flash memory.

12. The flash memory decoder of claim 10 or 11, further comprising:

an error monitoring module, communicatively coupled with the error detection module, and configured to monitor a rate of errors from the error detection module; and
 an adaptive encoding rate controller configured to modify a coding rate for a flash memory encoding module when the monitored rate of errors exceeds a threshold.

13. The flash memory decoder of claim 10, 11 or 12, further comprising:

the flash memory, communicatively coupled with the decoding module;
 an encoder, communicatively coupled with the flash memory, and configured to encode data at a coding rate for storage as the encoded data on the flash memory; and
 an adaptive encoding rate controller configured to modify the coding rate responsive to an age of the flash memory, wherein
 each of the error detection sub-modules is configured to read data from a set of one or sectors of flash memory different from other of the error detection sub-modules;
 the error correction module comprises a plurality of error correction sub-modules operating in parallel and fewer in number than the error detection sub-modules;
 each error detection sub-module is configured to direct error-free portions of the respective received streams to bypass the error correction module;
 the error detection module comprises the decoding module; and
 the encoded data is encoded with a Hamming code, a BCH code, a Turbo code, or a low-density parity check code.

14. A system comprising:

an encoder configured to encode data for storage on a flash memory;
 the flash memory, communicatively coupled with the encoding module, and configured to store the encoded data; and
 a decoder, communicatively coupled with the flash memory, and configured to:

retrieve the encoded data from flash memory to generate a plurality of data streams; and
 process, at each of a plurality of error detection sub-modules of the decoder operating in parallel, a different one of the plurality of data streams, wherein each error detection sub-module is configured to:

detect whether a portion of the respective received stream contains an error; and
 forward the portion of the respective received stream containing an error to an error correction module of the decoder; and
 correct, with the error correction module physically separate from the error detection module, the forwarded portions of the respective received streams containing an error.

15. The system of claim 14, wherein the encoder is further configured to adaptively modify the coding rate responsive to an age of the flash memory or a rate of errors associated with the decoded data.

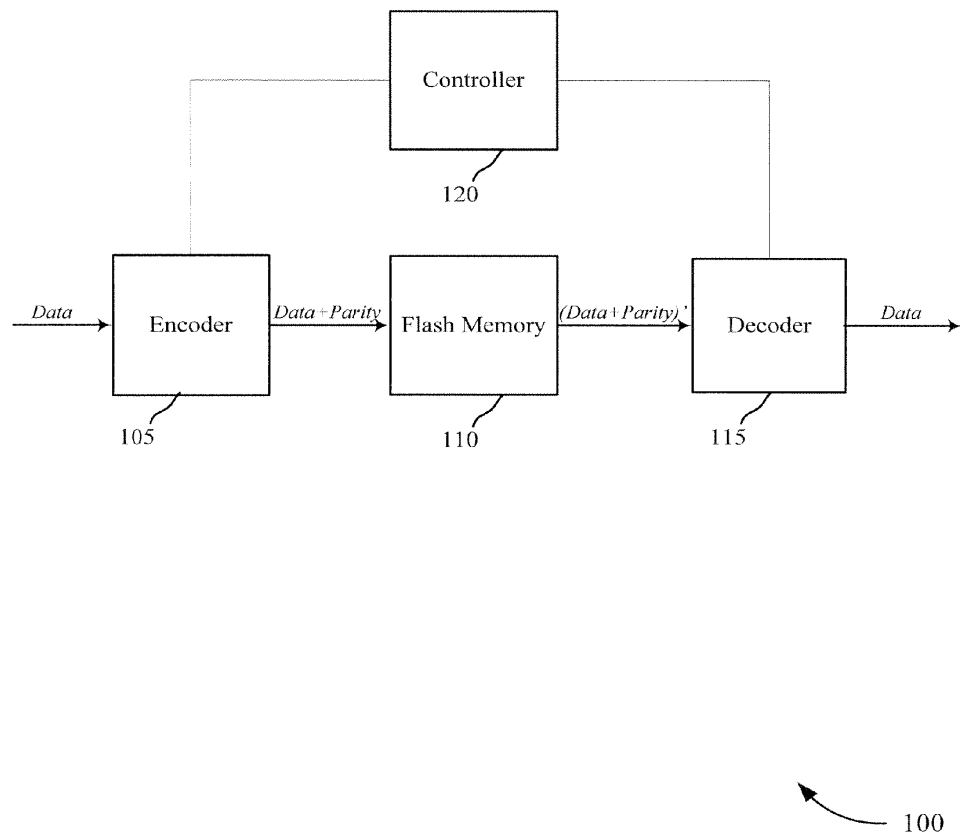


FIG. 1

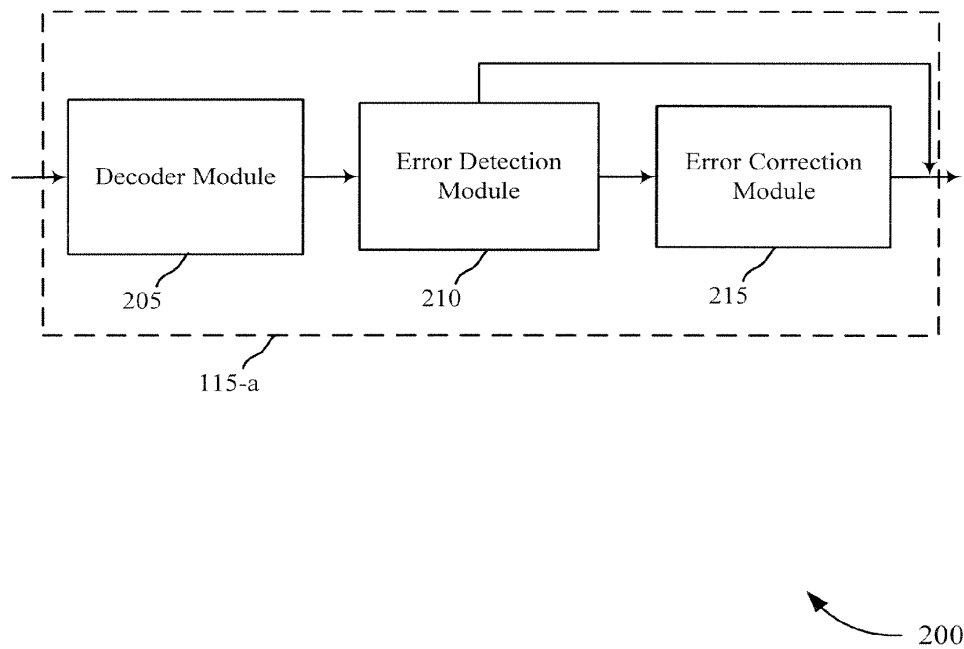


FIG. 2

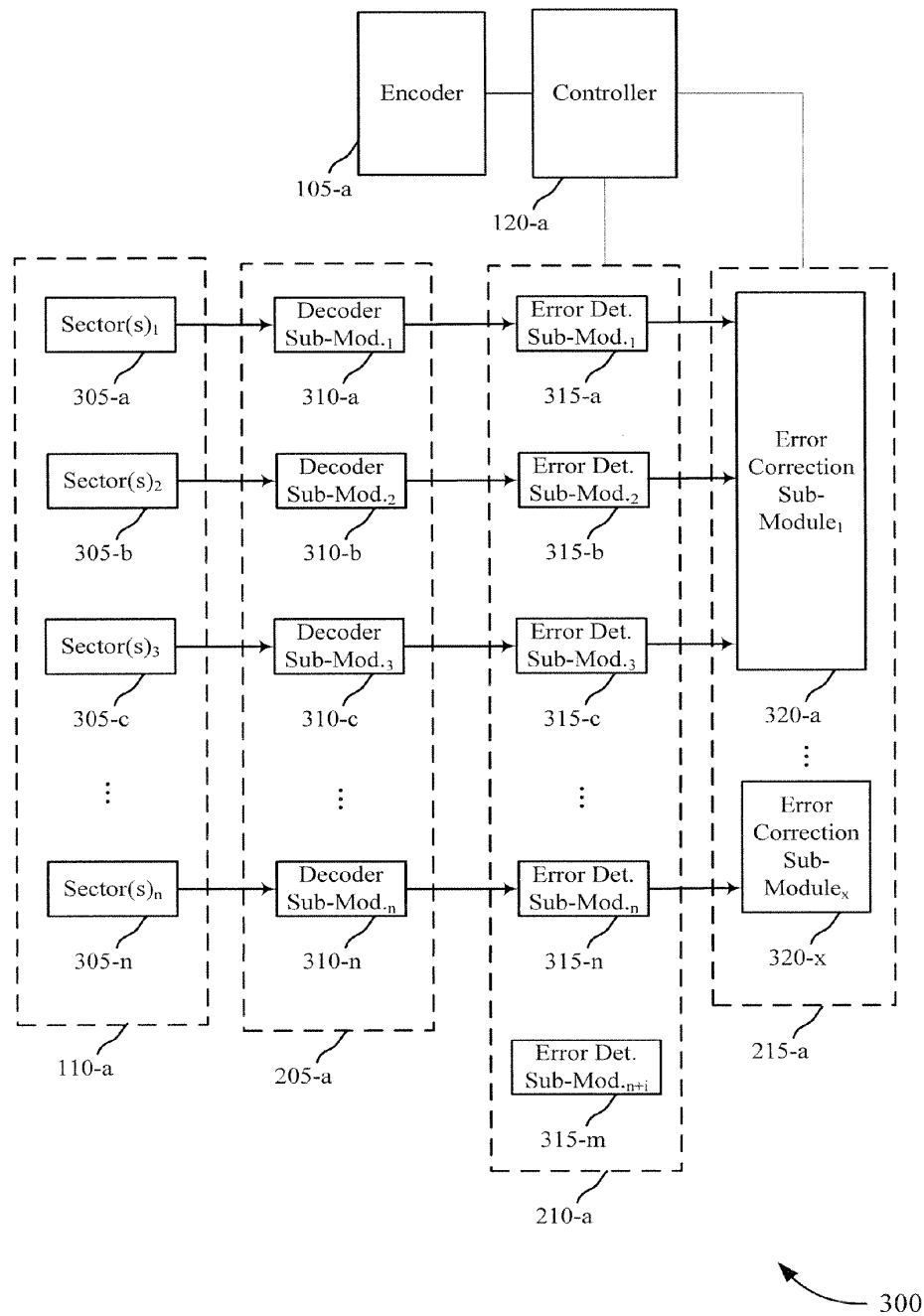
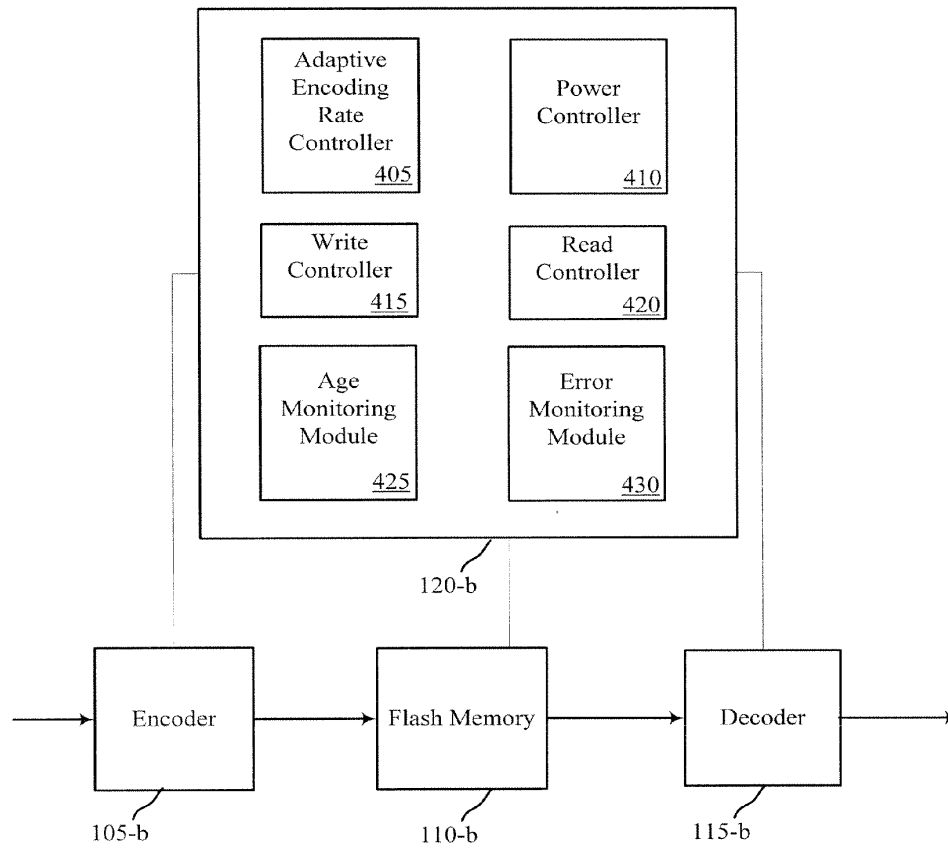


FIG. 3



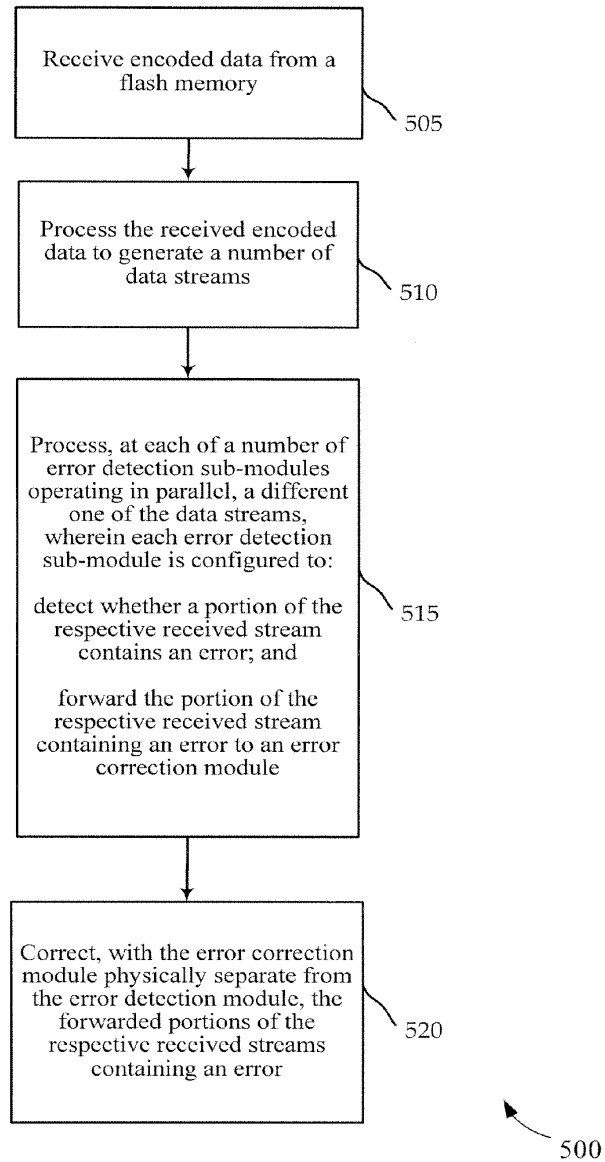
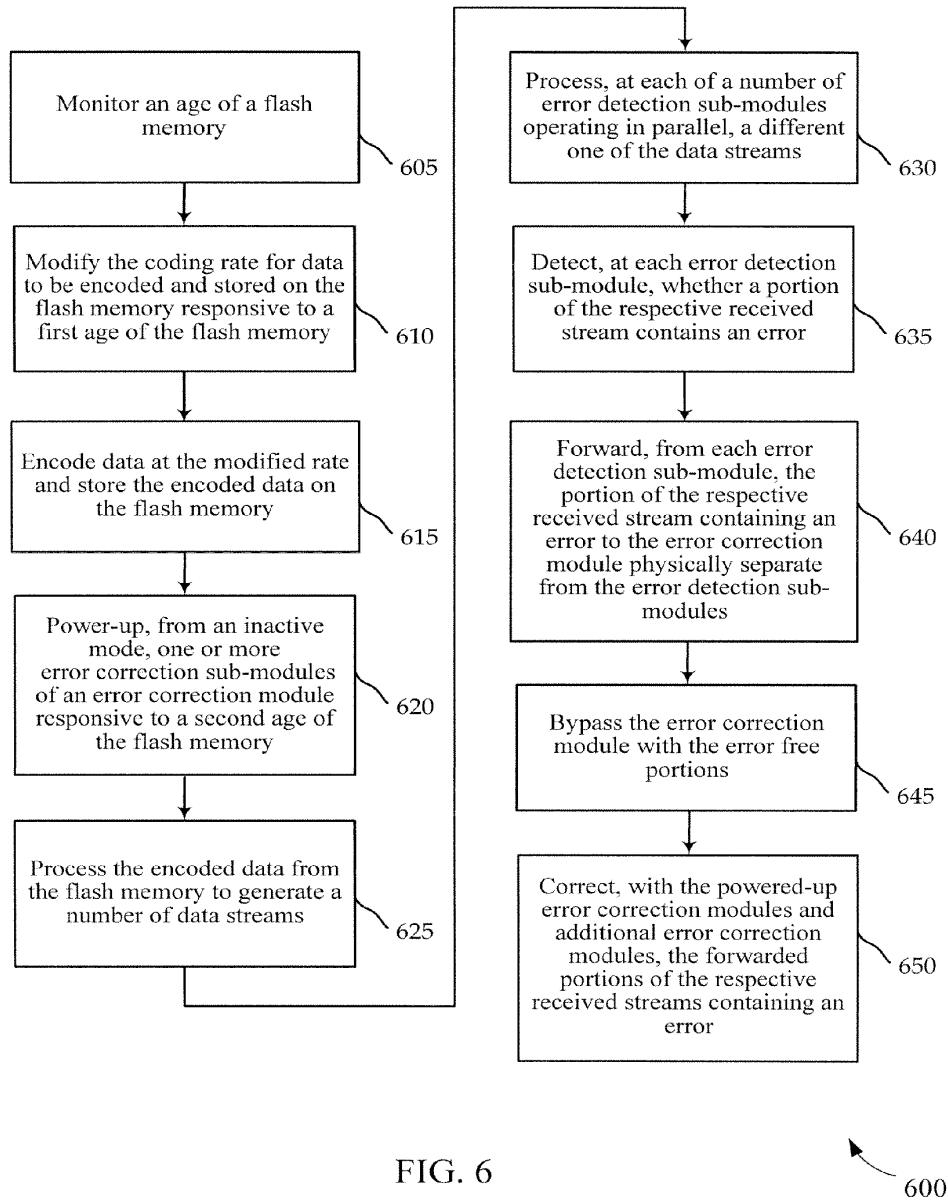


FIG. 5



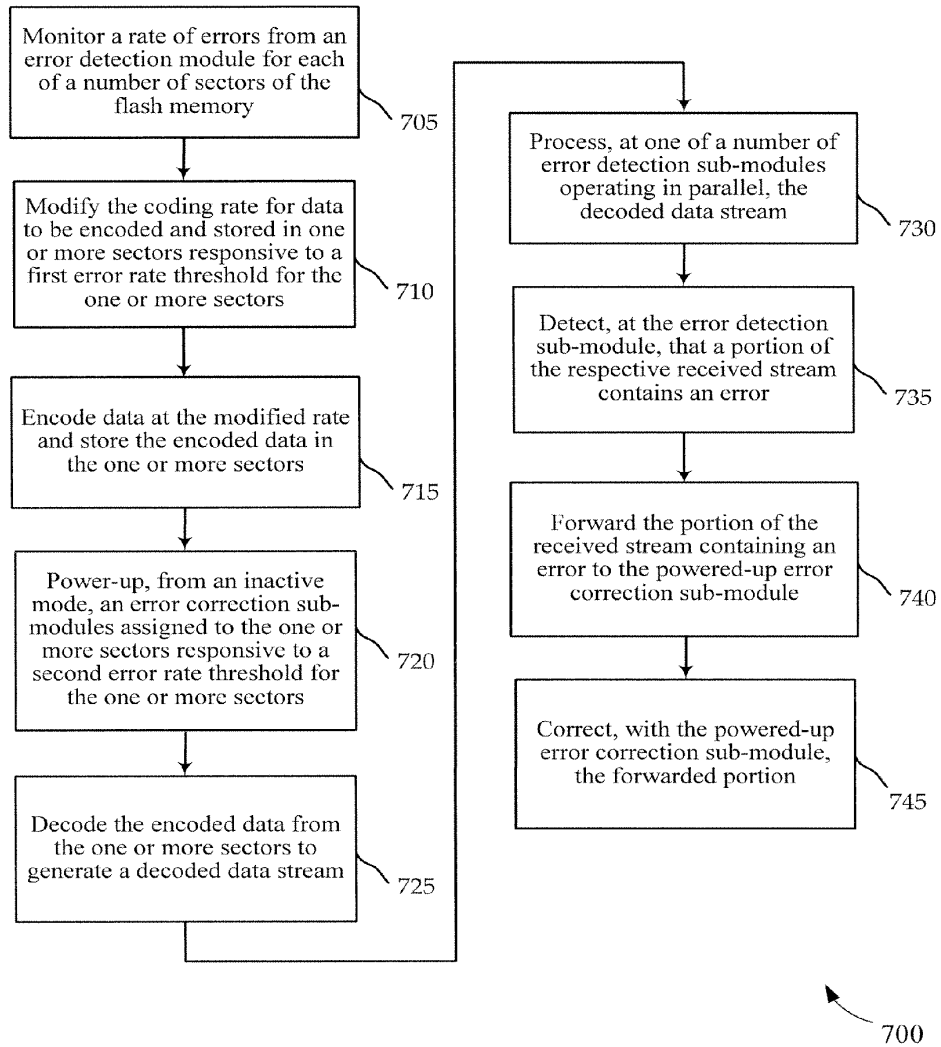


FIG. 7

REFERENCES CITED IN THE DESCRIPTION

This list of references cited by the applicant is for the reader's convenience only. It does not form part of the European patent document. Even though great care has been taken in compiling the references, errors or omissions cannot be excluded and the EPO disclaims all liability in this regard.

Patent documents cited in the description

- US 61234911 A [0001]

I hereby certify that this correspondence is being filed via
EFS-Web with the United States Patent and Trademark Office
on 1/26/2012.

PATENT
Attorney Docket No.: 90523-789306 (003710US)
Client Ref. No.: ECC-0407-US-2

KILPATRICK TOWNSEND & STOCKTON LLP

By: /Thao Pham/
Thao Pham

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

DAVE, Sameep et al.

Application No.: 12/858,510

Filed: August 18, 2010

For: FORWARD ERROR
CORRECTION FOR MEMORIES

Customer No.: 20350

Confirmation No.: 6028

Examiner: Jeffrey A. Gaffin

Art Unit: 2117

SUPPLEMENTAL INFORMATION
DISCLOSURE STATEMENT UNDER
37 CFR §1.97 and §1.98

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Commissioner:

The references cited on attached form PTO/SB/08A and PTO/SB/08B are being called to the attention of the Examiner. Copies of the reference Nos. 5-8 [in compliance with the requirements of 37 CFR §1.98(a)(2)] are enclosed. It is respectfully requested that the cited references be expressly considered during the prosecution of this application, and the references be made of record therein and appear among the "references cited" on any patent to issue therefrom.

Reference Nos. 1-5, and 7 were cited in an European Search Report from related European Application No. EP 2299362, a copy of which is enclosed as reference No. 8.

As provided for by 37 CFR §1.97(g) and (h), no inference should be made that the information and references cited are prior art merely because they are in this statement and no representation is being made that a search has been conducted or that this statement encompasses all the possible relevant information.

Applicant believes that no fee is required for submission of this statement. However, if a fee is required, the Commissioner is authorized to deduct such fee from the undersigned's Deposit Account No. 20-1430. Please deduct any additional fees from, or credit any overpayment to, the above-noted Deposit Account.

Respectfully submitted,

/Mymy N. Henderson/

Mymy N. Henderson
Reg. No. 64,975

KILPATRICK TOWNSEND & STOCKTON LLP
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MNH:t4t
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/858,510	08/18/2010	Sameep Dave	90523-789306 (003710US)	6028
61668 7590 01/31/2013 KILPATRICK TOWNSEND & STOCKTON, LLP/VIASAT VIASAT, INC. (CLIENT #017018) TWO EMBARCADERO CENTER 8TH FLOOR SAN FRANCISCO, CA 94111			EXAMINER MEHRMANESH, ELMIRA	
			ART UNIT 2113	PAPER NUMBER
			NOTIFICATION DATE 01/31/2013	DELIVERY MODE ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

Patent-admin@viasat.com
ipefiling@kilpatricktownsend.com

Office Action Summary	Application No.	Applicant(s)	
	12/858,510	DAVE ET AL.	
	Examiner	Art Unit	
	Elmira Mehrmanesh	2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on 18 August 2010.

2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.

3) ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on ____; the restriction requirement and election have been incorporated into this action.

4) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

5) ☒ Claim(s) 1-25 is/are pending in the application.

5a) Of the above claim(s) ____ is/are withdrawn from consideration.

6) ☐ Claim(s) ____ is/are allowed.

7) ☒ Claim(s) 1,2,13-15 and 17 is/are rejected.

8) ☒ Claim(s) 3-12,16 and 18-25 is/are objected to.

9) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10) ☒ The specification is objected to by the Examiner.

11) ☒ The drawing(s) filed on 18 August 2010 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) ☐ All b) ☐ Some * c) ☐ None of:

1. ☐ Certified copies of the priority documents have been received.

2. ☐ Certified copies of the priority documents have been received in Application No. ____.

3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☒ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date 9/2/10, 1/26/12

3) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. ____.

4) ☐ Other: ____.

DETAILED ACTION

The application of Dave et al., for a "Forward error correction for memories" filed on August 18, 2010 has been examined. The information disclosure statement (IDS) submitted on September 2, 2010 and January 26, 2012 have been considered.

Claims 1-25 are presented for examination.

Claims 1, 2, 13-15, and 17 are rejected under 35 USC § 102.

Claims 3-12, 16, and 18-25 are objected to.

Specification

The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 2, 13-15, and 17 are rejected under 35 U.S.C. 102(b) as being anticipated by Suzuki et al. (U.S. PGPUB 20050138521).

As per claim 1, Suzuki discloses a flash memory decoder comprising:

a decoding module configured to:

receive encoded data from the flash memory ([0121]); and

decode the received encoded data to generate a plurality of partially decoded data streams ([0122], [0123]);

an error detection module communicatively coupled with the decoding module, and comprising a plurality of error detection sub-modules operating in parallel, each error detection sub-module configured to:

receive a different one of the plurality of partially decoded data streams ([0123]);

detect whether a portion of the respective received stream contains an error ([0022]); and

forward the portion of the respective received stream containing an error to an error correction module; and an error correction module, communicatively coupled with and physically separate from the error detection module, and configured to correct the received portions of the respective received streams containing an error ([0142]).

As per claim 2, Suzuki discloses each of the error detection sub-modules is configured to read data from a set of one or sectors of flash memory different from other of the error detection sub-modules ([0107], [0123]).

As per claim 13, Suzuki discloses each error detection sub-module is configured to direct error-free portions of the respective received streams to bypass the error correction module ([0142]).

As per claim 14, Suzuki discloses the error detection module comprises the decoding module; and the encoded data is encoded with a Hamming code, a BCH code, a Turbo code, or a low-density parity check code ([0124]).

As per claim 15, Suzuki discloses a system comprising:

an encoder configured to encode data for storage on a flash memory ([0121]); the flash memory, communicatively coupled with the encoding module, and configured to store the encoded data; and

a decoder ([0122]), communicatively coupled with the flash memory ([0107]), and configured to:

retrieve the encoded data from flash memory to generate a plurality of data streams ([0123]); and process, at each of a plurality of error detection sub-modules of the decoder operating in parallel, a different one of the plurality of data streams ([0122], [0123]), wherein each error detection sub-module is configured to:

detect whether a portion of the respective received stream contains an error ([0022]); and

forward the portion of the respective received stream containing an error to an error correction module of the decoder; and correct, with the error correction module physically separate from the error detection module, the forwarded portions of the respective received streams containing an error ([0142]).

As per claim 17, Suzuki discloses a method comprising:

receiving encoded data from a flash memory comprising a plurality of data streams ([0121]); processing, at each of a plurality of error detection sub-modules operating in parallel, a different one of the plurality of data streams ([0122], [0123]), wherein each error detection sub-module is configured to:

detect whether a portion of the respective received stream contains an error ([0022]); and

forward the portion of the respective received stream containing an error to an error correction module; and correcting, with the error correction module physically separate from an error detection module, the forwarded portions of the respective received streams containing an error ([0142]).

Allowable Subject Matter

Claims 3-12, 16, and 18-25 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Related Prior Art

The following prior art is considered to be pertinent to applicant's invention, but not relied upon for claim analysis conducted above:

Litsyn et al. (U.S. PGPUB 20070208905) discloses multi-bit-per-cell flash memory device with non-bijective mapping and multiple ECC decoders ([0158]).

Okazaki et al. (U.S. Patent No. 7941731) discloses a decoder which generates a plurality of decoded data based on 1) input data and 2) a plurality of pairs of control data and redundant data, in each the pair, the control data defining a selected encoding

Art Unit: 2113

process and the redundant data being generated by the selected encoding process based on the control data and the input data (Abstract).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Elmira Mehrmanesh whose telephone number is (571)272-5531. The examiner can normally be reached on 10-6 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Scott Baderman can be reached on (571) 272- 3644. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/E. M./

Examiner, Art Unit 2113

/Scott T Baderman/

Supervisory Patent Examiner, Art Unit 2114

Application/Control Number: 12/858,510
Art Unit: 2113

Page 7

Notice of References Cited	Application/Control No. 12/858,510		Applicant(s)/Patent Under Reexamination DAVE ET AL.	
	Examiner Elmira Mehrmanesh		Art Unit 2113	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-2005/0138521 A1	06-2005	Suzuki et al.	714/755
*	B	US-7,257,764 B2	08-2007	Suzuki et al.	714/774
*	C	US-2007/0208905 A1	09-2007	Litsyn et al.	711/103
*	D	US-7,941,731 B2	05-2011	Okazaki et al.	714/774
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Index of Claims 	Application/Control No. 12858510	Applicant(s)/Patent Under Reexamination DAVE ET AL.
	Examiner Elmira Mehrmanesh	Art Unit 2113

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant			☐ CPA			☐ T.D.			☐ R.1.47		
CLAIM		DATE									
Final	Original	01/27/2013									
	1	✓									
	2	✓									
	3	○									
	4	○									
	5	○									
	6	○									
	7	○									
	8	○									
	9	○									
	10	○									
	11	○									
	12	○									
	13	✓									
	14	✓									
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	23	○									
	24	○									
	25	○									

Search Notes 	Application/Control No. 12858510	Applicant(s)/Patent Under Reexamination DAVE ET AL.
	Examiner Elmira Mehrmanesh	Art Unit 2113

CPC- SEARCHED		
Symbol	Date	Examiner

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner
714	758,773,774	1/27/2013	EM

SEARCH NOTES		
Search Notes	Date	Examiner
EAST search, please see the attached history.	1/27/2013	EM
Inventor name search.	1/27/2013	EM

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner

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Substitute for form 1449/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(Use as many sheets as necessary)</i>				Complete if Known	
				Application Number	12/858,510
				Filing Date	August 18, 2010
				First Named Inventor	Dave, Sameep
				Art Unit	12858510 - GAU: 2113
				Examiner Name	/Elmira Mehrmanesh/
Sheet	1	of	3	Attorney Docket Number	026258-003710US

U.S. PATENT DOCUMENTS					
Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number Kind Code ² (if known)			
	AA	US-7,203,874	04-10-2007	Roohparvar	
	AB	US-7,296,213	11-13-2007	Vainsencher et al.	
	AC	US-7,394,689	07-01-2008	Ryu	
	AD	US-7,356,755	04-08-2008	Fackenthal	
	AE	US-6,751,766	06-15-2004	Guterman et al.	
	AF	US-2007/0204206	08-30-2007	Lee et al.	
	AG	US-2004/0083334	04-29-2004	Chang et al.	
	AH	US-2008/0244362	10-02-2008	Liu et al.	
	AI	US-2008/0072120	03-20-2008	Radke	
	AJ	US-2007/0266295	11-15-2007	Conley	
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	AL	US-2008/0163028	07-03-2008	Mokhlesi	
	AM	US-2007/0283428	12-06-2007	Ma et al.	
	AN	US-7,231,585	06-12-2007	Vainsencher et al.	
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	AQ	US-2003/0041299	02-27-2003	Kanazawa et al.	
	AR	US-2008/0270680	10-30-2008	Chang	
	AS	US-2007/0271494	11-22-2007	Gorobets	
	AT	US-2008/0130341	06-05-2008	Shalvi et al.	
	AU	US-2008/0184094	07-31-2008	Murray et al.	
	AV	US-2007/0266296	11-15-2007	Conley	
	AW	US-2006/0059406	03-16-2006	Michelsoni et al.	
	AX	US-7,360,136	04-15-2008	Guterman et al.	
	AY	US-2007/0223277	09-27-2007	Tanaka et al.	
	AZ	US-7,304,893	12-04-2007	Hemink	
	BA	US-2008/0212371	09-04-2008	Roohparvar	
	BB	US-6,684,353	01-27-2004	Parker et al.	
	BC	US-2007/0171730	07-26-2007	Ramamoorthy et al.	
	BD	US-2008/0282128	11-13-2008	Lee et al.	
	BE	US-7,305,596	12-04-2007	Noda et al.	
	BF	US-2008/0109703	05-08-2008	Brandman	
	BG	US-2008/0168320	07-10-2008	Cassuto et al.	
	BH	US-2008/0276150	11-06-2008	Kong et al.	
	BI	US-2008/0301526	12-04-2008	Kohler et al.	
Examiner Signature	/Elmira Mehrmanesh/			Date Considered	12/13/2012

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. ¹ Applicant's unique citation designation number (optional). ² See Kind Codes of U.S. Patent Documents at www.uspto.gov or MPEP 901.04. ³ Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). ⁴ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁵ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. ⁶ Applicant is to place a check mark here if English language Translation is attached.

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ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /E.M./

Kioxia Exhibit 1002

Substitute for form 1449/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(Use as many sheets as necessary)</i>				Complete if Known	
				Application Number	12/858,510
				Filing Date	August 18, 2010
				First Named Inventor	Dave, Sameep
				Art Unit	12858510 - GAU: 2113
				Examiner Name	/Elmira Mehrmanesh/
Sheet	2	of	3	Attorney Docket Number	026258-003710US

U.S. PATENT DOCUMENTS					
Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number Kind Code ² (if known)			
	BJ	US-2008/0313493	12-18-2008	Roohparvar et al.	
	BK	US-2009/0013234	01-08-2009	Radke	

FOREIGN PATENT DOCUMENTS								
Examiner Initials*	Cite No. ¹	Foreign Patent Document			Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ⁶
		Country Code ³	Number ⁴	Kind Code ⁵ (if known)				
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								☐
								☐

Examiner Signature	/Elmira Mehrmanesh/	Date Considered	12/13/2012
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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. ¹ Applicant's unique citation designation number (optional). ² See Kind Codes of U.S. Patent Documents at www.uspto.gov or MPEP 901.04. ³ Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). ⁴ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁵ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. ⁶ Applicant is to place a check mark here if English language Translation is attached.

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Kioxia Exhibit 1002

Page 155

Substitute for form 1449/PTO				Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(Use as many sheets as necessary)</i>				Application Number	12/858,510
				Filing Date	August 18, 2010
				First Named Inventor	Dave, Sameep
				Art Unit	12858510 - GAU: 2113
				Examiner Name	/Elmira Mehrmanesh/
Sheet	3	of	3	Attorney Docket Number	026258-003710US

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials *	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
	BA	STMicroelectronics, "Error Correction Code in NAND Flash Memories", http://www.eetasia.com/ARTICLES/2004NOV29MEM_AN10.PDF?SOURCES=DOWNLOAD , May 11, 2004.	☐
	BB	Numonyx, "Error Correction Code in Single Level Cell NAND Flash Memories", http://www.numonyx.com/Documents/Application%20Notes/AN1823.pdf , May 26, 2008.	☐
	BC	Micron Technology, Inc., "ECC Module for Xilinx Spartan-3", http://download.micron.com/pdf/technotes/nand/tn2905.pdf , May 1, 2007.	☐
	BD	Micron Technology, Inc., "Hamming Codes for NAND Flash Memory Devices", http://download.micron.com/pdf/technotes/nand/tn2908.pdf , May 1, 2007.	☐
	BE	Sun et al., "Multilevel Flash Memory On-Chip Error Correction Based on Trellis Coded Modulation", http://www.ecse.rpi.edu/homepages/tzhang/pub/FLASHISCAS06.pdf .	☐
	BF	Micron Technology, Inc., "NAND Flash Design and Use Considerations", http://download.micron.com/pdf/technotes/nand/tn2917.pdf , August 1, 2006.	☐
	BG	Micron Technology, Inc., "Using COPYBACK Operations in NAND Flash Devices," http://download.micron.com/pdf/technotes/nand/tn2941_idm_copyback.pdf , October 1, 2008.	☐
	BH	Micron Technology, Inc., "NAND Flash Internal Data Move", http://download.micron.com/pdf/technotes/nand/tn2915.pdf , June 1, 2007.	☐
	BI	Micron Technology, Inc., "Wear-Leveling Techniques in NAND Flash Devices", http://download.micron.com/pdf/technotes/nand/tn2942_nand_wear_leveling.pdf , October 1, 2008.	☐
	BJ	Chen, et al., "Error Correction for Multi-Level NAND Flash Memory Using Reed-Solomon Codes", http://www.csie.ntu.edu.tw/~f95070/Flash%20Paper%20Collection/ERROR%20CORRECTION%20FOR%20MULTI-LEVEL%20NAND%20FLASH%20MEMORY%20USING%20REED-SOLOMON%20CODES.pdf , November 26, 2008.	

Examiner Signature	/Elmira Mehrmanesh/	Date Considered	12/13/2012
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¹ Applicant's unique citation designation number (optional). ² Applicant is to place a check mark here if English language Translation is attached.

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BIB DATA SHEET

CONFIRMATION NO. 6028

SERIAL NUMBER	FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.		
12/858,510	08/18/2010	714	2113	90523-789306 (003710US)		
APPLICANTS Sameep Dave, Stow, OH; Russell Fuerst, Mentor, OH; Mark Kohoot, Cleveland Heights, OH; Jim Keszenheimer, Chagrin Falls, OH; William H. Thesling, Hudson, OH; ** CONTINUING DATA ***** This appln claims benefit of 61/234,911 08/18/2009 ** FOREIGN APPLICATIONS ***** ** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ** 08/27/2010						
Foreign Priority claimed ☐ Yes ☒ No 35 USC 119(a-d) conditions met ☐ Yes ☒ No Verified and /ELMIRA MEHRMANESH/ Examiner's Signature Acknowledged		☐ Met after Allowance Initials	STATE OR COUNTRY OH	SHEETS DRAWINGS 7	TOTAL CLAIMS 25	INDEPENDENT CLAIMS 3
ADDRESS KILPATRICK TOWNSEND & STOCKTON, LLP/VIASAT VIASAT, INC. (CLIENT #017018) TWO EMBARCADERO CENTER 8TH FLOOR SAN FRANCISCO, CA 94111 UNITED STATES						
TITLE FORWARD ERROR CORRECTION FOR MEMORIES						
FILING FEE RECEIVED 1480	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:			☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit		

12858510 - GAU: 2113

Substitute for form 1449/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(Use as many sheets as necessary)</i>				Complete if Known	
				Application Number	12/858,510
				Filing Date	August 18, 2010
				First Named Inventor	Dave, Sameep
				Art Unit	~~2447~~
				Examiner Name	esh/
Sheet	1	of	1	Attorney Docket Number	90523-789306 (003710US)

U.S. PATENT DOCUMENTS					
Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number Kind Code ² (if known)			
	1	US-2003-037299 A1	02-20-2003	Smith, Kenneth Kay	
	2	US-2004-243906 A1	12-2-2004	Huang, Che-Chi	
	3	US-2005-172179 A1	08-04-2005	Brandenberger, Sarah H.	
	4	US-2008-052564 A1	02-28-2008	Yim, Yong-Tae	

FOREIGN PATENT DOCUMENTS								
Examiner Initials*	Cite No. ¹	Foreign Patent Document			Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ⁶
		Country Code ³	Number ⁴	Kind Code ⁵ (if known)				
	5	EP	1 612 950	A1	01-04-2006	St. Microelectronics SRL		☐
	6	EP	2 299 362	A2	05-04-2001	ViaSat, Inc.		☐
	7	WO	2006/013529	A1	02-09-2006	Koninkl Philipps Electronics NV		☐

NON PATENT LITERATURE DOCUMENTS				
Examiner Initials *	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ⁶	
	8	European Search Report and Search Opinion of April 5, 2011 for European Application No. EP 2299362.	☐	

Examiner Signature	/Elmira Mehrmanesh/	Date Considered	12/13/2012
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EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	3764	(714/758,773,774).CQLS.	US-PGPUB; USPAT; USOCR	OR	OFF	2013/01/27 21:05
L2	1346	(part\$3 partial\$4) near decod\$3 with errors	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/01/27 21:25
L3	47	1 and 2	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/01/27 21:25
L4	699	decod\$3 near5 (paths channels streams signals words) with (errors near5 (detect\$4 correct\$4) ECC CRC parit\$3 FEC) with (parallel concurrent\$3 simultaneous\$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/01/27 21:45
L5	82	((WILLIAM) near2 (THESLING)).INV.	US-PGPUB; USPAT	OR	ON	2013/01/27 21:46
L6	41	("20070283428" "20080148132" "20080163028" "20080244362" "20080301526" "7231585" "7305596" "7394689" "20040243906" "20050172179" "20030041299" "20080244370" "7304893" "20080282128" "6751766" "20070171730" "20070266296" "20080212371" "20080276150" "7203874" "20080072120" "20090013234" "20070204206" "20070223277" "20080109703" "20080130341" "20080270680" "6684353" "20080052564" "20060059406" "20070271494" "20080168320" "7296213" "7356755" "7360136" "20030037299" "20040083334" "20070266295" "20080184094" "20080313493" "7333364").PN.	US-PGPUB; USPAT	OR	ON	2013/01/27 21:46
L7	61	4 and (1 L5 L6)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO;	OR	ON	2013/01/27 21:46

			DERWENT; IBM_TDB			
L8	1	4 and 6	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/01/27 21:47
L9	11	4 same flash near5 memor\$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/01/27 21:48
L10	22	6 and decod\$3 with (errors near5 (detect\$4 correct\$4) ECC CRC parit\$3 FEC)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/01/27 21:54
L14	22	6 and decod\$3 same (errors near5 (detect\$4 correct\$4) ECC CRC parit\$3 FEC)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/01/27 22:24
L15	14	decod\$3 near5 (multiple pluralit\$3 various) near5 streams same errors near5 correct\$5 same detect\$5	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/01/27 22:26
S1	11	((SAMEEP) near2 (DAVE)).INV.	US-PGPUB; USPAT	OR	ON	2013/01/27 19:09
S2	8	((RUSSELL) near2 (FUERST)).INV.	US-PGPUB; USPAT	OR	ON	2013/01/27 19:09
S3	1	((MARK) near2 (KOHOT)).INV.	US-PGPUB; USPAT	OR	ON	2013/01/27 19:09
S4	1	((JIM) near2 (KESZENHEIMER)).INV.	US-PGPUB; USPAT	OR	ON	2013/01/27 19:10
S5	82	((WILLIAM) near2 (THESLING)).INV.	US-PGPUB; USPAT	OR	ON	2013/01/27 19:10
S6	41	("20070283428" "20080148132" "20080163028" "20080244362" "20080301526" "7231585" "7305596" "7394689" "20040243906" "20050172179" "20030041299" "20080244370" "7304893" "20080282128" "6751766" "20070171730" "20070266296" "20080212371" "20080276150" "7203874" "20080072120" "20090013234" "20070204206" "20070223277" "20080109703" "20080130341" "20080270680"	US-PGPUB; USPAT	OR	ON	2013/01/27 19:19

		"6684353" "20080052564" "20060059406" "20070271494" "20080168320" "7296213" "7356755" "7360136" "20030037299" "20040083334" "20070266295" "20080184094" "20080313493" "7333364").PN.				
S7	3456	(part\$3 partial\$4) near5 decod\$3 with errors	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/01/27 19:35
S8	1346	(part\$3 partial\$4) near decod\$3 with errors	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/01/27 19:36
S9	1	(S1 S2 S5 S6) and S8	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/01/27 19:36
S10	0	("2011/0047442").URPN.	USPAT	OR	ON	2013/01/27 19:36
S11	31	(part\$3 partial\$4) near decod\$3 with (errors near5 (detect\$4 correct\$4) EOC CRC parit\$3 FEC) with (parallel concurrent\$3 simultaneous\$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/01/27 19:40
S12	3	(S1 S2 S5 S6) and S7	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/01/27 19:58

1/ 27/ 2013 10:47:18 PM

C:\Users\emehrmanesh\Documents\EAST\Workspaces\12858510.wsp

I hereby certify that this correspondence is being filed via
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on April 29, 2013.

PATENT
Attorney Docket No.: 90523-789306 (003710US)
Client Ref. No.: ECC-0407-US-2

KILPATRICK TOWNSEND & STOCKTON LLP

By: /Mymy N. Henderson/
Mymy N. Henderson

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Sameep Dave et al.

Application No.: 12/858,510

Filed: August 18, 2010

For: FORWARD ERROR CORRECTION
FOR MEMORIES

Customer No.: 61668

Confirmation No.: 6028

Examiner: Elmira Mehrmanesh

Technology Center/Art Unit: 2113

AMENDMENT

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Commissioner:

In response to the Office Action mailed January 31, 2013, please enter the
following amendments and remarks:

Amendments to the Specification begin on page 2 of this paper.

Amendments to the Claims are reflected in the listing of claims, which begins on page 3 of this
paper.

Remarks/Arguments begin on page 9 of this paper.

Amendments to the Specification:

Please replace the title with the following amended title:

FORWARD ERROR CORRECTION WITH PARALLEL ERROR DETECTION FOR FLASH
MEMORIES

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

1. (Currently Amended) A flash memory decoder comprising:
a decoding module configured to:
receive encoded data from the flash memory; and
decode the received encoded data to generate a plurality of partially
decoded data streams;
an error detection module communicatively coupled with the decoding module,
and comprising a plurality of error detection sub-modules operating in parallel, each error
detection sub-module configured to:
receive a different one of the plurality of partially decoded data streams;
detect whether a portion of the respective received stream contains an
error; and
forward the portion of the respective received stream containing an error
to an error correction module; and
[[an]] the error correction module, communicatively coupled with and physically
separate from the error detection module, and configured to correct the received portions of the
respective received streams containing an error.
2. (Currently Amended) The flash memory decoder of claim 1, wherein each
of the error detection sub-modules is configured to read data from a set of one or more sectors of
flash memory different from other of the error detection sub-modules.
3. (Original) The flash memory decoder of claim 2, further comprising a
read controller configured to dynamically modify the error detection sub-modules assigned to at
least a subset of the sectors of flash memory.

4. (Original) The flash memory decoder of claim 1, wherein the error correction module comprises a plurality of error correction sub-modules operating in parallel and fewer in number than the error detection sub-modules.

5. (Original) The flash memory decoder of claim 4, further comprising a power controller configured to selectively power-up one or more of the error correction sub-modules responsive to an age of the flash memory.

6. (Currently Amended) The flash memory decoder of claim 4, further comprising:
an error monitoring module, communicatively coupled with the error detection module, and configured to monitor a rate of errors from the error detection module,
wherein ~~[[the]]~~ a power controller is configured to selectively power-up one or more of the error correction sub-modules when the monitored rate of errors exceeds a threshold.

7. (Original) The flash memory decoder of claim 4, further comprising:
an error monitoring module, communicatively coupled with the error detection module, and configured to monitor a rate of errors from the error detection module for each of a plurality of sectors of the flash memory,
wherein a power controller is configured to selectively power-up an error correction sub-module for assignment to a set of one or more of the monitored sectors when the monitored rate of errors for the set exceeds a threshold.

8. (Original) The flash memory decoder of claim 4, wherein,
each error correction sub-module is assigned a set of two or more error detection sub-modules different from error detection sub-modules associated with other of the error correction sub-modules; and
each error correction sub-module is configured to receive portions of the respective received streams containing an error detected in parallel by the set of two or more error detection sub-modules assigned to the respective error correction sub-module.

9. (Original) The flash memory decoder of claim 1, further comprising a read controller configured to selectively power-down one or more subsets of the error detection sub-modules.

10. (Original) The flash memory decoder of claim 1, further comprising:
the flash memory, communicatively coupled with the decoding module;
an encoder, communicatively coupled with the flash memory, and configured to encode data at a coding rate for storage as the encoded data on the flash memory; and
an adaptive encoding rate controller configured to modify the coding rate responsive to an age of the flash memory.

11. (Original) The flash memory decoder of claim 1, further comprising:
an error monitoring module, communicatively coupled with the error detection module, and configured to monitor a rate of errors from the error detection module; and
an adaptive encoding rate controller configured to modify a coding rate for a flash memory encoding module when the monitored rate of errors exceeds a threshold.

12. (Original) The flash memory decoder of claim 1, further comprising:
an error monitoring module, communicatively coupled with the error detection module, and configured to monitor a rate of errors from the error detection module for each of a plurality of sectors of the flash memory; and
an adaptive encoding rate controller configured to modify a coding rate of a set of one or more of the monitored sectors when the monitored rate of errors for the set exceeds a threshold.

13. (Original) The flash memory decoder of claim 1, wherein each error detection sub-module is configured to direct error-free portions of the respective received streams to bypass the error correction module.

14. (Original) The flash memory decoder of claim 1, wherein,
the error detection module comprises the decoding module; and
the encoded data is encoded with a Hamming code, a BCH code, a Turbo code, or a low-density parity check code.

15. (Original) A system comprising:
an encoder configured to encode data for storage on a flash memory;
the flash memory, communicatively coupled with the encoding module, and
configured to store the encoded data; and
a decoder, communicatively coupled with the flash memory, and configured to:
retrieve the encoded data from flash memory to generate a plurality of data
streams; and
process, at each of a plurality of error detection sub-modules of the
decoder operating in parallel, a different one of the plurality of data streams, wherein each error
detection sub-module is configured to:
detect whether a portion of the respective received stream contains
an error; and
forward the portion of the respective received stream containing an
error to an error correction module of the decoder; and
correct, with the error correction module physically separate from the
error detection module, the forwarded portions of the respective received streams containing an
error.

16. (Original) The system of claim 15, wherein the encoder is further
configured to adaptively modify the coding rate responsive to an age of the flash memory or a
rate of errors associated with the decoded data.

17. (Original) A method comprising:
receiving encoded data from a flash memory comprising a plurality of data
streams;
processing, at each of a plurality of error detection sub-modules operating in
parallel, a different one of the plurality of data streams, wherein each error detection sub-module
is configured to:
detect whether a portion of the respective received stream contains an
error; and

forward the portion of the respective received stream containing an error to an error correction module; and

correcting, with the error correction module physically separate from an error detection module, the forwarded portions of the respective received streams containing an error.

18. (Original) The method of claim 17, further comprising:
dynamically modifying the error detection sub-modules assigned to receive data from respective sectors of flash memory.

19. (Original) The method of claim 17, wherein the error correction module comprises a plurality of error correction sub-modules operating in parallel and fewer in number than the error detection sub-modules.

20. (Original) The method of claim 19, further comprising:
powering-up, from an inactive mode, one or more of the error correction sub-modules responsive to an age of the flash memory.

21. (Original) The method of claim 19, further comprising:
monitoring a rate of errors from the error detection module; and
powering-up one or more of the error correction sub-modules when the monitored rate of errors exceeds a threshold.

22. (Original) The method of claim 19, further comprising:
monitoring a rate of errors from the error detection module for each of a plurality of sectors of the flash memory; and
powering-up an error correction sub-module for assignment to a set of one or more of the monitored sectors when the monitored rate of errors for the set exceeds a threshold.

23. (Original) The method of claim 17, further comprising:
modifying a coding rate for data to be stored as the encoded data on the flash memory responsive to an age of the flash memory.

24. (Original) The method of claim 17, further comprising:
monitoring a rate of errors from the error detection module; and

modifying a coding rate for data to be stored as the encoded data on the flash memory when the monitored rate of errors exceeds a threshold.

25. (Currently Amended) The method of claim 17, further comprising:
monitoring a rate of errors from the error detection module for each of a plurality of sectors of the flash memory; and
modifying a coding rate for data to be stored as the encoded data on a set of one or more of the monitored sectors of the flash memory when the monitored rate of errors for the set exceeds a threshold.

REMARKS/ARGUMENTS

This Amendment is in response to the Office Action mailed January 31, 2013 (“Office Action”). Claims 1-25 were pending in the present application. This Amendment amends claims 1-2, 6, and 25 to correct clerical errors. Claims 1-25 remain pending in the application. Applicants submit that no new matter has been introduced by virtue of these amendments. Reconsideration of the rejected claims is respectfully requested.

THE SPECIFICATION

The title of the invention is allegedly not descriptive. Applicants have amended the title.

THE CLAIMS

Allowable Subject Matter

Applicants appreciate the indication of allowability of claims 3-12, 16, and 18-25 if rewritten in independent form to include the limitations of their respective base claims. As discussed below, the independent claims 1, 15, and 17 are allowable over the cited reference; hence, claims 3-12, 16, and 18-25 are each patentable at least for the reason of depending from a respective allowable claim.

35 U.S.C. § 102 Rejection of Claims 1, 2, 13-15 and 17

Claims 1-2, 13-15, and 17 are rejected under 35 U.S.C. §102(b) as allegedly being anticipated by U.S. Patent Publication No. 2005/0138521 to Suzuki et al. (hereinafter “Suzuki”).

Claims 1, 15, and 17

Claim 1 recites a flash memory decoder comprising a decoding module, an error detection module, and an error correction module. The decoding module is configured to decode received encoded data to generate a plurality of partially decoded data streams. The error detection module comprises a plurality of error detection sub-modules operating in parallel, where each error detection sub-module is configured to receive a different one of the partially decoded data streams, and to detect whether a portion of the respective received stream contains an error. The error correction module, which is physically separate from the error detection

module, is configured to correct received portions of the respective received streams containing an error. Applicants submit that at least some of these elements are not disclosed in Suzuki.

Suzuki is directed to a forward error correction (FEC) decoder that extracts FEC parameters encoded into a signal stream to adaptively change operational parameters. See Abstract. Suzuki's receiver includes an FEC chain decoding functional block and a parameter extraction functional block. See para. [0016]. The FEC chain decoding functional block decodes FEC blocks and detects if an FEC block is a Control Packet (CP) that includes FEC parameters. See Abstract, para. [0016]. The FEC chain decoding functional block is configured for the CP format, and all FEC blocks are decoded as being CPs, such that an error will be detected and flagged, by setting an error flag high, if the FEC block is not a CP. See para. [0140]-[0142]; FIG. 18B. If the error flag is set low (indicating an actual CP is detected/decoded), the parameter extraction functional block then processes the CP to extract the FEC parameters from the CP. See para. [0022] and [0140]-[0142]; FIG. 18B. The extracted FEC parameters are later used by the FEC chain decoding functional block for decoding subsequent FEC blocks. See para. [0017].

The Office Action relies on Suzuki at paragraphs [0122]-[0123] for the feature of the decoding module being configured to decode received encoded data to generate a plurality of partially decoded data streams. Paragraphs [0122]-[0123] of Suzuki refer to FIG. 13, which illustrates the functionality of the FEC decoding chain (i.e., the FEC chain decoding functional block). The FEC decoding chain of FIG. 13 includes, in series, a turbo decoder, a de-interleaver, a Reed Solomon (RS) decoder, a descrambler, and an MPEG packetizer. Paragraphs [0122]-[0123] describe a demodulator receiving an input signal and generating a Queue Block (QB) stream including Turbo Blocks (TBs). However, the cited paragraphs of Suzuki only discuss demodulating a single stream of data – the QB stream. This single QB stream is processed serially by the functional blocks of the FEC decoding chain of FIG. 13. In contrast, the claimed decoding module is configured to decode received encoded data to generate a plurality of partially decoded data streams. Thus, not only does the cited portion disclose demodulating versus the claimed decoding, only a single stream is disclosed versus the claimed plurality of streams. Accordingly, at least this feature of claim 1 is not shown in Suzuki.

Moreover, the claimed error detection module is also not disclosed in Suzuki. The claimed error detection module comprises a plurality of error detection sub-modules

operating in parallel, where each error detection sub-module is configured to receive a different one of the partially decoded data streams, and to detect whether a portion of the respective received stream contains an error. Thus, the multiple error detection sub-modules perform the same function on different streams. For the claimed error detection module and its functions, the Office Action relies on paragraphs [0123] and [0022] of Suzuki. As discussed above, paragraph [0123] describes the demodulator demodulating the single QB stream. Paragraph [0022] discusses the FEC decoding chain using an error flag when decoding/detecting a CP (Control Packet), and in response to the error flag setting, the CP processor extracting FEC parameters from the CP. However, the cited portions of Suzuki fail to disclose the claimed error detection module. The claimed error detection module comprises a plurality of error detection sub-modules performing the same functions and operating in parallel, whereas in Suzuki, the various functional blocks (e.g., the demodulator, blocks of the FEC decoding chain, the CP processor) perform different functions and operate serially. Accordingly, the features of the error detection module are also not shown in Suzuki.

Furthermore, the claimed error correction module is also not disclosed in Suzuki. The claimed error correction module, which is physically separate from the error detection module, is configured to correct received portions of the respective received streams containing an error. For the claimed error correction module, the Office Action relies on paragraph [0142] of Suzuki. As discussed above, paragraph [0142], which refers to FIG. 18B, describes the FEC chain decoding functional block decoding all FEC blocks as being CP, such that if an FEC block is not a CP, an error will be detected and flagged by setting the error flag high. If the FEC block is an actual CP, the error flag will be set low. A low error flag directs the CP processor (i.e., the parameter extraction functional block) to extract the FEC parameters from the CP. However, the cited portions of Suzuki fail to disclose the claimed error correction module. The error correction module is configured to correct received portions of the respective received streams containing an error, whereas in Suzuki, an error (indicated by the error flag set high) is not actually corrected by the CP processor, but simply indicates that the CP processor should not attempt to extract FEC parameters from the non-CP FEC block. Moreover, the claimed error correction module is physically separate from the claimed error detection module, but the cited portions of Suzuki teach conventional turbo decoding and RS decoding, wherein error detection and error correction for the respective FEC code is not performed by modules which are

physically separate. Accordingly, these features of the error correction module are also not shown in Suzuki.

For the above reasons, at least these elements of claim 1 are not disclosed by the relied-upon portions of Suzuki. Therefore, claim 1 is patentable over Suzuki. Applicants respectfully request withdrawal of the rejection and allowance of claim 1.

Claims 15 and 17 recite features similar to those discussed above with reference to claim 1. The Office Action rejected claims 15 and 17 under similar rationales as applied against claim 1. For at least similar reasons as those stated with respect to claim 1, claims 15 and 17 are patentable over Suzuki. Applicants respectfully request withdrawal of the rejections and allowance of claims 15 and 17.

Claims 2 and 13-14

Claims 2 and 13-14 depend from and incorporate all the features of independent claim 1. For at least the reasons stated above with respect to claim 1, claims 2 and 13-14 are patentable over Suzuki. Particular claims might have other reasons for allowability over the cited references, and not all of those reasons need be provided here. Applicants respectfully request withdrawal of the rejections and allowance of claims 2 and 13-14.

Amendments to the Claims

Unless otherwise specified, amendments to the claims are made for purposes of clarity, and are not intended to alter the scope of the claims or limit any equivalents thereof. The amendments are supported by the Specification as filed and do not add new matter.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

Further, the Commissioner is hereby authorized to charge any additional fees or credit any overpayment in connection with this paper to Deposit Account No. 20-1430.

Appl. No. 12/858,510
Amdt. dated April 29, 2013
Response to Office Action of January 31, 2013

PATENT

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 650-326-2400.

Respectfully submitted,

/Mymy N. Henderson/

Mymy N. Henderson
Registration No. 64,975

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Two Embarcadero Center, Eighth Floor
San Francisco, California 94111-3834
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Fax: 415-576-0300

Electronic Acknowledgement Receipt	
EFS ID:	15644436
Application Number:	12858510
International Application Number:	
Confirmation Number:	6028
Title of Invention:	FORWARD ERROR CORRECTION FOR MEMORIES
First Named Inventor/Applicant Name:	Sameep Dave
Customer Number:	61668
Filer:	Mymy Nguyen Henderson
Filer Authorized By:	
Attorney Docket Number:	90523-789306 (003710US)
Receipt Date:	29-APR-2013
Filing Date:	18-AUG-2010
Time Stamp:	22:13:48
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		Response.pdf	141363 970fd0dd9bb1f39e763e345ec891ada037ff a346	yes	13

Multipart Description/PDF files in .zip description		
Document Description	Start	End
Amendment/Req. Reconsideration-After Non-Final Reject	1	1
Specification	2	2
Claims	3	8
Applicant Arguments/Remarks Made in an Amendment	9	13

Warnings:

Information:

Total Files Size (in bytes):	141363
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This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875				Application or Docket Number 12/858,510		Filing Date 08/18/2010		☐ To be Mailed	
ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO									
APPLICATION AS FILED – PART I									
(Column 1)		(Column 2)							
FOR	NUMBER FILED	NUMBER EXTRA				RATE (\$)	FEE (\$)		
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A				N/A			
☐ SEARCH FEE (37 CFR 1.16(k), (l), or (m))	N/A	N/A				N/A			
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A				N/A			
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =		*			X \$	=		
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =		*			X \$	=		
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$310 (\$155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).								
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))									
* If the difference in column 1 is less than zero, enter "0" in column 2.						TOTAL			
APPLICATION AS AMENDED – PART II									
(Column 1)		(Column 2)		(Column 3)					
AMENDMENT	04/29/2013	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)		ADDITIONAL FEE (\$)	
	Total (37 CFR 1.16(i))	* 25	Minus	** 25	= 0	X \$80 =		0	
	Independent (37 CFR 1.16(h))	* 3	Minus	***3	= 0	X \$420 =		0	
	☐ Application Size Fee (37 CFR 1.16(s))								
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))								
TOTAL ADD'L FEE						0			
(Column 1)		(Column 2)		(Column 3)					
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)		ADDITIONAL FEE (\$)	
	Total (37 CFR 1.16(i))	*	Minus	**	=	X \$			
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X \$			
	☐ Application Size Fee (37 CFR 1.16(s))								
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))								
TOTAL ADD'L FEE									
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3. ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20". *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3". The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.									

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**
If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

61668 7590 08/20/2013
KILPATRICK TOWNSEND & STOCKTON, LLP/VIASAT
VIASAT, INC. (CLIENT #017018)
TWO EMBARCADERO CENTER
8TH FLOOR
SAN FRANCISCO, CA 94111

EXAMINER

MEHRMANESH, ELMIRA

ART UNIT

PAPER NUMBER

2113

DATE MAILED: 08/20/2013

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/858,510	08/18/2010	Sameep Dave	90523-789306 (003710US)	6028

TITLE OF INVENTION: FORWARD ERROR CORRECTION FOR MEMORIES

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$1780	\$300	\$0	\$2080	11/20/2013

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PART B - FEE(S) TRANSMITTAL

**Complete and send this form, together with applicable fee(s), to: Mail Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885**

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

61668 7590 08/20/2013
KILPATRICK TOWNSEND & STOCKTON, LLP/VIASAT
VIASAT, INC. (CLIENT #017018)
TWO EMBARCADERO CENTER
8TH FLOOR
SAN FRANCISCO, CA 94111

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/858,510	08/18/2010	Sameep Dave	90523-789306 (003710US)	6028

TITLE OF INVENTION: FORWARD ERROR CORRECTION FOR MEMORIES

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$1780	\$300	\$0	\$2080	11/20/2013

EXAMINER	ART UNIT	CLASS-SUBCLASS
MEHRMANESH, ELMIRA	2113	714-773000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

- (1) the names of up to 3 registered patent attorneys or agents OR, alternatively, 1 _____
- (2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed. 2 _____
- 3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

- ☐ Issue Fee
- ☐ Publication Fee (No small entity discount permitted)
- ☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): (**Please first reapply any previously paid issue fee shown above**)

- ☐ A check is enclosed.
- ☐ Payment by credit card. Form PTO-2038 is attached.
- ☐ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)

☐ Applicant certifying micro entity status. See 37 CFR 1.29

NOTE: Absent a valid certification of Micro Entity Status (see form PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

☐ Applicant asserting small entity status. See 37 CFR 1.27

NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

☐ Applicant changing to regular undiscounted fee status.

NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____

Date _____

Typed or printed name _____

Registration No. _____

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.



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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/858,510	08/18/2010	Sameep Dave	90523-789306 (003710US)	6028

61668	7590	08/20/2013
KILPATRICK TOWNSEND & STOCKTON, LLP/VIASAT		
VIASAT, INC. (CLIENT #017018)		
TWO EMBARCADERO CENTER		
8TH FLOOR		
SAN FRANCISCO, CA 94111		

EXAMINER	
MEHRMANESH, ELMIRA	

ART UNIT	PAPER NUMBER
2113	

DATE MAILED: 08/20/2013

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 471 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 471 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 12/858,510	Applicant(s) DAVE ET AL.	
	Examiner Elmira Mehrmanesh	Art Unit 2113	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to an amendment filed on 4/29/2013.
☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

3. ☒ The allowed claim(s) is/are 1-25. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a) ☐ All b) ☐ Some *c) ☐ None of the:

1. ☐ Certified copies of the priority documents have been received.

2. ☐ Certified copies of the priority documents have been received in Application No. _____.

3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

* Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)	5. ☐ Examiner's Amendment/Comment
2. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____	6. ☒ Examiner's Statement of Reasons for Allowance
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material	7. ☐ Other _____
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____	

/Bryce P Bonzo/ Primary Examiner, Art Unit 2113	
--	--

DETAILED ACTION

This action is in response to an amendment filed on April 29, 2013 for the application of Dave et al., for a "Forward error correction with parallel error detection for flash memories" filed on August 18, 2010.

Claims 1-25 are pending in the application.

Claims 1, 2, 6, and 25 have been amended.

Claims 1-25 are allowed.

Specification

In view of the Applicant's amendments to the title of the invention, the previous objections have been withdrawn.

Reasons for allowance

The following is an examiner's statement of reasons for allowance:

Applicant's arguments see pages 9-12, filed on April 29, 2013 with respect to claims 1-25 have been fully considered and are persuasive. The previous 102(b) rejection of claims 1, 2, 13-15, and 17 has been withdrawn.

In response to applicants' arguments regarding claims 1, 15, and 17, after a complete search of all the relevant prior art the examiner has determined the claims are in condition for allowance. The following limitations when viewed in combination with the remainder of the claim as a whole place this application in condition for allowance.

As per claim 1, the examiner finds the novel and non obvious feature of claim 1, when read as whole to be an error detection module communicatively coupled with the decoding module, and comprising a plurality of error detection sub-modules operating in

parallel, each error detection sub-module configured to: receive a different one of the plurality of partially decoded data streams; detect whether a portion of the respective received stream contains an error; and forward the portion of the respective received stream containing an error to an error correction module; and an error correction module, communicatively coupled with and physically separate from the error detection module, and configured to correct the received portions of the respective received streams containing an error.

Suzuki et al. (U.S. PGPUB 20050138521) discloses a forward error correction (FEC) decoder with error detection/correction capabilities ([0022]). Suzuki further discloses a plurality of data blocks with FEC decoding chain functionality ([0214]).

However Suzuki does not teach a plurality of error detection sub-modules operating in parallel, each error detection sub-module configured to: receive a different one of the plurality of partially decoded data streams; detect whether a portion of the respective received stream contains an error; and forward the portion of the respective received stream containing an error to an error correction module; and an error correction module, communicatively coupled with and physically separate from the error detection module as recited in claim 1. Therefore, claim 1 is allowable over Suzuki.

As per claims 15 and 17, same reasons as claim 1 apply.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Elmira Mehrmanesh whose telephone number is (571)272-5531. The examiner can normally be reached on 10-6 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, James Kramer can be reached on (571) 272-6783. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/E. M./

Examiner, Art Unit 2113

Notice of References Cited	Application/Control No. 12/858,510	Applicant(s)/Patent Under Reexamination DAVE ET AL.	
	Examiner Elmira Mehrmanesh	Art Unit 2113	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-2006/0245417 A1	11-2006	Conner et al.	370/352
*	B	US-7,155,063 B2	12-2006	Chiba, Yukio	382/233
*	C	US-2009/0249151 A1	10-2009	Zhou et al.	714/748
*	D	US-8,103,942 B2	01-2012	Kuroishi et al.	714/776
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L4	11	((SAMEEP) near2 (DAVE)).INV.	US-PGPUB; USPAT	OR	ON	2013/08/10 22:37
L5	12	((RUSSELL) near2 (FUERST)).INV.	US-PGPUB; USPAT	OR	ON	2013/08/10 22:37
L6	1	((MARK) near2 (KOHOT)).INV.	US-PGPUB; USPAT	OR	ON	2013/08/10 22:37
L7	1	((JIM) near2 (KESZENHEIMER)).INV.	US-PGPUB; USPAT	OR	ON	2013/08/10 22:37
L8	84	((WILLIAM) near2 (THESLING)).INV.	US-PGPUB; USPAT	OR	ON	2013/08/10 22:37
L9	41	("20070283428" "20080148132" "20080163028" "20080244362" "20080301526" "7231585" "7305596" "7394689" "20040243906" "20050172179" "20030041299" "20080244370" "7304893" "20080282128" "6751766" "20070171730" "20070266296" "20080212371" "20080276150" "7203874" "20080072120" "20090013234" "20070204206" "20070223277" "20080109703" "20080130341" "20080270680" "6684353" "20080052564" "20060059406" "20070271494" "20080168320" "7296213" "7356755" "7360136" "20030037299" "20040083334" "20070266295" "20080184094" "20080313493" "7333364").PN.	US-PGPUB; USPAT	OR	ON	2013/08/10 22:37
L10	3634	(part\$3 partial\$4) near5 decod\$3 with errors	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/08/10 22:37
L11	1407	(part\$3 partial\$4) near decod\$3 with errors	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/08/10 22:37
L12	1	(L4 L5 L8 L9) and L11	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT;	OR	ON	2013/08/10 22:37

			IBM_TDB			
L13	0	("2011/0047442").URPN.	USPAT	OR	ON	2013/08/10 22:37
L14	35	(part\$3 partial\$4) near decod\$3 with (errors near5 (detect\$4 correct\$4) ECC CRC parit\$3 FEC) with (parallel concurrent\$3 simultaneous\$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/08/10 22:37
L15	3	(L4 L5 L8 L9) and L10	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/08/10 22:37
L16	4123	(714/758,773,774).CCLS.	US-PGPUB; USPAT; USOCR	OR	OFF	2013/08/10 22:37
L17	1407	(part\$3 partial\$4) near decod\$3 with errors	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/08/10 22:38
L18	50	L16 and L17	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/08/10 22:38
L19	727	decod\$3 near5 (paths channels streams signals words) with (errors near5 (detect\$4 correct\$4) ECC CRC parit\$3 FEC) with (parallel concurrent\$3 simultaneous\$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/08/10 22:38
L20	84	((WILLIAM) near2 (THESLING)).INV.	US-PGPUB; USPAT	OR	ON	2013/08/10 22:38
L21	41	("20070283428" "20080148132" "20080163028" "20080244362" "20080301526" "7231585" "7305596" "7394689" "20040243906" "20050172179" "20030041299" "20080244370" "7304893" "20080282128" "6751766" "20070171730" "20070266296" "20080212371" "20080276150" "7203874" "20080072120" "20090013234" "20070204206" "20070223277" "20080109703" "20080130341" "20080270680" "6684353" "20080052564" "20060059406" "20070271494" "20080168320" "7296213" "7356755" "7360136" "20030037299" "20040083334" "20070266295"	US-PGPUB; USPAT	OR	ON	2013/08/10 22:38

		"20080184094" "20080313493" "7333364").PN.				
L22	62	L19 and (L16 L20 L21)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/08/10 22:38
L23	1	L19 and L21	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/08/10 22:38
L24	11	L19 same flash near5 memor\$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/08/10 22:38
L25	22	L21 and decod\$3 with (errors near5 (detect\$4 correct\$4) ECC CRC parit\$3 FEC)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/08/10 22:38
L26	22	L21 and decod\$3 same (errors near5 (detect\$4 correct\$4) ECC CRC parit\$3 FEC)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/08/10 22:38
L27	14	decod\$3 near5 (multiple pluralit\$3 various) near5 streams same errors near5 correct\$5 same detect\$5	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/08/10 22:38
L28	0	("2011/0047442").URPN.	USPAT	OR	ON	2013/08/10 22:40
L29	1	decod\$3 with (errors near5 (detect\$4 correct\$4) ECC CRC parit\$3 FEC) with (parallel concurrent\$3 simultaneous\$3) with physical\$4 near5 (separat\$3 locat\$4)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/08/10 22:42
L30	18	(errors near5 (detect\$4 correct\$4) ECC CRC parit\$3 FEC) with (parallel concurrent\$3 simultaneous\$3) with physical\$4 near5 (separat\$3 different\$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/08/10 22:42

L31	1774	parallel\$3 with (plural\$5 multiples) with (errors near\$5 detect\$4 ECC CRC parit\$3 FEC)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/08/10 22:50
L32	225	parallel\$3 with (plural\$5 multiples) with (errors near\$5 detect\$4 ECC CRC parit\$3 FEC) with decod\$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/08/10 22:50
L33	2	32 and (multiple pluralit\$3 various) near\$5 streams same errors near\$5 correct\$5 same detect\$5	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/08/10 22:53
L34	2	21 and parallel\$3 with (plural\$5 multiples) with (errors near\$5 detect\$4 ECC CRC parit\$3 FEC)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/08/10 22:54
L35	17	("2003/0041299").URPN.	USPAT	OR	ON	2013/08/10 22:56
L36	1	("2008/0244362").URPN.	USPAT	OR	ON	2013/08/10 22:56
L37	47	parallel\$3 with (plural\$5 multiples) with errors near\$5 detect\$4 with decod\$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2013/08/10 22:57
L42	0	decod\$3 with (errors near\$5 (detect\$4 correct\$4) ECC CRC parit\$3 FEC) with (parallel concurrent\$3 simultaneous\$3) with physical\$4 near\$5 (separat\$3 different\$3 locat\$4).clm.	US-PGPUB	OR	ON	2013/08/10 23:02
L43	4	decod\$3 near\$5 (multiple pluralit\$3 various) near\$5 streams same errors near\$5 correct\$5 same detect\$5.clm.	US-PGPUB	OR	ON	2013/08/10 23:02
L44	1	parallel\$3 with (plural\$5 multiples) with errors near\$5 detect\$4 with decod\$3 same physical\$4 near\$5 (separat\$3 different\$3 locat\$4).clm.	US-PGPUB	OR	ON	2013/08/10 23:03

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L38	1	decod\$3 with (errors near\$5 (detect\$4 correct\$4) ECC CRC parit\$3 FEC) with (parallel concurrent\$3 simultaneous\$3) with physical\$4 near\$5 (separat\$3 different\$3 locat\$4).clm.	US-PGPUB; USPAT; UPAD	OR	ON	2013/08/10 23:00

EAST Search History

L39	8	decod\$3 near5 (multiple pluralit\$3 various) near5 streams same errors near5 correct\$5 same detect\$5.clm.	US-PGPUB; USPAT; UPAD	OR	ON	2013/08/10:23:00
L40	1	parallel\$3 with (plural\$5 multiples) with errors near5 detect\$4 with decod\$3 same physical\$4 near5 (separat\$3 different\$3 locat\$4).clm.	US-PGPUB; USPAT; UPAD	OR	ON	2013/08/10:23:01
L41	0	decod\$3 with (errors near5 (detect\$4 correct\$4) ECC CRC parit\$3 FEC) with (parallel concurrent\$3 simultaneous\$3) with physical\$4 near5 (separat\$3 different\$3 locat\$4).clm.	US-PGPUB	OR	ON	2013/08/10:23:02

8/ 10/ 2013 11:03:27 PM

C:\ Users\ emehrmanesh\ Documents\ EAST\ Workspaces\ 12858510.wsp

Issue Classification 	Application/Control No. 12858510	Applicant(s)/Patent Under Reexamination DAVE ET AL.	
	Examiner Elmira Mehrmanesh	Art Unit 2113	

CPC						
Symbol					Type	Version

CPC Combination Sets					
Symbol			Type	Set	Ranking

/ELMIRA MEHRMANESH/ Examiner.Art Unit 2113 (Assistant Examiner)	08/10/2013 (Date)	Total Claims Allowed: 25	
/BRYCE BONZO/ Primary Examiner.Art Unit 2113 (Primary Examiner)	08/12/2013 (Date)	O.G. Print Claim(s) 1	O.G. Print Figure 1

Issue Classification 	Application/Control No. 12858510	Applicant(s)/Patent Under Reexamination DAVE ET AL.
	Examiner Elmira Mehrmanesh	Art Unit 2113

US ORIGINAL CLASSIFICATION						INTERNATIONAL CLASSIFICATION														
CLASS			SUBCLASS			CLAIMED					NON-CLAIMED									
714			773			G	0	6	F	11 / 00 (2006.01.01)										
CROSS REFERENCE(S)																				
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)																			
714	774																			

/ELMIRA MEHRMANESH/ Examiner.Art Unit 2113 (Assistant Examiner)	08/10/2013 (Date)	Total Claims Allowed: 25	
/BRYCE BONZO/ Primary Examiner.Art Unit 2113 (Primary Examiner)	08/12/2013 (Date)	O.G. Print Claim(s) 1	O.G. Print Figure 1

<i>Index of Claims</i> 	Application/Control No. 12858510	Applicant(s)/Patent Under Reexamination DAVE ET AL.
	Examiner Elmira Mehrmanesh	Art Unit 2113

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant				☐ CPA				☐ T.D.				☐ R.1.47			
CLAIM		DATE													
Final	Original	01/27/2013	08/10/2013												
	1	✓	=												
	2	✓	=												
	3	O	=												
	4	O	=												
	5	O	=												
	6	O	=												
	7	O	=												
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	12	O	=												
	13	✓	=												
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	15	✓	=												
	16	O	=												
	17	✓	=												
	18	O	=												
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	21	O	=												
	22	O	=												
	23	O	=												
	24	O	=												
	25	O	=												

Search Notes 	Application/Control No. 12858510	Applicant(s)/Patent Under Reexamination DAVE ET AL.
	Examiner Elmira Mehrmanesh	Art Unit 2113

CPC- SEARCHED		
Symbol	Date	Examiner

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner
714	758,773,774	1/27/2013	EM
714	758,773,774	8/10/2013	EM

SEARCH NOTES		
Search Notes	Date	Examiner
EAST search, please see the attached history.	1/27/2013	EM
Inventor name search.	1/27/2013	EM
Updated EAST search, please see the attached history.	8/10/2013	EM
Updated inventor name search.	8/10/2013	EM

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner
	US-PGPUB	8/10/2013	EM

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I hereby certify that this correspondence is being filed via
EFS-Web with the United States Patent and Trademark Office
on October 7, 2013.

PATENT
Attorney Docket No.: 90523-003710US-789306
Client Ref. No.: ECC-0407-US-2

KILPATRICK TOWNSEND & STOCKTON LLP

By: /Kelly Mak/

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Sameep Dave et al.

Application No.: 12/858,510

Filed: August 18, 2010

For: FORWARD ERROR CORRECTION
WITH PARALLEL ERROR DETECTION
FOR FLASH MEMORIES

Customer No.: 61668

Confirmation No.: 6028

Examiner: Elmira Mehrmanesh

Technology Center/Art Unit: 2113

AMENDMENT AFTER ALLOWANCE
UNDER 37 CFR § 1.312

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Commissioner:

In response to the Notice of Allowance mailed August 20, 2013, please enter the
following amendments and remarks:

Amendments to the Specification begin on page 2 of this paper.

Remarks/Arguments begin on page 3 of this paper.

Amendments to the Specification:

Please replace the title with the following amended title:

FORWARD ERROR CORRECTION WITH PARALLEL ERROR DETECTION FOR FLASH
MEMORIES

REMARKS/ARGUMENTS

This Amendment is in response to the Notice of Allowance mailed August 20, 2013 (hereinafter "Notice of Allowance"). The pending claims 1-25 are allowed and are not amended herein.

In response to the Non-Final Office Action mailed January 31, 2013, Applicants submitted an amendment to the title of the Specification in the Response filed April 29, 2013. On page 2 of the Notice of Allowability included with the Notice of Allowance, the Examiner acknowledged Applicants' amendment to the title and withdrew the objection to the Specification. However, the first page of the Notice of Allowance does not reflect the amended title.

Accordingly, Applicants are resubmitting the amendment to the title of the Specification along with a Supplemental Application Data Sheet to update the record with the amended title, as approved by the Examiner. Correction of the title is respectfully requested.

CONCLUSION

Entry of this amendment is respectfully urged since no additional search is required, no more than a cursory review of the record is needed, and the amendments do not require a substantial amount of work on the part of the Office.

If the Examiner believes a telephone conference would expedite prosecution of this application, please contact the undersigned at (650) 326-2400.

Respectfully submitted,

/Mymy N. Henderson/
Mymy N. Henderson
Registration No. 64,975

KILPATRICK TOWNSEND & STOCKTON, LLP

Attachment

KM

Electronic Acknowledgement Receipt	
EFS ID:	17061592
Application Number:	12858510
International Application Number:	
Confirmation Number:	6028
Title of Invention:	FORWARD ERROR CORRECTION FOR MEMORIES
First Named Inventor/Applicant Name:	Sameep Dave
Customer Number:	61668
Filer:	Mymy Nguyen Henderson
Filer Authorized By:	
Attorney Docket Number:	90523-789306 (003710US)
Receipt Date:	07-OCT-2013
Filing Date:	18-AUG-2010
Time Stamp:	19:11:32
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Application Data Sheet	SADS_789306.pdf	315887 083be8ef152d44371d5b9bed71aa888dc1b9df44	no	7

Warnings:

Information:

This is not an USPTO supplied ADS fillable form

2		Amend_789306.pdf	95334	yes	3
			c1df99c83854fcc857b3c298f074dffa7c0c59f6		
Multipart Description/PDF files in .zip description					
		Document Description	Start	End	
		Amendment after Notice of Allowance (Rule 312)	1	1	
		Specification	2	2	
		Applicant Arguments/Remarks Made in an Amendment	3	3	

Warnings:

Information:

Total Files Size (in bytes):	411221
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This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	90523-003710US-789306
		Application Number	<u>12/858,510</u>
Title of Invention	FORWARD ERROR CORRECTION <u>WITH PARALLEL ERROR DETECTION</u> FOR <u>FLASH</u> MEMORIES		
The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76. This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.			

Secrecy Order 37 CFR 5.2

	Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)
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Inventor Information

Inventor 1					
Legal Name					
Prefix	Given Name	Middle Name		Family Name	Suffix
	Sameep			Dave	
Residence Information (Select One)		☐ US Residency ☒ Non US Residency		☐ Active US military Service	
City	Stow	State/Province	Ohio	Country of Residence	US
Mailing Address of Inventor:					
Address 1	4689 Concord Drive				
Address 2					
City	Stow	State/Province	OH		
Postal Code	44224	Country	US		

Inventor 2					
Legal Name					
Prefix	Given Name	Middle Name		Family Name	Suffix
	Russell			Fuerst	
Residence Information (Select One)		☒ US Residency ☐ Non US Residency		☐ Active US military Service	

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	90523-003710US-789306
	Application Number	12/858,510
Title of Invention	FORWARD ERROR CORRECTION <u>WITH PARALLEL ERROR DETECTION</u> FOR <u>FLASH</u> MEMORIES	

City	Mentor	State/Province	OH	Country of Residence	US
Mailing Address of Inventor:					
Address 1	8475 Mansion Boulevard				
Address 2					
City	Mentor	State/Province	OH		
Postal Code	44060	Country	US		

Inventor 3					
Legal Name					
Prefix	Given Name	Middle Name		Family Name	Suffix
	Mark			Kohoot	
Residence Information (Select One)	☒ US Residency		☐ Non US Residency		☐ Active US military Service
City	Cleveland Heights	State/Province	OH	Country of Residence	United States of America
Mailing Address of Inventor:					
Address 1	2748 Lancashire Road				
Address 2					
City	Cleveland Heights	State/Province	OH		
Postal Code	44106	Country	US		

Inventor 4					
Legal Name					
Prefix	Given Name	Middle Name		Family Name	Suffix
	Jim			Keszenheimer	
Residence Information (Select One)	☒ US Residency		☐ Non US Residency		☐ Active US military Service

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	90523-003710US-789306
	Application Number	12/858,510
Title of Invention	FORWARD ERROR CORRECTION <u>WITH PARALLEL ERROR DETECTION</u> FOR <u>FLASH</u> MEMORIES	

City	Chagrin Falls	State/Province	OH	Country of Residence	US
Mailing Address of Inventor:					
Address 1	8025 Bainbrook				
Address 2					
City	Chagrin Falls	State/Province	OH		
Postal Code	44023	Country	US		

Inventor 5					
Legal Name					
Prefix	Given Name	Middle Name		Family Name	Suffix
	William	H.		Thesling	
Residence Information (Select One)	☒ US Residency		☐ Non US Residency		☐ Active US military Service
City	Hudson	State/Province	OH	Country of Residence	US
Mailing Address of Inventor:					
Address 1	7332 E. Firelands Drive				
Address 2					
City	Hudson	State/Province	OH		
Postal Code	44236	Country	OH		

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below. For further information see 37 CFR 1.33(a).	
☐	An Address is being provided for the correspondence information of this application
Customer Number	61668
Email Address	ipefiling@kilpatricktownsend.com

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	90523-003710US-789306
	Application Number	12/858,510
Title of Invention	FORWARD ERROR CORRECTION <u>WITH PARALLEL ERROR DETECTION</u> FOR <u>FLASH</u> MEMORIES	

Application Information:

Title of Invention	FORWARD ERROR CORRECTION <u>WITH PARALLEL ERROR DETECTION</u> FOR <u>FLASH</u> MEMORIES		
Attorney Docket Number	90523-003710US-789306	Small Entity Status Claimed	☐
Application Type	NonProvisional		
Subject Matter	Utility		
Total Number of Drawing Sheets (if any)	7	Selected Figure for Publication (if any)	4

Publication Information:

	Request Early Publication (Fee required at time of Request 37 CFR 1.219)
	Request Not to Publish. I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application has not and will not be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32). Either enter Customer Number or complete the Representative Name section below. If both sections are completed the Customer Number will be used for the Representative Information during processing.			
Please Select One:	☒ Customer Number	☐ US Patent Practitioner	☐ Limited Recognition (37 CFR 11.9)
Customer Number	61668		

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, or 365(c) or indicate National Stage entry from a PCT application. Providing this information in the application data sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78.
--

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	90523-003710US-789306
	Application Number	12/858,510
Title of Invention	FORWARD ERROR CORRECTION <u>WITH PARALLEL ERROR DETECTION</u> FOR <u>FLASH</u> MEMORIES	

Prior Application Status:	<u>Expired</u>				
Application Number	Continuity Type	Prior Application Number	Filing Date	Patent Number	Issue Date
This application is	A Non-provisional of	61/234,911	August 18, 2009		

Foreign Priority Information:

This section allows for the applicant to claim priority to a foreign application. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55(d). When priority is claimed to a foreign application this is eligible for retrieval under the priority document exchange program (PDX) the information will be used by the Office to automatically attempt retrieval pursuant to 37 CFR 1.55(h)(1) and (2). Under the PDX program, applicant bears the ultimate responsibility for ensuring that a copy of the foreign application is received by the Office from the participating foreign intellectual property office, or a certified copy of the foreign priority application is filed, within the time period specified in 37 CFR 1.55(g)(1).			
Application Number	Country	Filing Date	Access Code (if applicable)

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications

☐	This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to claimed invention that has an effective filing date on or after March 16, 2013.
--------------------------	--

Authorization to Permit Access:

X	Authorization to Permit Access to the Instant Application by the Participating Offices
If checked, the undersigned hereby grants the USPTO authority to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the World Intellectual Property Office (WIPO), and any other intellectual property offices in which a foreign application claiming priority to the instant patent application is filed access to the instant patent application. See 37 CFR 1.14(c) and (h). This box should not be checked if the applicant does not wish the EPO, JPO, KIPO, WIPO, or other intellectual property office in which a foreign application claiming priority to the instant patent application is filed to have access to the instant patent application. In accordance with 37 CFR 1.14(h) (3), access will be provided to a copy of the instant patent application with respect to: 1) the instant patent application-as-filed; 2) any foreign application to which the instant patent application claims priority under 35 U.S.C. 119(a)-(d) if a copy of the foreign application that satisfies the certified copy requirement of 37 CFR 1.55 has been filed in the instant patent application; and 3) any U.S. application-as-filed from which benefit is sought in the instant patent application. In accordance with 37 CFR 1.14(c), access may be provided to information concerning the date of filing this Authorization.	

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	90523-003710US-789306
	Application Number	12/858,510
Title of Invention	FORWARD ERROR CORRECTION <u>WITH PARALLEL ERROR DETECTION</u> FOR <u>FLASH</u> MEMORIES	

Applicant Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of the CFR to have an assignment recorded by the Office.			
Applicant 1			
If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section.			
☒ Assignee	☐ Legal Representative under 35 U.S.C. 117	☐ Joint Inventor	
☐ Person to whom the inventor is obligated to assign		☐ Person who shows sufficient proprietary interest	
If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:			
Name of the Deceased or Legally Incapacitated Inventor:			
If the Applicant is an Organization check here. ☒			
Organization Name:		ViaSat, Inc.	
Mailing Address Information:			
Address 1		6155 El Camino Real	
Address 2			
City		State/Province	CA
Country	US	Postal Code	92009
Phone Number		Fax Number	
Email Address			

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	90523-003710US-789306
	Application Number	12/858,510
Title of Invention	FORWARD ERROR CORRECTION <u>WITH PARALLEL ERROR DETECTION</u> FOR <u>FLASH</u> MEMORIES	

Non-Applicant Assignee Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of the CFR to have an assignment recorded by the Office.			
Assignee 1			
Complete this section only if non-applicant assignee information is desired to be included on the patent application publication in accordance with 37 CFR 1.215(b). Do not include in this section an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest), as the patent application publication will include the name of the applicant(s).			
If the Assignee is an Organization check here. ☐			
Organization Name			
Mailing Address Information for Non-Applicant Assignee:			
Address 1			
Address 2			
City		State/Province	
Country		Postal Code	
Phone Number		Fax Number	
Email Address			

Signature:

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.14 for signature requirements and certifications.					
Signature	/Mymy N. Henderson/			Date	2013-10-07
First Name	Mymy	Last Name	Henderson	Registration Number	64,975

This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY. DOCKET NO	TOT CLAIMS	IND CLAIMS
12/858,510	08/18/2010	2113	1480	90523-789306 (003710US)	25	3

CONFIRMATION NO. 6028

CORRECTED FILING RECEIPT



OC000000064555915

61668

KILPATRICK TOWNSEND & STOCKTON, LLP/VIASAT
VIASAT, INC. (CLIENT #017018)
TWO EMBARCADERO CENTER
8TH FLOOR
SAN FRANCISCO, CA 94111

Date Mailed: 10/24/2013

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Inventor(s)

Sameep Dave, Stow, OH;
Russell Fuerst, Mentor, OH;
Mark Kohoot, Cleveland Heights, OH;
Jim Keszenheimer, Chagrin Falls, OH;
William H. Thesling, Hudson, OH;

Applicant(s)

Sameep Dave, Stow, OH;
Russell Fuerst, Mentor, OH;
Mark Kohoot, Cleveland Heights, OH;
Jim Keszenheimer, Chagrin Falls, OH;
William H. Thesling, Hudson, OH;

Assignment For Published Patent Application

ViaSat, Inc., Carlsbad, CA

Power of Attorney: The patent practitioners associated with Customer Number 61668

Domestic Priority data as claimed by applicant

This appln claims benefit of 61/234,911 08/18/2009

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see <http://www.uspto.gov> for more information.) - None.

Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

If Required, Foreign Filing License Granted: 08/27/2010

page 1 of 3

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 12/858,510**

Projected Publication Date: Not Applicable

Non-Publication Request: No

Early Publication Request: No

Title

FORWARD ERROR CORRECTION WITH PARALLEL ERROR DIRECTION FOR FLASH
MEMORIES

Preliminary Class

714

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at <http://www.uspto.gov/web/offices/pac/doc/general/index.html>.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, <http://www.stopfakes.gov>. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

LICENSE FOR FOREIGN FILING UNDER
Title 35, United States Code, Section 184
Title 37, Code of Federal Regulations, 5.11 & 5.15

GRANTED

The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where the conditions for issuance of a license have been met, regardless of whether or not a license may be required as set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign Assets Control, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

SelectUSA

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The U.S. offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to promote and facilitate business investment. SelectUSA provides information assistance to the international investor community; serves as an ombudsman for existing and potential investors; advocates on behalf of U.S. cities, states, and regions competing for global investment; and counsels U.S. economic development organizations on investment attraction best practices. To learn more about why the United States is the best country in the world to develop technology, manufacture products, deliver services, and grow your business, visit <http://www.SelectUSA.gov> or call +1-202-482-6800.

I hereby certify that this correspondence is being filed via
EFS-Web with the United States Patent and Trademark Office
on November 1, 2013.

PATENT
Attorney Docket No.: 90523-003710US-789306
Client Ref. No.: ECC-0407-US-2

KILPATRICK TOWNSEND & STOCKTON LLP

By: /Kelly Mak/

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

Sameep Dave et al.

Application No.: 12/858,510

Filed: August 18, 2010

For: FORWARD ERROR
CORRECTION WITH PARALLEL
ERROR DETECTION FOR FLASH
MEMORIES

Customer No.: 61668

Confirmation No.: 6028

Examiner: Elmira Mehrmanesh

Art Unit: 2113

REQUEST FOR CORRECTED FILING
RECEIPT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Commissioner:

Attached is a marked-up copy of the Corrected Filing Receipt mailed October 24, 2013 received from the Patent and Trademark Office in connection with the above-noted application for which Applicants request correction. Also attached is a copy of the Amendment after Notice of Allowance (Rule 312) and the supplemental Application Data Sheet both filed October 7, 2013.

The title of the application is incorrectly listed on the Corrected Filing Receipt. The Title of the application should be (indicated with bold and underline):

**FORWARD ERROR CORRECTION WITH PARALLEL ERROR DETECTION FOR
FLASH MEMORIES**

(FORWARD ERROR CORRECTION WITH PARALLEL ERROR DIRECTION FOR FLASH
MEMORIES)

Sameep Dave
Application No.: 12/858,510
Page 2

PATENT

Applicant believes no fee is due for this correction. However, the Commissioner is authorized to charge any additional fees or credit overpayment to Deposit Account No. 20-1430.

Applicants respectfully request issuance of a corrected Filing Receipt.

Respectfully submitted,

/Mymy N. Henderson/

Mymy N. Henderson
Reg. No. 64,975

KILPATRICK TOWNSEND & STOCKTON LLP
Two Embarcadero Center, Eighth Floor
San Francisco, California 94111-3834
Tel: (650) 326-2400
Fax: (650) 326-2422
MNH:kep

I hereby certify that this correspondence is being filed via
EFS-Web with the United States Patent and Trademark Office
on October 7, 2013.

PATENT
Attorney Docket No.: 90523-003710US-789306
Client Ref. No.: ECC-0407-US-2

KILPATRICK TOWNSEND & STOCKTON LLP

By: /Kelly Mak/

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Sameep Dave et al.

Application No.: 12/858,510

Filed: August 18, 2010

For: FORWARD ERROR CORRECTION
WITH PARALLEL ERROR DETECTION
FOR FLASH MEMORIES

Customer No.: 61668

Confirmation No.: 6028

Examiner: Elmira Mehrmanesh

Technology Center/Art Unit: 2113

AMENDMENT AFTER ALLOWANCE
UNDER 37 CFR § 1.312

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Commissioner:

In response to the Notice of Allowance mailed August 20, 2013, please enter the
following amendments and remarks:

Amendments to the Specification begin on page 2 of this paper.

Remarks/Arguments begin on page 3 of this paper.

COPY

Amendments to the Specification:

Please replace the title with the following amended title:

FORWARD ERROR CORRECTION WITH PARALLEL ERROR DETECTION FOR FLASH
MEMORIES

COPY

REMARKS/ARGUMENTS

This Amendment is in response to the Notice of Allowance mailed August 20, 2013 (hereinafter "Notice of Allowance"). The pending claims 1-25 are allowed and are not amended herein.

In response to the Non-Final Office Action mailed January 31, 2013, Applicants submitted an amendment to the title of the Specification in the Response filed April 29, 2013. On page 2 of the Notice of Allowability included with the Notice of Allowance, the Examiner acknowledged Applicants' amendment to the title and withdrew the objection to the Specification. However, the first page of the Notice of Allowance does not reflect the amended title.

Accordingly, Applicants are resubmitting the amendment to the title of the Specification along with a Supplemental Application Data Sheet to update the record with the amended title, as approved by the Examiner. Correction of the title is respectfully requested.

CONCLUSION

Entry of this amendment is respectfully urged since no additional search is required, no more than a cursory review of the record is needed, and the amendments do not require a substantial amount of work on the part of the Office.

If the Examiner believes a telephone conference would expedite prosecution of this application, please contact the undersigned at (650) 326-2400.

Respectfully submitted,

/Mymy N. Henderson/
Mymy N. Henderson
Registration No. 64,975

KILPATRICK TOWNSEND & STOCKTON, LLP

Attachment

KM

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	90523-003710US-789306
		Application Number	12/858,510
Title of Invention	FORWARD ERROR CORRECTION WITH PARALLEL ERROR DETECTION FOR FLASH MEMORIES		
The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76. This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.			

Secrecy Order 37 CFR 5.2

	Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)
--	---

Inventor Information

Inventor 1				
Legal Name				
Prefix	Given Name	Middle Name	Family Name	Suffix
	Sameep		Dave	
Residence Information (Select One)	☐ US Residency		☒ Non US Residency	
			☐ Active US military Service	
City	Stow	State/Province	Ohio	Country of Residence
				US
Mailing Address of Inventor:				
Address 1	4689 Concord Drive			
Address 2				
City	Stow	State/Province	OH	
Postal Code	44224	Country	US	

Inventor 2				
Legal Name				
Prefix	Given Name	Middle Name	Family Name	Suffix
	Russell		Fuerst	
Residence Information (Select One)	☒ US Residency		☐ Non US Residency	
			☐ Active US military Service	

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	90523-003710US-789306
	Application Number	12/858,510
Title of Invention		FORWARD ERROR CORRECTION WITH PARALLEL ERROR DETECTION FOR FLASH MEMORIES

City	Mentor	State/Province	OH	Country of Residence	US
Mailing Address of Inventor:					
Address 1	8475 Mansion Boulevard				
Address 2					
City	Mentor	State/Province	OH		
Postal Code	44060	Country	US		

Inventor 3					
Legal Name					
Prefix	Given Name	Middle Name		Family Name	Suffix
	Mark			Kohoot	
Residence Information (Select One)		☒ US Residency		☐ Non US Residency	☐ Active US military Service
City	Cleveland Heights	State/Province	OH	Country of Residence	United States of America
Mailing Address of Inventor:					
Address 1	2748 Lancashire Road				
Address 2					
City	Cleveland Heights	State/Province	OH		
Postal Code	44106	Country	US		

Inventor 4					
Legal Name					
Prefix	Given Name	Middle Name		Family Name	Suffix
	Jim			Keszenheimer	
Residence Information (Select One)		☒ US Residency		☐ Non US Residency	☐ Active US military Service

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	90523-003710US-789306
	Application Number	12/858,510
Title of Invention	FORWARD ERROR CORRECTION WITH PARALLEL ERROR DETECTION FOR FLASH MEMORIES	

City	Chagrin Falls	State/Province	OH	Country of Residence	US
Mailing Address of Inventor:					
Address 1	8025 Bainbrook				
Address 2					
City	Chagrin Falls	State/Province	OH		
Postal Code	44023	Country	US		

Inventor 5					
Legal Name					
Prefix	Given Name	Middle Name		Family Name	Suffix
	William	H.		Thesling	
Residence Information (Select One)	☒ US Residency		☐ Non US Residency		☐ Active US military Service
City	Hudson	State/Province	OH	Country of Residence	US
Mailing Address of Inventor:					
Address 1	7332 E. Firelands Drive				
Address 2					
City	Hudson	State/Province	OH		
Postal Code	44236	Country	OH		

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below.
For further information see 37 CFR 1.33(a).

☐ An Address is being provided for the correspondence Information of this application

Customer Number	61668
Email Address	ipefiling@kilpatricktownsend.com

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	90523-003710US-789306
	Application Number	12/858,510
Title of Invention	FORWARD ERROR CORRECTION WITH PARALLEL ERROR DETECTION FOR FLASH MEMORIES	

Application Information:

Title of Invention	FORWARD ERROR CORRECTION WITH PARALLEL ERROR DETECTION FOR FLASH MEMORIES		
Attorney Docket Number	90523-003710US-789306	Small Entity Status Claimed	☐
Application Type	NonProvisional		
Subject Matter	Utility		
Total Number of Drawing Sheets (if any)	7	Selected Figure for Publication (if any)	4

Publication Information:

☐	Request Early Publication (Fee required at time of Request 37 CFR 1.219)
☐	Request Not to Publish. I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application has not and will not be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32). Either enter Customer Number or complete the Representative Name section below. If both sections are completed the Customer Number will be used for the Representative Information during processing.			
Please Select One:	☒ Customer Number	☐ US Patent Practitioner	☐ Limited Recognition (37 CFR 11.9)
Customer Number	61668		

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, or 365(c) or indicate National Stage entry from a PCT application. Providing this information in the application data sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78.
--

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	90523-003710US-789306
	Application Number	12/858,510
Title of Invention	FORWARD ERROR CORRECTION WITH PARALLEL ERROR DETECTION FOR FLASH MEMORIES	

Prior Application Status:	<u>Expired</u>				
Application Number	Continuity Type	Prior Application Number	Filing Date	Patent Number	Issue Date
This application is	A Non-provisional of	61/234,911	August 18, 2009		

Foreign Priority Information:

This section allows for the applicant to claim priority to a foreign application. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55(d). When priority is claimed to a foreign application this is eligible for retrieval under the priority document exchange program (PDX) the information will be used by the Office to automatically attempt retrieval pursuant to 37 CFR 1.55(h)(1) and (2). Under the PDX program, applicant bears the ultimate responsibility for ensuring that a copy of the foreign application is received by the Office from the participating foreign intellectual property office, or a certified copy of the foreign priority application is filed, within the time period specified in 37 CFR 1.55(g)(1).

Application Number	Country	Filing Date	Access Code (if applicable)

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications

- ☐ This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to claimed invention that has an effective filing date on or after March 16, 2013.

Authorization to Permit Access:

X	Authorization to Permit Access to the Instant Application by the Participating Offices
If checked, the undersigned hereby grants the USPTO authority to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the World Intellectual Property Office (WIPO), and any other intellectual property offices in which a foreign application claiming priority to the instant patent application is filed access to the instant patent application. See 37 CFR 1.14(c) and (h). This box should not be checked if the applicant does not wish the EPO, JPO, KIPO, WIPO, or other intellectual property office in which a foreign application claiming priority to the instant patent application is filed to have access to the instant patent application. In accordance with 37 CFR 1.14(h) (3), access will be provided to a copy of the instant patent application with respect to: 1) the instant patent application-as-filed; 2) any foreign application to which the instant patent application claims priority under 35 U.S.C. 119(a)-(d) if a copy of the foreign application that satisfies the certified copy requirement of 37 CFR 1.55 has been filed in the instant patent application; and 3) any U.S. application-as-filed from which benefit is sought in the instant patent application. In accordance with 37 CFR 1.14(c), access may be provided to information concerning the date of filing this Authorization.	

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	90523-003710US-789306
	Application Number	12/858,510
Title of Invention	FORWARD ERROR CORRECTION WITH PARALLEL ERROR DETECTION FOR FLASH MEMORIES	

Applicant Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of the CFR to have an assignment recorded by the Office.			
Applicant 1			
If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section.			
☒ Assignee	☐ Legal Representative under 35 U.S.C. 117	☐ Joint Inventor	
☐ Person to whom the inventor is obligated to assign		☐ Person who shows sufficient proprietary interest	
If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:			
Name of the Deceased or Legally Incapacitated Inventor:			
If the Applicant is an Organization check here. ☒			
Organization Name:		ViaSat, Inc.	
Mailing Address Information:			
Address 1		6155 El Camino Real	
Address 2			
City		State/Province	CA
Country	US	Postal Code	92009
Phone Number		Fax Number	
Email Address			

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	90523-003710US-789306
	Application Number	12/858,510
Title of Invention	FORWARD ERROR CORRECTION WITH PARALLEL ERROR DETECTION FOR FLASH MEMORIES	

Non-Applicant Assignee Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of the CFR to have an assignment recorded by the Office.			
Assignee 1			
Complete this section only if non-applicant assignee information is desired to be included on the patent application publication in accordance with 37 CFR 1.215(b). Do not include in this section an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest), as the patent application publication will include the name of the applicant(s).			
If the Assignee is an Organization check here. ☐			
Organization Name			
Mailing Address Information for Non-Applicant Assignee:			
Address 1			
Address 2			
City		State/Province	
Country		Postal Code	
Phone Number		Fax Number	
Email Address			

Signature:

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.14 for signature requirements and certifications.					
Signature	/Mymy N. Henderson/			Date	2013-10-07
First Name	Mymy	Last Name	Henderson	Registration Number	64,975

This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.



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United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
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Alexandria, Virginia 22313-1450
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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY. DOCKET NO	TOT CLAIMS	IND CLAIMS
12/858,510	08/18/2010	2113	1480	90523-789306 (003710US)	25	3

CONFIRMATION NO. 6028

CORRECTED FILING RECEIPT



61668

KILPATRICK TOWNSEND & STOCKTON, LLP/VIASAT
VIASAT, INC. (CLIENT #017018)
TWO EMBARCADERO CENTER
8TH FLOOR
SAN FRANCISCO, CA 94111

Date Mailed: 10/24/2013

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Inventor(s)

Sameep Dave, Stow, OH;
Russell Fuerst, Mentor, OH;
Mark Kohoot, Cleveland Heights, OH;
Jim Keszenheimer, Chagrin Falls, OH;
William H. Thesling, Hudson, OH;

Applicant(s)

Sameep Dave, Stow, OH;
Russell Fuerst, Mentor, OH;
Mark Kohoot, Cleveland Heights, OH;
Jim Keszenheimer, Chagrin Falls, OH;
William H. Thesling, Hudson, OH;

Assignment For Published Patent Application

ViaSat, Inc., Carlsbad, CA

Power of Attorney: The patent practitioners associated with Customer Number 61668

Domestic Priority data as claimed by applicant

This appln claims benefit of 61/234,911 08/18/2009

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see <http://www.uspto.gov> for more information.) - None.

Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

If Required, Foreign Filing License Granted: 08/27/2010

page 1 of 3

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 12/858,510**

Projected Publication Date: Not Applicable

Non-Publication Request: No

Early Publication Request: No

Title

DETECTION

FORWARD ERROR CORRECTION WITH PARALLEL ERROR DIRECTION FOR FLASH
MEMORIES

Preliminary Class

714

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at <http://www.uspto.gov/web/offices/pac/doc/general/index.html>.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, <http://www.stopfakes.gov>. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

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Title 37, Code of Federal Regulations, 5.11 & 5.15

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The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign Assets Control, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

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The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The U.S. offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to promote and facilitate business investment. SelectUSA provides information assistance to the international investor community; serves as an ombudsman for existing and potential investors; advocates on behalf of U.S. cities, states, and regions competing for global investment; and counsels U.S. economic development organizations on investment attraction best practices. To learn more about why the United States is the best country in the world to develop technology, manufacture products, deliver services, and grow your business, visit <http://www.SelectUSA.gov> or call +1-202-482-6800.

Electronic Acknowledgement Receipt	
EFS ID:	17295039
Application Number:	12858510
International Application Number:	
Confirmation Number:	6028
Title of Invention:	FORWARD ERROR CORRECTION WITH PARALLEL ERROR DIRECTION FOR FLASH MEMORIES
First Named Inventor/Applicant Name:	Sameep Dave
Customer Number:	61668
Filer:	Mymy Nguyen Henderson/Kelly Mak
Filer Authorized By:	Mymy Nguyen Henderson
Attorney Docket Number:	90523-789306 (003710US)
Receipt Date:	01-NOV-2013
Filing Date:	18-AUG-2010
Time Stamp:	16:27:26
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
------------------------	----

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Request for Corrected Filing Receipt	Corr_FR.pdf	110978 e404457d3a9349a75eaaac3ee2f72a1e09761efe	no	2

Warnings:

Information:

2	Miscellaneous Incoming Letter	COPY.pdf	492555 b164fd90eade3e11a9c9a1d32928e1871ef a8a1	no	10
Warnings:					
Information:					
3	Miscellaneous Incoming Letter	FR.pdf	199018 2bb549b08295d4018742bfd7aadb5702c0 e06b4d	no	3
Warnings:					
Information:					
Total Files Size (in bytes):				802551	
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					



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United States Patent and Trademark Office
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Alexandria, Virginia 22313-1450
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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY. DOCKET NO	TOT CLAIMS	IND CLAIMS
12/858,510	08/18/2010	2113	1480	90523-789306 (003710US)	25	3

CONFIRMATION NO. 6028

CORRECTED FILING RECEIPT



61668

KILPATRICK TOWNSEND & STOCKTON, LLP/VIASAT
VIASAT, INC. (CLIENT #017018)
TWO EMBARCADERO CENTER
8TH FLOOR
SAN FRANCISCO, CA 94111

Date Mailed: 11/07/2013

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Inventor(s)

Sameep Dave, Stow, OH;
Russell Fuerst, Mentor, OH;
Mark Kohoot, Cleveland Heights, OH;
Jim Keszenheimer, Chagrin Falls, OH;
William H. Thesling, Hudson, OH;

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Mark Kohoot, Cleveland Heights, OH;
Jim Keszenheimer, Chagrin Falls, OH;
William H. Thesling, Hudson, OH;

Assignment For Published Patent Application

ViaSat, Inc., Carlsbad, CA

Power of Attorney: The patent practitioners associated with Customer Number 61668

Domestic Priority data as claimed by applicant

This appln claims benefit of 61/234,911 08/18/2009

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see <http://www.uspto.gov> for more information.) - None.

Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

If Required, Foreign Filing License Granted: 08/27/2010

page 1 of 3

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 12/858,510**

Projected Publication Date: Not Applicable

Non-Publication Request: No

Early Publication Request: No

Title

FORWARD ERROR CORRECTION WITH PARALLEL ERROR DETECTION FOR FLASH
MEMORIES

Preliminary Class

714

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

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Title 37, Code of Federal Regulations, 5.11 & 5.15

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The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign Assets Control, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

SelectUSA

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The U.S. offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to promote and facilitate business investment. SelectUSA provides information assistance to the international investor community; serves as an ombudsman for existing and potential investors; advocates on behalf of U.S. cities, states, and regions competing for global investment; and counsels U.S. economic development organizations on investment attraction best practices. To learn more about why the United States is the best country in the world to develop technology, manufacture products, deliver services, and grow your business, visit <http://www.SelectUSA.gov> or call +1-202-482-6800.

I hereby certify that this correspondence is being filed via
EFS-Web with the United States Patent and Trademark Office
on October 7, 2013.

PATENT
Attorney Docket No.: 90523-003710US-789306
Client Ref. No.: ECC-0407-US-2

KILPATRICK TOWNSEND & STOCKTON LLP

By: /Kelly Mak/

OK TO ENTER: /E.M./

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Sameep Dave et al.

Application No.: 12/858,510

Filed: August 18, 2010

For: FORWARD ERROR CORRECTION
WITH PARALLEL ERROR DETECTION
FOR FLASH MEMORIES

Customer No.: 61668

Confirmation No.: 6028

Examiner: Elmira Mehrmanesh

Technology Center/Art Unit: 2113

AMENDMENT AFTER ALLOWANCE
UNDER 37 CFR § 1.312

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Commissioner:

In response to the Notice of Allowance mailed August 20, 2013, please enter the
following amendments and remarks:

Amendments to the Specification begin on page 2 of this paper.

Remarks/Arguments begin on page 3 of this paper.



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UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/858,510	08/18/2010	Sameep Dave	90523-789306 (003710US)	6028

61668 7590 11/14/2013
KILPATRICK TOWNSEND & STOCKTON, LLP/VIASAT
VIASAT, INC. (CLIENT #017018)
TWO EMBARCADERO CENTER
8TH FLOOR
SAN FRANCISCO, CA 94111

EXAMINER

MEHRMANESH, ELMIRA

ART UNIT	PAPER NUMBER
2113	

NOTIFICATION DATE	DELIVERY MODE
11/14/2013	ELECTRONICELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

Patent-admin@viasat.com
ipefiling@kilpatricktownsend.com
lfitzsimmons@kilpatricktownsend.com

Response to Rule 312 Communication	Application No.	Applicant(s)
	12/858,510	DAVE ET AL.
	Examiner	Art Unit
	Elmira Mehrmanesh	2113

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

1. ☒ The amendment filed on 07 October 2013 under 37 CFR 1.312 has been considered, and has been:

a) ☒ entered.

b) ☐ entered as directed to matters of form not affecting the scope of the invention.

c) ☐ disapproved because the amendment was filed after the payment of the issue fee.
Any amendment filed after the date the issue fee is paid must be accompanied by a petition under 37 CFR 1.313(c)(1) and the required fee to withdraw the application from issue.

d) ☐ disapproved. See explanation below.

e) ☐ entered in part. See explanation below.

/JAMES KRAMER/ Supervisory Patent Examiner, Art Unit 2113	
--	--

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: **Mail** **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax **(571)-273-2885**

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

61668 7590 08/20/2013
KILPATRICK TOWNSEND & STOCKTON, LLP/VIASAT
VIASAT, INC. (CLIENT #017018)
TWO EMBARCADERO CENTER
8TH FLOOR
SAN FRANCISCO, CA 94111

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/858,510	08/18/2010	Sameep Dave	90523-789306 (003710US)	6028

TITLE OF INVENTION: FORWARD ERROR CORRECTION FOR MEMORIES

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$1780	\$300	\$0	\$2080	11/20/2013

EXAMINER	ART UNIT	CLASS-SUBCLASS
MEHRMANESH, ELMIRA	2113	714-773000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

- (1) the names of up to 3 registered patent attorneys or agents OR, alternatively,
- (2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

- 1 Kilpatrick Townsend &
- 2 Stockton LLP
- 3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

ViaSat, Inc.

Carlsbad, California

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

- ☒ Issue Fee
- ☒ Publication Fee (No small entity discount permitted)
- ☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): (**Please first reapply any previously paid issue fee shown above**)

- ☐ A check is enclosed.
- ☒ Payment by credit card. ~~Form PTO-2038 is attached.~~
- ☐ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)

☐ Applicant certifying micro entity status. See 37 CFR 1.29

☐ Applicant asserting small entity status. See 37 CFR 1.27

☐ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see form PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature /Mymy N. Henderson/

Date November 19, 2013

Typed or printed name Mymy N. Henderson

Registration No. 64,975

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Electronic Patent Application Fee Transmittal				
Application Number:		12858510		
Filing Date:		18-Aug-2010		
Title of Invention:		FORWARD ERROR CORRECTION WITH PARALLEL ERROR DETECTION FOR FLASH MEMORIES		
First Named Inventor/Applicant Name:		Sameep Dave		
Filer:		Mymy Nguyen Henderson		
Attorney Docket Number:		90523-789306 (003710US)		
Filed as Large Entity				
Utility under 35 USC 111(a) Filing Fees				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Utility Appl Issue Fee	1501	1	1780	1780
Publ. Fee- Early, Voluntary, or Normal	1504	1	300	300

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				2080

Electronic Acknowledgement Receipt	
EFS ID:	17443378
Application Number:	12858510
International Application Number:	
Confirmation Number:	6028
Title of Invention:	FORWARD ERROR CORRECTION WITH PARALLEL ERROR DETECTION FOR FLASH MEMORIES
First Named Inventor/Applicant Name:	Sameep Dave
Customer Number:	61668
Filer:	Mymy Nguyen Henderson
Filer Authorized By:	
Attorney Docket Number:	90523-789306 (003710US)
Receipt Date:	19-NOV-2013
Filing Date:	18-AUG-2010
Time Stamp:	17:23:12
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	\$ 2080
RAM confirmation Number	4953
Deposit Account	201430
Authorized User	HENDERSON, MYMY
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees) Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)	

Charge any Additional Fees required under 37 C.F.R. Section 1.19 (Document supply fees)					
Charge any Additional Fees required under 37 C.F.R. Section 1.20 (Post Issuance fees)					
Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)					
File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Issue Fee Payment (PTO-85B)	IF_789306.pdf	122213 5b1c5dababa215b91fcd4c31fbc65913b68827a4	no	2
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	31958 4bf35ec16bdb2a5b079a4d21c56e79e64dec0166	no	2
Warnings:					
Information:					
Total Files Size (in bytes):			154171		
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/858,510	12/24/2013	8615700	90523-789306 (003710US)	6028

61668 7590 12/04/2013
KILPATRICK TOWNSEND & STOCKTON, LLP/VIASAT
VIASAT, INC. (CLIENT #017018)
TWO EMBARCADERO CENTER
8TH FLOOR
SAN FRANCISCO, CA 94111

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment is 520 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site <http://pair.uspto.gov> for additional applicants):

Sameep Dave, Stow, OH;
Russell Fuerst, Mentor, OH;
Mark Kohoot, Cleveland Heights, OH;
Jim Keszenheimer, Chagrin Falls, OH;
William H. Thesling, Hudson, OH;

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The USA offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to encourage and facilitate business investment. To learn more about why the USA is the best country in the world to develop technology, manufacture products, and grow your business, visit SelectUSA.gov.

AO 120 (Rev. 08/10)

TO: Mail Stop 8 Director of the U.S. Patent and Trademark Office P.O. Box 1450 Alexandria, VA 22313-1450	REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK
---	---

In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been filed in the U.S. District Court Western District of Texas on the following

☐ Trademarks or ☒ Patents. (☐ the patent action involves 35 U.S.C. § 292.):

DOCKET NO. 6:21-cv-1230	DATE FILED 11/29/2021	U.S. DISTRICT COURT Western District of Texas
PLAINTIFF Viasat, Inc.		DEFENDANT Western Digital Corporation and Western Digital Technologies, Inc.
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1 8,615,700	12/24/2013	Viasat, Inc.
2 8,966,347	2/24/2015	Viasat, Inc.
3		
4		
5		

In the above—entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY ☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading	
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1		
2		
3		
4		
5		

In the above—entitled case, the following decision has been rendered or judgement issued:

DECISION/JUDGEMENT		
CLERK	(BY) DEPUTY CLERK	DATE

Copy 1—Upon initiation of action, mail this copy to Director Copy 3—Upon termination of action, mail this copy to Director
 Copy 2—Upon filing document adding patent(s), mail this copy to Director Copy 4—Case file copy

AO 120 (Rev. 08/10)

TO: Mail Stop 8 Director of the U.S. Patent and Trademark Office P.O. Box 1450 Alexandria, VA 22313-1450	REPORT ON THE FILING OR DETERMINATION OF AN ACTION REGARDING A PATENT OR TRADEMARK
---	---

In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been filed in the U.S. District Court Western District of Texas on the following

☐ Trademarks or ☒ Patents. (☐ the patent action involves 35 U.S.C. § 292.):

DOCKET NO. 6:21-cv-01231	DATE FILED 11/29/2021	U.S. DISTRICT COURT Western District of Texas
PLAINTIFF Viasat, Inc.		DEFENDANT Kioxia Corporation and Kioxia America, Inc.
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1 8,615,700	12/24/2013	Viasat, Inc.
2		
3		
4		
5		

In the above—entitled case, the following patent(s)/ trademark(s) have been included:

DATE INCLUDED	INCLUDED BY ☐ Amendment ☐ Answer ☐ Cross Bill ☐ Other Pleading	
PATENT OR TRADEMARK NO.	DATE OF PATENT OR TRADEMARK	HOLDER OF PATENT OR TRADEMARK
1		
2		
3		
4		
5		

In the above—entitled case, the following decision has been rendered or judgement issued:

DECISION/JUDGEMENT		
CLERK	(BY) DEPUTY CLERK	DATE

Copy 1—Upon initiation of action, mail this copy to Director Copy 3—Upon termination of action, mail this copy to Director
 Copy 2—Upon filing document adding patent(s), mail this copy to Director Copy 4—Case file copy

POWER OF ATTORNEY TO PROSECUTE APPLICATIONS BEFORE THE USPTO

I hereby revoke all previous powers of attorney given in the application identified in the attached statement under 37 CFR 3.73(b).

I hereby appoint:



Practitioners associated with the Customer Number:

31864

OR



Practitioner(s) named below (if more than ten patent practitioners are to be named, then a customer number must be used):

Name	Registration Number	Name	Registration Number

as attorney(s) or agent(s) to represent the undersigned before the United States Patent and Trademark Office (USPTO) in connection with any and all patent applications assigned only to the undersigned according to the USPTO assignment records or assignment documents attached to this form in accordance with 37 CFR 3.73(b).

Please change the correspondence address for the application identified in the attached statement under 37 CFR 3.73(b) to:



The address associated with Customer Number:

31864

OR

☐ Firm or Individual Name			
Address			
City	State	Zip	
Country			
Telephone	Email		

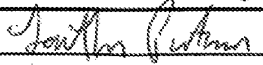
Assignee Name and Address:

VIASAT, INC.
6155 El Camino Real
Carlsbad, CA 92009

A copy of this form, together with a statement under 37 CFR 3.73(b) (Form PTO/SB/96 or equivalent) is required to be filed in each application in which this form is used. The statement under 37 CFR 3.73(b) may be completed by one of the practitioners appointed in this form if the appointed practitioner is authorized to act on behalf of the assignee, and must identify the application in which this Power of Attorney is to be filed.

SIGNATURE of Assignee of Record

The individual whose signature and title is supplied below is authorized to act on behalf of the assignee

Signature		Date	10/28/2020
Name	Jonathan Putnam	Telephone	760-893-1614
Title	Director of Patents		

This collection of information is required by 37 CFR 1.31, 1.32 and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

STATEMENT UNDER 37 CFR 3.73(b)

Applicant/Patent Owner: Sameep Dave

Application No./Patent No.: 8,615,700

Filed/Issue Date: 12-24-2013

Titled:

FORWARD ERROR CORRECTION WITH PARALLEL ERROR DETECTION FOR FLASH MEM

VIASAT, INC.

, a Corporation

(Name of Assignee)

(Type of Assignee, e.g., corporation, partnership, university, government agency, etc.)

states that it is:

1. ☒ the assignee of the entire right, title, and interest in;
2. ☐ an assignee of less than the entire right, title, and interest in
(The extent (by percentage) of its ownership interest is _____ %); or
3. ☐ the assignee of an undivided interest in the entirety of (a complete assignment from one of the joint inventors was made)

the patent application/patent identified above, by virtue of either:

- A. ☒ An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel 025064, Frame 0323, or a copy* is attached.

OR

- B. ☐ A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as follows:

1. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at
Reel _____, Frame _____, or a copy* is attached.

2. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at
Reel _____, Frame _____, or a copy* is attached.

3. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at
Reel _____, Frame _____, or a copy* is attached.

☐ Additional documents in the chain of title are listed on a supplemental sheet(s).

- ☒ *As required by 37 CFR 3.73(b)(1)(i), if a copy/copies is/are attached, the documentary evidence of the chain of title from the original owner to the assignee was, or concurrently is being, submitted for recordation pursuant to 37 CFR 3.11.

[NOTE: A separate copy (i.e., a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, to record the assignment in the records of the USPTO. See MPEP 302.]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

/Jonathan Putnam/

Signature

March 28, 2022

Date

Jonathan Putnam

Printed or Typed Name

60,102

Title or Registration Number

This collection of information is required by 37 CFR 3.73(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

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The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Acknowledgement Receipt	
EFS ID:	45344289
Application Number:	12858510
International Application Number:	
Confirmation Number:	6028
Title of Invention:	FORWARD ERROR CORRECTION WITH PARALLEL ERROR DETECTION FOR FLASH MEMORIES
First Named Inventor/Applicant Name:	Sameep Dave
Customer Number:	61668
Filer:	Jonathan Michael Putnam/Jennifer Riewald
Filer Authorized By:	Jonathan Michael Putnam
Attorney Docket Number:	90523-789306 (003710US)
Receipt Date:	29-MAR-2022
Filing Date:	18-AUG-2010
Time Stamp:	14:51:08
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Power of Attorney	220328_VS1407-US-2_POA_SB80.pdf	1073228	no	2
			310e2aa1dc50fc0e06ef31a6fa1e396d8393937b		

Warnings:

Information:					
2	Assignee showing of ownership per 37 CFR 3.73	220328_VS1407-US-2_POA_373b.pdf	185066 8f0db15604edfc243a0313f3c1c2e5fd5f263c94	no	2
Warnings:					
Information:					
Total Files Size (in bytes):			1258294		
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					



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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
12/858,510	08/18/2010	Sameep Dave	

31864
VIASAT, INC.
C/O PATENT DEPARTMENT
6155 EL CAMINO REAL
CARLSBAD, CA 92009

CONFIRMATION NO. 6028
POA ACCEPTANCE LETTER



Date Mailed: 03/31/2022

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 03/29/2022.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at (571) 272-4000 or (571) 272-4200 or 1-888-786-0101.

/nrhayden/



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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
12/858,510	08/18/2010	Sameep Dave	90523-789306 (003710US)

CONFIRMATION NO. 6028

POWER OF ATTORNEY NOTICE



OC000000132830328

61668

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Mailstop: IP Docketing - 22
1100 Peachtree Street
Suite 2800
Atlanta, GA 30309

Date Mailed: 03/31/2022

NOTICE REGARDING CHANGE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 03/29/2022.

- The Power of Attorney to you in this application has been revoked by the assignee who has intervened as provided by 37 CFR 3.71. Future correspondence will be mailed to the new address of record(37 CFR 1.33).

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at (571) 272-4000 or (571) 272-4200 or 1-888-786-0101.

/nrhayden/