

FORWARD ERROR CORRECTION FOR FLASH MEMORY

BACKGROUND OF THE INVENTION

- [0001] The present invention relates to forward error correction (FEC) in general and, in particular, to FEC for Flash Memory. The advancements of Flash Memory technology in recent years has dramatically increased storage capacity and decreased the cost of non-volatile semiconductor memory. This has made Solid State Drives (SSDs) (typically a Flash Memory based non-volatile memory system) an emerging substitute for magnetic Hard Disk Drive (HDD).
- [0002] The use of FEC to enhance the reliability and longevity of Flash Memory is one of the challenges for making SSDs perform on par with HDDs.

BRIEF DESCRIPTION OF THE DRAWINGS

- [0003] A further understanding of the nature and advantages of the present invention may be realized by reference to the following drawings. In the appended figures, similar components or features may have the same reference label. Further, various components of the same type may be distinguished by following the reference label by a dash and a second label that distinguishes among the similar components. If only the first reference label is used in the specification, the description is applicable to any one of the similar components having the same first reference label irrespective of the second reference label.

DETAILED DESCRIPTION OF THE INVENTION

- [0004] This description provides example embodiments only, and is not intended to limit the scope, applicability, or configuration of the invention. Rather, the ensuing description of the embodiments will provide those skilled in the art with an enabling description for implementing embodiments of the invention. Various changes may be made in the function and arrangement of elements without departing from the spirit and scope of the invention.
- [0005] Thus, various embodiments may omit, substitute, or add various procedures or components as appropriate. For instance, it should be appreciated that in alternative embodiments the methods may be performed in an order different from that described, and that various steps may be added, omitted, or combined. Also, features described with respect

to certain embodiments may be combined in various other embodiments. Different aspects and elements of the embodiments may be combined in a similar manner.

5 **[0006]** It should also be appreciated that the following systems, methods, and software may individually or collectively be components of a larger system, wherein other procedures may take precedence over or otherwise modify their application. Also, a number of steps may be required before, after, or concurrently with the following embodiments.

[0007] Systems, devices, methods, and software are described for FEC for Flash Memory. Although much of the following discussion relates specifically to Flash Memory, aspects of the inventions are applicable to other forms of solid state memory.

10 **[0008]** There are two basic types of Flash Memory architectures: NOR and NAND. For the purposes of this disclosure, the focus is on NAND-type Flash, while again noting that principles set forth herein have wider applicability.

15 **[0009]** There are two primary NAND Flash technologies. The earlier versions of NAND Flash were Single-Level Cell (SLC). With SLC Flash, there is only one programmed state in addition to the erased state. The total of two states allows a single data bit to be stored in the memory cell. The desire for higher density led to the more advanced Multiple-Level Cell (MLC). With MLC flash, there are multiple programmed states in addition to the erased state which allows multiple bits to be stored per memory cell.

20 **[0010]** Because of this increase in density and the related issues in manufacturing, one of the challenges for Flash Memory is to maintain high reliability and longevity. The deterioration of the oxide over time, and the disruptions from neighboring memory pages, can lead to data retention and corruption issues translating into bit errors. While the chances of any given data bit being corrupted is quite small, the vast number of data bits in a storage system makes the likelihood of data corruption a very real possibility. FEC may be one of
25 the tools used to address these bit errors to improve the reliability and lifespan of Flash Memory.

[0011] FEC may be used with Flash. The first step in this direction is the use of error detection codes that detect and flag bit errors. This may allow a Flash management device to filter out segments of memory that are erroneous and start replacing such segments with
30 replacements from a pool of available substitutes.

[0012] As Flash Memories become more dense, the inherent bit error probability becomes higher. Some simple FEC coding may be used to clean up these errors.

[0013] The Hamming Code, with correction capacity of 1 bit and detection capability of 2, may be used with Flash. With the desire for improving the performance, as well as the increased probability of inherent bit errors because of the denser memories, Bose Chaudhuri Hocqunghem (BCH) codes may be used, including the binary BCH and non-binary BCH (Reed Solomon (RS)) codes. These codes offer a higher correction capacity in comparison to the Hamming Code.

[0014] FIG. 1 shows a graph 100 illustrating the performance advantages of a variety of BCH class FEC codes. As more and more redundancy is added, the correction capacity improves and allows the code to drive an inherent high input bit-error probability to a low decoded error rate.

[0015] BCH encoding/decoding architectures may be the foundation of error correction in Flash, with the use of higher correction capacity as desired. But as we have learned from satellite communications, there are more advanced coding options that can provide better performance compared to BCH codes. These codes may be used for the FEC needs of Flash Memory as its density and performance demands increase. These advanced FEC codes include: Convolutional Turbo Codes (CTCs), Turbo Product Codes (TPCs), and Low Density Parity Check Codes (LDPCs).

[0016] These state-of-the-art codes perform very close to the theoretical limits (Shannon Limits) of error correction, providing the highest possible coding gain or improvement in Bit Error Rate (BER) performance for a given amount of redundancy. To fully appreciate what this means for Flash Memory reliability and longevity, it may be useful to derive the impact of these code on both.

[0017] As discussed previously, Flash Memory does have an inherent probability of error. Depending on the Flash Technology, this error rate is somewhere between 1e-5 and 1e-8. To be able to match the HDD read/write bit error rate of 1e-15 is required. As seen from Figure 1, low error correction BCH codes can help meet this reliability requirement for certain low inherent error rates.

[0018] The measure of how good a job a code can perform in increasing the reliability depends upon its correction capacity. If the probability of bit error for a Flash is p and the correction capacity of the code is t bits over a codeword length of n bits, the probability of making an error is

$$P_{\text{decoded}} = \sum_{i=t+1}^n p^i * (1-p)^{n-i} \quad (1)$$

[0019] From equation (1), for a given p the higher the correction capacity of the code, the smaller the probability of error after the decoding will be. The correction capacity can be expressed as the number of bits a code can correct over a codeword length, or an input BER, or probability of error that it can take down to a certain target decoded BER (as in FIG. 1).

5 The advanced ECCs can correct more errors over a certain length or take a higher input BER to the same decoded BER. As an example, FIG. 2 is a graph 200 shows the performance of a BCH class code with the same overhead (OH) compared to an advanced code. As the figure shows, the advanced code can take 10x the input BER to reach the same decoded BER. What this means is that for a given input error rate the advanced codes can drive the decoded error
10 rate to much lower leading to much higher reliability. Also, to get to the same reliability, the advanced codes can tolerate much higher input error rate which means they could increase the yields of Flash and are certainly more suited to higher level MLCs (which are more erroneous).

[0020] There is incentive to use advanced codes for Flash even with not so dense
15 memories. If the inherent error performance of Flash Memory stayed at a certain low level, there would probably be decreased need for advanced codes. But, in practice, Flash performance tends to degrade over time. The inherent error rate thus gradually increases with use as shown in the graph 300 of FIG. 3. This means that even with an advanced code to help improve the reliability of a Flash, over time the Flash may become lossy and, once the
20 error rate is high enough, it will be beyond repair by the code being used. Once this happens, the Flash may become unusable.

[0021] The solid lines in FIG. 3 depict three different profile samples of how a flash could degrade over time. These are: Linear, Exponential and Sudden-change. The two dotted lines indicate some error threshold values that two different ECCs can tolerate to get a satisfactory
25 decoder error rate. The x-axis on the plot is some abstract unit of time and the y-axis is some abstract unit of error rate. As can be seen from FIG. 3, the stronger code can tackle 1.6x higher error rate results in increasing the usability life-span of the Flash by 100% in the Linear profile, 50% in the Exponential profile and < 5 % in the Sudden-change profile. The impact of advanced FEC on the longevity of a Flash may depend upon the error rate profile
30 over time. Using an estimated profile of how the error rate changes over time allows a more accurate analysis of the impact of advanced codes. Also, code design may be tailored to suit the Flash Memory architecture for maximum performance benefits.

[0022] Flash Memory is often partitioned into a pool of small fixed-size sectors, and FEC is applied on a sector by sector basis. The Flash size may be defined by the number of sectors

that the Flash contains. As there is a chance of sectors going bad over time, there is a reserve/spare sector pool that allows Flash management tools to replace the bad sectors by the spares as needed to extend the life of the Flash.

[0023] A wear leveling technique may used by the Flash Management devices to make sure that various areas/sectors of the Flash “age” at a similar rate. Instead of the same sector being used over and over again, the read/writes are spread over much or the entire flash. And this translates into the probability of any sector being good (p_{good}) may be substantially the same for the various sectors in a Flash. If the size of the Flash is N sectors and there are Δ spare sectors, the probability that the Flash is still usable after time t is:

$$p_{usable} = \sum_{i=N}^{N+\Delta} (C_i^{N+\Delta} * (p_{good})^i * (1 - p_{good})^{N+\Delta-i}) \quad (2)$$

[0024] p_{good} may be a function of use time for a Flash sector. This is a component that is dependent upon the correction capacity of the code used. And so even with the spare sectors and the wear-leveling technique, the codes play a key role in the Flash being usable after a certain use time.

[0025] Given that the codes may have very steep performance curves, the p_{good} and p_{usable} should result in sharp curves as shown in the graph 400 of **FIG. 4**. The realistic profile of how the error rate changes over time and what percentage of spares are usually employed may be ascertained, and thus an accurate analysis may be made of how p_{good} and p_{usable} would vary over time. The one fact that would remain is that the advanced FECs may push the knee of this curve where it goes from usable to unusable much further out in time.

[0026] This analysis shows how better code selection for Flash may help improve the reliability as well as life-span of Flash Memories. This may result in one or more of the following: increased reliability of read/write, increased lifespan of the sectors before they have to retire, increased lifespan of the flash with the same spare overhead, reduced spare requirements to achieve the same lifespan, and increased yield for MLC by covering up inherent faults.

[0027] One of the concerns regarding advanced codes is how they fit into the sector sizes and OH requirements of Flash. TPC and LDPC codes offer a great degree of freedom in selecting the various code parameters like information block size, coded blocksize, and correction capacity, and would allow customization to suit any Flash configuration.

[0028] Another concern regarding advanced codes is that the implementation complexity may be especially high at very high speeds as desired for newer Flash Memories. With the increasing sophistication and densities of Flash Memory, the role of FEC becomes increasingly important.

5 **[0029]** It should be noted that the methods, systems, and devices discussed above are intended merely to be examples. It must be stressed that various embodiments may omit, substitute, or add various procedures or components as appropriate. For instance, it should be appreciated that, in alternative embodiments, the methods may be performed in an order different from that described, and that various steps may be added, omitted, or combined.

10 Also, features described with respect to certain embodiments may be combined in various other embodiments. Different aspects and elements of the embodiments may be combined in a similar manner. Also, it should be emphasized that technology evolves and, thus, many of the elements are examples and should not be interpreted to limit the scope of the invention.

[0030] Specific details are given in the description to provide a thorough understanding of the embodiments. However, it will be understood by one of ordinary skill in the art that the embodiments may be practiced without these specific details. For example, well-known circuits, processes, algorithms, structures, and techniques have been shown without unnecessary detail in order to avoid obscuring the embodiments.

20 **[0031]** Also, it is noted that the embodiments may be described as a process which is depicted as a flow diagram or block diagram. Although each may describe the operations as a sequential process, many of the operations can be performed in parallel or concurrently. In addition, the order of the operations may be rearranged. A process may have additional steps not included in the figure.

25 **[0032]** Moreover, as disclosed herein, the term "memory" or "memory unit" may represent one or more devices for storing data, including read-only memory (ROM), random access memory (RAM), magnetic RAM, core memory, magnetic disk storage mediums, optical storage mediums, flash memory devices, or other computer-readable mediums for storing information. The term "computer-readable medium" includes, but is not limited to, portable or fixed storage devices, optical storage devices, wireless channels, a sim card, other smart
30 cards, and various other mediums capable of storing, containing, or carrying instructions or data.

[0033] Furthermore, embodiments may be implemented by hardware, software, firmware, middleware, microcode, hardware description languages, or any combination thereof. When

implemented in software, firmware, middleware, or microcode, the program code or code segments to perform the necessary tasks may be stored in a computer-readable medium such as a storage medium. Processors may perform the necessary tasks.

5 **[0034]** Having described several embodiments, it will be recognized by those of skill in the art that various modifications, alternative constructions, and equivalents may be used without departing from the spirit of the invention. For example, the above elements may merely be a component of a larger system, wherein other rules may take precedence over or otherwise modify the application of the invention. Also, a number of steps may be undertaken before, during, or after the above elements are considered. Accordingly, the above description
10 should not be taken as limiting the scope of the invention.

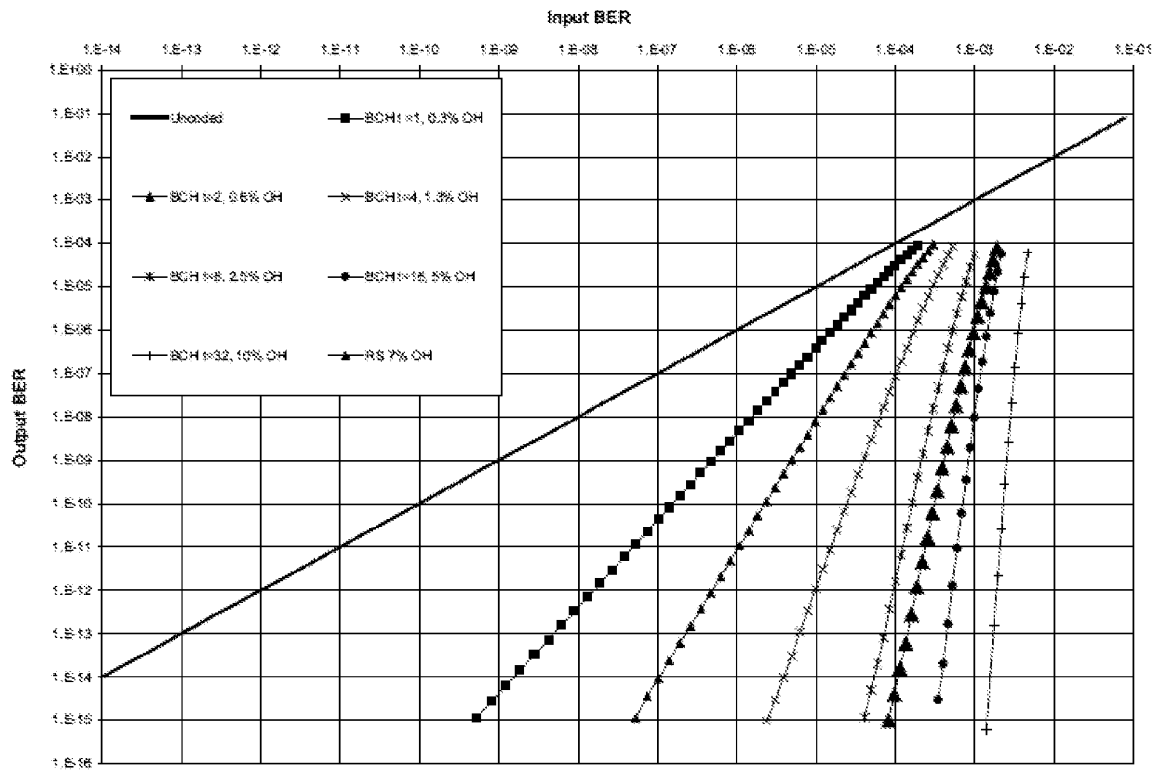
WHAT IS CLAIMED IS:

- 1 1. 1. A system, method, or device as set forth in the Specification
- 2 and/or the Drawings.

ABSTRACT OF THE DISCLOSURE

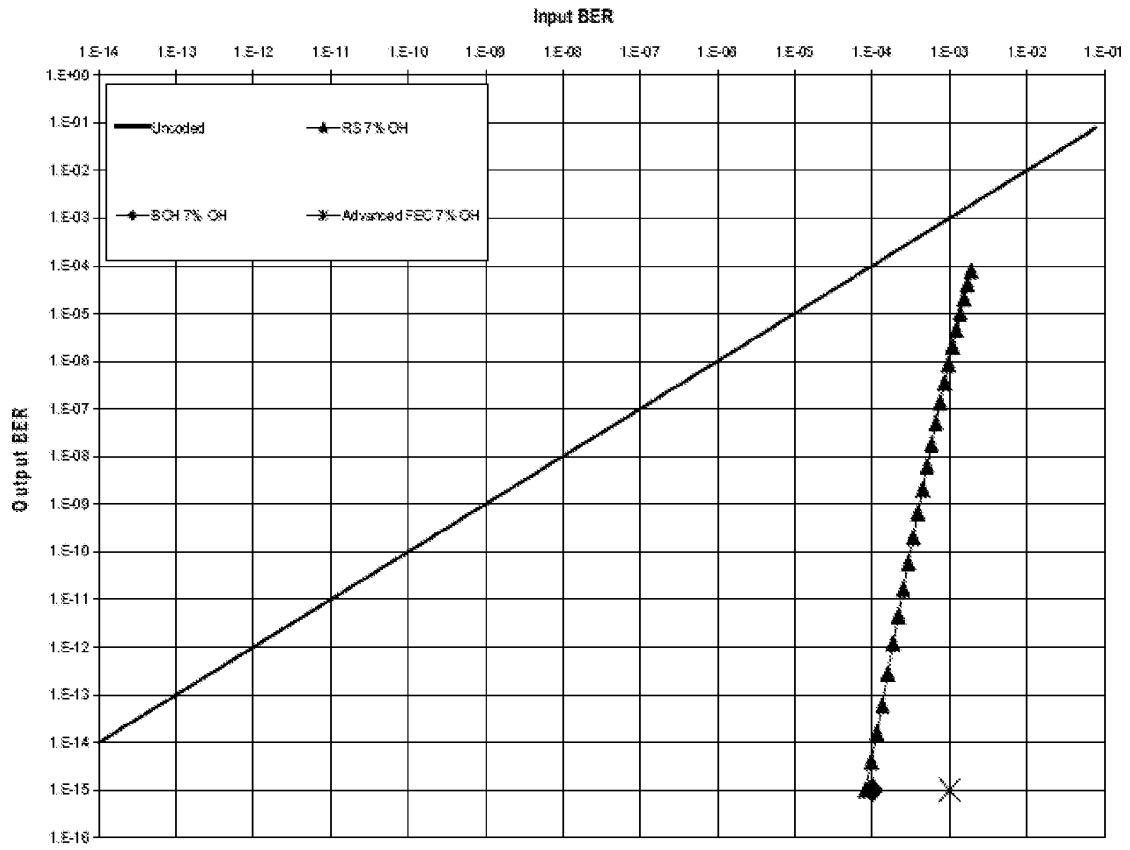
Methods, systems, and devices are described for forward error correction for Flash Memory.

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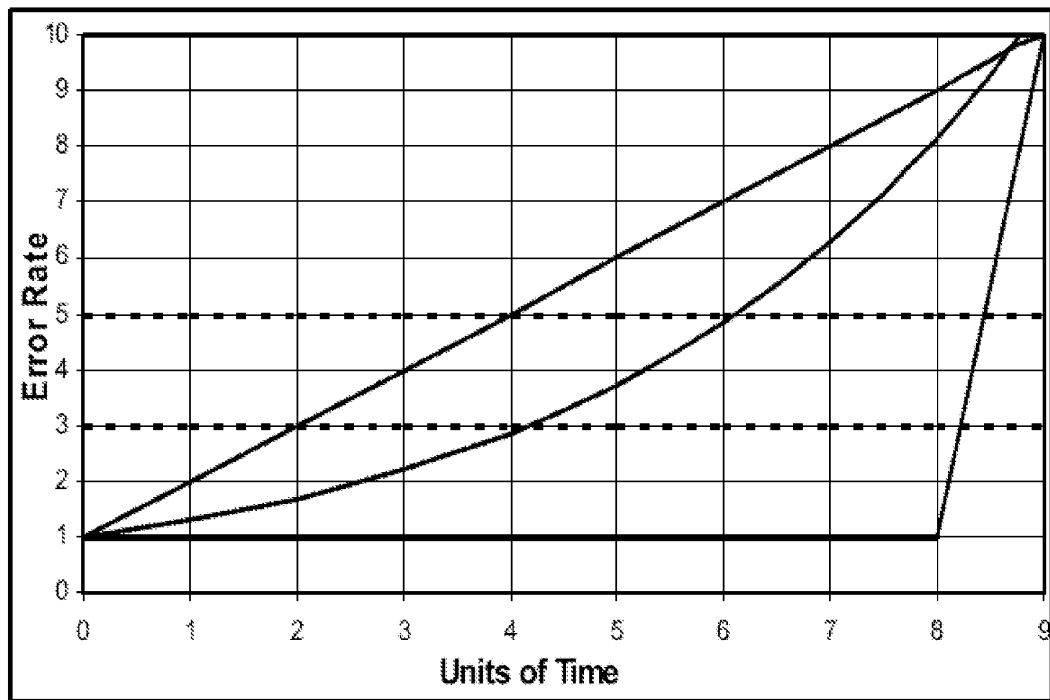
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FIG. 1



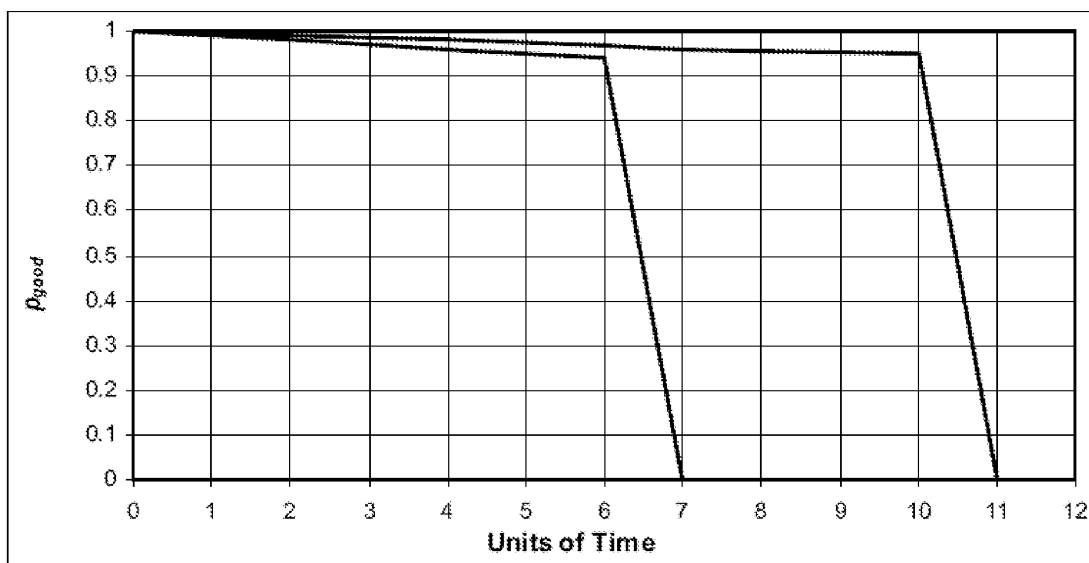
200

FIG. 2



300

FIG. 3



400

FIG. 4



Application Data Sheet

Application Information

Application number::
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Correspondence Information

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PROVISIONAL APPLICATION FOR PATENT COVER SHEET — Page 1 of 2

This is a request for filing a PROVISIONAL APPLICATION FOR PATENT under 37 CFR 1.53(c).

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<i>Additional inventors are being named on the _____ separately numbered sheets attached hereto</i>		
TITLE OF THE INVENTION (500 characters max)		
FORWARD ERROR CORRECTION FOR FLASH MEMORY		
Direct all correspondence to: CORRESPONDENCE ADDRESS ☒ The address corresponding to Customer Number: 61668 OR ☐ Firm or ☐ Individual Name Address City State Zip Country Telephone Email		
ENCLOSED APPLICATION PARTS (check all that apply)		
☒ Application Data Sheet. See 37 CFR 1.76 ☐ CD(s), Number of CDs _____ ☒ Drawing(s) Number of Sheets <u>4</u> ☐ Other (specify) _____ ☒ Specification (e.g., description of the invention) Number of Pages <u>9</u>		
Fees Due: Filing fee of \$220 (\$110 for small entity). If the specification and drawings exceed 100 sheets of paper, an application size fee is also due, which is \$270 (\$135 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).		
METHOD OF PAYMENT OF THE FILING FEE AND APPLICATION SIZE FEE FOR THIS PROVISIONAL APPLICATION FOR PATENT		
☐ Applicant claims small entity status. See 37 CFR 1.27. 220 ☐ A check or money order made payable to the <i>Director of the United States Patent and Trademark Office</i> is enclosed to cover the filing fee and application size fee (if applicable). TOTAL FEE AMOUNT (\$) ☐ Payment by credit card. Form PTO-2038 is attached. ☒ The Director is hereby authorized to charge the filing fee and application size fee (if applicable) or credit any overpayment to Deposit Account Number: <u>20-1430</u>		

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PROVISIONAL APPLICATION COVER SHEET
Page 2 of 2

PTO/SB/16 (12-08)

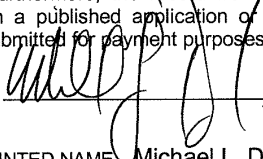
The invention was made by an agency of the United States Government or under a contract with an agency of the United States Government.

☒ No

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SIGNATURE 

Date August 18, 2009

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Electronic Patent Application Fee Transmittal				
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Title of Invention:		FORWARD ERROR CORRECTION FOR FLASH MEMORY		
First Named Inventor/Applicant Name:		Russell Fuerst		
Filer:		Michael L. Drapkin/Stephanie Klepp		
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First Named Inventor/Applicant Name:	Russell Fuerst
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Filer:	Michael L. Drapkin/Stephanie Klepp
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Attorney Docket Number:	026258-003700US
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Deposit Account	201430
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees) Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)	

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File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		026258_003700US_Application.pdf	116022 a1fd8db4d78fa93095ba32b2dfc0b178e912f7e	yes	9
	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Specification		1	7	
	Claims		8	8	
	Abstract		9	9	
Warnings:					
Information:					
2	Drawings-only black and white line drawings	026258_003700US_Drawings.pdf	102831 7d665271efdb2bbba6a0c332749b0ac41ec8c1ce	no	4
Warnings:					
Information:					
3	Application Data Sheet	026258_003700US_ADS.pdf	55873 5903a4eb742a7cc525f85b457ad33c5cc3419557	no	4
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Information:					
This is not an USPTO supplied ADS fillable form					
4	Provisional Cover Sheet (SB16)	026258_003700US_Provisional_Cover_Sheet.pdf	96826 97a1038c81405bce040ef360652550122ea33c70	no	2
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New Applications Under 35 U.S.C. 111

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National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Supplemental Application Data Sheet

Application Information

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Representative Information

Representative Number:: 61668

Domestic Priority Information

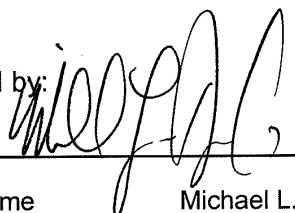
Application:: Continuity Type:: Parent Application:: Parent Filing Date::

Foreign Priority Information

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Country of mailing address:: US
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Submitted by: 
Signature _____ Date September 3, 2009
Printed Name Michael L. Drapkin Registration Number 55,127

Electronic Acknowledgement Receipt	
EFS ID:	6014441
Application Number:	61234911
International Application Number:	
Confirmation Number:	7148
Title of Invention:	FORWARD ERROR CORRECTION FOR FLASH MEMORY
First Named Inventor/Applicant Name:	Russell Fuerst
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Filer:	Michael L. Drapkin/Stephanie Klepp
Filer Authorized By:	Michael L. Drapkin
Attorney Docket Number:	026258-003700US
Receipt Date:	03-SEP-2009
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Application Type:	Provisional

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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Application Data Sheet	026258_003700US_SADS.pdf	115410 71772699f8ce9f4df290e1ea25951de6cc5c1b41	no	4

Warnings:

Information:

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115410

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If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY. DOCKET NO	TOT CLAIMS	IND CLAIMS
61/234,911	08/18/2009		220	026258-003700US		

CONFIRMATION NO. 7148

FILING RECEIPT



61668
TOWNSEND AND TOWNSEND AND CREW LLP
VIASAT, INC. (CLIENT #017018)
TWO EMBARCADERO CENTER
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Date Mailed: 09/08/2009

Receipt is acknowledged of this provisional patent application. It will not be examined for patentability and will become abandoned not later than twelve months after its filing date. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Applicant(s)

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Michael Drapkin--55127

If Required, Foreign Filing License Granted: 09/02/2009

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 61/234,911**

Projected Publication Date: None, application is not eligible for pre-grant publication

Non-Publication Request: No

Early Publication Request: No

Title

FORWARD ERROR CORRECTION FOR FLASH MEMORY

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same

page 1 of 3

effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

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