

**IN THE UNITED STATES DISTRICT COURT
WESTERN DISTRICT OF TEXAS
WACO DIVISION**

VIASAT, INC.,

Plaintiff,

vs.

**KIOXIA CORPORATION and KIOXIA
AMERICA, INC.,**

Defendants.

Case No. 6:21-cv-1231

VIASAT, INC.,

Plaintiff,

vs.

**WESTERN DIGITAL TECHNOLOGIES,
INC.,**

Defendant.

Case No. 6:21-cv-1230

DEFENDANTS' PRELIMINARY INVALIDITY CONTENTIONS

Pursuant to the May 10, 2022, Scheduling Order (Dkt. No. 39 in Case No. 6:21-cv-1231 (“the 1231 Action”); Dkt No. 43 in Case No. 6:21-cv-1230 (“the 1230 Action”)) and the Court’s default Order Governing Proceedings, Defendants Kioxia Corporation and Kioxia America, Inc. (together, “Kioxia”) and Western Digital Technologies, Inc. (“Western Digital”)¹ (collectively,

¹ Plaintiff Viasat, Inc. and Defendant Western Digital Corporation have stipulated to the dismissal of Western Digital Corporation in the 1230 Action.

“Defendants”) respectfully set forth their preliminary invalidity contentions for the asserted claims of the patents-in-suit, U.S. Patent Nos. 8,615,700 and 8,966,347.²

Defendants’ invalidity contentions address the following claims of the patents-in-suit, which are the claims currently asserted by Plaintiff ViaSat, Inc. (“Viasat” or “Plaintiff”) according to its Preliminary Infringement Contentions of April 15, 2022, against one or more Defendants:

Asserted Patent	Claims
U.S. Patent No. 8,615,700	1–25
U.S. Patent No. 8,966,347	1–11, 13–23

To the extent that Defendants’ invalidity contentions rely on or otherwise embody particular constructions of terms or phrases in the asserted claims, Defendants are not proposing any such constructions as proper constructions of those terms or phrases at this time. The Court established separate deadlines for the parties’ proposed claim constructions, and Defendants will disclose their proposed constructions according to those deadlines. For purposes of these invalidity contentions, Defendants may apply alternative claim construction positions, without conceding such constructions are proper, and will generally apply the broadest conceivable constructions of each term or phrase. In particular, certain of these invalidity contentions may be based on claim constructions that appear to underlie Viasat’s infringement contentions. Defendants, however, do not concede that Viasat’s apparent constructions are proper, reserve the right to contest any such constructions, and reserve the right to respond to alternative constructions proposed by (or indicated by) Viasat. Moreover, Defendants do not admit that any accused product, method, or

² As set forth herein, although Defendants are submitting together their Preliminary Invalidity Contentions, only certain claims of the ’700 patent have been asserted against Kioxia (*i.e.*, claims 1, 2, 3, 15, 17, 18) and Viasat has not asserted any claim of the ’347 patent against Kioxia. Accordingly, Kioxia joins these contentions only as to those claims specifically asserted against Kioxia.

service, or any of Defendants' other products, methods, or services, infringe any of the asserted claims. Nothing stated herein shall be treated as an admission or suggestion regarding either the scope of any of the asserted claims or that any of the accused technology meets any limitations of the asserted claims.

Nothing stated herein shall be construed as an admission or a waiver of any particular construction of any claim term. Moreover, the use of terms herein from the patents-in-suit should not be understood to mean that such terms as used in the patents-in-suit or claims thereof are definite or otherwise comply with 35 U.S.C. § 112. Likewise, the use of terms herein from the patents-in-suit should not be understood to suggest or imply a common, usual, ordinary, customary, plain, or accepted meaning in the art for any such term.

Defendants have, in the attached appendices, identified where the prior art references disclose subject matter recited in preambles of the asserted claims, without regard to whether the preambles are properly considered to be limitations of the asserted claims. Defendants reserve the right to argue that the preambles are or are not limitations during the claim construction proceedings in this case.

Defendants' invalidity contentions are based on their current knowledge of the patents-in-suit, the prior art, Viasat's infringement contentions, and upon information presently and reasonably available to Defendants. This litigation is in the early stages and Defendants' investigation of the prior art is ongoing. Defendants reserve the right to supplement, amend, modify, revise, or correct any aspect of their invalidity contentions, and to provide additional information as such information becomes available through discovery or otherwise. In particular, Defendants reserve the right to supplement their invalidity contentions as discovery continues and after the Court's claim construction rulings.

Defendants reserve the right to supplement their invalidity contentions should Viasat subsequently attempt to amend its disclosures in any way, or to otherwise modify their infringement allegations against Defendants or seek to establish an earlier date of invention (while reserving all rights to challenge any attempt by Viasat to do so). Defendants identify obviousness combinations below and, to the extent Plaintiff alleges that a reference does not disclose or teach a specific element, Defendants specifically identify which references render that element obvious as well as reasons to combine such references.

I. U.S. PATENT NO. 8,615,700 - INVALIDITY UNDER 35 U.S.C. §§ 102 AND 103

The asserted claims of U.S. Patent No. 8,615,700 (the “’700 Patent”) are invalid as anticipated by the prior art under various subsections of 35 U.S.C. § 102 and/or as obvious in view of the prior art under 35 U.S.C. § 103.

A. Identification of Prior Art

The charts attached as appendices to these invalidity contentions set forth how prior art identified by Defendants anticipates either expressly or inherently, and/or renders obvious, each asserted claim. Defendants cite the most relevant portions of the identified prior art references. However, other portions of the identified prior art may additionally anticipate, either expressly or inherently, and/or render obvious one or more of the asserted claims.

Where Defendants cite a particular drawing or figure in the accompanying charts, the citation encompasses the description of the drawing or figure, as well as any text associated with the drawing or figure (even if the associated text is not itself expressly cited). Similarly, where Defendants cite particular text concerning a drawing or figure in the accompanying charts, the citation encompasses that drawing or figure as well (even if the associated drawing or figure is not expressly cited). Defendants further incorporate by reference the prior art references cited in the patents-in-suit, any patents or patent applications related to the patents-in-suit, and any patent or

patent application sharing a common inventor with the patents-in-suit. This includes without limitation those identified in any other proceeding involving the patents-in-suit or related U.S. or foreign patents. Defendants additionally incorporate by reference all prior art produced or otherwise known to Plaintiff and all prior art known to the named inventor, any past or current owner, or any individual substantively involved in the prosecution of the patents-in-suit.

Defendants contend that at least some of the systems and products disclosed in one or more of the prior art references identified here or in the attached exhibits are prior art under 35 U.S.C. §§ 102(a), (b), (e), (f) and/or (g), and/or 103. Defendants' reference to any particular component, device, machine, or other product herein should also be interpreted as a reference to the product itself and any corresponding patents, publications, or product literature cited here or in the attached exhibits that relate to the cited component, device, machine, or other product. Defendants do not yet have complete information regarding the dates by which some of the cited products were publicly disclosed, used, sold, or offered for sale, the circumstances under which the research, design, and development activities were conducted, and the identities of the particular individuals involved in such activities through publicly available patents, publications, and product literature. Defendants anticipate that the actual dates, circumstances, and identities of individuals will be the subject of third-party discovery during this lawsuit.

It is understood that a person of ordinary skill in the art reads a prior art reference as a whole and in the context of other publications, literature, and general knowledge in the field. To understand and interpret any specific statement or disclosure in a prior art reference, a person of ordinary skill in the art also relies upon other information including other publications and general scientific, engineering or other relevant knowledge. Defendants reserve the right to rely upon the general scientific, engineering or other relevant knowledge in the field in interpreting the

disclosure of the prior art references. In addition, Defendants reserve the right to rely upon other publications and on expert testimony to provide context and to aid in the understanding of the prior art references. Defendants also reserve the right to rely upon other portions of the prior art references, other publications, and the testimony of experts to establish that the alleged inventions would have been obvious to a person of ordinary skill in the art, including the basis for modifying or combining the prior art references. Furthermore, Defendants reserve the right to rely upon any admissions relating to prior art found in the intrinsic evidence for the '700 Patent.

Certain pieces of identified prior art inherently disclose features of the asserted claims. Defendants may rely on inherency to demonstrate the invalidity of the asserted claims. Moreover, certain prior art references and solutions may inherently anticipate certain features of the asserted claims as construed by Viasat. Defendants may rely on other portions of the prior art, other documents, and expert testimony to establish the inherency of certain features of the prior art to invalidate the asserted claims. Defendants also may rely on any reference identified in these invalidity contentions or any other reference to prove that the references are enabled or to explain the meaning of a term used in the solutions or any reference.

1. Prior Art Patents and Publication References

The table below lists prior art patents, patent applications, and patent publications that describe the state of the art and/or render the Asserted Claims invalid under 35 U.S.C. §§ 102 and/or 103. Each listed reference became prior art at least as early as the dates provided on the face of the document. Defendants reserve the right to rely upon earlier dates of publication or public availability to the extent such information is uncovered during discovery.

Author/Inventor	Title	Date	Patent/ Application Number	Short Name
Ronald James Chapman; Ariel Brent, Christensen; Carl Evan Jones; Sushama Mahesh Paranjape	MULTI-BIT ERROR CORRECTION SYSTEM	4/2/2002	US 6,367,046 B1	Chapman et al
Jin-Yub Lee	SEMICONDUCTOR MEMORY DEVICE WITH AN ON-CHIP ERROR CORRECTION CIRCUIT AND A METHOD FOR CORRECTING A DATA ERROR THEREIN	1/21/2003	US 6,510,537 B1	Lee
Eiji Kobayashi	DEVICE, DATA SECTOR, METHOD OF PROCESSING DATA, AND SIGNAL-BEARING MEDIUM EMBODYING PROGRAM OF DEVICE	12/14/2006	US 2006/0282754 A1	Kobayashi
Xueshi YANG	METHODS, APPARATUSES, SYSTEMS, AND ARCHITECTURES FOR QUICKLY AND RELIABLY ENCODING AND/OR DECODING SYSTEM DATA	1/14/2010 (7/10/2009; 7/14/2008)	US 2010/0011275 A1	Yang
Ju-peng Chen	DUAL MODE ERROR CORRECTION CODE (ECC) APPARATUS FOR FLASH MEMORY AND METHOD THEREOF	4/22/2010 (10/16/2008)	US 2010/0100797 A1	Chen
Angelo Visconti	STRUCTURE AND METHOD FOR DETECTING ERRORS IN A MULTILEVEL	1/13/2009 (12/18/2003)	US 7,478,292 B2	Visconti

	MEMORY DEVICE WITH IMPROVED PROGRAMMING GRANULARITY			
Aaron K. Olbrich; Douglas A. Prins	PATROL FUNCTION USED IN FLASH STORAGE CONTROLLER TO DETECT DATA ERRORS	8/14/2012 (4/8/2008; 12/27/2007)	US 8,245,101 B2	Olbrich et al.
Namphil JO	MULTI-CHANNEL MEMORY SYSTEM INCLUDING ERROR CORRECTION DECODER ARCHITECTURE WITH EFFICIENT AREA UTILIZATION	3/5/2009 (8/27/2008)	US 2009/0063934 A1	JO (934)
Akira Yamaga	SEMICONDUCTOR STORAGE DEVICE, METHOD OF CONTROLLING THE SAME, AND ERROR CORRECTION SYSTEM	12/27/2011 (8/11/2010; 9/19/2008) 9/3/2009	US 8,086,933 B2 WO 2009/107267	Yamaga (933)
Yong June Kim; Jae Hong Kim; Jun Jin Kong	MEMORY DEVICES AND ENCODING AND/OR DECODING METHODS	10/2/2012 (2/27/2009)	US 8,281,217 B2	Kim et al.
Ju-Hyung Hong; Kwang-Seok Im	ECC CONTROL CIRCUITS, MULTI-CHANNEL MEMORY SYSTEMS INCLUDING THE SAME, AND RELATED METHODS OF OPERATION	2/12/2013 (8/21/2008)	US 8,375,257 B2	Hong et al.
Jun Kitahara; Nagamasa Mizushima	METHOD OF CORRECTING ERROR OF FLASH MEMORY DEVICE, AND, FLASH MEMORY DEVICE AND STORAGE SYSTEM USING THE SAME	12/17/2013 (2/2/2008)	US 8,612,830 B2	Kitahara et al.

NIEUWLAND, Andre, K.	DATA COMMUNICATION MODULE PROVIDING FAULT TOLERANCE AND INCREASED STABILITY	9/22/2005	WO 2005/088467 A1	NIEUWLAND
Masaru Uya	COMPLEMENTARY CHANNELTYPE MOS TRANSISTOR EXCLUSIVE OR/NOR LOGIC GATE CIRCUIT	11/22/83	US 4,417,161	Uya
Roderick J. Fletcher	INTEGRATED CIRCUIT HAVING OUTPUTS CONFIGURED FOR REDUCED STATE CHANGES	5/19/87	US 4,667,337	Fletcher
Erik A. de la Iglesia; Pochang Hsu; Rajendra M. Abhyankar; Siripong Sritanyaratana	BUS POWER SAVINGS USING SELECTIVE INVERSION IN AN ECC SYSTEM	12/3/2002	US 6,490,703 B1	de la Iglesia et al.
Kenneth Kay Smith	DYNAMIC VARIABLE- LENGTH ERROR CORRECTION CODE	11/1/2005	US 6,961,890 B2	Smith
Jaehong Kim; Yong June Kim; Junjin Kong; Seung-Hwan Song	DATA PROCESSING SYSTEM HAVING ECC ENCOOING AND DECODING CIRCUITS THEREN WITH CODE RATE SELECTION BASED ON BITERROR RATE DETECTION	9/23/2010 (3/3/2010)	US 2010/0241928 A1	Kim et al.
Robert C Chang; Bahman Qawami; Farshid Sabet- Sharghi	HYBRID IMPLEMENTATION FOR ERROR CORRECTION CODES WITHIN A NON- VOLATILE MEMORY SYSTEM	4/2/2013 (10/2/2003)	US 8,412,879 B2	Chang et al.

Bruce A. Wilson; Jorge Campello de Souza; Mario Blaum; Ivana Djurdjevic; Jihoon Park	ERROR CONTROL IN A FLASH MEMORY DEVICE	7/3/2012 (8/22/2008)	US 8,213,229 B2	Wilson et al.
Charles C. Lee; I- Kang Yu; Abraham Chih- Kang Ma; Ming- Shiang Shen	DATA ERROR DETECTION AND CORRECTION IN NON- VOLATILE MEMORY DEVICES	1/4/2011 (7/1/2008)	US 7,865,809 B1	Lee et al.
Shinichi Kanno	SEMICONDUCTOR MEMORY DEVICE AND ITS CONTROL METHOD	3/1/2011 (3/10/2009)	US 7,900,117 B2	Kanno
Jaekyun Moon Jihoon Park	ERROR DETECTION AND CORRECTION USING ERROR PATTERN CORRECTING CODES	6/19/2008	US 2008/0148129 A1	Moon et al.
Yong-Tae YIM	ERROR CORRECTION CIRCUIT AND METHOD FOR REDUCING MSCORRECTION PROBABILITY AND SEMICONDUCTOR MEMORY DEVICE INCLUDING THE CIRCUIT	7/3/2008	US 2008/0163033 A1	YIM
Hui Liu	METHOD AND SYSTEM FOR IMPROVING MEMORY INTERFACE DATA INTEGRITY IN PLDS	9/5/2006	US 7,102,544 B1	Liu
Maurizio Skerlj	APPARATUS AND METHOD FOR GENERATING A TRANSMIT SIGNAL AND APPARATUS AND METHOD FOR EXTRACTING AN ORIGINAL MESSAGE	2/14/2012 (11/29/2007)	US 8,117,526 B2	Skerlj

	FROM A RECEIVED SIGNAL			
Steven Shrader; Anujan Varma; Mohit Mittal	METHOD AND APPARATUS FOR PARALLEL ECC ERROR LOCATION	6/12/2012 (7/9/2008)	US 8,201,058 B2	Shrader et al.
Hiroshi Suzuki; Alan Y. Kwentus; Stephen Edward Kraft; Kevin M. Eddy; Steven T. Jaffe	FEC (FORWARD ERROR CORRECTION) DECODER WITH DYNAMIC PARAMETERS	6/23/2005	US 2005/0138521 A1	Suzuki et al.
Menahem Lasser; Avraham Meir	ERROR CORRECTION FOR NON-VOLATILE MEMORY	1/22/2004	US 2004/0015771 A1	Lasser et al.
Seung-Jun Bae	LOW POWER BALANCE CODE USING DATABUS INVERSION	10/18/2007	US 2007/0242508 A1	Bae
Richard E. Blahut	Algebraic Codes for Data Transmission, Cambridge University Press (2nd ed. 2003)	2003		Blahut
R. W. Hamming	Error Detecting and Error Correcting Codes, The Bell System Technical Journal (Apr. 1950)	Apr. 1950		Hamming
Satoshi Komatsu; Masahiro Fujita	An Optimization of Bus Interconnects Pitch for Low-Power and Reliable Bus Encoding Scheme, IEEE International Symposium on Circuits and Systems (2006)	2006		Komatsu et al.
Maurizio Skerlj & Paolo Ienne	Error Protected Data Bus Inversion Using Standard DRAM Components, 9th International Symposium on	2008		Skerlj Paper

	Quality Electronic Design, 35 (2008)			
Theresa C. Maxino	The Effectiveness of Checksums for Embedded Networks (May 2006), available at https://users.ece.cmu.edu/~koopman/thesis/maxino_ms.pdf (last visited Aug. 21, 2019)	May 2006		Maxino
Srinivasa R. Sridhara & Naresh R. Shanbhag	Coding for System-on-Chip Networks: A Unified Framework, Vol. 13, No. 6 IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 655 (2005)	June 2005		Sridhara et al.
Mircea R. Stan & Wayne P. Burleson	Bus-Invert Coding for Low-Power I/O, IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 49 (1995)	March 1995		Stan et al.
Andre K. Nieuwland, Atul Katoch, Daniele Rossi, Cecilia Metra	Coding Techniques for Low Switching Noise in Fault Tolerant Busses, Proceedings of the 11th IEEE International On-Line Testing Symposium, 1530-1591/05	2005		Nieuwland et al.
Michael Cornwell, Christopher Dudte	Use of 8-Bit or Higher A/D for NAND Cell Value	11/15/2007	US 2007/0262890	Cornwell et al.
Xueshi Yang, Zining Wu	Adaptive systems and methods for storing and retrieving data to and from memory cells	4/10/2008	US 2008/0086677 A1	Yang et al.
Eran Sharon, Idan Alrod	Flash memory device and system with randomizing for suppressing errors	6/26/2008	US 2008/0151618 A1	Sharon et al.
Kenneth J. Eldredge, Stephen P. Van Aken	Solid state storage element and method	7/3/2008	US 2008/0162791 A1	Eldredge et al.

Peter Leung, Chun Fung Man, Chong Ong	Method, apparatus, and system for dynamic ecc code rate adjustment	9/11/2008	US 2008/0222490 A1	Lueng et al.
Yu-an Chang, Chee-Kong Awyong, Chin Ling Wang	Flash memory system and method for controlling the same	8/14/2008	US 2008/195900 A1	Chang et al.
William Radke	Data storage with an outer block code and a stream-based inner code	1/8/2009 (7/6/2007)	US 2009/0013234 A1	Radke
Sung-Kyo JO et al.	Nonvolatile memory device, system, and method providing fast program and read operations	2/19/2009 (8/13/2008)	US 2009/0049364 A1	Jo et al. (364)
Mark Diggs et al.	Storage subsystem capable of adjusting ecc settings based on monitored conditions	3/12/2009 (9/6/2007)	US 2009/0070651 A1	Diggs et al.
Nam Phil Jo et al.	Memory system with error correction decoder architecture having reduced latency and increased throughput	3/12/2009 (8/14/2008)	US 2009/0070656 A1	Jo et al. (656)
Tony Yoon et al.	Error correcting code predication system and method	4/23/2009 (11/30/2007)	US 2009/0144598 A1	Yoon et al.
Mark Shlick et al.	Error correction in copy back memory operations	7/2/2009 (12/27/2007)	US 2009/0172498 A1	Shlick et al.
Shinichi Kanno	Semiconductor memory device and its control method	7/9/2009 (3/10/2009)	US 2009/0177944 A1	Kanno
Jason Tin et al.	System, method and memory device providing data scrambling compatible with on-chip copy operation	8/13/2009 (12/31/2007)	US 2009/0204824 A1	Tin et al.

Nam-Phil Jo et al.	Memory system and method for providing error correction	8/27/2009 (2/23/2009)	US 2009/0217140 A1	Jo et al. (140)
Steven Cheng et al.	Guaranteed memory card performance to end-of-life	11/5/2009 (4/30/2008)	US 2009/0276570 A1	Cheng et al.
Jan Gutsche et al.	Memory Cell Arrangement and Method for Reading State Information From a Memory Cell Bypassing an Error Detection Circuit	11/12/2009 (5/9/2008)	US 2009/0282308 A1	Gutsche et al.
Jun Wan et al.	Method for scrambling data in which scrambling data and scrambled data are stored in corresponding non-volatile memory locations	3/18/2010 (9/12/2008)	US 2010/0070681 A1	Wan et al.
Li-Lien Lin, Chao-Yu Wu, et al.	Storage controller with encoding/decoding circuit programmable to support different ecc requirements and related method thereof	3/27/2009	US 2010/0251068 A1	Lin et al. (068)
Akira Yamaga	Semiconductor storage device, method of controlling the same, and error correction system	9/19/2008	US 2010/0313099 A1	Yamaga (099)
Gurkirat Billing et al.	Non-volatile memory to store memory remap information	6/30/2009	US 2010/0332895 A1	Billing et al.
Chien-Chung Wu et al.	Multi-channel memory apparatus and method thereof	11/24/2009	US 2011/0126079 A1	Wu et al.
Daniel Post et al.	Data partitioning scheme for non-volatile memories	2/26/2010	US 2011/0213945 A1	Post et al.
Christopher Wilkerson et al.	Method and apparatus for using cache memory in a system that supports a low power state	5/21/2010	US 2011/0289380 A1	Wilkerson et al.

Avi Steiner et al.	System and method for multi-dimensional encoding and decoding	7/1/2010	US 2012/001778 A1	Steiner et al.
Yutaka Ito et al.	Semiconductor memory device and refresh period controlling method	2/17/2009 (6/15/2005)	US 7493531	Ito et al.
Steven Cheng et al.	Guaranteed memory card performance to end-of-life	4/30/2008	US 7971023	Cheng et al. (023)
Eran Sharon et al.	Avoiding errors in a flash memory by using substitution transformations	6/12/2006	US 7984360	Sharon et al.
Jun Jin Kong et al.	Multi-level cell memory devices using trellis coded modulation and methods of storing data in and reading data from the memory devices	5/22/2007	US 8020081	Kong et al. (081)
Idan Alrod et al.	Error correction decoding by trial and error	5/21/2006	US 8042029	Alrod et al. (029)
Jun Jin Kong et al.	Apparatuses and methods for encoding and decoding	1/18/2008	US 8239726	Kong et al. (726)
Li-Lien Lin et al.	Storage controller with encoding/decoding circuit programmable to support different ECC requirements and related method thereof	3/27/2007	US 8418021	Lin et al. (021)
Kenji Sakaue et al.	Memory system and control method for the same	6/1/2010	US 8448050	Sakaue et al.
Idan Alrod et al.	Method and apparatus for error correction according to erase counts of a solid-state memory	6/24/2008	US 8464134	Alrod et al. (134)
Jun Jin Kong et al.	Multi-level cell memory devices and methods of storing	5/24/2007	US 8499215	Kong et al. (215)

	data in and reading data from the memory devices			
Chien-Chung Wu et al.	Multi-channel memory apparatus and method thereof	11/24/2009	US 8510631	Wu et al. (631)
Robert Selinger et al.	Method and controller for performing a sequence of commands	12/30/2009	US 8595411	Selinger et al.
Nam Phil Jo	Flash memory system that uses an interleaving scheme for increasing data transfer performance between a memory device and a controller and a method thereof	10/23/2008	US 8667365	Jo et al. (365)
Jeremy Fillingim	Apparatus, system, and method for providing error correction	6/15/2010	US 8892980	Fillingim
Idan Alrod et al.	Methods for tag-grouping of blocks in storage devices	11/23/2008	US 9141475	Alrod et al. (475)
Ofir Shalvi et al.	Data storage in analog memory cell arrays having erase failures	4/23/2009	WO 2009050703 A2	Shalvi et al.
Hanan Weingarten et al.	Apparatus for coding at a plurality of rates in multi-level flash memory systems, and methods useful in conjunction therewith	6/25/2009	WO 2009078006 A2	Weingarten et al.
Koji Nishikawa et al.	Data reading device and data reading method for data reading device	7/30/2009	JP 2009169544A	Nishikawa et al.
	Memory device with adaptive capacity	4/6/2009	KR 20090033835A	KR835

2. Prior Art Systems Publicly Known or Offered for Sale

The table below lists prior art systems and products identified that reveal the state of the art and/or render the Asserted Claims invalid under 35 U.S.C. §§ 102 and/or 103. Some or all of

the supporting references for these systems may also qualify as prior art publications under 35 U.S.C. § 102 and may be used as invalidating prior art under 35 U.S.C. §§ 102 and 103.

On information and belief, each of the listed prior art systems were publicly known or used, or offered for sale prior to the critical date of the asserted patent, as described in each system's respective claim chart. The date of the offer or use, or the system became known, and the identity of the person or entity are provided in the respective system's claim chart, where applicable, based on the information reasonably available to Defendants. In addition, Defendants continue to investigate the systems and products, and reserve the right to supplement the contentions and accompanying claim charts after further discovery and investigation. Although additional information and prior art systems may be obtained through discovery, such prior art systems include at least the following:

Item Offered for Sale, Publicly Known or Used	Entity or Entities Making the Offer	Date
Flash memory products including the Daikoku2 controller ("Daikoku2") such as SSD products bearing part number THNSxxxGGxBxAA, including without limitation THNS128GG4BBAA(EPA), THNS256GG8BBAA(EPA), and THNS128GG4BBAA(PS)	Toshiba America Electronic Components, Inc.	March 20, 2009
Flash memory products including a SanDisk Griffin, Shark or Spinner controller, or similar, such as the SanDisk SSD Ultra ATA 5000 and all similar products as well as products within the SanDisk Memory Stick, Memory Stick Micro, Secure Digital, MicroSD product lines	SanDisk	At least by 2007

1. Daikoku2 is described, for example, in one or more of the following documents:

- a. DAIKOKU2 Block Diagram
 - b. NAND-DRAM.vsd files
 - c. Si-Disk ASIC DAIKOKU NANDC Register Specifications, Rev.0.2.9 (11/14/2008) (TJ)
 - d. Si-Disk ASIC ECC/COPY Error Correction Block (ECCCOPY-EXECC) Design Specifications Rev.1.1.2 (10/23/2008)
2. SanDisk controllers are described, for example, in one or more of the documents at the following bates ranges: WD-Viasat-WDTX00017967 through WD-Viasat-WDTX00018068; WD-Viasat-WDTX00019128 through WD-Viasat-WDTX00019169; WD-Viasat-WDTX00019544 through WD-Viasat-WDTX00019641; WD-Viasat-WDTX00021039 through WD-Viasat-WDTX00023856.

The prior art references and systems identified above are evidence of the state of the art, the scope and content of the prior art, the level of skill in the art, contemporaneous invention of the patented technology, and/or include teachings, suggestions, and motivations to modify or combine the prior art discussed above, as of the time of the alleged invention of the asserted claims.

To the extent that Viasat contends that any prior art does not disclose a limitation of one or more asserted claims, Defendants may rely on a combination of the prior art disclosed in these invalidity contentions, including the combinations listed by claim language, the knowledge of those skilled in the art, and/or other prior art to show that it would have been obvious to include the allegedly missing limitation. Such other prior art may include the patents, publications, and systems listed above.

3. Derivation Under Section 102(f)

Defendants do not have any disclosures under 35 U.S.C. § 102(f) at this time. Discovery is ongoing, however, and Defendants reserve the right to assert any of the preceding items of prior art under 35 U.S.C. § 102(f).

4. Knowledge and Teachings Available to Persons of Skill in the Art at the Time of Inventions

Persons of ordinary skill in the art at the time of the alleged invention of the '700 Patent understood the need for error detection and correction systems for flash memory as claimed, including decoding data to generate a plurality of partially decoded data stream, error detection sub-modules operating in parallel and an error correction module physically separate from the error detection sub-modules. This “common sense” industry understanding combined with the widespread and increasing use of flash memory error correction, before and at the time of the inventions created pressure and motivation to combine known error detection and correction systems for flash memory. In addition to the references noted above, persons of skill in the art would have had additional resources available to them with disclosures regarding these known methods and systems. These available references include those cited in the patents-in-suit and their related patents and those identified during prosecution of the patents-in-suit and their related patents.

In addition to the prior art identified above and the accompanying invalidity claim charts, Defendants also may rely on the “Background of the Invention” and other relevant portions of the patents-in-suit, other related patents, and their respective file histories (including references incorporated into and cited in the patents-in-suit and related patents), and other evidence, including fact and expert testimony about that evidence, to prove that the asserted claims are anticipated and/or rendered obvious under 35 U.S.C. §§ 102 and 103.

In addition to the references disclosed in these contentions, the attachments hereto, the patent-in suit and related patents and their prosecution histories, Patent Office proceedings related to the patents-in-suit and related patents, and the common sense knowledge of those in the industry at the time of the alleged inventions, invalidity may be demonstrated by the live testimony of

witnesses, which will be identified in accordance with the scheduling orders of these cases. Such witnesses may be used, among other purposes, to discuss issues of prior art systems, prior art references, and the knowledge of one of skill in the art at the time of the alleged inventions.

B. Anticipation

The prior art references or items listed below anticipate the asserted claims identified below, and thus those claims are invalid under 35 U.S.C. § 102(a), (b), (e) and/or (g). Each of the following charts identifies where specifically in each alleged item of prior art each element of each anticipated claim is found. To the extent a particular claim element is considered to be written in means-plus-function form and governed by 35 U.S.C. § 112, ¶ 6, the chart similarly identifies where specifically in each alleged item of prior art discloses the recited function being performed and the means that accomplishing that function. The corresponding claims are found in the accompanying charts.

Exhibit	Reference
A01	Daikoku2
A02	Chen
A03	Yamaga
A04	Kanno
A05	Lee '537
A06	Visconti
A07	JO
A08	Kim '928
A09	Chapman
A10	Kim '217
A11	Olbrich

Exhibit	Reference
A12	Hong
A13	Wan
A14	Wu
A15	Diggs
A16	Chang
A17	Cheng
A18	Gutsche
A19	Lee '809
A20	Yang
A21	Yim
A22	Smith
A23	Kitahara
A24	Nieuwland
A25	SanDisk

C. Obviousness

The prior art identified in these Initial Invalidity Contentions, including the exemplary charts referenced herein in Exhibits A01 to A25 demonstrate that the concepts of the Asserted Claims were well known to persons of ordinary skill in the art prior to the alleged invention of the patent-in-suit. Provided below are examples of the prior art that disclose various limitations of the Asserted Claims. Notwithstanding these examples, all of the prior art referenced in these Initial Invalidity Contentions either anticipate or render obvious (alone or in combination) the Asserted Claims.

Defendants believe that no showing of a specific motivation to combine prior art is required to combine the references disclosed above and in the attached charts. There was a reason to make each combination; each combination of art would have produced no unexpected results; and each combination at most would simply represent a known alternative to one of ordinary skill in the art. *See KSR Int'l Co. v. Teleflex, Inc.*, 550 U.S. 398, 415-18 (2007) (rejecting the Federal Circuit's "rigid" application of the teaching, suggestion, or motivation to combine test, instead espousing an "expansive and flexible" approach). Indeed, the Supreme Court held that a person of ordinary skill is "a person of creativity, not an automaton" and "in many cases a person of ordinary skill will be able to fit the teachings of multiple patents together like pieces of a puzzle." *Id.* at 420-21; *see also* Examination Guidelines for Determining Obviousness Under 35 U.S.C. §103 in view of the Supreme Court Decision in *KSR International Co. v. Telefax Inc.*, 72 Fed. Reg. 57,526 (Oct. 10, 2007).

One or more combinations of the prior art references identified above would have been obvious because these references would have been combined using: known methods to yield predictable results; known techniques in the same way; a simple substitution of one known, equivalent element for another to obtain predictable results; and/or a teaching, suggestion, or motivation in the prior art generally. In addition, it would have been obvious to try combining the prior art references identified above because there were only a finite number of predictable solutions and/or because known work in one field of endeavor prompted variations based on predictable design incentives and/or market forces either in the same field or a different one. In addition, the combination of the prior art references identified above would have been obvious because the combination represents the known potential options with a reasonable expectation of success.

Additional evidence that there would have been a motivation to combine the prior art references identified above includes the interrelated teachings of multiple prior art references; the effects of demands known to the design community or present in the marketplace; the existence of a known problem for which there was an obvious solution encompassed by the asserted claims; the existence of a known need or problem in the field of the endeavor at the time of the invention(s); and the background knowledge that would have been possessed by a person having ordinary skill in the art.

Thus, the motivation to combine the teachings of the prior art references disclosed herein is found in the references themselves and: (1) the nature of the problem being solved; (2) the express, implied and inherent teachings of the prior art; (3) the knowledge of persons of ordinary skill in the art; (4) the predictable results obtained in combining the different elements of the prior art; (5) the predictable results obtained in simple substitution of one known element for another; (6) the use of a known technique to improve similar devices, methods, or products in the same way; (7) the predictable results obtained in applying a known technique to a known device, method, or product ready for improvement; (8) the finite number of identified predictable solutions that had a reasonable expectation of success; and (9) known work in various technological fields that could be applied to the same or different technological fields based on design incentives or other market forces.

Any reference or combination of references that anticipates or makes obvious an asserted independent claim also makes obvious any asserted claim dependent on that independent claim because every element of each dependent claim was known by a person of ordinary skill at the time of the alleged invention, and it would have been obvious to combine those known elements with the independent claims at least as a matter of common sense and routine innovation.

Accordingly, Defendants contend that each asserted claim would have been obvious not only by the combinations explicitly defined in these contentions, but also by any combination of references that renders obvious an asserted claim.

By way of non-limiting example, the prior art identified herein and in the accompanying charts establishes that a person of ordinary skill would have been aware, understood and found obvious to incorporate into the prior-art systems that:

- 1) Non-volatile memories had used beneficially in a wide variety of applications, ranging, *e.g.*, from use in digital cameras, to mobile devices, to USB storage devices, to solid-state drives (SSDs). *See, e.g.*, Exhibits hereto; *see also, e.g.*, U.S. 2011/0126079 (“Wu”), ¶ 0022; U.S. 2010/0070681 (“Wan”), ¶ 0053; U.S. 2009/0276570 (“Cheng”), ¶ 0002; U.S. 8,412,879 (“Chang”), 1:30-2:41.
- 2) Increasing densities of non-volatile flash memory arrays, including increasing bits per cell, had been providing greater storage capacity, but also resulted in an increase in the appearance of errors, *i.e.*, instances where the data retrieved from a particular portion of memory is not identical to the data that had been stored in that portion of memory. *See, e.g.*, Exhibits hereto; *see also, e.g.*, Wu, ¶ 0006; U.S. 2008/0086677 (“Yang”), ¶ 0005; U.S. 2009/0063934 (“Jo”) ¶ 0009; U.S. 8,086,933 (“Yamaga”), Fig. 19.
- 3) A variety of error correction code (“ECC”) encoding schemes, and in particular forward error correction code encoding (“FEC”) schemes including, *e.g.*, Hamming code, a BCH code, a Turbo code, and low-density parity check code, were widely known and commonly employed for correcting these errors and thereby improving non-volatile memory performance, capacity, and lifetime. *See, e.g.*, Exhibits hereto; *see also, e.g.*,

Yang, ¶ 0051; U.S. 2010/0100797 (“Chen”), ¶¶ 0002, 0013-16; Yamaga, 14:59-66; Chang, 1:30-2:41, 5:4-49.

- 4) The error correction decoding could be implemented by distinct modules for partial decoding, followed by error detection, followed by error correction as needed. *See, e.g.*, Exhibits hereto.
- 5) Error detection and error correction modules were often physically distinct. *See, e.g.*, Exhibits hereto.
- 6) Generation of partially decoded data streams, e.g., by descrambling stored data, or, as Viasat appears to contend, by buffering and de-interleaving data retrieved from non-volatile memory was commonplace. *See, e.g.*, Exhibits hereto; *see also, e.g.*, Wan, ¶¶ 0049, 0051.
- 7) Non-volatile memory could be arranged in blocks, pages, and sectors. *See, e.g.*, Exhibits hereto; *see also, e.g.*, U.S. 2009/0070651 (“Diggs”), ¶ 0063; U.S. 8,612,830 (“Kitahara”), 3:48-4:16; Chang, 7:42-51.
- 8) A variety of schemes existed for interfacing with non-volatile memory systems and accessing different portions of memory using, e.g., access modules, controllers, DMAs, interfaces, to accommodate, e.g., cost, speed, storage capacity, system lifetime, power consumption, and system size objectives for a variety of applications. *See, e.g.*, Exhibits hereto; *see also, e.g.*, Jo, ¶ 0010.
- 9) A variety of schemes existed for allocating error correction encoding resources within non-volatile memory systems to accommodate, e.g., cost, speed, storage capacity, system lifetime, power consumption, and system size objectives for a variety of

applications. *See, e.g.*, Exhibits hereto; *see also, e.g.*, Cheng, ¶ 0022; U.S. 2009/0282308 (“Gutsche”), ¶¶ 0118-130; Chang, 1:30-2:41, 5:4-49.

10) Error detection modules (or sub-modules) might advantageously be assigned to error correction modules (or sub-modules) and might advantageously outnumber error correction modules (or sub-modules). *See, e.g.*, Exhibits hereto; *see also, e.g.*, Jo, ¶¶ 0040-41, 0047; U.S. 2008/0163033 (“Yim”), Fig. 7; U.S. 6,510,537 (“Lee ’537”) Figs. 6 and 12; U.S. 7,865,809 (“Lee ’809”), Fig. 5b.

11) Error correction coding schemes and coding rates could be advantageously changed in response to monitored performance degradation to enable correction of an increasing number of errors encountered when reading from a given portion of memory. *See, e.g.*, Exhibits hereto; *see also, e.g.*, U.S. 2010/0241928 (“Kim ’928”), ¶ 0029; U.S. 6,961,890 (“Smith”) 2:33-52; Diggs, ¶¶ 0006-7; Cheng, ¶¶ 0021-22, Yang, ¶¶ 0033-37; Gutsche, ¶ 0103; Chang, 1:30-2:41, 5:4-49.

12) Additional error correction modules could be advantageously employed in response to monitored performance degradation to enable timely correction of an increasing number of errors encountered when reading from a given portion of memory. *See, e.g.*, Exhibits hereto; *see also, e.g.*, Cheng, ¶ 0022; U.S. 8,245,101 (“Olbrich”), 44:7-18.

Further explanations are provided below. While certain claims are specifically identified, they rationale applies to those specific claims, as well as any other claim containing the same or substantially the same limitation (*e.g.*, any dependent claim from which an independent claim depends).

1. **“the error correction module, communicatively coupled with and physically separate from the error detection module” (e.g., ’700 Patent, claims 1, 15, 17)**

To the extent Plaintiff contends that any of the references identified above do not disclose this limitation, the limitation is obvious in light of the background knowledge possessed by a person of ordinary skill in the art, and/or the limitation can be found, for example, in one or more of the following references:

- U.S. Patent Pub. No. 2009/0063934 to JO
- U.S. Patent No. 7,865,809 to Lee
- U.S. Patent Pub. No. 2010/0100797 to Chen
- U.S. Patent No. 7,478,292 to Visconti
- PCT Pub. No. 2005/088467 to Nieuwland (“Nieuwland”)
- U.S. Patent No. 8,245,101 to Olbrich
- additional references charted for this limitation

A person of ordinary skill in the art desiring to physically separate error detection from correction would recognize that doing so would offer potential power savings in an error correction system. Such a person would understand that doing so would allow error correction circuitry to be powered off when no errors are detected by the error detectors, thereby saving power. Physically separating error detection from correction was a well-known technique well before the alleged invention of the '700 Patent. Each of the references listed above demonstrates that some form of physical separation between correction and detection circuitry is implemented. *See*, JO, Abstract, FIG. 2, [0007]-[0008], [0028], FIG. 5, [0034]-[0035], FIG. 6 [0037], [0041], *and* Claim 1; Lee '809 FIG. 5B, 2:22-37, 8:56-9:28, Claim 1, *and* Claim 7; Chen FIG. 1, [0004], [0011]-[0014]; Claim 1, Claim 2, *and* Claim 3; Visconti FIG. 3B, *and* 6:21-41; Nieuwland FIGS. 2-4, *and* FIG. 7; Olbrich 43:54-60 *and* FIG. 31. Each of the identified prior art references deals with error detection and correction. The fact that these issues are expressly disclosed in the '700 Patent suggests that a person of ordinary skill in the art at the time of invention would have been motivated to combine the teachings of the specifically identified prior art references with the teachings of a charted reference to physically separate error detection from correction.

2. **“a read controller configured to dynamically modify the error detection sub-modules assigned to at least a subset of the sectors of flash memory” (e.g., ’700 Patent, Claim 3)**

To the extent Plaintiff contends that any of the references identified above do not disclose this limitation, the limitation is obvious in light of the background knowledge possessed by a person of ordinary skill in the art, and/or in light of the disclosure in one or more of the following references:

- U.S. Patent No. 8,281,217 to Kim (“Kim ’217”);
- U.S. Patent Pub. No. 2010/0241928 to Kim et al.;
- U.S. Patent Pub. No. 2010/0100797 to Chen
- U.S. Patent No. 8,086,933 to Yamaga
- U.S. Patent No. 7,478,292 Visconti
- additional references charted for this limitation

A person of ordinary skill in the art desiring to dynamically modify error detection sub-modules assigned to at least a subset of flash memory sectors would recognize that doing so would improve transmission efficiency and would potentially optimize error control encoding overhead. Dynamic modification of error detection capabilities was a well-known technique well before the alleged invention of the ’700 Patent. Each of the references listed above demonstrates that some form of dynamic modification of error detection modules was implemented. Kim (’217) 1:46-50, 7:9-14; Kim (’928) [0030], [0037], [0035], *and* [0039]; *see also* Chen [0012]. Each of the identified prior art references deals with dynamically modifying error detection modules. The fact that these issues are expressly disclosed in the ’700 Patent suggests that a person of ordinary skill in the art at the time of invention would have been motivated to combine the teachings of the specifically identified prior art references with the teachings of a charted reference to dynamically modify error detection sub-modules assigned to at least a subset of flash memory sectors.

II. U.S. PATENT NO. 8,966,347 - INVALIDITY UNDER 35 U.S.C. §§ 102 AND 103

The asserted claims of U.S. Patent No. 8,966,347 (the “’347 Patent”) are invalid as anticipated by the prior art under various subsections of 35 U.S.C. § 102 and/or as obvious in view of the prior art under 35 U.S.C. § 103.

C. Identification of Prior Art

The charts attached as appendices to these invalidity contentions set forth how prior art identified by Defendants anticipates either expressly or inherently, and/or renders obvious, each asserted claim. Defendants cite the most relevant portions of the identified prior art references. However, other portions of the identified prior art may additionally anticipate, either expressly or inherently, and/or render obvious one or more of the asserted claims.

Where Defendants cite a particular drawing or figure in the accompanying charts, the citation encompasses the description of the drawing or figure, as well as any text associated with the drawing or figure (even if the associated text is not itself expressly cited). Similarly, where Defendants cite particular text concerning a drawing or figure in the accompanying charts, the citation encompasses that drawing or figure as well (even if the associated drawing or figure is not expressly cited). Defendants further incorporate by reference the prior art references cited in the patents-in-suit, any patents or patent applications related to the patent-in-suit, and any patent or patent application sharing a common inventor with the patents-in-suit. This includes without limitation those identified in any other proceeding involving the patents-in-suit or related U.S. or foreign patents. Defendants additionally incorporate by reference all prior art produced or otherwise known to Plaintiff and all prior art known to the named inventor, any past or current owner, or any individual substantively involved in the prosecution of the patents-in-suit.

Defendants contend that at least some of the systems and products disclosed in one or more of the prior art references identified here or in the attached exhibits are prior art under 35 U.S.C.

§§ 102(a), (b), (e), (f) and/or (g), and/or 103. Defendants' reference to any particular component, device, machine, or other product herein should also be interpreted as a reference to the product itself and any corresponding patents, publications, or product literature cited here or in the attached exhibits that relate to the cited component, device, machine, or other product. Defendants do not yet have complete information regarding the dates by which some of the cited products were publicly disclosed, used, sold, or offered for sale, the circumstances under which the research, design, and development activities were conducted, and the identities of the particular individuals involved in such activities through publicly available patents, publications, and product literature. Defendants anticipate that the actual dates, circumstances, and identities of individuals will be the subject of third party discovery during this lawsuit.

It is understood that a person of ordinary skill in the art reads a prior art reference as a whole and in the context of other publications, literature, and general knowledge in the field. To understand and interpret any specific statement or disclosure in a prior art reference, a person of ordinary skill in the art also relies upon other information including other publications and general scientific, engineering or other relevant knowledge. Defendants reserve the right to rely upon the general scientific, engineering or other relevant knowledge in the field in interpreting the disclosure of the prior art references. In addition, Defendants reserve the right to rely upon other publications and on expert testimony to provide context and to aid in the understanding of the prior art references. Defendants also reserve the right to rely upon other portions of the prior art references, other publications, and the testimony of experts to establish that the alleged inventions would have been obvious to a person of ordinary skill in the art, including the basis for modifying or combining the prior art references. Furthermore, Defendants reserve the right to rely upon any admissions relating to prior art found in the intrinsic evidence for the patents-in-suit.

Certain pieces of identified prior art inherently disclose features of the asserted claims. Defendants may rely on inherency to demonstrate the invalidity of the asserted claims. Moreover, certain prior art references and solutions may inherently anticipate certain features of the asserted claims as construed by Viasat. Defendants may rely on other portions of the prior art, other documents, and expert testimony to establish the inherency of certain features of the prior art to invalidate the asserted claims. Defendants also may rely on any reference identified in these invalidity contentions or any other reference to prove that the references are enabled or to explain the meaning of a term used in the solutions or any reference.

1. Prior Art Patents and Publication References

The table in Section I.A.1 above lists prior art patents, patent applications, and patent publications that describe the state of the art and/or render the Asserted Claims invalid under 35 U.S.C. §§ 102 and/or 103. Each listed reference became prior art at least as early as the dates provided on the face of the document. Defendants reserve the right to rely upon earlier dates of publication or public availability to the extent such information is uncovered during discovery.

2. Prior Art Systems Publicly Known or Offered for Sale

The table below lists prior art systems and products identified that reveal the state of the art and/or render the Asserted Claims invalid under 35 U.S.C. §§ 102 and/or 103. Some or all of the supporting references for these systems may also qualify as prior art publications under 35 U.S.C. § 102 and may be used as invalidating prior art under 35 U.S.C. §§ 102 and 103.

On information and belief, each of the listed prior art systems were publicly known or used, or offered for sale prior to the critical date of the asserted patent, as described in each system's respective claim chart. The date of the offer or use, or the system became known, and the identity of the person or entity are provided in the respective system's claim chart, where applicable, based on the information reasonably available to Defendants. In addition, Defendants continue to

investigate the systems and products, and reserve the right to supplement the contentions and accompanying claim charts after further discovery and investigation. Although additional information and prior art systems may be obtained through discovery, such prior art systems include at least the following (corresponding documents described above in Section I.A.2):

Item Offered for Sale, Publicly Known or Used	Entity or Entities Making the Offer	Date
Flash memory products including a SanDisk Griffin, Shark or Spinner controller, or similar, such as the SanDisk SSD Ultra ATA 5000 and all similar products as well as products within the SanDisk Memory Stick, Memory Stick Micro, Secure Digital, MicroSD product lines	SanDisk	At least by 2007

The prior art references and systems identified above are evidence of the state of the art, the scope and content of the prior art, the level of skill in the art, contemporaneous invention of the patented technology, and/or include teachings, suggestions, and motivations to modify or combine the prior art discussed above, as of the time of the alleged invention of the asserted claims.

To the extent that Viasat contends that any prior art does not disclose a limitation of one or more asserted claims, Defendants may rely on a combination of the prior art disclosed in these invalidity contentions, including the combinations listed by claim language, the knowledge of those skilled in the art, and/or other prior art to show that it would have been obvious to include the allegedly missing limitation. Such other prior art may include the patents, publications, and systems listed above.

3. Derivation Under Section 102(f)

Defendants do not have any disclosures under 35 U.S.C. § 102(f) at this time. Discovery is ongoing, however, and Defendants reserve the right to assert any of the preceding items of prior art under 35 U.S.C. § 102(f).

4. Knowledge and Teachings Available to Persons of Skill in the Art at the Time of Inventions

Persons of ordinary skill in the art at the time of the alleged invention of the '347 Patent understood the need for error detection and correction systems for flash memory as claimed. This “common sense” industry understanding combined with the widespread and increasing use of flash memory error detection and correction, before and at the time of the inventions created pressure and motivation to combine known error detection and correction systems for flash memory. In addition to the references noted above, persons of skill in the art would have had additional resources available to them with disclosures regarding these known methods and systems. These available references include those cited in the patents-in-suit and their related patents and those identified during prosecution of the patents-in-suit and their related patents.

In addition to the prior art identified above and the accompanying invalidity claim charts, Defendants also may rely on the “Background of the Invention” and other relevant portions of the patents-in-suit, other related patents, and their respective file histories (including references incorporated into and cited in the patents-in-suit and related patents), and other evidence, including fact and expert testimony about that evidence, to prove that the asserted claims are anticipated and/or rendered obvious under 35 U.S.C. §§ 102 and 103.

In addition to the references disclosed in these contentions, the attachments hereto, the patent-in suit and related patents and their prosecution histories, Patent Office proceedings related to the patents-in-suit and related patents, and the common sense knowledge of those in the industry

at the time of the alleged inventions, invalidity may be demonstrated by the live testimony of witnesses, which will be identified in accordance with the scheduling orders of these cases. Such witnesses may be used, among other purposes, to discuss issues of prior art systems, prior art references, and the knowledge of one of skill in the art at the time of the alleged inventions.

D. Anticipation

The prior art references or items listed below anticipate the asserted claims identified below, and thus those claims are invalid under 35 U.S.C. § 102(a), (b), (e) and/or (g). Each of the following charts identifies where specifically in each alleged item of prior art each element of each anticipated claim is found. To the extent a particular claim element is considered to be written in means-plus-function form and governed by 35 U.S.C. § 112, ¶ 6, the chart similarly identifies where specifically in each alleged item of prior art discloses the recited function being performed and the means that accomplishing that function. The corresponding claims are found in the accompanying charts.

Exhibit	Reference
B01	Diggs
B02	Cheng
B03	Chen
B04	Chang
B05	Gutsche
B06	Yang
B07	Kim '928
B08	Smith
B09	SanDisk

E. Obviousness

The prior art identified in these Initial Invalidity Contentions, including the exemplary charts referenced herein in Exhibits B01 to B09 demonstrate that the concepts of the Asserted Claims were well known to persons of ordinary skill in the art prior to the alleged invention of the '347 Patent. Provided below are examples of the prior art that disclose various limitations of the Asserted Claims. Notwithstanding these examples, all of the prior art referenced in these Initial Invalidity Contentions either anticipate or render obvious (alone or in combination) the Asserted Claims.

Defendants believe that no showing of a specific motivation to combine prior art is required to combine the references disclosed above and in the attached charts. There was a reason to make each combination; each combination of art would have produced no unexpected results; and each combination at most would simply represent a known alternative to one of ordinary skill in the art. *See KSR Int'l Co. v. Teleflex, Inc.*, 550 U.S. 398, 415-18 (2007) (rejecting the Federal Circuit's "rigid" application of the teaching, suggestion, or motivation to combine test, instead espousing an "expansive and flexible" approach). Indeed, the Supreme Court held that a person of ordinary skill is "a person of creativity, not an automaton" and "in many cases a person of ordinary skill will be able to fit the teachings of multiple patents together like pieces of a puzzle." *Id.* at 420-21; *see also* Examination Guidelines for Determining Obviousness Under 35 U.S.C. §103 in view of the Supreme Court Decision in *KSR International Co. v. Telefax Inc.*, 72 Fed. Reg. 57,526 (Oct. 10, 2007).

One or more combinations of the prior art references identified above would have been obvious because these references would have been combined using: known methods to yield predictable results; known techniques in the same way; a simple substitution of one known,

equivalent element for another to obtain predictable results; and/or a teaching, suggestion, or motivation in the prior art generally. In addition, it would have been obvious to try combining the prior art references identified above because there were only a finite number of predictable solutions and/or because known work in one field of endeavor prompted variations based on predictable design incentives and/or market forces either in the same field or a different one. In addition, the combination of the prior art references identified above would have been obvious because the combination represents the known potential options with a reasonable expectation of success.

Additional evidence that there would have been a motivation to combine the prior art references identified above includes the interrelated teachings of multiple prior art references; the effects of demands known to the design community or present in the marketplace; the existence of a known problem for which there was an obvious solution encompassed by the asserted claims; the existence of a known need or problem in the field of the endeavor at the time of the invention(s); and the background knowledge that would have been possessed by a person having ordinary skill in the art.

Thus, the motivation to combine the teachings of the prior art references disclosed herein is found in the references themselves and: (1) the nature of the problem being solved; (2) the express, implied and inherent teachings of the prior art; (3) the knowledge of persons of ordinary skill in the art; (4) the predictable results obtained in combining the different elements of the prior art; (5) the predictable results obtained in simple substitution of one known element for another; (6) the use of a known technique to improve similar devices, methods, or products in the same way; (7) the predictable results obtained in applying a known technique to a known device, method, or product ready for improvement; (8) the finite number of identified predictable solutions

that had a reasonable expectation of success; and (9) known work in various technological fields that could be applied to the same or different technological fields based on design incentives or other market forces.

Any reference or combination of references that anticipates or makes obvious an asserted independent claim also makes obvious any asserted claim dependent on that independent claim because every element of each dependent claim was known by a person of ordinary skill at the time of the alleged invention, and it would have been obvious to combine those known elements with the independent claims at least as a matter of common sense and routine innovation. Accordingly, Defendants contend that each asserted claim would have been obvious not only by the combinations explicitly defined in these contentions, but also by any combination of references that renders obvious an asserted claim.

By way of non-limiting example, the prior art identified herein and in the accompanying charts establishes that a person of ordinary skill would have been aware, understood and found obvious to incorporate into the prior-art systems that:

- 1) Non-volatile memories had used beneficially in a wide variety of applications, ranging, *e.g.*, from use in digital cameras, to mobile devices, to USB storage devices, to solid-state drives (SSDs). *See, e.g.*, Exhibits hereto; *see also, e.g.*, U.S. 2011/0126079 (“Wu”), ¶ 0022; U.S. 2010/0070681 (“Wan”), ¶ 0053; U.S. 2009/0276570 (“Cheng”), ¶ 0002; U.S. 8,412,879 (“Chang”), 1:30-2:41.
- 2) Increasing densities of non-volatile flash memory arrays, including increasing bits per cell, had been providing greater storage capacity, but also resulted in an increase in the appearance of errors, *i.e.*, instances where the data retrieved from a particular portion of memory is not identical to the data that had been stored in that portion of memory.

- See, e.g.*, Exhibits hereto; *see also, e.g.*, Wu, ¶ 0006; U.S. 2008/0086677 (“Yang”), ¶ 0005; U.S. 2009/0063934 (“Jo”) ¶ 0009; U.S. 8,086,933 (“Yamaga”), Fig. 19.
- 3) A variety of error correction code (“ECC”) encoding schemes, and in particular forward error correction code encoding (“FEC”) schemes including, e.g., Hamming code, a BCH code, a Turbo code, and low-density parity check code, were widely known and commonly employed for correcting these errors and thereby improving non-volatile memory performance, capacity, and lifetime. *See, e.g.*, Exhibits hereto; *see also, e.g.*, Yang, ¶ 0051; U.S. 2010/0100797 (“Chen”), ¶¶ 0002, 0013-16; Yamaga, 14:59-66; Chang, 1:30-2:41, 5:4-49.
 - 4) The error correction decoding could be implemented by distinct modules for partial decoding, followed by error detection, followed by error correction as needed. *See, e.g.*, Exhibits hereto.
 - 5) Error detection and error correction modules were often physically distinct. *See, e.g.*, Exhibits hereto.
 - 6) Generation of partially decoded data streams, e.g., by descrambling stored data, or, as Viasat appears to contend, by buffering and de-interleaving data retrieved from non-volatile memory was commonplace. *See, e.g.*, Exhibits hereto; *see also, e.g.*, Wan, ¶¶ 0049, 0051.
 - 7) Non-volatile memory could be arranged in blocks, pages, and sectors. *See, e.g.*, Exhibits hereto; *see also, e.g.*, U.S. 2009/0070651 (“Diggs”), ¶ 0063; U.S. 8,612,830 (“Kitahara”), 3:48-4:16; Chang, 7:42-51.
 - 8) A variety of schemes existed for interfacing with non-volatile memory systems and accessing different portions of memory using, e.g., access modules, controllers, DMAs,

interfaces, to accommodate, *e.g.*, cost, speed, storage capacity, system lifetime, power consumption, and system size objectives for a variety of applications. *See, e.g.*, Exhibits hereto; *see also, e.g.*, Jo, ¶ 0010.

- 9) A variety of schemes existed for allocating error correction encoding resources within non-volatile memory systems to accommodate, *e.g.*, cost, speed, storage capacity, system lifetime, power consumption, and system size objectives for a variety of applications. *See, e.g.*, Exhibits hereto; *see also, e.g.*, Cheng, ¶ 0022; U.S. 2009/0282308 (“Gutsche”), ¶ 0118-130; Chang, 1:30-2:41, 5:4-49.
- 10) Error detection modules (or sub-modules) might advantageously be assigned to error correction modules (or sub-modules) and might advantageously outnumber error correction modules (or sub-modules). *See, e.g.*, Exhibits hereto; *see also, e.g.*, Jo, ¶¶ 0040-41, 0047; U.S. 2008/0163033 (“Yim”), Fig. 7; U.S. 6,510,537 (“Lee”) Figs. 6 and 12; U.S. 7,865,809 (“Lee”), Fig. 5b.
- 11) Error correction coding schemes and coding rates could be advantageously changed in response to monitored performance degradation to enable correction of an increasing number of errors encountered when reading from a given portion of memory. *See, e.g.*, Exhibits hereto; *see also, e.g.*, U.S. 2010/0241928 (“Kim ’928”), ¶ 0029; U.S. 6,961,890 (“Smith”) 2:33-52; Diggs, ¶¶ 0006-7; Cheng, ¶¶ 0021-22, Yang, ¶¶ 0033-37; Gutsche, ¶ 0103; Chang, 1:30-2:41, 5:4-49.

III. INVALIDITY UNDER 35 U.S.C. § 112

A. Indefiniteness

On June 2, 2014, the United States Supreme Court established a new standard for indefiniteness. *Nautilus, Inc. v. Biosig Instruments, Inc.*, No. 13-369, 134 S. Ct. 2120 (June 2, 2014). Rejecting the Federal Circuit’s prior “insolubly ambiguous” standard, the Supreme Court

held that “a patent is invalid for indefiniteness if its claims, read in light of the specification delineating the patent, and the prosecution history, fail to inform, with reasonable certainty, those skilled in the art about the scope of the invention.” *Id.* at 2124. The following terms render one or more claims of the ’700 Patent indefinite under 35 U.S.C. § 112, as the claims, specifications, and prosecution histories fail to inform those of skill in the art of the scope of the claimed invention(s) with any reasonable certainty³:

Claim Term	Claim(s)
“partially decoded data streams” / “decode the received encoded data to generate a plurality of partially decoded data streams” / “receive a different one of the plurality of partially decoded data streams”	1–14
“the error correction module . . . physically separate from [the / an] error detection module”	1–25
“sectors of flash memory”	2, 18
“the encoding module”	15, 16
“the error detection module”	15, 16
““a read controller configured to dynamically modify the error detection sub-modules assigned to at least a subset of the sectors of flash memory”	3
“selectively power-up one or more of the error correction sub-modules”	5, 6
“a power controller is configured to selectively power-up an error correction sub-module for assignment to a set of one or more of the monitored sectors”	7
“a read controller configured to selectively power-down one or more subsets of the error detection sub-modules”	9

³ All dependent claims depending from an identified claim, even if not specifically listed, are included, *e.g.*, independent claims listed also include all asserted claims dependent thereon, even if those claims are not individually listed.

“the error detection module comprises the decoding module”	14
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In addition, the following claims of the '700 Patent, if found to be written in means-plus-function form pursuant to 35 U.S.C. § 112, ¶ 6, are indefinite because the recited functions either have no corresponding structure or because the recited functions are performed by general purpose computers without disclosure of the specific algorithm or other instructions used to perform the function. *See Triton Tech of Tex., LLC v. Nintendo of Am., Inc.*, 753 F.3d 1375, 1378 (Fed. Cir. 2014) (“Failure to disclose the corresponding algorithm for a computer-implemented means-plus-function term renders the claim indefinite.”).

Claim Term	Claim(s)
“error detection module”	1–25
“error detection sub-module” / “error detection sub-module configured to: receive a different one of the plurality of partially decoded data streams; detect whether a portion of the respective received stream contains an error; and forward the portion of the respective received stream containing an error to an error correction module”	1–14
“error detection sub-module” / “error detection sub-module is configured to: detect whether a portion of the respective received stream contains an error; and forward the portion of the respective received stream containing an error to an error correction module of the decoder”	15, 16
“error detection sub-module” / “error detection sub-module is configured to: detect whether a portion of the respective received stream contains an error; and forward the portion of the respective received stream containing an error to an error correction module”	17–25
“error correction module” / “an error correction module... configured to correct the received portions of the respective received streams containing an error”	1–14
“error correction module” / “[correct/correcting], with the error correction module ... the forwarded portions of the respective received streams containing an error”	15–25
“decoding module” / “a decoding module configured to: receive encoded data from the flash memory; and decode the received encoded data to generate a plurality of partially decoded data streams”	1–14

“each of the error detection sub-modules is configured to read data from a set of one or more sectors of flash memory different from other of the error detection sub-modules”	2
“an error monitoring module” / “an error monitoring module ... configured to monitor a rate of errors from the error detection module”	6, 11
“an error monitoring module” / “an error monitoring module ... configured to monitor a rate of errors from the error detection module for each of a plurality of sectors of the flash memory”	7, 12
“a plurality of error correction sub-modules operating in parallel and fewer in number than the error detection sub-modules”	4, 19
“each error correction sub-module is configured to receive portions of the respective received streams containing an error detected in parallel by the set of two or more error detection sub-modules assigned to the respective error correction sub-module”	8
“each error detection sub-module is configured to direct error-free portions of the respective received streams to bypass the error correction module”	13

The following claims of the '347 Patent, if found to be written in means-plus-function form pursuant to 35 U.S.C. § 112, ¶ 6, are indefinite because the recited functions either have no corresponding structure or because the recited functions are performed by general purpose computers without disclosure of the specific algorithm or other instructions used to perform the function.

Claim Term	Claim(s)
“a first error correction sub-module”	1–11, 13–23
“a second error correction sub-module”	1–11, 13–23

B. Written Description⁴

“To satisfy the written description requirement, the applicant must convey with reasonable clarity to those skilled in the art that, as of the filing date sought, he or she was in possession of the invention, and demonstrate that by disclosure in the specification of the patent.” *Novozymes A/S v. DuPont Nutrition Biosciences APS*, 723 Fed. 1336, 1344 (Fed. Cir. 2013) (internal quotation marks omitted).

The following terms render one or more of the claims of the ’700 Patent invalid for lack of written description under 35 U.S.C. § 112, as the original specification of the ’700 Patent does not demonstrate that the inventors were in possession of the claimed subject matter:

Claim Term	Claim(s)
“error detection module”	1–25
“error detection sub-module”	1–25
“error correction module”	1–25
“decoding module”	1–14
“error monitoring module”	6, 7, 11, 12
“decode the received encoded data to generate a plurality of partially decoded data streams”	1–14
“receive a different one of the plurality of partially decoded data streams”	1–14
“error correction module . . . physically separate from the error detection module”	1–25
“dynamically modify the error detection sub-modules assigned to at least a subset of the sectors of flash memory”	3, 18

⁴ All dependent claims depending from an identified claim, even if not specifically listed, are included, *e.g.*, independent claims listed also include all asserted claims dependent thereon, even if those claims are not individually listed. These claims are alternatively invalid for lack of enablement.

“a decoder ... configured to: retrieve the encoded data from flash memory to generate a plurality of data streams”	1–14
“the error detection module comprises the decoding module”	14

The following terms render one or more of the claims of the '347 Patent invalid for lack of written description under 35 U.S.C. § 112, as the original specification of the '347 Patent does not demonstrate that the inventors were in possession of the claimed subject matter:

Claim Term	Claim(s)
“a first error correction sub-module”	1–11, 13–23
“a second error correction sub-module”	1–11, 13–23
“retrieving the encoded data stored in the flash memory to generate a data stream”	1–11
“monitoring a metric of the flash memory while repeating the encoding, the storing, the retrieving and the processing, wherein the metric represents memory performance degradation of the flash memory	1–11
“retrieving the subsequently encoded data stored in the flash memory to generate a second data stream”	11
“a decoder to retrieve the encoded data stored in the flash memory to generate a data stream”	13–23
“a controller to: monitor a metric of the flash memory while repeating the encoding, the storing, the retrieving and the processing, wherein the metric represents memory performance degradation of the flash memory”	13–23
“the decoder retrieves the encoded data”	20
“the decoder: retrieves the subsequently encoded data stored in the flash memory to generate a second data stream”	23

IV. 101 CONTENTIONS

The following claim charts identify the exception to eligibility for the Challenged Claims of each patent-in-suit, and the factual and legal bases therefor, and whether each Challenged Claim is representative of any other Challenged Claims. Dependent claims are subject to the same arguments.

A. U.S. Patent No. 8,615,700

Challenged Claim	Exception to Eligibility	Factual and Legal Basis	Representative of Other Claims
1	Abstract idea	This claim contains an abstract idea without an inventive concept and is thus invalid under 35 U.S.C. § 101. The state of the art documents addressed above (and in defendants' accompanying invalidity contentions) illustrate that the elements of this claim in combination are well understood, routine, and conventional.	Claim 15, 17

B. U.S. Patent No. 8,966,347

Challenged Claim	Exception to Eligibility	Factual and Legal Basis	Representative of Other Claims
1	Abstract idea	This claim contains an abstract idea without an inventive concept and is thus invalid under 35 U.S.C. § 101. The state of the art documents addressed above (and in defendants' accompanying invalidity contentions) illustrate that the elements of this claim in combination are well understood, routine, and conventional.	Claim 13

V. PRODUCTION ACCOMPANYING INVALIDITY CONTENTIONS

Defendants identify that Kioxia and Western Digital are separately producing, and will separately identify by bates number, documentation sufficient to show the operation of aspects or

elements of the Accused Instrumentalities identified by the patent claimant in the chart, to the extent the Defendants could understand those contentions.

Defendants are jointly producing prior art references and corroborating evidence concerning prior art systems, including, but not limited to, VIASAT_DEFENDANTS'_PRIOR_ART-0000000001-2564; WD-Viasat-WDTX00017967 through WD-Viasat-WDTX00018068; WD-Viasat-WDTX00019128 through WD-Viasat-WDTX00019169; WD-Viasat-WDTX00019544 through WD-Viasat-WDTX00019641; WD-Viasat-WDTX00021039 through WD-Viasat-WDTX00023856. Defendants' search for prior art references, additional documentation, and/or corroborating evidence concerning prior art systems is ongoing. Accordingly, Defendants reserve the right to continue to supplement their production as Defendants obtain additional prior art references, documentation, and/or corroborating evidence concerning invalidity during the course of discovery.

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CERTIFICATE OF SERVICE

I hereby certify that a true and correct copy of Defendants' Joint Invalidity Contentions has been sent to counsel of record via electronic mail on this June 10, 2022.

/s/ Robinson Vu
Robinson Vu