

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

APPLE INC.
Petitioner

v.

ARIGNA TECHNOLOGY LTD
Patent Owner

Inter Partes Review Case No. IPR2023-00453
U.S. Patent No. 7,183,835

DECLARATION OF DR. DAVID KUAN-YU LIU

I, David Kuan-Yu Liu, hereby declare the following:

I. BACKGROUND AND QUALIFICATIONS

1. My name is David Kuan-Yu Liu, Ph.D and I am over 21 years of age and otherwise competent to make this Declaration. I make this Declaration based on facts and matters within my own knowledge and on information provided to me by others.

2. I have been retained by counsel for Petitioner as a technical expert in the above-captioned case. Specifically, I have been asked to render certain opinions in regard to the IPR petition with respect to U.S. Patent No. 7,183,835 (the “’835 Patent”). I understand that the Challenged Claims are claims 1 and 2. My opinions are limited to those Challenged Claims.

3. My compensation in this matter is not based on the substance of my opinions or the outcome of this matter. I have no financial interest in Petitioner.

4. In writing this declaration, I have considered my own knowledge and experience, including my work experience in the field of electrical and computer engineering and my experience working with others involved in this field, including in the design and analysis of integrated circuit systems and subsystems. In reaching my opinions in this matter, I have also reviewed the following references and materials:

- The ’835 Patent (Ex. 1001)
- Prosecution History for the ’835 Patent (Ex. 1002)

- U.S. Patent No. 6,906,574 (“Ohi”) (Ex. 1003)
- Machine Translation of JP4531500 (Ex. 1005)
- Dulau, et al., A New Gate Driver Integrated Circuit for IGBT Devices With Advanced Protections, IEEE Transactions on Power Electronics, Vol. 21, No. 1, January 2006 (“Dulau”) (Ex. 1006)
- Any additional background materials cited below

A. Educational Background

5. I received a Bachelor of Science degree in Electrical Engineering from the University of California, Berkeley, in 1983. I received a Master of Science and Ph.D. degrees in Electrical Engineering from Stanford University in 1985 and 1989, respectively.

B. Professional Experience

6. From 1989 to 1992, I was a member of technical staff at Texas Instruments, Inc. At Texas Instruments, my job responsibilities included process integration, device modeling, high-voltage CMOS process integration, and investigating novel source-side injection mechanisms for Flash EPROM channel hot-electron programming.

7. From 1992 to 1995, I was a member of the technical staff at Advanced Micro Devices, Inc. (AMD) where I was a key contributor in optimizing Flash cell and periphery devices in AMD’s CMOS-based 0.5um and 0.35um Flash EPROM technology. My job responsibilities at AMD also included process integration, device modeling, and development of triple-well process technology for accommodate x-decoder transistors and high voltage transistors for negative gate

erase operation. While at AMD, I was awarded a Spotlight Award for developing a method of manufacturing a self-aligned source (SAS) etch for a NOR flash memory.

8. I spent the next five years of my career in managerial and director roles at several California-based semiconductor companies. I was responsible for increasing yield and for leading teams of engineers working to develop next-generation memory devices.

9. In 2000, I co-founded Progressant Technologies in Fremont, California. Progressant Technologies developed IP for negative differential resistance transistor technology and was eventually acquired by Synopsys, Inc.

10. From 2000 to 2004, I was a Senior Manager at Xilinx, Incorporated, where I was responsible for developing nonvolatile memory process technology for flash and CPLD product applications, as well as advanced CMOS process technology (specifically 75nm CMOS technology node, a half node version between 90nm and 65nm). The flash memory products I developed at Xilinx are used as the configuration memory for the FPGA, with the configuration interface between them being the JTAG interface.

11. From 2004 to 2007, I was a Senior Scientist at Maxim Integrated Products where I was responsible for developing Embedded Non-volatile Memory process technology for Power Management product applications.

12. Since 2007, I have served as a technical consultant where I have provided expert advice regarding Flash memory technology, CMOS process technology, and semiconductor device physics.

13. I have 20 years of experience as an engineer and engineering manager/director of Complementary Metal Oxide Semiconductor (CMOS) technology development. During my career, I have worked at some of the leading technology companies in the world, such as Texas Instruments, Advanced Micro Devices, Altera Corporation (now a subsidiary of Intel Corp.), and Xilinx. At these companies, my work focused on various aspects of CMOS and semiconductor technology.

14. I hold over 95 U.S. patents, a large number of which are directed to logic CMOS processes technology and high voltage CMOS process technology. The vast majority of my patents are in the area of CMOS process technology and memory architecture. As such, I am intimately familiar with the implementation of integrated process flows that essentially are repetitive sequences of modules, each composed of a layer patterning step followed by selective deposition and etching of various semiconductor materials, with the area of selectivity dictated by the layer patterning.

15. I have also authored several technical papers that have been published in well-respected, peer-reviewed journals, such as the IEEE Electron Device Letters, the IEEE Journal of Solid-State Circuits, and the IEEE Transactions on Electron

Devices. As an example, I worked on a new conductivity-modulated Power MOSFET that features a buried minority-carrier injector to enhance the current conduction capability of the Power MOSFET. This work was published in the IEEE Transactions on Electron Devices. It is worth noting that this new conductivity modulated Power MOSFET is essentially a hybrid between an IGBT and a regular power MOSFET.

16. My curriculum vitae, which includes a more detailed summary of my background, experience, and publications, is attached as Appendix A.

II. LEGAL FRAMEWORK

17. I am a technical expert and do not offer any legal opinions. However, counsel has informed me as to certain legal principles regarding patentability and related matters under United States patent law, which I have applied in performing my analysis and arriving at my technical opinions in this matter.

18. I have been informed that the Patent Trial and Appeal Board (“PTAB”) now applies the claim construction standard applied by Article III courts (i.e., the *Phillips* standard) regardless of whether a patent has expired. I have been informed that under the *Phillips* standard, claim terms are to be given the meaning they would have to a person having ordinary skill in the art at the time of the invention, taking into consideration the patent, its file history, and, secondarily, any applicable extrinsic evidence (e.g., dictionary definitions). In my analyses below, I have applied

the plain and ordinary meaning pursuant to the *Phillips* standard for all claim language.

19. I understand that a prior art reference “anticipates” a claim, and thus renders the claim invalid, if all elements of the claim are disclosed in that prior art reference, either explicitly or inherently (*i.e.*, necessarily present or implied). This requirement is not met if a single limitation of the claim is missing from the prior art reference.

20. I understand that a prior art reference can disclose a particular claim element for anticipation purposes even if the reference does not explicitly identify that claim element. In particular, I understand that even if a prior art reference does not expressly disclose a limitation, it anticipates that claim limitation if a POSITA would have understood the prior art to disclose the limitation.

21. I have also been informed that a prior art reference can inherently disclose a claim element if that limitation is necessarily present when practicing the teachings of the reference, regardless of whether a POSITA would have recognized the presence of that limitation in the prior art reference. I understand that inherency cannot be established by mere probabilities or possibilities.

III. OPINION

A. Level of a Person of Ordinary Skill in the Art

22. I was asked to provide my opinion as to the level of skill of a person of ordinary skill in the art (“POSITA”) of the ’835 Patent at the time of the claimed invention, which counsel has told me to assume is January 6, 2004. In determining the characteristics of a hypothetical person of ordinary skill in the art of the ’835 Patent, I considered several factors, including the type of problems encountered in the art, the solutions to those problems, the rapidity with which innovations are made in the field, the sophistication of the technology, and the education level of active workers in the field. I also placed myself back in the time frame of the claimed invention and considered the colleagues with whom I had worked at that time.

23. In my opinion, a POSITA at the time of the claimed invention of the ’835 Patent would have had at least a graduate degree in electrical engineering or equivalent with at least two years of relevant work experience (e.g., in the field of circuit design). Additional education or experience might substitute for the above requirements. Such a POSITA would have been capable of understanding the ’835 Patent and the prior art references discussed herein.

24. Based on my education, training, and professional experience in the field of the claimed invention, I am familiar with the level and abilities of a person of ordinary skill in the art at the time of the claimed invention. Additionally, I met at least these minimum qualifications to be a person having ordinary skill in the art as of the time of the claimed invention of the ’835 Patent.

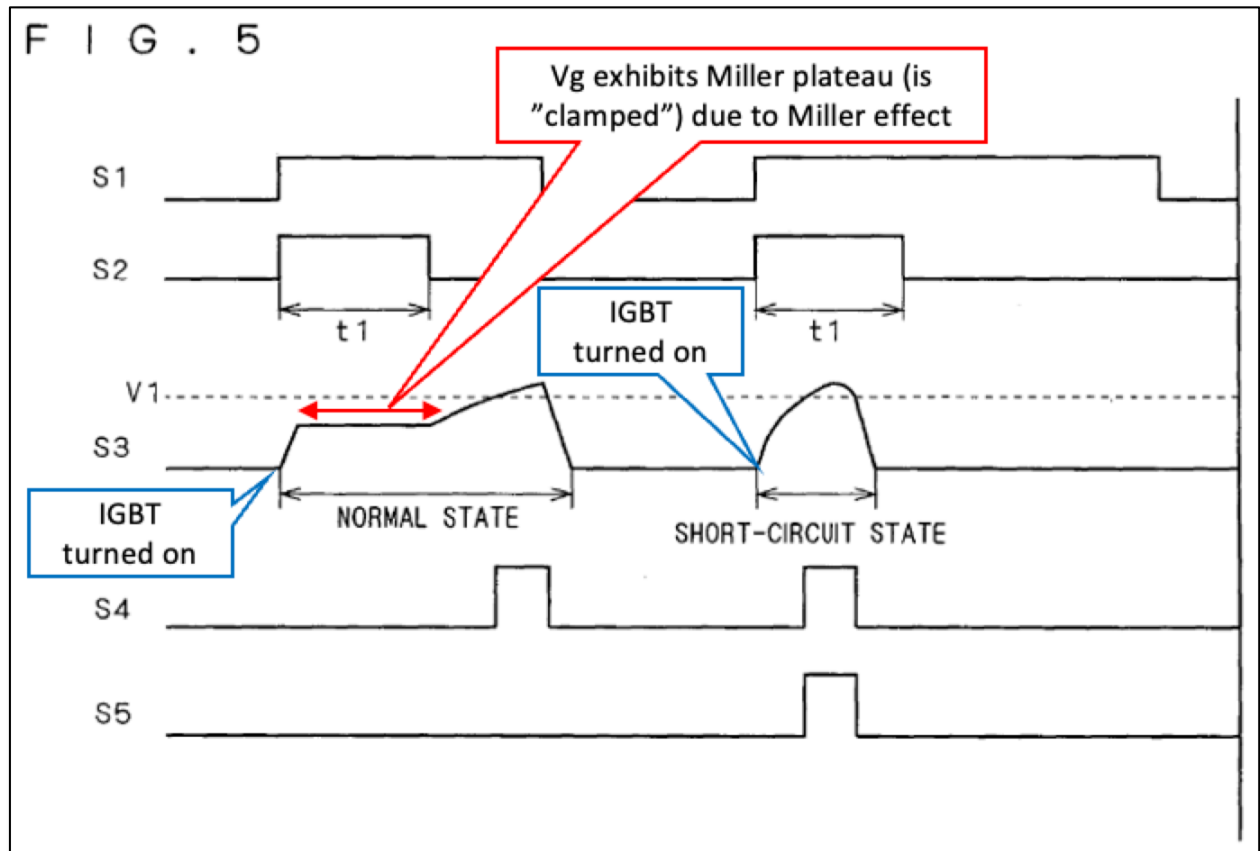
B. Description of the Alleged Invention of the '835 Patent

25. The '835 Patent is generally directed to a semiconductor device that controls the drive of an insulated gate bipolar transistor (IGBT) and provides a short-circuit protection for the IGBT. '835 Patent (Ex. 1001), 1:10-25. More specifically, “[t]he short-circuit is detected by monitoring the control output signal of the insulated gate transistor, and in case of the short-circuit, the short-circuit protection of the insulated gate transistor is performed by forcing the control device to stop that control output signal.” *Id.* at Abstract.

26. The short-circuit protection proposed by the '835 Patent is premised on a phenomenon in IGBT devices referred to in the field as the “Miller effect.” This phenomenon is well understood in the field. *See, e.g., Dulau* (Ex. 1006). According to the Miller effect, when an IGBT is turned on under normal operating conditions, the gate voltage of the IGBT initially increases and then plateaus (referred to as a “clamped” voltage) for a period of time before finally increasing to a normal operating voltage. *See, e.g., Dulau* (Ex. 1006), Fig. 3. This period when the gate voltage is clamped is commonly referred to in the field as the “Miller plateau.” *Id.*

27. The '835 Patent refers to the Miller plateau as “a clamp period.” '835 Patent (Ex. 1001), 5:62-6:62. The '835 Patent describes that, during the “clamp period,” the gate voltage is “clamped to a certain voltage for a determined period by

a [Miller]¹ effect.” *Id.* at 5:62-6:3. Conversely, in the event of a short-circuit condition, “a clamp period of the voltage does not exist . . . and the voltage . . . rises rapidly to be almost equal to that of the drive voltage[.]” ’835 Patent (Ex. 1001), 6:54-62. This difference is depicted in Fig. 5 below:



Id. at Fig. 5 (annotated).

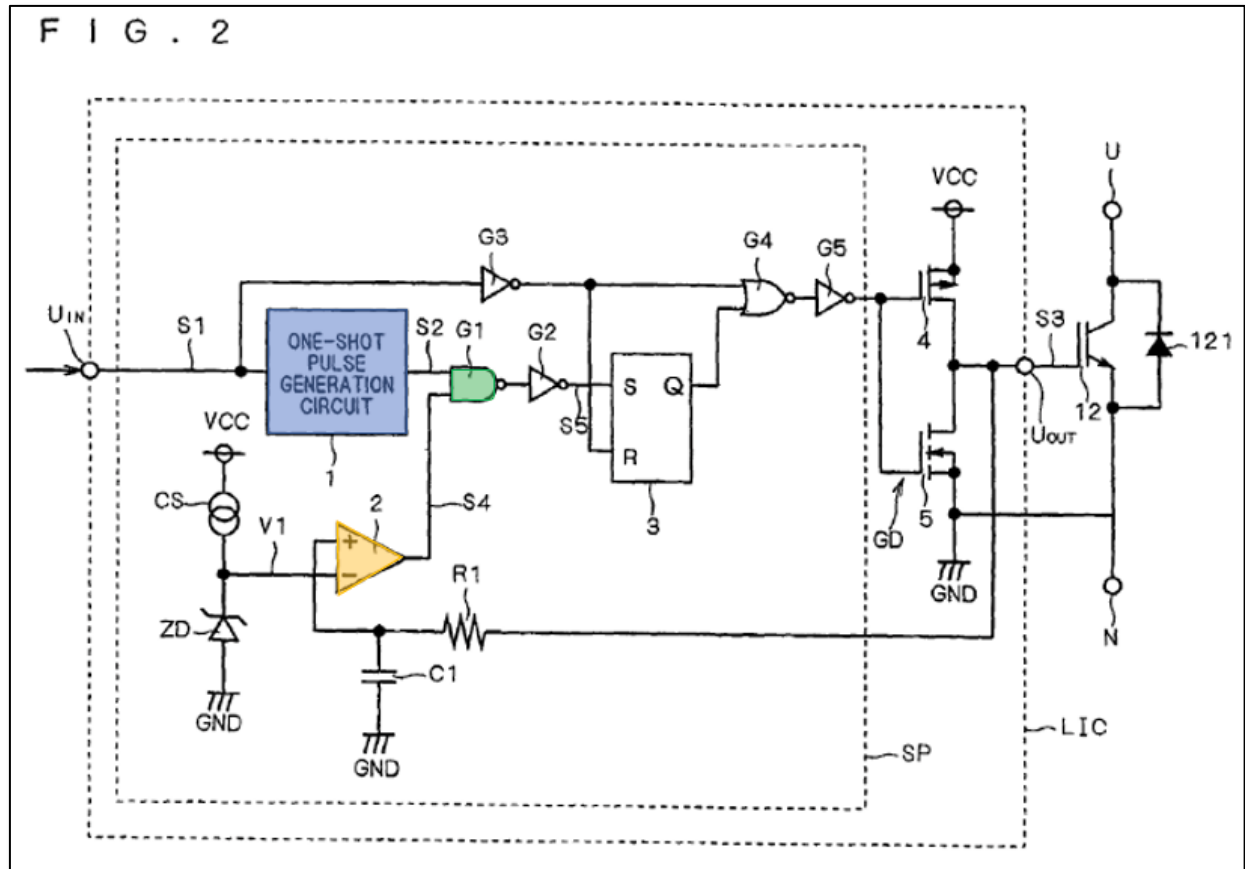
¹The ’835 Patent contains a typo, reciting “mirror effect,” rather than “Miller effect.” From my analysis and understanding, given the context of this language and my personal knowledge of the Miller effect, it is my opinion that this is a simple clerical error and should be read as “Miller effect.” I have reviewed a machine translation of the corresponding Japanese patent application, which confirms the intended phrase was “Miller effect.” Machine Translation of JP4531500 (Ex. 1005), 2:10 (“Therefore, the voltage of the control output signal S3 is set to a predetermined value due to the Miller effect.”).

28. This absence of a Miller plateau characteristic during a short-circuit state forms the foundation of the '835 Patent's process of detecting a short circuit state. The '835 Patent teaches that this clamped/Miller plateau should be used to define a short-circuit detection period t_1 :

[T]he one-shot pulse generation circuit 1 outputs the pulse signal S2 which comes to be in the significant condition according to the building up of the control input signal S1, and **a period t_1 in the significant condition, in the "H" state in this case, is set to be almost equal to a period when the control output signal S3 is clamped to a certain voltage.**

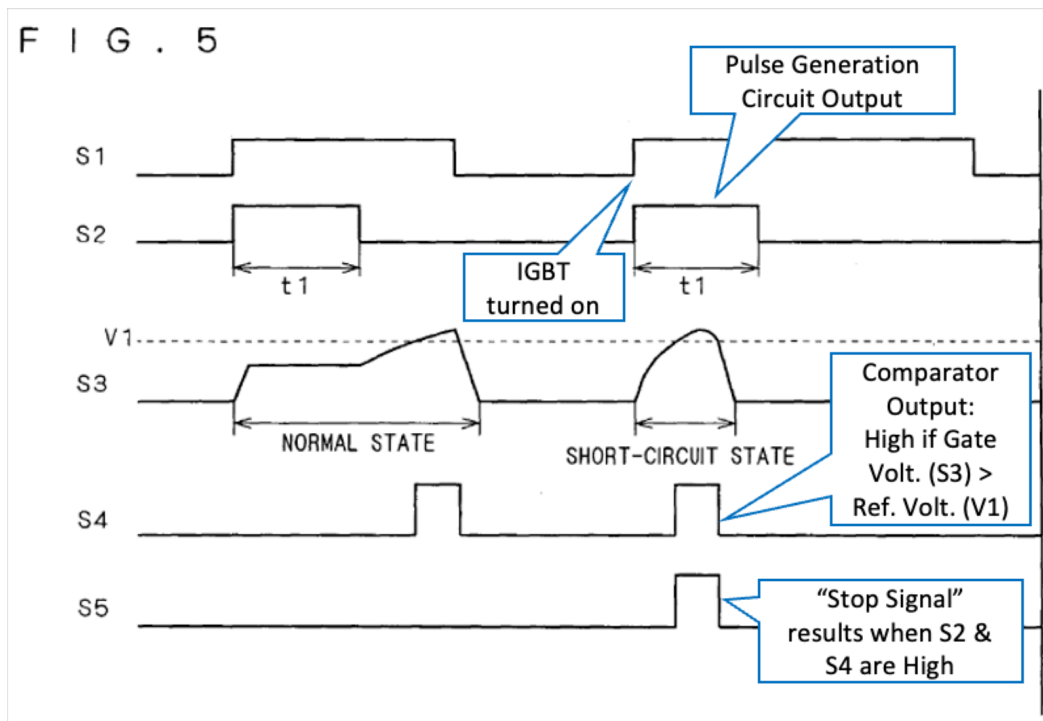
Id. at 6:35-40 (emphasis added). As illustrated in Fig. 5 above, the Miller effect clamping prevents the IGBT gate voltage from exceeding reference voltage V_1 during the measurement period, when the IGBT is operating in the normal state. Because a short circuit condition will not be similarly clamped, V_g will exceed the reference voltage V_1 even within the time period t_1 . As illustrated in Fig. 5 above, if V_1 is reached within the time period t_1 , the system assumes the IGBT is short circuited. When such a short circuit condition is detected, the '835 Patent proposes turning-off the IGBT by "forcing the driver to stop the control output signal." *Id.* at 1:52-62.

29. As illustrated in Fig. 2 below, the short-circuit protection circuit proposed by the '835 Patent includes three main elements: a pulse generation circuit, a comparator, and a logical circuit:



Id. at Fig. 2 (annotated). As illustrated, the **pulse generation circuit (1)** receives a control input signal (U_{IN})—the signal that causes IGBT 12 to turn on—and outputs a first pulse signal (S2) that is maintained as a high signal during the detecting period t_1 corresponding to the period of Miller plateau/clamped voltage. *Id.* at 4:56-60; 6:35-40. The **comparator (2)** compares the gate voltage of IGBT 12 (S3) to a reference voltage (V1), and outputs a high signal when the gate voltage exceeds the reference voltage. *Id.* at 4:27-42. Finally, the **logical circuit (G1)** receives the outputs from the pulse generation circuit (S2) and the comparator (S4) and outputs a “stop signal” when both outputs are high, forcing IGBT 12 into an off state. *Id.* at 7:4-21.

30. In sum, the proposed circuit can detect a short circuit when the gate voltage of IGBT 12 exceeds reference voltage (V_1) within a detecting period t_1 corresponding to the duration of the Miller plateau. When such a state is detected, the protection circuit forces IGBT 12 to an off state. Fig. 5 below is annotated to reflect this process:



Id. at Fig. 5 (annotated). Thus, the circuit in the '835 Patent focuses on this concept of forcing IGBT 12 to an off state when the gate voltage of IGBT 12 exceeds reference voltage (V_1) within the detecting period t_1 corresponding to the Miller plateau.

C. Opinions Related to *Ohi*

i. Overview of Ohi (Ex. 1003)

31. In the subsequent paragraphs, I address the purpose, structure, and operating modes of *Ohi*'s invention particularly relevant to my opinions below.

ii. Ohi's Purpose and Problem to Solve

32. Like the '835 Patent, *Ohi* is directed to "drive circuit[s] for driving a power semiconductor device and for detecting occurrence of an abnormality in the power semiconductor device." *Ohi* (Ex. 1003), 1:8-10. *Ohi*'s drive circuits are "capable of promptly detecting occurrence of a short circuit so as to protect the power semiconductor device even when applied to a high-voltage IGBT." *Id.* at 2:35-41.

33. Like the '835 Patent, the drive circuits taught by *Ohi* are also premised on the Miller effect. Namely, *Ohi* describes a "Miller time period" during which the IGBT's gate voltage is clamped:

When the drive circuit sends a gate instruction to instruct the IGBT 11 to turn on in response to a turn-on instruction under normal operating conditions, the gate voltage V_g of the IGBT 11 starts rising. When the gate voltage V_g then exceeds a threshold voltage, the collector current I_c starts increasing. When the collector current I_c flowing in the IGBT 11 becomes nearly equal to an inductive load electric current flowing through the inductive load, the collector-emitter voltage V_{ce} starts decreasing and **the gate voltage V_g then becomes a nearly-constant voltage. This time period** during which the gate voltage V_g is nearly constant after the collector current I_c has become nearly equal to the inductive load electric current **is known as a Miller time period. . . . At the conclusion of the Miller**

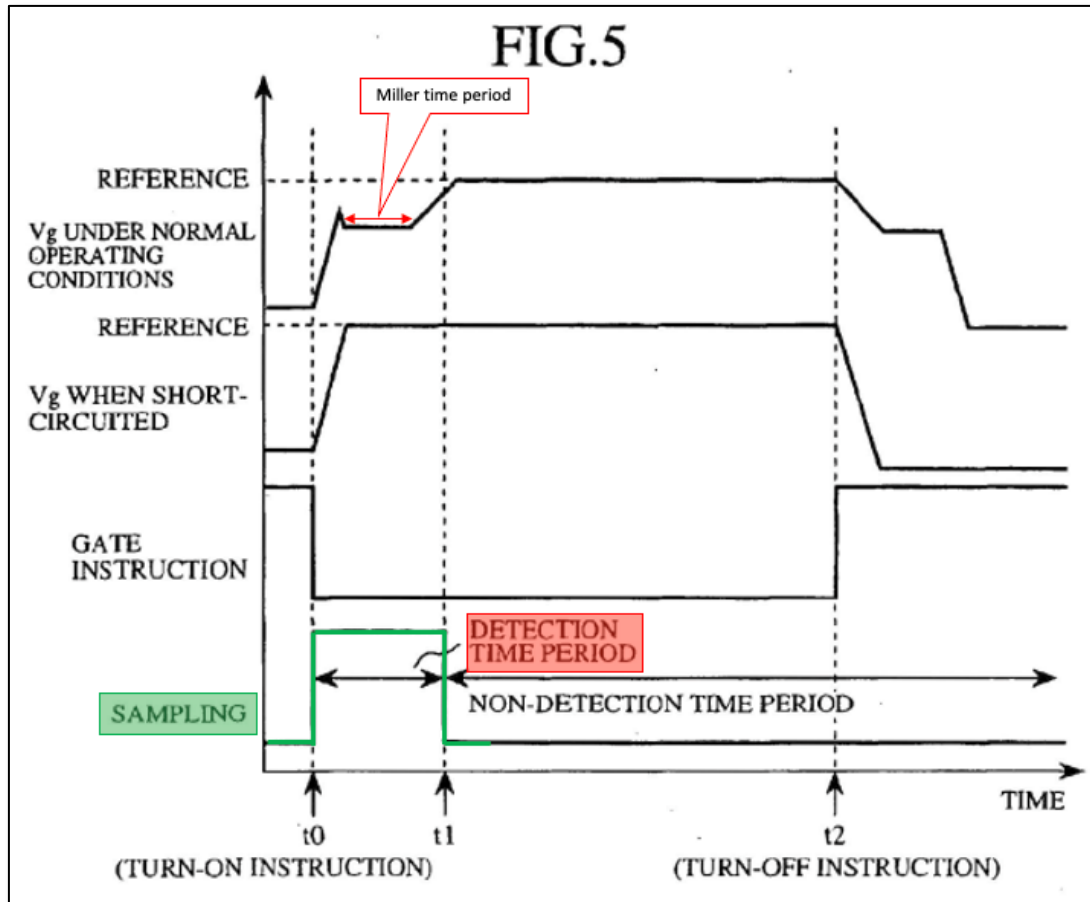
time period, the gate voltage V_g starts rising again. At this time, the gate voltage rises slowly with a smaller time constant than that with which the gate voltage has risen before the Miller time period because the feedback capacitance is large, and then reaches a certain on-state gate voltage. The gate voltage V_g enters a steady state after it has experienced the above-mentioned transition time period.

Id. at 5:61-6:25 (emphasis added). Also like the '835 Patent, *Ohi* uses the Miller time period (i.e., the time during which the IGBT gate voltage is clamped) to define the measurement/detection period during which V_g is monitored, ensuring that the detection period ends before V_g reaches its normal operating voltage when not short circuited:

[W]hen the control logic 12 receives a turn-on instruction from outside the drive circuit, as shown in FIG. 5, the **sampler 16 enables the gate voltage detector 17 to detect the gate voltage V_g at the time t_0 when the turn-on instruction is received.** After that, **when a certain time elapses and a time t_1 (before the gate voltage V_g reaches the on-state gate voltage, and the time t_1 is determined in consideration of the characteristics of the IGBT 11) comes, the sampler 16 disables the gate voltage detector 17 to detect the gate voltage V_g .** The **sampler 16 only has to be able to prevent the detection of the gate voltage V_g during a time period from the time t_1 to a time t_2** when a turn-off instruction is received, and the detection time period from the time t_0 to the time t_1 can include an off-state time period (i.e., a time period before the time t_0 or a time period after the time t_2).

The gate voltage detector 17 detects the gate voltage V_g that appears at the gate terminal of the IGBT 11 throughout the detection time period during which the sampler 16 enables the process of detecting the gate voltage V_g . **When the gate voltage V_g exceeds the reference value during the detection time period, the gate voltage detector 17 recognizes the occurrence of an abnormality in the IGBT 11 and delivers an abnormality signal to the control logic 12 and the turn-off speed control circuit 15.**

Id. at 7:32-56 (emphasis added). This timing depicted in Fig. 5 below:



Id. at Fig. 5 (annotated).

34. Finally, like the '835 Patent, *Ohi* teaches a short circuit detection method based on the fact that the gate voltage during normal operation will clamp for a period of time (i.e., the Miller plateau), but will not when short circuited. Namely, when a high-voltage IGBT is turned on, the gate voltage of the IGBT “doesn’t change to a steady-state value (i.e., a value acquired according to the static characteristics of the IGBT) instantaneously.” *Id.* at 2:18-21. Instead, due to the Miller effect, the gate voltage of the IGBT “reaches the steady-state value at the expiration of a certain transition time interval after the IGBT has been turned on.”

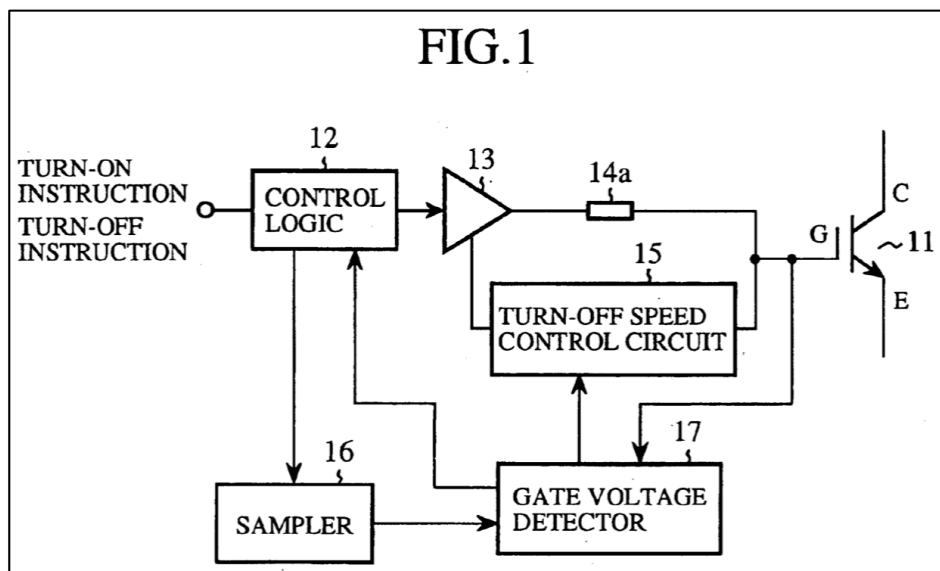
Id. at 2:18-21. In contrast with this normal operation, “[in a] short circuit state, the gate voltage V_g . . . has no Miller time period, and rapidly rises up to the on-state gate voltage.” *Id.* at 6:45-48; *see also id.* at 15:3-4 (“when a short circuit occurs in the IGBT [], there is no Miller time period”). *Ohi* proposes to solve the abovementioned problems by monitoring the IGBT gate voltage during the Miller time period “to detect the short-circuit state by detecting a difference in the gate voltage V_g between when the IGBT is under normal operating conditions and when a short circuit occurs in the IGBT.” *Id.* at 6:53-57.

35. In sum, both *Ohi* and the '835 Patent are directed to controlling semiconductor IGBT devices, detecting short circuit conditions in said IGBTs, and turning off the IGBTs when such a short circuit is detected. *Compare id.* at 2:35-41 (“[I]t is [] an object of the present invention to provide a high-reliability drive circuit for driving a power semiconductor device, capable of promptly detecting occurrence of a short circuit so as to protect the power semiconductor device even when applied to a high-voltage IGBT.”), *with '835 Patent* (Ex. 1001), 1:10-15 (“The present invention relates to a semiconductor device and a semiconductor device module, and more particularly, it relates to a semiconductor device and a semiconductor device module including a short-circuit protection function of an insulated gate type switching device such as an IGBT[.]”), Abstract (“The short-circuit is detected by monitoring the control output signal of the insulated gate transistor, and in case of

the short-circuit, the short-circuit protection of the insulated gate transistor is performed by forcing the control device to stop that control output signal.”).

iii. *Ohi's Drive Circuits*

36. Fig. 1 of *Ohi* below provides a block diagram that depicts the general “structure of a drive circuit for driving a power semiconductor device” according to the first embodiment in *Ohi*—concepts that also carry over to subsequent embodiments. *Id.* at 4:37-38. With reference to Fig. 1 below, “the power semiconductor device driven by the drive circuit” may be “an IGBT (Insulated Gate Bipolar Transistor)[.]” *Id.* at 4:40-42.

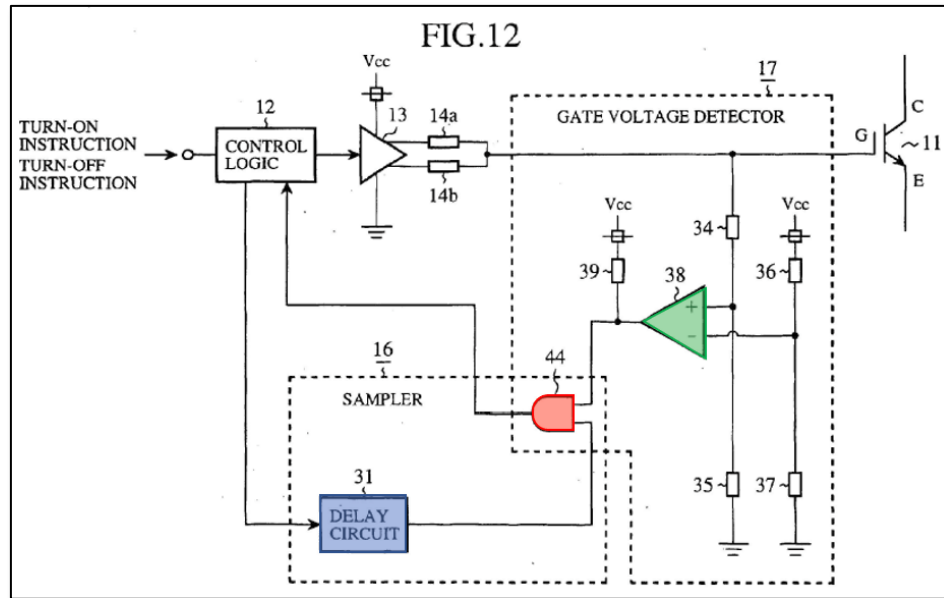


Id. at Fig. 1.

37. “Reference numeral 12 denotes a control logic for sending a gate instruction to turn on the IGBT 11 to a buffer 13 in response to a turn-on instruction from outside the drive circuit, and for sending a gate instruction to turn off the IGBT

11 to the buffer 13 in response to a turn-off instruction from outside the drive circuit.” *Id.* at 4:45-50. Fig. 1 also generally depicts short circuit detection aspects of *Ohi*’s embodiments. For example, “[r]eference numeral 16 denotes a sampler (i.e., a controllable variable value detection means) for allowing a process of detecting a gate voltage V_g . . . of the IGBT 11 only during a transition time period . . . immediately after the control logic 12 has received a turn-on instruction[.]” *Id.* at 4:64-5:3. “[R]eference numeral 17 denotes a gate voltage detector (i.e., a controllable variable value detection means and an abnormality detection means) that detects the gate voltage V_g that appears at the gate terminal of the IGBT 11 . . . throughout a time period during which the sampler 16 allows the process of detecting the gate voltage V_g [.]” *Id.* at 5:4-11.

38. *Ohi*’s fifth embodiment, as depicted in Fig. 12 below, utilizes three key components to detect a short circuit abnormality immediately following a turn-on instruction: (1) **Delay circuit 31 in sampler 16** that generates a *first pulse signal* that defines the “detection time period during which the gate voltage V_g of an IGBT is detected[.]” (2) **comparator 38** that output a *second pulse signal* when gate voltage V_g of the IGBT exceeds a threshold voltage, and (3) **AND circuit 44** that receives the first and second pulse signals and outputs a High signal when V_g exceeds the threshold during the detection time period. *Id.* at 12:32-58.



Id. at Fig. 12 (annotated). When a short circuit condition is encountered during the detection time period, **logical circuit 44** generates a stop signal that causes IGBT to be turned off. *Id.* at 12:53-60 (“[W]hen a short circuit occurs in the IGBT 11, the output-signal of the AND circuit 44 becomes a High level (i.e., a logical level indicating a detection of the occurrence of an abnormality in the IGBT . . . [.] After that, the drive circuit operates in the same way as that of embodiment 2 does[.]”), 10:14-21 (describing embodiment 2, teaching that the circuit “delivers an abnormality signal to the control logic 12[, and, a]s a result, the control logic 12 causes the IGBT 11 to become turned-off[.]”).

39. For clarity it is worth making a brief point about the structure of *Ohi*’s disclosure and the components that I discuss here. *Ohi* expressly teaches that its fifth embodiment includes components and functionalities identical to those in earlier described embodiments and does not repeat descriptions of functionalities that are

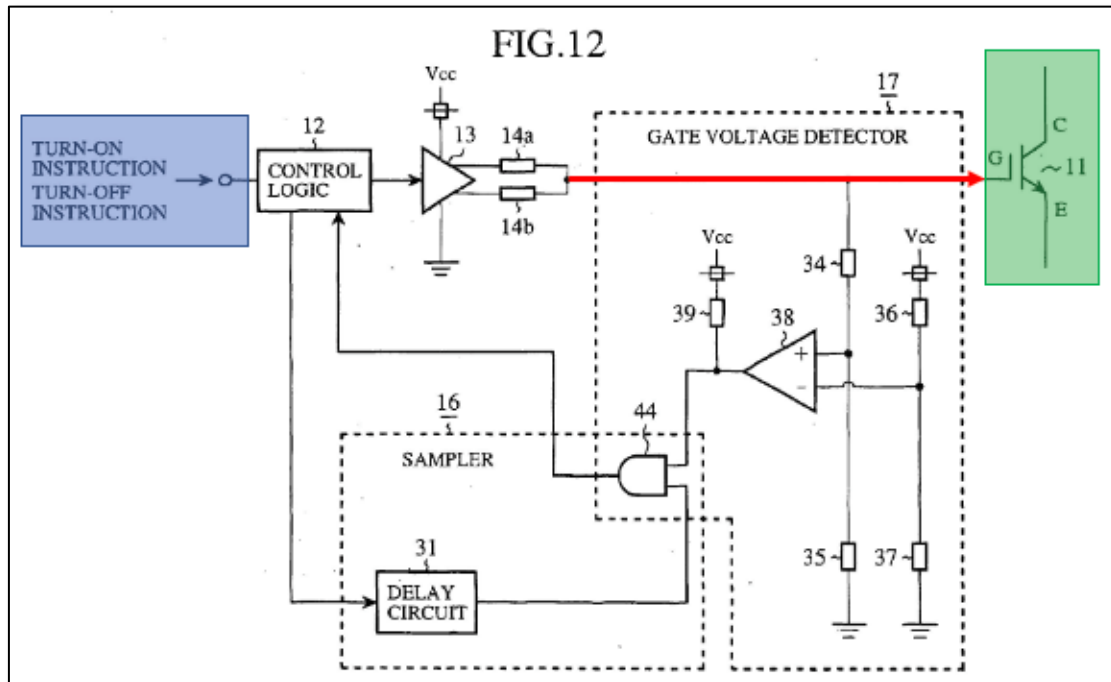
common between its various embodiments. *See, e.g., Ohi* (Ex. 1003), 12:19-25 (“In [Fig. 12], because the same reference numerals as shown in FIG. 6 denote the same components as those of the second embodiment or like components, the explanation of those components will be omitted hereafter.”), 12:59-61 (noting “the drive circuit operates in the same way [as] that of embodiment 2 [], and therefore the description of the operation will be omitted hereafter”). Throughout my declaration, I have cited the applicable description of the Fig. 12 circuit and its operation. Some of those descriptions are contained within discussions of earlier embodiments, including the second embodiment as depicted in Fig. 6. Although Figs. 6 and 12 share certain components and functionality, my opinions regarding invalidity focus on *Ohi*’s fifth embodiment as depicted in Fig. 12. I have not separately considered whether *Ohi*’s circuit depicted in Fig. 6 also satisfies the Challenged Claims.

D. Opinions Supporting Anticipation

1. *Claim 1[P] A semiconductor device controlling a drive of an insulated gate transistor by generating a control output signal on a basis of a control input signal, comprising:*

40. *Ohi* discloses a semiconductor device that controls the drive of an insulated gate transistor (i.e., an IGBT) by generating a control output signal on a basis of a control input signal. The following annotated Fig. 12 from *Ohi* illustrates a semiconductor circuit that receives **turn-on and turn-off instructions** (control input

signal) and uses those instructions to generate a **gate instruction** (control output signal) for turning on and off an **insulated gate bipolar transistor** (IGBT):



Ohi (Ex. 1003), Fig. 12 (annotated). As depicted above, control logic 12 is configured “for sending a **gate instruction** to turn on the **IGBT 11** to a buffer 13 in response to a **turn-on instruction** from outside the drive circuit, and for sending a **gate instruction** to turn off the **IGBT 11** to the **butter 13** in response to a **turn-off instruction** from outside the drive circuit.” *Id.* at 4:45-50.

41. *Ohi*’s embodiments are directed to drive circuits for driving power semiconductor devices such as an IGBT and detecting short circuits in such semiconductor devices:

The present invention is proposed to solve the above-mentioned problems, and it is therefore an object of the present invention to provide a high-reliability **drive circuit for driving a power**

semiconductor device, capable of promptly detecting occurrence of a short circuit so as to protect the power semiconductor device even when applied to a high-voltage IGBT.

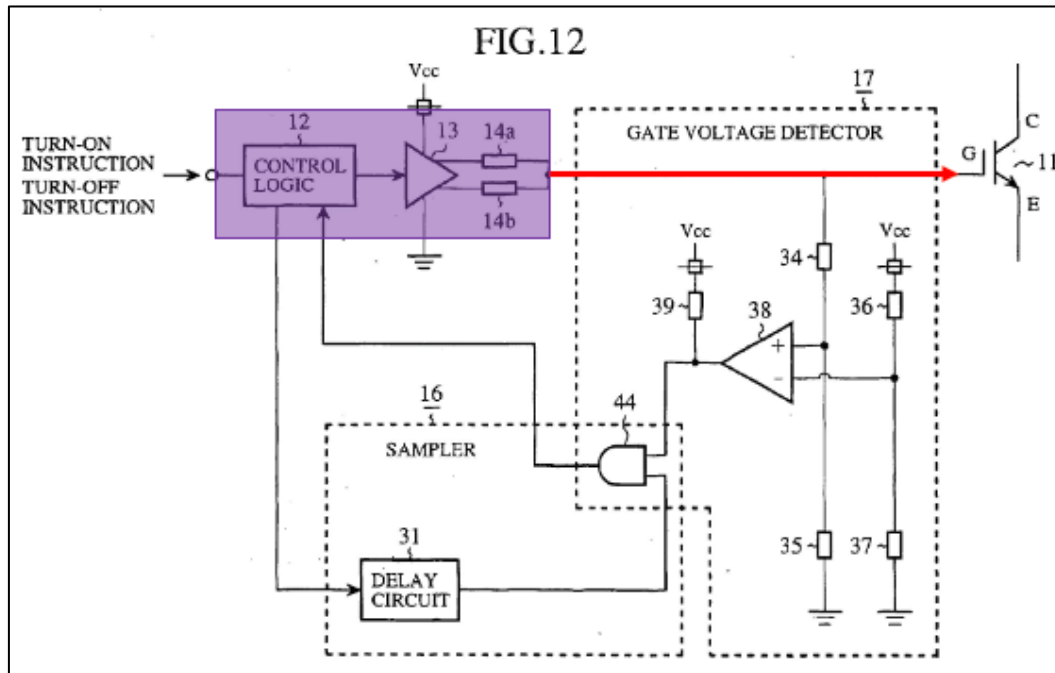
Id. at 2:35-41 (emphases added).

42. Although *Ohi* does not expressly describe the drive circuit as a semiconductor device, a POSITA would have understood that *Ohi*'s drive circuit is a semiconductor device that drives a power semiconductor IGBT. Indeed, *Ohi*'s drive circuit receives a simple on/off input instruction, drives a semiconductor IGBT, and is composed of standard logic components, which would lead that a POSITA to conclude that this drive circuit is a semiconductor device. Implementing these components as a semiconductor device would have produced a smaller, faster, and less expensive circuit than an alternative embodiment constructed of discrete electronic components. The simple on/off input instruction processed by *Ohi*'s drive circuits is well-suited for the depicted semiconductor logic circuit, avoiding the more complicated power electronics that would be required to implement *Ohi*'s circuit with discrete components.

2. ***Claim 1[a]: a driver outputting said control output signal and***

43. As I discussed above, Fig. 12 includes control logic 12 configured “for sending a gate instruction to turn on the IGBT 11 to a buffer 13 in response to a turn-on instruction from outside the drive circuit, and for sending a gate instruction to turn off the IGBT 11 to the buffer 13 in response to a turn-off instruction from

outside the drive circuit.” *Ohi* (Ex. 1003), 4:45-50. As annotated below in Fig. 12, control logic 12, buffer 13, and gate resistors 14a and 14b make up a driver for outputting the control output signal:



Id. at Fig. 12 (annotated).

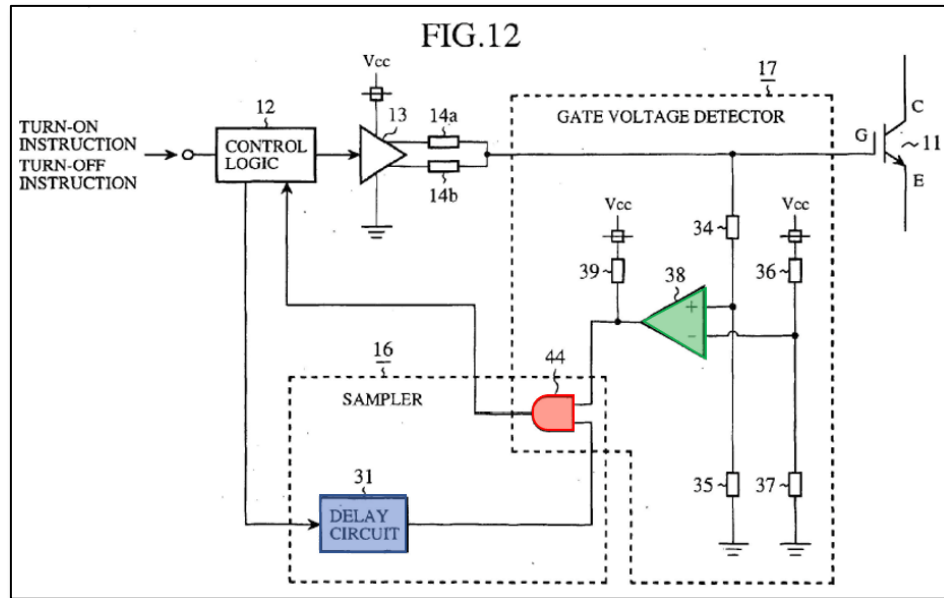
44. *Ohi* explains that the role of buffer 13 is to *amplify* the gate instruction generated by control logic 12 in response to control logic 12 receiving a turn-on (or turn-off) instruction from outside the circuit:

In response to a turn-on instruction from outside the drive circuit, the **control logic 12 delivers a gate instruction to cause the IGBT 11 become turned-on to the buffer 13**. When receiving the gate instruction to cause the IGBT 1 to become turned-on from the control logic 12, the **buffer 13 amplifies the gate instruction** and delivers the amplified gate instruction to the gate of the IGBT 11 by way of the on-state gate resistor 14a. As a result, the IGBT 11 becomes turned-on.

Id. at 7:1-9 (emphasis added); *see also id.* at 7:10-19 (similar description with respect to turning off the IGBT). Given that control logic 12, buffer 13, and the gate resistors work in concert to produce a control output signal that is a function of the control input signal, a POSITA would understand that this group of components satisfies the claimed driver outputting a control output signal.

3. ***Claim 1[b]: a short-circuit protection circuit detecting said control output signal and controlling and forcing said driver to stop said control output signal when a detecting voltage of said control output signal exceeds a predetermined reference voltage before a predetermined period passes after said control output signal indicates a conduction of said insulated gate transistor,***

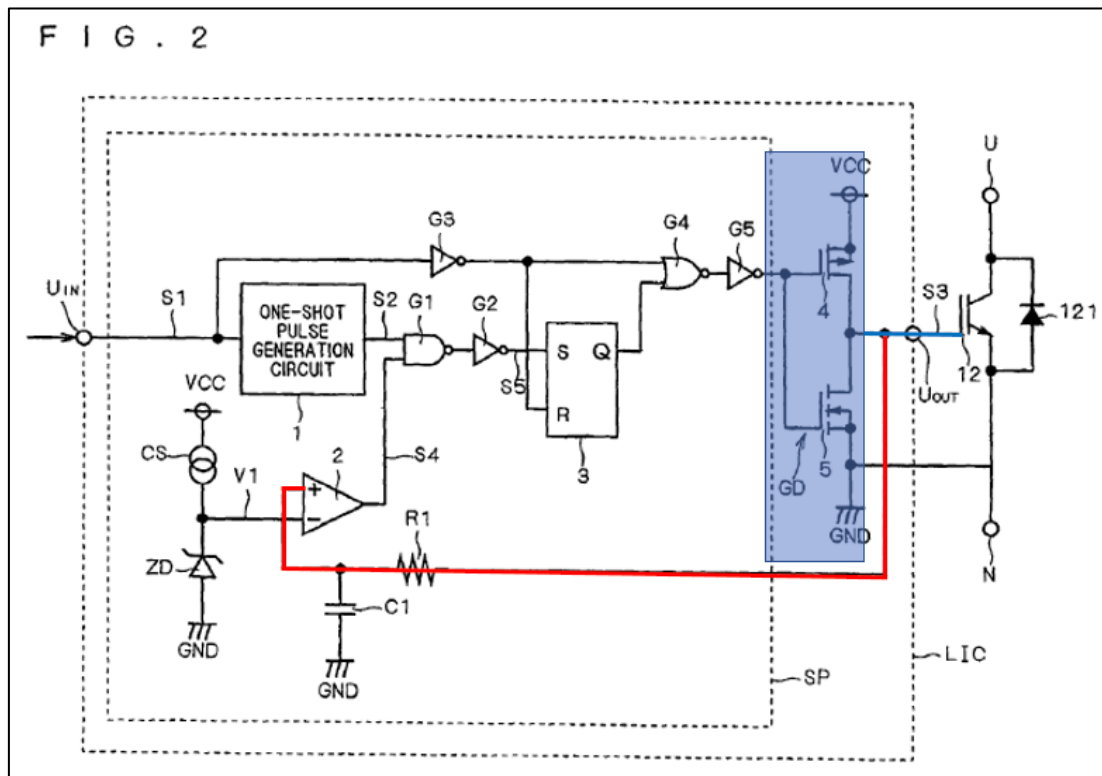
45. As I discussed above, the fifth embodiment, as depicted in Fig. 12 below, utilizes three key components to detect a short circuit abnormality immediately following a turn-on instruction: (1) **sampler 16** (including **delay circuit 31** in the Fig. 12 embodiment) that generates a *first pulse signal* that defines the “detection time period during which the gate voltage V_g of an IGBT is detected[,]” (2) **comparator 38** that outputs a *second pulse signal* when gate voltage V_g of the IGBT exceeds a threshold voltage, and (3) **AND circuit 44** that receives the first and second pulse signals and outputs a High signal when V_g exceeds the threshold during the detection time period. *Id.* at 12:32-58.



Id. at Fig. 12 (annotated). When a short circuit condition is encountered, **logical circuit 44** generates a stop signal to the control logic that causes IGBT to be turned off. *Id.* at 12:53-60 (“[W]hen a short circuit occurs in the IGBT 11, the output-signal of the AND circuit 44 becomes a High level (i.e., a logical level indicating a detection of the occurrence of an abnormality in the IGBT . . . [.] After that, the drive circuit operates in the same way that that of embodiment 2 does[.]”), 10:14-21 (describing embodiment 2, teaching that the circuit “delivers an abnormality signal to the control logic 12[, and, a]s a result, the control logic 12 causes the IGBT 11 to become turned-off[.]”).

46. This limitation recites a “detecting voltage of said control output signal[.]” Although somewhat confusing language, a POSITA would understand this is satisfied by detecting/measuring the gate voltage of the IGBT. The ’835 Patent teaches a control output signal that drives the IGBT gate. Accordingly, the detecting

voltage of control output signal is the measured gate voltage. Indeed, as illustrated in Fig. 2, the '835 Patent equates measuring the gate voltage with a *detecting voltage of control output signal*:



'835 Patent (Ex. 1001), Fig. 2 (annotated), 4:27-35 (“**gate driver GD . . . supplye[s] a control output signal S3** to the gate electrode of the transistor 12, and it is **inputted to . . . comparator 2 as a detecting voltage of the control output signal S3**”). Similarly, with reference to Fig. 6, the '835 Patent equates a divided-down gate voltage with the *detecting voltage of control output signal*. *Id.* at 7:54-63 (describing the IGBT gate voltage S13 and noting “the control output signal S13 is resistively **divided between a resistance R11 and a resistance R12 and is inputted to a + (plus) side**

input terminal of a **comparator 13 as a detecting voltage of the control output signal S13[.]**). Accordingly, a POSITA would understand that a “detecting voltage of said control output signal” is a measured gate voltage or a divided down representation of the measured gate voltage.

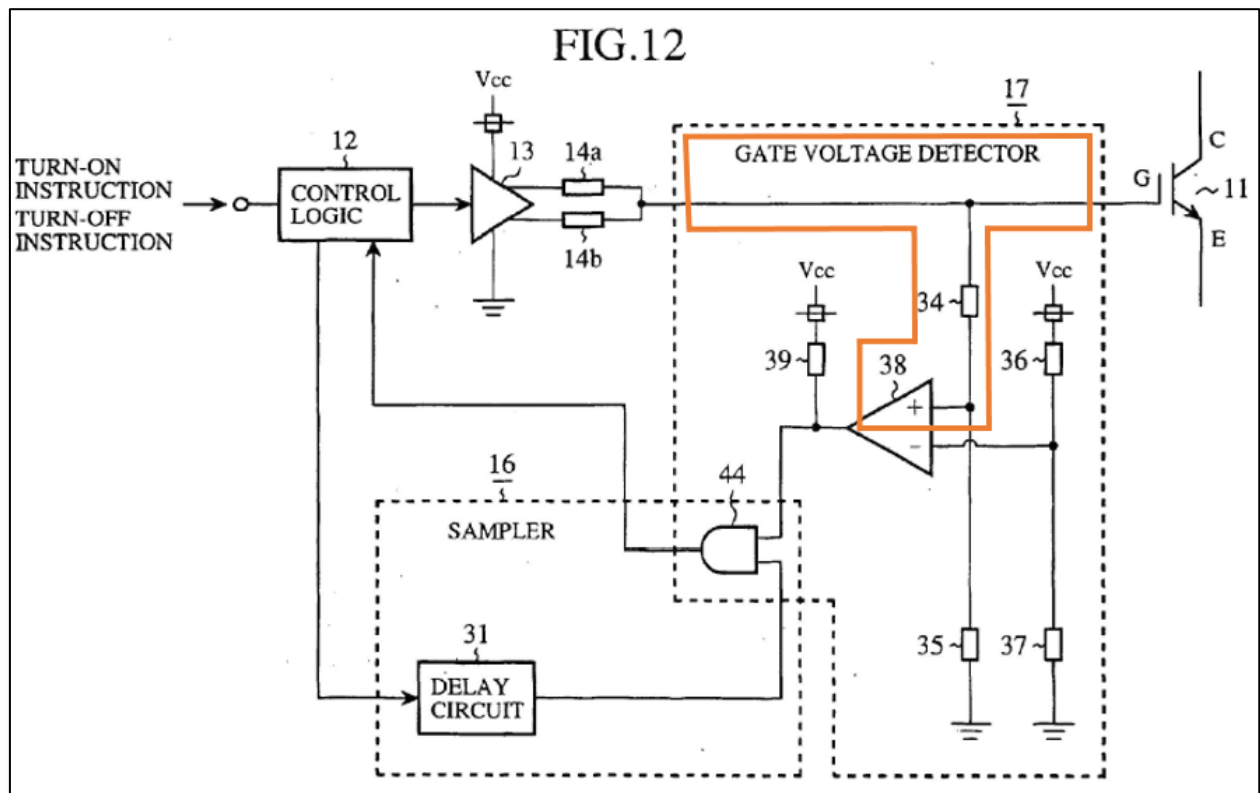
47. A divided down voltage may be obtained from a voltage divider that produces an output voltage that is a fraction of its input voltage. The voltage division is the result of distributing the input voltage among the components of the voltage divider. One example of a voltage divider is two resistors connected in series, with the input voltage applied across the resistor pair and the output voltage emerging from a connection between the two resistors. Indeed, resistively dividing down a voltage measurement from a given node is a well understood means of producing a ratioed and smaller, but representative measurement of the node.

48. *Ohi* teaches this precise arrangement. Namely, the drive circuit in *Ohi* includes a gate voltage detector 17 that provides a divided down representation of the gate terminal of IGBT 11 to comparator 38:

The comparator 38 of a gate voltage detector 17 compares a **divided voltage obtained from the gate voltage V_g of the IGBT** with a divided voltage obtained from the control voltage V_{cc} of the IGBT, like that of above-mentioned embodiment 2, and, when the gate voltage V_g reaches the control voltage V_{cc} in level, causes its output signal to make a transition from a Low level to a High level (see Fig. 13).

Ohi (Ex. 1003), 12:37-44 (emphasis added); *see also id.* at 5:4-9 (gate voltage detector 17 “detects the gate voltage V_g that appears at the gate terminal of the IGBT

11, as the controllable variable value that is applied to the IGBT 11 and is controlled by the buffer 13”). As I discussed above, the output of buffer 13 satisfies the claimed *control output signal*. Accordingly, the claimed *detecting voltage of said control output signal* is a divided down gate voltage of IGBT 11, which is performed by gate voltage detector 17 in *Ohi*’s Fig. 12. This arrangement is annotated in Fig. 12 below:



Ohi (Ex. 1003), Fig. 12 (annotated).

49. In sum, *Ohi*’s Fig. 12 circuit includes a *short-circuit protection circuit* that detects the gate voltage of IGBT 11, compares it to a threshold value during a predetermined period after turning on IGBT 11, causes the control output signal to

turn off IGBT 11 if the gate voltage exceeds the threshold within that predetermined period.

4. ***Claim 1[c] said short-circuit protection circuit includes: pulse generation circuit receiving said control input signal and outputting a first pulse signal being significant only in said predetermined period according to a timing when said control input signal indicates the conduction of said insulated gate transistor;***

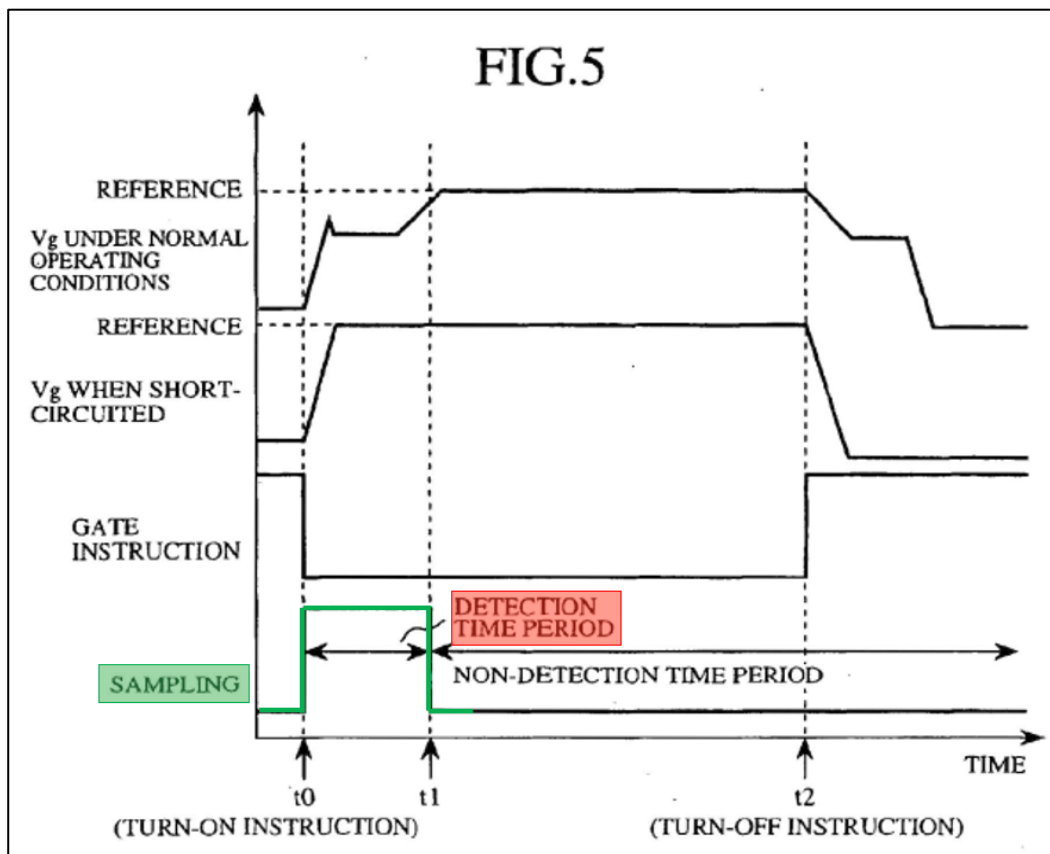
50. *Ohi* teaches a sampler 16² (*pulse generation circuit*) that receives the turn-on instruction from outside the circuit (*receiving said control input signal*) and outputs a level High pulse that defines the period after the IGBT is turned on during which the gate voltage is measured to detect a short-circuit condition (*outputting a first pulse signal being significant only in said predetermined period according to a timing when said control input signal indicates the conduction of said insulated gate transistor*):

[T]he drive circuit includes the **sampler 16 for allowing the process of detecting the gate voltage V_g** that appears at the gate terminal of the IGBT 11 **only during a transition time period** before the gate voltage V_g reaches the on-state gate voltage immediately **after the control logic 12 has received a turn-on instruction** from outside the drive circuit, and the gate voltage detector 17 that detects the gate

² Specifically, the claimed pulse generation circuit is satisfied by the circuitry in sampler 16 that generates a signal that is input into the AND gate 44. For example, Fig. 12 depicts a delay circuit 31 that performs this functionality. As discussed below in ¶¶ 52-55, *Ohi* also teaches an embodiment of sampler 16 that includes a delay circuit 31, a delay circuit 41, and an inverter. Although a dotted line in Fig. 12 suggests AND gate 44 is part of sampler 16, in my analysis, I do not contend that AND gate 44 satisfies the claimed pulse generation circuit. Instead, AND gate 44 satisfies the claimed “logical circuit.”

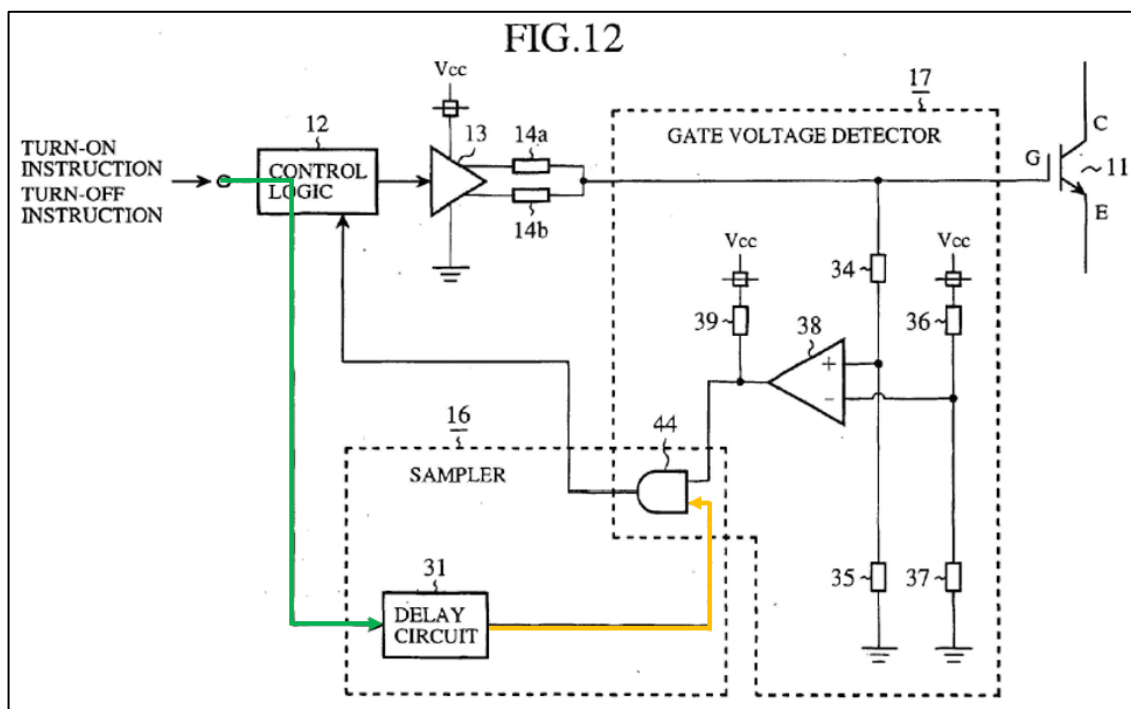
voltage V_g that appears at the gate terminal of the IGBT 11 throughout a detection time period during which the sampler 16 allows the process of detecting the gate voltage V_g , and that recognizes the occurrence of an abnormality in the IGBT 11 when the gate voltage V_g exceeds a reference value.

Ohi (Ex. 1003), 8:17-29 (emphasis added). Specifically, the claimed pulse generation circuit is satisfied by the circuitry in sampler 16 that generates a signal that is input into the AND gate 44. For example, Fig. 12 depicts a delay circuit 31 that performs this functionality. Fig. 5 illustrates an exemplary pulse generated by sampler 16 that is High (i.e., significant) only when the gate voltage is to be measured (i.e., from t_0 to t_1 , following a gate instruction turning on IGBT):



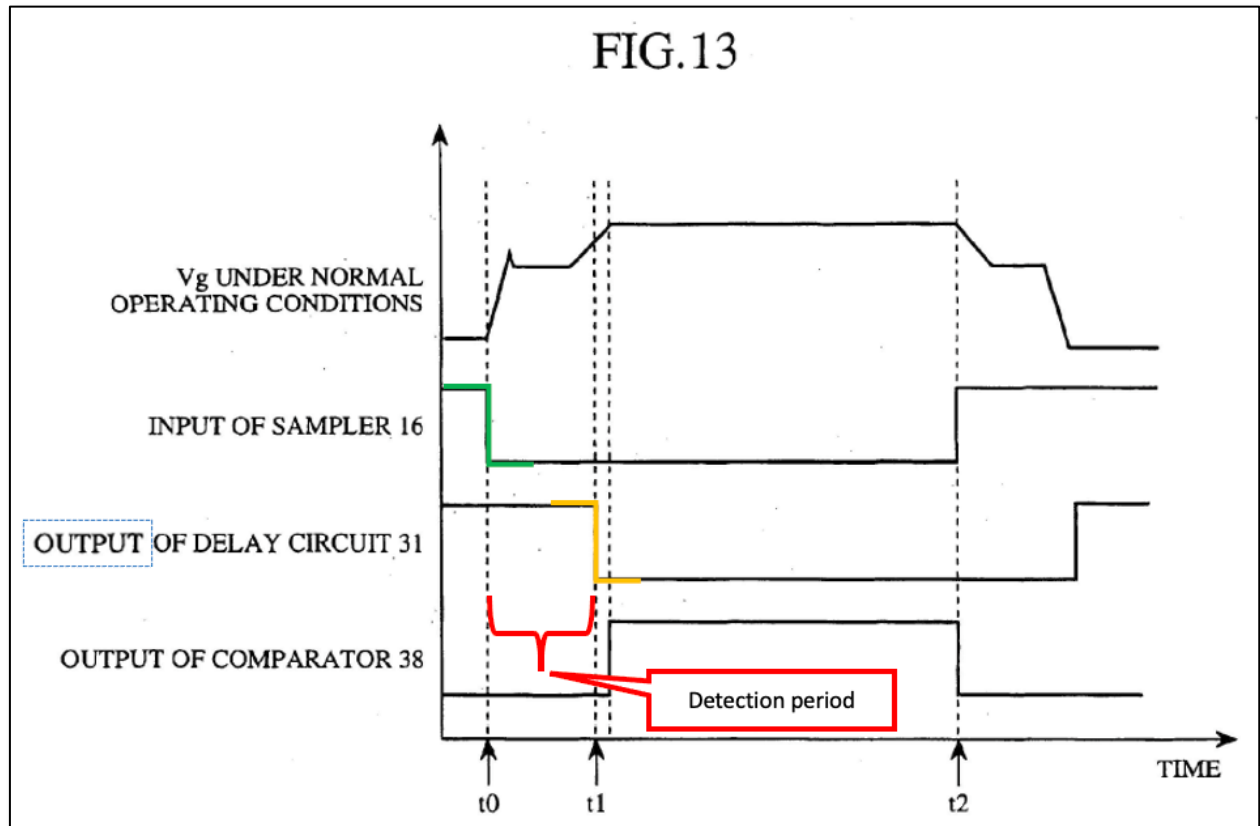
Id. at Fig. 5 (annotated).

51. For the fifth embodiment, specifically, *Ohi* teaches two distinct implementations of sampler 16. In a first example, as depicted in Fig. 12 and described with reference to *Ohi*'s embodiment five, delay circuit 31 receives a **turn-on instruction** from control logic 12 (in the form of a falling edge signal, i.e., a transition from high to low). *Id.* at 12:29-44. Delay circuit 31 **outputs** that falling edge signal after a predetermined amount of time has elapsed after the turn-on instruction is received, ensuring that its output remains significant only for that predetermined time after the IGBT is turned on. *Id.*



Id. at Fig. 12 (annotated). As illustrated in Fig. 13 below, a **detection time period** begins at time t_0 (when IGBT is turned on and sampler 16 receives the **turn-on**

instruction) and ends at t_1 (when the output of delay circuit 31 transitions from high to low in accordance with a preset delay time):



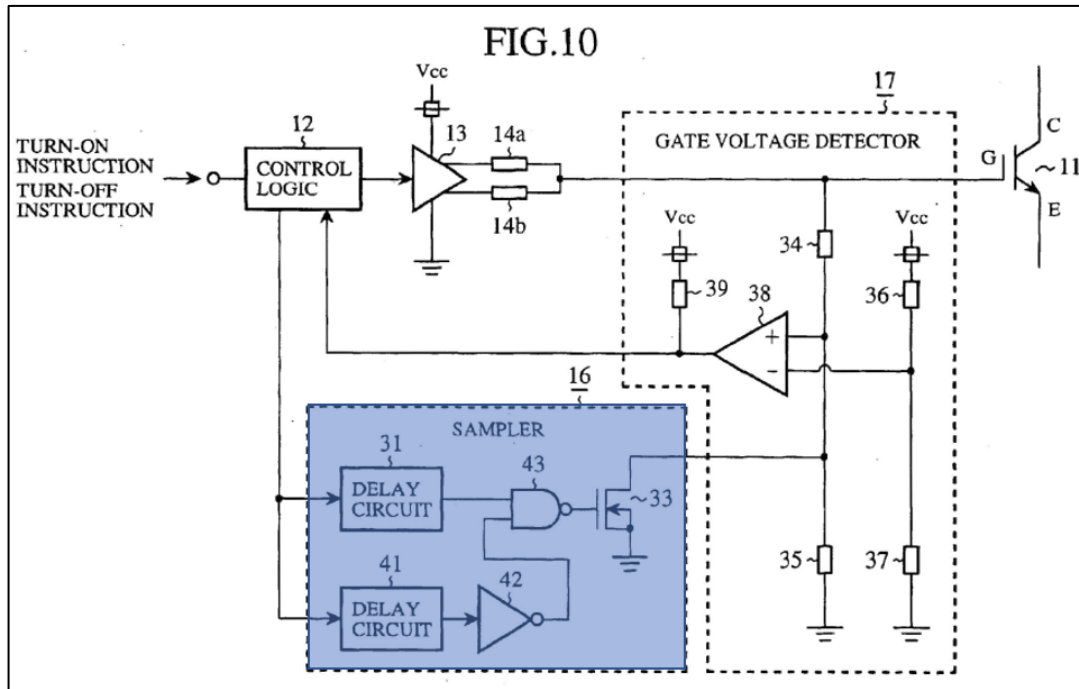
Id. at Fig. 13³, 12:31-36 (“The delay circuit 31 of a sampler 16 has a preset delay time with which the level of its output signal makes a transition from a High level to

³ Fig. 13 contains a typo. The second from the bottom signal is labeled “input of delay circuit 31” in *Ohi*. Based on the operation of the circuit and the illustrated signals in Fig. 13, a POSITA would recognize that the illustrated signal is in fact the output of delay circuit 31. I have indicated the correct label with a blue dashed box.

a Low level at a time t1 when a detection time period during which the gate voltage Vg of an IGBT is detected is ended[.]”).

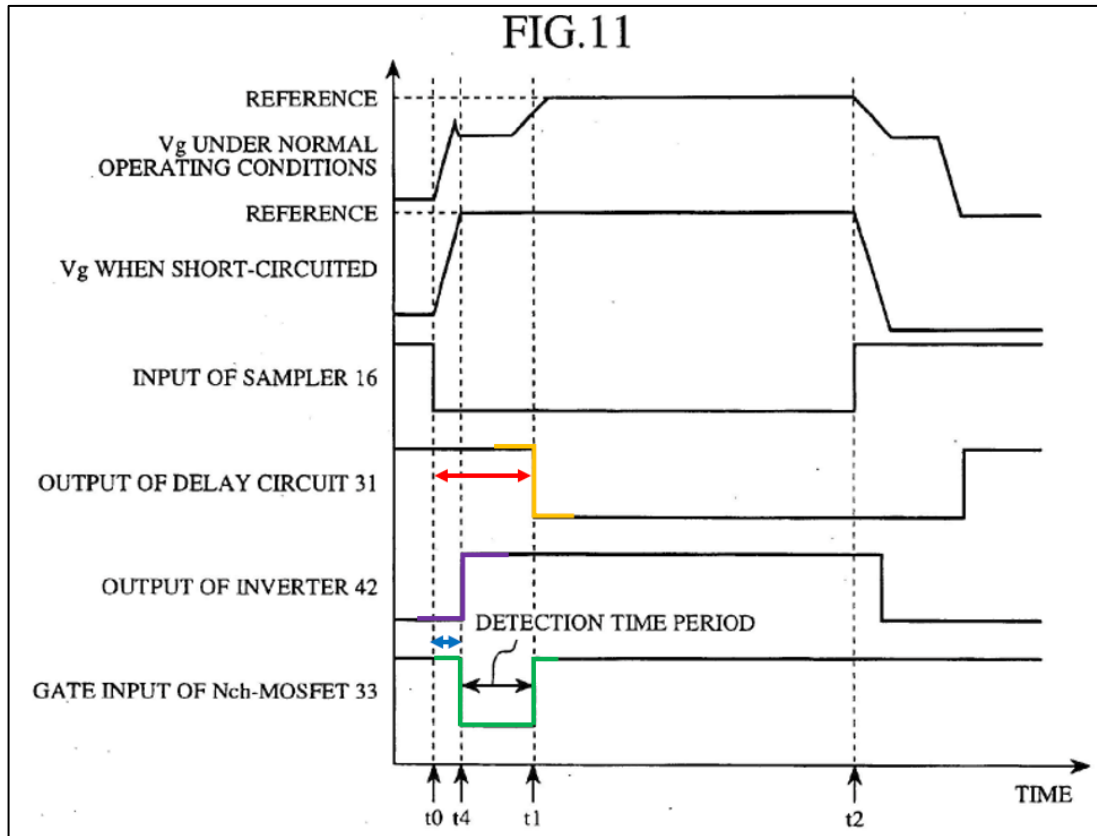
52. A second sampler 16 is expressly proposed as an alternative for *Ohi*’s fifth embodiment.⁴ This alternative is depicted in Fig. 10, described in detail with reference to *Ohi*’s embodiment four, and uses two delay circuits to define a “detection time period during which the gate voltage Vg is detected [that] excludes a certain time period (e.g., the time period from the time t0 to the time t4) immediately after the IGBT 11 is turned on.” *Id.* at 11:36-40. *Ohi* explains that waiting until t4 to begin gate voltage detection ensures the gate voltage measurement excludes a “recovery time” immediately after the IGBT is turned on. *Id.* at 11:48-57. The two-delay circuit structure is depicted in Fig. 10 below, and the t4->t1 detection period generated by this structure is illustrated in Fig. 11 below:

⁴ In ¶ 54, I discuss *Ohi*’s teachings that expressly propose implementing this alternative sampler 16 in its fifth embodiment.



Id. at Fig. 10 (annotated).

53. As depicted in Fig. 11 below, delay circuit 31 is configured to delay the falling edge turn-on signal by the **preset delay time t_0 to t_1** . In other words, it imposes the same delay as sampler 16 in Fig. 12, defining the **end of the detection time period**. Delay circuit 41 and inverter 42 are used to define the **start of the detection time period** by delaying (and inverting) the turn-on signal for a **preset delay time t_0 to t_4** . The result of this two-delay sampler 16 is a **pulse**, similar to the pulse depicted in Fig. 5, that is significant only when the gate voltage is to be measured (i.e., from t_4 to t_1 , following a gate instruction turning on IGBT):



Id. at Fig. 11 (annotated). As shown in Fig. 11, the pulse generated by sampler 16 is inverted such that it is Low during the detection time period.

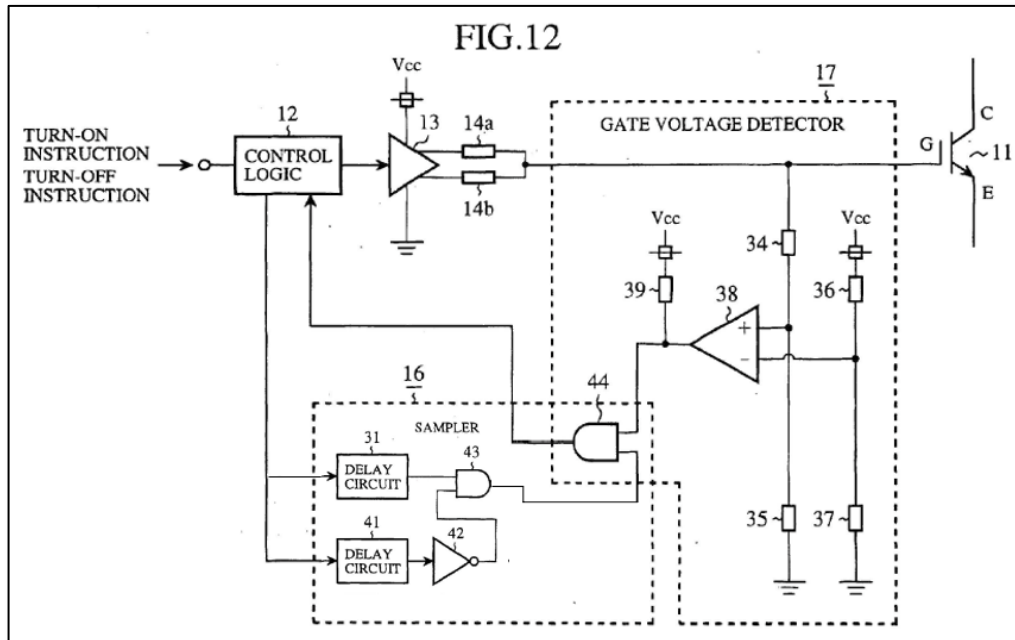
54. *Ohi* expressly teaches that the process for excluding recovery time from the detection period described with reference to embodiment 4 (Figs. 10-11) can be used in *Ohi's* embodiment five (Figs. 12-13). As stated with reference to embodiment five:

The detection time period during which the gate voltage V_g is detected can exclude a recovery time period immediately after the IGBT is turned on, like that of above-mentioned embodiment 4.

Id. at 12:66-13:2 (emphasis added). A POSITA would have understood that incorporating the fourth embodiment's recovery time exclusion into the fifth

embodiment's circuit is a straightforward replacement of the fifth embodiment's single delay circuit with the fourth embodiment's two delay circuit structure that defines both a start and end of the detection time period. As I have explained above, the fourth embodiment's delay circuit 31, delay circuit 41, inverter 42 and NAND gate 43 generate an inverted pulse as depicted in Fig. 11. Additionally, a POSITA would have understood that because the Fig. 12 sampler 16 outputs a High signal during the detection time period, to implement Fig. 10's sampler 16 in *Ohi's* fifth embodiment, an AND gate would replace NAND gate 43. This replacement would ensure that AND gate 44 in Fig. 12 (the fifth embodiment's circuit) receives a High signal from the sampler during the desired measurement period, rather than the inverted pulse that the Fig. 10 sampler 16 inputs to MOSFET 33 (as depicted in FIG. 11).

55. Depicted below is the result of implementing the sampler 16 of embodiment four in embodiment five to exclude from the measurement period a recovery time period immediately after the IGBT is turned on:

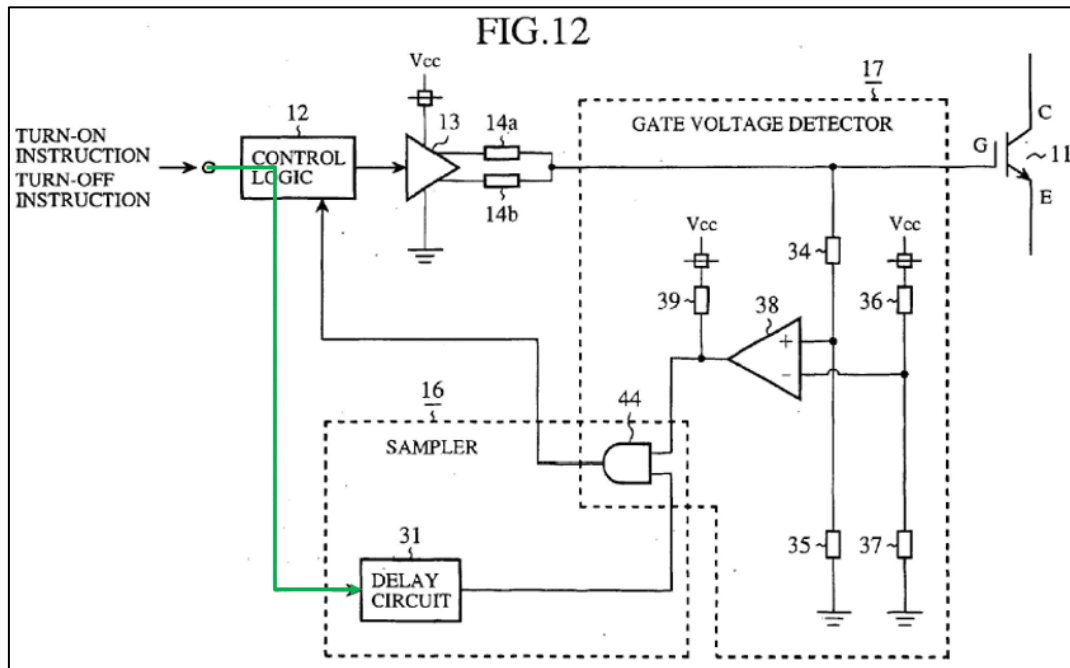


Ohi (Ex. 1003), Fig. 12 (modified by implementing the sampler 16 of embodiment four to exclude a recovery period from the detection time period).

56. This modification to Fig. 12 produces a pulse that excludes recovery time from the detection time period and is the result of implementing *Ohi*'s express teaching that the fifth embodiment's Fig. 12 circuit could exclude recovery time as expressly discussed in the fourth embodiment A POSITA would have understood that the modification to Fig. 12 depicted above outputs a High pulse that defines the detection time period and that is significant only during the detection time period following an instruction to turn on the IGBT (*significant only in said predetermined period according to a timing when said control input signal indicates the conduction of said insulated gate transistor*). Accordingly, sampler 16 in this modification to Fig. 12 satisfies the claimed first pulse signal.

Ohi's sampler 16 in Fig. 12 receives the turn-on instruction, as claimed

57. As discussed above and as depicted in Fig. 12 below, *Ohi's* sampler 16 (pulse generation circuit) receives the turn-on instruction from outside the circuit (receiving said control input signal):



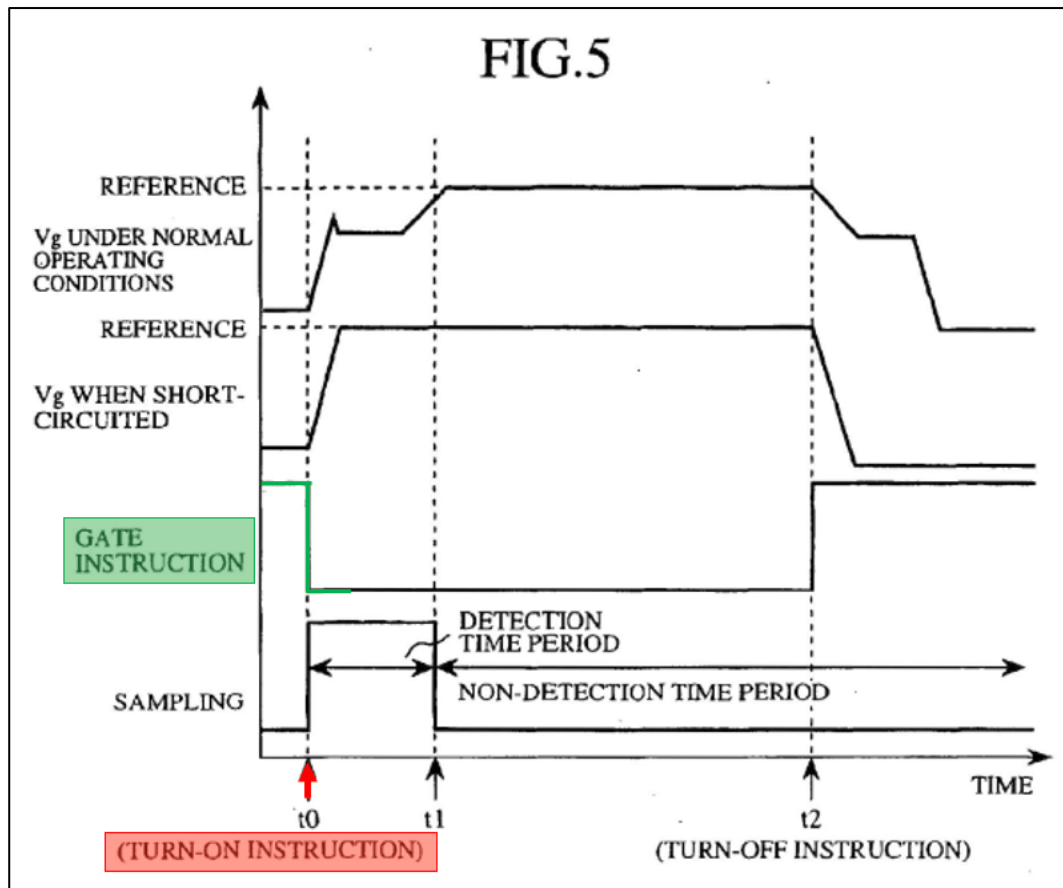
Ohi (Ex. 1003), Fig. 12 (annotated).

58. Although *Ohi* does not illustrate the turn-on instruction received by control logic 12, for a number of reasons set forth below, a POSITA would have understood (1) that this external signal is simply a toggled state change (e.g., a voltage transitioning from High to Low or Low to High) and (2) that the toggled state change is received by sampler 16, as claimed.

59. *Ohi* explains that control logic 12 outputs a “gate instruction” in response to receiving the turn-on or turn-off instructions:

In response to a turn-on instruction from outside the drive circuit, the control logic 12 delivers a gate instruction to cause the IGBT 11 become turned-on to the buffer 13. . . . On the other hand, in response to a turn-off instruction from outside the drive circuit, the control logic 12 delivers a gate instruction to cause the IGBT 11 to become turned-off to the buffer 13.

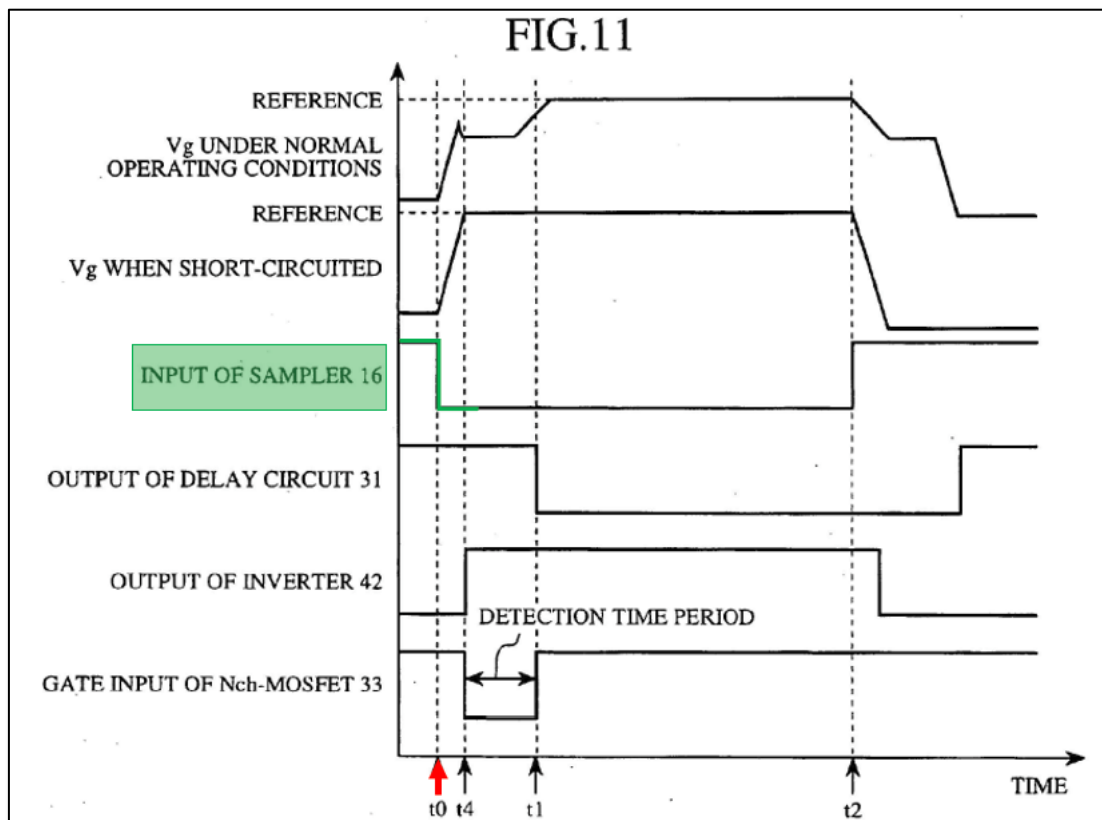
Ohi (Ex. 1003), 7:1-13. In Fig. 5 below, the **gate instruction** is depicted as falling edge (i.e., High to Low) state change that occurs when the turn-on instruction is received, t_0 :



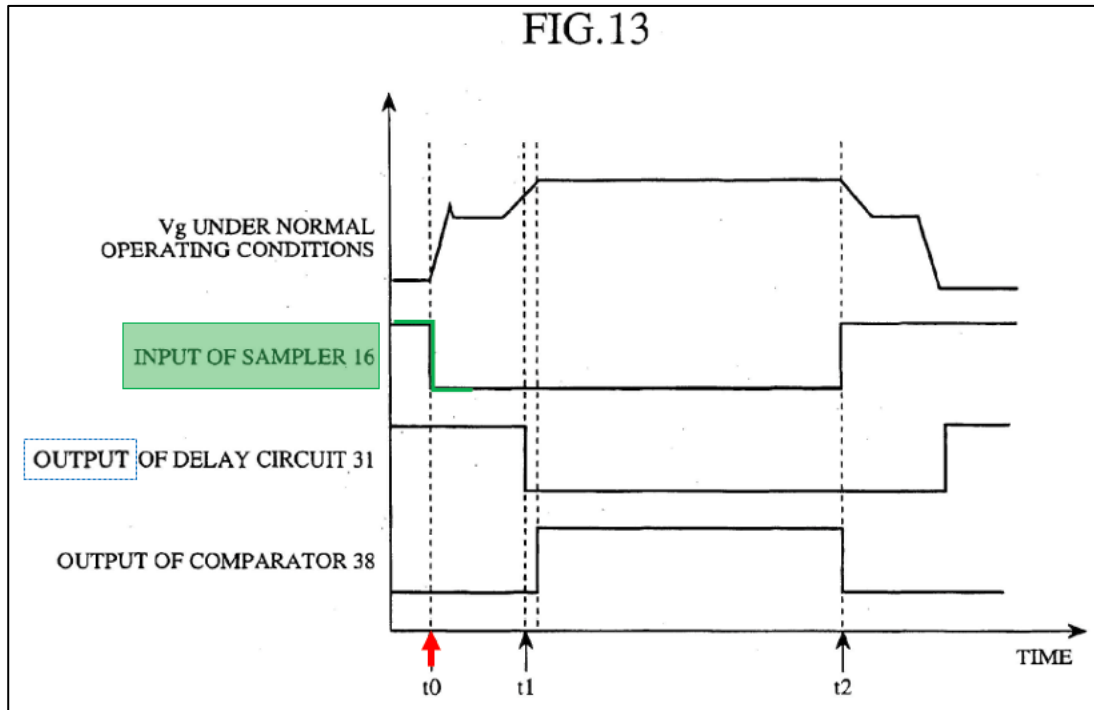
Id. at Fig. 5 (annotated). *Ohi* further explains that, as illustrated in Fig. 5 above, when the turn-on instruction is input into control logic 12, sampler 16 receives this signal and enables a detection time period during which the IGBT gate voltage is measured:

[W]hen the control logic 12 receives a turn-on instruction from outside the drive circuit, as shown in FIG. 5, the sampler 16 enables the gate voltage detector 17 to detect the gate voltage V_g at the time t_0 when the turn-on instruction is received. After that, when a certain time elapses and a time t_1 (before the gate voltage V_g reaches the on-state gate voltage, and the time t_1 is determined in consideration of the characteristics of the IGBT 11) comes, the sampler 16 disables the gate voltage detector 17 to detect the gate voltage V_g .

Id. at 7:32-41 (emphasis added). As depicted in both Figs. 11 and 13 below, sampler 16 receives the same falling edge signal that is depicted in Fig. 5 as the “gate instruction” that results from receiving a turn-on instruction from outside the drive circuit at time t_0 :



Id. at Fig. 11 (annotated).



Id. at Fig. 13 (annotated).

60. Based on the above disclosures and illustrations, a POSITA would have understood that sampler 16 (*pulse generation circuit*) receives the turn-on instruction from outside the circuit (*receiving said control input signal*), as claimed. First, although not illustrated in any of *Ohi's* timing diagrams, a POSITA would have understood that the turn-on instruction is simply a toggled state change (e.g., a voltage transitioning from High-to-Low or Low-to-High) received by logic circuit 12. Indeed, the drive circuit described by *Ohi* uses standard High/Low logic signals, which would apply to the turn-on instruction—a signal that transitions from High-to-Low or vice versa.

61. Second, a POSITA would have understood that sampler 16 *receives* this signal (i.e., the state change when a turn-on instruction is received at t_0), as claimed. As illustrated above, control logic 12 transmits the turn-on instruction signal as a High-to-Low state change at the precise moment, t_0 , the turn-on instruction is received from outside the circuit. Indeed, as illustrated in Figs. 11 and 13 above, the input of sampler 16 transitions from High-to-Low at t_0 —the moment a turn-on instruction is received.

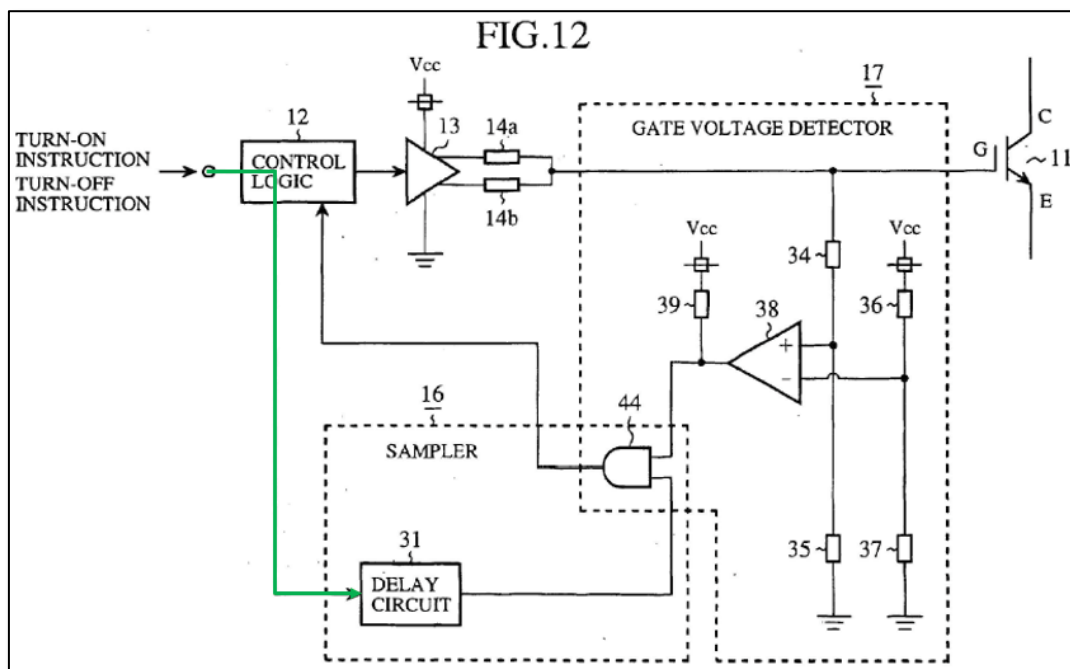
62. Finally, *Ohi* does not teach or suggest that the turn-on instruction received by control logic 12 at time t_0 is modified in any way prior to being transmitted to sampler 16. Accordingly, a POSITA would have understood that the turn-on instruction is a falling edge signal (i.e., a transition from High-to-Low) that is directly passed along by control logic 12 and is received by sampler 16 at time t_0 . Even assuming, for the sake of argument, that turn-on instruction were a rising edge signal that control logic 12 inverted before transmitting to sampler 16, this arrangement would still teach limitation [1(c)]. Indeed, the '835 Patent expressly allows for signals to pass through inverters and still considered them *supplied to* a destination. For example, the '835 Patent notes that control input signal S1 is supplied to one-shot generation circuit 1 and also to gate driver GD through two separate inverters and a NOR gate:

[A] **control input signal S1** supplied to control the transistor 12 from the outside through the control signal input terminal U_{IN} **is supplied**

not only to the gate driver GD via an inverter circuit G3, a NOR circuit G4 and an inverter circuit G5 but also to a one-shot generation circuit 1.

'835 *Patent* (Ex. 1001), 4:50-54 (emphasis added); Fig. 2 (illustrating the same). Accordingly, even if control logic 12 did invert *Ohi's* turn-on instruction before delivering it to sampler 16—there is no suggestion that such an inversion occurs—the turn-on instruction is still received by sampler 16, as claimed.

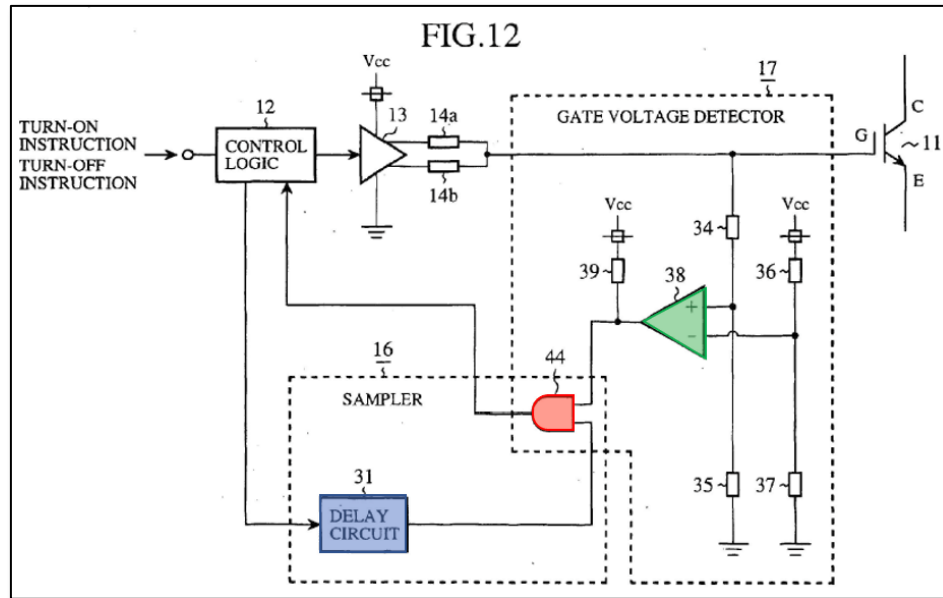
63. *Ohi's* teachings satisfy the claim language in a second manner. Namely, (1) the portion of control logic 12 that directly receives the turn-on instruction (*control input signal*) from outside the circuit and (2) sampler 16 collectively satisfy the claimed *pulse generation circuit*. As described in the preceding paragraphs, *Ohi's* turn-on instruction passes first through control logic 12 and then to sampler 16 as illustrated below:



Ohi (Ex. 1003), Fig. 12 (annotated). Accordingly, the combination of control logic 12 and sampler 16 also satisfies the claimed *pulse generation circuit receiving said control input signal*.

5. ***Claim 1[d] a comparator receiving the detecting voltage of said control output signal, performing a comparison with said reference voltage and outputting a second pulse signal being significant during a period when the detecting voltage of said control output signal exceeds said reference voltage; and***

64. As I discussed above, the fifth embodiment, as depicted in Fig. 12 below, utilizes three key components to detect a short circuit abnormality immediately following a turn-on instruction: (1) **sampler 16** (including **delay circuit 31** in the Fig. 12 embodiment) that generates a *first pulse signal* that defines the “detection time period during which the gate voltage V_g of an IGBT is detected[,]” (2) **comparator 38** that outputs a *second pulse signal* when gate voltage V_g of the IGBT exceeds a threshold voltage, and (3) **AND circuit 44** that receives the first and second pulse signals and outputs a High signal when V_g exceeds the threshold during the detection time period. *Id.* at 12:32-58.



Id. at Fig. 12 (annotated).

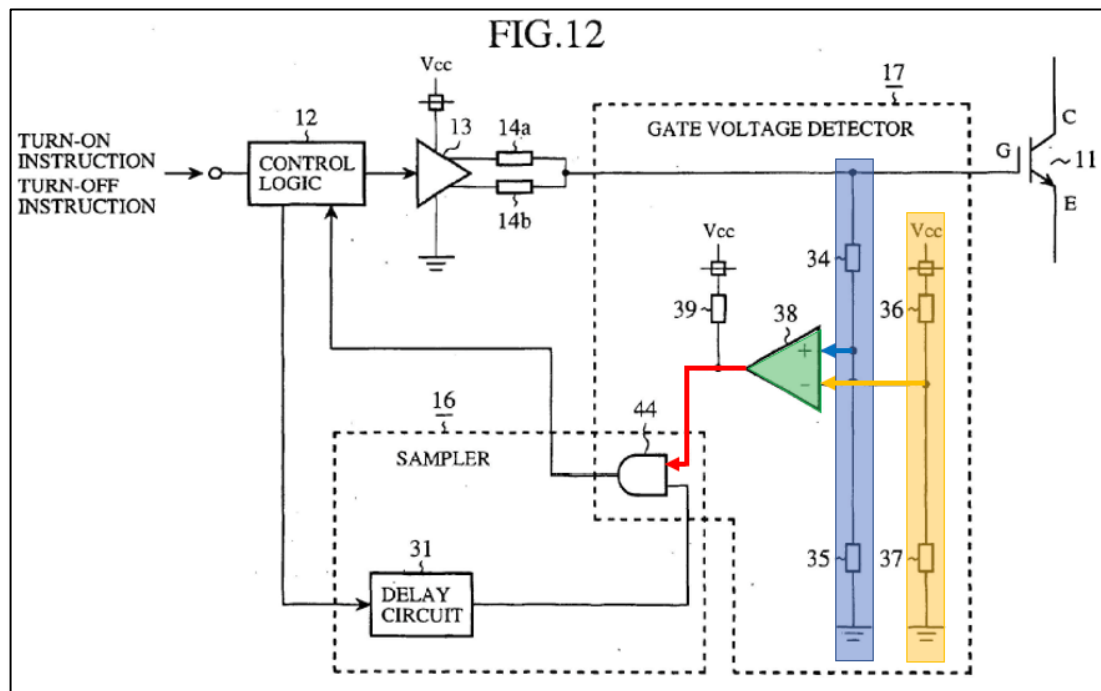
65. This limitation is satisfied by **comparator 38**, which receives at its “+” terminal input a divided-down gate voltage of IGBT 11 (*receiving the detecting voltage of said control output signal*), receives at its “-” terminal a *reference voltage*, and performs a comparison of those inputs, outputting a High signal when the divided-down gate voltage exceeds the reference voltage (*performing a comparison with said reference voltage and outputting a second pulse signal being significant during a period when the detecting voltage of said control output signal exceeds said reference voltage*).

66. This limitation recites a “detecting voltage of said control output signal[.]” As I discussed above, a POSITA would understand, pursuant to the ’835 Patent’s disclosure, that a “detecting voltage of said control output signal” is a measured gate voltage or a divided down representation of the measured gate

voltage. *Ohi* teaches the same arrangement as the '835 Patent. Namely, the drive circuit in *Ohi* includes a gate voltage detector 17 that provides a divided down representation of the gate terminal of IGBT 11 to comparator 38, which compares it to a reference voltage and outputs a High pulse signal when the gate voltage representation exceeds the reference voltage:

The **comparator 38** of a gate voltage detector 17 compares a divided voltage obtained from the gate voltage V_g of the IGBT with a divided voltage obtained from the control voltage V_{cc} of the IGBT, like that of above-mentioned embodiment 2, and, **when the gate voltage V_g reaches the control voltage V_{cc} in level, causes its output signal to make a transition from a Low level to a High level** (see Fig. 13).

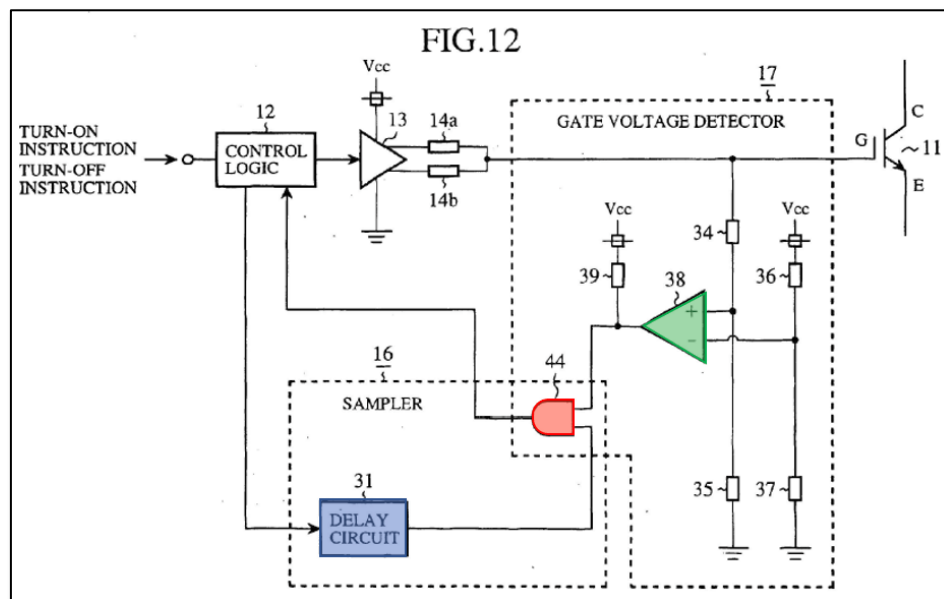
Ohi (Ex. 1003), 12:37-44 (emphasis added); Fig. 13. This arrangement is depicted below in Fig. 12:



Id. at Fig. 12 (annotated).

6. ***Claim 1[e] a logical circuit receiving said first and second pulse signals and outputting a stop signal forcing said driver to stop said control output signal when said second pulse signal becomes significant during a period when said first pulse signal is significant.***

67. As I discussed above, the fifth embodiment, as depicted in Fig. 12 below, utilizes three key components to detect a short circuit abnormality immediately following a turn-on instruction: (1) **Sampler 16** (including **delay circuit 31** in the Fig. 12 circuit) that generates a *first pulse signal* that defines the “detection time period during which the gate voltage V_g of an IGBT is detected[,]” (2) **comparator 38** that outputs a *second pulse signal* when gate voltage V_g of the IGBT exceeds a threshold voltage, and (3) **AND circuit 44** that receives the first and second pulse signals and outputs a High signal when V_g exceeds the threshold during the detection time period. *Id.* at 12:32-58.



Id. at Fig. 12 (annotated).

68. A short circuit condition is detected by AND gate 44 when both the output of comparator 38 and delay circuit 31 are High:

The AND circuit 44 receives the output signal of the comparator 38 and the output signal of the delay circuit 31 and then implements a logical AND operation on them. . . . **[W]hen a short circuit occurs in the IGBT 11, the output-signal of the AND circuit 44 becomes a High level** (i.e., a logical level indicating a detection of the occurrence of an abnormality in the IGBT) **because the output signal of the comparator 38 becomes a High level before the output signal of the delay circuit 31 becomes a Low level.**

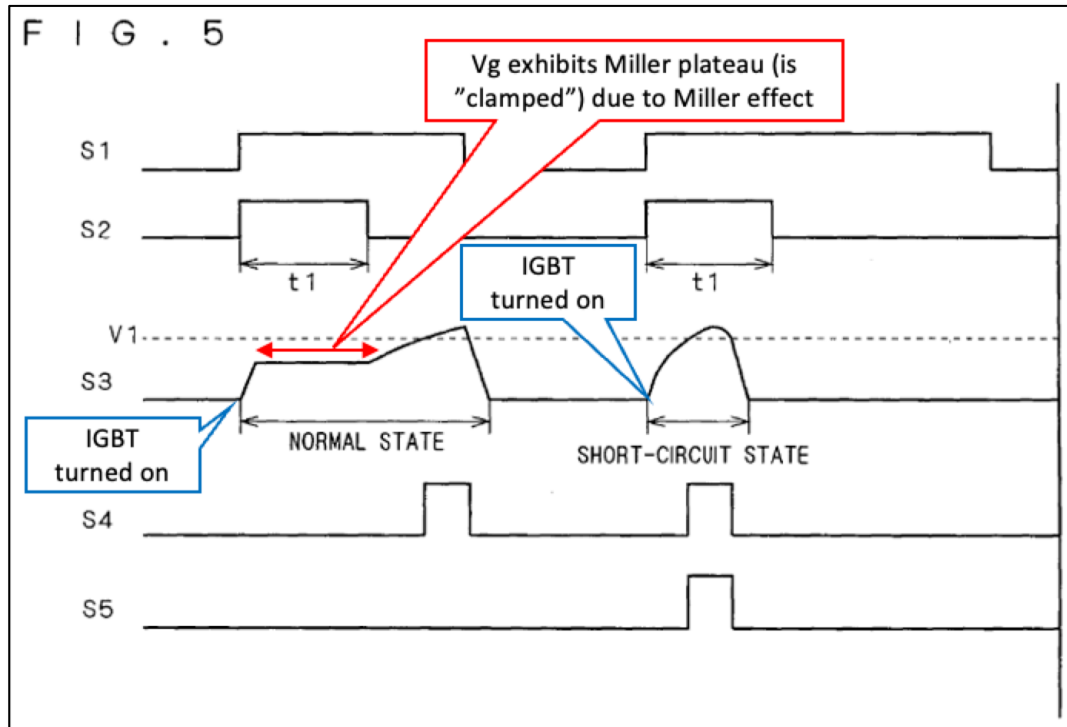
Id. at 12:45-58 (emphasis added). When such a short circuit condition is detected within the detection time window, **logical circuit 44** generates a stop signal that causes IGBT to be turned off. *Id.* at 12:53-60 (“[W]hen a short circuit occurs in the IGBT 11, the output-signal of the AND circuit 44 becomes a High level (i.e., a logical level indicating a detection of the occurrence of an abnormality in the IGBT . . . [.] After that, the drive circuit operates in the same way that that of embodiment 2 does[.]”), 10:14-21 (describing embodiment 2, teaching that the circuit “delivers an abnormality signal to the control logic 12[, and, a]s a result, the control logic 12 causes the IGBT 11 to become turned-off[.]”).

69. In sum, AND gate 44 (*a logical circuit*) receives as inputs the output of comparator 38 and the output of delay circuit 31 (*receiving said first and second pulse signals*) and outputs a stop signal forcing off IGBT 11 (*outputting a stop signal forcing said driver to stop said control output signal*) when delay circuit 31 produces a High signal defining the detection time period at the same time that comparator 38

produces a High signal indicating the gate voltage exceeds a reference voltage
*(produced when said second pulse signal becomes significant during a period when
said first pulse signal is significant).*

7. ***Claim 2: The semiconductor device according to claim 1, wherein said predetermined period when said first pulse signal is significant is set on a basis of a period when a voltage of said control output signal is clamped constantly when said insulated gate transistor normally operates.***

70. As I discussed above, the '835 Patent describes a phenomenon in IGBT devices referred to in the field as a “Miller effect” in which the gate voltage sticks at a mid-point voltage (referred to as a “Miller plateau” or as being “clamped” at that voltage) following a turn-on instruction for a period of time before rising to the normal operating voltage that is near V_{cc} . '835 Patent (Ex. 1001), 5:62-6:3. Therefore, the voltage of the control output signal S3 is set to a predetermined value due to the Miller effect. This clamping at a mid-point voltage for a period after the IGBT is turned on under normal operating conditions is illustrated in Fig. 5:



Id. at Fig. 5 (annotated). Consistent with the language of Claim 2, the '835 Patent further teaches that this clamped/Miller period should be used to define the short-circuit detection period t_1 , which is dictated by the time at which the pulse generation circuit's output S2 is "significant":

[T]he one-shot **pulse generation circuit 1 outputs** the pulse signal **S2 which comes to be in the significant condition** according to the building up of the control input signal S1, and a period t_1 in the significant condition, in the "H" state in this case, is set to be **almost equal to a period when the control output signal S3 is clamped to a certain voltage**.

Id. at 6:35-40 (emphasis added). As illustrated in Fig. 5 above, the Miller plateau clamping prevents the IGBT gate voltage from exceeding the reference voltage V1 during the measurement period under normal operating conditions. Because a short circuit condition will not be similarly clamped to the Miller plateaus voltage, the

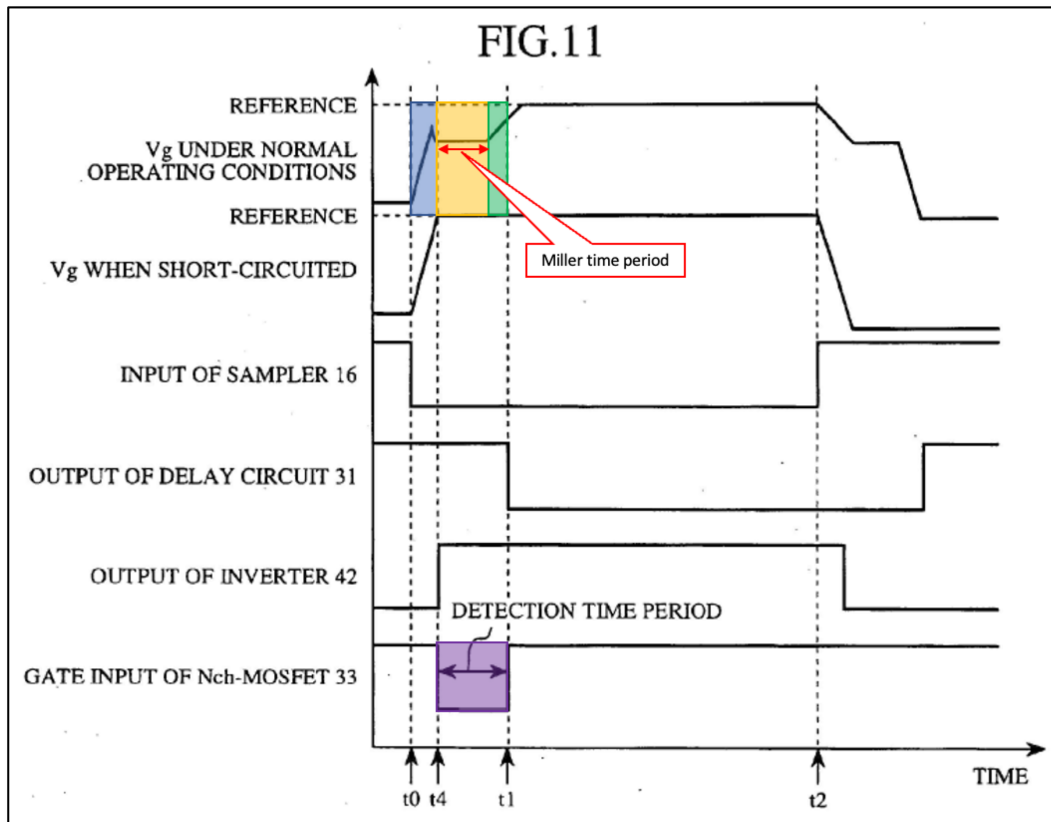
gate voltage V_g will exceed the reference voltage V_1 within the time period t_1 in the event of such a short circuit condition.

71. *Ohi* teaches this precise process and acknowledges that it is also based on the Miller effect described by the '835 Patent. Namely, as I discussed above, *Ohi* describes a “Miller time period” during which the IGBT’s gate voltage is clamped:

When the drive circuit sends a gate instruction to instruct the IGBT 11 to turn on in response to a turn-on instruction under normal operating conditions, the gate voltage V_g of the IGBT 11 starts rising. When the gate voltage V_g then exceeds a threshold voltage, the collector current I_c starts increasing. When the collector current I_c flowing in the IGBT 11 becomes nearly equal to an inductive load electric current flowing through the inductive load, the collector-emitter voltage V_{ce} starts decreasing and **the gate voltage V_g then becomes a nearly-constant voltage. This time period** during which the gate voltage V_g is nearly constant after the collector current I_c has become nearly equal to the inductive load electric current **is known as a Miller time period. . . . At the conclusion of the Miller time period, the gate voltage V_g starts rising again.** At this time, **the gate voltage rises slowly** with a smaller time constant than that with which the gate voltage has risen before the Miller time period because the feedback capacitance is large, **and then reaches a certain on-state gate voltage.** The gate voltage V_g enters a steady state after it has experienced the above-mentioned transition time period.

72. As I discussed above, *Ohi* teaches a sampler 16 that uses two delay circuits to define a “detection time period during which the gate voltage V_g is detected [that] excludes a certain time period (e.g., the time period from the time t_0 to the time t_4) immediately after the IGBT 11 is turned on.” *Id.* at 11:36-40. *Ohi* explains that this two-delay circuit sampler 16 excludes this time period from t_0 to t_4 “in order for the **detection time period** during which the gate voltage V_g is

detected **to start after the conclusion of the recovery time period** at the turn-on time[.]” *Id.* at 11:52-55 (emphasis added). In other words, the sampler 16 is designed specifically to ensure the detection time period does not begin until the Miller time period has been reached. This is depicted in Fig. 11 below:



Id. at Fig. 11 (annotated). As illustrated, the detection time period begins at the moment the **Miller time period** begins, i.e., as soon as the **recovery time period** ends.

73. As I discussed above, *Ohi* expressly teaches that this two-delay circuit sampler 16 can be incorporated into the fifth embodiment circuit as depicted in Fig. 12. And, when that sampler 16 is implemented in Fig. 12, sampler 16 outputs a pulse that remains High for a predetermined time period (*predetermined period when said*

first pulse signal is significant) and that time period, as illustrated in Fig. 11 above, is set to begin on the basis of when the Miller time period begins causing V_g of the IGBT to be clamped constantly during normal operation (*is set on a basis of a period when a voltage of said control output signal is clamped constantly when said insulated gate transistor normally operates*).

IV. CONCLUSION

74. I declare that all statements made herein of my knowledge are true, and that all statements made on information and belief are believed to be true, and that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Date: January 11, 2023

By: 

Dr. David Kuan-Yu Liu

Appendix A

DAVID KUAN-YU LIU, Ph.D.

42063 Benbow Drive, Fremont, CA 94539 • (510) 770-9449 or (510) 579-5029

www.davidkyliu.com davidkyliu@comcast.net

PROFESSIONAL PROFILE

- Technical expert with over 20 years of industrial experience in the development of advanced CMOS devices and process technology, with special emphasis on non-volatile semiconductor memory devices and process technology, and high-voltage semiconductor devices, with additional 12 years of experience serving as expert consultant.
 - Named inventor on 99 US patents.
- Consultant and expert witness for past 15 years in semiconductor intellectual property evaluation and patent litigation, with deposition experience and successful ITC trial testifying experience.
- Successful track record in transitioning products from development phase to high-volume manufacturing phase, both as an individual contributor and as manager/director.
- Co-founder of an LLC in the development and licensing of intellectual property with emphasis on embedded flash memory technology.
- Co-founder of a semiconductor memory start-up company (Progressant Technologies, Inc.); participated in its successful sale to Synopsys, Inc.
- Fluent in Mandarin Chinese (native language) and English; over 10 years experience as real-time translator of church sermons and proficient in written translation.

EDUCATION

Stanford University, Palo Alto, California

Ph.D., Electrical Engineering (1989)

Thesis: Physics and Technology of Novel Conductivity-Modulated Power MOSFET's

M.S., Electrical Engineering (1985)

Coursework in integrated-circuit technology, semiconductor device physics, computer modeling of semiconductor devices and fabrication processes, and solid-state physics

University of California, Berkeley, California

B.S., Electrical Engineering (1983)

Certificate of Distinction (awarded annually to the top EECS graduate)

KEY EXPERT WORK EXPERIENCE:

Case:	Netlist, Inc. vs. Samsung Electronics Co. Ltd. et al.,
Jurisdiction:	Civil Action No. 2:21-cv-00463 Eastern District of Texas
Work Product:	Expert relating to memory modules.
Nature of Case:	Civil action.
Counsel:	Retained by Fish & Richardson (Contact: Tony Nguyen)
Date:	8/22 – Current

Case: **Vervain, LLC vs. *Micron Technology* & related IPR Petition**
Jurisdiction: Action No. 6:21-cv-00487-ADA
Western District of Texas
Work Product: Patent analysis and prior art review toward preparation of IPR petition material and draft of declaration on 4 patents, all 4 petitions instituted, and deposed on both initial declaration and reply declaration.
Counsel: Retained by Orrick, Herrington & Sutcliffe LLP (Contact: Jared Bobrow)
Date: 8/21 – Current

Case: **Monterey Research vs. *Qualcomm* PTAB Matter**
Work Product: Patent analysis and prior art review toward preparation of IPR petition material and draft of declaration.
Counsel: Retained by Jones Day (Contact: David Cochran)
Date: 12/21 – Current

Case: ***Semiconductor Energy Laboratory Co., OLED Patent Matters***
Jurisdiction: Action No. 8:21-cv-00554-JAK-ADS
Central District of California
Work Product: Expert for infringement on 3 patents relating to OLED driver circuit and layout, responsibilities include source code viewing, GDS layers viewing, and claim charts review.
Nature of Case: Civil action.
Counsel: Retained by Fish & Richardson (Contact: Bryan Basso)
Date: 9/21 – 4/22

Case: ***Apple Inc. IPR Petition for U.S. Patents 6,622,108 & 6,807,505***
Work Product: Patent analysis and prior art review toward preparation of IPR petition material and draft of declaration.
Counsel: Retained by Erise IP (Contact: Paul Hart)
Date: 8/21 – 9/21

Case: ***Texas Instruments IPR Petition***
Work Product: Patent analysis and prior art review toward preparation of IPR petition material and draft of declaration.
Counsel: Retained by Fish & Richardson (Contact: Josh Griswold)
Date: 9/20 – 4/21

Case: ***Micron Technology vs. UMC/JinHua***
Jurisdiction: Case No. 4:17-CV-06932-MMC
United States District Court for the Northern District of California
Work Product: Testifying expert, trade secret documents review, and declaration submission.
Nature of Case: Trade secret contention of Micron confidential documents.
Counsel: Retained by Jones Day (Contact: Randy Kay)
Date: 3/17 – Current

Case: ***SK Hynix vs. BitMicro***
Jurisdiction: Investigation No. 337-TA-1097
United States International Trade Commission
Work Product: Testifying expert for non-infringement on 2 patents, issued expert rebuttal report, deposition taken, issued witness statement.
Nature of Case: ITC infringement case concerning module stacking of SDRAM.
Counsel: Retained by Fish Richardson (Contact: Joseph Colaianni)
Date: 11/18 – 4/19

Case: ***Rohm Company IPR Petition***
Work Product: Patent analysis and prior art review toward preparation of IPR petition material and draft of declaration.
Counsel: Retained by Fish & Richardson (Contact: Matt Colvin)
Date: 4/18 – 8/18

Case: ***Apple Inc., vs. Qualcomm Incorporated***
Jurisdiction: Case No. 3:17-CV-02402
United States District Court for the Southern District of California
Work Product: Patent analysis and prior art review toward preparation of IPR petition material and draft of declaration, 2 depositions taken.
Counsel: Fish & Richardson (Contact: Tony Nguyen)
Date: 1/18 – 5/19

Case: ***Macronix vs. Toshiba***
Jurisdiction: Investigation No. 337-TA-1046
United States International Trade Commission
Work Product: Testifying expert for infringement and non-invalidity on 2 patents, claim construction analysis, technical tutorial, database viewing for evidence gathering, issuing expert report and expert rebuttal report, deposition taken for 2 patents, issued witness statement and rebuttal witness statement, testified in ITC court on both infringement and invalidity.
Nature of Case: ITC infringement case concerning advanced NAND Flash memory.
Counsel: Retained by Fish Richardson (Contact: David Barken)
Date: 4/17 – 10/18

Case: *Novatek Microelectronics Corp. IPR Petition*
Work Product: Patent analysis and prior art review toward preparation of IPR petition material and draft of declaration.
Counsel: Retained by Kroub, Silbersher & Kolmykov PLLC (Contact: Sergey Kolmykov)
Date: 2/17 – 4/17

Case: *Taiwan Semiconductor Manufacturing Company IPR Petition*
Work Product: Patent analysis and prior art review toward preparation of IPR petition material and draft of declaration.
Counsel: Retained by Fish & Richardson (Contact: John Goetz)
Date: 7/15 – 4/17

Case: *Triune Systems, LLC vs. Wayne Chen, et al.,*
Jurisdiction: Case No. 296-03209-2013,
District Court of Collin County, TX
Work Product: Testifying expert, database viewing, expert report, video-taped testimony
Nature of Case: Defending against trade secret contention.
Counsel: Retained by Gordon & Rees LLP (Contact: Robert Bragalone)
Date: 5/15 – 9/15

Case: *Macronix vs. Spansion*
Jurisdiction: Investigation No. 337-TA-922
United States International Trade Commission
Work Product: Testifying expert, claim construction analysis, technical tutorial, database viewing for evidence gathering, expert report, expert rebuttal report.
Nature of Case: ITC infringement case concerning Flash memory cell
Counsel: Retained by Fish Richardson (Contact: David Barken)
Date: 9/14 – 1/15

Case: *Macronix vs. Spansion*
Jurisdiction: Investigation No. 337-TA-909
United States International Trade Commission
Work Product: Database viewing for evidence gathering, support technical content of expert report, support technical content against rebuttal report.
Nature of Case: ITC infringement case concerning Flash memory cell
Counsel: Retained by Winston & Strawn (Contact Michael Murray)
Date: 5/14 – 1/15

Case: ***Keranos, LLC v. Analog Devices et. al.***
Jurisdiction: Civil Case No. 2:10-CV-00207
United States District Court for the Eastern District of Texas
Work Product: Claim Chart Generation and Claim Construction
Nature of Case: Patent infringement case concerning split gate Flash memory cell
Counsel: Retained by Agility IP (Contact Michelle Breit)
Date: 2/09 – 2/14

Case: ***Silicon Storage Technology, Inc. v. Xicor, LLC***
Jurisdiction: Civil Case No. CV 10-01515
United States District Court for the Northern District of California
Work Product: Expert report and declarations
Nature of Case: Matter concerning United States Reissue Patent RE38,370 on the process of flash memory cell.
Counsel: Retained by Shore Chan Bragalone LLP (Contact Patrick Conroy)
Date: 6/11 – 10/11

Case: ***Fast Memory Erase, LLC v. Spansion et.al.***
Jurisdiction: Civil Case No. 3:10CV-481
United States District Court for the Northern District of Texas
Work Product: Declarations
Nature of Case: Defending Motion for Attorney Fees.
Counsel: Retained by Shore Chan Bragalone LLP (Contact Patrick Conroy)
Date: 2/10 – 6/10

Case: ***Fast Memory Erase, LLC v. Spansion et.al.***
Jurisdiction: Civil Case No. 3-08cv0977M
United States District Court for the Northern District of Texas
Work Product: Testifying expert: issuing expert report, declarations, and deposition taken.
Nature of Case: Patent infringement case concerning minimizing source current during erase of Flash memory cell.
Counsel: Retained by Shore Chan Bragalone LLP (Contact Patrick Conroy)
Date: 2/09 – 5/10

EXPERIENCE:

10/07 to present: **Technical Consultant/Expert Witness**

Serving as a technical consultant and advisor in the area of semiconductor device and process technologies. Expert witness in ITC cases and district court cases, with successful testifying experience in trial hearing. Depositions taken at least 6 times for both litigation cases and IPR petitions. Experienced in source code viewings of circuit schematics and GDS layouts; seasoned in reverse engineering of integrated circuits, as well as techniques for de-processing and analyzing semiconductor chips. Responsibilities including gathering and reviewing of evidence, issuing declaration on claim construction, giving technical tutorial, issuing expert report and expert rebuttal report. Technical consultant for evaluating numerous flash memory and CMOS image sensor patent portfolios for licensing and acquisition consideration. Assessed qualitative merits of each patent portfolio and identified potential infringers and potential licensees. Generated numerous claim charts against potential infringers based on published patents, technical papers and datasheets, and reverse engineering reports.

10/07 to 4/11: **Jonker, LLC**

Inventor and Partner. Developed an intellectual property (IP) portfolio (7 U.S. patents granted and 3 U.S. patent applications pending) on zero-cost CMOS-logic-compatible embedded flash memory. Successfully negotiated the acquisition of this IP portfolio by a major semiconductor company.

8/04 to 10/07: **Maxim Integrated Products, San Jose, California**

Senior Scientist. Responsible for developing embedded non-volatile memory process technology for battery management products. Duties included supervising the development of integrated process flows at the 0.35 μ m and 0.18 μ m CMOS technology nodes. Analyzed and solved process-related reliability issues.

5/00 to 8/04: **Xilinx, Incorporated, San Jose, California**

Senior Manager. Responsible for developing non-volatile memory process technology for flash and CPLD products, as well as advanced CMOS process technology (75nm node). Duties included supervising the development of integrated non-volatile memory process flows at multiple CMOS technology nodes to meet product application requirements. Analyzed and solved process-related reliability issues.

2/00 to 5/00 **Progressant Technologies, Fremont, California**

Co-Founder. Facilitated IP development and sale of the company to Synopsys, Inc.

9/98 to 2/00

Programmable Silicon Solutions, Sunnyvale, California

Director of Process Engineering. Responsible for developing a fully logic compatible embedded flash memory technology for WSMC (a semiconductor foundry). Developed a new integrated process flow to implement a proprietary flash cell in a high-performance logic process, supervised testchip and product tapeout, process optimization, device optimization, and product yield enhancement. Applied interpersonal skills to align the goals of the foundry technology development group to that of PSS. Participated in the strategic planning of a technology roadmap and foundry strategy for the company.

9/97 to 9/98

AMIC Technology, Santa Clara, California

Director of Flash Technology. Responsible for developing 0.35μm ETOX-based flash memory technology. Prepared the business plan and technology roadmap. Developed a new integrated process flow, supervised testchip and product tapeout, process optimization, device optimization, and product yield enhancement.

5/96 to 9/97

Altera Corp., San Jose, California

Device Engineering Manager. Responsible for technology development, process integration, and foundry interface for 0.35μm generation of logic and EEPROM programmable logic device technology. Duties included project schedule planning, supervision of testchip and product tapeout, process optimization, and product yield enhancement.

7/95 to 5/96

Information Storage Devices, San Jose, California

Technology Development Manager/Program Manager. Led a project team of 10 in technology development, process integration, and first product introduction, with a new foundry. Duties included project schedule planning, supervision of testchip and product tapeout, process optimization, resolution of sorting issues and yield enhancement.

5/92 to 7/95

Advanced Micro Devices, Sunnyvale, California

Member of Technical Staff. Led the development of low-energy/DINOR-type flash EPROM technology. Key individual contributor in optimizing the process and design of flash cell and periphery devices in AMD's 0.5μm and 0.35μm flash EPROM technologies. Duties included process integration, device modeling, and development of triple-well technology and high-voltage transistors for negative gate erase operation.

1/89 to 4/92

Texas Instruments, Dallas, Texas

Member of Technical Staff. Research and development of 16Mb generation of flash EPROM technology, as well as a new generation of antifuse-based FPGAs. Duties included process integration, device modeling, high-voltage CMOS process integration, and investigation of a novel source-side injection mechanism for EPROM channel hot-electron programming.

AWARDS/HONORS

U.C. Berkeley Certificate of Distinction Award, 1983

AEA Faculty Development Fellowship, 1983-1985

AMD Spotlight Award, 1995

PATENTS

1. U.S. Patent 5,106,773, "Programmable Gate Array and Methods for Its Fabrication" (with K-L. Chen and H. Tigelaar), issued April 21, 1992.
2. U.S. Patent 5,166,557, "Gate Array with Built-in Programmable Circuitry" (with K.-L. Chen), issued November 24, 1992.
3. U.S. Patent 5,202,576, "Asymmetrical Non-Volatile Memory Cell, Arrays, and Methods for Fabricating the Same" (with M. Wong), issued April 13, 1993.
4. U.S. Patent 5,219,782, "Sublithographic Antifuse and method for Manufacturing" (with K.-L. Chen), issued June 15, 1993.
5. U.S. Patent 5,250,464, "Method of Making a Low Capacitance, Low Resistance Sidewall Antifuse Structure" (with M. Wong), issued October 5, 1993.
6. U.S. Patent 5,264,384, "Method of Making a Non-Volatile Memory Cell" (with C. Kaya), issued November 23, 1993.
7. U.S. Patent 5,300,803, "Source Side Injection Non-volatile Memory Cell," issued April 5, 1994.
8. U.S. Patent 5,365,105, "Sidewall Antifuse Structure and Method for Making," issued November 15, 1994.
9. U.S. Patent 5,371,402, "Low Capacitance, Low Resistance Sidewall Antifuse Structure and Process" (with M. Wong), issued December, 1994
10. U.S. Patent 5,395,797, "Antifuse Structure and Method of Fabrication," issued March 7, 1995.
11. U.S. Patent 5,470,773, "Method of Protecting a Stacked Gate Edge in a Semiconductor Device from Self Aligned Source (SAS) Etch" (with Y. Sun and C. Chang), issued November 28, 1995.
12. U.S. Patent 5,482,880, "Non-Volatile Memory and Fabrication Method," (with C. Kaya), issued January 9 1996.
13. U.S. Patent 5,517,443, "Method and System for Protecting a Stacked Gate Edge in a Semiconductor Device from Self Aligned Source (SAS) Etch in a Semiconductor Device," issued May 14, 1996.
14. U.S. Patent 5,521,867, "Adjustable Threshold Voltage Conversion Circuit" (with Jian Chen), issued May 28, 1996.
15. U.S. Patent 5,534,455, "Method and System for Protecting a Stacked Gate Edge in a Semiconductor Device from Self Aligned Source (SAS) Etch in a Semiconductor Device," issued July 9, 1996.
16. U.S. Patent 5,541,875, "High Energy Buried Layer Implant To Provide A Low Resistance P-Well in A Flash EPROM Array" (with Jian Chen), issued May 28, 1996.
17. U.S. Patent 5,590,076, "Channel Hot-Carrier Page Write," issued December 31, 1996.

18. U.S. Patent 5,596,531, "Method for Decreasing the Discharge Time of A Flash Memory Cell," issued January 21, 1997.
19. U.S. Patent 5,612,914, "Asymmetrical Non-volatile Memory Cell, Arrays and Methods for Fabricating Same" (with Man Wong), issued May 18, 1997.
20. U.S. Patent 5,624,859, "Method for Providing Device Isolation and Off-State Leakage Current for a Semiconductor Device," issued April 29, 1997.
21. U.S. Patent 5,625,220, "Sublithographic Antifuse," (with K.L. Chen), issued April 29, 1997.
22. U.S. Patent 5,646,430, "Non-volatile Memory Cell Having Lightly-Doped Source Region" (with C. Kaya), Issued July 8, 1997.
23. U.S. Patent 5,650,964, "Method of Inhibiting Degradation of Ultra Short Channel Charge-carrying Devices during Discharge," (with Jian Chen), Issued July 22, 1997.
24. U.S. Patent 5,652,155, "Method for Making Semiconductor circuit Including Non-ESD Transistors with Reduced Degradation Due to an Impurity Implant," Issued July 27, 1997.
25. U.S. Patent 5,656,509, "Method and Test Structure for Determining Gouging in a Flash EPROM Cell During SAS Etch," Issued July 29, 1997
26. U.S. Patent 5,661,059, "Boron Penetration to Suppress Short Channel Effect in P-channel Device," Issued August 26, 1997.
27. U.S. Patent 5,674,764, "Method of Making Asymmetrical Non-volatile Memory Cell," Issued October 7, 1997.
28. U.S. Patent 5,693,972, "Method and System for Protecting a Stacked Gate Edge in a Semiconductor Device from Self-Aligned Source (SAS) Etch in a Semiconductor Device," Issued December 2, 1997.
29. U.S. Patent 5,751,631, "Flash memory cell and a new method for sensing the content of the new memory cell," Issued May 12, 1998
30. U.S. Patent 5,789,295, "Method of Eliminating or Reducing Poly1 Oxidation at Stacked Gate Edge in Flash EPROM Process," Issued August 4, 1998.
31. U.S. Patent 5,814,854, "Highly scalable FLASH EEPROM cell," Issued September 29, 1998.
32. U.S. Patent 5,814,864, "Semiconductor Circuit Including Non-ESD Transistors with Reduced Degradation Due to an Impurity Implant," Issued September 29, 1998.
33. U.S. Patent 5,912,836, "Circuit for Detecting Both Charge Gain and Charge Loss Properties in a Non-Volatile Memory Array," Issued June 15, 1999.
34. U.S. Patent 5,930,174, "Circuit and Method for Erasing Flash Memory Array," Issued July 27, 1999.
35. U.S. Patent 5,981,994, "Method and Semiconductor circuit for Maintaining Integrity of Field Threshold Voltage Requirements," Issued November 9, 1999.

36. U.S. Patent 5,995,418, "Circuit and Method for Erasing Flash Memory Array," Issued November 30, 1999.
37. U.S. Patent 6,026,017, "Compact nonvolatile memory," Issued February 15, 2000.
38. U.S. Patent 6,027,974, "Nonvolatile memory," Issued February 22, 2000.
39. U.S. Patent 6,088,263, "Non-volatile memory using substrate electrons," Issued July 11, 2000.
40. U.S. Patent 6,091,636, "Flash memory cell and a new method for sensing the content of the new memory cell," Issued July 18, 2000.
41. U.S. Patent 6,127,225, "Memory cell having implanted region formed between select and sense transistors," Issued October 3, 2000.
42. U.S. Patent 6,159,800, "Method of forming memory cell," Issued December 12, 2000.
43. U.S. Patent 6,188,604, "Flash memory cell & array with improved pre-program and erase characteristics," Issued February 13, 2001.
44. U.S. Patent 6,185,133, "Flash EPROM using junction hot hole injection for erase," Issued February 6, 2001.
45. U.S. Patent 6,252,799, "Device with embedded Flash and EERPOM memories," Issued June 26, 2001.
46. U.S. Patent 6,326,265, "Device with Embedded Flash and EPROM Memories," Issued December 4, 2001.
47. U.S. Patent 6,417,550, "High voltage MOS devices with high gated-diode breakdown voltage and punch-through voltage," Issued July 9, 2002.
48. U.S. Patent 6,479,862, "Charge trapping device and method for implementing a transistor having a negative differential resistance mode," Issued November 12, 2002.
49. U.S. Patent 6,512,274, "CMOS-process compatible, tunable NDR (negative differential resistance) device and method of operating same," Issued January 28, 2003.
50. U.S. Patent 6,596,617, "CMOS compatible process for making a tunable negative differential resistance (NDR) device," Issued July 22, 2003.
51. U.S. Patent 6,624,026, "Nonvolatile Memory," Issued September 23, 2003.
52. U.S. Patent 6,680,245, "Method for making both a negative differential resistance (NDR) device and a non-NDR device using a common MOS process," Issued January 20, 2004.
53. U.S. Patent 6,686,631, "Negative differential resistance (NDR) device and method of operating same," Issued February 3, 2004.
54. U.S. Patent 6,693,027, "Method for configuring a device to include a negative differential resistance (NDR) characteristic," Issued February 17, 2004.
55. U.S. Patent 6,700,155, "Charge trapping device and method for implementing a transistor having a configurable threshold," Issued March 2, 2004.

56. U.S. Patent 6,711,063, "EEPROM memory cell array architecture for substantially eliminating leakage," Issued March 23, 2004.
57. U.S. Patent 6,835,979, "Nonvolatile Memory," Issued December 28, 2004.
58. U.S. Patent 6,969,894, "Variable threshold semiconductor device and method of operating same," Issued November 29, 2005.
59. U.S. Patent 6,972,234, "High Voltage MOS Devices with High Gated-Diode Breakdown Voltage and Punch-through Voltage," Issued December 6, 2005.
60. U.S. Patent 6,972,465, "CMOS process compatible, tunable negative differential resistance (NDR) device and method of operating same," Issued December 6, 2005.
61. U.S. Patent 7,067,873, "Charge Trapping Device," Issued June 27, 2006.
62. U.S. Patent 7,091,077, "Method of directionally trimming polysilicon width," Issued August 15, 2006.
63. U.S. Patent 7,109,078, "CMOS compatible process for making a charge trapping device," Issued September 19, 2006.
64. U.S. Patent 7,301,194, "Shrinkable and highly coupled double poly EEPROM with Inverter," Issued November 27, 2007.
65. U.S. Patent 7,436,710, "EEPROM memory device with cell having NMOS in a P pocket as a control gate, PMOS program/erase transistor, and PMOS access transistor in a common well," Issued October 14, 2008.
66. U.S. Patent 7,535,758, "One or Multiple-Times Programming Device," Issued May 19, 2009.
67. U.S. Patent 7,782,668, "Integrated circuit embedded with Non-volatile One-Time-Programmable and Multiple-Time Programmable memory," Issued August 24, 2010.
68. U.S. Patent 7,787,295, "Integrated circuit embedded with Non-volatile Multiple-Time Programmable memory having variable coupling," Issued August 31, 2010.
69. U.S. Patent 7,787,304, "Method of making integrated circuit embedded with Non-volatile One-Time-Programmable and Multiple-Time Programmable memory," Issued August 31, 2010.
70. U.S. Patent 7,787,309, "Method of operating integrated circuit embedded with Non-volatile One-Time Programmable and Multiple-Time Programmable memory," Issued August 31, 2010.
71. U.S. Patent 7,791,955, "Method of erasing a block of memory cells," Issued September 7, 2010.
72. U.S. Patent 7,835,184, "EEPROM memory cell with first-dopant-type control gate transistor, and second-dopant type program/erase and access transistors formed in common well," Issued November 16, 2010.
73. U.S. Patent 7,835,186, "Method of programming a selected memory cell," Issued November 16, 2010.

74. U.S. Patent 7,852,672, "Integrated Circuit embedded with Non-Volatile programmable memory having variable coupling," Issued December 14, 2010
75. U.S. Patent 7,876,615, "Method of operating integrated circuit embedded with Non-Volatile programmable memory having variable coupling related application data," Issued January 25, 2011
76. U.S. Patent 7,920,426, "Non-volatile memory programmable through areal capacitive coupling," Issued April 5, 2011
77. U.S. Patent 7,944,750, "Multi-programmable Non-Volatile Memory Cell," Issued May 17, 2011
78. U.S. Patent 8,203,861, "Non-Volatile One-Time Programmable and Multiple-Time Programmable Device," Issued June 19, 2012
79. U.S. Patent 8,208,299, "Integrated Circuit Embedded with Non-Volatile Programmable Memory Having Variable Coupling and Separate Read/Write Paths," Issued June 26, 2012
80. U.S. Patent 8,300,470, "Two Terminal Programmable Hot Channel Electron Non-Volatile Memory," Issued October 30, 2012
81. U.S. Patent 8,305,805, "Common Drain Non-Volatile Multiple-Time Programmable Memory," Issued November 6, 2012
82. U.S. Patent 8,325,519, "Method of Operating Integrated Circuit Embedded with Non-Volatile Programmable Memory having Variable Coupling Ratio," Issued December 4, 2012.
83. U.S. Patent 8,580,622, "Method of Making Integrated Circuit Embedded with Non-Volatile Programmable Memory having Variable Coupling," Issued November 12, 2013.
84. U.S. Patent 8,582,342, "Non-Volatile One-Time-Programmable and Multiple-Time Programmable Memory Configuration Circuit," Issued November 12, 2013.
85. U.S. Patent 8,599,612, "Method of Operating Integrated Circuit Embedded with Non-Volatile Programmable Memory having Variable Coupling Related Application data," Issued December 3, 2013.
86. U.S. Patent 8,705,263, "Non-Volatile One-Time-Programmable and Multiple-Time Programmable Memory Configuration Circuit," Issued April 22, 2014.
87. U.S. Patent 8,988,103, "Capacitively Coupled Logic Gate," Issued March 24, 2015.
88. U.S. Patent 9,064,192, "Automatic Valid Vote Count Storage using Secure Embedded Non-Volatile Memory," Issued June 23, 2015.
89. U.S. Patent 9,224,739, "Method of Making Integrated Circuit Embedded with Non-Volatile Programmable Memory having Variable Coupling," Issued December 29, 2015.
90. U.S. Patent 9,305,931, "Zero Cost NVM Cell Using High Voltage Devices in Analog Process," Issued April 5, 2016.

91. U.S. Patent 9,324,438, "Method of Operating Incrementally Programmable Non-Volatile Memory," Issued April 26, 2016.
92. U.S. Patent 9,558,813, "Method of Operating Incrementally Programmable Non-Volatile Memory," Issued January 31, 2017.
93. U.S. Patent 9,570,161, "Method of Operating Incrementally Programmable Non-Volatile Memory," Issued February 14, 2017.
94. U.S. Patent 9,570,175, "Incrementally Programmable Non-Volatile Memory," Issued February 14, 2017.
95. U.S. Patent 10,061,738, "Ephemeral Peripheral Device," Issued August 28, 2018.
96. U.S. Patent 10,115,467, "One time Accessible (OTA) Non-Volatile Memory," Issued October 30, 2018.
97. U.S. Patent 10,198,889, "Automatic Valid Vote Count Storage Using Secure Embedded Non-Volatile Memory," Issued February 5, 2019
98. U.S. Patent 10,559,700, "Zero Cost ANVM Cell Using High Voltage Devices in Analog Process," Issued February 11, 2020.
99. U.S. Patent 10,629,607, "Semiconductor CMOS Non-Volatile Memory Device," Issued April 21, 2020

(additional patent applications pending)

PUBLICATIONS

1. S.D. Leeke, D. K. Y. Liu and J. P. McVittie, "Plasma mode trench etching with direct hydrocarbon injection," *Materials Research Society Symposium Proceedings*, Vol. 68, pp. 21-27, 1986.
2. D. K. Y. Liu and J. D. Plummer, "A novel trench-injector power device with low ON-resistance and high switching speed," *IEEE Electron Device Letters*, Vol. 9, No. 7, pp. 321-323, 1988.
3. D. M. Boisvert, D. K. Y. Liu and J. D. Plummer, "Circuit approaches to increasing IGBT switching speed," *IEEE Journal of Solid-State Circuits*, Vol. 23, No. 5, pp. 1276-1279, 1988.
4. D. K. Y. Liu and J. D. Plummer, "Device physics and optimization of conductivity-modulated power MOSFET's," *IEEE Transactions on Electron Devices*, Vol. 35, No. 12, pp. 2457-2458, 1988.
5. D. K. Y. Liu, K.-L. Chen, H. Tigelaar, J. Paterson and S. O. Chen, "Scaled dielectric antifuse structure for field-programmable gate array applications," *IEEE Electron Device Letters*, Vol. 12, No. 4, pp. 151-153, 1991.
6. M. Wong, D. K. Y. Liu, M. M. Moslehi and D. W. Reed, "Preoxidation treatment using HCl/HF vapor," *IEEE Electron Device Letters*, Vol. 12, No. 8, pp. 425-426, 1991.
7. D. K. Y. Liu, C. Kaya, M. Wong, J. Paterson and P. Shah, "Optimization of a source-side injection FAMOS cell for flash EPROM applications," *International Electron Devices Meeting Technical Digest*, pp. 315-318, 1991.
8. K.-L. Chen, D. K. Y. Liu, G. Misium, W. M. Gosney, S.-J. Wang, J. Camp and H. Tigelaar, "A sublithographic antifuse structure for field-programmable gate array applications," *IEEE Electron Device Letters*, Vol. 13, No. 1, pp. 53-55, 1992.
9. K. T. San, C. Kaya, D. K. Y. Liu, T. P. Ma, and P. Shah, "A new technique for determining capacitive coupling coefficients in flash EPROMs," *IEEE Electron Device Letters*, Vol. 13, No. 6, pp. 328-331, 1992.
10. C. Kaya, D. K. Y. Liu, J. Paterson and P. Shah, "Buried source-side injection (BSSI) for flash EPROM programming," *IEEE Electron Device Letters*, Vol. 13, No. 9, pp. 465-467, 1992.
11. M. Wong, D. K. Y. Liu and S. S.-W. Huang, "Analysis of the subthreshold slope and the linear transconductance techniques for the extraction of the capacitance coupling coefficients of floating-gate devices," *IEEE Electron Device Letters*, Vol. 13, No. 11, pp. 566-568, 1992.
12. D. K. Y. Liu and J. D. Plummer, "Design and analysis of a new conductivity-modulated power MOSFET," *IEEE Transactions on Electron Devices*, Vol. 40, No. 2, pp. 428-438, 1993.
13. J. Z. Peng, S. Haddad, H. Fang, C. Chang, S. Longcor, B. Ho, Y. Sun, D. Liu, Y. Tang, J. Hsu, S. Luan, J. Lien, "Flash EPROM endurance simulation using physics-based models," In *International Electron Devices Meeting Technical Digest*, pp. 295-298, 1994.
14. J. Chen, J. Hsu, S. Luan, Y. Tang, D. Liu, S. Haddad, C. Chang, S. Longcor, J. Lien, "Short Channel enhanced degradation during discharge of Flash EEPROM memory Cell," *International Electron Devices Meeting Technical Digest*, pp. 331-334, 1995.

15. V. H. Chan and D. Liu, "An Enhanced Erase Mechanism During Channel Fowler-Nordheim Tunneling in Flash EPROM Memory Devices," *IEEE Electron Devices Letters*, Vol. 20, No. 3, pp. 140-142, 1999.