

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

APPLE INC.
Petitioner

v.

ARIGNA TECHNOLOGY LTD
Patent Owner

Case No. IPR2023-00453
U.S. Patent No. 7,183,835

**PETITION FOR *INTER PARTES* REVIEW
OF U.S. PATENT NO. 7,183,835**

TABLE OF CONTENTS

TABLE OF CONTENTS	I
I. INTRODUCTION	1
II. SUMMARY OF THE '835 PATENT	1
A. THE '835 PATENT'S ALLEGED INVENTION.....	1
B. PROSECUTION HISTORY OF THE '835 PATENT	6
C. THE BOARD SHOULD EXERCISE ITS DISCRETION UNDER § 325(D)—THE EXAMINER MATERIALLY ERRED BY FAILING TO CONSIDER <i>OHI</i> 'S FIG. 12 EMBODIMENT	7
D. A PERSON OF ORDINARY SKILL IN THE ART	14
III. PROCEDURAL REQUIREMENTS UNDER 37 C.F.R. § 42.104	14
A. STANDING UNDER 37 C.F.R. § 42.104(A)	14
B. CHALLENGE UNDER 37 C.F.R. § 42.104(B) AND RELIEF REQUESTED	14
C. CLAIM CONSTRUCTION UNDER 37 C.F.R. § 42.104(B)(3).....	15
IV. THE CHALLENGED CLAIMS ARE UNPATENTABLE.....	16
A. GROUND 1: CLAIMS 1 AND 2 ARE ANTICIPATED BY U.S. PATENT NO. 6,906,574 TO OHI, ET AL. (" <i>OHI</i> ").	16
<i>Overview of Ohi</i>	16
<i>i. Claim 1</i>	23
<i>ii. Claim 2</i>	53
V. THE BOARD SHOULD NOT DENY INSTITUTION UNDER FINTIV	59
VI. CONCLUSION	60
VII. MANDATORY NOTICES UNDER 37 C.F.R. § 42.8(A)(1).....	61
A. REAL PARTY-IN-INTEREST	61
B. RELATED MATTERS	61
C. LEAD AND BACK-UP COUNSEL.....	61

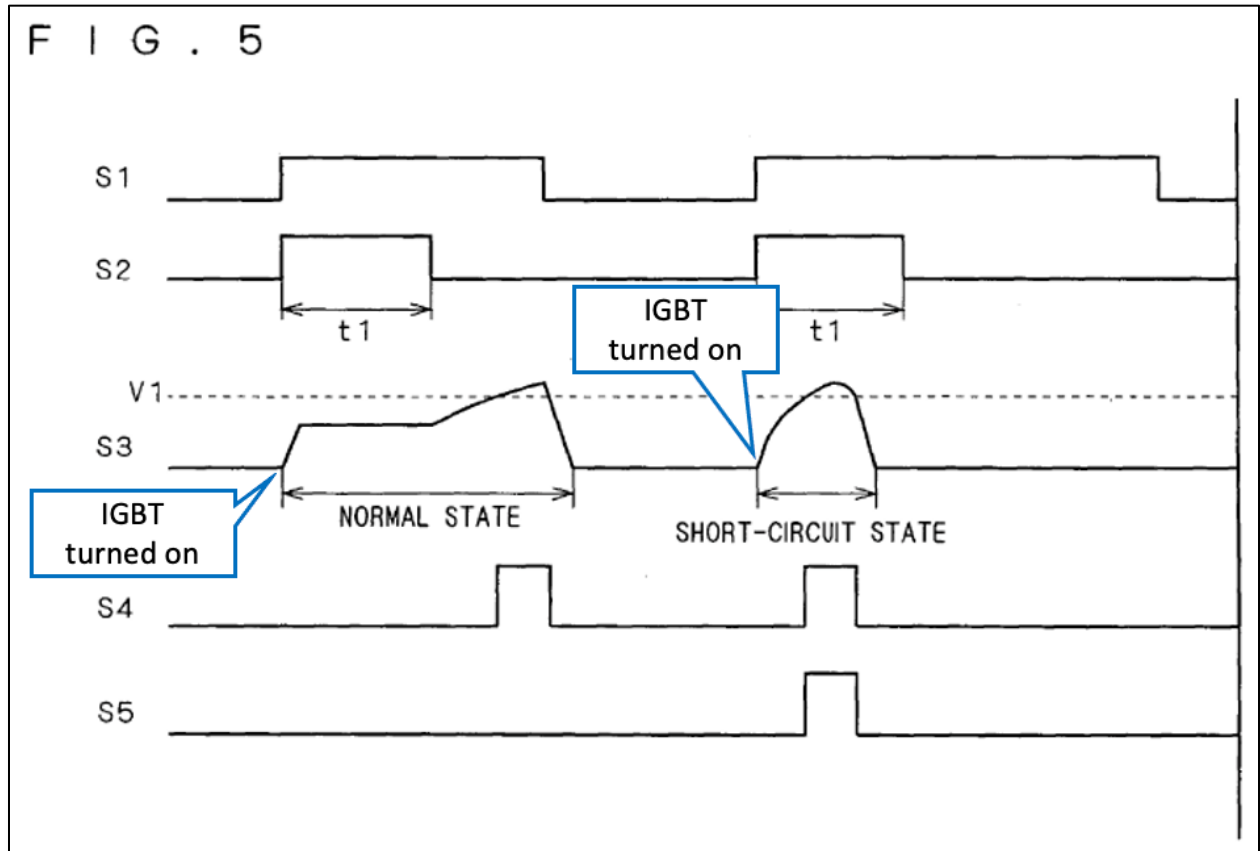
I. INTRODUCTION

Petitioner Apple Inc. (“Petitioner”) requests *Inter Partes* Review (“IPR”) of Claims 1 and 2 (the “Challenged Claims”) of U.S. Patent No. 7,183,835 (“the ’835 Patent”).

II. SUMMARY OF THE ’835 PATENT

A. The ’835 Patent’s Alleged Invention

The ’835 Patent is generally directed to a semiconductor device that controls the drive of an insulated gate bipolar transistor (IGBT) and provides short-circuit protection for the IGBT. ’835 *Patent* (Ex. 1001), 1:10-25. The short-circuit protection proposed by the ’835 Patent is premised on the fact that, during a short period of time after the IGBT is turned on, the IGBT’s gate voltage rises much faster when the IGBT is short-circuited as compared to the gate voltage rise in a normal operating state. *Id.* at 4:8-20. This difference is depicted in Fig. 5 below:



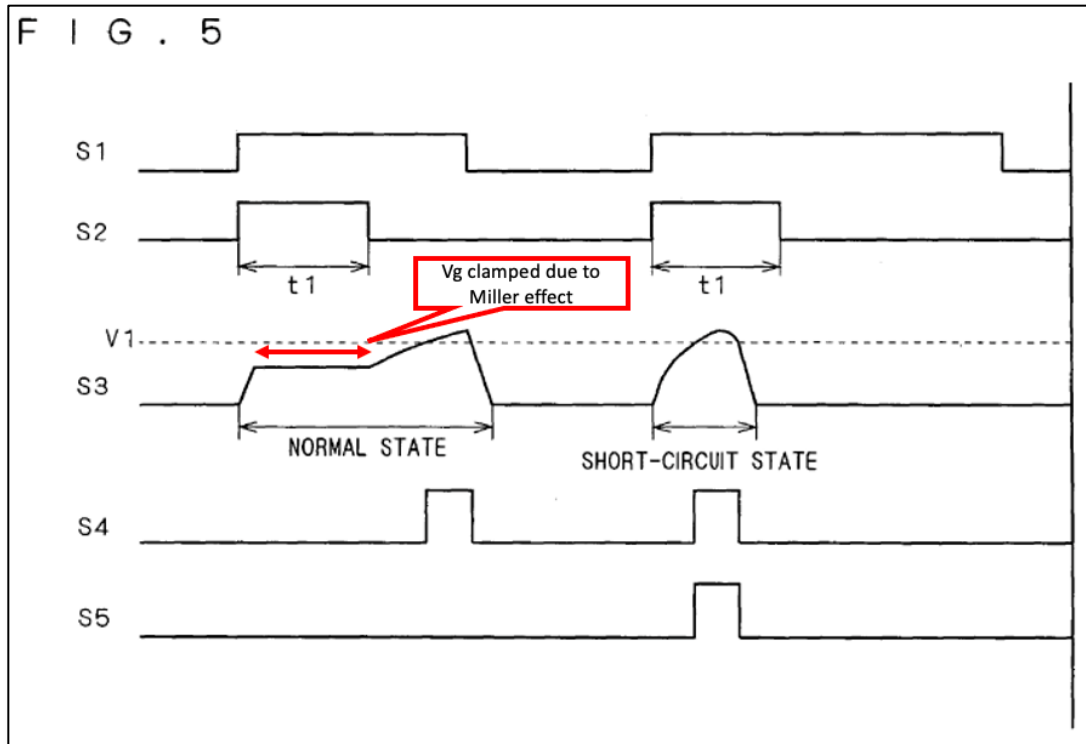
Id. at Fig. 5 (annotated). As shown, when the IGBT is turned on and exhibits normal operations (i.e., is not short circuited), gate voltage (S3) initially rises to a midpoint voltage, where it remains for a period of time, before slowly rising to threshold voltage V1. Conversely, when the IGBT is turned on and experiences a short circuit condition, gate voltage (S3) rises quickly to threshold voltage V1. This difference in the speed at which the gate voltage reaches the threshold voltage V1 forms the foundation of the '835 Patent's process of detecting a short circuit state. As illustrated above, if V1 is reached within the time period t1, the system assumes the IGBT is short circuited.

This timing differential is a direct result of what's known as the Miller effect. The '835 Patent describes a phenomenon in IGBT devices in which the gate voltage sticks at a mid-point voltage (referred to as "clamped" at that voltage) following a turn-on instruction for a period of time before rising to the normal operating voltage that is near V_{cc} :

[W]hen a voltage of the control output signal S3 exceeds a threshold value of the transistor 12, the transistor 12 comes to be in ON state, and a collector-emitter voltage of the transistor 12 drops, thus a voltage of the control output signal S3 is clamped to a certain voltage for a determined period by a [Miller]¹ effect, however, the voltage of the control output signal S3 rises to be a value almost equal to the drive voltage VCC of the gate driver GD after that.

'835 *Patent* (Ex. 1001), 5:62-6:3 (emphasis added). This clamping at a mid-point voltage for a period after the IGBT is turned on is illustrated in Fig. 5:

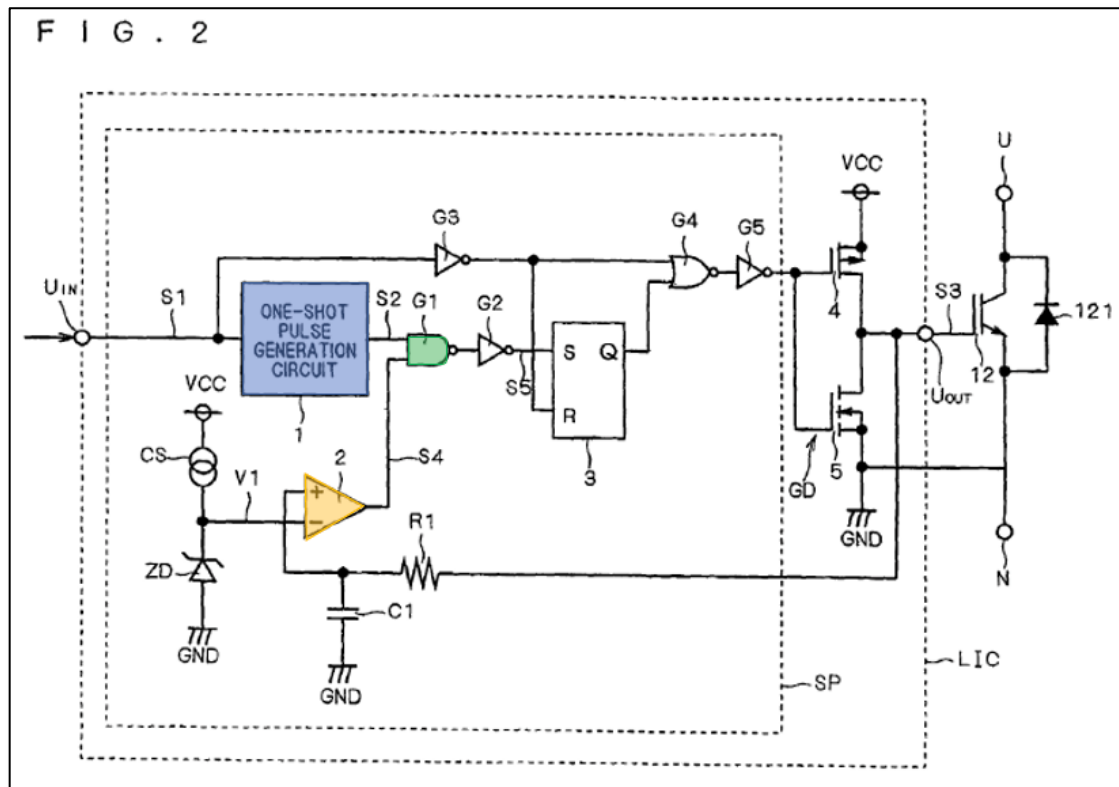
¹As explained in detail below with reference to Claim 2, the '835 Patent uses the term "mirror effect," which is a clerical error and should instead be "Miller effect."



Id. at Fig. 5 (annotated). The '835 Patent further teaches that this clamped/Miller period is used to define the short-circuit detection period t_1 , i.e., the time period during which the system measures the gate voltage to detect it exceeding a reference voltage V_1 . *Id.* at 6:35-40 (noting that “period t_1 ” can be “almost equal to a period when the control output signal S3 is clamped to a certain voltage.”). As illustrated in Fig. 5 above, the Miller effect clamping prevents the IGBT gate voltage from exceeding reference voltage V_1 during the measurement period. Because a short circuit condition will not be similarly clamped, V_g will exceed the reference voltage V_1 even within the time period t_1 .

When such a short circuit condition is detected, the '835 Patent proposes turning the IGBT off by “forcing the driver to stop the control output signal.” *Id.* at

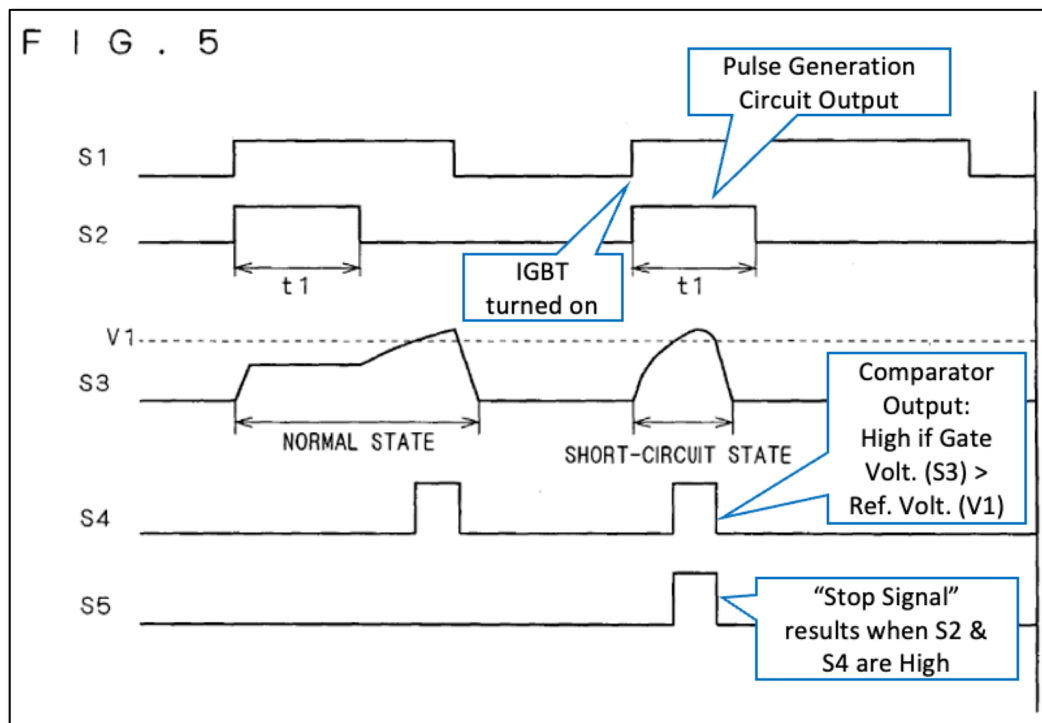
1:52-62. As recited in claim 1 of the '835 Patent and as illustrated in Fig. 2 below, the short-circuit protection circuit includes three main elements: a pulse generation circuit, a comparator, and a logical circuit:



Id. at Fig. 2 (annotated), 11:49-65 (Claim 1). As illustrated, the pulse generation circuit (1) receives a control input signal (U_{IN})—the signal that causes IGBT 12 to turn on—and outputs a first pulse signal (S2) that is maintained as a high signal for a predetermined period. *Id.* at 4:56-60. Comparator (2) compares the gate voltage of IGBT 12 (S3) to a reference voltage (V1), outputting a high signal when the gate voltage exceeds the reference voltage. *Id.* at 4:27-42. Finally, the logical circuit (G1) receives the outputs from the pulse generation circuit (S2) and the comparator (S4)

and outputs a “stop signal” when both outputs are high, forcing IGBT 12 into an off state. *Id.* at 7:4-21.

In sum, the proposed circuit can detect a short circuit when the gate voltage of IGBT 12 exceeds reference voltage (V1) quickly after being turned on. When such a state is detected, the circuit forces IGBT 12 to an off state. Fig. 5 below is annotated to reflect this process:



Id. at Fig. 5 (annotated).

B. Prosecution History of the '835 Patent

The '835 Patent issued from U.S. Application Serial No. 11/023,590 (the "'590 Application"), filed on December 29, 2004. '835 *Patent* (Ex. 1001). A first office action mailed July 7, 2007 (the "Office Action") rejected originally proposed

claim 1 under 35 U.S.C. 102(e) as being anticipated by U.S. Patent Application Publication No. 2004/0252432 to Sasaki et al. (“*Sasaki*”) and by U.S. Patent No. 6,906,574 to Ohi, et al. (“*Ohi*”). ’835 *Patent File History* (Ex. 1002), 194-206. The Office Action indicated that originally proposed claims 2 and 3 would be allowable if incorporated into independent claim 1. *Id.* at 201-202. Specifically, the Examiner identified Claim 2’s recitation of the following three elements of the short-circuit protection circuit that were allegedly not taught by *Sasaki* or *Ohi*: a pulse generation circuit, a comparator, and a logical circuit. *Id.* (observing that the short-circuit protection circuit in *Ohi* lacks “the relationship between the pulse generation circuit, comparator, and logical circuit as recited within claim 2”). *Id.* In response to the Office Action, proposed claim 2 was rewritten in independent form and ultimately issued at claim 1 of the ’835 Patent. *Id.* at 211-226, 235-242.

The face of the ’835 Patent references two separate Japanese priority filings. For purposes of this petition only, and without waiving its right to challenge the correct priority date, Petitioner applies the earliest of these Japanese filings—January 6, 2004—as the priority date for the ’835 Patent.

C. The Board Should Decline to Exercise its Discretion Under § 325(d)—the Examiner Materially Erred by Failing to Consider *Ohi*’s Fig. 12 Embodiment

The Proposed Grounds rely on the same *Ohi* reference relied upon by the Examiner in the sole office action issued during the ’835 Patent’s prosecution.

However, the Examiner focused entirely on *Ohi*'s second embodiment, depicted in Fig. 6, concluding that *Ohi* did not teach certain structural limitations in original proposed claim 2 and deeming those limitations allowable if incorporated into claim 1. *Id.* at 200-201 (discussing only Fig. 6 and its corresponding disclosure). The Examiner critically overlooked that *Ohi*'s fifth embodiment, depicted in Fig. 12, taught precisely that which was deemed lacking in Fig. 6. Because the Examiner erred in a manner material to patentability, 35 U.S.C. § 325(d) is no bar to institution.

Under § 325(d), the Board utilizes a two-part framework set forth in the Boards' *Advanced Bionics* decision. *Advanced Bionics, LLC v. MED-EL Elektromedizinische Geräte GmbH*, IPR2019-01469, Paper 6, *8 (PTAB Feb. 13, 2020) (precedential). The two-part framework asks the Board to assess "(1) whether the same or substantially the same art previously was presented to the Office or whether the same or substantially the same arguments previously were presented to the Office; and (2) if either condition of first part of the framework is satisfied, whether the petitioner has demonstrated that the Office erred in a manner material to the patentability of challenged claims." *Id.* at *8.

Ohi is "[p]reviously presented art" under part-one of the *Advanced Bionics* framework. *Id.* at *7-8. Accordingly, the analysis turns to part-two of the *Advanced Bionics* framework, which asks the Board to consider "whether the petitioner has demonstrated that the Office erred in a manner material to the patentability of

challenged claims.” *Id.* An example of a material error may include misapprehending or overlooking specific teachings of the relevant prior art where those teachings impact patentability of the challenged claims. *Id.* at *8, note 9. Here, the Examiner overlooked *Ohi*’s fifth embodiment, depicted in Fig. 12, which shows a pulse generation circuit, a comparator, and a logical circuit arranged precisely as required by originally proposed claim 2.

In applying the *Advanced Bionics* framework, the Board considers several non-exclusive “*Becton, Dickinson* factors”.² See *Becton, Dickinson & Co. v. B. Braun Melsungen AG*, IPR2017-01586, Paper 8, *17-18 (PTAB Dec. 15, 2017) (precedential as to § III.C.5, ¶1). *Becton, Dickinson* factors (c), (e), and (f) “relate to

² The *Becton, Dickinson* factors include:

- (a) the similarities and material differences between the asserted art and the prior art involved during examination;
- (b) the cumulative nature of the asserted art and the prior art evaluated during examination;
- (c) the extent to which the asserted art was evaluated during examination, including whether the prior art was the basis for rejection;
- (d) the extent of the overlap between the arguments made during examination and the manner in which petitioner relies on the prior art or patent owner distinguishes the prior art;
- (e) whether petitioner has pointed out sufficiently how the examiner erred in its evaluation of the asserted prior art; and
- (f) the extent to which additional evidence and facts presented in the petition warrant reconsideration of the prior art or arguments.

whether the petitioner has demonstrated a material error by the Office” in its prior consideration of the prior art or arguments. *Advanced Bionics*, *10.

Becton, Dickinson factor (c) asks the Board to consider “the extent to which the asserted art was evaluated during examination, including whether the prior art was the basis for rejection.” *Becton, Dickinson* at *17-18. Here, *Ohi* was the basis for rejection. However, *Advanced Bionics* made clear that, “if the record of the Office’s previous consideration of the art is not well developed or silent, then a petitioner may show the Office erred by overlooking something persuasive under [*Becton, Dickinson*] factors (e) and (f).” *Id.* at *10-11 (“Factor (c) focuses on the record developed by the Office in previously reviewing the art or arguments.”). Here, although *Ohi* was considered by the Examiner, the record indicates that the Examiner considered only *Ohi*’s second embodiment, ignoring that *Ohi*’s fifth embodiment taught precisely that which the Examiner deemed lacking in the second embodiment.

As set forth in detail below, the Examiner erred in a manner material to patentability. Pursuant to *Becton, Dickinson* factors (e) and (f), the Board should conclude that 35 U.S.C. § 325(d) is no bar to institution.

During the ’835 Patent’s prosecution, the Examiner concluded that *Ohi*’s Fig. 6 circuit did not teach “the relationships between the pulse generation circuit, comparator, and logical circuit as recited within [originally proposed] claim 2[.]”

'835 *Patent File History* (Ex. 1002), 201. That claimed relationship requires a logical circuit that receives the outputs from both the pulse generation circuit and the comparator:

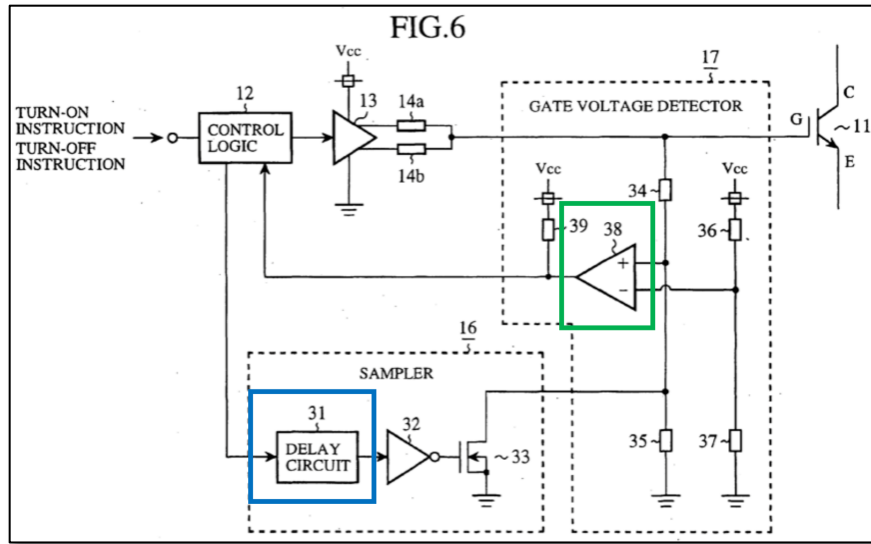
said short-circuit protection circuit includes:

pulse generation circuit receiving said control input signal and outputting a first pulse signal being significant only in said predetermined period according to a timing when said control input signal indicates the [[a]] conduction of said insulated gate transistor;

a comparator receiving the [[a]] detecting voltage of said control output signal, performing a comparison with said reference voltage and outputting a second pulse signal being significant during a period when the [[a]] detecting voltage of said control output signal exceeds said reference voltage; and

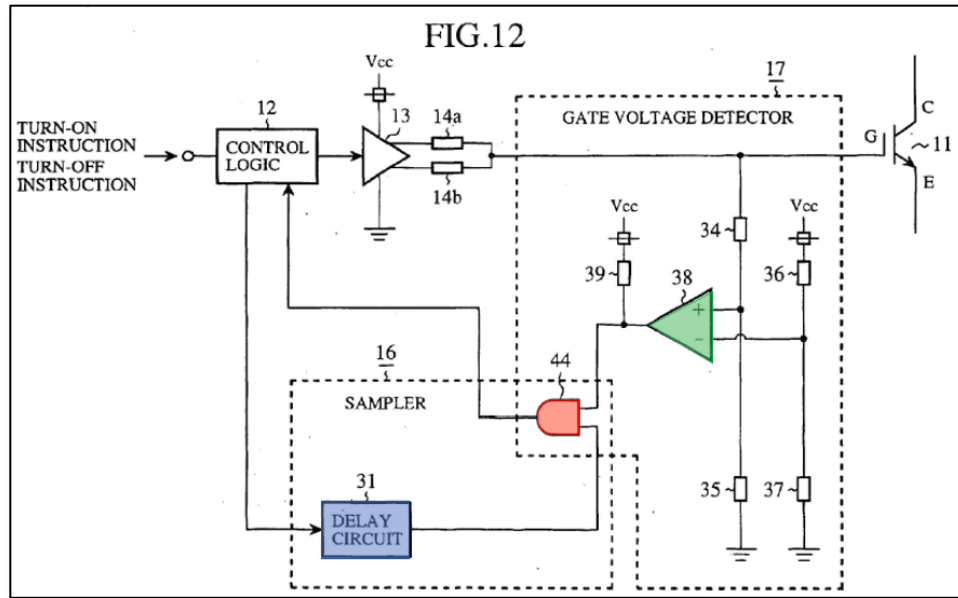
a logical circuit receiving said first and second pulse signals and outputting a stop signal forcing said driver to stop ~~an output of~~ said control output signal when said second pulse signal becomes significant during a period when said first pulse signal is significant.

Id. at 219 (annotated to highlight relationship between key components). As shown in an annotated version of *Ohi*'s Fig. 6 below, there is no such logical circuit in *Ohi*'s second embodiment. Rather, the pulse generation circuit (including delay circuit 31) produces an output that feeds into comparator 38, and there is no logical circuit at all that would satisfy the claimed relationship:



Ohi (Ex. 1004), Fig. 6 (annotated).

Ohi's fifth embodiment (as illustrated in Fig. 12), on the other hand, depicts precisely that which was missing from Fig. 6 relied upon by the Examiner. As illustrated below, a **pulse generation circuit** (**delay circuit 31**) generates a first pulse signal, a **comparator 38** generates a second pulse signal, and a **logical circuit** (**AND gate 44**) receives the first and second pulse signals, as claimed:



Id. at Fig. 12 (annotated). Indeed, **logical circuit 44** in *Ohi's* Fig. 12 performs the same function as the claimed logical circuit, generating a stop signal that causes IGBT to be turned off when a short circuit is detected. *Id.* at 12:53-60 (“[W]hen a short circuit occurs in the IGBT 11, the output-signal of the AND circuit 44 becomes a High level (i.e., a logical level indicating a detection of the occurrence of an abnormality in the IGBT . . . [.]) After that, the drive circuit operates in the same way that that of embodiment 2 does[.]”), 10:14-21 (describing embodiment 2, teaching that the circuit “delivers an abnormality signal to the control logic 12[, and, a]s a result, the control logic 12 causes the IGBT 11 to become turned-off[.]”)

In sum, the Examiner made a material error by failing to consider *Ohi's* Fig. 12, which shows the precise circuit arrangement that the Examiner deemed lacking in *Ohi's* Fig. 6. The proposed ground herein focuses on *Ohi's* fifth embodiment, as

depicted in Fig. 12, and does not ask the Board to reconsider the circuit in Fig. 6 that was rejected by the Examiner during prosecution. Accordingly, the Board should decline to exercise its discretion under § 325(d) and should institute *inter partes* review of the Challenged Claims.

D. A Person of Ordinary Skill in the Art

A person of ordinary skill in the art (“POSITA”) at the time of the ’835 Patent would have had a graduate degree in electrical engineering or equivalent with at least two years of relevant work experience (e.g., in the field of circuit design). Additional education or experience might substitute for the above requirements. *Dec.* (Ex. 1004), ¶¶ 22-24.

III. PROCEDURAL REQUIREMENTS UNDER 37 C.F.R. § 42.104

A. Standing Under 37 C.F.R. § 42.104(A)

Petitioner certifies that the ’835 Patent is available for IPR and that Petitioner is not barred or estopped from requesting an IPR challenging the claims of the ’835 Patent. Specifically, (1) Petitioner is not the owner of the ’835 Patent, (2) Petitioner has not filed a civil action challenging the validity of the claims of the ’835 Patent, and (3) this Petition is filed less than one year after the Petitioner was served with a complaint alleging infringement of the ’835 Patent.

B. Challenge Under 37 C.F.R. § 42.104(B) and Relief Requested

In view of the prior art and evidence presented, claims 1 and 2 of the ’835 Patent are unpatentable and should be cancelled. 37 C.F.R. § 42.104(b)(1). Further,

based on the prior art references identified below, IPR of the Challenged Claims should be granted. 37 C.F.R. § 42.104(b)(2).

Proposed Ground of Unpatentability	Exhibits
Ground 1: Claims 1 and 2 are anticipated under pre-AIA 35 U.S.C. § 102 by U.S. Patent No. 6,906,574 to Ohi, et al. (“ <i>Ohi</i> ”).	Ex. 1003

Section IV identifies where each element of the Challenged Claims is found in the prior art. 37 C.F.R. § 42.104(b)(4). The exhibit numbers of the evidence relied upon to support the challenges are provided above and the relevance of the evidence to the challenges raised is provided in Section IV. 37 C.F.R. § 42.104(b)(5). **Exhibits 1001-1006** are also attached.

C. Claim Construction Under 37 C.F.R. § 42.104(B)(3)

In this proceeding, claims are interpreted under the same standard applied by Article III courts (i.e., the *Phillips* standard). *See* 37 C.F.R § 42.100(b); *see also* 83 Fed. Reg. 197 (Oct. 11, 2018); *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312 (Fed. Cir. 2005) (en banc). Under this standard, words in a claim are given their plain meaning which is the meaning understood by a person of ordinary skill in the art in view of the patent and file history. *Phillips*, 415 F.3d 1303, 1212–13.

Although the parties are disputing a number of terms in a pending action before the International Trade Commission (ITC), Petitioner proposes that the Board need not construe any claim language to resolve the Proposed Ground.

IV. THE CHALLENGED CLAIMS ARE UNPATENTABLE

A. Ground 1: Claims 1 and 2 are anticipated by U.S. Patent No. 6,906,574 to Ohi, et al. (“*Ohi*”).

Overview of Ohi

U.S. Patent No. 6,906,574 to Ohi et al. (“*Ohi*”) (Ex. 1003) was filed on July 28, 2003, issued on June 14, 2005, and is prior art to the ’835 Patent under at least 35 U.S.C. § 102(e) (pre-AIA). *Ohi* was cited and considered during prosecution of the ’835 Patent. ’835 *File History* (Ex. 1002). However, for at least the reasons discussed above in Section II.C, the Office erred in a manner material to the patentability of the challenged claims, so the Board should institute the proposed ground, which relies entirely on *Ohi*’s fifth embodiment—a teaching the Examiner did not discuss during prosecution.

Ohi is generally directed to “a drive circuit for driving a power semiconductor device and for detecting occurrence of an abnormality in the power semiconductor device.” *Ohi* (Ex. 1003), 1:8-10. More specifically, like the ’835 Patent, *Ohi*’s circuit is “capable of promptly detecting occurrence of a short circuit so as to protect the power semiconductor device even when applied to a high-voltage IGBT.” *Id.* at 2:35-41.

Ohi teaches precisely the process described by the ’835 Patent and even acknowledges that it is also based on the Miller effect. Namely, *Ohi* describes a “Miller time period” during which the IGBT’s gate voltage is clamped:

When the drive circuit sends a gate instruction to instruct the IGBT 11 to turn on in response to a turn-on instruction under normal operating conditions, the gate voltage V_g of the IGBT 11 starts rising. When the gate voltage V_g then exceeds a threshold voltage, the collector current I_c starts increasing. When the collector current I_c flowing in the IGBT 11 becomes nearly equal to an inductive load electric current flowing through the inductive load, the collector-emitter voltage V_{ce} starts decreasing and **the gate voltage V_g then becomes a nearly-constant voltage. This time period** during which the gate voltage V_g is nearly constant after the collector current I_c has become nearly equal to the inductive load electric current **is known as a Miller time period. . . . At the conclusion of the Miller time period, the gate voltage V_g starts rising again.** At this time, **the gate voltage rises slowly** with a smaller time constant than that with which the gate voltage has risen before the Miller time period because the feedback capacitance is large, **and then reaches a certain on-state gate voltage.** The gate voltage V_g enters a steady state after it has experienced the above-mentioned transition time period.

Ohi (Ex. 1003), 5:61-6:25 (emphasis added).

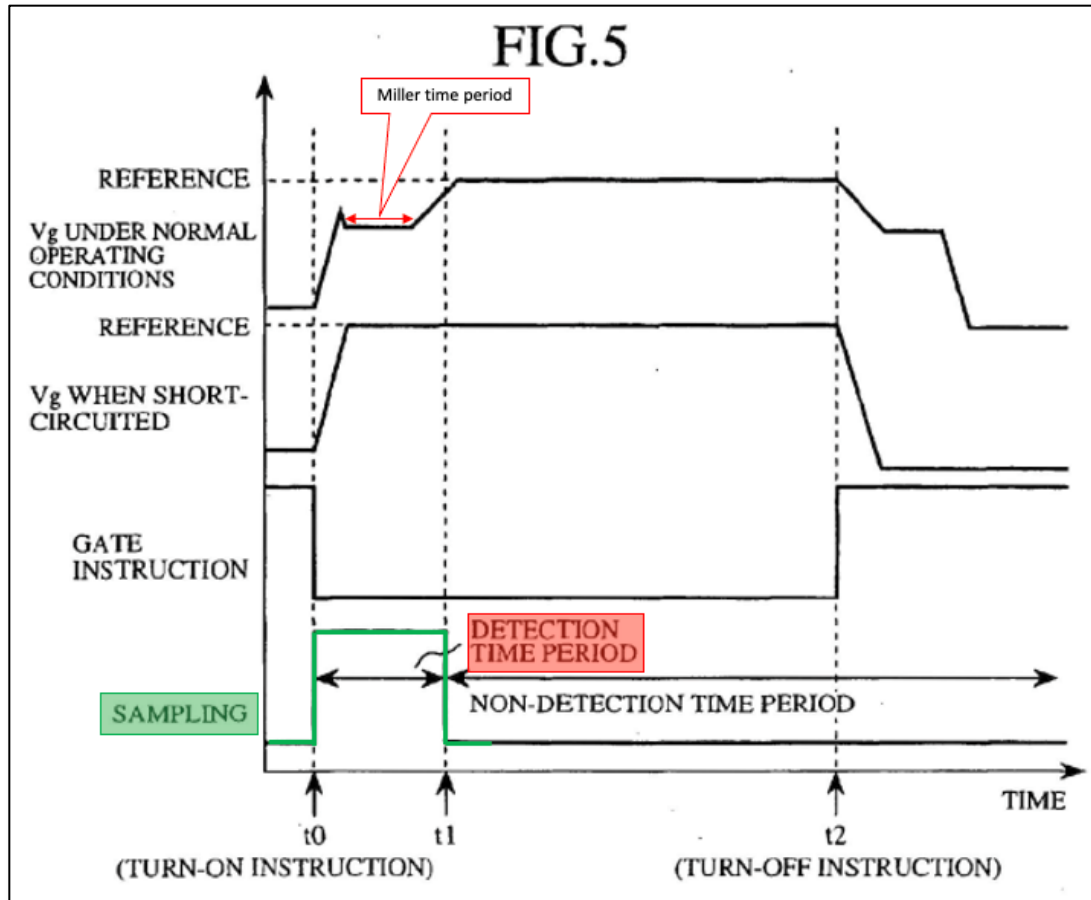
Like the '835 Patent, *Ohi* also uses the Miller time period (i.e., the time during which the IGBT gate voltage is clamped) to define the measurement/detection period during which V_g is monitored, ensuring that the detection period ends before V_g reaches its normal operating voltage when not short circuited:

[W]hen the control logic 12 receives a turn-on instruction from outside the drive circuit, as shown in FIG. 5, the **sampler 16 enables the gate**

voltage detector 17 to detect the gate voltage V_g at the time t_0 when the turn-on instruction is received. After that, when a certain time elapses and a time t_1 (before the gate voltage V_g reaches the on-state gate voltage, and the time t_1 is determined in consideration of the characteristics of the IGBT 11) comes, the sampler 16 disables the gate voltage detector 17 to detect the gate voltage V_g . The sampler 16 only has to be able to prevent the detection of the gate voltage V_g during a time period from the time t_1 to a time t_2 when a turn-off instruction is received, and the detection time period from the time t_0 to the time t_1 can include an off-state time period (i.e., a time period before the time t_0 or a time period after the time t_2).

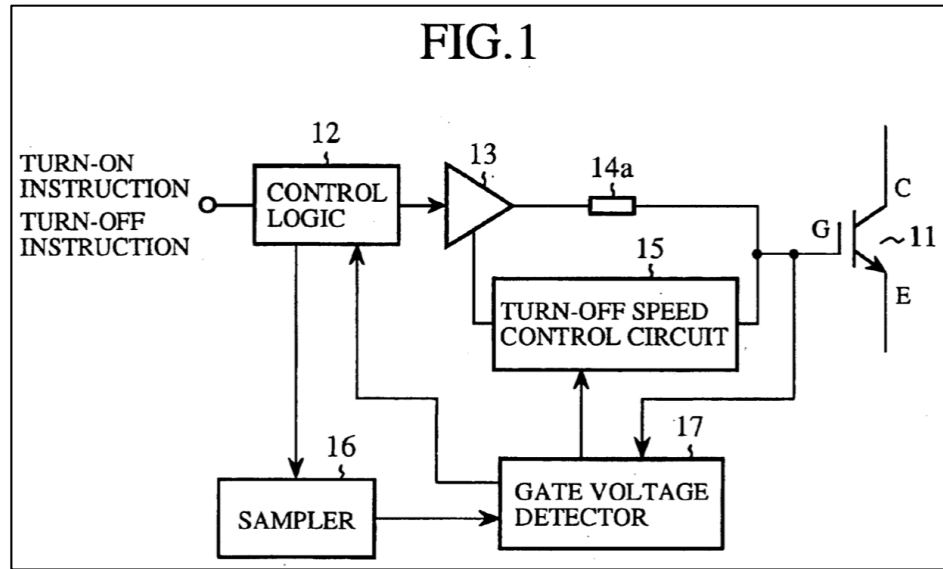
The gate voltage detector 17 detects the gate voltage V_g that appears at the gate terminal of the IGBT 11 throughout the detection time period during which the sampler 16 enables the process of detecting the gate voltage V_g . **When the gate voltage V_g exceeds the reference value during the detection time period, the gate voltage detector 17 recognizes the occurrence of an abnormality in the IGBT 11 and delivers an abnormality signal to the control logic 12 and the turn-off speed control circuit 15.**

Id. at 7:32-56 (emphasis added). This timing depicted in Fig. 5 below:



Id. at Fig. 5 (annotated).

As discussed in Section II.C, the focus of the instant challenge is *Ohi*'s fifth embodiment, as depicted in Fig. 12. For context, however, Fig. 1 of *Ohi* below provides a block diagram that depicts the general "structure of a drive circuit for driving a power semiconductor device" according to the first embodiment in *Ohi*—concepts that also carry over to subsequent embodiments. *Id.* at 4:37-38. With reference to Fig. 1 below, "the power semiconductor device driven by the drive circuit" may be "an IGBT (Insulated Gate Bipolar Transistor)[.]" *Id.* at 4:40-42.



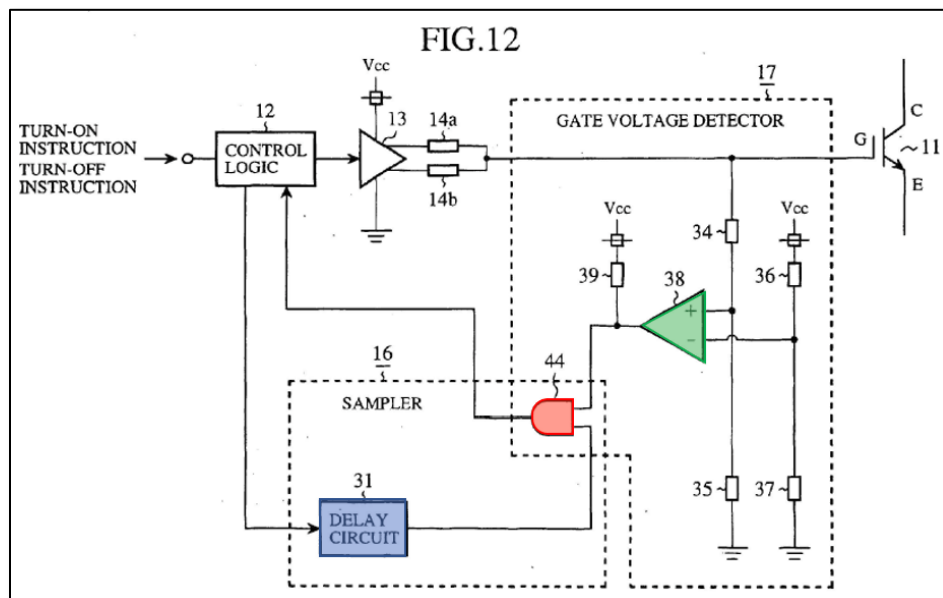
Id. at Fig. 1. “Reference numeral 12 denotes a control logic for sending a gate instruction to turn on the IGBT 11 to a buffer 13 in response to a turn-on instruction from outside the drive circuit, and for sending a gate instruction to turn off the IGBT 11 to the buffer 13 in response to a turn-off instruction from outside the drive circuit.” *Id.* at 4:45-50. Fig. 1 also generally depicts short circuit detection aspects of *Ohi*’s embodiments. For example, “[r]eference numeral 16 denotes a sampler (i.e., a controllable variable value detection means) for allowing a process of detecting a gate voltage V_g . . . of the IGBT 11 only during a transition time period . . . immediately after the control logic 12 has received a turn-on instruction[.]” *Id.* at 4:64-5:3. “[R]eference numeral 17 denotes a gate voltage detector (i.e., a controllable variable value detection means and an abnormality detection means) that detects the gate voltage V_g that appears at the gate terminal of the IGBT 11 . . .

throughout a time period during which the sampler 16 allows the process of detecting the gate voltage $V_g[.]$ ” *Id.* at 5:4-11.

Ohi’s fifth embodiment,³ as depicted in Fig. 12 below, utilizes three key components to detect a short circuit abnormality immediately following a turn-on

³ *Ohi* expressly teaches that its fifth embodiment includes components and functionalities identical to those in earlier described embodiments and does not repeat descriptions of functionalities that are common between its various embodiments. *See, e.g., Ohi* (Ex. 1003), 12:19-25 (“In [Fig. 12], because the same reference numerals as shown in FIG. 6 denote the same components as those of the second embodiment or like components, the explanation of those components will be omitted hereafter.”), 12:59-61 (noting “the drive circuit operates in the same way [as] that of embodiment 2 [], and therefore the description of the operation will be omitted hereafter”). Throughout the proposed ground, Petitioner has cited the applicable description of the Fig. 12 circuit and its operation. Some of those descriptions are contained within discussions of earlier embodiments, including the second embodiment as depicted in Fig. 6. That Figs. 6 and 12 shared certain components and functionality does not change the fact that the proposed ground herein is based on *Ohi*’s fifth embodiment as depicted in Fig. 12 and does not ask the Board to reconsider the Fig. 6 circuit that was discussed during prosecution.

instruction: (1) Delay circuit 31 in sampler 16 that generates a *first pulse signal* that defines the “detection time period during which the gate voltage V_g of an IGBT is detected[,]” (2) comparator 38 that output a *second pulse signal* when gate voltage V_g of the IGBT exceeds a threshold voltage, and (3) AND circuit 44 that receives the first and second pulse signals and outputs a High signal when V_g exceeds the threshold during the detection time period. *Id.* at 12:32-58.



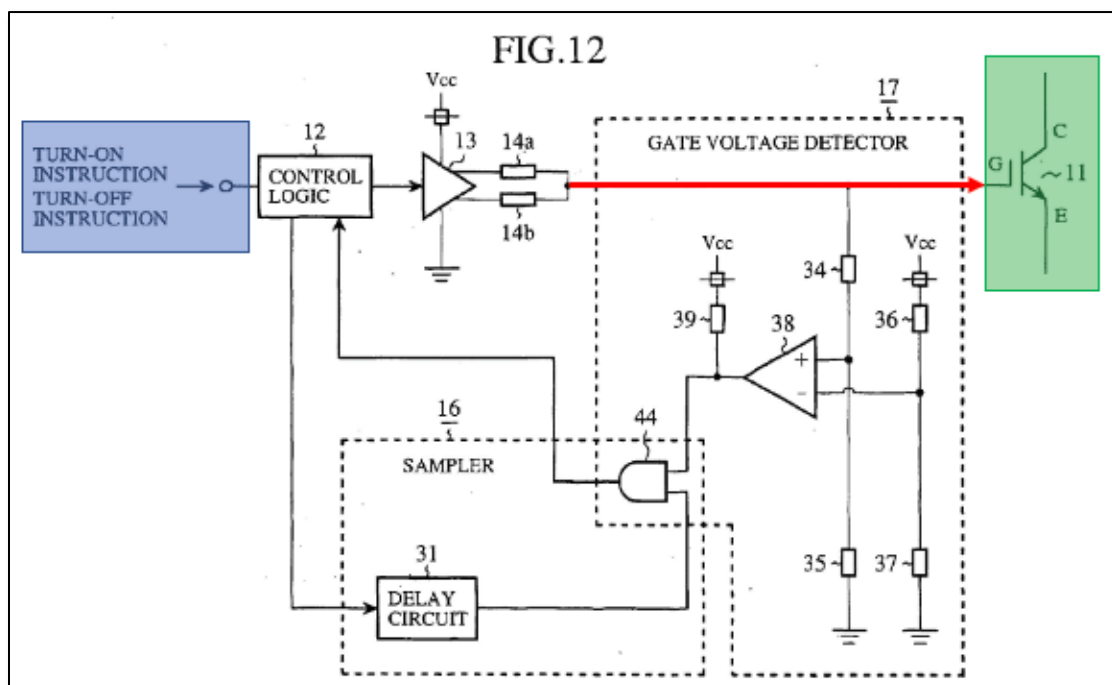
Id. at Fig. 12 (annotated). When a short circuit condition is encountered, **logical circuit 44** generates a stop signal that causes IGBT to be turned off. *Id.* at 12:53-60 (“[W]hen a short circuit occurs in the IGBT 11, the output-signal of the AND circuit 44 becomes a High level (i.e., a logical level indicating a detection of the occurrence of an abnormality in the IGBT . . . [.] After that, the drive circuit operates in the same way that that of embodiment 2 does[.]”), 10:14-21 (describing embodiment 2,

teaching that the circuit “delivers an abnormality signal to the control logic 12[, and, a]s a result, the control logic 12 causes the IGBT 11 to become turned-off[.]”).

i. Claim 1

[1(P)] A semiconductor device controlling a drive of an insulated gate transistor by generating a control output signal on a basis of a control input signal, comprising:

To the extent the preamble is limiting, *Ohi* teaches it. Namely, *Ohi* discloses a semiconductor device that controls the drive of an insulated gate transistor (i.e., an IGBT) by generating a control output signal on a basis of a control input signal. The following annotated Fig. 12 from *Ohi* illustrates a semiconductor circuit that receives **turn-on and turn-off instructions** (control input signal) and uses those instructions to generate a **gate instruction** (control output signal) for turning on and off an **insulated gate bipolar transistor** (IGBT):



Ohi (Ex. 1003), Fig. 12 (annotated). As depicted above, control logic 12 is configured “for sending a **gate instruction** to turn on the **IGBT 11** to a buffer 13 in response to a **turn-on instruction** from outside the drive circuit, and for sending a **gate instruction** to turn off the **IGBT 11 to the buffer 13** in response to a **turn-off instruction** from outside the drive circuit.” *Id.* at 4:45-50.

Ohi’s embodiments are directed to drive circuits for driving power semiconductor devices such as an IGBT and detecting short circuits in such semiconductor devices:

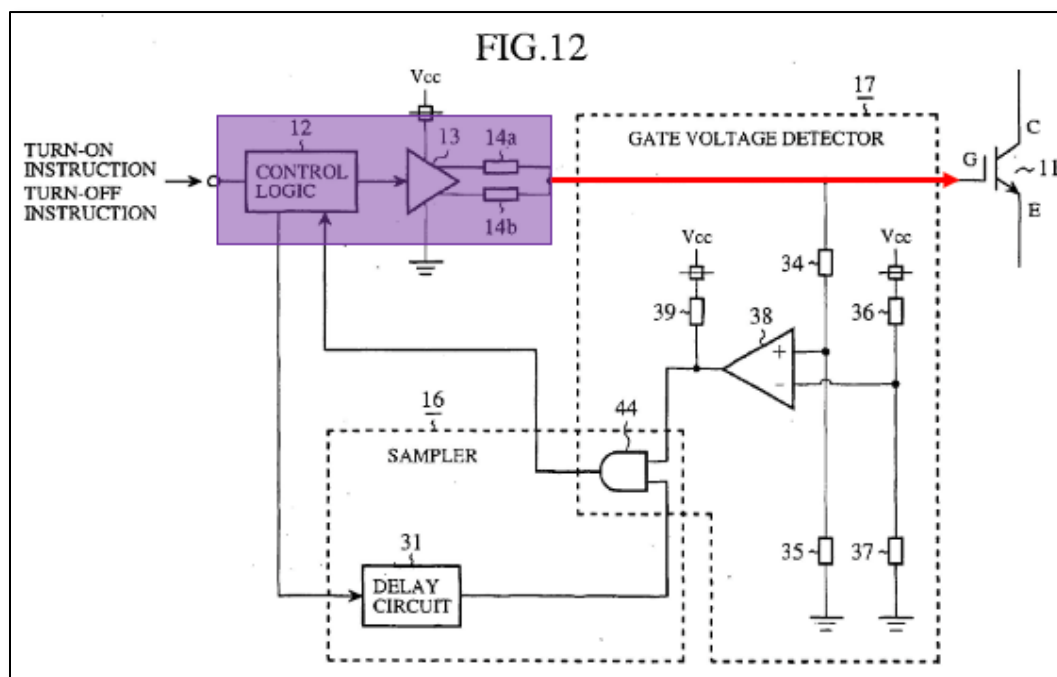
The present invention is proposed to solve the above-mentioned problems, and it is therefore an object of the present invention to provide a high-reliability **drive circuit for driving a power semiconductor device, capable of promptly detecting occurrence of a short circuit** so as to protect the power semiconductor device **even when applied to a high-voltage IGBT**.

Id. at 2:35-41 (emphases added). Although *Ohi* does not expressly describe the drive circuit as a semiconductor device, a POSITA would have understood that *Ohi*’s drive circuit is a semiconductor device that drives a power semiconductor IGBT. *Dec.* (Ex. 1004), ¶¶ 40-42 (explaining that *Ohi*’s drive circuit receives a simple on/off input instruction, drives a semiconductor IGBT, and is composed of standard logic components, and concluding that a POSITA would have understood the structure and function of this drive circuit would have been implemented as a semiconductor

device). Indeed, during prosecution, the Applicant did not take issue with the Examiner's characterization of *Ohi*'s drive circuit as a "semiconductor device." '835 *Patent File History* (Ex. 1002), 200-201 (office action discussing *Ohi*), 224-226 (office action response).

[1(a)] a driver outputting said control output signal and

As set forth above with reference to [1(pre)], Fig. 12 includes control logic 12 configured "for sending a gate instruction to turn on the IGBT 11 to a buffer 13 in response to a turn-on instruction from outside the drive circuit, and for sending a gate instruction to turn off the IGBT 11 to the buffer 13 in response to a turn-off instruction from outside the drive circuit." *Ohi* (Ex. 1003), 4:45-50. As annotated below in Fig. 12, control logic 12, buffer 13, and gate resistors 14a and 14b comprise a driver for outputting the control output signal:



Id. at Fig. 12 (annotated). Indeed, *Ohi* explains that the role of buffer 13 is to *amplify* the gate instruction generated by control logic 12 in response to control logic 12 receiving a turn-on (or turn-off) instruction from outside the circuit:

In response to a turn-on instruction from outside the drive circuit, the **control logic 12 delivers a gate instruction to cause the IGBT 11 become turned-on to the buffer 13**. When receiving the gate instruction to cause the IGBT 1 to become turned-on from the control logic 12, the **buffer 13 amplifies the gate instruction** and delivers the amplified gate instruction to the gate of the IGBT 11 by way of the on-state gate resistor 14a. As a result, the IGBT 11 becomes turned-on.

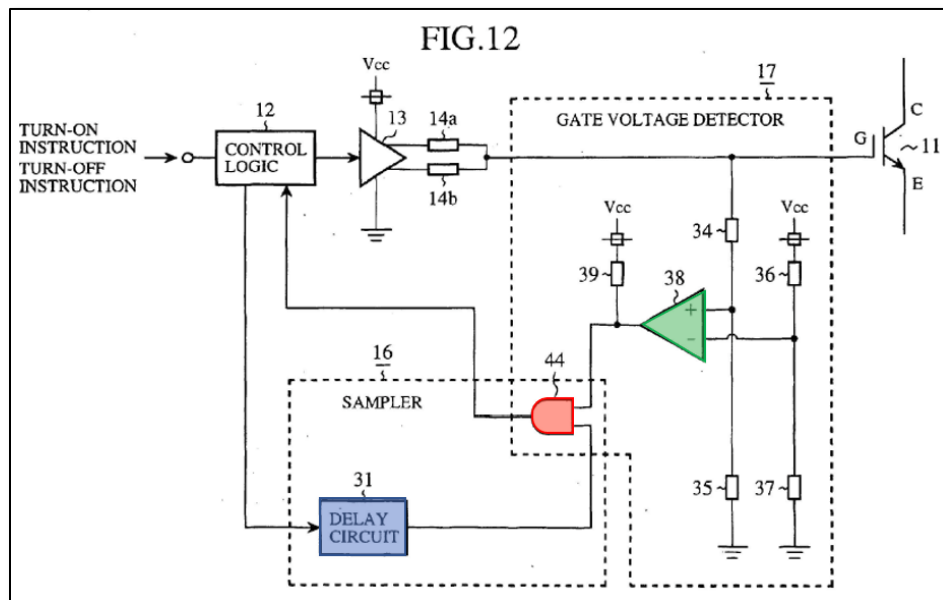
Id. at 7:1-9 (emphasis added); *see also id.* at 7:10-19 (similar description with respect to turning off the IGBT). Given that control logic 12, buffer 13, and the gate resistors work in concert to produce a control output signal that is a function of the control input signal, a POSITA would understand that this group of components satisfies the claimed driver outputting a control output signal. *Dec.* (Ex. 1004), ¶¶ 43-44.

[1(b)] a short-circuit protection circuit detecting said control output signal and controlling and forcing said driver to stop said control output signal when a detecting voltage of said control output signal exceeds a predetermined reference voltage before a predetermined period passes after said control output signal indicates a conduction of said insulated gate transistor,

As discussed above in the overview of *Ohi*, the fifth embodiment, as depicted in Fig. 12 below, utilizes three key components to detect a short circuit abnormality immediately following a turn-on instruction: (1) **sampler 16** (including **delay circuit 31** in the Fig. 12 embodiment) that generates a *first pulse signal* that defines the

“detection time period during which the gate voltage V_g of an IGBT is detected[.]”

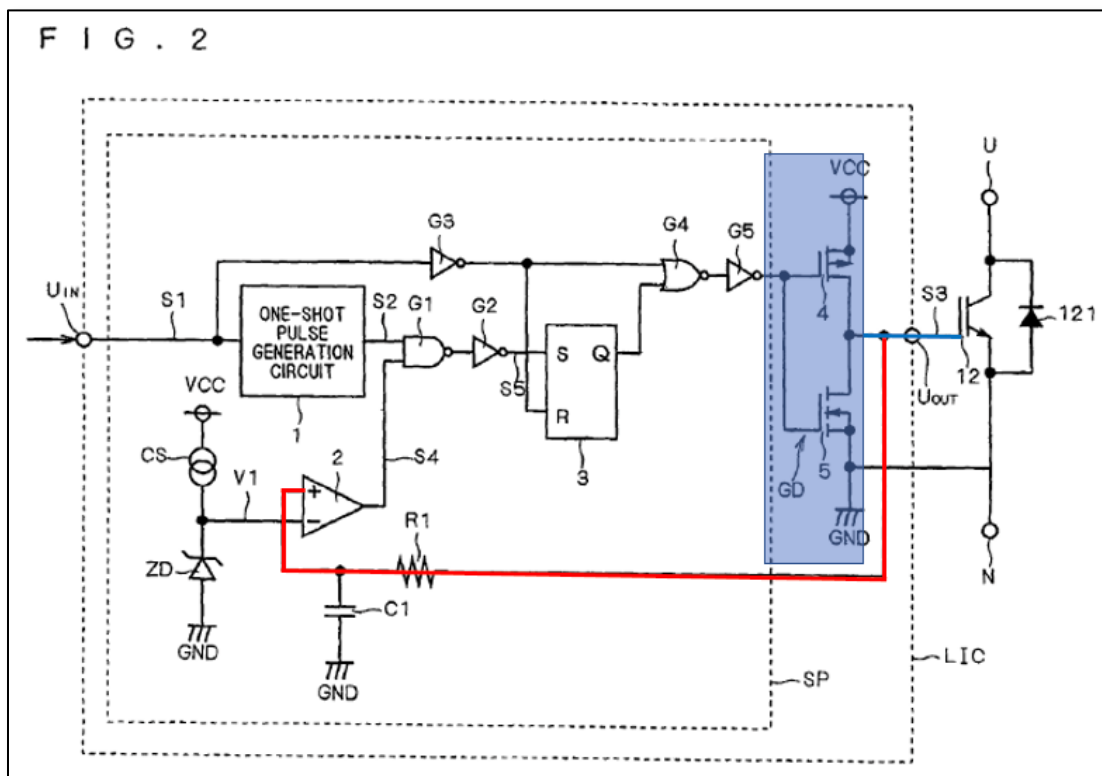
(2) **comparator 38** that outputs a *second pulse signal* when gate voltage V_g of the IGBT exceeds a threshold voltage, and (3) **AND circuit 44** that receives the first and second pulse signals and outputs a High signal when V_g exceeds the threshold during the detection time period. *Id.* at 12:32-58.



Id. at Fig. 12 (annotated). When a short circuit condition is encountered, **logical circuit 44** generates a stop signal that causes IGBT to be turned off. *Id.* at 12:53-60 (“[W]hen a short circuit occurs in the IGBT 11, the output-signal of the AND circuit 44 becomes a High level (i.e., a logical level indicating a detection of the occurrence of an abnormality in the IGBT . . . [.] After that, the drive circuit operates in the same way that that of embodiment 2 does[.]”), 10:14-21 (describing embodiment 2,

teaching that the circuit “delivers an abnormality signal to the control logic 12[, and, a]s a result, the control logic 12 causes the IGBT 11 to become turned-off[.]”).

This limitation recites a “detecting voltage of said control output signal[.]” Although somewhat confusing language, a POSITA would understand this is satisfied by detecting/measuring the gate voltage of the IGBT. *Dec.* (Ex. 1004), ¶ 46 (explaining that the '835 Patent teaches a control output signal that drives the IGBT gate and concluding that the detecting voltage of control output signal is the measured gate voltage). Indeed, as illustrated in Fig. 2, the '835 Patent equates measuring the gate voltage with a *detecting voltage of control output signal*:



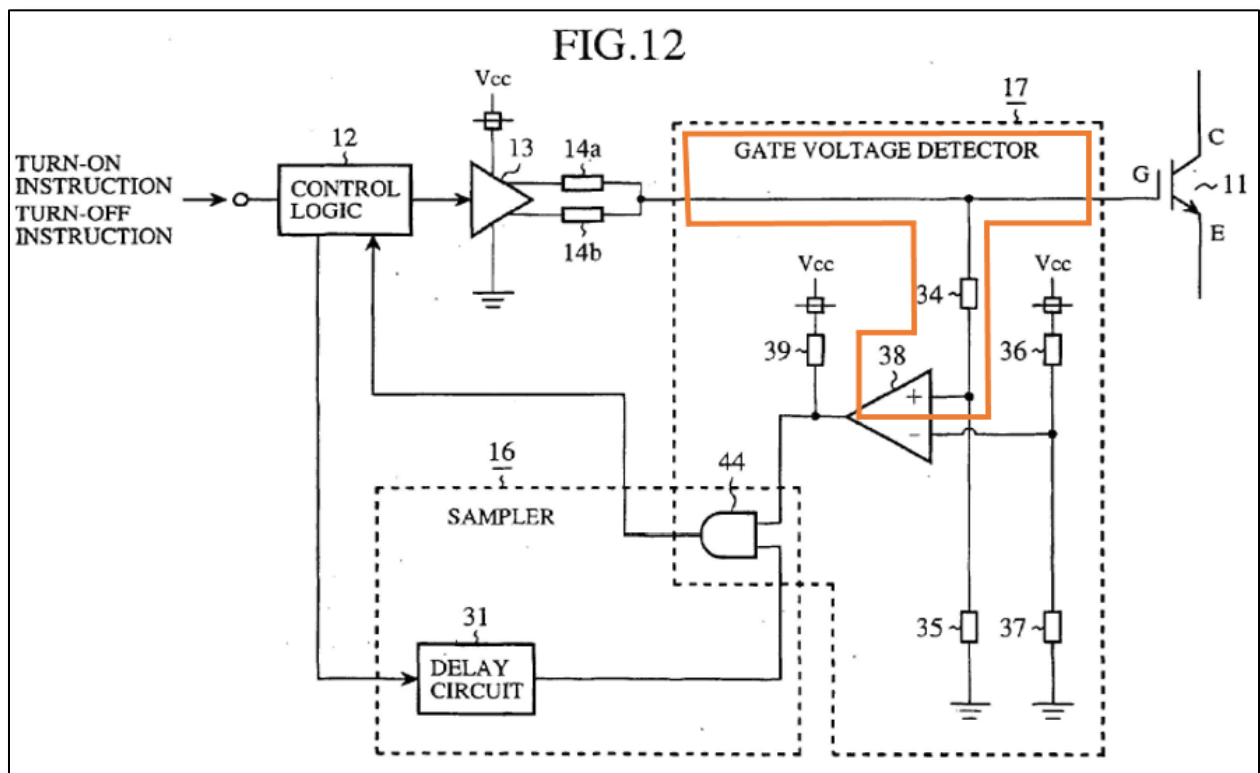
'835 Patent (Ex. 1001), Fig. 2 (annotated), 4:27-35 (“**gate driver GD . . . supply[s] a control output signal S3** to the gate electrode of the transistor 12, and it is **inputted to . . . comparator 2 as a detecting voltage of the control output signal S3**”). Similarly, with reference to Fig. 6, the '835 Patent equates a divided-down gate voltage with the *detecting voltage of control output signal*. *Id.* at 7:54-63 (describing the IGBT gate voltage S13 and noting “the control output signal S13 is resistively **divided between a resistance R11 and a resistance R12 and is inputted to a + (plus) side input terminal of a comparator 13 as a detecting voltage of the control output signal S13[.]**”). Accordingly, a POSITA would understand that a “detecting voltage of said control output signal” is a measured gate voltage or a divided down representation of the measured gate voltage. *Dec.* (Ex. 1004), ¶¶ 46-47 (noting that resistively dividing down voltage measurements is a well understood means of producing a smaller, but representative measurement of a given node).

Ohi teaches this precise arrangement. Namely, the drive circuit in *Ohi* includes a gate voltage detector 17 that provides a divided down representation of the gate terminal of IGBT 11 to comparator 38:

The comparator 38 of a gate voltage detector 17 compares a **divided voltage obtained from the gate voltage V_g of the IGBT** with a divided voltage obtained from the control voltage V_{cc} of the IGBT, like that of above-mentioned embodiment 2, and, when the gate voltage V_g

reaches the control voltage V_{cc} in level, causes its output signal to make a transition from a Low level to a High level (see Fig. 13).

Ohi (Ex. 1003), 12:37-44 (emphasis added); *see also id.* at 5:4-9 (gate voltage detector 17 “detects the gate voltage V_g that appears at the gate terminal of the IGBT 11, as the controllable variable value that is applied to the IGBT 11 and is controlled by the buffer 13”). As discussed above with reference to limitation [1(a)], the output of buffer 13 satisfies the claimed *control output signal*. Accordingly, the claimed *detecting voltage of said control output signal* is a divided down gate voltage of IGBT 11, which is performed by gate voltage detector 17 in *Ohi*’s Fig. 12. *Dec.* (Ex. 1004), ¶ 48. This arrangement is annotated in Fig. 12 below:



Ohi (Ex. 1003), Fig. 12 (annotated).

In sum, *Ohi's* Fig. 12 circuit includes *a short-circuit protection circuit* that detects the gate voltage of IGBT 11, compares it to a threshold value during a predetermined period after turning on IGBT 11, causes the control output signal to turn off IGBT 11 if the gate voltage exceeds the threshold within that predetermined period. This process is addressed in greater detail below with respect to limitations [1(c)]-[1(e)]. All evidence and arguments discussed below are hereby incorporated by reference.

[1(c)] said short-circuit protection circuit includes: pulse generation circuit receiving said control input signal and outputting a first pulse signal being significant only in said predetermined period according to a timing when said control input signal indicates the conduction of said insulated gate transistor;

Ohi teaches sampler 16⁴ (*pulse generation circuit*) that receives the turn-on instruction from outside the circuit (*receiving said control input signal*) and outputs

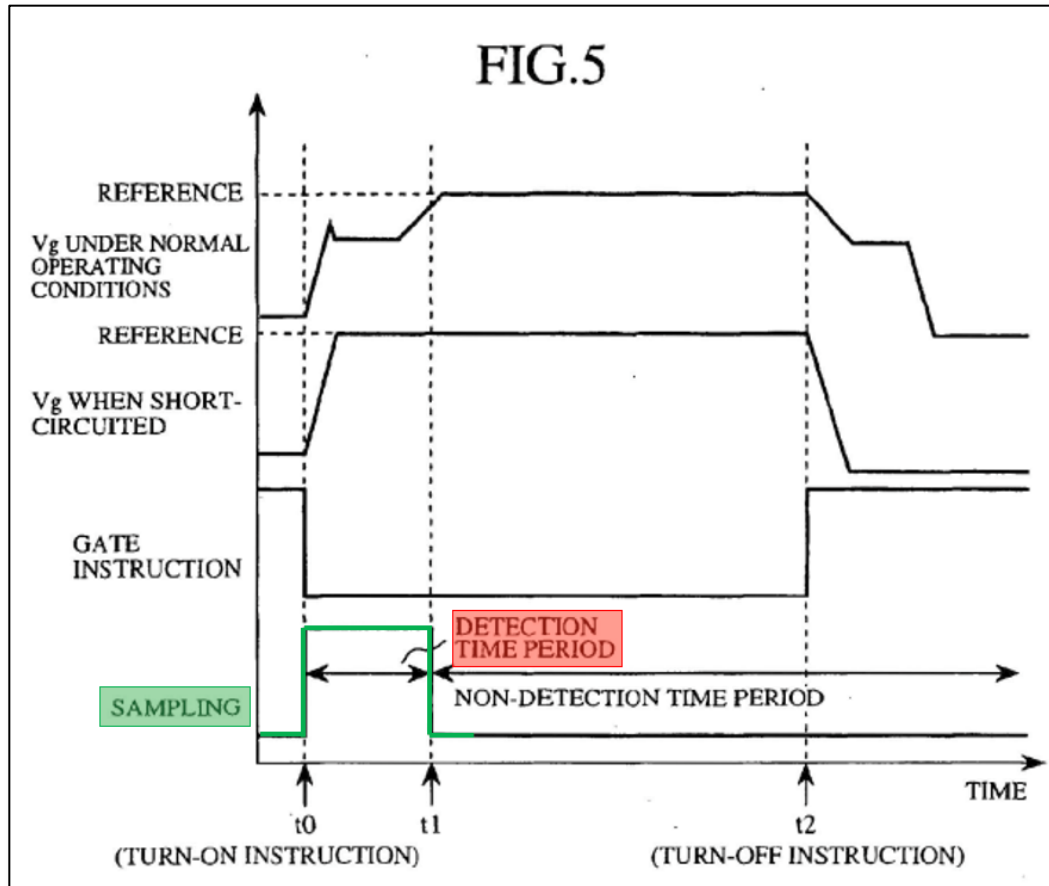
⁴ Specifically, the claimed pulse generation circuit is satisfied by the circuitry in sampler 16 that generates a signal that is input into the AND gate 44. For example, Fig. 12 depicts a delay circuit 31 that performs this functionality. As discussed below, *Ohi* also teaches an embodiment of sampler 16 that includes a delay circuit 31, a delay circuit 41, and an inverter. Although a dotted line in Fig. 12 suggests AND gate 44 is part of sampler 16, Petitioner does not contend that AND gate 44

a level High pulse that defines the period after the IGBT is turned on during which the gate voltage is measured to detect a short-circuit condition (*outputting a first pulse signal being significant only in said predetermined period according to a timing when said control input signal indicates the conduction of said insulated gate transistor*):

[T]he drive circuit includes the **sampler 16 for allowing the process of detecting the gate voltage V_g** that appears at the gate terminal of the IGBT 11 **only during a transition time period** before the gate voltage V_g reaches the on-state gate voltage immediately **after the control logic 12 has received a turn-on instruction** from outside the drive circuit, and the gate voltage detector 17 that detects the gate voltage V_g that appears at the gate terminal of the IGBT 11 throughout a detection time period during which the sampler 16 allows the process of detecting the gate voltage V_g , and that recognizes the occurrence of an abnormality in the IGBT 11 when the gate voltage V_g exceeds a reference value.

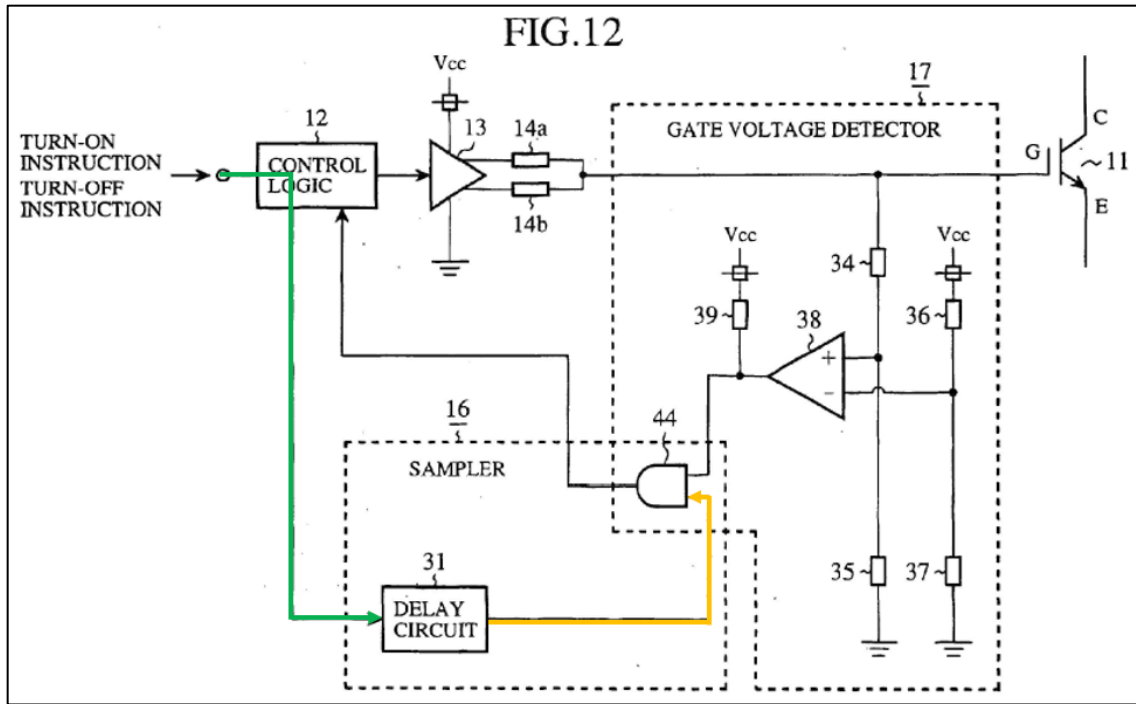
Ohi (Ex. 1003), 8:17-29 (emphasis added). Fig. 5 illustrates an exemplary **pulse generated by sampler 16** that is High (i.e., significant) only when the gate voltage is to be measured (i.e., from t_0 to t_1 , following a gate instruction turning on IGBT):

satisfies the claimed pulse generation circuit. Instead, the proposed ground is clear that AND gate 44 satisfies the claimed “logical circuit.”

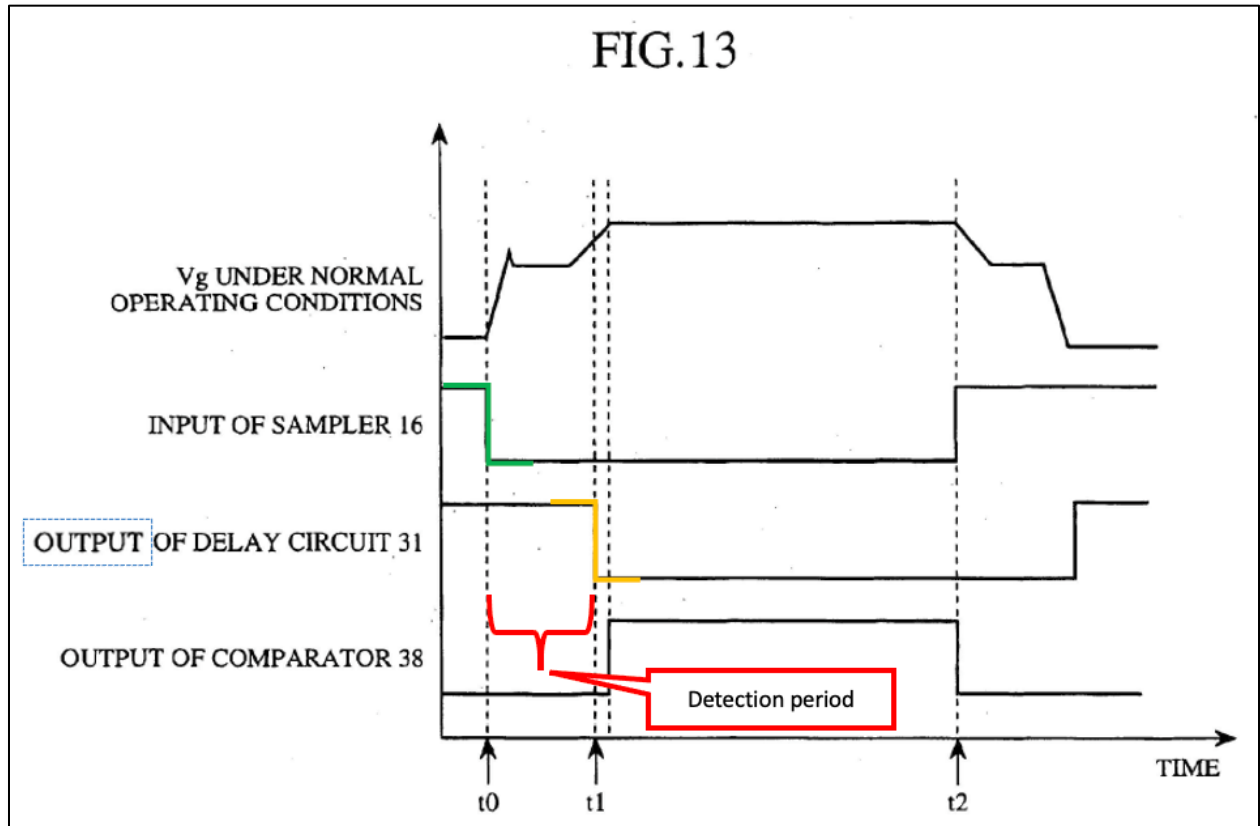


Id. at Fig. 5 (annotated).

For the fifth embodiment, specifically, on which the proposed ground is based, *Ohi* teaches two distinct implementations of sampler 16. In a first example, as depicted in Fig. 12, delay circuit 31 receives a **turn-on instruction** from control logic 12 (in the form of a falling edge signal, i.e., a transition from high to low). *Id.* at 12:29-44. Delay circuit 31 **outputs** that falling edge signal after a predetermined amount of time has elapsed after the turn-on instruction is received, ensuring that its output remains significant only for that predetermined time after the IGBT is turned on. *Id.*



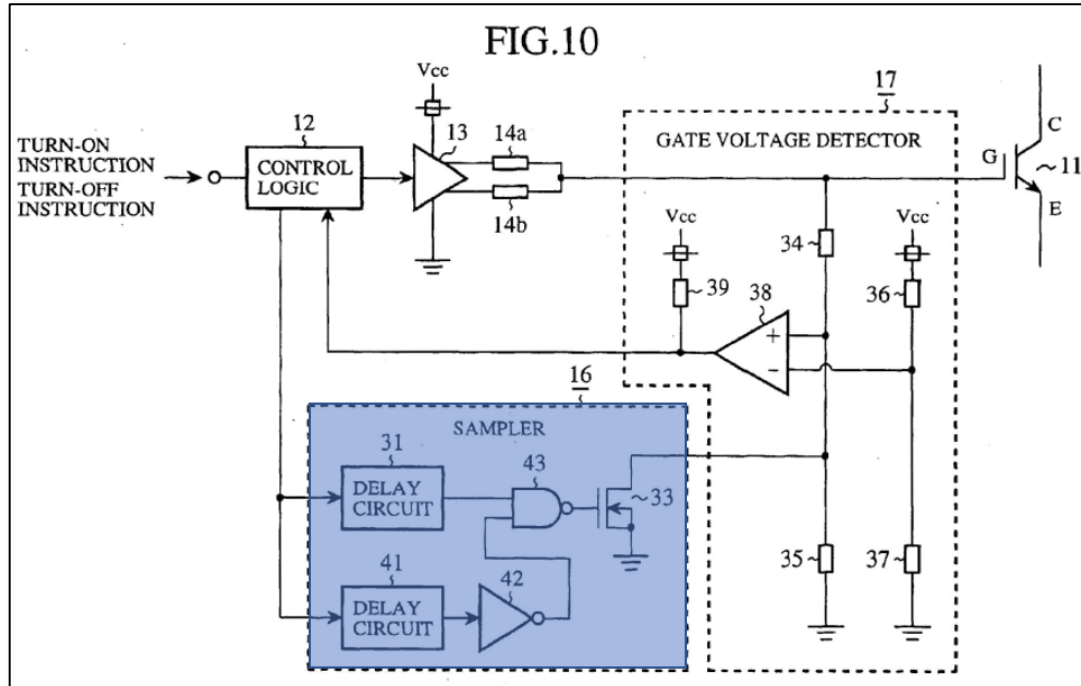
Id. at Fig. 12 (annotated). As illustrated in Fig. 13 below, a **detection time period** begins at time t_0 (when IGBT is turned on and sampler 16 receives the **turn-on instruction**) and ends at t_1 (when the **output of delay circuit 31 transitions from high to low** in accordance with a preset delay time):



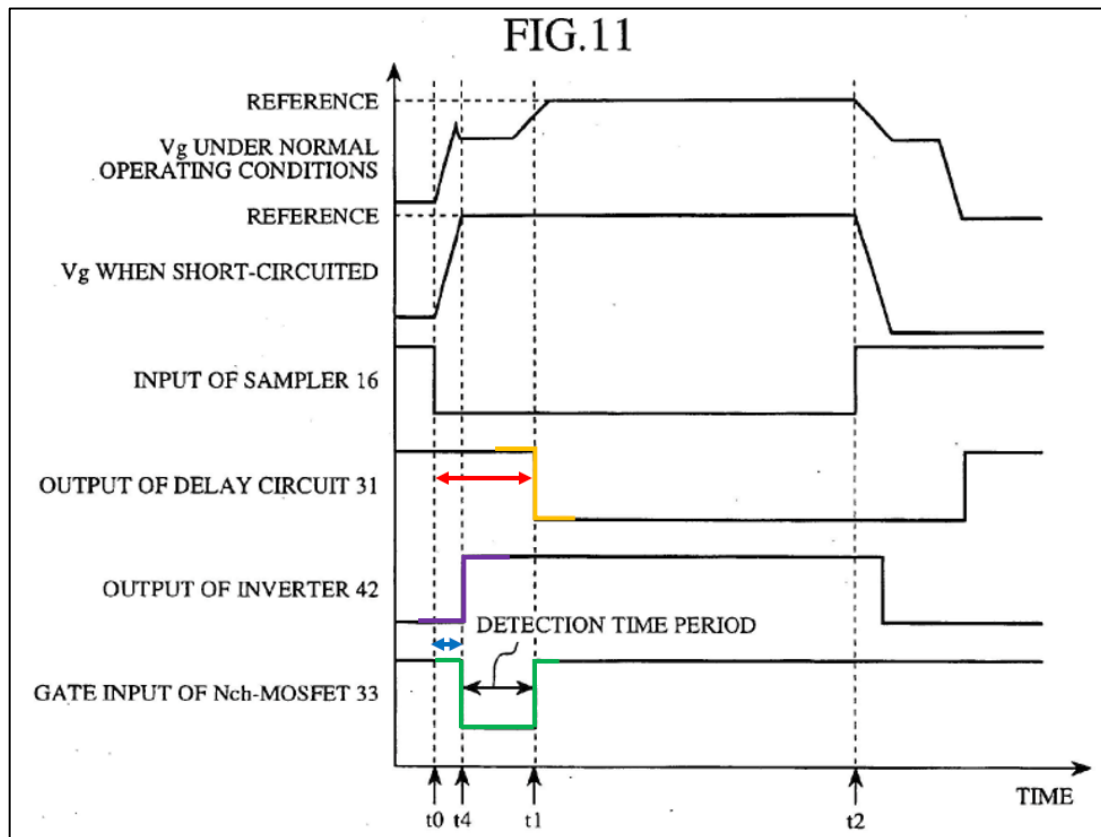
Id. at Fig. 13,⁵ 12:31-36 (“The delay circuit 31 of a sampler 16 has a preset delay time with which the level of its output signal makes a transition from a High level to a Low level at a time t1 when a detection time period during which the gate voltage Vg of an IGBT is detected is ended[.]”).

⁵ Fig. 13 contains a typo. The second from the bottom signal is labeled “input of delay circuit 31” in *Ohi*, but a POSITA would recognize that the illustrated signal is in fact the output of delay circuit 31. *Dec.* (Ex. 1004), ¶ 51, fn3. Petitioner has corrected the language herein, identifying the correction with a blue dashed box.

Ohi teaches a second implementation of sampler 16 that is expressly proposed as an alternative for its fifth embodiment. Described in detail with reference to *Ohi*'s embodiment four, this second implementation uses two delay circuits to define a “detection time period during which the gate voltage V_g is detected [that] excludes a certain time period (e.g., the time period from the time t_0 to the time t_4) immediately after the IGBT 11 is turned on.” *Id.* at 11:36-40. *Ohi* explains that waiting until t_4 to begin gate voltage detection ensures the gate voltage measurement excludes a “recovery time” immediately after the IGBT is turned on. *Id.* at 11:48-57. The two-delay circuit structure is depicted in Fig. 10 below, and the $t_4 \rightarrow t_1$ detection period generated by this structure is illustrated in Fig. 11 below:



Id. at Fig. 10 (annotated). As depicted in Fig. 11 below, delay circuit 31 is configured to delay the falling edge turn-on signal by the **preset delay time t_0 to t_1** . In other words, it imposes the same delay as sampler 16 in Fig. 12, defining the **end of the detection time period**. Delay circuit 41 and inverter 42 are used to define the **start of the detection time period** by delaying (and inverting) the turn-on signal for a **preset delay time t_0 to t_4** . The result of this two-delay sampler 16 is a **pulse**, similar to the pulse depicted in Fig. 5, that is significant only when the gate voltage is to be measured (i.e., from t_4 to t_1 , following a gate instruction turning on IGBT):



Id. at Fig. 11 (annotated). As shown in Fig. 11, the pulse generated by sampler 16 is inverted such that it is Low during the detection time period.

Ohi expressly proposes using the fourth embodiment sampler in its fifth embodiment

Ohi teaches that its fourth embodiment (Figs. 10-11) process for excluding recovery time from the detection period can be used in the fifth embodiment (Figs. 12-13):

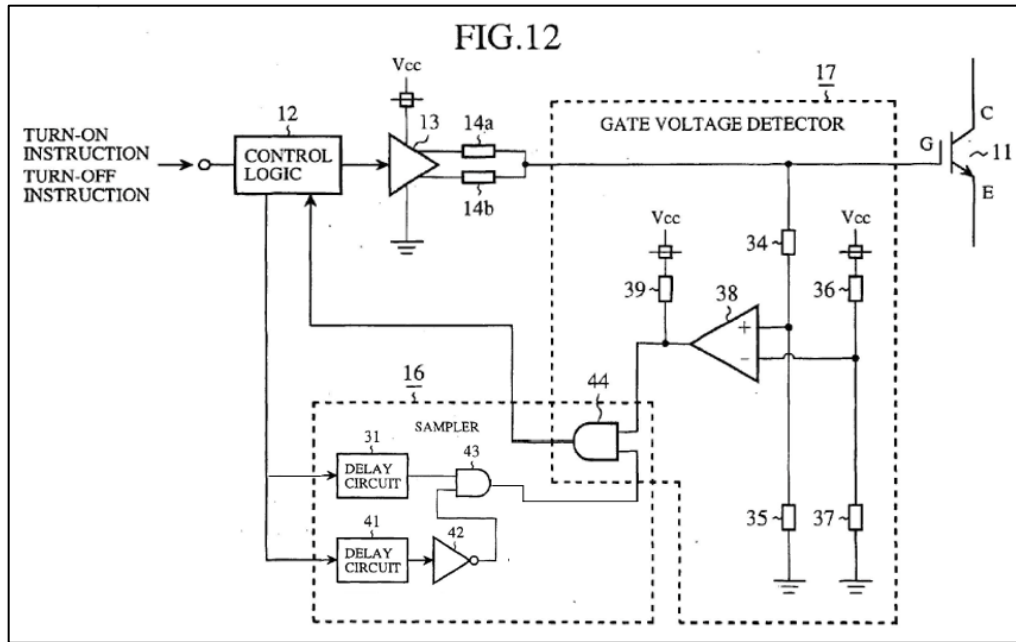
The detection time period during which the gate voltage V_g is detected can exclude a recovery time period immediately after the IGBT is turned on, like that of above-mentioned embodiment 4.

Id. at 12:66-13:2 (emphasis added). A POSITA would have understood that incorporating the fourth embodiment's recovery time exclusion into the fifth embodiment's circuit is a straightforward replacement of the fifth embodiment's single delay circuit with the fourth embodiment's two delay circuit structure that defines both a start and end of the detection time period.⁶ *Dec.* (Ex. 1004), ¶¶ 52-56

⁶ The Federal Circuit has repeatedly held that anticipation grounds may properly rely on teachings from different embodiments within a single reference, particularly where the reference contemplates combining teachings from separate embodiments. *Kennametal, Inc. v. Ingersoll Cutting Tool Co.*, 780 F.3d 1376, 1381 (Fed. Cir. 2015) (“[A] reference can anticipate a claim even if it ‘d[oes] not expressly spell out’ all the limitations arranged or combined as in the claim, if a person of skill in the art, reading the reference, would ‘at once envisage’ the claimed arrangement or

(explaining that the fourth embodiment's delay circuit 31, delay circuit 41, inverter 42, and NAND gate 43 generate an inverted pulse as depicted in Fig. 11). A POSITA would further have understood that, because the Fig. 12 sampler outputs a High signal during the detection time period, the fourth embodiment's NAND gate 43 would be replaced with an AND gate. *Id.* (explaining that the resulting pulse from said AND gate is High only during the desired measurement period, which is the inverse of the fourth embodiment's NAND gate 43, which produces a pulse that is Low only during the desired measurement period). The result of implementing the fourth embodiment's sampler in the fifth embodiment, as *Ohi* expressly contemplates, is depicted below:

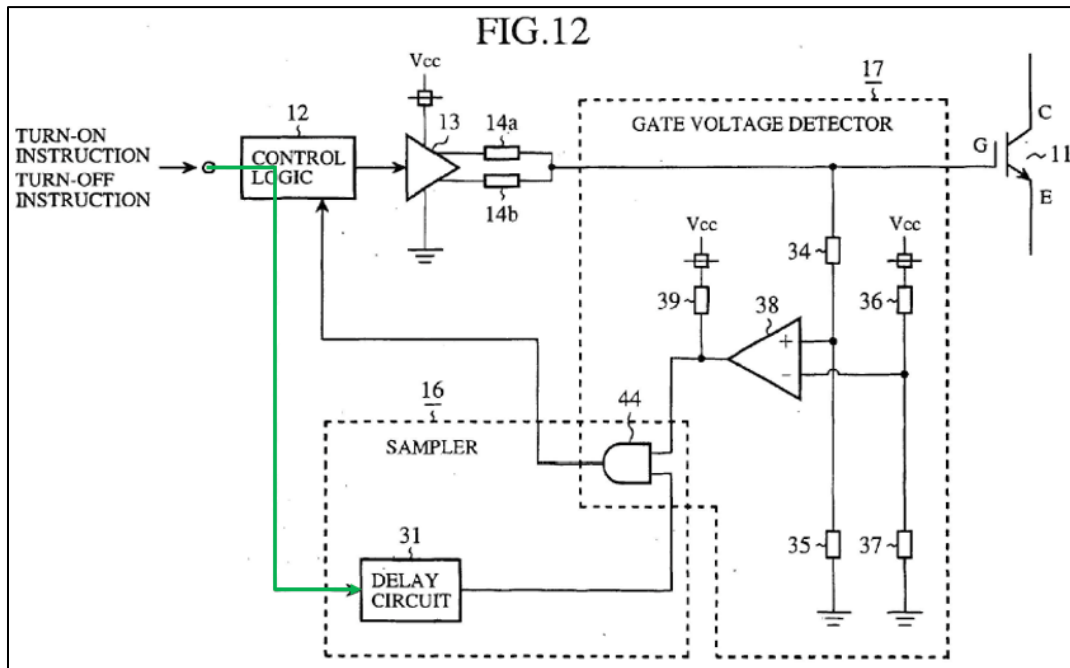
combination.”) (quoting *In re Petering*, 49 CCPA 993, 301 F.2d 676, 681 (1962)); *Hayward Indus., Inc. v. Pentair Water Pool & Spa, Inc.*, 814 F. App'x 592, 597 (Fed. Cir. 2020) (concluding that the Discenzo reference anticipates and noting that, “[a]lthough Discenzo teaches optimization and the arrangement of components in different embodiments of the patent, Discenzo also explains that these features may be combined.”). Here, as in *Hayward*, *Ohi* expressly teaches that the fourth embodiment's recovery time exclusion approach may be employed in the fifth embodiment. Accordingly, this combination of *Ohi*'s teachings anticipates the claimed pulse generation circuit.



Ohi (Ex. 1003), Fig. 12 (modified to implement the fourth embodiment's sampler 16, which produces a pulse that excludes recovery time from the detection time period); Dec. (Ex. 1004), ¶¶ 52-56 (explaining that this depicted modification of Fig. 12 is the result of implementing Ohi's express teaching that the fifth embodiment's Fig. 12 circuit could exclude recovery time as expressly discussed in the fourth embodiment). A POSITA would have understood that the modified Fig. 12 sample depicted above outputs a High pulse that defines the detection time period and that is significant *only* during the detection time period following an instruction to turn on the IGBT (*significant only in said predetermined period according to a timing when said control input signal indicates the conduction of said insulated gate transistor*). Dec. (Ex. 1004), ¶ 56 (concluding that sampler 16 in the modified Fig. 12 circuit satisfies the claimed first pulse signal).

Ohi's sampler 16 in Fig. 12 receives the turn-on instruction, as claimed

As discussed above and as depicted in Fig. 12 below, *Ohi's* sampler 16 (*pulse generation circuit*) receives the turn-on instruction from outside the circuit (*receiving said control input signal*):

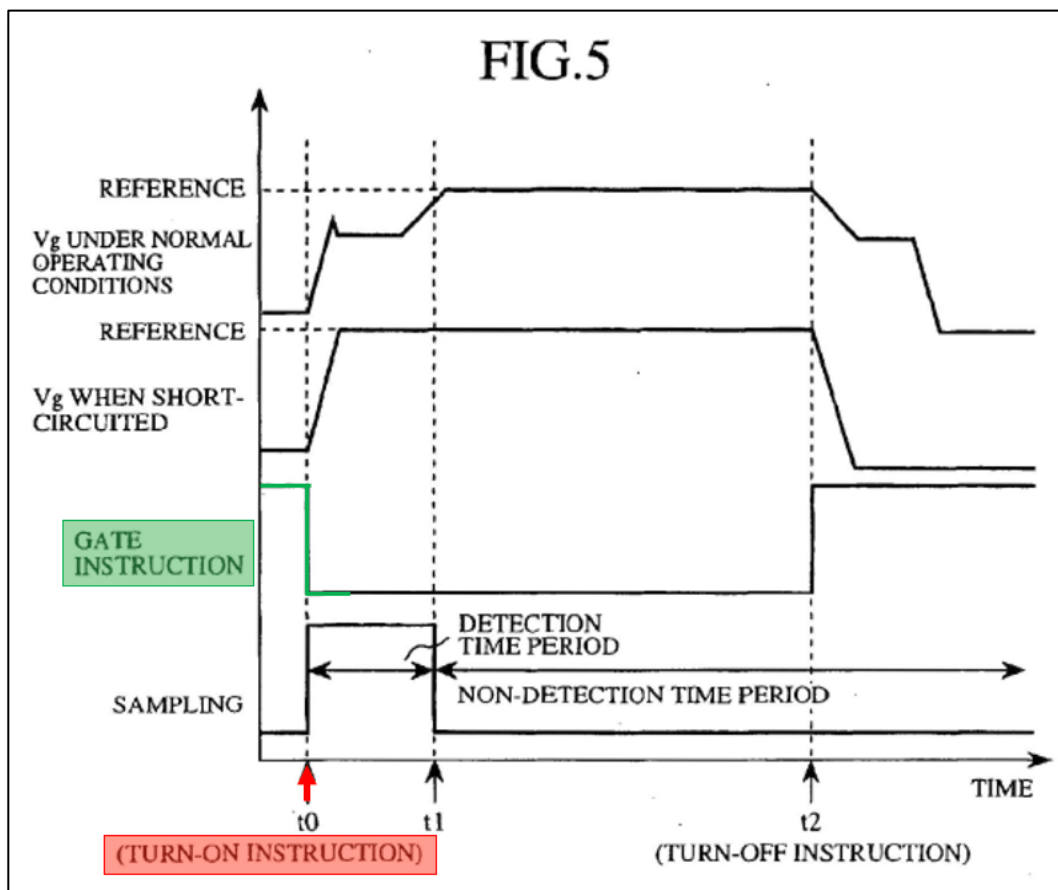


Ohi (Ex. 1003), Fig. 12 (annotated). Although *Ohi* does not illustrate the turn-on instruction received by control logic 12, for a number of reasons set forth below, a POSITA would have understood (1) that this external signal is simply state change (e.g., a voltage transitioning from High to Low or Low to High) and (2) that the state change is received by sampler 16, as claimed.

Ohi explains that control logic 12 outputs a “gate instruction” in response to receiving the turn-on or turn-off instructions:

In response to a turn-on instruction from outside the drive circuit, the control logic 12 delivers a gate instruction to cause the IGBT 11 become turned-on to the buffer 13. . . . On the other hand, in response to a turn-off instruction from outside the drive circuit, the control logic 12 delivers a gate instruction to cause the IGBT 11 to become turned-off to the buffer 13.

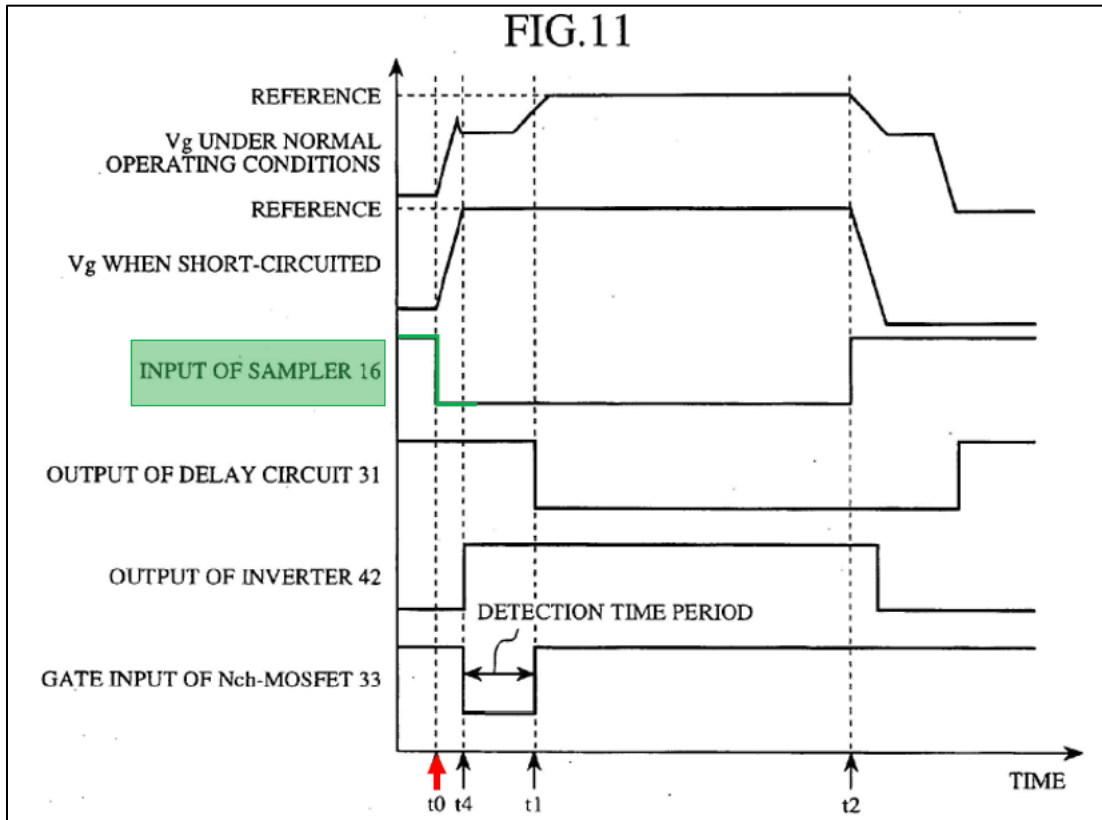
Ohi (Ex. 1003), 7:1-13. In Fig. 5 below, the **gate instruction** is depicted as a falling edge (i.e., High to Low) state change that occurs when the **turn-on instruction** is received, t_0 :



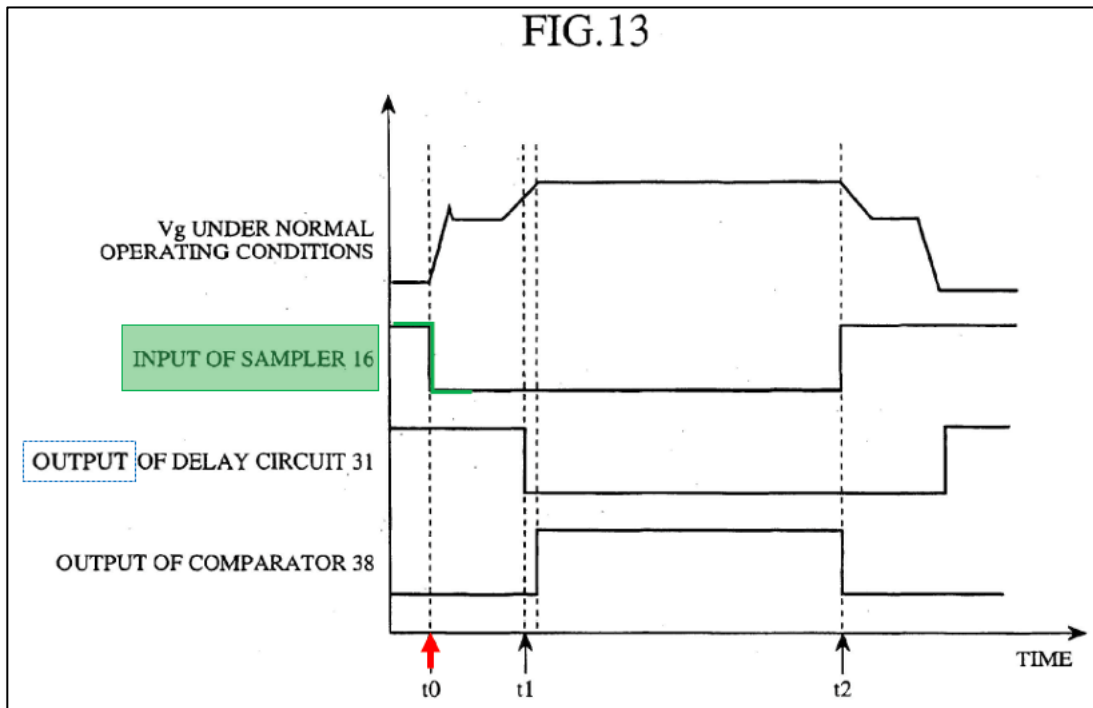
Id. at Fig. 5 (annotated). *Ohi* further explains that, as illustrated in Fig. 5 above, when the turn-on instruction is input into control logic 12, sampler 16 receives this signal and enables a detection time period during which the IGBT gate voltage is measured:

[W]hen the control logic 12 receives a turn-on instruction from outside the drive circuit, as shown in FIG. 5, the sampler 16 enables the gate voltage detector 17 to detect the gate voltage V_g at the time t_0 when the turn-on instruction is received. After that, when a certain time elapses and a time t_1 (before the gate voltage V_g reaches the on-state gate voltage, and the time t_1 is determined in consideration of the characteristics of the IGBT 11) comes, the sampler 16 disables the gate voltage detector 17 to detect the gate voltage V_g .

Id. at 7:32-41 (emphasis added). As depicted in both Figs. 11 and 13 below, sampler 16 receives the same falling edge signal that is depicted in Fig. 5 as the “gate instruction” that results from receiving a turn-on instruction from outside the drive circuit at time t_0 :



Id. at Fig. 11 (annotated).



Id. at Fig. 13 (annotated).

Dr. Liu explains that, based on the above disclosures and illustrations, a POSITA would have understood that sampler 16 (*pulse generation circuit*) receives the turn-on instruction from outside the circuit (*receiving said control input signal*), as claimed. First, although not illustrated in any of *Ohi*'s timing diagrams, a POSITA would have understood that the turn-on instruction is simply a state change (e.g., a voltage transitioning from High-to-Low or Low-to-High) received by logic circuit 12. *Dec.* (Ex. 1004), ¶¶ 58-60 (explaining that the drive circuit described by *Ohi* operates using standard High/Low logic signals and concluding that a POSITA would have understood the turn-on instruction is similarly a signal that transitions from High-to-Low or vice versa).

Second, a POSITA would have understood that sampler 16 receives this signal (i.e., the state change when a turn-on instruction is received at t_0). *Id.* at ¶ 61 (explaining that control logic 12 transmits the turn-on instruction signal as a High-to-Low state change at the precise moment, t_0 , the turn-on instruction is received from outside the circuit). Indeed, as illustrated in Figs. 11 and 13 above, the input of sampler 16 transitions from High-to-Low at t_0 —the moment a turn-on instruction is received. *Id.*

Finally, *Ohi* does not teach or suggest that the turn-on instruction received by control logic 12 at time t_0 is modified in any way prior to being transmitted to

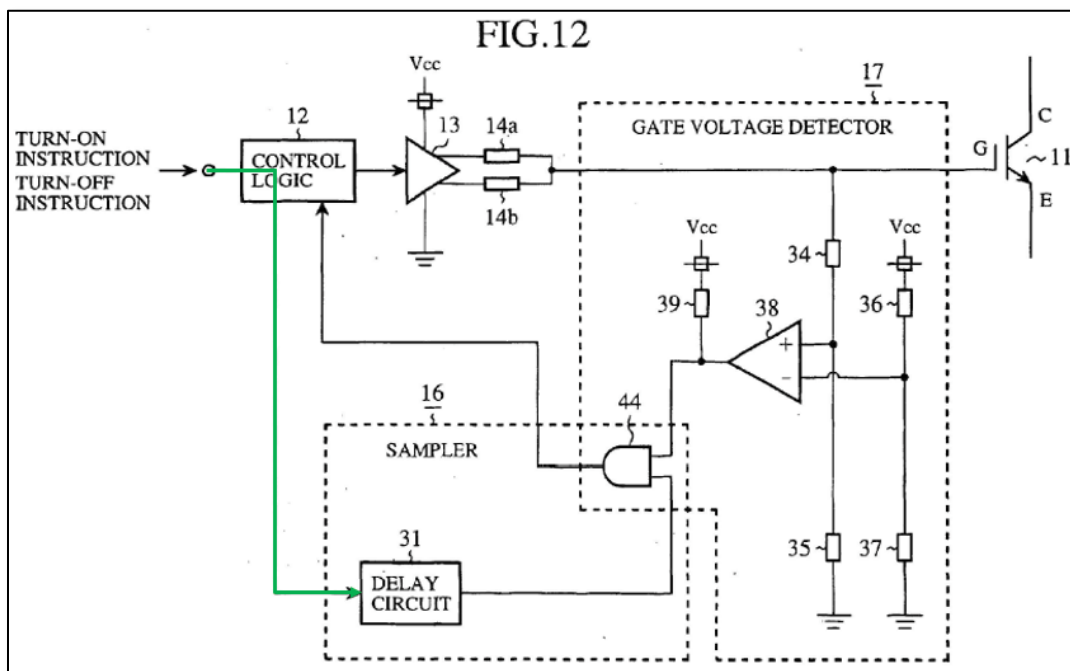
sampler 16. *Id.* at ¶ 62. Accordingly, a POSITA would have understood that the turn-on instruction is a falling edge signal (i.e., a transition from High-to-Low) that is directly passed along by control logic 12 and is received by sampler 16 at time t_0 . *Id.* Even assuming, for the sake of argument, that turn-on instruction were a rising edge signal that control logic 12 inverted before transmitting to sampler 16, this arrangement would still teach limitation [1(c)]. Indeed, the '835 Patent expressly allows for signals to pass through inverters and still considered them *supplied to* a destination. For example, the '835 Patent notes that control input signal S1 is supplied to one-shot generation circuit 1 and also to gate driver GD through two separate inverters and a NOR gate:

[A] **control input signal S1** supplied to control the transistor 12 from the outside through the control signal input terminal U_{IN} **is supplied not only to the gate driver GD via an inverter circuit G3, a NOR circuit G4 and an inverter circuit G5 but also to a** one-shot generation circuit 1.

'835 *Patent* (Ex. 1001), 4:50-55 (emphasis added); Fig. 2 (illustrating the same). Accordingly, even if control logic 12 did invert Ohi's turn-on instruction before delivering it to sampler 16—there is no suggestion that such an inversion occurs—the turn-on instruction is still received by sampler 16, as claimed. *Dec.* (Ex. 1004), ¶ 62.

Alternatively, Ohi's sampler 16 and control logic 12 satisfy the claimed pulse generation circuit

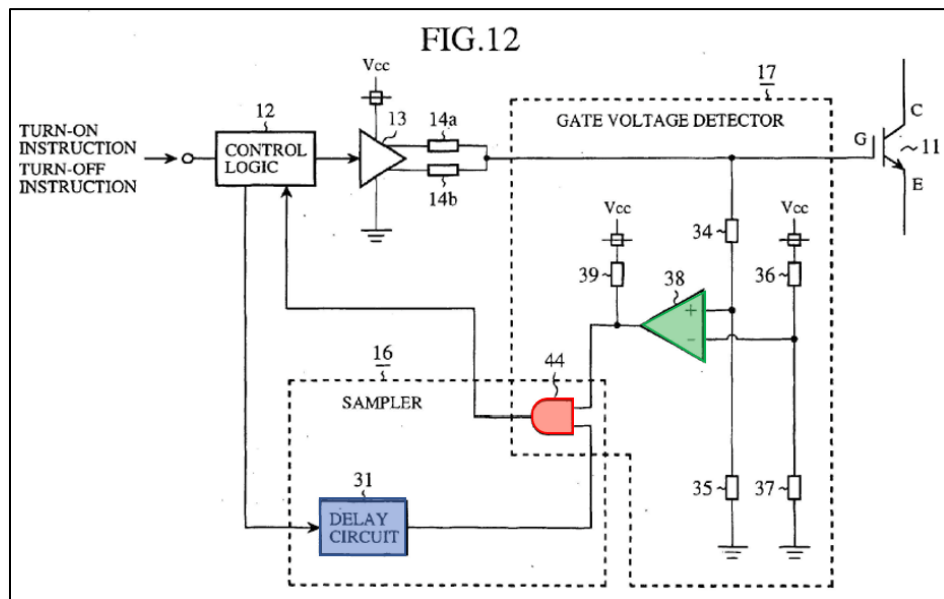
Alternatively, (1) the portion of control logic 12 that directly receives the turn-on instruction (*control input signal*) from outside the circuit and (2) sampler 16 collectively satisfy the claimed *pulse generation circuit*. As described in the preceding paragraphs, *Ohi's* turn-on instruction passes first through control logic 12 and then to sampler 16 as illustrated below:



Ohi (Ex. 1003), Fig. 12 (annotated). Accordingly, the combination of control logic 12 and sampler 16 also satisfies the claimed *pulse generation circuit receiving said control input signal*. *Dec.* (Ex. 1004), ¶ 63.

[1(d)] a comparator receiving the detecting voltage of said control output signal, performing a comparison with said reference voltage and outputting a second pulse signal being significant during a period when the detecting voltage of said control output signal exceeds said reference voltage; and

As discussed above with reference to limitation [1(b)], the fifth embodiment, as depicted in Fig. 12 below, utilizes three key components to detect a short circuit abnormality immediately following a turn-on instruction: (1) **sampler 16** (including **delay circuit 31** in the Fig. 12 embodiment) that generates a *first pulse signal* that defines the “detection time period during which the gate voltage V_g of an IGBT is detected[,]” (2) **comparator 38** that outputs a *second pulse signal* when gate voltage V_g of the IGBT exceeds a threshold voltage, and (3) **AND circuit 44** that receives the first and second pulse signals and outputs a High signal when V_g exceeds the threshold during the detection time period. *Id.* at 12:32-44.



Id. at Fig. 12 (annotated).

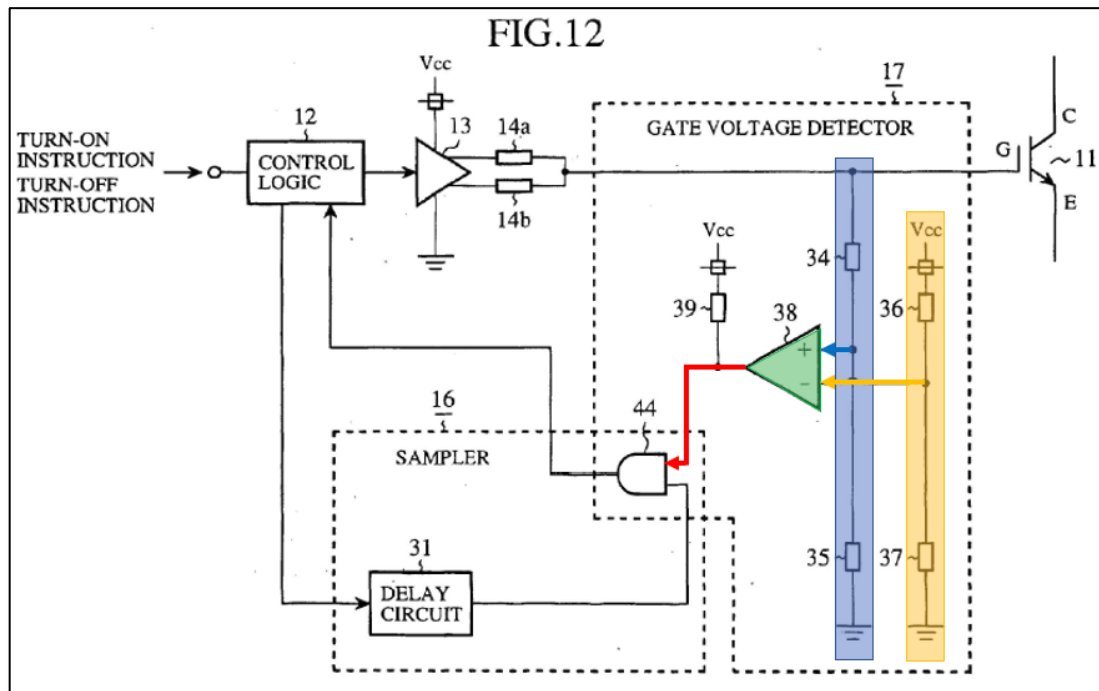
This limitation is satisfied by **comparator 38**, which receives at its “+” terminal input a divided-down gate voltage of IGBT 11 (*receiving the detecting voltage of said control output signal*), receives at its “–” terminal a *reference voltage*, and performs a comparison of those inputs, outputting a High signal when the divided-down gate voltage exceeds the reference voltage (*performing a comparison with said reference voltage and outputting a second pulse signal being significant during a period when the detecting voltage of said control output signal exceeds said reference voltage*).

This limitation recites a “detecting voltage of said control output signal[.]” As discussed above with reference to limitation [1(b)], a POSITA would understand, pursuant to the ’835 Patent’s disclosure, that a “detecting voltage of said control output signal” is a measured gate voltage or a divided down representation of the measured gate voltage. *Dec.* (Ex. 1004), ¶¶ 64-66. *Ohi* teaches the same arrangement as the ’835 Patent. Namely, the drive circuit in *Ohi* includes a gate voltage detector 17 that provides a divided down representation of the gate terminal of IGBT 11 to comparator 38, which compares it to a reference voltage and outputs a High pulse signal when the gate voltage representation exceeds the reference voltage:

The **comparator 38** of a gate voltage detector 17 compares a divided voltage obtained from the gate voltage V_g of the IGBT with a divided voltage obtained from the control voltage V_{cc} of the IGBT, like that of above-mentioned embodiment 2, and, **when the gate voltage V_g**

reaches the **control voltage V_{cc}** in level, causes its **output signal** to make a transition from a Low level to a High level (see Fig. 13).

Ohi (Ex. 1003), 12:37-44 (emphasis added); Fig. 13. This arrangement is depicted below in Fig. 12:

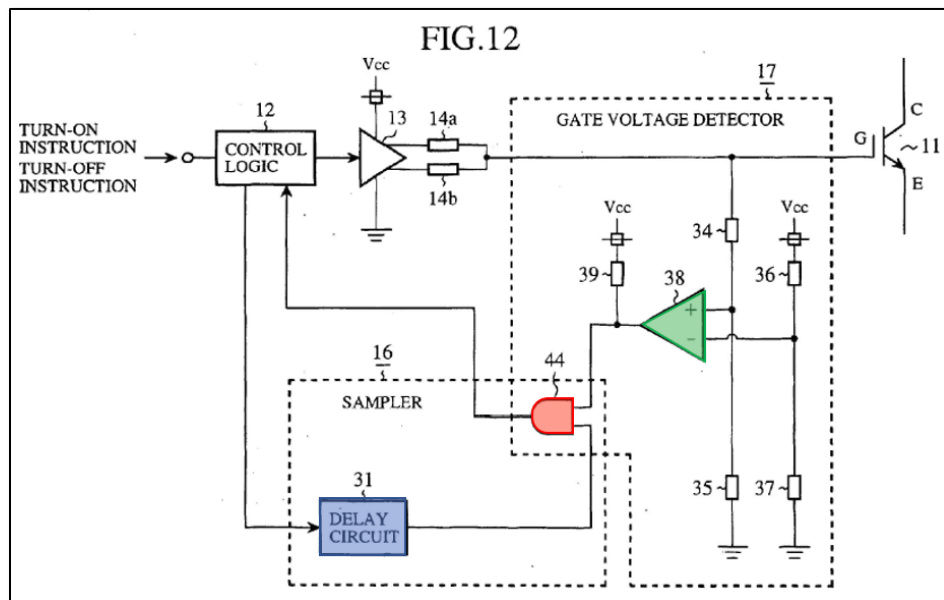


Id. at Fig. 12 (annotated).

[1(e)] a logical circuit receiving said first and second pulse signals and outputting a stop signal forcing said driver to stop said control output signal when said second pulse signal becomes significant during a period when said first pulse signal is significant.

As discussed above with reference to limitation [1(b)], the fifth embodiment, as depicted in Fig. 12 below, utilizes three key components to detect a short circuit abnormality immediately following a turn-on instruction: (1) **Sampler 16** (including **delay circuit 31** in the Fig. 12 circuit) that generates a *first pulse signal* that defines

the “detection time period during which the gate voltage V_g of an IGBT is detected[,]” (2) **comparator 38** that outputs a *second pulse signal* when gate voltage V_g of the IGBT exceeds a threshold voltage, and (3) **AND circuit 44** that receives the first and second pulse signals and outputs a High signal when V_g exceeds the threshold during the detection time period. *Id.* at 12:32-58.



Id. at Fig. 12 (annotated).

A short circuit condition is detected by AND gate 44 when both the output of comparator 38 and delay circuit 31 are High:

The AND circuit 44 receives the output signal of the comparator 38 and the output signal of the delay circuit 31 and then implements a logical AND operation on them. . . . **[W]hen a short circuit occurs in the IGBT 11, the output-signal of the AND circuit 44 becomes a High level** (i.e., a logical level indicating a detection of the occurrence of an abnormality in the IGBT) **because the output signal of the**

comparator 38 becomes a High level before the output signal of the delay circuit 31 becomes a Low level.

Id. at 12:45-58 (emphasis added). When such a short circuit condition is detected, **logical circuit 44** generates a stop signal that causes IGBT to be turned off. *Id.* at 12:53-60 (“[W]hen a short circuit occurs in the IGBT 11, the output-signal of the AND circuit 44 becomes a High level (i.e., a logical level indicating a detection of the occurrence of an abnormality in the IGBT . . . [.] After that, the drive circuit operates in the same way that that of embodiment 2 does[.]”), 10:14-21 (describing embodiment 2, teaching that the circuit “delivers an abnormality signal to the control logic 12[, and, a]s a result, the control logic 12 causes the IGBT 11 to become turned-off[.]”).

In sum, AND gate 44 (*a logical circuit*) receives as inputs the output of comparator 38 and the output of delay circuit 31 (*receiving said first and second pulse signals*) and outputs a stop signal forcing off IGBT 11 (*outputting a stop signal forcing said driver to stop said control output signal*) when delay circuit 31 produces a High signal defining the detection time period at the same time that comparator 38 produces a High signal indicating the gate voltage exceeds a reference voltage (*produced when said second pulse signal becomes significant during a period when said first pulse signal is significant*).

ii. Claim 2

The semiconductor device according to claim 1, wherein said predetermined period when said first pulse signal is significant is set on a basis of a period when a voltage of said control output signal is clamped constantly when said insulated gate transistor normally operates.

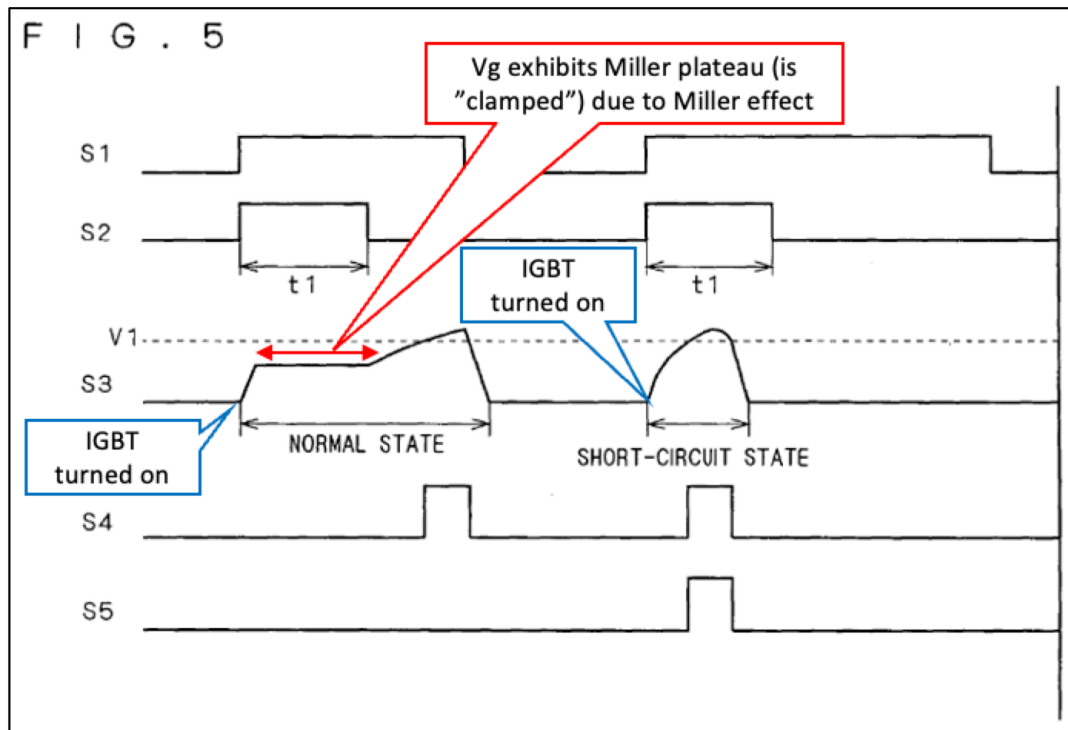
The '835 Patent describes a phenomenon in IGBT devices in which the gate voltage sticks at a mid-point voltage (referred to as “clamped” at that voltage) following a turn-on instruction for a period of time before rising to the normal operating voltage that is near V_{cc} :

[W]hen a voltage of the control output signal S3 exceeds a threshold value of the transistor 12, the transistor 12 comes to be in ON state, and a collector-emitter voltage of the transistor 12 drops, thus a voltage of the control output signal S3 is clamped to a certain voltage for a determined period by a [Miller]⁷ effect, however, the voltage of the

⁷The '835 Patent uses the term “mirror effect.” Petitioner believes this is a clerical error and should instead be “Miller effect.” Indeed, as Dr. Liu explains (and as *Ohi* confirms), this phenomenon of the gate voltage stalling or clamping at a mid-point voltage for a short period after the transistor is turned on is well understood in the field and is referred to as the “Miller effect.” *Dec.* (Ex. 1004), ¶ 27, fn1. Confirming Petitioner’s proposed fix for this clerical error, the machine translation of the '835 Patent’s Japanese language priority filing uses the phrase, “Miller effect.” *Machine*

control output signal S3 rises to be a value almost equal to the drive voltage VCC of the gate driver GD after that.

'835 Patent (Ex. 1001), 5:62-6:3 (emphasis added). This clamping at a mid-point voltage for a period after the IGBT is turned on is illustrated in Fig. 5:



Id. at Fig. 5 (annotated). Consistent with the language of Claim 2, the '835 Patent further teaches that this clamped/Miller period should be used to define the short-circuit detection period t_1 , which is dictated by the time at which the pulse generation circuit's output S2 is "significant":

Translation of JP4531500 (Ex. 1005), 2:10 ("Therefore, the voltage of the control output signal S3 is set to a predetermined value due to the Miller effect.").

[T]he one-shot **pulse generation circuit 1 outputs** the pulse signal **S2 which comes to be in the significant condition** according to the building up of the control input signal S1, and a period t1 in the significant condition, in the “H” state in this case, is set to be **almost equal to a period when the control output signal S3 is clamped to a certain voltage.**

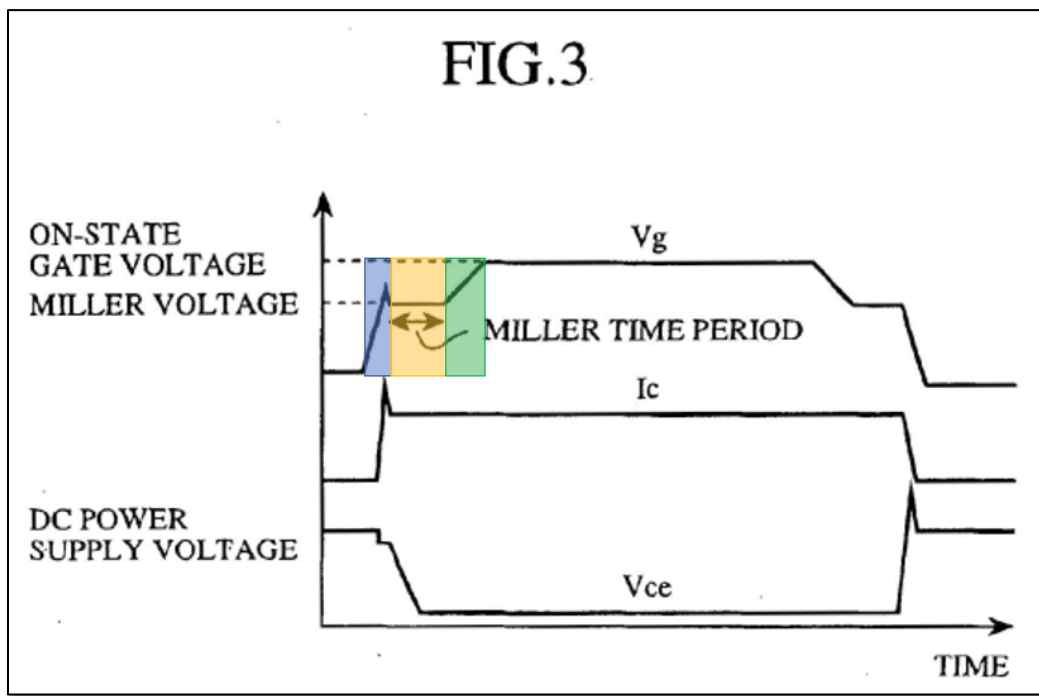
Id. at 6:35-40 (emphasis added). As illustrated in Fig. 5 above, the Miller effect clamping prevents the IGBT gate voltage from exceeding reference voltage V1 during the measurement period. Because a short circuit condition will not be similarly clamped, Vg will exceed the reference voltage V1 even within the time period t1.

Ohi teaches this precise process and acknowledges that it is also based on the Miller effect described by the '835 Patent. Namely, *Ohi* describes a “Miller time period” during which the IGBT’s gate voltage is clamped:

When the drive circuit sends a gate instruction to instruct the IGBT 11 to turn on in response to a turn-on instruction under normal operating conditions, the gate voltage Vg of the IGBT 11 starts rising. When the gate voltage Vg then exceeds a threshold voltage, the collector current Ic starts increasing. When the collector current Ic flowing in the IGBT 11 becomes nearly equal to an inductive load electric current flowing through the inductive load, the collector-emitter voltage Vce starts decreasing and **the gate voltage Vg then becomes a nearly-constant voltage. This time period** during which the gate voltage Vg is nearly constant after the collector current

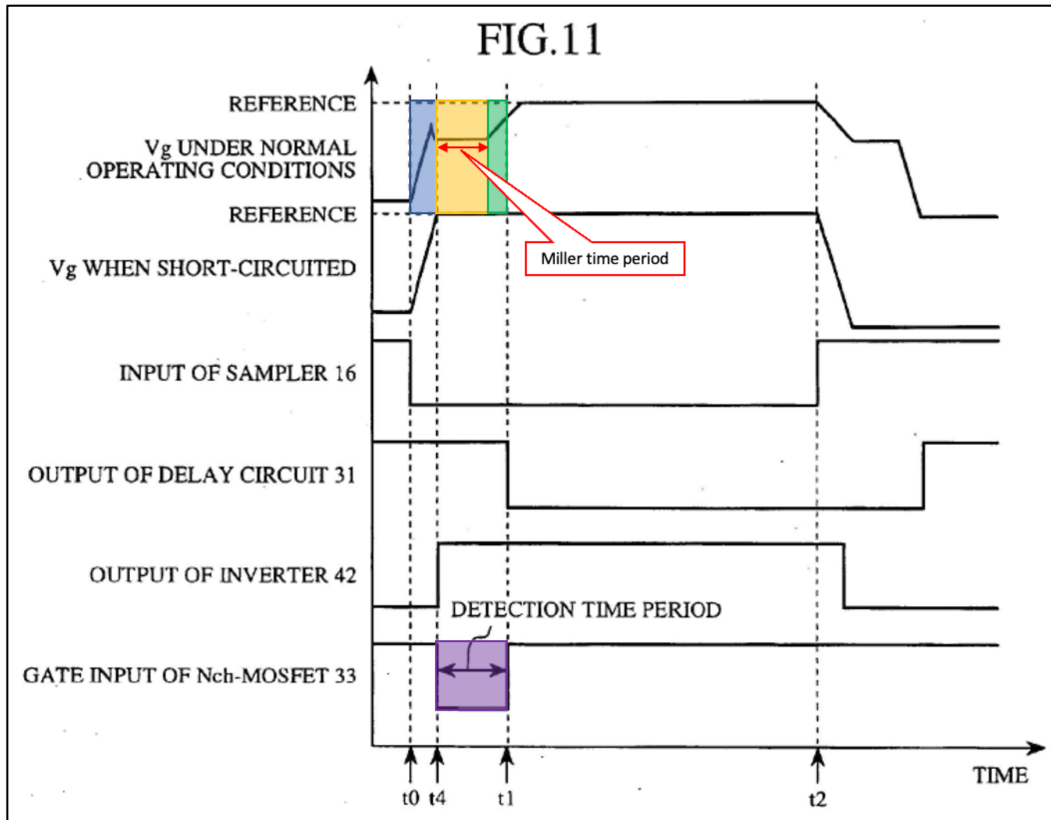
I_c has become nearly equal to the inductive load electric current is known as a Miller time period. . . . At the conclusion of the Miller time period, the gate voltage V_g starts rising again. At this time, the gate voltage rises slowly with a smaller time constant than that with which the gate voltage has risen before the Miller time period because the feedback capacitance is large, and then reaches a certain on-state gate voltage. The gate voltage V_g enters a steady state after it has experienced the above-mentioned transition time period.

Ohi (Ex. 1003), 5:61-6:25 (emphasis added). As described above and as illustrated below in Fig. 3, there are three distinct phases—(1) a first recovery time phase where V_g rises quickly and then drops back down to the Miller time period clamped voltage, (2) the Miller time period clamped voltage, and (3) a slower rise up to an on-state gate voltage:



Id. at Fig. 3.

Like the '835 Patent, *Ohi* also uses the Miller time period (i.e., the time during which the IGBT gate voltage is clamped) to determine the measurement/detection period. In one example, as discussed above with reference to limitation [1(c)], *Ohi* teaches a sampler 16 that uses two delay circuits to define a “detection time period during which the gate voltage V_g is detected [that] excludes a certain time period (e.g., the time period from the time t_0 to the time t_4) immediately after the IGBT 11 is turned on.” *Id.* at 11:36-40. *Ohi* explains that this two-delay circuit sampler 16 excludes this time period from t_0 to t_4 “in order for the **detection time period** during which the gate voltage V_g is detected **to start after the conclusion of the recovery time period** at the turn-on time[.]” *Id.* at 11:52-55 (emphasis added). In other words, the sampler 16 is designed specifically to ensure the detection time period does not begin until the Miller time period has been reached. *Dec.* (Ex. 1004), ¶¶ 70-73. This is depicted in Fig. 11 below:



Id. at Fig. 11 (annotated). As illustrated, the detection time period begins at the moment the **Miller time period** begins, i.e., as soon as the **recovery time period** ends.

As set forth above in the Claim 1 mapping, *Ohi* expressly teaches that this two-delay circuit sampler 16 can be incorporated into the fifth embodiment circuit as depicted in Fig. 12. And, when that sampler 16 is implemented in Fig. 12, sampler 16 outputs a pulse that remains High for a predetermined time period (*predetermined period when said first pulse signal is significant*) and that time period, as illustrated in Fig. 11 above, is set to begin on the basis of when the Miller time period begins causing V_g of the IGBT to be clamped constantly during normal operation (*is set on*

a basis of a period when a voltage of said control output signal is clamped constantly when said insulated gate transistor normally operates).

V. THE BOARD SHOULD NOT DENY INSTITUTION UNDER FINTIV

Under the “*Fintiv* factors,” the Board may consider parallel litigation, including an early trial date, in determining whether to institute under 35 U.S.C. § 314(a). *NHK Spring Co., Ltd., v. Intri-Plex Technologies, Inc.*, IPR2018-00752, 19–20 (PTAB Sept. 12, 2018) (precedential); *Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, 2–3, 6 (PTAB Mar. 20, 2020) (precedential). Director Vidal recently issued a memorandum setting forth Interim *Fintiv* Guidance (“*Fintiv Memo*”).⁸ The *Fintiv Memo* is “binding agency guidance” to the Board. *Fintiv Memo*, 3.

As stated in the *Fintiv Memo*, “[t]he [Board] will not discretionarily deny petitions based on applying *Fintiv* to a parallel ITC proceeding.” *Id* at 7. The Director’s reasoning is that “the ITC lacks authority to invalidate a patent and its invalidity rulings are not binding on either the Office or a district court[.]” and as such, “denying institution because of a parallel ITC investigation will not necessarily minimize potential conflicts” with Board proceedings. *Fintiv Memo*, 6-7. Here, the district court litigation is stayed pending resolution of the ITC investigation, which

⁸https://www.uspto.gov/sites/default/files/documents/interim_proc_discretionary_denials_aia_parallel_district_court_litigation_memo_20220621.pdf.

means the ITC investigation is the sole active parallel proceeding relevant to the *Fintiv* analysis. Accordingly, the Board should not discretionarily deny institution under *Fintiv*.

VI. CONCLUSION

For the foregoing reasons, Petitioner respectfully requests *inter partes* review of Claims 1 and 2 of the '835 Patent.

Respectfully submitted,

By: /s/ Paul R. Hart

Paul R. Hart, Reg. No. 59,646

Adam P. Seitz, Reg. No. 52,206

COUNSEL FOR PETITIONER

VII. MANDATORY NOTICES UNDER 37 C.F.R. § 42.8(A)(1)

A. Real Party-In-Interest

Petitioner is the real party-in-interest. 37 C.F.R. § 42.8(b)(1).

B. Related Matters

Pursuant to 37 C.F.R. § 42.8(b)(2), Petitioner is aware of the following matters involving the '835 Patent:

1. *Arigna Technology Limited v. Samsung Electronics Co., Ltd. et al.*, No. 6:22-cv-00151 (W.D. Tex.) (currently stayed); and
2. In the Matter of Certain Power Semiconductors, and Mobile Devices and Computers Containing Same, Inv. No. 337-TA-1308 (ITC).

C. Lead and Back-Up Counsel

Petitioner provides the following designation and service information for lead and back-up counsel. 37 C.F.R. § 42.8(b)(3) and (b)(4).

Lead Counsel	Back-Up Counsel
Paul R. Hart (Reg. No. 59,646) Paul.Hart@eriseip.com PTAB@eriseip.com	Adam P. Seitz (Reg. No. 52,206) Adam.Seitz@eriseip.com PTAB@eriseip.com
<u>Postal and Hand-Delivery Address:</u> Erise IP, P.A. 5299 DTC Blvd., Ste. 1340 Greenwood Village, Colorado 80111 Telephone: (913) 777-5600 Fax: (913) 777-5601	<u>Postal and Hand-Delivery Address:</u> Erise IP, P.A. 7015 College Blvd., Ste. 700 Overland Park, Kansas 66211 Telephone: (913) 777-5600 Fax: (913) 777-5601

APPENDIX OF EXHIBITS

Exhibit 1001	U.S. Patent No. 7,183,835 (“’835 <i>Patent</i> ”)
Exhibit 1002	File History for U.S. Patent 7,183,835 (“’835 <i>File History</i> ”)
Exhibit 1003	U.S. Patent No. 6,906,574 to Ohi et al. (“ <i>Ohi</i> ”)
Exhibit 1004	Declaration of David Kuan-Yu Liu in Support of IPR (“ <i>Dec.</i> ”)
Exhibit 1005	Machine Translation of JP4531500 (“ <i>Machine Translation of JP4531500</i> ”)
Exhibit 1006	Dulau, et al., A New Gate Driver Integrated Circuit for IGBT Devices With Advanced Protections, IEEE Transactions on Power Electronics, Vol. 21, No. 1, January 2006 (“ <i>Dulau</i> ”)

CERTIFICATION OF WORD COUNT

The undersigned certifies pursuant to 37 C.F.R. § 42.24 that the foregoing Petition for *Inter Partes* Review, excluding any table of contents, mandatory notices under 37 C.F.R. § 42.8, certificates of service or word count, or appendix of exhibits, contains 10,496 words according to the word-processing program used to prepare this document (Microsoft Word).

Dated: January 11, 2023

By: /s/ Paul R. Hart
Paul R. Hart, Reg. No. 59,646

COUNSEL FOR PETITIONER

CERTIFICATE OF SERVICE ON PATENT OWNER
UNDER 37 C.F.R. § 42.105

Pursuant to 37 C.F.R. §§ 42.6(e) and 42.105, the undersigned certifies that on January 11, 2023, a complete and entire copy of this Petition for *Inter Partes* Review including exhibits was provided via Federal Express to the Patent Owner by serving the correspondence address of record for the '835 Patent as listed on PAIR:

MCDERMOTT WILL & EMERY LLP
The McDermott Building
500 North Capitol Street, N.W.
Washington, DC 20001

Further, a courtesy copy of this Petition for *Inter Partes* Review was sent via email to Patent Owner's litigation counsel:

Amy V. Hall
ahall@susmangodfrey.com
Andres Healy
ahealy@susmangodfrey.com
Bryce T. Barcelo
bbarcelo@susmangodfrey.com
John E. Schiltz
jschiltz@susmangodfrey.com
Kemper P. Diehl
kdiehl@susmangodfrey.com
Matthew R. Berry
mberry@susmangodfrey.com
Robert Greenfeld
rgreenfeld@susmangodfrey.com
Matthew R. Berry
mberry@susmangodfrey.com

By: /s/ Paul R. Hart
Paul R. Hart, Reg. No. 59,646

COUNSEL FOR PETITIONER