

**UNITED STATES INTERNATIONAL TRADE COMMISSION
Washington, D.C.**

**Before the Honorable Monica Bhattacharyya
Administrative Law Judge**

In the Matter of

**CERTAIN POWER SEMICONDUCTORS, AND
MOBILE DEVICES AND COMPUTERS
CONTAINING SAME**

Inv. No. 337-TA-1308

RESPONDENTS' OPENING CLAIM CONSTRUCTION BRIEF

TABLE OF CONTENTS

	<u>Page</u>
I. INTRODUCTION	1
II. LEGAL PRINCIPLES OF CLAIM CONSTRUCTION	2
III. THE ASSERTED PATENT	4
A. Technology Background.....	5
B. Patent Overview	7
1. Purported shortcomings of the prior art using a shunt resistor for short-circuit detection.	7
2. The alleged solution.	8
3. The Figure 2 embodiment.	8
4. Operation of the alleged invention to protect against short-circuits.	10
IV. PERSON OF ORDINARY SKILL IN THE ART	13
V. DISPUTED CLAIM TERMS	13
A. Preamble (claim 1).....	13
1. The preamble provides antecedent basis for terms in the claim body.....	14
2. The preamble recites essential aspects of the alleged invention and gives life, meaning and vitality to the claim.	16
B. “insulated gate transistor” (claims 1 and 2)	21
C. “controlling a drive of an insulated gate transistor” (claim 1).....	25
D. “indicates a conduction of said insulated gate transistor” (claim 1).....	29
E. “significant” (claims 1 and 2)	30
F. “clamped constantly” (claim 2)	34
1. The “Miller effect” determines clamping.	35
2. “Miller effect” was wrongly translated as “mirror effect.”	38
G. “control output signal” (claim 1)	39
H. “short-circuit protection circuit” (claim 1)	41
VI. CONCLUSION.....	46

TABLE OF AUTHORITIES

	Page(s)
Cases	
<i>In re Abbott Diabetes Care Inc.</i> , 696 F.3d 1142 (Fed. Cir. 2012).....	23
<i>Allen Eng’g Corp. v. Bartell Indus.</i> , 299 F.3d 1336 (Fed. Cir. 2002).....	14
<i>Arista Networks, Inc. v. Cisco Sys.</i> , 908 F.3d 792 (Fed. Cir. 2018).....	3
<i>Bell Atl. Network Servs., Inc. v. Covad Comm’ns Grp., Inc.</i> , 262 F.3d 1258 (Fed. Cir. 2001).....	3
<i>Bell Commc’ns Research, Inc. v. Vitalink Commc’ns Corp.</i> , 55 F.3d 615 (Fed. Cir. 1995).....	13
<i>Bicon, Inc. v. Straumann Co.</i> , 441 F.3d 945 (Fed. Cir. 2006).....	13, 15, 16
<i>Bio-Rad Labs., Inc. v. 10X Genomics Inc.</i> , 967 F.3d 1353 (Fed. Cir. 2020).....	14
<i>Certain Mobile Tel. Handsets, Wireless Commun. Devices, and Components Thereof</i> , Inv. No. 337-TA-578, Comm’n Det., 2010 WL 1436458 (Mar. 1, 2010)	15
<i>Certain Power Inverters & Converters, Vehicles Containing the Same, & Components Thereof</i> , Inv. No. 337-TA-1267 (Jan. 18, 2022)	15, 18, 19, 20
<i>Certain Solid State Storage Drives, Stacked Elecs. Components, & Prod. Containing Same</i> , Inv. No. 337-TA-1097, Ord. No. 31, 2019, WL 2353508 (Mar. 26, 2019).....	14
<i>Computer Docking Station Corp. v. Dell, Inc.</i> , 519 F.3d 1366, 86 U.S.P.Q.2d 1129 (Fed. Cir. 2008)	17
<i>Eaton Corp. v. Rockwell Int’l Corp.</i> , 323 F.3d 1332 (Fed. Cir. 2003).....	14
<i>Ekchian v. Home Depot, Inc.</i> , 104 F.3d 1299 (Fed. Cir. 1997).....	42, 46

<i>Eon Corp. IP Holdings v. Silver Spring Networks</i> , 815 F.3d 1314 (Fed. Cir. 2016).....	2, 27
<i>In re Fought</i> , 941 F.3d 1175 (Fed. Cir. 2019).....	14
<i>Gen. Elec. Co. v. Nintendo Co.</i> , 179 F.3d 1350 (Fed. Cir. 1999).....	17, 18
<i>Groove Digital, Inc. v. United Bank</i> , 825 F. App'x 852 (Fed. Cir. 2020) (unpublished)	23
<i>Homeland Housewares, LLC v. Whirlpool Corp.</i> , 865 F.3d 1372 (Fed. Cir. 2017).....	3
<i>Indivior Inc. v. Dr. Reddy's Lab 'ys, S.A.</i> , 930 F.3d 1325 (Fed. Cir. 2019).....	43
<i>Markman v. Westview Instruments, Inc.</i> , 52 F.3d 967 (Fed. Cir. 1995) (en banc), <i>aff'd</i> , 517 U.S. 370 (1996).....	13, 27
<i>Mass. Institute of Tech. and Elecs. for Imaging v. Abacus Software</i> , 462 F.3d 1344 (Fed. Cir. 2006).....	3
<i>Multiform Desiccants, Inc. v. Medzam, Ltd.</i> , 133 F.3d 1473 (Fed. Cir. 1998).....	26
<i>Netword, LLC v. Centraal Corp.</i> , 242 F.3d 1347 (Fed. Cir. 2001).....	2
<i>O2 Micro Int'l Ltd. v. Beyond Innovation Tech. Co.</i> , 521 F.3d 1351 (Fed. Cir. 2008).....	<i>passim</i>
<i>On Demand Mach. Corp. v. Ingram Indus.</i> , 442 F.3d 1331 (Fed. Cir. 2006).....	17
<i>Openwave Sys., Inc. v. Apple Inc.</i> , 808 F.3d 509 (Fed. Cir. 2015).....	42
<i>Pacing Techs., LLC v. Garmin Int'l, Inc.</i> , 778 F.3d 1021 (Fed. Cir. 2015).....	14
<i>Phillips v. AWH Corp.</i> , 415 F.3d 1303 (Fed. Cir. 2005) (en banc).....	<i>passim</i>
<i>Pitney Bowes, Inc. v. Hewlett-Packard Co.</i> , 182 F.3d 1298 (Fed. Cir. 1999).....	<i>passim</i>

<i>Poly-Am., L.P. v. API Indus., Inc.</i> , 839 F.3d 1131 (Fed. Cir. 2016).....	23, 42, 46
<i>Poly-Am., L.P. v. GSE Lining Tech., Inc.</i> , 383 F.3d 1303 (Fed. Cir. 2004).....	19
<i>Profectus Tech. LLC v. Huawei Techs. Co.</i> , 823 F.3d 1375 (Fed. Cir. 2016).....	23
<i>Proveris Sci. Corp. v. Innovasystems, Inc.</i> , 739 F.3d 1367 (Fed. Cir. 2014).....	14, 17
<i>T D X Energy, L.L.C. v. Chesapeake Operating, Inc.</i> , 857 F.3d 253 (5th Cir. 2017)	16
<i>Toro Co. v. White Consol. Indus., Inc.</i> , 199 F.3d 1295 (Fed. Cir. 1999).....	2
<i>UltimatePointer, L.L.C. v. Nintendo Co.</i> , 816 F.3d 816 (Fed. Cir. 2016).....	43
<i>Unwired Planet L.L.C. v. Google, Inc.</i> , 660 F. App'x 974 (Fed. Cir. 2016)	20
<i>Verizon Servs. v. Vonage Holdings</i> , 503 F.3d 1295 (Fed. Cir. 2007).....	18
Other Authorities	
American Heritage Dictionary of the English Language 1619 (4th Ed. 2000)	33
B.J. Baliga, et al., <i>The Insulated Gate Transistor: A New Three-Terminal MOS- Controlled Bipolar Power Device</i> , IEEE TRANSACTIONS ON ELECTRON DEVICES, Vol. ED-31, No. 6, June 1984.....	21
B.J. Baliga, <i>Fast-Switching Insulated Gate Transistors</i> , IEEE ELECTRON DEVICE LETTERS, Vol. EDL-4, No. 12 (Dec. 1983)	21
M.P.E.P. § 2173.05(e).....	16
Cambridge Dictionary Online (https://dictionary.cambridge.org/us/dictionary/english/significant , last visited 8/5/2022)	33
Chambers Dictionary 1410 (2003).....	33
H. Yilmaz, <i>Insulated Gate Transistor Modeling and Optimization</i> , 1984 INTERNATIONAL ELECTRON DEVICES MEETING (Dec. 1984)	21

IEEE Standard Dictionary of Electrical and Electronic Terms (6th ed. 1996).....	35
Merriam-Webster’s Collegiate Dictionary 1091 (10th Ed. 1997)	33
New Oxford American Dictionary 1588 (2001).....	33

Respondents Apple Inc., TCL Electronics Holdings Ltd., TCL Communication Ltd., TTE Technology, Inc. and TCT Mobile (US) Inc. (collectively “Respondents”) submit this opening claim construction brief related to asserted U.S. Patent No. 7,183,835 (“the ’835 patent”).

I. INTRODUCTION

Complainant Arigna Technology Limited (“Arigna”) alleges that Respondents’ cellular mobile devices infringe claims 1 and 2 of the ’835 patent. The ’835 patent is directed to and claims a specific semiconductor circuit layout that allegedly performs short-circuit protection without a shunt resistor for insulated gate-type switching devices controlled by the output of the claimed circuit. *See, e.g.*, ’835 patent at Abstract, Claims 1 and 2.

Despite the narrow scope of the patent’s disclosure and claims, Arigna attempts through the claim construction process to expand the scope of its claims well beyond the claimed invention. Arigna takes aggressive positions—such as arguing that the preamble of claim 1 is not limiting, or attempting to capture short-circuit protection with a shunt resistor when “without shunt resistor” is in the patent’s title, and the patent repeatedly disclaims and disparages prior art use of a shunt resistor. Arigna also often proposes a “plain and ordinary meaning” that differs from Respondents’ and Staff’s understanding. In those instances, Arigna uses the abbreviation “*e.g.*” before providing any example of what it argues the plain and ordinary meaning could be, leaving its proposed constructions open-ended and unhelpful. Arigna’s plain and ordinary meaning proposals would not crystallize the scope of asserted claims, contrary to the purpose of claim construction.

By contrast, Respondents propose constructions that capture the meaning of disputed terms when read in light of the claims and specification, as further supported by extrinsic

evidence. Commission Investigative Staff agrees with Respondents' constructions for most terms. Respondents request that the ALJ adopt their proposed constructions.

II. LEGAL PRINCIPLES OF CLAIM CONSTRUCTION

The standards for claim construction are well-established: “[W]ords of a claim are generally given their ordinary and customary meaning,” which is “the meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention, i.e., as of the effective filing date of the patent application.” *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312-13 (Fed. Cir. 2005) (en banc) (internal quotation marks omitted). This analysis focuses on the intrinsic evidence, which includes the claims themselves, the specification and the prosecution history. *Id.* at 1314-17. “[T]he context in which a term is used in the asserted claim” and “[o]ther claims of the patent in question” can be instructive as to the meaning of particular claim terms. *Id.* at 1314. Furthermore, the specification “is always highly relevant to the claim construction analysis. Usually, it is dispositive; it is the single best guide to the meaning of the disputed term.” *Id.* at 1315.

“The ordinary meaning of a claim term is not ‘the meaning of the term in the abstract.’ Instead, ‘the ‘ordinary meaning’ of a claim term is its meaning to the ordinary artisan after reading the entire patent.’” *Eon Corp. IP Holdings v. Silver Spring Networks*, 815 F.3d 1314, 1320 (Fed. Cir. 2016), quoting *Phillips*, 415 F.3d at 1321; *see also Netword, LLC v. Centraal Corp.*, 242 F.3d 1347, 1352 (Fed. Cir. 2001) (“The claims are directed to the invention that is described in the specification; they do not have meaning removed from the context from which they arose.”); *Toro Co. v. White Consol. Indus., Inc.*, 199 F.3d 1295, 1299 (Fed. Cir. 1999) (“Determining the limits of a patent claim requires understanding its terms in the context in

which they were used by the inventor, considered by the examiner, and understood in the field of the invention.”).

If the specification reveals “[a] special definition given to a claim term by the patentee that differs from the meaning it would otherwise possess . . . the inventor’s lexicography governs.” *Phillips*, 415 F.3d at 1316. The “specification’s consistent focus” can compel a particular construction of a term. *Arista Networks, Inc. v. Cisco Sys.*, 908 F.3d 792, 798 (Fed. Cir. 2018); *see also Homeland Housewares, LLC v. Whirlpool Corp.*, 865 F.3d 1372, 1377 (Fed. Cir. 2017) (“[w]hen a patentee uses a claim term throughout the entire patent specification, in a manner consistent with only a single meaning, he has defined that term ‘by implication’.”) (quoting *Bell Atl. Network Servs., Inc. v. Covad Comm’ns Grp., Inc.*, 262 F.3d 1258, 1271 (Fed. Cir. 2001)).

Courts may also consider extrinsic evidence, which “consists of all evidence external to the patent and prosecution history, including expert and inventor testimony, dictionaries, and learned treatises.” *Phillips*, 415 F.3d at 1317; *see also id.* at 1322 (“Dictionaries or comparable sources are often useful to assist in understanding the commonly understood meaning of words”). Where the intrinsic evidence fails to define a term explicitly or implicitly, “it is appropriate . . . to look to dictionary definitions of the terms.” *Mass. Institute of Tech. and Elecs. for Imaging v. Abacus Software*, 462 F.3d 1344, 1351 (Fed. Cir. 2006). “[E]xtrinsic evidence can shed useful light on the relevant art . . . [but] it is less significant than the intrinsic record in determining the legally operative meaning of claim language.” *Phillips*, 415 F.3d at 1317 (internal quotations omitted).

III. THE ASSERTED PATENT

The '835 patent, titled “[s]emiconductor device which realizes a short-circuit protection function without shunt resistor, and semiconductor device module,” relates generally to the field of semiconductors and semiconductor circuits used to control other semiconductor devices. *See, e.g.,* '835 patent at (54); Abstract. The '835 patent is directed to “a semiconductor device and a semiconductor device module including a short-circuit protection function of an insulated gate type switching device such as an IGBT (Insulated Gate Bipolar Transistor) and so on.” *Id.* at 1:12-15. Arigna asserts claims 1 and 2 of the '835 patent against Respondents. Claims 1 and 2 recite as follows, with preamble and reference letters added to the claim 1 limitations:

- 1[preamble]. A semiconductor device controlling a drive of an insulated gate transistor by generating a control output signal on a basis of a control input signal, comprising:
 - 1[a] a driver outputting said control output signal and
 - 1[b] a short-circuit protection circuit detecting said control output signal and controlling and forcing said driver to stop said control output signal when a detecting voltage of said control output signal exceeds a predetermined reference voltage before a predetermined period passes after said control output signal indicates a conduction of said insulated gate transistor, wherein
 - 1[c] said short-circuit protection circuit includes:
 - 1[d] pulse generation circuit receiving said control input signal and outputting a first pulse signal being significant only in said predetermined period according to a timing when said control input signal indicates the conduction of said insulated gate transistor;
 - 1[e] a comparator receiving the detecting voltage of said control output signal, performing a comparison with said reference voltage and outputting a second pulse signal being significant during a period when the detecting voltage of said control output signal exceeds said reference voltage; and
 - 1[f] a logical circuit receiving said first and second pulse signals and outputting a stop signal forcing said driver to stop said control output signal when said second pulse signal becomes significant during a period when said first pulse signal is significant.
- 2. The semiconductor device according to claim 1, wherein said predetermined period when said first pulse signal is significant is set on a basis of a period when a voltage of said control output signal is clamped constantly when said insulated gate transistor normally operates.

A. Technology Background

At a high level, transistors are electronic devices that can be used as a switch (*i.e.*, turn on and off) for electric signals and power, or to amplify electric signals and power. Many types of transistors exist, but the '835 patent expressly recognizes two by name: Insulated Gate Bipolar Transistors (“IGBT”) and metal–oxide–semiconductor (“MOS”) transistors (also referred to in the art as metal–oxide–semiconductor field-effect transistors (“MOSFET”)). *See, e.g.*, '835 patent at 1:10-15; 4:27-42. The patent recognizes that IGBTs are often desirable for controlling components such as electric motors. *See, e.g., id.* at 2:58-60; Fig. 1. Though both IGBTs and MOSFETs can perform similar functions in certain use cases, they have different internal structures. The electric terminals of IGBTs are usually referred to as the collector, emitter, and gate (*see, e.g.*, '835 patent at 5:60-6:5), and the electric terminals of MOSFETs are usually referred to as the source, drain, and gate (*see, e.g., id.* at 9:4-8). Different symbols are also used to identify each type of transistor. For example, the IGBT transistor uses the symbols CGE (to refer to collector, emitter, and gate), along with angled lines and an arrow in a specific direction, while the MOSFET uses SDG (to refer to the source, drain, and gate) and uses straight lines and different arrows to refer to N-Channel and P-Channel MOS transistors:

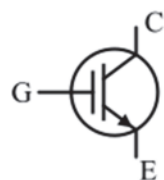
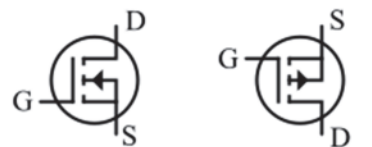


Figure 1 - IGBT



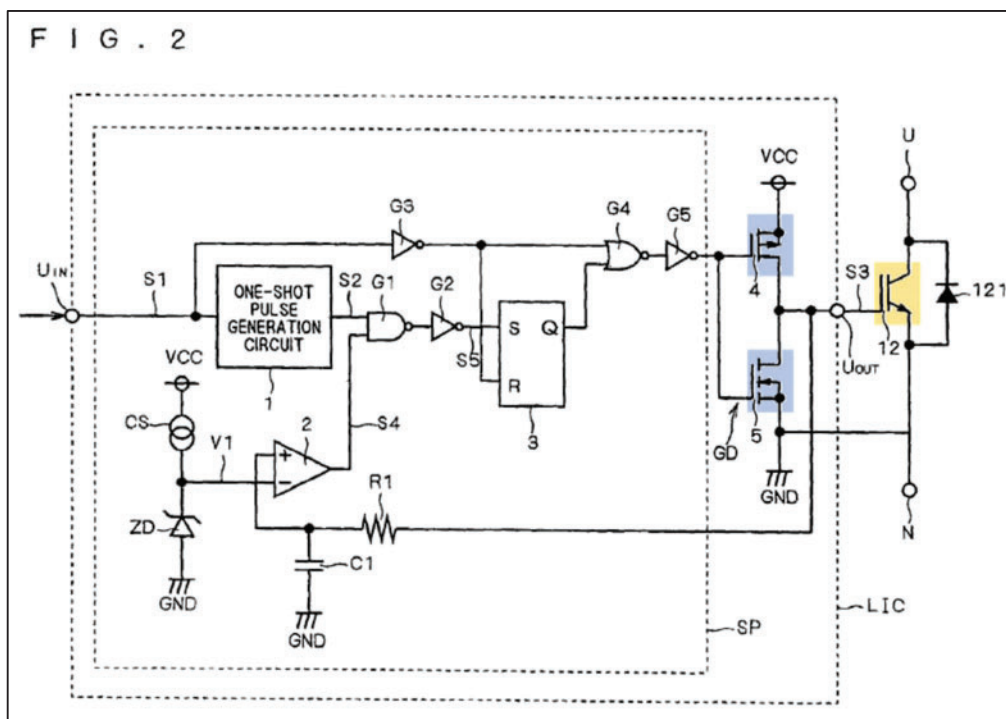
N-Channel

P-Channel

Figure 2 - MOSFET

See Difference between IGBT and MOSFET, <https://www.tutorialspoint.com/difference-between-igbt-and-mosfet> (last visited 8/5/2022). The patent uses both types of symbols in Figure 2. The patent uses the symbol for a MOSFET to represent MOSFETs (“P channel MOS transistor 4” and “N channel MOS transistor 5” (both annotated in blue below) used in the “gate

driver GD” circuit, the output of which is the “control output signal S3 to the gate electrode of the transistor 12,” “from the control signal output terminal U_{OUT}”). See ’835 patent at 4:14-42. And the patent uses the symbol for an IGBT to represent an IGBT transistor 12 (annotated in gold below)):



Id. at Fig. 6 (annotations added as described in text above).

In both types of transistors, when voltage is applied above a certain threshold to the gate of the transistor, current flows through the device; in the case of an IGBT, current flows via the collector-emitter path, and in a MOSFET, current flows via the source-drain path. See, e.g., *id.* at 1:17-25; 4:14-26; 4:27-42; 5:60-6:5; 7:4-21; 10:26-44; Figs. 2, 5, 6, 9. In other words, the gate terminal controls whether current flows between the two other terminals (collector-emitter or source-drain paths). A simple analogy is a water faucet: by turning the faucet handle (the gate), it causes water to flow from the water supply pipe (collector or source) out of the faucet opening (emitter or drain). In Figure 2, above, when a voltage is applied by the control output

signal S3 to the gate of transistor 12, it causes current to flow from terminal “P” towards terminal “U.” *See id.*; *see also* Fig. 1.

B. Patent Overview

The patent states that “[a] semiconductor device in which the insulated gate type switching device such as the IGBT and so on and a control circuit controlling a drive of that switching device are packaged is called as an IPM (Intelligent Power Module).” *Id.* at 1:17-20. When describing prior art systems for short-circuit protection of the IPM, the patent states that “with regard to a conventional IPM, a short-circuit protection is performed by connecting a shunt resistor detecting a main current flowing between main power terminals of the [insulated gate type] switching device outside the package and monitoring the main current.” *Id.* at 20-25. Since the shunt resistor would be connected across the main power terminals of the insulated gate type switching device (*e.g.*, the collector and emitter), if the current across the shunt resistor was outside of the expected range, it would indicate a short-circuit in the switching device. *Id.*

1. Purported shortcomings of the prior art using a shunt resistor for short-circuit detection.

The ’835 patent lists several alleged drawbacks to using a shunt resistor for short-circuit detection, as done in the prior art: (1) “the current detecting terminal is necessary to detect the voltage put on the shunt resistor”; (2) “it is necessary to set a filter circuit such as a CR filter and so on outside the package to remove a noise entering the shunt resistor and the current detecting terminal, and there is a possibility that a device becomes massive”; and (3) “when a length of a wiring from a ground main electrode to a ground terminal of the switching device becomes long by setting the shunt resistor, a voltage surge according to a switching of the switching device becomes large, and there is also a possibility that an error occurs.” *Id.* at 1:26-45.

2. The alleged solution.

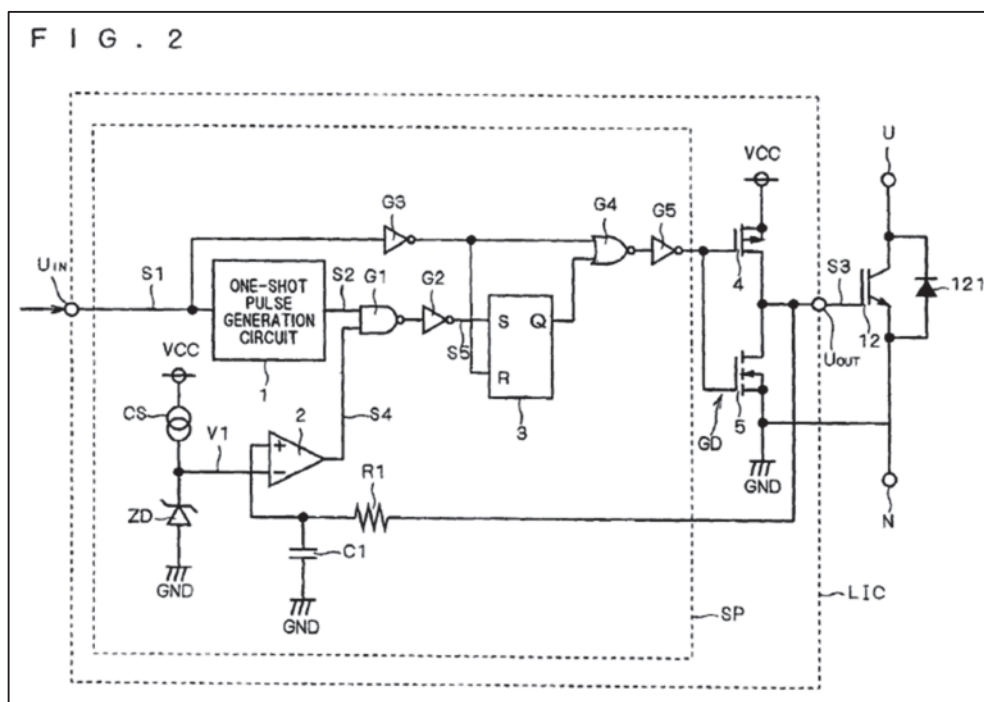
To overcome the purported drawbacks of using a shunt resistor for short-circuit protection, the patent discloses “[a] semiconductor device which realizes a short-circuit protection function without a shunt resistor and an IPM in which the semiconductor device is built... .” *Id.* at 1:49-51. The ’835 patent describes key aspects of “the present invention,” including that:

[The] semiconductor device controls a drive of an insulated gate transistor by generating a control output signal on a basis of a control input signal, and includes a driver outputting the control output signal and a short-circuit protection circuit detecting the control output signal and controlling and forcing the driver to stop the control output signal when a detecting voltage of the control output signal exceeds a predetermined reference voltage before a predetermined period passes after the control output signal indicates a conduction of the insulated gate transistor.

Id. at 1:52-62. In other words, by using the claimed “short-circuit protection circuit” and “controlling and forcing the driver to stop the control output signal” that controls the gate of the “insulated gate transistor,” the current flow through the “insulated gate transistor” is stopped when a short-circuit is detected. *Id.*

3. The Figure 2 embodiment.

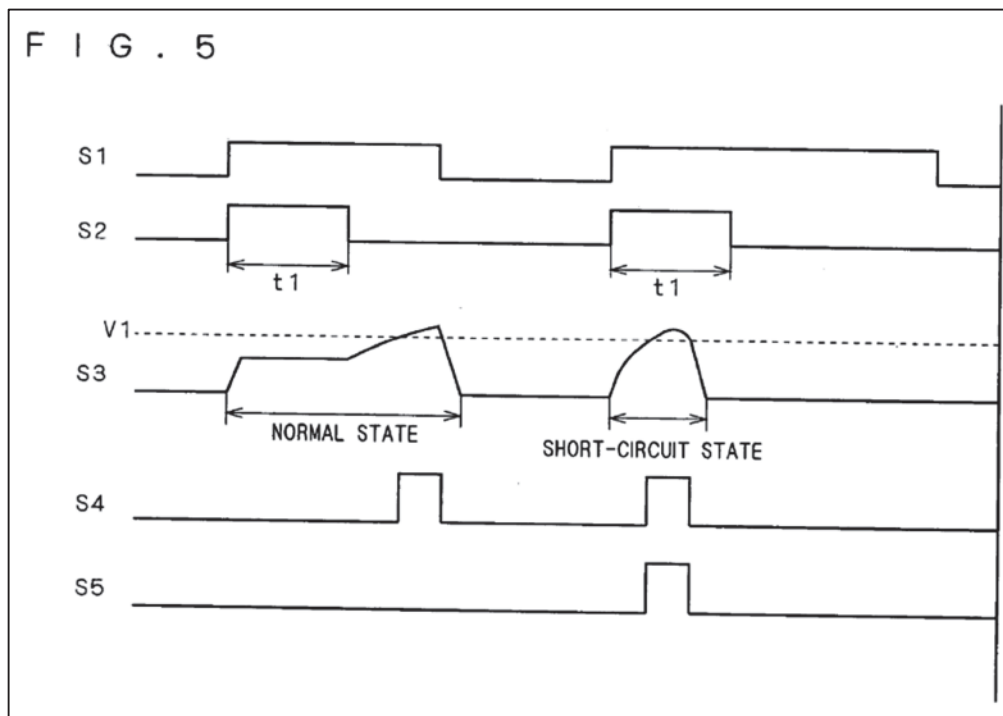
The ’835 patent discloses two embodiments of the alleged invention that purportedly perform short-circuit protection without the need for a shunt resistor. *See id.* at Figs. 2 and 6. The Fig. 2 embodiment is illustrative for purposes of asserted claim 1:



Id. at Fig. 2. In the Figure 2 embodiment, “the control output signal is supplied to the gate electrode of the transistor 12 from the control signal output terminal U_{OUT} of the control device LIC.” *Id.* at 4:14-16. The ’835 patent explains that the control output signal supplied to the insulated gate transistor “is also influenced when that transistor is short-circuited, and a signal waveform different from that in a normal operating state occurs.” *Id.* at 4:17-20. The ’835 patent states that “[t]he present invention is focused on this phenomenon, and it detects the short-circuit by monitoring the control output signal of the insulated gate transistor, and in case of the short-circuit, the short-circuit protection of the insulated gate transistor is performed by forcing the control device LIC to stop the control output signal.” *Id.* at 4:20-26. Thus, according to the ’835 patent, a key aspect of monitoring for and detecting the short-circuit without the use of a shunt resistor is based on detecting “a signal waveform different from that in a normal operating state.” *Id.* at 4:17-20.

4. Operation of the alleged invention to protect against short-circuits.

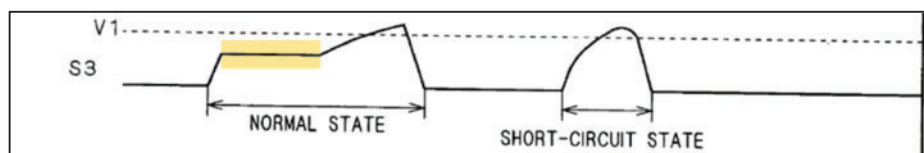
In the context of Figure 5, the '835 patent describes how to detect the abnormal waveform that is indicative of a short-circuit in the Figure 2 embodiment.



Id. at Fig. 5. In Figure 5, consistent with Figure 2, the line S1 is the claimed “control input signal” that is “supplied from the outside through the control signal input terminal U_{IN} .” *Id.* at 5:55-56. The “control input signal S1” has the effect of “mak[ing] the transistor 12 be ON according to its rising and the transistor 12 maintains the ON state during a period when that control input signal S1 is in a high potential state.” *Id.* at 5:56-59. In the timing diagram in Figure 5, “control output signal S3” is “outputted from the gate driver GD [and] rises according to the building up of the control input signal S1.” *Id.* at 5:60-62. The '835 patent explains that when “a voltage of the control output signal S3 exceeds a threshold value of the transistor 12, the transistor 12 comes to be in ON state.” *Id.* at 5:60-65. As described above, when a certain voltage is applied to the gate of an insulated gate transistor, current begins to flow. *See id.* at

5:65-66 (“ . . . the transistor 12 comes to be in ON state, and a collector-emitter voltage of the transistor 12 drops,” causing current to flow).

In this normal operation, the “control output signal S3 is clamped to a certain voltage for a determined period by a [Miller]¹ effect” (*see* ’835 patent at 5:67-6:1; Japanese Priority Patent Applications JP 2004-001057 and JP 2004-262033 at [050]). The portion of control output signal S3 that is “clamped to a certain voltage for a determined period by a [Miller] effect” is reflected in the portion of Figure 5 annotated in gold below:



Id. at Fig. 5 (annotation added as described in text above). The patent explains that when transistor 12 “normally operates,” “the transistor 12 which is the insulated gate type switching device such as the IGBT and so on has a characteristic that its control output signal S3 is clamped to a certain voltage for the determined period after its rising.” *Id.* at 6:6-10. In contrast, when a short-circuit occurs, “a clamp period of the voltage does not exist in the control output signal S3, and the voltage of the control output signal S3 rises rapidly to be almost equal to that of the drive voltage VCC,” as reflected in Figure 5. *Id.* at 6:54-64. In both the “normal state” and “short-circuit state,” however, the voltage of the control output signal S3 eventually exceeds a reference voltage V1; thus, the timing of when the voltage exceeds V1 is how the alleged invention determines whether the transistor is operating normally or has experienced a short-circuit.

¹ The specification reads “mirror effect,” but this is likely a mistranslation of the original Japanese patent application which reads “Miller effect.” The Miller effect is well-known by persons of skill in the art. *See* **Section V.F.**, below.

The '835 patent accounts for this timing by generating pulse signals at specific times during operation of the circuit (seen in Figure 5 as signals S2, S4 and S5), allowing the circuit to determine a short-circuit based on the generation of concurrent pulses. The patent explains that signal S2 is output by “the one-shot pulse generation circuit 1,” and that signal S2 is set to a high state for approximately the same duration as the time when the control output signal S3 is clamped to a certain voltage (annotated in gold in Figure 5 above). *Id.* at 6:35-49. In other words, signal S2 is approximated and set to account for the duration when the control output signal S3 will clamp to a certain voltage for a duration, as shown in “normal state” operation in Figure 5. *Id.* The patent further explains that “the control output signal S3 is supplied to the comparator 2, too, and compared with the reference voltage V1, and the comparator 2 makes the comparison result signal S4 which is the output of the comparator 2 be in a significant condition and a high potential ‘H’ state in this case, when the voltage of the control output signal S3 exceeds the reference voltage V1.” *Id.* at 6:11-26. Thus, signal S4 in Figure 5 shows a “high potential ‘H’ state” when control output signal S3 exceeds the reference voltage V1. *Id.* at 6:15.

In the Figure 2 embodiment, if both signals S2 and S4 are in a “high potential” state simultaneously, then signal S5 will also be in a “high potential” state, indicating a short-circuit state. *Id.* at 6:41-49; 6:65-7:21; Fig. 5. In a short-circuit state, the signal S5 is supplied to the “RS flip-flop circuit 3,” the result of which is that “the control output signal S3 is forced to stop” and “the transistor 12 is forced to be in OFF state.” *Id.* at 7:4-29. Thus, by monitoring the waveforms and the timing of the signals, the '835 patent claims that “it is not necessary for the inverter module 100 to set the shunt resistor outside of the package PG (FIG. 1), differing from the conventional IPM.” *Id.* at 7:23-31.

IV. PERSON OF ORDINARY SKILL IN THE ART

Respondents propose that a person of ordinary skill in the art would have had a graduate degree in electrical engineering, or at least a Bachelor of Science in electrical engineering or a similar discipline and at least two years of relevant work experience.

V. DISPUTED CLAIM TERMS

Eleven claim terms are in dispute. As set forth in the Joint Claim Construction Chart, the Parties jointly identified eight of these terms to be addressed in the *Markman* process.

Respondents have organized the brief by term in the order of the Joint Claim Construction Chart and listed the specific claim(s) in which the terms appear.

A. Preamble (claim 1)

Complainant's Proposed Construction	Respondents' Proposed Construction	Staff's Proposed Construction
Non-limiting preamble	The preamble is limiting.	The preamble is limiting.

Respondents and Staff agree the preamble is limiting. The preamble is limiting because it (1) recites essential structure, including by providing antecedent basis for several terms in the body of the claim, and (2) is necessary to give life, meaning, and vitality to the claim as a whole.

Preambles are construed in the same manner as other claim language. *Bell Commc'ns Research, Inc. v. Vitalink Commc'ns Corp.*, 55 F.3d 615, 620 (Fed. Cir. 1995). “[W]hether to treat a preamble as a claim limitation is determined on the facts of each case in light of the claim as a whole and the invention described in the patent.” *Bicon, Inc. v. Straumann Co.*, 441 F.3d 945, 952 (Fed. Cir. 2006). The “preamble is regarded as limiting if it recites essential structure that is important to the invention or necessary to give meaning to the claim.” *Id.* That is, “if the claim drafter chooses to use both the preamble and the body to define the subject matter of the claimed invention, the invention so defined, and not some other, is the one the patent protects.” *Id.* (internal quotation marks omitted). The Federal Circuit has “repeatedly held a preamble

limiting when it serves as antecedent basis for a term appearing in the body of a claim.” *In re Fought*, 941 F.3d 1175, 1178 (Fed. Cir. 2019); *Pacing Techs., LLC v. Garmin Int’l, Inc.*, 778 F.3d 1021, 1024 (Fed. Cir. 2015). Likewise, “if the preamble is ‘necessary to give life, meaning, and vitality’ to the claim, then the preamble is limiting.” *Certain Solid State Storage Drives, Stacked Elecs. Components, & Prod. Containing Same*, Inv. No. 337-TA-1097, Ord. No. 31, 2019, WL 2353508, at *12-13 (Mar. 26, 2019) (quoting *Allen Eng’g Corp. v. Bartell Indus.*, 299 F.3d 1336, 1436 (Fed. Cir. 2002)); *Proveris Sci. Corp. v. Innovasystems, Inc.*, 739 F.3d 1367, 1372 (Fed. Cir. 2014); *Pitney Bowes, Inc. v. Hewlett-Packard Co.*, 182 F.3d 1298, 1305 (Fed. Cir. 1999).

Here, the ALJ should find the preamble of claim 1 limiting because it both provides an antecedent basis and gives life and meaning to the claim, as Respondents and Staff propose.

1. The preamble provides antecedent basis for terms in the claim body.

The preamble is limiting because it provides antecedent basis for several terms in the body of the claim. Courts routinely find preambles limiting “[w]hen limitations in the body of the claim rely upon and derive antecedent basis from the preamble.” *Pacing Techs.*, 778 F.3d at 1024 (quoting *Eaton Corp. v. Rockwell Int’l Corp.*, 323 F.3d 1332, 1339 (Fed. Cir. 2003) (internal quotation marks omitted)). The fact that a preamble provides antecedent basis “is a strong indication that the preamble acts as a necessary component of the claimed invention.” *Bio-Rad Labs., Inc. v. 10X Genomics Inc.*, 967 F.3d 1353, 1370-72 (Fed. Cir. 2020) (quoting *Eaton Corp. v. Rockwell Int’l Corp.*, 323 F.3d 1332, 1339 (Fed. Cir. 2003) (internal quotation marks omitted)). For example, the Federal Circuit in *Pacing* found the preamble “[a] repetitive motion pacing system for pacing a user” was limiting because the term “a user” in the preamble provided the antecedent basis for the term “the user” in the claim’s body. *See Pacing Techs.*, 778 F.3d at 1022,

1024. The court reached the same conclusion in *Pitney Bowes*, finding that because the term “generated shapes” “first appear[ed] in the claim body” as “the generated shapes, ... the term can only be understood in the context of the preamble statement ‘producing on a photoreceptor an image of generated shapes.’” *Pitney Bowes*, 182 F.3d at 1306 (emphasis added); *see also Certain Mobile Tel. Handsets, Wireless Commun. Devices, and Components Thereof*, Inv. No. 337-TA-578, Comm’n Det., 2010 WL 1436458, at *18 (Mar. 1, 2010) (finding preamble limiting because it provided antecedent basis); *Bicon, Inc. v. Straumann Co.*, 441 F.3d 945, 953 (Fed. Cir. 2006) (same). In *Certain Power Inverters* (Inv. No. 1267), the ALJ likewise found a preamble limiting for providing antecedent basis. *Certain Power Inverters & Converters, Vehicles Containing the Same, & Components Thereof*, Inv. No. 337-TA-1267, at 32 (Jan. 18, 2022).

Here, the preamble provides antecedent basis for the terms “insulated gate transistor,” “control output signal,” and “control input signal,” as shown color-coded below.

1. A semiconductor device controlling a drive of **an insulated gate transistor** by generating **a control output signal** on a basis of **a control input signal**, comprising:
 - 1[a] a driver outputting **said control output signal** and
 - 1[b] a short-circuit protection circuit detecting **said control output signal** and controlling and forcing said driver to stop **said control output signal** when a detecting voltage of **said control output signal** exceeds a predetermined reference voltage before a predetermined period passes after **said control output signal** indicates a conduction of **said insulated gate transistor**, wherein
 - 1[c] said short-circuit protection circuit includes:
 - 1[d] pulse generation circuit receiving **said control input signal** and outputting a first pulse signal being significant only in said predetermined period according to a timing when **said control input signal** indicates the conduction of **said insulated gate transistor**;
 - 1[e] a comparator receiving the detecting voltage of **said control output signal**, performing a comparison with said reference voltage and outputting a second pulse signal being significant during a period when the detecting voltage of **said control output signal** exceeds said reference voltage; and
 - 1[f] a logical circuit receiving said first and second pulse signals and outputting a stop signal forcing said driver to stop **said control output signal** when said second pulse signal becomes significant during a period when said first pulse signal is significant.

2. The semiconductor device according to claim 1, wherein said predetermined period when said first pulse signal is significant is set on a basis of a period when a voltage of **said control output signal** is clamped constantly when **said insulated gate transistor** normally operates.

'835 patent at claims 1 and 2 (annotations added).

Each of these terms are preceded in the claim body by the term “said,” which means “aforementioned” and “refer[s] to something mentioned earlier.” *T D X Energy, L.L.C. v. Chesapeake Operating, Inc.*, 857 F.3d 253, 261 (5th Cir. 2017); *c.f.* M.P.E.P. § 2173.05(e), “Lack of Antecedent Basis” (“The lack of clarity could arise where a claim refers to ‘said lever’ or ‘the lever,’ where the claim contains no earlier recitation or limitation of a lever...”). The preamble thus introduces and provides context for each instance of these terms in the claim body. *T D X Energy*, 857 F.3d at 261. Moreover, these are not minor elements that may have been underappreciated or overlooked, as shown by the frequency with which these terms appear. The terms are critical to both the structure and function of the alleged invention. Because the preamble provides antecedent basis, “it is apparent that the claim drafter chose to use both the preamble and the body of the claim to define the subject matter of the claimed invention.” *Bicon, Inc. v. Straumann Co.*, 441 F.3d 945, 953 (Fed. Cir. 2006). The preamble should thus be found limiting on this basis alone.

2. The preamble recites essential aspects of the alleged invention and gives life, meaning and vitality to the claim.

The preamble is also limiting because it (1) recites essential aspects of the alleged invention, and (2) gives life and meaning to the claims by providing information essential to understanding certain terms in the body of the claim.

First, the preamble should be construed as limiting because it recites essential aspects of the alleged invention, namely that the alleged invention (1) controls a drive of an insulated gate

transistor, and (2) does so by generating a control output signal on a basis of a control input signal. A preamble is limiting when it provides more than “simply an introduction to the general field of the claim,” but rather recites “necessary and defining aspects of the invention.”

Computer Docking Station Corp. v. Dell, Inc., 519 F.3d 1366, 1375, 86 U.S.P.Q.2d 1129, 1134 (Fed. Cir. 2008). In *Proveris*, the Federal Circuit found a preamble limiting where it “recite[d] particular structure or steps that are highlighted as important by the specification.” *Proveris*, 739 F.3d at 1372. In particular, that preamble related to a “sequential set of images of a spray plume” and “a predetermined instant in time.” *Id.* at 1372-73. As the court found, although the specification described the invention in those terms, “the preamble of claim 3 is the only reference in any independent claim to the inventive concept of capturing a sequence of images in order to characterize the time evolution of the spray plume. This fact alone is likely sufficient to support a conclusion that the preamble is limiting.” *Id.* at 1373; *see also On Demand Mach. Corp. v. Ingram Indus.*, 442 F.3d 1331, 1343 (Fed. Cir. 2006).

Further, in *Nintendo*, the Federal Circuit found limiting a preamble for “[a] system for displaying a pattern on a raster scanned display device by mapping bits from a display location in a memory associated with a computer onto the raster.” *Gen. Elec. Co. v. Nintendo Co.*, 179 F.3d 1350, 1361-62 (Fed. Cir. 1999). The court reasoned:

[T]he . . . specification makes clear that the inventors were working on the particular problem of displaying binary data on a raster scan display device and not general improvements to all display systems. In light of the specification, to read the claim indiscriminately to cover all types of display systems would be divorced from reality. The invention so described is restricted to those display devices that work by displaying bits, which is not true with respect to all display systems recited in just the body of the claim.

Id.; see also *Certain Power Inverters & Converters, Vehicles Containing the Same, & Components Thereof*, Inv. No. 337-TA-1267, at 33-34 (Jan. 18, 2022) (finding preamble limiting because it recited features the specification highlighted as important).

Here, the '835 patent specification confirms that the preamble recites part of the invention: “[a]n aspect of a semiconductor device according to the present invention is that a semiconductor device controls a drive of an insulated gate transistor by generating a control output signal on a basis of a control input signal.” ’835 patent at 1:52-55; see also *Verizon Servs. v. Vonage Holdings*, 503 F.3d 1295, 1308 (Fed. Cir. 2007) (“When a patent thus describes the features of the ‘present invention’ as a whole, this description limits the scope of the invention.”) (citations omitted). Further, as explained in Section V.C below, the parties agree that “controlling a drive of” an insulated gate transistor refers to controlling the control output signal at the gate of the insulated gate transistor. The specification repeatedly describes that concept in relation to the preferred embodiments. *Id.* at 3:3-6 (“The inverter module 100 has a composition that a control output signal is supplied to respective gate electrodes of the transistors 11, 21 and 31 from respective control signal output terminals.”) (emphasis added); 3:36-39 (“The inverter module 100 has a composition that a control output signal is supplied to respective gate electrodes of the transistors 12, 22 and 32 from control signal output terminals”) (emphasis added); 4:14-16 (“As shown in FIG. 2, the control output signal is supplied to the gate electrode of the transistor 12 from the control signal output terminal”) (emphasis added); 4:28-33 (“an output signal of a gate driver GD . . . is supplied as a control output signal S3 to the gate electrode of the transistor 12”) (emphasis added). In view of the specification, “controlling a drive of an insulated gate transistor” is a key aspect of the claimed invention, and this language appears in the preamble of claim 1.

Moreover, all eight claims in the '835 patent recite a similar limitation directed to “controlling a drive” of an insulated gate transistor—some of them in the body of the claim when directed to controlling the drive of two insulated gate transistors. *Id.* at 11:38-14:20; *see, e.g., id.* at claim 3. There can be little doubt “that the inventor considered that [such] preamble language represented an important characteristic of the claimed invention.” *Poly-Am., L.P. v. GSE Lining Tech., Inc.*, 383 F.3d 1303, 1310 (Fed. Cir. 2004). Indeed, Arigna itself describes this concept as central to the purported invention. In its Complaint in this investigation, Arigna explained that “[t]he patent describes a novel IPM (Intelligent Power Module) package which consists of a semiconductor device having an insulated gate type switching device, such as an IGBT (Insulated Gate Bipolar Transistor), and a control circuit controlling the drive of that switching device.” Complaint, ¶¶ 40, 42 (emphasis added).

Second, the preamble should be construed as limiting because it provides information essential to understand the relationship between the control output signal and control input signal. Courts have found that a preamble gives life and meaning to a claim where the preamble is essential to understand associations between terms recited in the body of the claim. For example, in *Pitney Bowes*, the preamble recited an “[a]pparatus for producing on a photoreceptor an image of generated shapes made up of spots” and the claim body recited “directing a plurality of beams of light towards a photoreceptor, each beam of light generating a spot on the photoreceptor and controlling a parameter of the light beams to produce spots of different sizes whereby the appearance of smoothed edges are given to the generated shapes.” *Pitney Bowes*, 182 F.3d at 1302 (emphasis added). The Federal Circuit found it “is only discernible from the claim preamble” that the “claim term ‘spots’ refers to the components that together make up the images of generated shapes on the photoreceptor.” *Id.* at 1306. Because only the preamble

described the relationship between “spots” and “generated shapes,” the Federal Circuit found the preamble “necessary to give life, meaning, and vitality to the claim” and was thus limiting. *Id.*

The Federal Circuit similarly found the preamble limiting in *Unwired Planet*. There, the preamble stated “[a] method for recursively displaying on a screen of a mobile device an image having dimensions much larger than the dimension of the screen,” and the claim body recited “generating from the image an image hierarchy starting with a reduced image” and “forwarding the reduced image to the mobile device for display.” *Unwired Planet L.L.C. v. Google, Inc.*, 660 F. App’x 974, 985-86 (Fed. Cir. 2016) (nonprecedential) (emphasis added). The court found the preamble essential to understanding the relationship between terms in the claim body because, “absent the [preamble], [the] claims fail to indicate that the image hierarchy—or the reduced image that it starts with—is a smaller version of the image, or that the image had been reduced in size according to the mobile device’s screen.” *Id.* at 986 (internal quotation marks omitted). That is, the preamble was limiting because it is “essential to understand limitations or terms in the claim body—namely, the size difference between an image and the screen of a mobile device.” *Id.* (internal quotation marks omitted); *see also Certain Power Inverters & Converters, Vehicles Containing the Same, & Components Thereof*, Inv. No. 337-TA-1267, at 33-34 (Jan. 18, 2022) (finding preamble limiting because it “provides guidance as to the meaning of ‘offset’ in the body of the claim”).

Here, the body of the claim recites a “control output signal” and a “control input signal,” but does not describe any relationship between them. That relationship is “only discernible from the claim preamble,” which explains that a control output signal is generated “on a basis of a control input signal.” “Without the preamble term, there is no requirement” in the claim body that the control output signal is generated on a basis of the control input signal. *Unwired Planet*,

660 F. App'x at 986; *see also Pitney Bowes*, 182 F.3d at 1306. The preamble should thus be found limiting.

B. “insulated gate transistor” (claims 1 and 2)

Complainant’s Proposed Construction	Respondents’ Proposed Construction	Staff’s Proposed Construction
a transistor whose gate is electrically insulated from the channel	Plain meaning, i.e. IGBT (insulated gate bipolar transistor)	a transistor whose gate is electrically insulated from the channel

The plain and ordinary meaning of “insulated gate transistor” is an insulated gate bipolar transistor (IGBT). To determine the meaning of “terms that have a particular meaning in a field of art,” courts look to “what a person of skill in the art would have understood disputed claim language to mean,” including by examining “the words of the claims themselves, the remainder of the specification, the prosecution history, and extrinsic evidence concerning relevant scientific principles, the meaning of technical terms, and the state of the art.” *Phillips*, 415 F.3d at 1314.

The insulated gate transistor, or IGBT, was created in the early 1980s. The “initial name of IGBT was Insulated Gate Transistor (IGT),” and the bipolar nature of such devices was a critical feature of the design of the IGT. Ex. 1

(<https://www.electricalvolt.com/2022/05/insulated-gate-bipolar-transistor-its-working/>); Ex. 2, B.J. Baliga, *Fast-Switching Insulated Gate Transistors*, IEEE ELECTRON DEVICE LETTERS, Vol. EDL-4, No. 12 (Dec. 1983) (“Developed by the integration of MOS and bipolar technologies, insulated gate transistors (IGT’s) represent a new class of semiconductor power-switching devices”); Ex. 3, H. Yilmaz, *Insulated Gate Transistor Modeling and Optimization*, 1984 INTERNATIONAL ELECTRON DEVICES MEETING (Dec. 1984) (“The Insulated Gate Transistor (IGT) is a new power switching device . . . [that] is modeled as a Bipolar Junction Transistor (BJT) driven by a MOSFET.”); Ex. 4, B.J. Baliga, et al., *The Insulated Gate Transistor: A New*

Three-Terminal MOS-Controlled Bipolar Power Device, IEEE TRANSACTIONS ON ELECTRON DEVICES, Vol. ED-31, No. 6, June 1984 (“A new three-terminal power device, called the insulated gate transistor (IGT), with voltage-controlled output characteristics is described. In this device, the best features of the existing families of bipolar devices and power MOSFET’s are combined to achieve optimal device characteristics.”); Ex. 5, *Using SPICE For The Modelization Of The Static Behaviour* (the IGT is a “complex bipolar device”). The name “insulated gate transistor” was meant to distinguish the device from other transistors, such as MOSFETs and BJTs. *Id.*

By the late 1980s, the insulated gate transistor was referred to as Insulated Gate Bipolar Transistors (IGBTs). Ex. 6, *Insulated Gate Bipolar Transistor (IGBT) With A Trench Gate*. Since then, such devices have been commonly referred to by several names, including both “IGBT” and “insulated gate transistor (IGT).” Ex. 7, (<https://www.sciencedirect.com/topics/engineering/insulated-gate-bipolar-transistor>); Ex. 8, (<https://components101.com/articles/what-is-igbt-working-operation-symbol-and-types>) (“The different names of IGBT are Insulated Gate Transistor (IGT), Metal Oxide Insulated Gate Transistor (MOSIGT), Gain Modulated Field Effect Transistor (GEMFET), Conductively Modulated Field Effect Transistor (COMFET).”); Ex. 9, (https://www.electronics-notes.com/articles/electronic_components/fet-field-effect-transistor/what-is-igbt-insulated-gate-bipolar-transistor.php) (“The IGBT has also been referred to by several other names including: an IGT: insulated gate transistor, IGR: insulated gate rectifier, COMFET: conductivity modulated field effect transistor, GEMFET: gain enhanced MOSFET, BiFET: bipolar FET, and injector FET.”). Critically, though IGBTs are referred to by many names (including IGT), the inverse is not true—IGT is used singularly to refer to IGBTs. Stated differently, referring to

IGBTs using different names does not, by extension, imply that IGT can refer to multiple types of transistors.

The specification of the '835 patent likewise equates the term “insulated gate transistor” with an IGBT. The Federal Circuit has consistently clarified patent terms based on the specification where the patent’s specification “repeatedly, consistently, and exclusively” disclosed the invention in a specific way. *Groove Digital, Inc. v. United Bank*, 825 F. App’x 852, 856 (Fed. Cir. 2020) (unpublished) (quoting *In re Abbott Diabetes Care Inc.*, 696 F.3d 1142, 1150 (Fed. Cir. 2012)); *see also Poly-Am., L.P. v. API Indus., Inc.*, 839 F.3d 1131, 1137 (Fed. Cir. 2016) (same); *Profectus Tech. LLC v. Huawei Techs. Co.*, 823 F.3d 1375, 1380-81 (Fed. Cir. 2016) (same); *In re Abbott Diabetes Care Inc.*, 696 F.3d 1142, 1148-50 (Fed. Cir. 2012) (same). The only place in the specification that describes or depicts what the applicant meant by the term “insulated gate transistor” discloses that an “insulated gate transistor” is an IGBT. *See* '835 patent at 4:8-33; 11:28-31. For example, the specification explains that the insulated gate transistor is transistor 12 in Figure 2:

As shown in FIG. 2, the control output signal is supplied to the gate electrode of the transistor 12 from the control signal output terminal UOUT of the control device LIC, however, with regard to the insulated gate transistor, the control output signal is also influenced when that transistor is short-circuited, and a signal waveform different from that in a normal operating state occurs.

'835 patent at 4:14-20 (emphasis added). There is no dispute that transistor 12 is an IGBT. *See*, e.g., Ex. 10 (Difference between IGBT and MOSFET, <https://www.tutorialspoint.com/difference-between-igbt-and-mosfet> (last visited 8/5/2022)).

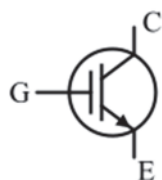
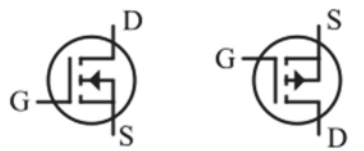
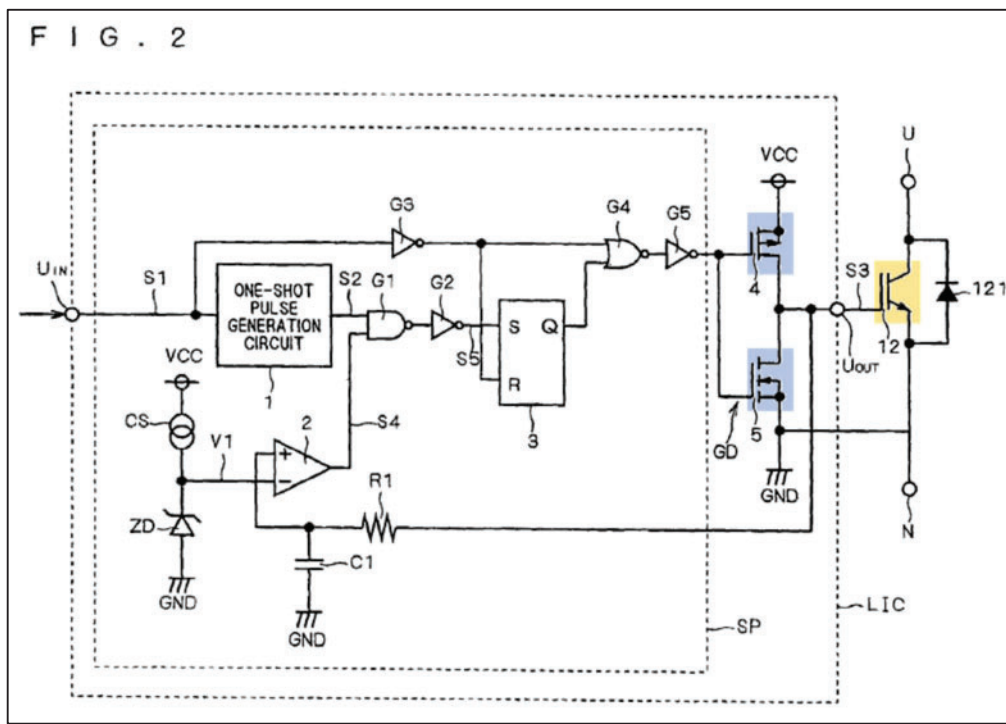


Figure 1 - IGBT



N-Channel
Figure 2 - MOSFET
P-Channel

Id. The '835 patent consistently uses the common and widely accepted symbol in the art to refer to the IGBT (annotated in gold below):



Id. at Fig. 2 (annotations added); *see also id.* at FIG. 6. The patent likewise refers to “the insulated gate transistors 11, 12, 21, 22, 31 and 32,” which are also all IGBTs. *Id.*, at 11:28-31, FIGS. 1, 2, 6.

Moreover, the specification never describes or implies that an “insulated gate transistor” is something other than an IGBT. Indeed, the specification discloses other types of transistors, such as “MOS transistor[s]” (labeled 4 and 5 in Figure 2, annotated in blue above), but never describes those MOS transistors as insulated gate transistors. The patentee understood that IGBTs and MOS transistors are different, and specifically chose to use MOS transistors as part of the “gate driver GD” circuit to control the drive of transistor 12, which is represented by the specific symbol for an IGBT. *See* '835 patent at 4:14-42. While the '835 patent discloses both

MOS transistors and IGBTs, it consistently identifies only the IGBTs as examples of “insulated gate transistors.” *Id.* at 4:14-20, 11:28-31.

Complainant and Staff seek to broaden the meaning of “insulated gate transistor” to mean any insulated gate type switching device. As described in the specification, the inventor seemed to believe other insulated gate type switching devices existed beyond the insulated gate transistor. But critically, the applicant failed to seek claims directed to such devices. The specification explains that the alleged invention “relates to a semiconductor device and a semiconductor device module including a short-circuit protection function of an insulated gate type switching device such as an IGBT (Insulated Gate Bipolar Transistor) and so on.” *Id.* at 1:10-15 (emphasis added). Similarly, the specification describes “the transistor 12 which is the insulated gate type switching device such as the IGBT and so on.” *Id.* at 6:6-7 (emphasis added). While such disclosures may have supported a broader claim directed to an “insulated gate type switching device,” the applicant did not seek or receive such broad claims, instead opting to claim only the narrower “insulated gate transistor.” The applicant clearly knew how to use broader terminology but chose not to do so. The ALJ should construe the term “insulated gate transistor” according to its plain meaning in view of the intrinsic evidence: an IGBT.

C. “controlling a drive of an insulated gate transistor” (claim 1)

Complainant’s Proposed Construction	Respondents’ Proposed Construction	Staff’s Proposed Construction
Non-limiting preamble Alternatively, plain and ordinary meaning, e.g., controlling the signal applied to the gate of an insulated gate transistor	controlling the voltage supplied to the gate of an insulated gate transistor to switch the transistor between ON and OFF states	controlling the voltage supplied to the gate of an insulated gate transistor to switch the transistor between ON and OFF states

The term “controlling a drive of an insulated gate transistor” appears in the preamble² of claim 1. Respondents and Staff agree that the term should be construed to mean “controlling the voltage supplied to the gate of an insulated gate transistor to switch the transistor between ON and OFF states.” If the preamble is found to be limiting, Arigna proposes that the term should be construed as “plain and ordinary meaning, e.g., controlling the signal applied to the gate of an insulated gate transistor.” Thus, there is no dispute that the construction of “controlling a drive of an insulated gate transistor” must include, at least, “the gate of an insulated gate transistor.”

On its face, Arigna’s construction appears somewhat close to Respondents’ and Staff’s proposed construction, but three key disputes remain. One, whether to include the open-ended phrase “plain and ordinary meaning, e.g.” (Arigna’s position). Two, whether “controlling a drive of an insulated gate transistor” requires “controlling the voltage supplied” (Respondents’ and Staff’s position) or “controlling the signal applied” (Arigna’s position) to the gate of an insulated gate transistor. Three, whether to include “to switch the transistor between ON and OFF states” (Respondents’ and Staff’s position). The intrinsic evidence confirms Respondents’ and Staff’s construction on all three points of dispute, and Arigna’s overly broad, open-ended construction should be rejected.

First, Respondents’ and Staff’s construction, which reflects the plain and ordinary meaning of “controlling a drive of an insulated gate transistor” in view of the intrinsic evidence, will resolve the parties’ dispute over claim construction. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312 (Fed. Cir. 2005) (en banc), quoting *Multiform Desiccants, Inc. v. Medzam, Ltd.*, 133 F.3d 1473, 1477 (Fed. Cir. 1998) (“The best source for understanding a technical term is the

² Respondents and Staff contend that the preamble of claim 1 is limiting. See **Section V.A.**, *supra*.

specification from which it arose . . . ”). Arigna’s construction will not resolve the dispute, because Arigna explains its purported plain and ordinary meaning using “e.g.” (shortened form of Latin *exempli gratia*, or “for example”) instead of “i.e.” (shortened form of Latin *id est*, or “that is”). By using “e.g.,” Arigna leaves its construction open-ended, ostensibly to preserve its ability to later argue that some other, different, and not-yet-disclosed examples reflect the plain meaning of the term. The inclusion of “e.g.” leaves the construction broadly unrestricted and is contrary to “[t]he purpose of claim construction,” which is “to ‘determin[e] the meaning and scope of the patent claims asserted to be infringed.’” *See O2 Micro Int’l Ltd. v. Beyond Innovation Tech. Co.*, 521 F.3d 1351, 1360 (Fed. Cir. 2008) (citing *Markman v. Westview Instruments, Inc.*, 52 F.3d 967, 976 (Fed. Cir. 1995) (en banc), *aff’d*, 517 U.S. 370 (1996)). Although “a sound claim construction need not always purge every shred of ambiguity,” it should “resolve a dispute about claim scope that has been raised by the parties” consistent with *O2 Micro*. *See Eon Corp. IP Holdings*, 815 F.3d at 1318-19 (quotation omitted; citing *O2 Micro*, 512 F.3d at 1360). Because Arigna’s inclusion of “e.g.” in its proposed construction fails to crystalize the meaning and scope of the asserted claims or to resolve the parties’ dispute about claim scope, the ALJ should reject it.

Second, the intrinsic evidence confirms that the voltage of a signal—not just a signal—is supplied to the gate of an insulated gate transistor to control the drive of the transistor. The ’835 patent explains: “[a]s shown in FIG. 2, the control output signal is supplied to the gate electrode of the transistor 12,” and “when a voltage of the control output signal S3 exceeds a threshold value of the transistor 12, the transistor 12 comes to be in ON state.” ’835 patent at 4:14-20; 4:27-38; 5:62-6:5. Thus, while the control output signal is supplied to the transistor’s gate, it is the voltage of the control output signal that controls the gate. When the voltage of the control

output signal switches the transistor to the ON state, “a voltage of the control output signal S3 is clamped to a certain voltage for a determined period” and “the voltage of the control output signal S3 rises to be a value almost equal to the drive Voltage VCC of the gate driver GD.” *Id.* The ’835 patent also explains that it is the voltage of the control output signal that is compared to a reference voltage during a set time period to determine whether a short-circuit has occurred, and if not, “the ON state in the transistor 12 is maintained.” *See, e.g., id.* at 6:47-53; 6:54-62, 10:45-52. Claim 1 further confirms that the voltage of the control output signal is the relevant value: “outputting a second pulse signal being significant during a period when the detecting voltage of said control output signal exceeds said reference voltage.” *Id.* at Claim 1. The specification confirms that it is the voltage of the control output signal that “control[s] [the] drive of an insulated gate transistor,” and not simply a signal more broadly, as Arigna’s construction asserts. Respondents’ and Staff’s construction more accurately reflects the disclosures of the intrinsic evidence.

Third, “controlling a drive of an insulated gate transistor” requires that the voltage supplied to the gate of the transistor is capable of switching the transistor between ON and OFF states, as reflected in Respondents’ and Staff’s construction. Merely supplying some voltage (or signal, as Arigna contends) to the gate of the transistor is not enough to “control[] the drive” of the transistor—rather, as the patent teaches, the voltage supplied to the gate must “exceed[] a threshold value of the transistor 12” so that “the transistor 12 comes to be in the ON state.” ’835 patent at 5:62-6:5. Conversely, when “[the voltage of the control output signal S3] falls according to a trailing edge of the control input signal S1,” then it “makes the transistor 12 be OFF.” *Id.* If “the control output signal S3 is maintained,” then “the ON state in the transistor 12 is maintained.” *Id.* at 6:47-53. Similarly, if the voltage supplied does not exceed the transistor’s

threshold value, the transistor remains in the OFF state, and the drive of the transistor is not controlled, as claimed. The ability to “switch the transistor between ON and OFF states” is also critical to the purpose of the alleged invention, which is to provide “a short-circuit protection function” for “an insulated gate type switching device.” *Id.* at 1:13-14. In the event of a short-circuit, the claimed semiconductor device must be able to force the transistor to an OFF state via the control output signal. *See, e.g., id.* at 6:54-62, 7:13-21, 10:35-43, 10:45-61. Thus, the ALJ also should adopt Respondents’ and Staff’s construction because it accurately captures that “to switch the transistor between ON and OFF states” is a crucial aspect of “controlling a drive of an insulated gate transistor.”

D. “indicates a conduction of said insulated gate transistor” (claim 1)

Complainant’s Proposed Construction	Respondents’ Proposed Construction	Staff’s Proposed Construction
Plain and ordinary meaning, e.g., indicates that said insulated gate transistor is turned on	indicates that said insulated gate transistor is in the ON state	indicates that said insulated gate transistor is in the ON state

Respondents and Staff agree that the term “indicates a conduction of said insulated gate transistor” should mean “indicates that said insulated gate transistor is in the ON state.” Arigna’s construction differs from Respondents’ and Staff’s construction in two ways: (1) it includes the phrase “[p]lain and ordinary meaning, e.g.,” and (2) uses the phrase “is turned on” instead of “is in the ON state.” As discussed above, Arigna’s use of “plain and ordinary meaning, e.g.,” in several proposals improperly leaves its constructions open-ended and fails to crystallize the scope of the asserted claims. *See O2 Micro*, 521 F.3d at 1360. Arigna’s proposal should be rejected for this reason alone. In addition, Respondents’ and Staff’s construction more accurately captures the plain meaning of “indicates a conduction of said insulated gate transistor,” and provides needed clarity to the meaning and scope of the term.

With respect to the second variance between the parties’ constructions—“is in the ON state” versus “is turned on”—Arigna inexplicably attempts to distance its proposed construction from the express disclosures of the intrinsic evidence, and fails to explain any basis for its distinction. Arigna has not yet explained why “is turned on” is more correct or what material difference exists from “ON state.” Regardless, “ON state” is the terminology used by the patent specification, and thus, Respondents’ and Staff’s construction more accurately reflects the intrinsic record. The specification explains: “when a voltage of the control output signal S3 exceeds a threshold value of the transistor 12, the transistor 12 comes to be in ON state, and a collector-emitter voltage of the transistor 12 drops.” ’835 patent at 5:62-6:5 (emphasis added). When the transistor is in the ON state, the voltage drop between the collector and emitter in the transistor causes current to flow through the transistor between the collector and emitter—*i.e.*, the transistor begins conducting. *Id.* Thus, the specification teaches that when the transistor is in the ON state, it “indicates a conduction of said insulated gate transistor,” consistent with Respondents’ and Staff’s construction.

E. “significant” (claims 1 and 2)

Complainant’s Proposed Construction	Respondents’ Proposed Construction	Staff’s Proposed Construction
Plain and ordinary meaning, <i>e.g.</i> active	Plain meaning, <i>i.e.</i> large or important enough to have a meaningful effect, <i>e.g.</i> a HIGH potential state	active-high or active-low state indicating a condition is met

The plain and ordinary meaning of “significant” with respect to signals in an integrated circuit is well-known and also informed by the intrinsic evidence, including the surrounding claim language and specification. Staff and Respondents seem to largely agree on the substance of the construction—a “significant” signal must be different from an insignificant signal and must do or indicate something as required by the claims. A “significant” signal must be “large or

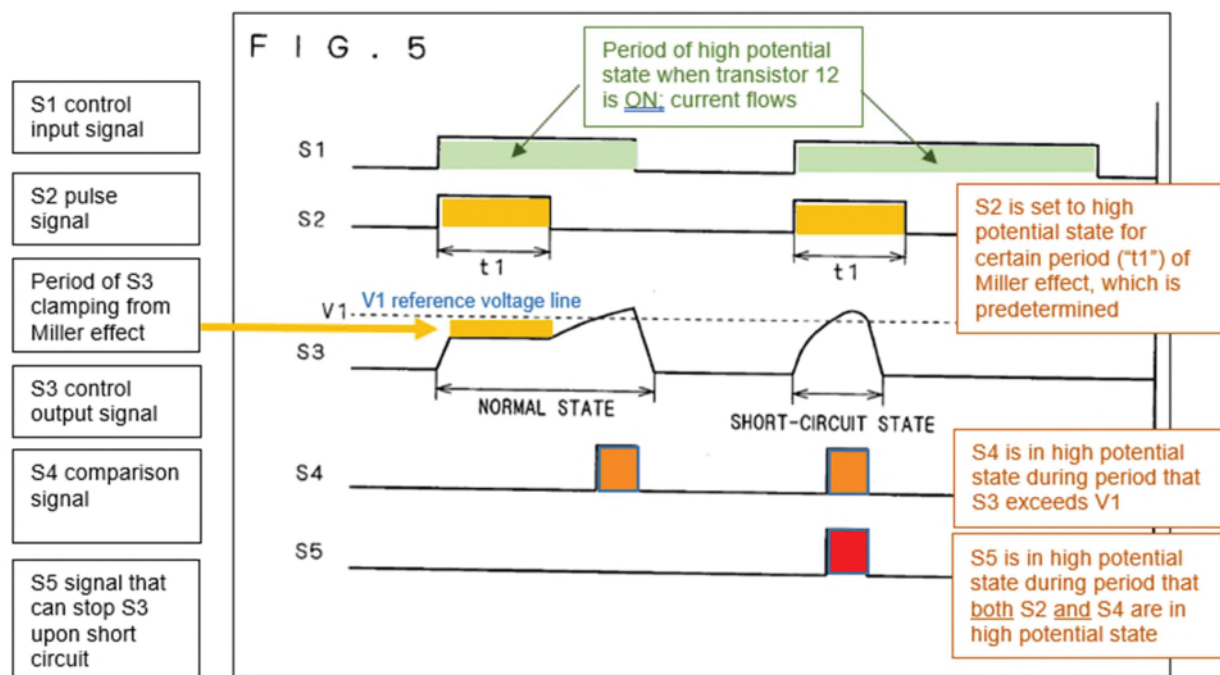
important enough to have a meaningful effect” (Respondents) or must be in a “active-high or active-low state indicating a condition is met” (Staff). By contrast, Arigna’s construction of “plain and ordinary meaning, *e.g.* active” relies entirely on a word—“active”—that does not appear in the claims or specification and would add ambiguity into the claim. Arigna’s use of “*e.g.*” in this context also leaves its construction open-ended and fails to crystallize the scope of the asserted claims. *See O2 Micro*, 521 F.3d at 1360.

The word “significant” appears multiple times in claims 1 and 2. In each instance where “significant” appears (emphasis added with underlining below), it refers to a significant condition of the claimed signal, not merely an active signal: “outputting a first pulse signal being significant in said predetermined period...” (claim 1[d]); “outputting a second pulse signal being significant during a period when the detecting voltage of said control output signal exceeds said reference voltage...” (claim 1[e]); “outputting a stop signal forcing said driver to stop said control output signal when said second pulse signal becomes significant during a period when said first pulse signal is significant” (claim 1[f]); “wherein said predetermined period when said first pulse signal is significant is set on a basis of a period when a voltage of said control output signal is clamped constantly...” (claim 2).

Figure 5, which is annotated below consistent with the description in **Section III.B.4.**, *supra*, is helpful to understand the claims. As shown, the first pulse signal S2 is significant (high) in the predetermined period [t1] set for approximately the same period the control output signal S3 is clamped during normal operation.³ *See* claims 1[b], 1[d], 2. The second pulse signal S4 is significant (high) when the control output signal S3 exceeds the reference voltage V1. *See* claim

³ Clamping due to the Miller effect is further explained in **Section V.F.**, below.

1[e]. And a “stop signal” S5 is output when S4 becomes significant (high) during a period that S2 also is significant (high)—*i.e.*, during a short circuit. See claims 1[f].



Thus, the “significant” conditions in Figure 5 are the “high potential states” shown in signal lines S1, S2, S4 and S5, above. These are the same “significant” conditions described by claim 1.

With each “significant” condition above, the signal change is “large or important enough to have a meaningful effect” as Respondents’ construction proposes: the S1 pulse has the effect of turning transistor 12 ON, the S2 pulse indicates the duration in which the normal Miller effect plateau is expected, the S4 pulse indicates when the control output signal has exceeded the reference voltage, and the S5 pulse both indicates a short-circuit has occurred and has the effect of stopping the control output signal.

Conveying some meaningful effect or intention is a critical aspect of what makes a signal pulse “significant”—not merely that it has some ill-defined “active” value. Arigna’s proposed construction completely ignores this nuance, offering only that the signal must be “e.g., active.”

Although the Staff's construction accurately captures the concept of indicating a condition, the terms "active-high" and "active-low" are not found in the patent and appear to inject additional ambiguity regarding the meaning of those terms. Respondents' construction is more clearly understood and applied in the context of the patent's intrinsic record.

Extrinsic evidence also supports Respondents' proposed construction. Oxford Dictionary defines significant as "large or important enough to have an effect or to be noticed." Ex. 11 (<https://www.oxfordlearnersdictionaries.com/us/definition/english/significant>); *see also* Ex. 20 (The New Oxford American Dictionary 1588 (2001)) ("sufficiently great or important to be worthy of attention; noteworthy"). Merriam-Webster's Collegiate Dictionary similarly defines significant as "1: having meaning; 2a: having or likely to have influence or effect." Ex. 12 (Merriam-Webster's Collegiate Dictionary 1091 (10th Ed. 1997)). The American Heritage Dictionary defines significant as "[h]aving or expressing a meaning; meaningful" or "[h]aving or likely to have a major effect; important." Ex. 13 (The American Heritage Dictionary of the English Language 1619 (4th Ed. 2000)). *See also* Ex. 21 (The Chambers Dictionary 1410 (2003)) ("having a meaning; full of meaning; important, worthy of consideration; indicative; having statistical significance"); Merriam-Webster Online (<https://www.merriam-webster.com/dictionary/significant>, last visited 8/5/2022); Cambridge Dictionary Online (<https://dictionary.cambridge.org/us/dictionary/english/significant>, last visited 8/5/2022).

Furthermore, specific to the context of the intrinsic evidence, the specification repeatedly explains that a significant condition is a high or "H" state. *See* '835 patent at 6:11-17 ("[T]he comparator 2 makes the comparison result signal S4 which is the output of the comparator 2 be in a significant condition and a high potential 'H' State in this case, when the voltage of the control output signal S3 exceeds the reference voltage V1."); *id.* at 6:35-40 ("Here, the one-shot

pulse generation circuit 1 outputs the pulse signal S2 which comes to be in the significant condition according to the building up of the control input signal S1, and a period t1 in the significant condition, in the “H” state in this case, is set to be almost equal to a period when the control output signal S3 is clamped to a certain Voltage.”); *id.* at 9:31-37 (“As shown in FIG. 8, the pulse signal S12 comes to be in the “H” state (significant condition) during a period when the level-shifted signal S11 is in the “H” state and the output signal S121 is in the “L” state... .”); *id.* at 10:21-25 (“That is to say, when the divided voltage of the control output signal S13 exceeds the reference voltage V1, the comparator 13 makes the comparison result signal S14 which is the output of the comparator 13 be in the significant condition, the ‘H’ state in this case.”); *id.* at 10:27-32 (“the pulse signal S12 is in the ‘H’ state at this time, thus the comparator 13 makes the comparison result signal S14 which is the output of the comparator 13 be in the ‘H’ state (the significant condition).”). However, Respondents’ proposed construction is not limited to a “high” or “H” potential state. For example, if the baseline of the signals above in Figure 5 was high/ON (instead of low/OFF as depicted), then the “low” or “L” OFF state could potentially be considered significant. Respondents’ proposed construction thus offers “e.g., a HIGH potential state” as an example of a significant state, and not as a narrowing limit.

For these reasons, the ALJ should adopt Respondents’ proposed construction of “significant” as “plain meaning, i.e. large or important enough to have a meaningful effect, e.g. a HIGH potential state.”

F. “clamped constantly” (claim 2)

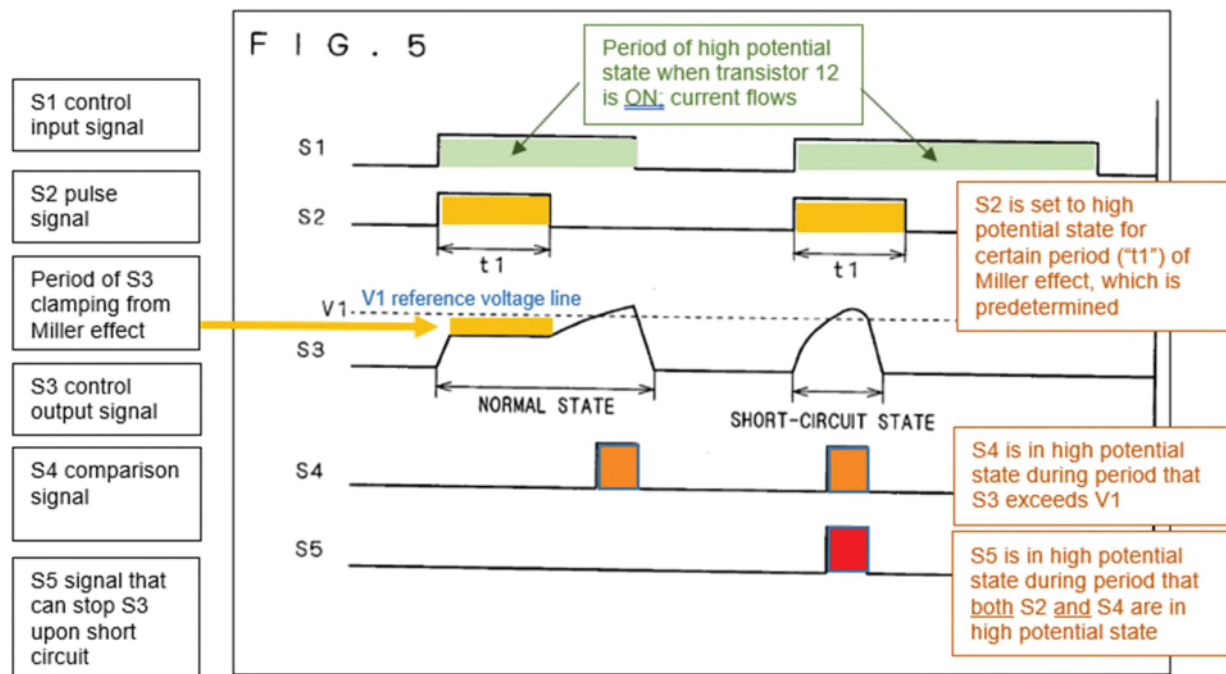
Complainant’s Proposed Construction	Respondents’ Proposed Construction	Staff’s Proposed Construction
held at a constant voltage	clamped to a certain voltage for a determined period by a Miller effect	held at a constant voltage

“Clamped constantly” does not mean “held at a constant voltage” when read in the context of the claims and specification. Rather, it means “clamped to a certain voltage for a predetermined period by a Miller effect,” as the specification explains. The alleged invention of the ’835 patent relates to providing short-circuit protection without a shunt resistor, and the ’835 patent does so by relying on the Miller effect (incorrectly translated as “mirror” effect in specification, as explained below) to determine if a short circuit has occurred.

In the context of electrical engineering generally, “clamping” in the context of “control” means “[a] function by which the extreme amplitude of a waveform is maintained at a given level.” Ex. 14, IEEE Standard Dictionary of Electrical and Electronic Terms (6th ed. 1996) (emphasis added). In the context of the ’835 patent, “a voltage of the control output signal S3 is clamped to a certain voltage for a determined period by a mirror effect.” See ’835 patent at 5:62-6:3 (emphasis added) & Fig. 5. The phrase “mirror effect” makes no sense without more context—it appears nowhere else in the ’835 patent and is not explained in any way, nor is it a term of art comprehensible to a POSITA. However, when viewed in the context of the intrinsic record, it is clear that “mirror effect” should have been written “Miller effect,” and an error occurred in translation, as explained below. The Miller effect is a critical part of the claimed invention.

1. The “Miller effect” determines clamping.

The Miller effect is best depicted in Figures 5 and 9—where the control output signal voltage S3 (in Fig. 5) or S13 (in Fig. 9) rises and then quickly stabilizes beneath V1 (the reference voltage line). The control output signal (S3 or S13) remains “clamped to a certain voltage for a predetermined period by a Miller effect” before further rising. As before, Figure 5 is annotated below consistent with the description in **Section III.B.4., *supra***:



As shown above, the Miller effect is part of the “NORMAL STATE” of operation, where the S3 control output signal is clamped beneath the reference voltage (V_1 line) for a predetermined period of time. ’835 patent at 5:67-6:1. The time duration for the period during which S3 should clamp (plateau) due to the Miller effect can be predetermined because the Miller effect has been known in the art of electrical engineering for more than 100 years. *See* Ex. 15.⁴ Thus, pulse signal S2 “maintain[s] a high potential (‘H’) state for a certain period which is predetermined.” *Id.* at 5:58-60. That “period t_1 in the significant condition, in the ‘H’ state in this case, is set to be almost equal to a period when the control output signal S3 is clamped to a certain voltage”—*i.e.*, the Miller effect period. *Id.* at 6:38-40. By contrast, in the “SHORT-CIRCUIT STATE,” no Miller effect or resulting plateau occurs, and the S3 control output signal

⁴ “Origin of the Miller Effect,” attaching John M. Miller, “Dependence of the input impedance of a three-electrode vacuum tube upon the load in the plate circuit,” Scientific Papers of the Bureau of Standards, 15(351):367-385 (1920).

voltage immediately ramps over the reference voltage V1. *Id.* at 6:54-64 (“the clamp period of the voltage does not exist...and the voltage of the control output signal rises rapidly”). The time period of the Miller effect and resulting plateau are thus critical to the alleged invention’s ability to detect a short circuit when monitoring the control output signal.

The ’835 patent uses two comparison signals to determine if exceeding the reference voltage is part of normal operation (after the Miller effect period) or due to a short-circuit. Comparison signal S4 is in a high potential state any time that S3 exceeds V1, but this is not abnormal if the t1 period has passed so that S2 is no longer in a high potential state (*i.e.*, the predetermined period of clamping has ended). *Id.* at 6:50-52. Comparison signal S5 (which also can be called a “stop signal,” *see* ’835 patent at 7:19-21) enters a high potential state when both S2 and S4 are in a high potential state, *i.e.*, during a short circuit. This is because, under normal operation, a Miller effect plateau is expected in control output signal S3—so if both the S2 and S4 pulses are significant at the same time, it indicates that a Miller effect plateau did not occur during the expected period “t1” and that a short-circuit occurred instead. *Id.* When S5 is in a high potential state, the ultimate result is “the control output signal S3 comes to be in the ‘L’ state and the transistor 12 is forced to be in the OFF state.” *See* ’835 patent at 7:13-18. Thus, the invention of the ’835 patent relies on the predetermined period of S3 clamping from the Miller effect in normal operation to determine if a short circuit has occurred and, if so, to shut the transistor OFF. *See, e.g., id.* For these reasons, Respondents’ proposed construction correctly captures that “clamped constantly” in the context of the ’835 patent claims means “clamped to a certain voltage for a determined period by a Miller effect.”

2. “Miller effect” was wrongly translated as “mirror effect.”

“Miller effect,” which is well-known in the art of electrical engineering, was incorrectly written as “mirror effect” when the ’835 patent specification was translated from Japanese. Compare Exs. 16-17 (translations of original Japanese applications) at [050] *with* ’835 patent at 5:67-6:1. Specifically, the two priority applications that led to the ’835 patent were filed in Japan and in the Japanese language. *See* ’835 patent at (30), listing “Foreign Application Priority Data” as JP 2004-001057 (Jan. 6, 2004) and JP 2004-262033 (Sept. 9, 2004). The specifications included in those foreign priority applications should be substantially the same as the ’835 patent specification. However, both foreign applications refer to the well-known “Miller effect” rather than the puzzling “mirror effect.” Certified translations of both JP 2004-262033 and JP 2004-001057 state:

Also, when the voltage of the control output signal S3 exceeds a threshold value of the transistor 12, the transistor 12 enters the on state, and a collector-emitter voltage of the transistor 12 drops, and thus, due to a Miller effect, the voltage of the control output signal S3 is clamped to a constant voltage for a predetermined period.

Ex. 16, JP 2004-262033 at [50]; Ex. 17, JP 2004-001057 at [050]. By contrast, the same sentence of the ’835 patent specification reads:

Moreover, when a voltage of the control output signal S3 exceeds a threshold value of the transistor 12, the transistor 12 comes to be in ON state, and a collector-emitter voltage of the transistor 12 drops, thus a voltage of the control output signal S3 is clamped to a certain voltage for a determined period by a mirror effect, however, the voltage of the control output signal S3 rises to be a value almost equal to the drive Voltage VCC of the gate driver GD after that.

See ’835 patent at 5:62-6:3 (emphasis added).

In sum, in the context of the art of electrical engineering and the ’835 patent—and specifically with reference to the Miller effect relied upon by the patent—“clamped constantly”

means “clamped to a certain voltage for a determined period by a Miller effect.” *See* ’835 patent at 5:62-6:3; Ex. 16, JP 2004-262033 at [50]; Ex. 17, JP 2004-001057 at [050].

G. “control output signal” (claim 1)

Complainant’s Proposed Construction	Respondents’ Proposed Construction	Staff’s Proposed Construction
Plain and ordinary meaning, e.g., output signal that is controlling an insulated gate transistor	signal supplied to the gate of an insulated gate transistor to switch the transistor between ON and OFF states	signal supplied to the gate of an insulated gate transistor to switch the transistor between ON and OFF states

The term “control output signal” is closely related to the term “controlling a drive of an insulated gate transistor,” as the voltage of the “control output signal” is supplied to the gate of the insulated gate transistor to control its drive. *See, e.g.*, ’835 patent at 4:14-20 (“[a]s shown in FIG. 2, the control output signal is supplied to the gate electrode of the transistor 12”); 3:3-7 (“The inverter module 100 has a composition that a control output signal is supplied to respective gate electrodes of the transistors 11, 21 and 31 from respective control signal output terminals.”), 3:36-40 (“The inverter module 100 has a composition that a control output signal is supplied to respective gate electrodes of the transistors 12, 22 and 32 from control signal output terminals”); 4:28-33 (“an output signal of a gate driver GD...is supplied as a control output signal S3 to the gate electrode of the transistor 12”); 5:62-6:5 (“when a voltage of the control output signal S3 exceeds a threshold value of the transistor 12, the transistor 12 comes to be in ON state”). Because these terms are closely related, Respondents and Staff propose similar constructions for both “controlling a drive of an insulated gate transistor” and “control output signal.” Specifically, “control output signal” should mean “signal supplied to the gate of an insulated gate transistor to switch the transistor between ON and OFF states.”

Once again, Arigna’s construction includes the phrase “plain and ordinary meaning, e.g.,” and for the same reasons discussed above, proposing such an open-ended construction is contrary

to the purpose of claim construction and should be rejected for this reason alone. *See O2 Micro*, 521 F.3d at 1360. The remainder of Arigna’s construction (“output signal that is controlling an insulated gate transistor”) confirms, at least, that the construction of “control output signal” should include the phrase “an insulated gate transistor.” Where the parties seemingly disagree is: (1) whether it is a “signal supplied to the gate” (Respondents and Staff) or an “output signal that is controlling” (Arigna) an insulated gate transistor; and (2) whether the “control output signal” must “switch the transistor between ON and OFF states” (Respondents’ and Staff’s position).

Respondents’ and Staff’s use of the phrase “signal supplied to the gate” in the construction for “control output signal” accurately reflects the disclosures of the patent specification. The ’835 patent explains: “[a]s shown in FIG. 2, the control output signal is supplied to the gate electrode of the transistor 12.” ’835 at 4:14-20; *see also* 3:3-7; 3:36-40; 4:32-33; 7:57-59. Arigna’s use of the phrase “output signal that is controlling” is both circular and does not reflect the intrinsic record as accurately as Respondents’ and Staff’s construction. It is also unclear why Arigna disagrees with Respondents’ and Staff’s use of “signal supplied to the gate.” Arigna’s alternative construction for “controlling a drive of an insulated gate transistor” is “plain and ordinary meaning, e.g., controlling the signal applied to the gate of an insulated gate transistor.” Applying this construction to Arigna’s phrase “output signal that is controlling an insulated gate transistor,” it would be “output signal that is [applied to the gate of an insulated gate transistor]”—almost identical to the portion of Respondents’ and Staff’s construction “signal supplied to the gate of an insulated gate transistor.” Thus, it is unclear why Arigna disputes at least this portion of Respondents’ and Staff’s construction.

With respect to the inclusion of the phrase “to switch the transistor between ON and OFF states” in the construction, the patent specification confirms that the “control output signal”

supplied to the gate of the transistor is responsible for switching the transistor between ON and OFF states, as reflected in Respondents’ and Staff’s construction. As discussed in the context of the term “controlling a drive of an insulated gate transistor,” merely supplying some signal to the gate of the transistor is not enough to “control[] the drive” of the transistor—rather, as the patent teaches, the “control output signal” voltage supplied to the gate must “exceed[] a threshold value of the transistor 12” so that “the transistor 12 comes to be in the ON state.” *Id.* at 5:62-6:5. Conversely, when “[the voltage of the control output signal S3] falls according to a trailing edge of the control input signal S1,” then it “makes the transistor 12 be OFF.” *Id.* If “the control output signal S3 is maintained,” then “the ON state in the transistor 12 is maintained.” *Id.* at 6:47-53. Similarly, if the voltage supplied does not exceed the transistor’s threshold value, the transistor remains in the OFF state, and the drive of the transistor is not controlled, as claimed. The ability to “switch the transistor between ON and OFF states” is also critical to the purpose of the alleged invention, which is to provide “a short-circuit protection function” for “an insulated gate type switching device.” *Id.* at 1:13-14. In the event of a short-circuit, the claimed semiconductor device must be able to force the transistor to an OFF state via the control output signal. *See, e.g., id.* at 6:54-62, 7:13-21, 10:35-43, 10:45-61. Respondents’ and Staff’s construction should be adopted because it most accurately captures the specification’s disclosures.

H. “short-circuit protection circuit” (claim 1)

Complainant’s Proposed Construction	Respondents’ Proposed Construction	Staff’s Proposed Construction
Plain and ordinary meaning, e.g. circuit that performs function of short-circuit protection	circuit that performs short-circuit protection without a shunt resistor	circuit that performs short-circuit protection without a shunt resistor

Respondents and Staff agree that the term “short-circuit protection circuit” means “circuit that performs short-circuit protection without a shunt resistor,” which reflects the specification’s clear and unambiguous disclaimer of conventional circuits that perform short-circuit protection functions with a shunt resistor. Arigna’s construction differs from Respondents’ and Staff’s construction in two ways: (1) it includes the phrase “[p]lain and ordinary meaning, e.g.,” and (2) it improperly seeks to recapture claim scope the patentee disavowed in the patent specification. As discussed above, Arigna’s use of “plain and ordinary meaning, e.g.,” in several proposals leaves its constructions open-ended and fails to delineate the scope of the asserted claims. *See O2 Micro*, 521 F.3d at 1360. Arigna’s proposal should be rejected for this reason alone. Further, Respondents’ and Staff’s construction remains faithful to the clear and unambiguous teachings of the patent specification, which consistently and repeatedly disparages conventional systems for performing short-circuit protection using a shunt resistor.

Statements in the specification can operate as a disclaimer of claim scope where they expressly or implicitly state that specific subject matter is outside the scope of the invention. Where, as here, a patentee disparages prior art lacking a particular feature, he or she disavows claim scope that would recapture that feature. *Poly-America, L.P. v. API Indus., Inc.*, 839 F.3d 1131, 1136 (Fed. Cir. 2016); *Ekchian v. Home Depot, Inc.*, 104 F.3d 1299, 1304 (Fed. Cir. 1997) (“[S]ince, by distinguishing the claimed invention over the prior art, an applicant is indicating what the claims do not cover, he is by implication surrendering such protection.”). Indeed, the Federal Circuit has repeatedly held that claims should be construed to exclude features repeatedly disparaged or distinguished in the specification. *See, e.g., Openwave Sys., Inc. v. Apple Inc.*, 808 F.3d 509, 514-17 (Fed. Cir. 2015) (construing claims to exclude mobile devices with “computer modules” where the specification repeatedly disparaged prior art devices with

“computer modules” and distinguished purported invention from such prior art devices); *Indivior Inc. v. Dr. Reddy’s Lab’s, S.A.*, 930 F.3d 1325, 1337 (Fed. Cir. 2019) (construing claims to exclude conventional top-air drying where specification repeatedly disparaged such features); *UltimatePointer, L.L.C. v. Nintendo Co.*, 816 F.3d 816, 823 (Fed. Cir. 2016) (construing claims to exclude “indirect pointing” handheld devices, where the specification repeatedly disparaged such features).

Respondents’ and Staff’s proposed construction properly reflects the patentee’s repeated disclaimers of conventional short-circuit protection circuits with shunt resistors. For starters, the ’835 Patent’s title is “Semiconductor Device Which Realizes a Short-Circuit Protection Function Without Shunt Resistor, And Semiconductor Device Module.”⁵ ’835 patent at Title (emphasis added). Next, in the “Description of the Background Art,” the ’835 patent states that “a semiconductor device in which the insulated gate type switching device... and a control circuit controlling a drive of that switching device are packaged is called an IPM (Intelligent Power Module)...” ’835 patent at 1:17-20. The specification further explains that “with regard to a conventional IPM, a short-circuit protection is performed by connecting a shunt resistor detecting a main current flowing between main power terminals of the switching device outside the package and monitoring the main current.” ’835 patent at 1:20-25 (emphasis added).

⁵ When the patentee originally filed the patent application, the title of the invention was “Semiconductor Device and Semiconductor Device Module.” Ex. 18 (December 29, 2004 Transmittal of New Application, Specification at 1). After the claims were rejected, the patentee filed narrowing amendments, including a request to change the title of the invention to “Semiconductor device which realizes a short-circuit protection function without shunt resistor, and semiconductor device module.” Ex. 19 (October 10, 2006 Applicant Amendments at 2). The patentee’s amendments demonstrate the intent to seek a narrow invention from the USPTO.

The specification repeatedly disparages conventional shunt resistor systems, noting numerous drawbacks of such systems. For example, the specification explains that conventional IPMs with shunt resistors, require a current detecting terminal external to the device to detect the voltage output by the device:

As described above, with regard to the conventional IPM, the short-circuit protection is performed by detecting the main current of the switching device by the shunt resistor set outside the package, thus the current detecting terminal is necessary to detect the voltage put on the shunt resistor.

Id. at 1:32-40 (emphasis added). The specification further emphasizes that conventional IPMs with shunt resistors can be massive due to the additional circuitry required to perform short circuit protection:

Moreover, it is necessary to set a filter circuit such as a CR filter and so on outside the package to remove a noise entering the shunt resistor and the current detecting terminal, and there is a possibility that a device becomes massive.

Id. at 1:37-40 (emphasis added). According to the specification, further drawbacks of shunt-resistor based short-circuit protection circuits is that they are susceptible to large voltage surges, are susceptible to errors in detecting short-circuits:

Moreover, when a length of a wiring from a ground main electrode to a ground terminal of the switching device becomes long by setting the shunt resistor, a voltage surge according to a switching of the switching device becomes large, and there is also a possibility that an error occurs.

Id. at 1:37-40 (emphasis added).

The '835 patent purports to solve these problems with conventional shunt-resistor based short-circuit protection circuits, describing the invention as a circuit that performs short-circuit protection without a shunt resistor:

A semiconductor device which realizes a short-circuit protection function without a shunt resistor and an IPM in which the semiconductor device is built are provided.

Id. at 1:37-40 (Summary of the Invention) (emphasis added).

Further emphasizing the distinction between the purported invention and conventional shunt-resistor based circuits, the patentee specifically distinguished each disclosed embodiment from conventional circuits with shunt resistors. For example, the specification describes the “Effect” of the circuit of embodiment A, as follows:

As described above, with regard to the control device LIC including the short-circuit protection function, the short circuit state is detected by monitoring the control output signal S3 of the transistor 12 constituting the main circuit, and in case that the transistor 12 comes to be in the short-circuit state, the control output signal S3 is forced to stop, thus it is not necessary for the inverter module 100 to set the shunt resistor outside of the package PG (FIG. 1), differing from the conventional IPM.

Id. at 7:23-31 (emphasis added). The specification next describes the benefits of purported invention resulting from the performance short-circuit protection without a shunt resistor:

Moreover, the shunt resistor is not necessary, thus the length of the wiring from the ground main potential to the ground terminal of the switching device can be made to be short, and the voltage surge according to the switching of the switching device can be reduced.

Id. at 7:32-43 (emphasis added). The specification similarly distinguishes the circuit of embodiment B from conventional shunt resistor based circuits, and highlights the benefits of the purported invention which result from performing short-circuit protection without a shunt resistor. *Id.* at 10:55-11:11.

The specification’s consistent and repeated disparaging of the prior art “shunt resistor” feature and characterization of the invention as a circuit that performs a short-circuit protection function “without a shunt resistor” limits the scope of the ’835 Patent’s claims. *See, e.g., Poly-*

America, 839 F.3d at 1136; *Ekchian*, 104 F.3d at 1304. The intrinsic evidence thus confirms that Respondents' and Staff's construction is correct and should be adopted.

VI. CONCLUSION

For the foregoing reasons, Respondents request that the ALJ adopt their proposed constructions.

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**UNITED STATES INTERNATIONAL TRADE COMMISSION
Washington, D.C.**

**Before The Honorable Monica Bhattacharyya
Administrative Law Judge**

In the Matter of

**CERTAIN POWER
SEMICONDUCTORS, AND MOBILE
DEVICES AND COMPUTERS
CONTAINING SAME**

Inv. No. 337-TA-1308

I, Debby Brady, hereby certify that on August 5, 2022, a copy of *Respondents' Opening Claim Construction Brief* served on the following as indicated:

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