

**UNITED STATES INTERNATIONAL TRADE COMMISSION
Washington, D.C.**

**Before the Honorable Monica Bhattacharyya
Administrative Law Judge**

In the Matter of

**CERTAIN POWER SEMICONDUCTORS, AND
MOBILE DEVICES AND COMPUTERS
CONTAINING SAME**

Inv. No. 337-TA-1308

RESPONDENTS' REBUTTAL CLAIM CONSTRUCTION BRIEF

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RIB	Respondents' Initial Claim Construction Brief (August 5, 2022)
SIB	Staff's Initial Claim Construction Brief (August 5, 2022)

I. INTRODUCTION

Arigna's initial brief proposes several broadened and changed constructions not disclosed before filing. The reason is clear—Arigna wants to keep the disputed claim terms as malleable as possible. That is not the purpose of claim construction, however. The purpose of claim construction is to determine the meaning and scope of claims asserted to be infringed, and claim constructions should resolve the parties' disputes over claim scope.

Arigna's constructions do not achieve that purpose. On the contrary, Arigna's initial brief backtracks from many of its original "plain and ordinary meaning, *e.g.*" proposals, which themselves were improperly open-ended, to even-broader proposals with no "*e.g.*" descriptions at all. For example, in the G.R. 6.1 Joint Disclosure of Disputed Claim Term Constructions filed on July 15, 2022, Arigna proposed that "controlling a drive of an insulated gate transistor" be defined as "plain and ordinary meaning, *e.g.*, controlling the signal applied to the gate of an insulated gate transistor" if the preamble were limiting. Arigna now argues "plain and ordinary meaning" without more, presumably so it might wrongly point to a signal applied to any portion of a transistor. As the Staff correctly argues, Arigna's original proposal "is entirely at odds with the device described and claimed by the '835 Patent" and "would be a tremendous distortion of the invention described and claimed." SIB at 21-22. Arigna's new proposal is even worse.

Arigna also backtracks from its original, overbroad construction of "short-circuit protection circuit" to argue "[n]o construction necessary." Arigna then continues to wrongly argue that its alleged invention of a "short-circuit protection function without shunt resistor" should cover use of a shunt resistor, when the '835 patent consistently disparages and distinguishes use of shunt resistors in prior art systems. As the Staff correctly observes, "[t]he

crux of the invention and sole purported advance over the prior art is a switching device that includes short-circuit protection *without a shunt resistor*.” SIB at 35-36 (emphasis in original).

Because Arigna’s non-constructions are wrong and will not resolve the parties’ disputes over claim scope, the ALJ should reject them. Instead, Respondents respectfully request that the ALJ adopt their constructions (often supported by Staff), which capture the meaning of disputed terms when read in light of the claims and specification as required.

II. DISPUTED CLAIM TERMS

Arigna modified several of its constructions from the G.R. 6.1 Joint Disclosure. Respondents have annotated in the charts below the modifications to Arigna’s constructions.

A. Preamble (claim 1)

Complainant’s Proposed Construction	Respondents’ Proposed Construction	Staff’s Proposed Construction
Non-limiting <u>preamble in part</u> ¹	The preamble is limiting.	The preamble is limiting.

Arigna concedes that most of the preamble is limiting, but asks the Court to carve out the first few words to find them non-limiting. Arigna’s argument fails because it (1) improperly splices the preamble into two portions, (2) incorrectly concludes that the first portion of the preamble does not contain structural elements, and (3) ignores the presumption that the preamble is limiting when, as here, it provides antecedent basis and gives life or meaning to the claim.

First, Arigna’s attempt to divide the preamble into limiting and non-limiting portions is inappropriate. The Federal Circuit has noted that it is “disinclined to sanction finding a preamble ‘partially’ limiting by splicing it as the district court did here.” *Bio-Rad Lab ’ys, Inc. v. 10X Genomics Inc.*, 967 F.3d 1353, 1371 (Fed. Cir. 2020) (finding district court’s construction

¹ Underlines indicate where Arigna made additions to its proposals from those put forth in the July 15 G.R. 6.1 Joint Disclosure, while strikethroughs indicate deletions.

erroneous and vacating finding of infringement).² The only support Arigna finds for severing the preamble in this way is *TomTom, Inc. v. Adolph*, 790 F.3d 1315 (Fed. Cir. 2015), but Arigna’s reliance on *TomTom* is misplaced. *TomTom* is inapplicable and has subsequently been distinguished by the Federal Circuit. In *TomTom*, the district court erred because its sole basis for construing an entire preamble as limiting was that one portion of the preamble contained an antecedent basis term. *TomTom*, 790 F.3d at 1323 (“the court erred in determining that it had to construe the entire preamble if it construed a portion of it”); *see TomTom, Inc. v. AOT Sys. GmbH*, No. 12-cv-528, Dkt. 198 (Markman Order) at 16-17 (E.D. Va. Feb. 25, 2014). *TomTom* is inapplicable here because Respondents do not rely solely on antecedent basis. RIB at 13-21.

The Federal Circuit’s discussion of *TomTom* in recent cases further distinguishes it from the facts here. In *TomTom*, “[t]he two-part preamble of the asserted claim recited: ‘[1] [a] method for generating and updating data [2] for use in a destination tracking system of at least one mobile unit comprising,’” and the first part of the preamble “did not recite essential structure or steps, or give necessary life, meaning, and vitality to the claim.” *Bio-Rad*, 967 F.3d at 1371. In a later case, the Federal Circuit clarified that *TomTom* does not apply to cases where the preamble “cannot be neatly packaged into two separate portions.” *Id.* Having distinguished *TomTom*, the Federal Circuit found in *Bio-Rad* that the claimed preamble for “[a] method for conducting a reaction in plugs in a microfluidic system, comprising the steps of” was limiting because two terms with antecedent basis, “reaction” and “microfluidic systems,” were “intertwined with the rest of the preamble” and were “a strong indication that the preamble acts ‘as a necessary component of the claimed invention.’” *Id.*

² All internal citations and footnotes throughout the brief are omitted unless otherwise indicated.

Just as in *Bio-Rad*, claim 1’s preamble “cannot be neatly packaged into two separate portions” and its antecedent basis terms (“an insulated gate transistor,” “a control output signal,” and “a control input signal”) are “intertwined with the rest of the preamble.” *Id.* The preamble links each item together through a series of prepositional phrases showing their interrelation: “[a] semiconductor device controlling a drive of an insulated gate transistor by generating a control output signal on a basis of a control input signal.” Without the first phrase (“controlling a drive of”) the next phrase—“an insulated gate transistor by generating a control output”—makes no sense. The phrases are linked, and Arigna’s strained proposal to splice them into two separate portions fails. *Pitney Bowes, Inc. v. Hewlett-Packard Co.*, 182 F.3d 1298, 1306 (Fed. Cir. 1999) (finding preamble limiting where it “is intimately meshed with the ensuing language in the claim”); *Certain Power Inverters & Converters, Vehicles Containing the Same, & Components Thereof*, Inv. No. 337-TA-1267, Order No. 30 at 34 (Jan. 18, 2022) (finding entire preamble limiting where portions are “intertwined with [a] phrase that forms an antecedent basis for the body of the claim.”). Moreover, the fact that the patentee used the preamble to provide antecedent basis for some terms “is a strong indication that the [entire] preamble acts as a necessary component of the claimed invention.” *Bio-Rad*, 967 F.3d at 1370-72 (quoting *Eaton Corp. v. Rockwell Int’l Corp.*, 323 F.3d 1332, 1339 (Fed. Cir. 2003)).

Second, Arigna incorrectly argues that the phrase “a semiconductor device controlling a drive of” merely states an intended use and “does not include any structural elements.” CIB at 4. In truth, the preamble is the only place in the claim that recites a “drive of” the insulated gate transistor, which is an essential structural part of the alleged invention. RIB at 17-19. As explained further below, this portion of the preamble informs a person of skill in the art that the “control output signal” must be connected to the gate of the transistor to “control[] [the] drive of”

the transistor. *See* Section II.C, *infra*. Moreover, statements of intended use are frequently found limiting, particularly where they recite structure or where they recite “necessary and defining aspects of the invention” rather than “simply an introduction to the general field of the claim.” *Comput. Docking Station Corp. v. Dell, Inc.*, 519 F.3d 1366, 1375 (Fed. Cir. 2008); *see also Pacing Techs., LLC v. Garmin Int’l, Inc.*, 778 F.3d 1021, 1024 (Fed. Cir. 2015) (finding preamble a necessary component of the claimed invention that provided antecedent basis for claim limitations); *Proveris Sci. Corp. v. Innovasystems, Inc.*, 739 F.3d 1367, 1372 (Fed. Cir. 2014) (finding preamble limiting on multiple grounds).

Third, while Arigna recognizes that preambles are found limiting where they provide life, meaning, or vitality to the claim (CIB at 3), Arigna ignores that aspect of the preamble here. Instead, Arigna argues that the preamble “merely duplicates” the elements recited in the body of the claim. CIB at 5-6. On the contrary, the preamble describes essential associations between claim elements—including between the control input and control output signals, and how the insulated gate transistor is controlled—that are “only discernible from the claim preamble.” *Pitney Bowes*, 182 F.3d at 1306; RIB at 19-21.

B. “insulated gate transistor” (claims 1 and 2)

Complainant’s Proposed Construction	Respondents’ Proposed Construction	Staff’s Proposed Construction
a transistor whose gate is electrically insulated from the channel	Plain meaning, i.e. IGBT (insulated gate bipolar transistor)	a transistor whose gate is electrically insulated from the channel

Arigna and Staff conflate two distinct terms in the specification of the ’835 patent: (1) “insulated gate type switching device,” and (2) “insulated gate transistor.” But the terms are different, and each have their own, unique plain meaning, which is confirmed by the specification of the ’835 patent and extrinsic evidence. Every instance of the term “insulated

gate type switching device” in the specification refers to a broader category of devices that have an insulated gate. The specification uses this term four times, and all of them refer to an “insulated gate type switching device such as the IGBT and so on.” ’835 patent at 1:14-15, 1:17-18, 2:50-51, 6:6-7. These “such as” and “so on” phrases make clear that the patentee intended this term to refer to IGBTs as well as other insulated gate type switching devices. Arigna and Staff focus exclusively on these disclosures. CIB at 6-7; SIB at 18-19.

But the patentee did not seek or receive claims directed to an “insulated gate type switching device”—the patentee claimed an “insulated gate transistor.” *See Sage Prods., Inc. v. Devon Indus., Inc.*, 126 F.3d 1420, 1425 (Fed. Cir. 1997) (“[A]s between the patentee who had a clear opportunity to negotiate broader claims but did not do so, and the public at large, it is the patentee who must bear the cost of its failure”). In contrast to the disclosures above, every use of the term “insulated gate transistor” in the specification refers exclusively to an IGBT. The specification does not use “such as” or “so on” phrases or otherwise imply that an insulated gate transistor can be anything other than an IGBT. Instead, it defines “the insulated gate transistor” as “transistor 12” (’835 patent at 4:14-26), and “transistors 11, 12, 21, 22, 31 and 32,” which are all undisputedly IGBTs. *Id.* at 11:28-30. Arigna and Staff ignore these disclosures.

Respondents cite nine sources of extrinsic evidence that confirm the plain meaning of “insulated gate transistor” is an IGBT. *See* RIB at 21-23, Exs. 1-9. Arigna and Staff have not identified any contrary extrinsic evidence. Instead, Arigna’s and Staff’s extrinsic evidence supports Respondents’ construction because it demonstrates that other switching devices with insulated gates (MOSFETs) are not referred to as “insulated gate transistors,” but are instead distinguished by the fact that they are FET devices. CIB, Ex. 1 (defining “insulated-gate field-

effect transistor (IGFET)”); SIB, Ex. 9 (“The Insulated-Gate Field-Effect Transistor (IGFET), also known as the Metal Oxide Field Effect Transistor (MOSFET)”).

The fundamental design concept of the insulated gate transistor is that it is a hybrid device that is an “integration of a MOSFET and a wide base Bipolar Junction Transistor (BJT).” RIB, Ex. 3, 274 (“The IGT is modeled as a Bipolar Junction Transistor (BJT) driven by a MOSFET.”); Ex. 1, 1 (The “IGBT” or “IGT” is a “cross between the Bipolar junction Transistor (BJT) and Metal Oxide Semiconductor Field-effect Transistor (MOSFET)”); Ex. 8, 2 (“Since IGBT is the combination of MOSFET and BJT they are also called by different names. The different names of IGBT are Insulated Gate Transistor (IGT). . . .”); *see* Exs. 2, 7. This “three-terminal power device, called the insulated gate transistor (IGT), [combines] the best features of the existing families of bipolar devices and power MOSFET’s . . . to achieve optimal device characteristics.” RIB, Ex. 4, 821. The name “insulated gate transistor” thus distinguishes the IGT device from the devices that came before it: BJTs and MOSFETs (IGFETs).³ *Id.* While the IGT includes design features from both, the IGT, by definition, is a distinct and different device.

The cases Arigna cites are inapposite. Respondents do not seek to import limitations from the specification into the claims. Respondents’ proposed construction provides the plain

³ The extrinsic evidence is replete with examples. An application note from Fairchild Semiconductor analyzes characteristics of the insulated gate transistor and discloses that the “insulated gate transistor (IGT) combines the high input impedance, voltage controlled turn on/turn off capabilities of power MOSFETs and the low on-state conduction losses of bipolar transistors, making it an ideal device for many power electronics switching control applications.” Ex. 20, *Parallel Operation Of Semiconductor Switches*, FAIRCHILD SEMICONDUCTOR CORP., Application Note AN-7513 Rev. A1, at 3 (2002). Similarly, Elbuluk and Kankam studied certain power devices, explaining that “the IGT is a hybrid MOS-gated turn on/off bipolar junction transistor (BJT) that combines the attributes of a MOSFET and a BJT.” Ex. 21, Motor Drive Technologies for the Power-By-Wire (PBW) Program, IEEE AES SYSTEMS MAGAZINE, at 31 (1995); *see* Ex. 22, Brand & Selberherr, *Electrothermal Analysis of Latch-Up in an Insulated Gate Transistor (IGT)*, IEICE TRANS. ELECTRON., Vol. E77-C, NO. 2 (1994).

meaning of the term in light of the specification and the alleged invention, and as supported by extrinsic evidence. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1314 (Fed. Cir. 2005) (*en banc*); *Groove Digital, Inc. v. United Bank*, 825 F. App’x 852, 856 (Fed. Cir. 2020) (unpublished) (“a patent’s repeated and consistent description of a claim term may inform its construction”) (citing *In re Abbott Diabetes Care Inc.*, 696 F.3d 1142, 1150 (Fed. Cir. 2012)); *Profectus Tech. LLC v. Huawei Techs. Co.*, 823 F.3d 1375, 1380-81 (Fed. Cir. 2016) (“When read in view of the specification, the claims do not permit the expansive construction proposed by Profectus.”). Arigna’s proposed construction, in contrast, seeks to unduly broaden the meaning of the claim beyond the plain and ordinary meaning and should be rejected. *In re Power Integrations, Inc.*, 884 F.3d 1370, 1376 (Fed. Cir. 2018) (finding “the board’s unduly broad reading of the language of claim 1 is unsupported by the specification”); *Home Semiconductor Corp. v. Samsung Elecs. Co. Ltd.*, 701 F. App’x 1006, 1010 (Fed. Cir. 2017) (finding construction unreasonably broad where it failed to account for “the context in which it is used in the claims and the specification”); *Taurus IP, LLC v. DaimlerChrysler Corp.*, 726 F.3d 1306, 1320-21 (Fed. Cir. 2013) (finding construction of “user” “improperly broad” and beyond plain meaning supported by specification).

C. “controlling a drive of an insulated gate transistor” (claim 1)

Complainant’s Proposed Construction	Respondents’ Proposed Construction	Staff’s Proposed Construction
Non-limiting preamble Alternatively, plain and ordinary meaning, e.g., controlling the signal applied to the gate of an insulated gate transistor	controlling the voltage supplied to the gate of an insulated gate transistor to switch the transistor between ON and OFF states	controlling the voltage supplied to the gate of an insulated gate transistor to switch the transistor between ON and OFF states

Respondents’ and Staff’s construction reflects the plain and ordinary meaning of “controlling a drive of an insulated gate transistor” in view of the intrinsic evidence. Arigna’s

new “plain and ordinary meaning” construction will not resolve the parties’ dispute over claim scope, and Arigna’s criticisms of Respondents’ and Staff’s construction lack merit.

1. The ALJ should reject Arigna’s new “plain and ordinary” construction.

When filing the G.R. 6.1 Joint Disclosure, Arigna included an example of what it considered the “plain and ordinary” meaning of the disputed term, “e.g., controlling the signal applied to the gate of an insulated gate transistor.” *See* Ex. 23 (G.R. 6.1 Joint Disclosure), Ex. A. Though superficially similar to Respondents’ and Staff’s construction, important differences exist. RIB at 26. Unbeknownst to Respondents and Staff⁴, however, Arigna backtracked in its initial brief by omitting this example. Arigna instead advocates for simply “plain and ordinary meaning,” if the preamble is found to be limiting. *Compare* CIB at 8, *with* Ex. 23.

Arigna does not attempt to explain away its earlier example, but rather ignores it entirely. Regardless, the ALJ should reject Arigna’s new broader construction because it fails to resolve the parties’ dispute over how to articulate the term’s plain and ordinary meaning. *See O2 Micro Int’l Ltd. v. Beyond Innovation Tech. Co. Ltd.*, 521 F.3d 1351, 1361 (Fed. Cir. 2008) (“A determination that a claim term ... has the ‘plain and ordinary meaning’ may be inadequate when a term has more than one ‘ordinary’ meaning or when reliance on a term’s ‘ordinary’ meaning does not resolve the parties’ dispute.”). Arigna argues the term “is not ambiguous and would reasonably have been understood by a skilled artisan at the time of invention” (CIB at 10), but then does not explain Arigna’s purported understanding of the term. Arigna cannot now advocate for an ambiguous “plain and ordinary meaning” construction that it is unwilling to

⁴ Arigna did not provide notice to Respondents or Staff of its shifting positions prior to filing initial briefs, which is why Respondents and Staff did not have the benefit of addressing Arigna’s belated revision in their initial briefs.

elaborate upon, especially given that Arigna disputes Respondents’ and Staff’s articulation of the claim term’s plain and ordinary meaning.

2. The intrinsic record contradicts Arigna’s arguments against Respondents’ and Staff’s construction.

Respondents’ and Staff’s construction appropriately explains the meaning of “controlling a drive of an insulated gate transistor” in the context of the intrinsic record. The ’835 patent teaches three critical aspects to “controlling a drive of an insulated gate transistor”: (1) that a signal is applied to the gate of the transistor; (2) that the signal must switch the transistor to its ON (or OFF) state; and (3) that the voltage of the signal “control[s]” the gate of the transistor by exceeding (or falling below) the transistor’s threshold voltage. RIB at 26-29; SIB at 19-22. Respondents’ and Staff’s construction properly reflects these key intrinsic disclosures, and each of Arigna’s arguments contradict these teachings.

a. The ’835 patent teaches that a signal is applied to the gate of the insulated gate transistor.

Arigna argues that the preamble is not limiting (CIB at 3-6, 9), but this conflicts with the ’835 patent’s teaching that a signal is applied to the gate of the insulated gate transistor. As discussed above, the entire preamble—including the phrase “[a] semiconductor device controlling a drive of”—is limiting. *See* Section II.A., *supra*. The phrase “controlling a drive of an insulated gate transistor” is not merely “[t]he intended use for the driver outputting a control output signal,” as Arigna contends (CIB at 9), but rather, it discloses structure for the claim. Specifically, the phrase provides structure because it informs a person of skill in the art that the “control output signal” must be connected to the gate of the transistor to “control[] [the] drive of” the transistor, as opposed to being used as a power supply. *See* RIB at 27-29; SIB at 19-22; *see also, e.g.*, ’835 patent at 4:14-15 (“[a]s shown in FIG. 2, the control output signal is supplied to the gate electrode of the transistor 12”), 5:62-65 (“when a voltage of the control output signal S3

exceeds a threshold value of the transistor 12, the transistor 12 comes to be in ON state.”). The ’835 patent never discloses that the “control output signal” can be supplied to anything other than the gate of a transistor. *See* RIB 27-29; SIB at 21-22. The preamble of claim 1 imparts this disclosed structure, *i.e.*, that the claimed semiconductor device is connected to the gate of an insulated gate transistor to control it. The remainder of claim 1 is not “structurally complete,” as Arigna insists (CIB at 5), because the rest of the claim does not expressly describe how the “control output signal” connects to the “insulated gate transistor.”

For the same reason, Arigna’s assertion that “[n]o such limitation [‘to the gate of’] is found in the claim language” (CIB at 11) is wrong—the phrase “controlling a drive of an insulated gate transistor” reflects the express disclosures of the patent that the “control output signal” is connected to the transistor’s gate to control it. And even though Arigna now tries to distance itself from the example it provided in the G.R. 6.1 Joint Disclosure, it is telling that Arigna had considered the plain meaning of the construction to require “controlling the signal applied to the gate of an insulated gate transistor.” *See* Ex. 23 (emphasis added). The phrase “controlling a drive of an insulated gate transistor” imparts essential structure to the claim: controlling the voltage supplied to the gate of an insulated gate transistor.

b. The ’835 patent teaches that the signal applied to the transistor must switch the transistor to its ON (or OFF) state.

Arigna further contends that “there is no reason to add the limitation ‘to switch the transistor between ON and OFF states’” to the construction. CIB at 10. But the phrase “to switch the transistor between ON and OFF states” is not a limitation—it explains what “controlling a drive of” a transistor means in the context of the ’835 patent. ’835 patent at 5:62-65. The disputed term must be construed in the context of the invention described in the specification. *See Netword, LLC v. Centraal Corp.*, 242 F.3d 1347, 1352 (Fed. Cir. 2001) (“The

claims are directed to the invention that is described in the specification; they do not have meaning removed from the context from which they arose.”); *Toro Co. v. White Consol. Indus., Inc.*, 199 F.3d 1295, 1299 (Fed. Cir. 1999) (“Determining the limits of a patent claim requires understanding its terms in the context in which they were used by the inventor, considered by the examiner, and understood in the field of the invention.”).

The patent teaches that the voltage supplied to the gate must “exceed[] a threshold value of the transistor 12” so that “the transistor 12 comes to be in the ON state.” RIB at 28; ’835 patent at 5:62-6:5. When “[the voltage of the control output signal S3] falls according to a trailing edge of the control input signal S1,” then it “makes the transistor 12 be OFF.” *Id.* Furthermore, so long as “the control output signal S3 is maintained,” then “the ON state in the transistor 12 is maintained.” ’835 patent at 6:47-53. If the voltage supplied is below the transistor’s threshold value, the transistor remains in the OFF state. Each of these disclosures confirms that “controlling a drive” requires switching the transistor between ON and OFF states.

Arigna wrongly argues that “[b]ecause ‘controlling’ can consist of switching a transistor between states or maintaining a state, it should not be construed in a manner that would limit ‘controlling’ to only mean switching a transistor between ON and OFF states.” CIB at 10. Arigna ignores the disclosures of the ’835 patent discussed immediately above—once the transistor switches to the ON state, so long as that voltage is maintained, the transistor will maintain the ON state; similarly, once the transistor switches to the OFF state, so long as the voltage is below the transistor’s threshold voltage, the transistor will maintain the OFF state. ’835 patent at 6:47-53. Arigna’s argument ignores that to maintain a state, the transistor must first switch into that state. Specifically, maintaining an ON state first requires applying a voltage

to the gate of the transistor above the threshold voltage, switching the transistor ON. After that, the transistor maintains the ON state for as long as the voltage remains above the threshold.

c. The '835 patent teaches that the voltage of the signal “control[s]” the gate of the transistor by exceeding (or falling below) said transistor’s threshold voltage.

Arigna also wrongly argues that “controlling a drive of an insulated gate transistor” should not be limited to a voltage. CIB at 11. This, too, directly contradicts the specification’s disclosure that the voltage of the signal “control[s]” the gate of the transistor by exceeding (or falling below) the transistor’s threshold voltage. RIB at 28; '835 patent at 5:62-6:5. There is no dispute that the '835 patent teaches that the “control output signal” is supplied to the gate of the claimed “insulated gate transistor.” *See, e.g.*, '835 patent at 3:3-5. And the specification is very clear that the voltage of the “control output signal” controls the “insulated gate transistor,” as detailed by Respondents and Staff in their initial briefs. *See* RIB at 27-28; SIB at 21-22. Arigna postulates about theoretical current-controlled circuits, but is off-base. CIB at 11. The patent is abundantly clear that the voltage of the “control output signal,” not the current, is supplied to the “insulated gate transistor” to control its drive. *Id.* Arigna improperly ignores these disclosures.

3. Arigna cannot improperly expand the scope of asserted claims.

In sum, Arigna attempts through claim construction to eradicate the preamble’s structural requirement that the claimed “control output signal” be supplied to the gate of the “insulated gate transistor.” Arigna improperly seeks to expand the scope of its asserted claims beyond switching transistors to cover power supply/amplifier circuits. Arigna’s broader construction would render the claim invalid for lack of written description and/or failure to enable the full scope of the claims since the '835 patent fails to disclose the use of the claimed invention in power supply or amplifier circuits. *Phillips*, 415 F.3d at 1327; *see also Trustees of Bos. Univ. v. Everlight Elecs. Co. Ltd.*, 896 F.3d 1357, 1365 (Fed. Cir. 2018) (“[I]f BU wanted to exclude others from what it

regarded as its invention, its patent needed to teach the public how to make and use that invention. That is ‘part of the quid pro quo of the patent bargain.’”) (citing *Sitrick v. Dreamworks, LLC*, 516 F.3d 993, 999 (Fed. Cir. 2008)). As Staff correctly recognizes, Arigna “seeks to not limit the claim language to a transistor that is being operated as a switch. But this is entirely at odds with the device described and claimed by the ’835 Patent.” SIB at 21. Arigna’s alternative “plain and ordinary meaning” construction is wrong and does nothing to resolve the parties’ dispute regarding the meaning of “controlling a drive of an insulated gate transistor.” The intrinsic record confirms Respondents’ and Staff’s construction.

D. “indicates a conduction of said insulated gate transistor” (claim 1)

Complainant’s Proposed Construction	Respondents’ Proposed Construction	Staff’s Proposed Construction
Plain and ordinary meaning, e.g., indicates that said insulated gate transistor is turned on	indicates that said insulated gate transistor is in the ON state	indicates that said insulated gate transistor is in the ON state

Respondents’ and Staff’s construction more accurately captures the plain and ordinary meaning of “indicates a conduction of said insulated gate transistor” based on the intrinsic record and provides needed clarity to the meaning and scope of the term. RIB at 29-30; SIB at 23-24. Arigna argues that “no construction is necessary or appropriate” (CIB at 12), but the parties dispute the plain meaning of the term, necessitating a construction. *O2 Micro*, 521 F.3d at 1361.

Arigna confirms that its example of plain and ordinary meaning “is not wholly dissimilar from the construction Respondents and Staff propose,” but that “Respondents’ and Staff’s construction is problematic because it would introduce further ambiguity into the claim language by suggesting that there must be a specific ‘ON state’ condition in the transistor.” CIB at 12. Arigna ignores important context in the specification to wrongly argue that Respondents and Staff are “importing a limitation from the specification,” when they are not. CIB at 13. The

'835 patent is clear: “when a voltage of the control output signal S3 exceeds a threshold value of the transistor 12, the transistor 12 comes to be in ON state,” and current starts to flow. '835 patent at 5:62-6:5 (emphasis added); RIB at 30; SIB at 23. Thus, if the “insulated gate transistor is in the ON state,” it “indicates a conduction of said insulated gate transistor” since, to quote Arigna, “a significantly non-zero current is flowing through the transistor” (CIB at 12). The transistor’s “ON state” is not an added limitation, as Arigna suggests; it is the condition in which current flows through the transistor, and by extension, “indicates a conduction of said insulated gate transistor.” Respondents’ and Staff’s construction is thus confirmed by the intrinsic record.

Furthermore, the claimed “insulated gate transistor” has an “ON state”—the '835 patent states that it does. '835 patent at 5:62-65 (“transistor 12 comes to be in ON state”). The specification uses “ON state,” and Arigna has provided zero basis for why “is turned on” is more correct or more accurate. As Staff correctly points out, Arigna’s construction might leave open the chance for Arigna to argue that “the transistor is ‘turned on’ whenever it is receiving a signal input even if the signal input is below the saturation threshold needed to switch the transistor to its ‘ON state’ and cause it to be conducting” (SIB at 24), which is likely Arigna’s endgame in injecting this ambiguous phrase. By contrast, Respondents’ and Staff’s construction is well-rooted in the intrinsic record, and should be adopted. RIB at 29-30; SIB at 23-24.

E. “significant” (claims 1 and 2)

Complainant’s Proposed Construction	Respondents’ Proposed Construction	Staff’s Proposed Construction
<u>No construction necessary. To the extent a construction is necessary, then the plain and ordinary meaning, e.g. active</u>	Plain meaning, <i>i.e.</i> large or important enough to have a meaningful effect, <i>e.g.</i> a HIGH potential state	active-high or active-low state indicating a condition is met

Respondents agree with Staff that Arigna’s proposed construction “suffers from a lack of clarity,” and that “[i]t could be problematic if Complainant were during the infringement stage

permitted to label nearly any signal output as ‘significant’ or ‘active’”—which would be contrary to the claims and specification. SIB at 28. As the Staff correctly argues, “the ‘significant’ signal limitations were a central part of the patent examiner’s stated reasons for allowance of the asserted patent claims. *See* Staff Ex. 12 (10/19/2006 Notice of Allowance). It is thus important to get this construction as precise as possible.” SIB at 14-25; Staff Ex. 12 at 4 (referring to independent claim 2, which issued after amendment as asserted claim 1).

Respondents’ proposed construction is precise and supported by the intrinsic and extrinsic evidence. RIB at 33, collecting dictionary definitions attached as Resp. Exs. 11, 12, 13, 21. Respondents’ construction does not exclude a LOW potential state. Respondents included the phrase “*e.g.*” in “*e.g.*, a HIGH potential state” in order for their construction to encompass that a LOW potential state could potentially also be considered significant. RIB at 34 (“Respondents’ proposed construction is not limited to a “high” or “H” potential state. For example, if the baseline of the signals ... was high/ON ..., then the “low” or “L” OFF state could potentially be considered significant.”). Therefore, Respondents’ would not object to a construction reading: “Plain meaning, *i.e.* large or important enough to have a meaningful effect, *e.g.* a HIGH potential state or a LOW potential state.”

Respondents agree with much of Staff’s construction, but remain concerned that it may leave open some potential for Arigna to twist Staff’s construction in an unintended way. For example, Arigna could attempt to point to a HIGH state and a LOW state in the same pulse signal, and then wrongly claim both signal states are “significant” because HIGH indicates an “ON” condition and LOW indicates an “OFF” condition. But Respondents’ and Staff’s briefs both explain at length why the “significant” condition is HIGH if the baseline is LOW, and LOW if the baseline is HIGH—the baseline state is not the claimed “significant” condition. SIB at 26

(“A pulse signal is a digital signal with only two states: HIGH and LOW.”) (“[T]he ‘significant’ condition for the pulse signals S2 and S4 always represents a change from the baseline (HIGH or LOW) condition that directly correlates to a particular condition or event having occurred.”) (citing ’835 patent at 10:17-26 & FIG. 5); RIB at 33 (“[I]f the baseline of the signals above in Figure 5 was high/ON (instead of low/OFF as depicted), then the “low” or “L” OFF state could potentially be considered significant.”). Put another way, HIGH and LOW states cannot both be “significant” at the same time—one state is the baseline condition of the signal, and the other state is “significant.” A signal can be recognized as “significant” if it is either large or important enough to have a meaningful effect (indicating that the signal has changed from its baseline condition) or if it indicates a particular condition (*i.e.* that the signal has changed from its baseline condition).

Accordingly, although Respondents believe that their construction is more precise, in the alternative, Respondents would not object to modifying the Staff’s construction as follows (with underlining added): “active-high or active-low state indicating a condition is met, where active-high indicates a condition is met when active-low is the baseline condition, and active-low indicates a condition is met when active-high is the baseline condition”).

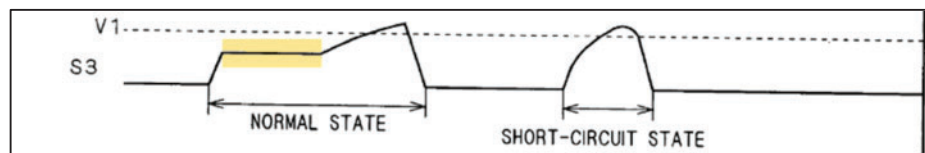
F. “clamped constantly” (claim 2)

Complainant’s Proposed Construction	Respondents’ Proposed Construction	Staff’s Proposed Construction
held at a constant voltage	clamped to a certain voltage for a determined period by a Miller effect	held at a constant voltage

Complainant and Staff incorrectly argue that, because there are several ways to clamp the voltage of signals generally, “clamped constantly” must mean simply “held at a constant voltage.” *See* SIB at 31; CIB at 17. However, claim 2 is not directed to clamping the voltage of

signals generally—clamped constantly means more in the context of the claim. *See Atlas IP, LLC v. Medtronic, Inc.*, 809 F.3d 599, 605 (Fed. Cir. 2005) (“although ‘establish’ might mean ‘initiate’ in some contexts, it must mean more in this context”).

Claim 2 recites that the “predetermined period” of claim 1 is set based on a period of time when the claimed “control output signal” behaves in the claimed way during normal operation of the insulated gate transistor. Thus, contrary to Arigna’s argument (CIB at 17), the Applicants did “recite in the claims how or why S3 is... ‘clamped constantly’ ‘to a certain voltage... .’” As Arigna admits, “FIG. 5 shows what ‘clamped constantly’ means” (CIB at 16)—and it shows the impact of the Miller effect on the voltage of claimed control output signal S3 during the “normal state” of operation of transistor 12. The portion of control output signal S3 that is “clamped to a certain voltage for a determined period by a [Miller] effect” is reflected below, annotated in gold:



’835 patent at Fig. 5 (annotation added as described in text above).

The disputed term “clamped constantly” must be construed in the context of the invention described in the specification and as understood in the field of electrical engineering. *See Netword*, 242 F.3d at 1352 (“The claims are directed to the invention that is described in the specification; they do not have meaning removed from the context from which they arose.”); *Toro Co.*, 199 F.3d at 1299 (“Determining the limits of a patent claim requires understanding its terms in the context in which they were used by the inventor, considered by the examiner, and understood in the field of the invention.”).

As described in Respondents’ and Staff’s initial briefs, the purported invention of the ’835 patent relies on differences in the voltage of the claimed control output signal between

normal operation and a short-circuit state in order to detect whether there has been a short-circuit without use of a shunt resistor. RIB at 8; SIB at 9-10 (“The short circuit protection mechanism of the ’835 Patent is based on recognition by the patent inventors that, in the event of a short circuit condition, ‘the control output signal’ that is supplied to the gate of the switching transistor in their semiconductor device module will also be transformed.”). The difference that the patent relies upon is whether the voltage of the control output signal supplied to the gate of an insulated gate transistor is clamped constantly for a predetermined period—which is caused by the Miller effect in normal operation of the insulated gate transistor—or whether the voltage spikes rapidly instead, indicating a short-circuit. ’835 patent at 5:62-6:3, 6:54-67. Claim 2 recites:

2. The semiconductor device according to claim 1, wherein said predetermined period when said first pulse signal is significant is set on a basis of a period when a voltage of said control output signal is clamped constantly when said insulated gate transistor normally operates.

’835 patent, claim 2.

The specification only discloses one way to clamp constantly the claimed “voltage of said control output signal [S3 or S13]” “when said insulated gate transistor normally operates” that is consistent with claim 2. This clamping for a period in normal operation, as shown in Figure 5, is due to the well-known electrical engineering phenomenon called “a mirror [sic: Miller] effect.” ’835 patent at 5:62-6:3 (“a voltage of the control output signal S3 is clamped to a certain voltage for a determined period by a mirror [sic: Miller] effect”); Ex. 15 (attaching 122-year-old Miller effect paper); Exs. 16-17 (translations of original Japanese applications) at [050]. When transistor 12 “normally operates,” “the transistor 12 which is the insulated gate type switching device such as the IGBT and so on has a characteristic that its control output signal S3 is clamped to a certain voltage for the determined period after its rising.”). ’835 patent at 6:6-10.

“The present invention [of the ’835 Patent] is focused on this phenomenon, and it detects the short-circuit by monitoring the control output signal of the insulated gate transistor[.]” *Id.* at 4:20-23 (emphasis added). Thus, when the control output signal does not behave in accordance with the Miller effect, “[t]he present invention...focused on this phenomenon...detects the short-circuit.” *Id.* at 4:20-23; *see also id.* at 4:18-20 (“[W]ith regard to the insulated gate transistor, the control output signal is also influenced when that transistor is short-circuited, a signal waveform different from that in a normal operating state occurs.”); *id.* at 6:54-64 (when “control output signal S3 [is] in a short circuit state” “the clamp period of the voltage does not exist...and the voltage of the control output signal rises rapidly”); *id.* at 6:65-67 (“when the transistor 12 is short-circuited, the voltage of the control output signal S3 rises rapidly and exceeds the reference voltage V1”).

The Staff points out that the specification describes using a particular type of circuit element called a Zener diode to clamp a different signal—the reference voltage V1, shown as a dotted line in Figure 5. SIB at 31, citing ’835 patent at 4:43-49. This clamping of V1 is unrelated to the claimed clamping of the control output signal S3 when the insulated gate transistor is in the normal state, and thus has nothing to do with claim 2. Respondents thus respectfully request that the Court construe “clamped constantly” as “clamped to a certain voltage for a determined period by a Miller effect.” *See Netword*, 242 F.3d at 1352 (claims must be construed in context of invention described in specification); *Toro*, 199 F.3d at 1299 (same).

G. “control output signal” (claim 1)

Complainant’s Proposed Construction	Respondents’ Proposed Construction	Staff’s Proposed Construction
<u>No construction necessary. To the extent a construction is necessary, then the plain and ordinary meaning,</u>	signal supplied to the gate of an insulated gate transistor to switch the	signal supplied to the gate of an insulated gate transistor to switch the

e.g., output signal that is controlling an insulated gate transistor	transistor between ON and OFF states	transistor between ON and OFF states
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Arigna argues that no construction is necessary for the term “control output signal” but proposes a “plain and ordinary meaning” that differs from Respondents’ and Staff’s construction. CIB at 18. The parties’ dispute as to the “plain and ordinary meaning” of the term necessitates a construction. *O2 Micro*, 521 F.3d at 1361. Arigna mischaracterizes any teaching from the specification reflected in Respondents’ and Staff’s construction as “import[ing] limitations from the specification.” CIB at 18. But “[t]he ordinary meaning of a claim term is not ‘the meaning of the term in the abstract.’ Instead, ‘the ‘ordinary meaning’ of a claim term is its meaning to the ordinary artisan after reading the entire patent.’” *Eon Corp. IP Holdings v. Silver Spring Networks*, 815 F.3d 1314, 1320 (Fed. Cir 2016) (quoting *Phillips*, 415 F.3d at 1321). “The claims are directed to the invention that is described in the specification; they do not have meaning removed from the context from which they arose.” *Netword*, 242 F.3d at 1352.

Arigna suggests that “it is instructive to read [the term] in the context of the claims, where the term ‘control output signal’ appears nine times in Claim 1.” CIB at 18. Arigna then lists purported “qualities” of the “control output signal,” concluding “[n]othing more is needed to define the ‘control output signal.’” CIB at 19. Arigna ignores a critical aspect of the “control output signal”—what it is supposed to do in the context of the claimed invention. As discussed above in Sections II.A. and II.C., the preamble provides the important structural detail that the “control output signal” must be connected to the gate of the transistor to “control[] [the] drive of” the transistor. *See also* RIB at 39-41; SIB at 31-34; ’835 patent at 4:14-15, 5:62-65. Arigna ignores these critical disclosures, focuses only on the express recitation of the phrase “control output signal” in the claim, and fails to identify the function performed by the “control output signal.” CIB at 19. Arigna’s argument is puzzling in view of its own proposal for the term

(“output signal that is controlling an insulated gate transistor”), which finds no support in Arigna’s list. *Id.* at 18. By contrast, Respondents’ and Staff’s construction correctly reflects that the “control output signal” is the “signal supplied to the gate of an insulated gate transistor to switch the transistor between ON and OFF states.” RIB at 39-41; SIB at 31-34.

Arigna’s other criticism of Respondents’ and Staff’s construction is that the use of the phrase “to switch the transistor between ON and OFF states” will supposedly “complicate[] the claim and introduce[] two terms (‘ON state’ and ‘OFF state’) that need further defining.” CIB at 19. As discussed above in the context of the “indicates a conduction of said insulated gate transistor” term, there is no ambiguity that the claimed “insulated gate transistor” has an “ON state” and an “OFF state,” nor is there any confusion as to what constitutes the “ON state” of the transistor. The ’835 patent explains that “when a voltage of the control output signal S3 exceeds a threshold value of the transistor 12, the transistor 12 comes to be in ON state.” ’835 patent at 5:62-6:5. If the voltage of the control output signal is below the transistor’s threshold voltage, the transistor remains in the “OFF state.” RIB at 40-41; SIB at 32-33.

Furthermore, it is Arigna’s construction that “unduly complicates the claim” and needs further defining. As explained in Respondents’ and Staff’s initial briefs, Arigna’s construction is simply a rearrangement of the term “control output signal,” and provides no clarity regarding how it is supposed to “control[] an insulated gate transistor.” RIB at 40-41; SIB at 32-33. By contrast, Respondent’s and Staff’s construction reflects the ’835 patent’s teachings that (1) the “control output signal” is supplied to the gate of the “insulated gate transistor” (’835 patent at 3:3-7; 3:36-40; 4:14-20; 4:32-33; 7:57-59; RIB at 40); and (2) that the voltage of the “control output signal” causes the “insulated gate transistor” to switch from its OFF state to ON state, or vice-versa (’835 patent at 5:62-6:5; RIB at 41). Arigna’s vague construction is yet another

attempt to impermissibly broaden its claims to encompass circuits that were never intended by the patentee to fall within the scope of the alleged invention.

H. “short-circuit protection circuit” (claim 1)

Complainant’s Proposed Construction	Respondents’ Proposed Construction	Staff’s Proposed Construction
No construction necessary. To the extent a <u>construction is necessary, then the</u> plain and ordinary meaning, e.g. circuit that performs function of short-circuit protection	circuit that performs short-circuit protection without a shunt resistor	circuit that performs short-circuit protection without a shunt resistor

The issue with respect to this term is straightforward—should Arigna be held to the purported invention disclosed in the specification, *i.e.*, a circuit that performs short-circuit protection without a shunt resistor, or not. RIB at 41-46; SIB at 34-37. Clearly, Arigna should. Arigna argues that no construction is necessary, but its proposed alternative construction would broaden claim 1 far beyond the alleged invention. The specification clearly and unambiguously describes the invention as a device that realizes a short-circuit protection function without the use of a shunt resistor. The specification repeatedly disparages conventional prior art systems’ use of shunt resistors and touts the benefit of the purported invention as the ability to perform the same short-circuit protection functions without a shunt resistor. RIB at 43-46; SIB at 35-37. Indeed, as the Staff correctly states, “[t]he crux of the invention and sole purported advance over the prior art is a switching device that includes short-circuit protection *without a shunt resistor*.” SIB at 35-36 (emphasis in original). Arigna’s alternative construction would improperly encompass the prior art systems disparaged and distinguished from the purported invention.

Arigna wrongly argues that the phrase “short-circuit protection circuit” need not be construed, and that the “claim itself provides the full definition” of the term by describing functions performed by the circuit and its components. CIB at 20-22. Arigna cannot be correct,

as this argument would render superfluous the claim language “short-circuit protection.” If the functions and components recited in the claims fully defined the circuit, then the phrase “short-circuit protection circuit” could simply be replaced with “circuit,” and the claims would have the same scope. *See, e.g., Intel Corp. v. Qualcomm Inc.*, 21 F.4th 801, 809–10 (Fed. Cir. 2021) (“It is highly disfavored to construe terms in a way that renders them void, meaningless, or superfluous.”); *Becton, Dickinson & Co. v. Tyco Healthcare Grp., LP*, 616 F.3d 1249, 1257 (Fed. Cir. 2010) (“Claims must be ‘interpreted with an eye toward giving effect to all terms in the claim.’”) (quoting *Bicon, Inc. v. Straumann Co.*, 441 F.3d 945, 950 (Fed. Cir. 2006)); *See also Elektro Instrument S.A. v. O.U.R. Scientific Int’l, Inc.*, 214 F.3d 1302, 1305–07 (Fed. Cir. 2000) (refusing to adopt a claim construction which would render claim language superfluous); *Cat Tech LLC v. TubeMaster, Inc.*, 528 F.3d 871, 885 (Fed. Cir. 2008) (same).

Arigna also levies two incorrect criticisms of Respondents’ and Staff’s construction. First, Arigna wrongly contends that the construction imports a limitation from the title. CIB at 22. The title supports Respondents’ and Staff’s understanding that the invention is directed to a circuit that “realizes a short-circuit protection function without shunt resistor” (’853 patent at Title), particularly given that this phrase was added during prosecution to be “indicative of the invention to which the claims are directed.” RIB at 43 n.5; SIB at 35. However, Respondents and Staff do not argue that the title, standing alone, operates as a disclaimer. The specification also clearly and unambiguously distinguishes use of a shunt resistor from the claimed invention and its benefits. RIB at 41-46; SIB at 35-36.

Second, Arigna wrongly contends that there is no disclaimer of the use of shunt resistors in the specification because (1) the “specification does not say that a shunt resistor is ‘prohibited’ or eliminated,” and (2) that “the Examiner did not refer to the absence of a shunt resistor in

allowing the claims.” CIB at 22. However, Arigna’s cited authority fails to support that disclaimer applies only in these circumstances. On the contrary, in *GE Lighting*, the Federal Circuit found that disclaimer can arise where, as here, “the patent repeatedly disparaged an embodiment ... and then detailed the ‘deficiencies [that] make it difficult’ to use.” *GE Lighting Sols., LLC v. AgiLight, Inc.*, 750 F.3d 1304, 1309 (Fed. Cir. 2014); *see also* RIB at 42-43 (citing cases in accord). Arigna’s reliance on *Ethanol Boosting* is similarly misplaced. There, the Federal Circuit found no disavowal of single-fuel systems in the specification at issue, in part because the specification disclosed embodiments with single-fuel systems. *Ethanol Boosting Sys., LLC v. Ford Motor Co.*, No. 2021-1949, 2022 WL 2798395, at *2 (Fed. Cir. July 18, 2022). Unlike the patent at issue in *Ethanol Boosting*, the ’853 patent (1) repeatedly and unambiguously disparages the use of shunt resistors in prior art systems, (2) discloses only embodiments which operate without the use of a shunt resistor, and (3) touts the benefits of the invention arising from performing short-circuit protection without a shunt resistor.

Therefore, the ’835 patent clearly and unambiguously disclaims the use of shunt resistors. RIB at 41-46. Because Respondents’ and Staff’s construction adheres to the clear and unambiguous teachings of the patent specification, the ALJ should adopt it.

III. CONCLUSION

For the foregoing reasons, Respondents request that the ALJ adopt their proposed constructions.

Dated: August 19, 2022

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**UNITED STATES INTERNATIONAL TRADE COMMISSION
Washington, D.C.**

**Before the Honorable Monica Bhattacharyya
Administrative Law Judge**

In the Matter of

**CERTAIN POWER
SEMICONDUCTORS, AND MOBILE
DEVICES AND COMPUTERS
CONTAINING SAME**

Inv. No. 337-TA-1308

**APPENDIX OF EXHIBITS IN SUPPORT OF RESPONDENTS' REBUTTAL
CLAIM CONSTRUCTION BRIEF**

Exhibit 20	AN-7513 - Application Note, June 1993, Parallel Operation of Semiconductor Switches
Exhibit 21	<i>Motor Drive Technologies for the Power-By-Wire (PBW) Program: Options, Trends and Tradeoffs Part II: Power Electronic Converters and Devices</i> , Malik E. Elbuluk and M. David Kankam
Exhibit 22	<i>Electrothermal Analysis of Latch0Up in an Insulated Gate Transistor (IGT)</i> , Hermann Brand and Siegfried Selberherr
Exhibit 23	Ground Rule 6.1 Joint Disclosure of Disputed Claim Term Constructions

EXHIBIT 20

In uninterruptable power supplies demands for current handling capability to meet load current In uninterruptable power supplies demands for current handling capability to meet load current requirements plus margins for overload and reliability purposes often exceed the capability of the largest semiconductor device type considered and paralleling may become an attractive alternative. All switching power semiconductors starting with SCR's [1], bipolar transistors [2-4] darlington's [5] and field effect transistors [6-10], have been successfully paralleled, but proper precaution had to be taken. We will review some of these methods, describe the characteristics of the insulated gate transistors, and show the proper methods to operate this relatively new family of devices in parallel.

All semiconductor circuits using parallel connected devices to switch a higher load current can easily be analyzed by using Kirchoff's law. As long as all voltage drops in the parallel branches are equal, the currents through the branches are equal.

This sounds sensible and logical, but as soon as we consider the different stages every switching device has to assume and we consider the parameters of each switching device which guarantees equal voltage drops in the branches over the required temperature range and over the duration of the switching cycle, complications begin to appear.

At first glance, each switching device has only two functional states, an "off-state" and an "on-state". But by closer examination, we have to consider how we get from "off" to "on" and back to "off", the "dynamic" area of the switching waveform

(Figure 1). The dynamic area is only a fraction of the total waveform, but it is by far the most important when it comes to parallel operation.

In power electronics, there are three different load types; resistive, capacitive, and inductive. The resulting waveforms are sufficiently different to require either different switching devices or the circuit designer may have to change the switching circuit to meet the different requirements, especially when devices are operated in parallel.

Off-State

The off-state is probably the least demanding state in parallel operation of semiconductor devices. As long as leakage current is low, even differences of more than 100% would not create any difficulties.

On-State

The on-state is again a relatively uncritical and uneventful period (Figure 2). Most devices in switching applications are overdriven and differences in gain or transconductance do not translate into proportional output current.

Even if a bipolar device takes a larger share of the total current, the rapid fall-off in gain and the increase in V_{SAT} as it takes the higher share will prevent disaster. Thermal runaway in bipolar applications is not as frequent as we may believe [2-4].

For bipolar devices, the parameter having a clear negative temperature coefficient is V_{BE} . $V_{CE(SAT)}$, on the other hand, can have positive or negative temperature coefficient depending on the device type (npn or pnp) and operating point.

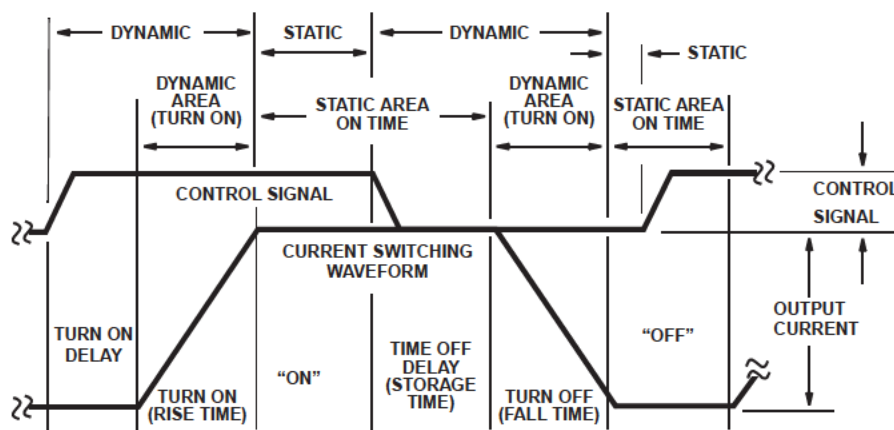


FIGURE 1. SWITCHING WAVEFORM DEFINITIONS

The ease of paralleling of power FETs has been pointed out by many authors [6-9], and has been demonstrated in many applications, although each application requires analysis of both dynamic and static sharing.

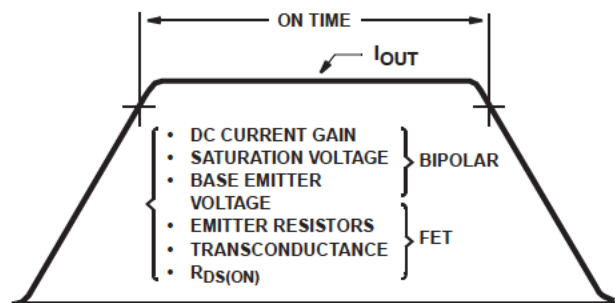


FIGURE 2. ON TIME OF SWITCHING WAVEFORM AND CONTROLLING PARAMETERS

Turn-On Delay Time

Turn-on delay time is the time from where the control signal is applied, reaches 10% amplitude, to the point where the switched current rises to the 10% amplitude (Figure 3).

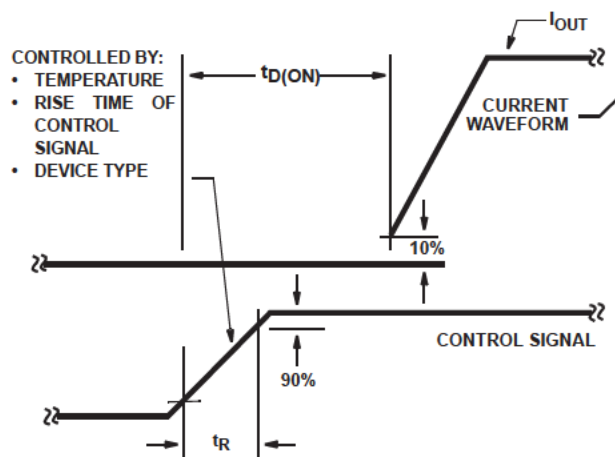


FIGURE 3. DEFINITION OF TURN-ON, DELAY TIME, $t_{D(ON)}$ AND CONTROLLING PARAMETERS

Fortunately, differences in turn-on delay are relatively small. Although this delay is significant in large-area SCR's, but it is much less a problem with bipolars or power FET's. It is less important when switching inductive loads, but should be monitored when devices to be paralleled switch resistive load, discharge capacitor or have to carry the recovery current of a diode.

Needless to say, it is desirable to have small turn-on delays for parallel operation. To reduce $t_{D(ON)}$, it is advisable to drive devices with fast rising control signals and use devices from the same mask design. The same device type number does not guarantee that they are made from the same mask design. Therefore, devices from different manufacturers should not be intermixed.

Rise Time

Rise time is an interesting part of the switching waveform (Figure 4). The device operates in an analog domain, although for a very short time, but nevertheless, analog.

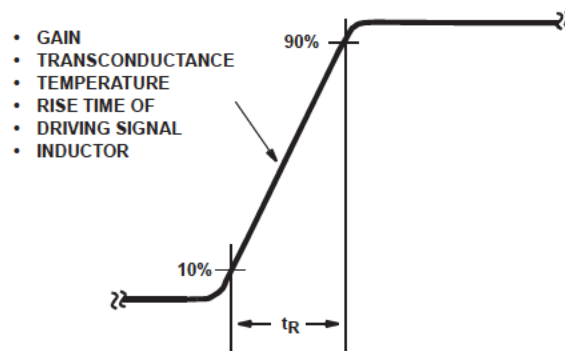


FIGURE 4. RISE TIME OF I_{OUT} WAVEFORMS AND PARAMETERS INFLUENCING IT

Again, transconductance and junction temperature become important considerations, but junction temperature differences as a result of rise time differences are relatively small. Inductors inserted into the emitter lead on bipolars, source lead on FET's or cathode lead on diodes, can be extremely effective [3]. All differences in turn-on delay and rise time become visible at thin part of the waveform. Differences which may exist, although small, require the evaluation of the forward biased safe operating area (FBSOA).

In most cases, transistors have almost rectangular FBSOA for the short durations they remain in the analog domain of the turn-on period. Problems seldom exist, but precautions should not be ignored either.

Note that the device with the shortest turn-on delay and the shortest rise-time will take most of the current. Most transistors have a negative temperature coefficient of input voltage and Miller effect feedback which can cause current hogging if power dissipation is high during turn on.

Turn-Off Delay Time (Storage Time)

Turn-off delay time is the prelude to the most important part of the switching waveform, especially on bipolar devices (Figure 5). On bipolar devices, it is important to remove the stored charge as fast as possible, which may require more expensive drive circuitry. Especially on large power darlington, negative bias or baker clamps result in significant reduction of storage time and improve parallel operations. The transition time of the base current signal from positive to negative (npn device) is important in the removal rate of the stored charge.

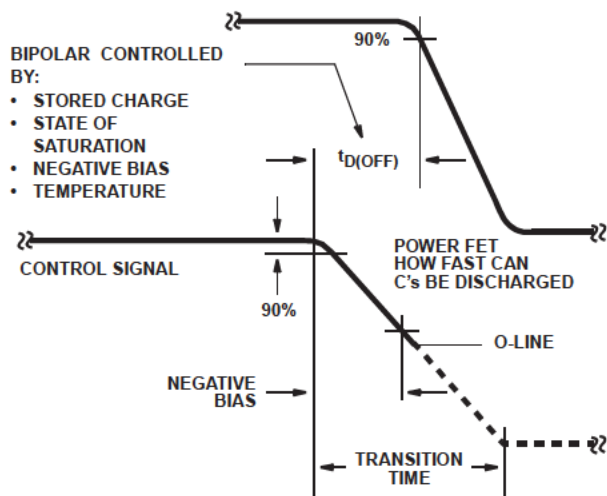


FIGURE 5. TURN-OFF WAVEFORM AND PARAMETERS INFLUENCING IT

Fall Time

Parameters which reduce storage time will also reduce fall time (Figure 6). For paralleled devices, differences in turn-off delay or storage time will have a noticeable effect on fall time.

When inductive loads are turned off, the reverse biased safe operating area (RBSOA) must be considered on bipolar devices. Hot spot formation [11] which results in sudden reduction of the V_{BE} and further increase in I_B could result in permanent damage.

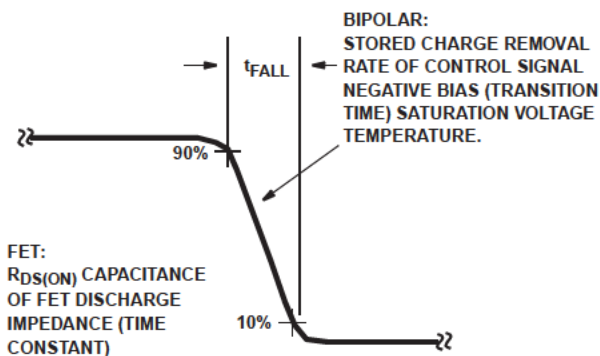


FIGURE 6. FALL TIME AND INFLUENCING PARAMETERS

The Insulated Gate Transistor

The insulated gate transistor (IGT) combines the high input impedance, voltage controlled turn on/turn off capabilities of power MOSFETs and the low on-state conduction losses of bipolar transistors, making it an ideal device for many power electronics switching control applications.

IGT Structure and Operation

The basic device structure is illustrated by the unit cell cross section of Figure 7. Like the MOSFET, the IGT consists of many individual cells connected in parallel. Processing of the IGT is similar to the vertical D-MOS technology used in MOSFETs. In the steady state, the n-channel IGT may be modeled as a bipolar pnp driven by an n-channel MOSFET. The MOSFET supplies base current to the pnp thus the MOSFET's gate voltage controls the total current.

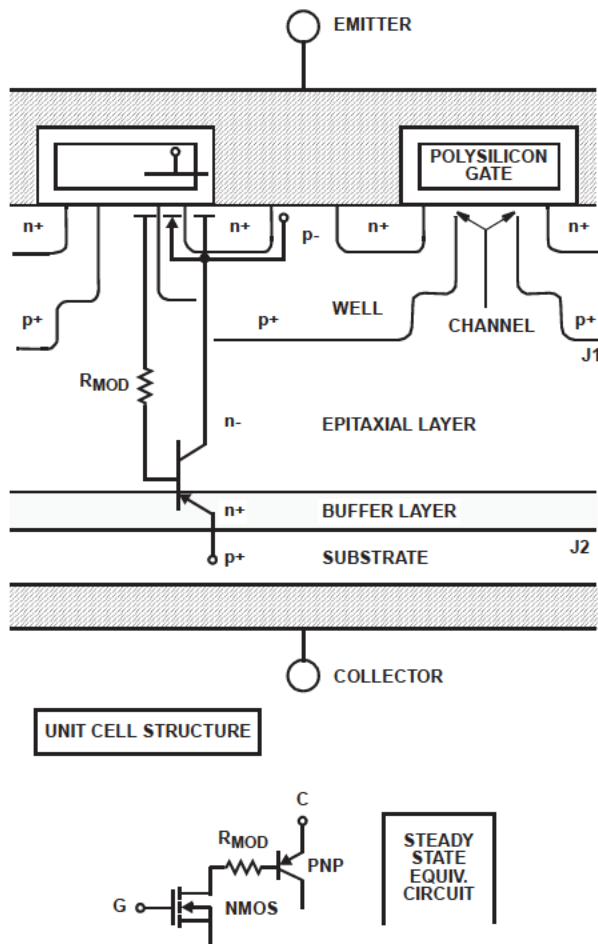


FIGURE 7. UNIT CELL CROSS SECTION AND STEADY STATE EQUIVALENT CIRCUIT OF IGT TRANSISTOR.

In normal operation, the emitter is grounded, the collector biased positive and with no gate-emitter voltage applied; J1 is reverse biased. The device is in the forward blocking mode. When a positive voltage is applied to the gate with respect to the emitter, an inversion channel is formed under the gate and MOSFET current flows from the n+ source region into the n-epi-layer to become the base current for the pnp. Junction J2 becomes forward biased and the device enters the conduction state. Holes are injected from the bot-

tom percent region into the n-epi-layer. The injected minority carrier density is 100 to 1000 times higher than the doping level of the n-type epi-region. This conductivity modulation allows the IGT to operate at a forward conduction current density 20 times that of an equivalent MOSFET. It is primarily in the thick epi, high-voltage devices where conductivity modulation has its major impact to reduce on-resistance.

The typical output characteristics and the symbol of the IGT are shown in Figure 8. Like on MOSFETs, the output characteristics curves are generated by plotting collector emitter currents, collector emitter voltage. Unlike the MOSFET, there is an offset voltage generated by the collector emitter junction of the npn-transistor. However, once this offset is overcome, the effective on-resistance in the saturation region is much lower for the IGT than for the MOSFET.

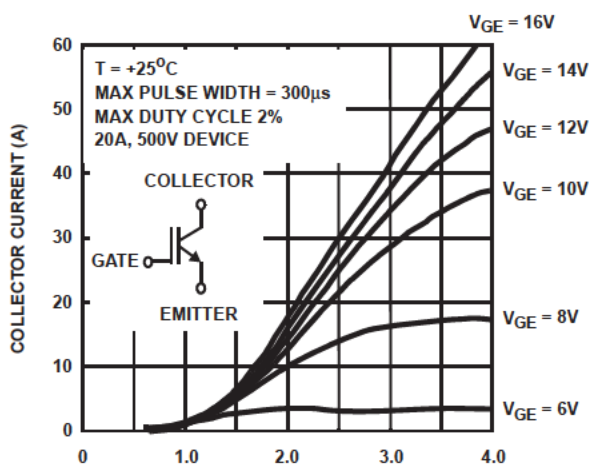


FIGURE 8. OUTPUT CHARACTERISTICS AND CIRCUIT SYMBOL FOR N-CHANNEL IGT TRANSISTOR

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Rev. H5

EXHIBIT 21

Motor Drive Technologies for the Power-By-Wire (PBW) Program: Options, Trends and Tradeoffs *Part II: Power Electronic Converters and Devices* (Part I Appeared Earlier)

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ABSTRACT

This is the second of two papers on the motor drive technology options for the Power-By-Wire (PBW). The organization of this paper is based on the four components of the electrical actuator (EA) system and the options available to suit the PBW program as given in the PBW studies. The first paper [1] discussed the options available for the motor and the controller parts of a drive. This paper discusses the power electronic converter and device options.

The power converter options are divided into hard-, snubbered- and soft-switching converters. The power device options are the MOSFET, the Insulated Gate Transistor (IGT), the gate turn-off thyristor (GTO) and the MOS Controlled Thyristor (MCT).

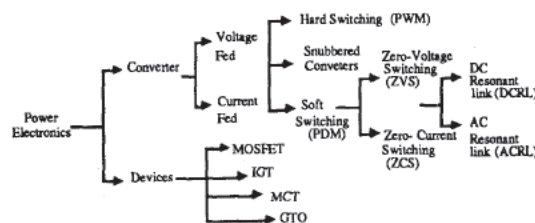


Fig. 1. Power Electronic Options for the PBW EA Systems

Each of the converter and device options is discussed, pointing out the trends and tradeoffs available and the potential for application in the PBW program.

INTRODUCTION

This and a companion paper [1] describe the options available in the four major components of an EA system, namely, the motor, the power electronic converters, the control system including the sensor requirements, and the actuator. In [1], the options available in the motor and the control and sensing schemes are discussed.

In this paper, the options available for the power electronic converters and devices with their trends and tradeoffs will be

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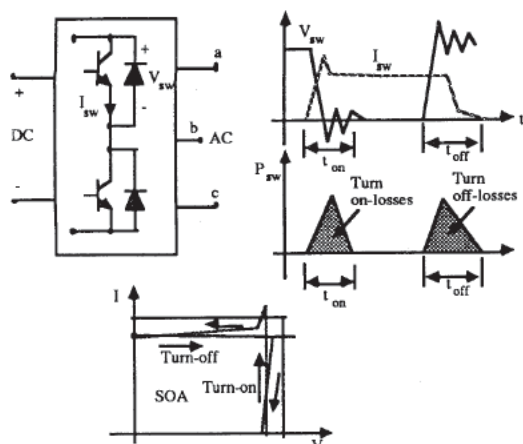


Fig. 2. Switching Device Waveforms and SOA Under Hard Switching

discussed. Fig. 1 (on previous page) shows the available options for the converters and devices.

The power converters used are the resonant link type (dc and ac), using the soft switching technique of pulse population density (PPD) or otherwise referred to as pulse density modulation (PDM) [2-4]. The Insulated Gate Transistor (IGT) has been the main switching device used in these converters. Some work has been done on the resonant ac link converter using the MOS-Controlled thyristor (MCT) [5-12]. The research and development of the PBW program continues to focus on the induction motor drives.

POWER CONVERTER OPTIONS

The performance, complexity, cost of the power electronic requirements and selection factors of the motor must be considered while designing a drive system. The converters are classified as voltage- and current-fed types, depending on the supply source. Based on its switching, each converter is further classified into three types, namely, the hard switching, the snubbed and the soft switching converters [16].

Hard-Switching Converters [14-17]

In hard-switching converters, the switching device is stressed heavily during turn-on and turn-off. At turn-on the device voltage drops after the load current is attained, and at turn-off, the device voltage rises before the current reaches zero. Stray effects such as capacitance, inductance and diode reverse recovery further increase the switching losses. Example of a hard switching converter is the pulse width modulation (PWM) inverter which has replaced the square wave inverter. The PWM inverter has been implemented in many of the commercially available induction motor and BLDC drives [15]. In this technique the ac source voltage is converted to an uncontrolled dc voltage which is then converted to ac variable voltage and frequency, using

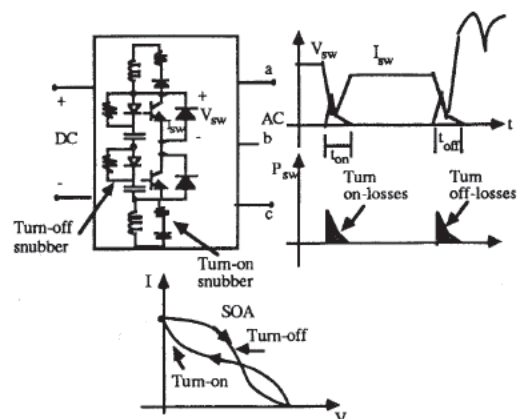


Fig. 3. Switching Device Waveforms and SOA Under Snubbed Switching

sinusoidally varying pulse width. Harmonics are shifted to a much higher frequency, resulting in low filtering requirements in nearly sinusoidal load current. Figure 2 shows a typical switch voltage and current waveforms in a PWM dc to 3-phase inverter usually used in induction motor drives. The switching device voltage and current limits of the safe operating area (SOA) may be exceeded [17].

The major consequences of hard switching are low switching frequencies, high device stress and, hence, low reliability, reduced efficiency and limited power range for the converter (i.e., not applicable in high power).

Snubbed Switching Converters [17-22]

Snubbed switching is a PWM switching modified by adding a turn-on series inductor to limit the inrush current and a turn-off parallel capacitor snubber to limit the voltage rise. The snubber reduces the stress on, and operates the device within the SOA, and facilitates diversion of the energy from being dissipated in the device during the switching transition. The parasitic elements destroy the effectiveness of the snubber, and the diode reverse recovery causes severe EMI. Fig. 3 shows a typical dc/ac switching waveforms and SOA [17].

Snubbed converters have high switching losses dissipated in the snubber and low switching frequency, and require special diodes, large inductors and low inductive power resistors.

Soft Switching Converters [2-13]

In snubber switching, normally, the stored energy is dissipated in an external resistor during a subsequent part of the switching cycle. However, a class of circuits has been shown to provide an automatic lossless resetting of the snubber network through inherent circuit operation. This allows for an oversizing of snubber network without incurring the normal penalty of trapped energy which needs to be dissipated. Such circuits are referred to as "soft switching converters."

Soft switching converters are of two types. Zero current switching (ZCS) uses purely inductive snubbers to turn-on and turn-off the device without any current in the device. Zero voltage

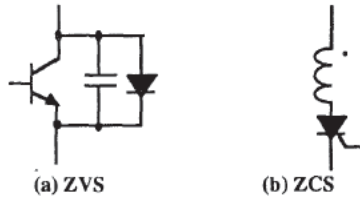


Fig. 4. Soft-Switching Elements

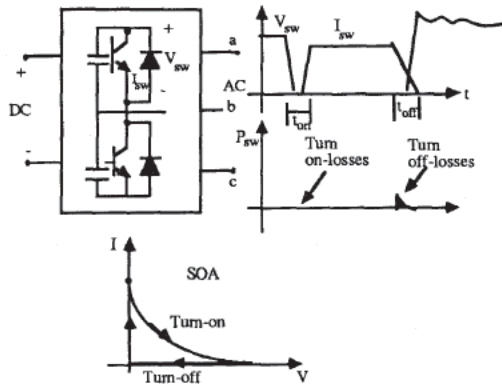


Fig. 5. Switching Device Waveforms and SOA Under ZVS

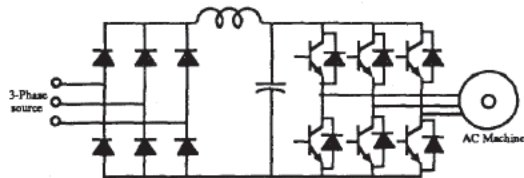


Fig. 6. Hard-Switched PWM Voltage Source Inverter

switching (ZVS) uses purely capacitive snubbers that require the device to turn-on with an antiparallel diode conducting. Fig. 4 shows the soft switch for ZVS and ZCS [12]. Fig. 5 depicts the switch waveforms and SOA under ZVS [17]. At turn-on, the device voltage equals zero prior to initial current flow, and is substantially reduced at turn-off. In this case, the parasitic elements are partially used in the circuit operation, and the diode reverse recovery is eliminated.

Soft switching reduces device losses, thereby allowing high switching frequencies, higher converter efficiency and higher reliability.

With the use of PWM voltage source inverters, the adjustable speed ac drives are economically viable and compete with the prevalent dc drive technology. The PWM permits the use of a single power stage for effecting fundamental voltage and frequency control simultaneously. A widely used 3-phase PWM voltage source inverter is shown in Fig. 6. The topology has been implemented with a wide range of power devices, including MOSFETs, BJTs, IGTs and GTOs for power ranging from 10 watts to 2 megawatts [13].

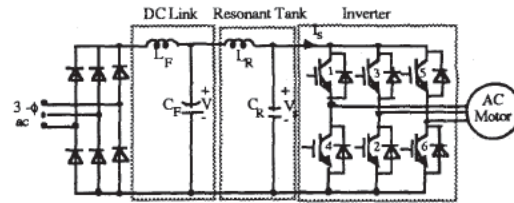


Fig. 7. The Conventional Resonant DC Link Inverter

Advantages of the PWM inverter are the simple power structure, minimum Volt-Ampere (VA) rating of the device, easy control and low cost. The disadvantages are peak stresses in the devices as a result of inductive switching (typical in motor drives) and diode reverse recovery, the need for snubbers, and low switching frequency operation which causes acoustic noise and poor control. Other disadvantages include larger reactive and filter elements, low power density, high dv/dt that results in high electromagnetic interference/radio frequency interference (EMI/RFI) and acoustic noise, and possible destructive failures [2-6].

Two alternative soft switching topologies have been proposed, and are expected to overcome many of the limitations of the PWM inverters. These are the resonant dc link converter and the resonant ac link converters, as discussed below.

Resonant DC-Link (RDCL) Converters [2-4]

Typically, the resonant dc link converter is used with a dc source, and drives a single machine. It converts a fixed dc input to a pulsating dc form [2], thereby allowing the devices to switch either at zero voltage (ZVS) or zero current (ZCS). Fig. 7 shows the conventional voltage-fed resonant dc link inverter. The actively-clamped resonant dc link inverter, one of the modifications in Fig. 7, is commonly used [13]. The clamp is proposed to limit the peak voltage stress on the devices to a reasonable value.

Compared with the PWM dc link converter, the resonant dc link offers the advantages of low switching losses, higher efficiency, lower heat dissipation and less cooling requirements, higher operating frequency and low acoustic noise, improved device reliability, and low EMI problems due to reduced dv/dt and di/dt . Also, it does not require snubbers.

Resonant AC Link (RACL) Converters [6-7, 9]

The resonant AC link is intended to operate from a single phase high frequency link, feeding many loads. It converts either a dc or a 3-phase low frequency voltage to a single-phase high frequency voltage which is then cycloconverted to a three-phase variable voltage and frequency for ac drives. The ac link voltage amplitude is maintained constant by a parallel resonant circuit as shown in Fig. 8 (on next page). This scheme has the advantages of the dc link, is bidirectional in power flow and its displacement power factor can be programmed to unity. Furthermore, the input power factor can be made unity, leading or lagging. Since the link voltage is ac, the devices have symmetric voltage blocking capability and must carry bilateral current, as shown in Fig. 8.

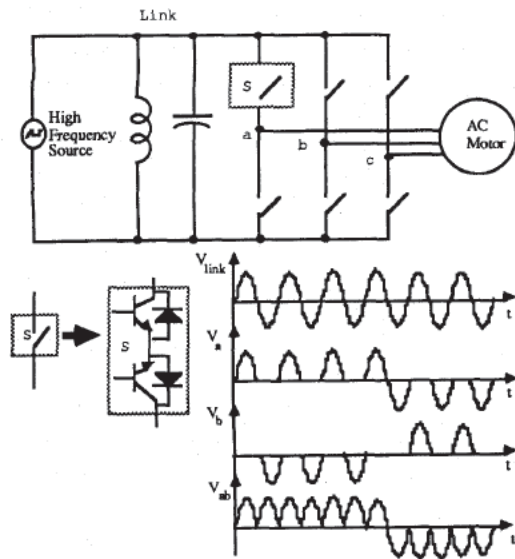


Fig. 8. The Resonant AC Link Converter System and Configuration of AC Switches

The input and output converters switch at zero voltage to synthesize the low frequency voltage waves by integral half cycle PWM method known as Pulse Density Modulation (PDM). The line currents are nearly sinusoidal, and the power flow is controllably bi-directional. The need for high frequency switches is the principal drawback of the scheme. Also, since the tank capacity is small, any small mismatch between the input and output instantaneous power will tend to modulate the link voltage. Besides, the link frequency will drift due to the loading effect. This will cause harmonic deterioration of the input and output currents, and possible system instability during fast transients [15].

Converter Comparisons and Tradeoffs

In case of the power converter, the comparison should include the type of power devices, the converter rating, the direction of power flow, the harmonic content in the supply and motor, the line power factor, the levels of electromagnetic interference (EMI) and of acoustic noise, the efficiency, the cost and the control complexity. A comparison of the voltage-fed PWM, dc and ac resonant link converters is given in [15] and summarized in Table 1. While the comparisons may generally be true, further research of the converters, their devices and the advances in control may change some of the tradeoff conclusions. For example, the control complexity could be a rapidly diminishing problem.

SEMICONDUCTOR DEVICE OPTIONS [8-16]

The power semiconductor devices constitute the heart of modern power electronic converters. The trends in the devices are important in assessing the technology of the converters.

Table 1. Comparison of Voltage-Fed Hard- and Soft-Switching Converters [15]

	PWM	R DC Link	RAC Link
Power devices	Asymmetric high frequency fast recovery diodes	High freq. asymmetric ac switches	High frequency symmetric ac switch
Rating	Few MWs	Tens of KWs	Tens of KWs
Power Flow	Only to output	to output*	Bidirectional
Load & Line Harmonics	Low load and high line harmonics	Medium Load & high line harmonics	Medium low load and line harmonics
Line power factor	Low due to high distortion current	Somewhat low	Unity, Leading or lagging possible
Acoustic noise	High	Very low	Very low
Losses & Efficiency	High switching loss, Medium Efficiency	No switching losses High efficiency	No switching losses, high efficiency
Cost	Low to med.	Medium	High
Control Complexity	less complex	Complex	Very Complex
Comments	popular Technology in most ac drives	High future potential	Topology under development

* Bidirectional power flow may be possible [15]

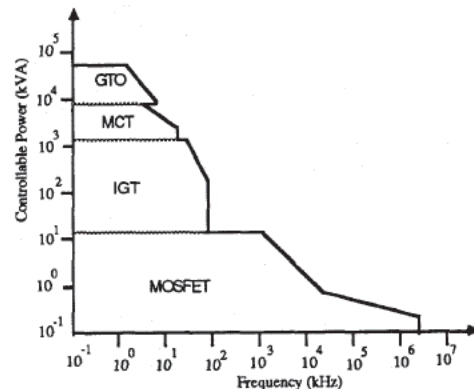


Fig. 9. Frequency and Power Ranges of Power Devices

Although the cost of a device may not exceed 20-30% of a converter total cost, the device heavily influences cost, size, weight and performance of the total power electronic apparatus. An important trend in power electronics is that the operating frequency of high power devices is continually increasing, and converter topology is undergoing modifications, constantly, to handle high frequency with high power, so as to shrink equipment size and improve its performance [15].

Four power devices have potential for application in the aforementioned power converters. These are the Gate Turn-off

thyristor (GTO), the power MOSFET, the Insulated Gate Transistor (IGT) and the MOS-Controlled thyristor (MCT). These devices are fully controlled. However, their characteristics of power and frequency application differ significantly. Fig. 9 (on previous page) compares the four devices and their projections for 1990s [15, 23-25], subject to the developments in each device. The next section discusses the devices and their suitability for the converters described above.

Gate Turn-Off Thyristors (GTO) [14-24]

The GTO is a thyristor-type device that can be turned on and off by a positive- and negative-going gate current pulses. Japanese device manufacturers have improved the GTO characteristics. GTOs with asymmetric or symmetric voltage blocking capability are currently available. The device's turn-off current gain is poor. High current concentration, during turn-off, introduced by a voltage spike in the anode voltage may create hot spots causing second breakdown. Therefore, a well designed snubber with large capacitor is necessary. The large switching losses of the GTO limit the device to a PWM frequency of 1.0-2.0 kHz. Typical uses of the GTO are in voltage source PWM inverter (600-1500 Vdc, 0.75 -1.5 kVA and 500-600 Hz) or in soft switching ZVS (1.5-6.5 kVdc, 2-12 MVA, and 700-1,200 Hz) [17]. The state of the art device ratings are about 4500 V, 3000 A [14].

Power MOSFETs

The power MOSFET is a unipolar, majority carrier, voltage controlled device. Its power rating characteristics have been improved dramatically. Concurrent sharp fall in its price has made the MOSFET a key competitor to all other devices. The device is, comparatively, extremely fast, has low switching losses and, therefore, requires minimal snubbing. Parallel a number of MOSFETs is facilitated by the inherent positive temperature coefficient of resistance which, also, causes negligible second breakdown of the device. Two drawbacks of the device are the drain resistance which increases with the voltage (V) rating (as $V^{2.5}$), and the slow reverse body diode in parallel with the device. Typically, MOSFETs are used in high frequency applications (few MHz) of few watts to few kilowatts. Typical applications can be in PWM voltage source inverters and a ZVS converter with ratings of 0-400 Vdc, 0.1-2 kVA, and 0.5-2 MHz. The device is popular in switch-mode power supplies and rarely used in ac drives [17]. However, if used in ac drives, the device will reduce the cooling requirements and increase reliability of the converter. MOSFETs are currently rated at 500 v and 140 A [14].

Insulated Gate Transistors (IGT) [13-15, 22-23]

The IGT is a hybrid MOS-gated turn on/off bipolar junction transistor (BJT) that combines the attributes of a MOSFET and a BJT. The device was commercially introduced in 1983, and since then its ratings and characteristics have been highly improved. The device offers significant advantages over the BJT in power range and

Table 2. Comparison of the GTO, IGT and MCT [15]

	GTO	IGT	MCT
Voltage & current rating	1200 V, 300 A (Peak)	600V, 100A (dc)	600V, 75A (rms)
Power Capability	4500 V, 3000 A	1200V, 400 A	To be determined
Voltage blocking	Symmetric or Asymmetric	Asymmetric	Asymmetric
Gating	Current	Voltage	Voltage
Temperature (T _j)	-40° to 125°C	-20 to 150°C	-55 to 150°C
SOA limit	Second breakdown at turn off	T _j limited	T _j limited
On-drop	4.0 V	3.2 V	1.1 V
frequency	up to 2.0 kHz	up to 50 kHz	up to 40 kHz
Turn-off current gain	4 to 5	-----	-----
Reapplied dv/dt	Limit for device loss	Limit for device loss	5,000 V/μs
Turn on di/dt	300 A/μs	Very high	1000 A/μs
Turn-on time	4.0 μs	0.9 μs	1.0 μs
Turn-off time	10 μs	1.4 μs	2.1 μs
Leakage curr.	30 mA	1.0 mA	1.0 mA
Protection	Gate inhibit or fast fuse	Gate control	Gate inhibit or fast fuse

frequency (few kilowatts to few hundred kilowatts, up to 50 kHz). The device is typically used in PWM voltage source inverter (0 -750 Vdc, 0 -300 kVA, 1.5 - 5 kHz) drives and ZVS voltage source converter (750 Vdc, 20 -150 KVA, 40 kHz) drives [17]. In such applications, the device offers the advantages of reduced cooling requirement, increased reliability, improved utilization and reduced voltage spikes at turn-off, lower module inductance and improved thermal life. Modules are available up to 600V, 400 A, or 1200V, 300A ratings. Ratings of 1200V, 500A are expected [14].

MOS-Controlled Thyristors [8-16, 22-23]

The MCT is a MOS-gated thyristor much like a GTO, but with very high turn-off current gain. It is a high power, medium frequency switching device. Its switching speed is comparable to an IGT, but has lower conduction drop. The device is currently under development. The first commercially available MCT was out in 1993 (600 V, 75A). Developmental devices were released by Harris Semiconductor (500V/1000V, 50A/100A). The device shows high hopes for future applications in drives, especially in snubbed voltage source inverters (0-400 Vdc, 0-100 KVA, 2 kHz), ZVS converter (0-400 Vdc, 20-150 KVA, 25 kHz), and ZCS converter (750 Vdc, 150 kVA, 40 KHz) drives [17]. Further competition between the MCT and the GTO is expected.

Device Comparisons and Tradeoffs [15]

From the above discussion, it seems that the candidate devices for EAs are the IGT, the GTO and the MCT. A good representative comparison between the three devices appears in [15] and summarized in Table 2 (on previous page).

CONCLUSIONS AND DIRECTIONS FOR FUTURE RESEARCH

Considerable work is done on the three ac brushless drive technologies and, as time progresses, there will be a lot of improvement in the design of motors, converters, power devices and controllers. Since there are many actuator loads in the PBW program, each of the three drives is expected to be superior to the other two drives for a specific load.

Further research in the PBW program should compare the three drive technologies in the context of the PBW load requirements. Issues of reliability and redundancy of components, continuous power or torque/speed requirements, motoring/braking operation, dynamic or regenerative braking, overload rating and duration, supply voltage and frequency, torque/inertia ratio, torque/ampere, power density, acoustic noise, protection arrangements, control and communication interface, electromagnetic interference (EMI), environmental factors, direct or gearbox drive among many other issues, remain to be closely examined and compared for the three motor drives, using actual PBW loads.

At this point, it is very difficult to favor any of the three drives over the other two, as each drive has its potential for application in the PBW program.

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EXHIBIT 22

Electrothermal Analysis of Latch-Up in an Insulated Gate Transistor (IGT)

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SUMMARY An advanced model for self-heating effects in power semiconductor devices is derived from principles of irreversible thermodynamics. The importance of the entropy balance equation is emphasized. The governing equations for the coupled transport of charge carriers and heat are valid in both the stationary and transient regimes. Four characteristic effects contributing to the heat generation can be identified: Joule heating, recombination heating, Thomson heating and carrier source heating. Bandgap narrowing effects are included. Hot carrier effects are neglected. Numerical methods to solve the governing equations for the coupled transport of charge carriers and heat are described. Finally, results obtained in simulating latch-up in an IGT are discussed.

key words: simulation, latch-up, IGT, thermodynamic, entropy

1. Introduction

In order to allow accurate computation of device characteristics and analysis of parasitic effects in modern power semiconductor devices, the electrothermal nature of such phenomena as thermal runaway, current crowding, avalanche injection, secondary breakdown and latch-up has to be accounted for. Realizing electrothermal effects a transport model for the simultaneous flow of charge carriers and heat is needed.

From a numerical point of view the simulation of transient self-heating effects in semiconductor devices requires the self-consistent solution of Poisson's equation, the continuity equations for electrons and holes and the heat flow equation in space and time.

Following a rigorous approach to treat self-heating effects, the ansatz and the derivation of the governing equations for the coupled transport of charge carriers and heat are discussed in Sect. 2. In Sect. 3, the numerical methods used to solve the system of nonlinear, coupled partial differential equations describing electrothermal interaction are described. Results obtained in investigating latch-up in an IGT are presented in Sect. 4.

2. The Mathematical Model

To derive a closed set of equations for the simultane-

ous flow of charge carriers and heat in a semiconductor device, principles of irreversible thermodynamics are utilized [3], [7], [9]. The idea is to explicitly set up the entropy balance equation for the semiconductor, to identify thermodynamic currents and conjugated forces, and to formulate the phenomenological equations. To obtain governing equations describing mutually coupled electrothermal transport phenomena, transport parameters have to be defined and specific state functions have to be evaluated [3], [7], [9].

Provided that the concept of local equilibrium is valid, the Gibbs fundamental equation for the semiconductor takes the form:

$$\frac{\partial u}{\partial t} = T \cdot \frac{\partial s}{\partial t} - q \cdot \varphi_n \cdot \frac{\partial n}{\partial t} + q \cdot \varphi_p \cdot \frac{\partial p}{\partial t} \quad (1)$$

u denotes the total internal energy per unit volume, s the entropy density. n means the electron, p the hole concentration. T is the temperature, φ_n , φ_p are the quasi-Fermi levels for electrons and holes, respectively, with q being the elementary charge. Note that u includes the energy due to the applied and built-in potential too.

The Gibbs equation (1) interrelates balances of electrodynamic and thermodynamic quantities. Usually continuity equations for charge carriers together with Poisson's equation are derived from Maxwell's equations [10].

$$\text{div } \vec{J}_n - q \cdot \frac{\partial n}{\partial t} = q \cdot R \quad (2)$$

$$\text{div } \vec{J}_p + q \cdot \frac{\partial p}{\partial t} = -q \cdot R \quad (3)$$

$\vec{J}_n$, $\vec{J}_p$ represent the current densities for electrons and holes, respectively. The net recombination rate R is introduced by definition [10]. The conservation equation for the total internal energy u reads:

$$\frac{\partial u}{\partial t} + \text{div } \vec{J}_u = 0 \quad (4)$$

$\vec{J}_u$ is the energy flux vector. Equation (4) represents the first axiom of thermodynamics in terms of vector analysis for continuous systems. Momentum balance equations are not considered, thus neglecting hot car-

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rier effects. The actual form of the entropy balance equation is obtained by substitution of continuity equations for the carrier concentrations n, p and the energy density u into the Gibbs fundamental equation (1),

$$\begin{aligned} \frac{\partial s}{\partial t} + \text{div} \left(\frac{1}{T} \cdot \vec{J}_h \right) \\ = \vec{J}_h \cdot \left(-\frac{1}{T^2} \cdot \text{grad } T \right) + \vec{J}_n \cdot \left(-\frac{1}{T} \cdot \text{grad } \varphi_n \right) \\ + \vec{J}_p \cdot \left(-\frac{1}{T} \cdot \text{grad } \varphi_p \right) + R \cdot \left(\frac{1}{T} \cdot q \cdot (\varphi_p - \varphi_n) \right) \end{aligned} \quad (5)$$

where

$$\vec{J}_h \equiv \vec{J}_u - \varphi_n \cdot \vec{J}_n - \varphi_p \cdot \vec{J}_p \quad (6)$$

is a definition of the heat flux $\vec{J}_h$.

The right-hand side of (5) is the local production of entropy. Due to the first postulate of irreversible thermodynamics it can be interpreted as the sum of products of thermodynamic currents and conjugated forces. Furthermore, exploiting the second postulate of irreversible thermodynamics, that each flux linearly depends on all thermodynamic forces [3], the so-called phenomenological equations result:

$$\begin{bmatrix} \vec{J}_n \\ \vec{J}_p \\ \vec{J}_h \\ R \end{bmatrix} = \begin{bmatrix} L_{nn} & 0 & L_{nT} & 0 \\ 0 & L_{pp} & L_{pT} & 0 \\ L_{Tn} & L_{Tp} & L_{TT} & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix} \cdot \begin{bmatrix} -\frac{1}{T} \text{grad } \varphi_n \\ -\frac{1}{T} \text{grad } \varphi_p \\ -\frac{1}{T^2} \text{grad } T \\ \frac{1}{T} \cdot q \cdot (\varphi_p - \varphi_n) \end{bmatrix} \quad (7)$$

Due to Onsager's symmetric reciprocal relations, known as the third postulate of irreversible thermodynamics, the number of independent kinetic coefficients in Eq.(7) can be reduced. Thus only conductivities σ and thermoelectric powers P for electrons n and holes p , respectively, have to be defined, together with the thermal conductivity χ .

$$\begin{aligned} \sigma_n &\equiv \frac{L_{nn}}{T} & P_n &\equiv -\frac{L_{nT}}{T^2 \cdot \sigma_n} \\ \sigma_p &\equiv \frac{L_{pp}}{T} & P_p &\equiv \frac{L_{pT}}{T^2 \cdot \sigma_p} \\ \chi &\equiv \frac{L'_{TT}}{T^2} - \sigma_n \cdot P_n^2 \cdot T - \sigma_p \cdot P_p^2 \cdot T \end{aligned} \quad (8)$$

The resulting current relations (9)-(11) for the thermoelectric transport in a semiconductor include both limiting cases, (i) flow of electric charge due to the imposition of the quasi-Fermi potential, and (ii) flow

of heat caused by a temperature gradient:

$$\vec{J}_n = \sigma_n \cdot (-\text{grad } \varphi_n + P_n \cdot \text{grad } T) \quad (9)$$

$$\vec{J}_p = \sigma_p \cdot (-\text{grad } \varphi_p - P_p \cdot \text{grad } T) \quad (10)$$

$$\vec{J}_h = -T \cdot P_n \cdot \vec{J}_n + T \cdot P_p \cdot \vec{J}_p - \chi \cdot \text{grad } T \quad (11)$$

If Eqs.(9)-(11) are reformulated in terms of the total current density $\vec{J} = \vec{J}_n + \vec{J}_p$ and the heat flux $\vec{J}_h$, the thermal conductivity χ has to be redefined in order to include the bipolar contribution. L'_{TT} assumes a lattice, an electron and a hole contribution.

With the heat flux (11) the entropy balance equation (5) can be transformed into the heat flow equation (12):

$$\begin{aligned} T \cdot \frac{\partial s}{\partial t} + \text{div} (-T \cdot P_n \cdot \vec{J}_n + T \cdot P_p \cdot \vec{J}_p - \chi \cdot \text{grad } T) \\ = -\vec{J}_n \cdot \text{grad } \varphi_n - \vec{J}_p \cdot \text{grad } \varphi_p + q \cdot R \cdot (\varphi_p - \varphi_n) \end{aligned} \quad (12)$$

The expansion of the divergence operator and some algebraic operations yield:

$$\begin{aligned} T \cdot \frac{\partial s}{\partial t} + \text{div} (-\chi \cdot \text{grad } T) \\ = \frac{\vec{J}_n \cdot \vec{J}_n}{\sigma_n} + \frac{\vec{J}_p \cdot \vec{J}_p}{\sigma_p} \\ + \vec{J}_n \cdot (\text{grad}(T \cdot P_n) - P_n \cdot \text{grad } T) \\ - \vec{J}_p \cdot (\text{grad}(T \cdot P_p) - P_p \cdot \text{grad } T) \\ + q \cdot R \cdot (\varphi_p - \varphi_n) \\ + T \cdot P_n \cdot \text{div } \vec{J}_n - T \cdot P_p \cdot \text{div } \vec{J}_p \end{aligned} \quad (13)$$

The right-hand side of Eq.(13) is the heat generation. It can be shown that (13) implies Thomson's laws.

The entropy density has to be regarded as a state function of the temperature and the carrier concentrations $s = s(T, n, p)$. Furthermore, the quasi-Fermi levels are considered as state functions of the electrostatic potential ψ , the carrier concentrations n, p , the temperature T , and the effective intrinsic carrier concentration n_{ie} to fit heavy doping effects [10]. Using Maxwell's relations [3], [12] and Boltzmann statistics the following system of nonlinear, coupled, partial differential equations results:

$$\text{div}(\epsilon \cdot \text{grad } \psi) = -q \cdot (p - n + C) \quad (14)$$

$$\begin{aligned} \text{div } q \cdot \mu_n \cdot n \cdot \left(\vec{E} - \frac{k \cdot T}{q} \cdot \text{grad}(\ln n_{ie}) \right. \\ \left. + \frac{k \cdot T}{q} \cdot \frac{1}{n} \cdot \text{grad } n + P_n^{eff} \cdot \text{grad } T \right) \\ = q \cdot \frac{\partial n}{\partial t} + q \cdot R \end{aligned} \quad (15)$$

$$\text{div } q \cdot \mu_p \cdot p \cdot \left(\vec{E} + \frac{k \cdot T}{q} \cdot \text{grad}(\ln n_{ie}) \right)$$

$$-\frac{k \cdot T}{q} \cdot \frac{1}{p} \cdot \text{grad } p - P_p^{eff} \cdot \text{grad } T) \\ = -q \cdot \frac{\partial p}{\partial t} - q \cdot R \quad (16)$$

$$C_h \cdot \frac{\partial T}{\partial t} + \text{div}(-\chi \cdot \text{grad } T) = G_h^J + G_h^R + G_h^T + G_h^S \quad (17)$$

$$G_h^J = \frac{J_n^2}{\sigma_n} + \frac{J_p^2}{\sigma_p} \quad (18)$$

$$G_h^R = q \cdot R \left(2 \cdot T \cdot \frac{kT}{q} \cdot \frac{1}{n_{ie}} \cdot \frac{\partial n_{ie}}{\partial T} \right) \quad (19)$$

$$G_h^T = \vec{J}_n \cdot T \cdot \text{grad } P_n - \vec{J}_p \cdot T \cdot \text{grad } P_p \quad (20)$$

$$G_h^S = T \cdot P_n^{eff} \cdot \text{div } \vec{J}_n - T \cdot P_p^{eff} \cdot \text{div } \vec{J}_p \quad (21)$$

$$\left(\frac{k}{q} \cdot \ln \frac{c}{n_{ie}} - \frac{kT}{q} \cdot \frac{1}{n_{ie}} \cdot \frac{\partial n_{ie}}{\partial T} \right) + P_c \equiv P_c^{eff} \quad (22)$$

Equation (14) is the well known Poisson equation. ϕ denotes the electrostatic potential, C the total net concentration of all ionized impurities. ϵ is the permittivity. Equations (15), (16) are continuity equations for electrons n and holes p including the so-called extended-drift extended-diffusion approximation of the current relations. That is, an effective electric field is introduced because of the possible dependence of the intrinsic concentration on position, and the diffusion not only accounts for concentration gradients but also for temperature gradients. μ denotes the mobility, k the Boltzmann constant. $\vec{E}$ is the electric field, P the thermoelectric power, c means 'carrier' and may take the value n or p for electrons and holes, respectively. Equation (17) is the heat flow equation. C_h denotes the heat capacity. The right-hand side in (17) represents the heat generation. Four contributions to the heat generation can be distinguished: Joule heat G_h^J (18), recombination heat G_h^R (19), Thomson heat G_h^T (20) and carrier source heat G_h^S (21). Equation (22) is a definition of the effective thermoelectric power P_c^{eff} . The expression in brackets arises due to the dependence of the quasi-Fermi potential on temperature.

The governing equations depend non-linearly on the lattice temperature. If lattice heating is significant, the thermal system becomes tightly coupled to the electrical system. Recombination, mobility, thermoelectric power and the effective intrinsic carrier density n_{ie} depend on temperature [10], while the temperature gradient acts as a driving force and the heat generation is a function of the electrical variables.

Auger recombination and carrier-carrier scattering, known as limiting physical effects for high injection conditions in power semiconductor devices [10], have been taken into account. As heavy doping effects limit thyristor operation, the effective intrinsic

carrier concentration is computed using [10], [11]. One obtains the relation:

$$\frac{\partial n_{ie}}{\partial T} = n_{ie} \cdot \left(\frac{E_g}{2 \cdot k \cdot T^2} + \frac{3}{2 \cdot T} \right) \\ - n_{ie} \cdot \left(\frac{q \cdot V_1 \cdot \left(\ln \left(\frac{N_D^+ + N_A^-}{N_0} \right) + \sqrt{\ln^2 \left(\frac{N_D^+ + N_A^-}{N_0} \right) + 0.5} \right)}{2 \cdot k \cdot T^2} \right) \\ + n_{ie} \cdot \left(\frac{9.025 \cdot 10^{-5} \frac{eV}{K} + 6.10 \cdot 10^{-7} \frac{eV}{K} \cdot \left(\frac{T}{K} \right)}{2 \cdot k \cdot T} \right) \\ + n_{ie} \cdot \left(\frac{3}{4} \cdot m_0 \cdot \left(\frac{1.4 \cdot 10^{-4} \frac{1}{K} \cdot m_n^* + 4.5 \cdot 10^{-4} \frac{1}{K} \cdot m_p^*}{m_n^* \cdot m_p^*} \right) \right) \quad (23)$$

Note also that the dependence of the bandgap energy E_g and the effective masses on temperature is accounted for in Eq.(23). Following [4], [8] the thermoelectric powers can be expressed as functions of contributions to the overall mobility [6].

For the electrical subsystem, either Dirichlet boundaries at ohmic contacts or Neumann boundaries are assumed. Mixed boundary conditions for the heat flow equation are mandatory in order to be able to model realistic imperfect cooling conditions. This is of special importance for transient electrothermal simulations, as the time constant for self-heating increases with increasing external thermal resistance.

3. Solution Methods

The simulation of the coupled transport of heat and charge carriers requires the self-consistent solution of Poisson's equation (14), the continuity equations for electrons n (15) and holes p (16) and the heat flow equation (17) in space and time. Spatial discretization is obtained using finite boxes [5], a generalization of finite differences, while time is discretized with the backward Euler method.

The electrothermal problem is computed self-consistently following a decoupled approach. At each time step the electrical subsystem of equations is solved first, the lattice temperature being regarded as an independent variable. Then the temperature distribution is updated by solving the heat flow equation. Newton's method and LU-decomposition are used to solve the electrical and thermal subsystems alternately until convergence is attained.

Usually, the characteristic time for the electrical and the thermal subsystem differ by several orders of magnitude. Thus a device is in steady state from the electrical point of view, whereas thermally it is still in transition.

4. Results

An IGT combines bipolar conduction with MOS gate control of the current. Due to bipolar conductivity modulation arising from carrier injection into the n^- -drift region an IGT can be operated at high forward current densities, even when supporting high blocking voltages. Due to its MOS gate the IGT can be driven with low power.

The concept of the IGT is to use a MOS gate created channel to link the n^+ -emitter region to the n^- -base [2]. In the on-state the lower junction towards the collector is forward-biased and the current flow in the IGT occurs via the channel. When latch-up occurs, however, the parasitic thyristor between the collector and emitter terminals in the four-layer IGT structure turns on, and the control of the collector current by the applied gate voltage is lost. In DC circuits latch-up usually produces catastrophic failure of the device as a result of excessive heat dissipation.

Static latch-up has been investigated in an IGT. It occurs when the forward conduction current density exceeds a critical value, while the collector voltage is low. Geometry and doping data of the IGT have been taken from [2]. The simulation area contains only one half of a symmetric IGT cell. Figure 1 shows a cross section of the most interesting part of the IGT with respect to latch-up analysis. The n^+ -emitter ($1 \cdot 10^{20} \text{ cm}^{-3}$) is embedded in a double doped p -base region ($1 \cdot 10^{18} \text{ cm}^{-3}$, $5 \cdot 10^{16} \text{ cm}^{-3}$). In order to support a blocking voltage of 300 V the n -drift layer ($1 \cdot 10^{15} \text{ cm}^{-3}$) has been chosen to be 65 μm long. The bottom of the simulation area is made up of a 10 μm p^+ -doped

substrate ($1 \cdot 10^{19} \text{ cm}^{-3}$) which cannot be seen in Fig. 1. A n -buffer layer is not included.

Figures 2 and 3 show the electron and hole concentration in the critical part of the IGT, containing the emitter and p -base region, under equilibrium conditions. Figures 1, 2 show how both, the p -base region together with the n^+ -emitter are incorporated in the lightly doped n -type drift layer, which is the central region of the IGT.

In order to find the critical value of the collector current I_c , the collector voltage V_{ce} has been ramped in a transient electrothermal simulation first. Then the electrothermal steady-state solution has been computed for $V_{ge}=15 \text{ V}$, $V_{ce}=1.5 \text{ V}$. The idea is to investigate one bias point (from the electrical point of view) but to modify the conditions for self-heating. Thus the current handling capability of the IGT limited by the onset of latch-up can be investigated as a function of lattice temperature determined by different thermal conditions.

Two different thermal boundary conditions have been chosen. First very good cooling conditions (heat sink thermal conductance $h=50 \text{ W/cm}^2\text{K}$), then realistic cooling conditions ($h=5 \text{ W/cm}^2\text{K}$) have been assumed. In the latter case a second simulation has been performed based on a heuristic heat generation model [1], [10]:

$$G_h = (J_n + J_p) \cdot \vec{E} + R \cdot E_g \quad (24)$$

Equation (24) accounts for two contributions to the overall heat generation, Joule heat with the electric field as a driving force and recombination heat considering the contribution of the bandgap only. Double sided cooling is assumed. The heat sink temperature T_o is

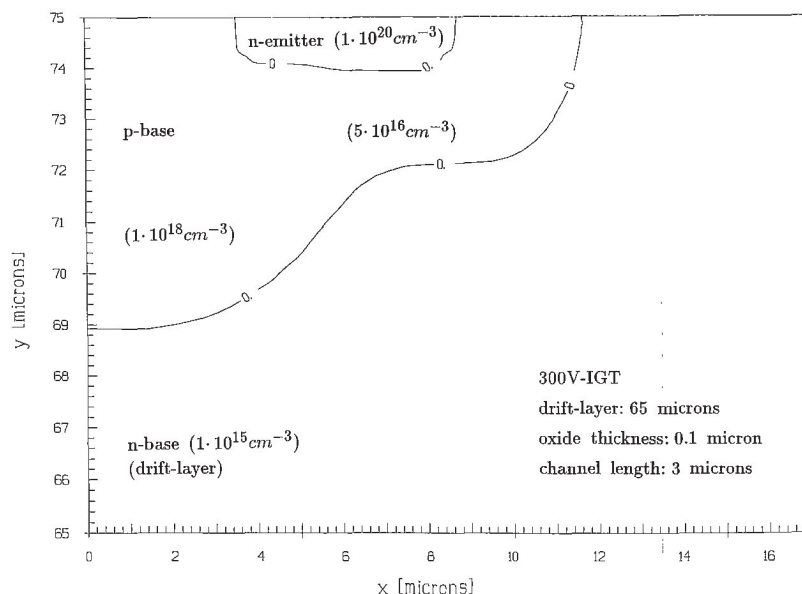


Fig. 1 cross section of IGT, (n^+ -emitter ($1 \cdot 10^{20} \text{ cm}^{-3}$), onset of n -base ($1 \cdot 10^{15} \text{ cm}^{-3}$) p -base ($1 \cdot 10^{18} \text{ cm}^{-3}$, $5 \cdot 10^{16} \text{ cm}^{-3}$)).

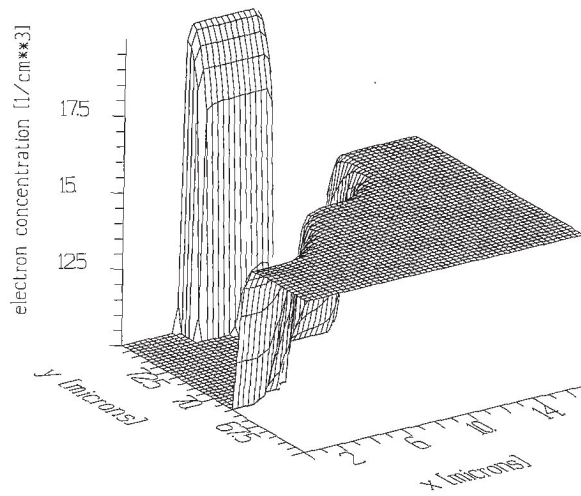


Fig. 2 electron concentration [cm⁻³] for equilibrium, $V_{ge}=0$ V, $V_{ce}=0$ V.

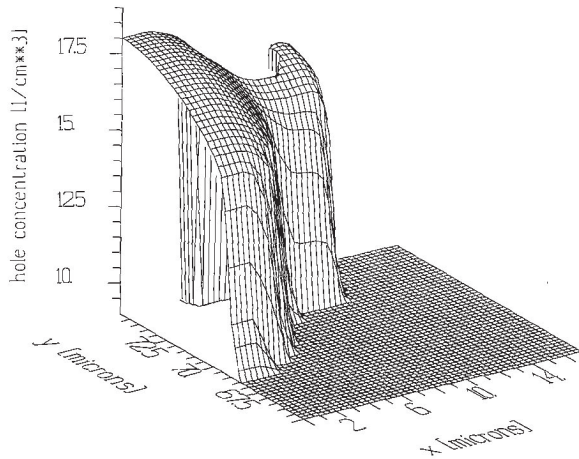


Fig. 3 hole concentration [cm⁻³] for equilibrium, $V_{ge}=0$ V, $V_{ce}=0$ V.

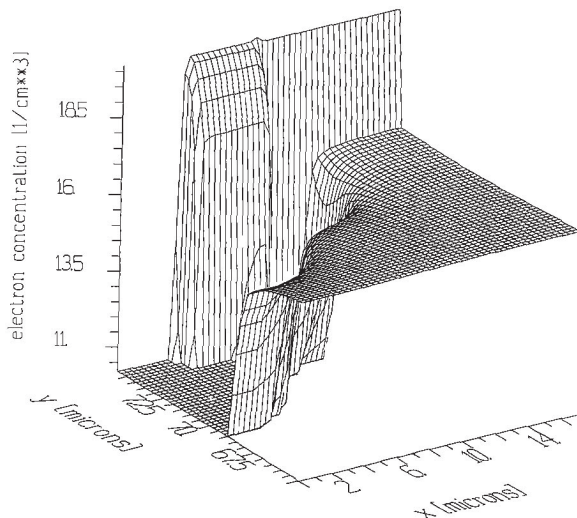


Fig. 4 electron concentration [cm⁻³], SOA, $V_{ge}=15$ V, $V_{ce}=1.5$ V, $T_o=300$ K, $h=50$ W/cm²K.

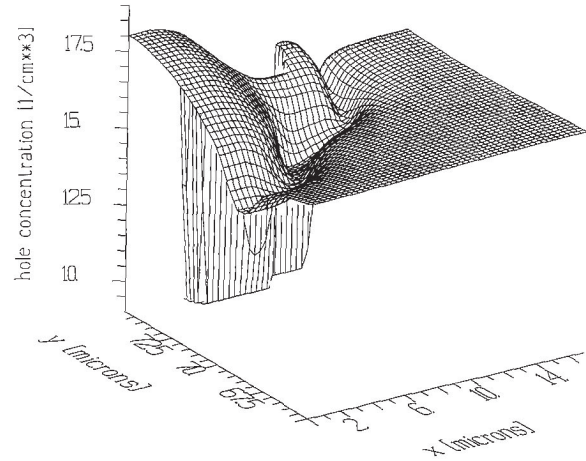


Fig. 5 hole concentration [cm⁻³], SOA, $V_{ge}=15$ V, $V_{ce}=1.5$ V, $T_o=300$ K, $h=50$ W/cm²K.

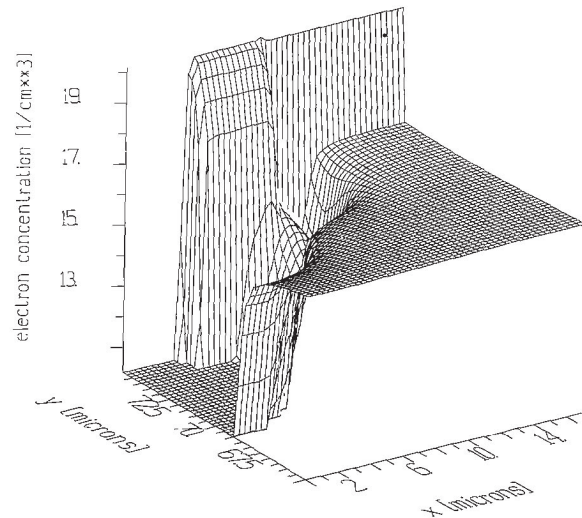


Fig. 6 electron concentration [cm⁻³], Latch-Up, $V_{ge}=15$ V, $V_{ce}=1.5$ V, $T_o=300$ K, $h=5$ W/cm²K.

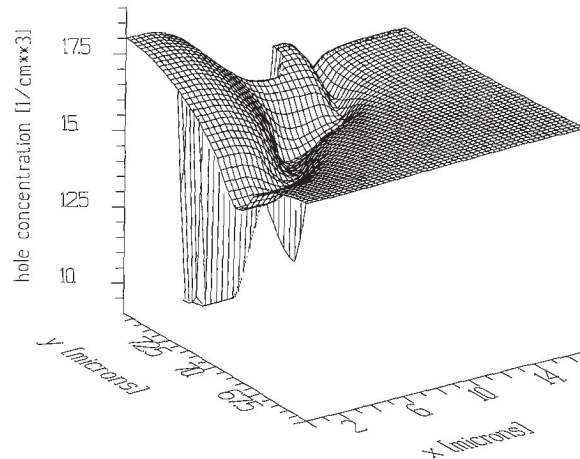


Fig. 7 hole concentration [cm⁻³], Latch-Up, $V_{ge}=15$ V, $V_{ce}=1.5$ V, $T_o=300$ K, $h=5$ W/cm²K.

300 K in all simulations.

When the heat sink thermal conductance is $50 \text{ W/cm}^2\text{K}$ the IGT is still in the save operating area (SOA). The peak lattice temperature is 305.2 K in this case. Figures 4, 5 show the carrier concentration in the n^+ -emitter, the channel region and the p -base. Latch-up, however, is very pronounced for a heat sink thermal conductance $5 \text{ W/cm}^2\text{K}$. The corresponding peak lattice temperature is 346.1 K. Figures 6, 7 present the electron and hole concentration for the onset of latch-up. Note that the difference between Figs. 4, 5 and 6,

7 is due to different cooling conditions only. In both cases $V_g=15 \text{ V}$, $V_c=1.5 \text{ V}$ have been applied. Thus it is demonstrated that latch-up in the IGT has to be regarded as an electrothermal problem.

The increase of lattice temperature, however, is not only determined by thermal boundary conditions but also by the local heat production. Using the heuristic heat generation model (24), (incorporated in many device simulators), the peak lattice temperature is predicted to be 329.5 K ($h=5 \text{ W/cm}^2\text{K}$ unchanged). Latch-up is much less pronounced. This fact indicates

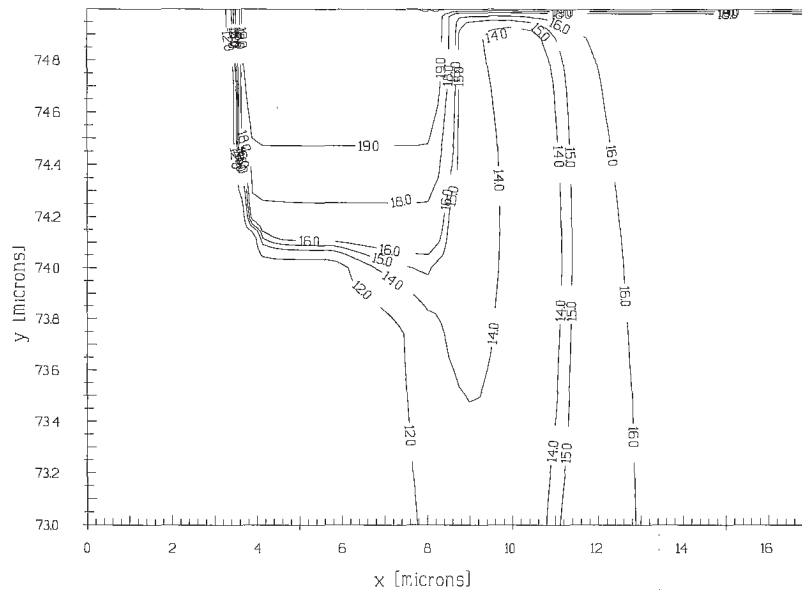


Fig. 8 contour lines of electron concentration [cm^{-3}] for Latch-Up, $V_{ge}=15 \text{ V}$, $V_{ce}=1.5 \text{ V}$, $T_o=300 \text{ K}$, $h=5 \text{ W/cm}^2\text{K}$.

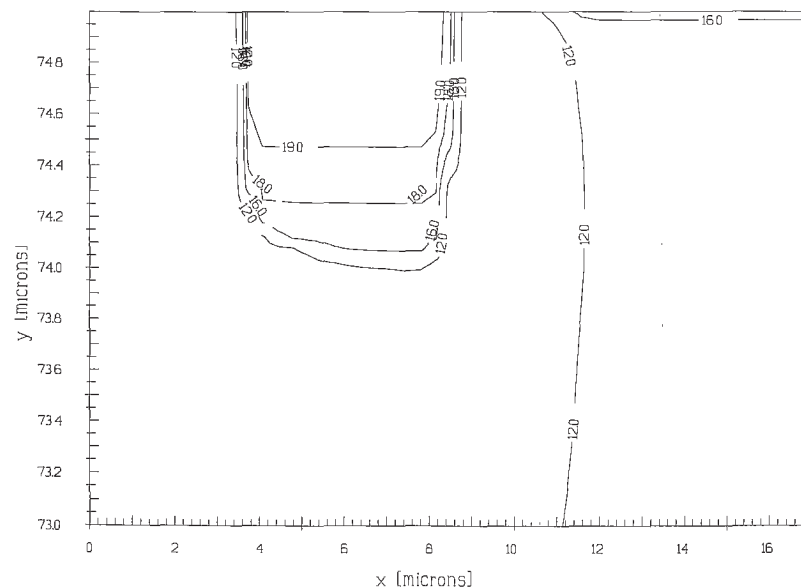


Fig. 9 contour lines of electron concentration [cm^{-3}] for equilibrium, $V_{ge}=0 \text{ V}$, $V_{ce}=0 \text{ V}$.

that the capability to accurately predict the safe operating area depends on the availability of an advanced model for local energy conversion.

When latch-up occurs the emitter injects electrons into the p -base as is made visible in Fig. 6. The emitter region spreads into the p -base, as is seen from Fig. 8 by comparison with the equilibrium distribution in Fig. 9, initiating the turn on of the parasitic thyristor in the IGT-structure.

In order to compare the different levels of injected electrons the IGT has been cut at the emitter edge for Fig. 10. The electron concentration in the p -base rises

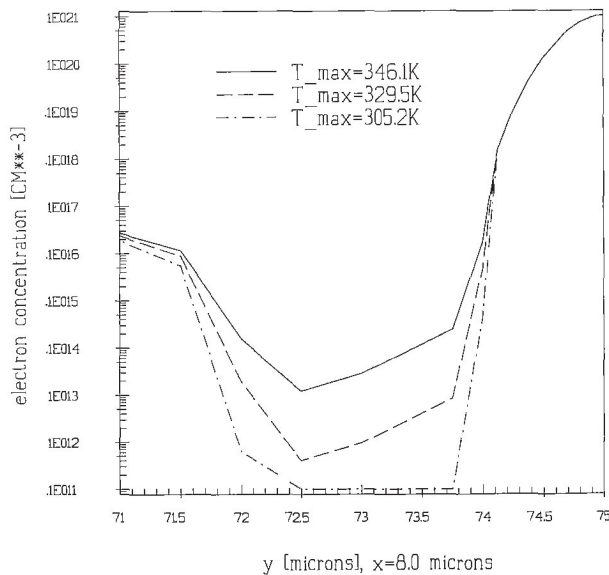


Fig. 10 comparison of electron concentration [cm^{-3}] at $x=8.0 \mu\text{m}$, $V_{ge}=15 \text{ V}$, $V_{ce}=1.5 \text{ V}$, $h=50 \text{ W/cm}^2\text{K}$, $h=5 \text{ W/cm}^2\text{K}$.

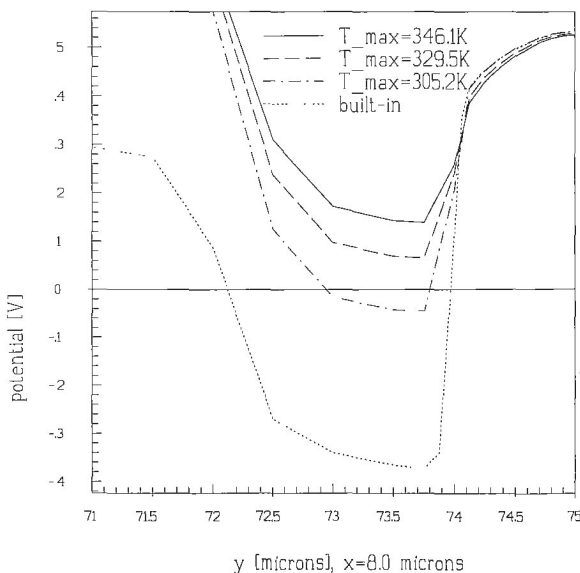


Fig. 11 comparison of potential [cm^{-3}] at $x=8.0 \mu\text{m}$, $V_{ge}=15 \text{ V}$, $V_{ce}=1.5 \text{ V}$, $h=50 \text{ W/cm}^2\text{K}$, $h=5 \text{ W/cm}^2\text{K}$.

with the increase of lattice temperature.

In isothermal silicon at 300 K, the critical value for the onset of latch-up is exceeded when the n^+ -emitter- p -base junction becomes forward-biased by more than 0.7 volt, usually because of lateral current flow in the p -base. Under non-isothermal conditions, however, the junction voltage is reduced which can be seen in Fig. 11. Therefore more electrons are injected. Furthermore the voltage drop in the p -base due to hole current flow is higher in the non-isothermal case because of the increase of the sheet resistance due to the excess lattice temperature. This effect is made visible in Fig. 12.

Figure 13 shows the excess temperature in the channel region after onset of latch-up. The maximum

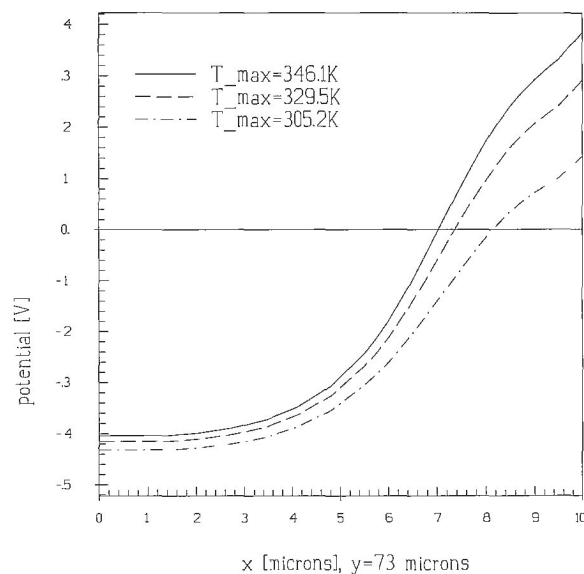


Fig. 12 comparison of potential [cm^{-3}] at $y=73 \mu\text{m}$, $V_{ge}=15 \text{ V}$, $V_{ce}=1.5 \text{ V}$, $h=50 \text{ W/cm}^2\text{K}$, $h=5 \text{ W/cm}^2\text{K}$.

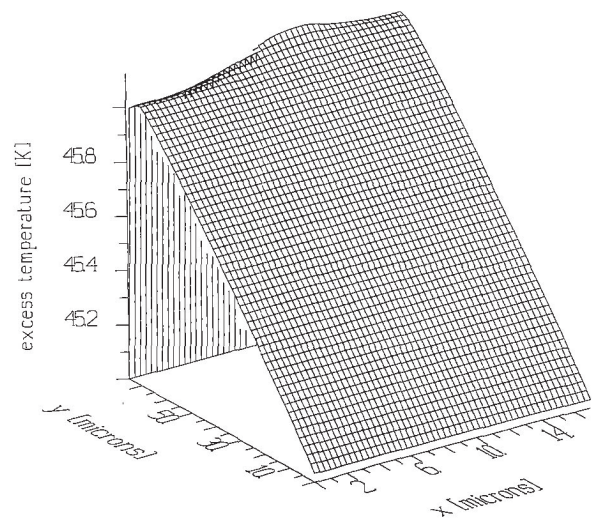


Fig. 13 excess temperature [K], Latch-Up, $V_{ge}=15 \text{ V}$, $V_{ce}=1.5 \text{ V}$, $T_o=300 \text{ K}$, $h=5 \text{ W/cm}^2\text{K}$.

temperature is found to be 346.1 K for the conditions cited above. The temperature distribution is almost homogeneous. Most of the temperature drop is external to the device. The temperature peak is located in the inversion layer due to excessive Joule heating.

It is found that the latching current is reduced with increasing temperature. The reason is that the gain of the *pnp*-transistor as well as the sheet resistance of the *p*-base increases with temperature. Furthermore the reduction of the n^+ -emitter-*p*-base junction voltage due to self-heating enhances latch-up. Thus the latching current reduction is a function of cooling conditions.

5. Conclusion

Emphasizing the entropy balance equation an advanced model for self-heating effects has been derived from principles of irreversible thermodynamics. It is valid in both the stationary and the transient regimes.

Four contributions to the heat generation can be distinguished: Joule heat, recombination heat, Thomson heat and carrier source heat.

The electrothermal nature of device behavior during latch-up in an IGT has been simulated. It has been found that accurate analysis of latch-up phenomena requires electrothermal simulation to account for the reduction of latching current due to self-heating. Furthermore it has been shown that simulations based on a heuristic model of electrothermal transport tend to predict a larger safe operating area of the IGT than simulations based on the suggested rigorous model of electrothermal interaction.

Acknowledgement

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EXHIBIT 23

UNITED STATES INTERNATIONAL TRADE COMMISSION
Washington, D.C.

Before the Honorable Monica Bhattacharyya
Administrative Law Judge

In the Matter of

**CERTAIN POWER SEMICONDUCTORS, AND
MOBILE DEVICES AND COMPUTERS
CONTAINING SAME**

Inv. No. 337-TA-1308

JOINT DISCLOSURE OF DISPUTED CLAIM TERM CONSTRUCTIONS

Pursuant to Ground Rule 6.1 and the Procedural Schedule (Order No. 8), Complainant Arigna Technology Limited (“Complainant”), Respondents Apple Inc., TCL Electronics Holdings Limited, TCL Communication Limited, TTE Technology, Inc. and TCT Mobile (US) Inc. (“Respondents”), and the Commission Investigative Staff (“Staff”) (collectively, “the Parties”) respectfully submit the claim chart attached as Exhibit A identifying agreed and disputed claim constructions for terms in the asserted claims of United States Patent No. 7,183,835 identified by one or more of the Parties for construction. The Parties have met and conferred in an attempt to limit their dispute. At this time, the Parties do not agree upon constructions for any term, however, the Parties are continuing to meet and confer in an effort to narrow or simplify the disputes.

Dated: July 15, 2022

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EXHIBIT A

EXHIBIT A

Term	Identifying Party	Complainant's Proposed Construction	Respondents' Proposed Construction	Staff's Proposed Construction
claim preamble ¹ (claim 1)	Respondents and Staff	Non-limiting preamble	The preamble is limiting.	The preamble is limiting.
“insulated gate transistor” (claims 1 and 2)	Respondents	a transistor whose gate is electrically insulated from the channel	Plain meaning, <i>i.e.</i> IGBT (insulated gate bipolar transistor)	a transistor whose gate is electrically insulated from the channel
“controlling a drive of an insulated gate transistor” (claim 1)	Respondents	Non-limiting preamble Alternatively, plain and ordinary meaning, <i>e.g.</i> , controlling the signal applied to the gate of an insulated gate transistor	controlling the voltage supplied to the gate of an insulated gate transistor to switch the transistor between ON and OFF states	controlling the voltage supplied to the gate of an insulated gate transistor to switch the transistor between ON and OFF states
“indicates a conduction of said insulated gate transistor” (claim 1)	Respondents	Plain and ordinary meaning, <i>e.g.</i> , indicates that said insulated gate transistor is turned on	indicates that said insulated gate transistor is in the ON state	indicates that said insulated gate transistor is in the ON state
“significant” (claims 1 and 2)	Respondents and Staff	Plain and ordinary meaning, <i>e.g.</i> , active	Plain meaning, <i>i.e.</i> large or important enough to have a meaningful effect, <i>e.g.</i> a HIGH potential state	active-high or active-low state indicating a condition is met

¹ Pursuant to Ground Rules 6.1 and 6.2, the Parties identify the first eight (8) terms listed in the above chart that the Parties believe are amenable to resolution in the *Markman* hearing process and likely to be significant to resolving the Parties' dispute.

“clamped constantly” (claim 2)	Respondents and Staff	held at a constant voltage	clamped to a certain voltage for a determined period by a Miller effect	held at a constant voltage
“control output signal” (claim 1)	Staff	Plain and ordinary meaning, e.g., output signal that is controlling an insulated gate transistor	signal supplied to the gate of an insulated gate transistor to switch the transistor between ON and OFF states	signal supplied to the gate of an insulated gate transistor to switch the transistor between ON and OFF states
“short-circuit protection circuit” (claim 1)	Staff	Plain and ordinary meaning, e.g., circuit that performs function of short-circuit protection	circuit that performs short-circuit protection without a shunt resistor	circuit that performs short-circuit protection without a shunt resistor
“detecting voltage” (claim 1)	Staff	Plain and ordinary meaning	detected voltage of the control output signal	smaller, proportional representation (of said control output signal)
“pulse generation circuit” (claim 1)	Staff	Plain and ordinary meaning, e.g., circuit that generates one or more pulses	Plain meaning, <i>i.e.</i> circuit that generates a pulse	circuit used to generate rectangular pulse
“normally operates” (claim 2)	Staff	Plain and ordinary meaning, e.g., operates in a normal state	operates without a short-circuit	is ON in the absence of a short circuit condition

CERTIFICATE OF SERVICE

I hereby certify that a copy of the foregoing has been served on July 15, 2022, as indicated, on the following:

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Washington, D.C.**

**Before The Honorable Monica Bhattacharyya
Administrative Law Judge**

In the Matter of

**CERTAIN POWER
SEMICONDUCTORS, AND MOBILE
DEVICES AND COMPUTERS
CONTAINING SAME**

Inv. No. 337-TA-1308

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