

Gregory F. Taylor

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Experience

- 2016- **Greg Taylor Consulting, Inc.**, Portland OR
Principal. Technical consulting on electronic product and integrated circuit development with a variety of clients.
- 2016-2020 **zGlue Corporation**, Hillsboro OR
zGlue Fellow. Consulted on new product planning; integrated circuit design, specification, validation, testing, and manufacturing; represented zGlue at opencompute.org's Open Domain Specific Architecture (ODSA) working group.
- 2014-2016 **Intel Corporation**, Platform Engineering Group, Hillsboro OR
Intel Fellow, Hard IP Group Chief Architect. Leading the worldwide circuit architecture teams for I/O, analog, and linear supply regulator design.
- 2008-2015 **Intel Fellow, Analog Review Committee lead.** Led an internal team driving the development of 22, 14, and 10 nm analog/mixed signal circuits across all product lines using Intel process technologies. Drove consistency and sharing of these IPs across most of the business units at Intel.
- 2013 **Intel Corporation**, Intel Labs, Hillsboro OR
Intel Fellow, Director of the Low Power Mixed Signal Lab. Started a new lab to develop analog/mixed signal circuits and design methods that will enable lower power computing and communication platforms.
- 2011-2013 **Intel Fellow, Director of the SoC Design Lab.** Led a multinational team to develop prototype Systems on Chip, including work to improve time to market and energy efficiency through improvements to chip design.
- 2008-2011 **Intel Fellow, Director of the Circuit Research Lab.** Led a team developing circuits and microarchitectures that will lead to lower power and higher performance computing platforms.
- 2004-2008 **Intel Corporation**, Logic Technology Development, Hillsboro OR
Intel Fellow, Director of Mixed Signal Circuit Technology. Led a cross organizational team coordinating the 45 nm and 32 nm collateral delivery between process technology development and multiple design projects. Technical lead for the team that developed I/O, clock generation, temperature sensing, and other analog circuits for use across all Intel microprocessors developed on 65 nm, 45 nm, and 32 nm manufacturing technologies, including the first commercial high-k metal gate based product. Started analog circuit development for what became the first commercial FinFET manufacturing process.
- 2002-2004 **Intel Fellow, Director of Mixed Signal Circuit Technology.** Managed the team responsible for the design of clock generation, clock distribution, I/O circuitry, package, power distribution and other mixed signal circuits for a pair of 90 and 65 nm Pentium® 4 processors, including the first commercial strained silicon based product.
- 1993-2002 **Principal Engineer/Component Design Manager.** Managed the team responsible for the design of clock generation, clock distribution, I/O circuitry, package, power distribution and other mixed signal circuits for Pentium, Pentium II, and Pentium III microprocessors in 0.35 through 0.13 μm technologies.
- 1991-1993 **Staff Design Engineer.** Designed a CMOS/ECL cache for the Pentium Microprocessor, Intel's first BiCMOS product, in 0.8 μm and 0.6 μm

technologies. Developed an Electrical Rules Checker to ensure the correctness of signaling between different frequency clock domains.

Bipolar Integrated Technology, Beaverton OR

- 1988-1991 **Principal Design Engineer**. Participated in all phases of the design of a second generation floating point chip. Made customer visits to determine product requirements; developed the architecture, test and validation plans; and designed the multiplier circuit. Developed an ECL Electrical Rules Checker and formal verification tool and supervised the package design. Consulted in the design, validation, and debug of Sparc® and MIPS® ECL microprocessors.
- 1986-1988 **Circuit Design Engineer**. Designed Emitter Coupled Logic floating point integrated circuits. Generated test suite and validated correctness of overall design. Developed a switch level simulator to verify the logical correctness of ECL gates. Completed debug and sustaining engineering.

Education

- 1983-1985 D.Eng. Computer and Systems Engineering, Rensselaer Polytechnic Institute (RPI), Troy, NY. Thesis topic: An Architecture for a Wafer Scale Integration Two Dimensional Fast Fourier Transform Processor.
- 1981-1983 MSEE Computer and Systems Engineering, RPI, Troy NY. Thesis topic: An ECL Floating Point Processor.
- 1977-1981 BSEE Computer and Systems Engineering, RPI, Troy, NY.

Other

- IEEE Fellow, 2009 to present.
- Fannie and John Hertz Foundation Fellowship, recipient, 1981 to 1985.
- VLSI Circuit Symposium Technical Committee, member, 1999 to 2006.
- Published more than 60 peer reviewed papers, 67 issued US patents.

Publications

- "A 1–2 GHz Computational-Locking ADPLL With Sub-20-Cycle Locktime Across PVT Variation", Fahim ur Rahman, Greg Taylor, Visvesh Sathe, IEEE Journal of Solid-State Circuits, September 2019.
- "Designing Software Configurable Chips and SIPs using Chiplets and zGlue", Jawad Nasrullah, Zhiquan Luo, Greg Taylor, International Symposium on Microelectronics, September 2019.
- "High Capacity on-Package Physical Link Considerations", Greg Taylor, Ramin Farjadrad, Bapiraju Vinnakota, Hot Interconnects Conference, August 2019.
- "Smart Silicon Substrate for Quick Time to Market Chip-Stacks and Systems-in-Package", Omar Alnaggar, Rakesh Kumar, Jawad Nasrullah, Greg Taylor, IEEE System on Chip Conference, September 2018.
- "Computational Locking: Accelerating Lock-Times in All-Digital PLLs", Fahim ur Rahman, Greg Taylor, Visvesh Sathe, VLSI Circuits Symposium, June 2017.
- "Product Scaling in the System on Chip Era", Greg Taylor, International Electron Devices Meeting, December 2013.
- "How to Reduce Power in 3D IC Designs- A Case Study with OpenSPARC T2 Core", Moongon Jung, Taigon Song, Yang Wan, Young-Joon Lee, Debabrata Mohapatra, Hong Wang, Greg Taylor, Devang Jariwala, Vijay Pitchumani, Patrick Morrow, Clair Webb, Paul Fischer, and Sung Kyu Lim, IEEE Custom Integrated Circuits Conference, September 2013.
- "A Novel Digital Loop Filter Architecture for Bang-Bang ADPLL", Moataz Abdelfattah, Maged Ghoneima, Yehea I Ismail, Amr Lotfy, Mohamed Abdel-moneum, Nasser A. Kurd, Greg Taylor, International System on Chip Conference, September 2012.
- "Modeling the Response of Bang-Bang Digital PLLs to Phase Error Perturbations", Moataz Abdelfattah, Maged Ghoneima, Yehea I Ismail, Amr Lotfy, Mohamed Abdelsalem, Mohamed Abdel-moneum, Nasser A. Kurd, Greg Taylor, IEEE Custom Integrated Circuits Conference, September 2012.
- "The Next Decade of Computing", Greg Taylor, Theory and Applications of Computational Chemistry, September 2012.
- "Digital Randomness", Greg Taylor and George Cox, IEEE Spectrum, September 2011.
- "Analog Mixed Signal Design: The Technology Scaling Rate Limiter", Greg Taylor, Frontiers in Analog CAD, July 2011.
- "SiP, SOC, and TSV: Issues in Getting from Technologies to Systems", Greg Taylor, GIT 3D System Workshop, June 2011.
- "HVM Performance Validation and DFM Techniques used in a 32nm CMOS Thermal Sensor System", D. Duarte, P. Zepeda, S. Hsu, A. Maheshwari and G. Taylor, IEEE Sensors, November 2010.
- "A Wide Dynamic Range Self-Biased Fully Differential Operational Amplifier for Micro Mechanical Sensors and Actuators Circuitry", Mohamed Abdel-moneum, David Duarte, Greg Taylor, IEEE Sensors, November 2010.
- "HVM Performance Validation and DFM Techniques used in a 32nm CMOS Thermal Sensor System", D. Duarte, P. Zepeda, S. Hsu, A. Maheshwari and G. Taylor, IEEE Custom Integrated Circuits Conference, September 2010.
- "2.4GHz 7mW All-Digital PVT-Variation Tolerant True Random Number Generator in 45nm CMOS", S. Srinivasan, S. Mathew, R. Ramanarayanan, F. Sheikh, M. Anders, H. Kaul, V. Erraguntla, R. Krishnamurthy, G. Taylor, VLSI Circuit Symposium, June 2010.
- "A 1.05 V 1.6 mW, 0.45 °C 3 σ Resolution SD Based Temperature Sensor With Parasitic Resistance Compensation in 32 nm Digital CMOS Process", Hasnain Lakdawala, Y. William

Li, Arijit Raychowdhury, Greg Taylor, and Krishnamurthy Soumyanath, IEEE Journal of Solid State Circuits, December 2009, pp. 3621-3630.

"A 1.05 V 1.6 mW, 0.45 °C 3 σ Resolution SD Based Temperature Sensor With Parasitic Resistance Compensation in 32 nm Digital CMOS Process", Hasnain Lakdawala, Y. William Li, Arijit Raychowdhury, Greg Taylor, and Krishnamurthy Soumyanath, International Solid State Circuits Conference, February 2009.

"Managing Process Variation in Intel's 45nm CMOS Technology", Kelin Kuhn, Chris Kenyon, Avner Kornfeld, Mark Liu, Atul Maheshwari, Wei-Kai Shih, Sam Sivakumar, Greg Taylor, Peter VanDerVoorn, Keith Zawadski, Intel Technology Journal, June 2008, pp. 93-110.

"A Band-Limited Active Damping Circuit With 13 dB Power Supply Resonance Reduction", Jianping Xu, Zuoguo Wu, Peter Hazucha, Paolo Aseron, Mingwei Huang, Fabrice Paillet, Gerhard Schrom, James Tschanz, Vivek De, Tanay Karnik, Greg Taylor, IEEE Journal of Solid State Circuits, January 2008, pp. 61-68.

"On-Die Supply-Resonance Suppression Using Band-Limited Active Damping", Jianping Xu, Peter Hazucha, Mingwei Huang, Paolo Aseron, Fabrice Paillet, Gerhard Schrom, James Tschanz, Cangsan Zhao, Vivek De, Tanay Karnik, Greg Taylor, International Solid State Circuits Conference, February 2007.

"Designing for Low Power", Tawfik Rahal-Arabi, Ali Muhtaroglu, and Greg Taylor, Electrical Performance of Electronic Packaging, October 2006.

"The Impact of Leakage to the Power Supply Impedance of a Microprocessor", Ananda Sarangi, Greg Taylor, Signal Propagation on Interconnects, May 2006, pp. 43-46.

"Enhancing Microprocessor Immunity to Power Supply Noise with Clock/Data Compensation", Keng L Wong, Tawfik Rahal-Arabi, Matthew Ma, Greg Taylor, IEEE Journal of Solid State Circuit Design, April 2006, pp. 749-758.

"Reducing the Impact of Power Supply Noise on Microprocessor Performance", T. Rahal-Arabi, K.L. Wong, M. Ma, J. Barkatullah, G. Taylor, Electrical Performance of Electronic Packaging, October 2005, pp. 307-310.

"Design and Validation of a Power Supply Noise Reduction Technique", Gang Ji, Tawfik R Arabi, Greg Taylor, IEEE Transactions on Advanced Packaging, August 2005, pp. 445-448.

"Enhancing Microprocessor Immunity to Power Supply Noise with Clock/Data Compensation", Tawfik Rahal-Arabi, Greg Taylor, Javed Barkatullah, Keng L Wong, Matthew Ma, 2005 Symposium on VLSI Circuits, June 2005, pp. 16-19.

"Impact of On-Die Decoupling on the Core and IO Supplies of High Performance Microprocessors", Tawfik Rahal-Arabi, Gang Ji, Greg Taylor, Signal Propagation on Interconnects, May 2005, pp. 31-34.

"I/O Self-Leakage Test", Ali Muhtaroglu, Benoit Provost, Tawfik Rahal-Arabi, Greg Taylor, International Test Conference, October 2004, pp. 903-906.

"Computational Electromagnetics for High-Frequency IC Design", Dan Liao, Changhong Dai, Shih-Wuu Lee, Tawfik Rahal-Arabi, Greg Taylor, Antennas and Propagation Society Symposium, Jun 2004, pp. 3317-3320.

"Development and Validation of an Electromagnetic Distributed Power Grid Model for High Frequency Microprocessors", Tawfik Rahal-Arabi, Gang Ji, Matthew Ma, Ali Muhtaroglu, Greg Taylor, 2004 Symposium on VLSI Circuits, June 2004, pp. 110-113.

"Dampening High Frequency Noise in High Performance Microprocessor Packaging", Tawfik Rahal-Arabi, Gang Ji, Greg Taylor, Signal Propagation on Interconnects, May 2005, pp. 53-56.

"On-Die Droop Detector for Analog Sensing of Power Supply Noise", Ali Muhtaroglu, Greg Taylor, Tawfik Rahal-Arabi, IEEE Journal of Solid State Circuit Design, April 2004, pp. 651-660.

"Maintaining Microprocessor Compatibility across Process Generations", Ananda Sarangi, Sean R. Babcock, Jeff R. Jones, Gregory F. Taylor, Electrical Performance of Electronic Packaging, October 2003.

"Design and Validation of a Power Supply Noise Reduction Technique", Gang Ji, Tawfik Arabi, Greg Taylor, Electrical Performance of Electronic Packaging, October 2003, pp. 137-140.

"On-Die Droop Detector for Analog Sensing of Power Supply Noise", Ali Muhtaroglu, Greg Taylor, Tawfik Rahal-Arabi, Kent Callahan, 2003 Symposium on VLSI Circuits, June 2003, pp. 193-196.

"A Design Methodology for The I/O Power Supply of Next Generation Packaging", Gang Ji, Tawfik Arabi, Greg Taylor, Mark Beiley, Electrical Performance of Electronic Packaging, October 2002, pp. 253-256.

"Design and Validation of the Core and IOs Decoupling of the Pentium® III and Pentium® 4 Processors", Tawfik Rahal-Arabi, Greg Taylor, Matthew Ma, Jeff Jones and Clair Webb, Electrical Performance of Electronic Packaging, October 2002, pp. 249-252.

"Power Level Management in an IA32 Microprocessor", Ananda Sarangi, Gregory F. Taylor, Rachael J. Parker, Edward P. Osburn, Patrick J. Ott, Electrical Performance of Electronic Packaging, October 2002, pp. 235-238.

"Design & Validation of the Pentium® III and Pentium® 4 Processors Power Delivery", Tawfik Rahal-Arabi, Greg Taylor, Matthew Ma, and Clair Webb, 2002 Symposium on VLSI Circuits, June 2002, pp. 220-223.

"An Approach to Measuring the Power Supply Impedance of Microprocessors", Greg Taylor, Craig Deutschle, Tawfik Arabi, Brian Owens, Electrical Performance of Electronic Packaging, October 2001, pp. 211-214.

"Design and Performance Evaluation of Pentium® III Microprocessor Packaging", Ananda Sarangi, Gang Ji, Tawfik Arabi, Gregory F. Taylor, Electrical Performance of Electronic Packaging, October 2001, pp. 291-294.

"A JTAG Based AC Leakage Self Test", Tawfik Rahal-Arabi, Greg Taylor, 2001 Symposium on VLSI Circuits, June 2001, pp. 205-206.

"On-die Clock Jitter Detector for High Speed Microprocessors", Ravi Kuppaswamy, Kent Callahan, Keng Wong, Dan Ratches, Greg Taylor, 2001 Symposium on VLSI Circuits, June 2001, pp. 187-190.

"High Performance Package Designs for a 1 GHz Microprocessor", Altaf Hasan, Ananda Sarangi, Christopher S Baldwin, Robert L Sankman, Gregory F Taylor, Electronic Components and Technology Conference, August 2000, pp. 1178-1184.

"Reliability and Performance Tradeoffs in the Design of On-Chip Power Delivery and Interconnects", Greg Taylor, Tawfik Arabi, Hans Greub, Richard Muyschondt, Alicia Manthe, and Payman Aminzadeh, Electrical Performance of Electronic Packaging, October 1999, pp. 49-52.

"Modeling, Simulation, and Design Methodology of the Interconnect and Packaging of an Ultra-High Speed Source Synchronous Bus", Tawfik Arabi, Jeff Jones, Greg Taylor, and Dave Riendeau, Electrical Performance of Electronic Packaging, October 1998, pp. 8-11.

"A 2MB, 3.6GB/s Back-side Bus Cache for an IA32 450 MHz Microprocessor", Greg Taylor, Tawfik Arabi, Ken Hose, Jeff Jones, Songmin Kim, Ravi Kuppaswamy, Randy Mooney, Jack Price, Ananda Sarangi, 2001 Symposium on VLSI Circuits, June 1998, pp. 184-185.

"Power-On Contention Elimination", Greg Taylor, Keng Wong, 1996 Symposium on VLSI Circuits, June 1996, pp. 22-23.

"Microprocessor Clock Distribution", Greg Taylor, George Geannopoulos, Electrical Performance of Electronic Packaging, October 1996, pp. 29.

"High Fan-in Circuit Design", Lawrence T. Clark and Gregory F. Taylor, IEEE Journal of Solid State Circuit Design, January 1996, pp. 91-96.

"High Fan-in Circuit Design", Lawrence T. Clark and Gregory F. Taylor, Bipolar Circuits and Technology Meeting, October 1994, pp. 27-32.

"Building the world's fastest floating point processor", G. Sanguinetti, G. Taylor, and D. Clinkenbeard, ASIC Technology & News, January 1991, pp. 12-13.

"An Approach to 150K Gate Low Power ECL Cell Based Integrated Circuits", G. Taylor, G. Sanguinetti, and R. Lane, International Conference on Computer Design, September 1990, pp. 263-268.

"A 100 MHz Floating Point/Integer Processor", Greg Taylor, Hot Chips, August 1990.

"A 100 MHz Floating Point/Integer Processor", Greg Taylor, Alex Rekow, Jory Radke, Greg Thompson, Custom Integrated Circuits Conference, May 1990, pp. 24.5.1-4.

"An Architecture for a Video Rate Two-Dimensional Fast Fourier Transform Processor", G. F. Taylor, R. H. Steinvorth, and J. F. McDonald, IEEE Transactions on Computers, September 1988.

"A Sub 10 ns Bipolar 64 Bit Integer/Floating Point Processor Implemented on Two Circuits", Bob Elkind, Jay Lessert, Jim Peterson, and Greg Taylor, Bipolar Circuits and Technology Meeting, September 1987, pp. 101-104.

"ECL gains ground in battle against CMOS", Bob Leibowitz and Greg Taylor, Computer Design, April 1987, pp. 91-95.

"Wafer Scale Integration Using Discretionary Microtransmission Line Interconnections", B. J. Donlan, G. F. Taylor, R. H. Steinvorth, A. S. Bergendahl, J. F. McDonald, chapter 2.3 of Wafer Scale Integration, edited by Chris Jesshope and Will Moore, Adam Hilger, Boston, © 1996, pp. 31-45.

"Thick Film Stripline Micro Transmission Line Interconnections for Wafer Scale Integration", A. S. Bergendahl, J. F. McDonald, R. H. Steinvorth, G. F. Taylor, VLSI Science and Technology/1985, pp. 175-184.

"Wafer Scale Integration of a Video Rate Fuzzy Golay Processor", R. H. Steinvorth, G. F. Taylor, J. F. McDonald, A. S. Bergendahl, International Conference on Computer Design, October 1985, pp. 672-677.

"Fabrication and Performance Considerations for Gallium Arsenide Wafer Scale Integration", J. F. McDonald, R. H. Steinvorth, A. S. Bergendahl, G. F. Taylor, International Conference on Computer Design, October 1985, pp. 400-405.

"An Architecture for a Video Rate Fuzzy Golay Processor", R. H. Steinvorth, G. F. Taylor, J. F. McDonald, T. Hunter, International Conference on Parallel Processing, 1985.

"A Thick Film Lift-Off Technique for High Frequency Interconnection in Wafer Scale Integration", A. S. Bergendahl, B. J. Donlan, J. F. McDonald, R. H. Steinvorth, G. F. Taylor, VLSI Multilevel Interconnect Conference, 1985.

"Thick Film Stripline Micro Transmission Line Interconnections for Wafer Scale Integration", A. S. Bergendahl, J. F. McDonald, R. H. Steinvorth, G. F. Taylor, Electrochemical Society Spring Meeting, May 1985, pp. 311-312.

"The Wafer Transmission Module - Wafer Scale Integration Packaging", G. F. Taylor, Lt. B. J. Donlan, J. F. McDonald, A. S. Bergendahl, R. H. Steinvorth, Custom Integrated Circuits Conference, May 1985, pp. 55-58.

"Computer-Aided Design and Fabrication for Wafer Scale Integration", Lt. B. J. Donlan, J. F. McDonald, G. F. Taylor, R. H. Steinvorth, A. S. Bergendahl, VLSI Design magazine, April 1985.

"An Architecture for a Wafer Scale Integration Video Rate Two Dimensional Fast Fourier Transform Processor", G. F. Taylor, R. H. Steinvorth, J. F. McDonald, International Conference on Computer Design, October 1984, pp. 623-628.