

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Apple Inc.,
Petitioner,

v.

Arigna Technology Limited,
Patent Owner.

Case IPR2023-00453
Patent 7,183,835

**DECLARATION OF DR. GREGORY F. TAYLOR IN SUPPORT OF
PATENT OWNER'S PRELIMINARY RESPONSE TO PETITION FOR
INTER PARTES REVIEW OF U.S. PATENT NO. 7,183,835**

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IX. MISCELLANEOUS 35

I. INTRODUCTION

1. My name is Gregory F. Taylor. I am over eighteen years of age, of sound mind, and qualified to make the statements set forth in this Declaration. With the exception of the legal principles counsel has supplied to me, all the facts and statements contained herein are within my personal knowledge and are in all respects true and correct.

2. I have been asked by Arigna Technology Limited (“Arigna”) to submit this declaration in response to a petition filed by Apple Inc. (the “Petition”) and declaration submitted by Dr. David Kuan-Yu Liu (the “Liu Declaration”) regarding U.S. Patent No. 7,183,835 (“the ’835 Patent”).

II. PROFESSIONAL BACKGROUND AND QUALIFICATIONS

3. I have summarized in this section some of my educational background, career history, publications, and other relevant qualifications. My full *curriculum vitae* is attached as Exhibit 2013 to this expert report. During the past 5 years I submitted declarations in IPR2022-00481, IPR2022-00285, and *ex parte* reexamination no. 90/019,063, but otherwise have not testified in any cases.

4. I earned a Doctor of Engineering (Ph.D.) degree in Computer and Systems Engineering from Rensselaer Polytechnic Institute in 1985. From 1986 to 1991 I worked as a Circuit Design Engineer and then Principal Design

Engineer for Bipolar Integrated Technology. I started as a new hire from the Ph.D. program at RPI and ended up as the chief architect, lead product designer, lead verification engineer, and developer of the world's only formal verification tool for bipolar circuits.

5. From 1991 until 2016 I worked for Intel Corporation, starting as a Senior Staff design engineer and quickly became a team leader delivering the package, I/O, and analog circuits for the first processors on each technology generation. In 2002 I was promoted to Intel Fellow (one of the company's highest technical positions) based on both results and risk management in getting five generations of microprocessors into high volume manufacturing on schedule, including the first use of C4 packaging at Intel. From 2002 to 2016 I worked as director of numerous groups within Intel (Mixed Signal Circuit Technology, Circuit Research Lab, SoC Design Lab, Low Power Mixed Signal Lab), where I led teams that delivered three separate firsts for both Intel and the world: the first microprocessors using strained silicon, the first products using high-k metal gate transistors, and the first Trigate (FinFET) product. During this time my role expanded to leading a new company-wide analog/mixed signal circuit review team and leading the worldwide circuit architecture teams for I/O, analog, and supply regulator design IP. I currently operate my own consulting firm (Greg Taylor Consulting, Inc.), where I provide technical consulting

services on electronic product and integrated circuit development for a variety of clients.

6. Additionally, I have been an IEEE fellow since 2009. I have published more than 60 peer reviewed papers, and I am the inventor of 67 U.S. patents on integrated circuit design and testing.

7. Most semiconductor process technologies include multiple types of transistors: low voltage transistors for digital logic, high voltage transistors for Input/Output (I/O) and analog use, and sometimes additional options necessitated by a given circuit design. To minimize risk and cost, the leading-edge logic processes that Intel developed and that I used for most of my career only included low voltage transistors. As a result, most of the processors I worked on included I/O circuits with power supply and signal voltage levels that were higher than a single transistor could survive, sometimes several times higher. And my team was responsible for delivering the analog, high voltage, voltage regulation, and I/O circuits.

8. While I was leading the Circuit Research Lab at Intel Corporation, engineers on my team developed a 100 MHz on-chip switching regulator technology that took a high voltage input supply (twice what any transistor on the chip could survive) and delivered a high efficiency, clean, low voltage output. We then worked with a product team that committed to this technology

working – they had no backup option if it didn’t. The product was successfully launched without any delays due to this technology.

III. MATERIALS REVIEWED

9. In forming my opinions in this proceeding, I have reviewed each of the references cited in this Declaration including the ’835 Patent, the Petition, the Liu Declaration, and the references that the Petition and Liu Declaration rely upon as invalidating prior art.

IV. LEGAL PRINCIPLES

10. I am not a lawyer. In forming my opinions as set forth in this Declaration, I have relied upon legal principles supplied to me by attorneys for Arigna. In forming my opinions, I have not relied upon Arigna’s attorneys for any purpose other than the following legal principles.

A. Claim Construction

11. I understand that determining whether a patent claim is valid requires a two-step analysis. First, the claim must be construed. Second, the properly construed claim must be compared to the prior art.

12. With respect to the first step, I understand that claims are construed from the perspective of a person of ordinary skill in the art (“POSITA”) at the time of the purported invention. I understand that in the context of an *inter partes* review proceeding, absent a disclaimer or express definition, claim terms are given their plain and ordinary meaning to a POSITA

in view of the specification and file history and the knowledge of a POSITA.

Unless otherwise noted, I have applied what I consider to be the plain and ordinary meaning of all terms as understood by a POSITA at the time of the invention, which I understand to be on or around January 6, 2004.

B. Anticipation

13. I understand that a patent claim is presumed to be valid. I understand that to overcome that presumption, the challenger must show that the claim is invalid by a preponderance of the evidence. I understand the preponderance of the evidence to require the greater weight of evidence in favor of the challenger.

14. I understand that, although not expressly disclosed, subject matter may be inherently disclosed in a prior art reference where that subject matter is necessarily present in the subject matter disclosed and would be understood to be so by those of ordinary skill in the art. I understand that the fact that a certain result or characteristic may occur or be present in the prior art is not sufficient to establish the inherency of that result or characteristic.

15. I understand that a claim is invalid if each and every element of the claim is disclosed in a single prior art reference with the elements arranged as specified in the claim, either expressly or inherently. I understand that

invalidity based on the disclosure of a single prior art reference in this manner is called anticipation.

C. Person of Ordinary Skill in the Art

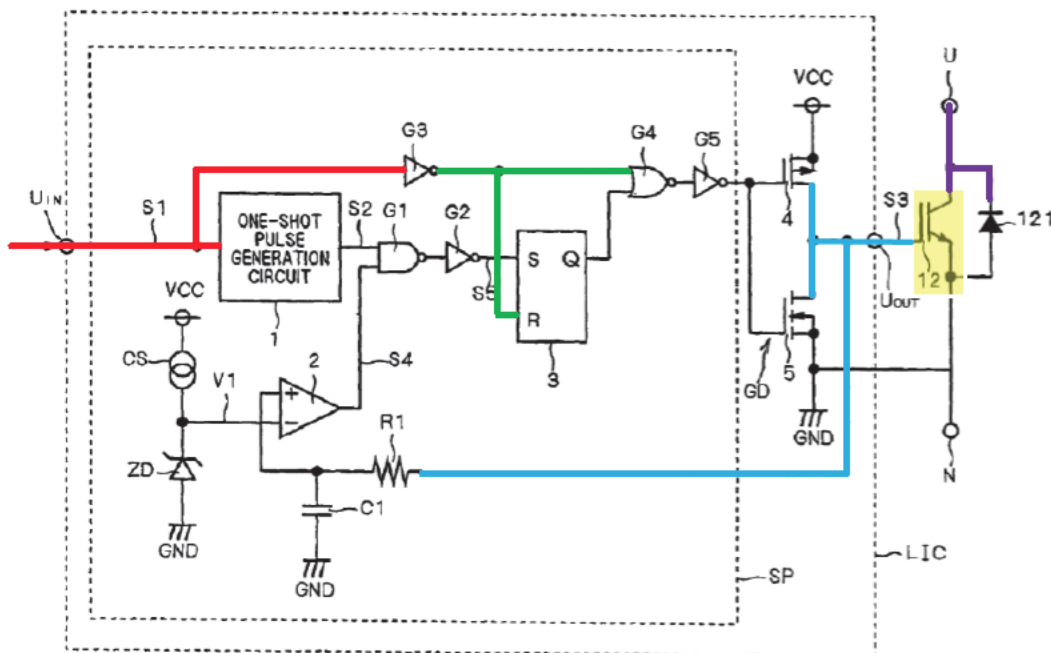
16. I understand that the meaning of claim terms and a patent's validity are to be determined from the vantage point of one of ordinary skill in the art at the time of the invention. In determining who would be one of such ordinary skill, I understand it is appropriate to consider criteria such as: (a) the type of problems encountered in the art; (b) prior art solutions to those problems; (c) the rapidity with which innovations are made; (d) the sophistication of the technology; and (e) the education level of active workers in the field.

V. THE '835 PATENT DISCLOSURE

17. In the '835 patent Sakata teaches a method to quickly detect that the output of an IGBT power transistor has been shorted and to shut the transistor off before it overheats and destroys itself. IGBTs are commonly used in high voltage switching applications and these high voltages can result in high power dissipation in switching transistors and more rapid onset of reliability risk. The method Sakata teaches utilizes the Miller capacitance to detect if the collector voltage of the IGBT is dropping (its normal behavior when the device is first turned on) or maintaining its voltage due to a short on the output.

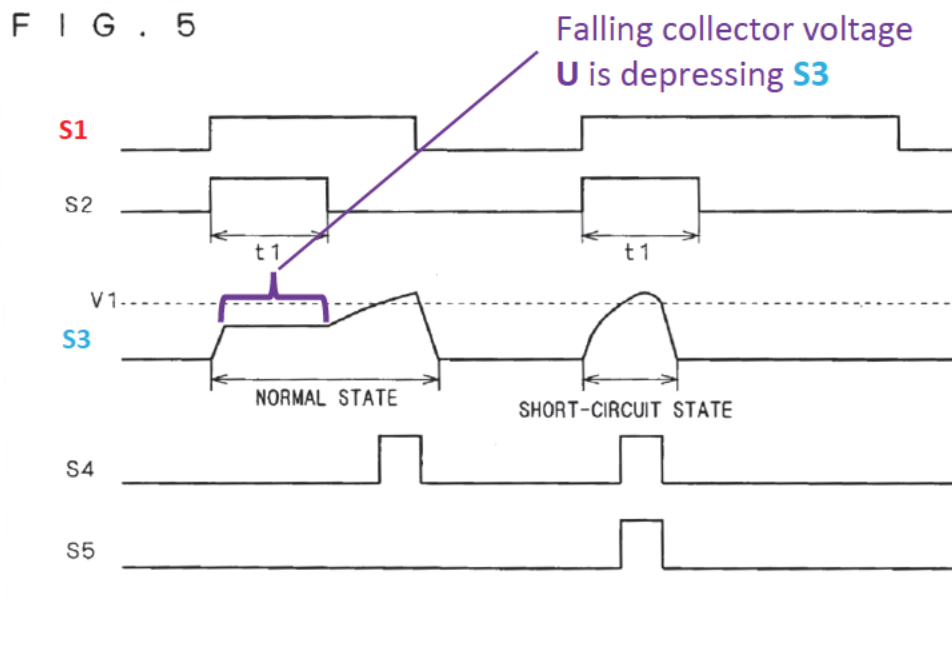
18. Fig. 2 shows one of Sakura's preferred embodiments. Signal $S1/U_{IN}$ is a control input. When $S1/U_{IN}$ is low IGBT 12 is off and no current flows through it. In this state the output of inverter G3 is high, RS latch 3 is being reset, and G4 and G5 control driver transistors 4 and 5 to force output $S3/U_{OUT}$ low. This is the starting condition for the circuit. When $S1/U_{IN}$ goes high, G3 switches low, latch 3 remains low, and G4 and G5 control driver transistors 4 and 5 to force output $S3/U_{OUT}$ high. Simultaneously one-shot pulse generation Circuit 1 is triggered and signal S2 goes temporarily high.

F I G . 2



19. Fig. 5 shows several key waveforms and illustrates the differences between the non-shortened and shortened output states. If the output is not shortened when IGBT 12 is turned on it starts conducting current and the

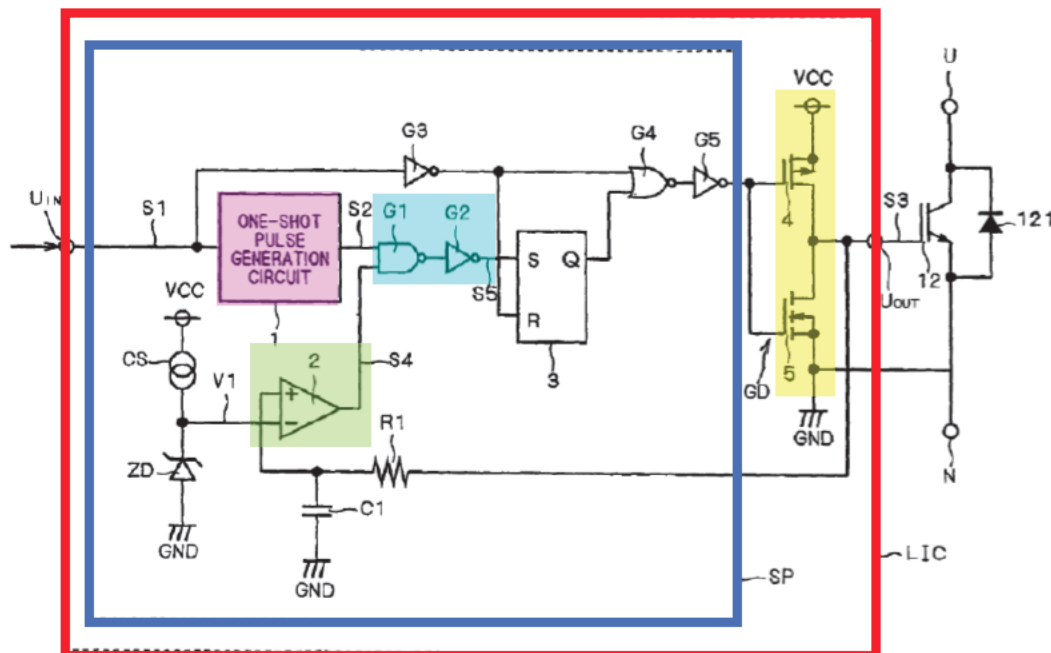
collector voltage **U** (not shown in Ohi's Fig. 5) drops. This dropping voltage couples through the Miller capacitance back into signal **S3/U_{OUT}**, the gate of **IGBT 12**, "stealing" some of the drive current supplied through transistor 4. This reduces and then stalls the voltage increase of **S3/U_{OUT}** until the output has almost completely switched and the collector voltage drop slows.



20. Comparator 2 continuously monitors the signal **S3/U_{OUT}** through an RC filter created by R1 and C1. In the case of normal operation **S3/U_{OUT}** will not rise above reference voltage V1 until after signal S2 has dropped low, blocking signal propagation through NAND gate G1. In the case where the output voltage is shorted to some constant voltage, e.g. ground, the collector voltage **U** doesn't change in response to **IGBT 12** turning on. Since the collector voltage doesn't change, there is no feedback current through the Miller

capacitance to slow down the rise of $S3/U_{OUT}$. This leads to $S3/U_{OUT}$ quickly rising above reference voltage $V1$, which causes signal $S4$ to go high while signal $S2$ is still high. This in turn sets latch 3, causing its Q output to rise. This propagates through $G4$ and $G5$ causing transistors 4 and 5 to drive $S3/U_{OUT}$ low, shutting off IGBT 12 before it can be damaged.

F I G . 2



21. This corresponds to the language in Claim 1 as indicated above (note: **colored fonts** match (out)lines of the same color, **highlighted text** matches regions highlighted with the same color):

Claim 1: A **semiconductor device controlling a drive of an insulated gate transistor** by generating a control output signal on a basis of a control input signal, comprising:

- a. a **driver outputting said control output signal** and
- b. a **short-circuit protection circuit** detecting said control output signal and controlling and forcing said driver to stop said control output signal when a detecting voltage of said control output signal exceeds a predetermined reference voltage before a predetermined period passes after said control output signal indicates a conduction of said insulated gate transistor, wherein
- c. said **short-circuit protection circuit** includes:
- d. **pulse generation circuit** receiving said control input signal and outputting a first pulse signal being significant only in said predetermined period according to a timing when said control input signal indicates the conduction of said insulated gate transistor;
- e. a **comparator** receiving the detecting voltage of said control output signal, performing a comparison with said reference voltage and outputting a second pulse signal being significant during a period when the detecting voltage of said control output signal exceeds said reference voltage; and
- f. a **logical circuit** receiving said first and second pulse signals and outputting a stop signal forcing said driver to stop said control

output signal when said second pulse signal becomes significant during a period when said first pulse signal is significant.

22. Claim element (d) above appears in Fig. 2 as one-shot pulse generation circuit 1. When the input U_{IN} to the one-shot rises, the one-shot outputs a high going pulse of fixed width. In Fig. 2 the width of this first pulse signal is designed to be the time during which the driver output U_{OUT} is prevented from rising to its final value by the impact of current flowing back into the driver through the Miller capacitance of IGBT 12.

23. The nature of the second pulse signal in claim element (e) is not provided by a one-shot. The beginning of this pulse starts when output drive signal U_{OUT} rises above reference voltage $V1$ and ends when U_{OUT} falls below $V1$ as IGBT 12 is turned off. In normal operation the falling edge of this signal is caused by U_{IN} falling, while in the case of a short the pulse is ended by the short-circuit protection circuit SP shutting off the driver of U_{OUT} .

24. The logical circuit in claim element (f) receives the first and second pulse signals and if they overlap in time (for example, if they're simultaneously both high) shuts off the driver control to protect the IGBT 12. In Fig. 2 this circuit includes a latch that remembers if the output was shut off by such an overlap and prevents IGBT 12 from being turned on again before U_{IN} drops low. When U_{IN} drops low it resets the latch and allows the short-circuit

protection to operate normally the next time U_{IN} goes high. In this way IGBT 12 is protected from transient short-circuit conditions but does not require any additional input to restart normal operation once the short-circuit is removed.

VI. THE ASSERTED REFERENCE

25. I understand that the Petitioner has asserted a single ground of invalidity against '835 Patent Claims 1-2 based on U.S. Patent No. 6,906,574 to Ohi ("Ohi"). I have not been asked to form any opinions as to whether the reference identified by the Petitioner qualifies as prior art. For purposes of my analysis here, I will assume that Ohi qualifies as prior art to the '835 Patent.

VII. TECHNICAL BACKGROUND

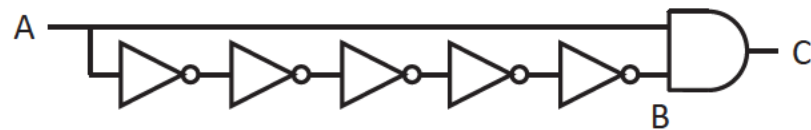
26. The operation of Sakata utilizes the Miller capacitance of the high voltage driver, an Insulated Gate Bipolar Transistor (IGBT). When a circuit amplifies a voltage signal and there is capacitance between the output and the input of the circuit, then the impact of this capacitance on the input is multiplied by the gain of the amplifier. It's worth noting that transistors always have some amount of parasitic capacitance between their gate/base (the typical input terminal) and their drain/collector (the typical output terminal). When the input signal changes, the amplifier (in these patents just a single transistor) causes the output to change by multiple of the input, referred to as the gain. If the gain is negative, as is the case here where the collector of the IGBT falls in response to

the gate rising, then the current that the input needs to supply to charge the Miller capacitance is the same current that would otherwise charge the gate. This results in a reduction in the applied gate voltage, slowing down the input signal and in the case of high-voltage switches potentially even stalling the input rise for a significant time before it is capable of completely switching.

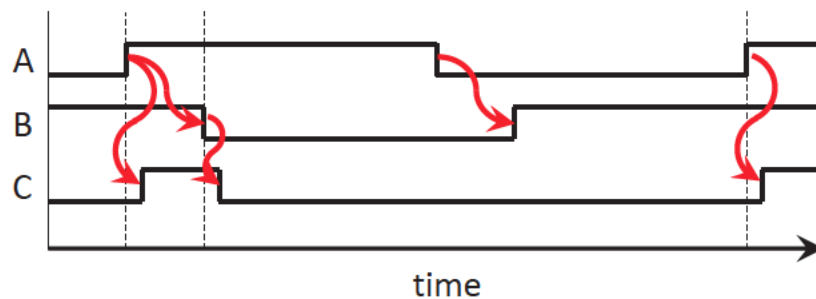
27. Sakata refers to a “pulse generation circuit” and “pulse signals”. Generally, a pulse generation circuit is a circuit that produces a pulse in response to an edge on its input. A one-shot is an example of such a circuit. When the input to a one-shot rises, the one-shot outputs a high going pulse of fixed width – the time at which this pulse ends depends only on the design of the one-shot and does not depend on the time at which the input falls. Variations of one-shots may trigger off the falling edge or both edges of the input, and the output may be a low going pulse instead of a high going one.

28. The presence of both rising and falling edges on a signal, without more, is not evidence of a pulse generation circuit. For example, pulse generation circuits often propagate a single signal through two parallel paths with different delays and then recombine the differently delayed versions of the signal to create a pulse as shown in the figure below. Output C is a pulse that starts in response to the rising edge of input A (causality is indicated by the **red arrows**) and continues until the falling edge of signal B. All the edges on output

C are ultimately caused by rising edges on input A. Output C does not change in response to the falling edge of signal A. Output C is not perfectly aligned with the edges of input A and signal B because of the delay of the AND gate. The high time of output C is approximately five inverter delays and independent of the high time of signal A.



(a) Pulse generation circuit



(b) Pulse generation circuit timing

VIII. OHI DOES NOT ANTICIPATE '835 PATENT CLAIMS 1 OR 2

29. I understand that for a claim to be anticipated each and every element of the claim must be disclosed in a single prior art reference with the elements arranged as specified in the claim. In my opinion, Ohi does not provide any disclosure in which each and every element of the '835 Patent Claims is disclosed as arranged in the claims.

30. Based on my review of Dr. Liu's declaration, I understand him to be relying at times on three different Ohi Embodiments:

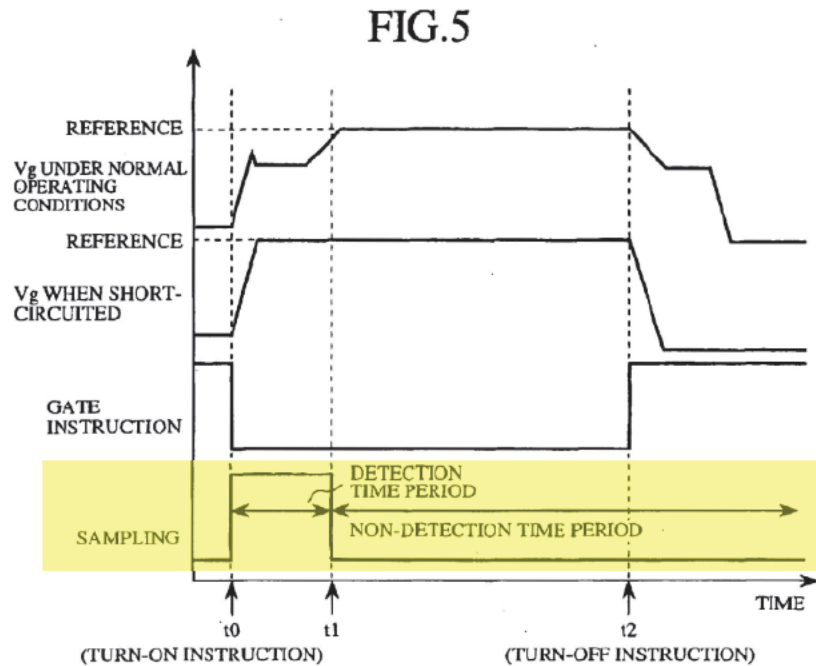
- a. Ohi Embodiment 2 (related to Figure 6)
- b. Ohi Embodiment 4 (related to Figure 10)
- c. Ohi Embodiment 5 (related to Figure 12)

31. My analysis of each of those embodiments is below. Additionally, Dr. Liu suggests that a POSITA would have understood Ohi to instruct a POSITA to modify Ohi Figure 12 as shown on page 38 of his declaration. I disagree, and address that below as well.

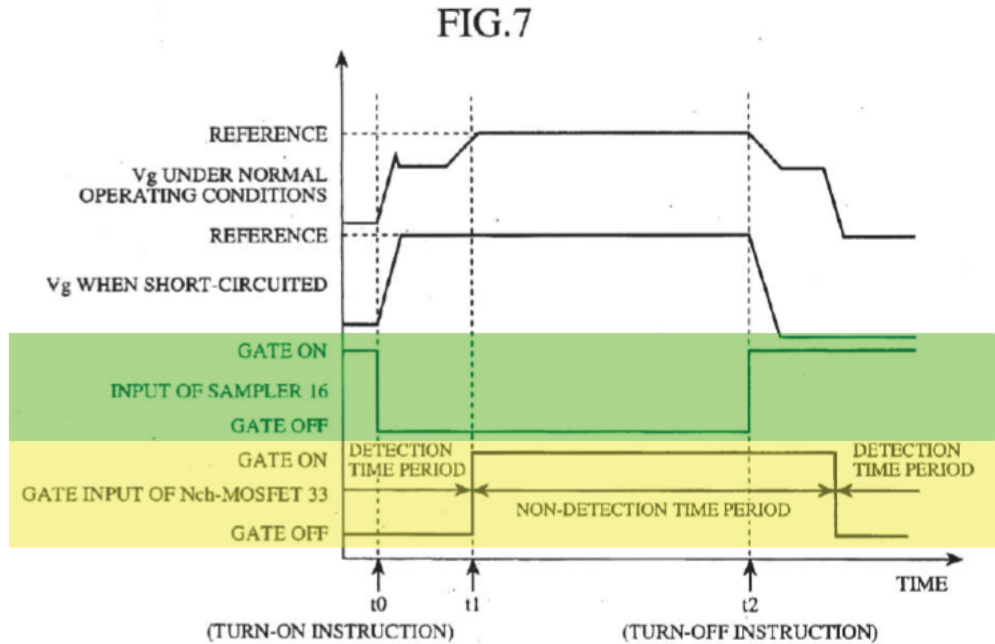
A. Ohi Embodiment 2 (Related to Figure 6)

32. At the end of EX1004 ¶39 Dr. Liu states “I have not separately considered whether Ohi’s circuit depicted in Fig. 6 also satisfies the Challenged Claims.” Fig. 6 shows Ohi’s Embodiment 2. I was asked to analyze whether Ohi’s Embodiment 2 and Figure 6 satisfy the Challenged Claims. In my opinion, it does not.

- c. Claim 1[c]: *said short-circuit protection circuit includes: pulse generation circuit receiving said control input signal and outputting a first pulse signal being significant only in said predetermined period according to a timing when said control input signal indicates the conduction of said insulated gate transistor;*



33. According to Ohi [EX1003 4:64-5:13] the sampler 16 controls the time interval during which gate voltage detector 17 is active. Note that while Ohi's Fig. 5 includes a bottom entry labeled "SAMPLING" to indicate when the gate voltage detector 17 is sampling the gate, this entry does not correspond to any individual signal in Fig. 6, it is only included to make the operation of the circuit clear.

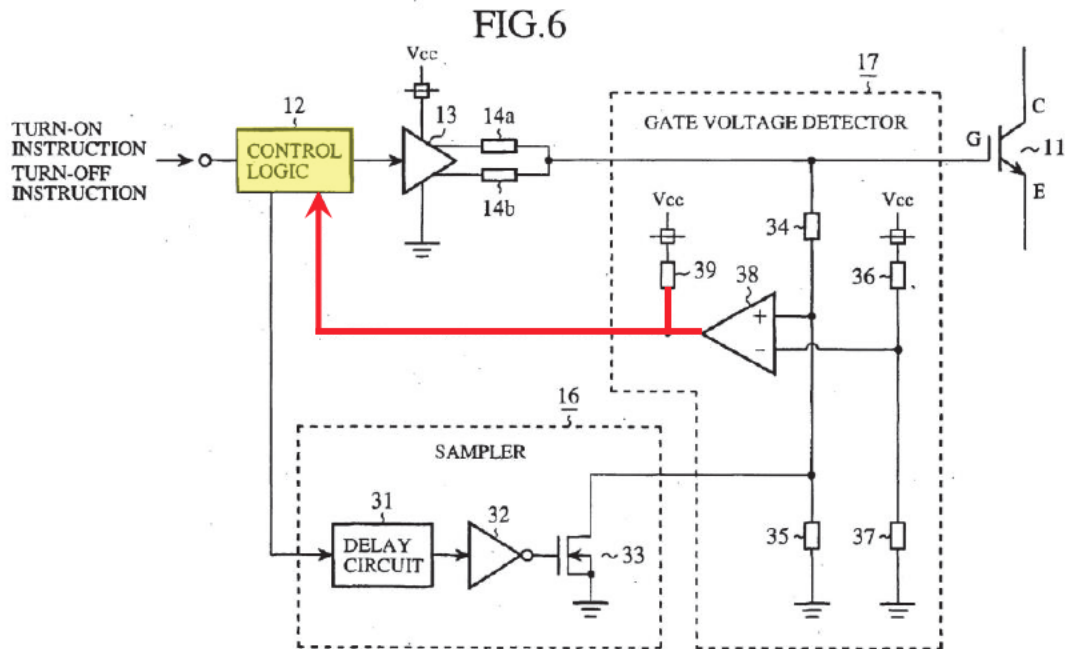


34. Furthermore, this entry in Fig. 5 does not accurately describe when the gate voltage in the second embodiment is being sampled. Fig. 7 shows the signal waveforms present in Fig. 6 and the **gate input of MOSFET 33** is low before the **input of sampler 16** arrives (falls). This is indicated in Fig. 7 where the detection time period on the left of the figure has already started before time t_0 , when V_g starts to rise. Similarly, we see that the detection time period on the right of the figure begins immediately after V_g falls, rather than waiting for the next *said control input signal* to arrive.

35. Consistent with the timing shown in Fig. 7, sampler 16 is triggered using a signal coming from control logic 12 that indicates when a turn-on instruction has been received. This signal is then passed to sampler 16 which simply outputs a delayed version of its input from control logic 12. Sampler 16

does not contain *pulse generation circuitry* and does not generate a pulse, it simply delays its input. There is no description of what happens in control logic 12 and thus no basis to assume that the needed *pulse generation circuitry* is present there. Even if sampler 16 were modified to become a *pulse generation circuit*, it receives an output from control logic 12 rather than *said control input signal*, and Ohi does not explain how the output of control logic 12 is generated. There is no *pulse generation circuit* and thus the output of sampler 16 cannot be the *first pulse signal* and Claim 1[c] is not met.

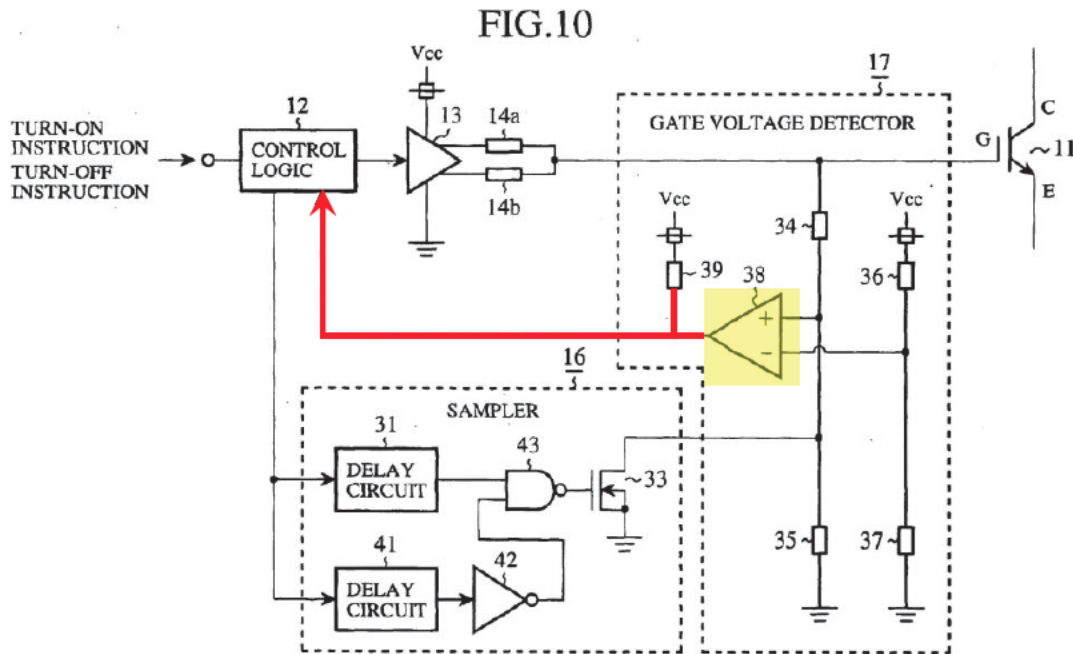
- e. Claim 1[e] *a logical circuit receiving said first and second pulse signals and outputting a stop signal forcing said driver to stop said control output signal when said second pulse signal becomes significant during a period when said first pulse signal is significant.*



36. The only logic that receives *the signal from comparator 38* is control logic 12. But control logic 12 does not receive any other signals from either sampler 16 or gate voltage detector 17 so even if *said first pulse control signal* could be identified in Fig. 6, it is not received by control logic 12 or any form of logical circuit.

37. In summary, embodiment 2 in Fig. 6 does not contain said *first pulse signal* nor does it contain a *logical circuit receiving said first and second pulse signals*. Without these components and connections embodiment 2 as illustrated in Fig. 6 does not meet Claim 1.

B. Ohi Embodiment 4 (Related to Figure 10)



Claim 1[e]: a logical circuit receiving said first and second pulse signals and outputting a stop signal forcing said driver to stop said control output signal when said second pulse signal becomes significant during a period when said first pulse signal is significant.

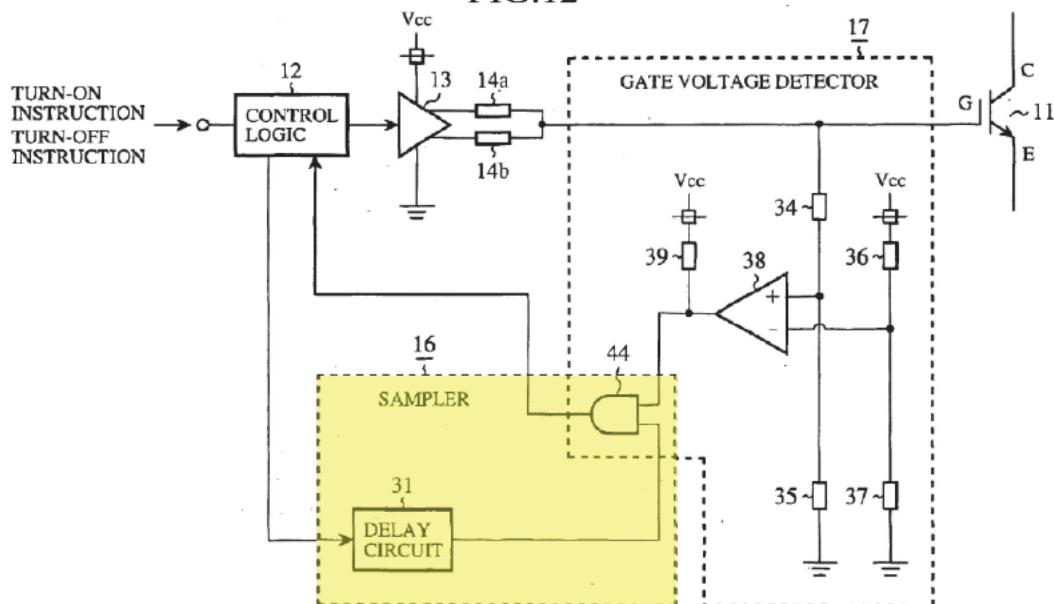
38. Looking at Fig. 10 above it is easily seen that there is no *logical circuit receiving said first and second pulse signals*. The output of sampler 16 is only connected to **comparator 38** (through MOSFET 33), and even if that output could be said to be a pulse, the claimed comparator is required to produce (not receive) the *second pulse signal*. Given that there is no *logical circuit receiving said first and second pulse signals*, embodiment 4 shown in Fig. 10 does not

meet Claim 1. The only logic that receives *the comparator output* is control logic 12. But control logic 12 does not receive any other signals from either sampler 16 or gate voltage detector 17 so even if *said first pulse control signal* was identified in Fig. 10, it is not received by control logic 12 or any form of logical circuit.

C. Ohi Embodiment 5 (Related to Figure 12)

39. Ohi's embodiment 5, shown in his Fig. 12 is a further modification to embodiment 2 shown in Fig. 6. As will be shown below, embodiment 5 as drawn in Fig. 12 does not satisfy Claim 1. Nor does Ohi specifically direct the reader to make any modifications which would meet Claim 1. And finally, combining control logic 12 with sampler 16 does not change the fact that Fig. 12 does not satisfy Claim 1. These three issues are dealt with individually.

FIG.6

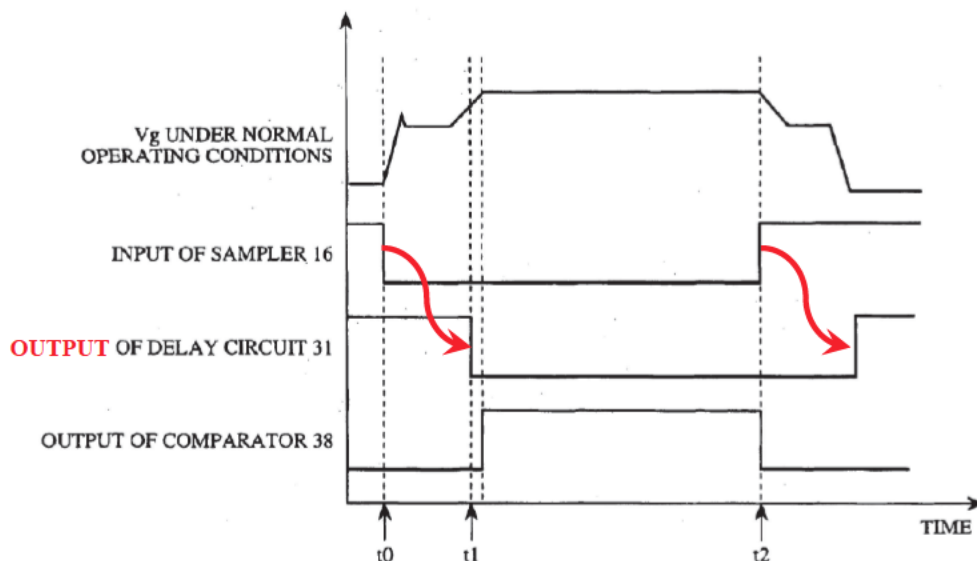


22

predetermined period according to a timing when said control input signal indicates the conduction of said insulated gate transistor;

40. Like the sampler in embodiment 2, the sampler in embodiment 5 shown in Fig. 12 does not contain a *pulse generation circuit*, it consists of only a delay circuit and an AND gate. The output of delay circuit 31 is simply a delayed version of the signal being input to the sampler as is shown in Fig. 13 below (note that the label of the third waveform has been changed to correct a typographical error in the original), it is not a pulse signal and thus it is not the *first pulse signal*.

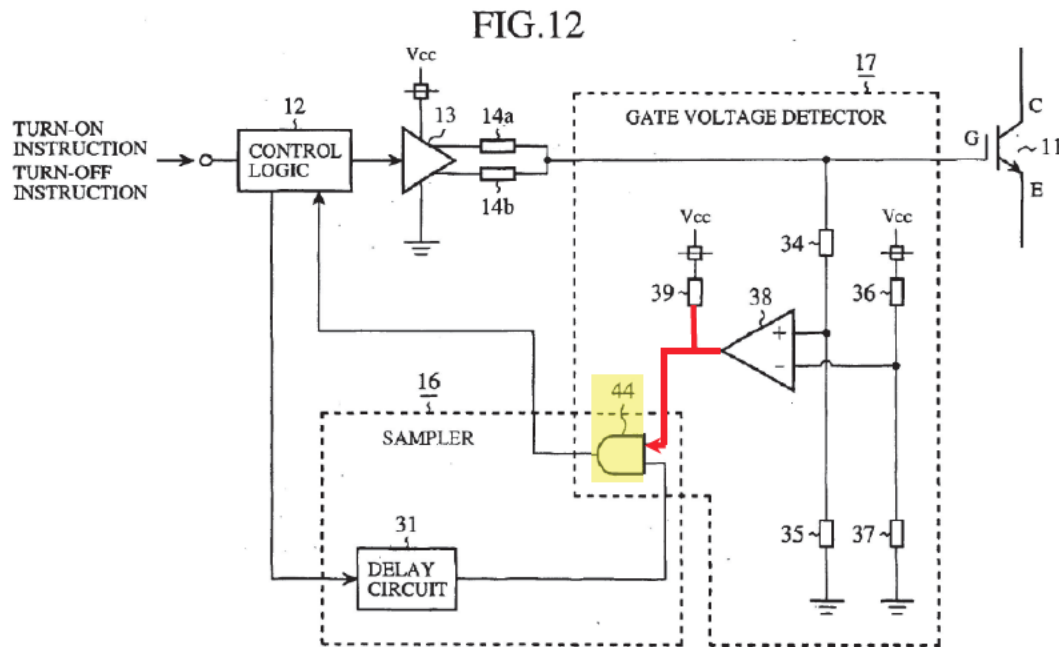
FIG.13



e. Claim 1[e]: *a logical circuit receiving said first and second pulse signals and outputting a stop signal forcing said driver to stop*

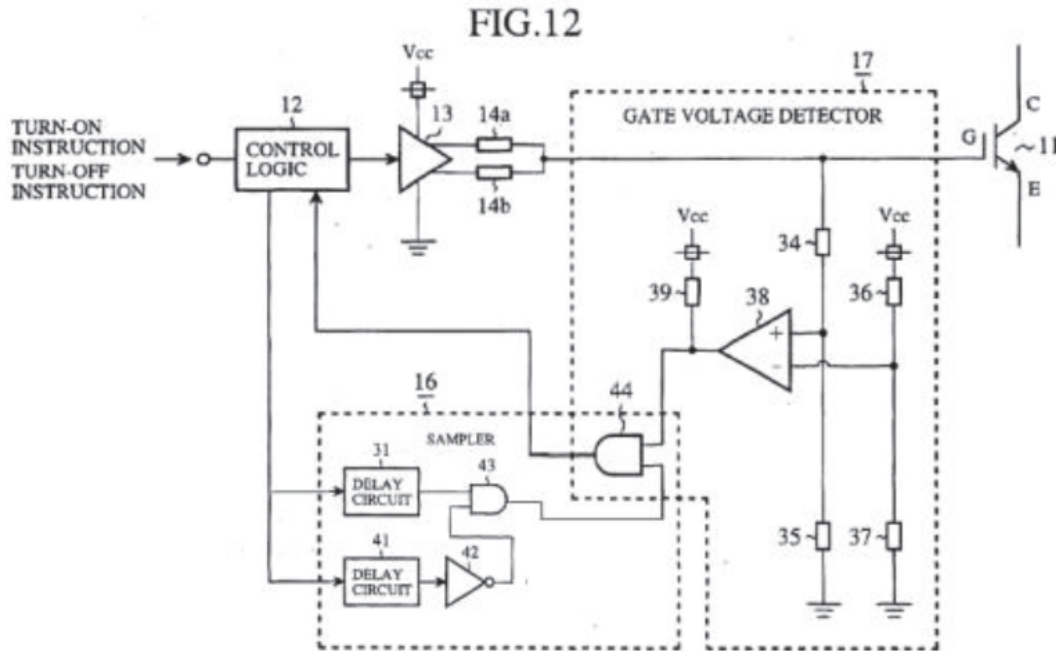
said control output signal when said second pulse signal becomes significant during a period when said first pulse signal is significant.

41. Nothing in embodiment 5 or Fig. 12 would be understood to generate a first pulse signal as claimed (as I noted above, the output of delay circuit 31 is simply a delayed version of the signal being input to the sampler). Even assuming comparator 38 provides a **second pulse signal** to a *logical circuit* (AND gate 44) as Dr. Liu suggests, without a *first pulse signal* Claim 1[e] is not met and Fig. 12 does not satisfy Claim 1.



2. Ohi does not teach a POSITA to modify Figure 12 as suggested by Dr. Liu

42. Dr. Liu suggests that a POSITA would have modified Ohi Fig. 12 to create the specific implementation shown on page 38 of his declaration.



43. I disagree that Ohi instructs a POSITA to make this specific modification—rather it appears that Dr. Liu started with knowledge of Claim 1 and then identified how to modify Fig. 12 to meet Claim 1: insert a *pulse circuit* to generate *said first pulse signal* into sampler 16, where it will be provided to the *logical circuit* that also receives *said second pulse circuit*. But my understanding is that in anticipation analysis a POSITA must start with the information available in Ohi, and not rely on reverse engineering Claim 1. Ohi's guidance is:

The detection time period during which the gate voltage V_g is detected can exclude a recovery time period immediately after the IGBT is turned on, like that of above-mentioned embodiment 4. [EX 1003 12:66-13:2].

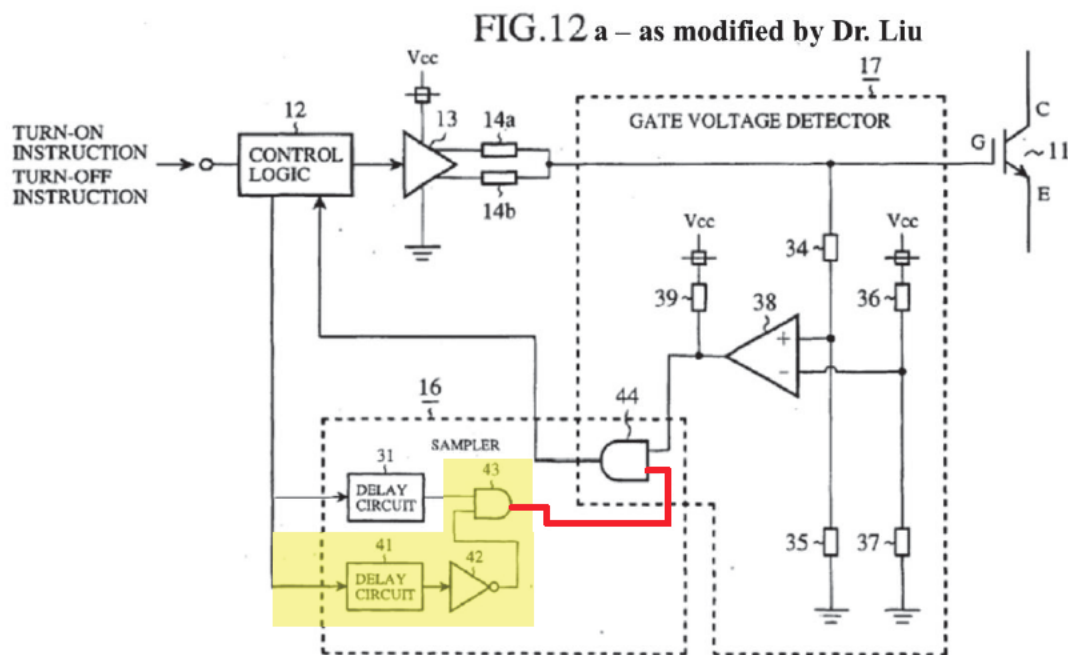
I interpret this as functional guidance to delay the start of the detection time, while I assume that Dr. Liu chose to interpret it as structural guidance saying specifically how to delay the start of the detection time period. However, in doing so he discovered that simply replacing the sampler structure shown in Fig. 12 with the sampler structure shown in Fig. 10 doesn't work (which undercuts his interpretation of the quoted passage as structural guidance). He then created a variation of this structure using Claim 1 as a guide, used that instead, and relied on that modified structure in his analysis of Claim 1. [EX 1004 ¶54]

44. Even if we start with the structural interpretation of the cited passage, we end up with different answers. Based on Ohi's teachings in embodiment 4:

In FIG. 10, reference numeral 41 denotes a delay circuit that accepts a gate instruction sent thereto from a control logic 12, and sends out the gate instruction after holding it only during a time period from a time t_0 to a time t_3 , reference numeral 42 denotes an inverter for inverting the logic of the gate instruction sent thereto from the delay circuit 41, and reference numeral 43 denotes a NAND circuit for placing an Nch-MOSFET 33 in an off state only during a time period from the time t_4 to a time t_l .

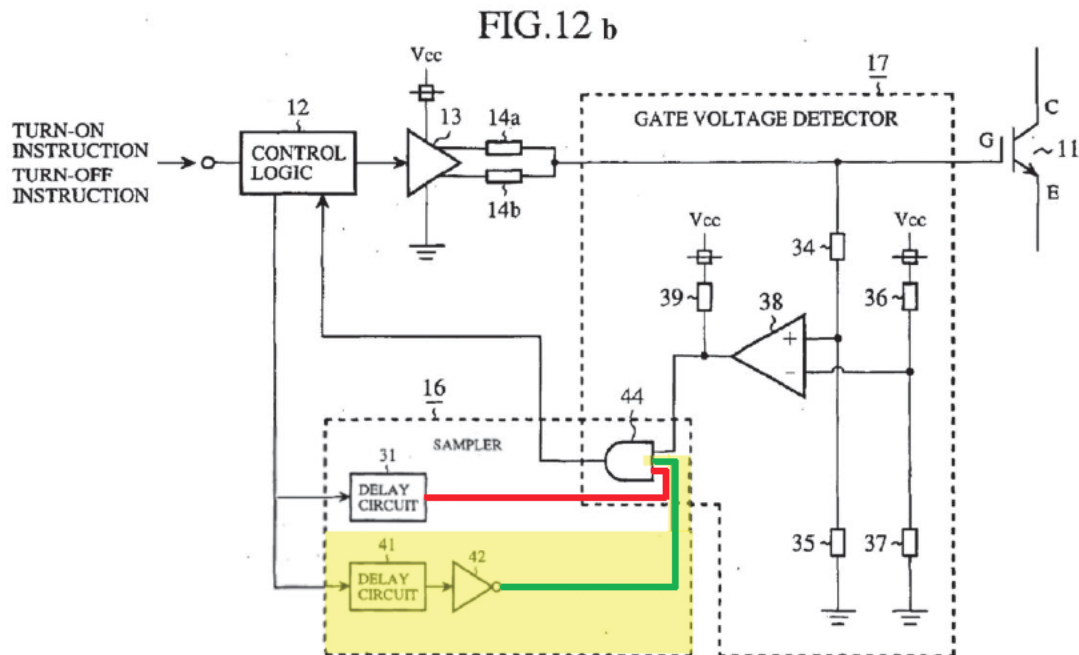
[EX 1003 11:21-30] Note that the reference to time t3 in this quote is a mistake. The correct reference is to time t4. Though this might have confused POSITA, it seems likely that they would have recognized that there are quite a few modifications that can be made to Fig. 12 that delay the beginning of the detection time period using a delay circuit 41 and an inverter 42. I address some of these potential modifications below as examples. In all cases the required circuit modifications are highlighted in yellow in the figures below.

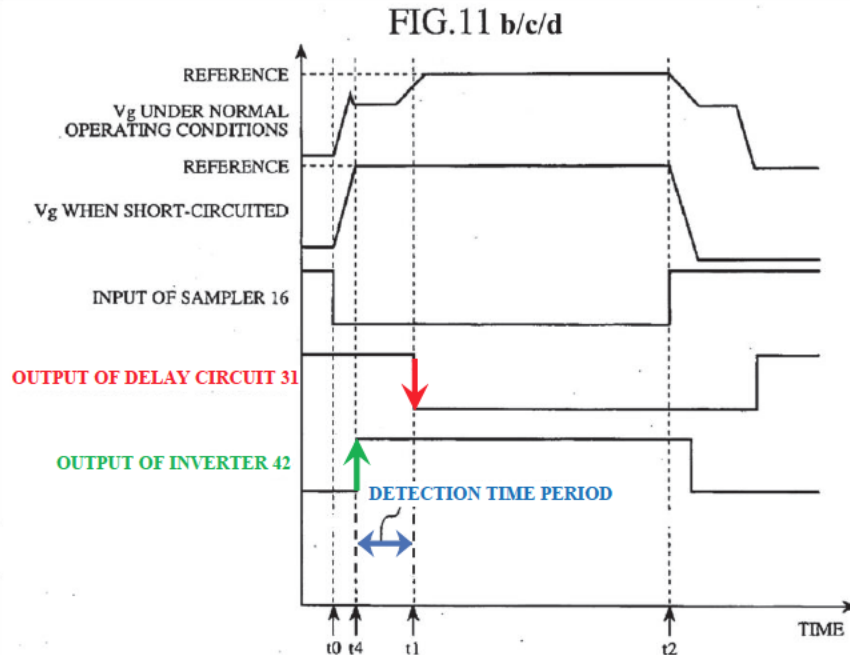
45. Shown below is Dr. Liu's modified Fig. 12 as Fig. 12a.



46. In Fig. 12a the output of AND gate 43 goes to AND gate 44. A pair of two input AND gates in this arrangement produces the same output signal as a three input AND gate. This leads to the implementation shown in Fig. 12b and the signal timing shown in Fig. 11b/c/d. A POSITA would recognize that a

single three input AND gate would be smaller, faster, lower power, and lower cost than a pair of two input gates in series. Though the improvements would be minor, I see nothing in Ohi that would have suggested that a POSITA use the less desirable modified version that Dr. Liu relies on. In this case sampler 16 no longer includes a *pulse generation circuit*. As shown in Fig. 11b/c/d two separate signals, the **output of inverter 42** and the **output of delay circuit 31**, delineate the start and end of the **detection time period** rather than a single pulse signal. As a result, this implementation does not satisfy Claim 1[c] or Claim 1[e].





47. If there is some reason to prefer a pair of two input AND gates, the implementations shown in Fig. 12c and Fig 12d are also possible, and share the waveforms shown in Fig. 11b/c/d. Neither contains a pulse generation circuit, nor do they meet the requirements of Claim 1[c] and Claim 1[e].

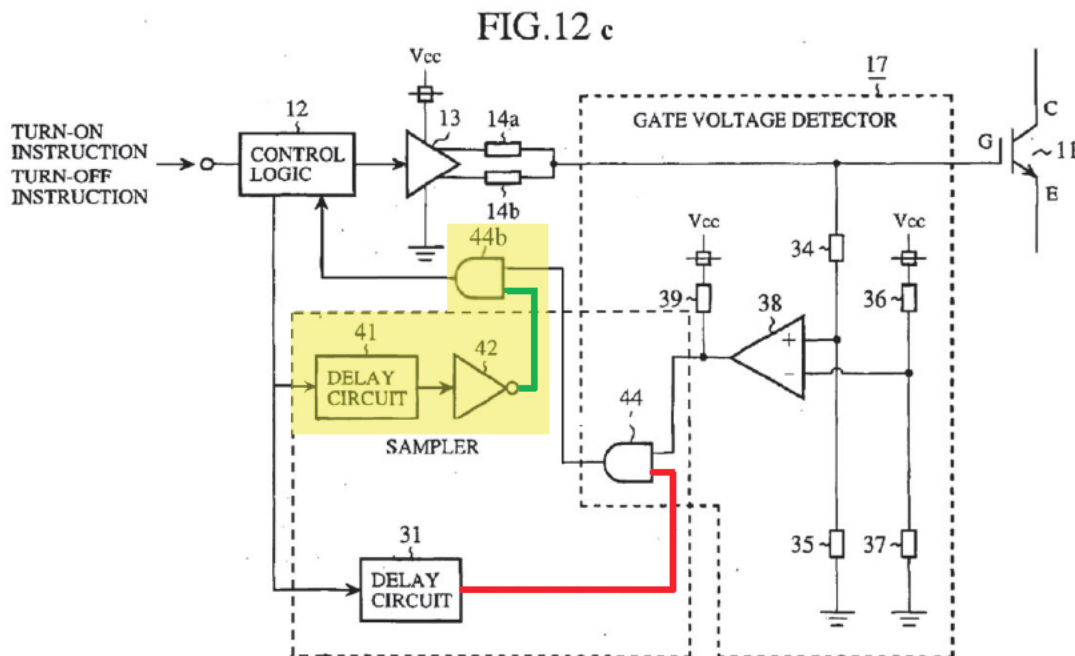
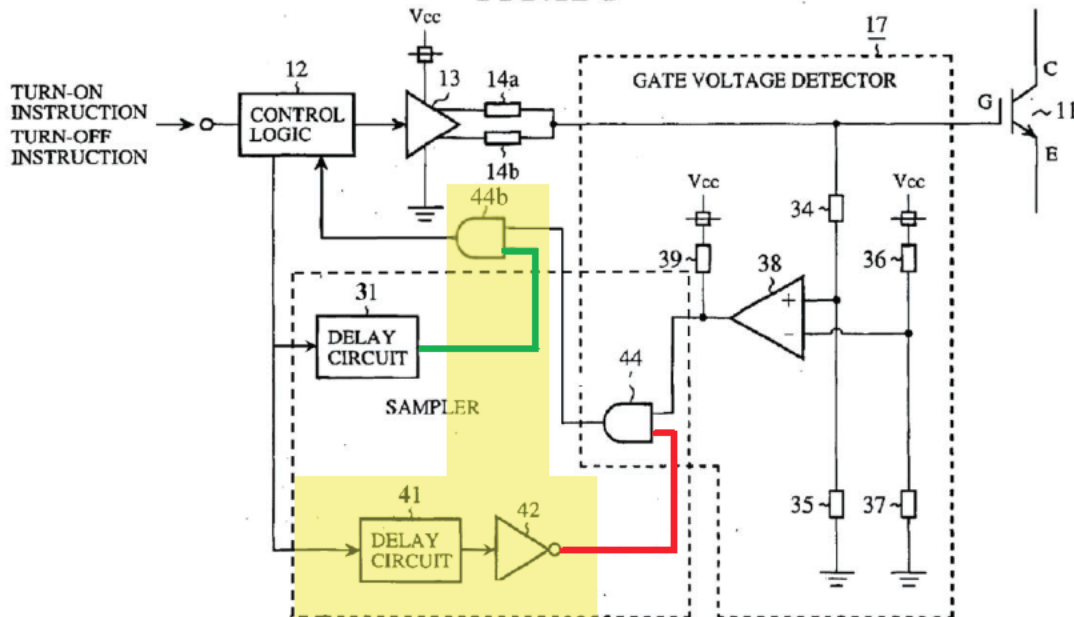


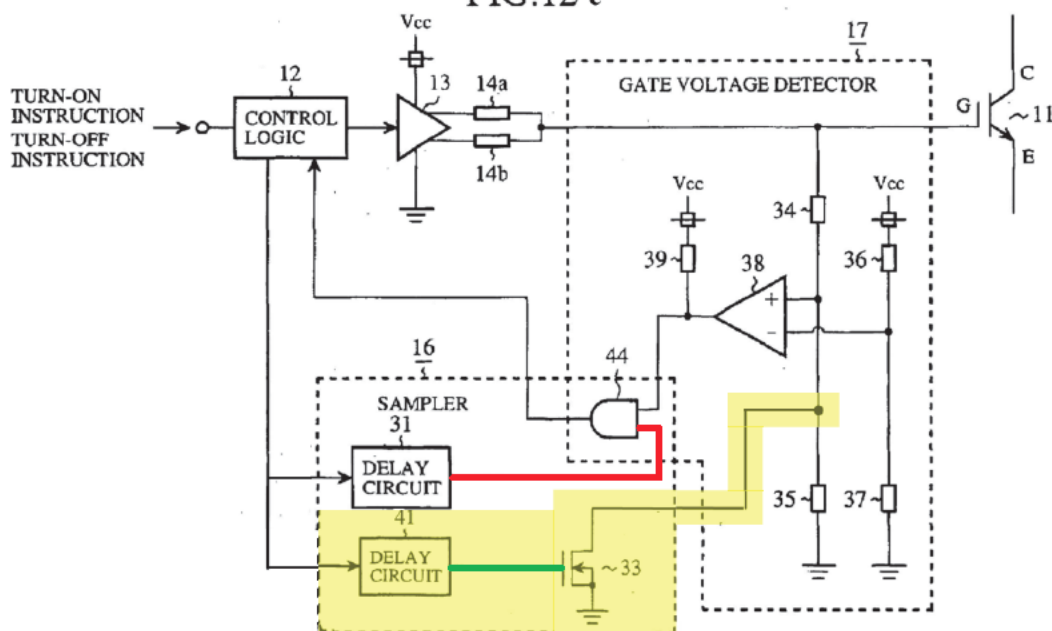
FIG.12 d

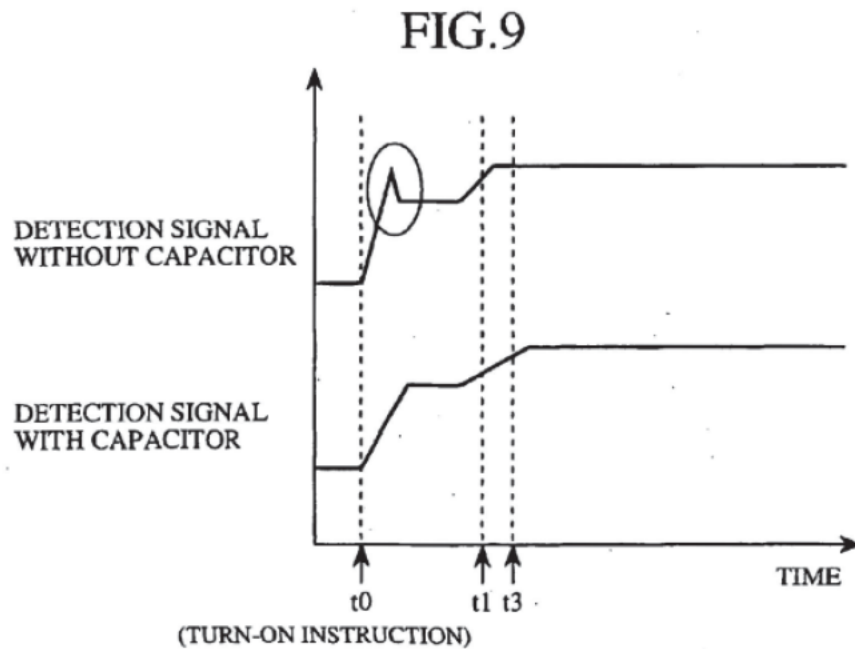
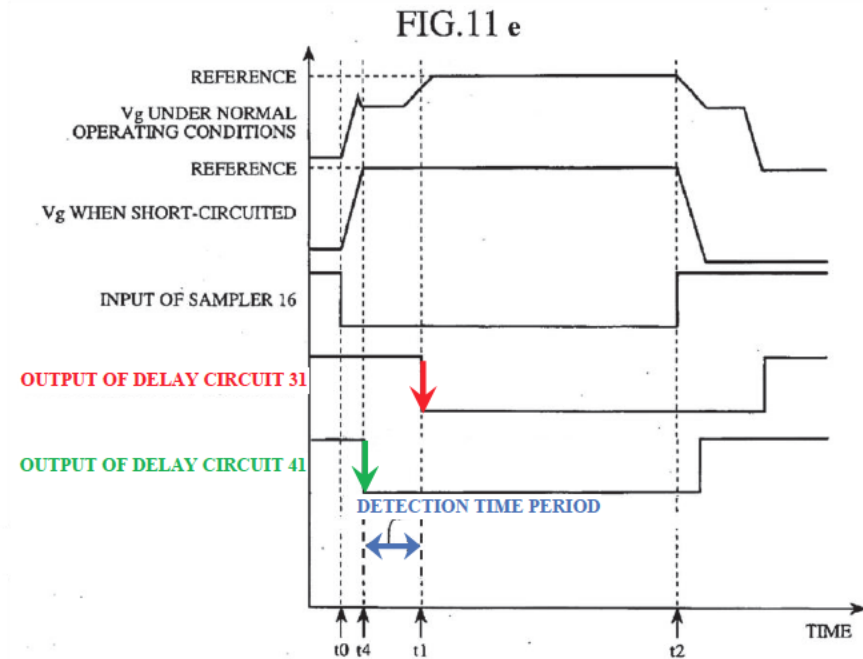


48. There is yet another way to insert delay circuit 41 to achieve a delay in the start of the detection time period, as shown in Fig. 12e. The timing for this circuit is shown in Fig. 11e. Again, there is no *pulse generation circuit* in sampler 16. As shown in Fig. 11e, two separate signals, the **output of delay circuit 41** and the **output of delay circuit 31**, delineate the start and end of the **detection time period** rather than a single pulse signal. As a result, this implementation does not satisfy Claim 1[c] or Claim 1[e]. This implementation requires the fewest added components of the five implementations and routes the output of transistor 33 to the input of comparator 38 in the same manner as Ohi's Fig. 10. An engineer knows that all components have parasitic capacitances and worries about the impact of adding this capacitance to critical signals. But Ohi teaches that adding extra capacitance to the positive input of the

comparator both reduces sensitivity to the initial peak in the gate waveform and makes the Miller plateau broader, both easing the precision required of delay circuits 31 and 41 [EX 1003 10:63-11:13]. Given this information a POSITA would have recognized that the extra capacitance of MOSFET 33 on this node is beneficial. This effect is shown in Ohi's Fig. 9.

FIG.12 e





49. In summary, Ohi 12:66-13:2 does not instruct to make the specific modification that Dr. Liu showed, but rather would have been understood to suggest a functional goal potentially met by multiple designs, of which I have provided several examples. None of the examples I provided

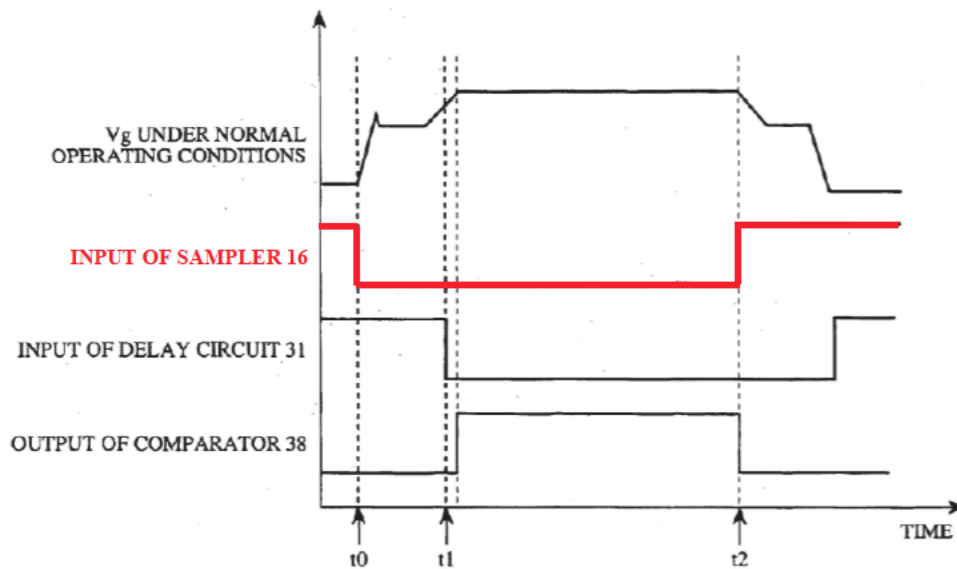
satisfy Claim 1 of the '835 patent, and this last example is simpler, likely more robust, and retains the capacitive benefits of Ohi Fig. 10 while Dr. Liu's proposal does not.

3. The “second manner” suggested by Dr. Liu in paragraph 63 still fails to teach every element of '835 Patent Claim 1

50. In EX 1004 ¶63 Dr. Liu suggests that Ohi's teachings somehow satisfy Claim 1 through the combination of control logic 12 and sampler 16. As shown in ¶33-35 and ¶40 above, embodiment 5 as shown in Fig. 12 fails to satisfy Claim 1[c] because it does not contain a *pulse generation circuit*. Dr. Liu suggests that somehow the series combination of control logic 12 and sampler 16 will rectify this shortcoming. But in Fig. 12 sampler 16 consists of just a delay circuit, as does sampler 16 in Fig. 6. Such a circuit cannot convert a single edge on its input into a pulse.

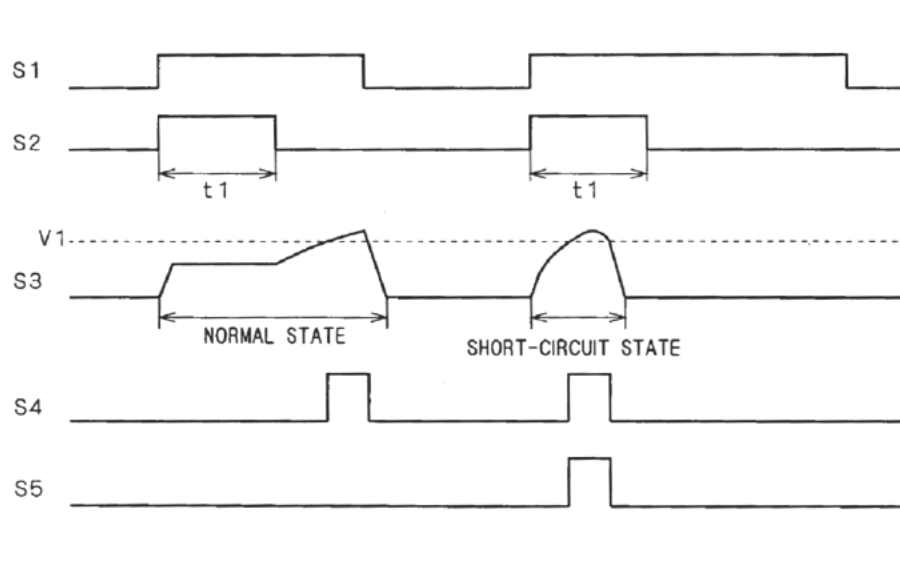
51. If control logic 12 contains a pulse generation circuit as Dr. Liu suggests, why does Fig. 13, the timing diagram for Fig. 12, not show a pulse appearing on the **input of sampler 16**? Instead, we see that the **input of sampler 16** has a single falling edge at time t0 aligned with the start of Vg being driven high and a single rising edge at time t2 aligned with the start of Vg being driven low. There are no pulses at either the start or the completion of the gate drive.

FIG.13



52. This reduces and then stalls the voltage increase of $S3/U_{OUT}$ until the output has almost completely switched and the collector voltage drop slows.

FIG. 5



53. In contrast to this is Fig. 5 of the '835 Patent. The timing diagram for the output S2 of the pulse generation circuit shows a pulse (containing both

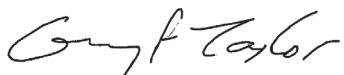
a rising and a falling edge) in response to the beginning of S1 being driven high, and no pulse aligned with S1 being driven low. The absence of such features show that the **input of sampler 16** shown in Fig. 13 is not the output of a *pulse generation circuit*. With no *pulse generation circuit* Claim 1[c] is not satisfied.

IX. MISCELLANEOUS

54. My work on this matter is being billed at an hourly rate of \$400 per hour and is not contingent on the outcome of this proceeding. I am also being reimbursed for reasonable expenses I incur in relation to my services provided for this proceeding.

55. All statements made herein of my own knowledge are true and all statements made on information and belief are believed to be true. I further understand that willful false statement and the like are punishable by fine or imprisonment, or both under Section 1001 of Title 18 of the United States Code. I declare under penalty of perjury that the foregoing is true and correct.

Date: April 26, 2023

By: 
Dr. Gregory F. Taylor