

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

APPLE INC.,
Petitioner,

v.

ARIGNA TECHNOLOGY LTD.,
Patent Owner.

IPR2023-00453
Patent 7,183,835 B2

Before GARTH D. BAER, SHARON FENICK, and
STEVEN M. AMUNDSON, *Administrative Patent Judges*.

AMUNDSON, *Administrative Patent Judge*.

DECISION
Denying Institution of *Inter Partes* Review
35 U.S.C. § 314

I. INTRODUCTION

Apple Inc. (“Petitioner”) filed a Petition requesting an *inter partes* review of claims 1 and 2 in U.S. Patent No. 7,183,835 B2 (Exhibit 1001, “the ’835 patent”) under 35 U.S.C. §§ 311–319. Paper 1 (“Pet.”). Arigna Technology Ltd. (“Patent Owner”) filed a Preliminary Response. Paper 6 (“Prelim. Resp.”).

Under 37 C.F.R. § 42.4(a), we have authority to determine whether to institute an *inter partes* review. We may institute an *inter partes* review only if “the information presented in the petition filed under section 311 and any response filed under section 313 shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.” 35 U.S.C. § 314(a) (2018). The “reasonable likelihood” standard is “a higher standard than mere notice pleading” but “lower than the ‘preponderance’ standard to prevail in a final written decision.” *Hulu, LLC v. Sound View Innovations, LLC*, IPR2018-01039, Paper 29 at 13 (PTAB Dec. 20, 2019) (precedential).

After considering the Petition, the Preliminary Response, and the evidence of record, and for the reasons explained below, we determine that Petitioner has not demonstrated a reasonable likelihood that it would prevail in proving the unpatentability of at least one claim challenged in the Petition. Hence, we deny the Petition and do not institute an *inter partes* review.

II. BACKGROUND

A. Real Parties in Interest

Petitioner identifies itself as the real party in interest. Pet. 61. Patent Owner identifies itself as the real party in interest. Paper 4, 2. The parties do not raise any issue about real parties in interest.

B. Related Matters

Petitioner and Patent Owner identify the following proceedings as related matters involving the '835 patent:

- *Arigna Technology Ltd. v. Samsung Electronics Co., Ltd. et al.*, No. 6:22-cv-00151 (W.D. Tex. filed Feb. 10, 2022) (currently stayed); and
- *In the Matter of Certain Power Semiconductors, and Mobile Devices and Computers Containing Same*, Inv. No. 337-TA-1308 (ITC filed Feb. 13, 2022).

Pet. 61; Paper 4, 2.

C. The '835 Patent (Exhibit 1001)

The '835 patent, titled “Semiconductor Device Which Realizes a Short-Circuit Protection Function Without Shunt Resistor, and Semiconductor Device Module,” issued on February 27, 2007, from an application filed on December 29, 2004. Ex. 1001, codes (22), (45), (54). The patent states that the “invention relates to a semiconductor device and a semiconductor device module, and more particularly, it relates to a semiconductor device and a semiconductor device module including a short-circuit protection function of an insulated gate type switching device such as an IGBT (Insulated Gate Bipolar Transistor) and so on.” *Id.* at 1:10–15; *see id.* at code (57).

For a conventional IGBT and a control circuit packaged together as “an IPM (Intelligent Power Module),” the '835 patent explains that “a short-circuit protection is performed by connecting a shunt resistor detecting a main current flowing between main power terminals of the switching device outside the package and monitoring the main current.” Ex. 1001, 1:17–25. The patent describes problems with a conventional IPM, such as the need for

a “current detecting terminal” and a “filter circuit such as a CR filter” to “remove a noise entering the shunt resistor and the current detecting terminal.” *Id.* at 1:32–45.

The ’835 patent purports to address those problems by providing a semiconductor device for controlling “a drive of an insulated gate transistor by generating a control output signal on a basis of a control input signal” and achieving “a short-circuit protection function without a shunt resistor.” Ex. 1001, 1:49–55; *see id.* at 3:65–4:2. The semiconductor device includes (1) “a driver outputting the control output signal” and (2) “a short-circuit protection circuit detecting the control output signal.” *Id.* at 1:52–58. The short-circuit protection circuit forces “the driver to stop the control output signal when a detecting voltage of the control output signal exceeds a predetermined reference voltage before a predetermined period passes after the control output signal indicates a conduction of the insulated gate transistor.” *Id.* at 1:56–62, 1:64–2:3.

The '835 patent's Figure 2 (reproduced below) depicts a semiconductor device for controlling a drive of an insulated gate transistor:

F I G . 2

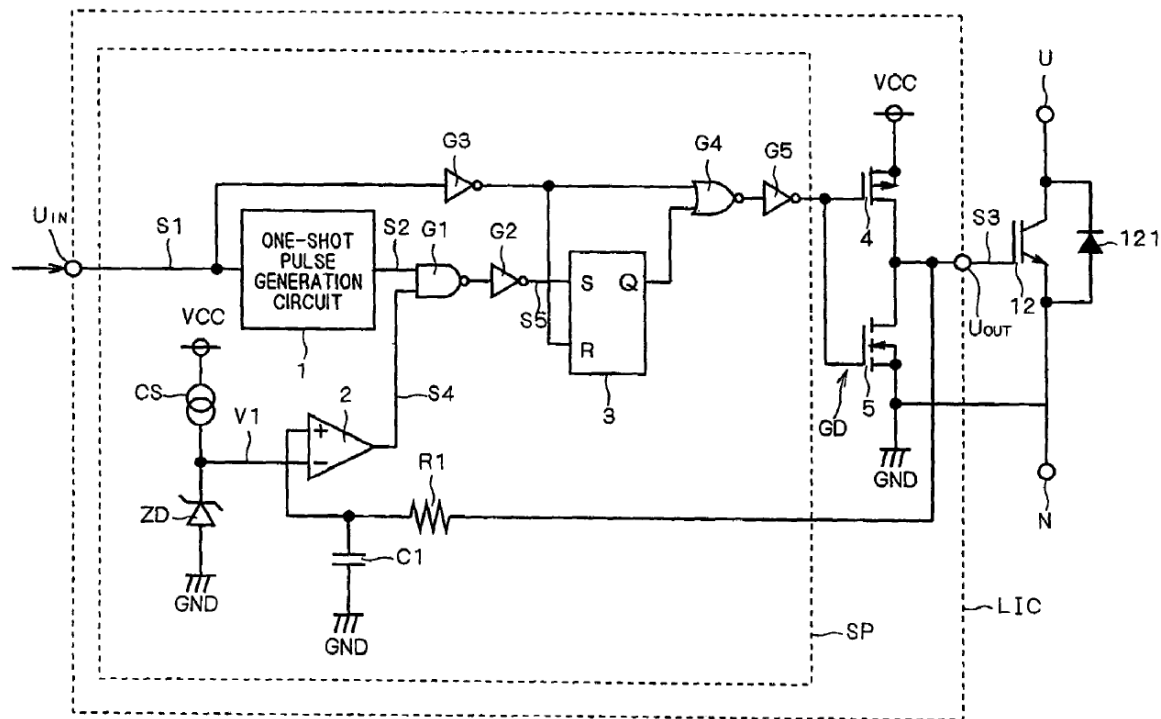


Figure 2 illustrates a control device LIC including a gate driver GD and a short-circuit protection circuit SP. *See* Ex. 1001, 2:15–17, 4:8–13, 5:50–51, Fig. 2. The control device's U_{out} terminal connects to “the gate electrode of the transistor 12.” *Id.* at 4:14–16, Fig. 2.

As Figure 2 shows, the gate driver GD includes “a P channel MOS transistor 4 and a[n] N channel MOS transistor 5 connected in series between a drive voltage VCC and the ground potential GND.” Ex. 1001, 4:28–31, Fig. 2. The gate driver GD supplies “a control output signal S3 to the gate electrode of the transistor 12.” *Id.* at 4:27–33, Fig. 2.

As Figure 2 also shows, short-circuit protection circuit SP includes, among other components, one-shot pulse generation circuit 1, comparator 2,

and RS flip-flop circuit 3. Ex. 1001, 5:35–40, Fig. 2. Comparator 2 receives the control output signal S3 at “a + (plus) side input terminal” and the reference voltage V1 at “a - (minus) side input terminal.” *Id.* at 4:32–37, Fig. 2. Comparator 2 outputs the comparison result as “a comparison result signal S4.” *Id.* at 4:37–38, Fig. 2.

The control device’s U_{in} terminal receives “a control input signal S1” supplied “from the outside.” Ex. 1001, 4:50–52, 5:55–56, Fig. 2. The control input signal S1 “is supplied not only to the gate driver GD via an inverter circuit G3, a NOR circuit G4 and an inverter circuit G5 but also to” one-shot pulse generation circuit 1. *Id.* at 4:51–55, Fig. 2.

One-shot pulse generation circuit 1 “is a circuit which rises according to a timing of a rising of the control input signal S1 and outputs singly a pulse signal S2 maintaining a high potential (‘H’) state for a certain period which is predetermined.” Ex. 1001, 4:56–60. “The pulse signal S2 outputted by the one-shot pulse generation circuit is supplied to a NAND circuit G1 with the comparison result signal S4 outputted by the comparator 2.” *Id.* at 5:35–38, Fig. 2. An “output of the NAND circuit G1 is supplied to a set input (S) of a RS flip-flop circuit 3 as a signal S5 via an inverter circuit G2.” *Id.* at 5:38–40, Fig. 2.

The '835 patent's Figure 5 (reproduced below) depicts a timing chart:

F I G . 5

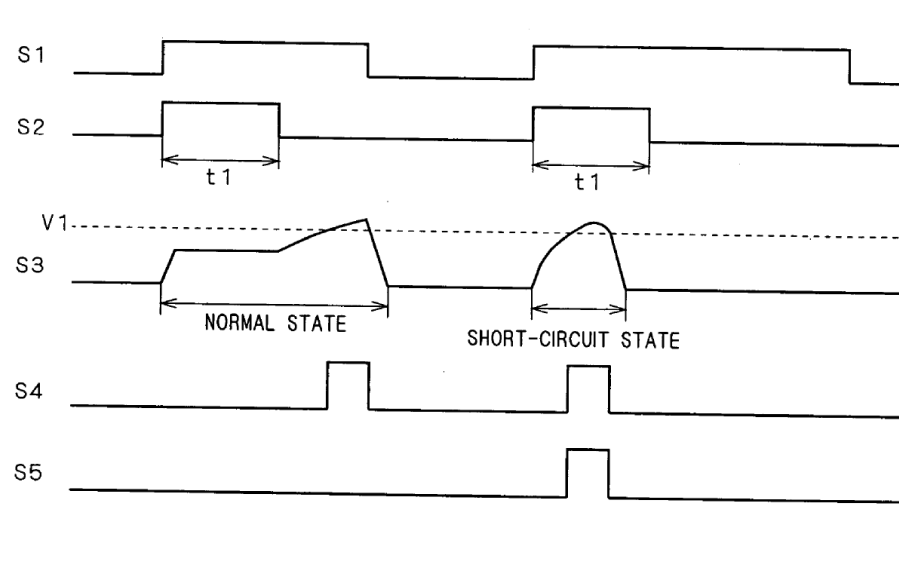


Figure 5 illustrates a timing chart for signals S1, S2, S3, S4, and S5 in Figure 2. *See* Ex. 1001, 2:22–24, 5:52–54, Fig. 5.

As Figure 5 shows, “the control output signal S3 outputted from the gate driver GD” increases as follows after the control input signal S1 transitions from a low level to a high level to turn on transistor 12:

- (1) “rises according to the building up of the control input signal S1”;
- (2) “is clamped to a certain voltage for a determined period by a mirror [sic] effect”; and
- (3) “rises to be a value almost equal to the drive voltage VCC of the gate driver GD after that.”

Ex. 1001, 5:55–6:3, Fig. 5; *see id.* at 6:6–10. Further, the control output signal S3 “falls according to a trailing edge of the control input signal S1” to turn off transistor 12. *Id.* at 6:3–5, Fig. 5.

As Figure 5 also shows, the pulse signal S2 is “in the significant condition according to the building up of the control input signal S1” during

the time period t1. Ex. 1001, 6:35–38, Fig. 5. Hence, “when the transistor 12 normally operates, the pulse signal S2 and the comparison result signal S4 outputted by the comparator 2 do not come to be in the significant condition synchronously.” *Id.* at 6:41–44, Fig. 5. As a result, (1) “the signal S5 supplied to the setting input of the RS flip-flop circuit 3 maintains the low potential (‘L’) state,” (2) “the Q output of the RS flip-flop circuit 3 maintains the ‘L’ state,” (3) “the control output signal S3 is maintained,” and (4) “the transistor 12 is maintained” in the ON state. *Id.* at 6:44–49, Fig. 5.

If, however, “the transistor 12 comes to be” in the ON state when “a short-circuit occurs between the source and the drain of the transistor 12,” a “clamp period of the voltage does not exist in the control output signal S3, and the voltage of the control output signal S3 rises rapidly to be almost equal to that of the drive voltage VCC.” Ex. 1001, 6:56–62, Fig. 5. Figure 5 shows this as the short-circuit state. *Id.* at 6:62–64, Fig. 5.

In the short-circuit state, “the voltage of the control output signal S3 rises rapidly and exceeds the reference voltage V1 of the comparator 2,” and “the comparison result signal S4 outputted from the comparator 2 comes to be in the significant condition.” Ex. 1001, 6:65–7:3, Fig. 5. Also, “the pulse signal S2 is outputted from the one-shot pulse generation circuit 1 according to the rising of the control input signal S1, and the comparison result signal S4 also comes to be in the significant condition during the period when the pulse signal S2 is in the significant condition.” *Id.* at 7:4–9, Fig. 5.

Hence, “a period when the pulse signal S2 and the comparison result signal S4 are in the significant condition synchronously exists.” Ex. 1001, 7:9–11, Fig. 5. As a result, (1) “the signal S5 supplied to the setting input of the RS flip-flop circuit 3 comes to be in the ‘H’ state during that period,”

(2) “the Q output of the RS flip-flop circuit 3 changes to be in the ‘H’ state,”
(3) “the P channel MOS transistor 4 of the gate driver GD comes to be in
OFF state,” (4) “the N channel MOS transistor 5 comes to be in ON state,”
(5) “the control output signal S3 comes to be in the ‘L’ state,” and (6) “the
transistor 12 is forced to be in OFF state.” *Id.* at 7:1–18.

Because “the short-circuit state is detected by monitoring the control
output signal S3 of the transistor 12” and “the control output signal S3 is
forced to stop” when a short circuit occurs, there is no need for a shunt
resistor or a current detecting terminal, unlike a conventional IPM.
Ex. 1001, 7:23–33.

D. The Challenged Claims

Petitioner challenges claims 1 and 2 in the ’835 patent. Pet. 1, 14–59.
Claims 1 and 2 read as follows (with formatting added for clarity and
numbers and letters added for reference purposes):¹

1. [1(p)] A semiconductor device controlling a drive of an
insulated gate transistor by generating a control output signal on
a basis of a control input signal, comprising:

[1(a)] a driver outputting said control output signal and

[1(b)] a short-circuit protection circuit detecting said
control output signal and controlling and forcing said driver to
stop said control output signal when a detecting voltage of said
control output signal exceeds a predetermined reference voltage
before a predetermined period passes after said control output
signal indicates a conduction of said insulated gate transistor,
wherein said short-circuit protection circuit includes:

[1(c)] pulse generation circuit receiving said
control input signal and outputting a first pulse signal
being significant only in said predetermined period

¹ We use the same numbers and letters that the parties use to identify the
claim language.

according to a timing when said control input signal indicates the conduction of said insulated gate transistor;

[1(d)] a comparator receiving the detecting voltage of said control output signal, performing a comparison with said reference voltage and outputting a second pulse signal being significant during a period when the detecting voltage of said control output signal exceeds said reference voltage; and

[1(e)] a logical circuit receiving said first and second pulse signals and outputting a stop signal forcing said driver to stop said control output signal when said second pulse signal becomes significant during a period when said first pulse signal is significant.

2. The semiconductor device according to claim 1, wherein said predetermined period when said first pulse signal is significant is set on a basis of a period when a voltage of said control output signal is clamped constantly when said insulated gate transistor normally operates.

Ex. 1001, 11:38–12:4.

E. The Asserted Reference

For its challenge, Petitioner relies on the following reference: U.S. Patent No. 6,906,574 B2, titled “Drive Circuit for Driving Power Semiconductor Device,” filed on July 28, 2003, and issued on June 14, 2005, to Ohi et al. (“Ohi”) (Exhibit 1003). *See* Pet. 14–59; Ex. 1003, codes (10), (22), (45), (54), (75). Petitioner asserts that Ohi qualifies as prior art under § 102(e). Pet. 16; *see* 35 U.S.C. § 102(e) (2006).²

² The Leahy-Smith America Invents Act (“AIA”), Pub. L. No. 112-29, 125 Stat. 284 (2011), amended 35 U.S.C. § 102 effective March 16, 2013. Because the filing date of the challenged claims predates the AIA’s amendments to § 102, this decision refers to the pre-AIA version of § 102.

At this stage of the proceeding, Patent Owner does not dispute that Ohi qualifies as prior art. *See* Prelim. Resp. 1–2, 20–61.

F. The Asserted Challenge to Patentability

Petitioner asserts the following challenge to patentability:

Claims Challenged	35 U.S.C. §	Reference/Basis
1–2	102(e)	Ohi

Pet. 14–59.

G. Testimonial Evidence

To support its challenge, Petitioner relies on the declaration of David Kuan-Yu Liu, Ph.D. (Exhibit 1004). Dr. Liu states, “I have been retained by counsel for Petitioner as a technical expert” and “have been asked to render certain opinions in regard to the IPR petition with respect to” the ’835 patent. Ex. 1004 ¶ 2. Dr. Liu also states, “I received a Bachelor of Science degree in Electrical Engineering from the University of California, Berkeley, in 1983,” “received a Master of Science and Ph.D. degrees in Electrical Engineering from Stanford University in 1985 and 1989, respectively,” and “have 20 years of experience as an engineer and engineering manager/director of Complementary Metal Oxide Semiconductor (CMOS) technology development.” *Id.* ¶¶ 5, 13.

To support its positions, Patent Owner relies on the declaration of Gregory F. Taylor, D. Eng. (Exhibit 2008). Dr. Taylor states, “I have been asked by” Patent Owner “to submit this declaration in response to a petition filed by Apple Inc. (the ‘Petition’) and declaration submitted by Dr. David Kuan-Yu Liu (the ‘Liu Declaration’).” Ex. 2008 ¶ 2. Dr. Taylor also states, “I earned a Doctor of Engineering (Ph.D.) degree in Computer and Systems Engineering from Rensselaer Polytechnic Institute in 1985,” “have been an

IEEE fellow since 2009,” “have published more than 60 peer reviewed papers,” and “am the inventor of 67 U.S. patents on integrated circuit design and testing.” *Id.* ¶¶ 4, 6.

III. DISCRETIONARY DENIAL

Patent Owner argues that we should exercise our discretion under § 325(d) to deny institution because:

- (1) the Examiner cited Ohi during the ’835 patent’s prosecution;
- (2) the “same art and arguments were previously presented to the Office”; and
- (3) the “patentability of the challenged claims was confirmed over that art and those arguments.”

See Prelim. Resp. 1, 11–20; 35 U.S.C. § 325(d); *Advanced Bionics, LLC v. MED-EL Elektromedizinische Geräte GmbH*, IPR2019-01469, Paper 6 (PTAB Feb. 13, 2020) (precedential).

Petitioner argues that we should decline to exercise our discretion under § 325(d) to deny institution because “the Examiner erred in a manner material to patentability” by failing to consider a particular embodiment in Ohi that “shows the precise circuit arrangement that the Examiner deemed lacking” from a cited embodiment in Ohi. *See* Pet. 10–14.

For the reasons explained below, we determine that Petitioner has not demonstrated a reasonable likelihood that it would prevail in proving the unpatentability of at least one claim challenged in the Petition. *See infra* § IV.D.2(a)(iii). Hence, we do not consider discretionary denial under § 325(d).

IV. PATENTABILITY ANALYSIS

A. Legal Principles: Anticipation

To “demonstrate anticipation, the proponent must show ‘that the four corners of a single, prior art document describe every element of the claimed invention.’” *Net MoneyIN, Inc. v. VeriSign, Inc.*, 545 F.3d 1359, 1369 (Fed. Cir. 2008) (quoting *Xerox Corp. v. 3Com Corp.*, 458 F.3d 1310, 1322 (Fed. Cir. 2006)). The prior-art document “must not only disclose all elements of the claim within the four corners of the document, but must also disclose those elements ‘arranged as in the claim.’” *Id.* (quoting *Connell v. Sears, Roebuck & Co.*, 722 F.2d 1542, 1548 (Fed. Cir. 1983)). Hence, a patent challenger cannot rely on portions from different, unrelated embodiments in a prior-art document to demonstrate anticipation. *See id.* at 1369, 1371.

The “disclosure of a limited number of combination possibilities” may anticipate a claim. *Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 851 F.3d 1270, 1274 (Fed. Cir. 2017). Hence, a reference may anticipate “if that reference teaches that the disclosed components or functionalities may be combined and one of skill in the art would be able to implement the combination.” *Blue Calypso, LLC v. Groupon, Inc.*, 815 F.3d 1331, 1344 (Fed. Cir. 2016). The “dispositive question regarding anticipation [is] whether one skilled in the art would reasonably understand or infer from the [reference’s] teaching” that it discloses every claim element arranged as in the claim. *In re Baxter Travenol Labs.*, 952 F.2d 388, 390 (Fed. Cir. 1991); *see Dayco Prods., Inc. v. Total Containment, Inc.*, 329 F.3d 1358, 1368 (Fed. Cir. 2003).

We analyze the anticipation issues according to these principles.

B. Level of Ordinary Skill in the Art

Factors pertinent to determining the level of ordinary skill in the art include (1) the educational level of the inventor; (2) the type of problems encountered in the art; (3) prior-art solutions to those problems; (4) the rapidity with which innovations are made; (5) the sophistication of the technology; and (6) the educational level of workers active in the field. *Envtl. Designs, Ltd. v. Union Oil Co.*, 713 F.2d 693, 696–97 (Fed. Cir. 1983). Not all factors may exist in every case, and one or more of these or other factors may predominate in a particular case. *Id.* These factors are not exhaustive, but merely a guide to determining the level of ordinary skill in the art. *Daiichi Sankyo Co. v. Apotex, Inc.*, 501 F.3d 1254, 1256 (Fed. Cir. 2007). Moreover, the prior art itself may reflect an appropriate skill level. *Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001).

Petitioner asserts that a person of ordinary skill in the art at the time of the alleged invention “would have had a graduate degree in electrical engineering or equivalent with at least two years of relevant work experience (e.g., in the field of circuit design).” Pet. 14. Petitioner also asserts that “[a]dditional education or experience might substitute for the above requirements.” *Id.* Dr. Liu’s testimony supports Petitioner’s assertions. *See* Ex. 1004 ¶¶ 22–24.

Patent Owner asserts that a person of ordinary skill in the art would have had either (1) “a bachelor’s degree in electrical engineering or a similar field, and approximately two years of industry or academic experience designing or analyzing power semiconductor devices” or (2) “a master’s degree or Ph.D. in electrical engineering or an equivalent field, with coursework, thesis, or dissertation work, or research experience in power

semiconductor devices.” Prelim. Resp. 8. Dr. Taylor does not specify an educational level or an amount of relevant work experience for ordinarily skilled artisan. *See, e.g.*, Ex. 2008 ¶ 16.

For an ordinarily skilled artisan with approximately two years of relevant work experience, Petitioner’s description requires more education (“a graduate degree”) than Patent Owner’s description (“a bachelor’s degree”). *See* Pet. 14; Prelim. Resp. 8. For an ordinarily skilled artisan with a graduate degree (“a master’s degree or Ph.D.”), Petitioner’s description requires more relevant work experience (“at least two years”) than Patent Owner’s description (no specified amount). *See* Pet. 14; Prelim. Resp. 8.

We adopt Petitioner’s description of an ordinarily skilled artisan because it comports with the technology and claims of the ’835 patent as well as the asserted prior art. For instance, a graduate degree and at least two years of relevant work experience would have allowed someone to understand the ’835 patent and the prior art. *See* Ex. 1004 ¶ 23. Additionally, someone with a higher skill level will understand the technology at least as well as someone with a lower skill level. *See Innovention Toys, LLC v. MGA Entm’t, Inc.*, 637 F.3d 1314, 1323 (Fed. Cir. 2011); *Tokai Corp. v. Easton Enters., Inc.*, 632 F.3d 1358, 1369 (Fed. Cir. 2011). We note that our analysis would not change if we adopted Patent Owner’s description of an ordinarily skilled artisan.

C. Claim Construction

We construe claim terms “using the same claim construction standard” that district courts use to construe claim terms in civil actions under 35 U.S.C. § 282(b). *See* 37 C.F.R. § 42.100(b) (2022). Under that standard, claim terms “are given their ordinary and customary meaning,

which is the meaning the term would have to a person of ordinary skill in the art at the time of the invention.” *Power Integrations, Inc. v. Fairchild Semiconductor Int’l, Inc.*, 904 F.3d 965, 971 (Fed. Cir. 2018) (citing *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312–13 (Fed. Cir. 2005) (en banc)). The meaning of claim terms may be determined by “look[ing] principally to the intrinsic evidence of record, examining the claim language itself, the written description, and the prosecution history, if in evidence.” *DePuy Spine, Inc. v. Medtronic Sofamor Danek, Inc.*, 469 F.3d 1005, 1014 (Fed. Cir. 2006) (citing *Phillips*, 415 F.3d at 1312–17).

Petitioner “proposes that the Board need not construe any claim language to resolve” the patentability challenge. Pet. 15.

Patent Owner “does not believe any constructions are necessary to resolve” the patentability challenge. Prelim. Resp. 10.

Based on the current record, we determine that no claim term requires an explicit construction to decide whether Petitioner satisfies the “reasonable likelihood” standard for instituting trial. “[O]nly those terms need be construed that are in controversy, and only to the extent necessary to resolve the controversy.” *Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999); see *Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017).

D. Alleged Anticipation by Ohi: Claims 1 and 2

Petitioner contends that claims 1 and 2 are unpatentable under § 102(e) as anticipated by Ohi. See Pet. 14–59. Patent Owner disputes Petitioner’s contentions. See Prelim. Resp. 20–61.

Below, we provide an overview of Ohi, and then we consider patentability arguments presented by the parties. As explained below, the

patentability challenge centers on whether Ohi discloses limitation 1(c)'s "pulse generation circuit" outputting a "first pulse signal" in an embodiment containing claim 1's other limitations. As also explained below, Petitioner does not establish sufficiently for purposes of institution that Ohi anticipates claims 1 and 2.

1. OVERVIEW OF OHI (EXHIBIT 1003)

Ohi is a U.S. patent titled "Drive Circuit for Driving Power Semiconductor Device," filed on July 28, 2003, and issued on June 14, 2005. Ex. 1003, codes (10), (22), (45), (54). Ohi states that the "invention relates to a drive circuit for driving a power semiconductor device and for detecting occurrence of an abnormality in the power semiconductor device," such as a short circuit in the power semiconductor device. *Id.* at 1:7–9; *see id.* at code (57). Ohi identifies an IGBT (Insulated Gate Bipolar Transistor) as an example of a power semiconductor device. *Id.* at 1:11–15.

Ohi describes problems with conventional drive circuits for IGBTs. *See* Ex. 1003, 2:12–31. For instance, "in a high-voltage IGBT, the collector-emitter voltage doesn't change to a steady-state value (i.e., a value acquired according to the static characteristics of the IGBT) instantaneously, but reaches the steady-state value at the expiration of a certain transition time interval after the IGBT has been turned on," e.g., reaching the steady-state value ten or more microseconds "after the IGBT has been turned on." *Id.* at 2:18–26. Further, "the above-mentioned transition time period needs to be masked" to "distinguish normal turning-on from a short circuit." *Id.* at 2:26–28.

Ohi purports to address those problems with various embodiments of drive circuits that include the following:

- (1) a “gate voltage detector” that detects “a gate-emitter voltage V_{ge} ” appearing between “the gate and emitter of a power semiconductor device throughout a detection time period”; and
- (2) a “sampler” that (i) allows “the process of detecting the gate-emitter voltage V_{ge} ” and (ii) recognizes “the occurrence of an abnormality in the power semiconductor device when the gate-emitter voltage V_{ge} exceeds a reference value” during the detection time period.

Ex. 1003, code (57); *see id.* at 2:42–52. Ohi identifies the various embodiments as embodiment 1 to embodiment 11. *See, e.g.*, 3:9–4:27, Fig. 1 (embodiment 1), Fig. 6 (embodiment 2), Fig. 8 (embodiment 3), Fig. 10 (embodiment 4), Fig. 12 (embodiment 5), Fig. 14 (embodiment 6), Fig. 15 (embodiment 7), Fig. 16 (embodiment 8), Fig. 19 (embodiment 9), Fig. 20 (embodiment 10), Fig. 23 (embodiment 11).

Ohi explains that the drive circuits “can protect the power semiconductor device with higher reliability by promptly detecting the occurrence of a short circuit even when the power semiconductor device is resistant to high voltages.” Ex. 1003, code 57; *see id.* at 2:34–41, 2:52–56, 2:66–3:2.

Ohi's Figure 6 (reproduced below) depicts embodiment 2 of a drive circuit for driving a power semiconductor device:

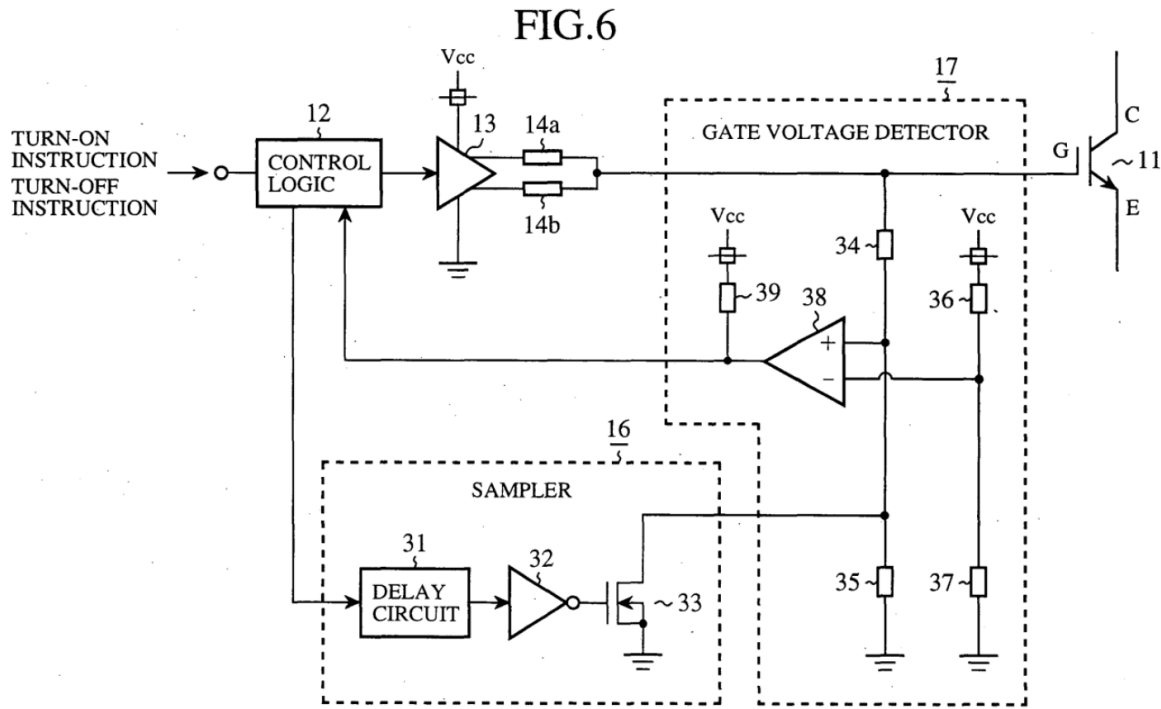


Figure 6 illustrates a drive circuit for IGBT 11 including control logic 12, buffer 13, on-state gate resistor 14a, off-state gate resistor 14b, sampler 16, and gate voltage detector 17. Ex. 1003, 3:29–31, 4:45–53, 8:54–62, Fig. 6.

As Figure 6 shows, embodiment 2's sampler 16 includes delay circuit 31, inverter 32, and Nch-MOSFET 33. Ex. 1003, 9:1–11, Fig. 6. At time t0, delay circuit 31 receives a turn-on gate instruction from control logic 12. *Id.* at 9:1–3, 9:45–51, Figs. 6–7. Delay circuit 31 holds the gate instruction until time t1 corresponding to the end of the detection time period. *Id.* at 9:3–4, 9:45–51, Figs. 6–7. At time t1, delay circuit 31 delivers the delayed gate instruction to inverter 32 by transitioning from a high level to a low level. *Id.* at 9:47–52, Figs. 6–7. When inverter 32 receives the delayed gate instruction from delay circuit 31, the inverter output (provided as the gate input to Nch-MOSFET 33) transitions from a low level to a high

level, thus turning on Nch-MOSFET 33 to prevent detection of the gate voltage V_g for IGBT 11. *Id.* at 9:6–12, 9:52–63, 10:3–4, Figs. 6–7.

As Figure 6 also shows, embodiment 2's gate voltage detector 17 includes the following:

- (1) a pair of resistors 34 and 35 for dividing the gate voltage V_g for IGBT 11;
- (2) a pair of resistors 36 and 37 for dividing the control voltage V_{cc} to generate a reference value;
- (3) comparator 38 receiving the divided gate voltage V_g at its + input and the divided control voltage V_{cc} (reference value) at its - input; and
- (4) resistor 39 connected between comparator 38's output and the control voltage V_{cc} .

Ex. 1003, 9:17–24, 9:41, 9:64–10:3, Fig. 6. “The dividing resistors 34 to 37 are so preset that when the gate voltage V_g reaches the control voltage V_{cc} , the divided voltage obtained thereby from the gate voltage V_g somewhat exceeds the reference value.” *Id.* at 9:24–27, 9:64–10:3.

If the divided gate voltage V_g exceeds the reference value during the detection time period, e.g., due to a short circuit, “comparator 38 delivers an abnormality signal to the control logic 12.” Ex. 1003, 10:14–19. Then, “the control logic 12 causes the IGBT 11 to become turned-off.” *Id.* at 10:19–21. But if the divided gate voltage V_g does not exceed the reference value during the detection time period, “comparator 38 sends out no abnormality signal even if the gate voltage V_g reaches the control voltage V_{cc} in level” at a later time. *Id.* at 10:3–12.

Ohi's Figure 10 (reproduced below) depicts embodiment 4 of a drive circuit for driving a power semiconductor device:

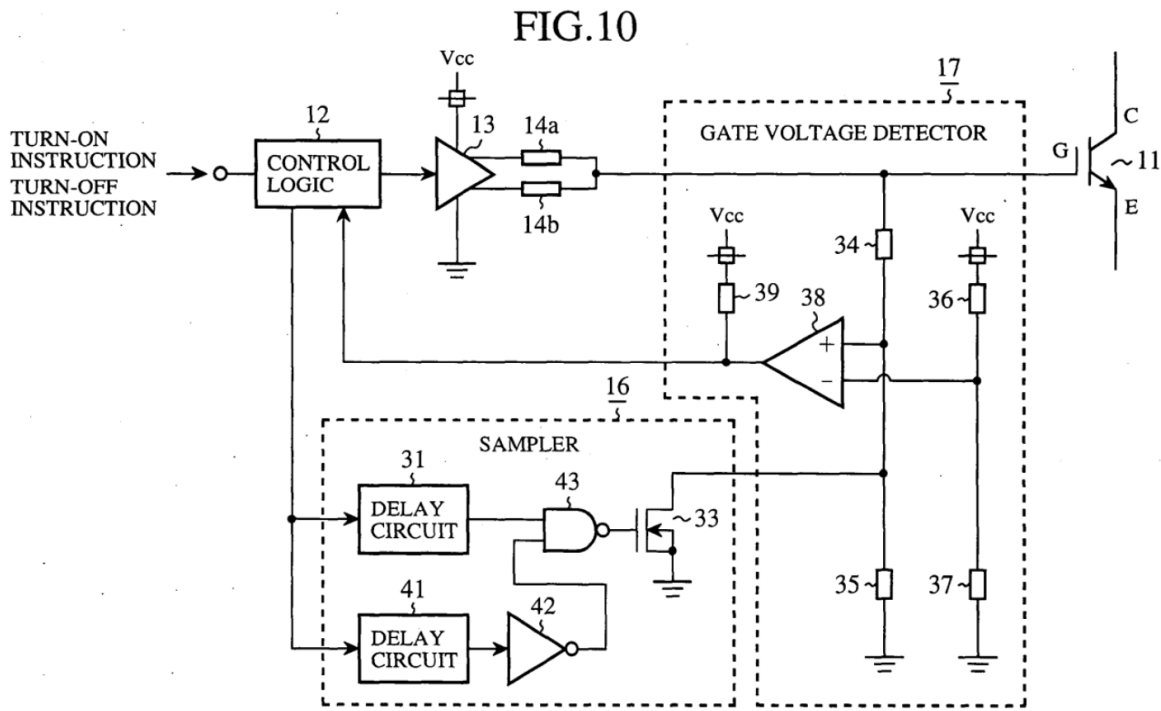


Figure 10 illustrates a drive circuit for IGBT 11 including control logic 12, buffer 13, on-state gate resistor 14a, off-state gate resistor 14b, sampler 16, and gate voltage detector 17. Ex. 1003, 3:44–46, 4:45–53, 8:54–62, Fig. 10. In Figures 6 and 10, the same reference numerals denote “the same components” or “like components.” *Id.* at 11:18–20.

As Figure 10 shows, embodiment 4's sampler 16 includes delay circuit 31, delay circuit 41, inverter 42, NAND circuit 43, and Nch-MOSFET 33. Ex. 1003, 11:21–30, Fig. 10. At time t_0 , delay circuit 31 and delay circuit 41 each receive a turn-on gate instruction from control logic 12. *Id.* at 11:41–47, 11:49–56, Figs. 10–11. Delay circuit 31 holds the gate instruction from time t_0 to time t_1 . *Id.* at 11:41–45, Fig. 11. Delay circuit 41 holds the gate instruction from time t_0 to time t_4 . *Id.* at 11:49–52, Fig. 11. Time t_1 extends beyond time t_4 such that time t_4 corresponds to the

start of the detection time period and time t1 corresponds to the end of the detection time period. *Id.* at 11:41–47, 11:49–56, 11:66–67, Fig. 11.

Specifically, at time t4 delay circuit 41 delivers the delayed gate instruction to inverter 42 by transitioning from a high level to a low level. Ex. 1003, 11:49–57, Figs. 10–11. Then, “inverter 42 inverts the logic of the gate instruction and furnishes it to” NAND circuit 43. *Id.* at 11:58–60, Fig. 11. When NAND circuit 43 receives the inverted gate instruction from inverter 42, the NAND circuit’s output (provided as the gate input to Nch-MOSFET 33) changes state, thus turning off Nch-MOSFET 33 to permit detection of the gate voltage Vg for IGBT 11. *Id.* at 11:60–65, Fig. 11.

Additionally, at time t1 delay circuit 31 delivers the delayed gate instruction to NAND circuit 43 by transitioning from a high level to a low level. Ex. 1003, 11:41–49, Figs. 10–11. When NAND circuit 43 receives the delayed gate instruction from delay circuit 31, the NAND circuit’s output (provided as the gate input to Nch-MOSFET 33) changes state, thus turning on Nch-MOSFET 33 to prevent detection of the gate voltage Vg for IGBT 11. *Id.* at 11:60–65, Fig. 11.

Consequently, “the Nch-MOSFET 33 is placed in an off state only during” the interval from time t4 to time t1 corresponding to the detection time period. Ex. 1003, 11:66–67, Fig. 11. In particular, the gate input to Nch-MOSFET 33 transitions from a high level to a low level at time t4 and transitions from a low level to a high level at time t1. *See id.* at 11:28–30, 11:41–65, Fig. 11.

As Figure 6 for embodiment 2 and Figure 10 for embodiment 4 show, embodiment 2’s gate voltage detector 17 and embodiment 4’s gate voltage

detector 17 include the same components connected in the same way. *See* Ex. 1003, 9:17–24, 9:41, 9:64–10:3, Figs. 6, 10.

Ohi describes the initial period from time t_0 to time t_4 as the “recovery time period.” Ex. 1003, 11:49–55. Ohi explains that “a voltage peak appears in the gate voltage V_g ” for IGBT 11 during the recovery time period due to “a current peak appear[ing] in the waveform of the collector current I_c ” for IGBT 11. *Id.* at 10:47–51. That transient voltage peak in the gate voltage V_g during the recovery time period may cause “a comparator 38 of a gate voltage detector 17” to use the peak voltage for comparison purposes and deliver “an abnormality signal under normal operating conditions.” *Id.* at 10:55–59. Ohi also explains that “masking changes” in the gate voltage V_g during the recovery time period may prevent improper operation. *Id.* at 10:59–62.

Ohi’s Figure 12 (reproduced below) depicts embodiment 5 of a drive circuit for driving a power semiconductor device:

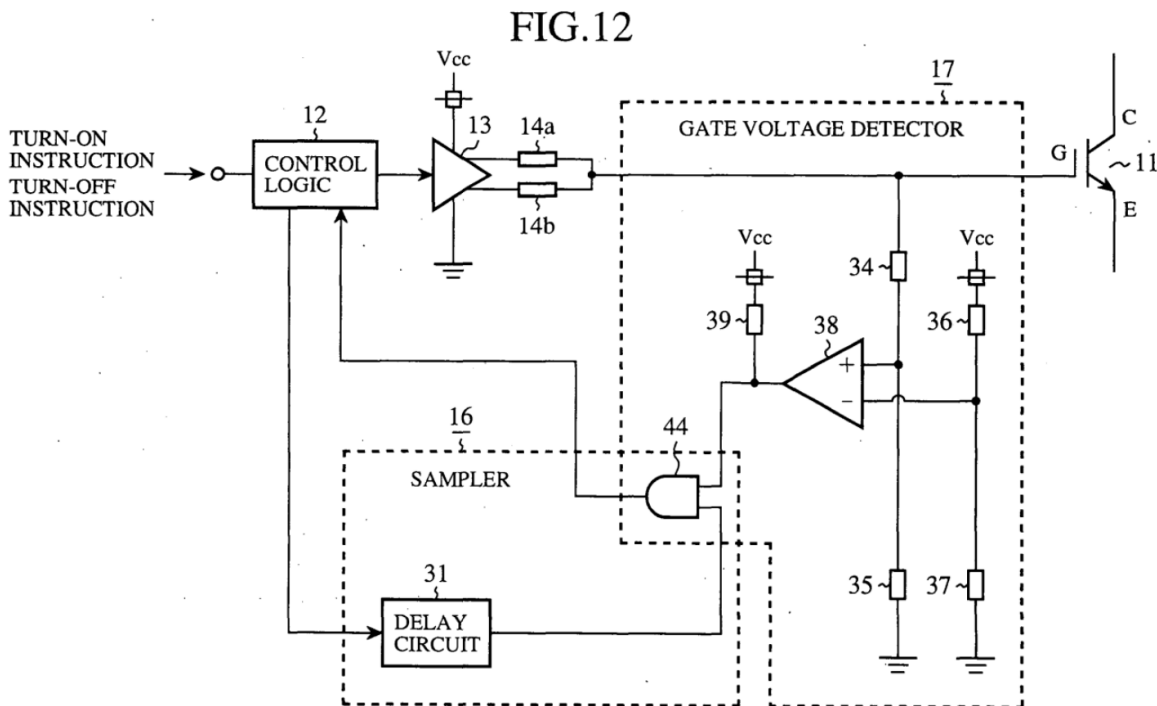


Figure 12 illustrates a drive circuit for IGBT 11 including control logic 12, buffer 13, on-state gate resistor 14a, off-state gate resistor 14b, sampler 16, and gate voltage detector 17. Ex. 1003, 3:52–54, 4:45–53, 8:54–62, 12:19–25, Fig. 12. In Figures 6, 10, and 12, the same reference numerals denote “the same components” or “like components.” *Id.* at 11:18–20, 12:22–24.

As Figure 12 shows, embodiment 5’s sampler 16 includes delay circuit 31 and AND circuit 44. Ex. 1003, 12:25–32, Fig. 12. At time t_0 , delay circuit 31 receives a turn-on gate instruction from control logic 12. *Id.* at 12:31–37, Figs. 12–13.³ Delay circuit 31 holds the gate instruction until time t_1 corresponding to the end of the detection time period. *Id.* at 12:31–37, Figs. 12–13; *see id.* at 9:45–51, Figs. 6–7. At time t_1 , delay circuit 31 delivers the delayed gate instruction to AND circuit 44 by transitioning from a high level to a low level. *Id.* at 12:31–37, 12:45–47, Figs. 12–13.

Like gate voltage detector 17 in embodiments 2 and 4, embodiment 5’s gate voltage detector 17 includes the following:

- (1) a pair of resistors 34 and 35 for dividing the gate voltage V_g for IGBT 11;
- (2) a pair of resistors 36 and 37 for dividing the control voltage V_{cc} to generate a reference value;
- (3) comparator 38 receiving the divided gate voltage V_g at its + input and the divided control voltage V_{cc} (reference value) at its - input; and

³ As an ordinarily skilled artisan would have recognized, Ohi’s Figure 13 includes the incorrect label “input of delay circuit 31” for the second-to-last graph instead of the correct label “output of delay circuit 31.” Ex. 1004 ¶ 51 n.3; Ex. 2008 ¶ 40.

- (4) resistor 39 connected between comparator 38's output and the control voltage V_{cc} .

Ex. 1003, 12:37–41, Fig. 12; *see id.* at 9:17–24, 9:41, 9:64–10:3. According to Figure 12, embodiment 5's gate voltage detector 17 also includes AND circuit 44 as a component shared with sampler 16. *Id.* at Fig. 12.

AND circuit 44 “receives the output signal of the comparator 38 and the output signal of the delay circuit 31 and then implements a logical AND operation on them.” Ex. 1003, 12:45–47, Fig. 12. During the detection time period, “the output signal of the delay circuit 31” has a high level, and “the output signal of the comparator 38” depends on the divided gate voltage V_g compared to the reference value. *See id.* at 12:37–44, 12:48–58, Fig. 13.

During normal operation, e.g., no short circuit, the output of AND circuit 44 remains at a low level during the detection time period because the divided gate voltage V_g does not exceed the reference value during the detection time period, thus causing “the output signal of the comparator 38” to remain at a low level during the detection time period. Ex. 1003, 12:37–44, 12:48–52, Fig. 13. But if “a short circuit occurs in the IGBT 11,” the divided gate voltage V_g exceeds the reference value during the detection time period, thus causing “the output signal of the comparator 38” to transition from a low level to a high level during the detection time period. *Id.* at 12:37–44, 12:52–58, Fig. 13. Because “the output signal of the delay circuit 31” also has a high level during the detection time period, AND circuit 44's output transitions from a low level to a high level, thus (1) delivering “an abnormality signal to the control logic 12” and (2) causing “the IGBT 11 to become turned-off.” *Id.* at 10:18–21, 12:59–65.

For embodiment 5, Ohi discloses that “[t]he detection time period during which the gate voltage V_g is detected can exclude a recovery time period immediately after the IGBT is turned on, like that of above-mentioned embodiment 4.” Ex. 1003, 12:66–13:2.

2. INDEPENDENT CLAIM 1

(a) Limitation 1(c): Pulse Generation Circuit

Claim 1 requires a “pulse generation circuit receiving said control input signal and outputting a first pulse signal being significant only in said predetermined period according to a timing when said control input signal indicates the conduction of said insulated gate transistor.” Ex. 1001, 11:50–54.

(i) Petitioner’s Position

Petitioner cites Ohi’s embodiment 5 as anticipating claim 1. *See* Pet. 23–52; Ex. 1004 ¶¶ 40–69. For limitation 1(c)’s “pulse generation circuit” outputting a “first pulse signal,” Petitioner asserts that embodiment 5’s sampler 16 includes “circuitry” outputting a signal to AND circuit 44 corresponding to limitation 1(e)’s “logical circuit.” Pet. 31 n.4, 31–32. In particular, Petitioner identifies delay circuit 31 in embodiment 5’s sampler 16 as performing the claimed functionality. *Id.* at 31 n.4; *see id.* at 41, 45–46. According to Petitioner, delay circuit 31:

- (1) “receives a turn-on instruction from control logic 12” as “a falling edge signal, i.e., a transition from high to low”; and
- (2) “outputs that falling edge signal after a predetermined amount of time has elapsed after the turn-on instruction is received, ensuring that its output remains significant only for that predetermined time after the IGBT is turned on.”

Id. at 33; *see id.* at 41–42, 45–46.

Petitioner asserts that Ohi's Figure 5 illustrates "an exemplary pulse generated by sampler 16 that is High (i.e., significant) only when the gate voltage is to be measured," i.e., only during the detection time period from time t_0 to time t_1 . Pet. 32. Specifically, Petitioner identifies a pulse in the "sampling" graph where the graph changes from a low level to a high level at time t_0 and changes from a high level to a low level at time t_1 , i.e., a pulse corresponding to the detection time period. *Id.* at 32–33.

Further, Petitioner quotes the following statement in Ohi: "The detection time period during which the gate voltage V_g is detected can exclude a recovery time period immediately after the IGBT is turned on, like that of above-mentioned embodiment 4." Pet. 38 (emphases omitted) (quoting Ex. 1003, 12:66–13:2). Based on the quoted statement, Petitioner asserts that Ohi expressly teaches using embodiment 4's sampler 16 as an alternative for embodiment 5. *Id.* at 36–38, 38 n.6.

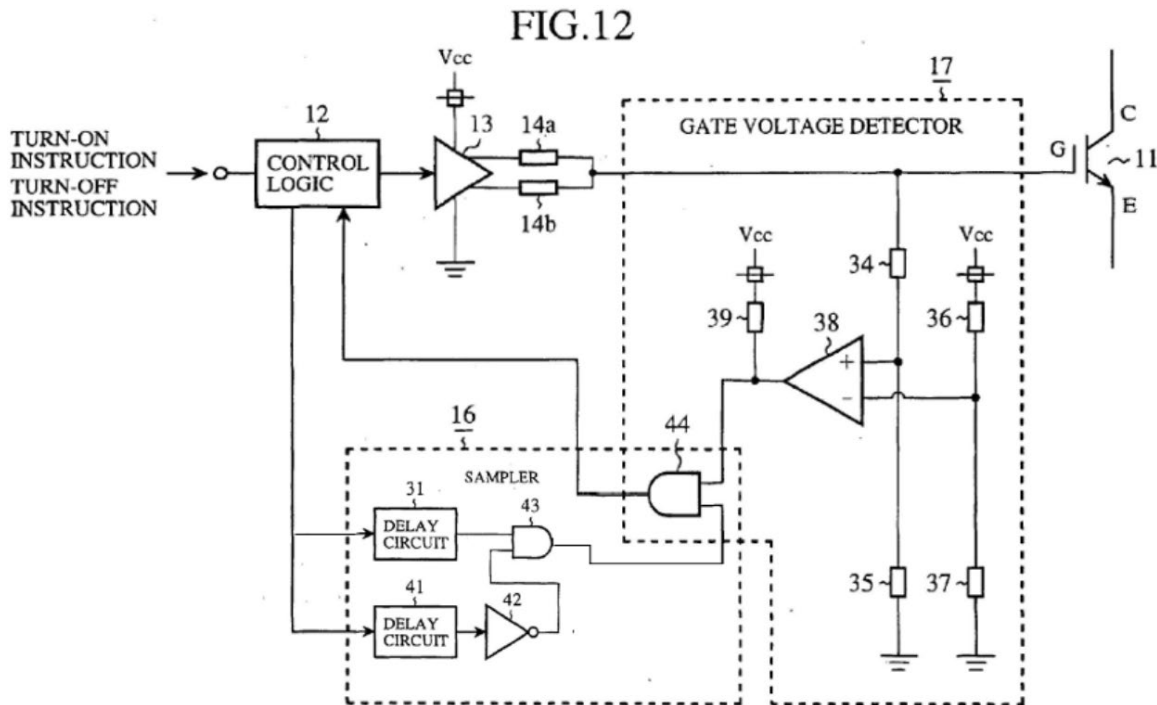
Petitioner asserts that embodiment 4's sampler 16 includes delay circuit 31, delay circuit 41, and inverter 42 arranged to define a "detection time period during which the gate voltage V_g is detected [that] excludes a certain time period (e.g., the time period from the time t_0 to the time t_4) immediately after the IGBT 11 is turned on." Pet. 36–37 (alteration by Petitioner) (quoting Ex. 1003, 11:36–40); *see id.* at 31 n.4. In particular, Petitioner contends that:

- (1) delay circuit 41 and inverter 42 define "the start of the detection time period by delaying (and inverting) the turn-on signal for a preset delay time t_0 to t_4 "; and
- (2) delay circuit 31 defines "the end of the detection time period" by delaying "the falling edge turn-on signal by the preset delay time t_0 to t_1 ."

Id. at 37.

Petitioner also asserts that an ordinarily skilled artisan “would have understood that incorporating” embodiment 4’s “recovery time exclusion” into embodiment 5 is a “straightforward replacement” of embodiment 5’s “single delay circuit” with embodiment 4’s “two delay circuit structure” that “defines both a start and end of the detection time period.” Pet. 38–39 (citing Ex. 1004 ¶¶ 52–56).

To support Petitioner’s assertions, Dr. Liu provides a modified version of Figure 12 for embodiment 5 as reproduced below (Ex. 1004 ¶ 55):



This modified version of Figure 12 illustrates a drive circuit for IGBT 11 including, among other components, sampler 16 and gate voltage detector 17. *See* Ex. 1003, 3:52–54, 4:45–53, 8:54–62, 12:19–25, Fig. 12; Ex. 1004 ¶ 55. This modified version of Figure 12 differs from Figure 12 by:

- (1) adding delay circuit 41, inverter 42, and AND circuit 43 to sampler 16 that already includes delay circuit 31;
- (2) connecting the output of delay circuit 31 as an input to AND circuit 43;
- (3) connecting the output of inverter 42 as another input to AND circuit 43; and
- (4) connecting the output of AND circuit 43 as an input to AND circuit 44.

See Pet. 40; Ex. 1003, Fig. 12; Ex. 1004 ¶ 55.

Dr. Liu testifies that embodiment 5 as modified above “produces a pulse that excludes recovery time from the detection time period and is the result of implementing Ohi’s express teaching that the fifth embodiment’s Fig. 12 circuit could exclude recovery time as expressly discussed in the fourth embodiment.” Ex. 1004 ¶ 56 (emphasis omitted).

Citing *Kennametal, Inc. v. Ingersoll Cutting Tool Co.*, 780 F.3d 1376 (Fed. Cir. 2015), and *Hayward Industries, Inc. v. Pentair Water Pool & Spa, Inc.*, 814 F. App’x 592 (Fed. Cir. 2020), Petitioner asserts that the “Federal Circuit has repeatedly held that anticipation” may rest on “teachings from different embodiments within a single reference, particularly where the reference contemplates combining teachings from separate embodiments.” Pet. 38 n.6.

(ii) Patent Owner’s Position

Patent Owner disputes that Ohi’s embodiment 5 anticipates claim 1 because, among other things, embodiment 5 lacks limitation 1(c)’s “pulse generation circuit” outputting a “first pulse signal.” See Prelim. Resp. 32–33, 59–61. Specifically, Patent Owner asserts that delay circuit 31 in embodiment 5’s sampler 16 outputs a single falling-edge signal instead of

a “first pulse signal” because “there is no predetermined period wherein the signal changes and then reverts.” *Id.* at 32–33, 61.

Regarding Ohi’s Figure 5, Patent Owner asserts that the “sampling” graph “is not even a signal—much less a pulse signal—and is merely an illustration to indicate when gate voltage detector 17 is sampling the gate.” Prelim. Resp. 31 n.6 (citing Ex. 2008 ¶ 33).

Patent Owner argues that anticipation may not properly rest on Dr. Liu’s modified embodiment 5 for several reasons. *See* Prelim. Resp. 33–41. First, Patent Owner asserts that Dr. Liu’s modified embodiment 5 does not employ the components in embodiment 4’s sampler 16 connected as in embodiment 4. *Id.* at 33. According to Patent Owner, Dr. Liu’s modified embodiment 5 differs from embodiment 4’s sampler 16 by:

- (1) replacing NAND circuit 43 with an AND circuit;
- (2) removing Nch-MOSFET 33; and
- (3) rerouting sampler 16’s output from comparator 38 to “a separate logic component.”

Id. at 33–35, 34 n.7.

Second, Patent Owner quotes the following statement in Ohi: “The detection time period during which the gate voltage V_g is detected can exclude a recovery time period immediately after the IGBT is turned on, like that of above-mentioned embodiment 4.” Prelim. Resp. 35 (quoting Ex. 1003, 12:66–13:2) (citing Pet. 38). Patent Owner then contends that the quoted statement does not instruct an ordinarily skilled artisan to “do anything remotely resembling replacing Ohi Figure 12’s single delay circuit

with Figure 10's two delay circuit approach" or "further modify" embodiment 4's sampler 16 in the way Dr. Liu proposes. *Id.*

Third, Patent Owner asserts that an ordinarily skilled artisan reviewing the quoted statement would have understood the statement "as suggesting possible additional functionality, not a specific structural change." Prelim. Resp. 35 (citing Ex. 2008 ¶¶ 42–49). Patent Owner also asserts that the quoted statement does not suggest that a "pulse generation circuit is even necessary" to implement additional functionality that excludes "a recovery time period immediately after the IGBT is turned on." *Id.* at 36. According to Patent Owner, Dr. Liu's modified embodiment 5 resulted from hindsight. *Id.* at 36–37, 40–41.

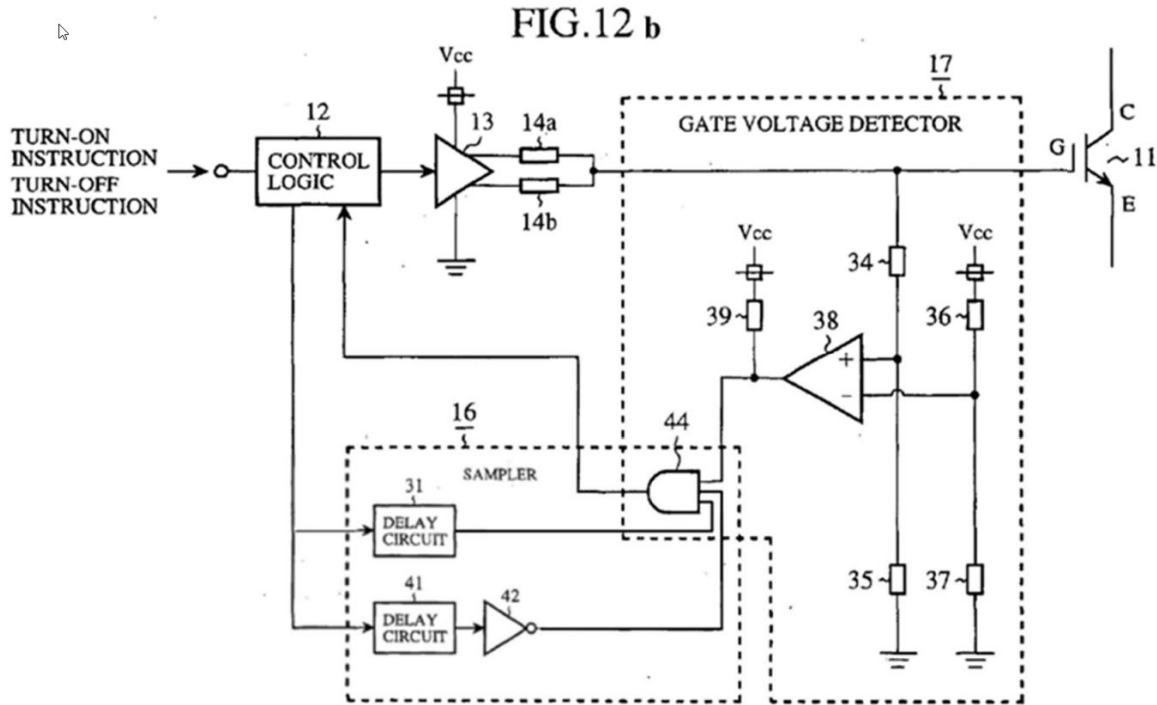
To support Patent Owner's assertions, Dr. Taylor testifies that an ordinarily skilled artisan would have understood Ohi "to suggest a functional goal potentially met by multiple designs," including "quite a few modifications" to Figure 12's circuitry that "delay the beginning of the detection time period using a delay circuit 41 and an inverter 42." Ex. 2008 ¶¶ 44, 49.

Fourth, Patent Owner asserts that an ordinarily skilled artisan reviewing the quoted statement and "looking to make such a change would be more likely to implement something" other than Dr. Liu's modified embodiment 5 to achieve "a simpler, smaller, faster, lower power, and lower cost" drive circuit. Prelim. Resp. 36–37; *see id.* at 37–41. To support Patent Owner's assertion, Dr. Taylor provides four example modifications to Figure 12's circuitry that (1) exclude "a recovery time period immediately after the IGBT is turned on" and (2) do not employ a "pulse generation

circuit” outputting a “first pulse signal” as required by limitation 1(c).

Ex. 2008 ¶¶ 46–48; *see* Prelim. Resp. 36–40.

As presented by Patent Owner, Dr. Taylor’s first modification to Ohi Figure 12’s circuitry is reproduced below and labeled by Dr. Taylor as Figure 12b (Prelim. Resp. 37; Ex. 2008 ¶ 46):

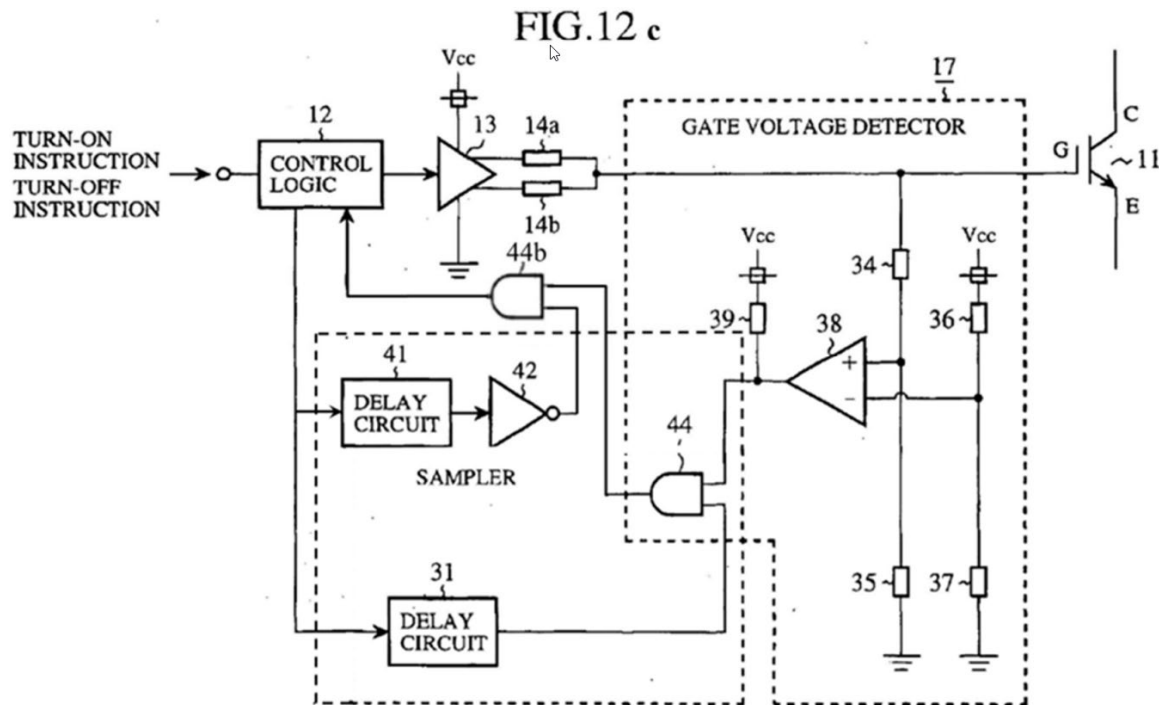


Dr. Taylor’s Figure 12b illustrates a drive circuit for IGBT 11 including, among other components, sampler 16 and gate voltage detector 17. *See* Ex. 1003, 3:52–54, 4:45–53, 8:54–62, 12:19–25, Fig. 12; Ex. 2008 ¶ 46. Figure 12b differs from Ohi’s Figure 12 by (1) adding delay circuit 41 and inverter 42 to sampler 16 that already includes delay circuit 31 and (2) changing AND circuit 44 from a two-input device to a three-input device that receives inputs from delay circuit 31, comparator 38, and inverter 42. *See* Prelim. Resp. 37; Ex. 1003, Fig. 12; Ex. 2008 ¶ 46.

Dr. Taylor testifies that an ordinarily skilled artisan would have recognized that using a single three-input AND circuit as in Figure 12b

“would be smaller, faster, lower power, and lower cost” than using a pair of two-input AND circuits in series as in Dr. Liu’s modified embodiment 5, i.e., AND circuit 43 and AND circuit 44 in Dr. Liu’s modified embodiment 5. Ex. 2008 ¶ 46; *see* Ex. 1004 ¶ 55. Dr. Taylor describes Dr. Liu’s modified embodiment 5 as “less desirable” than Figure 12b’s drive circuit. Ex. 2008 ¶ 46.

As presented by Patent Owner, Dr. Taylor's second modification to Ohi Figure 12's circuitry is reproduced below and labeled by Dr. Taylor as Figure 12c (Prelim. Resp. 40; Ex. 2008 ¶ 47):

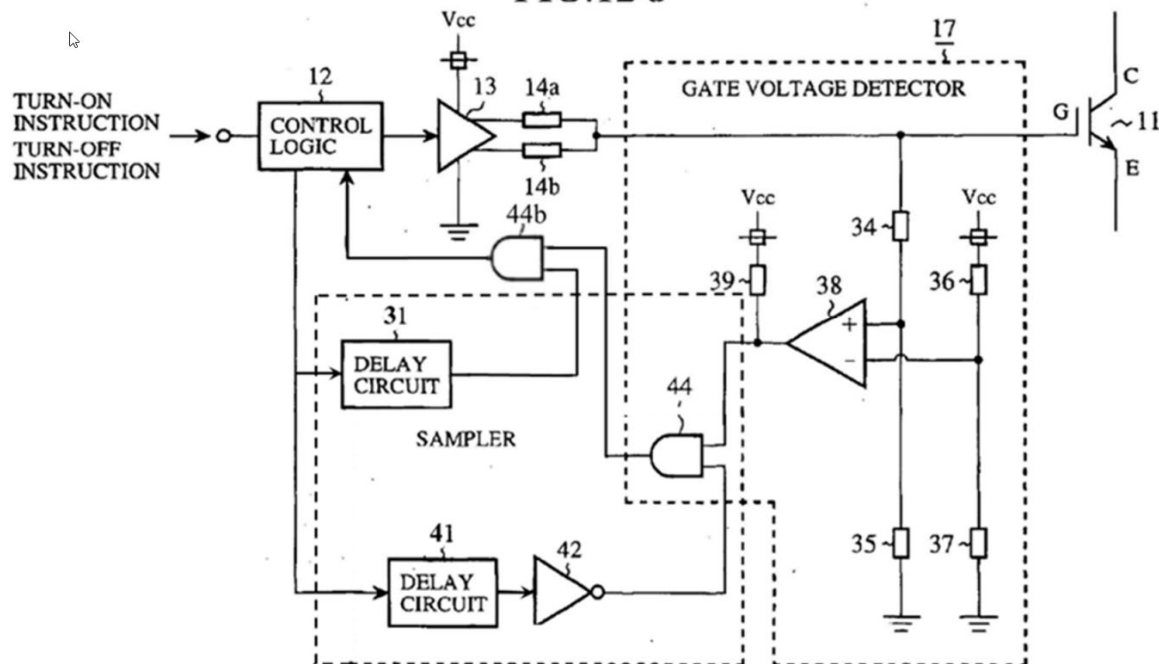


Dr. Taylor's Figure 12c illustrates a drive circuit for IGBT 11 including, among other components, sampler 16 and gate voltage detector 17. *See* Ex. 1003, 3:52–54, 4:45–53, 8:54–62, 12:19–25, Fig. 12; Ex. 2008 ¶ 47. Figure 12c differs from Ohi's Figure 12 by (1) adding delay circuit 41 and inverter 42 to sampler 16 that already includes delay circuit 31, (2) adding two-input AND circuit 44b, (3) providing the output of AND circuit 44 as an

input to AND circuit 44b, and (4) providing the output of inverter 42 as another input to AND circuit 44b. *See* Prelim. Resp. 40; Ex. 1003, Fig. 12; Ex. 2008 ¶ 47.

As presented by Patent Owner, Dr. Taylor's third modification to Ohl Figure 12's circuitry is reproduced below and labeled by Dr. Taylor as Figure 12d (Prelim. Resp. 40; Ex. 2008 ¶ 47):

FIG.12 d



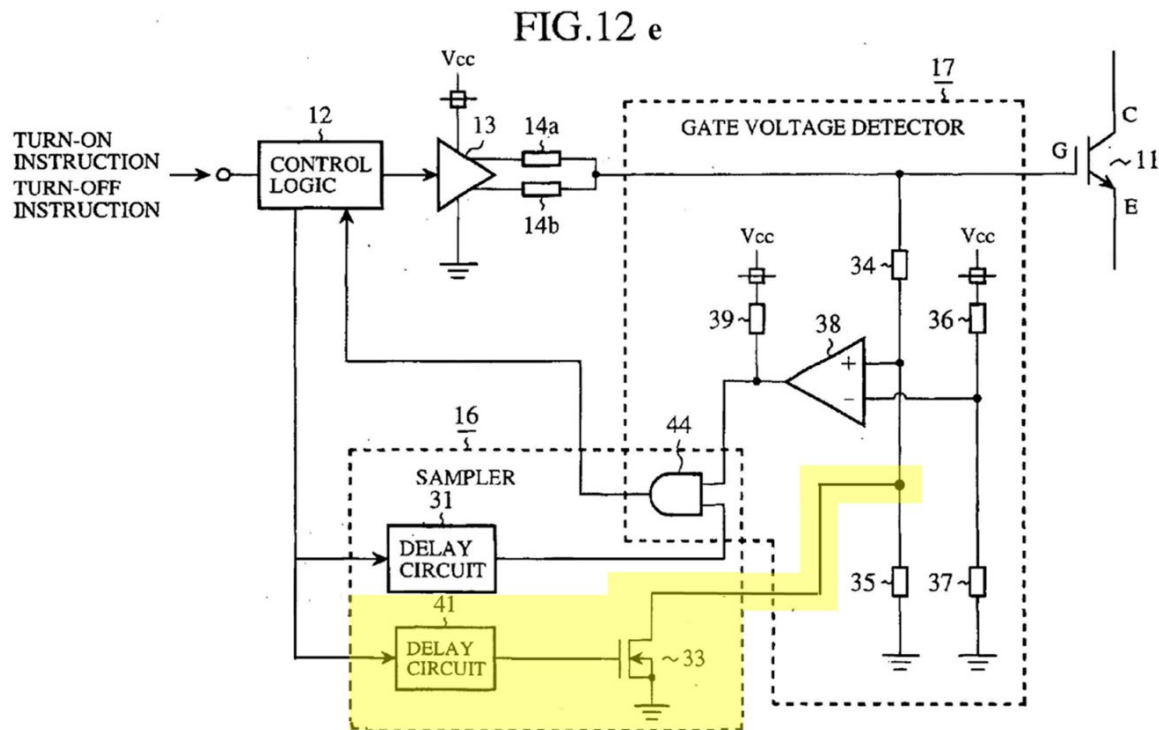
Dr. Taylor's Figure 12d illustrates a drive circuit for IGBT 11 including, among other components, sampler 16 and gate voltage detector 17. *See* Ex. 1003, 3:52–54, 4:45–53, 8:54–62, 12:19–25, Fig. 12; Ex. 2008 ¶ 47.

Figure 12d differs from Ohi's Figure 12 by (1) adding delay circuit 41 and inverter 42 to sampler 16 that already includes delay circuit 31, (2) providing the output of inverter 42 as an input to AND circuit 44, (3) adding two-input AND circuit 44b, (4) providing the output of AND circuit 44 as an input to AND circuit 44b, and (5) providing the output of delay circuit 31 as another

input to AND circuit 44b. *See* Prelim. Resp. 40; Ex. 1003, Fig. 12; Ex. 2008 ¶ 47.

Dr. Taylor testifies that an ordinarily skilled artisan could implement Figure 12c's drive circuit or Figure 12d's drive circuit if "there is some reason to prefer" a pair of two-input AND circuits in series. Ex. 2008 ¶ 47.

As presented by Patent Owner, Dr. Taylor's fourth modification to Ohi Figure 12's circuitry is reproduced below and labeled by Dr. Taylor as Figure 12e (Prelim. Resp. 38; Ex. 2008 ¶ 48):



Dr. Taylor's Figure 12e illustrates a drive circuit for IGBT 11 including, among other components, sampler 16 and gate voltage detector 17. *See* Ex. 1003, 3:52–54, 4:45–53, 8:54–62, 12:19–25, Fig. 12; Ex. 2008 ¶ 48. Figure 12e differs from Ohi's Figure 12 by (1) adding Nch-MOSFET 33 and delay circuit 41 to sampler 16 that already includes delay circuit 31 and (2) connecting Nch-MOSFET 33 to comparator 38's + input that receives the divided gate voltage V_g . *See* Prelim. Resp. 38; Ex. 1003, Fig. 12;

Ex. 2008 ¶ 48. Yellow highlighting in Figure 12e denotes these differences.
Ex. 2008 ¶ 44.

Dr. Taylor testifies that Figure 12e's drive circuit "requires the fewest added components of the five implementations." Ex. 2008 ¶ 48. He explains that Ohi's embodiment 4 has Nch-MOSFET 33 connected to comparator 38's + input as in Figure 12e's drive circuit. *Id.* He also explains that connecting Nch-MOSFET 33 to comparator 38's + input as in Figure 12e's drive circuit would retain embodiment 4's "capacitive benefit" as follows:

An engineer knows that all components have parasitic capacitances and worries about the impact of adding this capacitance to critical signals. But Ohi teaches that adding extra capacitance to the positive input of the comparator both reduces sensitivity to the initial peak in the gate waveform and makes the Miller plateau broader, both easing the precision required of delay circuits 31 and 41. Given this information [an ordinarily skilled artisan] would have recognized that the extra capacitance of MOSFET 33 on this node is beneficial.

Id. (internal citation omitted); *see id.* ¶ 49.

Further, Patent Owner asserts that Dr. Liu's modified embodiment 5 fails to anticipate claim 1 because the purported "pulse generation circuit" does not receive the "control input signal" as required by limitation 1(c). *See* Prelim. Resp. 41–47. In particular, Patent Owner contends that Petitioner maps (1) claim 1's "control input signal" to Ohi's "turn-on and turn-off instructions" and (2) claim 1's "control output signal" to Ohi's "gate instruction." *Id.* at 42 (citing Pet. 23). Patent Owner also contends that sampler 16 in Dr. Liu's modified embodiment 5 receives the "gate instruction" (Petitioner's "control output signal") instead of the "turn-on and

turn-off instructions” (Petitioner’s “control input signal”). *Id.* at 44–45 (emphases omitted).

(iii) Analysis

Based on the current record, Petitioner does not establish sufficiently for purposes of institution that Ohi discloses limitation 1(c)’s “pulse generation circuit” outputting a “first pulse signal” in an embodiment containing claim 1’s other limitations. *See* Pet. 23–52; Ex. 1004 ¶¶ 40–69; Ex. 2008 ¶¶ 39–50. As noted above, Petitioner cites Ohi’s embodiment 5 as anticipating claim 1. *See* Pet. 23–52; Ex. 1004 ¶¶ 40–69; *supra* § IV.D.2(a)(i). Embodiment 5 lacks limitation 1(c)’s “pulse generation circuit” outputting a “first pulse signal.” *See* Ex. 1003, 12:21–65, Fig. 12; Ex. 2008 ¶ 40.

In particular, embodiment 5’s sampler 16 includes delay circuit 31 and AND circuit 44. Ex. 1003, 12:25–32, Fig. 12; *see* Ex. 2008 ¶¶ 40, 50. At time t₀, delay circuit 31 receives a turn-on gate instruction from control logic 12. Ex. 1003, 12:31–37, Figs. 12–13; *see* Ex. 2008 ¶ 40. Delay circuit 31 holds the gate instruction until time t₁ corresponding to the end of the detection time period. Ex. 1003, 12:31–37, Figs. 12–13; *see id.* at 9:45–51, Figs. 6–7; Ex. 2008 ¶ 40. At time t₁, delay circuit 31 delivers the delayed gate instruction to AND circuit 44 by transitioning from a high level to a low level. Ex. 1003, 12:31–37, 12:45–47, Figs. 12–13; *see* Ex. 2008 ¶ 40. The single falling-edge signal resulting from that transition does not correspond to a pulse signal because that single falling-edge signal does not revert to its original value in a comparatively short time. *See* Ex. 1003, 12:31–37, Fig. 13; Ex. 2008 ¶¶ 40–41, 50–51; Ex. 2010, 5; *see also* Ex. 2009, 3.

Regarding Petitioner's reliance on Ohi's Figure 5, that figure relates to embodiment 1, not embodiment 5. Ex. 1003, 3:25–28; *see id.* at 6:66–8:52, Fig. 5; Pet. 32–33. Additionally, the “sampling” graph in Figure 5 conceptually depicts the detection time period from time t_0 to time t_1 when sampler 16 enables voltage gate detector 17 to detect the gate voltage V_g for IGBT 11. Ex. 1003, 7:29–51, Fig. 5; *see* Ex. 2008 ¶ 33. The “sampling” graph does not depict a specific signal in the drive circuit as a function of time. Ex. 1003, 7:29–51, Fig. 5; *see* Ex. 2008 ¶ 33. As Dr. Taylor testifies, the “sampling” graph “does not correspond to any individual signal” and “is only included to make the operation of the circuit clear.” Ex. 2008 ¶ 33.

Regarding Ohi's statement linking embodiment 4 and embodiment 5, Ohi explains as follows: “The detection time period during which the gate voltage V_g is detected can exclude a recovery time period immediately after the IGBT is turned on, like that of above-mentioned embodiment 4.” Ex. 1003, 12:66–13:2; *see* Pet. 38 (quoting Ex. 1003, 12:66–13:2); Prelim. Resp. 35 (quoting Ex. 1003, 12:66–13:2). Embodiment 4 excludes “a recovery time period immediately after the IGBT is turned on” due to:

- (1) the component arrangement in sampler 16, e.g., using two delay circuits and Nch-MOSFET 33;
- (2) sampler 16's connection to gate voltage detector 17, i.e., with Nch-MOSFET 33 connected to comparator 38's + input that receives the divided gate voltage V_g ; and
- (3) gate voltage detector 17's connection to control logic 12, i.e., with comparator 38's output connected to control logic 12.

See Ex. 1003, 11:21–12:8, Figs. 10–11; Ex. 1004 ¶¶ 52–53; Ex. 2008 ¶ 38.

To produce a functional drive circuit, embodiment 4's sampler 16 cannot simply replace embodiment 5's sampler 16 in embodiment 5. *See* Ex. 2008 ¶ 43. For instance, the output of embodiment 4's sampler 16 connects to comparator 38's + input that receives the divided gate voltage V_g to enable or disable comparator 38, and comparator 38's output connects to control logic 12. Ex. 1003, 10:3–13, 11:21–30, 11:36–40, 11:60–67, Fig. 10; Ex. 2008 ¶ 38. In contrast, the output of embodiment 5's sampler 16, i.e., the output of AND circuit 44, connects to control logic 12, and comparator 38's output connects to AND circuit 44. Ex. 1003, 12:25–28, 12:45–58, Fig. 12; Ex. 2008 ¶¶ 40–41.

Further, Petitioner does not assert that embodiment 4's sampler 16 can simply replace embodiment 5's sampler 16 in embodiment 5. *See* Pet. 36–40; Ex. 1004 ¶¶ 52 n.4, 54–56. Rather, Petitioner argues that Dr. Liu's modified embodiment 5 results from a “straightforward replacement” of embodiment 5's “single delay circuit” with embodiment 4's “two delay circuit structure” that “defines both a start and end of the detection time period.” Pet. 38–40 (citing Ex. 1004 ¶¶ 52–56).

We agree with Patent Owner that anticipation may not properly rest on Dr. Liu's modified embodiment 5. *See* Prelim. Resp. 33–41; Ex. 2008 ¶¶ 39, 42–49. Ohi's statement linking embodiment 4 and embodiment 5 describes desired functionality, i.e., excluding “a recovery time period immediately after the IGBT is turned on.” Ex. 1003, 12:66–13:2; Ex. 2008 ¶¶ 43, 49. That statement does not disclose a specific circuit for achieving that desired functionality. Ex. 1003, 12:66–13:2; *see* Ex. 2008 ¶¶ 42–44, 49.

We credit Dr. Taylor's testimony that an ordinarily skilled artisan would have understood Ohi “to suggest a functional goal potentially met by

multiple designs,” including “quite a few modifications” to Figure 12’s circuitry that “delay the beginning of the detection time period using a delay circuit 41 and an inverter 42.” Ex. 2008 ¶¶ 44, 49; *see* Prelim. Resp. 35. And Dr. Taylor provides four example modifications to Figure 12’s circuitry that (1) exclude “a recovery time period immediately after the IGBT is turned on” and (2) do not employ a “pulse generation circuit” outputting a “first pulse signal” as required by limitation 1(c). Ex. 2008 ¶¶ 46–48; *see* Prelim. Resp. 36–40.

Taking Dr. Taylor’s first modification to Figure 12’s circuitry (Figure 12b) as an example, an ordinarily skilled artisan would have recognized that using a single three-input AND circuit as in Figure 12b’s drive circuit “would be smaller, faster, lower power, and lower cost” than using a pair of two-input AND circuits in series as in Dr. Liu’s modified embodiment 5, i.e., AND circuit 43 and AND circuit 44 in Dr. Liu’s modified embodiment 5. Ex. 2008 ¶ 46; *see* Ex. 1004 ¶ 55.

Taking Dr. Taylor’s fourth modification to Figure 12’s circuitry (Figure 12e) as another example, an ordinarily skilled artisan would have recognized that connecting Nch-MOSFET 33 to comparator 38’s + input as in Figure 12e’s drive circuit would retain embodiment 4’s “capacitive benefit” that Dr. Liu’s modified embodiment 5 lacks. Ex. 2008 ¶¶ 48–49; *see* Ex. 1003, 10:63–11:2, 12:15–17, Figs. 8–9.

Based on the current record, an ordinarily skilled artisan would not have reasonably understood or inferred that Ohi discloses an embodiment with all of claim 1’s limitations arranged as in the claim. *See* Prelim. Resp. 23–52; Ex. 1004 ¶¶ 40–69; Ex. 2008 ¶¶ 39–50. The facts here parallel the facts in *Net MoneyIN*.

There, the claim at issue recited a payment system comprising five links. *Net MoneyIN*, 545 F.3d at 1368–69. The district court found that the iKP reference disclosed all five links in two separate payment protocols and that the iKP reference anticipated the claim at issue. *Id.* at 1369, 1371. The district court reasoned that a “simple combination” would produce the claimed payment system. *Id.* at 1369.

The Federal Circuit reversed the district court’s anticipation determination. *Net MoneyIN*, 545 F.3d at 1362, 1371. The Federal Circuit explained that the district court was “wrong to combine parts of the separate protocols shown in the iKP reference” because “differences between the prior art reference and a claimed invention, however slight, invoke the question of obviousness, not anticipation.” *Id.* at 1371.

Here, as in *Net MoneyIN*, Petitioner attempts to demonstrate anticipation by combining parts of separate embodiments in Ohi, i.e., by combining some components in embodiment 4’s sampler 16 with embodiment 5. *See* Pet. 23–52; Ex. 1004 ¶¶ 40–69.

As noted above, Petitioner cites *Kennametal* and *Hayward* to support the assertion that the “Federal Circuit has repeatedly held that anticipation” may rest on “teachings from different embodiments within a single reference, particularly where the reference contemplates combining teachings from separate embodiments.” *See* Pet. 38 n.6; *supra* § IV.D.2(a)(i). But the facts in *Kennametal* and *Hayward* differ materially from the facts here.

In *Kennametal*, the claim at issue recited a cutting tool comprising (1) a carbide-based substrate containing ruthenium as a binder and (2) a coating applied by physical vapor deposition. *Kennametal*, 780 F.3d

at 1378–79. The Grab reference disclosed a cutting tool comprising, among other things, (1) a carbide-based substrate containing “one or more of tungsten, iron, nickel, ruthenium, and rhenium” as a binder and (2) a coating applied by chemical vapor deposition, moderate-temperature chemical vapor deposition, or physical vapor deposition. *Id.* at 1379–80, 1382. The Board found that the “combination of one of five metals with one of three coatings leads to only fifteen possibilities” and that Grab anticipates each member of that “limited class,” including the claim at issue. *Id.* at 1380.

The Federal Circuit affirmed the Board because substantial evidence supported the Board’s determination that Grab “effectively teaches” fifteen combinations and one of the fifteen combinations anticipated the claim at issue. *Kennametal*, 780 F.3d at 1382–83. In doing so, the Federal Circuit noted that “a reference can anticipate a claim even if it ‘d[oes] not expressly spell out’ all the limitations arranged or combined as in the claim, if a person of skill in the art, reading the reference, would ‘at once envisage’ the claimed arrangement or combination.” *Id.* at 1381 (alteration in original) (quoting *In re Petering*, 301 F.2d 676, 681 (CCPA 1962)).

Here, in contrast to *Kennametal*, a person of skill in the art, reading Ohi, would not “at once envisage” claim 1’s arrangement or combination because a person of skill would have understood Ohi “to suggest a functional goal potentially met by multiple designs,” including “quite a few modifications” to Figure 12’s circuitry that “delay the beginning of the detection time period using a delay circuit 41 and an inverter 42.” *See* Ex. 2008 ¶¶ 44, 49.

In *Hayward*, the claim at issue recited a pumping system comprising, among other things, (1) a pump, (2) a motor, and (3) a pump controller

“operating the motor to substantially optimize energy consumption based on” certain information. *Hayward*, 814 F. App’x at 594. The Board determined that the Discenzo reference “did not teach the ‘optimize energy consumption’ limitation because it found that Discenzo was primarily focused on optimization of an overall system rather than optimization of a pump component.” *Id.* at 595; *see id.* at 596.

The Federal Circuit disagreed with the Board because the Board disregarded “specific disclosures in Discenzo that teach not only system optimization, but also component optimization.” *Hayward*, 814 F. App’x at 596–97. The Federal Circuit explained that an anticipatory reference “does not need to include an ‘express discussion of the actual combination to anticipate,’ but may instead teach that the disclosed elements may be combined such that one of skill in the art could implement the combination.” *Id.* at 597 (quoting *Blue Calypso, LLC v. Groupon, Inc.*, 815 F.3d 1331, 1344 (Fed. Cir. 2016)). The Federal Circuit reasoned that “[a]lthough Discenzo teaches optimization and the arrangement of components in different embodiments of the patent, Discenzo also explains that these features may be combined.” *Id.*

Here, in contrast to *Hayward*, Ohi does not disclose that some components in embodiment 4’s sampler 16 may be combined with embodiment 5 in the way Dr. Liu proposes. *See* Ex. 1003, 12:66–13:2; Ex. 1004 ¶ 55; Ex. 2008 ¶¶ 39, 42–49. Ohi’s statement linking embodiment 4 and embodiment 5 does not disclose a specific circuit for excluding “a recovery time period immediately after the IGBT is turned on.” Ex. 1003, 12:66–13:2; *see* Ex. 2008 ¶¶ 39, 42–44, 49. Instead, that statement describes desired functionality that an ordinarily skilled artisan

may implement in many ways. Ex. 1003, 12:66–13:2; Ex. 2008 ¶¶ 43–49. “[D]ifferences between the prior art reference and a claimed invention, however slight, invoke the question of obviousness, not anticipation.” *Net MoneyIN*, 545 F.3d at 1371.

(b) Conclusion Concerning Claim 1

Because Petitioner does not establish sufficiently for purposes of institution that Ohi discloses limitation 1(c)’s “pulse generation circuit” outputting a “first pulse signal” in an embodiment containing claim 1’s other limitations, Petitioner does not establish sufficiently for purposes of institution that Ohi anticipates claim 1. *See* Pet. 23–52; Ex. 1004 ¶¶ 40–69; Ex. 2008 ¶¶ 39–50; *supra* § IV.D.2(a)(iii). Hence, Petitioner does not demonstrate a reasonable likelihood of prevailing in proving claim 1 unpatentable under § 102(e) as anticipated by Ohi.

3. DEPENDENT CLAIM 2

Claim 2 depends directly from claim 1. Ex. 1001, 11:66–12:4. Hence, claim 2 incorporates all of claim 1’s limitations. *See* 35 U.S.C. § 112 ¶ 4 (2006).

Because Petitioner does not establish sufficiently for purposes of institution that Ohi anticipates claim 1, Petitioner does not establish sufficiently for purposes of institution that Ohi anticipates claim 2. *See supra* § IV.D.2(a)(iii).

V. CONCLUSION

After considering the Petition, the Preliminary Response, and the evidence of record, and for the reasons discussed above, we determine that Petitioner has not demonstrated a reasonable likelihood that it would prevail

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in proving the unpatentability of at least one claim challenged in the Petition.
Hence, we deny the Petition and do not institute an *inter partes* review.

VI. ORDER

Accordingly, it is

ORDERED that the Petition is denied and no trial is instituted.

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