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Paper: 20
Entered: October 19, 2022

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.,
Petitioner,

v.

NETLIST, INC.,
Patent Owner.

IPR2022-00615
Patent 7,619,912 B2

Before JON M. JURGOVAN, DANIEL R. GALLIGAN, and NABEEL U. KHAN, *Administrative Patent Judges.*

JURGOVAN, *Administrative Patent Judge*.

DECISION
Granting Institution of *Inter Partes* Review
35 U.S.C. § 314

I. INTRODUCTION

Samsung Electronics Co., Ltd. ("Petitioner") filed a Petition requesting *inter partes* review of claim 16 of U.S. Patent No. 7,619,912 [1] (Ex. 1001, "the '912 patent"). Paper 1 ("Pet."), 4. Netlist, Inc. ("Patent Owner") filed a Preliminary Response. Paper 7 ("Prelim. Resp."). Petitioner filed an authorized Preliminary Reply (Paper 14), and Patent Owner filed an authorized Preliminary Sur-Reply (Paper 15).

We have jurisdiction and authority to institute trial pursuant to 35 U.S.C. §§ 6 and 314(a), and 37 C.F.R. § 42.4(a). Upon consideration of the Petition, Preliminary Response, Reply, and Sur-Reply, we exercise our discretion to institute *inter partes* review under § 314(a).

II. BACKGROUND

A. Real Parties-in-Interest

Petitioner identifies itself and Samsung Semiconductor, Inc. as the real parties-in-interest involved in this case. Pet. 1. Patent Owner identifies itself as the real party-in-interest in this case. Paper 4, 1.

B. Related Matters

Petitioner and Patent Owner identify the following as matters that can affect or be affected by this proceeding. *See* Pet. 1–2; Paper 4, 1.

- *Netlist, Inc. v. Google LLC*, 4:09-cv-05718 (N.D. Cal. Dec. 4, 2009)
- *Samsung Electronics Co., Ltd. et al. v. Netlist, Inc.*, 1:21-cv-01453 (D. Del. Oct. 15, 2021)

[1] Challenged claim 16 was amended as part of an *inter partes* reexamination, as set forth in the reexamination certification (appended at the end of Ex. 1001).

- *Netlist, Inc. v. Inphi Corp.*, No. 2:09-cv-06900 (C.D. Cal. Sept. 22, 2009) (terminated)
- U.S. Application No. 17/403,832
- *Inter partes* Reexamination Nos. 95/000,578, 95/000,579, and 95/001,339 of the '912 patent (concluded)
- *Inter partes* Reexamination Nos. 95/000,546 and 95/000,577 of U.S. Patent No. 7,289,386 (concluded)
- *Inter partes* Reexamination No. 95/001,337 of U.S. Patent No. 7,636,274 (concluded)
- IPR2014-00882 of U.S. Patent No. 7,881,150 (concluded)
- IPR2014-00883 of U.S. Patent No. 8,081,536 (concluded)
- IPR2015-01021 of U.S. Patent No. 8,081,536 (concluded)
- IPR2017-00549 of U.S. Patent No. 8,756,364 (concluded)
- IPR2017-00667 of U.S. Patent No. 7,532,537 (concluded)
- IPR2017-00668 of U.S. Patent No. 7,532,537 (concluded)

C. Overview of the '912 Patent

The '912 patent is titled "Memory Module Decoder" and is directed to a memory module that is connectable to a computer system. Ex. 1001, codes (54), (57). Figure 1A of the '912 patent is reproduced below.

Figure 1A:

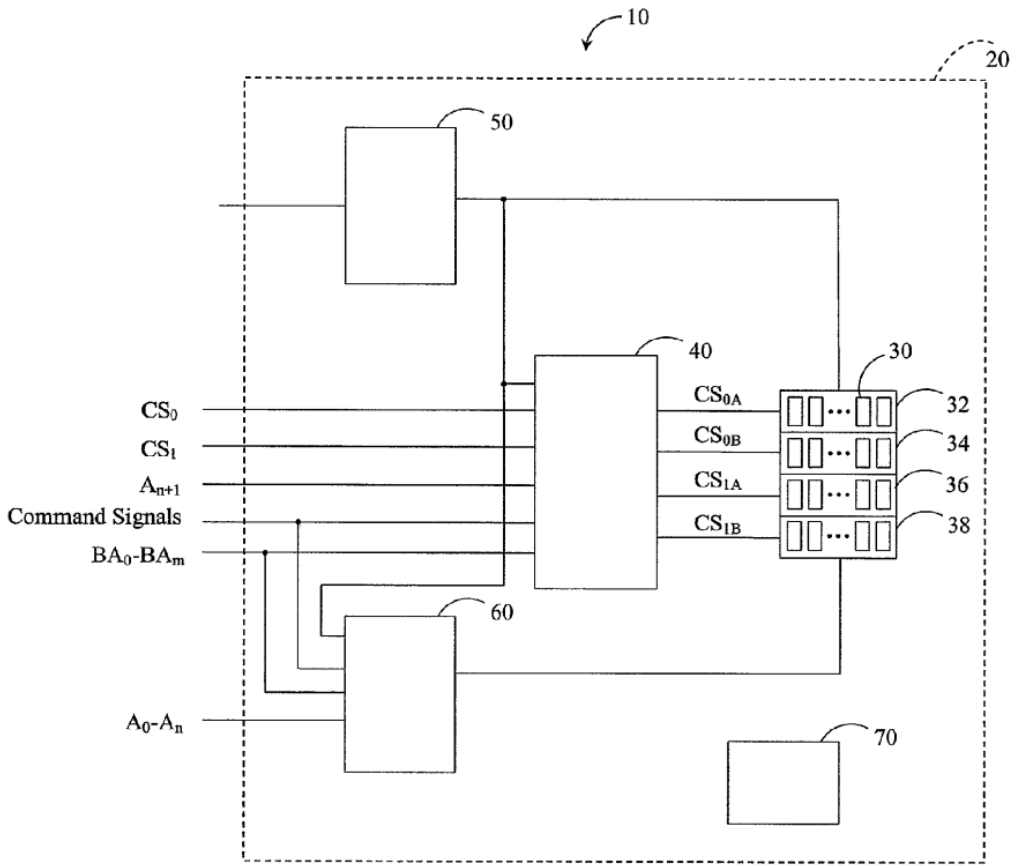

Figure 1A shows a memory module 10 with printed circuit board 20 and memory devices 30 connected to the printed circuit board. *Id.* at 5:9–11. Memory devices 30 are arranged in ranks 32, 34, 36, 38. *Id.* at 22:35–37. The memory devices 39 may be double-data rate (DDR) dynamic random-access memory (DRAM) devices. *Id.* at 6:12–16. The memory module 10 further comprises logic element 40 coupled to the printed circuit board 20. *Id.* at 5:13–14. Logic element 40 receives a set of input control signals and generates output control signals for select memory devices 30. *Id.* at 5:14–21. Phase-lock loop device 50 and register 60 are also mounted on printed circuit board 20. *Id.* at 5:25–27. The phase-lock loop device 50 generates clock signals to memory devices 30, logic element 40, and register 60.

Register 60 receives and buffers control signals including address signals, and transmits corresponding signals to appropriate memory devices 30. *Id.* at 5:31–36.

In Figure 1A, logic element 40 receives a set of input control signals from the computer system that include chip-select signals CS_0–CS_1, address signal A_{n+1}, and bank address signals BA_0–BA_m. *Id.* at 7:35–53. To the computer system, the memory module has only two ranks selectable with either CS_0 or CS_1. *Id.* at 6:55–7:19. However, logic element 40 generates a set of output control signals CS_{0A}, CS_{0B}, CS_{1A}, CS_{1B} corresponding to the four ranks 32, 34, 36, 38 of memory devices 30. *Id.* at 6:61–63. Logic element 40 also receives command signals (e.g., read or write) from the computer system and transmits the command signal to memory devices on the selected rank of the memory module. *Id.* at 6:55–61, 7:43–53. In some embodiments, logic element 40 transmits command signals to only a single memory device on a multi-device rank at a time. *Id.* at 8:49–54.

D. Claim 16 of the '912 Patent

Claim 16 of the '912 patent is an independent claim, and the only claim that is challenged in this proceeding. Claim 16 is reproduced below.

> [16.pre] A memory module connectable to a computer system, the memory module comprising:
>
> [16.a] a printed circuit board;
>
> [16.b] a plurality of double-data-rate (DDR) memory devices coupled to the printed circuit board, [16.b.i] the plurality of DDR memory devices having a first number of DDR memory devices arranged in a first number of ranks;
>
> [16.c] a circuit coupled to the printed circuit board, the circuit comprising a logic element and a register, [16.c.i] the logic element receiving a set of input signals from the computer

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Ex. 1023, p. 5

> system, the set of input signals comprising at least one row/column address signal, bank address signals, and at least one chip-select signal, [16.c.ii] the set of input signals configured to control a second number of DDR memory devices arranged in a second number of ranks, the second number of DDR memory devices smaller than the first number of DDR memory devices and the second number of ranks less than the first number of ranks, [16.c.iii] the circuit generating a set of output signals in response to the set of input signals, the set of output signals configured to control the first number of DDR memory devices arranged in the first number of ranks, [16.c.iv] wherein the circuit further responds to a command signal and the set of input signals from the computer system by selecting one or two ranks of the first number of ranks and transmitting the command signal to at least one DDR memory device of the selected one or two ranks of the first number of ranks; and
>
> [16.d] a phase-lock loop device coupled to the printed circuit board, [16.d.i] the phase-lock loop device operatively coupled to the plurality of DDR memory devices, the logic element, and the register,
>
> [16.e] wherein the command signal is transmitted to only one DDR memory device at a time.

Id. at *Inter Partes* Reexamination Certificate, 3:9–43.

E. Asserted References[2]

Reference		Date	Exhibit No.
Perego-422 [3]	US 7,363,422 B2	Apr. 22, 2008	1035

[2] Petitioner also relies upon the Declaration of Dr. Andrew Wolfe (Ex. 1003).

[3] Although the Petition refers to this reference as "Perego," we refer to it as "Perego-422" to distinguish it from another reference of record by the same

Reference		Date	Exhibit No.
[4]			
Amidi [5]	US 2006/0117152 A1	Jun. 1, 2006	1036
Ellsberry [6]	US 2006/0277355 A1	Dec. 7, 2006	1037

Pet. 4, 14–22.

F. Asserted Challenges to Patentability

Claim Challenged	Basis	Reference(s)/Basis
16	§ 103(a)	Perego-422
16	§ 103(a)	Perego-422, Amidi
16	§ 103(a)	Ellsberry

Pet. 4.

G. Procedural History

The ’912 patent was filed on September 7, 2007, as U.S. Application No. 11/862,931 (“the ’931 application”), and issued November 17, 2009. Ex. 1001, codes (21), (22). The ’912 patent indicates that it is a continuation of U.S. Application No. 11/173,175, filed on July 1, 2005, which issued as

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inventor, U.S. Patent No. 7,356,639 (“Perego-639”) (Ex. 1061).

[4] Petitioner contends Perego-422 is prior art under 35 U.S.C. §§ 102(a) and (e). Pet. 14.

[5] Petitioner contends Amidi is prior art under 35 U.S.C. §§ 102(a) and (e). Pet. 18.

[6] Petitioner contends Ellsberry is prior art under under 35 U.S.C. §§ 102(a) and (e). Pet. 20.

U.S. Patent No. 7,289,386 ("the '386 patent"). *Id.* at code (63). The '912 patent further indicates that this continuation is in turn a continuation-in-part of U.S. Application No. 11/075,395, filed March 7, 2005, now U.S. Patent No. 7,286,436 ("the '436 patent"). *Id.* The '912 patent also claims priority to U.S. Provisional No. 60/588,244 ("the '244 provisional") filed July 15, 2004, U.S. Provisional No. 60/550,668 ("the '668 provisional") filed March 5, 2004, and U.S. Provisional No. 60/575,595 ("the '595 provisional") filed May 28, 2004. *Id.* at code (60).

Perego-422 was not considered by the Examiner during examination of the '912 patent. However, a related patent with similar disclosure, Perego-639, was considered and is listed on the patent. Ex. 1002, 125; Ex. 1001, 2.

Amidi was considered and discussed by the Examiner during examination and is listed on the patent. Ex. 1002, 91, 509–510, 536; Ex. 1001, 2. Amidi was further considered in the reexamination of the '912 patent. Ex. 1010, 1, 2947, 3865–67.

During examination, the Examiner acknowledged Ellsberry's substance at a high level as including a memory module and phase-locked loop (PLL). Ex. 1002, 509–510, 516. However, the Examiner noted that Ellsberry was filed after the earliest effective filing date of the '931 application on which the '912 patent issued. *Id.* Consequently, the Examiner did not consider Ellsberry to be prior art to the '931 application. Ellsberry is listed on the '912 patent as having been considered by the Examiner. Ex. 1001, 2.

On September 22, 2009, Patent Owner served Inphi Corp. with a complaint for infringement of U.S. Patent No. 7,532,537 in the Central District of California. Exs. 2002, 2017.

On December 4, 2009, Patent Owner served Google, Inc. with a complaint for infringement of the ’912 patent in the Northern District of California. Ex. 2001. On May 18, 2010, the District Court for the Northern District of California stayed the litigation to await the outcome of reexamination of the ’912 patent.

Thereafter, Inphi Corporation (Requester 1), Smart Modular Technologies, Inc. (Requester 2), and Google, Inc. (Requester 3) filed *inter partes* reexaminations as Control Nos. 95/001,339, 95/000,578, and 95/000,579 on June 8, 2010, October 20, 2010 and October 21, 2010, respectively, against the ’912 patent. Ex. 1011, 5. On February 28, 2011, these proceedings were merged into a single proceeding under Control No. 95/000,578. *Id.*

During the reexamination, Amidi was cited in a Form PTO 1449. Ex. 1010, 1. Amidi was considered in combination with references called “Micron DDR2,” “Dell2,” and “Dell ’184” in proposed § 103 rejections against claim 16 of the ’912 patent. Ex. 1010, 2456–2457, 4442–4443, 5300–5303. The Examiner confirmed patentability of claim 16 and Patent Owner amended the claim into independent form. Ex. 1010, 3145, 3844, 3945–3946, 4569–4570, 4722, 5326. Requesters appealed to the Board, which affirmed the Examiner’s decision confirming claim 16 as patentable. *Id.* at 7259–7260; Ex. 1011, 78–80*; Inphi Corp. Requester 1, Smart Modular Tech. (WWH), Inc. Requester 2, and Google, Inc. Requester 3 v. Patent of Netlist, Inc., Patent Owner*, 2016 WL 3088604 (Patent Tr. & App. Bd.)

(May 31, 2016). Requesters sought reconsideration of the Board's decision, arguing that claim 16 would have been obvious in view of Amidi alone and combined with Dell 2. Ex. 1010, 7258–7264. The Board denied rehearing. Thereafter, Requesters appealed to the Court of Appeals for the Federal Circuit, which affirmed the Board's decision on June 15, 2020. *Id.* at 7905. The *Inter Partes* Reexamination Certificate confirming claim 16 issued on February 8, 2021. Ex. 1011, 7966.

From 2015 to 2020, Patent Owner licensed Petitioner under the '912 patent until Patent Owner terminated the license for "material breach." Prelim. Resp. 24 (citing Ex. 2023, 18–20).

On October 15, 2021, Petitioner filed a complaint for non-infringement and unenforceability, as well as breach of contract, against Patent Owner regarding the '912 patent and two other patents in the District Court for the District of Delaware. Ex. 1049. Patent Owner sought to dismiss the Delaware case for lack of subject matter jurisdiction and failure to state a claim upon which relief could be granted. Ex. 1052. The Northern District of California stayed Google's case in favor of the Delaware litigation. Ex. 1054. Thereafter, Patent Owner filed a complaint, and then an amended complaint, against Petitioner for infringement of the '912 patent and others in the Eastern District of Texas. Ex. 1056; Ex. 1057. Petitioner sought transfer of the Texas case to the Northern District of California, and alternatively requested the Texas court to either stay the Texas case pending resolution of a Ninth Circuit Appeal or consolidate this case with "the First Texas Case" (No. 2:21-cv-463). Ex. 1062.

The record also includes an Order from the Northern District of California granting intervening rights to the claims asserted by Patent Owner against Google except for claim 16 of the ’912 patent. Ex. 1053.

III. ANALYSIS

A. Statutory Time-Bar under 35 U.S.C. § 315(b)

Patent Owner argues that Google is an unnamed real party in interest and privy of Petitioner. Prelim. Resp. 6–16. Patent Owner contends that the Petition is time-barred under § 315(b) because Google was sued on the ’912 patent in 2009, and thus more than one year before filing of the Petition.

For the following reasons, we do not agree that Google is a real party in interest or privy or that the Petition is time-barred under § 315(b) due to the 2009 complaint against Google.

1. Whether Google is a Real Party in Interest

“Whether a party who is not a named participant in a given proceeding nonetheless constitutes a ‘real party-in-interest’ . . . to that proceeding is a highly fact-dependent question.” Consolidated Trial Practice Guide, 13 (Nov. 2019), available at https://www.uspto.gov/sites/default/files/documents/tpgnov.pdf (“TPG”). “[A]t a general level, the ‘real party-in-interest’ is the party that desires review of the patent,” and, thus, “may be the petitioner itself, and/or it may be the party or parties at whose behest the petition has been filed.” *Id.* at 14. “For example, a party that funds and directs and controls an IPR or PGR petition or proceeding constitutes a ‘real party-in-interest.’” *Id.* at 17. Several relevant factors for determining whether an unnamed party to an *inter partes* proceeding is a real party-in-interest include the party’s relationship with the petitioner, the party’s

relationship to the petition, and the nature of the entity filing the petition. *Id.* at 17–18. Determining whether an unnamed party is a real party-in-interest "demands a flexible approach that takes into account both equitable and practical considerations, with an eye toward determining whether the non-party is a clear beneficiary that has a preexisting, established relationship with the petitioner." *Applications in Internet Time, LLC v. RPX Corp.* ("*AIT*"), 897 F.3d 1336, 1351 (Fed. Cir. 2018).

Petitioner's initial identification of the real party-in-interest is accepted unless and until Patent Owner produces some evidence to support its argument that a particular third party should be named as a real party-in-interest. *Worlds Inc. v. Bungie, Inc.*, 903 F.3d 1237, 1242 (Fed. Cir. 2018). Petitioner bears the ultimate burden of persuasion to show that its Petition is not time-barred under § 315(b). *Id.*

Patent Owner focuses on three factors in contending that Google is a real party-in-interest: (1) Google's alleged interest and benefit from this proceeding; (2) Petitioner's alleged representation of Google's interest; and (3) Petitioner's business model, including its preexisting relationship with Google. Prelim. Resp. 8–14.

Turning to the first of these factors, Patent Owner contends Google's alleged infringement has been willful; that Google is the only entity with legal exposure to damages in the United States; that Google is time-barred under § 315(b) by the 2009 complaint served on it; and that Google's participation in the reexamination bars it from challenging the same claim in District Court. *Id.* at 8–9.

Petitioner, on the other hand, contends that Patent Owner lost its case against Google. Prelim. Reply 1. Specifically, Petitioner contends that

intervening rights precluded infringement before 2021 because all asserted claims were either amended or canceled during reexamination, and because the accused products from 2009 were no longer in use. *Id.* (citing Ex. 1053, 44:5–10; Ex. 1054, 10:4–10). Petitioner's assertion is supported by an order from the Northern District of California granting Google's motion for summary judgement on the issue of intervening rights for all but claim 16 of the '912 patent for which summary judgement was denied. Ex. 1053, 44. In addressing Google's motion to strike Patent Owner's assertion of claim 16 against Google, the Northern District of California stated in its order that "[c]onsistent with Google's assertion, it appears from this evidence that DDR4 DIMMs operating in PDA mode transmit a command signal to all DRAM in a given rank at the same time" and that "this evidence is largely unrebutted by [Patent Owner]." Reply 1–2 (citing Ex. 1053, 11:3–12). In contrast, claim 16 recites that "the command signal is transmitted to only one DDR memory device at a time." Ex. 1001, 3:42–43 (reexamination certificate). Consequently, the present record shows that Google may have little if anything to gain by this proceeding.

To specifically address Patent Owner's arguments concerning Google's alleged interest and benefit in this proceeding, Patent Owner does not explain why any alleged willful infringement on the part of Google would matter in the real party-in-interest analysis, let alone how its infringement case is sound in view of the Northern District of California's observations. *See* Prelim. Resp. 8–9. Patent Owner also does not explain why, if Google is the only party with legal exposure to damages, it also sued Petitioner for damages in the Eastern District of Texas for infringing the '912 patent. *See id.* at 9; Prelim. Reply 1; Ex. 1056; Ex. 1058. And

although Google's participation in the *inter partes* reexamination of the '912 patent may preclude it from asserting certain invalidity defenses in District Court, as Patent Owner contends (*see* Prelim. Resp. 9), Patent Owner does not address the possibility that Google achieved all it sought in the reexamination such that it has no interest in this proceeding.

Consequently, on the existing record, Petitioner has shown sufficiently that Google has little, if any, interest or benefit accruing to it in this proceeding.

Patent Owner contends that Petitioner is representing Google's interest because Petitioner admitted in filings in the District of Delaware that it was challenging the '912 patent at the behest of Google due to indemnification requests it received from Google and its subcontractor Lenovo. Prelim. Resp. 9–11 (citing Ex. 1049 ¶ 11; Ex. 1051 ¶ 14).

The record developed thus far does not show the language of Google's indemnification request or demand, nor does it show what the relevant agreements were between Google and Petitioner. Whatever their terms, Google's indemnification request (*see* Ex. 1051 ¶¶ 43–44) makes it unlikely that Google is funding or controlling this proceeding. *See* Prelim. Reply 2 (explaining that Google did not pay Petitioner to reduce its exposure and that Petitioner is the party with the apparent risk of infringement liability).

Patent Owner further contends that Google benefited by using the Petition and declaratory judgement sought by Petitioner in the District of Delaware as a reason to request a stay of the Northern District of California litigation. Prelim. Sur-Reply 12. Although Google may have derived a minor ancillary benefit in this respect, we find it unlikely that Petitioner's

purpose in filing the Petition was to provide Google with a basis to request a stay, particularly when, at the time the Petition was filed, Patent Owner had effectively "lost" its case due to intervening rights and the accused products no longer being in use. *See* Prelim. Reply 1. Any benefit that accrued to Google regarding the request for stay was marginal. If anything, the fact that Google and Patent Owner filed a joint motion to stay their litigation pending resolution of the district court litigation between Petitioner and Patent Owner tends to demonstrate that Google is not a real party-in-interest to this proceeding. Ex. 1064, 1–2.

The record shows that Patent Owner's threats against Petitioner and Petitioner's recognition that the '912 patent related to its products are what caused Petitioner to file its Petition, not any interest or benefit that would accrue to Google. Prelim. Reply 1. As Petitioner explains, Petitioner is the party with the apparent risk of infringement liability, not Google. *Id.* at 2.

Petitioner also cites the case of *Glenayre Electronics, Inc. v. Jackson*, 443 F.3d 851, 864 (Fed. Cir. 2006). Prelim. Reply 2. Under this case, "[a] party [Patent Owner] is precluded from suing to collect damages for direct infringement by a buyer and user of a product [Google] when actual damages covering that very use have already been collected from the maker and seller of that product [Petitioner]." *Glenayre*, 443 F.3d at 864. Thus, under the *Glenayre* case, Patent Owner can collect damages for direct infringements from either the manufacturer (Petitioner) or the buyer-user (Google), not both. Patent Owner's suit against Petitioner in the Eastern District of Texas, if successful, would preclude Patent Owner from collecting damages for the same acts of direct infringement from Google in the Northern District of California. And Google has represented to the

Northern District of California District Court that "the only products remaining at issue are 4-Rank DDR4 RDIMMS and 4- Rank DDR4 LRDIMMs that Google has purchased from Samsung." Ex. 2004, 14, *cited in* Prelim. Sur-Reply 4. Petitioner acknowledges that Patent Owner has asserted claim 16 of the '912 patent against its newly released products incorporating DDR4 technology. Prelim. Reply 1.

Consequently, on this record, Petitioner has shown sufficiently that Petitioner is not representing Google's interest, but solely its own interest, in this proceeding.

Although Patent Owner overstates Petitioner's and Google's relationship as "permeating all aspects of their businesses" (Prelim. Resp. 12), Patent Owner is correct to the extent it contends that the nature of Petitioner's and Google's businesses, and their preexisting relationship, is relevant to the real party-in-interest analysis. *See RPX Corp. v. Applications in Internet Time, LLC*, IPR2015-01750, Paper 128, 10 (Oct. 2, 2020) (considering the nature and relationship of petitioner and party); *Ventex Co., Ltd. v. Columbia Sportswear North America*, IPR2017-00651, Paper 148, 7 (Jan. 24, 2019) (precedential) (considering agreements between petitioner and an unnamed party).

As Patent Owner states, Google's business primarily pertains to its search engine from which it derives revenue for advertisements. Prelim. Resp. 12. Google also has a cloud business hosting data and applications. *Id.* These businesses utilize memory modules in servers and smartphones, although they are generally agnostic to what type of memory modules are used in these devices. *Id.* (acknowledging there is a "highly competitive market" for DIMMs). In addition, Google sells Pixel smartphones and other

devices. Ex. 2010.

Petitioner, on the other hand, manufactures electronic devices and components thereof, including memory modules. *Id.* Although, as Patent Owner contends (*id.* at 13–14), Samsung and Google have a close relationship by virtue of Google's Android operating system running on some of Petitioner's smartphones, Chromebook computers, and other products and services, these businesses are not directly connected to the memory modules produced by Petitioner or its competitors, let alone those described and claimed in the '912 patent. Ex. 2008; Ex. 2014. As Petitioner notes, Patent Owner's Exhibits pertain to arms-length transactions between the two conglomerates concerning Android smartphones, Chromebook computers, and smart watches, among other products and services. Prelim. Reply 3. Android smartphones and Chromebook computers are not the only phones and computers produced by Petitioner, and Petitioner is not the only manufacturer of Android smartphones and Chromebook computers. *See* Ex. 2009, 1. Petitioner's Tizen operating system competes directly against Android, and Petitioner's smartphones compete directly against Google's Pixel phones. Prelim. Resp. 14; Ex. 2010; Ex. 2027, 1 ("It's hard to know whether the two companies [Petitioner and Google] quietly hate each other while remaining diplomatic in public as they wrestle over a variety of mobile initiatives in the spirit of 'competing while cooperating.'").

The record does not show that any exclusive relationship exists between Petitioner and Google, such as Petitioner being the only supplier of memory modules, phones, or computers used in Google's businesses or Petitioner's devices using only Google's software to the exclusion of competitive offerings. *Cf. Ventex*, Paper 148, 9 (exclusive business

relationship found to be a factor in deciding that non-party was a real party-in-interest).

Petitioner and Google have aligned interests in the success of each other's businesses in some respects, but, as noted, in others they are competitive or disinterested. For example, the greater the number of Android smartphones and Chromebook computers that Petitioner sells to its customers, the greater the opportunity is for Google to offer its advertising and services on those devices. But, as noted, Google's Android operating system competes directly with Petitioner's Tizen operating system, just as Google's Pixel phone competes against Petitioner's phone offerings. Whatever aligned interest Petitioner and Google may have is not tied in any significant way to the particular type of memory modules claimed in the '912 patent. *Cf. Ventex*, Paper 148, 8 (unnamed and named parties had mutual interest tied to subject of infringement allegations).

We are also persuaded by Petitioner's contention that there was no overlap between this proceeding and the '912 patent claims asserted in the 2009 complaint until Patent Owner recently amended its complaints to assert claim 16 against Petitioner's newly released products. Prelim. Reply 1; Ex. 1056; Ex. 1059; *cf. Ventex*, Paper 148, 9 (overlap between claims in litigation and *inter partes* review considered in analysis of unnamed real party-in-interest). Claim 16 of the '912 patent was not included in the complaint against Google as originally filed in 2009 in the Northern District of California. Reply 1. Petitioner is correct that "it would be deeply unfair to allow [Patent Owner] to manufacture a time bar against [Petitioner]" merely by amending its complaints after the Petition was filed to assert claim 16 against Petitioner's DDR4 products that did not exist when the

2009 complaint was filed against Google. *See* Prelim. Reply 4; *AIT*, 897 F.3d at 1351 ("Determining whether a non-party is a 'real party in interest' demands a flexible approach that takes into account both *equitable and practical considerations*, with an eye toward determining whether the non-party is a clear beneficiary that has a preexisting, established relationship with the petitioner" (emphasis added)).

On this record, Petitioner has carried its burden to show that Petitioner is the sole real party-in-interest, i.e., that Google is not an unnamed real party in interest.

2. Privity

In *Taylor v. Sturgell*, 553 U.S. 880, 894–95 (2008), the Supreme Court provided a non-exhaustive list for examining whether the legal relationship between two parties establishes that one is the privy of the other: "(1) an agreement between the parties to be bound; (2) pre-existing substantive legal relationships between the parties; (3) adequate representation by the named party; (4) the non-party's control of the prior litigation; (5) where the non-party acts as a proxy for the named party to relitigate the same issues; and (6) where special statutory schemes foreclose successive litigation by the non-party (e.g., bankruptcy and probate)." Analysis under any one of the factors can support a finding of privity. *AIT*, 897 F.3d at 1363.

Patent Owner contends that it presented evidence of "pre-existing substantive legal relationships between the parties," which is the second *Taylor* category. Prelim. Sur-Reply 4. Examples of "[q]ualifying relationships include, but are not limited to, preceding and succeeding

owners of property, bailee and bailor, and assignee and assignor." *Taylor*, 553 U.S. at 894.

Patent Owner contends that *AIT* establishes that a privy is a party that has a direct relationship to the petitioner with respect to the allegedly infringing product or service. Prelim. Resp. 15 (citing *AIT* at 1350). Patent Owner contends that Google uses memory products supplied by Petitioner. *Id.* at 16. Patent Owner, however, has not provided persuasive authority to show that a supplier-integrator relationship alone would be sufficient to establish privity. On the contrary, Petitioner provides compelling authority that a customer relationship alone does not trigger privity. Prelim. Reply 3 (citing *Wi-Fi One, LLC v. Broadcom Corp.*, 887 F.3d 1329, 1340–41 (Fed. Cir. 2018); *WesternGeco LLC v. ION Geophysical Corp.*, 889 F.3d 1308, 1319–20 (Fed. Cir. 2018)).

Patent Owner argues that Petitioner represents Google's interest in this proceeding. Prelim. Resp. 9–12. To the extent Patent Owner argues that Petitioner is a proxy under the fifth *Taylor* factor, we have already discussed above that Petitioner is representing its own interests in this proceeding, not Google's. *See* Section III.A.1.

Accordingly, Petitioner has shown that it is the sole real party-in-interest in this proceeding, and that Google is not a real party-in-interest or privy of Petitioner. Consequently, the Petition is not time-barred under § 315(b) contrary to Patent Owner's assertions.

B. Discretionary Denial under § 314(a) – General Plastics

Patent Owner contends that we should deny the Petition as an improper serial challenge under *General Plastic Industrial Co., Ltd. v.*

Canon Kabushiki Kaisha, IPR2016-01357, Paper 19 (PTAB Sept. 6, 2017) (precedential) and *In re Vivint, Inc.*, 14 F.4th 1342, 1353 (Fed. Cir. 2021). Prelim. Resp. 16–25.

In *General Plastic*, a petitioner filed a first set of petitions that the Board denied on the merits. *General Plastic*, at 2. Several months later, the same petitioner filed follow-on petitions against the same patents. *Id.* at 3. Considering what are commonly now referred to as "the *General Plastic* factors" (*id.* at 16), the Board exercised its discretion to deny institution of the follow-on petitions. *Id.* at 22.

Patent Owner asks us to extend the *General Plastic* framework to discretionarily deny the Petition due to the prior *inter partes* reexamination of the '912 patent requested by Google and others. Although Patent Owner rightly asserts that *Valve Corp. v. Elec. Scripting Prods., Inc.*, IPR2019-00062, Paper 11, at 8–15 (PTAB Apr. 2, 2019) (precedential) applied *General Plastic* when a previous challenge was brought by a different petitioner (Prelim. Resp. 18), Patent Owner points to no authority that *General Plastic* has ever been applied to deny institution of a petition based on a prior reexamination. We decline to extend *General Plastic* to discretionarily deny the Petition on this basis.

In addition to *General Plastic*, Patent Owner relies on *Vivint* as supporting its contention that the Petition should be discretionarily denied due to the *inter partes* reexamination of the '912 patent. Prelim. Resp. 17. The facts in *Vivint*, however, are distinguishable from this proceeding. In *Vivint*, a petition for *inter partes* review was denied as "undesirable, incremental petitioning" and then the Office granted *ex parte* reexamination based on substantial new grounds of patentability, some of which were the

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same grounds raised in the *inter partes* review, while others were different. *Vivint*, 14 F.4th at 1353–54. In contrast, the arguments raised here are not the same as in the previous *inter partes* reexamination.

Consequently, we determine that *General Plastics* under § 314(a) is not applicable to the facts of this proceeding.

C. Discretionary Denial Under 35 U.S.C. § 325(d)

Under § 325(d), in determining whether to institute an *inter partes* review, "the Director may take into account whether, and reject the petition or request because, the same or substantially the same prior art or arguments previously were presented to the Office." In evaluating arguments under § 325(d), we use a two-part framework: (1) whether the same or substantially the same art previously was presented to the Office or whether the same or substantially the same arguments previously were presented to the Office; and (2) if either condition of the first part of the framework is satisfied, whether the petitioner has demonstrated that the Office erred in a manner material to the patentability of challenged claims. *Advanced Bionics, LLC v. MED-EL Elektromedizinische Geräte GmbH*, IPR2019-01469, Paper 6 at 8 (PTAB Feb. 13, 2020) (precedential) ("*Advanced Bionics*"). We also consider the non-exclusive factors set forth in *Becton, Dickinson and Co. v. B. Braun Melsungen AG*, IPR2017-01586, Paper 8 (PTAB Dec. 15, 2017) (precedential in relevant part) ("*Becton, Dickinson*"), which "provide useful insight into how to apply the framework" under § 325(d). *Advanced Bionics* at 9. Those non-exclusive factors are the following:

> (a) the similarities and material differences between the asserted art and the prior art involved during examination;

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> (b) the cumulative nature of the asserted art and the prior art evaluated during examination;
>
> (c) the extent to which the asserted art was evaluated during examination, including whether the prior art was the basis for rejection;
>
> (d) the extent of the overlap between the arguments made during examination and the manner in which Petitioner relies on the prior art or Patent Owner distinguishes the prior art;
>
> (e) whether Petitioner has pointed out sufficiently how the Examiner erred in its evaluation of the asserted prior art; and
>
> (f) the extent to which additional evidence and facts presented in the Petition warrant reconsideration of the prior art or arguments.

Becton, Dickinson at 17–18. "If, after review of factors (a), (b), and (d), it is determined that the same or substantially the same art or arguments previously were presented to the Office, then factors (c), (e), and (f) relate to whether the petitioner has demonstrated a material error by the Office." *Advanced Bionics* at 10.

1. Advanced Bionics Part 1

Turning to the first part of the *Advanced Bionics* framework, we consider whether the same or substantially the same art or arguments previously were presented to the Office. We find it necessary to address only Ellsberry in our analysis.

The record shows that the Examiner considered Ellsberry during examination of the '912 patent. Ex. 1001, 2; Ex. 1002, 509–510, 516, 548. Specifically, the Examiner commented that "Ellsberry et al., filed after the instant application's earliest effective filing date, show a memory module with controller and PLL." Ex. 1002, 510. Ellsberry was also considered in the reexamination of the '912 patent. Ex. 1010, 2032, 2465.

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Thus, under the first part of *Advanced Bionics*, we find that same or substantially the same art or arguments previously were presented to the Office regarding Ellsberry.

2. Advanced Bionics Part 2

Under the second part of the *Advanced Bionics* framework, we consider whether Petitioner has demonstrated that the Office erred in a manner material to the patentability of the challenged claims.

Petitioner contends "the Examiner clearly erred in allowing claim 16" because the Examiner assumed that Ellsberry was not prior art to the '912 patent based on its earliest effective filing date. Prelim. Reply 8; Ex. 1002, 510. Petitioner contends that the '912 patent is not entitled to the priority benefit of its provisional applications. Pet. 63–69. Specifically, Petitioner contends the '668 and '595 provisionals did not disclose a "logic element" let alone one that receives "at least one row/column address signal, bank address signals, and at least one chip-select signal," as required by claim 16. *Id.* at 63. Petitioner contends that the '244 provisional discloses an ASIC decoder which could be a "logic element," but does not disclose "bank address" signals as required by claim 16. *Id.* (citing Ex. 1005, 10, Fig. 1; Ex. 1003 ¶ 189).

Petitioner further contends the '436 patent, which is in the priority chain of the '912 patent, fails to provide support for "a circuit" comprising "a logic element" and a "register" as required in claim 16 and shown in Figure 1A of the '912 patent, and by lacking Verilog code showing use of "row" and "bank address signals." *Id.* at 64 (citing Ex. 1003 ¶ 190).

Petitioner contends that Patent Owner did not recognize the problem of "back-to-back read commands which cross memory device boundaries"

causing collisions until the ’386 patent, which is late in the priority chain of the ’912 patent. Pet. 65 (citing Ex. 1001, 23:65–24:12, Fig. 5; Ex. 1008, 24:16–30, Fig. 5; Ex. 1003 ¶ 192). According to Petitioner, the earlier applications would have suffered signal errors, and those errors could have destroyed drivers. *Id.* at 65–66 (citing Ex. 1043, 89–90; Ex. 1003 ¶ 193).

Petitioner further contends it is not until the ’912 patent that a solution to this problem is described involving electrical isolation of the DQS data strobe signal lines of the memory devices using FET switches. Pet. 67–68 (citing Ex. 1001, 24:23–28, 24:45–49, 25:58–60; Ex. 1008, 24:41–56, 26:9–12; Ex. ¶ 194). By this time, Petitioner contends that Ellsberry had already disclosed the solution to back-to-back read operations by using separate ports for memory devices along with bidirectional drivers instead of the ’912 patent’s FET switches. *Id.* (citing Ex. 1037 ¶¶ 9, 31, 40, 45, 57, Fig. 4; Ex. 1043, 89–90; Ex. 1001, 24:45–49, 25:6–25, Fig. 6D; Ex. 1003 ¶ 195). Petitioner further contends that Ellsberry describes FET switches as too slow and imprecise to comply with then current JEDEC standards. Pet. 68 (Ex. 1037 ¶¶ 9, 57; Ex. 1003 ¶ 195).

Petitioner thus contends the inventors of the ’912 patent were not in possession of, and did not provide an enabling disclosure for, the full scope of claim 16 of the ’912 patent, making Ellsberry prior art. *Id.* at 68–69 (citing Ex. 1003 ¶¶ 188, 196).

Patent Owner argues that during reexamination of the ’912 patent, Inphi (Requester 1) similarly argued that claims reciting a “logic element [that] generates a first number of chip-select signals . . . in response at least in part to clock signals received from the [PLL]” were unsupported by the 912 patent because a person of ordinary skill in the art “would not have

known for certain how the signals from PLL 50 were used by logic element 40." Prelim. Resp. 74 (citing Ex. 1011, 88–89). Patent Owner states that the Board was unpersuaded by Inphi's argument. *Id.* (citing Ex. 1011, 89). But Inphi's arguments pertained to clock signals, not the features Petitioner contends are missing from the priority applications. And the disclosure of "control signals" in Figure 1 of the '244 provisional is not explicit enough to disclose the row/column address, bank address, and chip-select signals that Petitioner asserts are missing. *Id.* at 75 (citing Ex. 1005, Fig. 1). Although Figure 11A of the '436 patent may disclose some of these features, it does not disclose a register separate from a logic element, nor FET switches to achieve electrical isolation. *Id.* (citing Ex. 1009, Fig. 11a).

Consequently, we find that Petitioner carried its initial burden to show that Ellsberry is prior art. The burden of production thus shifts to Patent Owner to show that the subject matter of claim 16 of the '912 patent is supported by its priority applications such that Ellsberry is not prior art. Patent Owner has not presented evidence at this preliminary stage in support of that burden. *See Dynamic Drinkware, LLC v. National Graphics, Inc.*, 800 F.3d 1375, 1379 (Fed. Cir. 2021).

Petitioner has shown sufficiently that the Examiner erred in a manner material to the patentability of the challenged claims under the second part of the *Advanced Bionics* framework. The Examiner assumed that Ellsberry was not prior art based on the '912 patent's earliest priority date without considering whether the features claimed in the '912 patent were supported by the earlier priority applications.

Accordingly, we proceed to the merits of Petitioner's obviousness contentions.

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D. Obviousness Challenges

1. Principles of the Law of Obviousness

A claim is unpatentable under 35 U.S.C. § 103 if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious to a person having ordinary skill in the art to which said subject matter pertains. *See KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations, including (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of skill in the art; and (4) where in evidence, so-called secondary considerations, including commercial success, long-felt but unsolved needs, failure of others, and unexpected results. *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

When evaluating a combination of teachings, we must also "determine whether there was an apparent reason to combine the known elements in the fashion claimed by the patent at issue." *KSR*, 550 U.S. at 418 (citing *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006)). "[T]here must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness." *Kahn*, 441 F.3d at 988.

2. Level of Ordinary Skill in the Art

Factors pertinent to a determination of the level of ordinary skill in the art include "(1) the educational level of the inventor; (2) type of problems encountered in the art; (3) prior art solutions to those problems; (4) rapidity with which innovations are made; (5) sophistication of the technology; and (6) educational level of active workers in the field." *Envtl. Designs, Ltd. v. Union Oil Co. of Cal.*, 713 F.2d 693, 696–697 (Fed. Cir. 1983) (citing

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Orthopedic Equip. Co. v. All Orthopedic Appliances, Inc., 707 F.2d 1376, 1381–1382 (Fed. Cir. 1983)). "Not all such factors may be present in every case, and one or more of these or other factors may predominate in a particular case." *Id.*

Petitioner contends that a person of ordinary skill in the art in the field of memory module design in 2004 or 2005 would have an advanced degree in electrical or computer engineering and at least two years working in the field, or a bachelor's degree in such engineering disciplines and at least three years working in the field. Pet. 5. Petitioner contends such person would have been familiar with various standards of the day including JEDEC industry standards, knowledgeable about the design and operation of standardized DRAM and SDRAM memory devices and memory modules and how they interacted with the memory controller of a computer system. *Id.* at 6.

For purposes of its Preliminary Response only, Patent Owner applies the skill level of a POSITA proposed by Petitioner. Prelim. Resp. 28.

On this record, we accept Petitioner's statement of the level of ordinary skill in the art except that we omit the qualifiers "at least" before years of education and experience because they render the level ambiguous and encompass levels that are beyond ordinary. Otherwise, we find Petitioner's statement of the level of ordinary skill in the art consistent with the '912 patent and the applied prior art references. *Okajima v. Bourdeau*, 261 F.3d 1350, 1354–55 (Fed. Cir. 2001) (the applied prior art may reflect an appropriate level of skill).

3. Claim Construction

We construe claim terms "using the same claim construction standard

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that would be used to construe the claim in a civil action under 35 U.S.C. 282(b)." 37 C.F.R. § 42.100(b) (2019). There is a presumption that claim terms are given their ordinary and customary meaning, as would be understood by a person of ordinary skill in the art in the context of the specification. *See In re Translogic Tech., Inc.*, 504 F.3d 1249, 1257 (Fed. Cir. 2007). Nonetheless, if the specification "reveal[s] a special definition given to a claim term by the patentee that differs from the meaning it would otherwise possess[,] ... the inventor's lexicography governs." *Phillips v. AWH Corp.*, 415 F.3d 1303, 1316 (Fed. Cir. 2005) (en banc) (citing *CCS Fitness, Inc. v. Brunswick Corp.*, 288 F.3d 1359, 1366 (Fed. Cir. 2002)). "In determining the meaning of the disputed claim limitation, we look principally to the intrinsic evidence of record, examining the claim language itself, the written description, and the prosecution history, if in evidence." *DePuy Spine, Inc. v. Medtronic Sofamor Danek, Inc.*, 469 F.3d 1005, 1014 (Fed. Cir. 2006) (citing Phillips, 415 F.3d at 1312–17). Only disputed claim terms must be construed, and then only to the extent necessary to resolve the controversy. *See Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017).

Petitioner contends that "rank" refers to "an independent set of one or more memory devices on a memory module that act together in response to command signals, including chip select signals, to read or write the full bit-width of the memory module." Pet. 12 (citing Ex. 1003 ¶ 74).

Patent Owner contends the Board correctly construed the term in the reexamination as "a group of memory devices enabled to receive and transmit data by a common chip-select signal." Prelim. Resp. 29–30 (citing Ex. 1011, 79–80; Ex. 2026, 7). Patent Owner contends this definition of

"rank" is consistent with all embodiments of the '912 patent which show multiple memory devices per rank. *Id.* at 30–32 (citing Ex. 1001, Figs. 1A, 1B, 2A, 3A, 6:31–38, 7:9–13, 7:55–8:43, 8:64–9:18, 10:31–35, 12:13–25).

Thus, the dispute to be resolved between the parties is whether the term "rank" may refer to only one memory device, as Petitioner contends, or requires multiple devices, as Patent Owner contends.

Both Petitioner and Patent Owner rely on the following textbook definition of "rank" as supporting their views:

> **10.2.2 Rank**
>
> Figure 10.5 shows a memory system populated with 2 ranks of DRAM devices. Essentially, a *rank* of memory is a *"bank"* of one or more DRAM devices that operate in lockstep in response to a given command. However, the word *bank* has already been used to describe the number of independent DRAM arrays within a DRAM device. To lessen the confusion associated with overloading the nomenclature, the word *rank* is now used to denote a set of DRAM devices that operate in lockstep to respond to a given command in a memory system.

Ex. 1033, 413; Pet. 13; Prelim. Resp. 34. This text sets forth two definitions for "rank": (1) a "bank" of one or more DRAM devices that operate in lockstep in response to a given command"; and (2) "a set of DRAM devices that operate in lockstep to respond to a given command in a memory system." Ex. 1033, 413. The textbook definition of "rank" does not resolve the dispute between the parties since one can read it to mean that a "rank" includes "one or more devices," or that a "rank" must include multiple memory devices operating "in lockstep." *Id.* Petitioner's and Patent

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Owner's declarants are similarly at odds over the definition of "rank." Ex. 1003 ¶ 74; Ex. 2007 ¶ 65.

"Rank" is further distinguished from "bank" as follows:

> The number of banks within a rank is usually equal to the number of banks within a single DRAM device. In the case of SDRAM, for example, there are two banks in a DRAM device, and so a bank identifier is a single bit sent over the address bus at the time of a command.

Ex. 1034, 4 n.3. Hence, "bank" refers to arrays within a single memory device of a rank.

Petitioner contends the meaning of "rank" can be gleaned from the '912 patent itself. Pet. 13–14. Specifically, the '912 patent states the following:

> In certain embodiments, the command signal is passed through to the **selected rank only** (e.g., state 4 of Table 1). In such embodiments, the command signal (e.g., read) is sent to **only one memory device** or the other memory device so that data is supplied from one memory device at a time. In other embodiments, the command signal is passed through to both associated ranks (e.g., state 6 of Table 1). In such embodiments, the command signal (e.g., refresh) is sent to both memory devices.

Pet. 13–14 (citing Ex. 1001, 8:50–58) (emphasis Petitioner's). Petitioner contends that this excerpt from the '912 patent implies that a rank can be composed of only one memory device. *Id.* Patent Owner does not adequately address Petitioner's contention. *See* Prelim. Resp. 32–34.

Patent Owner contends that, during reexamination, the Examiner allowed claim 16 because Amidi failed to teach "transmit[ting] a command signal to only one DDR memory device at a time **when there is a plurality of memory devices in a rank**." Prelim. Resp. 29 (citing Ex. 1010, 3865–

67, 3904) (emphasis Patent Owner's). The Examiner's point was merely that the Requester did not provide a reasonable explanation why one would transmit a command signal to only one DDR memory device at a time when Amidi teaches there are a plurality of memory devices in a rank. Contrary to Patent Owner's assertion, this is not the same as stating that claim 16 requires a plurality of memory devices in a rank. *Id.*

We find no illumination of the meaning of "rank" in the file history of the examination of the '912 patent. *See* Ex. 1002.

Patent Owner further contends that the Board's supposed construction during reexamination is consistent with the stipulated construction for "rank" in the Google litigation in the Northern District of California that "rank" is "a group of memory devices enabled to receive and transmit data by a common chip-select signal." Prelim. Resp. 30 (citing Ex. 2026, 7). Although the Northern District of California's view of the meaning of "rank" carries weight here, Petitioner notes that claim 16 was not at issue in that litigation until recently. Prelim. Reply 6–7. Furthermore, Petitioner was not a party to that litigation, so it is not precluded here from providing its own interpretation of what the term "rank" means.

Petitioner contends that U.S. Patent 9,858,215 B1 ("the '215 patent") is related to the '912 patent, and that it refers to "rank" as "at least one memory integrated circuit." Ex. 1058, 152, 187 (3:33–35), 204 (37:35–38). Although Patent Owner characterizes Petitioner's observation as a "trick" because Patent Owner added disclosure to the '215 patent that is not present in the '912 patent (Prelim. Sur-Reply 6–7), Patent Owner does not deny that the '215 patent defines "rank" in this way. Claim terms must be interpreted consistently across related patents. *See SightSound Techs., LLC v. Apple*

Inc., 809 F.3d 1307, 1316 (Fed. Cir. 2015); *NTP, Inc. v. Research In Motion, Ltd.*, 418 F.3d 1282, 1293 (Fed. Cir. 2005); *Jonsson v. The Stanley Works*, 903 F.2d 812, 818 (Fed. Cir. 1990).

For purposes of this decision, we determine that "rank" refers to "one or more memory devices." We do not construe the term further at this time. *See Nidec, supra*. We do not view this issue as closed and will continue to consider any additional argument and evidence on this issue at trial.

4. Perego-422 (Ex. 1035)

Perego-422 is titled "Configurable Width Buffered Module." Ex. 1035, code (54). Perego-422 discloses a memory system architecture/interconnect topology that includes a configurable width buffer device coupled to at least one memory device on the configurable width memory module. *Id.*, code (57).

Perego-422's Figure 3B is shown below.

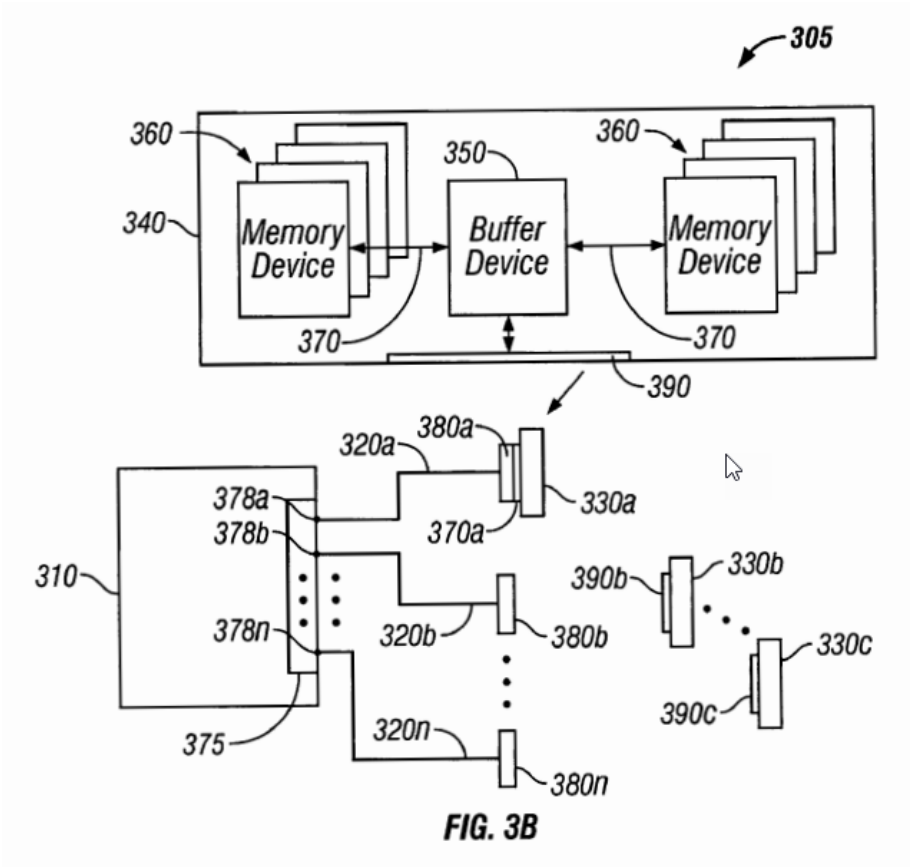


FIG. 3B

Figure 3B shows a system including memory controller 310 connected to multiple buffered memory modules 330a–330n. Each memory module 330a–330n may be configured like memory module 340 shown in the upper part of Figure 3B, to include a buffer device 350 and a plurality of memory devices 360. *Id.* at code (57), 4:63–5:15. The memory modules 330a–330n are connected in a dynamic point-to-point configuration. *Id.* at 6:57–62.

Perego-422's Figure 5B is shown below.

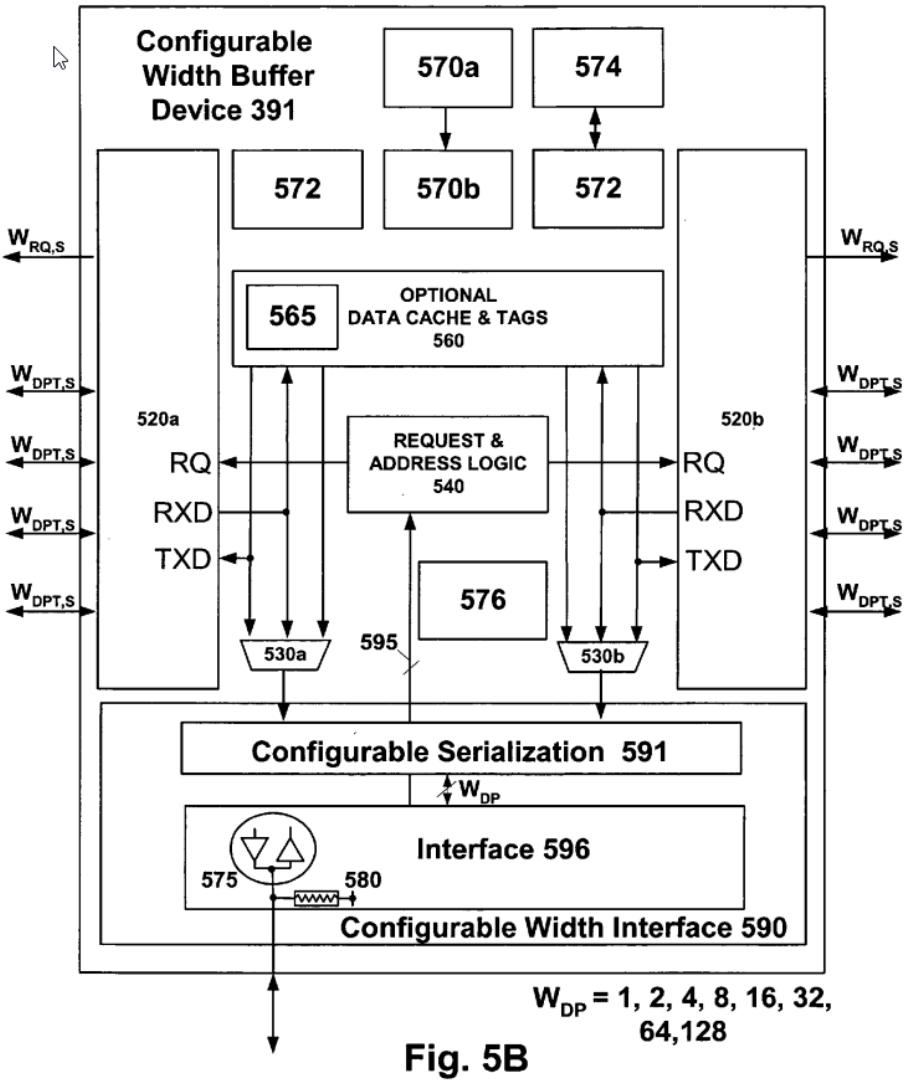


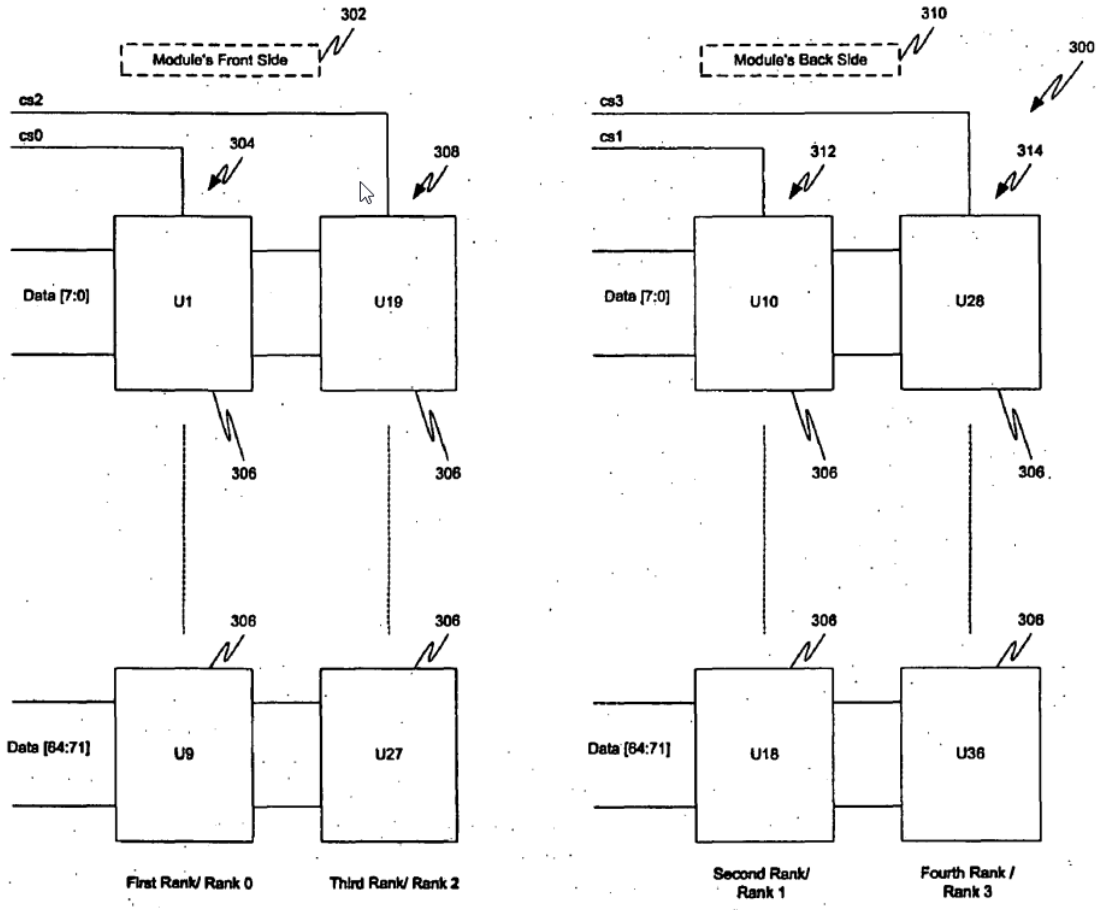
Fig. 5B

Perego-422's Figure 5B shows a configurable width buffer device 391 with programmable in interfaces 520a, 520b, which accommodate different numbers and types of memory devices. *Id.* at 13:60–14:15. Configurable width interface 590 communicates with the memory controller. *Id.* Serial interface 574 and operations circuit 572 provide information to the system memory controller for proper configuration and operation of the system. *Id.* at 12:20–34.

5. Amidi (Ex. 1036)

Amidi is titled "Transparent Four Rank Memory Module for Standard Two Rank Sub-Systems." Ex. 1036, code (54). The memory module has stacked memory ranks on its front and back sides. *Id.* at code (57). An emulator coupled to the memory module controls one memory rank based on signals from the memory controller. *Id.*

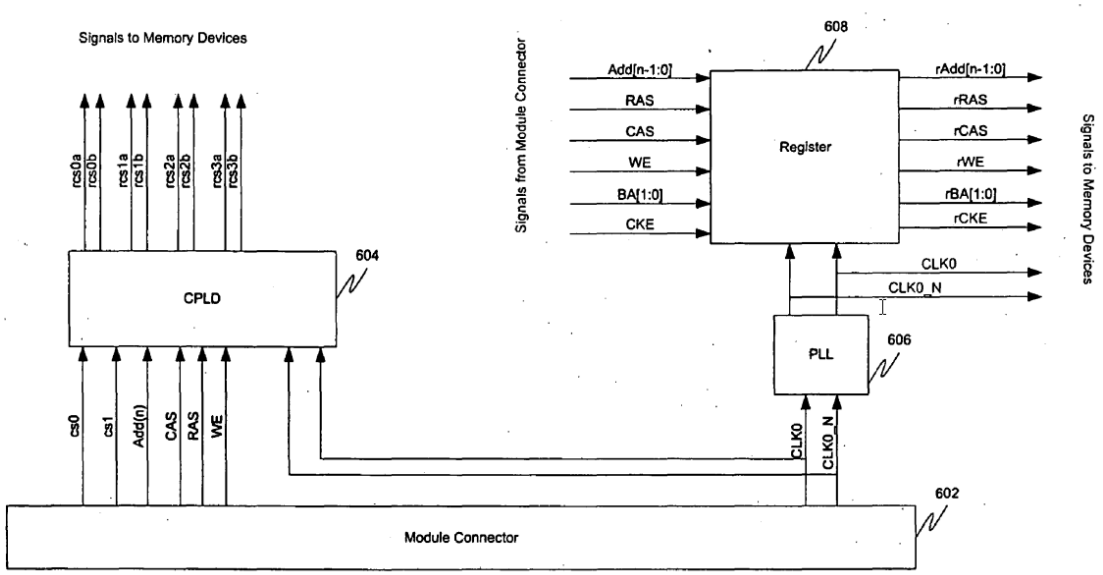
Amidi's Figure 3 is shown below.



Transparent Four Rank DDR Module Block Diagram
FIG. 3

Amidi's Figure 3 shows that each rank of the memory module has a corresponding chip select signal cs0–cs3.

Amidi's Figure 6A is shown below.



Row Address Decoding
FIG.6A

Figure 6A shows a Complex Programmable Logic Device CPLD 604 that uses command signals, chip select signals, and address signals to generate chip select signals (one for each rank). *Id.* ¶¶ 43, 50, 52. Figure 6A also shows a register 608 to store signals received from the module connector and provide them to the memory devices, as well as a phase-locked loop 606 to provide clock signals.

6. Ellsberry (Ex. 1037)

Ellsberry is titled "Capacity-Expanding Memory Device." Ex. 1037, code (54). "A control unit and memory bank switch are mounted on a memory module to selectively control write and/or read operations to/from memory devices communicatively coupled to the memory bank switch." *Id.* at code (57). "By selectively routing data to and from the memory devices, a plurality of memory devices may appear as a single memory device to the operating system." *Id.*

Figure 2 of Ellsberry is shown below.

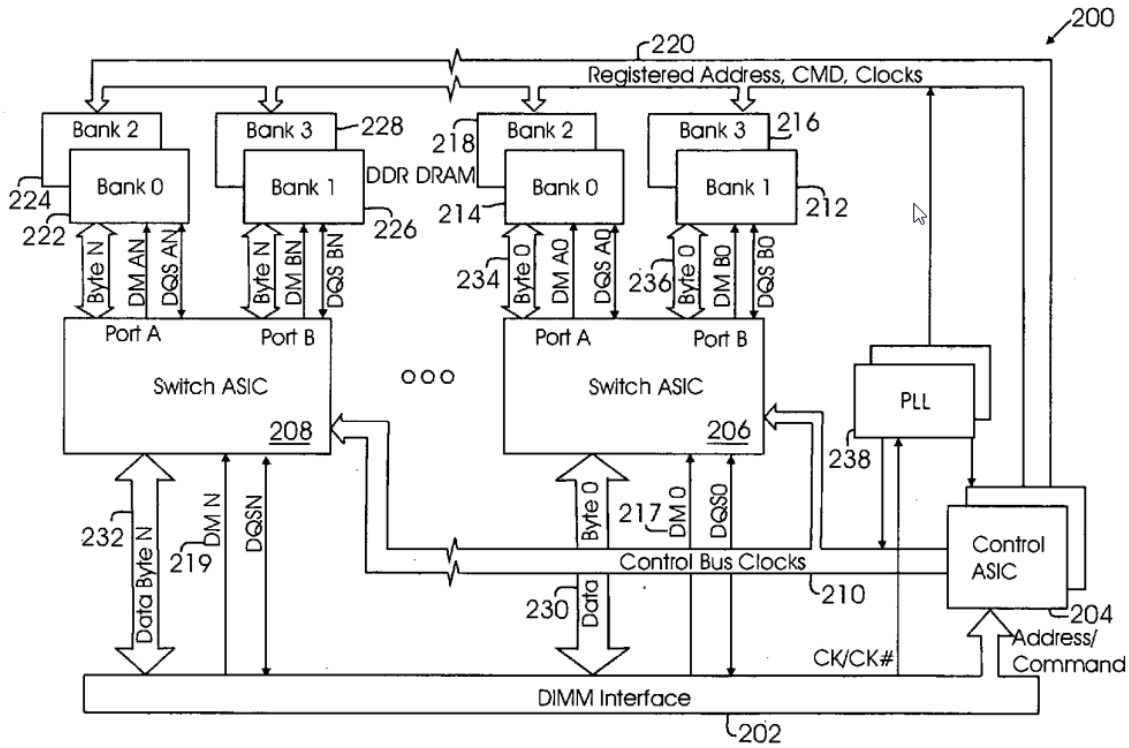


Fig. 2

Figure 2 "illustrates a block diagram of a capacity-expanding memory system 200 according to one embodiment." *Id.* ¶ 28. In Figure 2, system 200 has a DIMM interface 202 that couples to a "memory socket and communication bus over which data, memory addresses, commands, and control information are transmitted." *Id.* "The capacity-expanding feature of the invention is accomplished by a combination of control unit 204 and one or more memory bank switches 206 & 208." *Id.* Figure 2 of Ellsberry illustrates system 200 with control ASIC 204 that receives addresses and commands from DIMM interface 202 and generates corresponding control signals on bus 210 and addresses on bus 220 to selectively connect memory banks 212–228 to DIMM interface 202 via switch ASICs 206, 208. *Id.* ¶¶ 28–29.

Figure 12 of Ellsberry is shown below.

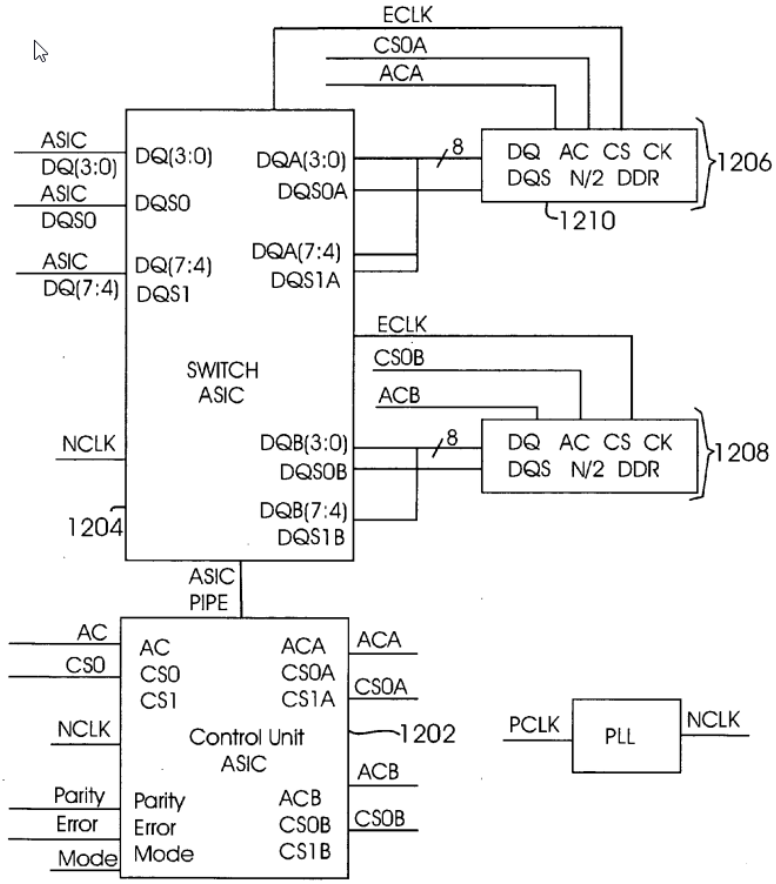


Fig. 12

Figure 12 of Ellsberry shows another configuration of the control unit and bank switch. *Id.* ¶ 52. In Figure 12, a single chip-select memory configuration includes one control unit 1202 and one bank switch 1204 which are used to control two memory banks 1206, 1208, each memory bank having one memory device 1210. *Id.* ¶ 55.

7. *Secondary Considerations of Obviousness*

Petitioner contends that the ’912 patent is remarkably similar to Ellsberry and that both were filed within a month of each other. Pet. 111. Petitioner contends Amidi and Perego-422 also recognized and solved the same problem in the 18 months before the ’912 patent. *Id.* Petitioner

contends this is evidence of "simultaneous invention" which is a secondary consideration of obviousness. *Id.* Patent Owner does not refute Petitioner's contentions. We give weight to Petitioner's evidence of "simultaneous invention" in our obviousness analysis.

8. Obviousness Challenge to Claim 16 based on Perego-422

Petitioner contends that claim 16 would have been obvious over Perego-422. Pet. 22–63. The preamble limitation [16.pre] of claim 16 recites "memory module connectable to a computer system." Ex. 1001, 3:9–11 (reexamination certificate). Petitioner contends the claimed "memory module" corresponds to Perego-422's memory module 340 with buffer device 350 and memory devices 360. Pet. 25 (citing Ex. 1035, Fig. 3B). Petitioner further contends the claimed "computer system" corresponds to Perego-422's memory system 305, including a controller 310 coupled to memory modules 330a–330c. *Id.* at 25–26 (citing Ex. 1035, 5:56–6:11, 7:39–41. 4:19–22, Fig. 3B; Ex. 1003 ¶¶ 108–109).

Petitioner sufficiently shows that the preamble of claim 16 is taught by Perego-422. It is thus unnecessary for us to determine whether the preamble is limiting.

Claim 16 further recites limitation [16.a] as "a printed circuit board." Ex. 1001, 3:12 (reexamination certificate). Petitioner contends that Perego-422 teaches that memory modules 340 "are incorporated onto individual substrates (e.g., PCBs)," noting that PCB stands for "printed circuit board." *Id.* at 26–27 (citing Ex. 1035, 5:60–62, 5:59–60, Fig. 3B; Ex. 1003 ¶¶ 111–113).

Petitioner sufficiently shows that limitation [16.a] of claim 16 is taught by Perego-422.

Claim 16 further recites limitation [16.b] as "a plurality of double-data-rate (DDR) memory devices coupled to the printed circuit board." Ex. 1001, 3:13–16 (reexamination certificate). Petitioner contends that Perego-422 teaches "memory devices 360 are discretely packaged synchronous type DRAM integrated circuits (ICs), for example, DDR memory devices." *Id.* at 27 (citing Ex. 1035, 8:1–9, 3:62–4:3, 10:56–59, Fig. 3B; Ex. 1003 ¶ 115). Petitioner further contends that Perego-422 teaches that the memory devices are coupled to the printed circuit board. *Id.* at 27–28 (citing Ex. 1035, 5:4–6, 5:60–62, 5:59–60, 6:12–15, Fig. 3B; Ex. 1003 ¶¶111–113, 116).

Claim 16 further recites limitation [16.b.i] as "the plurality of DDR memory devices having a first number of DDR memory devices arranged in a first number of ranks." Ex. 1001, 3:14–16 (reexamination certificate). Petitioner contends that Perego-422 teaches "grouping memory devices into multiple independent target subsets (i.e. more independent banks)." Pet. 28 (citing Ex. 1035, 15:37–45; Ex. 1003 ¶¶ 73–77, 118). Petitioner's declarant indicates that the term "rank" of memory is a bank of one or more DRAM devices that operate in lockstep in response to a given command. Ex. 1003 ¶ 75 (citing Ex. 1029, 6). Specifically, Petitioner contends that Perego-422 teaches a module with four memory devices arranged in four single device ranks. Pet. 30 (citing Ex. 1035, 10:17–20, 6:15–24, 9:58–60, 14:4–10, 10:56–67, 10:5–13, Fig. 4B; Ex. 1029, 6; Ex. 1003 ¶ 124).

Patent Owner contends that limitation [16.b.i] of claim 16 requires multiple-device ranks. Prelim. Resp. 40–41. However, Petitioner pointed out that Patent Owner's support for claim 16 relies on a passage of the '912 patent that may be construed as disclosing single device ranks. *See* Section

III.D.4 (claim construction); Pet. 13–14 (citing Ex. 1001, 8:50–56). As discussed above in Section III.D.4, we preliminarily determine that "rank" refers to "one or more memory devices." Thus, on this record, we disagree with Patent Owner's attempted distinction over the art.

Petitioner sufficiently shows that limitations [16.b] and [16.b.i] of claim 16 are taught by Perego-422.

Limitation [16.c] of claim 16 recites "a circuit coupled to the printed circuit board, the circuit comprising a logic element and a register." Ex. 1001, 3:17–18 (reexamination certificate). Petitioner contends that Perego-422's buffer device 405 is equivalent to the claimed "circuit," which comprises a "logic element" including request and address logic 540 that provides control and address lines (RQ) to memory interfaces 520a and 520b based on signals received from configurable interface 590. *Id.* at 33 (citing Ex. 1035, 5:56–67, 10:59–68, 9:58–60, 13:54–59, Figs. 4B, 5B, 5C; Ex. 1003 ¶¶ 111, 112, 116, 128).

Petitioner further contends that Perego-422 teaches that its buffer device includes a "register" that transceives and provides isolation for address, command, and data signals between the memory controller and memory devices on the module. *Id.* at 34 (citing Ex. 1035, 6:12–27). Petitioner contends that Perego-422's buffer device's interface 596 decodes control and address information. *Id.* (citing Ex. 1035, 13:54–59). Petitioner contends that a person of ordinary skill in the art would have understood from this disclosure that Perego-422's interface 596 includes registers (e.g., 597f–m in Fig. 5C) that latch the received address, command, and data signals to provide "isolation" and for decoding of the control and address information. *Id.* at 34–35 (citing Ex. 1035, 17:61–63).

Petitioner contends that Perego-422 discloses limitation [16.c.i] of claim 16 reciting "the logic element receiving a set of input signals from the computer system, the set of input signals comprising at least one row/column address signal, bank address signals, and at least one chip-select signal." Pet. 35–38; Ex. 1001, 3:18–22 (reexamination certificate). Specifically, Petitioner contends that Perego-422 teaches that control information and address information may be decoded by request and address logic 540. *Id.* at 36 (citing Ex. 1035, 13:54–59, Figs. 4B, 5B; Ex. 1003 ¶ 133). Petitioner contends a person of ordinary skill in the art would have understood that the address lines labeled RQ in Perego-422 would have conveyed row/column and bank addresses under the JEDEC standard. *Id.* at 37 (citing Ex. 1029, 6, 49; Ex. 1035, 3:67–4:3, 6:15–19, 8:1–9, 9:58–60, 10:56–59; Ex. 1032, 4.20–4.6; Ex. 1036 ¶¶ 30, 31; Ex. 1003 ¶ 134). Petitioner further contends that one of ordinary skill in the art would have understood that the logic element would need the claimed row/column, bank address, and chip-select signals to translate protocols so that the memory module can use DDR memory devices that are different than those the memory controller expected. *Id.* at 38 (citing Ex. 1035, 10:63–68; Ex. 1003 ¶¶ 135, 137–168).

Petitioner contends that Perego-422 discloses limitation [16.c.ii] reciting "the set of input signals configured to control a second number of DDR memory devices arranged in a second number of ranks, the second number of DDR memory devices smaller than the first number of DDR memory devices and the second number of ranks less than the first number of ranks." Pet. 38–51 (citing Ex. 1003 ¶¶ 137–164); Ex. 1001, 3:22–28 (reexamination certificate). Specifically, Petitioner contends that Perego-

422 discloses that the "second number of memory devices" is two memory devices arranged in "a second number of ranks" which is one rank. *Id.* at 38–39 (citing Ex. 1035, Fig. 4B). The "second number of memory devices" (two) is smaller than the "first number of memory devices" (four), and the "second number of ranks" (one) is smaller than the "first number of ranks" (two), as claim 16 requires.

Petitioner contends that Perego-422 teaches the limitation [16.c.iii] reciting "the circuit generating a set of output signals in response to the set of input signals, the set of output signals configured to control the first number of DDR memory devices arranged in the first number of ranks." Pet. 51–52 (citing Ex. 1003 ¶¶ 166–188); Ex. 1001, 3:28–31 (reexamination certificate). Petitioner contends that Perego-422 states that "[i]n a normal read operation, buffer device 350 receives control, and address information from controller 310 via point-to-point link 320a and in response, transmits corresponding signals to one or more, or all of memory devices 360." *Id.* at 51–52 (citing Ex. 1035, 6:15–19). According to Petitioner, Perego-422 further teaches that different types of memory devices may be used by utilizing the buffer to "translate protocols." *Id.* at 52 (citing Ex. 1035, 10:63–67).

Patent Owner contends that limitation [16.c.iii] of claim 16 requires multiple-device ranks. Prelim. Resp. 40–41. However, as noted above, we preliminarily disagree with this interpretation.

Petitioner contends that Perego-422 teaches the limitation [16.c.iv] reciting "wherein the circuit further responds to a command signal and the set of input signals from the computer system by selecting one or two ranks of the first number of ranks and transmitting the command signal to at least

one DDR memory device of the selected one or two ranks of the first number of ranks." Pet. 53–57 (citing Ex. 1003 ¶¶ 169–172); Ex. 1001, 3:32–37 (reexamination certificate). Petitioner contends that Perego-422 discloses selecting "one" memory device and transmitting the corresponding signals to the selected memory device. *Id.* at 53 (citing Ex. 1035, 6:15–19; Ex. 1003 ¶¶ 166–188). Petitioner contends that a person of ordinary skill in the art would have understood that a single memory device can form one rank. *Id.* (citing Ex. 1035, Fig. 4B; Ex. 1003 ¶ 170).

Petitioner has sufficiently shown that Perego-422 teaches limitations [16.c], [16.c.i]. [16.c.ii], [16.c.iii], and [16.c.iv] of claim 16.

Claim 16 recites a limitation [16.d] as "a phase-lock loop device coupled to the printed circuit board." Petitioner contends Perego-422 discloses limitation [16.d]. Pet. 57–58 (citing Ex. 1003 ¶¶ 176–179); Ex. 1001, 3:38–39 (reexamination certificate). Specifically, Petitioner contends that Perego-422 describes that buffer device 405 includes a clock circuit 570a–b which includes one or more clock alignment circuits for phase or delay adjusting internal clock signals with respect to an external clock. Pet. 57–58 (citing Ex. 1035, 12:65–13:5). Perego-422 further explains that the function of a "phase lock loop (PLL) generator device [is] to generate phase aligned clock signals for each memory device disposed on the module. *Id.* at 58 (citing Ex. 1035, 12:61–64). Petitioner contends a person of ordinary skill in the art would have understood that Perego-422's clock circuit 570a–b is a "phase-lock loop device." *Id.* (citing Ex. 1003 ¶ 177).

Claim 16 recites the limitation [16.d.i] as "the phase-lock loop device is operatively coupled to the plurality of DDR memory devices, the logic

element, and the register." Ex. 1001, 3:39–41 (reexamination certificate). Petitioner contends that Perego-422 discloses limitation [16.d.i]. Pet. 58–61 (citing Ex. 1003 ¶¶ 180–183). Specifically, Petitioner contends that the buffer device includes interfaces 520a and 520b which receive and transmit to memory devices disposed on the module. *Id.* at 59 (citing Ex. 1035, 11:48–51, Fig. 5B; Ex. 1003 ¶ 181). Petitioner further contends clock circuit 570a–b includes a "phase-lock loop device" that provides internal clock synchronizing signals to the circuit within the buffer device. *Id.* at 59–60 (citing Ex. 1035, 12:65–13:5; Ex. 1003 ¶ 181). Petitioner contends that, therefore, clock circuit 570a–b ("phase-locked loop device") is operatively coupled to the configurable width interface 590 (including the claimed "register"), request and address logic 540 (in the claimed "logic element"), and the interfaces 520 which are operatively coupled to "the DDR memory devices." *Id.* at 60 (citing Ex. 1035, Fig. 4B; Ex. 1003 ¶ 182).

Petitioner has sufficiently shown that Perego-422 teaches limitations [16.d] and [16.d.i] of claim 16.

Petitioner contends that Perego-422 discloses limitation [16.e] of claim 16 reciting "wherein the command signal is transmitted to only one DDR memory device at a time." Ex. 1001, 3:42–43 (reexamination certificate). Petitioner notes that Perego-422 discloses "[i]n a normal memory read operation, buffer device 350 receives control, and address information from controller 310 via point-to-point link 320a and in response, transmits corresponding signals to one or more, or all of memory devices 360 via channels 370." Pet. 62 (citing Ex. 1035, 6:15–19). Petitioner contends that Perego-422 directly teaches selecting "one" memory device and transmitting the corresponding signals to the selected memory device.

Id. Petitioner further contends that Perego-422 benefits from "multiple independent target subsets (i.e. more independent banks)" through reduced power and higher performance and that one of ordinary skill in the art would have understood that the command signal is not transmitted to memory devices that do not participate in the read or write transaction, consistent with the JEDEC standard. *Id.* (citing Ex. 1035, 15:31–45; Ex. 1029, 6, 49; Ex. 1003 ¶ 186).

Patent Owner argues that Petitioner has not provided any competent evidence that Perego-422 discloses limitation [16.e] of claim 16. Prelim. Resp. 41–42. Specifically, Patent Owner argues that claim 16 requires sending a command to a single device at a time even though there are multiple devices in each rank. *Id.* at 41. As discussed above in Section III.D.4, we preliminarily determine that a rank can have one device, and, therefore, we disagree with Patent Owner's argument.

Patent Owner further contends that Petitioner assumes each channel of Perego-422's Figure 4B corresponds to a rank when that is not supported by Perego-422. *Id.* at 42. Specifically, Patent Owner contends that the channels may operate in pairs or simultaneously so that a single device rank is not possible. *Id.* at 42–43 (citing Ex. 1035, 9:24–33, 10:22–36). However, Patent Owner does not address that Perego-422 states that a single channel is feasible or that more than two channels may be incorporated into the module. Ex. 1035, 10:14–17. Furthermore, Patent Owner does not address Petitioner's reliance on Perego-422 explaining that "[i]n a normal memory read operation, buffer device 350 receives control, and address information from controller 310 via point-to-point link 320a and in response, transmits corresponding signals to one or more, or all of memory devices

360 via channels 370." Pet. 62 (citing Ex. 1035, 6:15–19).

We determine that Petitioner has presented a reasonable likelihood that claim 16 of the '912 patent is unpatentable as obvious over Perego-422.

9. Obviousness Challenge to Claim 16 based on the Combination of Perego-422 and Amidi

Petitioner contends that a person of ordinary skill in the art would have been motivated to combine Perego-422 and Amidi for several reasons. Pet. 23–25. Specifically, Petitioner contends that Perego-422 and Amidi are analogous art to the '912 patent because they relate to the same field of memory modules and seek to improve performance and upgrade flexibility of memory modules. *Id*. at 23 (citing Ex. 1035, 3:13-28; Ex. 1036 ¶¶ 2, 18; Ex. 1001, 1:21–24, 5:1–5; Ex. 1003 ¶ 97). Petitioner further contends a person of ordinary skill in the art would have been motivated to implement rank multiplication functionality taught by Amidi in the memory module of Perego-422 to lower cost and increase upgrade flexibility of the memory modules. *Id.* (citing Ex. 1036 ¶ 18). Petitioner contends Perego-422 teaches that its buffer device is likewise designed for flexibility as well as backward compatibility. *Id.* (citing Ex. 1035, 6:34–43,2:26–30; Ex. 1003 ¶¶ 99, 101). Petitioner contends that Amidi's teachings on cost-effectiveness and practicality of using memory devices with low densities would have motivated a person of ordinary skill in the art to use lower-capacity memory devices in memory systems configured for higher-capacity memory devices. *Id.* at 23–24 (citing Ex. 1036 ¶ 18; Ex. 1003 ¶¶ 101, 106). Petitioner further contends a person of ordinary skill in the art would have been motivated to configure Perego-422's buffer to respond to control signals for a different type of memory device than the one implemented on its module, such as a

higher-capacity memory device, as taught by Amidi, to upgrade a system configured to handle those higher-capacity memory devices. *Id.* at 24 (citing Ex. 1035, 3:23–28; Ex. 1036 ¶ 71; Ex. 1003 ¶¶102–103).

Petitioner further contends that the combination of Perego-422 and Amidi would have been well within the skill of a person of ordinary skill in the art. Pet. 24. Specifically, Petitioner contends the two references disclose how to make a module with one type of memory device and add an interface to communicate with a memory controller configured for a different type of memory device according to relevant standards at the time. *Id.* (citing Ex. 1035, 10:17–20, 14:4–10, 17:34–35, Fig. 5D, 18:65–66; Ex. 1003 ¶ 105). Petitioner further contends that a person of ordinary skill in the art would have recognized that the combination would avoid problems like back-to-back read operations across device boundaries given Perego-422's teaching of a dedicated channel for each memory device. *Id.* (citing Ex. 1035, 10:17–20, 14:4–10, 17:34–35, Fig. 5D, 18:65–66; Ex. 1003 ¶ 105). Petitioner contends the combination "would have provided nothing more than what was expected at the time, a memory module that is built with one type of memory devices, e.g., lower-capacity memory devices, and operates in a system where the memory controller issues commands for another type of memory devices, such as higher-capacity memory devices." *Id.* at 24–25 (citing Ex. 1003 ¶ 106).

Patent Owner does not refute Petitioner's evidence of motivation to combine Perego-422 and Amidi at this time. *See* Prelim. Resp.

We determine Petitioner has sufficiently shown that a person of ordinary skill in the art would have been motivated to combine Perego-422 and Amidi with a reasonable expectation of success.

Petitioner relies on Amidi for several limitations, in the alternative, to the extent one might argue that Perego-422 alone does not disclose those limitations. *See, e.g.*, Pet. 29. For example, Petitioner further relies on Amidi as disclosing DDR memory devices in multiple ranks on a memory module (Pet. 29); a register (Pet. 35); and a phase-lock loop device (Pet. 58) among other features. Patent Owner does not dispute that Amidi teaches these features at this time. *See* Prelim. Resp.

Because we determine that Petitioner has presented a reasonable likelihood that claims 16 of the '912 patent is unpatentable over Perego-422 alone, we likewise determine that Petitioner has presented a reasonable likelihood that claim 16 is unpatentable as obvious over the combination of Perego-422 and Amidi. *See* Section III.D.8. In addition, we determine that Petitioner has presented a reasonable likelihood that claim 16 is unpatentable as obvious over the combination of Perego-422 and Amidi due to Amidi's additional teaching of claimed features together with sufficient evidence of motivation to combine with reasonable expectation of success in producing the memory module of claim 16.

10. Obviousness Challenge to Claim 16 based on Ellsberry

Petitioner further contends that Ellsberry teaches or suggests all limitations of claim 16. *Id.* at 69–111.

The preamble limitation [16.pre] of claim 16 recites "memory module connectable to a computer system." Ex. 1001, 3:9–11 (reexamination certificate). Petitioner contends that Ellsberry describes a memory module 106 with a capacity expanding device 108, connected to a computer system 100 that includes a processing unit 102 and I/O controller 104. Pet. 69 (citing Ex. 1037 ¶¶ 23, 27, Fig. 1; Ex. 1003 ¶¶ 198-199).

Petitioner sufficiently shows that the preamble limitation [16.pre] of claim 16 is taught by Ellsberry. It is thus unnecessary for us to determine whether the preamble is limiting.

Claim 16 further recites limitation [16.a] as "a printed circuit board." Ex. 1001, 3:12 (reexamination certificate). Petitioner contends that Ellsberry teaches a memory module with a printed circuit board. Pet. 72–73 (citing Ex. 1037 ¶ 2. Fig. 5).

Petitioner sufficiently shows that limitation [16.a] of claim 16 is taught by Ellsberry.

Claim 16 further recites limitation [16.b] as "a plurality of double-data-rate (DDR) memory devices coupled to the printed circuit board." Ex. 1001, 3:13–16 (reexamination certificate). Petitioner contends that Ellsberry teaches DDR and DDR 2 memory devices mounted on a circuit board. Pet. 73–74 (citing Ex. 1037 ¶¶ 3, 23, 26, 46; Ex. 1038, 4, 23; Ex. 1003 ¶¶ 209–213).

Claim 16 further recites limitation [16.b.i] as "the plurality of DDR memory devices having a first number of DDR memory devices arranged in a first number of ranks." Ex. 1001, 3:14–16 (reexamination certificate). Petitioner contends that Ellsberry teaches a memory module with two memory devices arranged in two single device ranks controlled by separate chip select signals (CS0A, CS0B). Pet. 74–76 (citing Ex. 1037 ¶¶ 3, 26, 30, 32, Fig. 12; Ex. 1003 ¶¶ 215, 218–221). Petitioner thus contends "a first number of DDR memory devices" is two and the "first number of ranks" is two. *Id.* Alternatively, Petitioner contends "a first number of DDR memory devices" is four and the "first number of ranks" is four. *Id.* at 76 (citing Ex. 1037, Fig. 13; Ex. 1003 ¶ 216).

Patent Owner contends that limitation [16.b.i] of claim 16 requires multiple-device ranks. Prelim. Resp. 40–41. As discussed above in Section III.D.4, we preliminarily determine that "rank" refers to "one or more memory devices." Thus, on this record, we disagree with Patent Owner's attempted distinction over the art.

Petitioner sufficiently shows that limitations [16.b] and [16.b.i] of claim 16 are taught by Ellsberry.

Limitation [16.c] of claim 16 recites "a circuit coupled to the printed circuit board, the circuit comprising a logic element and a register." Ex. 1001, 3:17–18 (reexamination certificate). Petitioner contends that Ellsberry teaches this limitation. Pet. 77–80 (citing Ex. 1003 ¶¶ 224–225). Specifically, Petitioner contends that Ellsberry teaches that the "circuit" is a control unit ASIC, that the "logic element" is a control block, and that the "register" corresponds to register 302. *Id.* at 77.

Petitioner contends that Ellsberry discloses limitation [16.c.i] of claim 16 reciting "the logic element receiving a set of input signals from the computer system, the set of input signals comprising at least one row/column address signal, bank address signals, and at least one chip-select signal." Pet. 75–78; Ex. 1001, 3:18–22 (reexamination certificate). Specifically, Petitioner contends that Ellsberry teaches a command processing system 300 with a control block possessing address/command decode logic 306, configuration decode logic 308, and bank switch state machine 308. *Id.* at 78–79 (citing Ex. 1037, Fig. 3). Petitioner notes that Ellsberry describes memory addresses and command information are received from DIMM interface 202, buffered in register 302, decoded in logic 304, and that a bank switch state machine 308 determines which

memory bank should be activated or accessed. *Id.* at 79 (citing Ex. 1037 ¶ 39). Petitioner contends that a person of ordinary skill in the art would have understood that Ellsberry's control block includes a "logic element" and "register" receiving row/column address signal, bank address signals, and chip-select signals. *Id.* (citing Ex. 1003 ¶ 224).

Petitioner contends that Ellsberry teaches limitation [16.c.ii] of claim 16 reciting "the set of input signals configured to control a second number of DDR memory devices arranged in a second number of ranks, the second number of DDR memory devices smaller than the first number of DDR memory devices and the second number of ranks less than the first number of ranks." Pet. 86–95 (citing Ex. 1003 ¶¶ 232–243); Ex. 1001, 3:22–28 (reexamination certificate). Specifically, Petitioner contends that Ellsberry teaches that the "set of input signals" corresponding to a single DDR2 memory device and the memory module uses two DDR2 memory devices to simulate a larger memory device. Pet. 87–88 (citing Ex. 1037, Figs. 7D, 12 [signals AC, C0]; Ex. 1003 ¶ 233). Petitioner contends that Ellsberry teaches that the "set of input signals" includes bank address, row address, and column address signals consistent with the JEDEC standard. *Id.* at 87–95 (citing Ex. 1037, Figs. 7D, 8A).

Petitioner further contends the "second number of DDR memory devices" is one, which is less than the "first number of DDR memory devices" which is two, and that the "second number of ranks" is one which is less than the "first number of ranks" which is two. *See* Ex. 1037, Fig. 12. These relations would also be satisfied for the alternative when the "first number of DDR memory devices" is four and the "first number of ranks" is four. *See* Pet. 76 (citing Ex. 1037, Fig. 13).

Petitioner contends that Ellsberry teaches the limitation [16.c.iii] of claim 16 reciting "the circuit generating a set of output signals in response to the set of input signals, the set of output signals configured to control the first number of DDR memory devices arranged in the first number of ranks." Pet. 95–99 (citing Ex. 1037, Figs. 12, 13; 1003 ¶¶ 244–246); Ex. 1001, 3:28–31 (reexamination certificate). Petitioner contends that Ellsberry teaches that "the circuit" corresponds to the Control Unit ASIC and that the "set of output signals" corresponds to Ellsberry's signals ACA, CS0A, ACB, CS0B that are responsive to the "set of input signals" corresponding to Ellsberry's signals AC, CS0. Pet. 95–96 (citing Ex. 1037, Fig. 12). Petitioner contends that Ellsberry teaches that the "circuit generat[es] the set of output signals in response to the set of input signals" because the relationship between the input signals and output signals is described in Ellsberry. *Id.* at 97–99 (citing Ex. 1037 ¶¶ 37, 42, 40, Figs. 7D, 8A; Ex. 1003 ¶¶ 232–243, 246). Petitioner further contends that "the set of output signals configured to control the first number of DDR memory devices arranged in the first number of ranks" corresponds to single device ranks 1206, 1208 corresponding to chip-select signals CS0A, CS0B. *Id.* at 95–96 (citing Ex. 1037, Fig. 12). In addition to this embodiment with two single-device ranks, Petitioner contends similar mappings apply to Ellsberry's embodiment with four-single device ranks. *Id.* (citing Ex. 1037, Fig. 13).

Patent Owner contends that limitation [16.c.iii] of claim 16 requires multiple-device ranks. Prelim. Resp. 40–41. However, as noted above, we preliminarily disagree with this interpretation.

Petitioner contends that Ellsberry teaches the limitation [16.c.iv] of

claim 16 reciting "wherein the circuit further responds to a command signal and the set of input signals from the computer system by selecting one or two ranks of the first number of ranks and transmitting the command signal to at least one DDR memory device of the selected one or two ranks of the first number of ranks." Pet. 99–103 (citing Ex. 1003 ¶¶ 248–254); Ex. 1001, 3:32–37 (reexamination certificate). Petitioner contends that the "command signal" corresponds to a read or write command under the JEDEC standard. Pet. 99 (citing Ex. 1029, 6, 49). Petitioner further contends that Ellsberry selects "one" rank and transmits the command signal to the selected "one" rank. *Id.*

Furthermore, Petitioner notes that Ellsberry states as follows:

> [t]he control unit maps a received logical address to a physical address corresponding to the particular memory bank configuration employed. It also directs commands to the memory banks to indicate which memory bank should be operational and which one should be passive (do nothing).

Id. at 100 (citing Ex. 1037 ¶ 11). Petitioner further notes that Ellsberry states that the control unit may send either the same command to both memory banks or different commands to each memory bank with a "no operation" command to the other memory bank. *Id.* at 100–101(citing Ex. 1037 ¶ 42, Fig. 8A; Ex. 1029, 48, 49; Ex. 1003 ¶¶ 229, 233–235, 249, 250). Petitioner contends this Ellsberry disclosure is similar to Example 1 of the Verilog code in the '912 patent. *Id.* at 102 (citing Ex. 1003 ¶ 251). Petitioner contends another embodiment of Ellsberry selects a target rank based on a row address bit that is bank specific, like Example 2 of the Verilog code in the '912 patent. *Id.* (citing Ex. 1003 ¶ 252).

Petitioner has sufficiently shown that Ellsberry teaches limitations

[16.c], [16.c.i]. [16.c.ii], [16.c.iii], and [16.c.iv] of claim 16.

Claim 16 recites a limitation [16.d] as "a phase-lock loop device coupled to the printed circuit board." Petitioner contends that Ellsberry teaches limitation [16.d]. Pet. 103–106 (citing Ex. 1037 ¶ 2, Figs. 12, 13; Ex. 1003 ¶¶ 255–257). Specifically, Petitioner contends that Ellsberry teaches a "phase lock loop (PLL) 238 [(yellow)] regenerates a clock signal that can be used by the components on the memory system 200." *Id.* at 104 (citing Ex. 1037 ¶ 30, Fig. 2; Ex. 1003 ¶ 256). Petitioner further contends that Ellsberry's PLL is coupled to the circuit board. Id. at 105 (citing Ex. 1037, ¶ 48, Fig. 5). Specifically, Petitioner contends that Ellsberry teaches that external phase lock loop (PLL) 514 receives a clock signal from the edge interface 506 and provides a clock signal to the memory module components. *Id.* (citing Ex. 1037, ¶¶ 39, 45, 48, 49, Figs. 2–4, 12; Ex. 1003 ¶ 257).

Claim 16 recites the limitation [16.d.i] as "the phase-lock loop device is operatively coupled to the plurality of DDR memory devices, the logic element, and the register." Ex. 1001, 3:39–41 (reexamination certificate). Petitioner contends that Ellsberry discloses limitation [16.d.i]. Pet. 106–109 (citing Ex. 1003 ¶¶ 259–263). Specifically, Petitioner contends Ellsberry's PLL receives a clock signal PCLK and generates a clock signal NCLK that is provided to the Control Unit ASIC and Switch ASIC. *Id.* at 106 (citing Ex. 1037 ¶ 30, Figs. 2–5, 12, 13; Ex. 1003 ¶¶ 255–257). Petitioner contends the Switch ASIC then uses the clock NCLK to derive the clock ECLK provided to the memory devices. *Id.* Petitioner thus contends Ellsberry's PLL is also operatively coupled to the plurality of DDR memory devices. *Id.* at 106–07 (citing Ex. 1037, Fig. 12; Ex. 1003 ¶ 260).

Petitioner contends Control Unit ASIC uses the clock signal NCLK from the PLL to derive its own local clocks that are provided to both the Control Block and register 302 in the Control Unit ASIC. Pet. 108 (citing Ex. 1037, Figs. 3, 12, 13; Ex. 1003 ¶ 261).

Petitioner contends that, to the extent Ellsberry does not sufficiently disclose a local clock of the Control Unit ASIC is provided to the register 302, a person of ordinary skill in the art would have understood that register 302 is clocked by a local clock signal as indicated by the small triangle at the bottom of the register 302. *Id.* at 108–09 (citing Ex. 1003 ¶ 262). Petitioner notes that Ellsberry states that the PLL "regenerates a clock signal that can be used by the components on the memory system 200." *Id.* at 109 (citing Ex. 1037 ¶ 30). Thus, Petitioner contends that Ellsberry's PLL provides a clock to the Control Unit ASIC, which can be used to operate its components, including the register 302, and that a person of ordinary skill in the art "would have understood and been motivated to use the local clock in the Control Unit ASIC to operate the register 302." *Id.* (citing Ex. 1003 ¶ 262).

Petitioner has sufficiently shown that Ellsberry teaches limitations [16.d] and [16.d.i] of claim 16.

Petitioner contends that Ellsberry discloses limitation [16.e] of claim 16 reciting "wherein the command signal is transmitted to only one DDR memory device at a time." Pet. 109–11 (citing Ex. 1003 ¶¶ 264–265); Ex. 1001, 3:42–43 (reexamination certificate). Specifically, Petitioner contends that Ellsberry teaches that an Activate, Write or Read command signal is transmitted to only the selected memory device and the other memory device receives a no-operation command. *Id.* at 109–11 (citing

Ex. 1037 ¶¶ 10, 33, 42, Figs. 8A, 12; Ex. 1003 ¶ 264).

Patent Owner argues that Petitioner has not provided any competent evidence that Ellsberry discloses limitation [16.e] of claim 16. Prelim. Resp. 41–42. Specifically, Patent Owner argues that claim 16 requires sending a command to a single device at a time even though there are multiple devices in each rank. *Id.* at 41. As discussed above in Section III.D.4, we preliminarily determine that a rank can have one device, and, therefore, we disagree with Patent Owner's argument.

We determine that Petitioner has shown a reasonable likelihood that claim 16 of the '912 patent is unpatentable as obvious over Ellsberry.

IV. CONCLUSION

Petitioner has carried its burden to show that it is the sole real party-in-interest in this proceeding, and that Petition is not time-barred under § 315(b) due to service of a complaint on an unnamed real party-in-interest more than one year before the filing of the Petition.

We do not deny this Petition based on an earlier *inter partes* reexamination under § 314(a) under *General Plastics*. No authority has been provided to support application of *General Plastics* in the context presented here.

We determine under the *Advanced Bionics* framework that, although Ellsberry was considered during examination of the '912 patent, Petitioner has shown that the Examiner erred by concluding that Ellsberry is not prior art to the '912 patent. Petitioner carried its initial burden to show that Ellsberry is prior art, and Patent Owner did not carry its burden of production to show that the subject matter of claim 16 of the '912 patent is

supported by its priority applications such that Ellsberry is not prior art. Accordingly, we decline to exercise our discretion to deny institution under § 325(d).

Petitioner has shown a reasonable likelihood that claim 16 would have been obvious over Perego-422, the combination of Perego-422 and Amidi, and Ellsberry. Accordingly, we institute inter partes review for claim 16 on all asserted challenges. *See SAS Institute, Inc. v. Iancu*, 138 S. Ct. 1348 (2018).

V. ORDER

For the foregoing reasons, it is

ORDERED that pursuant to 35 U.S.C. § 314(a), an *inter partes* review of claim 16 of the ’912 patent is hereby instituted on the grounds of unpatentability set forth in the Petition; and

FURTHER ORDERED that pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4, notice is hereby given of the institution of a trial; the trial will commence on the entry date of this decision.

Samsung Electronics Co., Ltd.
Ex. 1023, p. 59

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