UTILITY PATENT APPLICATION TRANSMITTAL *(Only for new nonprovisional applications under 37 CFR § 1.53(b))*	Attorney Docket No.	NL023-02US01
	First Inventor	Jefferey C. Solomon
	Title	MEMORY MODULE WITH DATA BUFFERING
	Electronically filed	August 16, 2021

APPLICATION ELEMENTS
See MPEP Chapter 600 concerning utility patent application contents.

Address to: **Commissioner for Patents**
P.O. Box 1450
Alexandria, VA 22313-1450

1. ☐ Fee Transmittal Form *(with duplicate for fee processing)*
2. ☐ Applicant claims Small Entity status, see 37 C.F.R. § 1.27
3. ☒ Specification [Total Pages 57]
4. ☒ Drawing(s) *(35 USC § 113)* [Total Sheets 23]
5. ☒ Oath or Declaration [Total Pages 1]
   a. ☐ Newly executed *(original or copy)*
   b. ☒ Copy from a prior application *(37 CFR § 1.63(d))*
6. ☒ Application Data Sheet, see 37 C.F.R. § 1.76
7. ☐ CD-ROM or CD-R in duplicate, large table or Computer Program *(Appendix)*
   ☐ Landscape Table on CD
8. ☐ Nucleotide and/or Amino Acid Sequence Submission *(if applicable, all necessary)*
   a. ☐ Computer Readable Form (CRF)
   b. ☐ Specification Sequence Listing on
      i. ☐ CD-ROM or CD-R (2 copies); or
      ii. ☐ Paper
   c. ☐ Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

9. ☐ Assignment Papers *(cover sheet & document(s))*
   Name of Assignee:
10. ☒ 37 CFR § 3.73(c) Statement
    a. ☒ Power of Attorney
11. ☐ English Translation Document *(if applicable)*
12. ☐ Information Disclosure Statement and PTO-1449
    a. ☐ Copies of citations attached
13. ☐ Preliminary Amendment
14. ☐ Return Receipt Postcard *(MPEP 503)*
15. ☐ Certified Copy of Priority Document(s) *(if foreign priority is claimed)*
16. ☐ Non-Publication Request under 35 U.S.C. § 122 (b)(2)(B)(i)
17. ☐ Other:

Note: (1) Benefit claims under 37 CFR 1.78 and foreign priority claims under 1.55 **MUST** be included in an Application Data Sheet (ADS).

(2) For applications filed under 35 U.S.C. 111, the application must contain an ADS specifying the applicant if the applicant is an assignee, person to whom the inventor is under an obligation to assign, or person who otherwise shows sufficient proprietary interest in the matter. See 37 CFR 1.46(b).

19. CORRESPONDENCE ADDRESS: Customer Number 79141

Signature	/ Jamie J. Zheng /	Date	August 16, 2021
Name (Print/Type)	Jamie J. Zheng	Registration No. (Attorney/Agent)	51,167

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	NL023-02US02
	Application Number	
Title of Invention	MEMORY MODULE WITH DATA BUFFERING	

The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76.
This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.

Secrecy Order 37 CFR 5.2:

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

Inventor Information:

Inventor 1 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Jefferey	C.	Solomon	

Residence Information (Select One) ● US Residency Non US Residency Active US Military Service

City	Irvine	State/Province	CA	Country of Residence	US

Mailing Address of Inventor:

Address 1	16 Silver Fir		
Address 2			
City	Irvine	State/Province	CA
Postal Code	92604	Country	US

Inventor 2 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Jayesh	R.	Bhakta	

Residence Information (Select One) ◉ US Residency Non US Residency Active US Military Service

City	Cerritos	State/Province	CA	Country of Residence	US

Mailing Address of Inventor:

Address 1	12220 Rose Street		
Address 2			
City	Cerritos	State/Province	CA
Postal Code	90703	Country	US

All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the **Add** button. Add

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below.
For further information see 37 CFR 1.33(a).

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	NL023-02US02
	Application Number	
Title of Invention	MEMORY MODULE WITH DATA BUFFERING	

☐ **An Address is being provided for the correspondence Information of this application.**

Customer Number	79141		
Email Address		Add Email	Remove Email

Application Information:

Title of the Invention	MEMORY MODULE WITH DATA BUFFERING		
Attorney Docket Number	NL023-02US02	**Small Entity Status Claimed**	☐
Application Type	Nonprovisional		
Subject Matter	Utility		
Total Number of Drawing Sheets (if any)	23	**Suggested Figure for Publication (if any)**	

Filing By Reference:

Only complete this section when filing an application by reference under 35 U.S.C. 111(c) and 37 CFR 1.57(a). Do not complete this section if application papers including a specification and any drawings are being filed. Any domestic benefit or foreign priority information must be provided in the appropriate section(s) below (i.e., "Domestic Benefit/National Stage Information" and "Foreign Priority Information").

For the purposes of a filing date under 37 CFR 1.53(b), the description and any drawings of the present application are replaced by this reference to the previously filed application, subject to conditions and requirements of 37 CFR 1.57(a).

Application number of the previously filed application	Filing date (YYYY-MM-DD)	Intellectual Property Authority or Country

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

☐ **Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32).
Either enter Customer Number or complete the Representative Name section below. If both sections are completed the customer Number will be used for the Representative Information during processing.

Please Select One:	● Customer Number	US Patent Practitioner	○ Limited Recognition (37 CFR 11.9)
Customer Number	79141		

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	NL023-02US02
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Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, 365(c), or 386(c) or indicate National Stage entry from a PCT application. Providing benefit claim information in the Application Data Sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78.
When referring to the current application, please leave the "Application Number" field blank.

Prior Application Status	Pending	Remove

Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
	Continuation of	16/695020	2019-11-25

Prior Application Status	Patented	Remove

Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
16/695020	Continuation of	15/857519	2017-12-28	10489314	2019-11-26

Prior Application Status	Patented	Remove

Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
15/857519	Continuation of	14/715486	2015-05-18	9858215	2018-01-02

Prior Application Status	Patented	Remove

Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
14/715486	Continuation of	13/971231	2013-08-20	9037774	2019-05-19

Prior Application Status	Patented	Remove

Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
13/971231	Continuation of	13/287081	2011-11-01	8516188	2013-08-20

Prior Application Status	Patented	Remove

Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
13/287081	Continuation of	13/032470	2011-02-22	8081536	2011-12-20

Prior Application Status	Patented	Remove

Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
13/032470	Continuation of	12/955711	2010-11-29	7916574	2011-03-29

Prior Application Status	Patented	Remove

Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
12/955711	Continuation of	12/629827	2009-12-02	781150	2011-02-01

Prior Application Status	Patented	Remove

Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
12/629827	Continuation of	12/408652	2009-03-20	7636274	2009-12-22

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	NL023-02US02
	Application Number	
Title of Invention	MEMORY MODULE WITH DATA BUFFERING	

Prior Application Status	Patented				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
12/408652	Continuation of	11/335875	2006-01-19	7532537	2009-05-12
Prior Application Status	Expired				Remove
Application Number	Continuity Type	Prior Application Number		Filing or 371(c) Date (YYYY-MM-DD)	
11/335875	Claims benefit of provisional	60/645087		2005-01-19	
Prior Application Status	Patented				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
11/335875	Continuation in part of	11/173175	2005-07-01	7289386	2007-10-30
Prior Application Status	Expired				Remove
Application Number	Continuity Type	Prior Application Number		Filing or 371(c) Date (YYYY-MM-DD)	
11/173175	Claims benefit of provisional	60/588244		2004-07-15	
Prior Application Status	Patented				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
11/173175	Continuation in part of	11/075395	2005-03-07	7286436	2007-10-23
Prior Application Status	Expired				Remove
Application Number	Continuity Type	Prior Application Number		Filing or 371(c) Date (YYYY-MM-DD)	
11/075395	Claims benefit of provisional	60/550668		2004-03-05	
Prior Application Status	Expired				Remove
Application Number	Continuity Type	Prior Application Number		Filing or 371(c) Date (YYYY-MM-DD)	
11/075395	Claims benefit of provisional	60/575595		2004-05-28	
Prior Application Status	Expired				Remove
Application Number	Continuity Type	Prior Application Number		Filing or 371(c) Date (YYYY-MM-DD)	
11/075395	Claims benefit of provisional	60/590038		2004-07-21	
Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the **Add** button.					Add

Foreign Priority Information:

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	NL023-02US02
	Application Number	
Title of Invention	MEMORY MODULE WITH DATA BUFFERING	

This section allows for the applicant to claim priority to a foreign application. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55. When priority is claimed to a foreign application that is eligible for retrieval under the priority document exchange program (PDX)[i] the information will be used by the Office to automatically attempt retrieval pursuant to 37 CFR 1.55(i)(1) and (2). Under the PDX program, applicant bears the ultimate responsibility for ensuring that a copy of the foreign application is received by the Office from the participating foreign intellectual property office, or a certified copy of the foreign priority application is filed, within the time period specified in 37 CFR 1.55(g)(1).

Remove

Application Number	Country[i]	Filing Date (YYYY-MM-DD)	Access Code[i] (if applicable)

Additional Foreign Priority Data may be generated within this form by selecting the **Add** button. Add

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications

☐ This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013.
NOTE: By providing this statement under 37 CFR 1.55 or 1.78, this application, with a filing date on or after March 16, 2013, will be examined under the first inventor to file provisions of the AIA.

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	NL023-02US02
	Application Number	
Title of Invention	MEMORY MODULE WITH DATA BUFFERING	

Authorization or Opt-Out of Authorization to Permit Access:

When this Application Data Sheet is properly signed and filed with the application, applicant has provided written authority to permit a participating foreign intellectual property (IP) office access to the instant application-as-filed (see paragraph A in subsection 1 below) and the European Patent Office (EPO) access to any search results from the instant application (see paragraph B in subsection 1 below).

Should applicant choose not to provide an authorization identified in subsection 1 below, applicant **must opt-out** of the authorization by checking the corresponding box A or B or both in subsection 2 below.

NOTE: This section of the Application Data Sheet is **ONLY** reviewed and processed with the **INITIAL** filing of an application. After the initial filing of an application, an Application Data Sheet cannot be used to provide or rescind authorization for access by a foreign IP office(s). Instead, Form PTO/SB/39 or PTO/SB/69 must be used as appropriate.

1. Authorization to Permit Access by a Foreign Intellectual Property Office(s)

A. Priority Document Exchange (PDX) - Unless box A in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the State Intellectual Property Office of the People's Republic of China (SIPO), the World Intellectual Property Organization (WIPO), and any other foreign intellectual property office participating with the USPTO in a bilateral or multilateral priority document exchange agreement in which a foreign application claiming priority to the instant patent application is filed, access to: (1) the instant patent application-as-filed and its related bibliographic data, (2) any foreign or domestic application to which priority or benefit is claimed by the instant application and its related bibliographic data, and (3) the date of filing of this Authorization. See 37 CFR 1.14(h)(1).

B. Search Results from U.S. Application to EPO - Unless box B in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the EPO access to the bibliographic data and search results from the instant patent application when a European patent application claiming priority to the instant patent application is filed. See 37 CFR 1.14(h)(2).

The applicant is reminded that the EPO's Rule 141(1) EPC (European Patent Convention) requires applicants to submit a copy of search results from the instant application without delay in a European patent application that claims priority to the instant application.

2. Opt-Out of Authorizations to Permit Access by a Foreign Intellectual Property Office(s)

☐ A. Applicant **DOES NOT** authorize the USPTO to permit a participating foreign IP office access to the instant application-as-filed. If this box is checked, the USPTO will not be providing a participating foreign IP office with any documents and information identified in subsection 1A above.

☐ B. Applicant **DOES NOT** authorize the USPTO to transmit to the EPO any search results from the instant patent application. If this box is checked, the USPTO will not be providing the EPO with search results from the instant application.

NOTE: Once the application has published or is otherwise publicly available, the USPTO may provide access to the application in accordance with 37 CFR 1.14.

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	NL023-02US02
	Application Number	
Title of Invention	MEMORY MODULE WITH DATA BUFFERING	

Applicant Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Applicant 1 Remove

If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section.

Clear

● Assignee	Legal Representative under 35 U.S.C. 117	Joint Inventor
Person to whom the inventor is obligated to assign.	Person who shows sufficient proprietary interest	

If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:

Name of the Deceased or Legally Incapacitated Inventor:

If the Applicant is an Organization check here. ☒

Organization Name	Netlist, Inc.

Mailing Address Information For Applicant:

Address 1	175 Technology		
Address 2	Suite 150		
City	Irvine	**State/Province**	CA
Country	US	Postal Code	92618
Phone Number		Fax Number	
Email Address			

Additional Applicant Data may be generated within this form by selecting the Add button. Add

Assignee Information including Non-Applicant Assignee Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	NL023-02US02
	Application Number	
Title of Invention	MEMORY MODULE WITH DATA BUFFERING	

Assignee 1

Complete this section if assignee information, including non-applicant assignee information, is desired to be included on the patent application publication. An assignee-applicant identified in the "Applicant Information" section will appear on the patent application publication as an applicant. For an assignee-applicant, complete this section only if identification as an assignee is also desired on the patent application publication.

Remove

If the Assignee or Non-Applicant Assignee is an Organization check here. ☐

Prefix	**Given Name**	Middle Name	**Family Name**	Suffix

Mailing Address Information For Assignee including Non-Applicant Assignee:

Address 1			
Address 2			
City		**State/Province**	
Country i		Postal Code	
Phone Number		Fax Number	
Email Address			

Additional Assignee or Non-Applicant Assignee Data may be generated within this form by selecting the Add button. Add

Signature:

Remove

NOTE: This Application Data Sheet must be signed in accordance with 37 CFR 1.33(b). **However, if this Application Data Sheet is submitted with the INITIAL filing of the application and either box A or B is not checked in subsection 2 of the "Authorization or Opt-Out of Authorization to Permit Access" section, then this form must also be signed in accordance with 37 CFR 1.14(c).**

This Application Data Sheet **must** be signed by a patent practitioner if one or more of the applicants is a **juristic entity** (e.g., corporation or association). If the applicant is two or more joint inventors, this form must be signed by a patent practitioner, **all** joint inventors who are the applicant, or one or more joint inventor-applicants who have been given power of attorney (e.g., see USPTO Form PTO/AIA/81) on behalf of **all** joint inventor-applicants.

See 37 CFR 1.4(d) for the manner of making signatures and certifications.

Signature	/Jamie J. Zheng/			Date (YYYY-MM-DD)	2021-08-16
First Name	Jamie J.	Last Name	Zheng	Registration Number	51167

Additional Signature may be generated within this form by selecting the Add button. Add

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Title of Invention	MEMORY MODULE WITH DATA BUFFERING	

This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1 The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3 A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent CooperationTreaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Samsung Electronics Co., Ltd.
Ex. 1059, p. 11

MEMORY MODULE WITH DATA BUFFERING

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] The present application is a continuation of U.S. Pat. Appl. No. 16/695,020, filed November 25, 2019, which is a continuation of U.S. Pat. Appl. No. 15/857,519, filed December 28, 2017, (US Pat. No. 10,489,314), which is a continuation of U.S. Pat. Appl. No. 14/715,486, filed May 18, 2015, (U.S. Pat. No. 9,858,215), which is a continuation of U.S. Pat. Appl. No. 13/971,231, filed August 20, 2013, (Pat. No. 9,037,774), which is a continuation of U.S. Pat. Appl. No. 13/287,081, filed November 1, 2011, (U.S. Pat. No. 8,516,188), which is a continuation of U.S. Pat. Appl. No. 13/032,470, filed February 22, 2011, (U.S. Pat. No. 8,081,536), which is a continuation of U.S. Pat. Appl. No. 12/955,711, filed November 29, 2010, (U.S. Pat. No. 7,916,574), which is a continuation of U.S. Pat. Appl. No. 12/629,827, filed December 2, 2009, (U.S. Pat. No. 7,881,150), which is a continuation of U.S. Pat. Appl. No. 12/408,652, filed March 20, 2009, (U.S. Pat. No. 7,636,274), which is a continuation of U.S. Pat. Appl. No. 11/335,875, filed January 19, 2006, (U.S. Pat. No. 7,532,537), which claims the benefit of U.S. Provisional Appl. No. 60/645,087, filed January 19, 2005 and which is a continuation-in-part of U.S. Pat. Appl. No. 11/173,175, filed July 1, 2005, (U.S. Pat. No. 7,289,386), which claims the benefit of U.S. Provisional Appl. No. 60/588,244, filed July 15, 2004 and which is a continuation-in-part of U.S. Pat. Appl. No. 11/075,395, filed March 7, 2005, (U.S. Pat. No. 7,286,436), which claims the benefit of U.S. Provisional Appl. No. 60/550,668, filed March 5, 2004, U.S. Provisional Appl. No. 60/575,595, filed May 28, 2004, and U.S. Provisional Appl. No. 60/590,038, filed July 21, 2004. U.S. Pat. Appl. Nos. 16/695,020, 15/857,519, 14/715,486, 13/287,081, 13/032,470, 12/955,711, 12/629,827, 12/408,652, 11/335,875, 11/173,175, and 11/075,395, and U.S. Provisional Appl. Nos. 60/550,668, 60/575,595, 60/590,038, 60/588,244, and 60/645,087, are each incorporated in its entirety by reference herein.

BACKGROUND OF THE INVENTION

1. Field of the Invention

[0002] The present invention relates generally to memory modules of a computer system, and more specifically to devices and methods for improving the performance, the memory capacity, or both, of memory modules.

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2. Description of the Related Art

[0003] Certain types of memory modules comprise a plurality of dynamic random-access memory (DRAM) devices mounted on a printed circuit board (PCB). These memory modules are typically mounted in a memory slot or socket of a computer system (e.g., a server system or a personal computer) and are accessed by the processor of the computer system. Memory modules typically have a memory configuration with a unique combination of rows, columns, and banks which result in a total memory capacity for the memory module.

[0004] For example, a 512-Megabyte memory module (termed a "512-MB" memory module, which actually has 2^{29} or 536,870,912 bytes of capacity) will typically utilize eight 512-Megabit DRAM devices (each identified as a "512-Mb" DRAM device, each actually having 2^{29} or 536,870,912 bits of capacity). The memory cells (or memory locations) of each 512-Mb DRAM device can be arranged in four banks, with each bank having an array of 2^{24} (or 16,777,216) memory locations arranged as 2^{13} rows and 2^{11} columns, and with each memory location having a width of 8 bits. Such DRAM devices with 64 M 8-bit-wide memory locations (actually with four banks of 2^{27} or 134,217,728 one-bit memory cells arranged to provide a total of 2^{26} or 67,108,864 memory locations with 8 bits each) are identified as having a "64 Mb×8" or "64 M×8-bit" configuration, or as having a depth of 64 M and a bit width of 8. Furthermore, certain commercially-available 512-MB memory modules are termed to have a "64 M×8-byte" configuration or a "64 M×64-bit" configuration with a depth of 64 M and a width of 8 bytes or 64 bits.

[0005] Similarly, a 1-Gigabyte memory module (termed a "1-GB" memory module, which actually has 2^{30} or 1,073,741,824 bytes of capacity) can utilize eight 1-Gigabit DRAM devices (each identified as a "1-Gb" DRAM device, each actually having 2^{30} or 1,073,741,824 bits of capacity). The memory locations of each 1-Gb DRAM device can be arranged in four banks, with each bank having an array of memory locations with 2^{14} rows and 2^{11} columns, and with each memory location having a width of 8 bits. Such DRAM devices with 128 M 8-bit-wide memory locations (actually with a total of 2^{27} or 134,217,728 memory locations with 8 bits each) are identified as having a "128 Mb×8" or "128 M×8-bit" configuration, or as having a depth of 128 M and a bit width of 8. Furthermore, certain commercially-available 1-GB memory modules are identified as having a "128 M×8-byte" configuration or a "128 M×64-bit" configuration with a depth of 128 M and a width of 8 bytes or 64 bits.

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[0006] The commercially-available 512-MB (64 M×8-byte) memory modules and the 1-GB (128 M×8-byte) memory modules described above are typically used in computer systems (e.g., personal computers) which perform graphics applications since such "×8" configurations are compatible with data mask capabilities often used in such graphics applications. Conversely, memory modules with "×4" configurations are typically used in computer systems such as servers which are not as graphics-intensive. Examples of such commercially available "×4" memory modules include, but are not limited to, 512-MB (128 M×4-byte) memory modules comprising eight 512-Mb (128 Mb×4) memory devices.

[0007] The DRAM devices of a memory module are generally arranged as ranks or rows of memory, each rank of memory generally having a bit width. For example, a memory module in which each rank of the memory module is 64 bits wide is described as having an "×64" organization. Similarly, a memory module having 72-bit-wide ranks is described as having an "×72" organization.

[0008] The memory capacity of a memory module increases with the number of memory devices. The number of memory devices of a memory module can be increased by increasing the number of memory devices per rank or by increasing the number of ranks. For example, a memory module with four ranks has double the memory capacity of a memory module with two ranks and four times the memory capacity of a memory module with one rank. Rather than referring to the memory capacity of the memory module, in certain circumstances, the memory density of the memory module is referred to instead.

[0009] During operation, the ranks of a memory module are selected or activated by address and command signals that are received from the processor. Examples of such address and command signals include, but are not limited to, rank-select signals, also called chip-select signals. Most computer and server systems support one-rank and two-rank memory modules. By only supporting one-rank and two-rank memory modules, the memory density that can be incorporated in each memory slot is limited.

[0010] Various aspects of the design of a memory module impose limitations on the size of the memory arrays of the memory module. Certain such aspects are particularly important for memory modules designed to operate at higher frequencies. Examples of such aspects include, but are not limited to, memory device (e.g., chip) densities, load fan-out, signal integrity, available rank selects, power dissipation, and thermal profiles.

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SUMMARY OF THE INVENTION

[0011] A memory module according to some embodiments is operable in a computer system that includes a memory controller coupled to a memory bus. The memory bus includes address and control signal lines and data signal lines. The memory module comprises a printed circuit board having a plurality of edge connections configured to be electrically coupled to a corresponding plurality of contacts of a module slot of the computer system, and logic coupled to the printed circuit board and configurable to receive input address and control signals associated with a read or write memory command via the address and control signal lines and to output registered address and control signals corresponding to the input address and control signals. The input address and control signals include a plurality of input chip select signals and other input address and control signals. The plurality of input chip select signals at least include a first input chip select signal and a second input chip select signal. In some embodiments, the first input chip select signal can have an active value while the second input chip select signal as an inactive value. The registered address and control signals include a plurality of registered chip select signals and other registered address and control signals. The plurality of registered chip select signals at least include a first registered chip select signal corresponding to the first input chip select signal and a second registered chip select signal corresponding to the second input chip select signal. In some embodiments, the first registered chip select signal can have an active value while the second registered chip select signal has an inactive value. In some embodiments, the logic is further configurable to output data transfer control signals associated with the read or write memory command.

[0012] The memory module further comprises memory devices mounted on the printed circuit board. The memory devices at least include first memory devices and second memory devices. In some embodiments, the first memory devices are configured to receive the first registered chip select signal and the other registered address and control signals, and to receive or output data signals associated with the read or write command. In some embodiments, the second memory devices are configured to receive the second registered chip select signal and the other registered address and control signals.

[0013] The memory module further comprises circuitry coupled between the memory devices and the data signal lines in the memory bus. In some embodiments, the circuitry is configurable to be in any of a plurality of states including a first state and a second

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state, and is configurable to transition from the first state to the second state in response to the data transfer control signals. In some embodiments, the circuitry in the first state is configured to disable signal communication through the circuitry. In some embodiments, the circuitry in the second state is configured to transfer the data signals associated with the read or write command via registered data transfers in accordance with a transfer time budget of the memory module. In some embodiments, the transfer time budget of the memory module includes a predetermined amount of time delay associated with the registered data transfers through the circuitry. In some embodiments, an overall CAS latency of the memory module is greater than an actual operational CAS latency of each of the memory devices by at least the predetermined amount of time delay.

[0014] In some embodiments, the memory module further comprises a phase locked loop clock driver configured to output a clock signal in response to one or more signals received from the memory controller, and the predetermined amount of time delay is at least one clock cycle time delay. In some embodiments, the memory devices are dynamic random access memory devices configured to operate synchronously with the clock signal, and wherein each memory device in the one of the plurality of ranks is configured receive or output a respective set of bits of the first burst of N-bit wide data signals on both edges of each of a respective set of data strobes.

[0015] In some embodiments, the circuitry includes data paths that are disabled when the circuitry is in the first state and enabled when the circuitry is in the second state. In some embodiments, the data paths are disabled when no data signals associated with any memory command are being transferred through the circuitry.

[0016] In some embodiments, each of the memory devices has a corresponding load, and the circuitry is configured to isolate the loads of the memory devices from the memory bus.

[0017] In some embodiments, the memory module has a specified data rate, and wherein the data signals are transferred through the data paths at the specified data rate.

BRIEF DESCRIPTION OF THE DRAWINGS

[0018] FIG. 1 schematically illustrates an example memory module in accordance with certain embodiments described herein.

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[0019] FIG. 2 schematically illustrates a circuit diagram of two memory devices of a conventional memory module.

[0020] FIGS. 3A and 3B schematically illustrate example memory modules having a circuit which selectively isolates one or both of the DQ data signal lines of the two memory devices from the computer system in accordance with certain embodiments described herein.

[0021] FIGS. 4A and 4B schematically illustrate example memory modules having a circuit which selectively isolates one or both of the DQ data signal lines of the two ranks of memory devices from the computer system in accordance with certain embodiments described herein.

[0022] FIGS. 5A-5D schematically illustrate example memory modules having a circuit comprising a logic element and one or more switches operatively coupled to the logic element in accordance with certain embodiments described herein.

[0023] FIG. 6A shows an exemplary timing diagram of a gapless read burst for a back-to-back adjacent read condition from one memory device.

[0024] FIG. 6B shows an exemplary timing diagram with an extra clock cycle between successive read commands issued to different memory devices for successive read accesses from different memory devices.

[0025] FIG. 7 shows an exemplary timing diagram in which the last data strobe of memory device “a” collides with the pre-amble time interval of the data strobe of memory device “b.”

[0026] FIGS. 8A-8D schematically illustrate circuit diagrams of example memory modules comprising a circuit which multiplexes the DQS data strobe signal lines from one another in accordance with certain embodiments described herein.

[0027] FIG. 9A schematically illustrates an example memory module with four ranks of memory devices compatible with certain embodiments described herein.

[0028] FIG. 9B schematically illustrates an example memory module with two ranks of memory devices compatible with certain embodiments described herein.

[0029] FIG. 9C schematically illustrates another example memory module in accordance with certain embodiments described herein.

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[0030] FIG. 10A schematically illustrates an exemplary memory module which doubles the rank density in accordance with certain embodiments described herein.

[0031] FIG. 10B schematically illustrates an exemplary circuit compatible with embodiments described herein.

[0032] FIG. 11A schematically illustrates an exemplary memory module which doubles number of ranks in accordance with certain embodiments described herein.

[0033] FIG. 11B schematically illustrates an exemplary circuit compatible with embodiments described herein.

[0034] FIG. 12 schematically illustrates an exemplary memory module in which a data strobe (DQS) pin of a first memory device is electrically connected to a DQS pin of a second memory device while both DQS pins are active.

[0035] FIG. 13 is an exemplary timing diagram of the voltages applied to the two DQS pins due to non-simultaneous switching.

[0036] FIG. 14 schematically illustrates another exemplary memory module in which a DQS pin of a first memory device is connected to a DQS pin of a second memory device.

[0037] FIG. 15 schematically illustrates an exemplary memory module in accordance with certain embodiments described herein.

[0038] FIGS. 16A and 16B schematically illustrate a first side and a second side, respectively, of a memory module with eighteen 64 M×4 bit, DDR-1 SDRAM FBGA memory devices on each side of a 184-pin glass-epoxy printed circuit board.

[0039] FIGS. 17A and 17B schematically illustrate an exemplary embodiment of a memory module in which a first resistor and a second resistor are used to reduce the current flow between the first DQS pin and the second DQS pin.

[0040] FIG. 18 schematically illustrates another exemplary memory module compatible with certain embodiments described herein.

[0041] FIG. 19 schematically illustrates a particular embodiment of the memory module schematically illustrated by FIG. 18.

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DETAILED DESCRIPTION OF EXAMPLE EMBODIMENTS

Load Isolation

[0042] FIG. 1 schematically illustrates an example memory module **10** compatible with certain embodiments described herein. The memory module **10** is connectable to a memory controller **20** of a computer system (not shown). The memory module **10** comprises a plurality of memory devices **30**, each memory device **30** having a corresponding load. The memory module **10** further comprises a circuit **40** electrically coupled to the plurality of memory devices **30** and configured to be electrically coupled to the memory controller **20** of the computer system. The circuit **40** selectively isolates one or more of the loads of the memory devices from the computer system. The circuit **40** comprises logic which translates between a system memory domain of the computer system and a physical memory domain of the memory module **10**.

[0043] As used herein, the term "load" is a broad term which includes, without limitation, electrical load, such as capacitive load, inductive load, or impedance load. As used herein, the term "isolation" is a broad term which includes, without limitation, electrical separation of one or more components from another component or from one another. As used herein, the term "circuit" is a broad term which includes, without limitation, an electrical component or device, or a configuration of electrical components or devices which are electrically or electromagnetically coupled together (e.g., integrated circuits), to perform specific functions.

[0044] Various types of memory modules **10** are compatible with embodiments described herein. For example, memory modules **10** having memory capacities of 512-MB, 1-GB, 2-GB, 4-GB, 8-GB, as well as other capacities, are compatible with embodiments described herein. Certain embodiments described herein are applicable to various frequencies including, but not limited to 100 MHz, 200 MHz, 400 MHz, 800 MHz, and above. In addition, memory modules **10** having widths of 4 bytes, 8 bytes, 16 bytes, 32bytes, or 32bits, 64 bits, 128 bits, 256 bits, as well as other widths (in bytes or in bits), are compatible with embodiments described herein. In certain embodiments, the memory module **10** comprises a printed circuit board on which the memory devices **30** are mounted, a plurality of edge connectors configured to be electrically coupled to a corresponding plurality of contacts of a module slot of the computer system, and a plurality of electrical conduits which electrically couple the memory

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devices **30** to the circuit **40** and which electrically couple the circuit **40** to the edge connectors. Furthermore, memory modules **10** compatible with embodiments described herein include, but are not limited to, single in-line memory modules (SIMMs), dual in-line memory modules (DIMMs), small-outline DIMMs (SO-DIMMs), unbuffered DIMMs (UDIMMs), registered DIMMs (RDIMMs), fully-buffered DIMM (FBDIMM), rank-buffered DIMMs (RBDIMMs), mini-DIMMs, and micro-DIMMs.

[0045] Memory devices **30** compatible with embodiments described herein include, but are not limited to, random-access memory (RAM), dynamic random-access memory (DRAM), synchronous DRAM (SDRAM), and double-data-rate DRAM (e.g., SDR, DDR-1, DDR-2, DDR-3). In addition, memory devices **30** having bit widths of 4, 8, 16, 32, as well as other bit widths, are compatible with embodiments described herein. Memory devices **30** compatible with embodiments described herein have packaging which include, but are not limited to, thin small-outline package (TSOP), ball-grid-array (BGA), fine-pitch BGA (FBGA), micro-BGA (μBGA), mini-BGA (mBGA), and chip-scale packaging (CSP). Memory devices **30** compatible with embodiments described herein are available from a number of sources, including but not limited to, Samsung Semiconductor, Inc. of San Jose, Calif., Infineon Technologies AG of San Jose, Calif., and Micron Technology, Inc. of Boise, Id. Persons skilled in the art can select appropriate memory devices **30** in accordance with certain embodiments described herein.

[0046] In certain embodiments, the plurality of memory devices **30** comprises a first number of memory devices **30**. In certain such embodiments, the circuit **40** selectively isolates a second number of the memory devices **30** from the computer system, with the second number less than the first number.

[0047] In certain embodiments, the plurality of memory devices **30** are arranged in a first number of ranks. For example, in certain embodiments, the memory devices **30** are arranged in two ranks, as schematically illustrated by FIG. 1. In other embodiments, the memory devices **30** are arranged in four ranks. Other numbers of ranks of the memory devices **30** are also compatible with embodiments described herein.

[0048] In certain embodiments, the circuit comprises a logic element selected from a group consisting of: a programmable-logic device (PLD), an application-specific integrated circuit (ASIC), a field-programmable gate array (FPGA), a custom-designed semiconductor

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device, and a complex programmable-logic device (CPLD). In certain embodiments, the logic element of the circuit **40** is a custom device. Sources of logic elements compatible with embodiments described herein include, but are not limited to, Lattice Semiconductor Corporation of Hillsboro, Oreg., Altera Corporation of San Jose, Calif., and Xilinx Incorporated of San Jose, Calif. In certain embodiments, the logic element comprises various discrete electrical elements, while in certain other embodiments, the logic element comprises one or more integrated circuits.

[0049] In certain embodiments, the circuit **40** further comprises one or more switches which are operatively coupled to the logic element to receive control signals from the logic element. Examples of switches compatible with certain embodiments described herein include, but are not limited to, field-effect transistor (FET) switches, such as the SN74AUC1G66 single bilateral analog switch available from Texas Instruments, Inc. of Dallas, Tex.

[0050] FIG. 2 schematically illustrates a circuit diagram of two memory devices **30a, 30b** of a conventional memory module showing the interconnections between the DQ data signal lines **102a**, **102b** of the memory devices **30a, 30b** and the DQS data strobe signal lines **104a**, **104b** of the memory devices **30a, 30b**. Each of the memory devices **30a, 30b** has a plurality of DQ data signal lines and a plurality of DQS data strobe signal lines, however, for simplicity, FIG. 2 only illustrates a single DQ data signal line and a single DQS data strobe signal line for each memory device **30a, 30b**. The DQ data signal lines **102a**, **102b** and the DQS data strobe signal lines **104a**, **104b** are typically conductive traces etched on the printed circuit board of the memory module. As shown in FIG. 2, each of the memory devices **30a, 30b** has their DQ data signal lines **102a**, **102b** electrically coupled to a common DQ line **112** and their DQS data strobe signal lines **104a**, **104b** electrically coupled to a common DQS line **114**. The common DQ line **112** and the common DQS line **114** are electrically coupled to the memory controller **20** of the computer system. Thus, the computer system is exposed to the loads of both memory devices **30a, 30b** concurrently.

[0051] In certain embodiments, the circuit **40** selectively isolates the loads of at least some of the memory devices **30** from the computer system. The circuit **40** of certain embodiments is configured to present a significantly reduced load to the computer system. In certain embodiments in which the memory devices **30** are arranged in a plurality of ranks, the

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circuit **40** selectively isolates the loads of some (e.g., one or more) of the ranks of the memory module **10** from the computer system. In certain other embodiments, the circuit **40** selectively isolates the loads of all of the ranks of the memory module **10** from the computer system. For example, when a memory module **10** is not being accessed by the computer system, the capacitive load on the memory controller **20** of the computer system by the memory module **10** can be substantially reduced to the capacitive load of the circuit **40** of the memory module **10**.

[0052] As schematically illustrated by FIGS. 3A and 3B, an example memory module **10** compatible with certain embodiments described herein comprises a circuit **40** which selectively isolates one or both of the DQ data signal lines **102a**, **102b** of the two memory devices **30a, 30b** from the common DQ data signal line **112** coupled to the computer system. Thus, the circuit **40** selectively allows a DQ data signal to be transmitted from the memory controller **20** of the computer system to one or both of the DQ data signal lines **102a**, **102b**. In addition, the circuit **40** selectively allows one of a first DQ data signal from the DQ data signal line **102a** of the first memory device **30a** or a second DQ data signal from the DQ data signal line **102b** of the second memory device **30b** to be transmitted to the memory controller **20** via the common DQ data signal line **112** (see, e.g., triangles on the DQ and DQS lines of FIGS. 3A and 3B which point towards the memory controller). While various figures of the present application denote read operations by use of DQ and DQS lines which have triangles pointing towards the memory controller, certain embodiments described herein are also compatible with write operations (e.g., as would be denoted by triangles on the DQ or DQS lines pointing away from the memory controller).

[0053] For example, in certain embodiments, the circuit **40** comprises a pair of switches **120** *a*, **120** *b* on the DQ data signal lines **102a**, **102b** as schematically illustrated by FIG. 3A. Each switch **120** *a*, **120** *b* is selectively actuated to selectively electrically couple the DQ data signal line **102a** to the common DQ signal line **112**, the DQ data signal line **102b** to the common DQ signal line **112**, or both DQ data signal lines **102a**, **102b** to the common DQ signal line **112**. In certain other embodiments, the circuit **40** comprises a switch **120** electrically coupled to both of the DQ data signal lines **102a**, **102b**, as schematically illustrated by FIG. 3B. The switch **120** is selectively actuated to selectively electrically couple the DQ data signal line **102a** to the common DQ signal line **112**, the DQ data signal line **102b** to the common DQ

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signal line **112**, or both DQ signal lines **102a**, **102b** to the common DQ signal line **112**. Circuits **40** having other configurations of switches are also compatible with embodiments described herein. While each of the memory devices **30a, 30b** has a plurality of DQ data signal lines and a plurality of DQS data strobe signal lines, FIGS. 3A and 3B only illustrate a single DQ data signal line and a single DQS data strobe signal line for each memory device **30a, 30b** for simplicity. The configurations schematically illustrated by FIGS. 3A and 3B can be applied to all of the DQ data signal lines and DQS data strobe signal lines of the memory module **10**.

[0054] In certain embodiments, the circuit **40** selectively isolates the loads of ranks of memory devices **30** from the computer system. As schematically illustrated in FIGS. 4A and 4B, example memory modules **10** compatible with certain embodiments described herein comprise a first number of memory devices **30** arranged in a first number of ranks **32**. The memory modules **10** of FIGS. 4A and 4B comprises two ranks **32a**, **32b**, with each rank **32a**, **32b** having a corresponding set of DQ data signal lines and a corresponding set of DQS data strobe lines. Other numbers of ranks (e.g., four ranks) of memory devices **30** of the memory module **10** are also compatible with certain embodiments described herein. For simplicity, FIGS. 4A and 4B illustrate only a single DQ data signal line and a single DQS data strobe signal line from each rank **32**.

[0055] The circuit **40** of FIG. 4A selectively isolates one or more of the DQ data signal lines **102a**, **102b** of the two ranks **32a**, **32b** from the computer system. Thus, the circuit **40** selectively allows a DQ data signal to be transmitted from the memory controller **20** of the computer system to the memory devices **30** of one or both of the ranks **32a**, **32b** via the DQ data signal lines **102a**, **102b**. In addition, the circuit **40** selectively allows one of a first DQ data signal from the DQ data signal line **102a** of the first rank **32a** and a second DQ data signal from the DQ data signal line **102b** of the second rank **32b** to be transmitted to the memory controller **20** via the common DQ data signal line **112**. For example, in certain embodiments, the circuit **40** comprises a pair of switches **120** *a*, **120** *b* on the DQ data signal lines **102a**, **102b** as schematically illustrated by FIG. 4A. Each switch **120** *a*, **120** *b* is selectively actuated to selectively electrically couple the DQ data signal line **102a** to the common DQ data signal line **112**, the DQ data signal line **102b** to the common DQ data signal line **112**, or both DQ data signal lines **102a**, **102b** to the common DQ data signal line **112**. In certain other embodiments, the circuit **40** comprises a switch **120** electrically coupled to both of the DQ data signal lines

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102a, **102b**, as schematically illustrated by FIG. 4B. The switch **120** is selectively actuated to selectively electrically couple the DQ data signal line **102a** to the common DQ data signal line **112**, the DQ data signal line **102b** to the common DQ data signal line **112**, or both DQ data signal lines **102a**, **102b** to the common DQ data signal line **112**. Circuits **40** having other configurations of switches are also compatible with embodiments described herein.

[0056] In the example embodiments schematically illustrated by FIGS. 3A, **3**B, **4**A, and **4**B, the circuit **40** comprises a logic element which is integral with and comprises the switches **120** which are coupled to the DQ data signal lines and the DQS data strobe signal lines. In certain such embodiments, each switch **120** comprises a data path multiplexer/demultiplexer. In certain other embodiments, the circuit **40** comprises a logic element **122** which is a separate component operatively coupled to the switches **120**, as schematically illustrated by FIGS. 5A-5D. The one or more switches **120** are operatively coupled to the logic element **122** to receive control signals from the logic element **122** and to selectively electrically couple one or more data signal lines to a common data signal line. Example switches compatible with embodiments described herein include, but are not limited to field-effect transistor (FET) switches, such as the SN74AUC1G66 single bilateral analog switch available from Texas Instruments, Inc. of Dallas, Tex. Example logic elements **122** compatible with certain embodiments described herein include, but are not limited to, programmable-logic devices (PLD), application-specific integrated circuits (ASIC), field-programmable gate arrays (FPGA), custom-designed semiconductor devices, and complex programmable-logic devices (CPLD). Example logic elements **122** are available from Lattice Semiconductor Corporation of Hillsboro, Oreg., Altera Corporation of San Jose, Calif., and Xilinx Incorporated of San Jose, Calif.

[0057] In certain embodiments, the load isolation provided by the circuit **40** advantageously allows the memory module **10** to present a reduced load (e.g., electrical load, such as capacitive load, inductive load, or impedance load) to the computer system by selectively switching between the two ranks of memory devices **30** to which it is coupled. This feature is used in certain embodiments in which the load of the memory module **10** may otherwise limit the number of ranks or the number of memory devices per memory module. In certain embodiments, the memory module **10** operates as having a data path rank buffer which advantageously isolates the ranks of memory devices **30** of the memory module **10** from one

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another, from the ranks on other memory modules, and from the computer system. This data path rank buffer of certain embodiments advantageously provides DQ-DQS paths for each rank or sets of ranks of memory devices which are separate from one another, or which are separate from the memory controller of the computer system. In certain embodiments, the load isolation advantageously diminishes the effects of capacitive loading, jitter and other sources of noise. In certain embodiments, the load isolation advantageously simplifies various other aspects of operation of the memory module **10**, including but not limited to, setup-and-hold time, clock skew, package skew, and process, temperature, voltage, and transmission line variations.

[0058] For certain memory module applications that utilize multiple ranks of memory, increased load on the memory bus can degrade speed performance. In certain embodiments described herein, selectively isolating the loads of the ranks of memory devices **30** advantageously decreases the load on the computer system, thereby allowing the computer system (e.g., server) to run faster with improved signal integrity. In certain embodiments, load isolation advantageously provides system memory with reduced electrical loading, thereby improving the electrical topology to the memory controller **20**. In certain such embodiments, the speed and the memory density of the computer system are advantageously increased without sacrificing one for the other.

[0059] In certain embodiments, load isolation advantageously increases the size of the memory array supported by the memory controller **20** of the computer system. The larger memory array has an increased number of memory devices **30** and ranks of memory devices **30** of the memory module **10**, with a corresponding increased number of chip selects. Certain embodiments described herein advantageously provide more system memory using fewer chip selects, thereby avoiding the chip select limitation of the memory controller.

[0060] An exemplary section of Verilog code corresponding to logic compatible with a circuit **40** which provides load isolation is listed below in Example 1. The exemplary code of Example 1 corresponds to a circuit **40** comprising six FET switches for providing load isolation to DQ and DQS lines.

[0061] Example 1

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```
//============================== declarations
  reg                   rasN_R, casN_R, weN_R;
  wire                  actv_cmd_R, pch_cmd_R, pch_all_cmd_R, ap_xfr_cmd_R_R;
  wire                  xfr_cmd_R,mrs_cmd,rd_cmd_R;

//- - - - - - - - - - - - - - - - - - - - - - - - DDR 2 FET
  reg                   brs0N_R;                    // registered chip sel
  reg                   brs1N_R;                    // registered chip sel
  reg                   brs2N_R;                    // registered chip sel
  reg                   brs3N_R;                    // registered chip sel
  wire                  sel;
  wire                  sel_01;
  wire                  sel_23;
  wire                  rd_R1;
  wire                  wr_cmd_R,wr_R1;
  reg                   rd_R2,rd_R3,rd_R4,rd_R5;
  reg                   wr_R2,wr_R3,wr_R4,wr_R5;
  reg                   enfet1,enfet2,enfet3,enfet4,enfet5,enfet6;
  wire                  wr_01_R1,wr_23_R1;
  reg                   wr_01_R2,wr_01_R3,wr_01_R4;
  reg                   wr_23_R2,wr_23_R3,wr_23_R4;
  wire                  rodt0_a,rodt0_b;

//============================== logic
 always @(posedge clk_in)
        begin
                brs0N_R <= brs0_in_N;    // cs0
                brs1N_R <= brs1_in_N;    // cs1
                brs2N_R <= brs2_in_N;    // cs2
                brs3N_R <= brs3_in_N;    // cs3
                rasN_R  <= brras_in_N ;
                casN_R  <= brcas_in_N ;
                weN_R   <= bwe_in_N ;
        end
assign sel = ~brs0N_R | ~brs1N_R | ~brs2N_R | ~brs3N_R ;
assign sel_01 = ~brs0N_R | ~brs1N_R ;
assign sel_23 = ~brs2N_R | ~brs3N_R ;
assign actv_cmd_R = !rasN_R & casN_R & weN_R; // activate cmd
assign pch_cmd_R = !rasN_R & casN_R & !weN_R ;// pchg cmd
assign xfr_cmd_R = rasN_R & !casN_R;                  // xfr cmd
assign mrs_cmd = !rasN_R & !casN_R & !weN_R ;   // md reg set cmd
assign rd_cmd_R = rasN_R & !casN_R & weN_R ;    // read cmd
assign wr_cmd_R = rasN_R & !casN_R & !weN_R ; // write cmd
//-------------------------------
assign    rd_R1 = sel & rd_cmd_R;  // rd cmd cyc 1
assign    wr_R1 = sel & wr_cmd_R; // wr cmd cyc 1
```


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```
//-----------------------------------------
  always @(posedge clk_in)
          begin
                    rd_R2 <= rd_R1 ;
                    rd_R3 <= rd_R2;


                  rd_R4 <= rd_R3;
                  rd_R5 <= rd_R4;
//                rd0_o_R6 <= rd0_o_R5;
                  wr_R2 <= wr_R1 ;
                  wr_R3 <= wr_R2;
                  wr_R4 <= wr_R3;
                  wr_R5 <= wr_R4;
          end
//-----------------------------------------
assign    wr_01_R1 = sel_01 & wr_cmd_R; // wr cmd cyc 1 for cs 2 & cs3
assign    wr_23_R1 = sel_23 & wr_cmd_R; // wr cmd cyc 1 for cs 2 & cs3
  always @(posedge clk_in)
          begin
                  wr_01_R2 <= wr_01_R1 ;
                  wr_01_R3 <= wr_01_R2;
                  wr_01_R4 <= wr_01_R3;
                  wr_23_R2 <= wr_23_R1 ;
                  wr_23_R3 <= wr_23_R2;
                  wr_23_R4 <= wr_23_R3;
          end
assign    rodt0_ab = (rodt0)          // odt cmd from sys
                  | (wr_23_R1)      // wr 1st cyc to other rnks (assume single dimm per channel)
                  | (wr_23_R2)      // wr 2nd cyc to other rnks (assume single dimm per channel)
                  | (wr_23_R3)      // wr 3rd cyc to other rnks (assume single dimm per channel)
                  ;
assign    rodt1_ab = (rodt1)          // odt cmd from sys
                  | (wr_01_R1)      // wr 1st cyc to other rnks (assume single dimm per channel)
                  | (wr_01_R2)      // wr 2nd cyc to other rnks (assume single dimm per channel)
                  | (wr_01_R3)      // wr 3rd cyc to other rnks (assume single dimm per channel)
                  ;
```


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```
//-----------------------------------------
 always @(posedge clk_in)
        begin
  if (
     |(rd_R2)                          // pre-am rd
     |(rd_R3)                          // 1st cyc of rd brst (cl3)
     |(rd_R4)                          // 2nd cyc of rd brst (cl3)
     |(wr_R1)                          // pre-am wr
     |(wr_R2)                          // wr brst 1st cyc
     |(wr_R3)                          // wr brst 2nd cyc
      ) begin
                  enfet1 <= 1'b1;      // enable fet
                  enfet2 <= 1'b1;      // enable fet
                  enfet3 <= 1'b1;      // enable fet
                  enfet4 <= 1'b1;      // enable fet
                  enfet5 <= 1'b1;      // enable fet
                  enfet6 <= 1'b1;      // enable fet
       end

   else
       begin
                  enfet1 <= 1'b0;      // disable fet
                  enfet2 <= 1'b0;      // disable fet
                  enfet3 <= 1'b0;      // disable fet
                  enfet4 <= 1'b0;      // disable fet
                  enfet5 <= 1'b0;      // disable fet

                  enfet6 <= 1'b0;      // disable fet
     end
end
```

Back-to-Back Adjacent Read Commands

[0062] Due to their source synchronous nature, DDR SDRAM (e.g., DDR1, DDR2, DDR3) memory devices operate with a data transfer protocol which surrounds each burst of data strobes with a pre-amble time interval and a post-amble time interval. The pre-amble time interval provides a timing window for the receiving memory device to enable its data capture circuitry when a known valid level is present on the strobe signal to avoid false triggers of the memory device's capture circuit. The post-amble time interval provides extra time after the last strobe for this data capture to facilitate good signal integrity. In certain embodiments, when the computer system accesses two consecutive bursts of data from the same memory device, termed herein as a "back-to-back adjacent read," the post-amble time interval of the first read command and the pre-amble time interval of the second read command are skipped by design protocol to increase read efficiency. FIG. 6A shows an exemplary timing diagram of this

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"gapless" read burst for a back-to-back adjacent read condition from one memory device.

[0063] In certain embodiments, when the second read command accesses data from a different memory device than does the first read command, there is at least one time interval (e.g., clock cycle) inserted between the data strobes of the two memory devices. This inserted time interval allows both read data bursts to occur without the post-amble time interval of the first read data burst colliding or otherwise interfering with the pre-amble time interval of the second read data burst. In certain embodiments, the memory controller of the computer system inserts an extra clock cycle between successive read commands issued to different memory devices, as shown in the exemplary timing diagram of FIG. 6B for successive read accesses from different memory devices.

[0064] In typical computer systems, the memory controller is informed of the memory boundaries between the ranks of memory of the memory module prior to issuing read commands to the memory module. Such memory controllers can insert wait time intervals or clock cycles to avoid collisions or interference between back-to-back adjacent read commands which cross memory device boundaries, which are referred to herein as "BBARX."

[0065] In certain embodiments described herein in which the number of ranks **32** of the memory module **10** is doubled or quadrupled, the circuit **40** generates a set of output address and command signals so that the selection decoding is transparent to the computer system. However, in certain such embodiments, there are memory device boundaries of which the computer system is unaware, so there are occasions in which BBARX occurs without the cognizance of the memory controller **20** of the computer system. As shown in FIG. 7, the last data strobe of memory device "a" collides with the pre-amble time interval of the data strobe of memory device "b," resulting in a "collision window."

[0066] FIGS. 8A-8D schematically illustrate circuit diagrams of example memory modules **10** comprising a circuit **40** which multiplexes the DQS data strobe signal lines **104a**, **104b** of two ranks **32a**, **32b** from one another in accordance with certain embodiments described herein. While the DQS data strobe signal lines **104a**, **104b** of FIGS. 8A-8D correspond to two ranks **32a**, **32b** of memory devices **30**, in certain other embodiments, the circuit **40** multiplexes the DQS data strobe signal lines **104a**, **104b** corresponding to two individual memory devices **30a, 30b**.

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[0067] FIG. 8A schematically illustrates a circuit diagram of an exemplary memory module **10** comprising a circuit **40** in accordance with certain embodiments described herein. In certain embodiments, BBARX collisions are avoided by a mechanism which electrically isolates the DQS data strobe signal lines **104a**, **104b** from one another during the transition from the first read data burst of one rank **32a** of memory devices **30** to the second read data burst of another rank **32b** of memory devices **30**.

[0068] In certain embodiments, as schematically illustrated by FIG. 8A, the circuit **40** comprises a first switch **130a** electrically coupled to a first DQS data strobe signal line **104a** of a first rank **32a** of memory devices **30** and a second switch **130b** electrically coupled to a second DQS data strobe signal line **104b** of a second rank **32b** of memory devices **30**. In certain embodiments, the time for switching the first switch **130a** and the second switch **130b** is between the two read data bursts (e.g., after the last DQS data strobe of the read data burst of the first rank **32a** and before the first DQS data strobe of the read data burst of the second rank **32b**). During the read data burst for the first rank **32a**, the first switch **130a** is enabled. After the last DQS data strobe of the first rank **32a** and before the first DQS data strobe of the second rank **32b**, the first switch **130a** is disabled and the second switch **130b** is enabled.

[0069] As shown in FIG. 8A, each of the ranks **32a**, **32b** otherwise involved in a BBARX collision have their DQS data strobe signal lines **104a**, **104b** selectively electrically coupled to the common DQS line **114** through the circuit **40**. The circuit **40** of certain embodiments multiplexes the DQS data strobe signal lines **104a**, **104b** of the two ranks **32a**, **32b** of memory devices **30** from one another to avoid a BBARX collision.

[0070] In certain embodiments, as schematically illustrated by FIG. 8B, the circuit **40** comprises a switch **130** which multiplexes the DQS data strobe signal lines **104a**, **104b** from one another. For example, the circuit **40** receives a DQS data strobe signal from the common DQS data strobe signal line **114** and selectively transmits the DQS data strobe signal to the first DQS data strobe signal line **104a**, to the second DQS data strobe signal line **104b**, or to both DQS data strobe signal lines **104a**, **104b**. As another example, the circuit **40** receives a first DQS data strobe signal from the first rank **32a** of memory devices **30** and a second DQS data strobe signal from a second rank **32b** of memory devices **30** and selectively switches one of the first and second DQS data strobe signals to the common DQS data strobe signal line **114**.

[0071] In certain embodiments, the circuit **40** also provides the load isolation

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described above in reference to FIGS. 1-5. For example, as schematically illustrated by FIG. 8C, the circuit **40** comprises both the switch **120** for the DQ data signal lines **102a**, **102b** and the switch **130** for the DQS data strobe signal lines **104a**, **104b**. While in certain embodiments, the switches **130** are integral with a logic element of the circuit **40**, in certain other embodiments, the switches **130** are separate components which are operatively coupled to a logic element **122** of the circuit **40**, as schematically illustrated by FIG. 8D. In certain such embodiments, the control and timing of the switch **130** is performed by the circuit **40** which is resident on the memory module **10**. Example switches **130** compatible with embodiments described herein include, but are not limited to field-effect transistor (FET) switches, such as the SN74AUC1G66 single bilateral analog switch available from Texas Instruments, Inc. of Dallas, Tex., and multiplexers, such as the SN74AUC2G53 2:1 analog multiplexer/demultiplexer available from Texas Instruments, Inc. of Dallas, Tex.

[0072] The circuit **40** of certain embodiments controls the isolation of the DQS data strobe signal lines **104a**, **104b** by monitoring commands received by the memory module **10** from the computer system and producing "windows" of operation whereby the appropriate switches **130** are activated or deactivated to enable and disable the DQS data strobe signal lines **104a**, **104b** to mitigate BBARX collisions. In certain other embodiments, the circuit **40** monitors the commands received by the memory module **10** from the computer system and selectively activates or deactivates the switches **120** to enable and disable the DQ data signal lines **102a**, **102b** to reduce the load of the memory module **10** on the computer system. In still other embodiments, the circuit **40** performs both of these functions together.

Command Signal Translation

[0073] Most high-density memory modules are currently built with 512-Megabit ("512-Mb") memory devices wherein each memory device has a 64 M×8-bit configuration. For example, a 1-Gigabyte ("1-GB") memory module with error checking capabilities can be fabricated using eighteen such 512-Mb memory devices. Alternatively, it can be economically advantageous to fabricate a 1-GB memory module using lower-density memory devices and doubling the number of memory devices used to produce the desired word width. For example, by fabricating a 1-GB memory module using thirty-six 256-Mb memory devices with 64 M×4-bit configuration, the cost of the resulting 1-GB memory module can be reduced since the unit cost of each 256-Mb memory device is typically lower than one-half the unit cost of each 512-

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Mb memory device. The cost savings can be significant, even though twice as many 256-Mb memory devices are used in place of the 512-Mb memory devices. For example, by using pairs of 512-Mb memory devices rather than single 1-Gb memory devices, certain embodiments described herein reduce the cost of the memory module by a factor of up to approximately five.

[0074] Market pricing factors for DRAM devices are such that higher-density DRAM devices (e.g., 1-Gb DRAM devices) are much more than twice the price of lower-density DRAM devices (e.g., 512-Mb DRAM devices). In other words, the price per bit ratio of the higher-density DRAM devices is greater than that of the lower-density DRAM devices. This pricing difference often lasts for months or even years after the introduction of the higher-density DRAM devices, until volume production factors reduce the costs of the newer higher-density DRAM devices. Thus, when the cost of a higher-density DRAM device is more than the cost of two lower-density DRAM devices, there is an economic incentive for utilizing pairs of the lower-density DRAM devices to replace individual higher-density DRAM devices.

[0075] FIG. 9A schematically illustrates an exemplary memory module **10** compatible with certain embodiments described herein. The memory module **10** is connectable to a memory controller **20** of a computer system (not shown). The memory module **10** comprises a printed circuit board **210** and a plurality of memory devices **30** coupled to the printed circuit board **210**. The plurality of memory devices **30** has a first number of memory devices **30**. The memory module **10** further comprises a circuit **40** coupled to the printed circuit board **210**. The circuit **40** receives a set of input address and command signals from the computer system. The set of input address and command signals correspond to a second number of memory devices **30** smaller than the first number of memory devices **30**. The circuit **40** generates a set of output address and command signals in response to the set of input address and command signals. The set of output address and command signals corresponds to the first number of memory devices **30**.

[0076] In certain embodiments, as schematically illustrated in FIG. 9A, the memory module **10** further comprises a phase-lock loop device **220** coupled to the printed circuit board **210** and a register **230** coupled to the printed circuit board **210**. In certain embodiments, the phase-lock loop device **220** and the register **230** are each mounted on the printed circuit board **210**. In response to signals received from the computer system, the phase-lock loop device **220** transmits clock signals to the plurality of memory devices **30**, the circuit

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40, and the register **230**. The register **230** receives and buffers a plurality of command signals and address signals (e.g., bank address signals, row address signals, column address signals, gated column address strobe signals, chip-select signals), and transmits corresponding signals to the appropriate memory devices **30**. In certain embodiments, the register **230** comprises a plurality of register devices. While the phase-lock loop device **220**, the register **230**, and the circuit **40** are described herein in certain embodiments as being separate components, in certain other embodiments, two or more of the phase-lock loop device **220**, the register **230**, and the circuit **40** are portions of a single component. Persons skilled in the art are able to select a phase-lock loop device **220** and a register **230** compatible with embodiments described herein.

[0077] In certain embodiments, the memory module **10** further comprises electrical components which are electrically coupled to one another and are surface-mounted or embedded on the printed circuit board **210**. These electrical components can include, but are not limited to, electrical conduits, resistors, capacitors, inductors, and transistors. In certain embodiments, at least some of these electrical components are discrete, while in other certain embodiments, at least some of these electrical components are constituents of one or more integrated circuits.

[0078] In certain embodiments, the printed circuit board **210** is mountable in a module slot of the computer system. The printed circuit board **210** of certain such embodiments has a plurality of edge connections electrically coupled to corresponding contacts of the module slot and to the various components of the memory module **10**, thereby providing electrical connections between the computer system and the components of the memory module **10**.

[0079] In certain embodiments, the plurality of memory devices **30** are arranged in a first number of ranks **32**. For example, in certain embodiments, the memory devices **30** are arranged in four ranks **32a**, **32b**, **32** *c*, **32** *d*, as schematically illustrated by FIG. 9A. In certain other embodiments, the memory devices **30** are arranged in two ranks **32a**, **32b**, as schematically illustrated by FIG. 9B. Other numbers of ranks **32** of the memory devices **30** are also compatible with embodiments described herein.

[0080] As schematically illustrated by FIGS. 9A and 9B, in certain embodiments, the circuit **40** receives a set of input command signals (e.g., refresh, precharge) and address signals (e.g., bank address signals, row address signals, column address signals, gated column

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address strobe signals, chip-select signals) from the memory controller **20** of the computer system. In response to the set of input address and command signals, the circuit **40** generates a set of output address and command signals.

[0081] In certain embodiments, the set of output address and command signals corresponds to a first number of ranks in which the plurality of memory devices **30** of the memory module **10** are arranged, and the set of input address and command signals corresponds to a second number of ranks per memory module for which the computer system is configured. The second number of ranks in certain embodiments is smaller than the first number of ranks. For example, in the exemplary embodiment as schematically illustrated by FIG. 9A, the first number of ranks is four while the second number of ranks is two. In the exemplary embodiment of FIG. 9B, the first number of ranks is two while the second number of ranks is one. Thus, in certain embodiments, even though the memory module **10** actually has the first number of ranks of memory devices **30**, the memory module **10** simulates a virtual memory module by operating as having the second number of ranks of memory devices **30**. In certain embodiments, the memory module **10** simulates a virtual memory module when the number of memory devices **30** of the memory module **10** is larger than the number of memory devices **30** per memory module for which the computer system is configured to utilize. In certain embodiments, the circuit **40** comprises logic (e.g., address decoding logic, command decoding logic) which translates between a system memory domain of the computer system and a physical memory domain of the memory module **10**.

[0082] In certain embodiments, the computer system is configured for a number of ranks per memory module which is smaller than the number of ranks in which the memory devices **30** of the memory module **10** are arranged. In certain such embodiments, the computer system is configured for two ranks of memory per memory module (providing two chip-select signals CS_0, CS_1) and the plurality of memory modules **30** of the memory module **10** are arranged in four ranks, as schematically illustrated by FIG. 9A. In certain other such embodiments, the computer system is configured for one rank of memory per memory module (providing one chip-select signal CS_0) and the plurality of memory modules **30** of the memory module **10** are arranged in two ranks, as schematically illustrated by FIG. 9B.

[0083] In the exemplary embodiment schematically illustrated by FIG. 9A, the memory module **10** has four ranks of memory devices **30** and the computer system is

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configured for two ranks of memory devices per memory module. The memory module **10** receives row/column address signals or signal bits (A_0-A_{n+1}), bank address signals (BA_0-BA_m), chip-select signals (CS_0 and CS_1), and command signals (e.g., refresh, precharge, etc.) from the computer system. The A_0-A_n row/column address signals are received by the register **230**, which buffers these address signals and sends these address signals to the appropriate ranks of memory devices **30**. The circuit **40** receives the two chip-select signals (CS_0, CS_1) and one row/column address signal (A_{n+1}) from the computer system. Both the circuit **40** and the register **230** receive the bank address signals (BA_0-BA_m) and at least one command signal (e.g., refresh, precharge, etc.) from the computer system.

Logic Tables

[0084] Table 1 provides a logic table compatible with certain embodiments described herein for the selection among ranks of memory devices **30** using chip-select signals.

TABLE 1

State	CS_0	CS_1	A_{n+1}	Command	CS_{0A}	CS_{0B}	CS_{1A}	CS_{1B}
1	0	1	0	Active	0	1	1	1
2	0	1	1	Active	1	0	1	1
3	0	1	x	Active	0	0	1	1
4	1	0	0	Active	1	1	0	1
5	1	0	1	Active	1	1	1	0
6	1	0	x	Active	1	1	0	0
7	1	1	x	x	1	1	1	1

Note:

1. CS_0, CS_1, CS_{0A}, CS_{0B}, CS_{1A}, and CS_{1B} are active low signals.
2. A_{n+1} is an active high signal.
3. 'x' is a Don't Care condition.
4. Command involves a number of command signals that define operations such as refresh, precharge, and other operations.

[0085] In Logic State 1: CS_0 is active low, A_{n+1} is non-active, and Command is active. CS_{0A} is pulled low, thereby selecting Rank **0**.

[0086] In Logic State 2: CS_0 is active low, A_{n+1} is active, and Command is active. CS_{0B} is pulled low, thereby selecting Rank **1**.

[0087] In Logic State 3: CS_0 is active low, A_{n+1} is Don't Care, and Command is active high. CS_{0A} and CS_{0B} are pulled low, thereby selecting Ranks **0** and **1**.

[0088] In Logic State 4: CS_1 is active low, A_{n+1} is non-active, and Command is

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active. CS_{1A} is pulled low, thereby selecting Rank **2**.

[0089] In Logic State 5: CS_1 is active low, A_{n+1} is active, and Command is active. CS_1B is pulled low, thereby selecting Rank **3**.

[0090] In Logic State 6: CS_1 is active low, A_{n+1} is Don't Care, and Command is active. CS_{1A} and CS_1B are pulled low, thereby selecting Ranks **2** and **3**.

[0091] In Logic State 7: CS_0 and CS_1 are pulled non-active high, which deselects all ranks, i.e., CS_{0A}, CS_{0B}, CS_{1A}, and CS_{1B} are pulled high.

[0092] The "Command" column of Table 1 represents the various commands that a memory device (e.g., a DRAM device) can execute, examples of which include, but are not limited to, activation, read, write, precharge, and refresh. In certain embodiments, the command signal is passed through to the selected rank only (e.g., state 4 of Table 1). In such embodiments, the command signal (e.g., read) is sent to only one memory device or the other memory device so that data is supplied from one memory device at a time. In other embodiments, the command signal is passed through to both associated ranks (e.g., state 6 of Table 1). In such embodiments, the command signal (e.g., refresh) is sent to both memory devices to ensure that the memory content of the memory devices remains valid over time. Certain embodiments utilize a logic table such as that of Table 1 to simulate a single memory device from two memory devices by selecting two ranks concurrently.

[0093] Table 2 provides a logic table compatible with certain embodiments described herein for the selection among ranks of memory devices **30** using gated CAS signals.

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TABLE 2

CS*	RAS*	CAS*	WE*	Density Bit	A_{10}	Command	CAS0*	CAS1*
1	x	x	x	x	x	NOP	x	x
0	1	1	1	x	x	NOP	1	1
0	0	1	1	0	x	ACTIVATE	1	1
0	0	1	1	1	x	ACTIVATE	1	1
0	1	0	1	0	x	READ	0	1
0	1	0	1	1	x	READ	1	0
0	1	0	0	0	x	WRITE	0	1
0	1	0	0	1	x	WRITE	1	0
0	0	1	0	0	0	PRE-CHARGE	1	1
0	0	1	0	1	0	PRE-CHARGE	1	1
0	0	1	0	x	1	PRE-CHARGE	1	1
0	0	0	0	x	x	MODE REG SET	0	0
0	0	0	1	x	x	REFRESH	0	0

[0094] In certain embodiments in which the density bit is a row address bit, for read/write commands, the density bit is the value latched during the activate command for the selected bank.

Serial-Presence-Detect Device

[0095] Memory modules typically include a serial-presence detect (SPD) device **240** (e.g., an electrically-erasable-programmable read-only memory or EEPROM device) comprising data which characterize various attributes of the memory module, including but not limited to, the number of row addresses the number of column addresses, the data width of the memory devices, the number of ranks, the memory density per rank, the number of memory devices, and the memory density per memory device. The SPD device **240** communicates this data to the basic input/output system (BIOS) of the computer system so that the computer system is informed of the memory capacity and the memory configuration available for use and can configure the memory controller properly for maximum reliability and performance.

[0096] For example, for a commercially-available 512-MB (64 M×8-byte) memory module utilizing eight 512-Mb memory devices each with a 64 M×8-bit configuration, the SPD device contains the following SPD data (in appropriate bit fields of these bytes):

Byte **3**: Defines the number of row address bits in the DRAM device in the memory module [13 for the 512-Mb memory device].

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Byte **4**: Defines the number of column address bits in the DRAM device in the memory module [11 for the 512-Mb memory device].

Byte **13**: Defines the bit width of the primary DRAM device used in the memory module [8 bits for the 512-Mb (64 M×8-bit) memory device].

Byte **14**: Defines the bit width of the error checking DRAM device used in the memory module [8 bits for the 512-Mb (64 M×8-bit) memory device].

Byte **17**: Defines the number of banks internal to the DRAM device used in the memory module [4 for the 512-Mb memory device].

[0097] In a further example, for a commercially-available 1-GB (128 M×8-byte) memory module utilizing eight 1-Gb memory devices each with a 128 M×8-bit configuration, as described above, the SPD device contains the following SPD data (in appropriate bit fields of these bytes):

Byte **3**: Defines the number of row address bits in the DRAM device in the memory module [14 for the 1-Gb memory device].

Byte **4**: Defines the number of column address bits in the DRAM device in the memory module [11 for the 1-Gb memory device].

Byte **13**: Defines the bit width of the primary DRAM device used in the memory module [8 bits for the 1-Gb (128 M×8-bit) memory device].

Byte **14**: Defines the bit width of the error checking DRAM device used in the memory module [8 bits for the 1-Gb (128 M×8-bit) memory device].

Byte **17**: Defines the number of banks internal to the DRAM device used in the memory module [4 for the 1-Gb memory device].

[0098] In certain embodiments, the SPD device **240** comprises data which characterize the memory module **10** as having fewer ranks of memory devices than the memory module **10** actually has, with each of these ranks having more memory density. For example, for a memory module **10** compatible with certain embodiments described herein having two ranks of memory devices **30**, the SPD device **240** comprises data which characterizes the memory module **10** as having one rank of memory devices with twice the memory density per rank. Similarly, for a memory module **10** compatible with certain embodiments described herein having four ranks of memory devices **30**, the SPD device **240** comprises data which characterizes the memory module **10** as having two ranks of memory devices with twice the

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memory density per rank. In addition, in certain embodiments, the SPD device **240** comprises data which characterize the memory module **10** as having fewer memory devices than the memory module **10** actually has, with each of these memory devices having more memory density per memory device. For example, for a memory module **10** compatible with certain embodiments described herein, the SPD device **240** comprises data which characterizes the memory module **10** as having one-half the number of memory devices that the memory module **10** actually has, with each of these memory devices having twice the memory density per memory device. Thus, in certain embodiments, the SPD device **240** informs the computer system of the larger memory array by reporting a memory device density that is a multiple of the memory devices **30** resident on the memory module **10**. Certain embodiments described herein advantageously do not require system level changes to hardware (e.g., the motherboard of the computer system) or to software (e.g., the BIOS of the computer system).

[0099] FIG. 9C schematically illustrates an exemplary memory module **10** in accordance with certain embodiments described herein. The memory module **10** comprises a pair of substantially identical memory devices **31**, **33**. Each memory device **31**, **33** has a first bit width, a first number of banks of memory locations, a first number of rows of memory locations, and a first number of columns of memory locations. The memory module **10** further comprises an SPD device **240** comprising data that characterizes the pair of memory devices **31**, **33**. The data characterize the pair of memory devices **31**, **33** as a virtual memory device having a second bit width equal to twice the first bit width, a second number of banks of memory locations equal to the first number of banks, a second number of rows of memory locations equal to the first number of rows, and a second number of columns of memory locations equal to the first number of columns.

[00100] In certain such embodiments, the SPD device **240** of the memory module **10** is programmed to describe the combined pair of lower-density memory devices **31**, **33** as one virtual or pseudo-higher-density memory device. In an exemplary embodiment, two 512-Mb memory devices, each with a 128 M×4-bit configuration, are used to simulate one 1-Gb memory device having a 128 M×8-bit configuration. The SPD device **240** of the memory module **10** is programmed to describe the pair of 512-Mb memory devices as one virtual or pseudo-1-Gb memory device.

[00101] For example, to fabricate a 1-GB (128 M×8-byte) memory module, sixteen

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512-Mb (128 M×4-bit) memory devices can be used. The sixteen 512-Mb (128 M×4-bit) memory devices are combined in eight pairs, with each pair serving as a virtual or pseudo-1-Gb (128 M×8-bit) memory device. In certain such embodiments, the SPD device **240** contains the following SPD data (in appropriate bit fields of these bytes):

Byte 3: 13 row address bits.

Byte 4: 12 column address bits.

Byte 13: 8 bits wide for the primary virtual 1-Gb (128 M×8-bit) memory device.

Byte 14: 8 bits wide for the error checking virtual 1-Gb (128 M×8-bit) memory device.

Byte 17: 4 banks.

[00102] In this exemplary embodiment, bytes **3**, **4**, and **17** are programmed to have the same values as they would have for a 512-MB (128 M×4-byte) memory module utilizing 512-Mb (128 M×4-bit) memory devices. However, bytes **13** and **14** of the SPD data are programmed to be equal to 8, corresponding to the bit width of the virtual or pseudo-higher-density 1-Gb (128 M×8-bit) memory device, for a total capacity of 1-GB. Thus, the SPD data does not describe the actual-lower-density memory devices, but instead describes the virtual or pseudo-higher-density memory devices. The BIOS accesses the SPD data and recognizes the memory module as having 4 banks of memory locations arranged in 2^{13} rows and 2^{12} columns, with each memory location having a width of 8 bits rather than 4 bits.

[00103] In certain embodiments, when such a memory module **10** is inserted in a computer system, the computer system's memory controller then provides to the memory module **10** a set of input address and command signals which correspond to the number of ranks or the number of memory devices reported by the SPD device **240**. For example, placing a two-rank memory module **10** compatible with certain embodiments described herein in a computer system compatible with one-rank memory modules, the SPD device **240** reports to the computer system that the memory module **10** only has one rank. The circuit **40** then receives a set of input address and command signals corresponding to a single rank from the computer system's memory controller, and generates and transmits a set of output address and command signals corresponding to two ranks to the appropriate memory devices **30** of the memory module **10**.

[00104] Similarly, when a two-rank memory module **10** compatible with certain embodiments described herein is placed in a computer system compatible with either one- or

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two-rank memory modules, the SPD device **240** reports to the computer system that the memory module **10** only has one rank. The circuit **40** then receives a set of input address and command signals corresponding to a single rank from the computer system's memory controller, and generates and transmits a set of output address and command signals corresponding to two ranks to the appropriate memory devices **30** of the memory module **10**.

[00105] Furthermore, a four-rank memory module **10** compatible with certain embodiments described herein simulates a two-rank memory module whether the memory module **10** is inserted in a computer system compatible with two-rank memory modules or with two- or four-rank memory modules. Thus, by placing a four-rank memory module **10** compatible with certain embodiments described herein in a module slot that is four-rank-ready, the computer system provides four chip-select signals, but the memory module **10** only uses two of the chip-select signals.

[00106] In certain embodiments, the circuit **40** comprises the SPD device **240** which reports the CAS latency (CL) to the memory controller of the computer system. The SPD device **240** of certain embodiments reports a CL which has one more cycle than does the actual operational CL of the memory array. In certain embodiments, data transfers between the memory controller and the memory module are registered for one additional clock cycle by the circuit **40**. The additional clock cycle of certain embodiments is added to the transfer time budget with an incremental overall CAS latency. This extra cycle of time in certain embodiments advantageously provides sufficient time budget to add a buffer which electrically isolates the ranks of memory devices **30** from the memory controller **20**. The buffer of certain embodiments comprises combinatorial logic, registers, and logic pipelines. In certain embodiments, the buffer adds a one-clock cycle time delay, which is equivalent to a registered DIMM, to accomplish the address decoding. The one-cycle time delay of certain such embodiments provides sufficient time for read and write data transfers to provide the functions of the data path multiplexer/demultiplexer. Thus, for example, a DDR2 400-MHz memory system in accordance with embodiments described herein has an overall CAS latency of four, and uses memory devices with a CAS latency of three. In still other embodiments, the SPD device **240** does not utilize this extra cycle of time.

Memory Density Multiplication

[00107] In certain embodiments, two memory devices having a memory density are

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used to simulate a single memory device having twice the memory density, and an additional address signal bit is used to access the additional memory. Similarly, in certain embodiments, two ranks of memory devices having a memory density are used to simulate a single rank of memory devices having twice the memory density, and an additional address signal bit is used to access the additional memory. As used herein, such simulations of memory devices or ranks of memory devices are termed as "memory density multiplication," and the term "density transition bit" is used to refer to the additional address signal bit which is used to access the additional memory by selecting which rank of memory devices is enabled for a read or write transfer operation.

[00108] For example, for computer systems which are normally limited to using memory modules which have a single rank of 128 M×4-bit memory devices, certain embodiments described herein enable the computer system to utilize memory modules which have double the memory (e.g., two ranks of 128 M×4-bit memory devices). The circuit **40** of certain such embodiments provides the logic (e.g., command and address decoding logic) to double the number of chip selects, and the SPD device **240** reports a memory device density of 256 M×4-bit to the computer system.

[00109] In certain embodiments utilizing memory density multiplication embodiments, the memory module **10** can have various types of memory devices **30** (e.g., DDR1, DDR2, DDR3, and beyond). The circuit **40** of certain such embodiments utilizes implied translation logic equations having variations depending on whether the density transition bit is a row, column, or internal bank address bit. In addition, the translation logic equations of certain embodiments vary depending on the type of memory module **10** (e.g., UDIMM, RDIMM, FBDIMM, etc.). Furthermore, in certain embodiments, the translation logic equations vary depending on whether the implementation multiplies memory devices per rank or multiplies the number of ranks per memory module.

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TABLE 3A

	128-Mb	256-Mb	512-Mb	1-Gb
Number of banks	4	4	4	4
Number of row address bits	12	13	13	14
Number of column address bits for "x 4" configuration	11	11	12	12
Number of column address bits for "x 8" configuration	10	10	11	11
Number of column address bits for "x 16" configuration	9	9	10	10

[00110] Table 3A provides the numbers of rows and columns for DDR-1 memory devices, as specified by JEDEC standard JESD79D, "Double Data Rate (DDR) SDRAM Specification," published February 2004, and incorporated in its entirety by reference herein.

[00111] As described by Table 3A, 512-Mb (128 M×4-bit) DRAM devices have 2^{13} rows and 2^{12} columns of memory locations, while 1-Gb (128 M×8-bit) DRAM devices have 2^{14} rows and 2^{11} columns of memory locations. Because of the differences in the number of rows and the number of columns for the two types of memory devices, complex address translation procedures and structures would typically be needed to fabricate a 1-GB (128 M×8-byte) memory module using sixteen 512-Mb (128 M×4-bit) DRAM devices.

[00112] Table 3B shows the device configurations as a function of memory density for DDR2 memory devices.

TABLE 3B

	Number of Rows	Number of Columns	Number of Internal Banks	Page Size (x4s or x8s)
256 Mb	13	11	4	1 KB
512 Mb	14	11	4	1 KB
1 Gb	14	11	8	1 KB
2 Gb	15	11	8	1 KB
4 Gb	16	11	8	1 KB

Table 4 lists the corresponding density transition bit for the density transitions between the DDR2 memory densities of Table 3B.

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TABLE 4

Density Transition	Density Transition Bit
256 Mb to 512 Mb	A_{13}
512 Mb to 1 Gb	BA_2
1 Gb to 2 Gb	A_{14}
2 Gb to 4 Gb	A_{15}

Other certain embodiments described herein utilize a transition bit to provide a transition from pairs of physical 4-Gb memory devices to simulated 8-Gb memory devices.

[00113] In an example embodiment, the memory module comprises one or more pairs of 256-Mb memory devices, with each pair simulating a single 512-Mb memory device. The simulated 512-Mb memory device has four internal banks while each of the two 256-Mb memory devices has four internal banks, for a total of eight internal banks for the pair of 256-Mb memory devices. In certain embodiments, the additional row address bit is translated by the circuit **40** to the rank selection between each of the two 256-Mb memory devices of the pair. Although there are eight total internal banks in the rank-converted memory array, the computer system is only aware of four internal banks. When the memory controller activates a row for a selected bank, the circuit **40** activates the same row for the same bank, but it does so for the selected rank according to the logic state of the additional row address bit A_{13}.

[00114] In another example embodiment, the memory module comprises one or more pairs of 512-Mb memory devices, with each pair simulating a single 1-Gb memory device. The simulated 1-Gb memory device has eight internal banks while each of the two 512-Mb memory devices has four internal banks, for a total of eight internal banks for the pair of 512-Mb memory devices. In certain embodiments, the mapped BA_2 (bank **2**) bit is used to select between the two ranks of 512-Mb memory devices to preserve the internal bank geometry expected by the memory controller of the computer system. The state of the BA_2 bit selects the upper or lower set of four banks, as well as the upper and lower 512-Mb rank.

[00115] In another example embodiment, the memory module comprises one or more pairs of 1-Gb memory devices, with each pair simulating a single 2-Gb memory device. Each of the two 1-Gb memory devices has eight internal banks for a total of sixteen internal banks, while the simulated 2-Gb memory device has eight internal banks. In certain embodiments, the additional row address bit translates to the rank selection between the two

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1-Gb memory devices. Although there are sixteen total internal banks per pair of 1-Gb memory devices in the rank-converted memory array, the memory controller of the computer system is only aware of eight internal banks. When the memory controller activates a row of a selected bank, the circuit **40** activates the same row for the same bank, but is does so for the selected rank according to the logic state of the additional row address bit A_{14}.

[00116] The circuit **40** of certain embodiments provides substantially all of the translation logic used for the decoding (e.g., command and address decoding). In certain such embodiments, there is a fully transparent operational conversion from the "system memory" density domain of the computer system to the "physical memory" density domain of the memory module **10**. In certain embodiments, the logic translation equations are programmed in the circuit **40** by hardware, while in certain other embodiments, the logic translation equations are programmed in the circuit **40** by software. Examples 1 and 2 provide exemplary sections of Verilog code compatible with certain embodiments described herein. As described more fully below, the code of Examples 1 and 2 includes logic to reduce potential problems due to "back-to-back adjacent read commands which cross memory device boundaries or "BBARX." Persons skilled in the art are able to provide additional logic translation equations compatible with embodiments described herein.

[00117] An exemplary section of Verilog code compatible with memory density multiplication from 512 Mb to 1 Gb using DDR2 memory devices with the BA_2 density transition bit is listed below in Example 2. The exemplary code of Example 2 corresponds to a circuit **40** which receives one chip-select signal from the computer system and which generates two chip-select signals.

[00118] Example 2

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```
always @(posedge clk_in)
    begin
                rs0N_R <= rs0_in_N;    // cs0
                rasN_R <= ras_in_N;
                casN_R <= cas_in_N;
                weN_R <= we_in_N;
    end
// Gated Chip Selects
assign          pcs0a_1 = (~rs0_in_N & ~ras_in_N & ~cas_in_N)                                   // ref,mrd reg set
                | (~rs0_in_N & ras_in_N & cas_in_N)                                             // ref exit, pwr dn
                | (~rs0_in_N & ~ras_in_N & cas_in_N & ~we_in_N & a10_in)                        // pchg all
                | (~rs0_in_N & ~ras_in_N & cas_in_N & ~we_in_N & ~a10_in & ~ba2_in)             // pchg single bnk
                | (~rs0_in_N & ~ras_in_N & cas_in_N & we_in_N       & ~ba2_in)                  // activate
                | (~rs0_in_N & ras_in_N & ~cas_in_N              & ~ba2_in)                     // xfr
                ;
assign          pcs0b_1 = (~rs0_in_N & ~ras_in_N & ~cas_in_N)                                   // ref,mrd reg set
                | (~rs0_in_N & ras_in_N & cas_in_N)                                             // ref exit, pwr dn
                | (~rs0_in_N & ~ras_in_N & cas_in_N & ~we_in_N & a10_in)                        // pchg all
                | (~rs0_in_N & ~ras_in_N & cas_in_N & ~we_in_N & ~a10_in & ba2_in)              // pchg single bnk
                | (~rs0_in_N & ~ras_in_N & cas_in_N & we_in_N       & ba2_in)                   // activate
                | (~rs0_in_N & ras_in_N & ~cas_in_N              & ba2_in) // xfr
                ;
//-------------------------------------
 always @(posedge clk_in)
    begin
                a4_r <= a4_in ;
                a5_r <= a5_in ;
                a6_r <= a6_in ;
                a10_r <= a10_in ;
                ba0_r <= ba0_in ;
                ba1_r <= ba1_in ;
                ba2_r <= ba2_in ;
                q_mrs_cmd_cyc1 <= q_mrs_cmd ;
    end
//////////////////////////////////////////////////////
// determine the cas latency
//////////////////////////////////////////////////////
assign q_mrs_cmd_r = (!rasN_R & !casN_R & !weN_R)
                     & !rs0N_R
                & (!ba0_r & !ba1_r)
                ;     // mrd reg set cmd
    always @(posedge clk_in)
        if (~reset_N)     // lmr
                cl3 <= 1'b1 ;
        else if (q_mrs_cmd_cyc1)  // load mode reg cmd
      begin
                cl3 <= (~a6_r & a5_r & a4_r ) ;
      end
    always @(posedge clk_in)
        if (~reset_N)             // reset
```


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```
                cl2 <= 1'b0 ;
        else if (q_mrs_cmd_cyc1)  // load mode reg cmd
        begin
                cl2 <= (~a6_r & a5_r & ~a4_r ) ;
        end
    always @(posedge clk_in)
        if (~reset_N)             // reset
                cl4 <= 1'b0 ;
        else if (q_mrs_cmd_cyc1)  // load mode reg cmd
        begin
                cl4 <= (a6_r & ~a5_r & ~a4_r ) ;
        end
  always @(posedge clk_in)
        if (~reset_N)           cl5 <= 1'b0 ;
        else if (q_mrs_cmd_cyc1)  // load mode reg cmd
        begin
                cl5 <= (a6_r & ~a5_r & a4_r ) ;
        end
assign          pre_cyc2_enfet = (wr_cmd_cyc1 & acs_cyc1 & cl3)     // wr brst cl3 preamble
                               ;
assign          pre_cyc3_enfet = (rd_cmd_cyc2 & cl3)                // rd brst cl3 preamble
                               | (wr_cmd_cyc2 & cl3)                // wr brst cl3 1st pair
                               | (wr_cmd_cyc2 & cl4)                // wr brst cl4 preamble
                               ;
assign          pre_cyc4_enfet = (wr_cmd_cyc3 & cl3)                // wr brst cl3 2nd pair
                               | (wr_cmd_cyc3 & cl4)                // wr brst cl4 1st pair
                               | (rd_cmd_cyc3 & cl3)                // rd brst cl3 1st pair
                               | (rd_cmd_cyc3 & cl4)                // rd brst cl4 preamble
                               ;
assign          pre_cyc5_enfet = (rd_cmd_cyc4 & cl3)                // rd brst cl3 2nd pair
                               | (wr_cmd_cyc4 & cl4)                // wr brst cl4 2nd pair
                               | (rd_cmd_cyc4 & cl4)                // rd brst cl4 1st pair
                               ;
// dq
assign          pre_dq_cyc = pre_cyc2_enfet
                   | pre_cyc3_enfet
                   | pre_cyc4_enfet
                   | pre_cyc5_enfet
                   ;
assign          pre_dq_ncyc = enfet_cyc2
                   | enfet_cyc3
                   | enfet_cyc4
                   | enfet_cyc5
                   ;
// dqs
assign          pre_dqsa_cyc = (pre_cyc2_enfet & ~ba2_r)
                   | (pre_cyc3_enfet & ~ba2_cyc2)
                   | (pre_cyc4_enfet & ~ba2_cyc3)
                   | (pre_cyc5_enfet & ~ba2_cyc4)
                   ;
assign          pre_dqsb_cyc = (pre_cyc2_enfet & ba2_r)
                   | (pre_cyc3_enfet & ba2_cyc2)
                   | (pre_cyc4_enfet & ba2_cyc3)
                   | (pre_cyc5_enfet & ba2_cyc4)
                   ;
assign          pre_dqsa_ncyc = (enfet_cyc2 & ~ba2_cyc2)
                   | (enfet_cyc3 & ~ba2_cyc3)
                   | (enfet_cyc4 & ~ba2_cyc4)
                   | (enfet_cyc5 & ~ba2_cyc5)
                   ;
assign          pre_dqsb_ncyc = (enfet_cyc2 & ba2_cyc2)
                   | (enfet_cyc3 & ba2_cyc3)
                   | (enfet_cyc4 & ba2_cyc4)
                   | (enfet_cyc5 & ba2_cyc5)
                   ;
```


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```
always @(posedge clk_in)
        begin
                        acs_cyc2 <= acs_cyc1 ;        // cs active
                        ba2_cyc2 <= ba2_r ;
                        ba2_cyc3 <= ba2_cyc2 ;
                        ba2_cyc4 <= ba2_cyc3 ;
                        ba2_cyc5 <= ba2_cyc4 ;
                        rd_cmd_cyc2 <= rd_cmd_cyc1 & acs_cyc1;
                        rd_cmd_cyc3 <= rd_cmd_cyc2 ;
                        rd_cmd_cyc4 <= rd_cmd_cyc3 ;
                        rd_cmd_cyc5 <= rd_cmd_cyc4 ;
                        rd_cmd_cyc6 <= rd_cmd_cyc5 ;
                        rd_cmd_cyc7 <= rd_cmd_cyc6 ;
                        wr_cmd_cyc2 <= wr_cmd_cyc1 & acs_cyc1;
                        wr_cmd_cyc3 <= wr_cmd_cyc2 ;
                        wr_cmd_cyc4 <= wr_cmd_cyc3 ;
                        wr_cmd_cyc5 <= wr_cmd_cyc4 ;
        end
 always @(negedge clk_in)
        begin
                        dq_ncyc <= dq_cyc;
                        dqs_ncyc_a <= dqs_cyc_a;
                        dqs_ncyc_b <= dqs_cyc_b;
        end
// DQ FET enables
assign                  enq_fet1 = dq_cyc | dq_ncyc             ;
assign                  enq_fet2 = dq_cyc | dq_ncyc ;
assign                 enq_fet3 = dq_cyc | dq_ncyc              ;
assign                  enq_fet4 = dq_cyc | dq_ncyc ;
assign                  enq_fet5 = dq_cyc | dq_ncyc ;
// DQS FET enables
assign                  ens_fet1a = dqs_cyc_a | dqs_ncyc_a    ;
assign                  ens_fet2a = dqs_cyc_a | dqs_ncyc_a    ;
assign                  ens_fet3a = dqs_cyc_a | dqs_ncyc_a    ;
assign                  ens_fet1b = dqs_cyc_b | dqs_ncyc_b    ;
assign                  ens_fet2b = dqs_cyc_b | dqs_ncyc_b     ;
assign                  ens_fet3b = dqs_cyc_b | dqs_ncyc_b    ;
```

[00119] Another exemplary section of Verilog code compatible with memory density multiplication from 256 Mb to 512 Mb using DDR2 memory devices and gated CAS signals with the row A_{13} density transition bit is listed below in Example 3. The exemplary code of Example 3 corresponds to a circuit **40** which receives one gated CAS signal from the computer system and which generates two gated CAS signals.

[00120] Example 3

```
// latched a13 flags cs0, banks 0-3
   always @(posedge clk_in)
      if (actv_cmd_R & ~rs0N_R & ~bnk1_R & ~bnk0_R )    // activate
      begin
                        1_a13_00 <= a13_r ;
      end
   always @(posedge clk_in)
      if (actv_cmd_R & ~rs0N_R & ~bnk1_R & bnk0_R)       // activate
      begin
                        1_a13_01 <= a13_r ;
      end
   always @(posedge clk_in)
      if (actv_cmd_R & ~rs0N_R & bnk1_R & ~bnk0_R)       // activate
```


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```
    begin
            1_a13_10 <= a13_r ;
    end
  always @(posedge clk_ in)
    if (actv_cmd_R & ~rs0N_R & bnk1_R & bnk0_R)      // activate
    begin
            1_a13_11 <= a13_r ;
    end
// gated cas
assign cas_i = ~(casN_R);
assign   cas0_o = ( ~rasN_R & cas_i)
            | ( rasN_R & ~1_a13_00 & ~bnk1_R & ~bnk0_R & cas_i)
            | ( rasN_R & ~1_a13_01 & ~bnk1_R & bnk0_R & cas_i)
            | ( rasN_R & ~1_a13_10 & bnk1_R & ~bnk0_R & cas_i)
            | ( rasN_R & ~1_a13_11 & bnk1_R & bnk0_R & cas_i)
            ;
assign   cas1_o = ( ~rasN_R & cas_i)
            | ( rasN_R & 1_a13_00          & ~bnk1_R & ~bnk0_R & cas_i)
            | ( rasN_R & 1_a13_01          & ~bnk1_R & bnk0_R & cas_i)
            | ( rasN_R & 1_a13_10          & bnk1_R & ~bnk0_R & cas_i)
            | ( rasN_R & 1_a13_11          & bnk1_R & bnk0_R & cas_i)
            ;
assign      pcas_0_N = ~cas0_o;
assign      pcas_1_N = ~cas1_o;
assign      rd0_o_R1 = rasN_R & cas0_o & weN_R & ~rs0N_R;   // rnk0 rd cmd cyc
assign      rd1_o_R1 = rasN_R & cas1_o & weN_R & ~rs0N_R;   // rnk1 rd cmd cyc
assign      wr0_o_R1 = rasN_R & cas0_o & ~weN_R & ~rs0N_R;   // rnk0 wr cmd cyc
assign      wr1_o_R1 = rasN_R & cas1_o & ~weN_R & ~rs0N_R ;   // rnk1 wr cmd cyc
    always @(posedge clk_in)
        begin
            rd0_o_R2 <= rd0_o_R1 ;
            rd0_o_R3 <= rd0_o_R2;
            rd0_o_R4 <= rd0_o_R3;
            rd0_o_R5 <= rd0_o_R4;
            rd1_o_R2 <= rd1_o_R1 ;
            rd1_o_R3 <= rd1_o_R2;
            rd1_o_R4 <= rd1_o_R3;
            rd1_o_R5 <= rd1_o_R4;
            wr0_o_R2 <= wr0_o_R1 ;
            wr0_o_R3 <= wr0_o_R2;
            wr0_o_R4 <= wr0_o_R3;
            wr1_o_R2 <= wr1_o_R1 ;
            wr1_o_R3 <= wr1_o_R2;
            wr1_o_R4 <= wr1_o_R3;
        end
    always @(posedge clk_in)
        begin
        if (
              (rd0_o_R2 & ~rd1_o_R4)                                  // pre-am rd if no ped on rnk 1
            | rd0_o_R3                                                // 1st cyc of rd brst
            | rd0_o_R4                                                // 2nd cyc of rd brst
            | (rd0_o_R5 & ~rd1_o_R2 & ~rd1_o_R3)                      // post-rd cyc if no ped on rnk 1
            | (wr0_o_R1)                                              // pre-am wr
            | wr0_o_R2 | wr0_o_R3                                     // wr brst 1st & 2nd cyc
            | (wr0_o_R4)                                              // post-wr cyc (chgef9)
            | wr1_o_R1 | wr1_o_R2 | wr1_o_R3 | wr1_o_R4               // rank 1 (chgef9)
            )
                                    en_fet_a <= 1'b1;                 // enable fet
        else
                                    en_fet_a <= 1'b0;                 // disable fet
        end
```


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```
always @(posedge clk_in)
        begin
        if(
                (rd1_o_R2 & ~rd0_o_R4)
              | rd1_o_R3
              | rd1_o_R4
              | (rd1_o_R5 & ~rd0_o_R2 & ~rd0_o_R3)
          | (wr1_o_R1)                                          // (chgef8)
          | wr1_o_R2 | wr1_o_R3
  | (wr1_o_R4)                                                  // post-wr cyc      (chgef9)
  | wr0_o_R1 | wr0_o_R2 | wr0_o_R3 | wr0_o_R4                   // rank 0 (chgef9)
                )
                        en_fet_b <= 1'b1;                       //
        else
                        en_fet_b <= 1'b0;
        end
```

[00121] In certain embodiments, the chipset memory controller of the computer system uses the inherent behavioral characteristics of the memory devices (e.g., DDR2 memory devices) to optimize throughput of the memory system. For example, for each internal bank in the memory array, a row (e.g., 1 KB page) is advantageously held activated for an extended period of time. The memory controller, by anticipating a high number of memory accesses or hits to a particular region of memory, can exercise this feature to advantageously eliminate time-consuming pre-charge cycles. In certain such embodiments in which two half-density memory devices are transparently substituted for a single full-density memory device (as reported by the SPD device **240** to the memory controller), the memory devices advantageously support the "open row" feature.

[00122] FIG. 10A schematically illustrates an exemplary memory module **10** which doubles the rank density in accordance with certain embodiments described herein. The memory module **10** has a first memory capacity. The memory module **10** comprises a plurality of substantially identical memory devices **30** configured as a first rank **32a** and a second rank **32b**. In certain embodiments, the memory devices **30** of the first rank **32a** are configured in pairs, and the memory devices **30** of the second rank **32b** are also configured in pairs. In certain embodiments, the memory devices **30** of the first rank **32a** are configured with their respective DQS pins tied together and the memory devices **30** of the second rank **32b** are configured with their respective DQS pins tied together, as described more fully below. The memory module **10** further comprises a circuit **40** which receives a first set of address and command signals from a memory controller (not shown) of the computer system. The first set of address and command signals is compatible with a second memory capacity substantially equal to one-half of the first memory capacity. The circuit **40** translates the first set of address and command

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signals into a second set of address and command signals which is compatible with the first memory capacity of the memory module **10** and which is transmitted to the first rank **32a** and the second rank **32b**.

[00123] The first rank **32a** of FIG. 10A has 18 memory devices **30** and the second rank **32b** of FIG. 10A has 18 memory devices **30**. Other numbers of memory devices **30** in each of the ranks **32a**, **32b** are also compatible with embodiments described herein.

[00124] In the embodiment schematically illustrated by FIG. 10A, the memory module **10** has a width of 8 bytes (or 64 bits) and each of the memory devices **30** of FIG. 10A has a bit width of 4 bits. The 4-bit-wide ("×4") memory devices **30** of FIG. 10A have one-half the width, but twice the depth of 8-bit-wide ("×8") memory devices. Thus, each pair of "×4" memory devices **30** has the same density as a single "×8" memory device, and pairs of "×4" memory devices **30** can be used instead of individual "×8" memory devices to provide the memory density of the memory module **10**. For example, a pair of 512-Mb 128 M×4-bit memory devices has the same memory density as a 1-Gb 128 M×8-bit memory device.

[00125] For two "×4" memory devices **30** to work in tandem to mimic a "×8" memory device, the relative DQS pins of the two memory devices **30** in certain embodiments are advantageously tied together, as described more fully below. In addition, to access the memory density of a high-density memory module **10** comprising pairs of "×4" memory devices **30**, an additional address line is used. While a high-density memory module comprising individual "×8" memory devices with the next-higher density would also utilize an additional address line, the additional address lines are different in the two memory module configurations.

[00126] For example, a 1-Gb 128 M×8-bit DDR-1 DRAM memory device uses row addresses A_{13}-A_0 and column addresses A_{11} and A_9-A_0. A pair of 512-Mb 128 M×4-bit DDR-1 DRAM memory devices uses row addresses A_{12}-A_0 and column addresses A_{12}, A_{11}, and A_9-A_0. In certain embodiments, a memory controller of a computer system utilizing a 1-GB 128 M×8 memory module **10** comprising pairs of the 512-Mb 128 M×4 memory devices **30** supplies the address and command signals including the extra row address (A_{13}) to the memory module **10**. The circuit **40** receives the address and command signals from the memory controller and converts the extra row address (A_{13}) into an extra column address (A_{12}).

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[00127] FIG. 10B schematically illustrates an exemplary circuit **40** compatible with embodiments described herein. The circuit **40** is used for a memory module **10** comprising pairs of "×4" memory devices **30** which mimic individual "×8" memory devices. In certain embodiments, each pair has the respective DQS pins of the memory devices **30** tied together. In certain embodiments, as schematically illustrated by FIG. 10B, the circuit **40** comprises a programmable-logic device (PLD) **42**, a first multiplexer **44** electrically coupled to the first rank **32a** of memory devices **30**, and a second multiplexer **46** electrically coupled to the second rank **32b** of memory devices **30**. In certain embodiments, the PLD **42** and the first and second multiplexers **44**, **46** are discrete elements, while in other certain embodiments, they are integrated within a single integrated circuit. Persons skilled in the art can select an appropriate PLD **42**, first multiplexer **44**, and second multiplexer **46** in accordance with embodiments described herein.

[00128] In the exemplary circuit **40** of FIG. 10B, during a row access procedure (CAS is high), the first multiplexer **44** passes the A_{12} address through to the first rank **32**, the second multiplexer **46** passes the A_{12} address through to the second rank **34**, and the PLD **42** saves or latches the A_{13} address from the memory controller. In certain embodiments, a copy of the A_{13} address is saved by the PLD **42** for each of the internal banks (e.g., 4 internal banks) per memory device **30**. During a subsequent column access procedure (CAS is low), the first multiplexer **44** passes the previously-saved A_{13} address through to the first rank **32a** as the A_{12} address and the second multiplexer **46** passes the previously-saved A_{13} address through to the second rank **32b** as the A_{12} address. The first rank **32a** and the second rank **32b** thus interpret the previously-saved A_{13} row address as the current A_{12} column address. In this way, in certain embodiments, the circuit **40** translates the extra row address into an extra column address in accordance with certain embodiments described herein.

[00129] Thus, by allowing two lower-density memory devices to be used rather than one higher-density memory device, certain embodiments described herein provide the advantage of using lower-cost, lower-density memory devices to build "next-generation" higher-density memory modules. Certain embodiments advantageously allow the use of lower-cost readily-available 512-Mb DDR-2 SDRAM devices to replace more expensive 1-Gb DDR-2 SDRAM devices. Certain embodiments advantageously reduce the total cost of the resultant memory module.

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[00130] FIG. 11A schematically illustrates an exemplary memory module **10** which doubles number of ranks in accordance with certain embodiments described herein. The memory module **10** has a first plurality of memory locations with a first memory density. The memory module **10** comprises a plurality of substantially identical memory devices **30** configured as a first rank **32a**, a second rank **32b**, a third rank **32** *c*, and a fourth rank **32** *d*. The memory module **10** further comprises a circuit **40** which receives a first set of address and command signals from a memory controller (not shown). The first set of address and command signals is compatible with a second plurality of memory locations having a second memory density. The second memory density is substantially equal to one-half of the first memory density. The circuit **40** translates the first set of address and command signals into a second set of address and command signals which is compatible with the first plurality of memory locations of the memory module **10** and which is transmitted to the first rank **32a**, the second rank **32b**, the third rank **32** *c*, and the fourth rank **32** *d*.

[00131] Each rank **32a**, **32b**, **32** *c*, **32** *d* of FIG. 11A has 9 memory devices **30**. Other numbers of memory devices **30** in each of the ranks **32a**, **32b**, **32** *c*, **32** *d* are also compatible with embodiments described herein.

[00132] In the embodiment schematically illustrated by FIG. 11A, the memory module **10** has a width of 8 bytes (or 64 bits) and each of the memory devices **30** of FIG. 11A has a bit width of 8 bits. Because the memory module **10** has twice the number of 8-bit-wide ("×8") memory devices **30** as does a standard 8-byte-wide memory module, the memory module **10** has twice the density as does a standard 8-byte-wide memory module. For example, a 1-GB 128 M×8-byte memory module with 36 512-Mb 128 M×8-bit memory devices (arranged in four ranks) has twice the memory density as a 512-Mb 128 M×8-byte memory module with 18 512-Mb 128 M×8-bit memory devices (arranged in two ranks).

[00133] To access the additional memory density of the high-density memory module **10**, the two chip-select signals (CS_0, CS_1) are used with other address and command signals to gate a set of four gated CAS signals. For example, to access the additional ranks of four-rank 1-GB 128 M×8-byte DDR-1 DRAM memory module, the CS_0 and CS_1 signals along with the other address and command signals are used to gate the CAS signal appropriately, as schematically illustrated by FIG. 11A. FIG. 11B schematically illustrates an exemplary circuit **40** compatible with embodiments described herein. In certain embodiments, the circuit **40**

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comprises a programmable-logic device (PLD) **42** and four "OR" logic elements **52**, **54**, **56**, **58** electrically coupled to corresponding ranks **32a**, **32b**, **32** *c*, **32** *d* of memory devices **30**.

[00134] In certain embodiments, the PLD **42** comprises an ASIC, an FPGA, a custom-designed semiconductor device, or a CPLD. In certain embodiments, the PLD **42** and the four "OR" logic elements **52**, **54**, **56**, **58** are discrete elements, while in other certain embodiments, they are integrated within a single integrated circuit. Persons skilled in the art can select an appropriate PLD **42** and appropriate "OR" logic elements **52**, **54**, **56**, **58** in accordance with embodiments described herein.

[00135] In the embodiment schematically illustrated by FIG. 11B, the PLD **42** transmits each of the four "enabled CAS" ($ENCAS_0a$, $ENCAS_0b$, $ENCAS_1a$, $ENCAS_1b$) signals to a corresponding one of the "OR" logic elements **52**, **54**, **56**, **58**. The CAS signal is also transmitted to each of the four "OR" logic elements **52**, **54**, **56**, **58**. The CAS signal and the "enabled CAS" signals are "low" true signals. By selectively activating each of the four "enabled CAS" signals which are inputted into the four "OR" logic elements **52**, **54**, **56**, **58**, the PLD **42** is able to select which of the four ranks **32a**, **32b**, **32** *c*, **32** *d* is active.

[00136] In certain embodiments, the PLD **42** uses sequential and combinatorial logic procedures to produce the gated CAS signals which are each transmitted to a corresponding one of the four ranks **32a**, **32b**, **32** *c*, **32** *d*. In certain other embodiments, the PLD **42** instead uses sequential and combinatorial logic procedures to produce four gated chip-select signals (e.g., CS_0a, CS_0b, CS_1a, and CS_1b) which are each transmitted to a corresponding one of the four ranks **32a**, **32b**, **32** *c*, **32** *d*.

Tied Data Strobe Signal Pins

[00137] For proper operation, the computer system advantageously recognizes a 1-GB memory module comprising 256-Mb memory devices with 64 M×4-bit configuration as a 1-GB memory module having 512-Mb memory devices with 64 M×8-bit configuration (e.g., as a 1-GB memory module with 128 M×8-byte configuration). This advantageous result is desirably achieved in certain embodiments by electrically connecting together two output signal pins (e.g., DQS or data strobe pins) of the two 256-Mb memory devices such that both output signal pins are concurrently active when the two memory devices are concurrently enabled. The DQS or data strobe is a bi-directional signal that is used during both read cycles

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and write cycles to validate or latch data. As used herein, the terms "tying together" or "tied together" refer to a configuration in which corresponding pins (e.g., DQS pins) of two memory devices are electrically connected together and are concurrently active when the two memory devices are concurrently enabled (e.g., by a common chip-select or CS signal). Such a configuration is different from standard memory module configurations in which the output signal pins (e.g., DQS pins) of two memory devices are electrically coupled to the same source, but these pins are not concurrently active since the memory devices are not concurrently enabled. However, a general guideline of memory module design warns against tying together two output signal pins in this way.

[00138] FIGS. 12 and 13 schematically illustrate a problem which may arise from tying together two output signal pins. FIG. 12 schematically illustrates an exemplary memory module **305** in which a first DQS pin **312** of a first memory device **310** is electrically connected to a second DQS pin **322** of a second memory device **320**. The two DQS pins **312**, **322** are both electrically connected to a memory controller **330**.

[00139] FIG. 13 is an exemplary timing diagram of the voltages applied to the two DQS pins **312**, **322** due to non-simultaneous switching. As illustrated by FIG. 13, at time t_1, both the first DQS pin **312** and the second DQS pin **322** are high, so no current flows between them. Similarly, at time t_4, both the first DQS pin **312** and the second DQS pin **322** are low, so no current flows between them. However, for times between approximately t_2 and approximately t_3, the first DQS pin **312** is low while the second DQS pin **322** is high. Under such conditions, a current will flow between the two DQS pins **312**, **322**. This condition in which one DQS pin is low while the other DQS pin is high can occur for fractions of a second (e.g., 0.8 nanoseconds) during the dynamic random-access memory (DRAM) read cycle. During such conditions, the current flowing between the two DQS pins **312**, **322** can be substantial, resulting in heating of the memory devices **310**, **320**, and contributing to the degradation of reliability and eventual failure of these memory devices.

[00140] A second problem may also arise from tying together two output signal pins. FIG. 14 schematically illustrates another exemplary memory module **305** in which a first DQS pin **312** of a first memory device **310** is electrically connected to a second DQS pin **322** of a second memory device **320**. The two DQS pins **312**, **322** of FIG. 14 are both electrically connected to a memory controller (not shown). The DQ (data input/output) pin **314** of the first

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memory device **310** and the corresponding DQ pin **324** of the second memory device **320** are each electrically connected to the memory controller by the DQ bus (not shown). Typically, each memory device **310**, **320** will have a plurality of DQ pins (e.g., eight DQ pins per memory device), but for simplicity, FIG. 14 only shows one DQ pin for each memory device **310**, **320**.

[00141] Each of the memory devices **310**, **320** of FIG. 14 utilizes a respective on-die termination or "ODT" circuit **332**, **334** which has termination resistors (e.g., 75 ohms) internal to the memory devices **310**, **320** to provide signal termination. Each memory device **310**, **320** has a corresponding ODT signal pin **362**, **364** which is electrically connected to the memory controller via an ODT bus **340**. The ODT signal pin **362** of the first memory device **310** receives a signal from the ODT bus **340** and provides the signal to the ODT circuit **332** of the first memory device **310**. The ODT circuit **332** responds to the signal by selectively enabling or disabling the internal termination resistors **352**, **356** of the first memory device **310**. This behavior is shown schematically in FIG. 14 by the switches **342**, **344** which are either closed (dash-dot line) or opened (solid line). The ODT signal pin **364** of the second memory device **320** receives a signal from the ODT bus **340** and provides the signal to the ODT circuit **334** of the second memory device **320**. The ODT circuit **334** responds to the signal by selectively enabling or disabling the internal termination resistors **354**, **358** of the second memory device **320**. This behavior is shown schematically in FIG. 14 by the switches **346**, **348** which are either closed (dash-dot line) or opened (solid line). The switches **342**, **344**, **346**, **348** of FIG. 14 are schematic representations of the operation of the ODT circuits **332**, **334**, and do not signify that the ODT circuits **332**, **334** necessarily include mechanical switches.

[00142] Examples of memory devices **310**, **320** which include such ODT circuits **332**, **334** include, but are not limited to, DDR2 memory devices. Such memory devices are configured to selectively enable or disable the termination of the memory device in this way in response to signals applied to the ODT signal pin of the memory device. For example, when the ODT signal pin **362** of the first memory device **310** is pulled high, the termination resistors **352**, **356** of the first memory device **310** are enabled. When the ODT signal pin **362** of the first memory device **310** is pulled low (e.g., grounded), the termination resistors **352**, **356** of the first memory device **310** are disabled. By selectively disabling the termination resistors of an active memory device, while leaving the termination resistors of inactive memory devices enabled, such configurations advantageously preserve signal strength on the active memory

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device while continuing to eliminate signal reflections at the bus-die interface of the inactive memory devices.

[00143] In certain configurations, as schematically illustrated by FIG. 14, the DQS pins **312**, **322** of each memory device **310**, **320** are selectively connected to a voltage VTT through a corresponding termination resistor **352**, **354** internal to the corresponding memory device **310**, **320**. Similarly, in certain configurations, as schematically illustrated by FIG. 14, the DQ pins **314**, **324** are selectively connected to a voltage VTT through a corresponding termination resistor **356**, **358** internal to the corresponding memory device **310**, **320**. In certain configurations, rather than being connected to a voltage VTT, the DQ pins **314**, **324** and/or the DQS pins **312**, **322** are selectively connected to ground through the corresponding termination resistors **352**, **354**, **356**, **358**. The resistances of the internal termination resistors **352**, **354**, **356**, **358** are selected to clamp the voltages so as to reduce the signal reflections from the corresponding pins. In the configuration schematically illustrated by FIG. 14, each internal termination resistor **352**, **354**, **356**, **358** has a resistance of approximately 75 ohms.

[00144] When connecting the first memory device **310** and, the second memory device **320** together to form a double word width, both the first memory device **310** and the second memory device **320** are enabled at the same time (e.g., by a common CS signal). Connecting the first memory device **310** and the second memory device **320** by tying the DQS pins **312**, **322** together, as shown in FIG. 14, results in a reduced effective termination resistance for the DQS pins **312**, **322**. For example, for the exemplary configuration of FIG. 14, the effective termination resistance for the DQS pins **312**, **322** is approximately 37.5 ohms, which is one-half the desired ODT resistance (for 75-ohm internal termination resistors) to reduce signal reflections since the internal termination resistors **352**, **354** of the two memory devices **310**, **320** are connected in parallel. This reduction in the termination resistance can result in signal reflections causing the memory device to malfunction.

[00145] FIG. 15 schematically illustrates an exemplary memory module **400** in accordance with certain embodiments described herein. The memory module **400** comprises a first memory device **410** having a first data strobe (DQS) pin **412** and a second memory device **420** having a second data strobe (DQS) pin **422**. The memory module **400** further comprises a first resistor **430** electrically coupled to the first DQS pin **412**. The memory module **400** further comprises a second resistor **440** electrically coupled to the second DQS pin **422** and to the first

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resistor **430**. The first DQS pin **412** is electrically coupled to the second DQS pin **422** through the first resistor **430** and through the second resistor **440**.

[00146] In certain embodiments, the memory module **400** is a 1-GB unbuffered Double Data Rate (DDR) Synchronous Dynamic RAM (SDRAM) high-density dual in-line memory module (DIMM). FIGS. 16A and 16B schematically illustrate a first side **462** and a second side **464**, respectively, of such a memory module **400** with eighteen 64 M×4-bit, DDR-1 SDRAM FBGA memory devices on each side of a 184-pin glass-epoxy printed circuit board (PCB) **460**. In certain embodiments, the memory module **400** further comprises a phase-lock-loop (PLL) clock driver **470**, an EEPROM for serial-presence detect (SPD) data **480**, and decoupling capacitors (not shown) mounted on the PCB in parallel to suppress switching noise on VDD and VDDQ power supply for DDR-1 SDRAM. By using synchronous design, such memory modules **400** allow precise control of data transfer between the memory module **400** and the system controller. Data transfer can take place on both edges of the DQS signal at various operating frequencies and programming latencies. Therefore, certain such memory modules **400** are suitable for a variety of high-performance system applications.

[00147] In certain embodiments, the memory module **400** comprises a plurality of memory devices configured in pairs, each pair having a first memory device **410** and a second memory device **420**. For example, in certain embodiments, a 128 M×72-bit DDR SDRAM high-density memory module **400** comprises thirty-six 64 M×4-bit DDR-1 SDRAM integrated circuits in FBGA packages configured in eighteen pairs. The first memory device **410** of each pair has the first DQS pin **412** electrically coupled to the second DQS pin **422** of the second memory device **420** of the pair. In addition, the first DQS pin **412** and the second DQS pin **422** are concurrently active when the first memory device **410** and the second memory device **420** are concurrently enabled.

[00148] In certain embodiments, the first resistor **430** and the second resistor **440** each has a resistance advantageously selected to reduce the current flow between the first DQS pin **412** and the second DQS pin **422** while allowing signals to propagate between the memory controller and the DQS pins **412**, **422**. In certain embodiments, each of the first resistor **430** and the second resistor **440** has a resistance in a range between approximately 5 ohms and approximately 50 ohms. For example, in certain embodiments, each of the first resistor **430** and the second resistor **440** has a resistance of approximately 22 ohms. Other resistance values

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for the first resistor **430** and the second resistor **440** are also compatible with embodiments described herein. In certain embodiments, the first resistor **430** comprises a single resistor, while in other embodiments, the first resistor **430** comprises a plurality of resistors electrically coupled together in series and/or in parallel. Similarly, in certain embodiments, the second resistor **440** comprises a single resistor, while in other embodiments, the second resistor **440** comprises a plurality of resistors electrically coupled together in series and/or in parallel.

[00149] FIGS. 17A and 17B schematically illustrate an exemplary embodiment of a memory module **400** in which the first resistor **430** and the second resistor **440** are used to reduce the current flow between the first DQS pin **412** and the second DQS pin **422**. As schematically illustrated by FIG. 17A, the memory module **400** is part of a computer system **500** having a memory controller **510**. The first resistor **430** has a resistance of approximately 22 ohms and the second resistor **440** has a resistance of approximately 22 ohms. The first resistor **430** and the second resistor **440** are electrically coupled in parallel to the memory controller **510** through a signal line **520** having a resistance of approximately 25 ohms. The first resistor **430** and the second resistor **440** are also electrically coupled in parallel to a source of a fixed termination voltage (identified by VTT in FIGS. 17A and 17B) by a signal line **540** having a resistance of approximately 47 ohms. Such an embodiment can advantageously be used to allow two memory devices having lower bit widths (e.g., 4-bit) to behave as a single virtual memory device having a higher bit width (e.g., 8-bit).

[00150] FIG. 17B schematically illustrates exemplary current-limiting resistors **430**, **440** in conjunction with the impedances of the memory devices **410**, **420**. During an exemplary portion of a data read operation, the memory controller **510** is in a high-impedance condition, the first memory device **410** drives the first DQS pin **412** high (e.g., 2.7 volts), and the second memory device **420** drives the second DQS pin **422** low (e.g., 0 volts). The amount of time for which this condition occurs is approximated by the time between t_2 and t_3 of FIG. 13, which in certain embodiments is approximately twice the tDQSQ (data strobe edge to output data edge skew time, e.g., approximately 0.8 nanoseconds). At least a portion of this time in certain embodiments is caused by simultaneous switching output (SSO) effects.

[00151] In certain embodiments, as schematically illustrated by FIG. 17B, the DQS driver of the first memory device **410** has a driver impedance R_1 of approximately 17 ohms, and the DQS driver of the second memory device **420** has a driver impedance R_4 of

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approximately 17 ohms. Because the upper network of the first memory device **410** and the first resistor **430** (with a resistance R_2 of approximately 22 ohms) is approximately equal to the lower network of the second memory device **420** and the second resistor **440** (with a resistance R_3 of approximately 22 ohms), the voltage at the midpoint is approximately 0.5*(2.7−0)=1.35 volts, which equals VTT, such that the current flow across the 47-ohm resistor of FIG. 17B is approximately zero.

[00152] The voltage at the second DQS pin **422** in FIG. 17B is given by $V_{DQS2}=2.7*R_4/(R_1+R_2+R_3+R_4)=0.59$ volts and the current flowing through the second DQS pin **422** is given by $I_{DQS2}=0.59/R_4=34$ milliamps. The power dissipation in the DQS driver of the second memory device **420** is thus $P_{DQS2}=34$ mA*0.59 V=20 milliwatts. In contrast, without the first resistor **430** and the second resistor **440**, only the 17-ohm impedances of the two memory devices **410**, **420** would limit the current flow between the two DQS pins **412**, **422**, and the power dissipation in the DQS driver of the second memory device **420** would be approximately 107 milliwatts. Therefore, the first resistor **430** and the second resistor **440** of FIGS. 17A and 17B advantageously limit the current flowing between the two memory devices during the time that the DQS pin of one memory device is driven high and the DQS pin of the other memory device is driven low.

[00153] In certain embodiments in which there is overshoot or undershoot of the voltages, the amount of current flow can be higher than those expected for nominal voltage values. Therefore, in certain embodiments, the resistances of the first resistor **430** and the second resistor **440** are advantageously selected to account for such overshoot/undershoot of voltages.

[00154] For certain such embodiments in which the voltage at the second DQS pin **422** is $V_{DQS2}=0.59$ volts and the duration of the overdrive condition is approximately 0.8 nanoseconds at maximum, the total surge is approximately 0.59 V*1.2 ns=0.3 V-ns. For comparison, the JEDEC standard for overshoot/undershoot is 2.4 V-ns, so certain embodiments described herein advantageously keep the total surge within predetermined standards (e.g., JEDEC standards).

[00155] FIG. 18 schematically illustrates another exemplary memory module **600** compatible with certain embodiments described herein. The memory module **600** comprises a termination bus **605**. The memory module **600** further comprises a first memory device **610**

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having a first data strobe pin **612**, a first termination signal pin **614** electrically coupled to the termination bus **605**, a first termination circuit **616**, and at least one data pin **618**. The first termination circuit **616** selectively electrically terminating the first data strobe pin **612** and the first data pin **618** in response to a first signal received by the first termination signal pin **614** from the termination bus **605**. The memory module **600** further comprises a second memory device **620** having a second data strobe pin **622** electrically coupled to the first data strobe pin **612**, a second termination signal pin **624**, a second termination circuit **626**, and at least one data pin **628**. The second termination signal pin **624** is electrically coupled to a voltage, wherein the second termination circuit **626** is responsive to the voltage by not terminating the second data strobe pin **622** or the second data pin **628**. The memory module **600** further comprises at least one termination assembly **630** having a third termination signal pin **634**, a third termination circuit **636**, and at least one termination pin **638** electrically coupled to the data pin **628** of the second memory device **620**. The third termination signal pin **634** is electrically coupled to the termination bus **605**. The third termination circuit **636** selectively electrically terminates the data pin **628** of the second memory device **620** through the termination pin **638** in response to a second signal received by the third termination signal pin **634** from the termination bus **605**.

[00156] FIG. 19 schematically illustrates a particular embodiment of the memory module **600** schematically illustrated by FIG. 18. The memory module **600** comprises an on-die termination (ODT) bus **605**. The memory module **600** comprises a first memory device **610** having a first data strobe (DQS) pin **612**, a first ODT signal pin **614** electrically coupled to the ODT bus **605**, a first ODT circuit **616**, and at least one data (DQ) pin **618**. The first ODT circuit **616** selectively electrically terminates the first DQS pin **612** and the DQ pin **618** of the first memory device **610** in response to an ODT signal received by the first ODT signal pin **614** from the ODT bus **605**. This behavior of the first ODT circuit **616** is schematically illustrated in FIG. 14 by the switches **672**, **676** which are selectively closed (dash-dot line) or opened (solid line).

[00157] The memory module **600** further comprises a second memory device **620** having a second DQS pin **622** electrically coupled to the first DQS pin **612**, a second ODT signal pin **624**, a second ODT circuit **626**, and at least one DQ pin **628**. The first DQS pin **612** and the second DQS pin **622** are concurrently active when the first memory device **610** and the

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second memory device **620** are concurrently enabled. The second ODT signal pin **624** is electrically coupled to a voltage (e.g., ground), wherein the second ODT circuit **626** is responsive to the voltage by not terminating the second DQS pin **622** or the second DQ pin **624**. This behavior of the second ODT circuit **626** is schematically illustrated in FIG. 14 by the switches **674**, **678** which are opened.

[00158] The memory module **600** further comprises at least one termination assembly **630** having a third ODT signal pin **634** electrically coupled to the ODT bus **605**, a third ODT circuit **636**, and at least one termination pin **638** electrically coupled to the DQ pin **628** of the second memory device **620**. The third ODT circuit **636** selectively electrically terminates the DQ pin **628** of the second memory device **620** through the termination pin **638** in response to an ODT signal received by the third ODT signal pin **634** from the ODT bus **605**. This behavior of the third ODT circuit **636** is schematically illustrated in FIG. 19 by the switch **680** which is either closed (dash-dot line) or opened (solid line).

[00159] In certain embodiments, the termination assembly **630** comprises discrete electrical components which are surface-mounted or embedded on the printed-circuit board of the memory module **600**. In certain other embodiments, the termination assembly **630** comprises an integrated circuit mounted on the printed-circuit board of the memory module **600**. Persons skilled in the art can provide a termination assembly **630** in accordance with embodiments described herein.

[00160] Certain embodiments of the memory module **600** schematically illustrated by FIG. 19 advantageously avoid the problem schematically illustrated by FIG. 12 of electrically connecting the internal termination resistances of the DQS pins of the two memory devices in parallel. As described above in relation to FIG. 14, FIGS. 18 and 19 only show one DQ pin for each memory device for simplicity. Other embodiments have a plurality of DQ pins for each memory device. In certain embodiments, each of the first ODT circuit **616**, the second ODT circuit **626**, and the third ODT circuit **636** are responsive to a high voltage or signal level by enabling the corresponding termination resistors and are responsive to a low voltage or signal level (e.g., ground) by disabling the corresponding termination resistors. In other embodiments, each of the first ODT circuit **616**, the second ODT circuit **626**, and the third ODT circuit **636** are responsive to a high voltage or signal level by disabling the corresponding termination resistors and are responsive to a low voltage or signal level (e.g., ground) by

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enabling the corresponding termination resistors. Furthermore, the switches **672**, **674**, **676**, **678**, **680** of FIG. 18 are schematic representations of the enabling and disabling operation of the ODT circuits **616**, **626**, **636** and do not signify that the ODT circuits **616**, **626**, **636** necessarily include mechanical switches.

[00161] The first ODT signal pin **614** of the first memory device **610** receives an ODT signal from the ODT bus **605**. In response to this ODT signal, the first ODT circuit **616** selectively enables or disables the termination resistance for both the first DQS pin **612** and the DQ pin **618** of the first memory device **610**. The second ODT signal pin **624** of the second memory device **620** is tied (e.g., directly hard-wired) to the voltage (e.g., ground), thereby disabling the internal termination resistors **654**, **658** on the second DQS pin **622** and the second DQ pin **628**, respectively, of the second memory device **620** (schematically shown by open switches **674**, **678** in FIG. 19). The second DQS pin **622** is electrically coupled to the first DQS pin **612**, so the termination resistance for both the first DQS pin **612** and the second DQS pin **622** is provided by the termination resistor **652** internal to the first memory device **510**.

[00162] The termination resistor **656** of the DQ pin **618** of the first memory device **610** is enabled or disabled by the ODT signal received by the first ODT signal pin **614** of the first memory device **610** from the ODT bus **605**. The termination resistance of the DQ pin **628** of the second memory device **620** is enabled or disabled by the ODT signal received by the third ODT signal pin **634** of the termination assembly **630** which is external to the second memory device **620**. Thus, in certain embodiments, the first ODT signal pin **614** and the third ODT signal pin **634** receive the same ODT signal from the ODT bus **605**, and the termination resistances for both the first memory device **610** and the second memory device **620** are selectively enabled or disabled in response thereto when these memory devices are concurrently enabled. In this way, certain embodiments of the memory module **600** schematically illustrated by FIG. 19 provides external or off-chip termination of the second memory device **620**.

[00163] Certain embodiments of the memory module **600** schematically illustrated by FIG. 19 advantageously allow the use of two lower-cost readily-available 512-Mb DDR-2 SDRAM devices to provide the capabilities of a more expensive 1-GB DDR-2 SDRAM device. Certain such embodiments advantageously reduce the total cost of the resultant memory module **600**.

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[00164] Certain embodiments described herein advantageously increase the memory capacity or memory density per memory slot or socket on the system board of the computer system. Certain embodiments advantageously allow for higher memory capacity in systems with limited memory slots. Certain embodiments advantageously allow for flexibility in system board design by allowing the memory module **10** to be used with computer systems designed for different numbers of ranks (e.g., either with computer systems designed for two-rank memory modules or with computer systems designed for four-rank memory modules). Certain embodiments advantageously provide lower costs of board designs.

[00165] In certain embodiments, the memory density of a memory module is advantageously doubled by providing twice as many memory devices as would otherwise be provided. For example, pairs of lower-density memory devices can be substituted for individual higher-density memory devices to reduce costs or to increase performance. As another example, twice the number of memory devices can be used to produce a higher-density memory configuration of the memory module. Each of these examples can be limited by the number of chip select signals which are available from the memory controller or by the size of the memory devices. Certain embodiments described herein advantageously provide a logic mechanism to overcome such limitations.

[00166] Various embodiments of the present invention have been described above. Although this invention has been described with reference to these specific embodiments, the descriptions are intended to be illustrative of the invention and are not intended to be limiting. Various modifications and applications may occur to those skilled in the art without departing from the true spirit and scope of the invention.

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WE CLAIM:

1. A memory module operable in a computer system, the computer system including a memory controller coupled to a memory bus, the memory bus including address and control signal lines and data signal lines, the memory module comprising:

a printed circuit board having a plurality of edge connections configured to be electrically coupled to a corresponding plurality of contacts of a module slot of the computer system;

logic coupled to the printed circuit board and configurable to receive input address and control signals associated with a read or write memory command via the address and control signal lines and to output registered address and control signals corresponding to the input address and control signals, the input address and control signals including a plurality of input chip select signals and other input address and control signals, the plurality of input chip select signals at least including a first input chip select signal and a second input chip select signal, the first input chip select signal having an active value and the second input chip select signal having an inactive value, the registered address and control signals including a plurality of registered chip select signals and other registered address and control signals, the plurality of registered chip select signals at least including a first registered chip select signal corresponding to the first input chip select signal and a second registered chip select signal corresponding to the second input chip select signal, the first registered chip select signal having an active value and the second registered chip select signal having an inactive value, wherein the logic is further configurable to output data transfer control signals associated with the read or write memory command;

memory devices mounted on the printed circuit board, the memory devices at least including first memory devices and second memory devices, wherein the first memory devices are configured to receive the first registered chip select signal and the other registered address and control signals, and to receive or output data signals associated with the read or write command, and wherein the second memory devices are configured to receive the second registered chip select signal and the other registered address and control signals; and

circuitry coupled between the memory devices and the data signal lines in the memory bus, and configurable to be in any of a plurality of states including a first state and a second state, wherein:

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the circuitry is configurable to transition from the first state to the second state in response to the data transfer control signals;

the circuitry in the first state is configured to disable signal communication through the circuitry;

the circuitry in the second state is configured to transfer the data signals associated with the read or write command via registered data transfers in accordance with a transfer time budget of the memory module;

the transfer time budget of the memory module includes a predetermined amount of time delay associated with the registered data transfers through the circuitry; and

an overall CAS latency of the memory module is greater than an actual operational CAS latency of each of the memory devices by at least the predetermined amount of time delay.

2. The memory module of claim 1, wherein each of the memory devices has a corresponding load, and the circuitry is configured to isolate the loads of the memory devices from the memory bus.

3. The memory module of claim 1, wherein the data signals include respective sets of consecutively transmitted data bits corresponding to respective data signal lines in the memory bus, and wherein each set of consecutively transmitted data bits are successively transferred through the circuitry in response to the data transfer control signals and in accordance with the transfer time budget of the memory module.

4. The memory module of claim 1, wherein each of the memory devices is 4-bits or 8-bits wide, and wherein the first memory devices form a rank that is 32-bits, 64-bits or 72-bits wide.

5. The memory module of claim 1, wherein each of the memory devices is 4-bits wide, and wherein the memory devices are configured in 8-bit-wide pairs.

6. The memory module of claim 1, wherein the circuitry includes logic pipelines configurable to enable data transfers between the memory devices and the memory bus through the circuitry.

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7. The memory module of claim 1, wherein the memory module has a specified data rate, and wherein the data signals are transferred between the first memory devices and the memory controller at the specified data rate.

8. The memory module of claim 1, further comprising a phase locked loop clock driver configured to output a clock signal in response to one or more signals received from the memory controller, wherein the predetermined amount of time delay is at least one clock cycle time delay.

9. The memory module of claim 8, wherein the memory devices are dynamic random access memory devices configured to operate synchronously with the clock signal, and wherein each memory device in the first memory devices is configured to receive or output a respective set of data strobes and to receive or output data bits on both edges of each of the respective set of data strobes.

10. The memory module of claim 1, wherein the circuitry includes data paths that are disabled when the circuitry is in the first state and enabled when the circuitry is in the second state.

11. The memory module of claim 10, wherein the data paths are disabled when no data signals associated with any memory command are being transferred through the circuitry.

12. The memory module of claim 10, wherein the memory module has a specified data rate, and wherein the data signals are transferred through the data paths at the specified data rate.

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MEMORY MODULE WITH DATA BUFFERING

ABSTRACT OF THE DISCLOSURE

A memory module operable to communicate data with a memory controller via a memory bus. The memory module comprises memory devices and logic configurable to receive and register a set of input address and control signals associated with a read or write memory command and to output data transfer control signals. The memory module further comprises circuitry coupled between the memory bus and the memory devices. The circuitry is configurable to be in any of a plurality of states including a first state and a second state, and to transition from the first state to the second state in response to the data transfer control signals. The circuitry in the first state is configured to disable signal communication through the circuitry. The circuitry in the second state is configured to transfer the data signals associated with the read or write command in accordance with a transfer time budget of the memory module.

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Customer No. 79141
Attorney Docket No.: NETL.018P2C7

Modified PTO/AIA/01 (06-12)

DECLARATION FOR UTILITY OR DESIGN APPLICATION

Title of Invention	LOAD-REDUCING CIRCUIT FOR MEMORY MODULE

As a below named inventor, I hereby declare that:

This declaration is directed to:

☐ The attached application, or

■ United States application or PCT international application number 13/971,231 filed on August 20, 2013.

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

Note to Inventor: 37 C.F.R. § 1.63(c) states: "A person may not execute an oath or declaration for an application unless that person has reviewed and understands the contents of the application, including the claims, and is aware of the duty to disclose to the Office all information known to the person to be material to patentability as defined in § 1.56."

First Inventor (Legal Name): Jefferey C. Solomon

Signature: Jeffrey Solomon Date (Optional): 10-14-2013

Second Inventor (Legal Name): Jayesh R. Bhakta

Signature: Jayesh Bhakta Date (Optional): 10-14-2013

Electronically filed August 16, 2021

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of:	Jefferey C. Solomon	Confirmation No.:	TBA
Serial No.:	Filed Herewith	Art Unit	TBA
Filed:	August 16, 2021	Examiner:	TBA
For:	MEMORY MODULE WITH DATA BUFFERING	Attorney Docket No.:	NL023-02US

STATEMENT UNDER 37 C.F.R. § 3.73(c)

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

NETLIST, INC., a corporation, states that it is the assignee of the entire right, title and interest in the patent application/patent identified above by virtue of an assignment from the inventor(s) of the parent of the patent application/patent identified above.

The assignment was recorded in the United States Patent and Trademark Office on July 17, 2006 at Reel 018104, Frame 0964, or for which a copy thereof is attached.

The undersigned is authorized to act on behalf of the assignee.

Date: August 16, 2021

/ Jamie J. Zheng / 51,167
Jamie J. Zheng (Reg. No.)
Customer No. 79141

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GENERAL POWER OF ATTORNEY BY APPLICANT FOR UNITED STATES PATENT

I hereby revoke all previous powers of attorney given in the application referenced in the attached transmittal letter (form PTO/AIA/82A or equivalent).

I hereby appoint the practitioner associated with the following Customer Number :

79141

as my/our attorney or agent, and to transact all business in the United States Patent and Trademark Office in connection with the application referenced in the attached transmittal letter (form PTO/AIA/82A or equivalent).

Please recognize or change the **correspondence address** for the application referenced in the attached transmittal letter to the address associated with the above-mentioned **Customer Number**.

I am the Applicant:

☐ Inventor or Joint Inventor

☐ Legal Representative of a Deceased or Legally Incapacitated Inventor

■ Assignee or Person to Whom the Inventor is Under an Obligation to Assign

☐ Person Who Otherwise Shows Sufficient Proprietary Interest (e.g., a petition under 37 CFR 1.46(b)(2) was granted in the application or is currently being filed in this document)

SIGNATURE of Applicant for Patent

Signature		Date: January 9, 2013
Name	**Gail Sasaki**	
Title	Vice President and Chief Financial Officer	
Company	Netlist, Inc.	

Note: Signature - this form must be signed by the Applicant or a person authorized to act on behalf of Applicant.

Submit multiple forms for more than one signature
Total of __ forms are submitted.

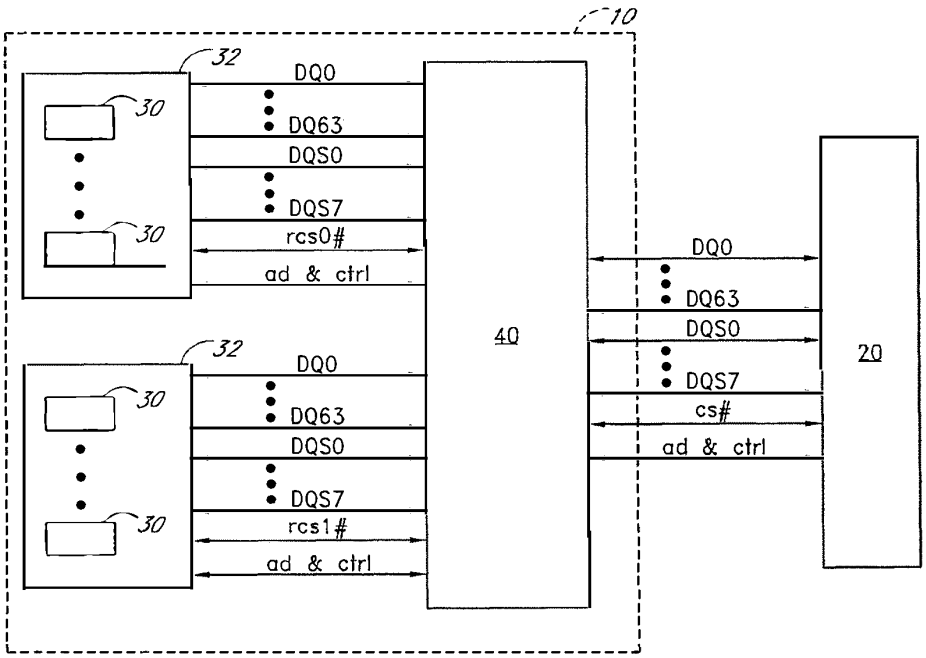

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32
30
30
DQ0
DQ63
DQS0
DQS7
rcs0#
ad & ctrl
32
30
30
DQ0
DQ63
DQS0
DQS7
rcs1#
ad & ctrl
40
DQ0
DQ63
DQS0
DQS7
cs#
ad & ctrl
20

FIG. 1

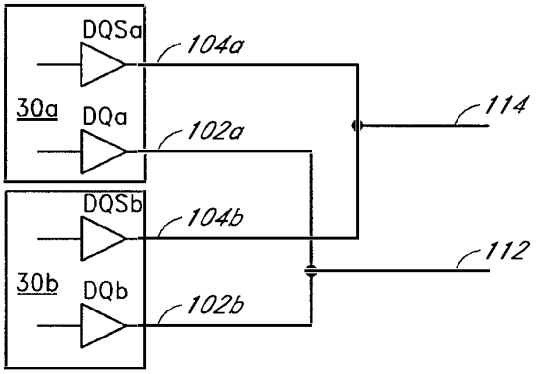


FIG. 2

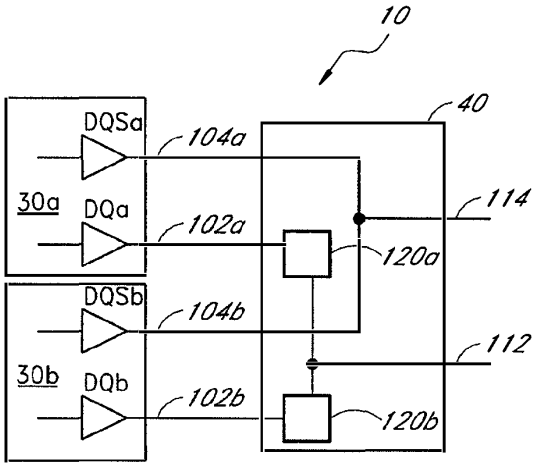

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104b
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FIG. 3A

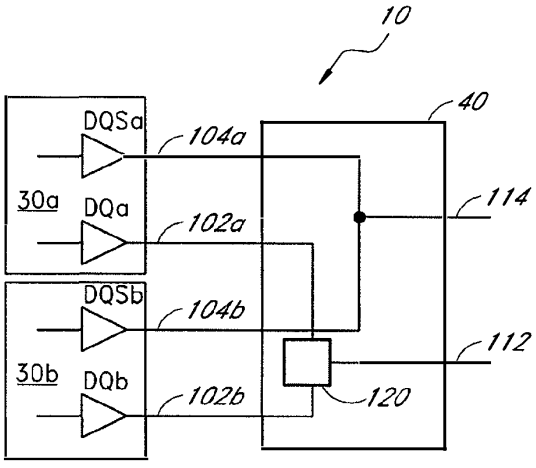

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30b
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120

FIG. 3B

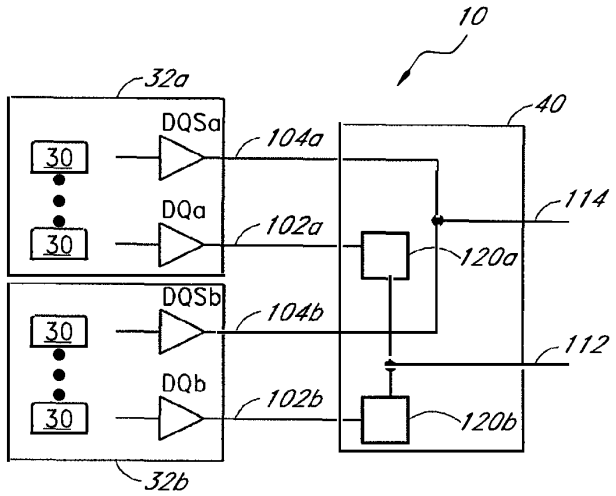

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32a
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104a
30
30
DQa
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40
114
120a
DQSb
104b
30
30
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102b
112
120b
32b

FIG. 4A

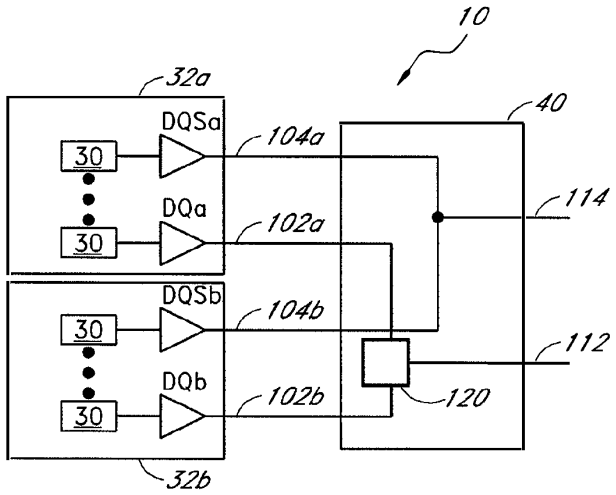

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40
114
DQSb
104b
30
30
DQb
102b
112
120
32b

FIG. 4B

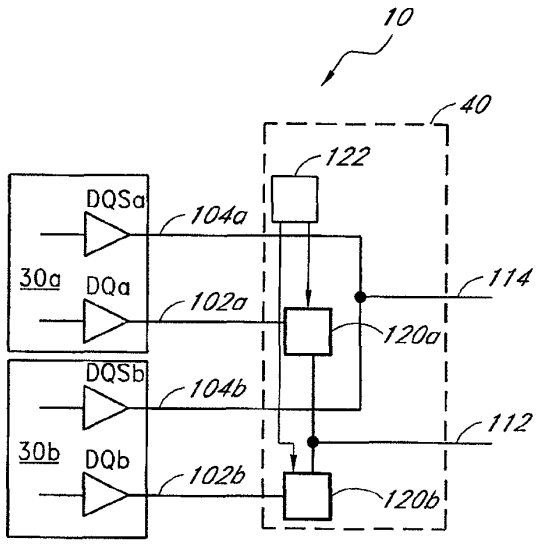

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DQa
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114
120a
DQSb
104b
112
30b
DQb
102b
120b

FIG. 5A

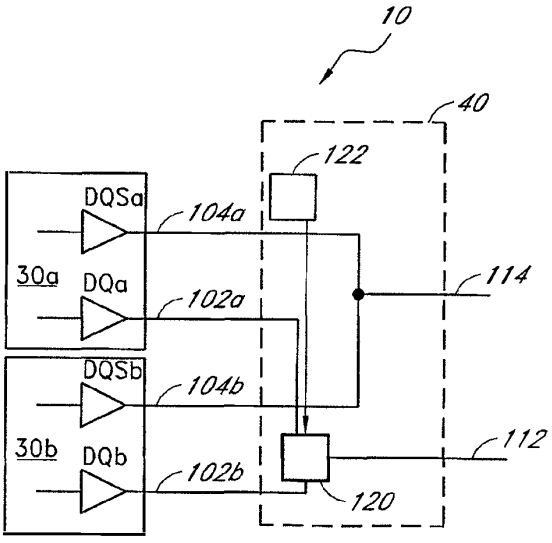

10
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30a
DQa
102a
114
DQSb
104b
112
30b
DQb
102b
120

FIG. 5B

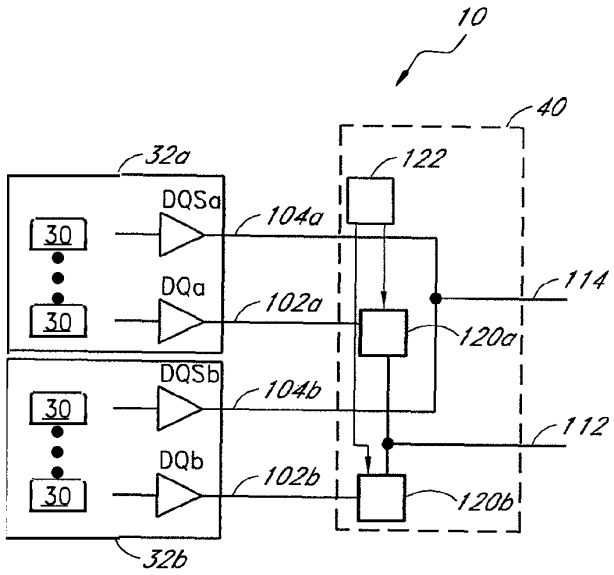

10
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32a
122
DQSa
104a
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30
DQa
102a
114
120a
DQSb
104b
30
30
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102b
120b
32b

FIG. 5C

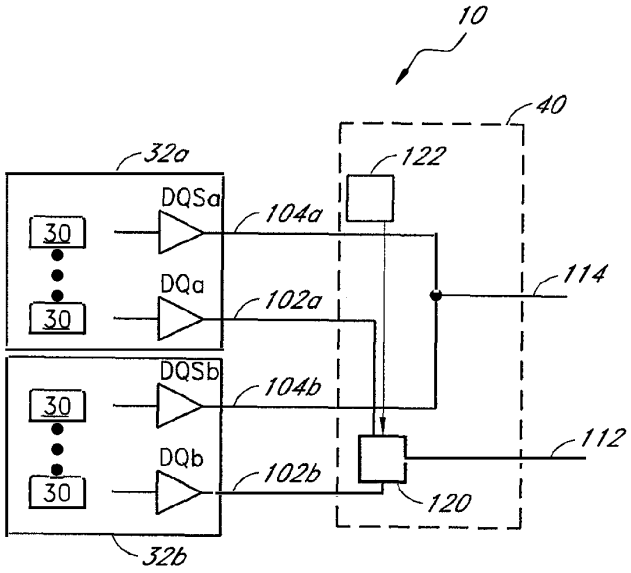

10
40
32a
122
DQSa
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30
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102a
114
DQSb
104b
30
30
112
DQb
102b
120
32b

FIG. 5D

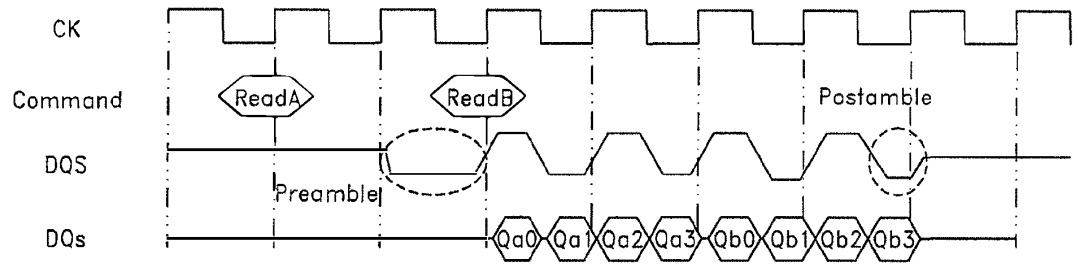


FIG. 6A

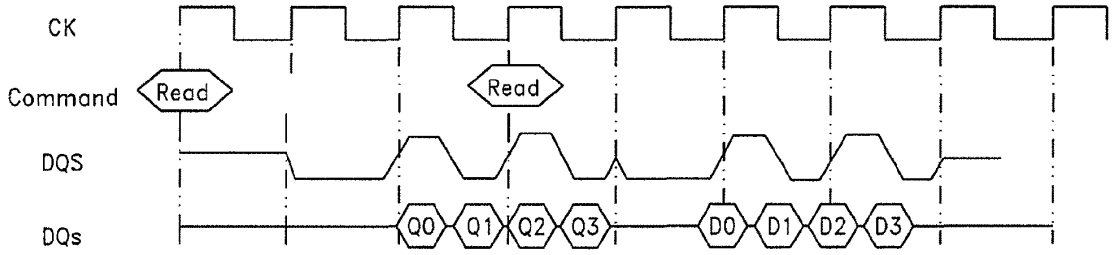


FIG. 6B

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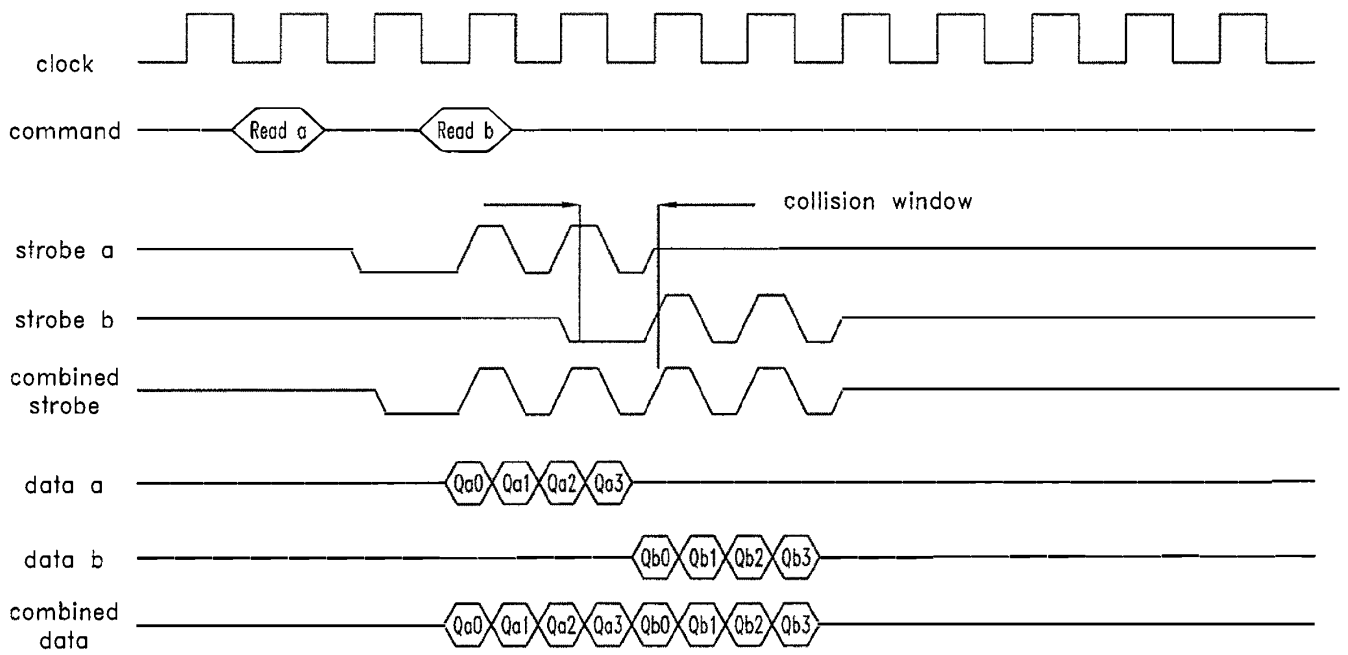

clock
command
Read a
Read b
collision window
strobe a
strobe b
combined strobe
data a
Qa0
Qa1
Qa2
Qa3
data b
Qb0
Qb1
Qb2
Qb3
combined data
Qa0
Qa1
Qa2
Qa3
Qb0
Qb1
Qb2
Qb3

FIG. 7

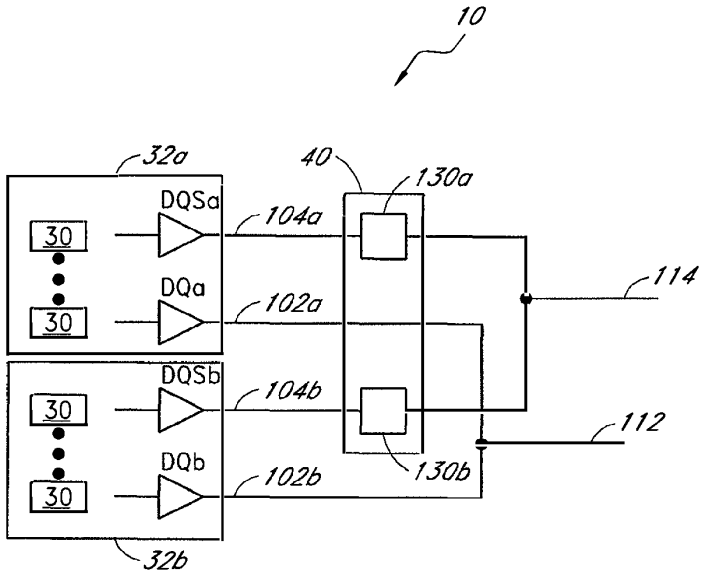

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102b
130b
32b

FIG. 8A

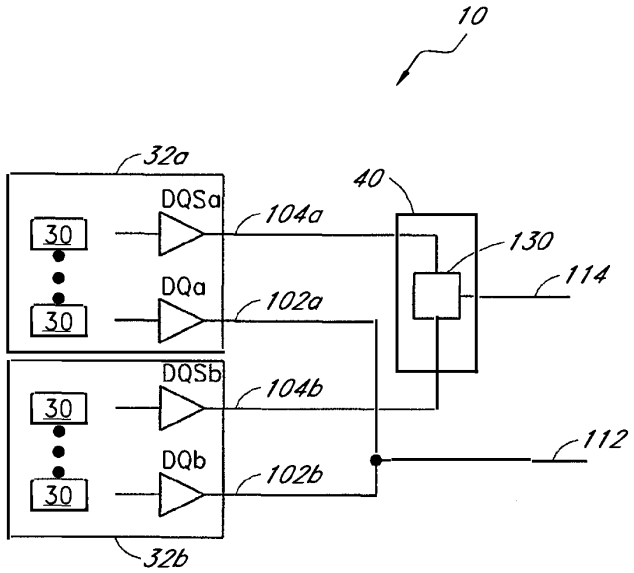

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DQb
102b
32b

FIG. 8B

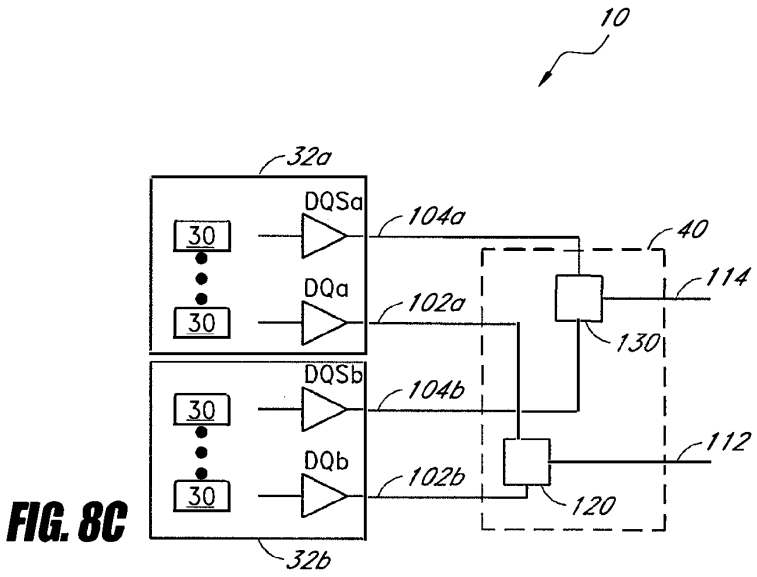

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120
32b

FIG. 8C

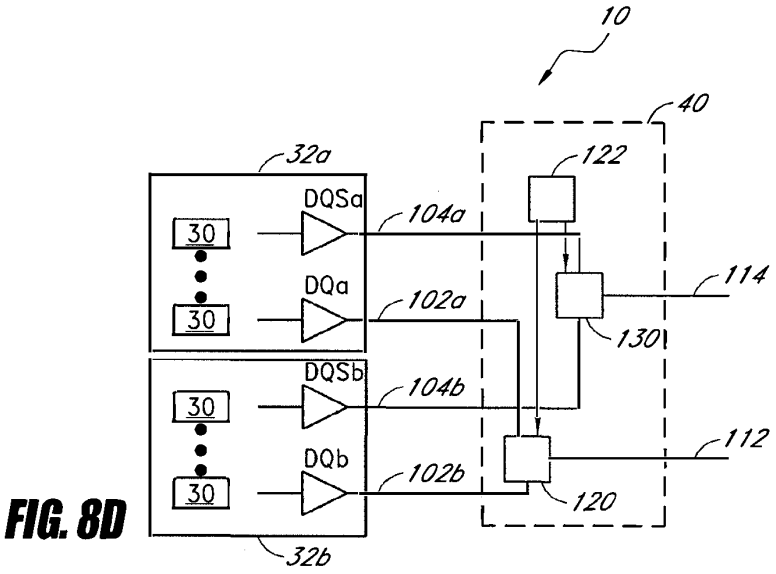

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32a
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104a
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30
130
DQSb
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30
112
DQb
102b
30
120
32b

FIG. 8D

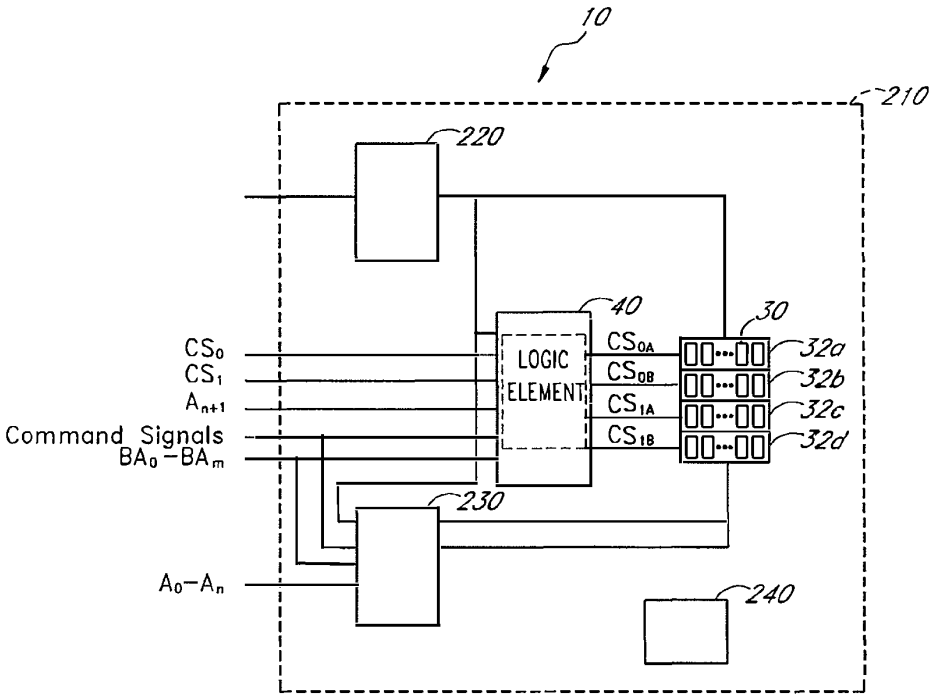

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LOGIC ELEMENT
CS0
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Command Signals
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CS0A
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A0–An
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FIG. 9A

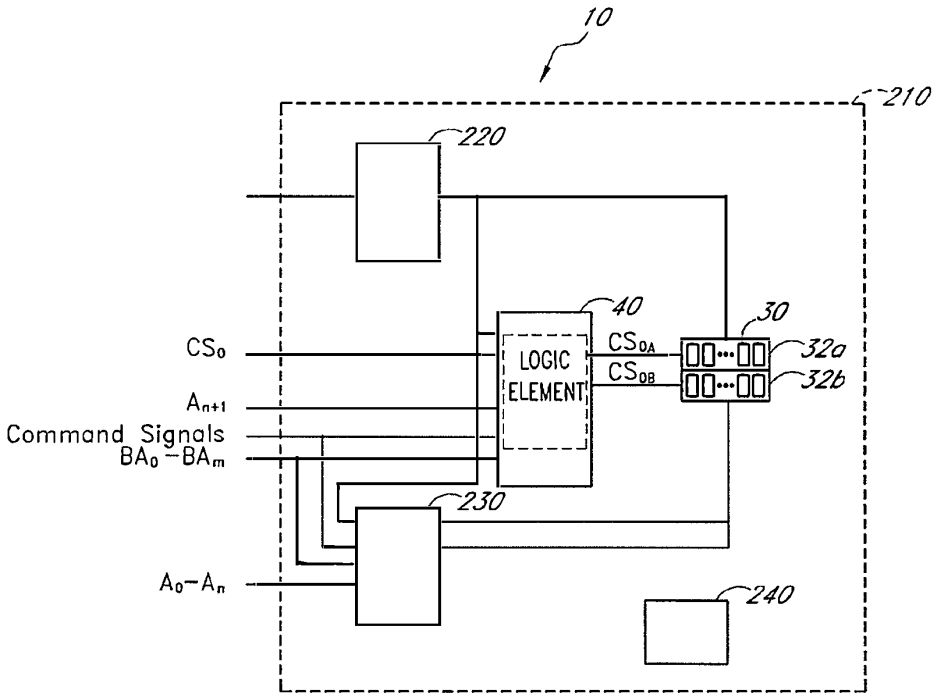

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LOGIC ELEMENT
CS0A
CS0B
32a
32b
CS0
An+1
Command Signals
BA0 – BAm
230
A0 – An
240

FIG. 9B

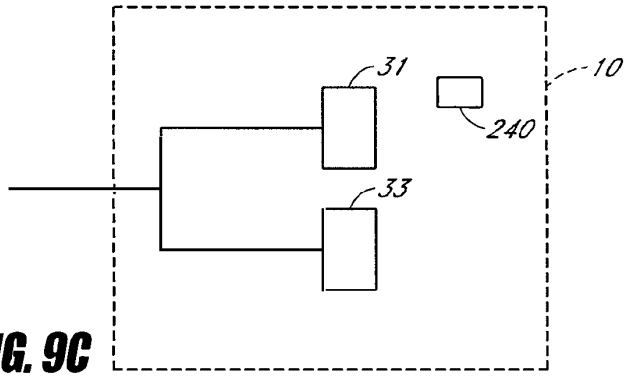


FIG. 9C

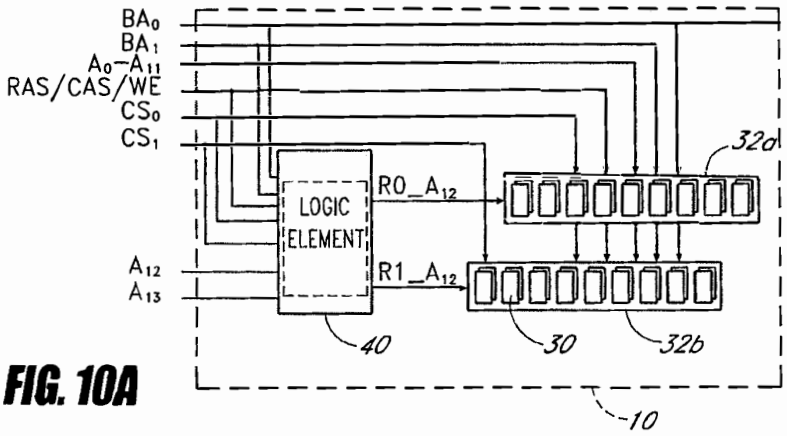


FIG. 10A

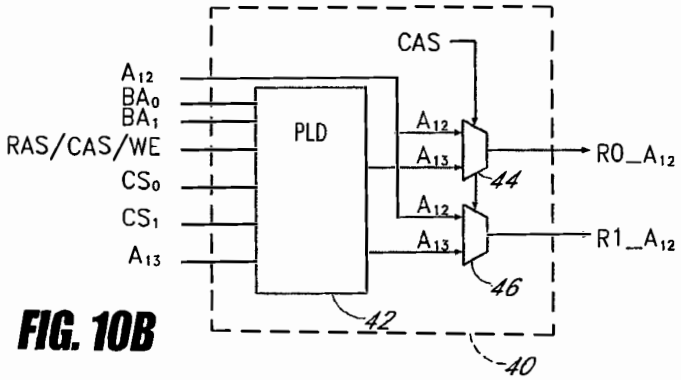


FIG. 10B

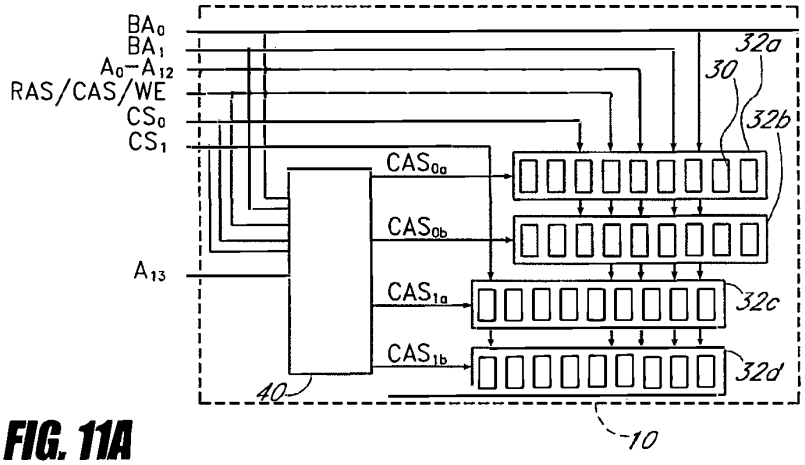


FIG. 11A

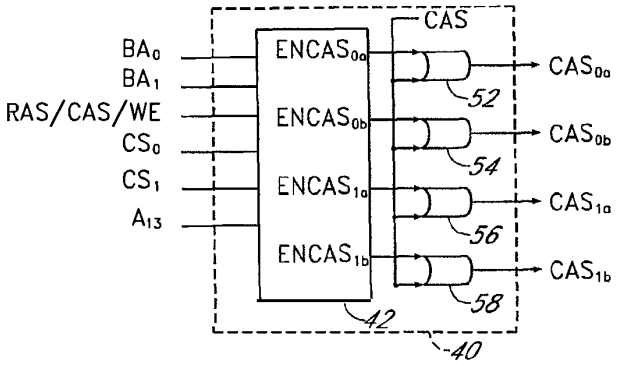


FIG. 11B

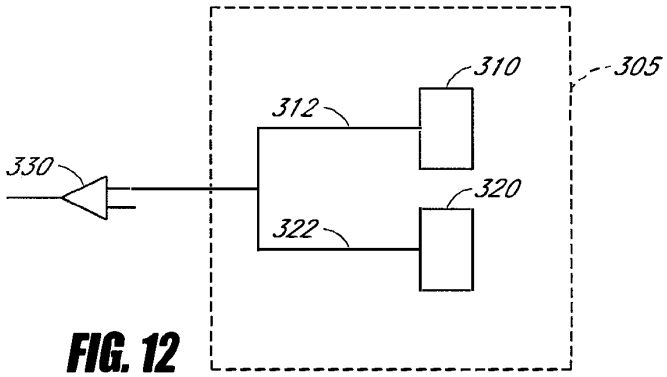


FIG. 12

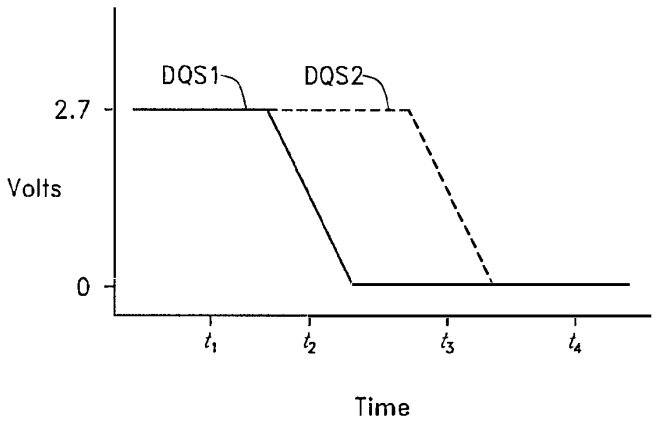


FIG. 13

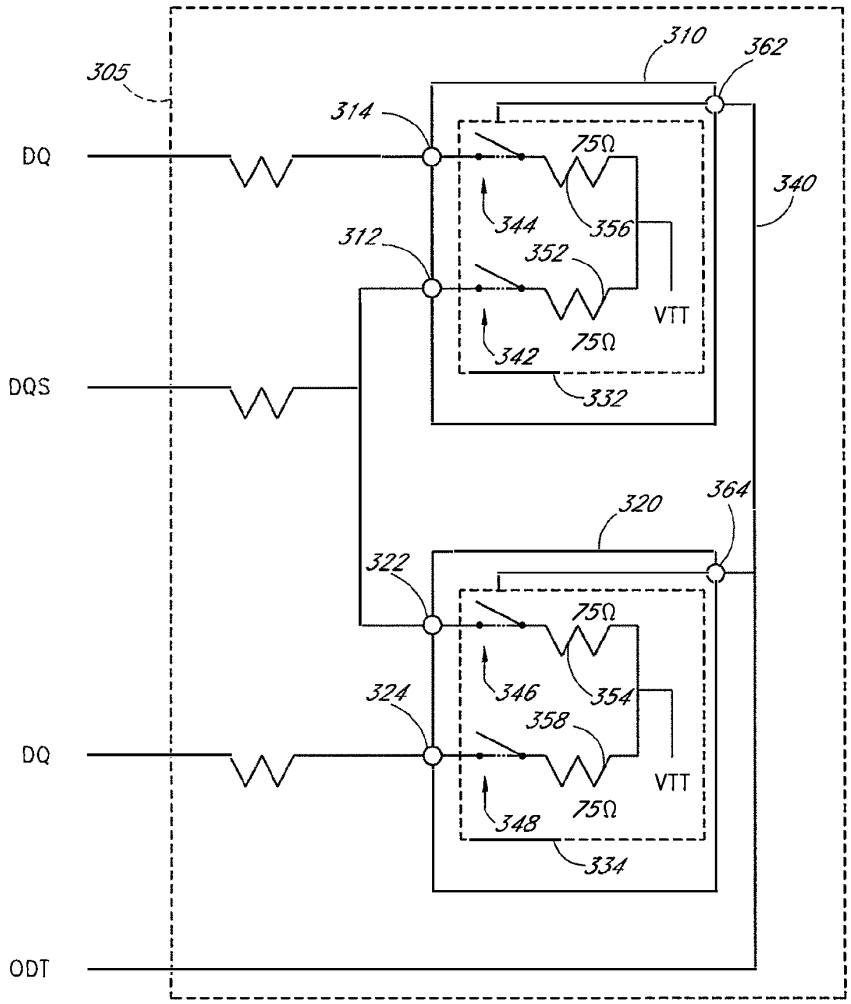

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FIG. 14

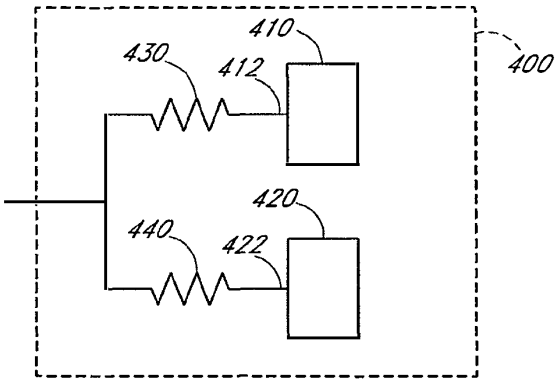


FIG. 15

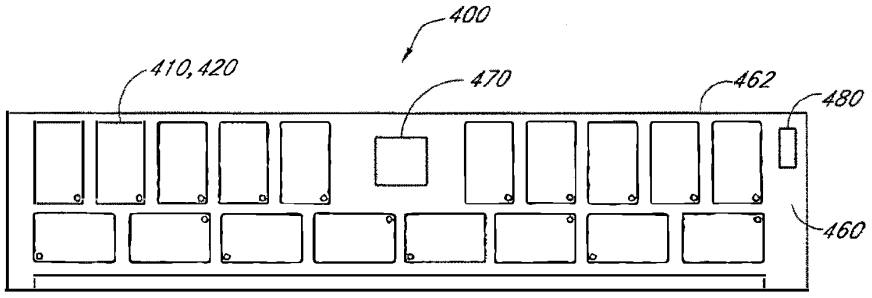


FIG. 16A

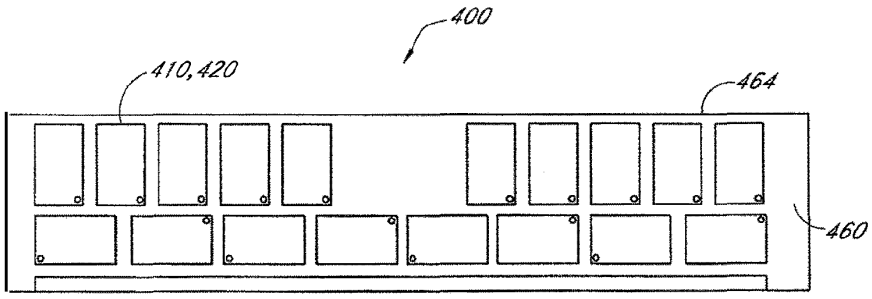


FIG. 16B

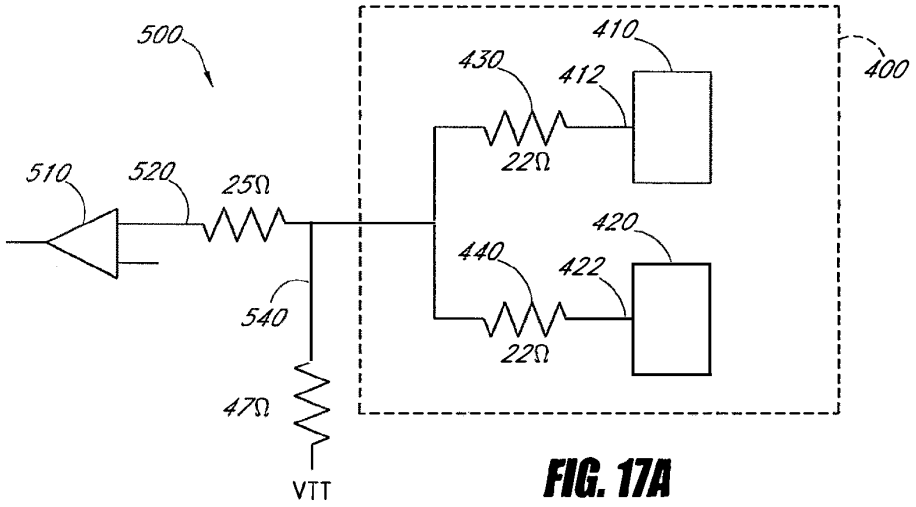


FIG. 17A

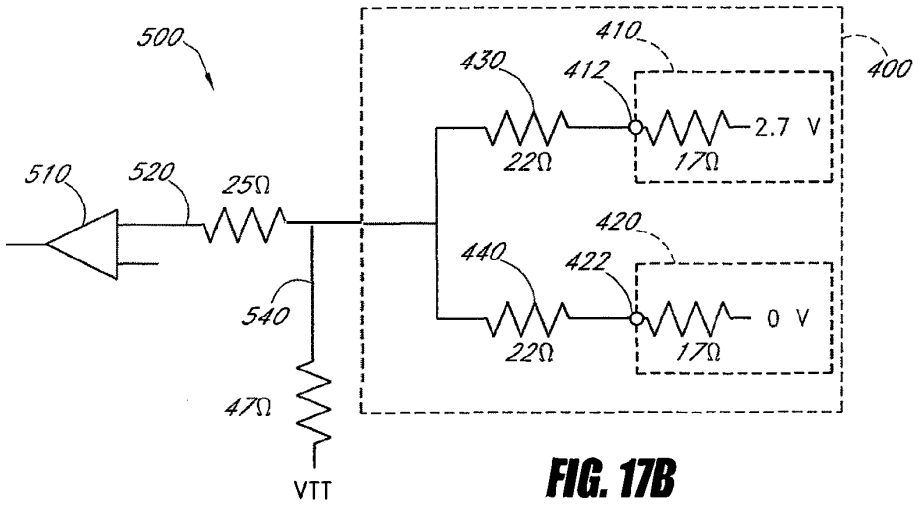


FIG. 17B

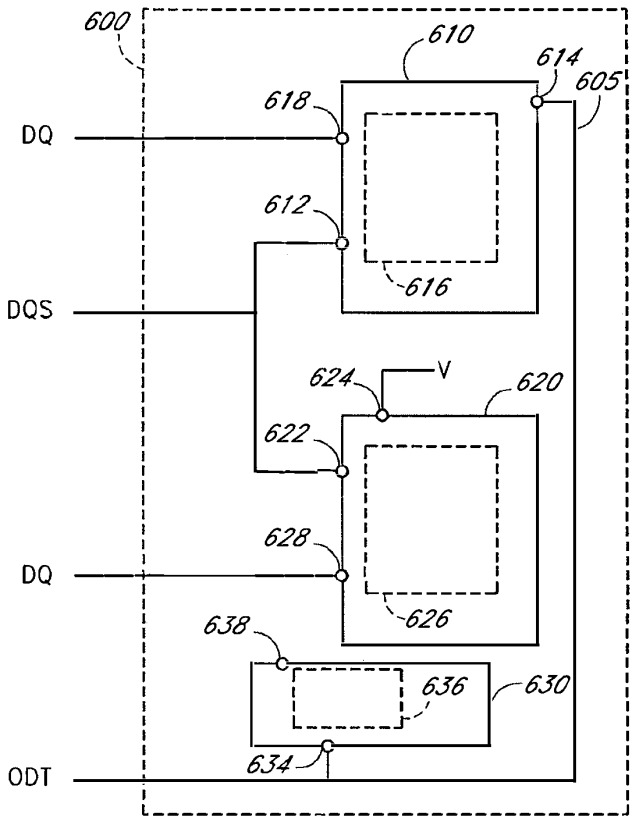

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FIG. 18

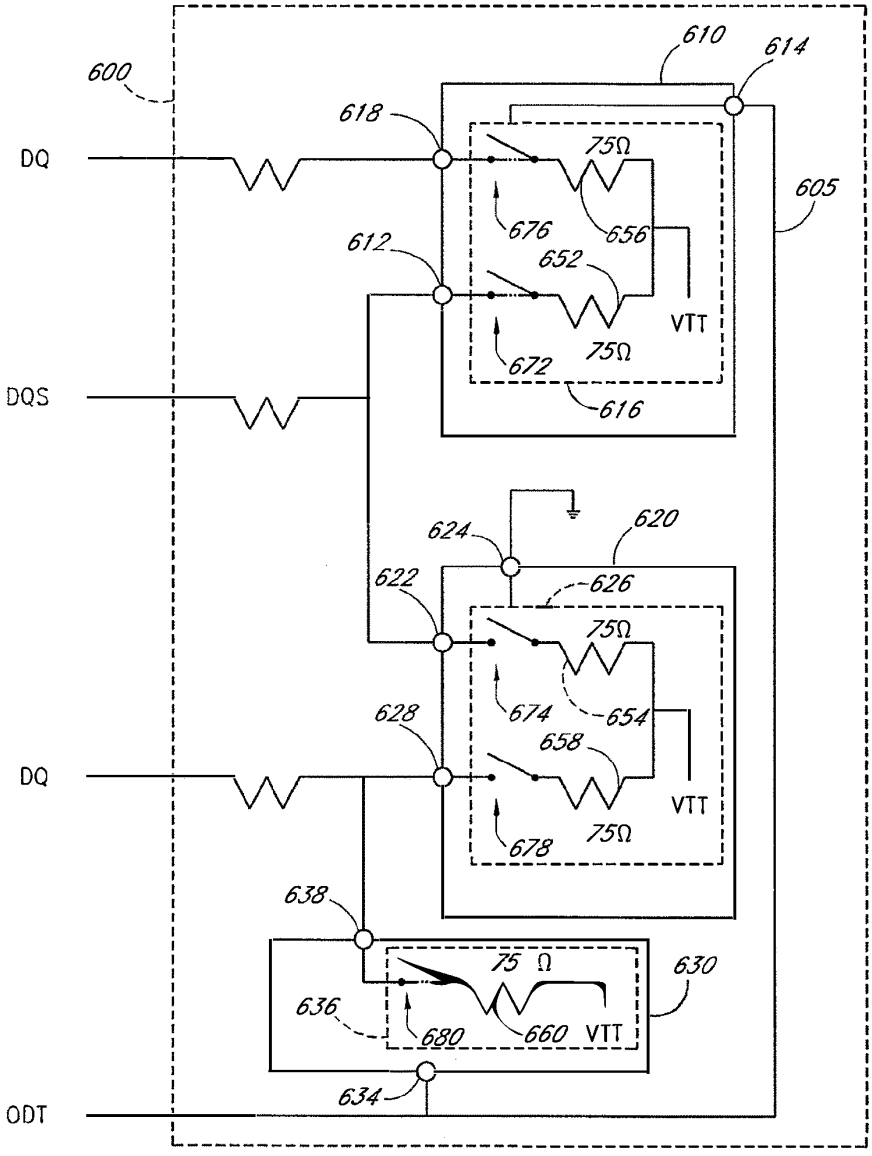

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FIG. 19

Electronic Patent Application Fee Transmittal

Application Number:	
Filing Date:	
Title of Invention:	MEMORY MODULE WITH DATA BUFFERING
First Named Inventor/Applicant Name:	Jefferey C. Solomon
Filer:	Jamie Jie Zheng
Attorney Docket Number:	NL023-02US02

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
UTILITY APPLICATION FILING	1011	1	320	320
UTILITY SEARCH FEE	1111	1	700	700
UTILITY EXAMINATION FEE	1311	1	800	800
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
		Total in USD ($)		**1820**

Electronic Acknowledgement Receipt	
EFS ID:	43524418
Application Number:	17403832
International Application Number:	
Confirmation Number:	3549
Title of Invention:	MEMORY MODULE WITH DATA BUFFERING
First Named Inventor/Applicant Name:	Jefferey C. Solomon
Customer Number:	79141
Filer:	Jamie Jie Zheng
Filer Authorized By:	
Attorney Docket Number:	NL023-02US02
Receipt Date:	16-AUG-2021
Filing Date:	
Time Stamp:	22:38:48
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	$1820
RAM confirmation Number	E20218FM41562067
Deposit Account	
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Transmittal of New Application	NL023-02US02_Appl_Transmittal.pdf	85233 c3b13bdc665da0fc905393f193347516977 47c42	no	1
Warnings:					
Information:					
2	Application Data Sheet	NL023-02US02_ADS.pdf	1257104 a5852b8cddfa3ba71f0a192e26426af6e08b 0eaf	no	10
Warnings:					
Information:					
3		NL023-02US02_Application.pdf	1040145 6d176c0124593cc14008f26c5f3878303e1d 6815	yes	57

Multipart Description/PDF files in .zip description		
Document Description	**Start**	**End**
Specification	1	53
Claims	54	56
Abstract	57	57

Warnings:					
Information:					
4	Oath or Declaration filed	NL023-02US02_OATH.pdf	67889 ab704ad8916a80dc8102fd47b36b942e00c 108f0	no	1
Warnings:					
Information:					
5	Assignee showing of ownership per 37 CFR 3.73	NL023-02US02_373_Statement.pdf	72716 565987dc5ed1413fcde58d9f92fe4471a4dd 4a71	no	2

Warnings:					
Information:					
6	Power of Attorney	General_POA_Netlist.pdf	151681 b397f182d5ebb2bff6bfab96b1036487015b2d89	no	1
Warnings:					
Information:					
7	Drawings-only black and white line drawings	NL023-02US02_Drawings.pdf	1005555 6ee751c18381663f933d2a9b5bf966ddbc7690a8	no	23
Warnings:					
Information:					
8	Fee Worksheet (SB06)	fee-info.pdf	43917 4e85a8d09541639b84259b23dc6b8700bce03b0b	no	2
Warnings:					
Information:					
			Total Files Size (in bytes):	3724240	

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If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.
<u>National Stage of an International Application under 35 U.S.C. 371</u>
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.
<u>New International Application Filed with the USPTO as a Receiving Office</u>
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number: 17/403,832

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY FEE($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	320
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	700
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	800
TOTAL CLAIMS (37 CFR 1.16(i))	12 minus 20 =	*			OR	x 100 =	0.00
INDEPENDENT CLAIMS (37 CFR 1.16(h))	1 minus 3 =	*				x 480 =	0.00
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	1820

APPLICATION AS AMENDED - PART II

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
AMENDMENT A	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE($)	ADDITIONAL FEE($)	OR	RATE($)	ADDITIONAL FEE($)
AMENDMENT B	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.

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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
17/403,832	08/16/2021	2139	1820	NL023-02US02	12	1

CONFIRMATION NO. 3549

79141
USCH Law, PC
3790 El Camino Real #1147
Palo Alto, CA 94304

FILING RECEIPT

OC000000127985221

Date Mailed: 08/27/2021

Receipt is acknowledged of this non-provisional utility patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF FIRST INVENTOR, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection.

Please verify the accuracy of the data presented on this receipt. If an error is noted on this Filing Receipt, please submit a written request for a corrected Filing Receipt, including a properly marked-up ADS showing the changes with strike-through for deletions and underlining for additions. If you received a "Notice to File Missing Parts" or other Notice requiring a response for this application, please submit any request for correction to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections provided that the request is grantable.

Inventor(s)

Jefferey C. Solomon, Irvine, CA;
Jayesh R. Bhakta, Cerritos, CA;

Applicant(s)

Netlist, Inc., Irvine, CA;

Power of Attorney: The patent practitioners associated with Customer Number 79141

Domestic Priority data as claimed by applicant

This application is a CON of 16/695,020 11/25/2019 PAT 11093417
which is a CON of 15/857,519 12/28/2017 PAT 10489314
which is a CON of 14/715,486 05/18/2015 PAT 9858215
which is a CON of 13/971,231 08/20/2013 PAT 9037774
which is a CON of 13/287,081 11/01/2011 PAT 8516188
which is a CON of 13/032,470 02/22/2011 PAT 8081536
which is a CON of 12/955,711 11/29/2010 PAT 7916574
which is a CON of 12/629,827 12/02/2009 PAT 7881150
which is a CON of 12/408,652 03/20/2009 PAT 7636274
which is a CON of 11/335,875 01/19/2006 PAT 7532537
which claims benefit of 60/645,087 01/19/2005
and is a CIP of 11/173,175 07/01/2005 PAT 7289386
which claims benefit of 60/588,244 07/15/2004
and is a CIP of 11/075,395 03/07/2005 PAT 7286436
which claims benefit of 60/550,668 03/05/2004

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Ex. 1059, p. 102

and claims benefit of 60/575,595 05/28/2004
and claims benefit of 60/590,038 07/21/2004

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.) - None.
Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

Permission to Access Application via Priority Document Exchange: Yes

Permission to Access Search Results: Yes

Applicant may provide or rescind an authorization for access using Form PTO/SB/39 or Form PTO/SB/69 as appropriate.

If Required, Foreign Filing License Granted: 08/25/2021

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 17/403,832**

Projected Publication Date: 12/02/2021

Non-Publication Request: No

Early Publication Request: No
Title

MEMORY MODULE WITH DATA BUFFERING

Preliminary Class

711

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

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Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

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Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

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Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
17/403,832	08/16/2021	Jefferey C. Solomon	NL023-02US02

CONFIRMATION NO. 3549

79141
USCH Law, PC
3790 El Camino Real #1147
Palo Alto, CA 94304

PUBLICATION NOTICE

OC000000130352019

Title:MEMORY MODULE WITH DATA BUFFERING

Publication No.US-2021-0382834-A1
Publication Date:12/09/2021

NOTICE OF PUBLICATION OF APPLICATION

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				First Named Inventor	*Jefferey C. Solomon*
				Art Unit	*2139*
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				First Named Inventor	*Jefferey C. Solomon*
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				First Named Inventor	*Jefferey C. Solomon*
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	420.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Exhibit 3001 to Final Decision, issued September 28, 2016
	421.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Exhibit 3001-2 to Final Decision, issued September 28, 2016
	422.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Exhibit 3002 to Final Decision, issued September 28, 2016
	423.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Exhibit 3003 to Final Decision, issued September 28, 2016
	424.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Exhibit 3004 to Final Decision, issued September 28, 2016
	425.	Inter Partes Review of U.S. Patent No. 8081536, Case No. IPR2015-01021, Patent Owner Response to Petition, filed February 22, 2016
	426.	Inter Partes Review of U.S. Patent No. 8081536, Case No. IPR2015-01021, Exhibit 2001, "Declaration of Professor Carl Sechen," filed February 22, 2016
	427.	Inter Partes Review of U.S. Patent No. 8081536, Case No. IPR2015-01021, Petitioner's Objections to Evidence, filed February 29, 2016
	428.	Inter Partes Review of U.S. Patent No. 8081536, Case No. IPR2015-01021, Petitioner's Reply, filed May 19, 2016
	429.	Inter Partes Review of U.S. Patent No. 8081536, Case No. IPR2015-01021, Supplemental Declaration of Dr. Jagannathan, filed May 19, 2016
	430.	Inter Partes Review of U.S. Patent No. 8081536, Case No. IPR2015-01021, Petitioner Request for Oral Argument, filed June 2, 2016
	431.	Inter Partes Review of U.S. Patent No. 8081536, Case No. IPR2015-01021, PATENT OWNER MOTION FOR OBSERVATIONS, filed June 2, 2016
	432.	Inter Partes Review of U.S. Patent No. 8081536, Case No. IPR2015-01021, PATENT OWNER REQUEST FOR ORAL ARGUMENT, filed June 2, 2016

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				First Named Inventor	*Jefferey C. Solomon*
				Art Unit	*2139*
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	433.	Inter Partes Review of U.S. Patent No. 8081536, Case No. IPR2015-01021, Patent Owner's SUBMISSION ON PROPRIETY OF PETITIONER REPLY, filed June 9, 2016
	434.	Inter Partes Review of U.S. Patent No. 8081536, Case No. IPR2015-01021, Petitioner's Response to Motion for Observations, filed June 10, 2016
	435.	Inter Partes Review of U.S. Patent No. 8081536, Case No. IPR2015-01021, Petitioner's Response to Patent Owner's Submission, filed June 13, 2016
	436.	Inter Partes Review of U.S. Patent No. 8081536, Case No. IPR2015-01021, Patent Owner's Objections to Petitioner's Demonstrative Exhibits, filed June 23, 2016
	437.	Inter Partes Review of U.S. Patent No. 8081536, Case No. IPR2015-01021, Patent Owner's Demonstrative Exhibits, filed June 24, 2016
	438.	Inter Partes Review of U.S. Patent No. 8081536, Case No. IPR2015-01021, Petitioner's Updated Exhibit List, filed June 24, 2016
	439.	Inter Partes Review of U.S. Patent No. 8081536, Case No. IPR2015-01021, Final Decision, issued September 28, 2016
	440.	Inter Partes Review of U.S. Patent No. 8756364, Case No. IPR2017-00549, Petition for Inter Partes Review, filed December 30, 2016
	441.	Inter Partes Review of U.S. Patent No. 8756364, Case No. IPR2017-00549, Exhibit 1003, "Declaration of Harold S. Stone," filed December 30, 2016
	442.	Inter Partes Review of U.S. Patent No. 8756364, Case No. IPR2017-00549, Exhibit 1008, Declaration of John J. Kelly Regarding Records of Joint Electron Device Engineering Council (JEDEC), filed December 30, 2016
	443.	Inter Partes Review of U.S. Patent No. 8,756,364, Case No. IPR2017-00549, DECISION Institution of Inter Partes Review, filed May 15, 2017.
	444.	Inter Partes Review of U.S. Patent No. 8,756,364, Case No. IPR2017-00549, Exhibit 2001 (DECLARATION OF PROFESSOR CARL SECHEN), filed September 15, 2017.
	445.	Inter Partes Review of U.S. Patent No. 8,756,364, Case No. IPR2017-00549, Patent Owner's Response, filed September 15, 2017.
	446.	Inter Partes Review of U.S. Patent No. 8,756,364, Case No. IPR2017-00549, PETITIONERS' OBJECTIONS TO EVIDENCE, filed September 15, 2017.
	447.	Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, Deposition Transcript of Carl Sechen, filed December 15, 2017.
	448.	Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, Petitioner's reply to Patent Owner's Response, filed December 15, 2017.

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				First Named Inventor	*Jefferey C. Solomon*
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	449.	Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, Supplemental Declaration of Harold S. Stone, filed December 15, 2017.
	450.	Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, Xilinx Xilinx CS280 package datasheet (1999), filed December 15, 2017.
	451.	Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, EXHIBIT 2004, filed January 9, 2017.
	452.	Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, Patent Owner's Motion for Observations, filed January 9, 2017.
	453.	Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, Petitioner's Motion to Exclude Certain Inadmissible Testimony of Patent Owner's Expert Carl Sechen, filed January 9, 2017.
	454.	Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, EXHIBIT 2003, 'Synchronous DRAM Architectures, Organization, and Alternative Technologies,' filed January 18, 2017.
	455.	Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, Petitioner's Response to Patent Owners Motion for Observations, filed January 23, 2018.
	456.	Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, Patent Owner's Opposition to Petitioner's Motion to Exclude, filed January 23, 2018.
	457.	Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, Petitioner's Reply in Support of Motion to Exclude Certain Inadmissible Testimony of Patent Owner's Expert Carl Sechen, filed January 30, 2018.
	458.	Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, Petitioner's Demonstratives, filed February 9, 2018.
	459.	Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, EXHIBIT 2005, filed February 9, 2018.
	460.	Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, Patent Owner's Updated Exhibit List, filed February 9, 2018.
	461.	Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, Petitioner's Updated Exhibit List, filed February 9, 2018.
	462.	Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, Final Written Decision, filed February 14, 2018.
	463.	Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, Hearing Transcript, filed February 14, 2018.
	464.	Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, Patent Owner's Supplemental Mandatory Notices, filed April 19, 2018.

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	465.	Inter Partes Review of U.S. Patent No. 8516185, Case No. IPR2017-00577, Petition for Inter Partes Review, filed January 5, 2017
	466.	Inter Partes Review of U.S. Patent No. 8516185, Case No. IPR2017-00577, Exhibit 1003, "Declaration of Harold S. Stone," filed January 5, 2017
	467.	Inter Partes Review of U.S. Patent No. 8,516,185, Case No. IPR2017-00577, DECISION Institution of Inter Partes Review, filed July 7, 2017.
	468.	Inter Partes Review of U.S. Patent No. 8,516,185, Case No. IPR2017-00577, SCHEDULING ORDER, filed July 7, 2017.
	469.	Inter Partes Review of U.S. Patent No. 8,516,185, Case No. IPR2017-00577, Exhibit 2003 (DECLARATION OF R. JACOB BAKER, PH.D., P.E.), filed October 25, 2017.
	470.	Inter Partes Review of U.S. Patent No. 8,516,185, Case No. IPR2017-00577, Exhibit 2004 (Deposition of HAROLD S. STONE, PH.D.), filed October 25, 2017.
	471.	Inter Partes Review of U.S. Patent No. 8,516,185, Case No. IPR2017-00577, Exhibit 2005 (Memory Systems: Cache, DRAM, Disk), filed October 25, 2017.
	472.	Inter Partes Review of U.S. Patent No. 8,516,185, Case No. IPR2017-00577, Exhibit 2006 (PC2100 and PC1600 DDR SDRAM Registered DIMM, Design Specification, Revision 1.3, January 2002), filed October 25, 2017.
	473.	Inter Partes Review of U.S. Patent No. 8,516,185, Case No. IPR2017-00577, Exhibit 2007 (DRAM CIRCUIT DESIGN: Fundamental and High-Speed Topics), filed October 25, 2017.
	474.	Inter Partes Review of U.S. Patent No. 8,516,185, Case No. IPR2017-00577, PATENT OWNER'S RESPONSE, filed October 25, 2017.
	475.	Inter Partes Review of U.S. Patent No. 8,516,185, Case No. IPR2017-00577, PETITIONERS' OBJECTIONS TO EVIDENCE, filed October 31, 2017.
	476.	Inter Partes Review of US Patent No.8516185, Case No. IPR2017-00577, Annotated version of Halbert Figure 4 showing 4:1 MUX/DeMUX and 4 ranks of memory (corrected Ex. 1035), filed February 6, 2018.
	477.	Inter Partes Review of US Patent No.8516185, Case No. IPR2017-00577, Annotated version of Halbert Figure 4 showing 4:1 MUX/DeMUX and 4 ranks of memory, filed February 6, 2018.
	478.	Inter Partes Review of US Patent No.8516185, Case No. IPR2017-00577, Annotated version of Halbert Figure 4 showing Fast components and Slow components, filed February 6, 2018.
	479.	Inter Partes Review of US Patent No.8516185, Case No. IPR2017-00577, Deposition Transcript of R. Jacob Baker (Jan. 12, 2018.), filed February 6, 2018.

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				First Named Inventor	*Jefferey C. Solomon*
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	480.	Inter Partes Review of US Patent No.8516185, Case No. IPR2017-00577, Excerpts from Brent Keeth and R. Jacob Baker, DRAM Circuit Design: A Tutorial (IEEE Press 2001), filed February 6, 2018.
	481.	Inter Partes Review of US Patent No.8516185, Case No. IPR2017-00577, Oral Testimony of R. Jacob Baker in Certain Memory Modules and Components Thereof, and Products Containing Same, Inv. No. 337-TA-1023 (May 11, 2017), filed February 6, 2018.
	482.	Inter Partes Review of US Patent No.8516185, Case No. IPR2017-00577, Petitioners' Reply to Patent Owner's Response, filed February 6, 2018.
	483.	Inter Partes Review of US Patent No.8516185, Case No. IPR2017-00577, Patent Owner's Objections to Evidence, filed February 13, 2018.
	484.	Inter Partes Review of US Patent No.8516185, Case No. IPR2017-00577, Patent Owner's Motion to Exclude, filed February 28, 2018.
	485.	Inter Partes Review of US Patent No.8516185, Case No. IPR2017-00577, Patent Owner's Request for Oral Argument, filed February 28, 2018.
	486.	Inter Partes Review of US Patent No.8516185, Case No. IPR2017-00577, Petitioner's Opposition to Patent Owner's Motion to Exclude, filed March 14, 2018.
	487.	Inter Partes Review of US Patent No.8516185, Case No. IPR2017-00577, Patent Owner's Reply to Opposition to Motion to Exclude, filed March 21, 2018.
	488.	Inter Partes Review of US Patent No.8516185, Case No. IPR2017-00577, Hearing Transcript, filed April 6, 2018.
	489.	Inter Partes Review of US Patent No.8516185, Case No. IPR2017-00577, Termination Decision Document, filed July 7, 2018.
	490.	Inter Partes Review of U.S. Patent No. 7,532,537, Case No. IPR2017-00667, DECISION Institution of Inter Partes Review, filed July 21, 2017.
	491.	Inter Partes Review of US Patent No.7532537, Case No. IPR2017-00667, Petitioner's Objections to Evidence, filed November 14, 2017.
	492.	Inter Partes Review of US Patent No.7532537, Case No. IPR2017-00667, Petitioner's Supplemental Objections to Evidence, filed November 14, 2017.
	493.	Inter Partes Review of US Patent No.7532537, Case No. IPR2017-00667, Deposition of Carl Sechen, Ph.D. taken December 8, 2017, filed February 26, 2018.
	494.	Inter Partes Review of US Patent No.7532537, Case No. IPR2017-00667, Deposition of Carl Sechen, Ph.D. taken February 8, 2018., filed February 26, 2018.
	495.	Inter Partes Review of US Patent No.7532537, Case No. IPR2017-00667, Google, Inc. et al. v. Netlist, Inc., Appeal 2014-00777, filed February 26, 2018.

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				First Named Inventor	*Jefferey C. Solomon*
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	496.	Inter Partes Review of US Patent No.7532537, Case No. IPR2017-00667, Petitioner's Reply to Patent Owner's Response, filed February 26, 2018.
	497.	Inter Partes Review of US Patent No.7532537, Case No. IPR2017-00667, Patent Owner's Objections to Evidence, filed March 5, 2018.
	498.	Inter Partes Review of US Patent No.7532537, Case No. IPR2017-00667, Exhibit 2007, Deposition of Harold S. Stone, filed March 19, 2018.
	499.	Inter Partes Review of US Patent No.7532537, Case No. IPR2017-00667, Patent Owner's Motion for Observations, filed March 19, 2018.
	500.	Inter Partes Review of US Patent No.7532537, Case No. IPR2017-00667, Patent Owner's Request for Oral Argument, filed March 19, 2018.
	501.	Inter Partes Review of US Patent No.7532537, Case No. IPR2017-00667, Petitioner's Motion to Exclude, filed March 19, 2018.
	502.	Inter Partes Review of US Patent No.7532537, Case No. IPR2017-00667, Patent Owner's Submission on Propriety of Petitioners Reply, filed March 20, 2018.
	503.	Inter Partes Review of US Patent No.7532537, Case No. IPR2017-00667, Petitioner's Response to Patent Owner's Submission on Propriety of Petitioner's Reply and Supplemental Stone Declaration 1, filed March 27, 2018.
	504.	Inter Partes Review of US Patent No.7532537, Case No. IPR2017-00667, Petitioner's Reply in Support of its Motion to Exclude Certain Inadmissible Testimony of Patent Owner's Expert Carl Sechen, filed April 2, 2018.
	505.	Inter Partes Review of US Patent No.7532537, Case No. IPR2017-00667, Petitioner's Updated Mandatory Notices, filed April 2, 2018.
	506.	Inter Partes Review of US Patent No.7532537, Case No. IPR2017-00667, Petitioner's Response to Patent Owner's Motion for Observations, filed April 2, 2018.
	507.	Inter Partes Review of US Patent No.7532537, Case No. IPR2017-00667, Patent Owner's Objection to Petitioner's Demonstratives, filed April 20, 2018.
	508.	Inter Partes Review of US Patent No.7532537, Case No. IPR2017-00667, Hearing Transcript, filed April 24, 2018.
	509.	Inter Partes Review of US Patent No.7532537, Case No. IPR2017-00667, Final Written Decision, filed July 18, 2018.
	510.	Inter Partes Review of U.S. Patent No. 7,532,537, Case No. IPR2017-00668, DECISION Institution of Inter Partes Review, filed July 21, 2017.
	511.	Inter Partes Review of US Patent No.7532537B2, Case No. IPR2017-00668, Petitioner's Objections to Evidence, filed November 14, 2017.
	512.	Inter Partes Review of US Patent No.7532537B2, Case No. IPR2017-00668, Notice of Deposition of Carl Sechen, filed January 30, 2018.

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				First Named Inventor	*Jefferey C. Solomon*
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	513.	Inter Partes Review of US Patent No.7532537B2, Case No. IPR2017-00668, Petitioner's Supplemental Objections to Evidence, filed February 15, 2018.
	514.	Inter Partes Review of US Patent No.7532537B2, Case No. IPR2017-00668, Petitioner's Reply to Patent Owner's Response, filed February 26, 2018.
	515.	Inter Partes Review of US Patent No.7532537B2, Case No. IPR2017-00668, Patent Owner's Objections to Evidence, filed March 5, 2018.
	516.	Inter Partes Review of US Patent No.7532537B2, Case No. IPR2017-00668, Patent Owner's Motion for Observations, filed March 19, 2018.
	517.	Inter Partes Review of US Patent No.7532537B2, Case No. IPR2017-00668, Patent Owner's Request for Oral Argument, filed March 19, 2018.
	518.	Inter Partes Review of US Patent No.7532537B2, Case No. IPR2017-00668, Patent Owner's Submission on Propriety of Petitioner's Reply, filed March 20, 2018.
	519.	Inter Partes Review of US Patent No.7532537B2, Case No. IPR2017-00668, Petitioner's Response to Patent Owner's Submission on Propriety of Petitioner's Reply and Supplemental Stone Declaration, filed March 27, 2018.
	520.	Inter Partes Review of US Patent No.7532537B2, Case No. IPR2017-00668, Patent Owner's Opposition to Petitioner's Motion to Exclude, filed April 2, 2018.
	521.	Inter Partes Review of US Patent No.7532537B2, Case No. IPR2017-00668, Petitioner's Response to Patent Owner's Motion for Observations, filed April 2, 2018.
	522.	Inter Partes Review of US Patent No.7532537B2, Case No. IPR2017-00668, Petitioner's Reply in Support of its Motion to Exclude Certain Inadmissible Testimony of Patent Owner's Expert Carl Sechen, filed April 9, 2018.
	523.	Inter Partes Review of US Patent No.7532537B2, Case No. IPR2017-00668, Patent Owner's Objections to Petitioner's Demonstratives, filed April 20, 2018.
	524.	Inter Partes Review of US Patent No.7532537B2, Case No. IPR2017-00668, Hearing Transcript, filed April 24, 2018.
	525.	Inter Partes Review of US Patent No.7532537B2, Case No. IPR2017-00668, Final Written Decision, filed July 18, 2018.
	526.	Inter Partes Review of US Patent No.8756364, Case No. IPR2017.-00549, Xilinx CoolRunner XPLA3 CPLD product specification (2000), filed December 15, 2017.
	527.	Inter Partes Review of US Patent No.8756364, Case No. IPR2017.-00549, Xilinx Programmable Logic Design Quick Start Handbook (2004), filed December 15, 2017.
	528.	Inter Partes Review of US Patent No.8756364, Case No. IPR2017.-00549, Xilinx Xilinx TQFP package datasheet (2000), filed December 15, 2017.
	529.	Inter Partes Review of US Patent No.8756364, Case No. IPR2017.-00549, Xilinx Xilinx VQFP package datasheet (2002), filed December 15, 2017.

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	530.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Exhibit 1022, Decision Denying Institution of Inter Partes Review, filed December 16, 2014
	531.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Exhibit 1023, Decision Denying Institution of Inter Partes Review, filed March 9, 2015
	532.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Exhibit 1024, Excepts from the Hearing in Certain Memory Modules and Components Thereof, and Products Containing Same, filed May 8, 2017.
	533.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Exhibit 1025, Complainant Netlist, Inc., Initial Post-Hearing Brief , filed May 30, 2017.
	534.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Exhibit 1026, Respondents' Post-Hearing Brief , filed May 30, 2017.
	535.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Declaration of Dr. Harold Stone, filed December 22, 2017.
	536.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Exhibit 1003: Declaration of Dr. Harold Stone, filed December 22, 2017.
	537.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Exhibit 1027, Demonstrative-Graphics-from-hynix-post-hearing-brief, filed December 22, 2017.
	538.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Exhibit 1028, Netlist-reply-post-hearing-brief, filed December 22, 2017.
	539.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Exhibit 1029, Respondent's Reply Post-Hearing Brief, filed December 22, 2017.
	540.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Exhibit 1030, High-Quality Versions of Demonstrative-Graphics-from-hynix-reply-post-hearing-brief, filed December 22, 2017.
	541.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Exhibit 1031, Institution of the '185 patent, filed December 22, 2017.
	542.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Exhibit 1032, Final Written Decision, Diablo Techs., Inc v. Netlist Inc., Paper No. 33, filed December 22, 2017.
	543.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Exhibit 1033, Decision, Netlist Inc., v. Diablo Techs., Inc., filed December 22, 2017.
	544.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Exhibit 1034, Netlist's Infringement Claim Chart of , filed December 22, 2017.

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	545.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Exhibit 1035, Stone, H.S. Microcomputer Interfacing, Reading, MA Addison Wesley, filed December 22, 2017.
	546.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Exhibit 1039, Intel E7525 Memory Controller Hub (MCH) Chipset Datasheet, filed December 22, 2017.
	547.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Exhibit 1040, Initial Determination, Certain Memory Modules and Components Thereof, and Products Containing Same, filed December 22, 2017.
	548.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Exhibit 1041, MEMORY-SYSTEMS-Cache-DRAM-Disk, Bruce Jacobs et al., filed December 22, 2017.
	549.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Exhibit 1042, Direct DRAM Datasheet, Bruce Jacobs et al., filed December 22, 2017.
	550.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Petition, filed December 22, 2017.
	551.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Exhibit 1011: JEDEC Standard DDR2 SDRAM Specification, JESD79-2B (January 2005), filed December 27, 2017.
	552.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Notice of Accorded Filing Date, filed January 10, 2018.
	553.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Patent Owner's Preliminary Response, filed April 10, 2018.
	554.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Granting Institution of Inter Partes Review, filed June 29, 2018.
	555.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Patent Owner's Objection to Petition Evidence, filed July 16, 2018.
	556.	Inter Partes Review of US Patent No. 9,606,907 B2, Case No. IPR2018-00362, and Case No. IPR2018-00363, EXHIBIT 3001, 'email from Mehran Arjomand,' filed July 30, 2018.
	557.	Inter Partes Review of US Patent No. 9,606,907 B2, Case No. IPR2018-00362, and Case No. IPR2018-00363, EXHIBIT 3001, 'email from Michael D. Hatcher,' filed July 30, 2018.
	558.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Order 37 C.F.R. 42.5, filed August 2, 2018.

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				First Named Inventor	*Jefferey C. Solomon*
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	575.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Petitioners' Request for Oral Argument, filed February 19, 2019.
	576.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Corrected Petitioners' Reply to Patent Owner's Response, filed February 20, 2019.
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				First Named Inventor	*Jefferey C. Solomon*
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	626.	Order Granting Request for Inter Partes Reexamination mailed January 18, 2011, for Control No. 95/000,577, filed October 20, 2010, 17 pages.
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	649.	Non-Final Action Closing Prosecution mailed June 21, 2011, for Control No. 95/001,381, filed June 9, 2010, 34 pages.
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	651.	Non-Final Action mailed June 15, 2011, for Control No. 95/001,381, filed June 9, 2010, 33 pages.
	652.	Right of appeal Notice mailed February 7, 2012, for Control No. 95/001,381, 33 pages.
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	667.	Other Reference-Patent/App/Search documents dated 11/22/2016 for Reexamination Control No. 95/001337
	668.	Patent Owner Comments on Examiner's Determination after Board Decision dated 02/22/2017 for Reexamination Control No. 95/001337
	669.	Patent Owner Comments on Examiner's Determination after Board Decision dated 10/14/2015 for Reexamination Control No. 95/001337
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	674.	Petition under Rule 41.3 to Chief Admin Patent Judge dated 11/22/2016 for Reexamination Control No. 95/001337
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	692.	Examiner's Determination on Patent Owner Response/Requester Comments after Board Decision dated 06/15/2015 for Reexamination Control No. 95/001337
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	857.	U.S. District Court Northern District of California, Case No. 4:13-CV-05889-YGR, Netlist, Inc. v. Smart Storage Systems, Inc., and Diablo Technologies, Inc., Diablo Technologies, Inc.'s Invalidity Contentions, dated June 6, 2014.
	858.	U.S. District Court Northern District of California, Case No. 4:13-CV-05889-YGR, Netlist, Inc. v. Smart Storage Systems, Inc., and Diablo Technologies, Inc., Exhibits F-1 to F-5 to "Diablo Technologies, Inc.'s Invalidity Contentions," dated June 6, 2014.
	859.	U.S. District Court Northern District of California, Case No. 4:13-CV-05889-YGR, Netlist, Inc. v. Smart Storage Systems, Inc., and Diablo Technologies, Inc., Exhibits G-1 to G-6 to "Diablo Technologies, Inc.'s Invalidity Contentions," dated June 6, 2014.
	860.	U.S. District Court Northern District of California, Case No. 4:13-CV-05889-YGR, Netlist, Inc. v. Smart Storage Systems, Inc., and Diablo Technologies, Inc., Exhibit H to "Diablo Technologies, Inc.'s Invalidity Contentions," dated June 6, 2014.
	861.	U.S. District Court Northern District of California, Case No. 4:13-CV-05889-YGR, Netlist, Inc. v. Smart Storage Systems, Inc., and Diablo Technologies, Inc., Smart Storage Systems, Inc.'s Invalidity Contentions, dated June 6, 2014
	862.	U.S. District Court Northern District of California, Case No. 4:13-CV-05889-YGR, Netlist, Inc. v. Smart Storage Systems, Inc., and Diablo Technologies, Inc., Exhibits E.1-E.7 to "Smart Storage Systems, Inc.'s Invalidity Contentions," dated June 6, 2014.

Examiner Signature		Date Considered	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				*Electronically filed December 11, 2021*	
				Application Number	*17/403,832*
				Filing Date	*August 16, 2021*
				First Named Inventor	*Jefferey C. Solomon*
				Art Unit	*2139*
				Examiner Name	*TBD*
Sheet	46	of	47	Attorney Docket Number	*NL023-02US02*

	863.	U.S. District Court Northern District of California, Case No. 4:13-CV-05889-YGR, Netlist, Inc. v. Smart Storage Systems, Inc., and Diablo Technologies, Inc., Diablo Technologies, Inc.'s Invalidity Contentions, dated June 6, 2014.
	864.	U.S. District Court Northern District of California, Case No. 4:13-CV-05889-YGR, Netlist, Inc. v. Smart Storage Systems, Inc., and Diablo Technologies, Inc., Exhibits D-1 to D6 to "Diablo Technologies, Inc.'s Invalidity Contentions," dated June 6, 2014.
	865.	U.S. District Court Central District of California, Case No. CV09 06900, Netlist, Inc. vs. Inphi Corporation, Complaint For Patent Infringement, filed Sep. 22, 2009 in 10 pages. cited by other.
	866.	U.S. District Court Central District of California, Case No. CV09 06900, Netlist, Inc. vs. INPHI Corporation, Defendant Inphi Corporation's Answer to Plaintiff's Complaint for Patent Infringement, filed Nov. 12, 2009 in 6 pages. cited by other.
	867.	U.S. District Court Central District of California, Case No. CV09 06900, Netlist, Inc. vs. INPHI Corporation, Defendant Inphi Corporation's Answer to Plaintiff's First Amended Complaint for Patent Infringement, filed Feb. 11, 2010 in 9 pages. cited by other.
	868.	U.S. District Court Central District of California, Case No. CV09 06900, Netlist, Inc. vs. INPHI Corporation, Defendant Inphi Corporation's Notice of Motion and Motion for Stay Pending Reexaminations and Interference Proceeding Regarding the Patents-In-Suit; Memorandum of Points and Authorities in Support Thereof, filed Apr. 21, 2010 in 28 pages. cited by other.
	869.	U.S. District Court Central District of California, Case No. CV09 06900, Netlist, Inc. vs. INPHI Corporation, Plaintiff Netlist Inc's Opposition to Defendant Inphi Corporation's Motion for Stay Pending Reexaminations and Interference Proceedings Regarding the Patents-In-Suit, filed May 3, 2010 in 23 pages. cited by other.
	870.	U.S. District Court Central District of California, Case No. CV09 06900, Netlist, Inc. vs. Inphi Corporation, Plaintiff Netlist, Inc's First Amended Complaint For Patent Infringement, filed Dec. 23, 2009 in 8 pages. cited by other.
	871.	US District Court Civil Docket; Netlist Inc. v. Google Inc.; 4:09cv5718; Date filed Dec. 4, 2009. In 10 pages. cited by other.
	872.	U.S. Court of Appeals for the Federal Circuit, Decision on Appeal for Reexamination Control No. 95/001,381, filed November 13, 2015, 14 pages
	873.	U.S. District Court Northern District of California, Case No. 4:13-CV-05889-YGR, Netlist, Inc. v. Smart Storage Systems, Inc., and Diablo Technologies, Inc., Corrected Joint Claim

Examiner Signature		Date Considered	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				*Electronically filed December 11, 2021*	
				Application Number	*17/403,832*
				Filing Date	*August 16, 2021*
				First Named Inventor	*Jefferey C. Solomon*
				Art Unit	*2139*
				Examiner Name	*TBD*
Sheet	47	of	47	Attorney Docket Number	*NL023-02US02*

	874.	Construction and Prehearing Statement Pursuant to Patent L.R. 4-3, including Exhibit A, filed August 27, 2014, 28 pages.
	875.	Notice of Allowance, U.S. Pat. App. No. 12/504,131, February 12, 2013, 52 pages
	876.	Non-Final Office Action, U.S. Pat. App. No. 12/761,179, September 13, 2012, 20 pages
	877.	Response to non-final office action dated September 13, 2012 for U.S. Patent Application No. 12/761,179, filed March 13, 2013, 16 pages
	878.	Notice of Allowance, U.S. Pat. App. No. 12/761,179, July 11, 2013, 37 pages
	879.	Non-Final Office Action, dated January 2, 2014, for U.S. Pat. App. No. 13/287,042 filed November 1, 2011, 42 pages
	880.	Response to Non-Final Office Action dated January 2, 2014 for U.S. Pat. App. No. 13/287,042, filed April 2, 2014, 12 pages
	881.	Non-final office action, U.S. Patent Application No. 13/288,850, October 14, 2013, 24 pages
	882.	Response to non-final office action dated October 14, 2013 for U.S. Patent Application No. 13/288,850, filed January 14, 2014, 15 pages
	883.	Non-final office action, U.S. Patent Application No. 13/411,344, December 31, 2013, 28 pages
	884.	Response to non-final office action dated 12/31/2013 for U.S. Patent Application No. 13/411,344, filed March 31, 2014, 12 pages
	885.	Non-Final Office Action, U.S. Pat. App. No. 13/412,243, January 2, 2014, 20 pages
	886.	Non-final office action, U.S. Patent Application No. 13/473,413, November 17, 2011, 46 pages
	887.	Office Action mailed April 2, 2014, for Japanese Patent Application No. JP 2012-520662 and English translation thereof, 7 pages
	888.	Written Opinion for International Application No. PCT/US2010/040826, date of mailing October 24, 2011 (NETL.048VPC) in 7 pages.
	889.	International Preliminary Report on Patentability for International Application No. PCT/US2010/040826, date of mailing November 28, 2011 (NETL.048VPC) in 34 pages.
	890.	International Search Report and Written Opinion for Related Application No. PCT/US2010/040826, mailed on September 27, 2010, in 15 pages.
	891.	International Search Report and Written Opinion, PCT Application No. PCT/US2011/059209, January 31, 2013

Examiner Signature		Date Considered	

Electronic Acknowledgement Receipt

EFS ID:	44492794
Application Number:	17403832
International Application Number:	
Confirmation Number:	3549
Title of Invention:	MEMORY MODULE WITH DATA BUFFERING
First Named Inventor/Applicant Name:	Jefferey C. Solomon
Customer Number:	79141
Filer:	Jamie Jie Zheng
Filer Authorized By:	
Attorney Docket Number:	NL023-02US02
Receipt Date:	11-DEC-2021
Filing Date:	16-AUG-2021
Time Stamp:	21:23:18
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Transmittal Letter	NL023-02US02_IDS_Transmittal.pdf	130279 359fc4975ecbbdcac05b3e23a1848815b7eb393e	no	4

Warnings:

Information:					
2	Information Disclosure Statement (IDS) Form (SB08)	NL023-02US02_IDS_List_2021-12-11.pdf	5635119 d6ff30dae8e792335bd52bec9406373a0655cc91	no	47
Warnings:					
Information:					
This is not an USPTO supplied IDS fillable form					
			Total Files Size (in bytes):	5765398	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Electronically filed December 11, 2021

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of:	Jefferey C. SOLOMON	Confirmation No.:	3549
Serial No.:	17/403,832	Group Art Unit:	2139
Filed:	August 16, 2021	Examiner:	TBA
For:	*MEMORY MODULE WITH DATA BUFFERING*	Attorney Docket No.:	NL023-02US02

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In accordance with the duty of disclosure provisions of 37 C.F.R. §1.56, there is hereby provided certain information which the Examiner may consider material to the examination of the subject U.S. patent application. It is requested that the Examiner make this information of record if it is deemed material to the examination of the application.

1. Enclosures accompanying this Information Disclosure Statement are:

1a. ☒ A list of all patents, publications, applications, or other information submitted for consideration by the office.

1b. A legible copy of:

☐ Each foreign patent;

☐ Each publication or that portion which caused it to be listed on the PTO-1449;

☐ For each cited pending U.S. application, the application specification including the claims, and any drawing of the application, or portion of the application which caused it to be listed on the PTO-1449 including any claims directed to that portion;

☐ all other information or portion which caused it to be listed on the PTO-1449.

1c. ☐ An English language copy of search report(s) from a counterpart foreign application or PCT International Search Report.

1d. ☐ Explanations of relevancy (ATTACHMENT 1(d), hereto) or English language abstracts of the non-English language publications.

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2. ☒ This Information Disclosure Statement is filed under 37 C.F.R. §1.97(b):

☐ Within three months of the filing date of a national application other than a continued prosecution application under §1.53(d);

☐ Within three months of the date of entry of the national stage as set forth in §1.491 in an international application;

☒ Before the mailing of the first Office action on the merits;

☐ Before the mailing of a first Office action after the filing of a request for continued examination under §1.114.

3. ☐ This Information Disclosure Statement is filed under 37 C.F.R. §1.97(c) after the period specified in 37 C.F.R. §1.97(b), but before the mailing date of any of a final action under 37 C.F.R. §1.113, a notice of allowance under 37 C.F.R. §1.311 or an action that otherwise closes prosecution in the application.

(Check either Item 3a, 3b, 3c or 3d)

3a. ☐ The Certification Statement in Item 5 below is applicable. Accordingly, no fee is required.

3b. ☐ The $260 (large entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Deposit Account No. 60-3916 (order no. NL057-10US01).

3c. ☐ The $130 (small entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Deposit Account No. 60-3916 (order no. NL057-10US01).

3d. ☐ The $120 (micro entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Deposit Account No. 60-3916 (order no. NL057-10US01).

(Items 3b or 3c to be checked if any reference known for more than 3 months)

4. ☐ This Information Disclosure Statement is filed under 37 C.F.R. §1.97(d) after the period specified in 37 C.F.R. §1.97(c), but on or before the date of payment of the issue fee.

(Check Item 4a, and 4b, 4c or 4d)

4a. ☐ The Certification Statement in Item 5 below is applicable.

4b. ☐ The $260 (large entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Deposit Account No. 60-3916 (order no. NL057-10US01).

4c. ☐ The $130 (small entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Deposit Account No. 60-3916 (order no. NL057-10US01).

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4d. ☐ The $120 (micro entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Deposit Account No. 60-3916 (order no. NL057-10US01).

5. ☐ Certification Statement (applicable if Item 3a or Item 4a is checked)

(Check either Item 5a, 5b, 5c or 5d)

5a. ☐ In accordance with 37 C.F.R. §1.97(e)(1), it is certified that each item of information contained in this information disclosure statement was first cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement.

5b. ☐ In accordance with 37 C.F.R. §1.97(e)(2), it is certified that no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 C.F.R. §1.56(c) more than three months prior to the filing of this information disclosure statement.

5c. ☐ Each item of information contained in this information disclosure statement was cited in a communication from a foreign patent office in a counterpart application, and the communication was not **received** by any individual designated in 37 C.F.R. §1.56(c) more than thirty days prior to the filing of this information disclosure statement.

5d. ☐ Pursuant to 37 C.F.R. §1.704(d), each item of information contained in this information disclosure statement was cited in a communication from a foreign patent office in a counterpart application, and the communication was not **received** by any individual designated in 37 C.F.R. §1.56(c) more than thirty days prior to the filing of this information disclosure statement.

6. ☒ Copies of each cited U.S. patent and each U.S. patent application publication are not enclosed pursuant to the USPTO OG Notice dated 05 August 2003 waiving the requirement under 37 C.F.R. 1.98(a)(2)(i) for U.S. patent applications filed after June 30, 2003.

7. ☒ This application is a continuation application under 37 C.F.R. §1.53(b) or (d).

(Check appropriate Items 7a, 7b and/or 7c)

7a. ☐ A Petition to Withdraw from issue under 37 C.F.R. §1.313(b)(5) is concurrently filed herewith.

7b. ☒ Copies of publications listed on Form PTO-1449 from prior application Serial Nos. **15/857,519**, filed on **December 28, 2017**, **14/715,486**, filed on **May 18, 2015**; **13/971,231** , filed on **August 20, 2013**; **13/287,081** , filed on **November 1, 2011**; **13/032,470** , filed on **February 22, 2011**; **12/955,711** , filed on **November 29, 2010**; **12/629,827** , filed on **December 2, 2009**; **12/408,652** , filed on **March 20, 2009**; **11/335,875** , filed on **January 19, 2006**; **11/173,175** , filed on **July 1, 2005**; **11/075,395** , filed on **March 7, 2005**, of which this application claims priority under

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35 U.S.C. §120, are not being submitted pursuant to 37 C.F.R. §1.98(d).

7c. ☐ Copies of the publications listed on the attached Form PTO-1449 that were not previously cited in prior application Serial No. , filed on , are provided herewith.

8. ☐ This is a Supplemental Information Disclosure Statement. (Check Item 8a)

8a. ☐ This Supplemental Information Disclosure Statement under 37 C.F.R. §1.97(f) supplements the Information Disclosure Statement filed on . A bona fide attempt was made to comply with 37 C.F.R. §1.98, but inadvertent omissions were made. These omissions have been corrected herein. Accordingly, additional time is requested so that this Supplemental Information Disclosure Statement can be considered as if properly filed on .

9. ☐ In accordance with 37 C.F.R. §1.98, a concise explanation of what is presently understood to be the relevance of each non-English language publication is:

(Check Item 9a, 9b, or 9c)

9a. ☐ satisfied because all non-English language publications were cited on the enclosed English language copy of the PCT International Search Report or the search report from a counterpart foreign application indicating the degree of relevance found by the foreign office.

9b. ☐ set forth in the application.

9c. ☐ enclosed as an attachment hereto.

10. ☒ The Commissioner is authorized to charge any additional fee required or credit any overpayment for this Information Disclosure Statement and/or Petition to Deposit Account No. 60-3916 (order no. NL023-02US02).

11. ☒ No admission is made that the information cited in this Statement is, or is considered to be, material to patentability nor a representation that a search has been made (other than a search report of a foreign counterpart application or PCT International Search Report if submitted herewith). 37 C.F.R. §§1.97(g) and (h).

Respectfully submitted,

Date: December 11, 2021

/Jamie J. Zheng/ 51,167
Jamie J. Zheng (Reg. No.)
Customer No. 79141

Samsung Electronics Co., Ltd.
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INFORMATION DISCLOSURE CITATION Substitute for Form 1449-PTO				*Electronically filed August 5, 2022*	
				Application Number	17/403,832
				Filing Date	August 16, 2021
				First Named Inventor	Jefferey C. SOLOMON
				Art Unit	2139
				Examiner Name	TBA
Sheet	1	of	5	Attorney Docket Number	***NL023-02US02***

PATENT DOCUMENTS

Examiner Initials	Cite No.	Document Number Number - Kind Code[2]	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	1	6185704 B2	2001-02-06	Pawate	
	2	6493250 B2	2002-12-10	Halbert	
	3	7363422 B2	2008-04-22	Perego	
	4	7526597 B2	2009-04-28	Perego	
	5	20020026600 A1	2007-07-17	Jung	
	6	20020112119 A1	2002-08-15	Halbert	
	7	20030174550 A1	2003-09-18	Acharya	
	8	20040107326 A1	2004-06-03	Janzen	

FOREIGN PATENT DOCUMENTS

Examiner Initials	Cite No.	Foreing Patent Document Country Code[3] – Number[4] - Kind Code[5] *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]
	9	JP2003151273 A	2003-05-23	Koji Kato		
	10	WO2002025454A2	2002-03-28	John Halbert		

NON PATENT LITERATURE DOCUMENTS

Examiner Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published
	11	Inter Partes Review of US Patent No. 10489314, Case No. IPR2022-00744, 'PETITION FOR INTER PARTES REVIEW,' filed March 30, 2022
	12	Inter Partes Review of US Patent No. 10489314, Case No. IPR2022-00745, "PETITION FOR INTER PARTES REVIEW," filed March 30, 2022
	13	Inter Partes Review of US Patent No. 10489314, Case Nos. IPR2022-00744 and IPR2022-00745, 'Declaration of Dr. Vojin Oklobdzija,' filed March 30, 2022
	14	Inter Partes Review of US Patent No. 10489314, Case No. IPR2022-00744, 'PATENT OWNER'S PRELIMINARY RESPONSE,' filed August 3, 2022
	15	Inter Partes Review of US Patent No. 10489314, Case No. IPR2022-00745, "PATENT OWNER'S PRELIMINARY RESPONSE," filed August 3, 2022

Examiner Signature		Date Considered	

INFORMATION DISCLOSURE CITATION Substitute for Form 1449-PTO				*Electronically filed August 5, 2022*	
				Application Number	17/403,832
				Filing Date	August 16, 2021
				First Named Inventor	Jefferey C. SOLOMON
				Art Unit	2139
				Examiner Name	TBA
Sheet	2	of	5	Attorney Docket Number	***NL023-02US02***

	16	Inter Partes Review of US Patent No. 7619912, Case No. IPR2022-00615, 'PETITION FOR INTER PARTES REVIEW,' filed February 27, 2022
	17	Inter Partes Review of US Patent No. 7619912, Case No. IPR2022-00615, 'Declaration of Dr. Andrew Wolfe,' filed February 27, 2022
	18	Inter Partes Review of US Patent No. 7619912, Case No. IPR2022-00615, 'Patent Owner's Preliminary Response,' filed July 21, 2022
	19	Inter Partes Review of US Patent No. 7619912, Case No. IPR2022-00615, 'Declaration of Michael C. Brogioli, Ph.D,' filed July 21, 2022
	20	Inter Partes Review of US Patent No. 10,217,523, Case No. IPR2022-00063, 'DECISION - Granting Institution of Inter Partes Review,' issued May 5, 2022
	21	Complaint for Patent Infringement, Netlist, Inc. v. Micron Technology, Inc., Micron Semiconductor Products, Inc., and Micron Technology Texas LLC, Case No. 6:21-cv-00431-ADA (W.D. Tex. Apr. 28, 2021), 74 pages.
	22	Netlist, Inc.'s Disclosure of Asserted Claims and Preliminary Infringement Contentions to Defendants, Netlist, Inc. v. Micron Technology, Inc., Micron Semiconductor Products, Inc., and Micron Technology Texas LLC, Case No. 6:21-cv-00431-ADA (W.D. Tex. Sept. 10, 2021), 9 pages.
	23	Netlist Inc.'s Preliminary Infringement Contentions, 'Exhibit A - Infringement of U.S. Patent No. 10,489,314 (the Solomon Patent)," Netlist, Inc. v. Micron Technology, Inc., Micron Semiconductor Products, Inc., and Micron Technology Texas LLC, Case No. 6:21-cv-00431-ADA (W.D. Tex. Sept. 10, 2021), 150 pages.
	24	Micron's Preliminary Invalidity Contentions in Netlist, Inc. v. Micron Technology, Inc., Micron Semiconductor Products, Inc., and Micron Technology Texas LLC, Case No. 6:21-cv-00431-ADA (W.D. Tex. Nov. 5, 2021), 38 pages.
	25	Invalidity Chart for U.S. Patent No. 10,489,314 based on US Patent No. 6,185,704 to Pawate et al., Netlist, Inc. v. Micron Technology, Inc., Micron Semiconductor Products, Inc., and Micron Technology Texas LLC, Case No. 6:21-cv-00431 (W.D. Tex. Nov. 5, 2021), 117 pages.
	26	Invalidity Chart for U.S. Patent No. 10,489,314 based on U.S. Patent No. 6,493,250 to Halbert et al., Netlist, Inc. v. Micron Technology, Inc., Micron Semiconductor Products, Inc., and Micron Technology Texas LLC, Case No. 6:21-cv-00431 (W.D. Tex. Nov. 5, 2021), 172 pages.
	27	Invalidity Chart for U.S. Patent No. 10,489,314 based on US Patent No. 6,526,473 to Kim, Netlist, Inc. v. Micron Technology, Inc., Micron Semiconductor Products, Inc., and Micron Technology Texas LLC, Case No. 6:21-cv-00431 (W.D. Tex. Nov. 5, 2021), 49 pages.

Examiner Signature		Date Considered	

INFORMATION DISCLOSURE CITATION Substitute for Form 1449-PTO				*Electronically filed August 5, 2022*	
				Application Number	17/403,832
				Filing Date	August 16, 2021
				First Named Inventor	Jefferey C. SOLOMON
				Art Unit	2139
				Examiner Name	TBA
Sheet	3	of	5	Attorney Docket Number	***NL023-02US02***

	28	Invalidity Chart for U.S. Patent No. 10,489,314 based on US Patent No. 8,250,295 to Amidi et al., Netlist, Inc. v. Micron Technology, Inc., Micron Semiconductor Products, Inc., and Micron Technology Texas LLC, Case No. 6:21-cv-00431 (W.D. Tex. Nov. 5, 2021), 166 pages.
	29	Invalidity Chart for U.S. Patent No. 10,489,314 based on US Patent Application Publication No. 2001/0008006 to Klein, Netlist, Inc. v. Micron Technology, Inc., Micron Semiconductor Products, Inc., and Micron Technology Texas LLC, Case No. 6:21-cv-00431 (W.D. Tex. Nov. 5, 2021), 163 pages.
	30	Invalidity Chart for U.S. Patent No. 10,489,314 based on US Patent Application Publication No. 2002/0112119 to Halbert et al., Netlist, Inc. v. Micron Technology, Inc., Micron Semiconductor Products, Inc., and Micron Technology Texas LLC, Case No. 6:21-cv-00431 (W.D. Tex. Nov. 5, 2021), 247 pages.
	31	Invalidity Chart for U.S. Patent No. 10,489,314 based on US Patent Application Publication No. 2005/0281096 to Bhakta et al, Netlist, Inc. v. Micron Technology, Inc., Micron Semiconductor Products, Inc., and Micron Technology Texas LLC, Case No. 6:21-cv-00431 (W.D. Tex. Nov. 5, 2021), 517 pages.
	32	Invalidity Chart for U.S. Patent No. 10,489,314 based on B. Prince, "Application specific DRAMs Today," (2003), Netlist, Inc. v. Micron Technology, Inc., Micron Semiconductor Products, Inc., and Micron Technology Texas LLC, Case No. 6:21-cv-00431 (W.D. Tex. Nov. 5, 2021), 109 pages.
	33	Invalidity Chart for U.S. Patent No. 10,489,314 based on the DDR2 SDRAM Specification JEDEC Standard JESD79-2A, Netlist, Inc. v. Micron Technology, Inc., Micron Semiconductor Products, Inc., and Micron Technology Texas LLC, Case No. 6:21-cv-00431 (W.D. Tex. Nov. 5, 2021), 150 pages.
	34	Invalidity Chart for U.S. Patent No.10,489,314 based on the DDR SDRAM RDIMM Design Specification JEDEC Standard 21-C (4.20.4), Netlist, Inc. v. Micron Technology, Inc., Micron Semiconductor Products, Inc., and Micron Technology Texas LLC, Case No. 6:21-cv-00431 (W.D. Tex. Nov. 5, 2021), 599 pages.
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	36	Micron's Preliminary Identification of Proposed Claim Constructions, Netlist, Inc. v. Micron Technology, Inc., Micron Semiconductor Products, Inc., and Micron Technology Texas LLC, Case No. 6:21-cv-00431-ADA (W.D. Tex. Dec. 23, 2021), 14 pages.
	37	Netlist, Inc.'s Preliminary Proposed Claim Constructions, Netlist, Inc. v. Micron Technology, Inc., Micron Semiconductor Products, Inc., and Micron Technology Texas LLC, Case No. 6:21-cv-00431-ADA (W.D. Tex. Dec. 23, 2021), 7 pages.

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Sheet	4	of	5	Attorney Docket Number	***NL023-02US02***

	38	Defendants' Identification of Extrinsic Evidence in Support of Their Preliminary Proposed Constructions, Netlist, Inc. v. Micron Technology, Inc., Micron Semiconductor Products, Inc., and Micron Technology Texas LLC, Case No. 6:21-cv-00431-ADA (W.D. Tex. Jan. 13, 2022), 21 pages.
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	52	JEDEC Standard JESD82-3B, "Definition of the SSTVN16857 2.5-2.6 V 14-Bit SSTL_2 Registered Buffer," November 2004
	53	JEDEC Standard JESD82-7A, "Definition of the SSTU32864 1.8-V Configurable Registered Buffer for DDR2 RDIMM Applications," October 2004

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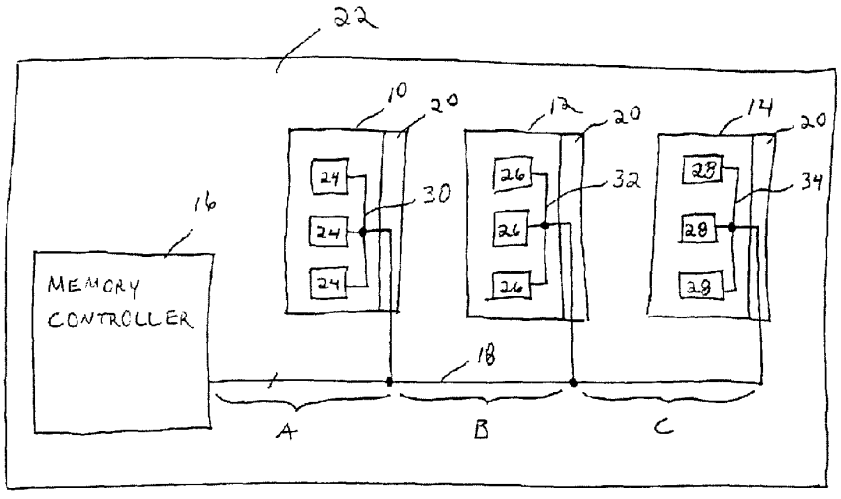
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[Continued on next page]

(54) Title: MEMORY MODULE HAVING BUFFER FOR ISOLATING STACKED MEMORY DEVICES



(57) Abstract: The present invention utilizes a buffer to isolate a stack of memory devices, thereby taking advantage of the increased memory density available from stacked memory devices while reducing capacitive loading. A memory module in accordance with the present invention may include a stack of memory devices and a buffer coupled to the first and second memory devices and arranged to capacitively isolate the first and second memory devices from a bus. In a memory system in accordance with the present invention, multiple buffered stacks of memory devices are preferably coupled in a point-to-point arrangement, thereby further reducing capacitive loading.

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MEMORY MODULE HAVING BUFFER FOR ISOLATING STACKED MEMORY DEVICES

BACKGROUND OF THE INVENTION

Fig. 1 is a block diagram of a prior art memory system. The system of Fig. 1 includes three memory modules 10, 12, and 14 that are coupled to a memory controller 16 through a bus 18. Each memory module is fabricated on a circuit board that plugs into a connector 20 on a mother board 22. Each module includes multiple memory devices 24, 26, and 28 that are coupled to the bus 18 to allow the memory controller to access the memory devices.

To increase the memory density of the modules, memory devices can be stacked on top of each other, thereby increasing the memory capacity of each module without increasing the space required on the circuit board. Stacking memory devices, however, increases the capacitive loading of the signals on the bus. For example, from the perspective of the memory controller 16, each data line in the bus 18 has a total capacitance that equals the sum of the capacitance of each portion of the signal line running through sections A, B, and C of the bus, plus the capacitance of the portion of the data line in sections 30, 32, and 34 that couple the memory devices to the bus, plus the sum of the input capacitance of all of the memory devices (which are attached to sections 30, 32, and 34 in parallel). If additional memory devices are stacked on devices 24, 26, and 28, then the capacitance of the additional devices are added to the total capacitance seen by the controller. Therefore, when the memory controller drives a data signal onto the bus, it must overcome the combined capacitance of all of the stacked memory devices. This heavy capacitive loading reduces the maximum operating speed and increases the power consumption by the memory system, especially at higher operating frequencies.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a block diagram of a prior art memory system.

Fig. 2 is a block diagram of an embodiment of a memory module in accordance with the present invention.

Fig. 3 is a side view showing the mechanical arrangement of an embodiment of a memory module in accordance with the present invention.

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Fig. 4 is a block diagram of an embodiment of a memory system in accordance with the present invention.

DETAILED DESCRIPTION

Fig. 2 is a block diagram of an embodiment of a memory module 100 in accordance with the present invention. Module 100 includes a first memory device 104 which is mounted on a circuit board 108. A second memory device 106 is stacked on top of the first memory device to form a stack 102. A buffer 110 is mounted on the circuit board and electrically coupled to the memory devices 104 and 106 through signal lines 112. A connector 114 is attached to the circuit board for coupling the memory module to a bus that leads to a memory controller on another circuit board, e.g., a computer mother board. The buffer 110 is arranged to capacitively isolate the stack of memory devices from the bus. Therefore, the capacitive loading seen by a memory controller (or other device) driving the bus is reduced. This increases the maximum operating speed of the memory module and reduces power consumption.

The buffer 110 sends and receives signals to and from the memory controller through connector 114 over signal lines 120. In a preferred embodiment, the buffer 110 is designed to receive signals from the memory controller over a first bus and redrive them back out the connector over signal lines 122 (shown in broken lines) and to a second memory module over a second bus.

Fig. 3 is a side view showing the mechanical arrangement of an embodiment of a memory module in accordance with the present invention. The stack 102 can be extended to include additional memory devices (shown in broken lines). Additional stacks can also be added, and they can be buffered by the first buffer 110, or a separate buffer can be used for each stack.

Fig. 4 is a block diagram of an embodiment of a memory system in accordance with the present invention. The system of Fig. 4 includes two modules 100A and 100B coupled to a memory controller 116 on a computer mother board 117 through a bus system 118 which includes buses 118A and 118B. The modules may be coupled through connectors 130A and 130B which plug into connectors 132A and 132B, respectively, on the mother board. Each module a stack of memory devices 102A,102B and a buffer 110A,110B that isolates the corresponding stack from the bus system. In the example of

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Fig. 4, the modules are coupled to the memory controller in a point-to-point arrangement. That is, the memory controller 116 is coupled to module 100A, which is designed to receive signals from the memory controller and redrive them to module 100B. The use of point-to-point wiring further reduces the capacitive loading seen by the memory controller. Alternatively, the modules 110A and 110B and memory controller 116 may be coupled together in a multi-drop arrangement in which both of the modules are essentially coupled in parallel on a single bus.

The memory controller 116 is shown in Fig. 4 as part of a central processing unit (CPU) 126, however, it may alternatively be implemented as one chip of a chipset, or in any other suitable form. The memory system shown in Fig. 4 includes two memory modules for purposes of illustration, but may be implemented with only a single memory module or with any number of modules. The buffers need not be mounted on the memory modules, but can also be mounted on the mother board or any other device on which the bus system resides. Moreover, the stacks of memory devices need not be mounted on modules. Instead, an entire memory system in accordance with the present invention may be fabricated on a single circuit board including the memory controller, bus, stacks of memory devices, and buffers arranged to capacitively isolate the stacks from the bus. The advantages of the present invention can be realized wherever memory devices are stacked by buffering the stack from other components, thereby reducing the capacitance load seen by the other component.

Having described and illustrated the principles of the invention in some preferred embodiments thereof, it should be apparent that the invention can be modified in arrangement and detail without departing from such principles. We claim all modifications and variations coming within the spirit and scope of the following claims.

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CLAIMS

1. A memory system comprising:

a first memory device;

a second memory device stacked on the first memory device; and

a buffer coupled to the first and second memory devices.

2. A memory system according to claim 1 further comprising a third memory device stacked on the second memory device and coupled to the buffer.

3. A memory system according to claim 1 further comprising a bus coupled to the buffer.

4. A memory system according to claim 3 further comprising a memory controller coupled to the bus.

5. A memory system according to claim 1 wherein the buffer is a first buffer and further comprising:

a third memory device;

a fourth memory device stacked on the third memory device; and

a second buffer coupled to the third and fourth memory devices and to the first buffer.

6. A memory system according to claim 5 wherein the first buffer is adapted to receive a signal and redrive the signal to the second buffer.

7. A memory system according to claim 5 wherein the first buffer is adapted to receive a plurality of signals and redrive the plurality of signals to the second buffer.

8. A memory system according to claim 5 further comprising a memory controller coupled to the first buffer.

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9. A memory system according to claim 8 wherein the memory controller, the first buffer, and the second buffer are coupled together in a multi-drop arrangement.

10. A memory system according to claim 8 wherein the memory controller, the first buffer, and the second buffer are coupled together in a point-to-point arrangement.

11. A memory module comprising:
a first memory device;
a second memory device stacked on the first memory device; and
a buffer coupled to the first and second memory devices and arranged to capacitively isolate the first and second memory devices from a bus.

12. A memory module according to claim 11 further comprising a connector attached to the module and adapted to couple the module to a bus.

13. A memory module according to claim 11 further comprising a third memory device stacked on the second memory device and coupled to the buffer.

14. A memory module according to claim 11 wherein the memory module is adapted to receive a signal from the bus and to redrive the signal to another memory module.

15. A memory module according to claim 11 wherein the memory module is adapted to receive a plurality of signals from the bus and to redrive the plurality of signals to another memory module.

16. A memory module according to claim 11 wherein the buffer is adapted to receive a signal from the bus and to redrive the signal to another memory module.

17. A memory system comprising:
a bus;
a stack of memory devices; and

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a buffer coupled between the stack of memory devices and the memory bus.

18. A memory system according to claim 17 further comprising:

a second stack of memory devices; and

a second buffer coupled between the second stack of memory devices and the bus.

19. A memory system according to claim 17 wherein the buffer is a first buffer and further comprising:

a second stack of memory devices; and

a second buffer coupled between the second stack of memory devices and the first buffer.

20. A memory system according to claim 17 further including a memory controller coupled to the bus.

21. A memory system according to claim 17 wherein the stack of memory devices is mounted on a memory module.

22. A memory system according to claim 21 wherein the buffer is mounted on the memory module.

23. A memory system according to claim 21 wherein the bus is fabricated on a circuit board and the buffer is mounted on the circuit board.

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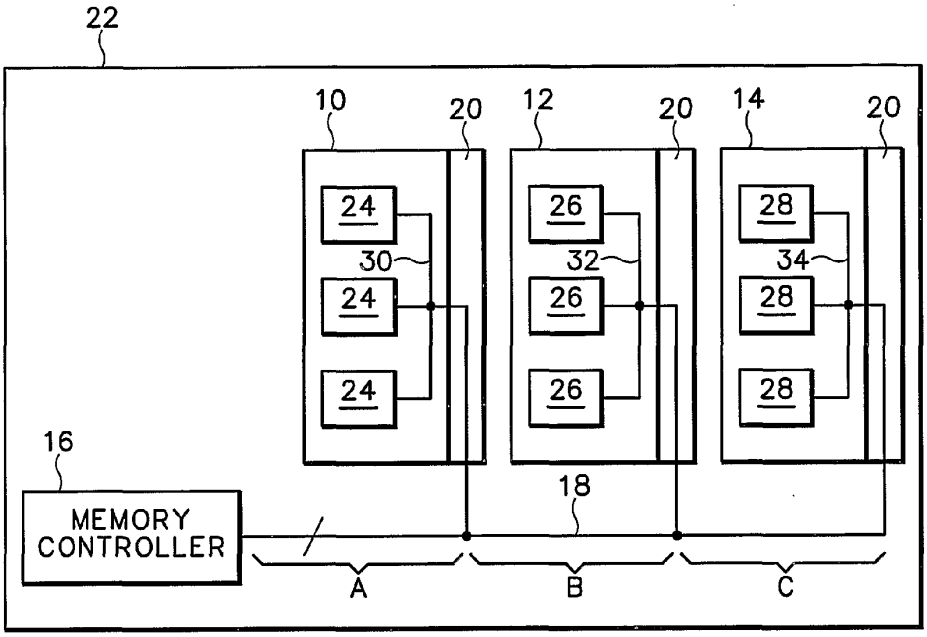


FIG.1
(PRIOR ART)

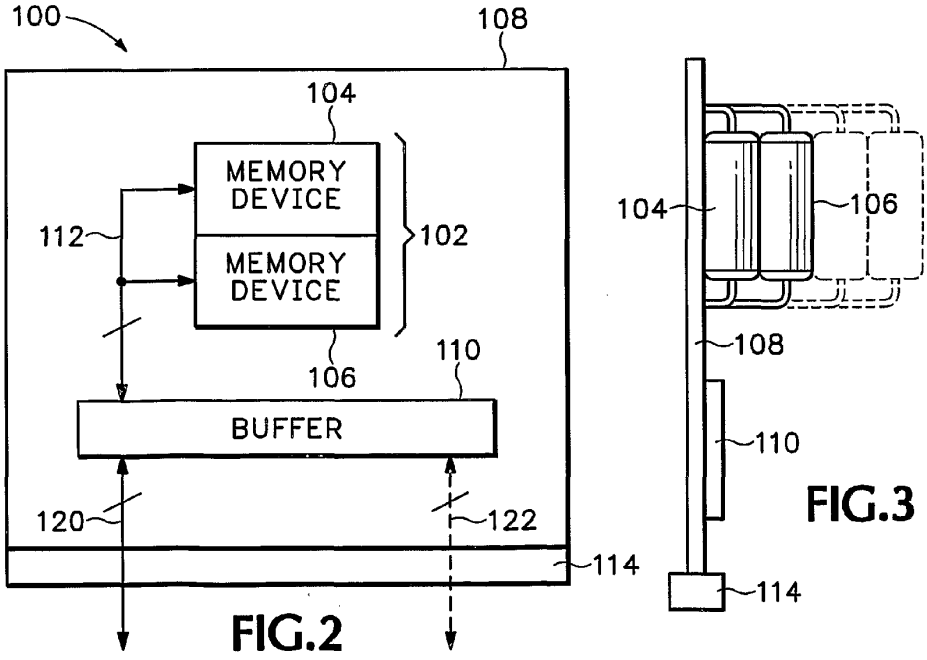


FIG.2

FIG.3

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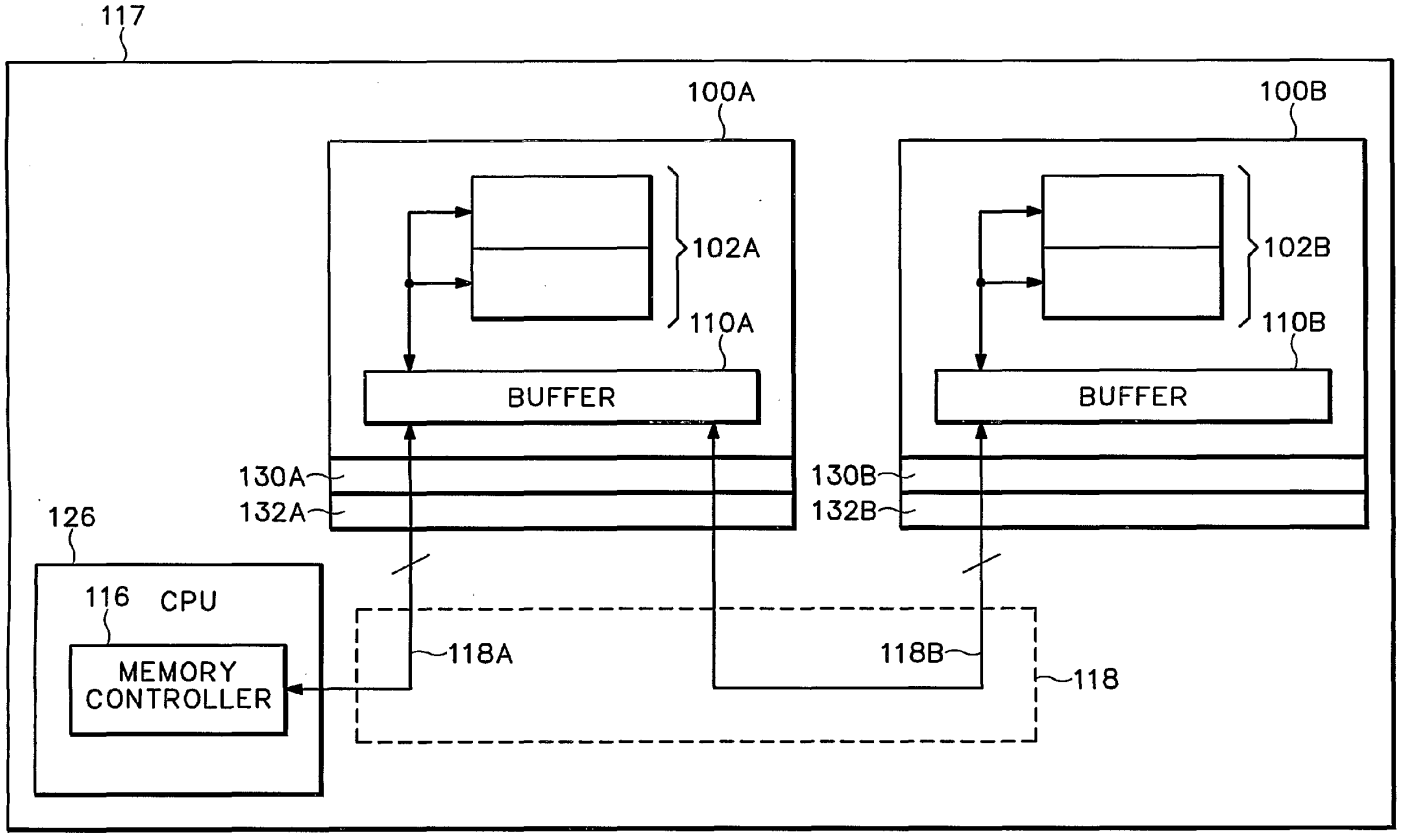

117
100A
100B
102A
102B
110A
110B
BUFFER
BUFFER
130A
132A
130B
132B
126
116 CPU
MEMORY CONTROLLER
118A
118B
118

FIG.4

Patents JP2003151273

Storage device, internal control method for storage device, system, and control method for storage means in system

Abstract

PROBLEM TO BE SOLVED: To provide a storage device to which efficient access can be performed and in which current consumption can be reduced without changing a package, an internal control method for a storage device, a system, and a control method for a storage means in a system. SOLUTION: A memory device changes a shape of a logic address map of a DRAM core in accordance with a page length specifying signal outputted from a mode register. And when page length is set shorter than full page by the page length specifying signal, a row address Row increased by the above is taken in simultaneously with a column address Co1 at the time of the first red-command RD1. At the time, the address Row being increased is taken in from an external address terminal being not used at the time.

JP2003151273A

Japan

Find Prior Art Similar

Other languages: Japanese

Inventor: Koji Kato 加藤 浩治

Current Assignee :

Worldwide applications

2001 JP

Application JP2001345266A events

2001-11-09	Application filed by Fujitsu VLSI Ltd, Fujitsu Ltd
2001-11-09	Priority to JP2001345266A
2002-10-23	Priority claimed from TW091124572A
2003-05-23	Publication of JP2003151273A
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2021-11-09	Anticipated expiration
Status	Expired - Fee Related

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Claims (7)

Hide Dependent

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[Claims] 1. An address terminal for simultaneously taking in an M-bit first address and an N-bit second address, or
Alternatively, a memory device having an address terminal having a larger number of M-bit first address and N-bit second address, and accessing a memory cell array in which memory cells are arrayed at the first address and the second address In the first address or the second address, based on access form information for changing the logical address map shape of the memory cell array, part of the external address input from the address terminal is used.
A storage device comprising address control means for substituting an address. 2. An address terminal for simultaneously receiving an M-bit first address and an N-bit second address, or
Alternatively, a memory device having an address terminal having a larger number of M-bit first address and N-bit second address, and accessing a memory cell array in which memory cells are arrayed at the first address and the second address The memory device according to claim 1, further comprising address invalidation means for invalidating an external address input from the address terminal or a part thereof based on access form information for changing a logical address map shape of the memory cell array. . 3. An address terminal for simultaneously receiving an M-bit first address and an N-bit second address, or
Alternatively, a memory device having an address terminal having a larger number of M-bit first address and N-bit second address, and accessing a memory cell array in which memory cells are arrayed at the first address and the second address In the internal control method, wherein a part of the external address input from the address terminal is converted into a first address or a second address based on access form information for changing a logical address map shape of the memory cell array.
An internal control method in a storage device characterized by replacing with an address. 4. An address terminal for simultaneously taking in an M-bit first address and an N-bit second address, or
Alternatively, a memory device having an address terminal having a larger number of M-bit first address and N-bit second address, and accessing a memory cell array in which memory cells are arrayed at the first address and the second address The internal control method according to claim 1, wherein an external address or a part thereof inputted from the address terminal is invalidated based on access form information for changing a logical address map shape of the memory cell array. Internal control method. 5 An address terminal for simultaneously taking in an M-bit first address and an N-bit second address, or
Alternatively, a storage means is provided which has an address terminal having a larger number of a M-bit first address and an N-bit second address, and which accesses a memory cell array in which memory cells are arrayed at the first address and the second address. And a system including control means for accessing and controlling the access means, the control means supplies the access form information at any time to the storage means, and the storage means changes based on the access form information. The system, wherein the increased address of i bits, which increases according to the shape of the logical address map of the memory cell array, is generated in the device after the generation of the first address. 6. The system according to claim 5, wherein the control means performs the access form information by using one of an address, a decoder, and code information based on a control signal. 7. An address terminal for simultaneously receiving an M-bit first address and an N-bit second address,
Alternatively, a storage means is provided which has an address terminal having a larger number of a M-bit first address and an N-bit second address, and which accesses a memory cell array in which memory cells are arrayed at the first address and the second address. And a control method of a storage unit in a system including a control unit for accessing and controlling the storage unit, wherein the control unit is a logical address of a memory cell array included in the storage unit according to access form information at each memory cycle time, and a storage unit in a system, wherein a control means for generating an i-bit increased address that increases capacity to the fixed address (next stage) controls the access rate in a time-division operating processing, and the control means

Description

[Detailed Description of the Invention]

[0001]

BACKGROUND OF THE INVENTION 1. Field of the Invention The present invention relates to a storage device, a storage device internal control method, a system, and a storage means control method in the system.

access form information at each memory cycle time, and a storage unit in a system, wherein a control means for generating an i-bit increased address that increases capacity to the fixed address (next stage) controls the access rate in a time-division operating processing, and the control means

2. Description of the Related Art Current consumption tends to increase due to the expansion of the C bus width (increasing the width of the number of bits handling data in one access). With this,
The current consumption of the entire system equipment equipped with the memory device is also increasing, and customers are demanding to reduce the power consumption of the memory device.

Further, the increase in the above-mentioned current consumption may cause a rise in the chip temperature of the memory device. Generally, D
RAM cell data retention characteristics (= Refresh characteristics: TREF)
Is deteriorated at high temperature (holding time is shortened), and for this reason also, reduction of current consumption is required.

Therefore, semiconductor memories are required to have improved performance such as increased storage capacity, increased access speed, and expanded I / O bus width, as well as reduced power consumption.

[0005]

2. Description of the Related Art A memory device has a memory cell array in which a plurality of memory cells are arranged in an array and a sense amplifier. Each memory cell is connected to a word line and a bit line, and the sense amplifier is connected to the bit line. The sense amplifier is paired with the bit line and amplifies and holds information (read data) of one cell.

The memory cell array is array-developed in the X-expansion direction in which the word line is expanded by the row address and in the Y-expansion direction in which the bit line and the sense amplifier are expanded by the column address. If the memory capacity is 1 Mbit, the logical address of the memory device is 10 bits (2

^{10} = 1024 word lines: WL) X address (Row

Address) can be configured from a Y address (Column Address) of 10 bits (2 ^{10} = 1024 bit lines: BL (1024 sense amplifiers)) (Note: bit line definition = pair of complementary bit lines)). At this time, if the wiring pitches of the word lines and the bit lines are the same, the logical memory array is imaged as a square.

The internal operation of the memory device is an SDRAM (Synchr) which is synchronous with the system clock CLK.
Onous DRAM) will be described as an example. SDRAM is
Active / synchronous with the system clock CLK to activate / deactivate the memory device as a control command.
It operates by a precharge command (falling and rising of a chip enable signal / CE ("/" indicates a bar) in an asynchronous memory device) and a read / write command for inputting / outputting data to / from the memory device.

When an active command is externally applied at the rising edge of the system clock CLK, the X address is fetched and decoded by the X decoder to select one word line and activate it. Each memory cell connected to the selected word line outputs data to each bit line, and each sense amplifier amplifies and holds the

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data (latches the data).

After that, when a read command is externally applied at the rising edge of the system clock CLK (with a delay of several CLKs from the active command), the Y address is fetched and decoded by the Y decoder to be held in one sense amplifier. Output data to the outside of the memory device.
Further, when a write command is externally applied, the Y address is fetched and decoded by the Y decoder to write the write data (input when the write command is applied) to the memory cell via one sense amplifier. After that, if necessary, read / write commands are issued at any time, and the desired Y The memory cell is accessed according to the address and the outside.

After the read / write command is completed,
At the rising edge of the system clock CLK (with a few CLK delay from the read / write command), a precharge command is applied to reset (equalize) the activated word line, sense amplifier and bit line, and the memory array becomes Return to the initial state (preparing for the next active command).

It takes an internal time until the reset operation, and it is necessary to wait (wait) for several CLKs in order to apply the next active command from the precharge command. Similarly, it is necessary to delay (wait) several CLK from the active command to the read / write command.

Although the number of input / output bits of the memory array is 1 for simplicity of explanation, the number of input / output bits is n (ni / O) (ex.4i / O).)
In this case, n sense amplifiers are simultaneously selected by the Y address. Each sense amplifier is connected to n I / O ports via n I / O buses.

The depth of the Y address is called the page length. In response to one active command, the memory device operates at least I / O bus width × page length sense amplifiers. For example, in the case of an SDRAM in which the Y address is set to 8 bits (YA <0: 7>), the page length is 256. This SDRAM is a 32-bit I / O With the O bus width, at least 8,192 (= 256 × 32) sense amplifiers operate in response to the active command.

The SDRAM latches information of a plurality of memory cells connected to a word line selected by an active command in a plurality of sense amplifiers by a read command input at any time. Therefore, by activating one word line, the information of the memory cells for the page length can be appropriately read out. More specifically, for each read / write command that is input at any time, the Y decoder is used to select a sense amplifier at any time according to the Y address that is input at the same time as the command, so that information is read from the memory cell at an arbitrary Y address. That is, the X address can be randomly accessed while the X address is fixed. Such an operation is called a Y address priority operation. Information can be similarly written to the memory cell of an arbitrary Y address in response to a write command.

In this Y address priority operation, in addition to the advantage of random access, it is possible to efficiently use a plurality of data latched in each sense amplifier of the sense amplifier group which operates by one active command. . In other words, one word line charge / discharge current and one (plural) sense amplifier (plural) bit line charge / discharge currents enable random access to the memory cells included in page 256.

Therefore, the current consumption required for one access is a value obtained by dividing the current consumption due to the charge / discharge of the word line and the charge / discharge of the bit line by the number of accesses to the page activated at the same time. Therefore, as the number of accesses in a page activated at the same time increases, the current consumption of the SDRAM per access decreases.

Further, in the Y address priority operation, the number of clocks required from application of the active command to the read / write command and the number of clocks required from application of the precharge command to the next active command are The share of the Therefore, the ratio of data occupying the input / output bus (data occupancy) is high, and the efficiency of the I / O bus in the system is good. For these, the higher the system clock frequency (higher frequency), the greater the latency that must be taken.
In M, the data occupation rate of the input / output bus can be increased.

[0018]

By the way, the SDRAM
Depending on the customer's system that uses, the bit length to be accessed is small (for example, continuous 4 bits or 8 bits). SDRAM by such a system
Access from a single active command to the precharge command, the number of reads / reads that is less than the page length.
The write operation cannot be performed and X is generated by the next active command.
The address is changed. For convenience, such an operation is performed as X.
This is called address priority operation. In this operation, the sense amplifier activated by one active command is not used efficiently.

For example, the Y address is changed (the X address is constant) and four memory cells are accessed. In this case, the charge / discharge current of one word line selected by the X address and the number of activated sense amplifiers (8192).
Current) (including the charge / discharge current of the bit line by the sense amplifier). The current consumption at this time is P (y). Therefore, the consumption current for accessing one memory cell is P (y) / 4.

On the other hand, when the X address is changed (the Y address is arbitrary) to access four memory cells, an active command and a precharge command are required every time the X address is changed. Therefore, in the case of this access method, four times (4
× P (y)), and the current consumption for accessing one memory cell is P (y).

Therefore, in the case of a system or application which frequently uses the X address priority operation, a memory device having a shallow Y address (a small number of pages) and a deep X address is effective.

However, the X address priority operation and the Y address priority operation may be mixed depending on the access method of the system using the memory device and the step of the application. In such a case, if a memory device having a shallow Y address is used, the access speed may be extremely slow

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depending on the access order, which hinders the speed improvement. On the other hand, using a memory device with a shallow X address hinders reduction of current consumption.

Further, such memory devices having different depths of the X address and the Y address have different pin arrangements and package sizes from the standard products, so that the memory devices cannot be simply replaced. For this reason, it has been necessary to re-create a board or the like on which the memory device is mounted, which causes an increase in cost and a longer development period.

Further, when a large current consumption operation such as an X address priority operation is repeated, the chip temperature (junction temperature) of the memory device may be increased. In this case, the data retention characteristic deteriorates due to the temperature rise, and the refresh operation, which is a data retention operation, must be frequently performed. Then, the chip temperature is the sum of the temperature rise due to the access to the memory device and the self-heating due to the refresh operation of the memory device, which leads to the deterioration of the data retention characteristic and the further increase of the current consumption due to the frequent refresh operation. Further, when the data holding operation is performed asynchronously regardless of the control of the customer system side (self-refresh operation), the busy state in which the refresh operation does not respond to the access from the outside increases, and the system performance increases. Decrease (the data occupancy of the I / O bus decreases).

The present invention has been made to solve the above problems, and an object of the present invention is to provide a storage device and a storage device which can achieve efficient access and reduction of current consumption without changing the package. Internal control method, system.
Another object of the present invention is to provide a method of controlling storage means in the system.

[0026]

According to the invention described in claims 1 and 3, an M-bit first address and an N-bit second address are provided.
A memory device that accesses a memory cell array in which memory cells are arranged in an array by an address has a first address and a second address. Either an address terminal for taking in an address at the same time is provided, or an address terminal having a larger number of the first address and the second address is provided. Then, the storage device replaces a part of the external address with the first address or the second address based on the access form information that changes the shape of the logical address map of the memory cell array.

According to the second and fourth aspects of the invention, the storage device invalidates the external address or a part thereof based on the access form information for changing the logical address map shape of the memory cell array.

According to the fifth and seventh aspects of the present invention, either an address terminal for simultaneously taking in the M-bit first address and the N-bit second address is provided, or the M-bit first address and the N-bit first address. A memory means for accessing a memory cell array in which memory cells are arrayed at the first address and the second address, and a control means for accessing and controlling the memory cell array are provided. In the above system, the control means supplies the access form information to the storage means at any time.
Then, the storage means generates an i-bit increased address that increases according to the logical address map shape of the memory cell array changed based on the access form information in a time division after generating the first address.

According to the invention of claim 6, claim 6
In addition to the operation of the invention described in (1), the control means performs the access form information by any one of the address, the decoder and the code information by the control signal.

[0030]

BEST MODE FOR CARRYING OUT THE INVENTION (First Embodiment) A first embodiment of the present invention will be described below.

FIG. 1 shows a memory device (SDRAM) 1.
It is a block diagram for explaining the outline of 0. The memory device 10 is connected to a CPU (not shown), and the CPU
Gives the access form information to the memory device 10 once or before access is started. The memory device 10
It has a function of changing the logical address map shape according to the access form information. More specifically, the memory device 10
Changes the logical address map shape in response to access form information applied from the outside (CPU). Therefore,
The CPU functions as a memory controller that controls the logical address map shape of the memory device 10.

The logical address map shape is determined by the depth of the X address and the Y address. The capacity of the memory cell array is constant. Therefore, the memory device 10
The depth of the X address and the depth of the Y address are changed complementarily.

The memory device 10 inputs an address signal of the number of bits required for designating the maximum value of the X address and the maximum value of the Y address from the external address terminal by using a plurality of logical address map shapes. And
The memory device 10 has the same outer shape as a standardized memory device having substantially the same memory capacity.

For example, a memory device having a capacity of 64 Mbits (32 I / O, 4-bank structure) generally (standard) has 0.5 MB memory cells for each I / O in each bank. Each bank is selected by a 2-bit bank address. The memory cells in each bank are plural (2048 lines) selected by an 11-bit row address (X address) and plural (256 lines) selected by an 8-bit column address (Y address).
Are arrayed by bit lines. And SD
A memory device such as a RAM is configured to take in an X address and a Y address by an address multiplexing method. Therefore, a typical memory device is

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It has 3 address pins from which a 13-bit X
An address (of which, a 2-bit bank address) and a Y address are fetched in a time division manner.

Next, the functional configuration of the memory device 10 will be described. The memory device 10 includes the clock buffer 1
1, a command decoder 12, an address buffer 13, an input / output buffer 14, a control signal latch 15, a mode register 16, an address generation circuit 17, a write / read (I / O) control circuit 18, and a DRAM core 19.

The clock buffer 11 inputs the clock enable signal CKE and the external clock signal CLK from an external device and outputs the internal clock signal CLK1 generated based on them to each circuit.

The command decoder 12 responds to the internal clock signal CLK1 from the clock buffer 11, that is, the clock signal CLK, in response to an external command C from an external device.
Enter the OM. In the present embodiment, the external command COM is composed of a chip select signal / CS, a column address strobe signal / CAS, a write enable signal / WE and a row address strobe signal / RAS. Then, the command decoder 12 responds to the internal clock signal CLK1 at that time by the external command COM,
That is, various commands such as a write command, a read command, and a refresh command are decoded from the state (H level or L level) of each signal / CAS, / WE, / CS, / RAS. Then, the command decoder 12 uses the various commands decoded from the external command COM as an internal command and an enable signal and the like, the address buffer 13, the input / output buffer 14, the control signal latch 15,
It outputs to the mode register 16 and the I / O control circuit 18.

The address buffer 13 has a buffer function and a latch function, and based on an internal command from the command decoder 12, an address signal A0-A from an external device is sent.
10 and bank address signals BA0 and BA1 are input
The address buffer 13 receives the input address signals A0 to A0.
A10 and bank address signals BA0 and BA1 are amplified, address data based on them are latched, and are output to the control signal latch 15, the mode register 16 and the address generation circuit 17.

The input / output buffer 14 is activated based on the enable signal from the command decoder 12, and receives write data DQ0 to DQ31 and a mask control signal DQM from an external device. The input / output buffer 14 is responsive to the internal clock signal CLK1 to write data DQ0 to DQ.
31 is output to the I / O control circuit 18. Further, the input / output buffer 14 responds to the internal clock signal CLK1 with the I
Read data DQ0 to DQ31 from the / O control circuit 18
To an external device. Further, the input / output buffer 14 is
Write data DQ0 to DQ0 in response to the mask control signal DQM
Mask DQ31.

The control signal latch 15 inputs the internal command from the command decoder 12 and the address data from the address buffer 13. Then, the control signal latch 15 outputs control signals for various processing operations such as write data write, read data read, refresh, and self refresh to the DRAM core 19 based on these internal commands and address data. To do.

The mode register 16 inputs the internal command (mode register set command) from the command decoder 12 and the address data from the address buffer 13. Then, the mode register 16 determines the DRAM core 1 based on these internal commands and address data.
9 holds the mode of various processing operations to be carried out for 9. Then, the mode register 16 outputs a control signal based on the held mode information.

The mode information held by the mode register 16 includes access form information. The access form information is information indicating the logical address map shape of the DRAM core 19. The mode register 16 outputs an address configuration selection signal generated based on the access form information to the address generation circuit 17.

The address generating circuit 17 inputs address data based on the address signals A0 to A10 from the address buffer 13. Then, the address generation circuit 17
Based on the mode of the mode register 16 and the address configuration selection signal, the row address data and the column address data generated corresponding to the logical address map shape of the DRAM core 19 at that time are output to the DRAM core 19. The address generation circuit 17 has a function of automatically generating a column address incremented from an input address based on the burst length set in the mode register 16.

The I / O control circuit 18 controls input or output based on the internal command from the command decoder 12. The I / O control circuit 18 outputs the write data (32 bits) from the input / output buffer 14 to the DRAM core 19 and the read data (32 bits) from the DRAM core 19 to the input / output buffer 14.

The DRAM core 19 is composed of a plurality of (four in this embodiment) banks, and each bank has a control signal from the control signal latch 15 and row address data and column address data from the address generation circuit 17. Respectively. That is, the DRA in the address buffer 13
Bank address signal BA corresponding to the number of banks of the M core
0, BA1 are input, and the control signal latch 15 and the address generation circuit 17 are provided for each bank.

The DRAM core 19 executes various processing operations such as write data write, read data read, refresh, and self-refresh on the built-in memory cell array based on the control signal and the address data. Therefore, the DRAM core 19 writes the write data DQ0 to DQ31 input from the input / output buffer 14 into the memory cell at the predetermined address based on the control signal and the address data.

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FIG. 2 is a schematic block diagram of the DRAM core 19. For simplification of description, one bank that constitutes the DRAM core 19 will be described here.
DRA
Each bank of the M core 19 includes a memory cell array 21,
The memory cell array 21 is configured by arranging a pluraiity of memory cells in an array. Each memory cell has a word line W
It is connected to L and a bit line (not shown), and the bit line is connected to the sense amplifier S / A. A column selection line CL is connected to the sense amplifier S / A. That is, in the memory cell array 21, the X expansion direction in which the word line WL is expanded by the X address (row address) and the column selection line CL and the sense amplifier S / A (S / A column) by the Y address (column address). The array is expanded in the Y expansion direction.

The memory cell array 21 has a plurality of row blocks divided in the X development direction and a plurality of column blocks divided in the Y development direction.
k). Here, the row block is a sense amplifier S / A (S) in the X expansion direction of the memory cell array 21.
/ A column). Further, the column block is a region divided in units of sub word lines SWL connected to the word lines WL in the Y expansion direction of the memory cell array 21.

The memory cell array 21 has a function of changing the logical address map shape according to the access form information held by the mode register 16, and this logical address map shape is an address configuration selection signal output from the mode register 16. (In this embodiment, the page
It is changed by the long designation signal).

More specifically, the memory cell array 21 changes the X address and the Y address according to the page length designation signal to change the logical address map shape. When the page length (the depth of the Y address) is changed by the page length designation signal, the sense amplifier S activated in response to the change.
The number of / A is changed. That is, the number of data that can be continuously accessed is changed.

The DRAM core 19 thus constructed
Are address signals A0 to A10 and bank address signals B input from a predetermined number of external address terminals.
Various processing operations such as data writing and reading are executed with respect to the memory cells at predetermined X and Y addresses based on A0 to BA1.

It should be noted that the number of external address terminals is set to the larger one of the number of terminals required for fetching the X address and the number of terminals required for fetching the Y address. Specifically, in the memory device 10 in which the X address is set to M bits and the Y address is set to N bits, for example, when M> N, the number of external address terminals is set to M. That is, the memory device (SDRAM) 10 of the present embodiment is provided with 13 external address terminals for taking in a maximum of 13-bit X address (including row address and bank address).

FIG. 3 is a block diagram illustrating a method of controlling the memory device 10. In the following description, the number of external address terminals is M. and the X address when the page length is set to the maximum value (hereinafter, full page) by the page length designation signal is M bits (XA <0: m>, (m = M-1)) and the Y address is N bits (YA <0: n>, (n = N-1)) (where M> N). Although the address buffer 13 (see FIG. 1) is functionally divided into the first to third address buffers 13a to 13c in FIG. 1 for convenience of description, the address buffer 13 may be configured without division.

Now, it is assumed that a page length shorter than the full page is set based on the page length designation signal from the mode register 16 and the X address increased by the page length designation signal is i bits. At this time, the Y address is reduced by i bits. This is because the substantial capacity (2^{M+N}) × I / O count of the memory cell array 21 does not change. Then, the increased i-bit X address is fetched from i of the (M-N + i) external address terminals which are not needed at the time of fetching the Y address.

More specifically, the first address buffer 13a
Is an internal command from the command decoder 12 (in the figure,
Address signal A based on the row address capture signal)
Enter 0-Am. The first address buffer 13a is
The input address signals A0-Am are amplified, and X address data based on them are latched and output to the address generation circuit 17.

The second address buffer 13b has an internal command (Column Addre in the figure) from the command decoder 12.
address signals A0-A (n
-Enter i). The second address buffer 13b amplifies the input address signals A0 to A (n-i), latches Y address data based on them, and outputs them to the address generation circuit 17.

The third address buffer 13c has an internal command (Column Addre in the figure) from the command decoder 12.
address signal A (n-i +)
1) -An is input. Third address buffer 13b
Amplifies the input address signals A (n-i + 1) to An, latches X address data or Y address data based on them, and outputs them to the address generation circuit 17.

The address generation circuit 17 includes first to third decoders (selection circuits in the figure) 17a to 17c, a clamp circuit 17d, and a switch circuit 17e. First to third
The decoders 17a to 17c, based on the address data from the first to third address buffers 13a to 13c, bank (BANK), row block (Row Block), word line W
L, column block (column block), column select line CL
Is appropriately selected according to the function of each decoder. The clamp circuit 17d invalidates any input address data and changes the decoding

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compression rate. For the sake of convenience of description, in the present embodiment, the address generation circuit 17 is functionally divided into the first to third decoders 17a to 17c, but may be configured not to be divided.

The first decoder 17a will be described in detail below.
Selects a bank, a row block, and a word line WL based on the X address data output from the first address buffer 13a, and DRs the X address corresponding to them.
Output to the AM core 19.

The second decoder 17b selects the column selection line CL based on the Y address data output from the second address buffer 13b, and outputs the corresponding Y address to the DRAM core 19.

Here, when the page length designating signal designates a page length shorter than the full page, the page length designating signal switches the switch circuit 17e to a predetermined connection position, and the third address buffer 13c becomes the third page. It is connected to the decoder 17c.

As a result, the third decoder 17c operates as the third decoder 17c.
Based on the X address data output from the address buffer 13c, the column block (specifically, the word line W
L) is selected and the corresponding X address is output to the DRAM core 19. That is, the i-bit X address increased by the page length designation signal is taken in from i of the (M−N + i) external address terminals which are not needed at the time of taking in the Y address. At this time, the switch circuit 17e connects the second decoder 17b to the clamp circuit 17d. As a result, the clamp circuit 17d
Invalidates unnecessary Y addresses when fetching Y addresses.

When the full page is designated by the page length designation signal, the third address buffer 13c is connected to the second decoder 17b. As a result, the second decoder 17b selects the column selection line CL based on the Y address data output from the third address buffer 13c, and outputs the corresponding Y address to the DRAM core 19.
Output to. At this time, the clamp circuit 17d
It is connected to the third decoder 17c and invalidates an unnecessary X address when the Y address is fetched.

For comparison, FIG. 33 shows a block diagram for explaining a conventional method of controlling a memory device. Conventionally, the address buffer 51 for fetching the X address
And an address buffer 52 for fetching the Y address
Are provided respectively. When using a short page length, the number (M or N) of external address terminals is increased according to the increased number of bits of the X address or Y address at that time.

FIG. 7 shows the memory device 10 of this embodiment.
5 is a waveform diagram showing the internal operation of FIG. Here, as an example, an operation waveform diagram of a 64 Mbit (megabit) SDRAM (32 I / O) is shown.

Now, in the initial state, the memory device 1
0 is a 13-bit X address (row address RA <0:10
>, Bank address BA <0: 1>), 8-bit Y address (column address CA <0: 7>), and the page length is set to 256 (full page). .

The memory device 10 responds to the mode register set command MRS with address signals A0-A.
10 is taken in as the address code Code (CodeA <0:10>), and the bank address Bank (BA <0: 1>) is taken in. Then, the memory device 10 determines the page length Pa based on the address code Code (CodeA <0:10>).
various settings such as ge, cast latency tCL, and burst length BL.

Now, the cast latency tCL = 3, the burst length BL = 2, and the page length Page = 32.
At this time, the memory device 10 uses the 16-bit X address (row address RA <0:13>, bank address BA <0: 1>
) 5-bit Y address (column address CA <0: 4>
) Of the logical address map shape. That is, the row address is increased by 3 bits as the page length is changed.

The memory device 10 takes in the address signals A0 to A10 as the row address Row (RA <0:10>) and takes in the bank address Bank (BA <0: 1>) in response to the active command ACT. Note that the fetching of the bank address is the same hereafter, and is therefore omitted.

The mode register set command MRS
The page length (= 32) set at the time of input may be set at the time of input of this active command ACT.
In this case, the number of row addresses to be fetched is reduced by the number of bits required to set the page length. For example, if 2 bits are required to set the page length, the memory device 10
The address signals A0 to A8 are set to the row address Row (RA <0: 8>
) And the address signals A9 and A10 as setting information. Alternatively, it may be fetched from another pin (DQ mask pin or the like) that is not used when the active command ACT is input.

Then, the memory device 10 responds to the read command RD1 input after a predetermined clock (for example, two clocks) after the input of the active command ACT, and outputs the address signals A0 to A5 to the column address Col (Col (C
The address signals A6 to A8 are taken in as the row address Row (RA <11:13>) as A <0: 4>).

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That is, the 3-bit row address Row which increases with the page length variable is fetched from the external address terminal which is not required when the column address Col (CA <0: 4>) is fetched when the read command RD1 is inputted. Be done. Then, the memory device 10 selects the column block and the word line WL based on the row address Row (RA <11:13>), and activates the selected word line WL and the sense amplifier S / A corresponding thereto. Let

In response to the active command ACT, the address signals A0 to A10 are transferred to the row address Row (RA <3:
13>) and address signals A6 to A8 in response to the read command RD1 to the row address Row (RA <0: 2>
). Further, the address signals A6 to A8 may be taken in at arbitrary bit positions of the row address Row in response to the read command RD1.

The memory device 10 sends the read command R
When D1 is issued, the set cast latency tC
Based on L (= 3) and burst length BL (= 2), read data D11 and D12 are sequentially output 3 clocks after the read command RD1 is input.

After that, the memory device 10 sequentially responds to the read commands RD2 and RD3 and outputs the column address Col (CA <0: 4>) and the bank address Bank (BA <0: 1.
>). At this time, in the second and subsequent read commands RD2 and RD3, the increased row address Row is not captured, and only the column address Col (CA <0: 4>) and the bank address Bank (BA <0: 1>) are captured.

In this embodiment, the read command RD
1 to RD3 have been described, the same applies to the case of a write command. That is, the active command AC
The increased row address Row (RA <11:13>) is taken in by the first write command after T input. And 2
In the write command after the first time, the column address Col
Only (CA <0: 4>) and bank address Bank (BA <0: 1>) are fetched.

For comparison, waveform diagrams showing the internal operation of the conventional memory device are shown in FIGS. 34 and 35. Figure 3
FIG. 4 is an operation waveform diagram of the 64 Mbit (megabit) SDRAM when the page length Page is set to 256 (full page). As shown in the figure, after the mode register set command MRS is input, the memory device
Row address R in response to active command ACT
ow (RA <0.10>) is taken in. Then, the memory device sequentially responds to the read commands RD1 to RD3 and fetches the column address Col (CA <0: 7>).

FIG. 35 is an operation waveform diagram of a 64 Mbit (Megabit) SDRAM in which the page length Page is set to 32. As shown in the figure, when a short page length (= 32) is used, the row address Row increases by 3 bits. That is, the memory device uses the active command A
Address signals A0 to A10 are fetched as row address Row (RA <0:10>) in response to CT, and address signal A1
Row address Row (RA <11:13>) with 3 to A15 increased
Take in as. Therefore, conventionally, a short page length (=
In the memory device set to 32), the number of external address terminals for taking in the increased 3-bit row address Row increases compared to the standard product.

FIG. 8 is a block diagram for explaining access control after issuing the active command ACT in FIG. In the figure, the same components as those in FIG. 3 are designated by the same reference numerals, and detailed description thereof will be partially omitted.

The command decoder 12 (see FIG. 1) includes a command judging circuit (Command judging circuit in the drawing) 12a,
First page command detection circuit (Pa in the figure) for detecting the first activation signal output from the command determination circuit 12a.
ge Command first detection circuit) (hereinafter, command detection circuit) 12b is included. In this embodiment, the activation signal is a signal that activates the word line WL and the sense amplifier S / A.

The command determination circuit 12a determines a read command and a write command among various commands decoded in response to the internal clock signal CLK1 and outputs a read activation signal or a write activation signal according to the determination.

Now, when the read command RD1 shown in FIG. 7 is input, the command determination circuit 12a outputs a read activation signal. The second address buffer 13b (Address Latch in the figure) includes an OR circuit 31 and a delay circuit 3.
The address signals A0 to A4 are input based on the read activation signal (read command RD1) input via 2. Then, the second address buffer 13b converts the column address data based on the address signals A0 to A4 into the second decoder 17b (Column Address Decoder in the figure).
Output to.

Third address buffer 13c (in the figure, Addr
ess Latch) receives the command detection circuit 12 by the first read activation signal (read command RD1) input to the command detection circuit 12b via the OR circuit 31.
Address signal A5 based on the detection signal output from b
-Enter A7. Then, the third address buffer 13
c is a third decoder 17c (in the figure, Column Block) that outputs the row address data based on the address signals A5 to A7.
Output to the selection Address Decoder).

The second decoder 17b selects the column selection line Ci. based on the column address data output from the second address buffer 13b. Third decoder 17c
Are column blocks and word lines WL based on the row address data output from the third address buffer 13c.

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Select. As a result, the word line WL and the sense amplifier S / A are activated.

In this way, the command detection circuit 12b
Detects only the first read activation signal (read command RD1) output from the command determination circuit 12a, and based on the detection signal from the command detection circuit 12b, the expanded row address Row (RA <11 : 13>) is held in the third decoder 17c.

Then, the second read activation signal (see FIG.
The read command RD2) shown in FIG.
No detection signal is output from 2b. That is, in the read commands RD2 and RD3 issued after the second time, the address signals A5 to A7 are not taken into the third address buffer 13c.

13 and 14 are circuit diagrams showing an example of the specific circuit configuration of FIG. 6 described above. Moreover, FIG.
FIG. 5 is a waveform diagram showing an example of the internal operation of the circuits shown in FIGS. 13 and 14.

For comparison, a block diagram for explaining conventional access control is shown in FIG. Since this figure explains the principle of conventional access control, the same reference numerals are given to the components having the same functions. As shown in FIG. 36, since the page length is 256 in the related art,
The column address Col (CA <0: 4>) and the column address Col (CA <5: 7>) are fetched each time a read or write activation signal (that is, a read or write command) is output.

FIG. 9 is a block diagram for explaining a case where the access control described in FIG. 8 is performed according to the page length. In this configuration, the connection position of each of the switch circuits 33a and 33b is switched based on the page length designation signal, so that the address signals latched by the second and third address buffers 13b and 13c are appropriately changed according to the page length. be able to. Accordingly, the second and third decoders 1
7b and 17c are DRAMs according to the page length.
The row address and the column address generated corresponding to the logical address map shape of the core 19 are output to the DRAM core 19.

FIG. 10 is a schematic block diagram illustrating activation control of word line WL and sense amplifier S / A.
As shown in the figure, the word line activation circuit 41 and the sense amplifier activation circuit 42 respond to the output signal of either the command determination circuit 12a or the command detection circuit 12b input according to the page length designation signal. Word line WL,
Each sense amplifier S / A is activated.

More specifically, when the page length Page is set to the full page by the page length designation signal, each activation circuit 41, 42 responds to the active signal (active command) from the command determination circuit 12a. W
L and the sense amplifier S / A are activated respectively. This is because all the bits of the row address necessary for selecting the word line WL and the sense amplifier S / A are aligned when the active command is received.

On the other hand, the page length P is given by the page length designation signal.
When the page length is set to be shorter than the full page, each activation circuit 41, 42 responds to the detection signal from the detection circuit 12a, that is, the read or write activation signal (read or write command), to write the word. The line WL and the sense amplifier S / A are activated respectively. This is because a row address accepted by the active command and a row address accepted by the page command are required to select the word line WL and the sense amplifier S / A to be activated.

For comparison, FIG. 37 shows a block diagram for explaining a conventional control method of the activation circuit. Since this figure illustrates the principle of conventional activation control, the same reference numerals are given to components having the same function. As shown in FIG. 37, conventionally, each activation circuit 41, 42 is
Activates the word line WL and the sense amplifier S / A only by the active signal from the command determination circuit 12a.

As described above, according to this embodiment, the following effects can be obtained. (1) The memory device 10 responds to the page length designation signal output from the mode register 16 in accordance with the DRAM core 1
9 changes the logical address map shape. When the page length is set shorter than that of the full page, the row address Row thus increased is fetched when the first read command RD1 is input. In this way, the increasing row address Row is fetched in a time division manner by using the external address terminals which are not used at that time,
The page length can be changed without changing the number and arrangement of external address terminals, and a general-purpose package can be used. Therefore, it is possible to prevent the development period from increasing and the cost from increasing.

(2) Since the page length can be changed without changing the package, an efficient access method according to the system of the customer who uses the memory device can be realized.

(3) Since the page length can be shortened without changing the package, the activation number of the sense amplifier S / A can be reduced to the necessary minimum, and the current consumption can be reduced. Can be realized.

(Second Embodiment) A second embodiment of the present invention will be described below. In the present embodiment, when the page length is similarly changed from 256 to 32 using the memory device 10 of the first embodiment, another control method of the row address fetching method that increases with the page length change. To explain. Therefore, the same name is assigned to the same component, and the detailed description thereof is partially omitted.

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FIG. 18 is a waveform diagram showing the internal operation of the second embodiment. In the present embodiment, as shown in FIG.
The read command RD1 is input one clock after the active command ACT. That is, the first read command RD1 after the active command ACT is input.
Is set to tRCD = 1, and the read command RD1 is input one clock earlier than in the first embodiment. (By the way, in the first embodiment, tRCD = 2 (see FIG. 7).) Therefore, the row address Row (RA <11:13>) that increases with the page length change (change from 256 to 32) is executed in the first embodiment. it is taken in by one clock earlier than the form, and thereby the word line WL and the sense amplifier S / A corresponding thereto are activated almost one clock earlier.

By the way, generally, in order to completely complete the activation operation of the word line WL, it is necessary to delay (wait) from the input of the active command ACT to the start of the access operation by the input of the read command RD1. This grace period varies depending on the frequency of the clock signal, but normally 2 clocks are required at the general clock frequency of the device currently used. Therefore, it is necessary to delay the start timing of the access operation based on the read command RD1 by substantially one clock from the time when the read command RD1 is input.

On the other hand, the CAS latency tCL defines the period (clock number) from the input of the read command to the output of the read data. Therefore, as shown in FIG. 18, the CAS latency tCL corresponding to the first read command RD1 is a preset value of the CAS latency tCL from tCL = 3 (set value) to tCL = 4. Is changed to. Therefore, the memory device reads the read data D1 4 clocks after the read command RD1 is issued.
1, D12 are sequentially output.

Thereafter, the memory device responds to the read commands RD2 and RD3 and outputs the column address Col (CA <0:
4>) and the bank address Bank (BA <0: 1>) are sequentially taken in, and the preset latency tCL (tCL = tCL =
3: Read data is sequentially output according to the set value).

At this time, similarly to the above, in the second and subsequent read commands RD2 and RD3, the increased row address Row is not taken in and the column address Col (CA <0: 4
>) And bank address Bank (BA <0: 1>) are taken in. In the present embodiment, the read commands RD1 to R
Although D3 has been described, the same applies to the case of a write command.

FIG. 19 is a block diagram for explaining the control method of the cast latency tCL. In this embodiment, the command decoder 12 (see FIG. 1) includes the command determination circuit 12a, a page command first detection circuit 12b, and a Cas Latency control circuit 12c.

Similarly to the above, the command determination circuit 12a
Determines whether it is a read command or a write command, and outputs a read activation signal or a write activation signal. The command detection circuit 12b is the command determination circuit 12
The first read activation signal or write activation signal output from a is detected, and the detection signal is output to the CAS latency control circuit 12c.

The CAS latency control circuit 12c outputs an output control signal at a predetermined clock number in response to the internal clock signal CLK1 and issues an internal command (read commands RD1 to RD3 in FIG. 18). The time from when the output data is determined to when the output data is determined, that is, the CAS latency tCL is controlled.

Then, the CAS latency control circuit 12c
When the detection signal is output from the command detection circuit 12b, changes the value of the CAS latency tCL at that time in response to the detection signal. In addition, specifically, the CAS latency control circuit 12c of the present embodiment responds to the detection signal from the command detection circuit 12b in response to the CAS latency t.
The value of CL is increased by 1 from a predetermined value (setting value).

That is, in FIG. 18, the cast latency tCL is set to tCL = 3 (set value) by the mode register set command MRS. Next, after issuing the active command ACT, the first read command R
When D1 is input, the CAS latency control circuit 12c
A detection signal output from the command detection circuit 12b is input to the. In response to this detection signal, the CAS latency control circuit 12c causes the value of the CAS latency tCL (t
CL = 3: set value) is changed to tCL = 4. That is, the CAS latency control circuit 12c changes tCL = 4 only when the first read command RD1 is input, and sets tCL = 3 for the second and subsequent read commands RD2 and RD3.

As described above, this embodiment has the following effects. (1) In the present embodiment, the first read command RD1 after the active command ACT is input is input one clock earlier than that in the first embodiment, so that the row address Row that increases as the page length is changed is first input. 1 rather than form
It is captured earlier by the clock. Therefore, the word line WL and the sense amplifier S / A can be activated earlier by almost one clock. At that time, the CAS latency tCL corresponding to the read command RD1 is changed to tCL = 4 by the CAS latency control circuit 12c, thereby activating the word line WL and the sense amplifier S / A and then outputting the read data. The period is sufficiently secured
This prevents the start timing of the access operation based on the read command RD1 from being delayed when the page length is variable.

(Third Embodiment) The third embodiment of the present invention will be described below. In the present embodiment, when the page length is similarly changed from 256 to 32 using the memory device 10 of the first embodiment, another control method of the row address fetching method that increases with the page length change. To explain. Therefore, the same name is assigned to the same component, and the detailed description thereof is partially omitted.

FIG. 20 is a block diagram for explaining the access control of the third embodiment. In the present embodiment, the command decoder 12 (see FIG. 1)

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includes the command determination circuit 12a and a predetermined time detection circuit (hereinafter, time detection circuit) 12d.

The detection circuit 12d has an internal clock signal C
LK1, the active signal and the read or write activation signal output from the command determination circuit 12a are input.

That is, the command determination circuit 12a outputs an active signal when the internal command is the active command ACT. In response to the active signal, the time detection circuit 12d outputs an address fetch signal for fetching the increased row address after a predetermined time (hereinafter referred to as address latency tAL) has elapsed.

In the present embodiment, the address latency tAL is set based on the internal clock signal CLK1, and the time detection circuit 12d uses the internal clock signal CLK.
After counting a predetermined number of clocks based on 1, an address fetch signal is output. At this time, the time detection circuit 1
2d outputs the address take-in signal until the command read circuit 12a outputs the first read activation signal or write activation signal.

Now, when the page length is set to 32, the switch circuit 33 is switched to the connection position shown in FIG. 20 by the page length designating signal.
Third address buffer 1
3c amplifies the input address signals A0-An based on the address take-in signal from the time detection circuit 12d, latches the row address data based on them, and outputs the row address data to the third decoder 17c. Then, the third decoder 17c
Is a row address (RA <0: n>) for specifying the column block (word line WL) corresponding to the row address data.
To the DRAM core 19 (FIG. 1).

Incidentally, as shown in FIG. 20, the row address (increased row address) fetched based on the detection signal from the time detection circuit 12d is changed to the second and third buffers 13b, 13b based on the page length designation signal. It is taken in by any of 13c. Note that FIG. 22 is a circuit diagram showing an example of a specific circuit configuration of the time detection circuit 12d of FIG.

FIG. 21 is a waveform diagram showing the internal operation of this embodiment. In the same figure, a case where the address latency tAL of the time detection circuit 12d is set to, for example, tAL = 1 will be described.

As shown in FIG. 21, the page length is variable (25
Row address Row increased with the change from 6 to 32)
(RA <0: 4>) is captured by the address capture signal from the time detection circuit 12d one clock after the active command ACT is input. As a result, the column block and the word line WL are selected, and the selected word line WL
And the corresponding sense amplifier S / A is activated.

Thereafter, the memory device 10 sequentially responds to the read commands RD1 to RD3 and outputs the column address C.
ol (CA <0: 4>) and bank address Bank (BA <0: 1>)
Of the preset cast latency (tCL
= 3), the read data is sequentially output according to the burst length (BL = 2). At this time, similarly to the above, in the read commands RD1 to RD3, the increased row address Ro is increased.
The w is not fetched, but only the column address Col (CA <0: 4>) and the bank address Bank (BA <0: 1>) are fetched. In the present embodiment, read commands RD1 to RD
3 has been described, the same applies to the case of a write command.

As described above, this embodiment has the following effects. (1) The command decoder 12 includes the command determination circuit 12
A time detection circuit 12d that outputs an address fetch signal after a predetermined time (address latency tAL) has elapsed in response to the active signal from a is provided. As a result, the row address Row that has increased as the page length is changed is fetched one clock after the active command ACT (tAL
= 1). Therefore, similarly to the second embodiment, the word line WL and the sense amplifier S / A can be activated quickly. Further, in the present embodiment, the increased row address Ro
Since w is fetched at a timing earlier than the input of the read command RD1, the fetch is not affected by the arrangement of external address terminals.

(2) The timing of the active command ACT and the read command RD, and the address signal designated at the time of output thereof do not depend on the page length (logical address map shape). That is, the memory controller (CP
U) It only outputs the address signal corresponding to the row address extended between the active command ACT and the read command RD. Therefore, the change is easy, and a new function (function of changing the logical address map shape) can be used without trouble.

(Fourth Embodiment) A fourth embodiment of the present invention will be described below. In this embodiment, the address latency t of the time detection circuit 12d in the third embodiment is used.
The case where AL is set to, for example, tAL = 0.5 will be described.

FIG. 23 is a waveform diagram showing the internal operation of the fourth embodiment. In this embodiment, as shown in FIG.
The row address Row that increases as the page length is changed (changed from 256 to 32) is taken in by an address take-in signal from the time detection circuit 12d 0.5 clocks after the input of the active command.

That is, the memory device 10 takes in the row address Row (RA <0:10>) at the rising edge of the clock signal CLK based on the input of the active command ACT, and clock signal CL after 0.5 clocks.
The row address Row (RA <that increased at the falling edge of K

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0: 4>).

As described above, in this embodiment, by setting the address latency tAL = 0.5, the increased row address Row is fetched by 0.5 clock earlier than in the third embodiment, whereby the word line is read. The WL and the corresponding sense amplifier S / A are activated for about 0.5 clocks.

Thereafter, the memory device 10 sequentially responds to the read commands RD1 to RD3 and outputs the column address C.
ol (CA <0: 4>) and bank address Bank (BA <0: 1>)
Of the preset cast latency (tCL
= 3), the read data is sequentially output based on the burst length (BL = 2). At this time, similarly to the above, in the read commands RD1 to RD3, the increased row address R
ow is not taken in, column address Col (CA <0. 4>)
And only the bank address Bank (BA <0: 1>) is fetched. In the present embodiment, read commands RD1 to RD
3 has been described, the same applies to the case of a write command.

As described above, according to this embodiment, the following effects can be obtained. (1) In this embodiment, the address latency tAL is
Since tAL = 0.5 is set, the row address Row increased as the page length is changed is changed to the active command A
Captured 0.5 clocks after CT. Therefore, the word line WL and the sense amplifier S / A can be activated by about 0.5 clock earlier than in the third embodiment.
This prevents the start timing of the access operation based on the read command RD1 from being delayed when the page length is variable.

The above embodiments may be implemented in the following modes. In each of the above embodiments, the number of bits of the memory cell, the address configuration, the switching type of the address configuration, etc. are not limited to this example.

In FIG. 3, the clamp circuit 17d is
Although it is provided in the address generation circuit 17, it may be provided separately. The configuration of FIG. 3 may be modified as shown in FIG. That is, dedicated address buffers 13f and 13g for fetching the Y address and the X address based on the address signals A (n-i + 1) to An may be provided, respectively.

The configuration of FIG. 3 may be modified as shown in FIG. That is, each of the address buffers 13h to 13j
Are configured to share an address buffer for fetching the X address or the Y address, respectively. Then, those output signals (X address data or Y address data) may be appropriately selected by the XY switching signal.

The configuration of FIG. 3 may be modified as shown in FIG. That is, as in FIG. 5, each address buffer 1
3k, 13l, and 13n are configured to share an address buffer for fetching an X address or a Y address, respectively, and an address (X
Address buffer 13 for fetching only (address)
You may make it provide m separately.

The command determination circuit 12a and the command detection circuit 12b shown in FIG. 8 may be replaced with another configuration which does not depend on the clock signal CLK1 when the memory device is an asynchronous type.

In FIG. 16, the sense amplifier (S /
A) Only the activation circuit 42 may be controlled. The configuration of FIG. 8 may be modified as shown in FIG.
That is, the third address buffer 13c fetches the address signals A5 to A7 every time for each read / write activation signal (that is, read / write command) from the command determination circuit 12a. Then, based on the detection signal from the command detection circuit 12b, the third decoder 17c causes the third address buffer 1 to perform the read / write command after the second time.
The row address data from 3c may not be re-latched. 16 and 17 are circuit diagrams showing an example of the specific circuit configuration of FIG.

Further, FIG. 12 shows a case where the address control performed by the configuration of FIG. 11 is performed according to the page length. In this configuration, the connection positions of the switch circuits 33a and 33b are switched by the page length designation signal, so that the row address and the column address generated corresponding to the logical address map shape of the DRAM core 19 at each time according to the page length. Is the second and third decoders 17b, 1
7c respectively outputs.

In the first and second embodiments, the address increased as the page length is changed is changed to the active command ACT.
The Y address is fetched at the same time as the Y address fetched by the first read / write command after input, but the present invention is not limited to this example. That is, the increased address is read / read first
After being fetched by the write command, the Y address may be fetched after a predetermined clock (for example, one clock) of the command.

In the third and fourth embodiments, the time detection circuit 12d outputs the detection signal after a predetermined clock in response to the active signal, but when embodying it in an asynchronous memory device, , internal clock signal CL
The detection signal may be output after a predetermined time (tAL) has elapsed regardless of K1.

A double data rate (DDR) method is used as another means for realizing the method of fetching the row address Row increased at the address latency tAL = 0.5 as in the fourth embodiment. You may embody it. That is, the clock signals CLK, / CL
Using two clock signals represented by K (/ is a bar), a row address is fetched at the rising edge of the clock signal CLK, and a clock signal / C having a 180 ° phase difference immediately after that is fetched.
The row address increased at the rising edge of LK may be fetched.

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In each of the above embodiments, the page length is specified when the mode register set command MRS is input or when one type of active command ACT is input. However, two types of active commands ACT are used to specify the page length. The page length may be designated based on the input of ACT.

In each of the above-mentioned embodiments, the synchronous memory device is embodied, but an asynchronous memory may be configured so that the logical address map shape can be changed. Since the schematic configuration of the asynchronous memory is already known, the drawing and description thereof are omitted.

This memory device determines the address signal ADD as the X address (row address) at the fall of the chip enable signal (/ CE) or the row address strobe signal (/ RAS). Next, the memory device determines the address signal as a Y address (column address) by a read or write control signal,
The cell specified by those addresses is accessed.

The change of the logical address map shape is performed by the following illegal entry method (a control method from the outside which is not normally used in the access from the outside). In the illegal entry method, the address configuration select signal inside the memory device is generated earlier than the word line activation signal from the chip enable signal / CE, as in the case of using the mode register set command in the synchronous method (MRS method). To do. As a result, access delay can be prevented without delaying the switching operation of the address generation circuit or its output.

The illegal entry method will be described in detail. FIG. 24 is a waveform diagram illustrating a mode setting cycle for address configuration. The memory device has a dedicated terminal for mode setting for address configuration, and by fetching the necessary information from the dedicated terminal to the information for determining each type of address configuration, it is possible to prevent external access delay and prevent malfunction. The safe operation of normal operation can be guaranteed.

That is, the memory device does not operate normally when the chip enable signal / CE1 is at the H level. During this period, the address code Code based on the address signal ADD is fetched in response to the program mode signal / PE (= address configuration setting terminal) input from the dedicated terminal. Specifically, the memory device activates the input of the address code at the falling edge of the program mode signal / PE, and latches the address code information at the rising edge of the signal / PE.

On the other hand, when the chip enable signal / CE1 is at the L level, the memory device enters the operation state corresponding to the external access and fetches the address signal ADD corresponding to the external access.

In the figure, t1 to t5 are external specification timing conditions. At the timing shown in the figure, the input circuit of the external dedicated terminal is activated at the fall of the program mode signal / PE to start the decoding operation for the address signal. Then, the decoding result is determined at the rising edge of the program mode signal / PE, and the input circuit is deactivated. By this operation, power consumption can be reduced.

In the mode setting cycle for the above address configuration, the logic of the program mode signal / PE may be inverted. The address code may be input from a data terminal (called a DQ or I / O pin).

Further, as will be described later, the mode may be determined after the program cycle by the code method is repeated several times. FIG. 25 is an explanatory diagram of commands.

When using this command, a memory device of a specification system which recognizes a command with respect to a reference clock (system clock CLK or chip enable signal / CE1) and performs an external access operation is targeted.

Therefore, in the memory device of the specification system which does not operate by the command with respect to the chip enable signal / CE1, the address is simply used as information for determining each kind of address configuration based on FIG. It can be used as the number of times

Commands (1) to (6), (8) to (1
0) is a command used in normal operation, and commands (7) and (11) are commands that have no meaning in normal operation. The command (7) is a write (WR) operation but does not input data (masked) because the signals / LB and / UB are at the H level. Command (11)
Is a read (RD) operation, but similarly the signal / LB,
No data is output because it is masked by / IB.

As described above, by fetching a command (illegal command) not used for normal operation as information for determining each type of address configuration, it is possible to set information without providing a dedicated terminal.

FIG. 26 is a waveform diagram for explaining the mode setting cycle for address configuration. By continuously inputting a plurality of commands (11) shown in FIG. 25, information necessary for mode setting for address configuration is shown. Shows the case where is taken in as an address code

The memory device takes in the address signal ADD as the address code Code in response to the command (11). This operation is repeated N times. N from the first time
When all the N address codes Code fetched corresponding to the command (11) up to the first match, the address code Code is validated and the mode setting for the address configuration is performed.

The command (11) is N? When they match once, mode setting for address configuration may be performed based on the address code Code fetched corresponding to the Nth command (11). Further, the fetching of the address code Code is performed in an arbitrary cycle (for example, 1
It may be changed to the first time). Various other applications can be developed.

As the address code for setting the mode, the number of address Bits may be determined corresponding to the number of types of address configuration. In the

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case of N mode setting cycles as shown in FIG. 26, a counter circuit is used inside the device. When the upper bits of the counter circuit change for N number of mode setting cycle entries, the circuit configuration is such that the mode is determined.

FIG. 27 is an operation waveform diagram of an entry control circuit which is a mode setting circuit for program address configuration. As shown in FIG. 27A, the first entry circuit outputs the H-level first address enable signal proaddz in the third cycle, and outputs the first entry signal proentz in the fourth cycle. Then, the first entry circuit uses the first address enable signal proa.
Reset ddz and the first entry signal proentz at the same time. As a result, the memory device sends the previously determined address configuration information to the 4th by the first entry signal proentz.
The information of the latest address configuration is changed according to the address code information fetched in the second cycle.

As shown in FIG. 27 (b), the first entry circuit causes the other commands (device activation active command and read / write command) during counting. When is accepted, the count is reset. As a result, the first address enable signal proaddz and the enable signal proaddz are held at the L level.

That is, in the mode setting for determining each type of address configuration, if the same command for that purpose does not continue for the specified number of times, it is canceled. (The memory device maintains the previously determined address configuration information) FIG. 28 is an operation waveform diagram of the entry control circuit (second entry circuit) which is the mode setting circuit for the program address configuration corresponding to FIG. is there.

The second entry circuit outputs the H-level address enable signal peaddz in response to the L-level program mode signal / PE, and then responds to the H-level program mode signal / PE in the H-level enable signal.
Output peaddz. As a result, the memory device transmits the information of the previously determined address configuration to the second entry signal proe.
It is changed to the latest address configuration information according to the address code information imported by ntz.

FIG. 29 is an operation waveform diagram of the entry signal generating circuit. As shown in FIG. 29A, the signal generation circuit responds to the first entry signal proentz by generating the combined signal en.
Output tz. Further, as shown in FIG. 29 (b), the signal generation circuit responds to the entry signal peentz by combining signal en
Output tz.

FIG. 30 is an operation waveform diagram of the mode setting address buffer for address configuration. The address buffer activates the input circuit in response to the H-level address enable signal peaddz and outputs the address signal az <0: 3>. The same operation is performed in response to the first address enable signal proaddz.

FIG. 31 is an operation waveform diagram of the mode setting address latch for address configuration. The address latch uses the address setting az <0: 3> output in response to the H level address enable signal peaddz and latches the code Code latched in response to the combined signal entz for setting the mode. Output as <0: 3>.
The same operation is performed in response to the first address enable signal proaddz.

The mode setting decoder for address configuration uses the mode setting address signal paz <for address configuration.
0: 3> is decoded and an address configuration select signal for several types of address maps is output.

FIG. 32 is an operation waveform diagram of the mode setting decoder. The decoder uses the mode setting address signal pa
Decode z <0: 3> to select one of the address configuration select signals for several types of address maps and bring it to H level.

When the depth of the X address is smaller than the depth of the Y address, the address configuration setting terminal can be shared by the address terminals which are not used when active.
The command for setting the address configuration can be a precharge command or another new command in addition to the active command.

The function of changing the address map is independently realized for each bank. System performance is further improved by setting (changing) the logical address map for each bank.

The position of the address bit to be clamped may be changed appropriately. The position of the address bit to be invalidated may be changed appropriately. In each of the above embodiments, the logical address map shape can be changed from outside at any time, but a ROM such as bonding or Fuse is provided, and the logical address map shape is changed to a desired shape at the time of shipment or user use,
You may make it maintain the shape. Also, a ROM that can be rewritten from the outside may be provided, and the logical address map shape may be changed as necessary. In these cases, the logical address map shape is fixed for a short period or a long period. Therefore, the existing program and CPU can be used. Further, it is possible to save the trouble of changing the logical address map shape for each row access cycle.

The features of this embodiment are summarized as follows. (Supplementary note 1) M-bit first address and N-bit second
An address terminal for taking in an address at the same time is provided, or an address terminal having a larger number of M-bit first address and N-bit second address is provided, and memory cells are arrayed at the first address and the second address. In a storage device accessing an arrayed memory cell array, a part of an external address input from the address terminal is set to a first address or a second address based on access form information for changing a logical address map shape of the memory cell array. A storage device comprising address replacement means for replacement. (Supplementary Note 2) M-bit first address and N-bit second
An address terminal for taking in an address at the same time is provided, or an address terminal having a larger number of M-bit first address and N-bit second address is provided, and memory cells are arrayed at the first address and the second address. In a storage device that accesses arranged memory cell arrays, an address invalidating unit that invalidates an external address or a part thereof input from the address terminal based on access form information that changes a logical address map shape of the memory cell array. A storage device comprising: (Supplementary Note 3) A predetermined time detecting means is

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provided for outputting a control signal for fetching an i-bit increasing address that increases in accordance with the change of the logical address map shape, after a lapse of a predetermined time after the first address fetch. 3. The storage device according to appendix 1 or 2, characterized in that. (Supplementary note 4) The storage device according to supplementary note 3, wherein the predetermined time detection unit outputs the control signal after a predetermined clock of a clock signal in response to an active command for fetching the first address. (Supplementary Note 5) A control signal for fetching an i-bit increasing address that increases according to the change of the logical address map shape is generated based on a command issued at the time of the (N-i) -bit second address fetch control. 3. The storage device according to appendix 1 or 2, further comprising a command detection unit for outputting. (Additional remark 6) The command detection unit detects the first read or write command after the active command for fetching the first address, and outputs the control signal based on the read or write command. 5. The storage device according to item 5. (Supplementary Note 7) The storage device according to Supplementary Note 6, further comprising a cast latency control unit that delays the cast latency corresponding to the first read or write command based on a control signal from the command detection circuit. (Supplementary note 8) The storage device according to any one of supplementary notes 3 to 6, further comprising a word line activation unit that activates a word line based on a control signal for fetching the increased address of i bits. (Supplementary note 9) The supplementary note 3 is characterized in that it further comprises a sense amplifier activating means for activating the sense amplifier based on a control signal for fetching the i-bit increased address.

7. The storage device according to any one of items 6 to 6. (Supplementary note 10) The storage device according to supplementary note 2, wherein the address invalidating unit includes a unit that clamps an arbitrary address in order to vary a compression rate of decoding. (Supplementary Note 11) A control signal to which the access form information is applied, or a combination of a plurality of control signals, is provided, which is provided with a unit for generating an address configuration selection signal according to the setting of the logical address map shape, and the address control unit or the Note 1 that the address invalidating means executes the replacement or the invalidation based on the address configuration selection signal

Alternatively, the storage device according to item 2. (Supplementary Note 12) An external address is input, and based on the address configuration selection signal, an output signal thereof is converted into a first signal generation circuit for generating a selection signal in the first address direction and a selection signal in the second address direction. 12. The storage device according to appendix 11, further comprising an address generation circuit having a switching circuit for switching to a second signal generation circuit for generation. (Supplementary note 13) The storage device according to Supplementary note 1 or 2, wherein the address control unit or the address invalidation unit includes a ROM such as a bonding or a Fuse that stores the access form information. (Supplementary Note 14) The storage device according to Supplementary Note 1 or 2, wherein the address control unit or the address invalidation unit includes an externally rewritable ROM that stores the access form information. (Supplementary Note 15) is there an address terminal for simultaneously capturing an M-bit first address and an N-bit second address?

Alternatively, a memory device having an address terminal having a larger number of M-bit first address and N-bit second address, and accessing a memory cell array in which memory cells are arrayed at the first address and the second address In the internal control method, wherein a part of the external address input from the address terminal is replaced with a first address or a second address based on access form information for changing a logical address map shape of the memory cell array. Internal control method for storage device. (Supplementary Note 16) is there an address terminal for simultaneously taking in an M-bit first address and an N-bit second address?

Alternatively, a memory device having an address terminal having a larger number of M-bit first address and N-bit second address, and accessing a memory cell array in which memory cells are arrayed at the first address and the second address The internal control method according to claim 1, wherein the external address input from the address terminal or a part thereof is invalidated based on access form information for changing the logical address map shape of the memory cell array. Internal control method. (Supplementary Note 17) The internal control method for a storage device according to Supplementary Note 15 or 16, wherein the access mode information is set to be set during a standby period or at the same time as an active operation. (Supplementary note 18) The internal control method in the storage device according to any one of supplementary notes 15 to 17, wherein the number of activated sense amplifiers is controlled according to the shape of the logical address map (Supplementary Note 19) Supplementary note 15 characterized in that the compression rate of decoding is varied according to the shape of the logical address map.

19. An internal control method in the storage device according to any one of 18 to 18. (Supplementary Note 20) An address configuration selection signal according to the setting of the logical address map shape is generated by a control signal to which the access form information is applied, or a combination of a plurality of control signals, and the address configuration selection signal is generated based on the address configuration selection signal. 19. The internal control method for a storage device according to any one of appendices 15 to 18, characterized in that the replacement or the invalidation is executed. (Supplementary note 21) The internal of the storage device according to supplementary note 20, wherein the first and second addresses are generated by a common address generating means, and an output destination of the common address generating means is switched by the address configuration selection signal. Control method. (Additional remark 22) The first and second address generating means for generating the first and second addresses according to an external address are provided, and the input destination of the external address is switched by the address configuration selection signal. An internal control method in the storage device described. (Supplementary note 23) The internal of the storage device according to supplementary note 15 or 16, characterized in that an i-bit increasing address that increases according to a change in the shape of the logical address map is fetched in time division after the first address is fetched. Control method. (Supplementary Note 24) The address latency control is such that after the first address is fetched in synchronization with a clock signal, the i-bit increased address is fetched in synchronization with a predetermined clock of the clock signal. 24. An internal control method in the storage device according to attachment 23. (Supplementary Note 25) The address latency control is based on the i

25. The storage device according to claim 24, further comprising, a step of previously capturing a predetermined number of clocks of the clock signal after capturing the first address so as to generate a control signal for capturing an increased address of bits. Internal control method. (Supplementary note 26) The internal control method in the storage device according to supplementary note 25, wherein the step is performed before or at the time of fetching the first address. (Supplementary Note 27) The supplementary note 25, wherein the step is performed by a command and is set in a mode register.

Or an internal control method in the storage device according to item 26. (Supplementary note 28) The above step is performed with a command including an address code before fetching the first address,

Note 25 or 26, characterized in that the first address is fetched by two types of active commands

An internal control method in the storage device described. (Supplementary note 29) The supplementary note 15 or 16, wherein an i-bit increasing address that increases in accordance with the change of the logical address map shape is performed simultaneously with the fetch control of the (N−i) -bit second address.

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Internal control method in storage device. (Supplementary note 30) An increased address of i bits that increases according to the change of the logical address map shape is output from an address terminal that is not used when the second address of (Ni) bits is taken out of the N address terminals. The internal control method in the storage device according to appendix 15 or 16, wherein the internal control method is incorporated. (Supplementary note 31) The supplementary note 15 or 16 is characterized in that an i-bit incremented address that increases in accordance with the change of the logical address map shape is performed at the next command after the active command for fetching the first address. Internal control method in storage device. (Supplementary note 32) The internal control method in the storage device according to supplementary note 31, wherein the increased address of i bits is fetched at the same time as the read or write command after the active command. (Supplementary Note 33) A command detecting unit for detecting a first read or write command after the active command is provided, and delaying the CAS latency corresponding to the first read or write command based on an output signal of the command detecting unit is provided. 33. An internal control method in a storage device according to Supplementary Note 32. (Supplementary Note 34) A predetermined time detecting means for outputting a signal for taking in the increased address of the i-bit after a lapse of a predetermined time after taking in the first address is provided, and an output signal of the command detecting means or the predetermined time detecting means is provided. 34. An internal control method in a memory device as set forth in appendix 33, wherein the word line is activated based on the above. (Supplementary note 35) The internal control method in the storage device according to supplementary note 33 or 34, wherein the sense amplifier is activated based on an output signal of the command detecting unit or the predetermined time detecting unit. (Supplementary Note 36) Is there an address terminal for simultaneously taking in an M-bit first address and an N-bit second address?
Alternatively, a storage means is provided which has an address terminal having a larger number of a M-bit first address and an N-bit second address, and which accesses a memory cell array in which memory cells are arrayed at the first address and the second address. And a control means for accessing and controlling the access means, the control means supplies the access form information to the storage means from time to time, and the storage means changes based on the access form information. The system, wherein the increased address of i bits, which increases according to the shape of the logical address map of the memory cell array, is generated in a time division after the generation of the first address. (Supplementary note 37) The system according to supplementary note 36, wherein the control means performs the access form information by using one of an address, a decoder, and code information based on a control signal. (Supplementary note 38) The system according to supplementary note 36 or 37, wherein the control means supplies the access form information at the same time as or before the start of access. (Supplementary note 39) Is there an address terminal for simultaneously taking in an M-bit first address and an N-bit second address?
Alternatively, a storage means is provided which has an address terminal having a larger number of a M-bit first address and an N-bit second address, and which accesses a memory cell array in which memory cells are arrayed at the first address and the second address. And a control method of a storage means in a system including a control means for accessing and controlling the storage means, wherein the control means comprises a logical address of a memory cell array included in the storage means in accordance with access form information at each time. A control method of a storage unit in a system, wherein a map shape is changed, and an i-bit increasing address that increases according to the logical address map shape is controlled to be generated in a time division after generating the first address.

[0168]

As described in detail above, according to the present invention,
It is possible to provide a storage device, an internal control method of the storage device, a system, and a control method of a storage means in the system, which can efficiently access and reduce current consumption without changing the package.

[Brief description of drawings]

FIG. 1 is a block diagram illustrating an outline of an SDRAM.

FIG. 2 is a schematic configuration diagram of a DRAM core

FIG. 3 is a block diagram illustrating a method of controlling the memory device according to the first embodiment.

FIG. 4 is a block diagram illustrating another control method.

FIG. 5 is a block diagram illustrating another control method.

FIG. 6 is a block diagram illustrating another control method.

FIG. 7 is a waveform diagram showing an internal operation of the memory device of the first embodiment.

FIG. 8 is a block diagram illustrating access control.

FIG. 9 is a block diagram illustrating access control according to page length.

FIG. 10 is a block diagram illustrating a method of controlling the activation circuit.

11 is a block diagram showing another configuration of FIG. 8. FIG.

FIG. 12 is a block diagram illustrating access control according to page length.

FIG. 13 is a circuit diagram showing a specific configuration example of FIG.

FIG. 14 is a circuit diagram showing a specific configuration example of FIG.

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FIG. 15 is a waveform diagram showing the internal operation of FIGS. 13 and 14.

16 is a circuit diagram showing a specific configuration example of FIG.

FIG. 17 is a circuit diagram showing a specific configuration example of FIG.

FIG. 18 is a waveform diagram showing the internal operation of the second embodiment.

FIG. 19 is a block diagram illustrating a method of controlling the cast latency

FIG. 20 is a block diagram illustrating access control according to the third embodiment.

FIG. 21 is a waveform chart showing the internal operation of the third embodiment.

FIG. 22 is a circuit diagram showing a specific configuration example of a predetermined time detection circuit.

FIG. 23 is a waveform chart showing the internal operation of the fourth embodiment.

FIG. 24 is a waveform diagram illustrating a mode setting cycle

FIG. 25 is an explanatory diagram of commands.

FIG. 26 is a waveform diagram illustrating a mode setting cycle.

FIG. 27 is an operation waveform diagram of the program mode setting circuit.

FIG. 28 is an operation waveform diagram of the program mode setting circuit.

FIG. 29 is an operation waveform diagram of the combined entry signal generation circuit.

FIG. 30 is an operation waveform diagram of a mode setting address buffer.

FIG. 31 is an operation waveform diagram of a mode setting address latch.

FIG. 32 is an operation waveform diagram of the mode setting decoder.

FIG. 33 is a block diagram illustrating a conventional method of controlling a memory device.

FIG. 34 is a waveform diagram showing a conventional internal operation

FIG. 35 is a waveform chart showing an internal operation when the conventional page length is changed.

FIG. 36 is a block diagram illustrating conventional access control.

FIG. 37 is a block diagram illustrating a control method for a conventional activation circuit.

[Explanation of symbols]

Row X address (row address) as first address Col Y address (column address) as second address 10 Memory device 21 as memory device 21 Memory cell array

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JP2007200959A *	2007-05-01	2007-08-09	Fujitsu Ltd	Storage device, address control method and system
WO2007116459A1 *	2006-03-30	2007-10-18	Fujitsu Limited	Semiconductor memory and memory system
JP2007310959A *	2006-05-16	2007-11-29	Fujitsu Ltd	Semiconductor memory and operation method of same
JP2008541334A *	2005-05-31	2008-11-20	インテル コーポレイション	Partial page scheme for memory technology

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最終頁に続く

(54)【発明の名称】記憶装置、記憶装置の内部制御方法、システム、及びシステムにおける記憶手段の制御方法

(57)【特許請求の範囲】

【請求項１】

所定数のアドレス端子を用いてＭビットの第１アドレスと該Ｍビットよりも少ないＮビットの第２アドレスとを取り込み、メモリセルがアレイ配列されたメモリセルアレイをアクセスする記憶装置において、

前記メモリセルアレイの論理アドレスマップ形状を、アクセス形態情報に基づいて、前記所定数のアドレス端子よりもｉビット多い（Ｍ＋ｉ）ビットの第１アドレスと前記Ｎビットよりもｉビット少ない（Ｎ－ｉ）ビットの第２アドレスとで表される論理アドレスマップ形状に変更し、該変更に伴い増加した前記ｉビットの第１アドレスを、前記Ｍビットの第１アドレスを発生させた後に時分割で発生させるアドレス制御手段を備え、

前記アドレス制御手段は、前記（Ｎ－ｉ）ビットの第２アドレスに対応する第１リードコマンドの発行から第１データ出力までの第１レイテンシが、前記（Ｎ－ｉ）ビットの第２アドレスに対応する第２リードコマンドの発行から第２データ出力までの第２レイテンシよりも長くなるように、前記増加したｉビットの第１アドレスを取り込むことを特徴とする記憶装置。

【請求項２】

前記アドレス制御手段は、アクティブコマンドの発行後に発行される前記第１リードコマンドに伴って、前記増加したｉビットの第１アドレスを取り込むことを特徴とする請求項１記載の記憶装置。

【請求項３】

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前記第１アドレスはロウアドレスであり、前記第２アドレスはコラムアドレスであることを特徴とする請求項１記載の記憶装置。

【請求項４】

前記第２レイテンシは、モードレジスタに設定されていることを特徴とする請求項１記載の記憶装置。

【請求項５】

前記増加はページ長変化に伴いなされることを特徴とする請求項１記載の記憶装置。

【請求項６】

所定数のアドレス端子を用いてＭビットの第１アドレスと該Ｍビットよりも少ないＮビットの第２アドレスとを取り込み、メモリセルがアレイ配列されたメモリセルアレイをアクセスする記憶装置において、

前記メモリセルアレイの論理アドレスマップ形状が、前記所定数のアドレス端子よりもｉビット多い（Ｍ＋ｉ）ビットの第１アドレスと前記Ｎビットよりもｉビット少ない（Ｎ－ｉ）ビットの第２アドレスとで表される論理アドレスマップ形状に変更されたとき、該論理アドレスマップ形状を変更するアクセス形態情報に基づいて、前記（Ｎ－ｉ）ビットの第２アドレスの取り込み時に不要となる前記ｉビットの第２アドレスを無効化するアドレス無効化手段と、

前記論理アドレスマップ形状の変更に伴い増加した前記ｉビットの第１アドレスを、前記Ｍビットの第１アドレスを発生させた後に時分割で発生させるアドレス制御手段と、を備え、

前記アドレス制御手段は、前記（Ｎ－ｉ）ビットの第２アドレスに対応する第１リードコマンドの発行から第１データ出力までの第１レイテンシが、前記（Ｎ－ｉ）ビットの第２アドレスに対応する第２リードコマンドの発行から第２データ出力までの第２レイテンシよりも長くなるように、前記増加したｉビットの第１アドレスを取り込むことを特徴とする記憶装置。

【請求項７】

所定数のアドレス端子を用いてＭビットの第１アドレスと該Ｍビットよりも少ないＮビットの第２アドレスとを取り込み、メモリセルがアレイ配列されたメモリセルアレイをアクセスする記憶装置における内部制御方法であって、

前記メモリセルアレイの論理アドレスマップ形状を、アクセス形態情報に基づいて、前記所定数のアドレス端子よりもｉビット多い（Ｍ＋ｉ）ビットの第１アドレスと前記Ｎビットよりもｉビット少ない（Ｎ－ｉ）ビットの第２アドレスとで表される論理アドレスマップ形状に変更すること、

前記論理アドレスマップ形状の変更に伴い増加した前記ｉビットの第１アドレスを、前記Ｍビットの第１アドレスを発生させた後に時分割で発生させること、

前記（Ｎ－ｉ）ビットの第２アドレスに対応する第１リードコマンドの発行から第１データ出力までの第１レイテンシが、前記（Ｎ－ｉ）ビットの第２アドレスに対応する第２リードコマンドの発行から第２データ出力までの第２レイテンシよりも長くなるように、前記増加したｉビットの第１アドレスを取り込むこと、

を備えたことを特徴とする記憶装置における内部制御方法。

【請求項８】

所定数のアドレス端子を用いてＭビットの第１アドレスと該Ｍビットよりも少ないＮビットの第２アドレスとを取り込み、メモリセルがアレイ配列されたメモリセルアレイをアクセスする記憶装置における内部制御方法であって、

前記メモリセルアレイの論理アドレスマップ形状を、アクセス形態情報に基づいて、前記所定数のアドレス端子よりもｉビット多い（Ｍ＋ｉ）ビットの第１アドレスと前記Ｎビットよりもｉビット少ない（Ｎ－ｉ）ビットの第２アドレスとで表される論理アドレスマップ形状に変更すること、

前記論理アドレスマップ形状の変更に伴い不要となる前記ｉビットの第２アドレスを無効化すること、

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前記（Ｎ－ｉ）ビットの第２アドレスに対応する第１リードコマンドの発行から第１データ出力までの第１レイテンシが、前記（Ｎ－ｉ）ビットの第２アドレスに対応する第２リードコマンドの発行から第２データ出力までの第２レイテンシよりも長くなるように、前記増加したｉビットの第１アドレスを取り込むこと、
を備えたことを特徴とする記憶装置における内部制御方法。

【請求項９】

所定数のアドレス端子を用いてＭビットの第１アドレスと該Ｍビットよりも少ないＮビットの第２アドレスとを取り込み、メモリセルがアレイ配列されたメモリセルアレイをアクセスする記憶手段を備えたシステムにおいて、

前記記憶手段にアクセス形態情報を供給する制御手段を備え、

前記記憶手段は、前記アクセス形態情報に基づいて、前記メモリセルアレイの論理アドレスマップ形状を前記所定数のアドレス端子よりもｉビット多い（Ｍ＋ｉ）ビットの第１アドレスと前記Ｎビットよりもｉビット少ない（Ｎ－ｉ）ビットの第２アドレスとで表される論理アドレスマップ形状に変更し、該変更に伴い増加した前記ｉビットの第１アドレスを、前記Ｍビットの第１アドレスを発生させた後に時分割で発生させ、前記（Ｎ－ｉ）ビットの第２アドレスに対応する第１リードコマンドの発行から第１データ出力までの第１レイテンシが、前記（Ｎ－ｉ）ビットの第２アドレスに対応する第２リードコマンドの発行から第２データ出力までの第２レイテンシよりも長くなるように、前記増加したｉビットの第１アドレスを取り込むことを特徴とするシステム。

【請求項１０】

前記制御手段は、前記アクセス形態情報を、アドレスとデコーダと制御信号によるコード情報のうちいずれかで行うことを特徴とする請求項９記載のシステム。

【請求項１１】

所定数のアドレス端子を用いてＭビットの第１アドレスと該Ｍビットよりも少ないＮビットの第２アドレスとを取り込み、メモリセルがアレイ配列されたメモリセルアレイをアクセスする記憶手段と、該記憶手段を制御する制御手段とを備えたシステムにおける記憶手段の制御方法であって、

前記制御手段が、前記記憶手段にアクセス形態情報を供給すること、

前記記憶手段が、前記アクセス形態情報に基づいて、前記メモリセルアレイの論理アドレスマップ形状を前記所定数のアドレス端子よりもｉビット多い（Ｍ＋ｉ）ビットの第１アドレスと前記Ｎビットよりもｉビット少ない（Ｎ－ｉ）ビットの第２アドレスとで表される論理アドレスマップ形状に変更し、該変更に伴い増加した前記ｉビットの第１アドレスを、前記Ｍビットの第１アドレスを発生させた後に時分割で発生させ、前記（Ｎ－ｉ）ビットの第２アドレスに対応する第１リードコマンドの発行から第１データ出力までの第１レイテンシが、前記（Ｎ－ｉ）ビットの第２アドレスに対応する第２リードコマンドの発行から第２データ出力までの第２レイテンシよりも長くなるように、前記増加したｉビットの第１アドレスを取り込むこと、
を備えた、システムにおける記憶手段の制御方法。

【発明の詳細な説明】

【０００１】

【発明の属する技術分野】

本発明は、記憶装置、記憶装置の内部制御方法、システム、及びシステムにおける記憶手段の制御方法に関するものである。

【０００２】

近年、データ保持動作が随時必要な半導体メモリ（ダイナミックＲＡＭ:Dynamic RAM）は、顧客（システム側）から要求される記憶容量の増大、アクセス高速化（動作周波数の高周波化）、Ｉ／Ｏバス幅の拡張（１アクセスでデータを扱うビット数幅の増大）などにより、消費電流が増大する傾向にある。これに伴い、メモリデバイスを搭載したシステム機器全体の消費電流も増加する傾向となっており、顧客からメモリデバイスの消費電力削減が求められている。

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【０００３】
また、前述の消費電流の増大は、メモリデバイスのチップ温度上昇を招く場合がある。一般に、ＤＲＡＭセルのデータ保持特性（≒ Refresh特性：TREF）は高温で悪化する（保持時間が短くなる）ので、この理由からも消費電流の削減が求められる。
【０００４】
従って、半導体メモリは、記憶容量の増大やアクセスの高速化、Ｉ／Ｏバス幅の拡張などの性能の向上と、消費電力の削減が同時に求められている。
【０００５】
【従来の技術】
メモリデバイスは、複数のメモリセルがアレイ配置されたメモリセルアレイとセンスアンプを有している。各メモリセルはワード線とビット線に接続され、センスアンプはビット線に接続されている。センスアンプはビット線と対であり、１つのセルの情報（リードデータ）の増幅と保持を行う。
【０００６】
メモリセルアレイは行アドレスによりワード線が展開されるＸ展開方向と、列アドレスによりビット線とセンスアンプが展開されるＹ展開方向とにアレイ展開される。１Ｍビットのメモリ容量であれば、一例としてメモリデバイスの論理アドレスは、１０ビット（2^{10}＝１０２４本のワード線：ＷＬ）のＸアドレス（Row Address ）を、１０ビット（2^{10}＝１０２４本のビット線：ＢＬ（１０２４個のセンスアンプ））のＹアドレス（Column Address）から構成することができる（注：ビット線定義＝一対の相補ビット線）。このとき、仮にワード線とビット線の配線ピッチが同じであれば、論理的なメモリアレイは正方形にイメージされる。
【０００７】
メモリデバイスの内部動作を、システムクロックＣＬＫに対して同期型であるＳＤＲＡＭ（Synchronous ＤＲＡＭ）を例にして説明する。
ＳＤＲＡＭは、制御コマンドとしてメモリデバイスが活性／非活性するためのシステムクロックＣＬＫに同期したアクティブ／プリチャージコマンド（非同期型のメモリデバイスではチップイネーブル信号／ＣＥ（”／”はバーを示す）の立下りと立上り）と、メモリデバイスにデータを入出力する為のリード／ライトコマンドにより動作する。
【０００８】
システムクロックＣＬＫの立上りエッジに於いてアクティブコマンドを外部印加されると、Ｘアドレスを取り込みＸデコーダでデコードして一本のワード線を選択し、それを活性化させる。選択されたワード線に接続されたそれぞれのメモリセルがそれぞれのビット線にデータを出力し、それぞれのセンスアンプがデータを増幅し保持（データのラッチ）する。
【０００９】
その後、システムクロックＣＬＫの立上りエッジに於いて（アクティブコマンドから数ＣＬＫ遅れで）リードコマンドを外部印加されると、Ｙアドレスを取り込みＹデコーダでデコードして一つのセンスアンプの保持されたデータをメモリデバイス外部に出力する。また、ライトコマンドを外部印加されると、Ｙアドレスを取り込みＹデコーダでデコードして（ライトコマンド印加時に入力された）書込みデータを一つのセンスアンプを介してメモリセルに書き込む。その後、更に必要に応じてリード／ライトコマンドを随時行ない、希望のＹアドレスに応じたメモリセルと外部とのアクセスを行なう。
【００１０】
リード／ライトコマンドが終了した後は、システムクロックＣＬＫの立上りエッジに於いて（リード／ライトコマンドから数ＣＬＫ遅れで）プリチャージコマンドを印加して、活性化されたワード線とセンスアンプとビット線をリセット（イコライズ）してメモリアレイは初期状態（次のアクティブコマンドに備える）に戻る。
【００１１】
リセット動作までは内部時間が掛かり、プリチャージコマンドから次のアクティブコマン

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ドを印加するには数ＣＬＫの猶予（待ち）が必要である。同様に、アクティブコマンドからリード／ライトコマンドまで数ＣＬＫの猶予（待ち）が必要である。

【００１２】

尚、ここでは説明の簡素化の為にメモリアレイの入出力ビット数が１の場合で説明したが、入出力のビット数がｎ（ｎＩ／Ｏと記す（ｅｘ．４Ｉ／Ｏ））の場合には、Ｙアドレスによって同時にｎ個のセンスアンプが選択される。そして、各センスアンプはそれぞれｎ個のＩ／Ｏバスを介してそれぞれｎ個のＩ／Ｏポートに接続される。

【００１３】

Ｙアドレスの深さは、ページ長と呼ばれる。メモリデバイスは、１回のアクティブコマンドに応答し、少なくともＩ／Ｏバス幅×ページ長の数のセンスアンプを動作させる。例えば、Ｙアドレスが８ビット（ＹＡ<0:7>）に設定されたＳＤＲＡＭの場合、ページ長は２５６である。このＳＤＲＡＭが３２ビットのＩ／Ｏバス幅を持つ場合、アクティブコマンドに応答して少なくとも８，１９２（＝２５６×３２）個のセンスアンプが動作する。

【００１４】

ＳＤＲＡＭは、随時入力されるリードコマンドによりアクティブコマンドで選択したワード線に接続された複数のメモリセルの情報を複数のセンスアンプにそれぞれラッチする。従って、１本のワード線を活性化すれば、ページ長分のメモリセルの情報を適宜外部に読み出すことができる。詳述すると、随時入力されるリード／ライトコマンド毎に該コマンドと同時に入力されるＹアドレスによりＹデコーダで随時センスアンプを選択することで、任意のＹアドレスのメモリセルから情報を読み出す。即ち、Ｘアドレスは固定したままＹアドレスをランダムにアクセスすることができる。このような動作をＹアドレス優先動作と呼ぶ。尚、ライトコマンドに対しても同様に任意のＹアドレスのメモリセルに情報を書き込むことができる。

【００１５】

このＹアドレス優先動作では、ランダムアクセスの優位性に加えて、一回のアクティブコマンドにより動作するセンスアンプ群のそれぞれのセンスアンプにラッチした複数のデータを効率的に利用することができる。つまり、一回のワード線の充放電電流と一回の（複数）センスアンプによる（複数）ビット線充放電電流により、２５６ページに含まれるメモリセルに対してランダムなアクセスが可能となる。

【００１６】

故に、１回のアクセスに要する消費電流は、同じ時に活性化されるページ内へのアクセス回数でワード線の充放電とビット線の充放電による消費電流を割った値となる。従って、同時に活性化されるページ内のアクセス回数が多いほど、ＳＤＲＡＭのアクセス回数あたりの消費電流は少なくなる。

【００１７】

更に、Ｙアドレス優先動作では、アクティブコマンドからリード／ライトコマンドを印加するまでに必要なクロック数と、プリチャージコマンドから次のアクティブコマンドを印加するまでに必要なクロック数は、動作全体に占める割合が少ない。従って、入出力バスをデータが占有する割合（データ占有率）が高く、システムにおいてＩ／Ｏバスの効率がよい。これらは、システムクロックの周波数が高くなる（高周波になる）ほど、レイテンシを大きくとらなければならないＳＤＲＡＭでは入出力バスのデータ占有率が高くできるという効果がある。

【００１８】

【発明が解決しようとする課題】

ところで、ＳＤＲＡＭを使用する顧客のシステムによっては、アクセスするビット長が少ない（例えば連続した４ビット、８ビットなど）ものがある。このようなシステムによるＳＤＲＡＭのアクセスは、１回のアクティブコマンドからプリチャージコマンドの間に、ページ長より少ない数のリード／ライト動作しかせず、次のアクティブコマンドによりＸアドレスが変更される。このような動作を、便宜的にＸアドレス優先動作と呼ぶ。この動作では、１回のアクティブコマンドにより活性化されるセンスアンプが効率的に使用され

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ていない。

【００１９】

例えば、Ｙアドレスを変更（Ｘアドレスは一定）して４つのメモリセルに対してアクセスする。この場合、Ｘアドレスにより選択される１本のワード線の充放電電流と、活性化するセンスアンプの数（８１９２個）（センスアンプによるビット線の充放電電流を含む）に対応する電流を消費する。このときの消費電流をＰ（ｙ）とする。従って１つのメモリセルに対するアクセスの消費電流は、Ｐ（ｙ）／４となる。

【００２０】

一方、Ｘアドレスを変更（Ｙアドレスは任意）して４つのメモリセルをアクセスする場合、Ｘアドレスを変更する毎にアクティブコマンドとプリチャージコマンドを必要とする。従って、このアクセス方法の場合、Ｘアドレスを固定してアクセスするときの４倍（４×Ｐ（ｙ））の消費電流となり、１つのメモリセルに対するアクセスの消費電流はＰ（ｙ）となる。

【００２１】

従って、Ｘアドレス優先動作を多用するシステムやアプリケーションの場合、Ｙアドレスが浅く（ページ数が少なく）Ｘアドレスが深いメモリデバイスが有効である。

【００２２】

しかし、メモリデバイスを使用するシステムのアクセス方法、アプリケーションのステップによりＸアドレス優先動作とＹアドレス優先動作が混在する場合がある。このような場合、Ｙアドレスが浅いメモリデバイスを使用すると、アクセスの順序によってアクセス速度が極めて遅くなる場合があり、速度向上の妨げとなる。一方、Ｘアドレスが浅いメモリデバイスを使用すると、消費電流低減の妨げとなる。

【００２３】

また、このようなＸアドレス、Ｙアドレスの深さが異なるメモリデバイスは標準品とピン配列やパッケージの大きさが異なり、メモリデバイスを単純に置き換えすることができない。このため、メモリデバイスを実装する基板等を作成しなおさなければならずコストの増加や開発期間の長期化を招いていた。

【００２４】

更に、Ｘアドレス優先動作のような消費電流の大きい動作を繰り返すと、メモリデバイスのチップの温度（ジャンクション温度）を上昇させることがある。この場合、温度上昇によってデータ保持特性が悪化し、データ保持動作であるリフレッシュ動作を頻繁に行なわなければならなくなる。すると、メモリデバイスへのアクセスによる温度上昇にメモリデバイスのリフレッシュ動作による自己発熱を加えたチップ温度となり、データ保持特性の悪化と頻繁なリフレッシュ動作による消費電流の更なる増大を招く。また、データ保持動作を顧客システム側の制御に関係なく非同期で行なう場合（セルフリフレッシュ動作）には、これらリフレッシュ動作における外部からのアクセスに応答しないビジー状態が増加することになり、システムのパフォーマンスが低下（Ｉ／Ｏバスのデータ占有率の低下）する。

【００２５】

本発明は上記問題点を解決するためになされたものであって、その目的はパッケージを変更することなく効率的なアクセスと消費電流の低減を図ることのできる記憶装置、記憶装置の内部制御方法、システム、及びシステムにおける記憶手段の制御方法を提供することにある。

【００２６】

【課題を解決するための手段】

請求項１に記載の発明によれば、所定数のアドレス端子を用いてＭビットの第１アドレスと該Ｍビットよりも少ないＮビットの第２アドレスとを取り込み、メモリセルがアレイ配列されたメモリセルアレイをアクセスする記憶装置において、前記メモリセルアレイの論理アドレスマップ形状を、アクセス形態情報に基づいて、前記所定数のアドレス端子よりもｉビット多い（Ｍ＋ｉ）ビットの第１アドレスと前記Ｎビットよりもｉビット少ない

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（Ｎ－ｉ）ビットの第２アドレスとで表される論理アドレスマップ形状に変更し、該変更に伴い増加した前記ｉビットの第１アドレスを、前記Ｍビットの第１アドレスを発生させた後に時分割で発生させるアドレス制御手段を備え、前記アドレス制御手段は、前記（Ｎ－ｉ）ビットの第２アドレスに対応する第１リードコマンドの発行から第１データ出力までの第１レイテンシが、前記（Ｎ－ｉ）ビットの第２アドレスに対応する第２リードコマンドの発行から第２データ出力までの第２レイテンシよりも長くなるように、前記増加したｉビットの第１アドレスを取り込む。

請求項２に記載の発明によれば、前記アドレス制御手段は、アクティブコマンドの発行後に発行される前記第１リードコマンドに伴って、前記増加したｉビットの第１アドレスを取り込む。

請求項３に記載の発明によれば、前記第１アドレスはロウアドレスであり、前記第２アドレスはコラムアドレスである。

請求項４に記載の発明によれば、前記第２レイテンシは、モードレジスタに設定されている。

請求項５に記載の発明によれば、前記増加はページ長変化に伴いなされる。

請求項６に記載の発明によれば、所定数のアドレス端子を用いてＭビットの第１アドレスと該Ｍビットよりも少ないＮビットの第２アドレスとを取り込み、メモリセルがアレイ配列されたメモリセルアレイをアクセスする記憶装置において、前記メモリセルアレイの論理アドレスマップ形状が、前記所定数のアドレス端子よりもｉビット多い（Ｍ＋ｉ）ビットの第１アドレスと前記Ｎビットよりもｉビット少ない（Ｎ－ｉ）ビットの第２アドレスとで表される論理アドレスマップ形状に変更されたとき、該論理アドレスマップ形状を変更するアクセス形態情報に基づいて、前記（Ｎ－ｉ）ビットの第２アドレスの取り込み時に不要となる前記ｉビットの第２アドレスを無効化するアドレス無効化手段と、前記論理アドレスマップ形状の変更に伴い増加した前記ｉビットの第１アドレスを、前記Ｍビットの第１アドレスを発生させた後に時分割で発生させるアドレス制御手段と、を備え、前記アドレス制御手段は、前記（Ｎ－ｉ）ビットの第２アドレスに対応する第１リードコマンドの発行から第１データ出力までの第１レイテンシが、前記（Ｎ－ｉ）ビットの第２アドレスに対応する第２リードコマンドの発行から第２データ出力までの第２レイテンシよりも長くなるように、前記増加したｉビットの第１アドレスを取り込む。

請求項７に記載の発明によれば、所定数のアドレス端子を用いてＭビットの第１アドレスと該Ｍビットよりも少ないＮビットの第２アドレスとを取り込み、メモリセルがアレイ配列されたメモリセルアレイをアクセスする記憶装置における内部制御方法であって、前記メモリセルアレイの論理アドレスマップ形状を、アクセス形態情報に基づいて、前記所定数のアドレス端子よりもｉビット多い（Ｍ＋ｉ）ビットの第１アドレスと前記Ｎビットよりもｉビット少ない（Ｎ－ｉ）ビットの第２アドレスとで表される論理アドレスマップ形状に変更すること、前記論理アドレスマップ形状の変更に伴い増加した前記ｉビットの第１アドレスを、前記Ｍビットの第１アドレスを発生させた後に時分割で発生させること、前記（Ｎ－ｉ）ビットの第２アドレスに対応する第１リードコマンドの発行から第１データ出力までの第１レイテンシが、前記（Ｎ－ｉ）ビットの第２アドレスに対応する第２リードコマンドの発行から第２データ出力までの第２レイテンシよりも長くなるように、前記増加したｉビットの第１アドレスを取り込むこと、を備えた。

請求項８に記載の発明によれば、所定数のアドレス端子を用いてＭビットの第１アドレスと該Ｍビットよりも少ないＮビットの第２アドレスとを取り込み、メモリセルがアレイ配列されたメモリセルアレイをアクセスする記憶装置における内部制御方法であって、前記メモリセルアレイの論理アドレスマップ形状を、アクセス形態情報に基づいて、前記所定数のアドレス端子よりもｉビット多い（Ｍ＋ｉ）ビットの第１アドレスと前記Ｎビットよりもｉビット少ない（Ｎ－ｉ）ビットの第２アドレスとで表される論理アドレスマップ形状に変更すること、前記論理アドレスマップ形状の変更に伴い不要となる前記ｉビットの第２アドレスを無効化すること、前記（Ｎ－ｉ）ビットの第２アドレスに対応する第１リードコマンドの発行から第１データ出力までの第１レイテンシが、前記（Ｎ－ｉ）ビッ

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トの第２アドレスに対応する第２リードコマンドの発行から第２データ出力までの第２レイテンシよりも長くなるように、前記増加したｉビットの第１アドレスを取り込むこと、を備えた。

請求項９に記載の発明によれば、所定数のアドレス端子を用いてＭビットの第１アドレスと該Ｍビットよりも少ないＮビットの第２アドレスとを取り込み、メモリセルがアレイ配列されたメモリセルアレイをアクセスする記憶手段を備えたシステムにおいて、前記記憶手段にアクセス形態情報を供給する制御手段を備え、前記記憶手段は、前記アクセス形態情報に基づいて、前記メモリセルアレイの論理アドレスマップ形状を前記所定数のアドレス端子よりもｉビット多い（Ｍ＋ｉ）ビットの第１アドレスと前記Ｎビットよりもｉビット少ない（Ｎ－ｉ）ビットの第２アドレスとで表される論理アドレスマップ形状に変更し、該変更に伴い増加した前記ｉビットの第１アドレスを、前記Ｍビットの第１アドレスを発生させた後に時分割で発生させ、前記（Ｎ－ｉ）ビットの第２アドレスに対応する第１リードコマンドの発行から第１データ出力までの第１レイテンシが、前記（Ｎ－ｉ）ビットの第２アドレスに対応する第２リードコマンドの発行から第２データ出力までの第２レイテンシよりも長くなるように、前記増加したｉビットの第１アドレスを取り込む。

【００２９】

請求項１０に記載の発明によれば、請求項９に記載の発明の作用に加えて、制御手段は、アクセス形態情報を、アドレスとデコーダと制御信号によるコード情報のうちいずれかで行う。

請求項１１に記載の発明によれば、所定数のアドレス端子を用いてＭビットの第１アドレスと該Ｍビットよりも少ないＮビットの第２アドレスとを取り込み、メモリセルがアレイ配列されたメモリセルアレイをアクセスする記憶手段と、該記憶手段を制御する制御手段とを備えたシステムにおける記憶手段の制御方法であって、前記制御手段が、前記記憶手段にアクセス形態情報を供給すること、前記記憶手段が、前記アクセス形態情報に基づいて、前記メモリセルアレイの論理アドレスマップ形状を前記所定数のアドレス端子よりもｉビット多い（Ｍ＋ｉ）ビットの第１アドレスと前記Ｎビットよりもｉビット少ない（Ｎ－ｉ）ビットの第２アドレスとで表される論理アドレスマップ形状に変更し、該変更に伴い増加した前記ｉビットの第１アドレスを、前記Ｍビットの第１アドレスを発生させた後に時分割で発生させ、前記（Ｎ－ｉ）ビットの第２アドレスに対応する第１リードコマンドの発行から第１データ出力までの第１レイテンシが、前記（Ｎ－ｉ）ビットの第２アドレスに対応する第２リードコマンドの発行から第２データ出力までの第２レイテンシよりも長くなるように、前記増加したｉビットの第１アドレスを取り込むこと、を備えた。

【００３０】

【発明の実施の形態】

（第一実施形態）

以下、本発明を具体化した第一実施形態を説明する。

【００３１】

図１は、メモリデバイス（ＳＤＲＡＭ）１０の概略を説明するためのブロック図である。メモリデバイス１０は、ＣＰＵ（図示略）に接続され、該ＣＰＵは、アクセス開始前の１回又は随時アクセス形態情報をメモリデバイス１０に与える。メモリデバイス１０は、アクセス形態情報に従って論理アドレスマップ形状を変更する機能を持つ。詳述すると、メモリデバイス１０は、外部（ＣＰＵ）より印加されるアクセス形態情報に応答して論理アドレスマップ形状を変更する。従って、ＣＰＵは、メモリデバイス１０の論理アドレスマップ形状を制御するメモリコントローラとして機能する。

【００３２】

論理アドレスマップ形状は、ＸアドレスとＹアドレスの深さにより決定される。メモリセルアレイの容量は一定である。従って、メモリデバイス１０は、Ｘアドレスの深さとＹアドレスの深さを相補的に変更する。

【００３３】

メモリデバイス１０は、複数の論理アドレスマップ形状により、Ｘアドレスの最大値とＹ

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アドレスの最大値をそれぞれ指定するために必要なビット数のアドレス信号を外部アドレス端子から入力する。そして、このメモリデバイス１０は、実質的に同じメモリ容量を持つ規格化されたメモリデバイスと同じ外形形状を有している。

【００３４】

例えば、６４Ｍビットの容量を持つメモリデバイス（３２Ｉ／Ｏ，４バンク構成）は、一般的（標準規格）に、各バンクに１Ｉ／Ｏについて０．５ＭＢのメモリセルを持つ。各バンクは２ビットのバンクアドレスにより選択される。各バンクのメモリセルは、１１ビットのロウアドレス（Ｘアドレス）により選択される複数（２０４８本）のワード線と、８ビットのコラムアドレス（Ｙアドレス）により選択される複数（２５６本）のビット線によりアレイ配列されている。そして、ＳＤＲＡＭ等のメモリデバイスは、アドレスマルチプレクス方式によりＸアドレスとＹアドレスを取り込むように構成されている。従って、一般的なメモリデバイスは、１３本のアドレスピンを備え、それらから１３ビットのＸアドレス（うち２ビットのバンクアドレス）と、Ｙアドレスを時分割で取り込む。

【００３５】

次に、メモリデバイス１０の機能構成を説明する。

メモリデバイス１０は、クロックバッファ１１、コマンドデコーダ１２、アドレスバッファ１３、入出力バッファ１４、制御信号ラッチ１５、モードレジスタ１６、アドレス発生回路１７、書き込み・読み出し（Ｉ／Ｏ）制御回路１８及びＤＲＡＭコア１９を有する。

【００３６】

クロックバッファ１１は、クロックイネーブル信号ＣＫＥ及び外部クロック信号ＣＬＫを外部装置から入力し、それらに基づいて生成した内部クロック信号ＣＬＫ１を各回路へ出力する。

【００３７】

コマンドデコーダ１２は、クロックバッファ１１からの内部クロック信号ＣＬＫ１、つまりクロック信号ＣＬＫに応答して、外部装置から外部コマンドＣＯＭを入力する。外部コマンドＣＯＭは、本実施形態では、チップセレクト信号／ＣＳ、コラムアドレスストローブ信号／ＣＡＳ、ライトイネーブル信号／ＷＥ及びロウアドレスストローブ信号／ＲＡＳから構成されている。そして、コマンドデコーダ１２は、内部クロック信号ＣＬＫ１に応答して、その時に外部コマンドＣＯＭ、即ち、各信号／ＣＡＳ，／ＷＥ，／ＣＳ，／ＲＡＳの状態（Ｈレベル又はＬレベル）からライトコマンド、リードコマンド、リフレッシュコマンド等の各種のコマンドをデコードする。そして、コマンドデコーダ１２は外部コマンドＣＯＭからこれらデコードした各種コマンドを内部コマンド及びイネーブル信号等としてアドレスバッファ１３、入出力バッファ１４、制御信号ラッチ１５、モードレジスタ１６及びＩ／Ｏ制御回路１８に出力する。

【００３８】

アドレスバッファ１３は、バッファ機能及びラッチ機能を有し、コマンドデコーダ１２からの内部コマンドに基づいて外部装置からアドレス信号Ａ０～Ａ１０とバンクアドレス信号ＢＡ０，ＢＡ１を入力する。アドレスバッファ１３は、入力したアドレス信号Ａ０～Ａ１０及びバンクアドレス信号ＢＡ０，ＢＡ１を増幅し、それらに基づくアドレスデータをラッチするとともに制御信号ラッチ１５、モードレジスタ１６及びアドレス発生回路１７に出力する。

【００３９】

入出力バッファ１４は、コマンドデコーダ１２からのイネーブル信号に基づいて活性化され、外部装置からライトデータＤＱ０～ＤＱ３１、マスク制御信号ＤＱＭを入力する。入出力バッファ１４は、内部クロック信号ＣＬＫ１に応答してライトデータＤＱ０～ＤＱ３１をＩ／Ｏ制御回路１８に出力する。また、入出力バッファ１４は、内部クロック信号ＣＬＫ１に応答してＩ／Ｏ制御回路１８からのリードデータＤＱ０～ＤＱ３１を外部装置に出力する。また、入出力バッファ１４は、マスク制御信号ＤＱＭに応答してライトデータＤＱ０～ＤＱ３１をマスクする。

【００４０】

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制御信号ラッチ１５は、コマンドデコーダ１２からの内部コマンド及びアドレスバッファ１３からのアドレスデータを入力する。そして、制御信号ラッチ１５は、これら内部コマンド及びアドレスデータに基づいてＤＲＡＭコア１９に対してライトデータの書き込み、リードデータの読み出し、リフレッシュ、セルフリフレッシュ等の各種の処理動作のための制御信号を出力する。

【００４１】

モードレジスタ１６は、コマンドデコーダ１２からの内部コマンド（モードレジスタセットコマンド）及びアドレスバッファ１３からのアドレスデータを入力する。そして、モードレジスタ１６は、これら内部コマンド及びアドレスデータに基づいてＤＲＡＭコア１９に対して行う各種の処理動作のモードを保持する。そして、モードレジスタ１６は、保持したモードの情報に基づく制御信号を出力する。

【００４２】

モードレジスタ１６が保持するモードの情報には、アクセス形態情報が含まれる。アクセス形態情報は、ＤＲＡＭコア１９の論理アドレスマップ形状を示す情報である。モードレジスタ１６は、そのアクセス形態情報に基づいて生成したアドレス構成選択信号をアドレス発生回路１７に出力する。

【００４３】

アドレス発生回路１７は、アドレスバッファ１３からアドレス信号Ａ０～Ａ１０に基づくアドレスデータを入力する。そして、アドレス発生回路１７は、モードレジスタ１６のモードとアドレス構成選択信号に基づいて、その時々のＤＲＡＭコア１９の論理アドレスマップ形状に対応して生成したロウアドレスデータとコラムアドレスデータをＤＲＡＭコア１９に出力する。アドレス発生回路１７は、モードレジスタ１６に設定されたバースト長に基づいて入力アドレスからインクリメントしたコラムアドレスを自動生成する機能を有する。

【００４４】

Ｉ／Ｏ制御回路１８は、コマンドデコーダ１２からの内部コマンドに基づいて、入力又は出力制御する。Ｉ／Ｏ制御回路１８は、入出力バッファ１４からのライトデータ（３２ビット）をＤＲＡＭコア１９に出力し、ＤＲＡＭコア１９からのリードデータ（３２ビット）を入出力バッファ１４に出力する。

【００４５】

ＤＲＡＭコア１９は、複数（本実施形態では４つ）のバンクから構成され、各バンクには、制御信号ラッチ１５からの制御信号、アドレス発生回路１７からのロウアドレスデータとコラムアドレスデータをそれぞれ入力する。即ち、アドレスバッファ１３にはＤＲＡＭコアのバンクの数に対応するバンクアドレス信号ＢＡ０，ＢＡ１が入力され、制御信号ラッチ１５及びアドレス発生回路１７は、各バンク毎に設けられている。

【００４６】

ＤＲＡＭコア１９は、制御信号及びアドレスデータに基づいて内蔵したメモリセルアレイに対してライトデータの書き込み、リードデータの読み出し、リフレッシュ、セルフリフレッシュ等の各種の処理動作を実行する。従って、ＤＲＡＭコア１９は、入出力バッファ１４から入力されたライトデータＤＱ０～ＤＱ３１を制御信号及びアドレスデータに基づいて所定のアドレスのメモリセルに書き込む。

【００４７】

図２は、ＤＲＡＭコア１９の概略構成図である。尚、説明の簡素化のため、ここではＤＲＡＭコア１９を構成する１つのバンクについて説明する。

ＤＲＡＭコア１９の各バンクはメモリセルアレイ２１を含み、メモリセルアレイ２１は、複数のメモリセルがアレイ配置されて構成されている。各メモリセルは、ワード線ＷＬとビット線（図示略）に接続され、ビット線はセンスアンプＳ／Ａに接続されている。センスアンプＳ／Ａにはコラム選択線ＣＬが接続されている。即ち、メモリセルアレイ２１は、Ｘアドレス（ロウアドレス）によりワード線ＷＬが展開されるＸ展開方向と、Ｙアドレス（コラムアドレス）によりコラム選択線ＣＬとセンスアンプＳ／Ａ（Ｓ／Ａ列）が展開

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されるＹ展開方向とにアレイ展開されている。

【００４８】

メモリセルアレイ２１は、そのＸ展開方向に区画される複数のロウブロック(Row Block)と、Ｙ展開方向に区画される複数のコラムブロック(Column Block)を有する。ここで、ロウブロックは、メモリセルアレイ２１のＸ展開方向に於いて各センスアンプＳ／Ａ（Ｓ／Ａ列）で区画される領域である。また、コラムブロックは、メモリセルアレイ２１のＹ展開方向に於いてワード線ＷＬに接続されるサブワード線ＳＷＬ単位で区画される領域である。

【００４９】

メモリセルアレイ２１は、モードレジスタ１６が保持するアクセス形態情報に応じて論理アドレスマップ形状を変更する機能を有し、この論理アドレスマップ形状は、モードレジスタ１６から出力されるアドレス構成選択信号（本実施形態では、以下、ページ(Page)長指定信号という）によって変更される。

【００５０】

詳述すると、メモリセルアレイ２１は、ページ長指定信号によりＸアドレスとＹアドレスとを可変して論理アドレスマップ形状を変更する。そして、ページ長指定信号によりページ長（Ｙアドレスの深さ）が変更されると、それに応じて活性化されるセンスアンプＳ／Ａの数が変更される。つまり、連続アクセスできるデータ数が変更される。

【００５１】

このように構成されるＤＲＡＭコア１９は、予め定められた本数の外部アドレス端子から入力されたアドレス信号Ａ０～Ａ１０、バンクアドレス信号ＢＡ０～ＢＡ１に基づく所定のＸアドレス、Ｙアドレスのメモリセルに対してデータの書き込み、読み出し等の各種の処理動作を実行する。

【００５２】

尚、外部アドレス端子の本数は、Ｘアドレスの取り込み時に必要とする端子数またはＹアドレスの取り込み時に必要とする端子数のいずれか多い方の端子数に設定されている。詳しくは、ＸアドレスがＭビット、ＹアドレスがＮビットに設定されたメモリデバイス１０において、例えばＭ＞Ｎの場合、外部アドレス端子の本数はＭ本に設定される。即ち、本実施形態のメモリデバイス（ＳＤＲＡＭ）１０では、最大で１３ビットのＸアドレス（ロウアドレス、バンクアドレスを含む）を取り込むための１３本の外部アドレス端子が備えられている。

【００５３】

図３は、メモリデバイス１０の制御方法を説明するブロック図である。

以下の説明では、外部アドレス端子の本数をＭ本とし、ページ長指定信号によりページ長が最大値（以下、フルページ）に設定される場合のＸアドレスをＭビット(XA<0:m>,(ｍ＝Ｍ－１))、ＹアドレスをＮビット(YA<0:n>,(ｎ＝Ｎ－１))とする（ただし、Ｍ＞Ｎ）。尚、同図では、説明の便宜上、アドレスバッファ１３（図１参照）は第１～第３アドレスバッファ１３ａ～１３ｃに機能的に分割した状態で示すが、分割しない状態で構成してもよい。

【００５４】

今、モードレジスタ１６からのページ長指定信号に基づいてフルページより短いページ長が設定され、そのページ長指定信号により増加するＸアドレスがｉビットとする。このとき、Ｙアドレスは、ｉビット減少する。これは、メモリセルアレイ２１の実質的な容量（2^{M+N}）×Ｉ／Ｏ数が変化しないからである。そして、その増加したｉビットのＸアドレスは、Ｙアドレスの取り込み時に不要となる（Ｍ－Ｎ＋ｉ）本の外部アドレス端子のうちのｉ本から取り込まれる。

【００５５】

詳述すると、第１アドレスバッファ１３ａは、コマンドデコーダ１２からの内部コマンド（図中、Row Address 取り込み信号）に基づいてアドレス信号Ａ０～Ａｍを入力する。第１アドレスバッファ１３ａは、入力したアドレス信号Ａ０～Ａｍを増幅し、それらに基づ

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くＸアドレスデータをラッチするとともにアドレス発生回路１７に出力する。

【００５６】

第２アドレスバッファ１３ｂは、コマンドデコーダ１２からの内部コマンド（図中、Column Address取り込み信号）に基づいてアドレス信号Ａ０～Ａ(ｎ－ｉ)を入力する。第２アドレスバッファ１３ｂは、入力したアドレス信号Ａ０～Ａ(ｎ－ｉ)を増幅し、それらに基づくＹアドレスデータをラッチするとともにアドレス発生回路１７に出力する。

【００５７】

第３アドレスバッファ１３ｃは、コマンドデコーダ１２からの内部コマンド（図中、Column Address取り込み信号）に基づいてアドレス信号Ａ(ｎ－ｉ＋１)～Ａｎを入力する。第３アドレスバッファ１３ｂは、入力したアドレス信号Ａ(ｎ－ｉ＋１)～Ａｎを増幅し、それらに基づくＸアドレスデータ又はＹアドレスデータをラッチするとともにアドレス発生回路１７に出力する。

【００５８】

アドレス発生回路１７は、第１～第３デコーダ（図中、各選択回路）１７ａ～１７ｃ、クランプ回路１７ｄ、及びスイッチ回路１７ｅを含む。

第１～第３デコーダ１７ａ～１７ｃは、第１～第３アドレスバッファ１３ａ～１３ｃからのアドレスデータに基づいて、バンク(BANK)、ロウブロック(Row Block)、ワード線ＷＬ、コラムブロック(Column Block)、コラム選択線ＣＬを各デコーダの機能に応じて適宜選択する。クランプ回路１７ｄは、入力した任意のアドレスデータを無効化し、デコードの圧縮率を可変させる。尚、説明の便宜上、本実施形態では、アドレス発生回路１７は第１～第３デコーダ１７ａ～１７ｃに機能的に分割した状態で構成したが、分割しない状態で構成してもよい。

【００５９】

以下、詳述すると、第１デコーダ１７ａは、第１アドレスバッファ１３ａから出力されるＸアドレスデータに基づいてバンク、ロウブロック、及びワード線ＷＬを選択し、それらに対応するＸアドレスをＤＲＡＭコア１９に出力する。

【００６０】

第２デコーダ１７ｂは、第２アドレスバッファ１３ｂから出力されるＹアドレスデータに基づいてコラム選択線ＣＬを選択し、それに対応するＹアドレスをＤＲＡＭコア１９に出力する。

【００６１】

ここで、ページ長指定信号によってフルページよりも短いページ長が指定される場合、そのページ長指定信号によりスイッチ回路１７ｅが所定の接続位置に切り替えられ、第３アドレスバッファ１３ｃが第３デコーダ１７ｃと接続される。

【００６２】

これにより、第３デコーダ１７ｃは、第３アドレスバッファ１３ｃから出力されるＸアドレスデータに基づいてコラムブロック（具体的にはワード線ＷＬ）を選択し、それに対応するＸアドレスをＤＲＡＭコア１９に出力する。つまり、ページ長指定信号により増加したｉビットのＸアドレスは、Ｙアドレスの取り込み時に不要となる（Ｍ－Ｎ＋ｉ）本の外部アドレス端子のうちのｉ本から取り込まれる。また、このときスイッチ回路１７ｅによって第２デコーダ１７ｂがクランプ回路１７ｄに接続される。これにより、クランプ回路１７ｄは、Ｙアドレスの取り込み時において、不要となるＹアドレスを無効化する。

【００６３】

尚、ページ長指定信号によってフルページが指定される場合には、第３アドレスバッファ１３ｃが第２デコーダ１７ｂと接続される。これにより、第２デコーダ１７ｂは、第３アドレスバッファ１３ｃから出力されるＹアドレスデータに基づいてコラム選択線ＣＬを選択し、それに対応するＹアドレスをＤＲＡＭコア１９に出力する。また、このとき、クランプ回路１７ｄは、第３デコーダ１７ｃに接続され、Ｙアドレスの取り込み時において、不要となるＸアドレスを無効化する。

【００６４】

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尚、比較のため、従来のメモリデバイスの制御方法を説明するブロック図を図３３に示す。従来では、Ｘアドレスを取り込むためのアドレスバッファ５１と、Ｙアドレスを取り込むためのアドレスバッファ５２がそれぞれ設けられる。そして、ページ長を短く使用する際には、そのときに増加したＸアドレス又はＹアドレスのビット数に応じて外部アドレス端子の本数（Ｍ又はＮ）を増加させるようにする。

【００６５】

図７は、本実施形態のメモリデバイス１０の内部動作を示す波形図である。尚、ここでは、例として６４Mbit（メガビット）ＳＤＲＡＭ（３２Ｉ／Ｏ）の動作波形図を示す。

【００６６】

今、初期状態において、メモリデバイス１０は、１３ビットのＸアドレス（ロウアドレスRA<0:10>、バンクアドレスBA<0:1>）、８ビットのＹアドレス（コラムアドレスCA<0:7>）よりなる論理アドレスマップ形状を有し、ページ長が２５６（フルページ）に設定されている。

【００６７】

メモリデバイス１０は、モードレジスタセットコマンドＭＲＳに応答して、アドレス信号Ａ０～Ａ１０をアドレスコードＣｏｄｅ(CodeA<0:10>)として取り込むとともに、バンクアドレスＢａｎｋ(BA<0:1>)を取り込む。そして、メモリデバイス１０は、アドレスコードＣｏｄｅ(CodeA<0:10>)に基づいて、ページ長Ｐａｇｅ、キャスレイテンシｔＣＬ、バースト長ＢＬ等の各種設定を行う。

【００６８】

今、キャスレイテンシｔＣＬ＝３、バースト長ＢＬ＝２、ページ長Ｐａｇｅ＝３２に設定される。このとき、メモリデバイス１０は、１６ビットのＸアドレス（ロウアドレスRA<0:13>、バンクアドレスBA<0:1>）、５ビットのＹアドレス（コラムアドレスCA<0:4>）よりなる論理アドレスマップ形状に変更する。即ち、ページ長可変に伴い、ロウアドレスが３ビット分増加する。

【００６９】

メモリデバイス１０は、アクティブコマンドＡＣＴに応答してアドレス信号Ａ０～Ａ１０をロウアドレスＲｏｗ(RA<0:10>)として取り込むとともにバンクアドレスＢａｎｋ(BA<0:1>)を取り込む。尚、バンクアドレスの取り込みは、以降同じであるため省略する。

【００７０】

尚、モードレジスタセットコマンドＭＲＳ入力時に設定したページ長（＝３２）は、このアクティブコマンドＡＣＴ入力時に設定するようにしてもよい。この場合、ページ長を設定するために必要なビット数分取り込むロウアドレスが少なくなる。例えば、ページ長の設定に２ビット必要な場合、メモリデバイス１０は、アドレス信号Ａ０～Ａ８をロウアドレスＲｏｗ(RA<0:8>)として取り込み、アドレス信号Ａ９，Ａ１０を設定情報として取り込む。又は、アクティブコマンドＡＣＴ入力時に使用しない他ピン（ＤＱマスクピンなど）から取り込んでもよい。

【００７１】

次いで、メモリデバイス１０は、アクティブコマンドＡＣＴ入力後の所定クロック後（例えば２クロック後）に入力されるリードコマンドＲＤ１に応答して、アドレス信号Ａ０～Ａ５をコラムアドレスＣｏｌ(CA<0:4>)として、アドレス信号Ａ６～Ａ８をロウアドレスＲｏｗ(RA<11:13>)として取り込む。

【００７２】

つまり、ページ長可変に伴い増加する３ビットのロウアドレスＲｏｗは、リードコマンドＲＤ１の入力時において、コラムアドレスＣｏｌ(CA<0:4>)の取り込み時に不要となる外部アドレス端子から取り込まれる。そして、メモリデバイス１０は、そのロウアドレスＲｏｗ(RA<11:13>)に基づいてコラムブロック、ワード線ＷＬを選択し、その選択したワード線ＷＬ及びそれに対応するセンスアンプＳ／Ａを活性化させる。

【００７３】

尚、アクティブコマンドＡＣＴに応答してアドレス信号Ａ０～Ａ１０をロウアドレスＲｏ

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ｗ(RA<3:13>)として取り込み、リードコマンドＲＤ１に応答してアドレス信号Ａ６～Ａ８をロウアドレスＲｏｗ(RA<0:2>)として取り込む構成としてもよい。また、リードコマンドＲＤ１に応答してアドレス信号Ａ６～Ａ８をロウアドレスＲｏｗの任意のビット位置に取り込む構成としても良い。

【００７４】

メモリデバイス１０は、リードコマンドＲＤ１が発行されると、設定されたキャスレイテンシｔＣＬ（＝３）及びバースト長ＢＬ（＝２）に基づいて、該リードコマンドＲＤ１入力後の３クロック後にリードデータＤ１１，Ｄ１２を順次出力する。

【００７５】

その後、メモリデバイス１０は、リードコマンドＲＤ２，ＲＤ３に順次応答して、コラムアドレスＣｏｌ(CA<0:4>)及びバンクアドレスＢａｎｋ(BA<0:1>)を取り込む。この際、２回目以降のリードコマンドＲＤ２，ＲＤ３では、増加したロウアドレスＲｏｗは取り込まれず、コラムアドレスＣｏｌ(CA<0:4>)及びバンクアドレスＢａｎｋ(BA<0:1>)のみ取り込まれる。

【００７６】

尚、本実施形態では、リードコマンドＲＤ１～ＲＤ３について説明したが、ライトコマンドの場合についても同様である。即ち、アクティブコマンドＡＣＴ入力後の最初のライトコマンドにて、増加したロウアドレスＲｏｗ(RA<11:13>)が取り込まれる。そして、２回目以降のライトコマンドでは、コラムアドレスＣｏｌ(CA<0:4>)及びバンクアドレスＢａｎｋ(BA<0:1>)のみが取り込まれる。

【００７７】

尚、比較のため、従来のメモリデバイスの内部動作を示す波形図を図３４及び図３５に示す。

図３４は、ページ長Ｐａｇｅが２５６（フルページ）に設定される場合の６４Mbit（メガビット）ＳＤＲＡＭの動作波形図である。同図に示すように、モードレジスタセットコマンドＭＲＳ入力後において、メモリデバイスは、アクティブコマンドＡＣＴに応答して、ロウアドレスＲｏｗ(RA<0:10>)を取り込む。次いで、メモリデバイスは、リードコマンドＲＤ１～ＲＤ３に順次応答して、コラムアドレスＣｏｌ(CA<0:7>)を取り込む。

【００７８】

図３５は、ページ長Ｐａｇｅが３２に設定された６４Mbit（メガビット）ＳＤＲＡＭの動作波形図である。同図に示すように、短いページ長（＝３２）を使用する場合には、ロウアドレスＲｏｗが３ビット増加する。即ち、メモリデバイスは、アクティブコマンドＡＣＴに応答してアドレス信号Ａ０～Ａ１０をロウアドレスＲｏｗ(RA<0:10>)として取り込み、アドレス信号Ａ１３～Ａ１５を増加したロウアドレスＲｏｗ(RA<11:13>)として取り込む。従って、従来では、短いページ長（＝３２）に設定されたメモリデバイスは、増加した３ビットのロウアドレスＲｏｗを取り込むための外部アドレス端子数が規格品に比べて増加する。

【００７９】

図８は、図７におけるアクティブコマンドＡＣＴ発行後のアクセス制御を説明するブロック図である。尚、同図において、図３と同様の構成部分には、同一符号を付してその詳細な説明を一部省略する。

【００８０】

コマンドデコーダ１２（図１参照）は、コマンド判定回路（図中、Command 判定回路）１２ａと、コマンド判定回路１２ａから出力される最初の活性化信号を検出するページコマンド１回目検出回路（図中、Page Command１回目検出回路）（以下、コマンド検出回路）１２ｂを含む。尚、本実施形態において、活性化信号は、ワード線ＷＬ及びセンスアンプＳ／Ａを活性化させる信号である。

【００８１】

コマンド判定回路１２ａは、内部クロック信号ＣＬＫ１に応答してデコードした各種コマンドのうち、リードコマンドとライトコマンドを判定し、判定に応じてリード活性化信号

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又はライト活性化信号を出力する。

【００８２】

今、図７に示すリードコマンドＲＤ１入力時においては、コマンド判定回路１２ａは、リード活性化信号を出力する。

第２アドレスバッファ１３ｂ（図中、Address Latch ）は、オア回路３１及び遅延回路３２を介して入力されるリード活性化信号（リードコマンドＲＤ１）に基づいてアドレス信号Ａ０～Ａ４を入力する。そして、第２アドレスバッファ１３ｂは、それらアドレス信号Ａ０～Ａ４に基づくコラムアドレスデータを第２デコーダ１７ｂ（図中、Column Address Decoder）に出力する。

【００８３】

第３アドレスバッファ１３ｃ（図中、Address Latch ）は、オア回路３１を介してコマンド検出回路１２ｂに入力される１回目のリード活性化信号（リードコマンドＲＤ１）により、当該コマンド検出回路１２ｂから出力される検出信号に基づいてアドレス信号Ａ５～Ａ７を入力する。そして、第３アドレスバッファ１３ｃは、それらアドレス信号Ａ５～Ａ７に基づくロウアドレスデータを第３デコーダ１７ｃ（図中、Column Block 選択用 Address Decoder）に出力する。

【００８４】

第２デコーダ１７ｂは、第２アドレスバッファ１３ｂから出力されるコラムアドレスデータに基づいてコラム選択線ＣＬを選択する。

第３デコーダ１７ｃは、第３アドレスバッファ１３ｃから出力されるロウアドレスデータに基づいてコラムブロック、ワード線ＷＬを選択する。これにより、ワード線ＷＬ及びセンスアンプＳ／Ａが活性化される。

【００８５】

このようにして、コマンド検出回路１２ｂは、コマンド判定回路１２ａから出力される１回目のリード活性化信号（リードコマンドＲＤ１）のみを検出し、そのコマンド検出回路１２ｂからの検出信号に基づいて、拡張されたロウアドレスＲｏｗ(RA<11:13>) が第３デコーダ１７ｃに保持される。

【００８６】

そして、２回目のリード活性化信号（図７に示すリードコマンドＲＤ２）ではコマンド検出回路１２ｂから検出信号が出力されない。つまり、２回目以降に発行されるリードコマンドＲＤ２，ＲＤ３では、アドレス信号Ａ５～Ａ７は第３アドレスバッファ１３ｃに取り込まれない。

【００８７】

尚、図１３及び図１４は、上述した図８の具体的な回路構成の一例を示す回路図である。

又、図１５は、図１３及び図１４に示す回路の内部動作の一例を示す波形図である。

【００８８】

尚、比較のため、従来のアクセス制御を説明するブロック図を図３６に示す。同図は、従来のアクセス制御の原理を説明するものであるので、同様の機能を持つ構成部分については、同一符号を付す。図３６に示すように、従来では、ページ長が２５６であるため、コラムアドレスＣｏｌ(CA<0:4>) とともにコラムアドレスＣｏｌ(CA<5:7>) がリード又はライト活性化信号（即ち、リード又はライトコマンド）の出力毎に取り込まれる。

【００８９】

図９は、図８にて説明したアクセス制御をページ長に応じて行う場合について説明するブロック図である。

この構成では、ページ長指定信号に基づいて各スイッチ回路３３ａ，３３ｂの接続位置を切替えることで、第２及び第３アドレスバッファ１３ｂ，１３ｃにてラッチするアドレス信号をページ長に応じて適宜変更することができる。これにより、第２及び第３デコーダ１７ｂ，１７ｃは、ページ長に応じたその時々のＤＲＡＭコア１９の論理アドレスマップ形状に対応して生成したロウアドレスとコラムアドレスをＤＲＡＭコア１９に出力する。

【００９０】

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図１０は、ワード線ＷＬ及びセンスアンプＳ／Ａの活性化制御を説明する概略ブロック図である。
同図に示すように、ワード線活性化回路４１及びセンスアンプ活性化回路４２は、ページ長指定信号に応じて入力されるコマンド判定回路１２ａ又はコマンド検出回路１２ｂのいずれかの出力信号に応答してワード線ＷＬ、センスアンプＳ／Ａをそれぞれ活性化させる。
【００９１】
詳しくは、ページ長指定信号によりページ長Ｐａｇｅがフルページに設定される場合、各活性化回路４１，４２は、コマンド判定回路１２ａからのアクティブ信号（アクティブコマンド）に応答してワード線ＷＬ、センスアンプＳ／Ａをそれぞれ活性化させる。これは、アクティブコマンドの受け付け時にワード線ＷＬ及びセンスアンプＳ／Ａを選択するために必要なロウアドレスの全てのビットがそろうからである。
【００９２】
一方、ページ長指定信号によりページ長Ｐａｇｅがフルページよりも短いページ長に設定される場合、各活性化回路４１，４２は、検出回路１２ａからの検出信号、つまりリード又はライト活性化信号（リード又はライトコマンド）に応答してワード線ＷＬ、センスアンプＳ／Ａをそれぞれ活性化させる。これは、活性化するワード線ＷＬ及びセンスアンプＳ／Ａを選択するために、アクティブコマンドにより受け付けるロウアドレスと、ページコマンドにより受け付けるロウアドレスとが必要となるからである。
【００９３】
尚、比較のため、従来の活性化回路の制御方法を説明するブロック図を図３７に示す。同図は、従来の活性化制御の原理を説明するものであるので、同様の機能を持つ構成部分については、同一符号を付す。図３７に示すように、従来では、各活性化回路４１，４２は、コマンド判定回路１２ａからのアクティブ信号によってのみ、ワード線ＷＬ、センスアンプＳ／Ａをそれぞれ活性化させる。
【００９４】
以上記述したように、本実施形態によれば、以下の効果を奏する。
（１）メモリデバイス１０は、モードレジスタ１６から出力されるページ長指定信号に応じて、ＤＲＡＭコア１９の論理アドレスマップ形状を変更する。そして、ページ長がフルページより短く設定される場合には、それにより増加したロウアドレスＲｏｗが、最初のリードコマンドＲＤ１入力時に取り込まれる。このように、増加するロウアドレスＲｏｗが、その時に使用されていない外部アドレス端子を使用して時分割で取り込まれるため、外部アドレス端子の本数や配列を変更することなくページ長を変更でき、汎用パッケージを使用することができる。従って、開発期間の長期化やコスト増加を抑止することができる。
【００９５】
（２）パッケージを変更することなくページ長を変更することができるため、メモリデバイスを使用する顧客のシステムに応じた効率的なアクセス方法が実現可能となる。
【００９６】
（３）また、パッケージを変更することなく、ページ長を短く使用することができるため、センスアンプＳ／Ａの活性化数を必要最小限まで少なくすることができ、消費電流の低減化を図ることができる。
【００９７】
（第二実施形態）
以下、本発明を具体化した第二実施形態を説明する。
本実施形態は、第一実施形態のメモリデバイス１０を使用して、同様にページ長を２５６から３２に変更する場合に、そのページ長変更に伴い増加するロウアドレスの取り込み方法の他の制御方法を説明するものである。従って、同様な構成部分については、同一名称及び同一符号を付してその詳細な説明を一部省略する。
【００９８】

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図１８は、第二実施形態の内部動作を示す波形図である。
本実施形態では、図１８に示すように、リードコマンドＲＤ１が、アクティブコマンドＡＣＴの１クロック後に入力される。つまり、アクティブコマンドＡＣＴが入力されてから最初のリードコマンドＲＤ１が入力されるまでの時間ｔＲＣＤがｔＲＣＤ＝１に設定され、当該リードコマンドＲＤ１が第一実施形態よりも１クロック早く入力される。（ちなみに、第一実施形態では、ｔＲＣＤ＝２（図７参照）。）
従って、ページ長変更（２５６から３２に変更）に伴い増加するロウアドレスＲｏｗ(RA<11:13>)が第一実施形態よりも１クロック分早く取り込まれ、それによりワード線ＷＬ及びそれに対応するセンスアンプＳ／Ａがほぼ１クロック分早く活性化される。

【００９９】
ところで、一般には、ワード線ＷＬの活性化動作を完全に終了させるために、アクティブコマンドＡＣＴ入力からリードコマンドＲＤ１入力によってアクセス動作が開始されるまでの猶予（待ち）が必要である。この猶予期間は、クロック信号の周波数により異なるが現在使用されている機器の一般的なクロック周波数では通常２クロック必要である。従って、リードコマンドＲＤ１に基づくアクセス動作の開始タイミングを、該リードコマンドＲＤ１入力時から実質的に１クロック分遅らせる必要がある。

【０１００】
一方、キャスレイテンシｔＣＬは、リードコマンドの入力からリードデータの出力までの期間（クロック数）を規定するものである。このため、図１８に示すように、最初のリードコマンドＲＤ１に対応するキャスレイテンシｔＣＬは、予め設定されたキャスレイテンシｔＣＬの値、ｔＣＬ＝３（設定値）からｔＣＬ＝４に変更される。従って、メモリデバイスは、リードコマンドＲＤ１発行後の４クロック後にリードデータＤ１１，Ｄ１２を順次出力する。

【０１０１】
その後、メモリデバイスはリードコマンドＲＤ２，ＲＤ３に応答してコラムアドレスＣｏｌ(CA<0:4>)とバンクアドレスＢａｎｋ(BA<0:1>)を順次取り込み、予め設定されたキャスレイテンシｔＣＬ（ｔＣＬ＝３：設定値）に従ってリードデータを順次出力する。

【０１０２】
この際、前記と同様に、２回目以降のリードコマンドＲＤ２，ＲＤ３では、増加したロウアドレスＲｏｗは取り込まれず、コラムアドレスＣｏｌ(CA<0:4>)とバンクアドレスＢａｎｋ(BA<0:1>)のみ取り込まれる。尚、本実施形態では、リードコマンドＲＤ１～ＲＤ３について説明したが、ライトコマンドの場合についても同様である。

【０１０３】
図１９は、キャスレイテンシｔＣＬの制御方法を説明するブロック図である。本実施形態において、上記コマンドデコーダ１２（図１参照）は、前記コマンド判定回路１２ａ、ページコマンド１回目検出回路１２ｂ、及びキャスレイテンシ(Cas Latency)制御回路１２ｃを含む。

【０１０４】
前記と同様に、コマンド判定回路１２ａは、リードコマンド又はライトコマンドであるか否か判定し、リード活性化信号又はライト活性化信号を出力する。コマンド検出回路１２ｂは、コマンド判定回路１２ａから出力される最初のリード活性化信号又はライト活性化信号を検出し、その検出信号をキャスレイテンシ制御回路１２ｃに出力する。

【０１０５】
キャスレイテンシ制御回路１２ｃは、内部クロック信号ＣＬＫ１に応答して予め定められた所定のクロック数で出力制御信号を出力し、内部コマンド（図１８ではリードコマンドＲＤ１～ＲＤ３）が発行されてからその出力データが確定されるまでの時間つまりキャスレイテンシｔＣＬを制御する。

【０１０６】
そして、キャスレイテンシ制御回路１２ｃは、コマンド検出回路１２ｂから検出信号が出力されると、その検出信号に応答してその時のキャスレイテンシｔＣＬの値を変更する。

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尚、具体的には、本実施形態のキャスレイテンシ制御回路１２ｃは、コマンド検出回路１２ｂからの検出信号に応答して、キャスレイテンシｔＣＬの値を予め定められた値（設定値）より１大きくする。

【０１０７】

つまり、図１８において、キャスレイテンシｔＣＬは、モードレジスタセットコマンドＭＲＳによりｔＣＬ＝３（設定値）に設定されている。次に、アクティブコマンドＡＣＴ発行後、最初のリードコマンドＲＤ１が入力されると、キャスレイテンシ制御回路１２ｃには、コマンド検出回路１２ｂから出力される検出信号が入力される。この検出信号に応答してキャスレイテンシ制御回路１２ｃは、キャスレイテンシｔＣＬの値（ｔＣＬ＝３：設定値）をｔＣＬ＝４に変更する。即ち、キャスレイテンシ制御回路１２ｃは、最初のリードコマンドＲＤ１入力時のみｔＣＬ＝４に変更し、２回目以降のリードコマンドＲＤ２，ＲＤ３ではｔＣＬ＝３にする。

【０１０８】

以上記述したように、本実施形態によれば、以下の効果を奏する。

（１）本実施形態では、アクティブコマンドＡＣＴ入力後の最初のリードコマンドＲＤ１が第一実施形態よりも１クロック分早く入力されることで、ページ長可変に伴い増加するロウアドレスＲｏｗが第一実施形態よりも１クロック分早く取り込まれる。従って、ワード線ＷＬ及びセンスアンプＳ／Ａをほぼ１クロック分早く活性化させることができる。その際、キャスレイテンシ制御回路１２ｃによってリードコマンドＲＤ１に対応するキャスレイテンシｔＣＬがｔＣＬ＝４に変更されることで、ワード線ＷＬとセンスアンプＳ／Ａを活性化させてからリードデータを出力するまでの期間が十分に確保される。これにより、ページ長可変時において、リードコマンドＲＤ１に基づくアクセス動作の開始タイミングが遅れることはない。

【０１０９】

（第三実施形態）

以下、本発明を具体化した第三実施形態を説明する。

本実施形態は、第一実施形態のメモリデバイス１０を使用して、同様にページ長を２５６から３２に変更する場合に、そのページ長変更に伴い増加するロウアドレスの取り込み方法の他の制御方法を説明するものである。従って、同様な構成部分については、同一名称及び同一符号を付してその詳細な説明を一部省略する。

【０１１０】

図２０は、第三実施形態のアクセス制御を説明するブロック図である。

本実施形態において、上記コマンドデコーダ１２（図１参照）は、前記コマンド判定回路１２ａ及び所定時間検出回路（以下、時間検出回路）１２ｄを含む。

【０１１１】

検出回路１２ｄには、内部クロック信号ＣＬＫ１と、コマンド判定回路１２ａから出力されるアクティブ(Active)信号及びリード又はライト活性化信号が入力される。

【０１１２】

つまり、コマンド判定回路１２ａは、内部コマンドがアクティブコマンドＡＣＴである場合にアクティブ信号を出力する。時間検出回路１２ｄは、アクティブ信号に応答し、予め定めた所定時間（以下、アドレスレイテンシｔＡＬという）経過後に、増加したロウアドレスを取り込むためのアドレス取込信号を出力する。

【０１１３】

尚、本実施形態において、アドレスレイテンシｔＡＬは、内部クロック信号ＣＬＫ１に基づいて設定され、時間検出回路１２ｄは内部クロック信号ＣＬＫ１に基づく所定クロック数をカウントした後、アドレス取込信号を出力する。そして、このとき時間検出回路１２ｄは、コマンド判定回路１２ａから最初のリード活性化信号又はライト活性化信号が出力されるまで、アドレス取込信号を出力する。

【０１１４】

今、ページ長が３２に設定されるとき、そのページ長指定信号によりスイッチ回路３３が

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図２０に示す接続位置に切替えられる。
第３アドレスバッファ１３ｃは、時間検出回路１２ｄからのアドレス取込信号に基づいて入力したアドレス信号Ａ０～Ａｎを増幅し、それらに基づくロウアドレスデータをラッチして第３デコーダ１７ｃに出力する。そして、第３デコーダ１７ｃは、ロウアドレスデータに対応するコラムブロック（ワード線ＷＬ）を指定するためのロウアドレス(RA<0:n>)をＤＲＡＭコア１９（図１）に出力する。
【０１１５】
ちなみに、図２０に示すように、時間検出回路１２ｄからの検出信号に基づいて取り込まれるロウアドレス（増加したロウアドレス）は、ページ長指定信号に基づいて第２及び第３バッファ１３ｂ，１３ｃのいずれかにて取り込まれる。尚、図２２は、図２０の時間検出回路１２ｄの具体的な回路構成の一例を示す回路図である。
【０１１６】
図２１は、本実施形態の内部動作を示す波形図である。尚、同図では、時間検出回路１２ｄのアドレスレイテンシｔＡＬが、例えばｔＡＬ＝１に設定される場合について説明する。
【０１１７】
図２１に示すように、ページ長可変（２５６から３２に変更）に伴い増加したロウアドレスＲｏｗ(RA<0:4>)は、アクティブコマンドＡＣＴ入力後の１クロック後に、時間検出回路１２ｄからのアドレス取込信号によって取り込まれる。これにより、コラムブロック及びワード線ＷＬが選択され、選択されたワード線ＷＬ及び対応するセンスアンプＳ／Ａが活性化される。
【０１１８】
その後、メモリデバイス１０は、リードコマンドＲＤ１～ＲＤ３に順次応答してコラムアドレスＣｏｌ(CA<0:4>)及びバンクアドレスＢａｎｋ(BA<0:1>)を取り込み、予め設定されたキャスレイテンシ（ｔＣＬ＝３）、バースト長（ＢＬ＝２）に従ってリードデータを順次出力する。この際、前記同様に、各リードコマンドＲＤ１～ＲＤ３において、増加したロウアドレスＲｏｗは取り込まれず、コラムアドレスＣｏｌ(CA<0:4>)及びバンクアドレスＢａｎｋ(BA<0:1>)のみ取り込まれる。尚、本実施形態では、リードコマンドＲＤ１～ＲＤ３について説明したが、ライトコマンドの場合についても同様である。
【０１１９】
以上記述したように、本実施形態によれば、以下の効果を奏する。
（１）コマンドデコーダ１２は、コマンド判定回路１２ａからのアクティブ信号に応答して所定時間（アドレスレイテンシｔＡＬ）経過後にアドレス取込信号を出力する時間検出回路１２ｄを備える。これにより、ページ長可変に伴い増加したロウアドレスＲｏｗは、アクティブコマンドＡＣＴの１クロック後（ｔＡＬ＝１）に取り込まれる。従って、第二実施形態と同様、ワード線ＷＬ及びセンスアンプＳ／Ａをはやく活性化させることができる。また、本実施形態では、増加したロウアドレスＲｏｗがリードコマンドＲＤ１入力よりも早いタイミングで取り込まれるため、その取り込み時において、外部アドレス端子の配列に左右されない。
【０１２０】
（２）アクティブコマンドＡＣＴとリードコマンドＲＤのタイミング、及びそれらの出力時に指定するアドレス信号はページ長（論理アドレスマップ形状）によらない。すなわち、メモリコントローラ（ＣＰＵ）アクティブコマンドＡＣＴとリードコマンドＲＤの間に拡張されるロウアドレスに対応するアドレス信号を出力するだけである。従って、変更が容易であり、手間をかけることなく新たな機能（論理アドレスマップ形状を変更する機能）を利用することができる。
【０１２１】
（第四実施形態）
以下、本発明を具体化した第四実施形態を説明する。
本実施形態は、第三実施形態における時間検出回路１２ｄのアドレスレイテンシｔＡＬが

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、例えばｔＡＬ＝０．５に設定される場合について説明するものである。

【０１２２】

図２３は、第四実施形態の内部動作を示す波形図である。

本実施形態では、図２３に示すように、ページ長変更（２５６から３２に変更）に伴い増加するロウアドレスＲｏｗは、アクティブコマンド入力後の０．５クロック後に、時間検出回路１２ｄからのアドレス取込信号によって取り込まれる。

【０１２３】

つまり、メモリデバイス１０は、アクティブコマンドＡＣＴの入力に基づくクロック信号ＣＬＫの立上がりエッジでロウアドレスＲｏｗ(RA<0:10>)を取り込み、その０．５クロック後におけるクロック信号ＣＬＫの立下がりエッジで増加したロウアドレスＲｏｗ(RA<0:4>)を取り込む。

【０１２４】

このように、本実施形態では、アドレスレイテンシｔＡＬ＝０．５に設定することにより、増加したロウアドレスＲｏｗが第三実施形態よりも０．５クロック分早く取り込まれ、それによりワード線ＷＬ及び対応するセンスアンプＳ／Ａがほぼ０．５クロック分はやく活性化される。

【０１２５】

その後、メモリデバイス１０は、リードコマンドＲＤ１～ＲＤ３に順次応答してコラムアドレスＣｏｌ(CA<0:4>)及びバンクアドレスＢａｎｋ(BA<0:1>)を取り込み、予め設定されたキャスレイテンシ（ｔＣＬ＝３）、バースト長（ＢＬ＝２）に基づいてリードデータを順次出力する。この際、前記同様に、各リードコマンドＲＤ１～ＲＤ３において、増加したロウアドレスＲｏｗは取り込まれず、コラムアドレスＣｏｌ(CA<0:4>)及びバンクアドレスＢａｎｋ(BA<0:1>)のみ取り込まれる。尚、本実施形態では、リードコマンドＲＤ１～ＲＤ３について説明したが、ライトコマンドの場合についても同様である。

【０１２６】

以上記述したように、本実施形態によれば、以下の効果を奏する。

（１）本実施形態では、アドレスレイテンシｔＡＬが、ｔＡＬ＝０．５に設定されるため、ページ長可変に伴い増加したロウアドレスＲｏｗが、アクティブコマンドＡＣＴの０．５クロック後に取り込まれる。従って、ワード線ＷＬ及びセンスアンプＳ／Ａを第三実施形態よりもほぼ０．５クロック分早く活性化させることができる。これにより、ページ長可変時において、リードコマンドＲＤ１に基づくアクセス動作の開始タイミングが遅れることはない。

【０１２７】

尚、上記各実施形態は、以下の態様で実施してもよい。

・上記各実施形態において、メモリセルのビット数、アドレス構成、アドレス構成の切替え種類などは、この例に限定されない。

【０１２８】

・図３において、クランプ回路１７ｄは、アドレス発生回路１７内に設けたが、別途備えるようにしてもよい。

・図３の構成は、図４に示すように変更してもよい。即ち、アドレス信号Ａ(ｎ－ｉ＋１)～Ａｎに基づくＹアドレス、Ｘアドレスを取り込むための専用のアドレスバッファ１３ｆ、１３ｇをそれぞれ設けるようにしてもよい。

【０１２９】

・図３の構成は、図５に示すように変更してもよい。即ち、各アドレスバッファ１３ｈ～１３ｊが、それぞれＸアドレス又はＹアドレスを取り込むためのアドレスバッファを共有するように構成する。そして、それらの出力信号（Ｘアドレスデータ又はＹアドレスデータ）をＸＹ切替え信号によって適宜選択するようにしてもよい。

【０１３０】

・図３の構成は、図６に示すように変更してもよい。即ち、図５と同様に、各アドレスバッファ１３ｋ、１３ｌ、１３ｎが、それぞれＸアドレス又はＹアドレスを取り込むための

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アドレスバッファを共有するように構成し、ページ長可変に伴い増加するアドレス（Ｘアドレス）のみを取り込むためのアドレスバッファ１３ｍを別途設けるようにしてもよい。

【０１３１】

・図８のコマンド判定回路１２ａ、コマンド検出回路１２ｂは、メモリデバイスが非同期型である場合には、クロック信号ＣＬＫ１に依存しない他の構成に代えてもよい。

【０１３２】

・図１０において、センスアンプ（Ｓ／Ａ）活性化回路４２のみ制御する構成としてもよい。

・図８の構成は、図１１に示すように変更してもよい。即ち、第３アドレスバッファ１３ｃは、コマンド判定回路１２ａからのリード／ライト活性化信号（即ちリード／ライトコマンド）毎にアドレス信号Ａ５～Ａ７を毎回取り込む。そして、コマンド検出回路１２ｂからの検出信号に基づいて、第３デコーダ１７ｃが、２回目以降のリード／ライトコマンドでは、第３アドレスバッファ１３ｃからのロウアドレスデータを再ラッチしないようにしてもよい。尚、図１６及び図１７は、図１１の具体的な回路構成の一例を示す回路図である。

【０１３３】

・また、図１２は、図１１の構成によって行うアドレス制御をページ長に応じて行う場合について示す。この構成では、ページ長指定信号によりスイッチ回路３３ａ，３３ｂの接続位置が切替えられることにより、ページ長に応じたその時々のＤＲＡＭコア１９の論理アドレスマップ形状に対応して生成したロウアドレス、コラムアドレスが第２及び第３デコーダ１７ｂ，１７ｃからそれぞれ出力される。

【０１３４】

・第一及び第二実施形態では、ページ長可変に伴い増加したアドレスをアクティブコマンドＡＣＴ入力後の最初のリード／ライトコマンドで取り込まれるＹアドレスと同時に取り込むようにしたが、この例に限定されない。即ち、増加したアドレスを最初のリード／ライトコマンドにて取り込んだ後、当該コマンドの所定クロック後（例えば１クロック後）にＹアドレスが取り込まれるようにしてもよい。

【０１３５】

・第三及び第四実施形態では、時間検出回路１２ｄは、アクティブ信号に応答して所定クロック後に検出信号を出力するようにしたが、非同期型のメモリデバイスに具体化する場合には、内部クロック信号ＣＬＫ１に依らず所定時間（ｔＡＬ）経過後に検出信号を出力する構成としてもよい。

【０１３６】

・第四実施形態のように、アドレスレイテンシｔＡＬ＝０．５にて増加したロウアドレスＲｏｗを取り込む方法を実現するその他の手段として、ダブルデータレート（Double Date Rate，ＤＤＲ）方式を用いて具体化してもよい。即ち、クロック信号ＣＬＫ、／ＣＬＫ（／は、バー）で表現される２つのクロック信号を用いて、クロック信号ＣＬＫの立上りでロウアドレスを取り込み、直後の１８０度位相が異なるクロック信号／ＣＬＫの立上りで増加したロウアドレスを取り込むようにしてもよい。

【０１３７】

・上記各実施形態では、モードレジスタセットコマンドＭＲＳ入力時、又は１種類のアクティブコマンドＡＣＴ入力時にページ長を指定するようにしたが、２種類のアクティブコマンドＡＣＴを用いて、それらアクティブコマンドＡＣＴの入力に基づいてページ長を指定するようにしてもよい。

【０１３８】

・上記各実施形態では、同期型のメモリデバイスに具体化したが、非同期型メモリにて論理アドレスマップ形状を変更可能に構成してもよい。尚、非同期型メモリの概略構成は既に公知であるため図面及び説明を省略する。

【０１３９】

このメモリデバイスは、チップイネーブル信号（／ＣＥ）もしくはロウアドレスストロー

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ブ信号（／ＲＡＳ）の立ち下がりでアドレス信号ＡＤＤをＸアドレス（ロウアドレス）として確定する。次に、メモリデバイスは、リードもしくはライト制御信号等でアドレス信号をＹアドレス（コラムアドレス）として確定し、それらアドレスにて指定されるセルに対してアクセスを行なう。

【０１４０】

論理アドレスマップ形状の変更は、以下のイリーガルエントリー方式（通常外部からのアクセスでは使用しない外部からの制御方法）により行う。

イリーガルエントリー方式は、同期式でのモードレジスタセットコマンドを使用（ＭＲＳ方式）した場合と同様に、メモリデバイス内部のアドレス構成セレクト信号をチップイネーブル信号／ＣＥからのワード線活性化信号よりも早く生成する。これにより、アドレス発生回路もしくはその出力の切換え動作を遅らせることなくアクセス遅延を防止できる。

【０１４１】

イリーガルエントリー方式について詳述する。

図２４はアドレス構成の為のモード設定サイクルを説明する波形図である。

メモリデバイスは、アドレス構成の為のモード設定用の専用端子を備え、その専用端子からアドレス構成の種類毎を決める為の情報に必要な情報を取り込むことで、外部アクセス遅延を防止でき誤動作を防止し通常動作の安全動作を保証できる。

【０１４２】

即ち、メモリデバイスはチップイネーブル信号／ＣＥ１がＨレベルの時に通常動作を行わない。この期間に、専用端子から入力されるプログラムモード信号／ＰＥ(＝アドレス構成設定端子)に応答してアドレス信号ＡＤＤに基づくアドレスコードＣｏｄｅを取り込む。詳しくは、メモリデバイスは、プログラムモード信号／ＰＥの立ち下がりでアドレスコードの入力を活性化し、同信号／ＰＥの立ち上がりでアドレスコード情報をラッチする。

【０１４３】

一方、メモリデバイスは、チップイネーブル信号／ＣＥ１がＬレベルの時、外部アクセスに対応した動作状態となり外部アクセスに対応したアドレス信号ＡＤＤを取り込む。

【０１４４】

尚、図中ｔ１～ｔ５は外部仕様タイミング条件である。

尚、図のタイミングにおいて、プログラムモード信号／ＰＥの立ち下がりで外部専用端子の入力回路を活性化し、アドレス信号に対するデコード動作を開始する。そして、プログラムモード信号／ＰＥの立ち上がりでデコード結果を確定し、前記入力回路を非活性化する。この動作によって、消費電力の低減を図ることができる。

【０１４５】

上記したアドレス構成の為のモード設定サイクルにおいて、プログラムモード信号／ＰＥの論理を反転してもよい。また、アドレスコードはデータ端子（ＤＱやＩ／Ｏピンと呼んでいる）から入力しても良い。

【０１４６】

更に、後述の様に、前記コード方式によるプログラムサイクルを数回繰り返した後に、モードを確定するようにしても良い。

図２５は、コマンドの説明図である。

【０１４７】

このコマンドを利用する場合は、基準クロック(システムクロックＣＬＫやチップイネーブル信号／ＣＥ１)に対して、コマンド認識して外部アクセス動作を行なう仕様方式のメモリデバイスが対象となる。

【０１４８】

よって、チップイネーブル信号／ＣＥ１に対してコマンドで動作しない仕様方式のメモリデバイスでは、前記図７を基本に単にアドレスをアドレス構成の種類毎を決める為の情報として対応し、モード設定の為の回数として利用すればよい。

【０１４９】

コマンド（１）～（６），（８）～（１０）は通常動作にて用いられるコマンドであり、

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コマンド（７），（１１）は通常動作では意味をなさないコマンドである。コマンド（７）は、ライト（ＷＲ）動作であるが信号／ＬＢ，／ＵＢがＨレベルであるためデータを入力しない（マスクされている）。コマンド（１１）は、リード（ＲＤ）動作であるが、同様に信号／ＬＢ，／ＩＢによりマスクされているためデータを出力しない。

【０１５０】

このように、通常動作に用いないコマンド（イリーガルコマンド）をアドレス構成の種類毎を決める為の情報として取り込むことで、専用端子を設けることなく情報の設定を行うことができる。

【０１５１】

図２６は、アドレス構成の為のモード設定サイクルを説明する波形図であり、図２５のコマンド（１１）を複数継続して入力することでアドレス構成の為のモード設定に必要な情報をアドレスコードとして取り込む場合を示す。

【０１５２】

メモリデバイスは、コマンド（１１）に応答してアドレス信号ＡＤＤをアドレスコードＣｏｄｅとして取り込む。この動作をＮ回繰り返す。１回目からＮ回目までコマンド（１１）に対応して取り込んだＮ個のアドレスコードＣｏｄｅが全て一致する場合に、そのアドレスコードＣｏｄｅを有効にしてアドレス構成の為のモード設定を行う。

【０１５３】

尚、コマンド（１１）がＮ？１回一致した場合に、Ｎ回目のコマンド（１１）に対応して取り込んだアドレスコードＣｏｄｅに基づいてアドレス構成の為のモード設定を行うようにしてもよい。また、アドレスコードＣｏｄｅの取り込みを任意のサイクル（例えば１回目）に変更して実施しても良い。他にも種々の応用が展開できる。

【０１５４】

モードを設定するアドレスコードは、アドレス構成の種類数に対応してアドレスＢｉｔ数を確定すればよい。

図２６の様にＮ回のモード設定サイクルの場合、デバイス内部ではカウンタ回路を用いる。Ｎ回のモード設定サイクルのエントリに対してカウンタ回路の上位ビットが変化したら、モードを確定する回路構成となる。

【０１５５】

図２７は、プログラムアドレス構成の為のモード設定回路であるエントリコントロール回路の動作波形図である。

図２７（ａ）に示すように、第１エントリ回路は、３回目のサイクルでＨレベルの第１のアドレスイネーブル信号proaddz を出力し、４回目のサイクルで第１のエントリ信号proentz を出力する。そして、第１エントリ回路は、第１のアドレスイネーブル信号proaddz 及び第１のエントリ信号proentz を同時にリセットする。これによりメモリデバイスは前に確定したアドレス構成の情報を、第１のエントリ信号proentz により４回目のサイクルで取り込んだアドレスコード情報に従った最新のアドレス構成の情報に変更される。

【０１５６】

図２７（ｂ）に示すように、第１エントリ回路は、カウントの途中でその他のコマンド（デバイス活性のアクティブコマンドやリード／ライトコマンド）を受け付けるとカウントをリセットする。その結果、第１のアドレスイネーブル信号proaddz 及びイネーブル信号proaddz をＬレベルに保持する。

【０１５７】

つまりアドレス構成の種類毎を決める為のモード設定において、その為の同じコマンドが連続して規定回数続かなければキャンセルされる。（メモリデバイスは前に確定したアドレス構成の情報を維持する）

図２８は、図２４に対応したプログラムアドレス構成の為のモード設定回路であるエントリコントロール回路（第２エントリ回路）の動作波形図である。

【０１５８】

第２エントリ回路は、Ｌレベルのプログラムモード信号／ＰＥに応答してＨレベルのアド

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レスイネーブル信号peaddzを出力した後、Ｈレベルのプログラムモード信号／ＰＥに応答してＨレベルのイネーブル信号peaddzを出力する。これによりメモリデバイスは前に確定したアドレス構成の情報を、第２のエントリ信号proentz により取り込んだアドレスコード情報に従った最新のアドレス構成の情報に変更される。

【０１５９】

図２９は、エントリ信号生成回路の動作波形図である。

図２９（ａ）に示すように、信号生成回路は、第１のエントリ信号proentz に応答して合成信号entzを出力する。また、図２９（ｂ）に示すように、信号生成回路は、エントリ信号peentzに応答して合成信号entzを出力する。

【０１６０】

図３０は、アドレス構成の為のモード設定用アドレスバッファの動作波形図である。

アドレスバッファは、Ｈレベルのアドレスイネーブル信号peaddzに応答して入力回路を活性化してアドレス信号az<0:3> を出力する。尚、第１のアドレスイネーブル信号proaddzに応答して同様に動作する。

【０１６１】

図３１は、アドレス構成の為のモード設定用アドレスラッチの動作波形図である。

アドレスラッチは、Ｈレベルのアドレスイネーブル信号peaddzに応答して出力されたアドレス信号az<0:3> を合成信号entzに応答してラッチしたコードＣｏｄｅをアドレス構成の為のモード設定用アドレス信号paz<0:3>として出力する。尚、第１のアドレスイネーブル信号proaddz に応答して同様に動作する。

【０１６２】

アドレス構成の為のモード設定用デコーダは、アドレス構成の為のモード設定用アドレス信号paz<0:3>をデコードして数種類のアドレスマップのためのアドレス構成セレクト信号を出力する。

【０１６３】

図３２は、モード設定用デコーダの動作波形図である。

デコーダは、モード設定用アドレス信号paz<0:3>をデコードして数種類のアドレスマップのためのアドレス構成セレクト信号のうちの１つを選択してそれをＨレベルにする。

【０１６４】

・Ｘアドレスの深さ＜Ｙアドレスの深さの場合は、アドレス構成設定端子は、アクティブ時に使用されないアドレス端子にて共用することも可能である。また、アドレス構成を設定するコマンドは、アクティブコマンドの他に、プリチャージコマンドや、別の新規コマンドでも可能である。

【０１６５】

・アドレスマップを変更できる機能は、バンク毎に独立して機能化されている。バンク毎に論理アドレスマップを（変更）設定できる事で、システムのパフォーマンスはさらに向上する。

【０１６６】

・クランプするアドレスビットの位置を適宜変更してもよい。

・無効化するアドレスビットの位置を適宜変更してもよい。

・上記各実施形態では、外部から論理アドレスマップ形状を随時変更可能に構成したが、ボンディングションもしくはＦｕｓｅなどのＲＯＭを備え、出荷時やユーザ使用時に論理アドレスマップ形状を所望の形状に変更し、その形状を維持するようにしてもよい。また、外部から書き換え可能なＲＯＭを備え、必要に応じて論理アドレスマップ形状を変更するようにしてもよい。これらの場合、論理アドレスマップ形状が短期又は長期に亘って固定される。従って、既存のプログラムやＣＰＵを使用することができる。また、行アクセスサイクル毎に論理アドレスマップ形状を変更する手間を省くことができる。

【０１６７】

本実施形態の特徴をまとめると以下のようになる。

（付記１）　Ｍビットの第１アドレスとＮビットの第２アドレスを同時に取り込むアドレ

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ス端子を備えるか、或いはＭビットの第１アドレスとＮビットの第２アドレスのいずれか多い数のアドレス端子を備え、前記第１アドレスと前記第２アドレスにてメモリセルがアレイ配列されたメモリセルアレイをアクセスする記憶装置において、
前記メモリセルアレイの論理アドレスマップ形状を変更するアクセス形態情報に基づいて、前記アドレス端子から入力する外部アドレスの一部を第１アドレス又は第２アドレスに置き換えるアドレス制御手段を備えたことを特徴とする記憶装置。
（付記２）　Ｍビットの第１アドレスとＮビットの第２アドレスを同時に取り込むアドレス端子を備えるか、或いはＭビットの第１アドレスとＮビットの第２アドレスのいずれか多い数のアドレス端子を備え、前記第１アドレスと前記第２アドレスにてメモリセルがアレイ配列されたメモリセルアレイをアクセスする記憶装置において、
前記メモリセルアレイの論理アドレスマップ形状を変更するアクセス形態情報に基づいて、前記アドレス端子から入力する外部アドレス又はその一部を無効化するアドレス無効化手段を備えたことを特徴とする記憶装置。
（付記３）　前記論理アドレスマップ形状の変更に応じて増加するｉビットの増加アドレスを取り込むための制御信号を、前記第１アドレス取り込み後における所定時間経過後に出力する所定時間検出手段を備えたことを特徴とする付記１又は２記載の記憶装置。
（付記４）　前記所定時間検出手段は、前記第１アドレスを取り込むためのアクティブコマンドに応答して、クロック信号の所定クロック後に前記制御信号を出力することを特徴とする付記３記載の記憶装置。
（付記５）　前記論理アドレスマップ形状の変更に応じて増加するｉビットの増加アドレスを取り込むための制御信号を、（Ｎ－ｉ）ビットの第２アドレスの取り込み制御時に発行されるコマンドに基づいて出力するコマンド検出手段を備えたことを特徴とする付記１又は２記載の記憶装置。
（付記６）　前記コマンド検出手段は、前記第１アドレスを取り込むアクティブコマンド後の最初のリード又はライトコマンドを検出し、該リード又はライトコマンドに基づいて前記制御信号を出力することを特徴とする付記５記載の記憶装置。
（付記７）　前記コマンド検出回路からの制御信号に基づいて前記最初のリード又はライトコマンドに対応するキャスレイテンシを遅らせるキャスレイテンシ制御手段を備えたことを特徴とする付記６記載の記憶装置。
（付記８）　前記ｉビットの増加アドレスを取り込むための制御信号に基づいてワード線を活性化させるワード線活性化手段を備えることを特徴とする付記３乃至６のいずれか一記載の記憶装置。
（付記９）　前記ｉビットの増加アドレスを取り込むための制御信号に基づいてセンスアンプを活性化させるセンスアンプ活性化手段を備えることを特徴とする付記３乃至６のいずれか一記載の記憶装置。
（付記１０）　前記アドレス無効化手段は、デコードの圧縮率を可変させるために任意のアドレスをクランプする手段を備えることを特徴とする付記２記載の記憶装置。
（付記１１）　前記アクセス形態情報が印加される制御信号、又は複数の制御信号の組み合わせにより前記論理アドレスマップ形状の設定に応じたアドレス構成選択信号を生成する手段を備え、
前記アドレス制御手段又は前記アドレス無効化手段は、前記アドレス構成選択信号に基づいて前記置き換え又は前記無効化を実行する付記１又は２記載の記憶装置。
（付記１２）　外部アドレスを入力し、前記アドレス構成選択信号に基づいて、その出力信号を、前記第１アドレス方向の選択信号を生成する第１信号生成回路と前記第２アドレス方向の選択信号を生成する第２信号生成回路とに切り替える切替回路を有するアドレス発生回路を備えたことを特徴とする付記１１記載の記憶装置。
（付記１３）　前記アドレス制御手段又は前記アドレス無効化手段は、前記アクセス形態情報を記憶するボンディングション又はＦｕｓｅなどのＲＯＭを備えることを特徴とする付記１又は２記載の記憶装置。
（付記１４）　前記アドレス制御手段又は前記アドレス無効化手段は、前記アクセス形態

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情報を記憶する外部から書き換え可能なＲＯＭを備えることを特徴とする付記１又は２記載の記憶装置。

（付記１５）　Ｍビットの第１アドレスとＮビットの第２アドレスを同時に取り込むアドレス端子を備えるか、或いはＭビットの第１アドレスとＮビットの第２アドレスのいずれか多い数のアドレス端子を備え、前記第１アドレスと前記第２アドレスにてメモリセルがアレイ配列されたメモリセルアレイをアクセスする記憶装置における内部制御方法であって、

前記メモリセルアレイの論理アドレスマップ形状を変更するアクセス形態情報に基づいて、前記アドレス端子から入力する外部アドレスの一部を第１アドレス又は第２アドレスに置き換えることを特徴とする記憶装置における内部制御方法。

（付記１６）　Ｍビットの第１アドレスとＮビットの第２アドレスを同時に取り込むアドレス端子を備えるか、或いはＭビットの第１アドレスとＮビットの第２アドレスのいずれか多い数のアドレス端子を備え、前記第１アドレスと前記第２アドレスにてメモリセルがアレイ配列されたメモリセルアレイをアクセスする記憶装置における内部制御方法であって、

前記メモリセルアレイの論理アドレスマップ形状を変更するアクセス形態情報に基づいて、前記アドレス端子から入力する外部アドレス又はその一部を無効化することを特徴とする記憶装置における内部制御方法。

（付記１７）　前記アクセス形態情報は、スタンバイ期間中もしくはアクティブ動作と同時に設定されることを設定されることを特徴とする付記１５又は１６記載の記憶装置における内部制御方法。

（付記１８）　前記論理アドレスマップ形状に応じてセンスアンプの活性化数を制御することを特徴とする付記１５乃至１７のいずれか一記載の記憶装置における内部制御方法。

（付記１９）　前記論理アドレスマップ形状に応じてデコードの圧縮率を可変させることを特徴とする付記１５乃至１８のいずれか一記載の記憶装置における内部制御方法。

（付記２０）　前記アクセス形態情報が印加される制御信号、又は複数の制御信号の組み合わせにより前記論理アドレスマップ形状の設定に応じたアドレス構成選択信号を生成し、該アドレス構成選択信号に基づいて前記置き換え又は前記無効化を実行することを特徴とする付記１５乃至１８のいずれか一記載の記憶装置における内部制御方法。

（付記２１）　前記第１及び第２アドレスは共通アドレス発生手段にて生成され、該共通アドレス発生手段の出力先を前記アドレス構成選択信号により切り替えることを特徴とする付記２０記載の記憶装置における内部制御方法。

（付記２２）　外部アドレスにより前記第１及び第２アドレスを生成する第１及び第２アドレス発生手段を備え、前記アドレス構成選択信号にて前記外部アドレスの入力先を切り替えることを特徴とする付記２０記載の記憶装置における内部制御方法。

（付記２３）　前記論理アドレスマップ形状の変更に応じて増加するｉビットの増加アドレスを、前記第１アドレスを取り込んだ後に時分割で取り込むことを特徴とする付記１５又は１６記載の記憶装置における内部制御方法。

（付記２４）　クロック信号に同期して前記第１アドレスを取り込んだ後、該クロック信号の所定クロック後に同期して前記ｉビットの増加アドレスを取り込むようにしたアドレスレイテンシ制御であることを特徴とする付記２３記載の記憶装置における内部制御方法。

（付記２５）　前記アドレスレイテンシ制御は、前記ｉビットの増加アドレスを取り込むための制御信号を発生させるべく、前記第１アドレス取り込み後における前記クロック信号の所定クロックの数を予め取り込むためのステップを含むことを特徴とする付記２４記載の記憶装置における内部制御方法。

（付記２６）　前記ステップは、前記第１アドレスを取り込む前又は取り込み時に行われることを特徴とする付記２５記載の記憶装置における内部制御方法。

（付記２７）　前記ステップは、コマンドで行われ、モードレジスタにセットされることを特徴とする付記２５又は２６記載の記憶装置における内部制御方法。

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（付記２８）　前記ステップは、前記第１アドレスを取り込む前にはアドレスコードを含むコマンドで行われ、前記第１アドレスの取り込み時には２種類のアクティブコマンドで行われることを特徴とする付記２５又は２６記載の記憶装置における内部制御方法。
（付記２９）　前記論理アドレスマップ形状の変更に応じて増加するｉビットの増加アドレスを、（Ｎ－ｉ）ビットの第２アドレスの取り込み制御と同時に行うことを特徴とする付記１５又は１６記載の記憶装置における内部制御方法。
（付記３０）　前記論理アドレスマップ形状の変更に応じて増加するｉビットの増加アドレスを、前記Ｎ本のアドレス端子のうち、（Ｎ－ｉ）ビットの第２アドレスの取り込み時に使用されないアドレス端子から取り込むことを特徴とする付記１５又は１６記載の記憶装置における内部制御方法。
（付記３１）　前記論理アドレスマップ形状の変更に応じて増加するｉビットの増加アドレスを、前記第１アドレスを取り込むアクティブコマンド後の次のコマンド時に行われることを特徴とする付記１５又は１６記載の記憶装置における内部制御方法。
（付記３２）　前記ｉビットの増加アドレスを、前記アクティブコマンド後のリード又はライトコマンドと同時に取り込むことを特徴とする付記３１記載の記憶装置における内部制御方法。
（付記３３）　前記アクティブコマンド後の最初のリード又はライトコマンドを検出するコマンド検出手段を備え、前記コマンド検出手段の出力信号に基づいて前記最初のリード又はライトコマンドに対応するキャスレイテンシを遅らせることを特徴とする付記３２記載の記憶装置における内部制御手法。
（付記３４）　前記第１アドレス取り込み後の所定時間経過後に前記ｉビットの増加アドレスを取り込むための信号を出力する所定時間検出手段を備え、前記コマンド検出手段又は前記所定時間検出手段の出力信号に基づいてワード線を活性化させることを特徴とする付記３３記載の記憶装置における内部制御手法。
（付記３５）　前記コマンド検出手段又は前記所定時間検出手段の出力信号に基づいてセンスアンプを活性化させることを特徴とする付記３３又は３４記載の記憶装置における内部制御手法。
（付記３６）　Ｍビットの第１アドレスとＮビットの第２アドレスを同時に取り込むアドレス端子を備えるか、或いはＭビットの第１アドレスとＮビットの第２アドレスのいずれか多い数のアドレス端子を備え、前記第１アドレスと前記第２アドレスにてメモリセルがアレイ配列されたメモリセルアレイをアクセスする記憶手段と、それへのアクセスと制御を行う制御手段を備えたシステムにおいて、前記制御手段は、前記記憶手段に対するその時々のアクセス形態情報を供給し、
前記記憶手段は、前記アクセス形態情報に基づいて変更した前記メモリセルアレイの論理アドレスマップ形状に応じて増加するｉビットの増加アドレスを、前記第１アドレスを発生させた後に時分割で発生させることを特徴とするシステム。
（付記３７）　前記制御手段は、前記アクセス形態情報を、アドレスとデコーダと制御信号によるコード情報のうちいずれかで行うことを特徴とする付記３６記載のシステム。
（付記３８）　前記制御手段は、前記アクセス形態情報の供給を、アクセスの開始と同時又はそれ以前に行うことを特徴とする付記３６又は３７記載のシステム。
（付記３９）　Ｍビットの第１アドレスとＮビットの第２アドレスを同時に取り込むアドレス端子を備えるか、或いはＭビットの第１アドレスとＮビットの第２アドレスのいずれか多い数のアドレス端子を備え、前記第１アドレスと前記第２アドレスにてメモリセルがアレイ配列されたメモリセルアレイをアクセスする記憶手段と、それへのアクセスと制御を行う制御手段を備えたシステムにおける記憶手段の制御方法であって、
前記制御手段は、その時々のアクセス形態情報に応じて前記記憶手段が有するメモリセルアレイの論理アドレスマップ形状を変更し、その論理アドレスマップ形状に応じて増加するｉビットの増加アドレスを、前記第１アドレスを発生させた後に時分割で発生させるよう制御するシステムにおける記憶手段の制御方法。
【０１６８】

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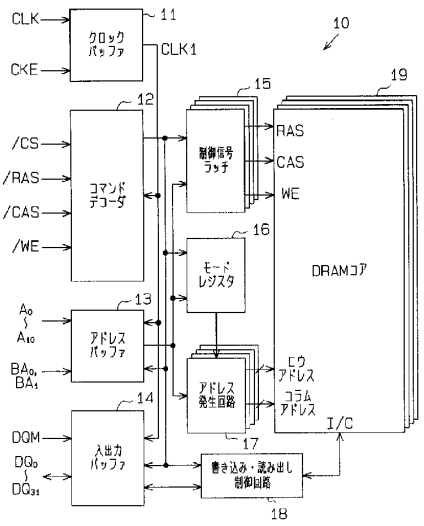
【発明の効果】
以上詳述したように、本発明によれば、パッケージを変更することなく効率的なアクセスと消費電流の低減を図ることのできる記憶装置、記憶装置の内部制御方法、システム、及びシステムにおける記憶手段の制御方法を提供することができる。
【図面の簡単な説明】
【図１】　ＳＤＲＡＭの概略を説明するためのブロック図である。
【図２】　ＤＲＡＭコアの概略構成図である。
【図３】　第一実施形態のメモリデバイスの制御方法を説明するブロック図である。
【図４】　別の制御方法を説明するブロック図である。
【図５】　別の制御方法を説明するブロック図である。
【図６】　別の制御方法を説明するブロック図である。
【図７】　第一実施形態のメモリデバイスの内部動作を示す波形図である。
【図８】　アクセス制御を説明するブロック図である。
【図９】　ページ長に応じたアクセス制御を説明するブロック図である。
【図１０】　活性化回路の制御方法を説明するブロック図である。
【図１１】　図８の別の構成を示すブロック図である。
【図１２】　ページ長に応じたアクセス制御を説明するブロック図である。
【図１３】　図８の具体的な構成例を示す回路図である。
【図１４】　図８の具体的な構成例を示す回路図である。
【図１５】　図１３及び図１４の内部動作を示す波形図である。
【図１６】　図１１の具体的な構成例を示す回路図である。
【図１７】　図１１の具体的な構成例を示す回路図である。
【図１８】　第二実施形態の内部動作を示す波形図である。
【図１９】　キャスレイテンシの制御方法を説明するブロック図である。
【図２０】　第三実施形態のアクセス制御を説明するブロック図である。
【図２１】　第三実施形態の内部動作を示す波形図である。
【図２２】　所定時間検出回路の具体的な構成例を示す回路図である。
【図２３】　第四実施形態の内部動作を示す波形図である。
【図２４】　モード設定サイクルを説明する波形図である。
【図２５】　コマンドの説明図である。
【図２６】　モード設定サイクルを説明する波形図である。
【図２７】　プログラムモード設定回路の動作波形図である。
【図２８】　プログラムモード設定回路の動作波形図である。
【図２９】　合成エントリ信号生成回路の動作波形図である。
【図３０】　モード設定用アドレスバッファの動作波形図である。
【図３１】　モード設定用アドレスラッチの動作波形図である。
【図３２】　モード設定用デコーダの動作波形図である。
【図３３】　従来のメモリデバイスの制御方法を説明するブロック図である。
【図３４】　従来の内部動作を示す波形図である。
【図３５】　従来のページ長可変時の内部動作を示す波形図である。
【図３６】　従来のアクセス制御を説明するブロック図である。
【図３７】　従来の活性化回路の制御方法を説明するブロック図である。
【符号の説明】
Ｒｏｗ　第１アドレスとしてのＸアドレス（ロウアドレス）
Ｃｏｌ　第２アドレスとしてのＹアドレス（コラムアドレス）
１０　記憶装置としてのメモリデバイス
２１　メモリセルアレイ

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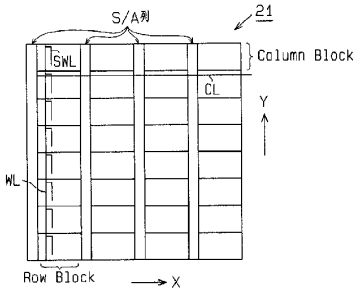
【図１】

SDRAMの概略を説明するためのブロック図



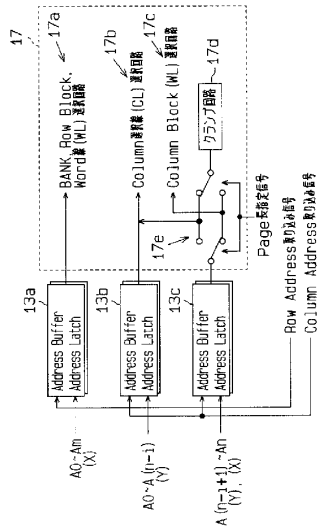
【図２】

DRAMコアの概略構成図



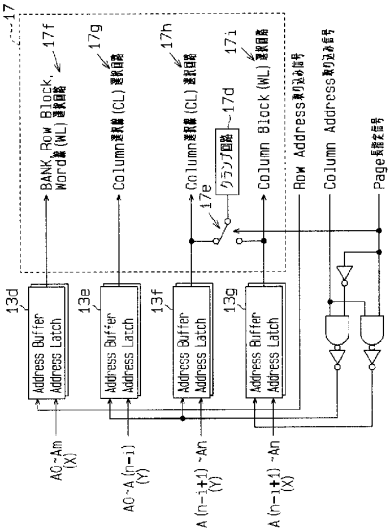
【図３】

第一実施形態のメモリデバイスの制御方法を説明するブロック図



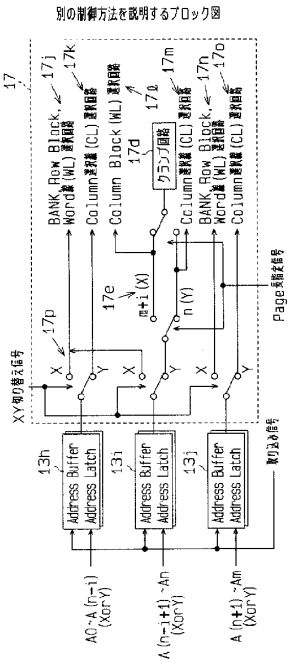
【図４】

別の制御方法を説明するブロック図

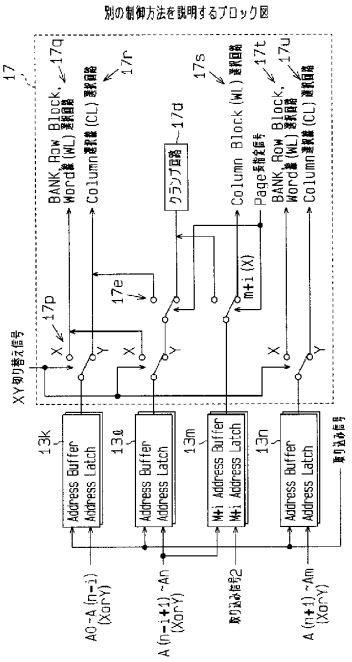


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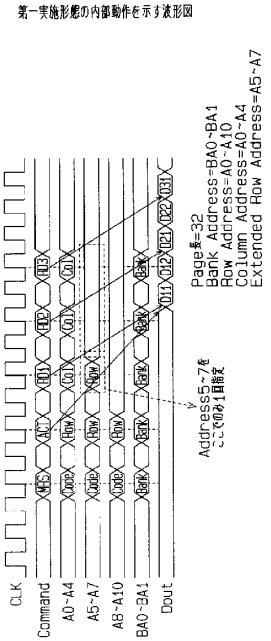
【図５】



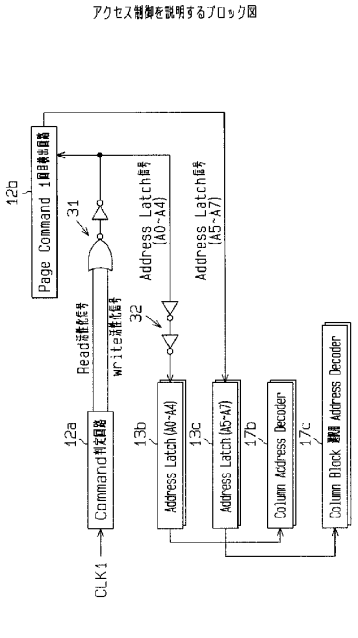
【図６】



【図７】

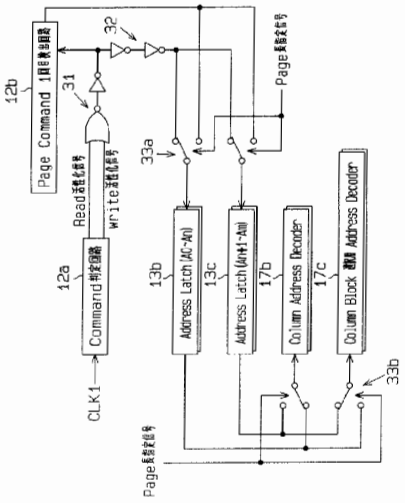


【図８】



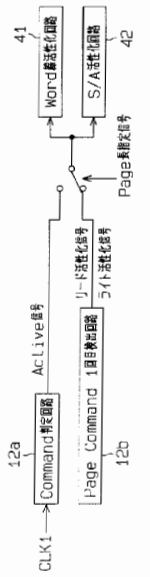
【図９】

ページ長に応じたアクセス制御を説明するブロック図



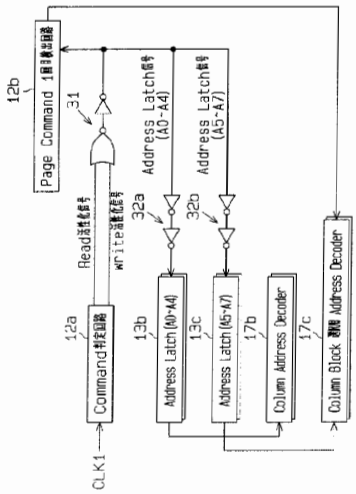
【図１０】

活性化回路の制御方法を説明するブロック図



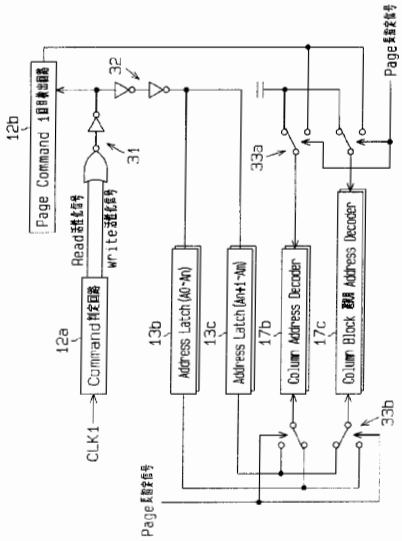
【図１１】

第８の別の構成を示すブロック図



【図１２】

ページ長に応じたアクセス制御を説明するブロック図



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【図１３】

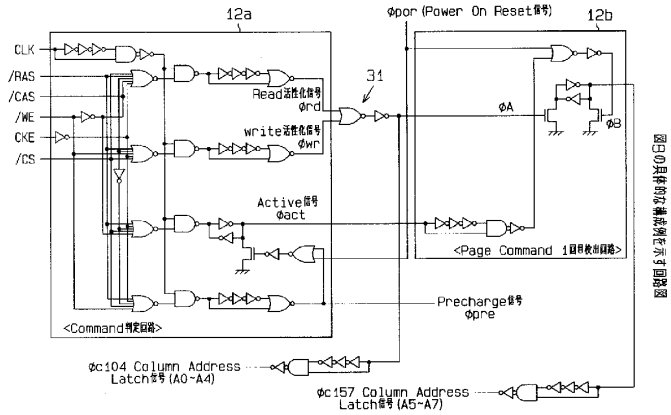


図13の具体的な構成例を示す回路図

【図１４】

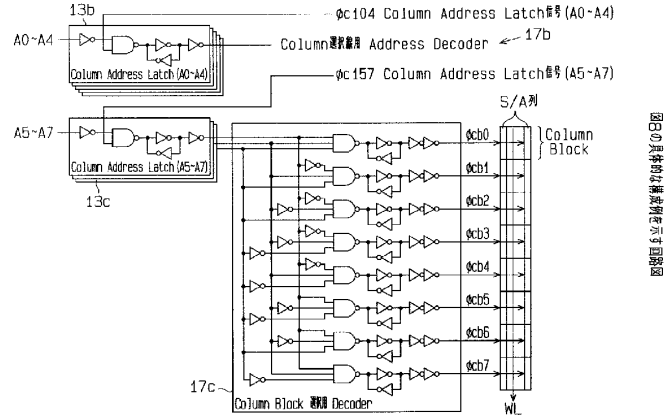


図14の具体的な構成例を示す回路図

【図１５】

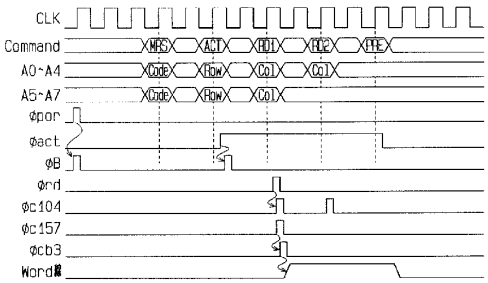


図13及び図14の内部動作を示すタイミング図

【図１６】

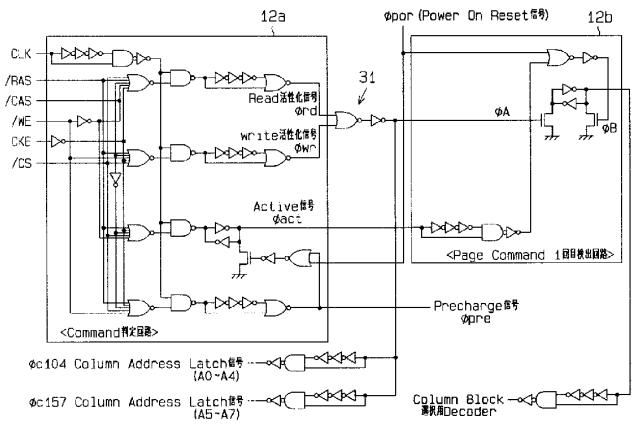


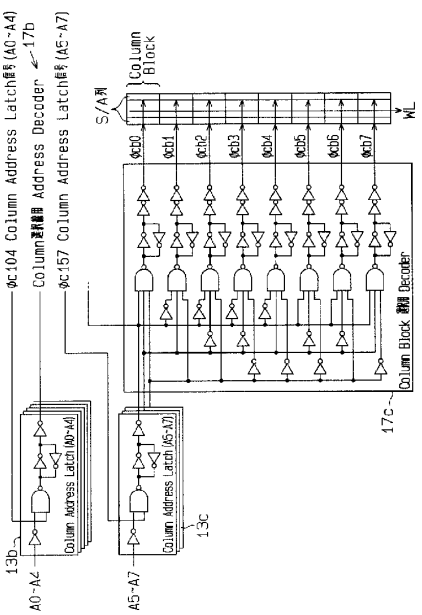
図10の具体的な構成例を示す回路図

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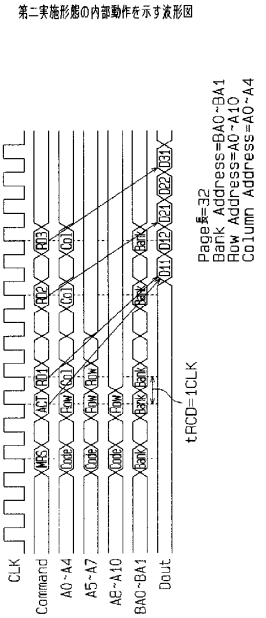
【図１７】

図１１の具体的な構成例を示す回路図



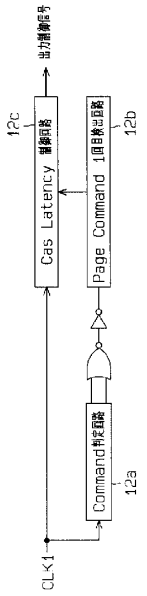
【図１８】

第二実施形態の内部動作を示す波形図



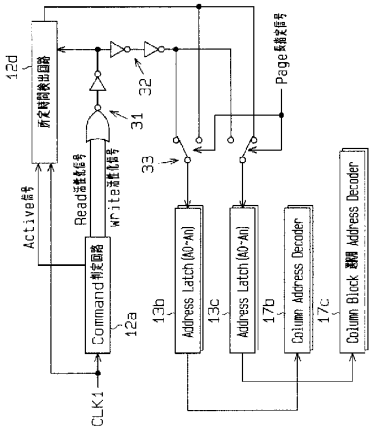
【図１９】

キャスレイテンシの制御方法を説明するブロック図



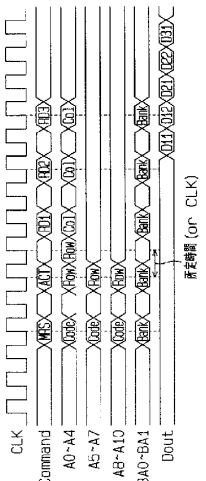
【図２０】

第三実施形態のアクセス制御を説明するブロック図



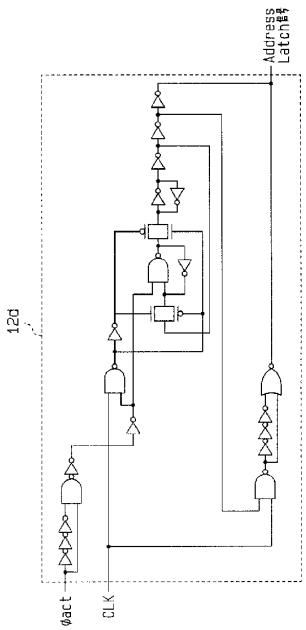
【図２１】

第三実施形態の内部動作を示す波形図



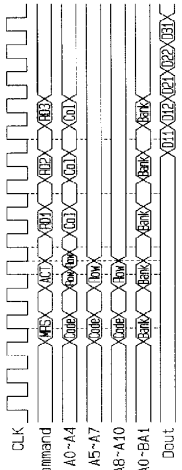
【図２２】

所定時間検出回路の具体的な構成例を示す回路図



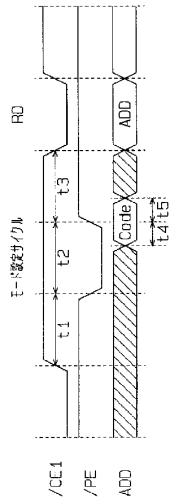
【図２３】

第四実施形態の内部動作を示す波形図



【図２４】

モード設定サイクルを説明する波形図



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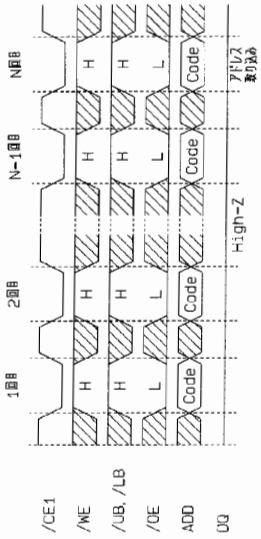
【図２５】

コマンドの説明図

	CE2	/CE1	/WE	/OE	/LB	/UB	LDQ	UDQ	Mode
1	L	*	*	*	*	*	HZ	HZ	PD
2	H	H	*	*	*	*	HZ	HZ	STB
3	H	L	H	H	*	*	HZ	HZ	OD
4	H	L	L	H	L	L	Din	Din	WR
5	H	L	L	H	L	H	Din	*	LWR
6	H	L	L	H	H	L	*	Din	UWR
7	H	L	L	H	H	H	*	*	Non WR
8	H	L	H	L	L	L	Dout	Dout	RD
9	H	L	H	L	L	H	Dout	HZ	LRD
10	H	L	H	L	H	L	HZ	Dout	URD
11	H	L	H	L	H	H	HZ	HZ	Non RD

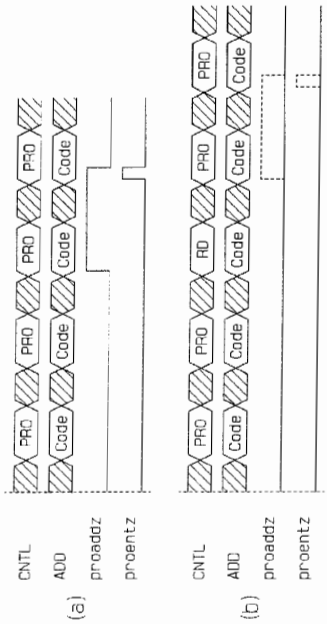
【図２６】

モード設定サイクルを説明する波形図



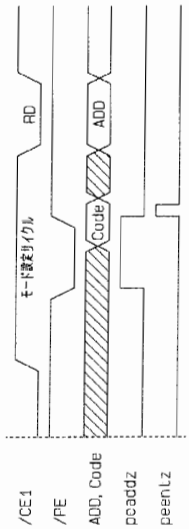
【図２７】

プログラムモード設定回路の動作波形図



【図２８】

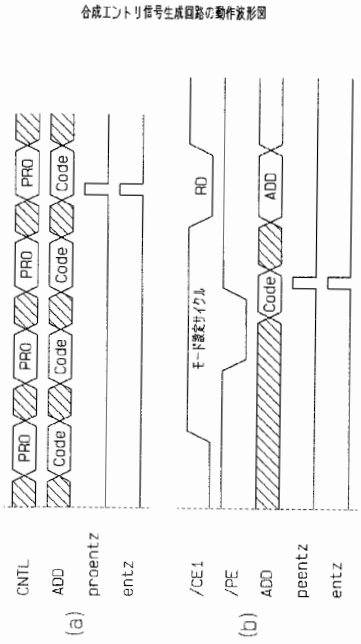
プログラムモード設定回路の動作波形図



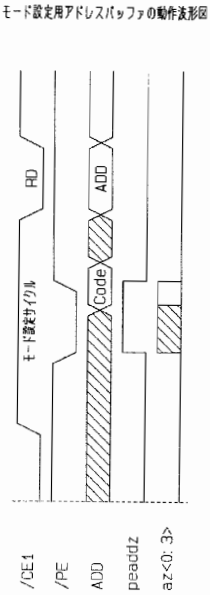
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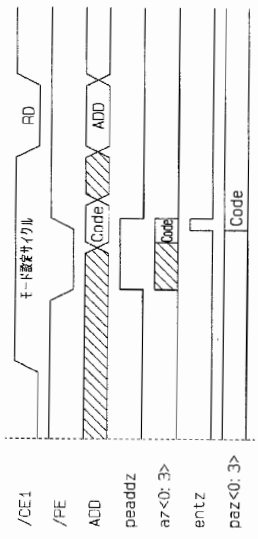
【図２９】



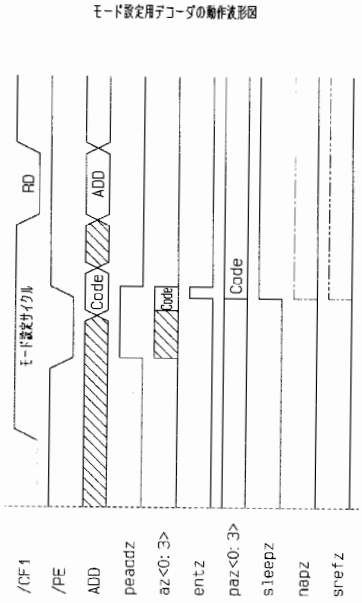
【図３０】



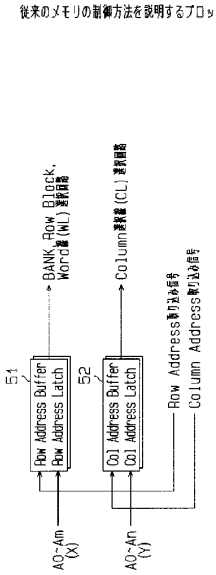
【図３１】



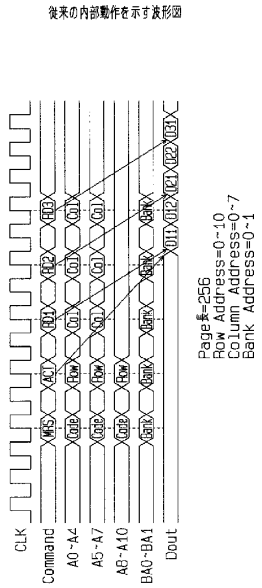
【図３２】



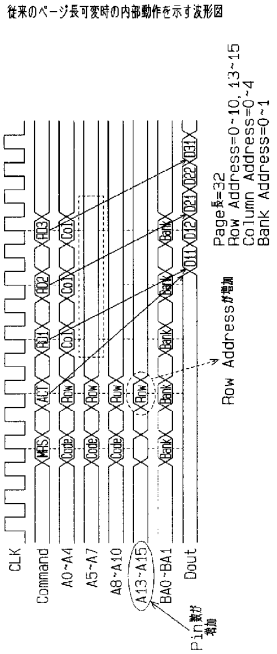
【図３３】



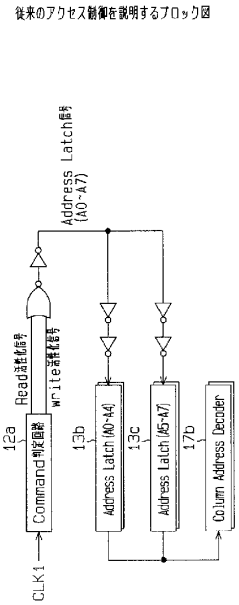
【図３４】



【図３５】



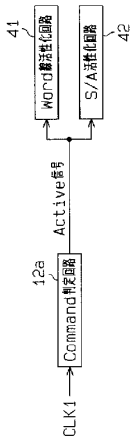
【図３６】



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【図３７】

従来の活性化回路の制御方法を説明するブロック図



フロントページの続き

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特開昭６３－２０１９８８（ＪＰ，Ａ）
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(58)調査した分野(Int.Cl.，ＤＢ名)
C11C 11/40-11/409

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ELECTRONIC ACKNOWLEDGEMENT RECEIPT

APPLICATION #	RECEIPT DATE / TIME	ATTORNEY DOCKET #
17/403,832	**08/06/2022 01:22:40 AM ET**	**NL023-02US02**

Title of Invention

MEMORY MODULE WITH DATA BUFFERING

Application Information

APPLICATION TYPE	Utility - Nonprovisional Application under 35 USC 111(a)	PATENT #	-
CONFIRMATION #	3549	FILED BY	Jamie Zheng
PATENT CENTER #	60849425	FILING DATE	08/16/2021
CUSTOMER #	79141	FIRST NAMED INVENTOR	Jefferey C. Solomon
CORRESPONDENCE ADDRESS	-	AUTHORIZED BY	-

Documents

TOTAL DOCUMENTS: 50

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WO2002025454A2-Halbert434.pdf	10	Foreign Reference	701 KB
IPR2022-00745_Petition.pdf	112	Non Patent Literature	1073 KB
IPR2022-00744_Petition.pdf	100	Non Patent Literature	1027 KB
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Micron_ID_Extrinisic_Evidence.pdf	21	Non Patent Literature	188 KB
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NL023-02US02_IDS_Transmittal_2022-08-05.pdf	4	Transmittal Letter	126 KB

Digest

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Stone_Declaration.pdf	8EAE0D190E099C5CD8E8A59261B4BBD72E64950A988E162E5AB77D7779B4C04736E6EEC520C2354005D90DFBF72AA38B5706E855A246D1114BEAEED43DE49B87
Smith_Declaration.pdf	12FEEC555985A10419303BA02B6B9756B08AF8531BDA23A1DE0578ACC31F2AE2D233043A1EDD6FCB215959878E64E5978050741FE63927B614A2B71B72CEE9C4
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Joint_CC.pdf	89DC08A6B1D8DC3E03C08ADA62AF9A9F8532EA9D744DC14DD740E357ED544EFC4099F7778A0AFE62D9F0FA1688D50659AC53C7F37F1A283D0FB00E7620710A6A
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Stone-Microcomputer_interfacing_Part1.pdf	26BB209494F9025D587CCB1D014A7C9F48684327F96C1D53D5635F751292C63C7341002350D6F14CED7B4F6D7A43EC52B55028C4C373985FF0FCF42C74A7C158

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This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Electronically filed August 5, 2022

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of:	Jefferey C. SOLOMON	Confirmation No.:	3549
Serial No.:	17/403,832	Group Art Unit:	2139
Filed:	August 16, 2021	Examiner:	TBA
For:	*MEMORY MODULE WITH DATA BUFFERING*	Attorney Docket No.:	NL023-02US02

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In accordance with the duty of disclosure provisions of 37 C.F.R. §1.56, there is hereby provided certain information which the Examiner may consider material to the examination of the subject U.S. patent application. It is requested that the Examiner make this information of record if it is deemed material to the examination of the application.

1. Enclosures accompanying this Information Disclosure Statement are:

1a. ☒ A list of all patents, publications, applications, or other information submitted for consideration by the office.

1b. A legible copy of:

☒ Each foreign patent;

☒ Each publication or that portion which caused it to be listed on the PTO-1449;

☐ For each cited pending U.S. application, the application specification including the claims, and any drawing of the application, or portion of the application which caused it to be listed on the PTO-1449 including any claims directed to that portion;

☒ all other information or portion which caused it to be listed on the PTO-1449.

1c. ☐ An English language copy of search report(s) from a counterpart foreign application or PCT International Search Report.

1d. ☒ Explanations of relevancy (ATTACHMENT 1(d), hereto) or English language abstracts of the non-English language publications.

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2. ☒ This Information Disclosure Statement is filed under 37 C.F.R. §1.97(b):

☐ Within three months of the filing date of a national application other than a continued prosecution application under §1.53(d);

☐ Within three months of the date of entry of the national stage as set forth in §1.491 in an international application;

☒ Before the mailing of the first Office action on the merits;

☐ Before the mailing of a first Office action after the filing of a request for continued examination under §1.114.

3. ☐ This Information Disclosure Statement is filed under 37 C.F.R. §1.97(c) after the period specified in 37 C.F.R. §1.97(b), but before the mailing date of any of a final action under 37 C.F.R. §1.113, a notice of allowance under 37 C.F.R. §1.311 or an action that otherwise closes prosecution in the application.

(Check either Item 3a, 3b, 3c or 3d)

3a. ☐ The Certification Statement in Item 5 below is applicable. Accordingly, no fee is required.

3b. ☐ The $260 (large entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Deposit Account No. 60-3916.

3c. ☐ The $130 (small entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Deposit Account No. 60-3916.

3d. ☐ The $120 (micro entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Deposit Account No. 60-3916.

(Items 3b or 3c to be checked if any reference known for more than 3 months)

4. ☐ This Information Disclosure Statement is filed under 37 C.F.R. §1.97(d) after the period specified in 37 C.F.R. §1.97(c), but on or before the date of payment of the issue fee.

(Check Item 4a, and 4b, 4c or 4d)

4a. ☐ The Certification Statement in Item 5 below is applicable.

4b. ☐ The $260 (large entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Deposit Account No. 60-3916.

4c. ☐ The $130 (small entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Deposit Account No. 60-3916.

4d. ☐ The $120 (micro entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Deposit Account No. 60-3916.

5. ☐ Certification Statement (applicable if Item 3a or Item 4a is checked)

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(Check either Item 5a, 5b, 5c or 5d)

5a. ☐ In accordance with 37 C.F.R. §1.97(e)(1), it is certified that each item of information contained in this information disclosure statement was first cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement.

5b. ☐ In accordance with 37 C.F.R. §1.97(e)(2), it is certified that no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 C.F.R. §1.56(c) more than three months prior to the filing of this information disclosure statement.

5c. ☐ Each item of information contained in this information disclosure statement was cited in a communication from a foreign patent office in a counterpart application, and the communication was not **received** by any individual designated in 37 C.F.R. §1.56(c) more than thirty days prior to the filing of this information disclosure statement.

5d. ☐ Pursuant to 37 C.F.R. §1.704(d), each item of information contained in this information disclosure statement was cited in a communication from a foreign patent office in a counterpart application, and the communication was not **received** by any individual designated in 37 C.F.R. §1.56(c) more than thirty days prior to the filing of this information disclosure statement.

6. ☒ Copies of each cited U.S. patent and each U.S. patent application publication are not enclosed pursuant to the USPTO OG Notice dated 05 August 2003 waiving the requirement under 37 C.F.R. 1.98(a)(2)(i) for U.S. patent applications filed after June 30, 2003.

7. ☒ This application is a continuation application under 37 C.F.R. §1.53(b) or (d).

(Check appropriate Items 7a, 7b and/or 7c)

7a. ☐ A Petition to Withdraw from issue under 37 C.F.R. §1.313(b)(5) is concurrently filed herewith.

7b. ☐ Copies of publications listed on Form PTO-1449 from prior application Serial No. , filed on , are not being submitted pursuant to 37 C.F.R. §1.98(d).

7c. ☒ Copies of the publications listed on the attached Form PTO-1449 that were not previously cited in prior application Serial Nos. **15/857,519**, filed on **December 28, 2017**, **14/715,486**, filed on **May 18, 2015**; **13/971,231** , filed on **August 20, 2013**; **13/287,081** , filed on **November 1, 2011**; **13/032,470** , filed on **February 22, 2011**; **12/955,711** , filed on **November 29, 2010**; **12/629,827** , filed on **December 2, 2009**; **12/408,652** , filed on **March 20, 2009**; **11/335,875** , filed on **January 19, 2006**; **11/173,175** , filed on **July 1, 2005**; **11/075,395** , filed on **March 7, 2005**, of which this application claims priority under 35 U.S.C. §120, are provided herewith.

8. ☐ This is a Supplemental Information Disclosure Statement. (Check Item 8a)

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8a. ☐ This Supplemental Information Disclosure Statement under 37 C.F.R. §1.97(f) supplements the Information Disclosure Statement filed on . A bona fide attempt was made to comply with 37 C.F.R. §1.98, but inadvertent omissions were made. These omissions have been corrected herein. Accordingly, additional time is requested so that this Supplemental Information Disclosure Statement can be considered as if properly filed on .

9. ☐ In accordance with 37 C.F.R. §1.98, a concise explanation of what is presently understood to be the relevance of each non-English language publication is:

(Check Item 9a, 9b, or 9c)

9a. ☐ satisfied because all non-English language publications were cited on the enclosed English language copy of the PCT International Search Report or the search report from a counterpart foreign application indicating the degree of relevance found by the foreign office.

9b. ☐ set forth in the application.

9c. ☐ enclosed as an attachment hereto.

10. ☒ The Commissioner is authorized to charge any additional fee required or credit any overpayment for this Information Disclosure Statement and/or Petition to Deposit Account No. 60-3916 (order no. NL023-02US02).

11. ☒ No admission is made that the information cited in this Statement is, or is considered to be, material to patentability nor a representation that a search has been made (other than a search report of a foreign counterpart application or PCT International Search Report if submitted herewith). 37 C.F.R. §§1.97(g) and (h).

Respectfully submitted,

Date: August 5, 2022

/Jamie J. Zheng/ 51,167
Jamie J. Zheng (Reg. No.)
Customer No. 79141

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UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/403,832	08/16/2021	Jefferey C. Solomon	NL023-02US02	3549

79141 7590 09/02/2022

USCH Law, PC
3790 El Camino Real #1147
Palo Alto, CA 94304

EXAMINER	
NGUYEN, VAN THU T	

ART UNIT	PAPER NUMBER
2824	

NOTIFICATION DATE	DELIVERY MODE
09/02/2022	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

eofficeaction@appcoll.com
jzheng@uschlaw.com
patents@uschlaw.com

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Office Action Summary	Application No. 17/403,832	Applicant(s) Solomon et al.	
	Examiner VANTHU NGUYEN	Art Unit 2824	AIA (FITF) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☑ Responsive to communication(s) filed on 08/16/2021.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL.** 2b) ☑ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5) ☑ Claim(s) 1-12 is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6) ☐ Claim(s) _____ is/are allowed.

7) ☑ Claim(s) 1-12 is/are rejected.

8) ☐ Claim(s) _____ is/are objected to.

9) ☐ Claim(s) _____ are subject to restriction and/or election requirement

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to **PPHfeedback@uspto.gov.**

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☑ The drawing(s) filed on 08/16/2021 is/are: a)☑ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☑ Notice of References Cited (PTO-892)

2) ☑ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date 12/11/2021,08/06/2022.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date _____.

4) ☐ Other: _____.

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DETAILED ACTION

1. The present application is being examined under the pre-AIA first to invent provisions.

2. Claims 1-12 are pending and examined.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of pre-AIA 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

4. Claims 1-12 are rejected under pre-AIA 35 U.S.C. 102(a) as being anticipated by US 7,155,627 to Matsui (hereafter Matsui).

Regarding independent claim 1, Matsui teaches a memory module (*FIG. 6: memory module 103a*) operable in a computer system, the computer system including a memory controller (*FIG. 6: memory controller 101*) coupled to a memory bus, the memory bus including address and control signal lines and data signal lines (*FIG. 11: command address bus, DQ bus*), the memory module comprising:

- a printed circuit board having a plurality of edge connections configured to be electrically coupled to a corresponding plurality of contacts of a module slot of the computer system (*see FIG. 3*);
- logic coupled to the printed circuit board (*FIG. 6: buffer105 of module 103a*) and configurable to receive input address and control signals associated with a read or write memory command via the address and control signal lines and to output registered address and control signals corresponding to the input address and

control signals (*FIG. 11: signals on command/address bus*), the input address and control signals including a plurality of input chip select signals (*e.g. bits to identify ranks 1 to 4, see 17:49-51*) and other input address and control signals, the plurality of input chip select signals at least including a first input chip select signal and a second input chip select signal, the first input chip select signal having an active value and the second input chip select signal having an inactive value, the registered address and control signals including a plurality of registered chip select signals and other registered address and control signals, the plurality of registered chip select signals at least including a first registered chip select signal corresponding to the first input chip select signal and a second registered chip select signal corresponding to the second input chip select signal, the first registered chip select signal having an active value and the second registered chip select signal having an inactive value, wherein the logic is further configurable to output data transfer control signals associated with the read or write memory command (*because one of ranks 1 to 4 is selected at a time read/write operation, see 17:52 to 18:3*);

- memory devices mounted on the printed circuit board, the memory devices at least including first memory devices and second memory devices, wherein the first memory devices are configured to receive the first registered chip select signal and the other registered address and control signals, and to receive or output data signals associated with the read or write command (*FIG. 6: e.g. one of the DRAMs 110r1 of rank 1 configured to receive CA signals from buffer 105 for read/write operation*), and wherein the second memory devices are configured to

receive the second registered chip select signal and the other registered address and control signals (*FIG. 6: e.g. one of the DRAMs 110r2 of rank 2 configured to receive CA signals from buffer 105 for read/write operation*); and

- circuitry coupled between the memory devices and the data signal lines in the memory bus, and configurable to be in any of a plurality of states including a first state and a second state (*FIG. 42: the circuitry as shown for transferring data between DRAM 110 and DQ*), wherein:
    - the circuitry is configurable to transition from the first state to the second state in response to the data transfer control signals (*FIG. 46: the driver circuit transfers write data when to write data phase signal WDPS active*);
    - the circuitry in the first state is configured to disable signal communication through the circuitry (*FIG. 42: the driver circuit does not transfer write data when write data phase signal WDPS inactive*);
    - the circuitry in the second state is configured to transfer the data signals associated with the read or write command via registered data transfers in accordance with a transfer time budget of the memory module (*FIG. 46: for DRAM module, time budget is write latency, which is WL=6*);
    - the transfer time budget of the memory module includes a predetermined amount of time delay associated with the registered data transfers through the circuitry (*i.e. the write latency*); and
    - an overall CAS latency of the memory module is greater than an actual operational CAS latency of each of the memory devices by at least the predetermined amount of time delay (*FIGS. 31-32 show the write latency*

of a memory device WL=4; FIGS. 41 and 46 show the write latency of a DRAM module WL=6).

Regarding dependent claim 2, Matsui teaches wherein each of the memory devices has a corresponding load, and the circuitry is configured to isolate the loads of the memory devices from the memory bus (*FIG. 19: the load of a memory device is isolated with NMOS transistor turns off*).

Regarding dependent claim 3, Matsui teaches wherein the data signals include respective sets of consecutively transmitted data bits corresponding to respective data signal lines in the memory bus, and wherein each set of consecutively transmitted data bits are successively transferred through the circuitry in response to the data transfer control signals and in accordance with the transfer time budget of the memory module (*FIG. 46: see consecutively outputted data bits after WL=6*).

Regarding dependent claim 4, Matsui teaches wherein each of the memory devices is 4-bits or 8- bits wide (*8-bits wide, see 12:31-36*), and wherein the first memory devices form a rank that is 32-bits, 64-bits or 72-bits wide (*FIG. 6: 8 of 8-bits wide memory devices form a rank of 64-bits wide*).

Regarding dependent claim 5, Matsui teaches wherein each of the memory devices is 4-bits wide, and wherein the memory devices are configured in 8-bit-wide pairs (*see FIGS. 4-5 and 16:24-37*).

Regarding dependent claim 6, Matsui teaches wherein the circuitry includes logic pipelines configurable to enable data transfers between the memory devices and the memory bus through the circuitry (*the pipeline comprising circuitry shown in FIG. 42 for each DRAM 110 and buffer 105 shown in FIG. 44, which transfer data between DRAM 110 and DQ terminal*).

Regarding dependent claim 7, Matsui teaches wherein the memory module has a specified data rate, and wherein the data signals are transferred between the first memory devices and the memory controller at the specified data rate (*Double Data Rate, see 13:54-67*).

Regarding dependent claim 8, Matsui teaches a phase locked loop clock driver configured to output a clock signal in response to one or more signals received from the memory controller (*FIG. 44: DLL 205, which is in response to global clock as shown in FIG. 46*), wherein the predetermined amount of time delay is at least one clock cycle time delay (*FIG. 46: the predetermined amount of time delay is 2 global clock cycles in this case*).

Regarding dependent claim 9, Matsui teaches wherein the memory devices are dynamic random access memory devices configured to operate synchronously with the clock signal, and wherein each memory device in the first memory devices is configured to receive or output a respective set of data strobes and to receive or output data bits on both edges of each of the respective set of data strobes (*the memory module is SDRAMs with DDR memories, see 13:54-67*).

Regarding dependent claim 10, Matsui teaches wherein the circuitry includes data paths that are disabled when the circuitry is in the first state and enabled when the circuitry is in the second state (*FIG. 42: data receiver 202 is either enabled or disabled for transferring data in response to WDPS*).

Regarding dependent claim 11, Matsui teaches wherein the data paths are disabled when no data signals associated with any memory command are being transferred through the circuitry (*FIG. 42: data receiver 202 is disabled when WDPS is inactive*).

Regarding dependent claim 12, Matsui teaches wherein the memory module has a specified data rate, and wherein the data signals are transferred through the data paths at the specified data rate (*Double Data Rate, see 13:54-67*).

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to VANTHU NGUYEN whose telephone number is (571)272-1881. The examiner can normally be reached M-F: 9:00AM - 5:00PM.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at http://www.uspto.gov/interviewpractice.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on (571) 272-1869. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of published or unpublished applications may be obtained from Patent Center. Unpublished application information in Patent Center is available to registered users. To file and manage patent submissions in Patent Center, visit: https://patentcenter.uspto.gov. Visit https://www.uspto.gov/patents/apply/patent-center for more information about Patent Center and https://www.uspto.gov/patents/docx for information about filing in DOCX format. For additional questions, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

August 27, 2022

/VANTHU T NGUYEN/
Primary Examiner, Art Unit 2824

Notice of References Cited	Application/Control No. 17/403,832	Applicant(s)/Patent Under Reexamination Solomon et al.	
	Examiner VANTHU NGUYEN	Art Unit 2824	Page 1 of 1

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*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
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*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	CPC Classification
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Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

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Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/403,832	Solomon et al.
	Examiner	Art Unit
	VANTHU NGUYEN	2824

CPC - Searched*		
Symbol	Date	Examiner
G11C 5/04 , 7/1072, 15/00		

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Symbol	Date	Examiner

US Classification - Searched*			
Class	Subclass	Date	Examiner

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

Search Notes		
Search Notes	Date	Examiner
SEARCH (see print out history)	08/27/2022	VTN

Interference Search			
US Class/CPC Symbol	US Subclass/CPC Group	Date	Examiner

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				Application Number	17/403,832
				Filing Date	August 16, 2021
				First Named Inventor	Jefferey C. SOLOMON
				Art Unit	2139
				Examiner Name	TBA
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				First Named Inventor	Jefferey C. SOLOMON
				Art Unit	2139
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				First Named Inventor	Jefferey C. SOLOMON
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				First Named Inventor	Jefferey C. SOLOMON
				Art Unit	2139
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				First Named Inventor	Jefferey C. SOLOMON
				Art Unit	2139
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Ref #	Hits	Search Query	DBs	Default Operator	Plurals	British Equivalents	Time Stamp
L1	1	"17403832"	(US-PGPUB; USPAT; USOCR; FIT (WO))	OR	ON	ON	2022/08/25 10:31 AM
L2	5786	select$3 WITH rank$1 WITH module$1	(US-PGPUB; USPAT; USOCR; FIT (WO))	OR	ON	ON	2022/08/25 11:55 AM
L3	227	(L2 AND @ad<"20040305") NOT netlist	(US-PGPUB; USPAT; USOCR; FIT (WO))	OR	ON	ON	2022/08/25 11:58 AM
L4	12	"12955711"	(US-PGPUB; USPAT; USOCR; FIT (WO))	OR	ON	ON	2022/08/27 01:50 PM
L5	36	"12955711" "12629827" "12408652" "11335875" "11173175" "11335875" "11075395" "11173175" "11075395" "11075395"	(US-PGPUB; USPAT; USOCR; FIT (WO))	OR	ON	ON	2022/08/27 01:51 PM
L6	12	"12955711"	(US-PGPUB; USPAT; USOCR; FIT (WO))	OR	ON	ON	2022/08/27 01:53 PM

PE2E SEARCH - Search History (Interference)

There are no Interference searches to show.

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				Filing Date	*August 16, 2021*
				First Named Inventor	*Jefferey C. Solomon*
				Art Unit	*2139*
				Examiner Name	*TBD*
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				First Named Inventor	*Jefferey C. Solomon*
				Art Unit	*2139*
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				First Named Inventor	*Jefferey C. Solomon*
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	313.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00363, EXHIBITS 1045, 'Deposition Transcript of R. Jacob Baker in IPR2017-00577 concerning the parent to the '907 Patent (Jan. 12, 2018),' filed February 22, 2019
	314.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00363, EXHIBITS 1046, 'Final Written Decision in IPR2017-00577 invalidating all challenged claims to the parent to the '907 Patent (July 5, 2018),' filed February 22, 2019
	315.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00363, EXHIBITS 1048, 'U.S. Patent No. 7,133,960,' filed February 22, 2019
	316.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00363, Petitioners' Reply to Patent Owner's Response, filed February 22, 2019
	317.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00363, Patent Owner's Objections To Reply Evidence, filed March 1, 2019
	318.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00363, Petitioners' Request for Oral Argument, filed March 4, 2019

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				First Named Inventor	*Jefferey C. Solomon*
				Art Unit	*2139*
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	319.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00363, Patent Owner's Request For Oral Argument, filed March 4, 2019
	320.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00363, Patent Owner's Motion To Exclude, filed March 4, 2019
	321.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00363, Petitioners' Opposition to Patent Owner's Motion to Exclude, filed March 11, 2019
	322.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00363, Patent Owner's Sur-Reply To Petitioner's Reply, filed March 15, 2019
	323.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00363, Patent Owner's Reply To Petitioner's Opposition To Motion To Exclude, filed March18, 2019
	324.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00363, Order, Trial Hearing, filed March 22, 2019
	325.	Inter Partes Review Case No. IPR2014-00882, Exhibit 1007 to Petition for Inter Partes Review, "Declaration of Dr. Srinivasan Jagannathan," filed on June 22, 2014.
	326.	Petition for Inter Partes Review filed on 6/22/2014 for U.S. Patent No. 7,881,150, Case No. IPR2014-00882 and Case No. IPR2014-01011, and all associated documents including cited references and expert declarations, available at https://ptabtrials.uspto.gov
	327.	Inter Partes Review Case No. IPR2014-00882, Corrected Petition for Inter Partes Review of U.S. Patent No. 7,881,150, filed on July 8, 2014.
	328.	Inter Partes Review of U.S. Patent No. 7,881,150, Case No. IPR2014-00882, Patent Owner's Preliminary Response Pursuant to 37 C.F.R. § 42.107, filed October 7, 2014
	329.	Inter Partes Review of U.S. Patent No. 7,881,150, Case No. IPR2014-00882, Decision – Institution of Inter Partes Review 37 C.F.R. § 42.108, issued December 16, 2014
	330.	Inter Partes Review Case No. IPR2014-00882, Patent Owner Response, filed May 8, 2015
	331.	Inter Partes Review Case No. IPR2014-00882, Exhibit 2002, 'Declaration of Professor Carl Sechen,' filed May 8, 2015
	332.	Inter Partes Review Case No. IPR2014-00882, Exhibit 2003, 'Transcript of Videotaped Deposition of Srinivasan Jagannathan, Ph. D,' filed May 8, 2015
	333.	Inter Partes Review Case No. IPR2014-00882, Petitioner Diablo Technologies, Inc.'s Reply to Patent Owner Netlist, Inc.'s Response, filed June 19, 2015
	334.	Inter Partes Review Case No. IPR2014-00882, Exhibit 1022, 'Professor Carl Sechen Deposition Transcript,' filed June 19, 2015

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	335.	Inter Partes Review Case No. IPR2014-00882, Exhibit 1023, 'Dr. Srinivasan Jagannathan Supplemental Declaration,' filed June 19, 2015
	336.	Inter Partes Review Case No. IPR2014-00882, Petitioner's Request for Oral Argument, filed July 1, 2015
	337.	Inter Partes Review Case No. IPR2014-00882, Patent Owner's Request for Oral Argument, filed July 3, 2015
	338.	Inter Partes Review Case No. IPR2014-00882, Order - Request for Oral Argument - 37 C.F.R. 42.70, filed July 10, 2015
	339.	Inter Partes Review Case No. IPR2014-00882, Record of Oral Hearing, filed November 16, 2015
	340.	Inter Partes Review Case No. IPR2014-00882, Final Written Decision 35 USC 318 and 37 CFR 42.73, filed December 14, 2015
	341.	Inter Partes Review Case No. IPR2014-00882, Netlist Inc.'s Notice of Appeal, filed February 10, 2016
	342.	Inter Partes Review Case No. IPR2014-00883, Exhibit 1011 to Petition for Inter Partes Review, "Declaration of Dr. Srinivasan Jagannathan," filed on June 21, 2014.
	343.	Petition for Inter Partes Review filed on 6/24/2014 for U.S. Patent No. 8,081,536, Case No. IPR2014-00883, and all associated documents including cited references and expert declarations, available at https://ptabtrials.uspto.gov
	344.	Inter Partes Review Case No. IPR2014-00883, Corrected Petition for Inter Partes Review of U.S. Patent No. 8,081,536, filed on July 8, 2014.
	345.	Inter Partes Review of U.S. Patent No. 8,081,536, Case No. IPR2014-00883, Patent Owner's Preliminary Response Pursuant to 37 C.F.R. § 42.107, filed October 7, 2014
	346.	Inter Partes Review of U.S. Patent No. 8,081,536, Case No. IPR2014-00883, Decision – Institution of Inter Partes Review 37 C.F.R. § 42.108, issued December 16, 2014
	347.	Inter Partes Review Case No. IPR2014-00883, Patent Owner Response, filed May 8, 2015
	348.	Inter Partes Review Case No. IPR2014-00883, Petitioner Diablo Technologies, Inc.'s Reply to Patent Owner Netlist, Inc.'s Response, filed June 19, 2015
	349.	Inter Partes Review Case No. IPR2014-00883, Exhibit 1025, 'Professor Carl Sechen Deposition Transcript,' filed June 19, 2015
	350.	Inter Partes Review Case No. IPR2014-00883, Exhibit 1026, 'Dr. Srinivasan Jagannathan Supplemental Declaration,' filed June 19, 2015
	351.	Inter Partes Review Case No. IPR2014-00883, Petitioner's Request for Oral Argument, filed July 1, 2015

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	352.	Inter Partes Review Case No. IPR2014-00883, Patent Owner's Request for Oral Hearing, filed July 3, 2015
	353.	Inter Partes Review Case No. IPR2014-00883, Order - Request for Oral Argument - 37 C.F.R. 42.70, filed July 10, 2015
	354.	Inter Partes Review Case No. IPR2014-00883, Record of Oral Hearing, filed November 16, 2015
	355.	Inter Partes Review Case No. IPR2014-00883, Final Written Decision - 35 USC 318 and 37 CFR 42.73, filed December 14, 2015
	356.	Inter Partes Review Case No. IPR2014-00883, Netlist Inc.'s Notice of Appeal, filed February 10, 2016
	357.	Inter Partes Review Case No. IPR2014-01011, Exhibit 1007 to Petition for Inter Partes Review, "Declaration of Dr. Srinivasan Jagannathan." filed on June 22, 2014.
	358.	Inter Partes Review Case No. IPR2014-01011, Corrected Petition for Inter Partes Review of U.S. Patent No. 7,881,150, filed on July 8, 2014.
	359.	Inter Partes Review of U.S. Patent No. 7,881,150, Case No. IPR2014-01011, Patent Owner's Preliminary Response Pursuant to 37 C.F.R. § 42.107, filed October 7, 2014
	360.	Inter Partes Review of U.S. Patent No. 7,881,150, Case No. IPR2014-01011, Decision – Institution of Inter Partes Review 37 C.F.R. § 42.108, issued December 16, 2014
	361.	Inter Partes Review of U.S. Patent No. 7,881,150, Case No. IPR2014-01011, Exhibit 3001 to Decision – Institution of Inter Partes Review, Excerpts from IEEE Dictionary, issued December 16, 2014
	362.	Inter Partes Review of U.S. Patent No. 7,881,150, Case No. IPR2014-01011, Exhibit 3002 to Decision – Institution of Inter Partes Review, Excerpts from IEEE Dictionary, issued December 16, 2014
	363.	Inter Partes Review of U.S. Patent No. 7,881,150, Case No. IPR2014-01011, Exhibit 3003 to Decision – Institution of Inter Partes Review, Excerpts from Oxford English Dictionary, issued December 16, 2014
	364.	Inter Partes Review of U.S. Patent No. 7,881,150, Case No. IPR2014-01011, Exhibit 3004 to Decision – Institution of Inter Partes Review, Excerpts from Oxford English Dictionary, issued December 16, 2014
	365.	Inter Partes Review Case No. IPR2014-01011, Patent Owner Response, filed May 8, 2015
	366.	Inter Partes Review Case No. IPR2014-01011, Petitioner Diablo Technologies, Inc.'s Reply to Patent Owner Netlist, Inc.'s Response, filed June 19, 2015
	367.	Inter Partes Review Case No. IPR2014-01011, Exhibit 1027, 'Professor Carl Sechen Deposition Transcript,' filed June 19, 2015

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	368.	Inter Partes Review Case No. IPR2014-01011, Exhibit 1028, 'Dr. Srinivasan Jagannathan Supplemental Declaration,' filed June 19, 2015
	369.	Inter Partes Review Case No. IPR2014-01011, Petitioner's Request for Oral Argument, filed July 1, 2015
	370.	Inter Partes Review Case No. IPR2014-01011, Patent Owner's Request for Oral Hearing, filed July 3, 2015
	371.	Inter Partes Review Case No. IPR2014-01011, Order - Request for Oral Argument - 37 C.F.R. 42.70, filed July 10, 2015
	372.	Inter Partes Review Case No. IPR2014-01011, Record of Oral Hearing, filed November 16, 2015
	373.	Inter Partes Review Case No. IPR2014-01011, Final Written Decision - 35 USC 318 and 37 CFR 42.73, filed December 14, 2015
	374.	Inter Partes Review Case No. IPR2014-01011, Netlist Inc.'s Notice of Appeal, filed February 10, 2016
	375.	Inter Partes Review Case No. IPR2014-01020, Exhibit 1002 to Petition for Inter Partes Review, "Declaration of Dr. Srinivasan Jagannathan," filed on April 7, 2015.
	376.	Inter Partes Review Case No. IPR2014-01020, Exhibit 1023 to Petition for Inter Partes Review, curriculum vitae of Dr. Srinivasan Jagannathan, filed on April 7, 2015.
	377.	Inter Partes Review Case No. IPR2014-01020, Exhibit 1025 to Petition for Inter Partes Review, "operational," The Pocket Oxford American Dictionary of Current English, Oxford University Press, 2002, filed on April 7, 2015.
	378.	Inter Partes Review Case No. IPR2014-01020, Decision to Institute Inter Partes Review of D U.S. Patent No. 7,881,150, dated October 8, 2015.
	379.	Inter Partes Review Case No. IPR2014-01021, Exhibit 1026 to Petition for Inter Partes Review, curriculum vitae of Dr. Srinivasan Jagannathan, filed on April 7, 2015.
	380.	Inter Partes Review Case No. IPR2014-01021, Corrected Exhibit 1002 to Petition for Inter Partes Review, "Declaration of Dr. Srinivasan Jagannathan," filed on April 22, 2015.
	381.	Inter Partes Review Case No. IPR2014-01021, Decision to Institute Inter Partes Review of U.S. Patent No. 8,081,536, dated October 8, 2015
	382.	Petition for Inter Partes Review filed on 6/24/2014 for U.S. Patent No. 8,516,185, Case No. IPR2014-01029, and all associated documents including cited references and expert declarations, available at https://ptabtrials.uspto.gov
	383.	Inter Partes Review Case No. IPR2014-01029, Petition for Inter Partes Review of U.S. Patent No. 8,516,185, filed on June 24, 2014.

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	384.	Inter Partes Review Case No. IPR2014-01029, Exhibit 1008 to Petition for Inter Partes Review, "Declaration of Charles J. Neuhauser, Ph.D. under 37 C.F.R. § 1.68," filed on June 24, 2014.
	385.	Inter Partes Review Case No. IPR2014-01029, Supplemental Petition for Inter Partes Review of U.S. Patent No. 8,516,185, filed on July 23, 2014.
	386.	Inter Partes Review Case No. IPR2014-01029, Patent Owner's Preliminary Response pursuant to 37 C.F.R. § 42.107, filed on October 17, 2014.
	387.	Inter Partes Review Case No. IPR2014-01029, Decision Denying Institution of Inter Partes Review 37 C.F.R. § 42.108, issued December 16, 2014.
	388.	Inter Partes Review Case No. IPR2014-01029, Petitioner's Request for Rehearing pursuant to 37 C.F.R. § 42.71, filed on January 15, 2015.
	389.	Inter Partes Review Case No. IPR2014-01029, Decision Denying Request for Rehearing, Issued on March 3, 2015.
	390.	Inter Partes Review Case No. IPR2014-01369, Decision Denying Institution of Inter Partes Review 37 C.F.R. § 42.108, issued March 9, 2014.
	391.	Inter Partes Review Case No. IPR2014-01369, Corrected Petition for Inter Partes Review of Claims 1-19 of U.S. Patent No. 8,516,185, filed on September 22, 2014.
	392.	Inter Partes Review Case No. IPR2014-01369, Exhibit 1008 to Corrected Petition for Inter Partes Review, "Declaration of Dr. Nader Bagherzadeh under 37 C.F.R. § 1.68," filed on September 22, 2014.
	393.	Inter Partes Review Case No. IPR2014-01369, Exhibit 1013 to Corrected Petition for Inter Partes Review, "Webster's II New College Dictionary," filed on September 22, 2014.
	394.	Inter Partes Review Case No. IPR2014-01369, Exhibit 1014 to Corrected Petition for Inter Partes Review, "Standard Dictionary of Electrical and Electronics Terms," IEEE 1988, filed on September 22, 2014.
	395.	Inter Partes Review Case No. IPR2015-0 021, Petition for Inter Partes Review of U.S. Patent No. 8,081,536, filed on April 7, 2015
	396.	Inter Partes Review Case No. IPR2015-01020, Petition for Inter Partes Review of U.S. Patent No. 7,881,150, filed on April 7, 2015.
	397.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Related Matters, filed April 28, 2015
	398.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Patent Owner Response to Petition, filed February 22, 2016
	399.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Exhibit 2001, "Declaration of Professor Carl Sechen," filed February 22, 2016

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				First Named Inventor	*Jefferey C. Solomon*
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	400.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Exhibit 2002, "Videotaped Deposition of Srinivasan Jagannathan, Ph.D on February 12, 2016," filed February 22, 2016
	401.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Exhibit 2003, "Videotaped Deposition of Srinivasan Jagannathan, Ph.D on April 20, 2015," filed February 22, 2016
	402.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Petitioner's Objections to Evidence, filed February 29, 2016
	403.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Petitioner's Reply, filed May 19, 2016
	404.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Supplemental Declaration of Dr. Jagannathan, filed May 19, 2016
	405.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, May 10, 2016 Deposition of Carl Sechen, filed May 19, 2016
	406.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Petitioner Request for Oral Argument, filed June 2, 2016
	407.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, PATENT OWNER MOTION FOR OBSERVATIONS, filed June 2, 2016
	408.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, PATENT OWNER REQUEST FOR ORAL ARGUMENT, filed June 2, 2016
	409.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Exhibit 2007, "Deposition of Dr. Srinivasan Jagannathan on May 25, 2016," filed June 2, 2016
	410.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, ORDER Trial Hearing, filed June 8, 2016
	411.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Patent Owner's SUBMISSION ON PROPRIETY OF PETITIONER REPLY, filed June 9, 2016
	412.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Petitioner's Response to Motion for Observations, filed June 10, 2016
	413.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Petitioner's Response to Netlist's Submission, filed June 13, 2016
	414.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Patent Owner's Objections to Petitioner's Demonstrative Exhibits, filed June 23, 2016
	415.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Patent Owner's Demonstrative Exhibits, filed June 24, 2016

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	416.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Petitioner's Updated Exhibit List, filed June 24, 2016
	417.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Petitioner's Demonstrative Exhibits, filed June 24, 2016
	418.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Record of Oral Hearing, dated July 26, 2016
	419.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Final Written Decision, issued September 28, 2016
	420.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Exhibit 3001 to Final Decision, issued September 28, 2016
	421.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Exhibit 3001-2 to Final Decision, issued September 28, 2016
	422.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Exhibit 3002 to Final Decision, issued September 28, 2016
	423.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Exhibit 3003 to Final Decision, issued September 28, 2016
	424.	Inter Partes Review of U.S. Patent No. 7881150, Case No. IPR2015-01020, Exhibit 3004 to Final Decision, issued September 28, 2016
	425.	Inter Partes Review of U.S. Patent No. 8081536, Case No. IPR2015-01021, Patent Owner Response to Petition, filed February 22, 2016
	426.	Inter Partes Review of U.S. Patent No. 8081536, Case No. IPR2015-01021, Exhibit 2001, "Declaration of Professor Carl Sechen," filed February 22, 2016
	427.	Inter Partes Review of U.S. Patent No. 8081536, Case No. IPR2015-01021, Petitioner's Objections to Evidence, filed February 29, 2016
	428.	Inter Partes Review of U.S. Patent No. 8081536, Case No. IPR2015-01021, Petitioner's Reply, filed May 19, 2016
	429.	Inter Partes Review of U.S. Patent No. 8081536, Case No. IPR2015-01021, Supplemental Declaration of Dr. Jagannathan, filed May 19, 2016
	430.	Inter Partes Review of U.S. Patent No. 8081536, Case No. IPR2015-01021, Petitioner Request for Oral Argument, filed June 2, 2016
	431.	Inter Partes Review of U.S. Patent No. 8081536, Case No. IPR2015-01021, PATENT OWNER MOTION FOR OBSERVATIONS, filed June 2, 2016
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	433.	Inter Partes Review of U.S. Patent No. 8081536, Case No. IPR2015-01021, Patent Owner's SUBMISSION ON PROPRIETY OF PETITIONER REPLY, filed June 9, 2016
	434.	Inter Partes Review of U.S. Patent No. 8081536, Case No. IPR2015-01021, Petitioner's Response to Motion for Observations, filed June 10, 2016
	435.	Inter Partes Review of U.S. Patent No. 8081536, Case No. IPR2015-01021, Petitioner's Response to Patent Owner's Submission, filed June 13, 2016
	436.	Inter Partes Review of U.S. Patent No. 8081536, Case No. IPR2015-01021, Patent Owner's Objections to Petitioner's Demonstrative Exhibits, filed June 23, 2016
	437.	Inter Partes Review of U.S. Patent No. 8081536, Case No. IPR2015-01021, Patent Owner's Demonstrative Exhibits, filed June 24, 2016
	438.	Inter Partes Review of U.S. Patent No. 8081536, Case No. IPR2015-01021, Petitioner's Updated Exhibit List, filed June 24, 2016
	439.	Inter Partes Review of U.S. Patent No. 8081536, Case No. IPR2015-01021, Final Decision, issued September 28, 2016
	440.	Inter Partes Review of U.S. Patent No. 8756364, Case No. IPR2017-00549, Petition for Inter Partes Review, filed December 30, 2016
	441.	Inter Partes Review of U.S. Patent No. 8756364, Case No. IPR2017-00549, Exhibit 1003, "Declaration of Harold S. Stone," filed December 30, 2016
	442.	Inter Partes Review of U.S. Patent No. 8756364, Case No. IPR2017-00549, Exhibit 1008, Declaration of John J. Kelly Regarding Records of Joint Electron Device Engineering Council (JEDEC), filed December 30, 2016
	443.	Inter Partes Review of U.S. Patent No. 8,756,364, Case No. IPR2017-00549, DECISION Institution of Inter Partes Review, filed May 15, 2017.
	444.	Inter Partes Review of U.S. Patent No. 8,756,364, Case No. IPR2017-00549, Exhibit 2001 (DECLARATION OF PROFESSOR CARL SECHEN), filed September 15, 2017.
	445.	Inter Partes Review of U.S. Patent No. 8,756,364, Case No. IPR2017-00549, Patent Owner's Response, filed September 15, 2017.
	446.	Inter Partes Review of U.S. Patent No. 8,756,364, Case No. IPR2017-00549, PETITIONERS' OBJECTIONS TO EVIDENCE, filed September 15, 2017.
	447.	Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, Deposition Transcript of Carl Sechen, filed December 15, 2017.
	448.	Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, Petitioner's reply to Patent Owner's Response, filed December 15, 2017.

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				Art Unit	*2139*
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	449.	Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, Supplemental Declaration of Harold S. Stone, filed December 15, 2017.
	450.	Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, Xilinx Xilinx CS280 package datasheet (1999), filed December 15, 2017.
	451.	Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, EXHIBIT 2004, filed January 9, 2017.
	452.	Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, Patent Owner's Motion for Observations, filed January 9, 2017.
	453.	Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, Petitioner's Motion to Exclude Certain Inadmissible Testimony of Patent Owner's Expert Carl Sechen, filed January 9, 2017.
	454.	Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, EXHIBIT 2003, 'Synchronous DRAM Architectures, Organization, and Alternative Technologies,' filed January 18, 2017.
	455.	Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, Petitioner's Response to Patent Owners Motion for Observations, filed January 23, 2018.
	456.	Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, Patent Owner's Opposition to Petitioner's Motion to Exclude, filed January 23, 2018.
	457.	Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, Petitioner's Reply in Support of Motion to Exclude Certain Inadmissible Testimony of Patent Owner's Expert Carl Sechen, filed January 30, 2018.
	458.	Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, Petitioner's Demonstratives, filed February 9, 2018.
	459.	Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, EXHIBIT 2005, filed February 9, 2018.
	460.	Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, Patent Owner's Updated Exhibit List, filed February 9, 2018.
	461.	Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, Petitioner's Updated Exhibit List, filed February 9, 2018.
	462.	Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, Final Written Decision, filed February 14, 2018.
	463.	Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, Hearing Transcript, filed February 14, 2018.
	464.	Inter Partes Review of US Patent No.8756364, Case No. IPR2017-00549, Patent Owner's Supplemental Mandatory Notices, filed April 19, 2018.

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				First Named Inventor	*Jefferey C. Solomon*
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	465.	Inter Partes Review of U.S. Patent No. 8516185, Case No. IPR2017-00577, Petition for Inter Partes Review, filed January 5, 2017
	466.	Inter Partes Review of U.S. Patent No. 8516185, Case No. IPR2017-00577, Exhibit 1003, "Declaration of Harold S. Stone," filed January 5, 2017
	467.	Inter Partes Review of U.S. Patent No. 8,516,185, Case No. IPR2017-00577, DECISION Institution of Inter Partes Review, filed July 7, 2017.
	468.	Inter Partes Review of U.S. Patent No. 8,516,185, Case No. IPR2017-00577, SCHEDULING ORDER, filed July 7, 2017.
	469.	Inter Partes Review of U.S. Patent No. 8,516,185, Case No. IPR2017-00577, Exhibit 2003 (DECLARATION OF R. JACOB BAKER, PH.D., P.E.), filed October 25, 2017.
	470.	Inter Partes Review of U.S. Patent No. 8,516,185, Case No. IPR2017-00577, Exhibit 2004 (Deposition of HAROLD S. STONE, PH.D.), filed October 25, 2017.
	471.	Inter Partes Review of U.S. Patent No. 8,516,185, Case No. IPR2017-00577, Exhibit 2005 (Memory Systems: Cache, DRAM, Disk), filed October 25, 2017.
	472.	Inter Partes Review of U.S. Patent No. 8,516,185, Case No. IPR2017-00577, Exhibit 2006 (PC2100 and PC1600 DDR SDRAM Registered DIMM, Design Specification, Revision 1.3, January 2002), filed October 25, 2017.
	473.	Inter Partes Review of U.S. Patent No. 8,516,185, Case No. IPR2017-00577, Exhibit 2007 (DRAM CIRCUIT DESIGN: Fundamental and High-Speed Topics), filed October 25, 2017.
	474.	Inter Partes Review of U.S. Patent No. 8,516,185, Case No. IPR2017-00577, PATENT OWNER'S RESPONSE, filed October 25, 2017.
	475.	Inter Partes Review of U.S. Patent No. 8,516,185, Case No. IPR2017-00577, PETITIONERS' OBJECTIONS TO EVIDENCE, filed October 31, 2017.
	476.	Inter Partes Review of US Patent No.8516185, Case No. IPR2017-00577, Annotated version of Halbert Figure 4 showing 4:1 MUX/DeMUX and 4 ranks of memory (corrected Ex. 1035), filed February 6, 2018.
	477.	Inter Partes Review of US Patent No.8516185, Case No. IPR2017-00577, Annotated version of Halbert Figure 4 showing 4:1 MUX/DeMUX and 4 ranks of memory, filed February 6, 2018.
	478.	Inter Partes Review of US Patent No.8516185, Case No. IPR2017-00577, Annotated version of Halbert Figure 4 showing Fast components and Slow components, filed February 6, 2018.
	479.	Inter Partes Review of US Patent No.8516185, Case No. IPR2017-00577, Deposition Transcript of R. Jacob Baker (Jan. 12, 2018.), filed February 6, 2018.

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				First Named Inventor	*Jefferey C. Solomon*
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	480.	Inter Partes Review of US Patent No.8516185, Case No. IPR2017-00577, Excerpts from Brent Keeth and R. Jacob Baker, DRAM Circuit Design: A Tutorial (IEEE Press 2001), filed February 6, 2018.
	481.	Inter Partes Review of US Patent No.8516185, Case No. IPR2017-00577, Oral Testimony of R. Jacob Baker in Certain Memory Modules and Components Thereof, and Products Containing Same, Inv. No. 337-TA-1023 (May 11, 2017), filed February 6, 2018.
	482.	Inter Partes Review of US Patent No.8516185, Case No. IPR2017-00577, Petitioners' Reply to Patent Owner's Response, filed February 6, 2018.
	483.	Inter Partes Review of US Patent No.8516185, Case No. IPR2017-00577, Patent Owner's Objections to Evidence, filed February 13, 2018.
	484.	Inter Partes Review of US Patent No.8516185, Case No. IPR2017-00577, Patent Owner's Motion to Exclude, filed February 28, 2018.
	485.	Inter Partes Review of US Patent No.8516185, Case No. IPR2017-00577, Patent Owner's Request for Oral Argument, filed February 28, 2018.
	486.	Inter Partes Review of US Patent No.8516185, Case No. IPR2017-00577, Petitioner's Opposition to Patent Owner's Motion to Exclude, filed March 14, 2018.
	487.	Inter Partes Review of US Patent No.8516185, Case No. IPR2017-00577, Patent Owner's Reply to Opposition to Motion to Exclude, filed March 21, 2018.
	488.	Inter Partes Review of US Patent No.8516185, Case No. IPR2017-00577, Hearing Transcript, filed April 6, 2018.
	489.	Inter Partes Review of US Patent No.8516185, Case No. IPR2017-00577, Termination Decision Document, filed July 7, 2018.
	490.	Inter Partes Review of U.S. Patent No. 7,532,537, Case No. IPR2017-00667, DECISION Institution of Inter Partes Review, filed July 21, 2017.
	491.	Inter Partes Review of US Patent No.7532537, Case No. IPR2017-00667, Petitioner's Objections to Evidence, filed November 14, 2017.
	492.	Inter Partes Review of US Patent No.7532537, Case No. IPR2017-00667, Petitioner's Supplemental Objections to Evidence, filed November 14, 2017.
	493.	Inter Partes Review of US Patent No.7532537, Case No. IPR2017-00667, Deposition of Carl Sechen, Ph.D. taken December 8, 2017, filed February 26, 2018.
	494.	Inter Partes Review of US Patent No.7532537, Case No. IPR2017-00667, Deposition of Carl Sechen, Ph.D. taken February 8, 2018., filed February 26, 2018.
	495.	Inter Partes Review of US Patent No.7532537, Case No. IPR2017-00667, Google, Inc. et al. v. Netlist, Inc., Appeal 2014-00777, filed February 26, 2018.

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	497.	Inter Partes Review of US Patent No.7532537, Case No. IPR2017-00667, Patent Owner's Objections to Evidence, filed March 5, 2018.
	498.	Inter Partes Review of US Patent No.7532537, Case No. IPR2017-00667, Exhibit 2007, Deposition of Harold S. Stone, filed March 19, 2018.
	499.	Inter Partes Review of US Patent No.7532537, Case No. IPR2017-00667, Patent Owner's Motion for Observations, filed March 19, 2018.
	500.	Inter Partes Review of US Patent No.7532537, Case No. IPR2017-00667, Patent Owner's Request for Oral Argument, filed March 19, 2018.
	501.	Inter Partes Review of US Patent No.7532537, Case No. IPR2017-00667, Petitioner's Motion to Exclude, filed March 19, 2018.
	502.	Inter Partes Review of US Patent No.7532537, Case No. IPR2017-00667, Patent Owner's Submission on Propriety of Petitioners Reply, filed March 20, 2018.
	503.	Inter Partes Review of US Patent No.7532537, Case No. IPR2017-00667, Petitioner's Response to Patent Owner's Submission on Propriety of Petitioner's Reply and Supplemental Stone Declaration 1, filed March 27, 2018.
	504.	Inter Partes Review of US Patent No.7532537, Case No. IPR2017-00667, Petitioner's Reply in Support of its Motion to Exclude Certain Inadmissible Testimony of Patent Owner's Expert Carl Sechen, filed April 2, 2018.
	505.	Inter Partes Review of US Patent No.7532537, Case No. IPR2017-00667, Petitioner's Updated Mandatory Notices, filed April 2, 2018.
	506.	Inter Partes Review of US Patent No.7532537, Case No. IPR2017-00667, Petitioner's Response to Patent Owner's Motion for Observations, filed April 2, 2018.
	507.	Inter Partes Review of US Patent No.7532537, Case No. IPR2017-00667, Patent Owner's Objection to Petitioner's Demonstratives, filed April 20, 2018.
	508.	Inter Partes Review of US Patent No.7532537, Case No. IPR2017-00667, Hearing Transcript, filed April 24, 2018.
	509.	Inter Partes Review of US Patent No.7532537, Case No. IPR2017-00667, Final Written Decision, filed July 18, 2018.
	510.	Inter Partes Review of U.S. Patent No. 7,532,537, Case No. IPR2017-00668, DECISION Institution of Inter Partes Review, filed July 21, 2017.
	511.	Inter Partes Review of US Patent No.7532537B2, Case No. IPR2017-00668, Petitioner's Objections to Evidence, filed November 14, 2017.
	512.	Inter Partes Review of US Patent No.7532537B2, Case No. IPR2017-00668, Notice of Deposition of Carl Sechen, filed January 30, 2018.

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	514.	Inter Partes Review of US Patent No.7532537B2, Case No. IPR2017-00668, Petitioner's Reply to Patent Owner's Response, filed February 26, 2018.
	515.	Inter Partes Review of US Patent No.7532537B2, Case No. IPR2017-00668, Patent Owner's Objections to Evidence, filed March 5, 2018.
	516.	Inter Partes Review of US Patent No.7532537B2, Case No. IPR2017-00668, Patent Owner's Motion for Observations, filed March 19, 2018.
	517.	Inter Partes Review of US Patent No.7532537B2, Case No. IPR2017-00668, Patent Owner's Request for Oral Argument, filed March 19, 2018.
	518.	Inter Partes Review of US Patent No.7532537B2, Case No. IPR2017-00668, Patent Owner's Submission on Propriety of Petitioner's Reply, filed March 20, 2018.
	519.	Inter Partes Review of US Patent No.7532537B2, Case No. IPR2017-00668, Petitioner's Response to Patent Owner's Submission on Propriety of Petitioner's Reply and Supplemental Stone Declaration, filed March 27, 2018.
	520.	Inter Partes Review of US Patent No.7532537B2, Case No. IPR2017-00668, Patent Owner's Opposition to Petitioner's Motion to Exclude, filed April 2, 2018.
	521.	Inter Partes Review of US Patent No.7532537B2, Case No. IPR2017-00668, Petitioner's Response to Patent Owner's Motion for Observations, filed April 2, 2018.
	522.	Inter Partes Review of US Patent No.7532537B2, Case No. IPR2017-00668, Petitioner's Reply in Support of its Motion to Exclude Certain Inadmissible Testimony of Patent Owner's Expert Carl Sechen, filed April 9, 2018.
	523.	Inter Partes Review of US Patent No.7532537B2, Case No. IPR2017-00668, Patent Owner's Objections to Petitioner's Demonstratives, filed April 20, 2018.
	524.	Inter Partes Review of US Patent No.7532537B2, Case No. IPR2017-00668, Hearing Transcript, filed April 24, 2018.
	525.	Inter Partes Review of US Patent No.7532537B2, Case No. IPR2017-00668, Final Written Decision, filed July 18, 2018.
	526.	Inter Partes Review of US Patent No.8756364, Case No. IPR2017.-00549, Xilinx CoolRunner XPLA3 CPLD product specification (2000), filed December 15, 2017.
	527.	Inter Partes Review of US Patent No.8756364, Case No. IPR2017.-00549, Xilinx Programmable Logic Design Quick Start Handbook (2004), filed December 15, 2017.
	528.	Inter Partes Review of US Patent No.8756364, Case No. IPR2017.-00549, Xilinx Xilinx TQFP package datasheet (2000), filed December 15, 2017.
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	530.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Exhibit 1022, Decision Denying Institution of Inter Partes Review, filed December 16, 2014
	531.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Exhibit 1023, Decision Denying Institution of Inter Partes Review, filed March 9, 2015
	532.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Exhibit 1024, Excepts from the Hearing in Certain Memory Modules and Components Thereof, and Products Containing Same, filed May 8, 2017.
	533.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Exhibit 1025, Complainant Netlist, Inc., Initial Post-Hearing Brief , filed May 30, 2017.
	534.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Exhibit 1026, Respondents' Post-Hearing Brief , filed May 30, 2017.
	535.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Declaration of Dr. Harold Stone, filed December 22, 2017.
	536.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Exhibit 1003: Declaration of Dr. Harold Stone, filed December 22, 2017.
	537.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Exhibit 1027, Demonstrative-Graphics-from-hynix-post-hearing-brief, filed December 22, 2017.
	538.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Exhibit 1028, Netlist-reply-post-hearing-brief, filed December 22, 2017.
	539.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Exhibit 1029, Respondent's Reply Post-Hearing Brief, filed December 22, 2017.
	540.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Exhibit 1030, High-Quality Versions of Demonstrative-Graphics-from-hynix-reply-post-hearing-brief, filed December 22, 2017.
	541.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Exhibit 1031, Institution of the '185 patent, filed December 22, 2017.
	542.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Exhibit 1032, Final Written Decision, Diablo Techs., Inc v. Netlist Inc., Paper No. 33, filed December 22, 2017.
	543.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Exhibit 1033, Decision, Netlist Inc., v. Diablo Techs., Inc., filed December 22, 2017.
	544.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Exhibit 1034, Netlist's Infringement Claim Chart of , filed December 22, 2017.

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	545.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Exhibit 1035, Stone, H.S. Microcomputer Interfacing, Reading, MA Addison Wesley, filed December 22, 2017.
	546.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Exhibit 1039, Intel E7525 Memory Controller Hub (MCH) Chipset Datasheet, filed December 22, 2017.
	547.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Exhibit 1040, Initial Determination, Certain Memory Modules and Components Thereof, and Products Containing Same, filed December 22, 2017.
	548.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Exhibit 1041, MEMORY-SYSTEMS-Cache-DRAM-Disk, Bruce Jacobs et al., filed December 22, 2017.
	549.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Exhibit 1042, Direct DRAM Datasheet, Bruce Jacobs et al., filed December 22, 2017.
	550.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Petition, filed December 22, 2017.
	551.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Exhibit 1011: JEDEC Standard DDR2 SDRAM Specification, JESD79-2B (January 2005), filed December 27, 2017.
	552.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Notice of Accorded Filing Date, filed January 10, 2018.
	553.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Patent Owner's Preliminary Response, filed April 10, 2018.
	554.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Granting Institution of Inter Partes Review, filed June 29, 2018.
	555.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Patent Owner's Objection to Petition Evidence, filed July 16, 2018.
	556.	Inter Partes Review of US Patent No. 9,606,907 B2, Case No. IPR2018-00362, and Case No. IPR2018-00363, EXHIBIT 3001, 'email from Mehran Arjomand,' filed July 30, 2018.
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	558.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Order 37 C.F.R. 42.5, filed August 2, 2018.

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	559.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Patent Owner's Supplemental Mandatory Notices, filed September 17, 2018.
	560.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Exhibit 2002: Declaration of R. Jacob Baker, Ph.D, P.E., filed October 19, 2018.
	561.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Exhibit 2003: Deposition of Harold S. Stone, Ph. D, October 5, 2018., filed October 19, 2018.
	562.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Exhibit 2004: United States International Trade Commission, Inv. No. 337-TA-1089, Joint List of Claim Terms for Construction and Proposed Constructions, filed October 19, 2018.
	563.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Exhibit 2005: United States International Trade Commission, Inv. No. 337-TA-1089, Order No. 17: Construing Terms of the Asserted Patents, filed October 19, 2018.
	564.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Patent Owner's Response, filed October 19, 2018.
	565.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, EXHIBITS 1043, 'Chart comparing text in Dr. Baker's declaration [Ex. 2002] with identical text in Patent Owner's Response [Paper No. 14],' filed February 11, 2019.
	566.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, EXHIBITS 1044, 'Deposition Transcript of R. Jacob Baker (Jan. 26, 2019.),' filed February 11, 2019.
	567.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, EXHIBITS 1045, 'Deposition Transcript of R. Jacob Baker (Jan. 12, 2018) in IPR2017-00577 concerning the parent to the '907 Patent,' filed February 11, 2019.
	568.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, EXHIBITS 1046, 'Final Office Action concerning U.S. Patent Application No. 15/470,856 (dated 7/27/18),' filed February 11, 2019.
	569.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, EXHIBITS 1047, 'Certified translation of the Examination Decision issued by the State Intellectual Property Office of the P.R.C. (dated 5/30/18),' filed February 11, 2019.
	570.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, EXHIBITS 1048, 'Certified translation of the Preliminary Opinion issued by the German Patent and Trademark Office (dated 1/8/19),' filed February 11, 2019.
	571.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Petitioners' Reply to Patent Owner's Response, filed February 11, 2019.
	572.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Patent Owner Motion To Exclude, filed February 19, 2019.

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	573.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Patent Owner Objections To Reply Evidence, filed February 19, 2019.
	574.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Patent Owner Request For Oral Argument, filed February 19, 2019.
	575.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Petitioners' Request for Oral Argument, filed February 19, 2019.
	576.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Corrected Petitioners' Reply to Patent Owner's Response, filed February 20, 2019.
	577.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, EXHIBITS 3002, 'Patent Owner's Request for Sur Reply,' filed March 1, 2019.
	578.	Inter Partes Review of US Patent No.9606907, Case No. IPR2018-00362, Petitioners' Opposition to Patent Owner's Motion to Exclude, filed March 5, 2019.
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	863.	U.S. District Court Northern District of California, Case No. 4:13-CV-05889-YGR, Netlist, Inc. v. Smart Storage Systems, Inc., and Diablo Technologies, Inc., Diablo Technologies, Inc.'s Invalidity Contentions, dated June 6, 2014.
	864.	U.S. District Court Northern District of California, Case No. 4:13-CV-05889-YGR, Netlist, Inc. v. Smart Storage Systems, Inc., and Diablo Technologies, Inc., Exhibits D-1 to D6 to "Diablo Technologies, Inc.'s Invalidity Contentions," dated June 6, 2014.
	865.	U.S. District Court Central District of California, Case No. CV09 06900, Netlist, Inc. vs. Inphi Corporation, Complaint For Patent Infringement, filed Sep. 22, 2009 in 10 pages. cited by other.
	866.	U.S. District Court Central District of California, Case No. CV09 06900, Netlist, Inc. vs. INPHI Corporation, Defendant Inphi Corporation's Answer to Plaintiff's Complaint for Patent Infringement, filed Nov. 12, 2009 in 6 pages. cited by other.
	867.	U.S. District Court Central District of California, Case No. CV09 06900, Netlist, Inc. vs. INPHI Corporation, Defendant Inphi Corporation's Answer to Plaintiff's First Amended Complaint for Patent Infringement, filed Feb. 11, 2010 in 9 pages. cited by other.
	868.	U.S. District Court Central District of California, Case No. CV09 06900, Netlist, Inc. vs. INPHI Corporation, Defendant Inphi Corporation's Notice of Motion and Motion for Stay Pending Reexaminations and Interference Proceeding Regarding the Patents-In-Suit; Memorandum of Points and Authorities in Support Thereof, filed Apr. 21, 2010 in 28 pages. cited by other.
	869.	U.S. District Court Central District of California, Case No. CV09 06900, Netlist, Inc. vs. INPHI Corporation, Plaintiff Netlist Inc's Opposition to Defendant Inphi Corporation's Motion for Stay Pending Reexaminations and Interference Proceedings Regarding the Patents-In-Suit, filed May 3, 2010 in 23 pages. cited by other.
	870.	U.S. District Court Central District of California, Case No. CV09 06900, Netlist, Inc. vs. Inphi Corporation, Plaintiff Netlist, Inc's First Amended Complaint For Patent Infringement, filed Dec. 23, 2009 in 8 pages. cited by other.
	871.	US District Court Civil Docket; Netlist Inc. v. Google Inc.; 4:09cv5718; Date filed Dec. 4, 2009. In 10 pages. cited by other.
	872.	U.S. Court of Appeals for the Federal Circuit, Decision on Appeal for Reexamination Control No. 95/001,381, filed November 13, 2015, 14 pages
	873.	U.S. District Court Northern District of California, Case No. 4:13-CV-05889-YGR, Netlist, Inc. v. Smart Storage Systems, Inc., and Diablo Technologies, Inc., Corrected Joint Claim

Examiner Signature	/VANTHU T NGUYEN/	Date Considered	08/27/2022

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /VTN/

INFORMATION DISCLOSURE STATEMENT BY APPLICANT Substitute for Form 1449-PTO				*Electronically filed December 11, 2021*	
				Application Number	*17/403,832*
				Filing Date	*August 16, 2021*
				First Named Inventor	*Jefferey C. Solomon*
				Art Unit	*2139*
				Examiner Name	*TBD*
Sheet	47	of	47	Attorney Docket Number	*NL023-02US02*

	874.	Construction and Prehearing Statement Pursuant to Patent L.R. 4-3, including Exhibit A, filed August 27, 2014, 28 pages.
	875.	Notice of Allowance, U.S. Pat. App. No. 12/504,131, February 12, 2013, 52 pages
	876.	Non-Final Office Action, U.S. Pat. App. No. 12/761,179, September 13, 2012, 20 pages
	877.	Response to non-final office action dated September 13, 2012 for U.S. Patent Application No. 12/761,179, filed March 13, 2013, 16 pages
	878.	Notice of Allowance, U.S. Pat. App. No. 12/761,179, July 11, 2013, 37 pages
	879.	Non-Final Office Action, dated January 2, 2014, for U.S. Pat. App. No. 13/287,042 filed November 1, 2011, 42 pages
	880.	Response to Non-Final Office Action dated January 2, 2014 for U.S. Pat. App. No. 13/287,042, filed April 2, 2014, 12 pages
	881.	Non-final office action, U.S. Patent Application No. 13/288,850, October 14, 2013, 24 pages
	882.	Response to non-final office action dated October 14, 2013 for U.S. Patent Application No. 13/288,850, filed January 14, 2014, 15 pages
	883.	Non-final office action, U.S. Patent Application No. 13/411,344, December 31, 2013, 28 pages
	884.	Response to non-final office action dated 12/31/2013 for U.S. Patent Application No. 13/411,344, filed March 31, 2014, 12 pages
	885.	Non-Final Office Action, U.S. Pat. App. No. 13/412,243, January 2, 2014, 20 pages
	886.	Non-final office action, U.S. Patent Application No. 13/473,413, November 17, 2011, 46 pages
	887.	Office Action mailed April 2, 2014, for Japanese Patent Application No. JP 2012-520662 and English translation thereof, 7 pages
	888.	Written Opinion for International Application No. PCT/US2010/040826, date of mailing October 24, 2011 (NETL.048VPC) in 7 pages.
	889.	International Preliminary Report on Patentability for International Application No. PCT/US2010/040826, date of mailing November 28, 2011 (NETL.048VPC) in 34 pages.
	890.	International Search Report and Written Opinion for Related Application No. PCT/US2010/040826, mailed on September 27, 2010, in 15 pages.
	891.	International Search Report and Written Opinion, PCT Application No. PCT/US2011/059209, January 31, 2013

Examiner Signature	/VANTHU T NGUYEN/	Date Considered	08/27/2022

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Electronically filed December 11, 2021

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of:	Jefferey C. SOLOMON	Confirmation No.:	3549
Serial No.:	17/403,832	Group Art Unit:	2139
Filed:	August 16, 2021	Examiner:	TBA
For:	*MEMORY MODULE WITH DATA BUFFERING*	Attorney Docket No.:	NL023-02US02

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In accordance with the duty of disclosure provisions of 37 C.F.R. §1.56, there is hereby provided certain information which the Examiner may consider material to the examination of the subject U.S. patent application. It is requested that the Examiner make this information of record if it is deemed material to the examination of the application.

1. Enclosures accompanying this Information Disclosure Statement are:

1a. ☒ A list of all patents, publications, applications, or other information submitted for consideration by the office.

1b. A legible copy of:

☐ Each foreign patent;

☐ Each publication or that portion which caused it to be listed on the PTO-1449;

☐ For each cited pending U.S. application, the application specification including the claims, and any drawing of the application, or portion of the application which caused it to be listed on the PTO-1449 including any claims directed to that portion;

☐ all other information or portion which caused it to be listed on the PTO-1449.

1c. ☐ An English language copy of search report(s) from a counterpart foreign application or PCT International Search Report.

1d. ☐ Explanations of relevancy (ATTACHMENT 1(d), hereto) or English language abstracts of the non-English language publications.

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2. ☒ This Information Disclosure Statement is filed under 37 C.F.R. §1.97(b):

☐ Within three months of the filing date of a national application other than a continued prosecution application under §1.53(d);

☐ Within three months of the date of entry of the national stage as set forth in §1.491 in an international application;

☒ Before the mailing of the first Office action on the merits;

☐ Before the mailing of a first Office action after the filing of a request for continued examination under §1.114.

3. ☐ This Information Disclosure Statement is filed under 37 C.F.R. §1.97(c) after the period specified in 37 C.F.R. §1.97(b), but before the mailing date of any of a final action under 37 C.F.R. §1.113, a notice of allowance under 37 C.F.R. §1.311 or an action that otherwise closes prosecution in the application.

(Check either Item 3a, 3b, 3c or 3d)

3a. ☐ The Certification Statement in Item 5 below is applicable. Accordingly, no fee is required.

3b. ☐ The $260 (large entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Deposit Account No. 60-3916 (order no. NL057-10US01).

3c. ☐ The $130 (small entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Deposit Account No. 60-3916 (order no. NL057-10US01).

3d. ☐ The $120 (micro entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Deposit Account No. 60-3916 (order no. NL057-10US01).

(Items 3b or 3c to be checked if any reference known for more than 3 months)

4. ☐ This Information Disclosure Statement is filed under 37 C.F.R. §1.97(d) after the period specified in 37 C.F.R. §1.97(c), but on or before the date of payment of the issue fee.

(Check Item 4a, and 4b, 4c or 4d)

4a. ☐ The Certification Statement in Item 5 below is applicable.

4b. ☐ The $260 (large entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Deposit Account No. 60-3916 (order no. NL057-10US01).

4c. ☐ The $130 (small entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Deposit Account No. 60-3916 (order no. NL057-10US01).

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4d. ☐ The $120 (micro entity) fee set forth in 37 C.F.R. §1.17(p) in accordance with 37 C.F.R. §1.97(c) is to be charged to Deposit Account No. 60-3916 (order no. NL057-10US01).

5. ☐ Certification Statement (applicable if Item 3a or Item 4a is checked)

(Check either Item 5a, 5b, 5c or 5d)

5a. ☐ In accordance with 37 C.F.R. §1.97(e)(1), it is certified that each item of information contained in this information disclosure statement was first cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement.

5b. ☐ In accordance with 37 C.F.R. §1.97(e)(2), it is certified that no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 C.F.R. §1.56(c) more than three months prior to the filing of this information disclosure statement.

5c. ☐ Each item of information contained in this information disclosure statement was cited in a communication from a foreign patent office in a counterpart application, and the communication was not **received** by any individual designated in 37 C.F.R. §1.56(c) more than thirty days prior to the filing of this information disclosure statement.

5d. ☐ Pursuant to 37 C.F.R. §1.704(d), each item of information contained in this information disclosure statement was cited in a communication from a foreign patent office in a counterpart application, and the communication was not **received** by any individual designated in 37 C.F.R. §1.56(c) more than thirty days prior to the filing of this information disclosure statement.

6. ☒ Copies of each cited U.S. patent and each U.S. patent application publication are not enclosed pursuant to the USPTO OG Notice dated 05 August 2003 waiving the requirement under 37 C.F.R. 1.98(a)(2)(i) for U.S. patent applications filed after June 30, 2003.

7. ☒ This application is a continuation application under 37 C.F.R. §1.53(b) or (d).

(Check appropriate Items 7a, 7b and/or 7c)

7a. ☐ A Petition to Withdraw from issue under 37 C.F.R. §1.313(b)(5) is concurrently filed herewith.

7b. ☒ Copies of publications listed on Form PTO-1449 from prior application Serial Nos. **15/857,519**, filed on **December 28, 2017**, **14/715,486**, filed on **May 18, 2015**; **13/971,231** , filed on **August 20, 2013**; **13/287,081** , filed on **November 1, 2011**; **13/032,470** , filed on **February 22, 2011**; **12/955,711** , filed on **November 29, 2010**; **12/629,827** , filed on **December 2, 2009**; **12/408,652** , filed on **March 20, 2009**; **11/335,875** , filed on **January 19, 2006**; **11/173,175** , filed on **July 1, 2005**; **11/075,395** , filed on **March 7, 2005**, of which this application claims priority under

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35 U.S.C. §120, are not being submitted pursuant to 37 C.F.R. §1.98(d).

7c. ☐ Copies of the publications listed on the attached Form PTO-1449 that were not previously cited in prior application Serial No. , filed on , are provided herewith.

8. ☐ This is a Supplemental Information Disclosure Statement. (Check Item 8a)

8a. ☐ This Supplemental Information Disclosure Statement under 37 C.F.R. §1.97(f) supplements the Information Disclosure Statement filed on . A bona fide attempt was made to comply with 37 C.F.R. §1.98, but inadvertent omissions were made. These omissions have been corrected herein. Accordingly, additional time is requested so that this Supplemental Information Disclosure Statement can be considered as if properly filed on .

9. ☐ In accordance with 37 C.F.R. §1.98, a concise explanation of what is presently understood to be the relevance of each non-English language publication is:

(Check Item 9a, 9b, or 9c)

9a. ☐ satisfied because all non-English language publications were cited on the enclosed English language copy of the PCT International Search Report or the search report from a counterpart foreign application indicating the degree of relevance found by the foreign office.

9b. ☐ set forth in the application.

9c. ☐ enclosed as an attachment hereto.

10. ☒ The Commissioner is authorized to charge any additional fee required or credit any overpayment for this Information Disclosure Statement and/or Petition to Deposit Account No. 60-3916 (order no. NL023-02US02).

11. ☒ No admission is made that the information cited in this Statement is, or is considered to be, material to patentability nor a representation that a search has been made (other than a search report of a foreign counterpart application or PCT International Search Report if submitted herewith). 37 C.F.R. §§1.97(g) and (h).

Respectfully submitted,

Date: December 11, 2021

/Jamie J. Zheng/ 51,167
Jamie J. Zheng (Reg. No.)
Customer No. 79141

/VANTHU T NGUYEN/ 08/27/2022

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