

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.,
Petitioner,

v.

NETLIST, INC.,
Patent Owner.

Case No. IPR2023-00454
Patent No. 11,093,417

PATENT OWNER PRELIMINARY RESPONSE

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EXHIBIT LIST

Exhibit No.	Document
EX2001	Crisp, R., “Direct Rambus Technology: The New Main Memory Standard,” <i>IEEE Micro</i> , pp. 18-28 (1997)
EX2002	Datasheet for Samsung’s RIMM MR16R1624 (Wolfe Deposition Exhibit 2100)
EX2003	Deposition Transcript of Dr. Andrew Wolfe from IPR2022-00615
EX2004	Samsung datasheet on Rambus Direct RDRAM (Dec. 2001)
EX2005	Deposition Transcript of SungJoo Park in <i>Netlist, Inc. v. Samsung Electronics Co., Ltd.</i> , 2:21-cv-00463-JRG (E.D. Tex. November 23, 2022) (excerpt)
EX2006	Ex. 7 to Park Depo
EX2007	<i>Frequently Asked Questions</i> , What is the difference between a "bank" and a "rank?", Micron, https://web.archive.org/web/20141231144416/https://www.micron.com/support/faqs (last accessed Mar. 7, 2023).
EX2008	Reserved
EX2009	“XDR Architecture “ by Rambus (last modified December 2005), downloaded from https://web.archive.org/web/20110724044154/http://www.rambus.com/assets/documents/products/dl_0161_v0_8.pdf
EX2010	IDT, “DDR4 LRDIMMs Unprecedented Memory Bandwidth on Samsung DDR4 LRDIMM Enabled by IDT’s Register and Data Buffer,” downloaded from https://www.renesas.com/us/en/document/whp/ddr4-lrdimms-both-memory-capacity-and-speed

EX2011	“HyperCloud HCDIMM: Scaling the High Density Memory Cliff,” July 14, 2012, downloaded from https://web.archive.org/web/20120915083048/http://www.netlist.com/media/blog/hypercloud-memory-scaling-the-high-density-memory-cliff/
EX2012	<i>What is a Memory Rank</i> , Crucial: Micron, https://www.crucial.com/support/articles-faq-memory/what-is-a-memory-rank (last accessed Mar. 7, 2023)
EX2013	<i>Lecture 15: DRAM Main Memory Systems</i> , University of Utah, https://my.eng.utah.edu/~cs6810/pres/11-6810-15.pdf
EX2114	“Configuring and using DDR3 memory with HP ProLiant Gen8 Servers: Best Practice Guidelines for ProLiant Servers with Intel Xeon Processors” by HP, downloaded from https://web.archive.org/web/20121023195754/http://h20000.www2.hp.com/bc/docs/support/SupportManual/c03293145/c03293145.pdf
EX2015	Ganesh, B. et al., <i>Fully-Buffered DIMM Memory Architectures: Understanding Mechanisms, Overheads and Scaling</i> , HPCA (2007)
EX2116	Datasheet for Micron DDR2 SDRAM FBDIMM MT36HTF51272FD
EX2017	U.S. Patent No. 7,356,639 (“Perego-639”)
EX2018	Redline Comparison of EX1035 (U.S. Patent No. 7,363,422 to Perego) With Related U.S. Patent No. 7,356,639
EX2019	US District Court – Judicial Caseload Profile (as of December 31, 2022)
EX2020	JESD79-2B
EX2021	Amended Docket Control Order in <i>Netlist, Inc. v. Samsung Electronics Co. Ltd.</i> , 2:22-cv-00293-JRG (E.D. Tex. Feb. 1, 2023)

EX2022	Cover pleading of Samsung's invalidity contentions in <i>Netlist, Inc. v. Samsung Electronics Co. Ltd.</i> , 2:22-cv-00293-JRG (E.D. Tex. April 13, 2023)
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I. INTRODUCTION¹

Petitioner challenges all claims of U.S. Patent No. 11,093,417 based on Perego, in combination with JESD79-2 and optionally with also Ellsberry or Halbert. Perego is assigned to Rambus and features a memory system having a completely different design than the JEDEC-style memory architecture. *See* EX1069, pp. 11-16 (discussing the differences between JEDEC-style memory and Rambus memory); EX2001 (discussing the differences between Direct Rambus memory technology and conventional JEDEC-style architecture). Notably, as Petitioner’s own evidence observes, Rambus memory technology does not have a “chip-select network.” EX1069, p.12. Instead, Perego operates on an individual device basis, and its memory devices are thus not organized into ranks, each consisting of memory devices that “act together in response to command signals, including chip select signals, to read or write the full bit-width of [a] memory module.” Pet. 26; *see* EX2001, 23 (conventional DRAMs “are frequently ganged together in parallel to provide the necessary aggregate bandwidth”; in contrast, “[b]ecause a Direct RDRAM spans the entire channel, the CPU accesses each RDRAM independently”); EX2009, 16 (noting the need to modify memory controller to address a single device). Accordingly, Perego does not mention “input chip-select signals” or

¹ All emphases are added unless otherwise noted.

“registered chip-select signals.” *See* EX1071 *generally*.

Despite the fundamentally different memory architecture between Perego and JEDEC-style memory systems, Petitioner argues that “[a] POSITA would have ... been motivated to implement Perego’s memory modules in a registered DIMM format with DDR memory devices that fits into DIMM connectors and uses DIMM module input signals, according to JEDEC standards, including JESD21-C and JESD79-2.” Pet. 32. As a preliminary matter, Petitioner does not explain why a POSITA would have incurred cost to modify Perego’s memory modules into structurally distinct JEDEC-compliant RDIMMs that were readily available in the market. Petitioner also does not address the fact that its proposed modification would require changing the fundamental operating principles of Perego—including the use of point-to-point topology and the configurable width buffers, something that a POSITA would not do.

Moreover, even though Perego’s data buffer, with its ability to translate between different signaling protocols, can work with JEDEC-style SDRAMs, nothing in Perego or other references disclose or suggest that the data buffer would receive a plurality of input chip-select signals, or output a plurality of registered chip-select signals, one of which having an active signal value and one or more having a non-active signal value, as required by elements 1.c.2-1.c.3.

Instead, the evidence of record suggests otherwise. Ellsberry, for example,

suggests that read/write commands can be sent to selected memory devices while NOP commands can be sent to non-selected memory devices. EX1073, [0033]. According to JESD79-2, read/write and NOP commands all have chip-select signals set to active low. *See* EX1064, p.49. Another reference, Halbert, teaches that both ranks of memory devices participate in each read/write operation, such that if Halbert involves JEDEC-compliant SDRAMs, these SDRAMs would also each receive chip-select signals with an active signal value, contrary to what is required by the claims (*e.g.*, 1.c.3). *See* EX1078, Figs. 5-6; EX1064, p.49.

In addition to not having shown a likelihood of success with respect to limitations concerning chip-select signals and the related “rank” concept, Petitioner has also not overcome the examiner’s prior finding that the art of record—which included Halbert, Ellsberry and a family member of Perego—did not disclose the limitations related to CAS latency of the memory module. EX1002, p.229.

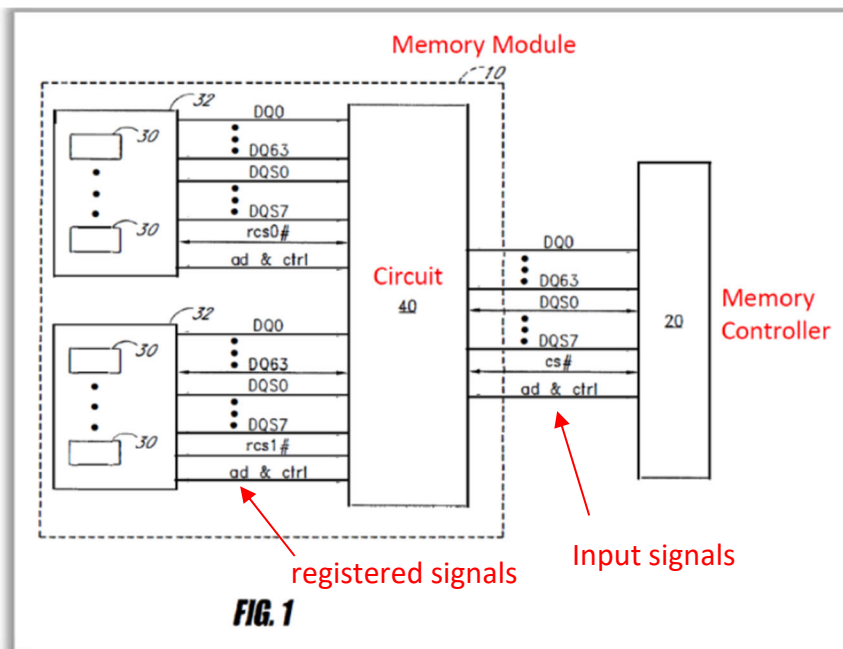
Consequently, for reasons stated here and below, the Board should deny institution.

II. OVERVIEW OF THE ’417 PATENT

The ’417 patent, titled “Memory Module With Data Buffering,” relates to a memory module that effects “registered transfers of N-bit wide data signals with [a] memory read or write command between [a] N-bit wide memory bus and [] memory devices in response to [] data buffer control signals and in accordance with an overall

CAS latency of the memory module, which is greater than an actual operational CAS latency of the memory devices.” EX1001, field (54), abstract. The data buffer control signals are outputted by a logic on the module, which is “configurable to receive a set of input address and control signals associated with [the] read or write memory command and output registered address and control signals [in addition to] data buffer control signals.” *Id.*

Figure 1, reproduced below with annotation, illustrates such a memory module. EX1001, 5:65-67



As shown in Figure 1, “[t]he memory module 10 is connectable to a memory controller 20 of a computer system (not shown).” *Id.*, 5:67-6:1. In the Figure 1 example, the memory module 10 includes multiple memory devices 30 arranged in

two ranks 32, each rank having multiple memory devices 30. *See* Fig. 1, 7:11-13. Other number of ranks are possible. *Id.*, 7:13-16.

The memory module 10 also includes a circuit 40 electrically coupled to the memory devices 30 and to the memory controller 20 of the computer system. *Id.*, 6:4-7. The circuit 40 includes a logic that translates between a system memory domain of the computer system and a physical memory domain of the memory module 10. *Id.*, 6:9-12. This may be achieved by the logic receiving input data signals, chip-select signals and other control/address signals from the memory controller 20, and outputting corresponding registered data signals, registered chip-select signals and other registered control/address signals to the memory devices 30. *See* EX1001, Fig. 1, 21:66-22:35; *see also id.*, 18:37-19:9 (showing how the logic translates the input control/address and chip-select signals).

The memory module also includes an SPD device 240 that can report the CAS latency (CL) of the memory module to the memory controller 20. *Id.*, 22:36-38. The reported CL value of the memory module may be “one more cycle than does the actual operational CL of the memory array,” for example to account for the fact that in some embodiments, “data transfers between the memory controller 20 and the memory module are registered for one additional clock cycle by the circuit 40.” *Id.*, 22:38-43. The extra cycle time provides for time needed by a data buffer to perform address decoding, and/or data path multiplexing/demultiplexing, for

example. *Id.*, 22:46-56. The extra latency time, however, is optional. *Id.*, 22:60-61.

III. SKILL LEVEL OF A POSITA

For purposes of this preliminary response only, Patent Owner applies the skill level proposed by Petitioner.

IV. CLAIM CONSTRUCTION

Netlist disagrees with Petitioner's proposed construction for "rank," in particular, that a rank could include a single memory device. *Contra* Pet. 26. Netlist notes, however, the arguments made herein are independent of that dispute. As such, the Board need not construe the term at this stage.

V. ASSERTED PRIOR ART

A. Perego

Perego discloses a memory system with point-to-point topology including a "memory module having a buffer device (e.g., having a configurable width) isolating data, control, and address signals of the memory devices from the connector interface." EX1071, 4:38-45; Abstract; 5:35-55; 8:10-17, 8:20-26. Buffer device 350 is coupled to memory controller interface 375, which includes a "plurality of memory subsystem ports 378a-378n." *Id.*, 4:63-5:15. Perego's configurable width buffer device is connected to ports 378a-378n of the memory controller via a point-to-point links 320. *Id.*, 5:12-21. Perego repeatedly and consistently emphasizes the

benefits of its point-to-point architecture over a conventional JEDEC-style bus. *See, e.g.*, 3:47-56, 4:65-5:1, 5:6-15, 5:32-55, 6:15-19, 13:49-59, 21:46-50, Figs. 3A/3B, Fig. 5A.

Perego's buffer communicates to the plurality of memory devices on the buffered module via channels 370. *Id.*, 5:4-6, 6:13-24, 7:65-67; Fig. 3B. But in contrast to a conventional registered DIMM ("RDIMM"), in Perego's architecture, control/address information is transmitted to the module via packets and multiplexed with data in order to be transmitted via the point-to-point links. *Id.* 13:49-59 (configurable width interface 590 may "extract the address and control information from the data"). In the example of a "normal memory read operation," Perego explains that "device 350 receives control, and address *information* from controller 310 via point-to-point link 320a, and *in response, transmits corresponding signals to one or more, or all of memory devices 360* via channels 370," *id.*, 6:12-19, but the same paragraph contrasts this approach with that of the conventional RDIMM buffer. *See id.*, 6:27-30 ("By way of comparison, buffers disposed on the conventional DIMM module in U.S. Pat. No. 5,513,135 are employed to buffer or register control signals such as RAS, and CAS, etc., and address signals."); Pet. Pet. 32-33 (Petitioner arguing that the '135 patent (EX1081) is an example of a JEDEC-compliant RDIMM that Perego allegedly would make upgradeable with its invention).

Perego discloses that regardless of the module width, “[a]module's full set of data stored on the associated memory devices is available[.]” EX1071, 7:54-56. “With wider interface widths, different subsets of memory devices and memory cells may be accessed through different sets of interface connections. With narrower data or interface widths, the different subsets of memory devices and memory cells are accessed through a common set of interface connections.” *Id.*, 7:56-62. Address bits are used to specify the memory devices to be accessed at narrower interface width. *Id.*, 7:62-64

Perego also teaches that power is saved by powering only selected memory devices. *Id.*, 20:51-57. Accordingly, for example, in Figure 4B, “two channels 415c and 415d may transfer information simultaneously and the memory devices on the other two channels 415a and 415b remain in a ready or standby state until called upon to perform memory access operations.” *Id.*, 21:16-20. Because devices not in use are not powered or activated (20:51-57), no translated commands need to be (or can be) sent to those dormant devices such that they “remain in a ready or standby state until called upon to perform memory access operations” (21:16-20).

B. Ellsberry

Ellsberry discloses a memory module architecture, as depicted in Figure 2, that “permits transparent bank switching of memory devices.” EX1037, [0001]. As depicted in Figure 2, Control ASIC 204 (red) “receives memory addresses and

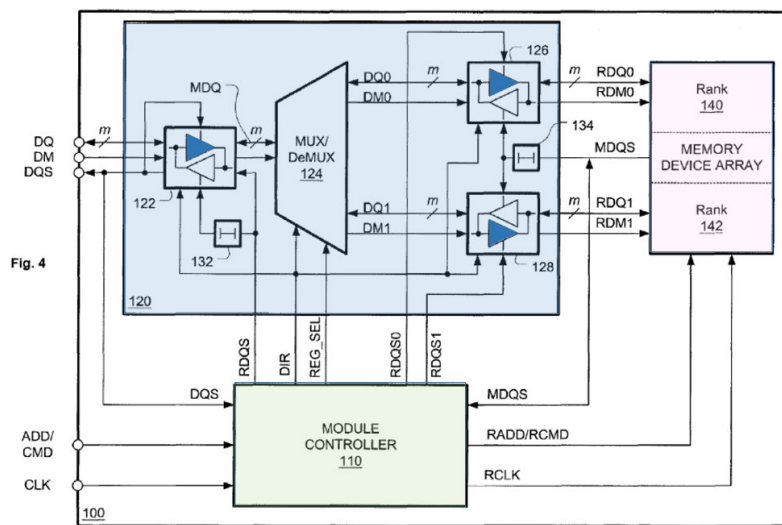
commands over the DIMM interface 202” from the system memory controller, and switch ASICs 206 and 208 (purple) “receive data information from the DIMM interface 202 via data buses 230 & 232, respectively.” *Id.*, [0028]-[0029]. Each switch ASIC is connected to a number of memory banks (e.g., Bank 0-3 below). *Id.* Switch ASICs 206 and 208 receive respectively data byte group N and data byte group 0, provided “simultaneously” by the DIMM interface 202. *Id.*, [0030], Fig. 2 (depicting at least two data groups); Fig. 5 (depicting nine data groups).

Control ASIC 204 sends command signals to memory devices in different memory banks via bus 220. *Id.*, [0030]. This includes mode register set (MSR) commands that sets the CAS latency (CL). *See*, Fig. 8A for commands. MSR is not sent to the ASIC switches. *See* EX1073 *generally*.

Each ASIC switch includes two data ports, Port A and Port B, coupled respectively to data busses 234 and 236. Ellsberry discloses that in column addressing scheme, memory devices coupled to both ports A and B are read but only the data from the target memory device is multiplexed onto the DIMM interface. EX1073, [0033]. In contrast, in row addressing mode, read command is sent to the targeted memory devices and NOP is sent to the non-targeted memory devices. *Id.* In either case, however, to the extent JEDEC-compliant chip select signals are sent to the memory devices, the chip select signals will assume an active signal value (“L”). *See, e.g.*, EX1064, p.49 (“L” for CS for read/write and NOP).

C. Halbert

Halbert describes “a group of buffered memory module architectures.” EX1078, 3:42-43. Halbert’s Figure 4 configuration relied on by Petitioner includes “a module controller 110 [green]; a data interface circuit 120 [blue]; and a memory device array 140/142 [mauve].” *Id.*, 4:36-39.



In the above configuration, “[d]ata interface circuit 120 provides for m-bit-wide data transfers between the module and the system memory data bus and for $R \times m$ -bit-wide data transfers between the interface circuit and the memory device array.” *Id.*, 4:49-52. In Figure 4, R equals 2 for the two ranks 140 and 142. *Id.*, 4:52-55. In Halbert, “**multiple ranks ...will perform memory operations** with the interface circuit **concurrently**.” *Id.*, 4:57-59.

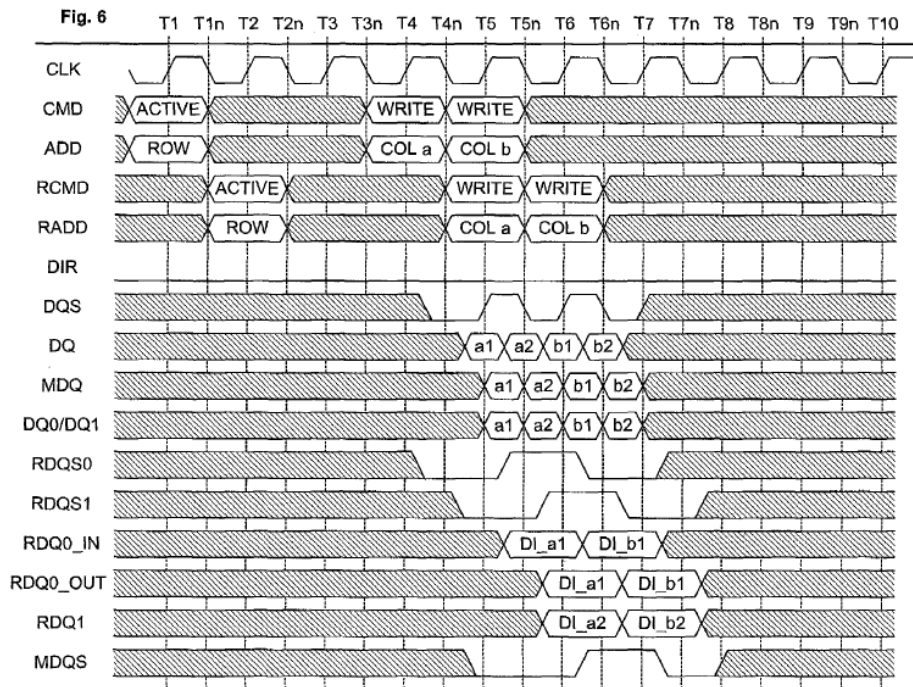
Halbert’s data interface circuit 120 in Figure 4 has one bi-directional buffer 122 that can receive (for write operations) or drive (for read operations) m-bit-wide

data signals DQ on the system memory data bus. *Id.*, 4:60-64. Data buffer 122 can also drive a data strobe signal DQS onto the memory data bus for read operations. *Id.*, 5:4-5.

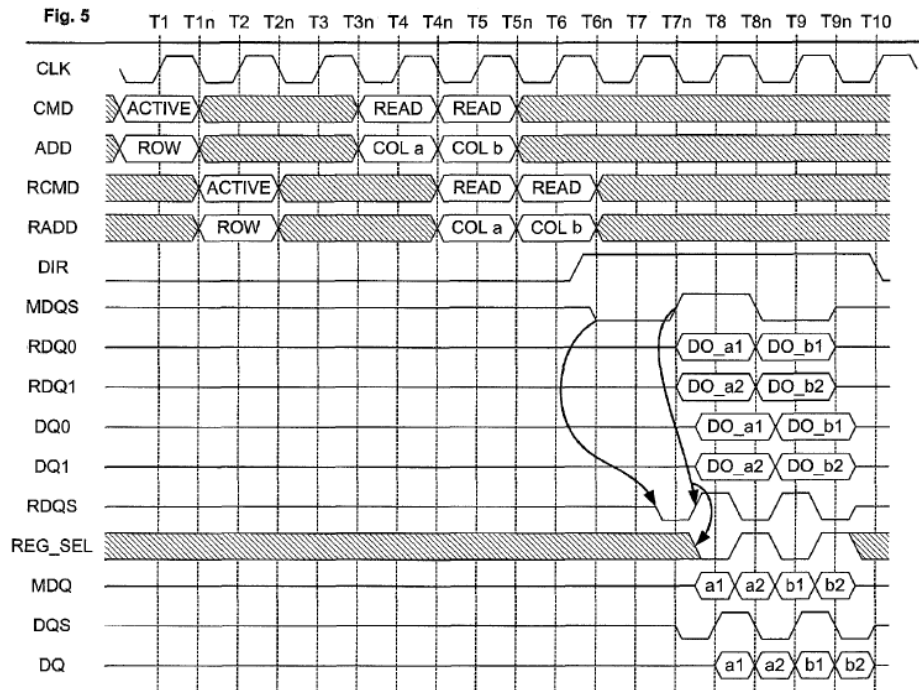
Halbert's data interface circuit 120 further includes two bi-directional data registers 126 and 128 that each receive from (for read) or drive to (for write) a corresponding memory rank (140 and 142 respectively) m-bit-wide words (*e.g.*, RDQ0 or RDQ1), "over a dedicated point-to-point module data bus." *Id.*, 5:6-11. Registers 126 and 128 can also drive registered data-mask signals (*e.g.*, RDM0 or RDM1) to the corresponding memory rank. *Id.*, 5:11-14.

Between the buffer 122 and registers 126 and 128 is a MUX/DeMux 124, which multiplexes data signals DQ0 or DQ1 received from registers 126 and 128 in read operations, and de-multiplexes data signals MDQ from buffer 122 into DQ0 or DQ1 for delivery to registers 126 and 128 respectively in write operations. *Id.*, 5:15-22. In a write operation, transitions of registered strobing signals RDQS0 and RDQS1 cause registers 126 and 128 to latch m-bits of DQ0 and DQ1 respectively in consecutive clock cycles. *Id.*, 5:54-61. "Both register contents are then written to memory device array 140/142 **during a single device write cycle**" in response to MDQS signaled to memory device array. *Id.*, 5:61-65. Consistent with the above description, Halbert presents a "timing diagram for two consecutive write operations" in Figure 6. As seen from Figure 6, write data associated with each

WRITE command is broken into two subsets, *e.g.*, a1 and a2, and b1 and b2. The first subset (*e.g.*, a1 and b1) is latched into register 126 and written to rank 140 while the second subset (*e.g.*, a2 and b2) is latched into register 128 and written to rank 142.



Similarly in a read operation, 2m bits of data are read into the data registers per read cycle, and are then driven m-bits at a time through MUX 124. *Id.*, 5:40-48. Then, in response to register data strobe RDQS, “buffer 122 latches data from MUX 124 and drives that data onto the memory data bus.” *Id.*, 5:48-50. A timing diagram for a read operation is shown in Figure 5. *Id.*, 5:66-6:65 (describing signals and timing for read operations). As in a write operation, datasets for each read operation is also broken into two subsets and read concurrently from ranks 140 and 142.



VI. PETITIONER HAS NOT SHOWN A REASONABLE LIKELIHOOD OF SUCCESS TO PREVAIL UNDER GROUND 1

A. Perego does not disclose or suggest “a plurality of input chip select signals”

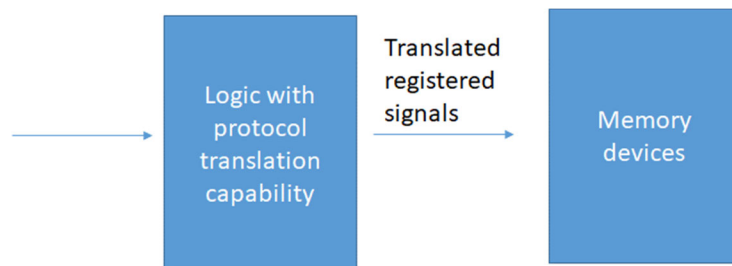
1. Neither Perego nor JESD79-2 disclose input chip-select signals to a data buffer

It is undisputed that Perego does not mention “chip-select signal(s)” or “chip-select line(s).” *See* EX1071 *generally*; *see also* EX2003, 84:14-19 (“Q. And where does the word ‘chip select signal’ appear in Perego? A. In one place their individual device. Let me see. I don't think there's an explicit description of a chip select line....”).

Petitioner argues, however, because JEDEC-compliant DRAM devices would receive chip-select signals and DDR2 SDRAMs are compatible with Perego's

invention, Perego discloses a set of input address and control signals that include “a plurality of input chip select signals” to be received by a logic device on a DRAM module. Pet. 51-54; xiii (elements 1.c.1-1.c.2). Specifically, Petitioner points to JESD79-2 to argue that the limitation 1.c.2 is met. *Id.* Yet, Perego never describes the types of memory systems suitable for its invention as JEDEC-compliant. *E.g.*, EX1071, 10:54-67 (mentioning Rambus DRAM or DDR2 DRAM devices and SDRAM devices, but not describing them as JEDEC compliant).

Moreover, even if the devices were JEDEC-compliant, the cited JESD79-2 specification, entitled the “DDR2 SDRAM Specification,” describes the input/output to SDRAM devices, and not the input/output to a logic device coupled between a memory controller and memory devices. *See* EX1064, cover. Indeed, Perego discloses that it can achieve flexibility and upgradeability “by employing buffer device 405 to translate protocols employed by controller 310 to the protocol utilized in a particular memory device implementation.” EX1071, 10:63-67; *see* illustration below. In other words, the type of input signals to a control logic differs from the output signals.



This is particularly the case for Perego, which is a patent assigned to Rambus. *See* EX1017, cover. Petitioner's own evidence contrasts Rambus memory technology and JEDEC-style memory technology. EX1069, pp.11-16; *see also* EX2001, p.19, Fig. 2 & p.20 (unlike buses in traditional memory modules that have different loading delays, Rambus Direct memory organization has signal wires with equal loading and a fan-out architecture); *id.*, p.20 (Rambus's Direct RDRAM technology "uses a narrow bus topology operating at a high clock rate to solve the memory bandwidth problem" in which "[a] Direct Rambus channel includes a controller and one or more DRAMs connected together via a common bus"), *accord* EX1071, Figs. 4A-4B and 9:34-45 (channels consist of signal lines in a relatively short multi-drop bus implementation with relatively few memory devices coupled to each channel); EX2009, p.16 (noting that rather than addressing a rank, the memory controller need to address a single device in Rambus XDR architecture).

EX1069 cited by Petitioner further states that in contrast to traditional JEDEC-style memory system, "all of the information for the operation of the DRAM is carried over a single bus in Rambus's architecture; moreover, ***there is no separate chip-select network.***" EX1069, p.11; *see also* p.12 ("In the Rambus memory organization, there is no chip-select network"). Even in later generations of Rambus memories that utilized separate busses for address/control and data, there is still no separate chip-select bus. *See* EX1069, pp.2-3 (JEDEC style memory system

includes a chip-select bus in addition to control, address and data busses), p.9 (discussing Rambus's Concurrent RDRAM and Direct RDRAM, with no reference to the fourth chip-select bus that appears in JEDEC-style architecture); *see also* EX2001, pp. 20-24 (no mentioning of a separate chip-select line for Rambus Direct and on p.23, contrasting its topology in which "a Direct RDRAM spans the entire channel" so that "CPU accesses each RDRAM independently" with traditional DRAM systems in which "several conventional DRAMs [i.e. a rank of memory devices] are frequently ganged together in parallel to provide the necessary aggregate bandwidth"); EX2002 [Samsung RIMM], pp. 3-5 (no chip-select pins or signals mentioned); EX2009, p.16 (the memory controller need to address a single device in Rambus XDR architecture); EX2016, pp. 3-4, 6 (FBDIMMs that were standardized by JEDEC in 2008 receive packetized PS[9:0] and PS#[9:0] that do not include chip select signals; instead its advanced memory buffer (AMB) generates chip select signals on DIMM).

Accordingly, even when Perego discusses providing "individual control lines," it never mentions a signal line for a chip-select signal. *E.g.*, EX1071, 9:58-60. Adding chip-select signals would require adding new pins and affect system layout resources. EX1071, 9:60-64 ("Individual point-to-point control and address lines increase the number of parallel signal connection paths, thereby increasing system layout resource requirements with respect to a narrow 'packet protocol'

approach.”). A Rambus peer-reviewed articles observes that increased pin counts affect not only the memory modules and the devices, but also the CPU design in the host. EX2001, 19 (increasing memory interface pins is not an attractive option for core logic chips in the host), 20-21 (Rambus’s solution “uses a narrow bus topology operating at a high clock rate” which has 8 control/address pins and 18 data pins, such that adding 4 chip select pins for a 4-rank memory would increase the control/address pins by 50%).

This is not a factual dispute. The Petitioner does not provide any competent analysis as to why Perego necessarily or even obviously employs JESD79-2 for its DDR2 SDRAM devices, nor why if it employs JESD79-2, it would then go beyond this specification and also include a chip-select bus on the memory module for providing input chip-select signals to Perego’s buffer device.

2. Modifying Perego to comply with JEDEC would alter the fundamental operation of Perego

If Petitioner’s argument is that a POSITA would have modified Perego to comply with the JEDEC standard, the Petition relies on Perego’s non-JEDEC compliant point-to-point configurations and/or configurable width buffers. *See, e.g.*, Pet. 38-39, 43-46, 61-62, 68-69, 78-79 (Fig. 5B with configurable width buffer, Fig. 5A with point-to-point link interface), 55 (citing to 6:12-24 that specifically mentions “point-to-point link”); *id.* (Fig. 3C with configurable width buffer);

EX2003, 43:12-20 (a JEDEC compliant memory module does not ordinarily have a configurable buffer width).

Perego specifically contrasts the relied-on configuration with “conventional DIMM module” designs that Petitioner suggests are JEDEC compliant. EX1071, 6:27-33; Pet. 32-33. For instance, Petitioner cites to JEDEC21-C, which has a register that buffers only address/control signals but not data signals as contrasted by Perego. *Compare* EX1062, pp.10-16 (inputs and outputs for the register do not include data), EX1066, pp.9-18 (same) with EX1071, 6:12-33 (data as well as control/address information passes through Perego’s buffer, in contrast to prior art buffered module where data I/Os of the memory devices were connected directly to the DIMM connector without going through the buffer).

Hence, looking to JEDEC21-C for its alleged form, signaling and functions (*see* Pet. 33-34) would require a fundamental redesign of Perego, including the subject of Perego’s invention, the “Configurable Width Buffered Modules” (*see* EX1071, cover). As the Federal Circuit has explained, where “the ‘suggested combination of references would require a substantial reconstruction and redesign of the elements shown’ in [one of them], or a ‘change in its basic principles’” under which it was designed to operate, that counsels against finding of obviousness. *Univ. of Md. Biotechnology Inst. v. Presens Precision Sensing GmbH*, 711 F. App’x 1007,

1011 (Fed. Cir. 2017) (quoting *In re Ratti*, 270 F.2d 810, 813 (CCPA 1959) (en banc)).

Petitioner's own cited references also indicate that Rambus's memory architecture was known to be fundamentally different from JEDEC-style memory systems. *See* EX1069, pp.11-16 (no chip-select network, signaling that is more similar to network signaling than memory bus signaling); *see also* EX2001 [Direct RDRAM], p.23 (describing Direct RDRAM architecture and contrasts it with JEDEC-style architecture, *e.g.*, in JEDEC-architecture, "several conventional DRAMs are frequently ganged together in parallel to provide the necessary aggregate bandwidth" but "[the] parallel combination does not increase the number of system banks, instead it just adds to their size"; in contrast, "[b]ecause a Direct RDRAM spans the entire channel, the CPU accesses each RDRAM independently. So each RDAM directly adds to the number of memory banks accessible to the memory controller" with the number of independent banks directly affect the number of concurrent or interleaving operations); EX2004, PDF pp.8-11 (even with multiple row address/control pins and column address/control pins, RDRAM still utilizes a packet format that does not include chip select); EX2009 (Rambus's dynamic point-to-point XDR architecture still uses packet signaling without reference to chip-select signals). The Petition does not provide competent evidence that a POSITA would have been motivated to modify Perego to comply with JEDEC

as that would have required altering Perego's basic operating principles. *See Univ. of Md. Biotechnology Inst.*, 711 F. App'x at 1011; *In re Ratti*, 270 F.2d at 813.

Petitioner argues instead that a POSITA "would have ... been motivated to implement Perego's memory modules in a registered DIMM format with DDR memory devices that fits into DIMM connectors and uses DIMM module input signals, according to JEDEC standards" in light of Perego's objective of providing cost effective upgradability. Pet. 32; *see also* Pet. 33 (regarding alleged desire for backward compatability). But Perego's upgradeability and backward compatability are not achieved by a particular form factor or pin assignment on the module input, but "by employing buffer device 405 to translate protocols employed by controller 310 to the protocol utilized in a particular memory device implementation." EX1071, 10:63-67. Indeed, if the goal is to have a JEDEC-compliant RDIMM with JEDEC-compliant SDRAM devices at low costs, that could be done by buying commercially available standardized DIMMs (*see, e.g.*, EX1062, EX1066). Modifying Perego's memory module into a fixed 64-bit width with the same type of signaling and input pins as JEDEC-compliant RDIMM would not only incur unnecessary cost, but would take away Perego's central subject matter of a "configuration width buffered module." *See* EX1071, title, abstract. Petitioner has provided no competent reason why a POSITA would have incurred the cost to

transform Perego into something that operated with a completely different architecture and was readily available in the market already.

In other words, Perego describes an architecture that differs from JEDEC, and it solves the problem of compatibility with different DRAM devices by using a buffer that can translate different signaling protocols at the memory module I/Os and at the device I/Os. *See* EX1071, 10:63-67. Petitioner has not provided any competent reason for why a POSITA would alter Perego's memory module format or incoming signaling in order to accommodate JEDEC-compliant devices on the module: Perego's design already has the feature that accommodates different types of memory devices, while a JEDEC-compliant module that fit Petitioner's description would already be readily available in the market without the need to modify Perego. *See South-Tek Sys., LLC v. Engineered Corrosion Sols., LLC*, 748 F. App'x 1003, 1007 (Fed. Cir. 2018) ("Given the redundant functions of Viking's drum drip and Wood's condensate drain, the Board found a [POSITA] would not have been motivated to add a condensate drain to Viking in addition to the system's drum drip drain."); *Ex parte Fritsche*, Appeal No. 2015-001835, at 5 (PTAB, Nov. 14, 2016) (no reason for the combination because "although providing a movable section of an air vent may allow air flow to be distributed to different parts of an automobile, [primary reference] already provides such a movable section that achieves the same function").

3. Perego's disclosure in 15:37-45 does not disclose or suggest ranks or chip-select signals

Petitioner suggests that chip select signals are implied by the alleged disclosure of ranks in Perego. *See* Pet. 54-55. For example, Petitioner argues that Perego, 15:37-45 discloses grouping DRAM devices into ranks. *Id.* This is an entirely conclusory statement. Petitioner's own expert, Dr. Wolfe, disagrees that the passage "specifies how ranks are selected or enabled." EX2003, 202:8-204:10 (discussing 15:37-40 and then 15:40-45, "Q: So you don't think this paragraph has anything to do with grouping devices into different ranks? A: I do not think that this paragraph specifies how ranks are selected or enabled."). And Dr. Wolfe further confirms that "independent banks" appearing in the passage refers to "the number of page registers which can be activated corresponding to different addresses" and not to "ranks" as Petitioner alleges. *Id.*, 203:15-204:3.

Perego's disclosure in 15:37-40 also has nothing to do with ranks. That passage discloses selecting a "target subset of secondary channel signal lines ... *via address bits* provided as part of the primary channel request" (i.e., request from the host). *See* EX1071, 15:37-45; Pet. 51. Dr. Wolfe confirms that this disclosure has nothing to do with "selecting a particular group of devices to respond to a single read or write request" (which is required of a rank per Petitioner's definition on Pet. 26),

but only “specific to [selecting] channel signal lines.” EX2003, 202:8-203:9 (*e.g.*, 203:2-9).

Additionally, this disclosure relates to using address bits for selection. Petitioner’s own references distinguishes between address signals and chip select signals. *E.g.*, EX1069, 2 (“examples of ***different types of DRAM pins*** include ***address pins***, data input and output pins, one or more clock input pins, and ***control pins*** (*e.g.*, CAS and RAS input strobes, write-enable, ***chip-select***, etc.)”), *id.* (“The busses in a JEDEC-style organization are classified by their function and organization into data, address, control and chip-select busses.”); *see also* EX1062, 4.20.4-6 to 4.20.4-7 (distinguishing between “SDRAM address bus” A0-A15 and “SDRAM chip select lines” S0-S3).

While in the ‘417 patent, address bits may be used in combination with chip-select signals to generate additional gated chip select signals for transmission to DDR devices (*e.g.*, EX1001, Fig. 10A), they are still different signals. Otherwise, the claims would not have separately enumerated “input chip select signals” and “other input address and control signals.” *E.g.*, Pet. xiii, 1.c.2; *see also* EX1001, Fig. 1 (separate signal lines for CS and other address/control signals). Perego’s reference to address bits therefore does not disclose or suggest “input chip select signals.”

4. Perego’s disclosure in 6:12-24 does not disclose or suggest chip-select signals

Petitioner also cites 6:12-24 to argue that Perego discloses chips select signals. Pet. 55. But that passage only states that “[i]n a normal read operation, buffer device 350 receives control, and address information from controller 310 via point-to-point link 320a ...,” with no reference whatsoever to “chip select signals” or chip select lines. EX1071, 6:12-24.

To the extent that Petitioner argues that the control and address information would include chip-select information, that still does not satisfy the remainder of the claims, including the requirement that the “set of input address and control signals” (which include the input chip select signals and other input address and control signals) are received “via []address and control signal lines” in the memory bus. *See* Pet. xiii, 1.a.3, 1.c.1-1.c.2; *cf.*, EX1071, 1:67-2:3 (“a separate group of signals (e.g., address lines and data lines),” indicating that a particular signal is delivered over a dedicated line).

Specifically, as Petitioner acknowledged, the “control information and address information [is] decoded and separated from multiplexed data” Pet. 63 (citing Perego disclosures for 1.c.4). According to Petitioner’s own evidence, when Perego utilizes a packetized protocol in which control and address information is demultiplexed from data as in Perego, the input control/address information is ***not***

received “via the address and control signal lines” as required by the claims. EX1069, p.11 (in the Rambus’s ‘multiplexed’ bus organization, “[a]t different points in time, the same physical lines carry dissimilar classes of information”). Otherwise, if control/address information is carried on dedicated “control and address signal lines” as required by 1.a.3 and 1.c.1 (*see* Pet xiii), there would be no need to demultiplex the information from data. Moreover, even when Perego discusses providing “individual control lines,” it never mentions a signal line for a chip-select signal, despite referencing other control lines. *E.g.*, EX1071, 9:58-60.

B. Perego does not disclose or suggest a “plurality of registered chip select signals including one registered chip select signal having an active signal value and one or more other registered chip select signals each having a non-active signal value” (1.c.3) or the related limitations in 1.d.2-1.d.3

Element 1.c.3. recites a plurality of registered chip select signals that include “one registered chip select signal having an active signal value and one or more other registered chip select signals each having a non-active signal value.” Pet. xiii, 1.c.3. Petitioner again points to JESD79-2 to argue that the limitation is met. Pet. 58-61. But even if Perego’s memory module utilizes JEDEC-compliant SDRAMs, nothing in the cited JEDEC specifications requires the registered chip-select signals sent to those SDRAM devices have different signal values.

1. A POSITA would not have had a reason to modify Perego into a JEDEC compliant memory module with JEDEC-compliant SDRAMs

As noted for “input chip select signals,” no competent reason has been given for why a POSITA would have had a reason to modify Perego into a JEDEC-compliant RDIMM with JEDEC-compliant SDRAMs. Moreover, as noted above, a JEDEC-compliant memory module with JEDEC-compliant SDRAMs would have been readily available, and a POSITA would not have been motivated to incur the cost to modify Perego into something that was readily available. Furthermore, if Perego’s memory module implements non-JEDEC SDRAMs, JESD79-2 does not apply to those non-JEDEC SDRAMs, meaning that there lacks competent evidence that these SDRAMs would even have chip-select pins or that there would be a need for them to receive registered chip-select signals. *See* elements 1.c.3 and related 1.d.2-1.d.3.

2. Petitioner’s own reference indicates that any registered chip-select signals would have the same signal value

JEDEC-Compliant SDRAM devices do not inherently (or obviously) result in the recited limitation. To the extent that Perego uses JEDEC-compliant SDRAM devices, the registered chip select signals outputted to those devices can all be set to low without affecting the devices’ or the module’s operation. For instance, read, write and bank activate operations specifically called out by Petitioner all have CS

as “L.” Pet. 54 (citing EX1064, p.49). For commands where the combination of !CS, !RAS, !CAS and !WE can take a “HXXX” value, the same command can be expressed as “LHHH.” See EX1064, p.49 for Self Refresh Exit, Power Down Entry and Power Down Exit. Likewise, as Petitioner acknowledges, “[t]he Deselect command performs the same function as a No Operation [NOP] command.” Pet. 52 (citing EX1064, p.48). Hence, a non-targeted device can be sent a NOP command with a signal value of “L” for !CS to indicate no-operation or non-selection. That is, the logic can send only registered chip-select signals having an active signal value to memory devices, while still selectively targeting only some devices for read/write.

Ellsberry and Halbert are in accord. The course of action taken by POSITAs as reflected in these references is instructive on what a POSITA would have done, because these are the only references in the record that discuss the types of commands sent to different ranks of memory devices on a memory module that buffer both the control/address signals and data signals. *Cf., Samsung Electronics Co. Ltd. v. Netlist Inc.*, IPR2022-00063, paper 53, 34-36 (May 3, 2023) (absence of evidence of distributing self-testing functionality is evidence that the alleged combination does not involve simple rearrangement of known elements); *Arendi S.A.R.L. v. Apple Inc.*, 832 F.3d 1355 (Fed. Cir. 2016) (missing limitation cannot be satisfied by resort to common sense).

Specifically, in Ellsberry's row read mode, read/write commands are sent to the target memory devices and NOP commands are sent to the non-targeted memory devices. EX1073, [0033]; EX1064, p.49 (command truth table including values for !CS); *see also* Pet. 118 (Petitioner acknowledging that "Ellsberry discloses sending NOP commands to the non-targeted ranks"). But as specified in the JEDEC specification, NOP and read/write commands all set !CS to "L." EX1064, p.49. That is, if one were to look to Ellsberry for implementation details as Petitioner suggests (Pet. 114), they would have arrived at a design in which the registered chip-select signals each have an "L" signal value, contrary to what is required by 1.c.3 and 1.d.2.

And in Ellsberry's column read mode, data is read from memory devices in both ranks, indicating read commands are sent to both ranks such that both ranks would receive an active signal value for the registered CS. EX1073, [0033]; EX1064, p.49 (command truth table including values for !CS). Likewise, in Halbert, because data is read from or written to both ranks, if registered CS signals are involved, both sets of memory devices would again receive signals of the same signal value. EX1078, Fig. 4 (same registered address/command—RCMD and RADD—sent to both ranks), Fig. 5 & 6:29-39 (showing device arrays 140 and 142 providing data respectively onto data lines RDQ0 and RDQ1, indicating that if registered CS's are received, both need to be of an active signal value in order to

read out the data); Figs. 4 & 6 (data being written simultaneously into ranks 140 and 142 connected to RDQ0 and RDQ1 respectively, again indicating that both memory devices would receive an active signal value).

Evidence cited by Petitioner does not indicate otherwise. For instance, the statement “CS provides for external Rank selection on systems with multiple Ranks” does not say that different memory devices are provided with registered chip select signals of different signal values, or even that each rank of memory devices need to be provided with a CS signal even when they are not selected for a read/write operation. Pet. 60 (citing EX1064, p.6); *compare* Pet. xiii-xiv, 1.c.3 & 1.d.2. Likewise, the cited passages from EX1062 and EX1066 do not state that signals RS0 and RS1 are of different values or must be provided to non-targeted memory devices.

As to EX1069, pp.2-3, it describes a conventional JEDEC-compliant DRAM system. EX1069, p.2 (“the chip-select bus, is *essential in a JEDEC-style memory system*”). Perego, being a Rambus memory system, is not JEDEC compliant and does not indicate that it would be JEDEC compliant. *See*, EX1071, 6:27-33 (comparing Perego data buffer to conventional data buffer); EX1069, p.12 (discussing how Rambus’s protocol differs from traditional JEDEC style protocol, including how the absence of chip-select networks in Rambus memory organization affect other aspects of design and signaling).

Moreover, under Petitioner’s own theory, Perego has buffer devices that can

generate different registered control/address signals for different subsets of memory devices based on received input information. Pet. 60-61 (Petitioner arguing that Perego allegedly could be made to generate four registered chip-select signals to select one of the physical ranks belonging to the same logic rank selected by the memory controller). For instance, Perego discloses that different types of memory devices can be included in a memory system and its buffer device can translate input control/address information into appropriate signals for use by the corresponding DRAM devices. *E.g.*, EX1071, 10:63-67. This implies different types of registered signals for use with different types of memory devices. In that translation, the non-selected JEDEC-compliant memory devices can be sent NOP commands as suggested by Ellsberry, which would result in the registered CS having the same “L” signal value as in read/write commands. *See* discussion above. In other words, EX1069’s discussion of JEDEC-compliant memory modules with no buffers (*see* EX1069, p.3, Fig.3 (no registers/buffers in the illustrated DIMMs)) is not informative of how a POSITA would have configured a buffered memory module like that in Perego. The art in the record involving buffered or registered data is Ellsberry and Halbert, both of which disclose the use of commands having the same signal value for the chip-select signal for different ranks of JEDEC-compliant memory devices, contrary to what the claims require. Thus, like *Arendi*, where a material limitation is absent from the prior art, no *prima facie* case of obviousness

has been made.

3. Perego's buffer device selectively sends registered signals to only targeted memory devices, obviating the need for registered chip-select signals having a non-active signal value

A chip-select signal “[e]nables the associated SDRAM command decoder when low and disables decoder when high.” EX1066, p.7. In other words, as Petitioner’s expert, Dr. Wolfe states, “[a] chip select signal determines whether or not to pay attention to the command in a DDR environment.” EX2003, 141:2-4. But a device has no need to determine whether it should pay attention to a command or not if command signals are only sent to targeted memory devices, as in Perego. For example, Perego discloses,

In a normal memory read operation, *buffer device 350* receives control, and address information from controller 310 via point-to-point link 320a and *in response, transmits corresponding signals to one or more*, or all of *memory devices 360* via channels 370. *One or more of memory devices 360 may respond* by transmitting data to Buffer device 350

Pet. 55 (citing EX1071, 6:12-24). That is, instead of always sending commands to all memory devices, the buffer device sends commands to the targeted “one or more ... of memory devices 360” *Id.* With Perego’s buffer device tasked with determining to which devices the control/address signals should be sent, registered

chip select signals, if any, are sent to only targeted devices, for which the signals need to be of an active value in order to cause any JEDEC-compliant devices to output or receive data.

Accordingly, Perego states, “[a]ccording to *embodiments of the present invention*, subsets of available memory devices on configurable width module 395 are activated or powered-on during various modes of operation” to “achieve power savings by only powering particular memory devices.” EX1071, 20:41-46. If the non-targeted ones are not even powered on, no registered signals could be received by them, contrary to the requirement that “each of the plurality of registered chip select signals is received by memory devices [in] one respective N-bit wide rank of the plurality of N-bit wide ranks.” See Pet. xiv, 1.d.2. There is thus no need to output or generate a plurality of registered chip select signals, some of which each having a non-active signal values as required by element 1.c.3. Pet. xiii, 1.c.3.

Similarly, in the quad channel example in Figure 4B, “two channels 415*c* and 415*d* may transfer information simultaneously and the memory devices on the other two channels 415*a* and 415*b* remain in a ready or standby state until *called upon* to perform memory access operations.” EX1071, 21:16-20. In other words, no commands are sent to the non-targeted memory devices in channels 415*a* and 415*b* to “call[] upon” them to perform memory access operations. *Id.*; see also *id.*, 9:64-67 (individual device select lines), 9:67-10:4 (“individual device identification

values”).

As a result, Petitioner has not provided any competent evidence that Perego either discloses or suggests a plurality of registered chip selects signals (output by the buffer device’s logic and sent to the memory device) that include one having an active signal value (“L”) and one or more each having a non-inactive signal value (“H”), with each registered chip-select signal associated with and received by a corresponding “rank” (if Perego discloses ranks). *See* elements 1.c.3, 1.d.2-1.d.3.

C. Petitioner has not made a *prima facie* case for elements 1.d.1-1.d.3.

1. Perego does not disclose “ranks” of memory devices

Petitioner relies on Perego’s disclosures 15:37-45 for allegedly suggesting the concept “rank.” Pet. 67. But Petitioner’s own expert, Dr. Wolfe, disagrees that the passage “specifies how ranks are selected or enabled.” EX2003, 202:8-204:10 (discussing 15:37-40 and then 15:40-45, “Q: So you don’t think this paragraph has anything to do with grouping devices into different ranks? A: I do not think that this paragraph specifies how ranks are selected or enabled.”). Dr. Wolfe further explains that “independent banks” referenced in that paragraph refers to “the number of page registers which can be activated corresponding to different addresses” and not to “ranks” as Petitioner alleges. EX2003, 203:15-204:3. Given Dr. Wolfe’s admission,

Petitioner does not explain how Perego, 15:37-45, allegedly renders obvious the claim limitation “ranks” as it asserts. *Contra* Pet. 67.

Petitioner then suggests that devices connected to each of interfaces 520a and 520b, a single channel, and/or two channels, can be a rank. Pet. 67-71. As a preliminary matter, Petitioner has not provided any competent evidence that the devices connected to a single channel or interface “act together” in response to a single read/write command as it defines. For instance, in Figure 5F, although both memory devices 652 and 653 are connected to channel DQ1, “[b]oth memory cells 652a and 653b are not accessed via channel DQ1 during a single access operation in an embodiment of the present invention.” EX1071, 20:30-33. Likewise in Figure 5E, there is no evidence that devices 652 and 653 are accessed in a single operation. *See id.*, 20:11-16.

Moreover, unlike the traditional JEDEC-compliant DIMMs, Perego’s memory modules are “configurable width buffered module[s].” EX1071, title; EX2003, 43:12-20 (a JEDEC compliant memory module does not ordinarily have a configurable buffer width). That means Perego’s modules do not have a fixed width. Yet, under Petitioner’s own definition for “rank,” a rank refers to a set of DRAM devices “on a memory module that act together in response to command signals, including chip-select signals, to read or write *the full bit-width* of the memory module.” Pet. 26. With a memory module having a configurable width and

purportedly JEDEC-compliant SDRAMs having fixed widths (in order to satisfy other limitations, see Pet. 32-34), the number of devices in a purported “rank” would necessarily change as the “full bit-width of the memory module” changes. For instance, Perego observes:

The number of signal lines of channels 370 may be increased or decreased as the memory device access width changes. Channels 370 (FIG. 3C) may be subdivided into several addressable subsets. *The address of the transaction will determine which target subset of channels 370 will be utilized for the data transfer portion of the transaction.* In addition, *the number of transceiver circuits included in interface 520a and 520b that are employed to communicate with one or more memory devices may be configured based on the desired serialization ratio.* Typically, configuration of the transceivers may be effectuated by enabling or disabling how many transceivers are active in a given transfer between one or more memory devices and configurable width buffer device 391.

EX1071, 14:62-15:6. As another example, Perego discloses

memory system 700 may concentrate bandwidth as it is required while in operation. For example, memory system 700 may employ only one of channels 415a-415d and match throughput to the corresponding point-to-point link. As bandwidth requirements increase, memory system 700 may dynamically activate more of channels 415a-415d and increase the throughput on the point-to-point link along with the

number of channels accordingly to meet the bandwidth requirements for a given operation.

EX1071, 21:29-38; *see also id.*, 17:1-8 (width of configurable width buffer device can be changed even after it has been used for a particular width, all in general without need to power-down or reset configurable width buffer device), 10:22-33 (in quad-channel module 450, channels 415c and 415d may operate in parallel with channels 415a and 415b, or all four may operate simultaneously); Pet. 38 (Petitioner allege that “[a] POSITA would have understood that a data width of $W_{DP}=64$ corresponds to the 64-bit data width of a JEDEC-compliant registered DIMM module).

Nothing in the ‘417 patent or any JEDEC documents suggests, however, a rank of memory devices refers to a group of memory devices that is dynamically reconstituted to account for the changing memory bit width. *See, e.g.*, EX1001, Figs. 1, 4A-4B, 5C-5D, 8A-8D, 9A-9B, 10A-10B, 11A-11B and associated text.

Moreover, while Perego configures addressable subsets of a channel for a given transaction based on addresses, (*see* EX1071, 14:62-15:6), Samsung’s definition for a rank requires the use of chip-select signals. *See* Pet. 26; EX2006 [Park Ex. 7], p.146 (Samsung previously defining a rank of memory as “the collection of SDRAMs driven by a given rank select signal”); EX2005, 86:19-87:17 (Samsung corporate witness denies that a rank can include a single DRAM). Perego,

however, never mentions “chip-select” signals, lines or the alike. *See* EX1071 *generally*. Hence, Petitioner has not provided any competent evidence that the interfaces or channels it points to are ranks as it defines.

2. Perego’s Rambus-style memory organization is incongruent with JEDEC’s rank concept

Petitioner also argues that it would have been obvious to arrange Perego’s memory devices into ranks in light of the JEDEC specification. But Petitioner’s own evidence distinguishes JEDEC-style memory organization and Rambus-style memory organization as two distinct approaches. EX1069, pp. 11-16. This is not an issue of weighing competing evidence presented by Petitioner and Patent Owner. This is an issue of the Petitioner ignoring the express teachings of its own evidence.

As EX1069 observed, a distinguishing feature of Rambus memory organization, compared to JEDEC, is its lack of chip-select network. EX1069, p.11 (in Rambus memory systems, “there is no separate chip select network”); p.12 (“In the Rambus memory organization, there is no chip select network”). In contrast, in JEDEC, “there is a chip-select network that uses one unique wire per DRAM rank” *Id.*, p. 9. Hence, Perego, an example of a Rambus memory organization, does not disclose or suggest a rank of memory devices, a concept unique to JEDEC-style memory systems and intricately intertwined with the notion of “chip-select” signals.

Even in later Rambus iterations that added separate control and address busses, no chip-select bus was introduced. EX1069, p.9; EX2002 (no chip select input for RIMMs); EX2001 [IEEE Micro], 20-23 (no chip select signals mentioned for Rambus Direct). Instead, Rambus memory systems, including Perego, uses “device identification” to select devices that “share the same channel.” EX1071, 9:67-10:4; *see also* EX1069, p.12 (devices in Rambus’s system would know whether a packet is intended for it via unique identification number contained in the packet); EX2004 [Samsung Direct RDRAM datasheet] at original pages 6-7, Tables 3-4, Fig. 3. In other words, *Perego’s memory systems operate on an individual device basis*, and do not “act together” as required by the concept of “rank.” Pet. 26; EX2001, 23 (“Because a Direct RDRAM spans the entire channel, the CPU accesses each RDRAM independently. So each RDRAM directly adds to the number of memory banks accessible to the memory controller.”); EX2009, p.16 (in a dynamic point-to-point architecture, memory controller needs to address a single device instead of a rank of devices). That is why Perego can provide the flexibility of having different memory devices operate independently, in parallel or simultaneously. *E.g.*, EX1071, 10:22-26, 10:31-33, 21:16-24 (dynamic grouping or device utilization for different applications and during different processing windows). In this manner, Perego’s memory module data output width can also be adjusted dynamically. *E.g.*, EX1071, 5:32-44 (when a second memory module is removed from a memory system, the

bandwidth of the first memory module doubles to retain the same overall system bandwidth: “when the second memory module is removed from the system ... the plurality of point-to-point connections are routed to the first memory module to retain system bandwidth between memory modules and the controller or increase the bandwidth to the first memory module”). Modifying Perego to fit into the JEDEC framework that has fixed ranks and fixed bandwidth would require changing the fundamental operating principle of Perego, which is evidence of non-obviousness. *Univ. of Md. Biotechnology Inst.*, 711 F. App’x at 1011 (quoting *In re Ratti*, 270 F.2d at 813) (not obvious where “the ‘suggested combination of references would require a substantial reconstruction and redesign of the elements shown’ in [one of them], or a ‘change in its basic principles’” under which it was designed to operate); see also *Innogenetics N.V. v. Abbott Laboratories*, 512 F.3d 1363, 1373 (Fed. Cir. 2008) (“knowledge of a problem and motivation to solve it are entirely different from motivation to combine particular references to reach the particular claimed method”).

Indeed, if the design goal is to obtain JEDEC compliant RDIMM with JEDEC compliant SDRAMs (*see, e.g.*, Pet. 31-32), such modules would have been readily available. *E.g.*, EX1062; EX1066. Petitioner has not provided any evidence that a POSITA would have been motivated to undertake the substantial effort to redesign Perego in order to obtain something that was already available.

3. Petitioner has not shown that Figure 4B would disclose all limitations under its own theory(ies)

Petitioner also suggests that Netlist previously conceded Perego Figure 4B disclosed two ranks. Pet. 71. What Netlist said was, given Petitioner’s requirement that a rank refers to a set of memory devices that would act together and because Perego describes channels 415c and d (or 415a and b) as operating together, then—even under Petitioner’s suggested modification in which each channel includes but one device—there would be two devices in a “rank.” EX1019, p.43; EX1020, ¶¶93-94. At any rate, neither channels 415c and 415d nor channels 415a and 415b would meet Petitioner’s own definition of a rank.

First, according to Petitioner, the data width accessed in a memory transaction (W_A) corresponds to the bit-width of each rank of memory device “when only ‘one’ of the ‘one or more channels 370’ ... is used for a read or write operation.” Pet. 69. Accordingly, where channels 415c/d (or 415a/b) collectively form a rank—that is, more than one channel is used for a read/write operation, the data width accessed in a memory transaction would differ from the bit-width of a rank of memory device under Petitioner’s own reasoning. Yet, under Petitioner’s definition, a rank is “an independent set of ... memory devices on a memory module that act together ... to *read or write full bit-width of the memory module.*” Pet. 26. Petitioner does not explain why channels 415c/d together read or write *full bit-width of the memory*

module under its own theory, given that if each channel width equals the width of the full module, two channels would have a data width twice that of the memory module. And likewise, given that two channels would provide twice the width of a single channel and each channel allegedly provides N-bit width, 415c/d (or 415a/b) are not “N-bit wide ranks” as identified by Petitioner.

Second, although much of the Petition’s theory relies on the module width being 64 bits, the data width in Perego’s Figure 4B is 16 bits. *See* Pet. 38 (“A POSITA would have understood that a data width of $W_{DP}=64$ corresponds to the 64-bit data width of a JEDEC-compliant registered DIMM module.”), 58-59, 67 (each rank 64 bit wide). Petitioner does not give any reason for changing the module width from 16 bits to 64 bits, other than to argue that the 64-bit width is that of a JEDEC-compliant RDIMM so that a POSITA would modify Perego to be JEDEC compliant. But that reasoning is circular and is clearly using the claims as a roadmap for assembling the elements. That is textbook hindsight.

Third, as EX1069 notes, in Rambus systems, there are no fixed “N-bit wide” burst sizes; instead, “the block size is programmed every time the CPU sends a new request to the DRAM.” EX1069, p.16. This is in contrast to JEDEC style memory system that reads or writes fixed 64-bit bursts of data (72-bit with ECC). Pet. 38 (Petitioner alleging “the 64-bit data width of a JEDEC-compliant registered DIMM module”); EX1062, p.5 (x64 or x72 module); EX1066, p.4 (x72 ECC module). And

this is in contrast to 1.d.3's requirement that one of the N-bit wide ranks (the targeted one) is to output or receive a burst of N-bit wide data signals in response to a read/write command. Perego's burst size can vary for each new request, and does not have a fixed N-bit width.

Fourth, Petitioner makes no effort to show that memory devices in channels 415c/d would receive one registered chip select signal and memory devices in channels 415a/b would receive another registered chip select signal of a different value as required by element 1.d.2. Instead, registered signals may only be sent to targeted devices in channels 415c/d and not to non-targeted devices in channels 415a/b. *E.g.*, EX1071, 21:16-20 ("the memory devices on the other two channels 415a and 415b remain in a ready or standby state *until called upon* to perform memory access operations").

For at least these reasons, Perego, alone or in combination, does not disclose or suggest a "rank" of memory devices even under Petitioner's own definition.

D. Perego does not disclose or suggest limitations related to overall CAS latency of the memory modules

Petitioner's theory is again based on an assumption that Perego is JEDEC compliant or would be made so. Pet. 92-96. But as explained above, Perego does not mention JEDEC once and in fact contrasts its configuration or topology with the traditional JEDEC style organization. EX1071, 6:27-33.

As a preliminary matter, nothing in Perego itself suggests that Perego's data buffer would transfer bursts of data signals "in accordance with an overall CAS latency of the memory module" as required by element 1.e. For instance, while Perego's buffer exchanges "access latency values" with the host via sideband signaling (*e.g.*, via I2C signaling of the SPD device) (*see* EX1071, 12:20-34), Perego does not state that the "access latency values" relate to the "overall CAS latency of the memory module," as opposed to a latency value of the memory device itself. *Id.* Nor does Perego ever suggest that the timing of the data transfer would be based on the latency of the memory module as opposed to that of the device. *See* EX1071, 12:20-34 and *generally*.

Petitioner suggests instead that because in JEDEC DDR RDIMMs, the CAS latency of the memory module would be one cycle more than the reported value for the memory device, a POSITA would do the same in Perego. Pet. 94-95. But Perego expressly distinguishes its data buffer to that on a traditional RDIMM. EX1071, 6:27-33. Moreover, no similar language is found in JEDEC's DDR2 RDIMM specification. *Compare* EX1066, pp.94-96 *with* EX1062, p.68. As such, there is no competent evidence that a POSITA would have viewed DDR RDIMM specification as applicable to how Perego's invention should be implemented or modified at the time of the invention.

Petitioner also suggests that Netlist is bound by the Board’s prior ruling in another IPR. Pet. 93-94. But the claims there do not recite CAS latency of the memory module at all; and it did not involve the Perego reference. *See* EX1030. In other words, the Board neither found that the requirement that the data bursts be transferred “in accordance with an overall latency of the memory module” obvious, nor that Perego disclosed or suggested such a limitation.

In that respect, the examiner found that the recited CAS latency relationship is not disclosed by art of record, which included Halbert, Ellsberry and Perego-639 that is substantially the same as Perego. EX1002, 245 (#199, Perego-639), 245 (#167, Halbert), 247 (#257, Ellsberry), 229 (NOA); EX2018 [Perego-639]; EX2018 (redline of Perego-639 versus Perego); *see also* 325(d) discussion below.

Petitioner has also not provided competent evidence for element 1.f. For instance, Petitioner ignores that Perego’s buffer device includes caches that speed up data access. *E.g.*, EX1071, 12:4-9 (“Cache 560 is one performance enhancing feature that may be incorporated onto buffer device 405. Employing a cache 560 may improve memory access time by providing storage of most frequently referenced data and associated tag addresses with ***lower access latency characteristics than those of the memory devices.***”). Petitioner provides no analysis on how the module level CAS latency would compare to device-level latency given the low-latency cache feature as required by element 1.f.

Petitioner also argues that element 1.f. is met because JEDEC allows for additive latency in addition to CAS latency. Pet. 95. But the actual operational CAS latency of a memory device would include the AL as well as specified CL. EX1064, p.24 (noting read latency, RL, is the sum of AL and CL, and write latency is RL-1). This is because CAS latency measures “a delay time which elapses between the moment the memory controller ... informs the memory modules ... to access a particular column in a selected rank or row and the moment the data for or from the particular column is on the output pins of the selected rank or row.” EX1075, 15:52-57. AL, however, represents the time during which a device holds a command “before it [the command] is issued inside the device.” EX1064, p.24. In accordance, read CAS latency includes both the AL portion when the command is received by the device but not released for processing and the CL portion that represents the delay due to processing time. *Id.* And, WL, being RL minus one, would also include both AL and CL portions. *Id.* That is, in those systems, AL plus CL provides a measure of the actual operational CAS latency of the memory device.

These deficiencies are not remedied by combining Perego with Ellsberry or Halbert because neither Ellsberry nor Halbert has the cache or write buffer structures featured in Perego. Hence, the fact that Ellsberry’s or Halbert’s memory modules might have an overall CAS latency greater than the actual operational latency of the memory device, even if true, sheds no light on how Perego’s system would operate.

Nor has Petitioner provided any competent analysis to explain what is allegedly missing from Perego such that a POSITA would look to either Ellsberry or Halbert for implementation details. Perego has a detailed description of how its system, including the buffer device, is to operate. *See* Figs. 3-8 and associated text. The Petition gives no reason why a POSITA would even think of replacing Perego's buffer with those from Ellsberry or Halbert or modifying Perego in light of Ellsberry or Halbert. There is also no discussion whatsoever on how Perego is supposed to operate if its buffer device is modified in light of Ellsberry or Halbert. The proposed combinations are therefore the product of hindsight.

VII. PETITIONER FAILS TO ESTABLISH A REASONABLE LIKELIHOOD OF SUCCESS ON GROUND 2

Petitioner argues that Perego in view of Ellsberry renders challenged claims obvious. A POSITA would not have modified Perego in view of Ellsberry because Ellsberry is not a proper IPR reference and because Perego and Ellsberry have different architectures.

A. Ellsberry is not a “printed publication” under §311(b)

Petitioner asserts that the '417 patent is not entitled to a priority date before July 1, 2005. Even if true, Ellsberry is a *patent application* published after that date. EX1073, cover (published in December 2006). Consequently, Ellsberry does not qualify as a patent or a printed publication required under §311(b).

In particular, under the AIA, an IPR petition may be only "on the basis of prior art consisting of patents or printed publications." 35 U.S.C. §311(b). Ellsberry is not a patent; so the question is whether it qualifies as "printed publications." It does not.

Pre-AIA patent law only refers to certain art as "printed publication." In particular, pre-AIA 35 U.S.C. §102 provides that the prior art includes inventions that "w[ere]...described in a *printed publication*...before" the invention, §102(a), or "in a *printed publication*...more than one year prior to the date of [one's] application for patent," §102(b). The critical date for a "printed publication" is the date it is "*published, i.e., accessible to the public.*" *Samsung Elecs. Co. v. Infobridge Pte. Ltd.*, 929 F.3d 1363, 1368, 1370 (Fed. Cir. 2019) (emphasis added).

There can be no dispute that Ellsberry became a printed publication on its publication date of December 2006, after even Petitioner's alleged invention date of July 1, 2005. EX1073, cover.

While Ellsberry is prior art under §102(e), that does not automatically make it into a "printed publication" before the invention date: §102(e) does not even mention "printed publication" or describe a qualifying application as a printed publication before its date of publication. Netlist is also not aware of any Federal Circuit cases that specifically characterize a patent application as a printed publication before its publication date. And Petitioner—who bears the burden of

establishing that its Petition satisfies the requirements in §311(b)—has not cited any authority to the contrary. It simply assumes that a §102(e) patent application qualifies as a printed publication as of its effective filing date. Pet. 20. Yet, the Federal Circuit has made clear that prior art becomes a “printed publication” only when it became published. *In re Klopfenstein*, 380 F.3d 1345, 1348 n.2 (Fed. Cir. 2004) (quoting *In re Cronyn*, 890 F.2d 1158, 1160 (Fed. Cir. 1989) (“The statutory phrase ‘printed publication’ has been interpreted to mean that before the [relevant] date the reference must have been sufficiently accessible to the public interested in the art; dissemination and public accessibility are the keys to the legal *determination whether a prior art reference was “published.”*)).

Consequently, because patent applications are “printed publication” prior art only as of the date they became published and available to the public (*id.*) and because Ellsberry is a patent application published after the invention date, it does not qualify as either “patents” or “printed publications” required by §311(b). Thus, Ground 2 fails.

B. Ellsberry does not cure the deficiency of Perego

As noted above, Perego does not involve “input chip select signals,” nor does it involve outputting a plurality of registered chip select signals, each associated with a different rank, one of which having an active signal value and one or more having a non-active signal value. *See* Pet. xiii-ix, 1.c.3, 1.d.2-1.d.3. Adding Ellsberry

would not cure that deficiency. For instance, Petitioner asserts that selected banks would receive read/write commands and non-selected banks would receive NOP commands. *See* Pet. 117 (Petitioner's annotated Fig. 2 showing that read/write commands are sent to targeted Bank 1 and NOP commands are sent to non-targeted banks 0, 2 and 3).² But according to Petitioner's own evidence, both NOP and read/write involve a chip select signal having a "L" signal value. *See* Pet. 49 (citing EX1064, p.49, reproduced below).

² Netlist disagrees that Ellsberry's logic utilizes address information and chip-select signals to decide which port to activate. Pet. 117-118. Ellsberry only discloses using addresses to determine which memory bank to activate. EX1073, [0031]. Chip-select signals are not mentioned in connection with port or memory bank selection. *Id.* But the Board need not resolve this dispute to determine whether to institute.

Table 10 — Command truth table.

Function	CKE		$\overline{\text{CS}}$	$\overline{\text{RAS}}$	$\overline{\text{CAS}}$	$\overline{\text{WE}}$	BA0 BA1 BA2	A15-A11	A10	A9 - A0	Notes
	Previous Cycle	Current Cycle									
(Extended) Mode Register Set	H	H	L	L	L	L	BA	OP Code			1,2
Refresh (REF)	H	H	L	L	L	H	X	X	X	X	1
Self Refresh Entry	H	L	L	L	L	H	X	X	X	X	1
Self Refresh Exit	L	H	H	X	X	X	X	X	X	X	1,7
			L	H	H	H					
Single Bank Precharge	H	H	L	L	H	L	BA	X	L	X	1,2
Precharge all Banks	H	H	L	L	H	L	X	X	H	X	1
Bank Activate	H	H	L	L	H	H	BA	Row Address			1,2
Write	H	H	L	H	L	L	BA	Column	L	Column	1,2,3
Write with Auto Precharge	H	H	L	H	L	L	BA	Column	H	Column	1,2,3
Read	H	H	L	H	L	H	BA	Column	L	Column	1,2,3
Read with Auto-Precharge	H	H	L	H	L	H	BA	Column	H	Column	1,2,3
No Operation	H	X	L	H	H	H	X	X	X	X	1
Device Deselect	H	X	H	X	X	X	X	X	X	X	1
Power Down Entry	H	L	H	X	X	X	X	X	X	X	1,4
			L	H	H	H					
Power Down Exit	L	H	H	X	X	X	X	X	X	X	1,4
			L	H	H	H					

Thus, Ellsberry cannot cure the deficiencies for 1.c.3. In making its argument otherwise, Petitioner conflates “NOP” and “Deselect.” Pet. 118 (asserting “a NOP or ‘Deselect’ command”). In Ellsberry, NOP and Device Deselect are different commands. *See* EX1073, Fig. 8B (Different entries for NOP and “DEVICE DESELECT”). Ellsberry, however, is clear that NOP commands, and not DESELECT, are sent to the non-targeted devices. EX1073, [0033], Figs. 8A-8B.

Petitioner also cites Ellsberry for the latency-related limitations, relying on Ellsberry’s disclosure of “if cl_mode=subtract, cl = cl-1 to DDRs.” Pet. 118-119. As a preliminary matter, nothing in Ellsberry suggests that the CL parameter—set

via the mode register command—is ever sent to Ellsberry’s switch ASICs (the purported data buffers). *See* EX1073, Fig. 2 (registered command, address and clocks are sent via control ASIC to memory devices directly), Fig. 8A (MRS-mode register set command—differs from EMRS command), [0044] & Fig. 9 (only mentioning squelching or suppressing certain parameters of extended mode register set (EMRS), and even then, the POSTED CAS_n is passed through to the memory devices). That is, there is no indication that Ellsberry’s data buffer even receives CL, let alone transferring data in accordance with that parameter.

Furthermore, neither Ellsberry nor Petitioner explains when “cl_mode=subtract” occurs, how the subtract mode is supposed to operate in the “cl_mode=subtract” mode (*e.g.*, whether that implies the data is transferred in accordance with revised memory device latency or in accordance with the overall latency of the memory module), or whether this operating condition would apply in Perego’s vastly different architecture. Pet. 118-119. Petitioner simply assumes that a POSITA would have blindly applied any teaching from Ellsberry to Perego without examining its applicability. *Id.* That is improper and a complete failure in proof.

Nor has Petitioner shown a competent reason for combining Perego with Ellsberry. As Petitioner acknowledges, Perego involves a centralized data buffer while Ellsberry has a distributed data buffer architecture. Pet. 114-115. While Petitioner attempts to waive aside that significant difference by characterizing them

as “known alternatives for data buffering,” the fact is the difference had a significant impact on latency and signal integrity. For instance, IDT, a data buffer supplier notes the following when comparing DDR3 LRDIMM’s centralized memory buffer design and DDR4 LRDIMM’s distributed buffer design.

DDR3 LRDIMM Design	Characteristic	Downside
Centralized memory buffer	Longer I/O trace lengths	Longer stubs connected to memory channel cause worse signal reflections, resulting in poorer signal integrity
		Longer traces cause increased latency
		Longer traces cause longer I/O bus turnaround time
Component latency	Delay is approximately 2.5ns	Longer propagation delay adds to latency

DDR4 LRDIMM Design	Characteristic	Upside
Distributed buffers	Shorter I/O trace lengths	Shorter stubs connected to memory channel cause less pronounced signal reflections, resulting in improved signal integrity
		Shorter traces reduce latency
		Shorter traces reduce I/O bus turnaround time
Component latency	Delay is approximately 1.2ns	50% less latency than DDR3 memory buffer,

(EX2010, 2)

In particular, IDT noted that distributed buffer architecture provides “less pronounced signal reflections, resulting in improved signal integrity,” “reduce[d] latency,” “reduce[d] I/O bus turnaround time” and “50% less latency than DDR3 memory buffer.” EX2010, 2; *see also* EX2011 (performance difference comparison between DDR3 HCDIMM with distributed buffer technology and DDR3 LRDIMM

with a centralized buffer). At the same time, Perego includes latency-reduction features such as data cache that is absent from Ellsberry. EX1071, 12:5-9 (“Employing a cache 560 may improve memory access time by providing storage of most frequently referenced data and associated tag addresses with lower access latency characteristics than those of the memory devices.”). There is no analysis at all on how to reconcile the different architectural features and how those different features would affect the resulting latency or why the required latency would follow in the combination.

Indeed, Petitioner does not even assert that Perego lacks any particular implementation detail that it argues would have motivated a POSITA to consult Ellsberry, but merely asserts that a POSITA would look to Ellsberry for alleged implementation detail for memory modules with data buffers. Pet. 114-115. Yet, Perego describes in detail the features needed for its invention. *See* EX1071 *generally*. Petitioner’s apparent attempt to “[d]efin[e] the problem in terms of its solution reveals improper hindsight in the selection of the prior art relevant to obviousness.” *Monarch Knitting Mach. Corp. v. Sulzer Morat GmbH*, 139 F.3d 877, 880 (Fed. Cir. 1998).

Petitioner’s assertion of predictability in general is also insufficient to make out a *prima facie* case of obviousness. As articles comparing performance of centralized buffer and distributed buffer have made clear, the difference in

performance is large and unpredictable. EX2010, 2 (comparing DDR4's LRDIMMs with a distributed buffer topology with DDR3 LRDIMMs with a central buffer topology); EX2011, 3; EX2014, 27 (Netlist's DDR3 HDIMM with a distributed buffer topology outperformed DDR3 LRDIMMs with a centralized structure).

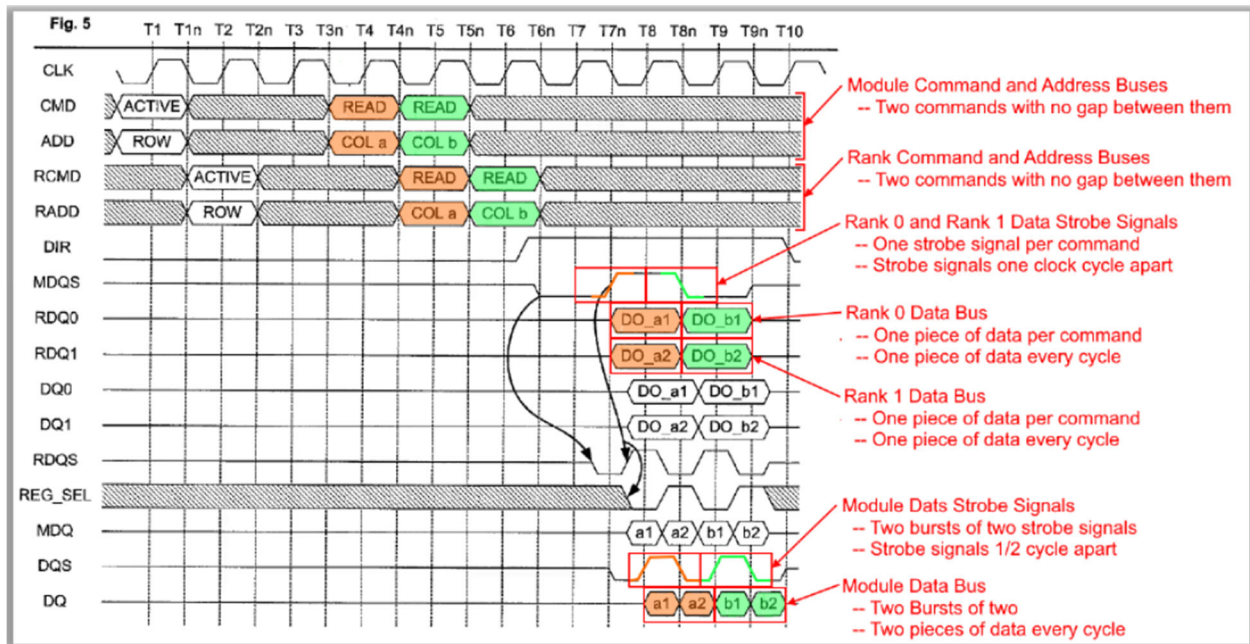
Sample Memory Configurations (2CPU)	Total Memory (GB)	Number of DIMMs	DIMM Size	DIMM Ranks	DIMM Type (UDIMM, RDIMM, LRDIMM)	Data Rate	DIMMs per Channel	Unloaded Latency (ns)	Loaded Latency (ns)	Throughput (GB/s)	Idle Power (W)	Loaded Power (W)
24 x 16GB 2R 1333 H	384	24	16GB	2R	HDIMM	1333	2	65.7	114.0	72.4	144.5	286.1
16 x 32GB 4R 1333 L	512	16	32GB	4R	LRDIMM	1333	2	66.8	138.9	68.1	35.3	110.8

To the extent Petitioner bases the combinability on the allegation that Ellsberry is JEDEC compliant and a POSITA would look to it for JEDEC compliance, Petitioner does not explain why a POSITA would modify Perego to make it comply with JEDEC. Pet. 114-115. Perego, a Rambus architecture, is designed to be different from JEDEC. EX1069, pp. 11-16 (contrasting Rambus memory organization and JEDEC memory organization, noting Rambus memory organization is revolutionary in that it resembles more a computer bus architecture than a typical memory bus architecture). Those two systems are based on different design principles, (*id.*) and forcing Rambus architecture to fit into the JEDEC framework would require fundamental redesign of Perego's/Rambus's system. That is evidence of non-obviousness. *See Univ. of Md. Biotechnology Inst.*, 711 F. App'x at 1011; *In re Ratti*, 270 F.2d at 813.

**VIII. PETITIONER HAS NOT MADE A *PRIMA FACIE* CASE OF
OBVIOUSNESS FOR GROUND 3**

A. Halbert does not cure the deficiency of Perego

Halbert does not cure the deficiencies of Perego. For example, Perego does not disclose a logic that outputs a plurality of registered chip-select signals, one of which having an active signal value and one or more of the rest each having a non-active signal value. Pet. xiii, 1.c.3. Halbert does not teach this limitation either. Specifically, Halbert aims to “widen[] the data bus on the memory module as compared to the width of the system memory data bus,” as this “allow[s] a faster system memory data bus to operate at full speed with slower memory devices.” EX1078, [0023]. This is achieved by accessing, via 2m data lines, the slower memory devices in multiple ranks 140 and 142 simultaneously and in parallel, while the data interface circuit 120 interfaces such parallel memory device accesses with faster serial data transfers to or from the system memory controller. *Id.*, [0027]-[0033]. Accordingly, “multiple ranks will receive the same address and commands, and will perform memory operations with the interface circuit concurrently.” *Id.*, [0030]. A corresponding timing diagram for a read operation with annotation is shown below.



As is clear from the timing diagram and the associated description, in response to each read (or write) command, both ranks participate in the read/write operation. See EX1078, Figs. 5-6. Hence, to the extent both ranks of Halbert utilize JEDEC-compliant SDRAM devices that receive chip-select signals as part of the read/write commands, both ranks will receive chip-select signals of the same active signal value, instead of one receiving an active signal value and the other receiving a non-active signal value as required by 1.c.3.

Likewise, Petitioner has not pointed to any evidence that Halbert's data buffer is configured to transfer data in accordance with the overall CAS latency of the memory module, as opposed to the latency of the device after the device receives the read/write commands. Pet. 125-126. What the Petition at most shows is that due to the one-cycle delay between when the command is issued by the memory

controller and when the device receives the command, the time interval between when the memory controller issues a read command and when data appears on memory bus is greater than the time interval between when the memory device receives the command and when data appears on memory bus. But that result does not evidence how the result is achieved: that is, the timing could simply result when the data buffer just transports data without reference to the overall CAS latency of memory module at all, but in reference to some other signals or parameters (*e.g.*, the relevant data data strobe signals). *E.g.*, EX1078, 6:19-28 (“Device array 140/142 signifies that it is about to drive data onto buses RDQ0 and RDQ1 by taking data strobe MDQS low ... Module controller 110 senses the transition on MDQS—this causes module controller 110 to take register data strobe RDQS low in turn, thereby signaling to the primary memory controller that data transfer is about to occur.”).

B. Petitioner has not stated a *prima facie* reason to combine Perego and Halbert

Petitioner suggests that “a POSITA would have been motivated to use Halbert’s rank-based arrangements in Perego’s module ...since they ‘allow the memory devices to be isolated from the full capacitive loading effects of the system memory data bus ... [and] avoid arrangements of competing memory banks that load each other” Pet. 122. But according to Petitioner, “[a] POSITA would [already] have understood that the input and output latches 597f-m [of Perego] isolate the load

of the ‘memory devices’ from the memory controller ... since the memory controller only sees the load of the latches 597f-m.” Pet. 97. Similarly, by buffering all control/address and data signals between the memory controller and memory devices, Perego’s memory devices in different channels are already isolated from one another due to the intervening buffer device. *See* EX1071, Figs. 3A-3C. In other words, Perego already has the feature that Petitioner alleges would have motivated a POSITA to incorporate from Halbert. But a POSITA would not have been motivated to make the combination given the redundancy to the existing features. *See South-Tek Sys., LLC*, 748 F. App’x at 1007 (“Given the redundant functions of Viking’s drum drip and Wood’s condensate drain, the Board found a [POSITA] would not have been motivated to add a condensate drain to Viking in addition to the system’s drum drip drain.”).

Petitioner also provides no detail whatsoever on how it suggests a POSITA should incorporate Halbert’s design in Perego. For instance, is Petitioner proposing to modify Perego so that it adopts Halbert’s multi-rank participation per read/write operation? If so, as explained in Section A above, the resulting configuration would not satisfy element 1.c.3.

Or is Petitioner suggesting that, contrary to its assertion for Ground 1, Perego actually does not disclose or suggest the concept of rank, but a POSITA would have nevertheless looked to Halbert to incorporate the rank concept into Perego’s design?

But if so, why would a POSITA be motivated to modify Perego to incorporate the rank concept? Perego operates on an individual device level, with “individual device identification values” even when multiple devices share the same channel. *See* EX1071, 9:64-10:4; EX1069, p.12 (having a unique identification number for each DRAM is needed to identify recipient of a request packet because Rambus memory organization does not involve “chip-select network”). Modifying Perego to incorporate Halbert’s “rank-based arrangement,” in which a predetermined set of memory devices act together in response to a received command, would require changing of Perego’s operating principles. As such, the modification would not be obvious to a POSITA. *See Univ. of Md. Biotechnology Inst.*, 711 F. App’x at 1011; *In re Ratti*, 270 F.2d at 813.

IX. DISCRETIONARY DENIAL IS WARRANTED

A. 325(d) Favors Denial

The Board uses a two-part framework in evaluating whether to exercise discretion under 35 U.S.C. § 325(d). Under Part 1, the Board considers “whether the same or substantially the same art previously was presented to the Office or whether the same or substantially the same arguments previously were presented to the Office.” *Advanced Bionics, LLC v. MED-EL Elektromedizinische Geräte GmbH*, IPR2019-01469, Paper 6 at 8 (P.T.A.B. Feb. 13, 2020). Under Part 2, if either condition in Part 1 is satisfied, the Board considers “whether the petitioner has

demonstrated that the Office erred in a manner material to the patentability of challenged claims.” *Id.* Applying the *Advanced Bionics* framework confirms that the Petition should be denied institution under §325(d).

Petitioner admits that Ellsberry and Halbert were disclosed in an IDS during prosecution. Pet. 127. The examiner has also considered both references. *See* EX1002, 245 (#167), 247 (#257) (examiner stating that he considered all the references on the IDS except where lined through, and Halbert and Ellsberry were not lined through).

Petitioner also admits that “family members of Perego were disclosed” during prosecution. Pet. 127. Indeed, Perego (EX1071) is materially the same as Perego-639 (EX2017), a continuation-in-part of Perego that was considered by the examiner during prosecution of the ’417 Patent. *See id.*, 1:4-6; EX1001, 3 (listing Perego-639); EX1002, 245 (#199). As shown by a redline of Perego-639 against Perego-422, the entirety of Perego’s specification was maintained in Perego-639. *See* EX2018. Thus, Perego also qualifies as the same or substantially the same art presented to the office.

Finally, the JEDEC standard is also the same as art presented to the office. Petitioner admits as much, stating that “[a] POSITA would have been familiar with these JEDEC standards,” and that “[t]he prior art also refers to these JEDEC standards.” Pet. 9-10 (citing passages from Perego and Ellsberry discussing JEDEC

standards), *id.*, 118 (asserting that the JESD79-2 standard was “incorporated by reference” into Ellsberry). Furthermore, IDS also includes substantially the same JEDEC specifications. *See* EX1001, p.9 (listing JEDEC Standard DDR2 SDRAM Specification, JESD79-2B); EX1002, 265; *compare* EX1064 (September 2003 version, JESD79-2), *with* EX2020 (January 2005 slightly updated version, JESD79-2B).

Petitioner’s sole argument against Part 1 being satisfied is that the asserted references allegedly “were buried in an IDS,” but that applies an incorrect standard. *See Nespresso USA, Inc. v. K-Fee System GMBH*, IPR2021-01221, Paper 9 at 13 (P.T.A.B. Jan. 18, 2022) (in denying institution based on references listed among a long list in IDS, the Board remarked “[t]he precedential decision in *Advanced Bionics* unambiguously instructs, however, ‘**Previously presented art** includes art made of record by the Examiner, and art provided to the Office by an applicant, **such as on an Information Disclosure Statement (IDS)**, in the prosecution history of the challenged patent.’”) (quoting *Advanced Bionics*, Paper 6 at 7-8); *Roku, Inc. v. Universal Electronics, Inc.*, IPR2019-01619, Paper 17 at 6-7 (P.T.A.B. May 25, 2021) (denying rehearing request because the Board “did not misapprehend *Advanced Bionics* in finding that Herz was previously was presented to the Office” as a result of being cited in an IDS). Moreover, the examiner states that “ALL REFERENCES CONSIDERED EXCEPT WHEN LINED THROUGH.” EX1002,

243, 245, 247; *see also* 291 (L16 search included US 6502161 (Perego grandparent)). The references at issue were not lined through. That is, Petitioner improperly speculates that the examiner did not consider the references when the examiner expressly stated that he did consider them.

Turning to Part 2 of *Advanced Bionics*, the Petition does not show that the Office erred in its examination. *See Advanced Bionics*, IPR2019-01469, Paper 6 at 10 (noting that this inquiry “focus[es] on the petitioner’s evidence of previous Office error”). Petitioner does not specifically identify any errors and instead conclusory rests on its arguments for Grounds 1-3. Pet., 127-128. However, as discussed thoroughly above, the Office did not err, as none of the references in the Petition render the challenged claims obvious. Petitioner’s arguments at most show that a reasonable mind could differ in the conclusion, which is not sufficient to show material error under the *Advanced Bionics* framework. Discretionary denial is warranted.

B. 314(a) Favors Denial

The Petition should be denied under §314(a) pursuant to the *Fintiv* factors in light of parallel litigation between the parties.

1. Likelihood of a stay – Petitioner has sought a stay pending a Ninth Circuit appeal on a contract action. The motion has been pending since last fall, and it is unlikely that the court will grant it. Petitioner has not sought a stay based on the

IPRs; nor is such a request likely granted because, as stated below, trial will likely occur long before any final written decision is issued. This factor weighs against institution.

2. Proximity of the court's trial date to a final written decision – Trial in the parallel litigation is currently scheduled for April 15, 2024. Ex. 2021, 1. Thus, it is very likely that trial will conclude before the issuance of any final written decision, as the statutory deadline will be fifteen months from the date of this POPR, which is August 9, 2024. *Allergan, Inc. v. BTL Healthcare Technologies A.S.*, PGR2021-00016, Paper 16 at 13-19 (P.T.A.B. June 16, 2021) (denying institution under 314(a) because of the significant overlap with parallel ITC proceeding which would end four months before a final written decision). Furthermore, the most recent published median time-to-trial for EDTX is only 19 months (placing the start of trial at March 1, 2024), which is much shorter than Petitioner's out-of-date, COVID-19 influenced statistic. *Compare* EX2019, 35, *with* EX1092, 35. Having to litigate in parallel with an IPR proceeding would be an unnecessary waste of time and resources, particularly in light of the weakness of the Petition.

This factor weighs against institution. *Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 11 at 9 (PTAB March 20, 2020) (precedential) ("If the court's trial date is earlier than the projected statutory deadline, the Board generally has weighed this fact in favor of exercising authority to deny institution under *NHK*."); *Samsung*

Electronics Co., Ltd. v. California Institute of Technology, IPR2023-00130, Paper 10 at 16 (P.T.A.B. May 4, 2023) (“Regardless of whether we consider the scheduled trial date or the trial date expected based on time-to-trial statistics, the trial in the Underlying Litigation would commence several months before the expected date of our final written decision.”).

3. Investment in the parallel proceeding by the court and the parties –

The parties have already exchanged infringement and invalidity contentions, and fact discovery is underway. EX2021. Furthermore, by the time of the institution decision, claim construction will be underway. This factor weighs against institution.

4. Overlap with parallel proceedings – There is a significant overlap between the validity issues present here and the issues to be decided by the district court. Petitioner is accused of infringing all challenged claims of the ’417 Patent, and has served invalidity contentions against all challenged claims, including Perego, JESD79-2, Ellsberry, and Halbert as prior art references. EX2022, 1, 17-20. Furthermore, Petitioner has not submitted a *Sotera* stipulation stating that, if this IPR is instituted, it will not pursue any grounds it has or could have raised in the Petition (although that would still not outweigh the other factors). And Petitioner’s past conduct—including pursuing invalidity grounds that is clearly covered by the *Sotera* stipulation even after being notified of the violation by Netlist—strongly indicates

that it has no intention of honoring the stipulation until being told by the district court, at which point resources have already been wasted. This factor weighs against institution.

5. Whether the Petitioner and the defendant in the parallel proceedings are the same party – Petitioner is a defendant in the parallel litigation. This weighs against institution.

6. Other circumstances – The merits of the Petition are weak, which weighs against institution. As such, a denial of institution under the *Fintiv* factors would not be in conflict with Director Vidal’s 2022 Memorandum. Petitioner has not demonstrated a reasonable likelihood of success, let alone that the merits of the Petition are *compelling*. *CommScope Techs. LLC v. Dali Wireless, Inc.*, IPR2022-01242, Paper 23 at 3 (P.T.A.B. Feb. 23, 2023) (precedential) (“[T]he compelling merits standard is a higher standard...”). Discretionary denial is warranted.

X. CONCLUSION

Based on the foregoing, the Board should decline to institute an *inter partes* review.

Dated: May 9, 2023

Respectfully submitted,

/Hong Zhong/

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CERTIFICATE OF WORD COUNT

I hereby certify, pursuant to 37 C.F.R. section 42.24, that the foregoing Patent Owner Preliminary Response contains 13,900 words, excluding the words in the table of contents, table of authorities, mandatory notices under section 42.8, this certificate of word count, certificate of service or exhibit list. The word count is based on the word count of the Microsoft Word program used to prepare the Patent Owner Preliminary Response.

/Hong Zhong/
H. Annita Zhong (66,530)

CERTIFICATE OF SERVICE

I hereby certify, pursuant to 37 C.F.R. section 42.6, that on May 9, 2023, a complete copy of the **PATENT OWNER'S PRELIMINARY RESPONSE and EXHIBITS 2001-2007 and 2009-2022** were served upon the following, by ELECTRONIC MAIL:

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