

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.,
Petitioner,

v.

NETLIST, INC.,
Patent Owner.

Case No. IPR2023-00454
Patent No. 11,093,417

PATENT OWNER'S PRE-INSTITUTION SUR-REPLY

Mail Stop "PATENT BOARD"
Patent Trial and Appeal Board
U.S. Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450

TABLE OF CONTENTS

	<u>Page</u>
I. Discretionary Denial Under § 325(d) is Warranted	1
II. <i>Sotera</i> Stipulation does not moot <i>Fintiv analysis</i>	4

EXHIBIT LIST

Exhibit No.	Document
EX2001	Crisp, R., “Direct Rambus Technology: The New Main Memory Standard,” <i>IEEE Micro</i> , pp. 18-28 (1997)
EX2002	Datasheet for Samsung’s RIMM MR16R1624 (Wolfe Deposition Exhibit 2100)
EX2003	Deposition Transcript of Dr. Andrew Wolfe from IPR2022-00615
EX2004	Samsung datasheet on Rambus Direct RDRAM (Dec. 2001)
EX2005	Deposition Transcript of SungJoo Park in <i>Netlist, Inc. v. Samsung Electronics Co., Ltd.</i> , 2:21-cv-00463-JRG (E.D. Tex. November 23, 2022) (excerpt)
EX2006	Ex. 7 to Park Depo
EX2007	<i>Frequently Asked Questions</i> , What is the difference between a "bank" and a "rank?", Micron, https://web.archive.org/web/20141231144416/https://www.micron.com/support/faqs (last accessed Mar. 7, 2023).
EX2008	Reserved
EX2009	“XDR Architecture “ by Rambus (last modified December 2005), downloaded from https://web.archive.org/web/20110724044154/http://www.rambus.com/assets/documents/products/dl_0161_v0_8.pdf
EX2010	IDT, “DDR4 LRDIMMs Unprecedented Memory Bandwidth on Samsung DDR4 LRDIMM Enabled by IDT’s Register and Data Buffer,” downloaded from https://www.renesas.com/us/en/document/whp/ddr4-lrdimms-both-memory-capacity-and-speed

EX2011	“HyperCloud HCDIMM: Scaling the High Density Memory Cliff,” July 14, 2012, downloaded from https://web.archive.org/web/20120915083048/http://www.netlist.com/media/blog/hypercloud-memory-scaling-the-high-density-memory-cliff/
EX2012	<i>What is a Memory Rank</i> , Crucial: Micron, https://www.crucial.com/support/articles-faq-memory/what-is-a-memory-rank (last accessed Mar. 7, 2023)
EX2013	<i>Lecture 15: DRAM Main Memory Systems</i> , University of Utah, https://my.eng.utah.edu/~cs6810/pres/11-6810-15.pdf
EX2114	“Configuring and using DDR3 memory with HP ProLiant Gen8 Servers: Best Practice Guidelines for ProLiant Servers with Intel Xeon Processors” by HP, downloaded from https://web.archive.org/web/20121023195754/http://h20000.www2.hp.com/bc/docs/support/SupportManual/c03293145/c03293145.pdf
EX2015	Ganesh, B. et al., <i>Fully-Buffered DIMM Memory Architectures: Understanding Mechanisms, Overheads and Scaling</i> , HPCA (2007)
EX2116	Datasheet for Micron DDR2 SDRAM FBDIMM MT36HTF51272FD
EX2017	U.S. Patent No. 7,356,639 (“Perego-639”)
EX2018	Redline Comparison of EX1035 (U.S. Patent No. 7,363,422 to Perego) With Related U.S. Patent No. 7,356,639
EX2019	US District Court – Judicial Caseload Profile (as of December 31, 2022)
EX2020	JESD79-2B
EX2021	Amended Docket Control Order in <i>Netlist, Inc. v. Samsung Electronics Co. Ltd.</i> , 2:22-cv-00293-JRG (E.D. Tex. Feb. 1, 2023)

EX2022	Cover pleading of Samsung's invalidity contentions in <i>Netlist, Inc. v. Samsung Electronics Co. Ltd.</i> , 2:22-cv-00293-JRG (E.D. Tex. April 13, 2023)
EX2023	IPR2023-00203, Paper 8

I. Discretionary Denial Under § 325(d) is Warranted

Advanced Bionics Prong I: Petitioner insists that the examiner could not have considered the asserted references because they were submitted with many other references and not expressly discussed. Reply 1. That is sheer speculation because the examiner signed the IDS listing those references where he stated “ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /G.B./.” EX1002, 245, 247. He did not line through the asserted references. *Id.*

Petitioner then argues that discretionary denial is not warranted under the proposed rulemaking. Reply 1. The (controversial) proposed rulemaking is not in force, and does not govern the proceeding. Instead, the binding precedential *Advanced Bionics* holds that “[p]reviously presented art includes art provided to the Office by an applicant, such as the on an Information Disclosure Statement (IDS), in the prosecution history of the challenged patent.” *Advanced Bionics*, 7-8.

Wolfspeed is not on point because there, the second proceeding did not involve a reference that was the basis of the Board’s no-motivation-to-combine conclusion. It does not establish a new standard that discretionary denial under 325(d) requires a reference that was substantially discussed during prosecution.

Advanced Bionics Prong II: Petitioner acknowledges that it needs to show “the Office erred by overlooking something persuasive.” Reply 2. Yet, instead of presenting “evidence of previous Office error,” *Advanced Bionics*, 10, the Reply

only lists its disagreement with selected aspects of the POPR. Reply 2-4 (not disputing, e.g., POPR 25-33). This is insufficient under *Advanced Bionics*.

Petitioner first argues that the examiner identified Janzen as the closest art and Netlist does not contend the combination is cumulative of Janzen. Reply 2. The pertinent question is instead whether the examiner erred in finding that Janzen is closer art than the combination, a finding that Petitioner does not contest.

Petitioner then incorrectly argues that the Board has found Perego discloses or renders obvious “rank.” Reply 2. In IPR2022-00615, because of the RPI issue, Netlist’s POPR only had space to explore one reason why Perego does not disclose “ranks.” In IPR2023-00203, when Netlist provided additional reasoning, the Board declined to reach the merits for the Perego-based grounds. EX2023, Paper 8, 13. One reason why Perego does not disclose “rank[s]” as Petitioner defines is Perego configures its memory system—even if that system utilizes JEDEC-style DDR2—in a non-JEDEC manner. POPR 33-42; *cf.*, EX2014, 5 (Netlist’s HyperCloud DIMM uses DDR3, but is not itself a JEDEC-standardized module at the time).

Also contrary to Petitioner’s assertion, Dr. Wolfe did not testify that Perego used chip-select signals together with address signals to select a rank. EX2003, 82:14-83:14, 204:12-21; Reply 2-3. Instead, he testified that address information could be used as chip-selects (*id.*, 81:5-82:13), and that he “do[es] not think” Perego 15:37-45 “specifies how ranks are selected or enabled.” *Id.*, 202:8-204:10; POPR

33-34. As to Figure 5F versus 5E of Perego, the POPR discusses why neither supports Petitioner's theory. *See* POPR 34. Petitioner argues that Perego's buffer width could be fixed, but as noted in the POPR, the Petition relies on the "configurable width" characteristics of the buffer. POPR 17-18.

Petitioner then insists that because Perego could use DDR2 devices, a chip-select signal must have been received by Perego's buffer. Reply 3. JESD79-2, a specification for DDR devices, does not specify what signals are received by the memory module or buffers on the module, only what should be transmitted to DDRx. Petitioner also does not dispute that the chip-select signals needed by the DDR2 devices can be generated internally by Perego's buffer that can translate different signaling protocols. POPR 14, 20-21; EX1071:10:63-67; *cf.*, EX2015, 1 (FBDIMM's AMB buffer converts packetized information "to the DDRx protocol"). Petitioner argues that Perego may use a bus structure, but nothing in Perego states that chip-selects are transmitted over the bus. *See* POPR 15-17 (undisputed).

As the examiner found expressly, the prior art of record does not disclose limitations related to CAS latency of the memory modules. EX1002, 229. Petitioner disagrees, noting that JEDEC-compliant DDR RDIMMs would add one extra clock cycle. Reply 4. But not even Petitioner argues that Perego involves a JEDEC-compliant RDIMM. Petitioner also does not deny that Perego discloses caches that speed up data access, but argues that is an optional feature. *Id.* The pertinent question

is though why a POSITA would have added the extra clock cycle to slow data transfer when Perego has a solution that does not require one. As such, this disagreement does not show that the examiner has overlooked anything material. Petitioner also does not dispute factual underpinning on POPR 50-51, 56-57, contending only that Netlist has not submitted any supporting expert testimony. Reply 4. The lack of expert declaration at this stage does not even remotely establish that the examiner has overlooked something material. *Advanced Bionics*, 7-9.

Finally, concerning Halbert, Petitioner only contests whether the relied-on portion of Halbert necessarily requires simultaneous access to multiple ranks. Reply 4. That assertion is not only wrong (POPR 55-56), but also does not address the multitude of other reasons why Halbert does not cure the deficiencies of Perego or why the two are not combinable (POPR 56-59).

II. *Sotera* Stipulation does not moot *Fintiv* analysis.

Petitioner has attempted to evade *Sotera* stipulation in the district court by relying primarily on the asserted IPR references, but sprinkling references to APA, knowledge of POSITAs or system art. The Board should only consider a *Sotera* stipulation if Petitioner is willing to state explicitly which grounds it will pursue in the district court so the Board can evaluate the overlap between the two proceedings.

Dated: June 26, 2023

Respectfully submitted,
/Hong Zhong/
H. Annita Zhong (Reg. No. 66,530)

IRELL & MANELLA LLP
1800 Avenue of the Stars, Suite 900
Los Angeles, CA 90067
Tel: (310) 277-1010
Fax: (310) 203-7199
Email: HZhong@irell.com

CERTIFICATE OF SERVICE

I hereby certify, pursuant to 37 C.F.R. section 42.6, that on June 26, 2023, a complete copy of the **PATENT OWNER'S PRE-INSTITUTION SUR-REPLY** and **EXHIBIT 2023** were served upon the following, by ELECTRONIC MAIL:

BAKER BOTTS L.L.P.

Eliot D. Williams, Reg. No. 50,822
Theodore W. Chandler, Reg. No. 50,319
Ferenc Pazmandi, Reg. No. 66,216
John F. Gaustad, Reg. No. 69,522
Brianna L. Potter, Reg. No. 76,748

DLSamsungNetlistIPRs@BakerBotts.com

/Susan M. Langworthy/
Susan M. Langworthy