256Mbit XDR DRAM(F-die)

2M x 16(/8/4) bit x 8s Banks

Version 1.0

Jan. 2005

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Change History

Version 0.1(July 2004) - Preliminary
- First Copy *- Based on the Rambus XDR DRAM™ Datasheet Version 0.81*

Version 1.0(Jan. 2005)
- Delete "Preliminary" *- Based on the Rambus XDR DRAM™ Datasheet Version 0.85*

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Overview

The Rambus XDR DRAM device is a general-purpose high-performance memory device suitable for use in a broad range of applications, including computer memory, graphics, video, and any other application where high bandwidth and low latency are required.

The 256Mb XDR DRAM device is a CMOS DRAM organized as 16M words by 16bits. The use of Differential Rambus Signaling Level(DRSL) technology permits 4000/3200/2400 Mb/s transfer rates while using conventional system and board design technologies. XDR DRAM devices are capable of sustained data transfers up to 8000 MB/s.

XDR DRAM device architecture allows the highest sustained bandwidth for multiple, interleaved randomly addressed memory transactions. The highly-efficient protocol yields over 95% utilization while allowing fine access granuarity. The device's eight banks support up to four interleaved transactions.

Features

♦ Highest pin bandwidth available
- 4000/3200/2400 Mb/s Octal Data Rate(ODR) Signaling

♦ Bi-directional differential RSL(DRSL)
- Flexible read/write bandwidth allocation
- Minimum pin count

♦ Programmable on-chip termination
- Adaptive impedance matching
- Reduced system cost and routing complexity

♦ Highest sustained bandwidth per DRAM device
- Up to 8000 MB/s sustained data rate
- Eight banks : bank-interleaved transaction at full bandwidth
- Dynamic request scheduling
- Early-read-after-write support for maximum efficiency
- Zero overhead refresh

♦ Low Latency
- 2.0/2.5/3.33ns request packets
- Point-to-point data interconnect for fastest possible flight time
- Support for low-latency, fast-cycle cores

♦ Low Power
- 1.8V V_{DD}
- Programmable small-swing I/O signaling(DRSL)
- Low power PLL/DLL design
- Powerdown self-refresh support
- Per pin I/O powerdown for narrow-width operation

♦ 0.98us refresh intervals(16K/16ms refresh)

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Key Timing Parameters/Part Numbers

Organization	Bandwidth ($1/t_{BIT}$)[a]	Latency(t_{RAC})[b]	Bin[c,d]	Part Number
16Mx16	2400	36	A	K4Y54164UF-JCA2
	3200	35	B	K4Y54164UF-JCB3
	3200	35	C	K4Y54164UF-JCC3
	4000	28	C	K4Y54164UF-JCC4
32Mx8	2400	36	A	K4Y54084UF-JCA2
	3200	35	B	K4Y54084UF-JCB3
	3200	35	C	K4Y54084UF-JCC3
	4000	28	C	K4Y54084UF-JCC4
64Mx4	2400	36	A	K4Y54044UF-JCA2
	3200	35	B	K4Y54044UF-JCB3
	3200	35	C	K4Y54044UF-JCC3
	4000	28	C	K4Y54044UF-JCC4

a. Data rate measured in Mbit/s per DQ differential pair. See “Timing Conditions” on page 55 and “ Timing Characteristics” on page 58. Note that $tBIT=t_{CYCLE}/8$
b. Read access time t_{RAC} (= $t_{RCD-R}+t_{CAC}$) measured in ns. See “Timing Parameters” on page 59.
c. Timing parameter bin. See “Timing Parameters” on page 59. This is a measure of the number of interleaved read transactions needed for maximum efficiency (the value Ceiling(t_{RC-R}/t_{RR-D}). For bin A, $t_{RC-R}/t_{RR-D}=4$, and for bin B, $t_{RC-R}/t_{RR-D}=5$.
d. Bin support is vendor dependent.

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General Description

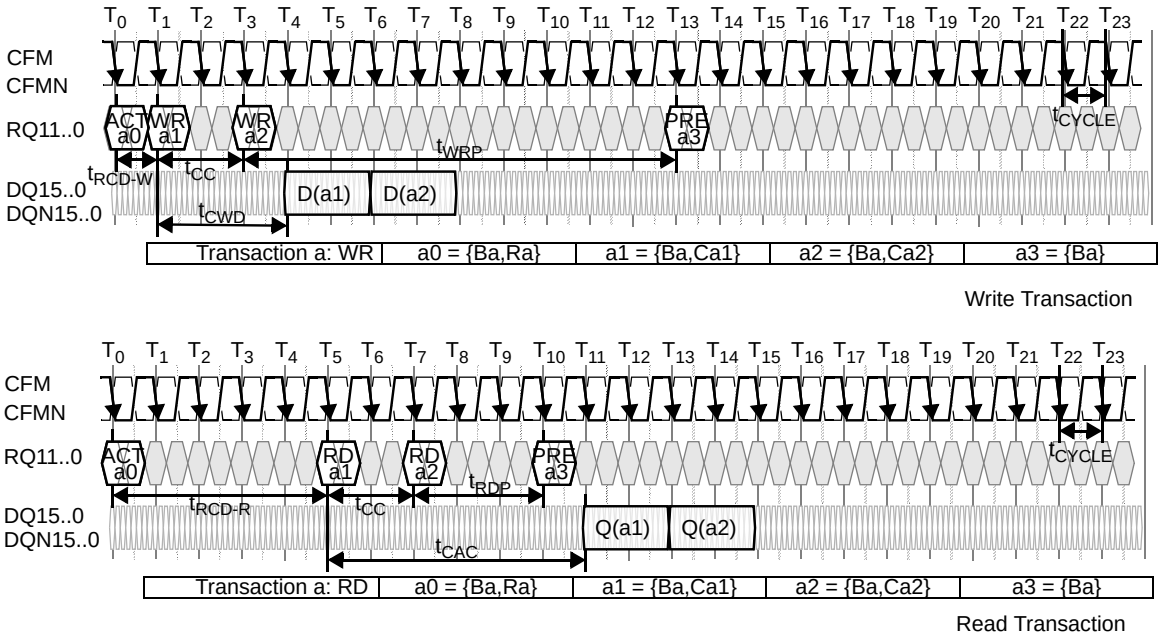
The timing diagrams in Figure 1 illustrate XDR DRAM device write and read transactions. There are three sets of pins used for normal memory access transactions: CFM/CFMN clock pins, RQ11..0 request pins, and DQ15..0/DQN15..0 data pins. The “N” appended to a signal name denotes the complementary signal of a differential pair.

A transaction is a collection of packets needed to complete a memory access. A packet is a set of bit windows on the signals of a bus. There are two buses that carry packets: the RQ bus and DQ bus. Each packet on the RQ bus uses a set of 2 bit-windows on each signal, while the DQ bus uses a set of 16 bit-windows on each signal.

In the write transaction shown in Figure 1, a request packet (on the RQ bus) at clock edge T_0 contains an activate (ACT) command. This causes row Ra of bank Ba in the memory component to be loaded into the sense amp array for the bank. A second request packet at clock edge T_1 contains a write (WR) command. This causes the data packet D(a1) at edge T_4 to be written to column Ca1 of the sense amp array for bank Ba. A third request packet at clock edge T_3 contains another write (WR) command. This causes the data packet D(a2) at edge T_6 to also be written to column Ca2. A final request packet at clock edge T_{13} contains a precharge (PRE) command.

The spacings between the request packets are constrained by the following timing parameters in the diagram: t_{RCD-W} , t_{CC} , and t_{WRP} . In addition, the spacing between the request packets and data packets is constrained by the t_{CWD} parameter. The spacing of the CFM/CFMN clock edges is constrained by t_{CYCLE}.

Figure 1 : XDR DRAM Device Write and Read Transactions



The read transaction shows a request packet at clock edge T_0 containing an ACT command. This causes row Ra of bank Ba of the memory component to load into the sense amp array for the bank. A second request packet at clock edge T_5 contains a read (RD) command. This causes the data packet Q(a1) at edge T_{11} to be read from column Ca1 of the sense amp array for bank Ba. A third request packet at clock edge T_7 contains another RD command. This causes the data packet Q(a2) at edge T_{13} to also be read from column Ca2. A final request packet at clock edge T_{10} contains a PRE command.

The spacings between the request packets are constrained by the following timing parameters in the diagram: t_{RCD-R} , t_{CC} , and t_{RDP} . In addition, the spacing between the request and data packets are constrained by the t_{CAC} parameter.

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Pinouts and Definitions

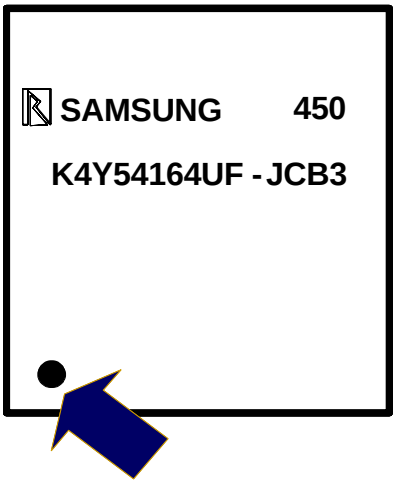
The following table shows the pin assignment of the center-bonded fanout XDR DRAM Package. The mechanical dimensions of this package are shown on page 71. Note - Pin #1 is at the A1 postion.

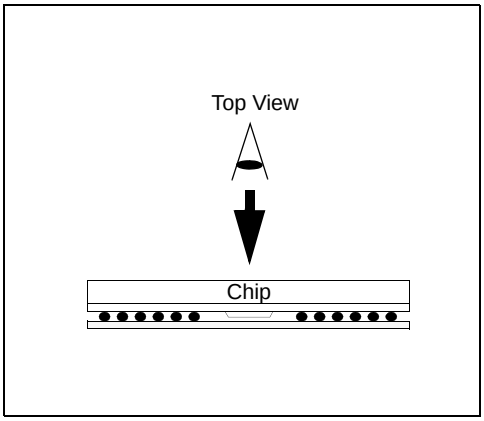
Table 1: 104ball XDR DRAM Package(Top View)

16	DQ10	DQ0	SDO	V_{DD}	GND		V_{DD}	V_{DD}	GND	DQ1	DQ11
15	DQN10	DQN0	RST						SCK	DQN1	DQN11
14	DQ6	DQ12	GND	RQ2	RQ5		RQ6	RQ8	CMD	DQ13	DQ7
13	DQN6	DQN12	V_{DD}	RQ1	V_{REF}		RQ7	RQ9	V_{DD}	DQN13	DQN7
12	V_{DD}	GND	GND			V_{DD}			GND	GND	V_{DD}
11	GND	V_{TERM}		V_{DD}	GND	GND	V_{DD}	GND		V_{TERM}	GND
10											
9											
8											
7											
6	GND	GND		V_{DD}	V_{DD}	GND	GND	GND		GND	GND
5	V_{DD}	V_{DD}	V_{TERM}			V_{DD}			V_{TERM}	V_{DD}	V_{DD}
4	DQ14	DQ4	GND	RQ3	RSRV		CFMN	RQ11	GND	DQ5	DQ15
3	DQN14	DQN4	RQ0	RQ4	RSRV		CFM	RQ10	V_{DD}	DQN5	DQN15
2	DQ2	DQ8	GND						V_{DD}	DQ9	DQ3
1	DQN2	DQN8	SDI	V_{DD}	GND		V_{DD}	GND	V_{DD}	DQN9	DQN3
Top View	A	B	C	D	E	F	G	H	J	K	L

ROW

COL





The pin #1(ROW1, COLA) is located at the A1 position on the top side and the A1 position is marked by the marker “ ”.

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Pin Description

Table2 summarizes the pin functionality of the XDR DRAM device. The first group of pins provide the necessary supply voltages. These include V_{DD} and GND for the core and interface logic, V_{REF} for receiving input signals, and V_{TERM} for the driving output signals.

The next group of pins are used for high bandwidth memory accesses. These include DQ15 ... DQ0 and DQN15 ... DQN0 for carrying read and write data signals, RQ11 ... RQ0 for carrying request signals, and CFM and CFMN for carrying timing information used by the DQ, DQN and RQ signals.

The final set of pins comprise the serial interface that is used for control register accesses. These include RST for initializing the state of the device, CMD for carrying command signals, SDI and SDO for carrying register read data, and SCK for carrying the timing information used by the RST, SDI, SDO, and CMD signals.

Table 2 : Pin Description

Signal	I/O	Type	No. of pins	Description
V_{DD}	-	-	22[a]	Supply voltage for the core and interface logic of the device.
GND	-	-	24[a]	Ground reference for the core and interface logic of the device.
V_{REF}	-	-	1	Logic threshold reference voltage for RSL signals.
V_{TERM}	-	-	4[a]	Termination voltage for DRSL signals.
DQ15..0	I/O	DRSL[b]	16	Positive data signals that carry write or read data to and from the device.
DQN15..0	I/O	DRSL[b]	16	Negative data signals that carry write or read data to and from the device.
RQ11..0	I	RSL[b]	12	Request signals that carry control and address information to the device.
CFM	I	DIFFCLK[b]	1	Clock from master — Positive interface clock used for receiving RSL signals, and receiving and transmitting DRSL signals from the Channel.
CFMN	I	DIFFCLK[b]	1	Clock from master — Negative interface clock used for receiving RSL signals, and receiving and transmitting DRSL signals from the Channel.
RST	I	RSL[b]	1	Reset input — This pin is used to initialize the device.
CMD	I	RSL[b]	1	Command input — This pin carries command, address, and control register write data into the device.
SCK	I	RSL[b]	1	Serial clock input — Clock source used for reading from and writing to the control registers.
SDI	I	RSL[b]	1	Serial data input — This pin carries control register read data through the device. This pin is also used to initialize the device.
SDO	O	CMOS[b]	1	Serial data output — This pin carries control register read data from the device. This pin is also used to initialize the device.
RSRV	-	-	2	Reserved pins — Follow Rambus XDR system design guidelines for connecting RSRV pins
Total pin count per package			104	

a. The exact number of V_{DD}/GND/V_{TERM} pins may vary between XDR DRAM vendors.
b. All DQ and CFM signals are high-true; low voltage is logic 0 and high voltage is logic 1.
All DQN, CFMN, RQ, RSL, and CMOS signals are low-true; high voltage is logic 0 and low voltage is logic 1.

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Block Diagram

A block diagram of the XDR DRAM device is shown in Figure2. It shows all interface pins and major internal blocks.

The CFM and CFMN clock signals are received and used by the clock generation logic to produce three virtual clock signals : $1/t_{CYCLE}$, $2/t_{CYCLE}$, and $16/t_{CC}$. The frequency of these signals are 1x, 2x, and 8x that of the CFM and CFMN signals. These virtual signals show the effective data rate of the logic blocks to which they connect; they are not necessarily present in the actual memory component.

The RQ11 ... RQ0 pins receive the request packet. Two 12-bit words are received in one t_{CYCLE} interval. This is indicated by the $2/t_{CYCLE}$ clocking signal connected to the 1:2 Demux Block that assembles the 24-bit request packet. These 24bits are loaded into a register(clocked by the $1/t_{CYCLE}$ clocking signal) and decoded by the Decode Block. The V_{REF} pin supplies a reference voltage used by the RQ receivers.

Three sets of control signals are produced by the Decode Block. These include the bank(BA) and row(R) addresses for an activate(ACT) command, the bank(BR) and row(REFr) addresses for a refresh activate(REFA) command, the bank(BP) address for a precharge(PRE) command, the bank(BR) adddress for a refresh precharge(REFP) command, and the bank(BC) and column(C and SC) addresses for a read(RD) or write(WR or WRM) command. In addition, a mask(M) is used for a masked write(WRM) command.

These commands can all be optionally delayed in increments of t_{CYCLE} under control of delay fields in the request. The control signals of the commands are loaded into registers and presented to the memory core. These registers are clocked at maximum rates determined by core timing parameters, in this case $1/t_{RR}$, $1/t_{PP}$, and $1/t_{CC}$(1/4, 1/4, and 1/2 the frequency of CFM in the -3200 component). These registers may be loaded at any t_{CYCLE} rising edge. Once loaded, they should not be changed until a t_{RR}, t_{PP}, or t_{CC} time later because timing paths of the memory core need time to settle.

A bank address is decoded for an ACT command. The indicated row of the selected bank is sensed and placed into the associated sense amp array for the bank. Sensing a row is also referred to as “Opening a page”for the bank.

Another bank address is decoded for a PRE command. The indicated bank and associated sense amp array are precharged to a state in which a subsequent ACT command can be applied. Precharging a bank is also called “closing the page” for the bank.

After a bank is given an ACT command and before it is given a PRE command, it may receive read(RD) and write(WR) column commands. These commands permit the data in the bank’s associated sense amp array to be accessed.

For a WR command, the bank address is decoded. The indicated column of the associated sense amp array of the selected bank is written with the data received from the DQ15 ... DQ0 pins.

The bank address is decoded for a RD command. The indicated column of the selected bank’s associated sense amp array is read. The data is transmitted onto the DQ15 ... DQ0 pins.

The DQ15 ... DQ0 pins receive the write data packet(D) for a write transaction. 16 sixteen-bit words are received in one t_{CC} interval. This is indicated by the $16/t_{CC}$ clocking signal connected to the 1:16 Demux Block that assembles the 16x16-bit write data packet. The write data is then driven to the selected Sense Amp Array Bank.

16 sixteen-bit words are accessed in the selected Sense Amp Array Bank for a read transaction. The DQ15 ... DQ0 pins transmit the read data packet(Q) in one t_{CC} interval. This is indicated by the $16/t_{CC}$ clocking signal connected to the 16:1 Mux Block. The V_{TERM} pin supplies a termination voltage for the DQ pins.

The RST, SCK, and CMD pins connect to the Control Register block. These pins supply the data, address and conrol needed to write the control registers. The read data for these registers is accessed through the SDO/SDI pins. These pins are also used to initialize the device.

The control registers are used to transition between power modes, and are also used for calibrating the high speed transmit and receive circuits of the device. The control registers also supply bank(REFB) and row(REFr) address for refresh operations.

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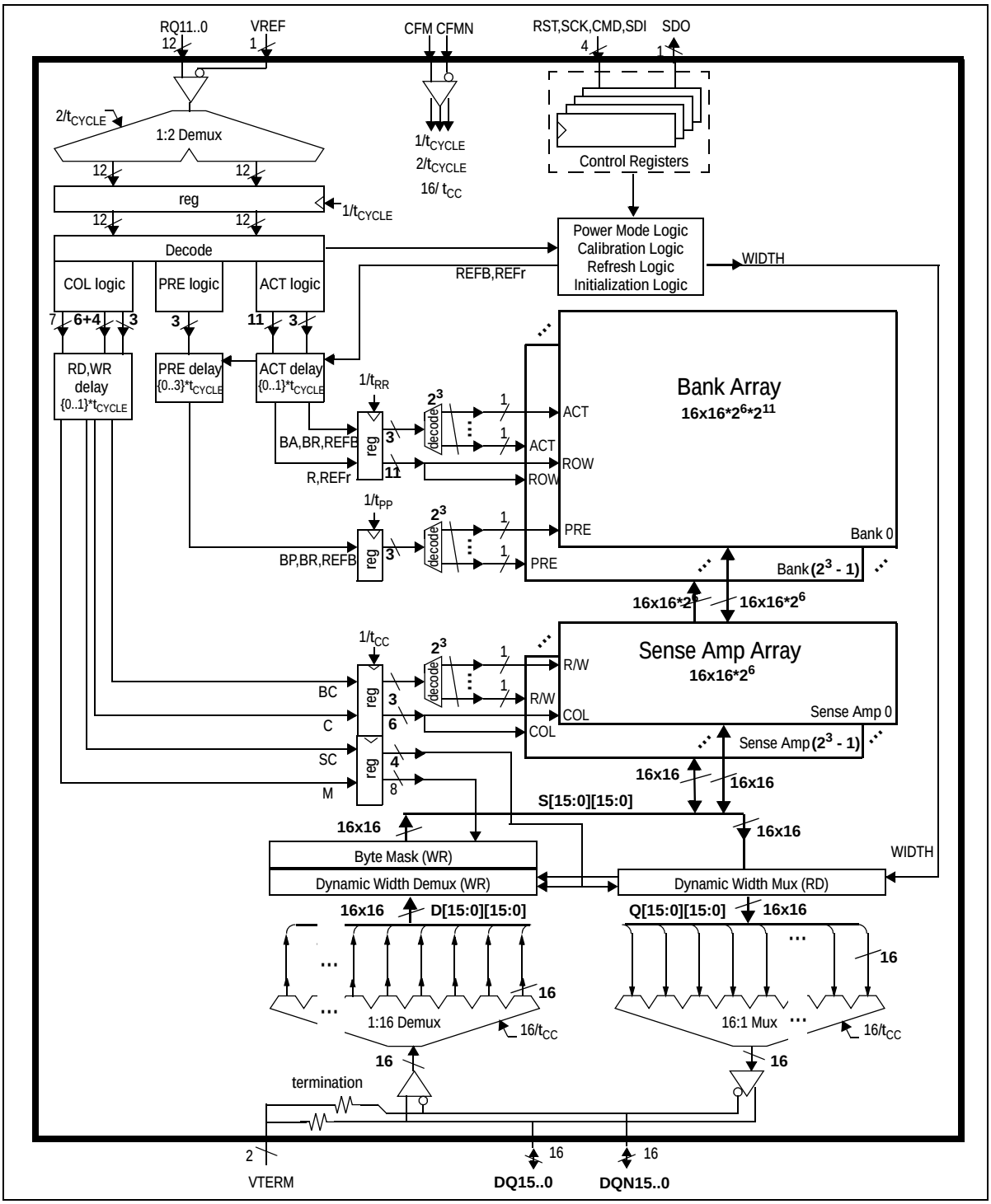
Figure 2 : 256Mb (8x2Mx16) XDR DRAM Block Diagram



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Request Packets

A request packet carries address and control information to the memory device. This section contains tables and diagrams for packet formats, field encodings and packet interactions.

Request Packet Formats

There are five types of request packets:

1. ROWA — specifies an ACT command
2. COL — specifies RD and WR commands
3. COLM — specifies a WRM command
4. ROWP — specifies PRE and REF commands
5. COLX — specifies the remaining commands

Table 3 describes fields within different request packet types. Various request packet type formats are illustrated in Figure3.

Each packet type consists of 24 bits sampled on the RQ11..0 pins on two successive edges of the CFM/CFMN clock. The request packet formats are distinguished by the OP3..0 field. This field also specifies the operation code of the desired command.

In the ROWA packet, a bank address (BA), row address (R), and command delay (DELA) are specified for the activate (ACT) command.

In the COL packet, a bank address (BC), column address (C), sub-column address (SC), command delay (DELC), and sub-opcode (WRX) are specified for the read (RD) and write (WR) commands.

In the COLM packet, a bank address (BC), column address (C), sub-column address (SC), and mask field (M) are specified for the masked write (WRM) command.

In the ROWP packet, two independent commands may be specified. A bank address (BP) and sub-opcode (POP) are specified for the precharge (PRE) commands. An address field (RA) and sub-opcode (ROP) are specified for the refresh (REF) commands.
In the COLX packet, a sub-operation code field (XOP) is specified for the remaining commands.

Table 3 : Request Field Description

Field	Packet Types	Description
OP3..0	ROWA/ROWP /COL/COLM/COLX	4-bit operation code that specifies packet format. (Encoded commands are in Table 4 on page 10.)
DELA	ROWA	Delay the associated row activate command by 0 or 1 t_{CYCLE} .
BA2..0	ROWA	3-bit bank address for row activate command.
R10..0	ROWA	11-bit row address for row activate command.
WRX	COL	Specifies RD (=0) or WR (=1) command.
DELC	COL	Delay the column read or write command by 0 or 1 t_{CYCLE} .
BC2..0	COL/COLM	3-bit bank address for column read or write command.
C9..4	COL/COLM	6-bit column address for column read or write command.
SC3..0	COL/COLM	4-bit sub-column address for dynamic width (see “Dynamic Width Control” on page 46).
M7..0	COLM	8-bit mask for masked-write command WRM.
POP2..0	ROWP	3-bit operation code that specifies row precharge command with a delay of 0 to 3 t_{CYCLE}. (Encoded commands are in Table 6 on page 11).
BP2..0	ROWP	3-bit bank address for row precharge command.
ROP2..0	ROWP	3-bit operation code that specifies refresh commands. (Encoded commands are in Table 5 on page 10).
RA7..0	ROWP	8-bit refresh address field (specifies BR bank address, delay value, and REFr load value)
XOP3..0	COLX	4-bit extended operation code that specifies calibration and powerdown commands. (Encoded commands are in Table 7 on page 11).

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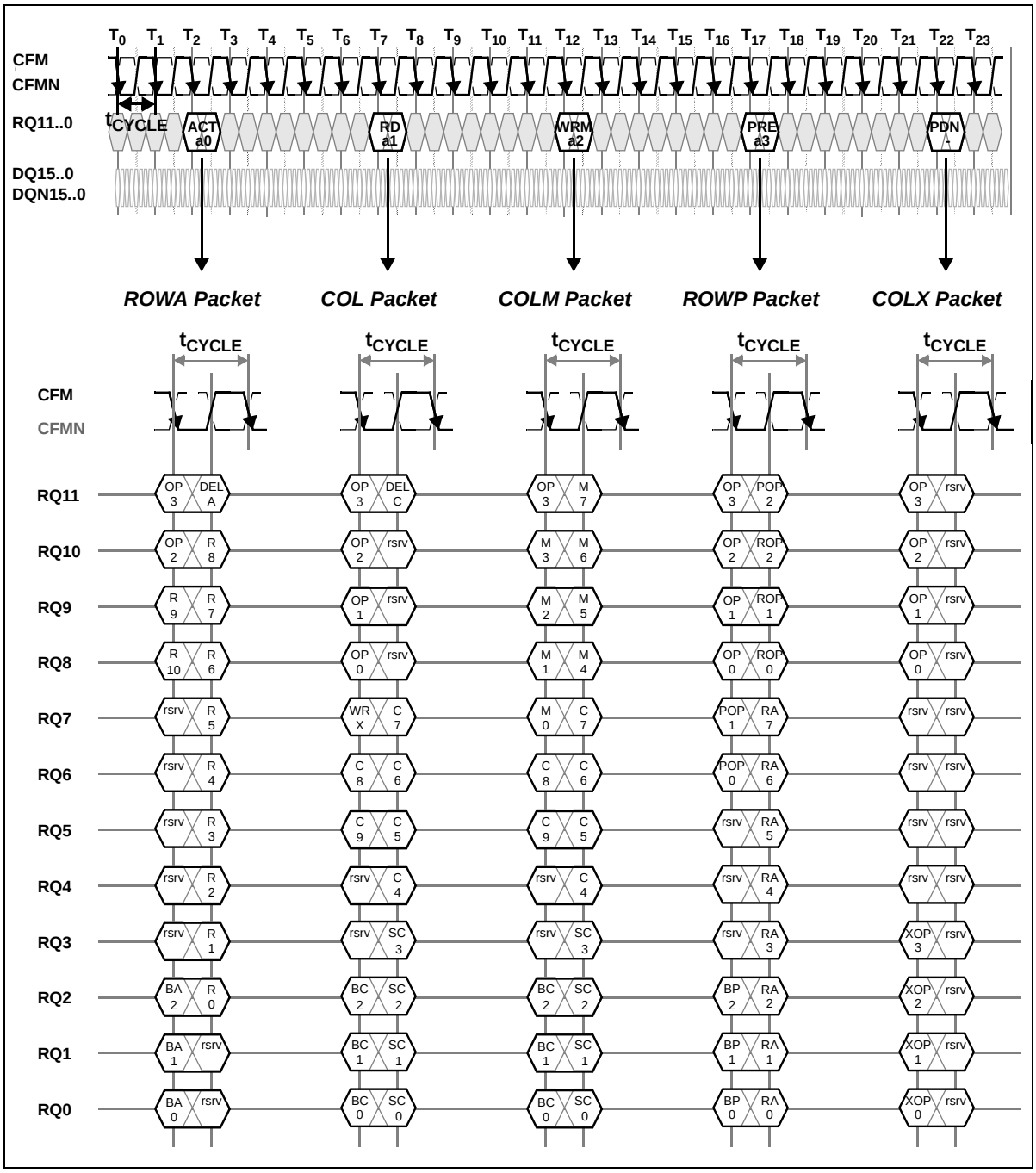
Figure 3 : Request Packet Formats



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Request Field Encoding

Operation code fields are encoded within different packet types to specify commands. Table4 through Table7 provides packet type and encoding summaries.

Table4 shows the OP field encoding for five packet types. The COLM and ROWA packets each specify a single command : ACT and WRM. The COL, COLX, and ROWP packets each use additional fields to specify multiple commands : WRX, XOP, and POP/ROP, respectively. The COLM packet specifies the masked write command WRM. This is like the WR unmasked write command, except that a mask field M7...0 indicates whether each byte of the write data packet is written or not written. The ROWA packet specifies the row activate command ACT. The COL packet uses the WRX field to specify the column read and column write(unmasked) commands.

Table 4 : OP Field Encoding Summary

OP [3:0]	Packet	Command	Description
0000	-	NOP	No operation.
0001	COL	RD	Column read (WRX=0). Column C9..4 of sense amp in bank BC2..0 is read to DQ bus after DELC*t_{CYCLE}.
		WR	Column write (WRX=1). Write DQ bus to column C9..4 of sense amp in bank BC2..0 after DELC*t_{CYCLE}.
0010	COLX	CALy	XOP3..0 specifies a calibrate or powerdown command — see Table 7 on page 11.
0011	ROWP	PREx	POP2..0 specifies a row precharge command — see Table 6 on page 11.
		REFy,LRRr	ROP2..0 specifies a row refresh command or load REFr register command — see Table 5 on page 10.
01xx	ROWA	ACT	Row activate command. Row R10..0 of bank BA2..0 is placed into the sense amp of the bank after DELA*t_{CYCLE}.
1xxx	COLM	WRM	Column write command (masked) — mask M7..0 specifies which bytes are written.

Encoding of the ROP field in the ROWP packet is shown in Table5. The first encoding specifies a NOPR (no operation) command. The REFP command uses the RA field to select a bank to be precharged. The REFA and REFI commands use the RA field and REFH/M/L registers to select a bank and row to be activated for refresh. The REFI command also increments the REFH/M/L register. The REFP, REFA, and REFI commands may also be delayed by up to 3*t_{CYCLE} using the RA[7:6] field. The LRR0, LRR1, and LRR2 commands load the REFH/M/L registers from the RA[7:0] field.

Table 5 : ROP Field Encoding Summary

ROP[2:0]	Command	Description
000	NOPR	No operation
001	REFP	Refresh precharge command. Bank RA2..0 is precharged. This command is delayed by {0,1,2,3}*t_{CYCLE} (the value is given by the expression (2*RA[7]+RA[6]).
010	REFA	Refresh activate command. Row R[10:0] (from REFH/M/L register) of bank RA2..0 is placed into sense amp. This command is delayed by {0,1,2,3}*t_{CYCLE} (the value is given by the expression (2*RA[7]+RA[6]).
011	REFI	Refresh activate command. Row R[10:0] (from REFH/M/L register) of bank RA2..0 is placed into sense amp. This command is delayed by {0,1,2,3}*t_{CYCLE} (the value is given by the expression (2*RA[7]+RA[6]). R[10:0] field of REFH/M/L register is incremented after the activate command has completed.
100	LRR0	Load Refresh Low Row register (REFL). RA[7:0] is stored in R[7:0] field.
101	LRR1	Load Refresh Middle Row register (REFM). RA[2:0] is stored in R[10:8] field.
110	LRR2	Load Refresh High Row register — not used with this device.
111	-	Reserved

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The REFH/M/L registers are also refreshed to as the REFr registers. Note that only the bits that are needed for specifying the refresh row(11 bits in all) are implemented in the REFr registers - the rest are reserved. Note also that the RA2 ... RA0 field that specifies the refresh bank address is also referred to as BR2...0. See “Refresh Transactions” on page37.

Table6 shows the POP field encoding in the ROWP packet. The first encoding specifies a NOPP(no operation) command. There are four variations of PRE(precharge) command. Each uses the BP field to specify the bank to be precharged. Each also specifies a different delay of up to 3*t_{CYCLE} using the POP[1:0] field. A precharge command may be specified in addition to a refresh command using the ROP field.

Table 6 : POP Field Encoding Summary

POP[2:0]	Command	Description
000	NOPP	No operation.
001	-	Reserved.
010	-	Reserved.
011	-	Reserved.
100	PRE0	Row precharge command — Bank BP2..0 is precharged. This command is delayed by 0*t_{CYCLE}.
101	PRE1	Row precharge command — Bank BP2..0 is precharged. This command is delayed by 1*t_{CYCLE}.
110	PRE2	Row precharge command — Bank BP2..0 is precharged. This command is delayed by 2*t_{CYCLE}.
111	PRE3	Row precharge command — Bank BP2..0 is precharged. This command is delayed by 3*t_{CYCLE}.

Table7 shows the XOP field encoding in the COLX packet. This field encodes the remaining commands.

The CALC and CALE commands perform calibration operations to ensure signal integrity on the Channel. See “Calibration Transactions” on page 39.

The PDN command causes the device to enter a power-down state. See”Power State Management” on page 40.

Table 7 : XOP Field Encoding Summary

XOP [3:0]	Command	Command and Description	XOP [3:0]	Command	Command and Description
0000	-	Reserved.	1000	CALC	Current calibration command.
0001	-	Reserved.	1001	CALZ	Impedance calibration command.
0010	-	Reserved.	1010	CALE	End calibration command (CALC).
0011	-	Reserved.	1011	-	Reserved.
0100	-	Reserved.	1100	PDN	Enter powerdown power state.
0101	-	Reserved.	1101	-	Reserved.
0110	-	Reserved.	1110	-	Reserved.
0111	-	Reserved.	1111	-	Reserved.

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Request Field Interactions

A summary of request packet interaction is Table8. Each case is limited to request packets with commands that perform memory operations(including refresh commands). This includes all commands in ROWA, ROWP, COL, and COLM packets. The commands in COLX packets are described in later sections. See “Maintenance Operations” on page38.

Request packet/command “a” is followed by request/ command “b”. The minimum possible spacing between these two packet/command is $0*t_{CYCLE}$. However, a larger time interval may be needed because of a resource interaction between the two packet/commands. If the minimum possible sapcing is $0*t_{CYCLE}$, then an entry of “No limit” is shown in the table.

Note that the spacing values shown in the table are relative to the effective beginning of a packet/command. The use of the delay field with a command will delay the position of the effective packet/command from the position of the actual packet/command. See “Dynamic Request Scheduling” on page18 .

Any of the packet/command encoding under one of the four operation types is equivalent in terms of the resource constraints. Therefore. both the horisontal columns(packet “a”) and vertical rows(packet “b”) of the interaction table are divided into four major groups.

The four possible operation types for request packet a and b include :

: [A] Active Row ROWA/ACT
ROWP/REFA
ROWP/REFI
: [R] Read Column COL/RD
: [W] Write Column COL/WR
COLM/WRM
: [P] Precharge Row ROWP/PRE
ROWP/REFP

Table 8 : Packet Interaction Summary

First packet/command to bank Ba		Second packet/command to bank Bb			
		Activate Row [A]	**Read Column [R]**	**Write Column [W]**	**Precharge Row [P]**
		ROWA - ACT Bb ROWP - REFA Bb ROWP - REFI Ba	**COL - RD Bb**	**COL - WR Bb COLM - WRM Bb**	**ROWP - PRE Bb ROWP - REFP Bb**
Activate Row [A] ROWA - ACT Ba ROWP - REFA Ba ROWP - REFI Ba	Ba,Bb different	Case AAd: t_{RR}	Case ARd: No limit	Case AWd: No limit	Case APd: No limit
	Ba,Bb same	Case AAs: t_{RC}	Case ARs: t_{RCD-R}	Case AWs: t_{RCD-W}	Case APs: t_{RAS}
Read Column [R] COL - RD Ba	Ba,Bb different	Case RAd: No limit	Case RRd: t_{CC}	Case RWd:[a] $t_{\Delta RW}$	Case RPd: No limit
	Ba,Bb same	Case RAs:[b] $t_{RDP}+t_{RP}$	Case RRs: t_{CC}	Case RWs: [a] $t_{\Delta RW}$	Case RPs: t_{RDP}
Write Column [W] COL - WR Ba COLM - WRM Ba	Ba,Bb different	Case WAd: No limit	Case WRd:[c] $t_{\Delta WR}$	Case WWd: t_{CC}	Case WPd: No limit
	Ba,Bb same	Case WAs[b]:$t_{WRP}+t_{RP}$	Case WRs:[c] $t_{\Delta WR}$	Case WWs: t_{CC}	Case WPs: t_{WRP}
Precharge Row [P] ROWP - PRE Ba ROWP - REFP Ba	Ba,Bb different	Case PAd: No limit	Case PRd: No limit	Case PWd: No limit	Case PPd: t_{PP}
	Ba,Bb same	Case PAs: t_{RP}	Case PRs:[d] $t_{RP}+t_{RCD-R}$	Case PWs:[d] $t_{RP}+t_{RCD-W}$	Case PPs: t_{RC}
See Examples:		Figure 4	Figure 5	Figure 6	Figure 7

a. $t_{\Delta RW}$ is equal to $t_{CC} + t_{RW-BUB,XDRDRAM} + t_{CAC} - t_{CWD}$ and is defined in Table 18. This also depends upon propagation delay - See “Propagation Delay” on page 27.
b. A PRE command is needed between the RD and ACT/REFA commands or the WR/WRM and ACT/REFA commands.
c. $t_{\Delta RW}$ is defined in Table 18.
d. An ACT command is needed between the PRE/REFP and RD commands or the PRE/REFP and WR/WRM commands.

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The first request is shown along the vertical axis on the left of the table. The second request is shown along the horizontal axis at the top of the table. Each request includes a bank specification “Ba” and “Bb”. The first and second banks may be the same, or they may be different. These two subcases for each interaction are shown along the vertical axis on the letf.

There are 32 possible interaction cases altogether. The table gives each case a label of the form “xyz”, where “x” and “y” are one of the four operation types(“A” for Activate, “R” for Read, “W” for Write, or “P” for Precharge) for the first and second request, respectively, and “z” indicates the same bank(“s”) or different bank(“d”).

Along the horizontal axis at the bottom of the table are cross references to four figures(Figure4 through Figure7). Each figure illustrates the eight cases in the corresponding vertical column. Thus, Figure4 shows the eight cases when the second request is an activate operation(“A”). In the following discussion of the cases, only those in which the interaction interval is greater than t_{CYCLE} will be described.

Request Interactions Cases

In Figure4. the interaction interval for the AAd case is t_{RR}. This parameter is the row-to-row time and is the minimum interval between activate commands to different banks of a device.

The interaction interval for the AAs case is t_{RC}. This is the row cycle time parameter and is the minimum interval between activate commands to same banks of a device. A precharge operation must be inserted between the two activate operations.

The interaction interval for the RAs case is t_{RDP} + $t_{RP.}$ A precharge operation must be inserted between the read and activate operation. The minimum interval between a read and a precharge operation to a bank is t_{RDP}. The minimum interval between a precharge and an activate operation to a bank is t_{RP}.

The interaction interval for the WAs case is t_{WDP} + $t_{RP.}$ A precharge operation must be inserted between the read and the activate operation. The minimum interval between a write and a precharge operation to a bank is t_{WDP}. The minimum interval between a precharge and an activate operation to a bank is t_{RP}.

The interaction interval for the PAs case is t_{RP}. The minimum interval between a precharge and an activate operation to a bank is t_{RP}.

In Figure5, the interaction interval for the ARs case is t_{RCD-R}. This is the row-to-column-read time parameter and represents the minimum interval between an activate operation and a read operation to a bank.

The interaction interval for the RRd and RRs cases is t_{CC}. This is the column-to-column time parameter and represents the minimum interval between two read operations.

The interaction interval for the WRd and WRs cases is $t_{\Delta WR}$. This is the write-to-read time parameter and represents the minimum interval between a write and a read operation to any banks. See “Read/Write Interaction” on page 26.

The interaction interval for the PRs case is t_{RP} + t_{RCD-R}. An activate operation must be inserted between the precharge and the read operation. The minimum interval between a precharge and an activate operation to a bank is t_{RP}. The minimum interval between an activate and a read operation to a bank is t_{RCD-R}.

In Figure6. the interaction interval for the AWs case is t_{RCD-W}. This is the row-to-column-write timing parameter and represents the minimum interval between an activate operation and a write operation to a bank.

The interaction interval for the RWd and RWs cases is $t_{\Delta RW}$. This is the read-to-write time parameter and represents the minimum interval between a read and a write operation to any banks. See “Read/Write Interaction” on page26.

The interaction interval for the WWd and WWs cases is t_{CC}. This is the column-to-column time parameter and represents the minimum interval between two write operations.

The interaction interval for the PWs case is t_{RP} + t_{RCD-W}. An activate operation must be inserted between the precharge and the write operation. The minimum interval between a precharge and an activate operation to a bank is t_{RP}. The minimum interval between an activate and a write operation to a bank is t_{RCD-W}.

In Figure7, the interaction interval for the APs case is t_{RAS}. This parameter is the minimum activate-to-precharge time to a bank.

The interaction interval for the RPs and WPs cases are t_{RDP} and t_{WDP}, respectively. These are the read-or write-to-precharge time parameters to a bank.

Ths interaction interval for the PPd case is t_{PP}. This parameter is the precharge-to-precharge time and the minimum interval between precharge commands to different banks of a device.

The interaction interval for the PPs case is t_{RC}. This is the row cycle time parameter and the minimum interval between precharge commands to same banks of a device. An activate operation must be inserted between the two activate operations. This activate operation must be placed a time t_{RP} after the first, and a time t_{RAS} before the second precharge.

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Figure 4 : ACT-, RD-, WR-, PRE-to-ACT Packet Interactions

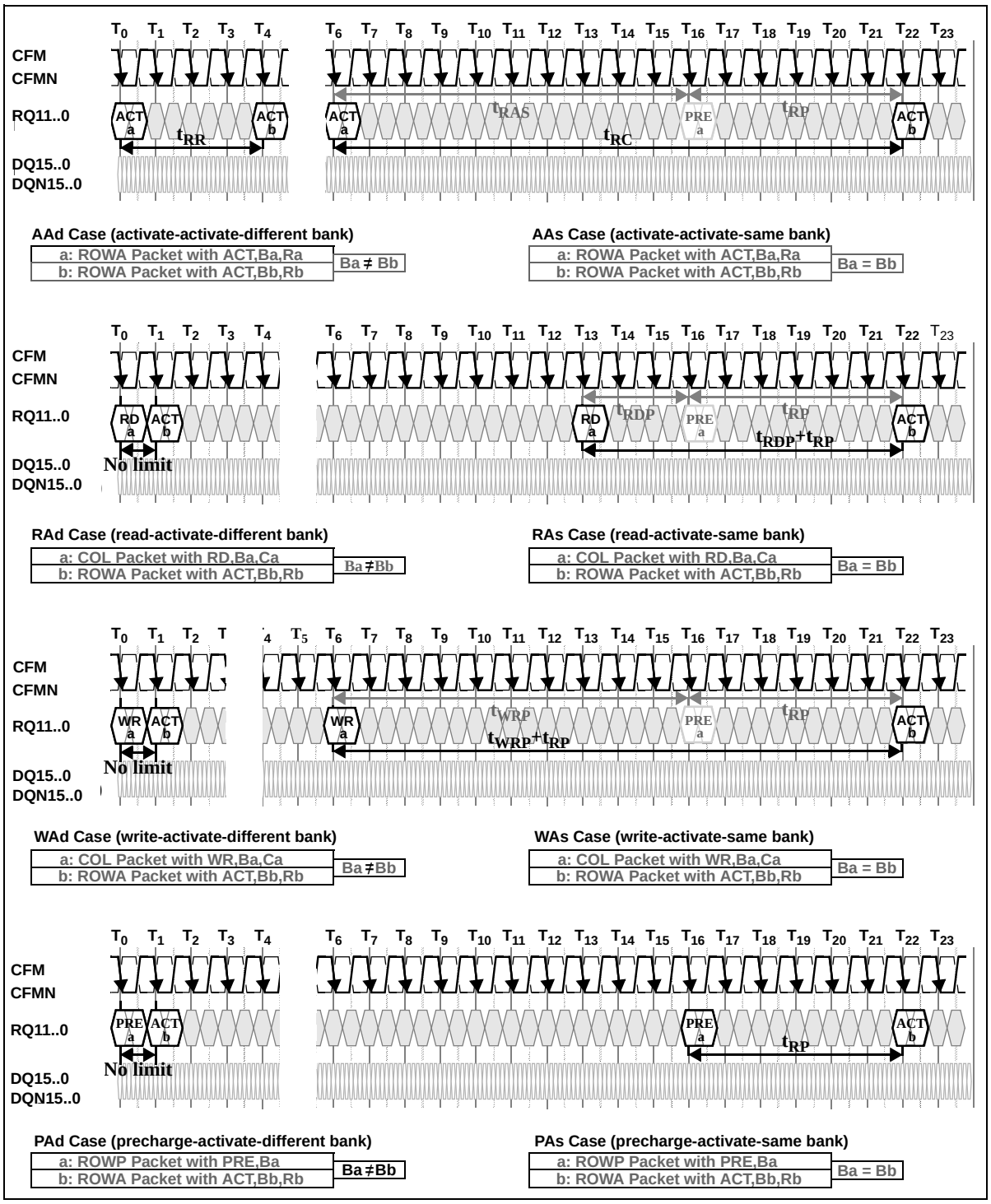

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Figure 5 : ACT-, RD-, WR-, PRE-to-RD Packet Interactions

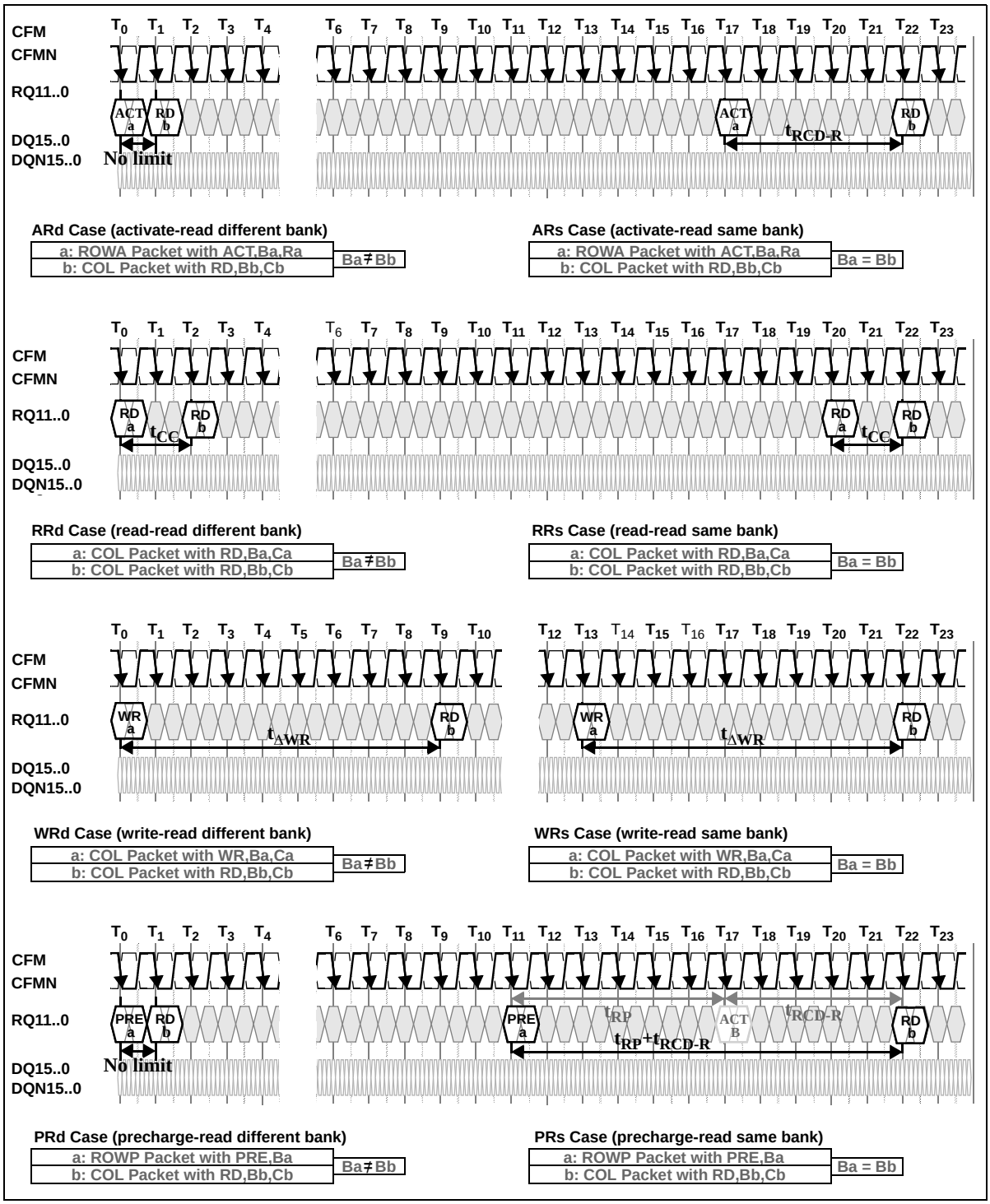

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Figure 6 : ACT-, RD-, WR-, PRE-to-WR Packet Interactions

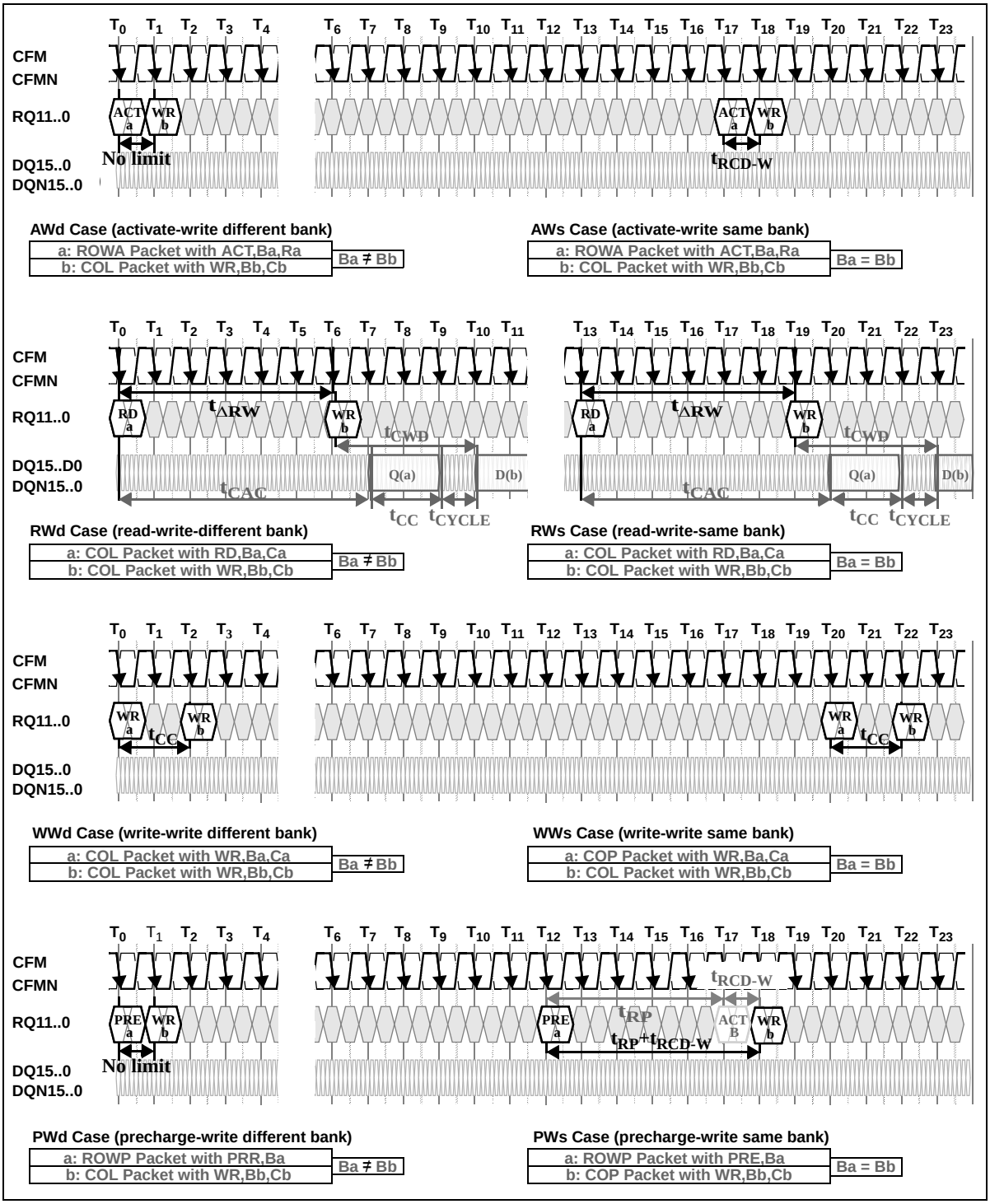

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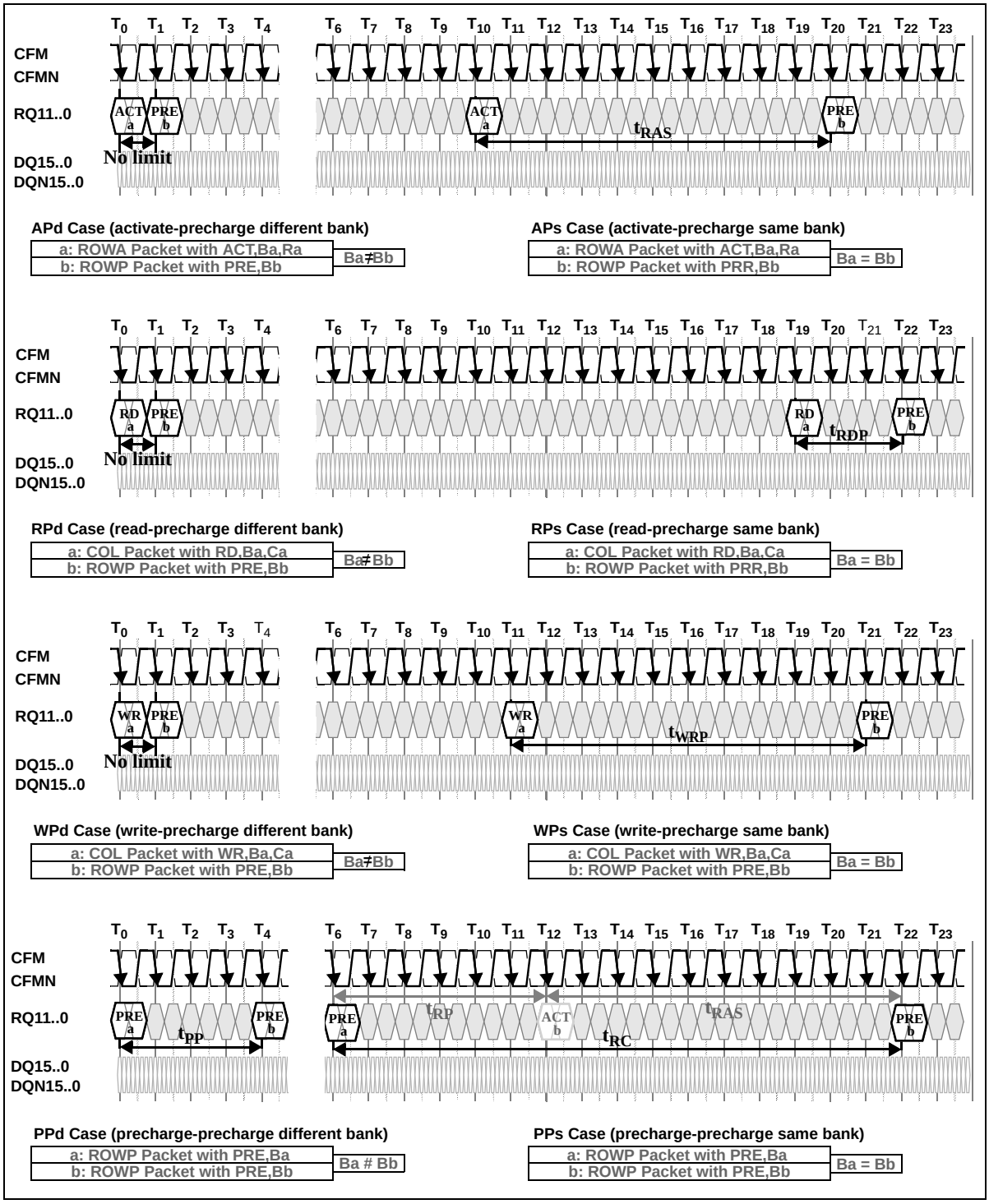
Figure 7 : ACT-, RD-, WR-, PRE-to-PRE Packet Interactions



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Dynamic Request Scheduling

Delay fields are present in the ROWA, COL, and ROWP packet. They permit the associated command to optionally wait for a time of one (or more) t_{CYCLE} before taking effect. This allows a memory controller more scheduling flexibility when issuing request packets. Figure8 illustrates the use of the delay fields.

In the first timing diagram, a ROWA packet with an ACT command is present at cycle T_0. The DELA field is set to “1”. This request packet will be equivalent to a ROWA packet with an ACT command at cycle T_1 with the DELA field is set to “0”. This equivalence should be used when analyzing request packet interactions.

In the second timing diagram, a COL packet with a RD command is present at cycle T_0. The DELC field is set to “1”. This request packet will be equivalent to a COL packet with an RD command at cycle T_1 with the DELC field is set to “0”. This equivalence should be used when analyzing request packet interactions.

In a similar fashion, a COL packet with a WR command is present at cycle T_{12}. The DELC field is set to”1”. This request packet will be equivalent to a COL packet with a WR command at cycle T_{13} with the DELC field is set to “0”. This equivalence should be used when analyzing request packet interactions.

In the COL packet with a RD command example, the read data delay, t_{CAC} is measured between the Q read data packet and the virtual COL packet at cycle T_1.

Likewise, for the example with the COL packet with a WR command, the write data delay, t_{CWD} is measured between the D write data packet and the virtual COL packet at cycle T_{13}.

In the third timing diagram, a ROWP packet with a PRE command is present at cycle T_0. The DEL field(POP[1:0]) is set to “11”. This request packet will be equivalent to a ROWP packet with a PRE command at cycle T_1 with the DEL field is set to “10”, it will be equivalent to a ROWP packet with a PRE commmand at cycle T_2 with the DEL field is set to “01”, and it will be equivalent to a ROWP packet with a PRE command at cycle T_3 with the DEL field is set to “00”. This equivalence should be used when analyzing request packet interactions.

In the fourth timing diagram, a ROWP packet with a REFP command is present at cycle T_0. The DEL field(RA[7:6]) is set to “11”. This request packet will be equivalent to a ROWP packet with a REFP command at cycle T_1 with the DEL field is set to “10”, it will be equivalent to a ROWP packet with a REFP command at cycle T_2 with the DEL field is set to “01”, and it will be equivalent to a ROWP packet with a REFP command at cycle T_3 with the DEL field is set to “00”. This equivalence should be used when analyzing request packet interactions.

The two examples for the REFA and REFI commands are identical to the example just described for the REFP command.

The ROWP packet allows two independent operations to be specified. A PRE precharge command uses the POP and BP fields, and the REFP, REFA, or REFI commands use the ROP and RA fields. Both operations have an optional delay field(the POP field for the PRE command and the RA field with the REFP, REFA, or REFI commands). The two delay mechanisms are independent of one another. The POP field does not affect the timing of the REFP, REFA, or REFI commands, and the RA field does not affect the timing of the PRE command.

When the interactions of a ROWP packet are analyzed, it must be remembered that there are two independent commands specified, both of which may affect how soon the next request packet can be issued. The constraints from both commands in a ROWP packet must be considered, and the one that requires the longer time interval to the next request packet must be used by the memory controller. Furthermore, the two commands within a ROWP packet may not reference the same bank in the BP and RA fields.

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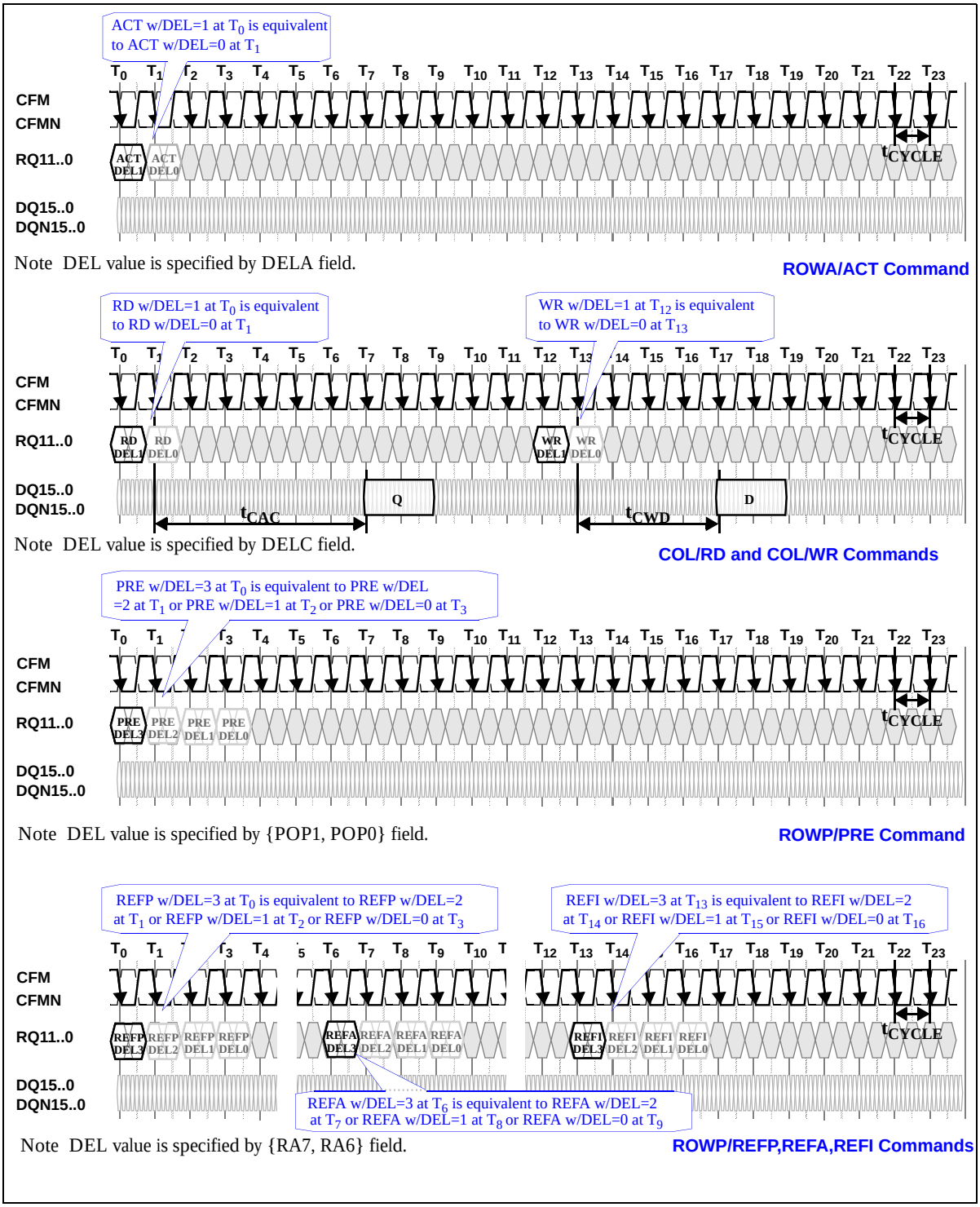
Figure 8 : Request Scheduling Examples



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Memory Operations

Write Transactions

Figure9 shows four examples of memory write transactions. A transaction is one or more request packets (and the associated data packets) needed to perform a memory access. The state of the memory core and the address of the memory access determine how many request packets are needed to perform the access.

The first timing diagram shows a page-hit write transaction. In this case, the selected bank is already open (a row is already present in the sense amp array for the bank). In addition, the selected row for the memory access matches the address of the row already sensed (a page hit). This comparison must be done in the memory controller. In this example, the access is made to row Ra of bank Ba.

In this case, write data may be directly written into the sense amp array for the bank, and row operations(activated or precharge) are not needed. A COL packet with WR command to column Ca1 of bank Ba is presented on edge T_0, and a second COL packet with WR command to column Ca1 of bank Ba is presented on edge T_2. Two write data packets D(a1) and D(a2) follow these COL packets after the write data delay t_{CWD}. The two COL packets are separated by the column-cycle time t_{CC}. This is also the length of each write data packet.

The second timing diagram shows an example of a page-miss write transaction. In this case, the selected bank is already open (a row is already present in the sense amp array for the bank). However, the selected row for the memory access does not match the address of the row already sensed (a page miss). This comparsion must be done in the memory controller. In this example, the access is made to row Ra of bank Ba, and the bank contains a row other than Ra.

In this case, write data may not be directly written into the sense amp array for the bank. It is necessary to close the present row (precharge) and access the requested row (activate). A precharge command (PRE to bank Ba) is presented on edge T_0. An activate command (ACT to row Ra of bank Ba) is presented on edge T_6 a time t_{RP} later. A COL packet with WR command to column Ca1 of bank Ba is presented on edge T_7 a time t_{RCD-W} later. A second COL packet with WR command to column Ca2 of bank Ba is presented on edge T_9. Two write data packets D(a1) and D(a2) follow these COL packets after the write data delay t_{CWD}. The two COL packets are separated by the column-cycle time t_{CC}. This is also the length of each write data packet.

The third timing diagram shows an example of a page-empty wirte transaction. In this case, the selected bank is already closed (no row is present in the sense amp array for the bank). No row comparison is necessary for this case; however, the memory controller must still remember that bank Ba has been left closed. In this example, the access is made to row Ra of bank Ba.

In this case, write data may not be directly written into the sense amp array for the bank. It is necessary to access the requested row (activate). An activate command (ACT to row Ra of bank Ba) is presented on edge T0. A COL packet with WR command to column Ca1 of bank Ba is presented on edge T_1 a time t_{RCD-W} later. A second COL packet with WR command to column Ca2 of bank Ba is presented on edge T_3. Two write data packets D(a1) and D(a2) follow these COL packets after the write data delay t_{CWD}. The two COL packets are separated by the column-cycle time t_{CC}. This is also the length of each write data packet. After the final write command, it may be necessary to close the present row (precharge). A precharge command (PRE to bank Ba) is presented on edge T_{14} a time t_{WRP} after the last COL packet with a WR command. The decision whether to close the bank or leave it open is made by memory controller and its page policy.

The fourth timing diagram shows another example of a page-empty write transaction. This is similar to the previous example except that only a single write command is presented, rather than two write commands. This example shows that even with a minimum length write transaction, t_{RAS} parameter will not be a constraint. The t_{RAS} measures the minimum time between an activate command and a precharge command to a bank. This time interval is also constrained by the sum $t_{RCD-W} + t_{WRP}$ which will be larger for a write transaction. These two constraints (t_{RAS} and $t_{RCD-W} + t_{WRP}$) will be a function of the memory device's speed bin and the data transfer length (the number of write commands issued between the activate and precharge commands), and the t_{RAS} parameter could become a constraint for future speed bins. In this example, the sum $t_{RCD-W} + t_{WRP}$s is greater than t_{RAS} by the amount Δt_{RAS}.

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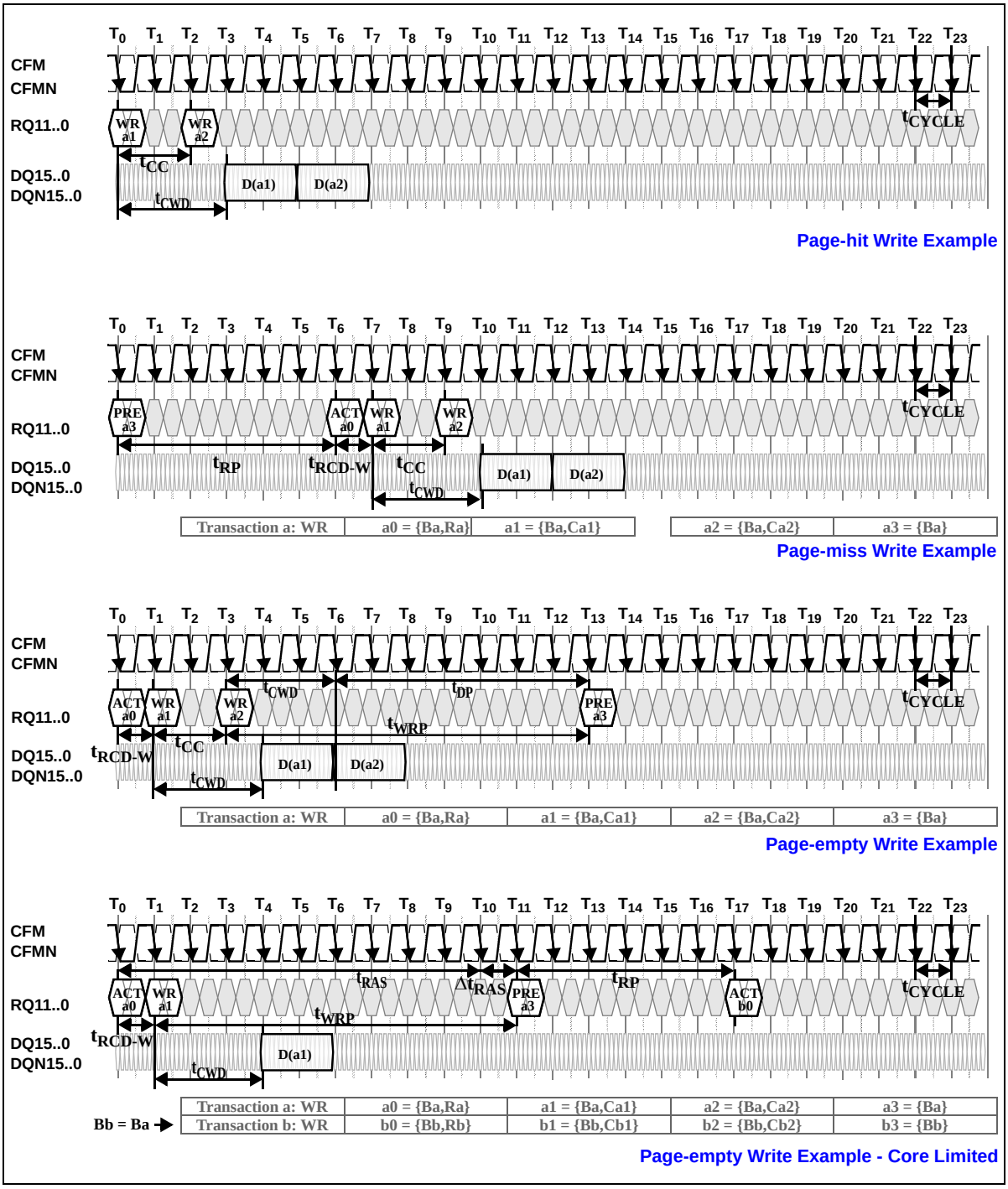
Figure 9 : Write Transactions



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Read Transactions

Figure10 shows four examples of memory read transactions. A transaction is one or more request packets (and the associated data packets) needed to perform a memory access. The state of the memory core and the address of memory access determine how many request packets are needed to perform the access.

The first timing diagram shows a page-hit read transaction. In this case, the selected bank is already open (a row is already present in the sense amp array for the bank). In addition, the selected row for the memory access matches the address of the row already sensed (a page hit). This comparison must be done in the memory controller. In this example, the access is made to row Ra of bank Ba.

In this case, read data may be directly read from the sense amp array for the bank and no row operations (actiavate or precharge) are needed. A COL packet with RD command to column Ca1 of bank Ba is presented on edge T_0 and a second COL packet with RD command to column Ca2 of bank Ba is presented on edge T_2. Two read data packets Q(a1) and Q(a2) follow these COL packets after the read data delay t_{CAC}. The two COL packets are separated by the column-cycle time t_{CC}. This is also the length of each read data packet.

The second timing diagram shows an example of a page-miss read transaction. In this case, the selected bank is already open (a row is already present in the sense amp array for the bank). However, the selected row for the memory access does not match the address of the row already sensed(a page miss). This comparison must be done in the memory controller. In this example, the access is made to row Ra of bank Ba, and the bank contains a row other than Ra.

In this case, read data may not be directly read from the sense amp array for the bank. It is necessary to close the present row (precharge) and access the requested row (activate). A precharge command (PRE to bank Ba) is presented on edge T_0. An activate command (ACT to row Ra of bank Ba) is presented on edge T_6 a time t_{RP} later. A COL packet with RD command to column Ca1 of bank Ba is presented on edge T_{11} a time t_{RCD-R} later. A second COL packet with RD command to column Ca2 of bank Ba is presented on edge T_{13}. Two read data packets Q(a1) and Q(a2) follow these COL packets after the read data delay t_{CAC}. The two COL packets are separated by the column-cycle time t_{CC}. This is also the length of each read data packet.

The third timing diagram shows an example of a page-empty write transaction. In this case, the selected bank is already closed (no row is present in the sense amp array for the bank). No row comparison is necessary for this case; however, the memory controller must still remember that bank Ba has been left closed. In this example, the access is made to row Ra of bank Ba.

In this case, read data may not be directly read from the sense amp array for the bank. It is necessary to access the requested row (activated). An activate command (ACT to row Ra of bank Ba) is presented on edge T_0. A COL packet with RD command to column Ca1 of bank Ba is presented on edge T_5 a time t_{RCD-R} later. A second COL packet with RD command to column Ca2 of bank Ba is presented on edge T_7. Two read data packets Q(a1) and Q(a2) follow these COL packets after the read data delay t_{CAC}. The two COL packets are separated by the column-cycle time t_{CC}. This is also the length of each read data packet. After the final read command, it may be necessary to close the present row (precharge). A precharge command - PRE to bank Ba - is presented on edge T_{10} a time t_{RDP} after the last COL packet with a RD command. Whether the bank is closed or left open depends on the memory controller and its page policy.

The fourth timing diagram shows another example of a page-empty read transaction. This is similar to the previous example except that it uses one read command instead of two read commands. In this case, the core parameter t_{RAS} may also be a constraint upon when the precharge command may be issued.

The t_{RAS} measures the minimum time between an activate command and a precharge command to a bank. This time interval is also constrained by the sum t_{RCD-R} + t_{RDP} and must be set to whichever is larger. These two constraints (t_{RAS} and t_{RCD-R} + t_{RDP}) will be a function of the memory device's speed bin and the data transfer length (the number of read commands issued between the activate and precharge commands). In this example, the t_{RAS} is greater than the sum t_{RCD-R} + t_{RDP} by the amount Δt_{RDP}.

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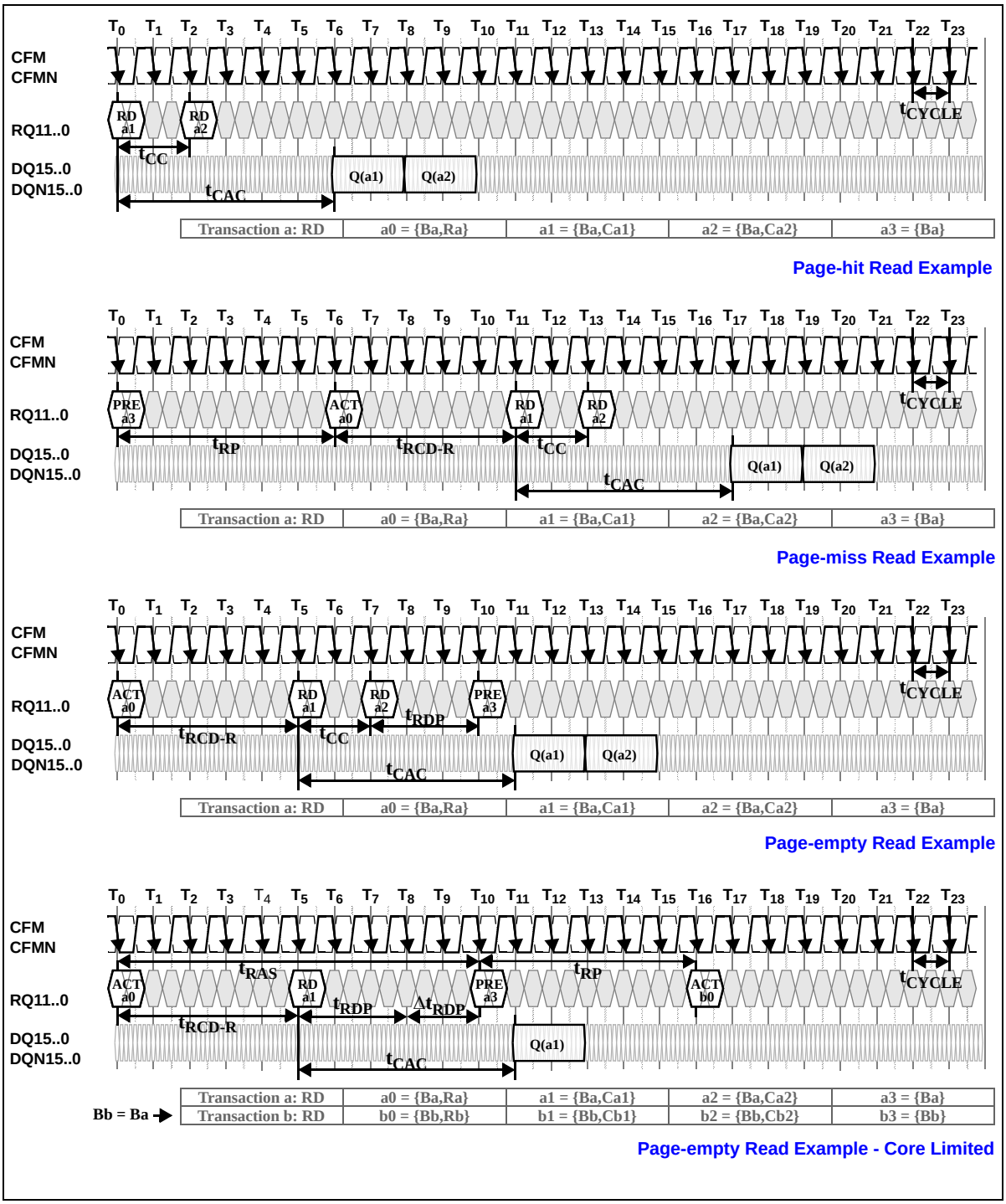
Figure 10 : Read Transactions



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Interleaved Transactions

Figure11 shows two examples of interleaved transactions. Interleaved transactions are overlapped with one another; a transaction is started before an earlier one is completed.

The timing diagram at the top of the figure shows interleaved write transactions. Each transaction assumes a page-empty access; that is, a bank is in a closed state prior to an access and is precharged after the access. With this assumption, each transaction requires the same number of request packets at the same relative positions. If bank were allowed to be in an open state, then each transaction would require a different number of request packets depending upon whether the transaction was page-empty, page-hit or page-miss. This situation is more complicated for the memory controller and will not be analyzed in this document.

In the interleaved page-empty write example, there are four sets of request pins RQ11...0 shown along the left side of the timing diagram. The first three show the timing slots used by each of the three requests packet types (ACT, COL and PRE), and the fourth set (ALL) shows the previous three merged together. This allows the pattern used for allocating request slots for the different packets to be seen more clearly.

The slots at {T_0, T_4, T_8, T_{12} ...} are used for ROWA packets with ACT commands. This spacing is determined by the t_{RR} parameter. There should not be interference between the interleaved transactions due to resource conflicts because each bank address - Ba, Bb, Bc, Bd and Be - is assumed to be different from another. If two of the bank addresses are the same, the later transaction would need to wait until the earlier transaction had completed its precharge operation. Five different banks are needed because the effective t_{RC} ($t_{RC} + \Delta t_{RC}$) is $20*t_{CYCLE}$.

The slots at {T_1, T_3, T_5, T_7, T_9, T_{11}, ...} are used for COL packets with WR commands. This frequency of the COL packet spacing is determined by the t_{CC} parameter and by the fact that there are two column accesses per row access. The phasing of the COL packet spacing is determined by the t_{RCD-W} parameter. If the value of t_{RCD-W} required the COL packets to occupy the same request slots as the ROWA packets (this case is not shown), the DELC field in the COL packet could be used to place the COL packet one t_{CYCLE}s earlier.

The DQ bus slots at {T_7, T_9, T_{11}, T_{13}, ...} carry the write data packets {D(a1), D(a2), D(b1), D(b2), ...}. Two write data packets are written to a bank in each transaction. The DQ bus is completely filled with write data; no idle cycles need to be introduced because there are no resource conflicts in this example.

The slots at {T_{14}, T_{18}, T_{22}, ...} are used for ROWP packets with PRE commands. This frequency of ROWP packet spacing is determined by the t_{PP} parameter. The phasing of the ROWP packet spacing is determined by the t_{WRP} paramter. If the value of t_{WRP} required the ROWP packets to occupy the same request slots as the ROWA or COL packets already assigned (this case is not shown), the delay field in the ROWP packet could be used to place the ROWP packet one or more t_{CYCLE} earlier.

There is an example of an interleaved page-empty read at the bottom of the figure. As before, there are four sets of request pins RQ11...0 shown along the left side of the timing diagram, allowing the pattern used for allocating request slots for the different packets to be seen more clearly.

The slots at {T_0, T_4, T_8, T_{12}, ...} are used for ROWA packets with ACT command. This spacing is determined by the t_{RR} parameter. There should not be interference between the interleaved transactions due to resource conflicts because each bank address - Ba, Bb, Bc and Bd - is assumed to be different from another. Four different banks are needed because the effective t_{RC} is $16 * t_{CYCLE}$.

The slots at {T_5, T_7, T_9, T_{11}, ...} are used for COL packets with RD commands. This frequency of the COL packet spacing is determined by the t_{CC} paramter and by the fact that there are two column accesses per row access. The phasing of the COL packet spacing is determined by the t_{RCD-R} parameter. If the value of t_{RCD-R} required the COL packets to occupy the same request slots as the ROWA packets (this case is not shown), the DELC field in the COL packet could be used to place the packet one t_{CYCLE} earlier.

The DQ bus slots at {T_{11}, T_{13}, T_{15}, T_{17}, ...} carry the read data packets {Q(a1), Q(a2), Q(b1), Q(b2), ...}, Two read data packets are read from a bank in each transaction. The DQ bus is completely filled with read data - That is, no idle cycles need to be introduced because there are no resource conflicts in this example.

The slots at {T_{10}, T_{14}, T_{18}, T_{22}, ...} are used for ROWP packets with PRE commands. This frequency of the ROWP packet spacing is determined by the t_{PP} parameter. The phasing of the ROWP packet spacing is determined by the t_{RDP} parameter. If the value of t_{RDP} required the ROWP packets to occupy the same request slots as the ROWA or COL packets already assigned (this case is not shown), the delay field in the ROWP packet could be used to place the ROWP packet one or more t_{CYCLE}s earlier.

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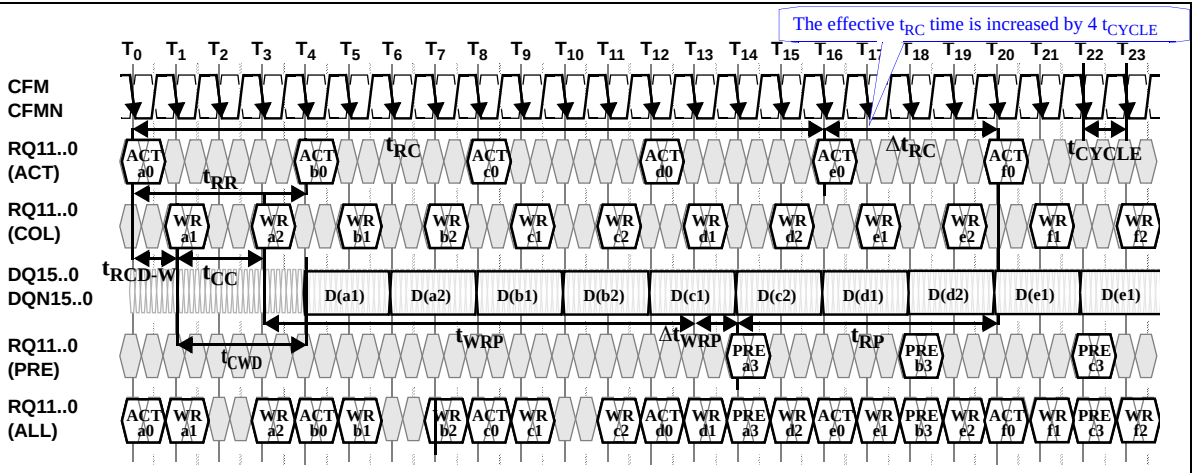
Figure 11 : Interleaved Transactions

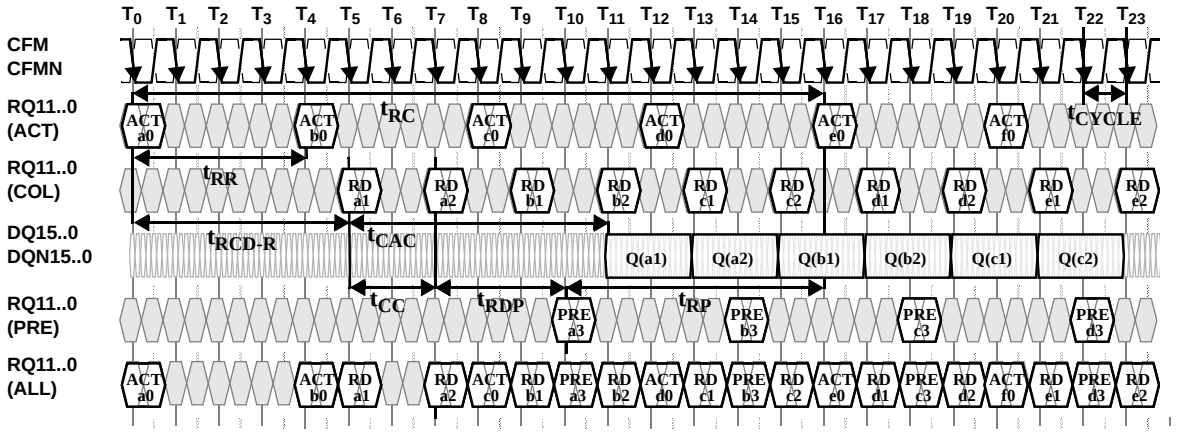


Ba,Bb,Bc,Bd,Be are different banks.

Bf = Ba

Transaction a: WR	a0 = {Ba,Ra}	a1 = {Ba,Ca1}	a2 = {Ba,Ca2}	a3 = {Ba}
Transaction b: WR	b0 = {Bb,Rb}	b1 = {Bb,Cb1}	b2 = {Bb,Cb2}	b3 = {Bb}
Transaction c: WR	c0 = {Bc,Rc}	c1 = {Bc,Cc1}	c2 = {Bc,Cc2}	c3 = {Bc}
Transaction d: WR	d0 = {Bd,Rd}	d1 = {Bd,Cd1}	a2 = {Bd,Cd2}	d3 = {Bd}
Transaction e: WR	e0 = {Be,Re}	e1 = {Be,Ce1}	e2 = {Be,Ce2}	e3 = {Be}
Transaction f: WR	e0 = {Bf,Rf}	f1 = {Bf,Cf1}	f2 = {Bf,Cf2}	f3 = {Bf}

Interleaved Page-empty Write Example



Ba,Bb,Bc,Bd are different banks.

Be = Ba

Transaction a: RD	a0 = {Ba,Ra}	a1 = {Ba,Ca1}	a2 = {Ba,Ca2}	a3 = {Ba}
Transaction b: RD	b0 = {Bb,Rb}	b1 = {Bb,Cb1}	b2 = {Bb,Cb2}	b3 = {Bb}
Transaction c: RD	c0 = {Bc,Rc}	c1 = {Bc,Cc1}	c2 = {Bc,Cc2}	c3 = {Bc}
Transaction d: RD	d0 = {Bd,Rd}	d1 = {Bd,Cd1}	a2 = {Bd,Cd2}	d3 = {Bd}
Transaction e: RD	e0 = {Be,Re}	e1 = {Be,Ce1}	e2 = {Be,Ce2}	e3 = {Be}

Interleaved Page-empty Read Example

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Read/Write Interaction

The previous section described overlapped read transactions and overlapped write transactions in isolation. This section will describe the interaction of read and write transactions and the spacing required to avoid channel and core resource conflicts.

Figure12 shows a timing diagram (top) for the first case, a write transaction followed by a read transaction. Two COL packets with WR commands are presented on cycles T_0 and T_2. The write data packets are presented a time t_{CWD} later on cycles T_4 and T_6. The device requires a time $t_{\Delta WR}$ after the second COL packet with a WR command before a COL packet with a RD command may be presented. Two COL packets with RD commands are presented on cycles T_{11} and T_{13}. The read data packets are returned a time t_{CAC} later on cycles T_{17} and T_{19}. The time $t_{\Delta WR}$ is required for turning around internal bi-directional interconnections (inside the device). This time must be observed regardless of whether the write and read commands are directed to same banks or different banks. A gap $t_{WR\text{-}BUB,XDRDRAM}$ will appear on the DQ bus between the end of the D(a2) packet and the beginning of the Q(b1) packet (measured at the appropriate packet reference points). The size of this gap can be evaluated by calculating the difference between cycles T_2 and T_{17} using the two timing paths :

$t_{WR\text{-}BUB,\ XDRDRAM} = t_{\Delta WR} + t_{CAC} - t_{CWD} - t_{CC}$

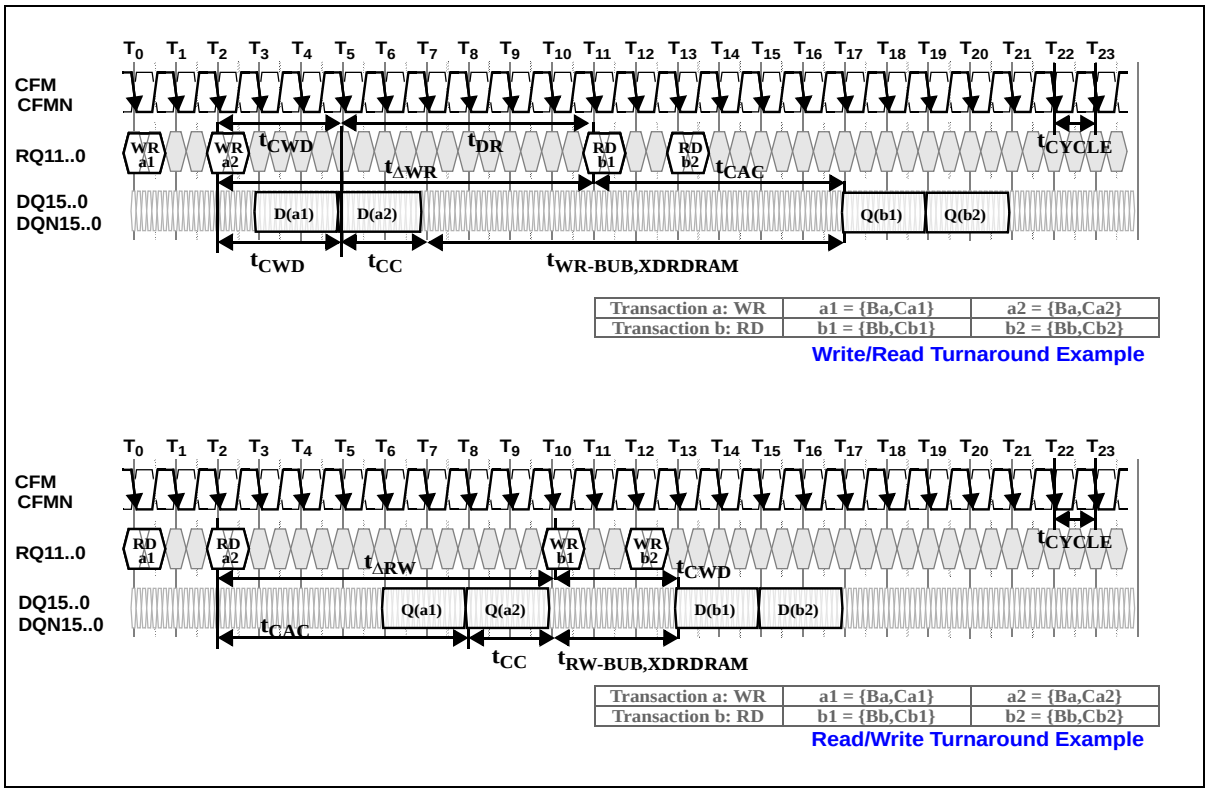
In this example, the value of $t_{WR\text{-}BUB,XDRDRAM}$ is greater than its minimum value of $t_{WR\text{-}BUB,XDRDRAM,MIN}$. The values of $t_{\Delta WR}$ and t_{CAC} are equal to their minimum values.

In the second case, the timing diagram displayed at the bottom of Figure12 illustrates a read transaction followed by a write transaction. Two COL packets with RD commands are presented on cycles T_0 and T_2. The read data packets are returned a time t_{CAC} later on cycles T_6 and T_8. The device requires a time $t_{\Delta RW}$ after the second COL packet with a RD command before a COL packet with a WR command may be presented. Two COL packets with WR commands are presented on cycles T_{10} and T_{12}. The write data packets are presented a time t_{CWD} later on cycles T_{13} and T_{15}. The time $t_{\Delta RW}$ is required for turning around the external DQ bi-directional interconnections (outside the device). This time must be observed regardless whether the read and write commands are directed to the same banks or different banks. The time $t_{\Delta RW}$ depends upon four timing parameters. and may be evaluated by calculating the difference between cycles T_2 and T_{11} using the two timing paths :

$t_{\Delta RW} + t_{CWD} = t_{CAC} + t_{CC} + t_{RW\text{-}BUB,\ XDRDRAM}$ or $t_{\Delta RW} = (t_{CAC} - t_{CWD}) + t_{CC} + t_{RW\text{-}BUB,\ XDRDRAM}$

In this example, the values of $t_{\Delta RW}$, t_{CAC}, t_{CWD}, t_{CC}, and $t_{WR\text{-}BUB,\ XDRDRAM}$ are equal to their minimum values.

Figure 12 : Write/Read Interaction



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Propagation Delay

Figure 13 shows two timing diagrams that display the system-level timing relationships between the memory component and the memory controller.

The timing diagram at the top of the figure shows the case of a write-read-write command and data at the memory component. In this case, the timing will be identical to what has already been shown in the previous sections; i,e. with all timing measured at the pins of the memory component. This timing diagram was produced by merging portions of the top and bottom timing diagrams in Figure12.

The example shown is that of a single COL packet with a write command, followed by a single COL packet with a read command, followed by a second COL packet with a write command. These accesses all assume a page-hit to an open bank.

A timing interval $t_{\Delta WR}$ is required between the first WR command and the RD command, and a timing interval $t_{\Delta RW}$ is required between the RD command and the second WR command. There is a write data delay t_{CWD} between each WR command and the associated write data packet D. There is a read data delay t_{CAC} between the RD command and the associated read data packet Q. In this example, all timing parameters have assumed their minimum values except $t_{WR\text{-}BUB,\ XDRDRAM}$.

The lower timing diagram in the figure shows the case where timing skew is present between the memory controller and the memory component. This skew is the result of the propagation delay of signal wavefronts on the wire carrying the signals.

The example in the lower diagram assumes that there is a propagation delay of $t_{PD\text{-}RQ}$ along both the RQ wires and the CFM/CFMN clock wires between the memory controller and the memory component (the value of $t_{PD\text{-}RQ}$ used here is $1*t_{CYCLE}$). Note that in an actual system the $t_{PD\text{-}RQ}$ value will be different for each memory component connected to the RQ wires.

In addition, it is assumed that there is a propagation delay $t_{PD\text{-}D}$ along the DQ/DQN wires between the memory controller and the memory component (the direction in which write data travels, and it is assumed that there is the same propagation delay $t_{PD\text{-}Q}$ along the DQ/DQN wires between the memory component and the memory controller (the direction in which read data travels). The sum of these two propagation delays is also denoted by the timing parameter $t_{PD,CYC} = t_{PD\text{-}D} + t_{PD\text{-}Q}$.

As a result of these propagation delays, the position of packets will have timing skews that depend upon whether they are measured at the pins of the memory controller or the pins of memory component. For example, the CFM/CFMN signals at the points of the memory component are $t_{PD\text{-}RQ}$ later than at the pins of the memory controller. This is shown by the cycle numbering of the CFM/CFMN signals at the two locations - in this example cycle T_1 at the memory controller.

All the request packets on the RQ wires will have a $t_{PD\text{-}RQ}$ skew at the memory component relative to the memory controller in this example. Because the $t_{PD\text{-}D}$ propagation delay of write data matches the $t_{PD\text{-}RQ}$ propagation delay of the write command, the controller may issue the write data packet D(a0) relative to the COL packet with the first write command “WR(a0)” with normal write data delay t_{CWD}. If the propagation delays between the memory controller and memory component were different for the RQ and DQ buses (not shown in this example), the write data delay at the memory controller would need to be adjusted.

A propagation delay is seen by the read command - that is, the read command will be delayed by a $t_{PD\text{-}RQ}$ skew at the memory component relative to the memory controller. The memory componet will return the read data packet Q(b0) relative to this read command with the normal read data delay t_{CAC} (at the pins of the memory componet).

The read data packet will be skewed by an additional propagation delay of $t_{PD\text{-}Q}$ as it travels from the memory component back to the memory controller. The effective read data delay measured between the read command and the read data at the memory controller will be $t_{CAC} + t_{PD\text{-}RQ} + t_{PD\text{-}Q}$.

$t_{PD\text{-}RQ}$ factor is casued by the propagaion delay of the request packets as they travel from memory controller to memory component. The $t_{PD\text{-}Q}$ factor is casued by the propagation delay of the read data packets as they travel from memory componet to memory controller.

All timing parameters will be equal to their minimum values except $t_{WR\text{-}BUB,XDRDRAM}$ (as in the top diagram), and the timing parameters $t_{RW\text{-}BUB,XDRDRAM}$ and $t_{\Delta RW}$. These will be larger than their minimum values by the amount $(t_{PD,CYC} - t_{PD,CYC,MIN})$, where $t_{PD,CYC} = t_{PD\text{-}D} + t_{PD\text{-}Q}$. This may be seen by evaluating the two timing paths between cycle T_9 at th controller and cycle T_{21} at the XDR DRAM:

$t_{\Delta RW} + t_{PD\text{-}RQ} + t_{CWD} = t_{PD\text{-}RQ} + t_{CAC} + t_{CC} + t_{RW\text{-}BUB,XDRDRAM}$ or $t_{\Delta RW} = (t_{CAC} - t_{CWD}) + t_{CC} + t_{RW\text{-}BUB,XDRDRAM}$

The following relationship was shown for Figure12.

$t_{\Delta RW,\ MIN} = (t_{CAC} - t_{CWD}) + t_{CC} + t_{RW\text{-}BUB,\ XDRDRAM,\ MIN}$ or $(t_{\Delta RW} - t_{\Delta RW,\ MIN}) = (t_{RW\text{-}BUB,\ XDRDRAM} - t_{RW\text{-}BUB,\ XDRDRAM,\ MIN})$

In other words, the two timing parameters $t_{RW\text{-}BUB,XDRDRAM}$ and $t_{\Delta RW}$ will change together. The relationship of this change to the propagation delay $t_{PD,CYC}$ $(=t_{PD\text{-}D} + t_{PD\text{-}Q})$ can be derived by looking at the two timing paths from T_{15} to T_{21} at the XDR DRAM:

$t_{PD\text{-}Q} + t_{CC} + t_{RW\text{-}BUB,XIO} + t_{PD\text{-}D} = t_{CC} + t_{RW\text{-}BUB,XDRDRAM}$ or $t_{RW\text{-}BUB,XDRDRAM} = t_{RW\text{-}BUB,XIO} + t_{PD\text{-}D} + t_{PD\text{-}Q}$ or

$t_{RW\text{-}BUB,XDRDRAM} = t_{RW\text{-}BUB,XIO} + t_{PD,CYC}$

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in a system with minimum propagation delays:

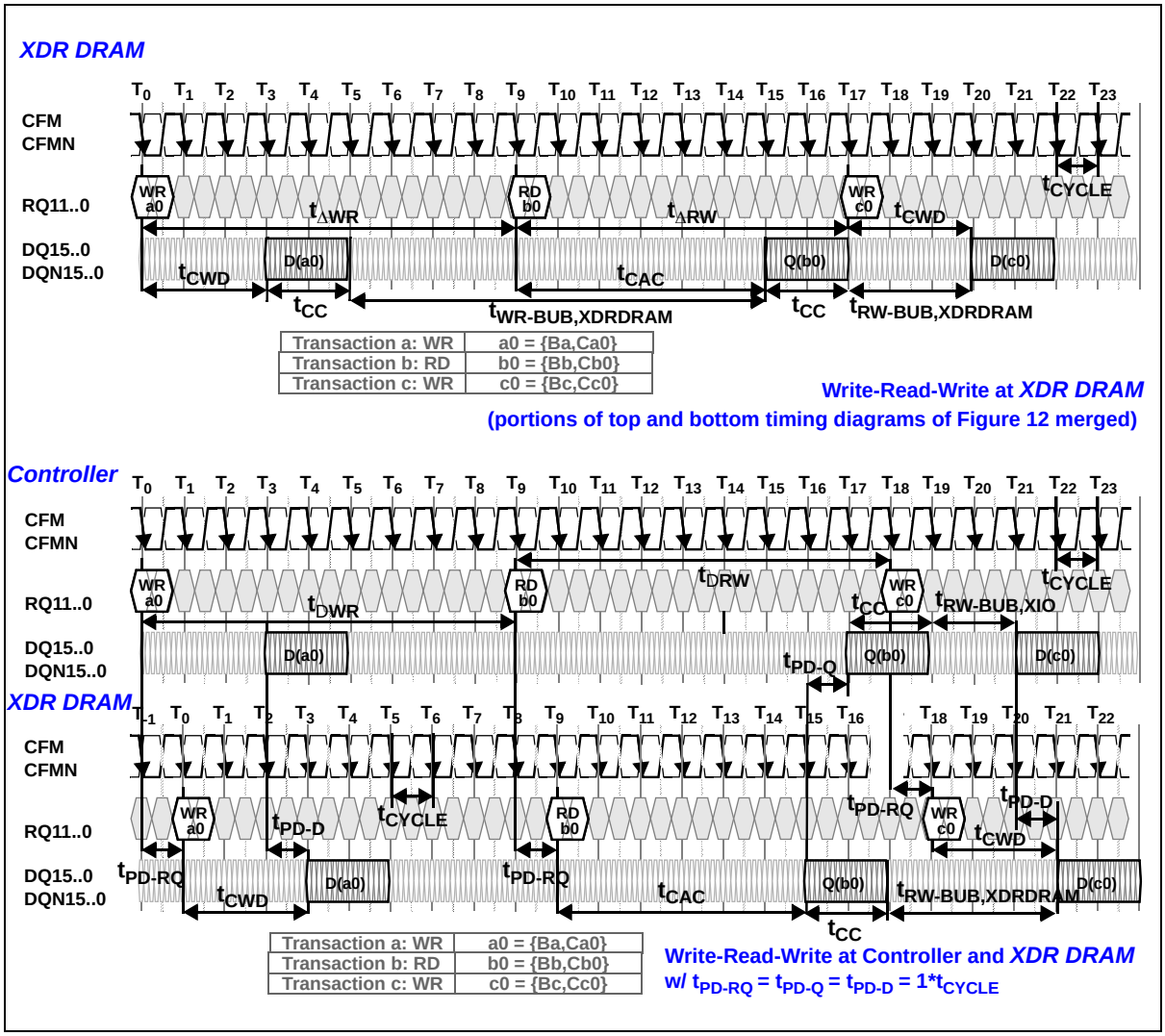
$t_{RW\text{-}BUB,XDRDRAM,MIN} = t_{RW\text{-}BUB,XIO} + t_{PD,CYC,MIN}$

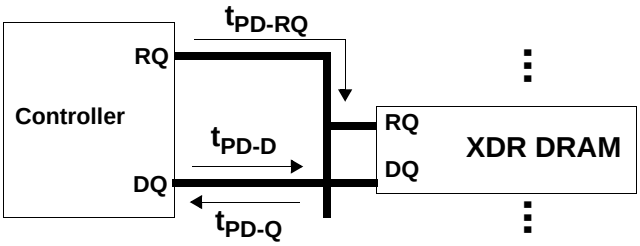
and since $t_{RW\text{-}BUB,XIO}$ is equal to $t_{RW\text{-}BUB,XIO,MIN}$ in the both cases, the following is true:

$(t_{PD,CYC} - t_{PD,CYC,MIN}) = (t_{RW\text{-}BUB,XDRDRAM} - t_{RW\text{-}BUB,XDRDRAM,MIN}) = (t_{\Delta RW} - t_{\Delta RW,MIN})$

In other words, the values of the $t_{RW\text{-}BUB,XDRDRAM,MIN}$ and $t_{\Delta RW,MIN}$ timing parameters correspond to the value of $t_{PD,CYC,MIN}$ for the system (this is equal to one t_{CYCLE}). As $t_{PD,CYC}$ is increased from this minimum value, $t_{RW\text{-}BUB,XDRDRAM}$ and $t_{\Delta RW}$ increase from their minimum values by an equivalent amount.

Figure 13 : Propagation Delay





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Register Operations

Serial Transactions

The serial interface consists of five pins. This includes RST, SCK, CMD, SDI and SDO. SDO uses CMOS signaling levels. The other four pins use RSL signaling levels. RST, CMD, SDI and SDO use a timing window which surrounds the falling edge of SCK. The RST pin is used for initialization.

Figure14 and Figure15 show examples of a serial write transaction and a serial read transaction. Each transaction starts on cycle S_4 and requires 32 SCK edges. The next serial transaction can begin on cycle S_{36}. SCK does not need to be asserted if there is no transaction.

Serial Write Transactions

The serial device write transaction in Figure14 begins with the Start [3:0] field. This consists of bits “1100” on the CMD pin. This indicates to the XDR DRAM that the remaining 28 bits constitute a serial transaction.

The next two bits are the SCMD[1:0] field. This field contains the serial command, the bits 00 in the case of a serial device write transaction.

The next eight bits are “00” and the SID[5:0] field. This field contains the serial identification of the device being accessed.

The next eight bits are the SADR[7:0] field. This field contains the serial address of the control register being accessed.

A single bit “0” follows next. This bit allows one cycle for the access time to the control register.

The next eight bits on the CMD pin is the SWD[7:0] field. this is the write data that is placed into the selected control register.

A final bit”0” is driven on the CMD pin to finish the serial write transaction.

A serial broadcast write is identical except that the contents of the SID[5:0] field in the transaction is ignored and all devices perform the register write. The SDI and SDO pins are not used during either serial write transaction.

Serial Read Transactions

The serial device read transaction in Figure15 begins with the Start[3:0] field. This consists of bits “1100” on the CMD pin. This indicates that the remaining 28 bits constitute a serial transaction.

The next two bits are the SCMD [1:0] field. This field contains the serial command, and the bits “10” in the case of a serial device read transaction.

The next eight bits are “00” and the SID [5:0] field. This field contains the serial identification of the device being accessed.

The next eight bits are the SADR [7:0] field and contain the serial address of the control register being accessed.

A single bit “0” follows next. This bit allows one cycle for the access time to the control register and time to turn on the SDO output driver.

The next eight bits on the CMD pin are the sequence “00000000”. At the same time, the eight bits on the SDO pin are the SRD [7:0] field. This is the read data that is accessed from the selected control register. Note the output timing convention here: bit SRD [7] is driven from a time $t_{Q,SI,MAX}$ after edge S_{26} to a time $t_{Q,SI,MIN}$ after edge S_{27}. The bit is sampled in the controller by the edge S_{27}.

A final bit “0” is driven on the CMD pin to finish the serial read transaction.

A serial forece read is identical except that the contents of the SID [5:0] field in the transaction is ignored and all devices perform the register read. This is used for device testing.

Figure16 shows the response of a DRAM to a serial device read transaction when its internal SID [5:0] register field doesn’t match the SID [5:0] field of the transaction. Instead of driving read data from an internal register for cycle edges S_{27} through S_{34} on the SDO output pin, it passes the input data from the SDI input pin to the SDO output pin during this same period.

Table 9: SCMD Field Encoding Summary

SCMD[1:0]	Command	DESCRIPTION
00	SDW	Serial device write-one device is written, the one whose SID[5:0] register matches the SID[5:0] field of the transaction.
01	SBW	Serial broadcast write - all devices are written, regardless of the contents of the SID [5:0] register and the SID [5:0] transaction field.
10	SDR	Serial device read - one device is read, the one whose SID[5:0] register matches the SID[5:0] field of the transaction.
11	SFR	Serial forced read - all devices are read, regardless of the contents of the SID[5:0] register and the SID[5:0] transaction field

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Figure 14 : Serial Write Transaction

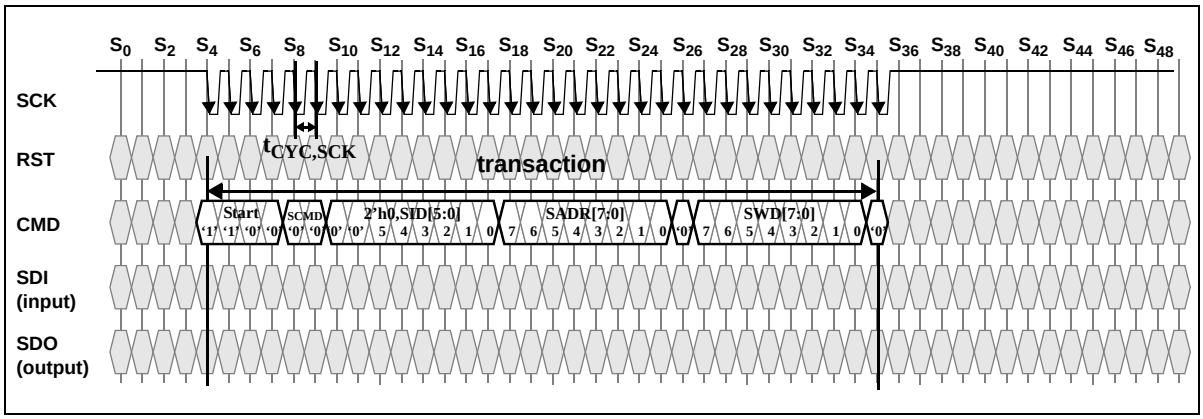


Figure 15 : Serial Read Transaction — Selected DRAM

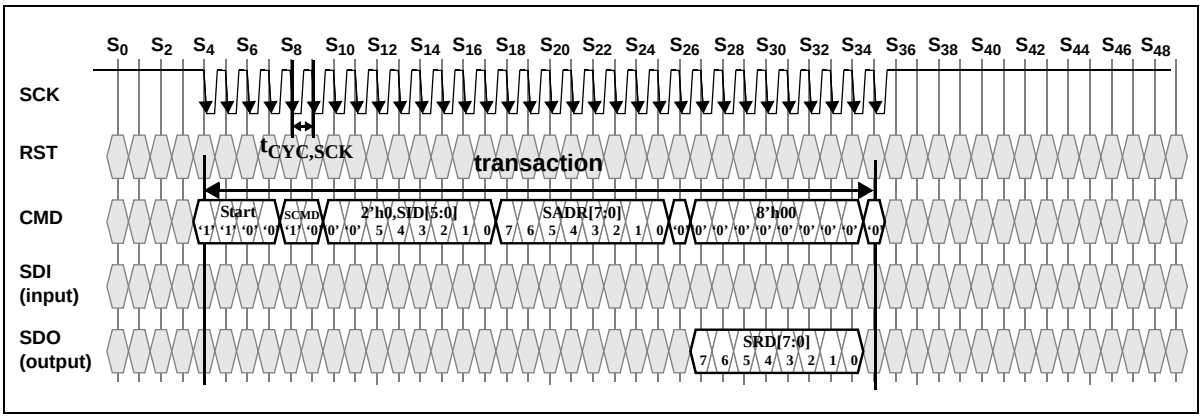
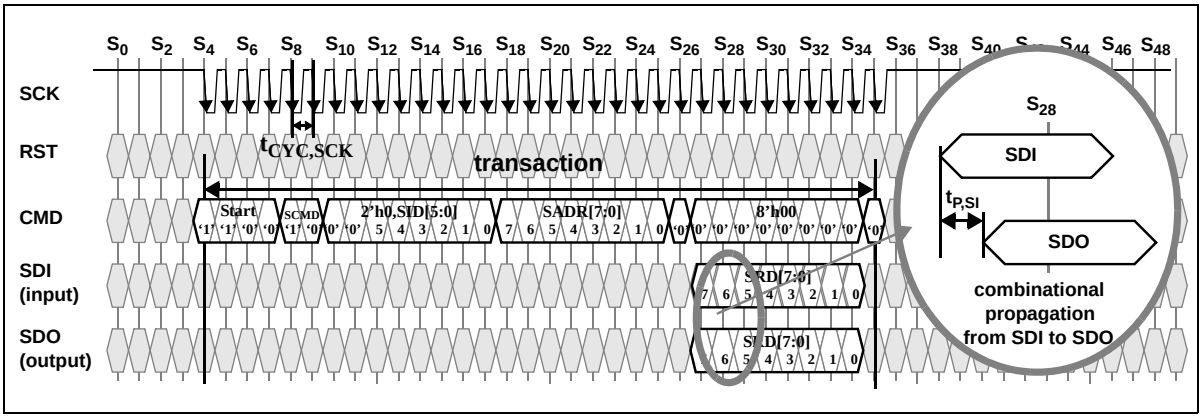


Figure 16 : Serial Read Transaction — Non-selected DRAM



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Register Summary

Figure17 through Figure42 show the control register in the memory component. The control registers are responsible for configuring the component's operating mode, for managing power state transactions, for managing refresh, and for managing calibration operations.

A control register may contain up to eight bits. Each figure shows defined bits in white and reserved bits in gray. Reserved bits must be written as 0 and must be ignored when read. Write-only fields must be ignored when read .

Each figure displays the following register information:

1. Register name
2. Register mnemonic
3. Register address (SADR [7:0] value needed to access it)
4. Read-only, write-only or read-write
5. Initialization state
6. Description of each defined register field

Figure17 shows the Serial Identification register. The register contains the SID [5:0] (serial identification field). This field contains the serial identification value for the deice. The value is compared to the SID[5:0] field of a serial transaction to determine if the serial transaction is directed to this device. The serial identification value is set during the initialization sequence.

Figure18 shows the Configuration Register. It contains three fields. The first is the WIDTH field. This field allows the number of DQ/DQN pins used for memory read and write accesses to be adjusted. The SLE field enables data to be written into the memory through the serial interface using the WDSL register.

Figure19 shows the Power Management Register. It contains two fields. The first is the PX field. When this field is written with a "1", the memory component transactions from powerdown to active state. It is usually unnecessary to write a "0" into this field; this is done automatically by the PDN command in a COLX packet. The PST field indicates the current power state of the memory component.

Figure20 shows the Write Data Serial Load Register. It permits data to be written into memory via the Serial Interface.

Figure23 shows the Refresh Bank Control Register. It contains two fields: BANK and MBR. The BANK field is read-write and contains the bank address used by self-refresh during the powerdown state. The MBR field controls how many banks are refreshed during each refresh operation. Figure24, Figure25 and Figure26 show different fields of the Refresh Row Register (high, middle and low). This read-write field contains the row address used by self- and auto-refresh. See"Refresh Transactions" on page 37 for more details.

Figure28 and Figure29 show the Current Calibration 0 and 1 registers. They contain the CCVALUE0 and CCVALUE1 fields, respectively. These are read-write fields which control the amount of IOL current driven by the DQ and DQN pins during a read transaction. The Current Calibration 0 Register controls the even-numbered DQ and DQN pins, and the Current Calibration 1 controls the odd-numbered DQ and DQN pins.

Figure30 and Figure31 show the Impedance Calibration 0 and 1 registers. They contain the ZCVALUE0 and ZCVALUE1 field, respectively. These are read-write fields that control the impedance of the on-chip termination components in the DQ and DQN pins. The Impedance Calibration 0 Register controls the even-numbered DQ and DQN pins, and the Impedance Calibration 1 controls the odd-numbered DQ and DQN pins.

Figure 36 through Figure 41 and Figure 43 shows the test registers. This includes the TEST, DLL, PLL0, PLL1, IFT, DA and PARTn registers. These are used during device testing. They are not to be read or written during normal operation.

Figure42 shows the DLY register. This is used to set the value of t_{CAC} and t_{CWD} used by the component. See "Timing Parameters" on page59.

Figure 17 : Serial Identification (SID) Register

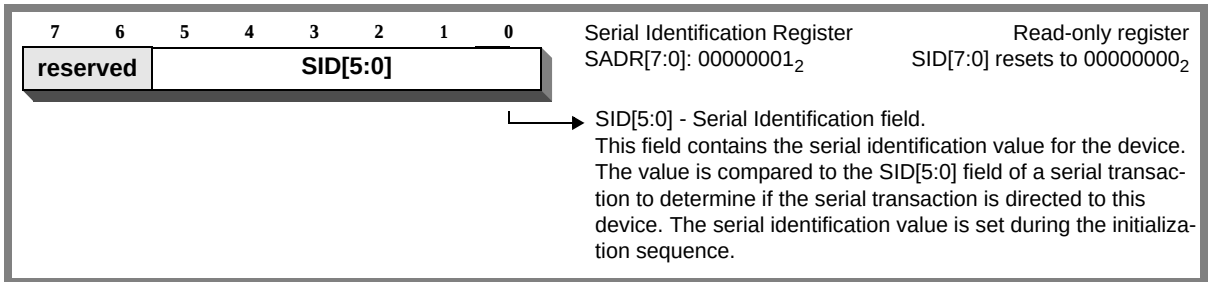

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Figure 18 : Configuration (CFG) Register

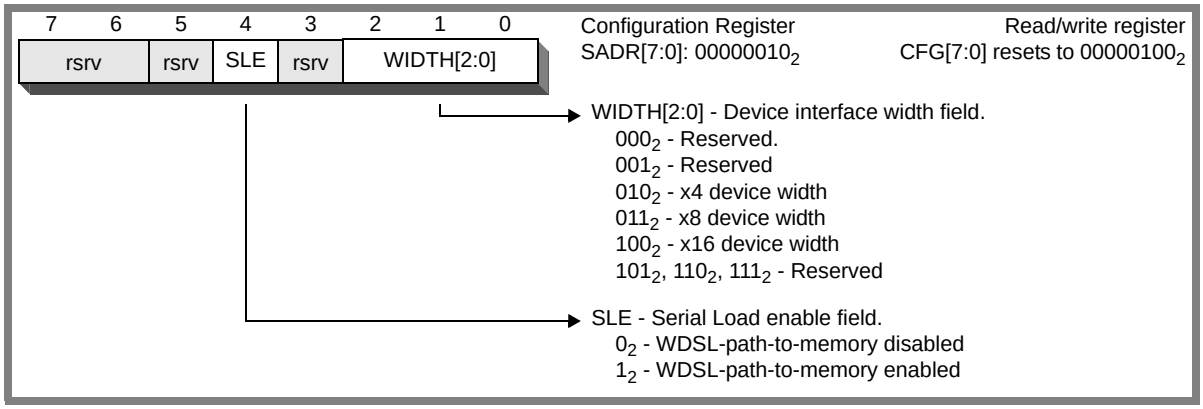

Figure 19 : Power Management (PM) Register

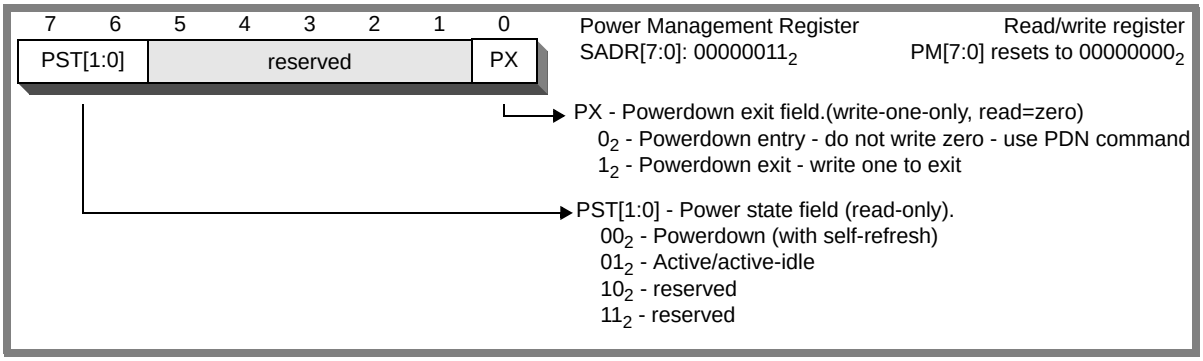

Figure 20 : Write Data Serial Load (WDSL) Control Register

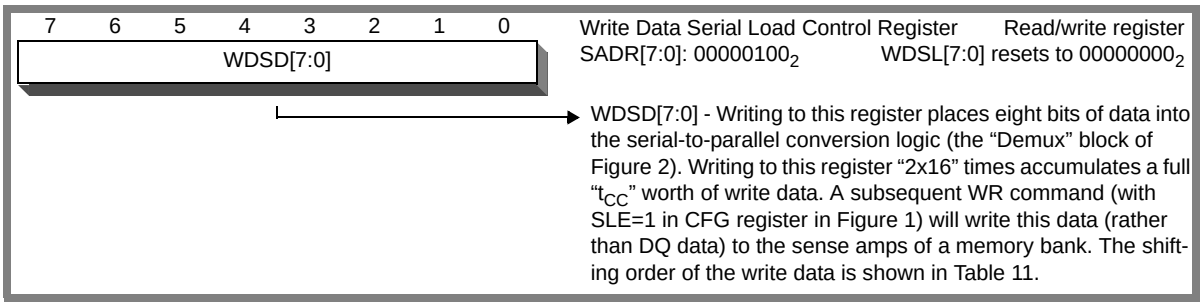

Figure 21 : RQ Scan High (RQH) Register

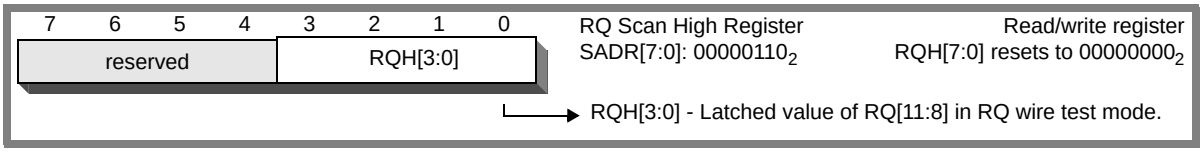

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Figure 22 : RQ Scan Low (RQL) Register

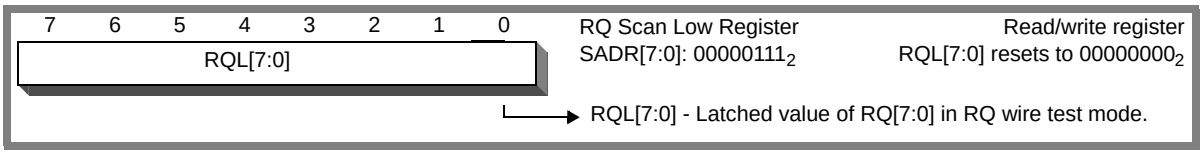

Figure 23 : Refresh Bank (REFB) Control Register

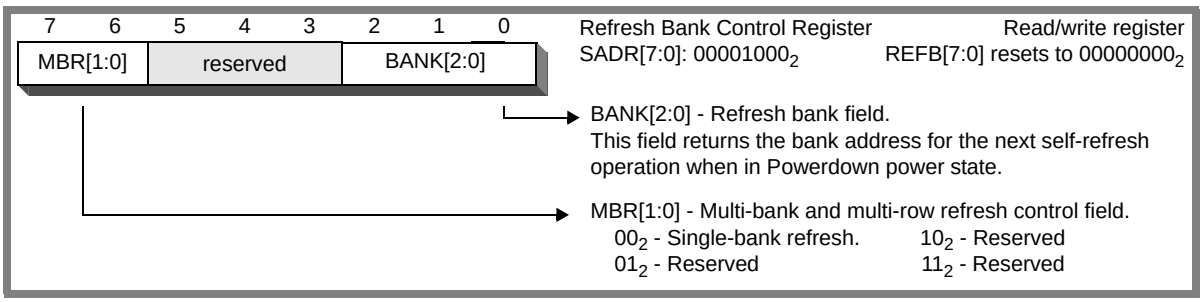

Figure 24 : Refresh High (REFH) Row Register

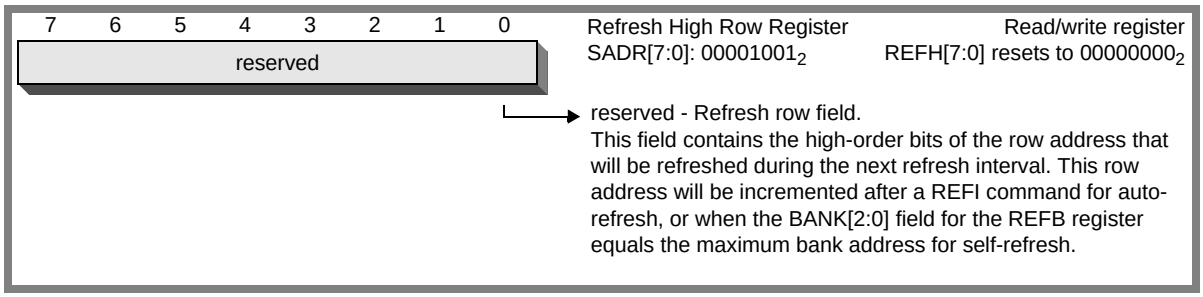

Figure 25 : Refresh Middle (REFM) Row Register

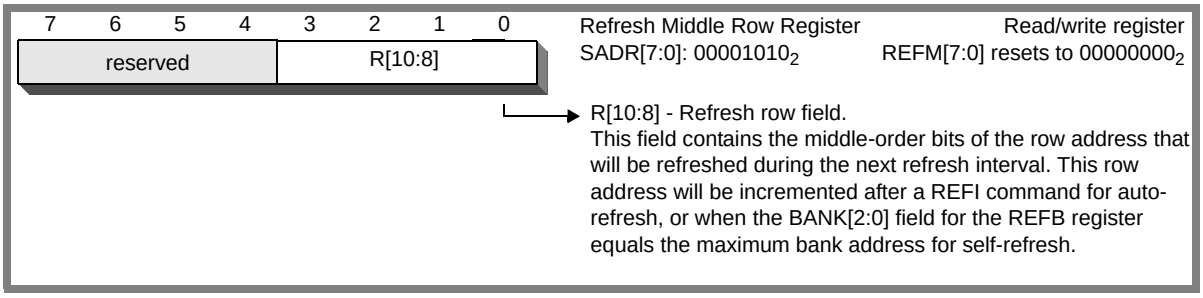

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Figure 26 : Refresh Low (REFL) Row Register

7	6	5	4	3	2	1	0
R[7:0]							

Refresh Low Row Register — Read/write register
SADR[7:0]: 00001011_2 — REFL[7:0] resets to 00000000_2

R[7:0] - Refresh row field.
This field contains the low-order bits of the row address that will be refreshed during the next refresh interval. This row address will be incremented after a REFI command for auto-refresh, or when the BANK[2:0] field for the REFB register equals the maximum bank address for self-refresh.

Figure 27 : IO Configuration (IOCFG) Register

7	6	5	4	3	2	1	0
reserved						ODF[1:0]	

IO Configuration Register — Read/write register
SADR[7:0]: 00001111_2 — IOCFG[7:0] resets to 00000000_2

ODF[1:0] - Overdrive Function field.
00 - Nominal $V_{OSW,DQ}$ range
01 - reserved
10 - reserved
11 - reserved

Figure 28 : Current Calibration 0 (CC0) Register

7	6	5	4	3	2	1	0
reserved	CCVALUE0[5:0]						

Current Calibration 0 Register — Read/write register
SADR[7:0]: 00010000_2 — CC0[7:0] resets to $vvvvvvvv_2$
(vendor-dependent reset value)

CCVALUE0[5:0] - Current calibration value field.
This field controls the amount of current drive for the even-numbered DQ and DQN pins.

Figure 29 : Current Calibration 1 (CC1) Register

7	6	5	4	3	2	1	0
reserved	CCVALUE1[5:0]						

Current Calibration 1 Register — Read/write register
SADR[7:0]: 00010001_2 — CC1[7:0] resets to $vvvvvvvv_2$
(vendor-dependent reset value)

CCVALUE1[5:0] - Current calibration value field.
This field controls the amount of current drive for the odd-numbered DQ and DQN pins.

Figure 30 : Impedance Calibration 0 (ZC0) Register

7	6	5	4	3	2	1	0
reserved							

Impedance Calibration 0 Register — Read/write register
SADR[7:0]: 00010010_2 — ZC0[7:0] resets to 00000000_2

reserved

Figure 31 : Impedance Calibration 1 (ZC1) Register

7	6	5	4	3	2	1	0
reserved							

Impedance Calibration 1 Register — Read/write register
SADR[7:0]: 00010011_2 — ZC1[7:0] resets to 00000000_2

reserved

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Figure 32 : Current Fuse Setting 0 (FZC0) Register

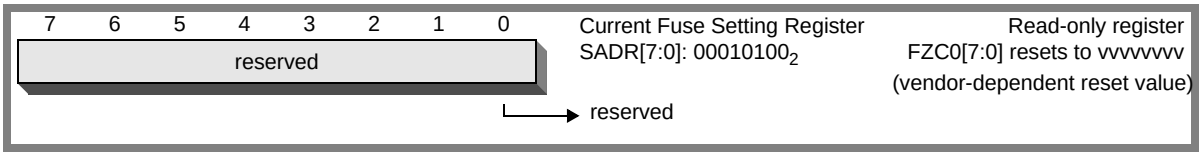

Figure 33 : Current Fuse Setting 1 (FZC1) Register

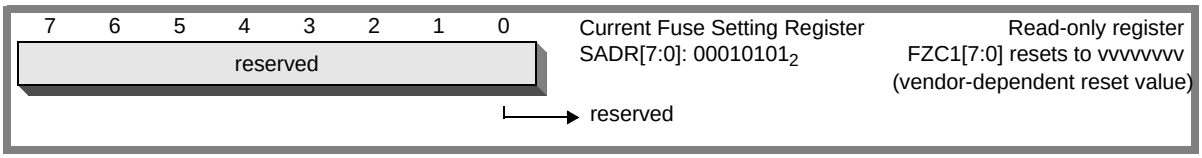

Figure 34 : Read Only Memory 0 (ROM0) Register

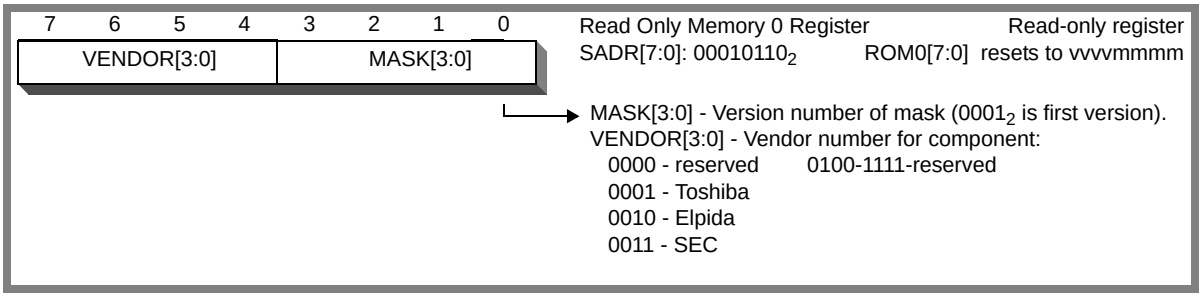

Figure 35 : Read Only Memory 1 (ROM1) Register

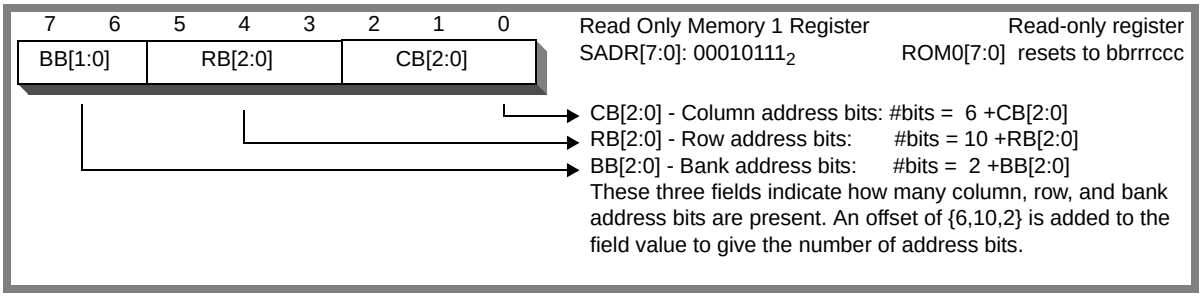

Figure 36 : TEST Register

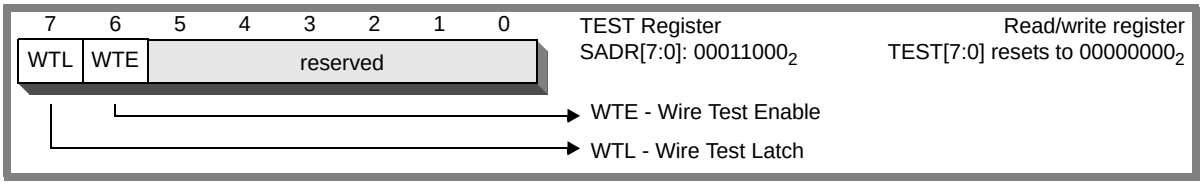

Figure 37 : DLL Register

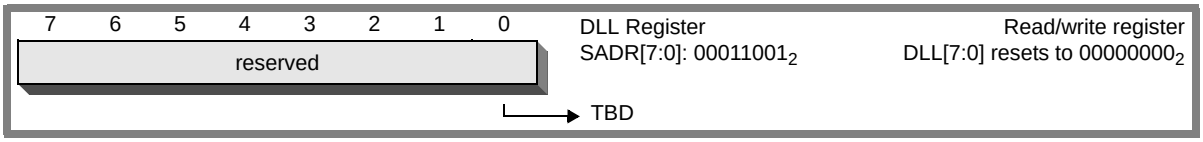

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Figure 38 : PLL0 Register

7	6	5	4	3	2	1	0
reserved							

PLL0 Register — Read/write register
SADR[7:0]: 00011010_2 — PLL0[7:0] resets to 00000000_2

→ TBD

Figure 39 : PLL1 Register

7	6	5	4	3	2	1	0
reserved							

PLL1 Register — Read/write register
SADR[7:0]: 00011011_2 — PLL1[7:0] resets to 00000000_2

→ TBD

Figure 40 : IFT Register

7	6	5	4	3	2	1	0
reserved							

IFT Register — Read/write register
SADR[7:0]: 00011100_2 — IFT[7:0] resets to 00000000_2

→ TBD

Figure 41 : DA Register

7	6	5	4	3	2	1	0
reserved							

DA Register — Read/write register
SADR[7:0]: 00011101_2 — DA[7:0] resets to 00000000_2

→ TBD

Figure 42 : Delay (DLY) Control Register

7	6	5	4	3	2	1	0
CWD[3:0]				CAC[3:0]			

DLY Register — Read/write register
SADR[7:0]: 00011111_2 — DLY[7:0] resets to 00110110_2

→ CAC[3:0] - Programmed value of t_{CAC} timing parameter:
0110_2 - $t_{CAC} = 6*t_{CYCLE}$ 1000_2 - $t_{CAC} = 8*t_{CYCLE}$
0111_2 - $t_{CAC} = 7*t_{CYCLE}$ others - Reserved.

→ CWD[3:0] - Programmed value of t_{CWD} timing parameter:
0011_2 - $t_{CWD} = 3*t_{CYCLE}$
0100_2 - $t_{CWD} = 4*t_{CYCLE}$ others - Reserved.

Figure 43 : Partner-Definable (PART0-PARTF) Registers

7	6	5	4	3	2	1	0
reserved							

PART0 Register — Read/write register
SADR[7:0]: 10000000_2 — PART0[7:0] resets to 00000000_2

7	6	5	4	3	2	1	0
reserved							

PART1 Register — Read/write register
SADR[7:0]: 10000001_2 — PART1[7:0] resets to 00000000_2

⋮

7	6	5	4	3	2	1	0
reserved							

PARTF Register — Read/write register
SADR[7:0]: 10001111_2 — PARTF[7:0] resets to 00000000_2

Note - The partner-definable registers should not be written or read; doing so will produce undefined results.

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Maintenance Operations

Refresh Transactions

Figure44 contains two timing diagrams showing examples of refresh transactions. The top timing diagram shows a single refresh operation. Bank Ba is assumed to be closed (in a precharged state) when a REFA command is received in a ROWP packet on clock edge T_0. The REFA command causes the row addressed by the REFr register (REFH/REFM/REFL) to be opened (sensed) and placed in the sense amp array for the bank.

Note that the REFA and REFI commands are similar to the ACT command functionally; both specify a bank address and delay value, and both cause the selected bank to open (to become sensed.). The difference is that the ACT command is accompanied by a row address in the ROWA packet, while the REFA and REFI commands use a row address in the REFr register (REFH/REFM/REFL).

After a time t_{RAS}, a ROWP packet with REFP command to bank Ba is presented. This causes the bank to be closed (precharged), leaving the bank in the same state as when the refresh transaction began.

Note that the REFP command is equivalent to the PRE command functionally; both specify a bank address and delay value, and both cause the selected bank to close (to become precharged).

After a time t_{RP}, another ROWP packet with REFA command to bank Bb is presented (banks Ba and Bb are the same in this example). This starts a second refresh cycle. Each refresh transaction requires a total time $t_{RC} = t_{RAS} + t_{RP}$, but refresh transactions to different banks may be interleaved like normal read and write transactions.

Each row of each bank must be refreshed once in every t_{REF} interval. This is shown with the fourth ROWP packet with a REFA command in the top timing diagram.

Interleaved Refresh Transaction

The lower timing diagram in Figure44 represents one way a memory controller might handle refresh maintenance in a real system.

A series of eight ROWP packets with REFA commands (except for the last which is a REFI command) are presented starting at edge T_0. The packets are spaced with intervals of t_{RR}. Each REFA or REFI command is addressed to a different bank (Ba through Bh) but uses the same row address from the REFr (REFH/REFM/REFL) register. The eighth REFI command uses this address and then increments it so the next set of eight REFA/REFI commands will refresh the next set of rows in each bank.

A series of eight ROWP packets with REFP commands are presented effectively at edge T_{10} (a time t_{RAS} after the first ROWP packet with a REFA command). The packets are spaced with intervals of t_{PP}. Like the REFA/REFI commands, each REFP command is addressed to a different bank (Ba through Bh).

This burst of eight refresh transactions fully utilizes the memory component. However, other read and write transactions may be interleaved with the refresh transactions before and after the burst to prevent any loss of bus efficiency. In other words, a ROWA packet with ACT command for a read or write could have been presented at edge T_4 (a time t_{RR} before the first refresh transaction starts at edge T_0). Also, a ROWA packet with ACT command for a read or write could have been presented at edge T_{36} (a time t_{RR} after the last refresh transaction starts at edge T_{32}). In both cases, the other request packets for the interleaved read or write accesses (the precharge commands and the read or write commands) could be slotted in among the request packets for the refresh transaction.

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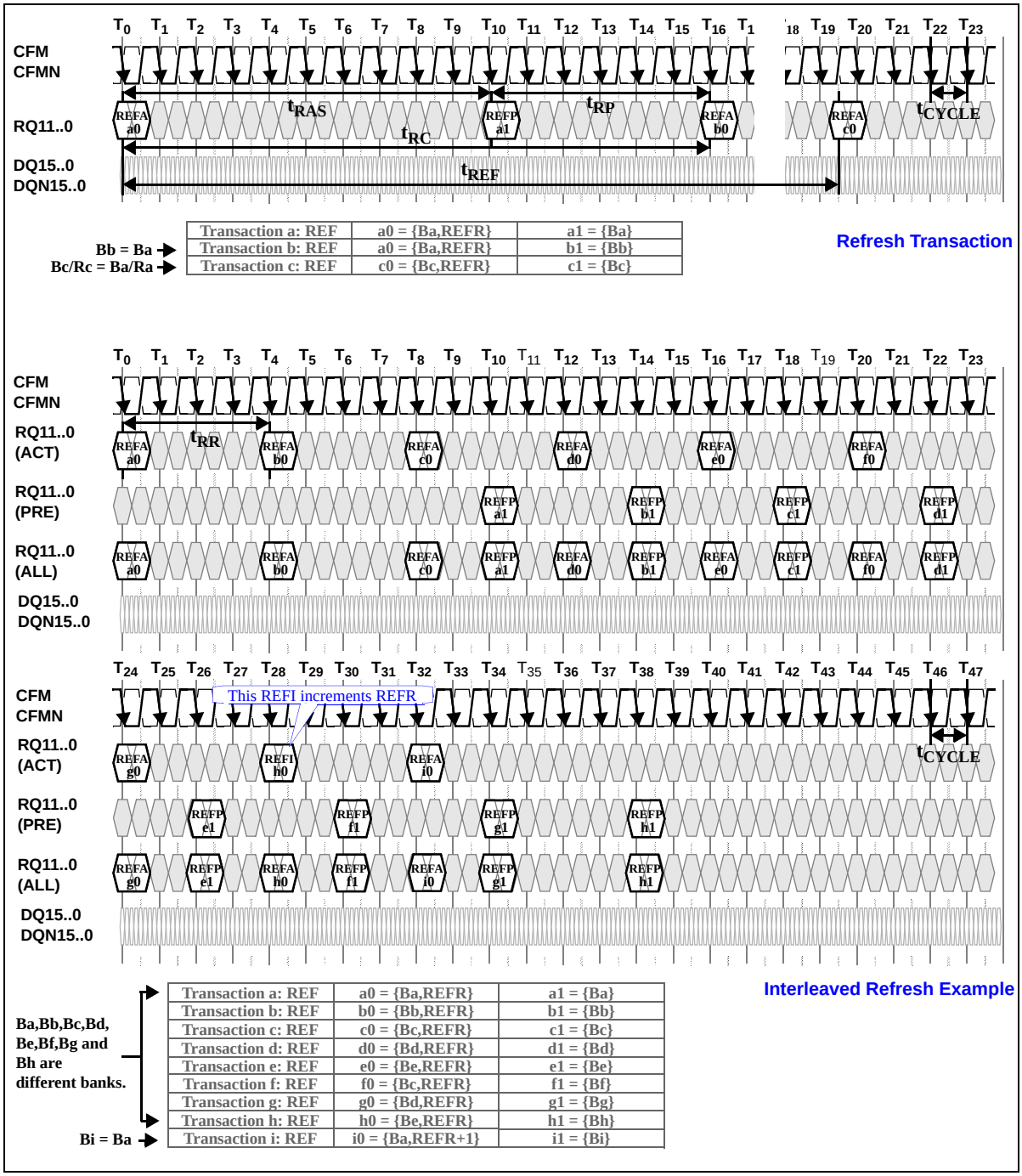
Figure 44 : Refresh Transactions



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Calibration Transactions

Figure45 shows the calibration transaction diagrams for the XDR DRAM device. There is one calibration operation supported: calibration of the output current level I_{OL}, each DQi and DQNi pin.

The output current calibration sequence is shown in the upper diagram. It begins when a period of $t_{CMD-CALC}$ is observed after the last RQ packet (with command “CMD a” in this example). No request packets should be issued in this period.

A COLX packet with a “CALC b” command is then issued to start the current calibration sequence. A period of t_{CALCE} is observed after this packet. No request packets should be issued during this period.

A COLX packet with a “CALE c” command is then issued to end the current calibration sequence. A period of $t_{CALE-CMD}$ is observed after this packet. No request packets should be issued during this period. The first request packet may then be issued (with command “CMD d” in this example).

A second current calibration sequence must be started within an interval of t_{CALC}. In this example. the next COLX packet with a “CALC e” command starts a subsequent sequence.

The dynamic termination calibration sequence is shown in the lower diagram. Note that this memory component does not use this sequence; termination calibraion is performed during the manufacturing process. However, the termination sequence shown will be issued by the controller for those memory component which do use a periodic calibration mechanism.

It begins when a period of $t_{CMD-CALZC}$ is observed after the packet edge T_0(with command CMDa in this example). No request packets should be issued in this period.

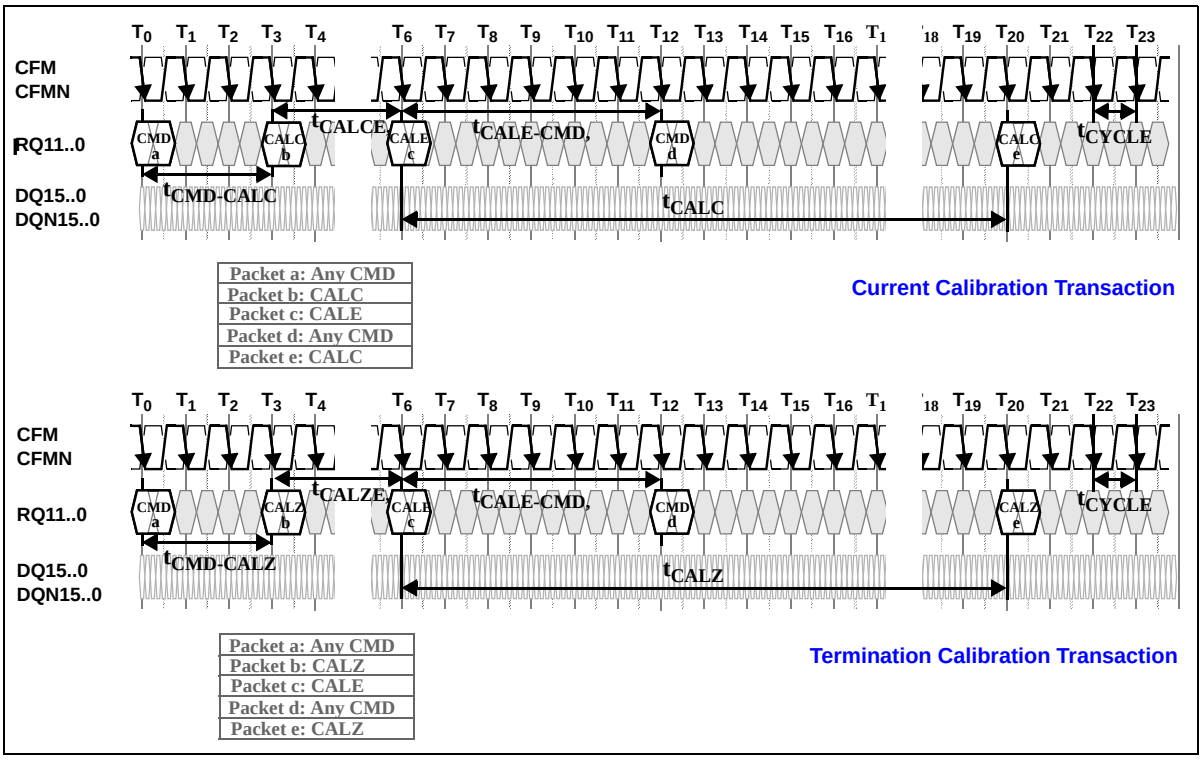
A COLX packet with a CALZ command is then issued at edge T_3 to start the current calibration sequence. A second period of t_{CALZE} is ovserved after this packet. No request packets should be issued during this period.

A COLX packet with a CALE command is then issued at dege T_6 to end the current calibration sequence. A third period of $t_{CALE-CMD}$ is observed after this pakets. No request packets should be issued during this period. The first request pakcet may be issued at edge T_{12}(with command CMDd in this example).

A second current calibration sequence must be started within an interval of t_{CALZ}. In this example, the next COLX pakcet with a CALZ command occurs at edge T_{20}.

Note that the labels for the CFM clock edges(of the form Ti) are not to scale, and are used to identify events in the diagrams.

Figure 45 : Calibration Transactions



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Power State Management

Figure46 shows power state transition diagrams for the XDR DRAM device. There are two power states in the XDR DRAM: Powerdown and Active. Powerdown state is to be used in applications in which it is necessary to shut down the CFM/CFMN clock signals. In this state, the contents of the storage cells of the XDR DRAM will be retained by an internal state machine which performs periodic refresh operations using the REFB and REFr control registers.

The upper diagram shows the sequence needed for Powerdown entry. Prior to starting the sequence, all banks of XDR DRAM must be precharged so they are left in a closed state. Also, all 2^3 banks must be refreshed using the current value of the REFr registers, and the REFr registers must not be incremented with the REFI command at the end of this special set of refresh transactions. This ensures that no matter what value has been left in the REFB register, no row of any bank will be skipped when automatic refresh is first started in Powerdown. There may be some banks at the current row value in the REFr registers that are refreshed twice during the Powerdown entry process.

After the last request packet (with the command CMDa in the upper diagram of the figure), an interval of $t_{CMD-PDN}$ is observed. No request packets should be issued during this period.

A COLX packet with the PDN command is issued after this interval, causing the XDR DRAM to enter Powerdown state after an interval of $t_{PDN-ENTRY}$ has elapsed (this is the parameter that should be used for calculating the power dissipation of the XDR DRAM). The CFM/CFMN clock signals may be removed a time $t_{PDN-CFM}$ after the COLX packet with the PDN command. Also, the termination voltage supply may be removed (set to the ground reference) from the Vterm pins a time $t_{PDN-CFM}$ after the COLX pakcet with the PDN command. The voltage on the DQ/DQN pins will follow the voltae on the Vterm pins during Powerdonwn entry.

When the XDR DRAM is in Powerdown, an internal frequency source and state machine will automatically generate internal refresh transactions. It will cycle through all 2^3 state combinations of the REFB register. When the largest value is reached and the REFB value wraps around, the REFr register is incremented to the next value. The REFB and REFr values select which bank and which row are refreshed during the next automatic refresh transaction.

The lower diagram shows the sequence needed for Powerdown exit. The sequence is started with a serial broadcast write (SBW command) transaction using the serial bus of the XDR DRAM. This transaction writes the value “00000001” to the Power Management (PM) register (SADR = “00000011”) of all XDR DRAMs connected to the serial bus. This sets the PX bit of the PM register, causing the XDR DRAMs to return to Active power state.

The CFM/CFMN clock signals must be stable a time $t_{CFM-PDN}$ before the end of the SBW transaction. Also, the termination voltage supply must be restored to its normal operating point ($V_{TERM,DRSL}$) on the Vterm pins a time $t_{CFM-PDN}$ before the end of the SWB transaction. The voltage on the DQ/DQN pins will follow the voltage on the Vterm pins during Powerdown exit.

The XDR DRAM will enter Active state after an interval of $t_{PDN-EXIT}$ has elapsed from the end of the SBW transaction (this is the parameter that should be used for calculating the power dissipation of the XDR DRAM).

The first request packet may be issued after an interval of $t_{PDN-CMD}$ has elapsed from the end of the SBW transaction, and must contain a “REFA” command in a ROWP packet. In this example, this packet is denoted with the command “REFA 1”. No other request packets should be issued during this $t_{PDN-CMD}$ interval.

All “n” banks (in the example, $n=2^3$) must be refreshed using the current value of the REFr registers. The “nth” refresh transaction will use a “REFI” command to inrement the REFr register (instead of a “REFR” command). This ensures that no matter what value has been left in the REFB register, no row of any bank will be skipped when normal refresh is restarted in Active state. There may be some banks at the current row value in the REFr registers that are refreshed twice during the Powerdown exit process.

Note that during the Powerdown state an internal time source keeps the device refreshed. However, during the $t_{PDN-CMD}$ interval, no internal refresh operations are performed. As a result, an additional burst of refresh transactions must be issued after the burst of “n” transactions described above. This second burst consists of “m” refresh transactions:

$m = \text{ceiling}[2^3 * 2^{11} * t_{PDN-CMD}/t_{REF}]$

Where “2^{11}” is the number of rows per bank, and “2^3” is the number of banks. Every ”nth” refresh transaction (where $n=2^3$) will use a “REFI” command (to increment the REFr register) instead of a “REFA” command.

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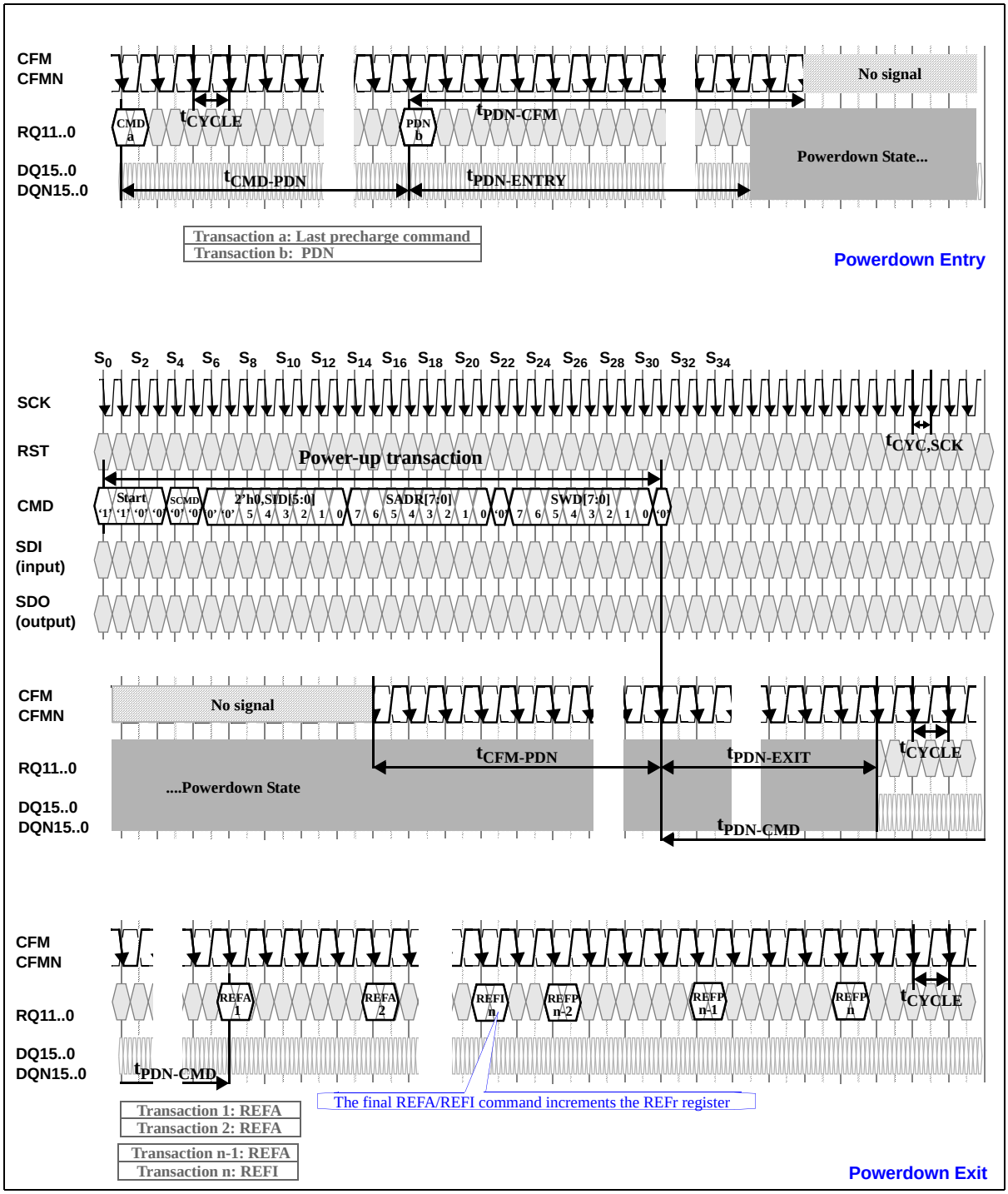
Figure 46 : Power State Management



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Initialization

Figure47 shows the topology of the serial interface signals of a XDR DRAM system. The three signals RST, CMD, and SCK are transmitted by the controller and are received by each XDR DRAM device along the bus. The signals are terminated to the V_{TERM} supply through termination components at the end farthest from the controller. The SDI input of the XDR DRAM device furthest from the controller is also terminated to V_{TERM}. The SDO output of each XDR DRAM device is transmitted to the SDI input of the next XDR DRAM device (in the direction of the controller). This SDO/SDI daisy chain topology continues to the controller, where it ends at the SRD input of the controller. All the serial interface signals are low-true. All the signals use RSL signaling circuits, except for the SDO output which uses CMOS signaling circuits.

Figure 47 : Serial Interface Systems Topology

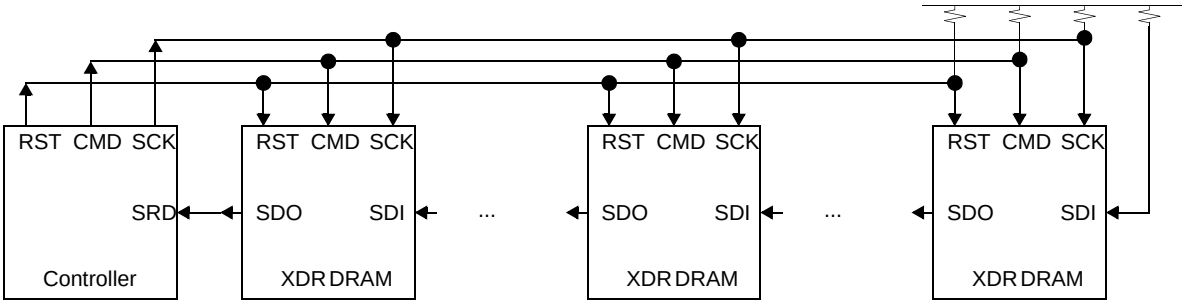
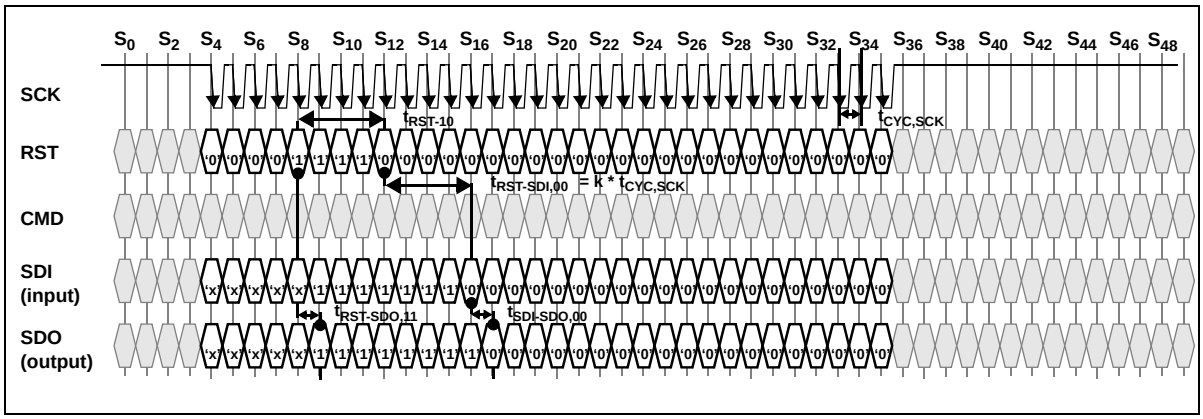


Figure48 shows the initialization timing of the serial interface for the XDR DRAM [k] device in the system shown above. Prior to initialization, the RST is held at zero. The CMD input is not used here, and should also be held at zero. Note that the inputs are all sampled by the negative edge of the SCK clock input. The SDI input for the XDR DRAM[0] device is zero, and is unknown for the remaining devices.

On negative SCK edge S_8 the RST input is sampled one. It is sampled one on the next four edges, and is sampled zero on edge S_{12} a time t_{RST-10} after it was first sampled one. The state of the control registers in the XDR DRAM device are set to their reset values after the first edge (S_8) in which RST is sampled one.

Figure 48 : Initialization Timing for XDR DRAM [k] Device



The SDI inputs will be sampled one within a time $t_{RST-SDO,11}$ after RST is first sampled one in all the XDR DRAMs except for XDR DRAM [0]. XDR DRAM [0]'s SDI input will always be sampled zero.

XDR DRAM [k] will see its RST input sampled zero at S_{12}, and will then see its SDI input sampled zero at S_{16} (after SDI had previously been sampled one). This interval (measured in $t_{CYC,SCK}$ units) will be equal to the index [k] of the XDR DRAM device along the serial interface bus. In this example, k is equal to 4.

This is because each XDR DRAM device will drive its SDO output zero around the SCK edge a time $t_{SDI-SDO,00}$ after its SDI input is sample zero.

In other words, the XDR DRAM [0] device will see RST and SDI both sampled zero on the same edge S_{12} ($t_{RST-SDI,00}$ will be 0 *$t_{CYC,SCK}$ units), and will drive its SDO to zero around the subsequent edge (S_{13}).

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The XDR DRAM [1] device will see SDI sampled zero on edge S_{13} ($t_{RST\text{-}SDI,00}$ will be 1*$t_{CYC,SCK}$ units), and will drive its SDO to zero around the subsequent edge (S_{14}).

The XDR DRAM [2] device will see SDI sampled zero on edge S_{14} ($t_{RST\text{-}SDI,00}$ will be 2* $t_{CYC,SCK}$ units), and will drive its SDO to zero around the subsequent edge (S_{15}).

This continues until the last XDR DRAM device drives the SRD input of the controller. Each XDR DRAM device contains a state machine which measures the interval $t_{RST\text{-}SDI,00}$ between the edges in which RST and SDI are both sampled zero, and uses this value to set the SID [5:0] field of the SID (Serial Identification) register. This value allows directed read and write transactions to be made to the individual XDR DRAM devices.

Table 10 summarizes the range of the timing parameters used for initialization by the serial interface bus.

Table 10 : Initialization Timing Parameters

Symbol	Parameter	Min	Max	Unit	Figure (s)
$t_{RST,10}$	Number of cycles between RST being sampled one and RST being sampled zero	2	-	$t_{CYC,SCK}$	-
$t_{RST\text{-}SDO,11}$	Number of cycles between RST being sampled one and SDO being driven to one	1	1	$t_{CYC,SCK}$	-
$t_{RST,SDI,00}$	Number of cycles between RST being sampled zero (after being sampled one for $t_{RST,10,MIN}$ or more cycles) and SDI being sampled zero. This will be equal to the index [k] of the XDR DRAM device along the serial interface bus	0	63	$t_{CYC,SCK}$	-
$t_{SDI\text{-}SDO,00}$	Number of cycles between SDI being sampled one (after RST has been sampled one for $t_{RST,10,MIN}$ or more cycles and is then sampled zero) and SDO being driven to zero	1	1	$t_{CYC,SCK}$	-
$t_{RST\text{-}SCK}$	Asynchronous reset interval.	20	-	$t_{CYC,SCK}$	-

XDR DRAM Initialization Overview

[1] Apply voltage to VDD, VTERM, and VREF pins. VTERM and VREF voltages must be less or equal to VDD voltage at all times. Wait a time interval $t_{COREINIT}$. Power-on reset circuit in XDR DRAM places XDR DRAM into low-power state.

[2] Assert RST, SCK, SDI and CMD to logical zero, Then:

- Pulse SCK to logical one, then to logical zero four times.
- Assert RST to logical one. Reset circuit places XDR DRAM into low-power state(identical to power-on reset)
- Perform remaining initialization sequence in Figure 48.

[3] XDR DRAM has valid Serial ID and all registers have default values that are defined in Figure17 through Figure42.

[4] Perform broadcast or directed register writes to adjust registers which need a value different from their default value.

[5] Perform Powerdown Exit sequence shown in Figure46. This includes the activity from SCK cycle S_0 through the final REFP command.

[6] Perform termination/current calibration. The CALZ /CALE sequence shown in Figure 45 is issued 128 times. After this, each sequence is issued once every t_{CALZ} or t_{CALC} interval.

[7] Condition the XDR DRAM banks by performing a REFA/REFI activate and REFP precharge operation to each bank eight times. This can be interleaved to save time. The row address for the activate operation will step through eight successive values of the REFr registers. The sequence between cycles T_0 and T_{32} in the Interleaved Refresh Example in Figure 44 could be performed eight times to satisfy this conditioning requirement.

XDR DRAM Pattern Load with WDSL Register

The XDR memory system requires a method of deterministically loading pattern data to XDR DRAMs before beginning Receive Timing Calibration (RX TCAL). The method employed by the XDR DRAMs to achieve this is called Write Data Serial Load (WDSL). A WDSL packet sends one-byte of serial data which is serially shifted into a holding register within the XDR DRAM. Initialization software sends a sequence of WDSL packets, each of which shifts the new byte in and advances the shifter by 8 positions. In this way, XDR DRAMs of varying widths can be loaded with a single command type.

Each sequence of WDSL packets will load one full column of data to the internal holding register of the target XDR DRAM. Depending upon the ratio of native device width to programmed width, there may be more than one sub-column per column. After loading a full column, a series of WR commands will be issued to sequentially transfer each sub-column of the column to the XDR DRAM core(s), based upon the SC [3:0] bits.

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Table 11 : WDSL-to-Core Mapping (First Generation x16/x8/x4 XDR DRAM, BL = 16)

DQ Pins Used			Core Word	WDSL Core Word Load Order	x16	x8		x4			
x4	x8	x16		WD[n][15:0]	SC[3:2] =xx	SC[3:2] = 0x	SC[3:2] = 1x	SC[3:2] = 00	SC[3:2] = 01	SC[3:2] = 10	SC[3:2] = 11
LOGICAL VIEW OF XDR DRAM					Word Written (1 = Written, 0 = Not Written)						
DQ0	DQ0	DQ0	WD[0][15:0]	WDSL Word 8	1	1	0	1	0	0	0
DQ1	DQ1	DQ1	WD[1][15:0]	WDSL Word 7	1	1	0	1	0	0	0
DQ2	DQ2	DQ2	WD[2][15:0]	WDSL Word 12	1	1	0	1	0	0	0
DQ3	DQ3	DQ3	WD[3][15:0]	WDSL Word 3	1	1	0	1	0	0	0
DQ0	DQ4	DQ4	WD[4][15:0]	WDSL Word 10	1	1	0	0	1	0	0
DQ1	DQ5	DQ5	WD[5][15:0]	WDSL Word 5	1	1	0	0	1	0	0
DQ2	DQ6	DQ6	WD[6][15:0]	WDSL Word 14	1	1	0	0	1	0	0
DQ3	DQ7	DQ7	WD[7][15:0]	WDSL Word 1	1	1	0	0	1	0	0
DQ0	DQ0	DQ8	WD[8][15:0]	WDSL Word 9	1	0	1	0	0	1	0
DQ1	DQ1	DQ9	WD[9][15:0]	WDSL Word 6	1	0	1	0	0	1	0
DQ2	DQ2	DQ10	WD[10][15:0]	WDSL Word 13	1	0	1	0	0	1	0
DQ3	DQ3	DQ11	WD[11][15:0]	WDSL Word 2	1	0	1	0	0	1	0
DQ0	DQ4	DQ12	WD[12][15:0]	WDSL Word 11	1	0	1	0	0	0	1
DQ1	DQ5	DQ13	WD[13][15:0]	WDSL Word 4	1	0	1	0	0	0	1
DQ2	DQ6	DQ14	WD[14][15:0]	WDSL Word 15	1	0	1	0	0	0	1
DQ3	DQ7	DQ15	WD[15][15:0]	WDSL Word 0	1	0	1	0	0	0	1
PHYSICAL VIEW OF XDR DRAM					Word Written (1 = Written, 0 = Not Written)						
DQ2	DQ6	DQ14	WD[14][15:0]	WDSL Word 15	1	0	1	0	0	0	1
		DQ6	WD[6][15:0]	WDSL Word 14	1	1	0	0	1	0	0
	DQ2	DQ10	WD[10][15:0]	WDSL Word 13	1	0	1	0	0	1	0
		DQ2	WD[2][15:0]	WDSL Word 12	1	1	0	1	0	0	0
DQ0	DQ4	DQ12	WD[12][15:0]	WDSL Word 11	1	0	1	0	0	0	1
		DQ4	WD[4][15:0]	WDSL Word 10	1	1	0	0	1	0	0
	DQ0	DQ8	WD[8][15:0]	WDSL Word 9	1	0	1	0	0	1	0
		DQ0	WD[0][15:0]	WDSL Word 8	1	1	0	1	0	0	0
DQ1	DQ1	DQ1	WD[1][15:0]	WDSL Word 7	1	1	0	1	0	0	0
		DQ9	WD[9][15:0]	WDSL Word 6	1	0	1	0	0	1	0
	DQ5	DQ5	WD[5][15:0]	WDSL Word 5	1	1	0	0	1	0	0
		DQ13	WD[13][15:0]	WDSL Word 4	1	0	1	0	0	0	1
DQ3	DQ3	DQ3	WD[3][15:0]	WDSL Word 3	1	1	0	1	0	0	0
		DQ11	WD[11][15:0]	WDSL Word 2	1	0	1	0	0	1	0
	DQ7	DQ7	WD[7][15:0]	WDSL Word 1	1	1	0	0	1	0	0
		DQ15	WD[15][15:0]	WDSL Word 0	1	0	1	0	0	0	1

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Table 12 : Core Data Word-to-WDSL Format[a]

DQ Serialization Order																
CFM/PCLK Cycle	Cycle 0								Cycle 1							
Symbol (Bit) Time	t0	t1	t2	t3	t4	t5	t6	t7	t8	t9	t10	t11	t12	t13	t14	t15
Bit Transmitted on DQ pins	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15
WDSL Byte/Bit Transfer Order																
Core Word	Core Word WD[n][15:0]															
WDSL Byte Order	WDSL Byte 0								WDSL Byte 1							
SWD Field of Serial Packet	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Bit Transmitted on CMD pin	D15	D11	D7	D3	D14	D10	D6	D2	D13	D9	D5	D1	D12	D8	D4	D0

a. Applies for first generation x16/x8/x4 XDR DRAM with BL=16

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Special Feature Description

Dynamic Width Control

This XDR DRAM device includes a feature called dynamic width control. This permits the device to be configured so that read and write data can be accessed through differing widths of DQ pins. Figure 49 shows a diagram of the logic in the path of the read data (Q) and write data (D) that accomplishes this.

The read path is on the right of the figure. There are 16 sets of S signals (the internal data bus connecting to the sense amps of the memory core), with 16 signals in each set. When the XDR DRAM device is configured for maximum width operation (using the WIDTH [2:0] field in the CFG register), each set of 16 S signals goes to one of the 16 DQ pins (via the Q[15:0][15:0] read bus) and are driven out in the 16 time slots for a read data packet.

When the XDR DRAM device is configured for a width that is less than the maximum, some of the DQ pins are used and the rest are not used. The SC [3:0] field of the COL request packets which S[15:0] [15:0] signals are passed to the Q[15:0] [15:0] read bus and driven as read data.

Figure 50 shows the mapping from the S bus to the Q bus as a function of the WIDTH [2:0] register field and the SC[3:0] field of the COL request packet. There is a separate table for each valid value of WIDTH [2:0]. In each table, there is an entry in the left column for each valid value of SC[3:0]. This field should be treated as an extension of the C[9:4] column address field. The right hand column shows which sets of S[15:0] [15:0] signals are mapped to the Q read data bus for a particular value of SC[3:0].

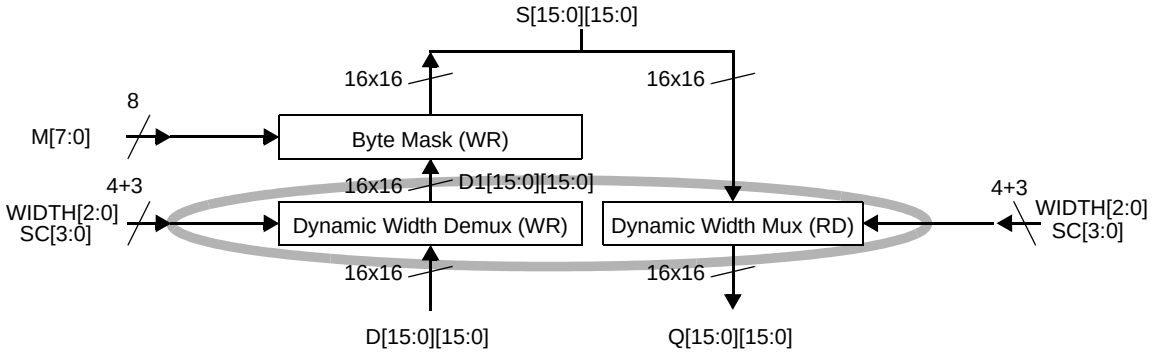
For example, assume that the WIDTH [2:0] value is “010”, indicating a device width of x4. Looking at the appropriate table in Figure50, it may be seen that in the SC [3:0] field, the SC [1:0] sub-column address bits are not used. The remaining SC [3:0] address bit(s) selects one of the 64-bit blocks of S bus signals, causing them to be driven onto the Q [3:0] [15:0] read data bus, which in turn is driven to the DQ3...0/DQN3...0 data pins. The Q[15:4] [15:0] signals and DQ15...4/DQN15....4 data pins are not used for a device width of x4.

The write path is shown on the left side of Figure 49. As shown, there are 16 sets of S signals(the internal data bus connecting to the sense amps of the memory core), with 16 signals in each set. When the XDR DRAM device is configured for maximum width operation (using the WIDTH [2:0] field in the CFG register), each set of 16 S signals is driven from one fo the 16 DQ pins (via the D[15:0] [15:0] write bus) from each of the 16 time slots for a write data packet.

Figure 50 also shows the mapping from the D bus to the S bus as a function of the WIDTH[2:0] register field and the SC[3:0] field of the COL request packet. There is a separate table for each valid value of WIDTH[2:0]. In each table, there is an entry in the left column for each valid value of SC[3:0]. This field should be treated as an extension of the C[9:4] column address field. The right hand column shows which set of S[15:0] [15:0] signals are mapped from the D read data bus for a particular value of SC[3:0].

For example, assume that the WIDTH[2:0] value is “001”, indicating a device width of x2. Looking at the appropriate table in Figure50, it may be seen that in the SC[3:0] field, the SC[0] sub-column address bit is not used. The remaining SC [3:0] address bit(s) selects one of the 32-bit blocks of S bus signals, causing them to be driven from the D [1:0] [15:0] write data bus, which in turn is driven from the DQ1... 0/DQN1... 0 data pins. The D[15:2] [15:2] signals and DQ15... 2/DQN15...2 data pins are not used for a device width of x2.

Figure 49 : Multiplexes for Dynamic Width Control



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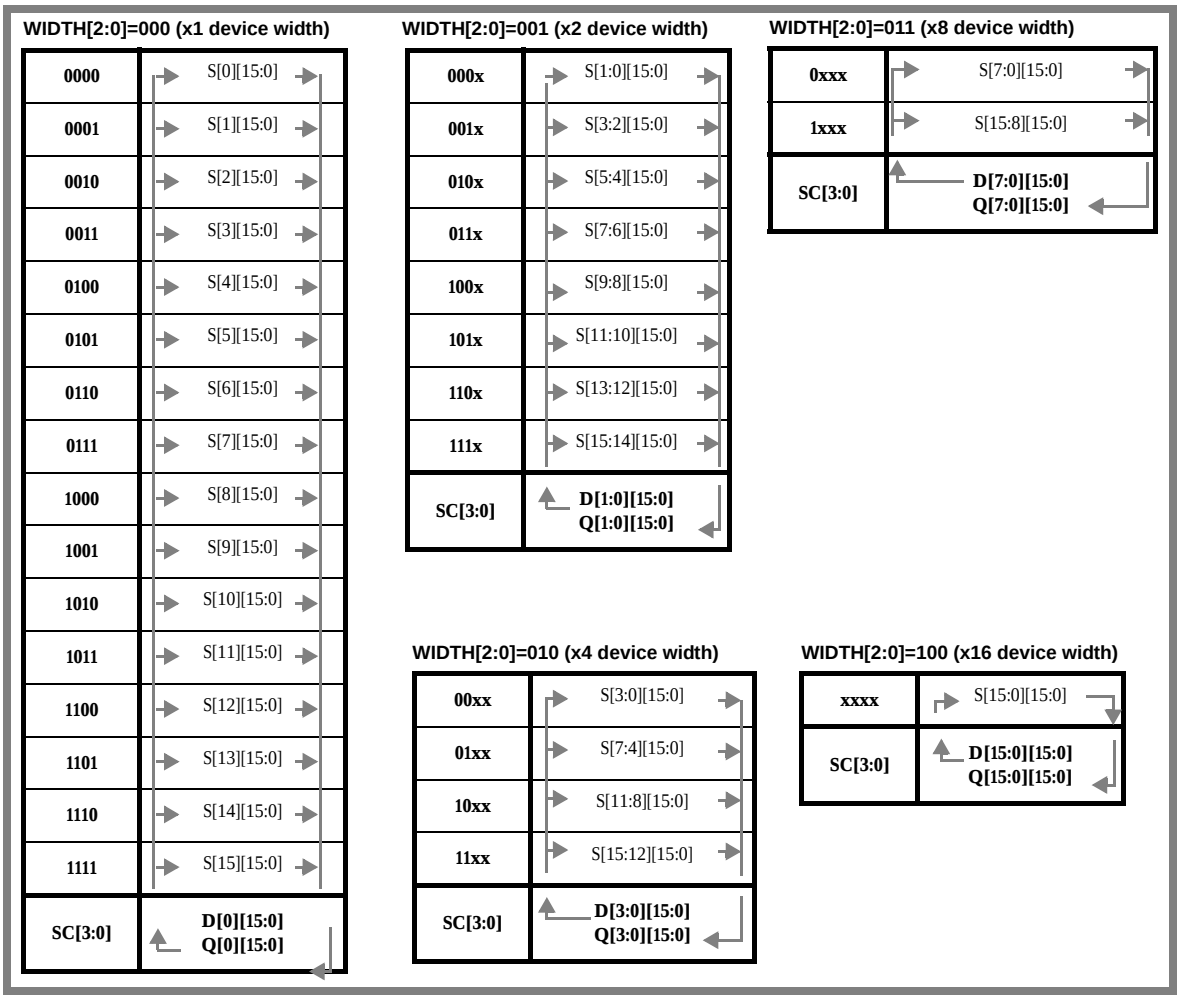
The block diagram in Figure 49 indicates that the Dynamic Width logic is positioned after the serial-to-parallel conversion (demux block) in the data receiver block and before the parallel-to-serial conversion (mux block) in the data transmitter block (see also the block diagram in Figure2). The block diagram is shown in this manner so the functionality of the logic can be made as clear as possible. Some implementations may place this logic in the data receiver and transmitter blocks, performing the mapping in Figure 50 on the serial data rather than the parallel data. However, this design choice will not affect the functionality of the Dynamic Width logic; it is strictly an implementation decision.

Figure 50 : D-toS and S-to-D Mapping for Dynamic Width Control



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Write Masking

Figure 51 shows the logic used by the XDR DRAM device when a write-masked command (WRM) is specified in a COLM packet. This masking logic permits individual byte of a write data packet to be written or not written according to the value of an eight bit write mask M [7:0].

In Figure 51, there are 16 sets of 16 bit signals forming the D1[15:0] [15:0] input bus for the Byte Mask block. These are treated as 2 x 16 8-bit bytes:

D1 [15] [15.8]

D1 [15] [7:0]

...

D1 [1] [15:8]

D1 [1] [7:0]

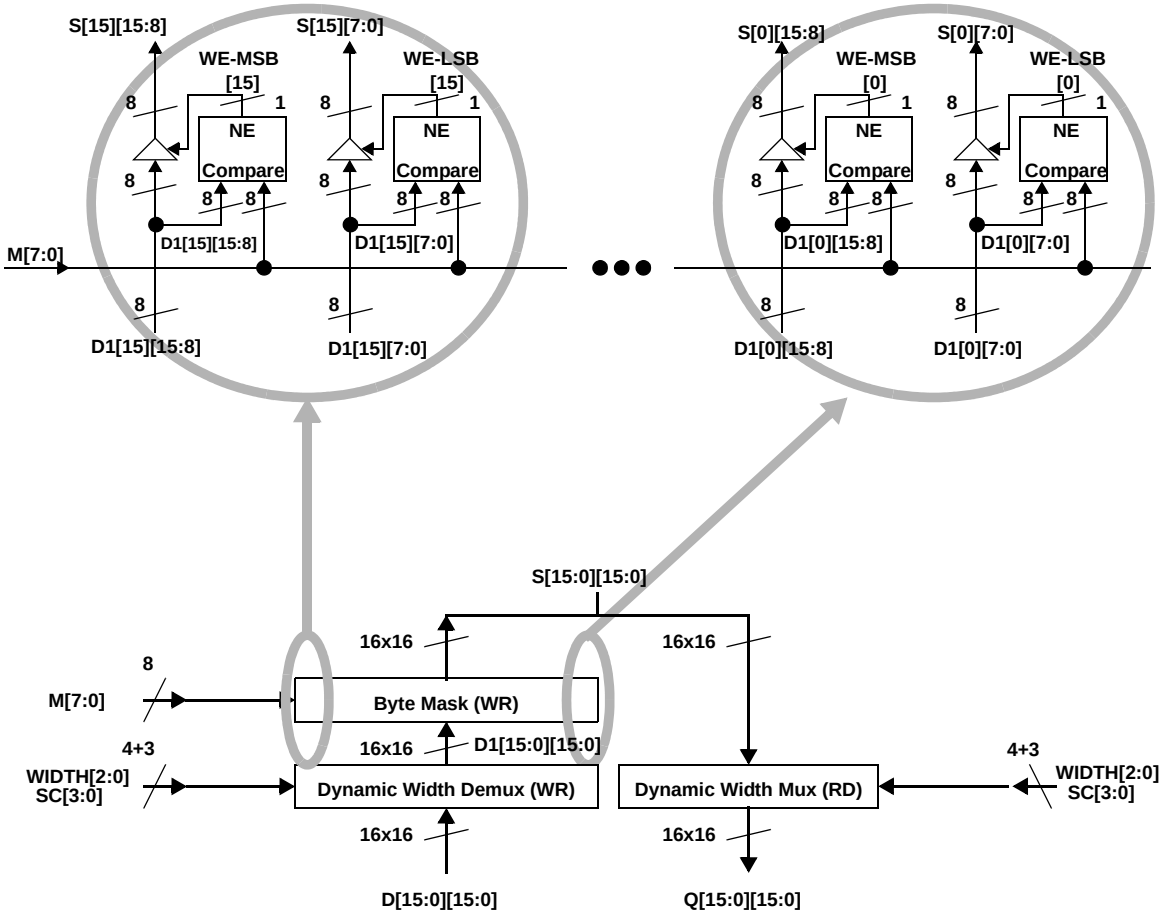
D1 [0] [15:8]

D1 [0] [7:0]

The eight bits of each byte is compared to the value in the byte mask field (M[7:0]). If they are not equal (NE), then the corresponding write enable signal (WE) is asserted and the byte is written into the sense amplifier. If they are equal, then corresponding write enable signal (WE) is deasserted and the byte is not written into the sense amplifier.

In the example of Figure 51, a WRM command performs a masked write of a 64 byte data packet to all the memory devices connected to the RQ bus (and receiving the command). It is the job of the memory controller to search the 64 bytes to find an eight bit data value that is not used and place it into the M [7:0] field. This will always be possible because there are 256 possible 8-bit values and there are only 64 possible values used in the bytes in the data packet.

Figure 51 : Byte Mask Logic



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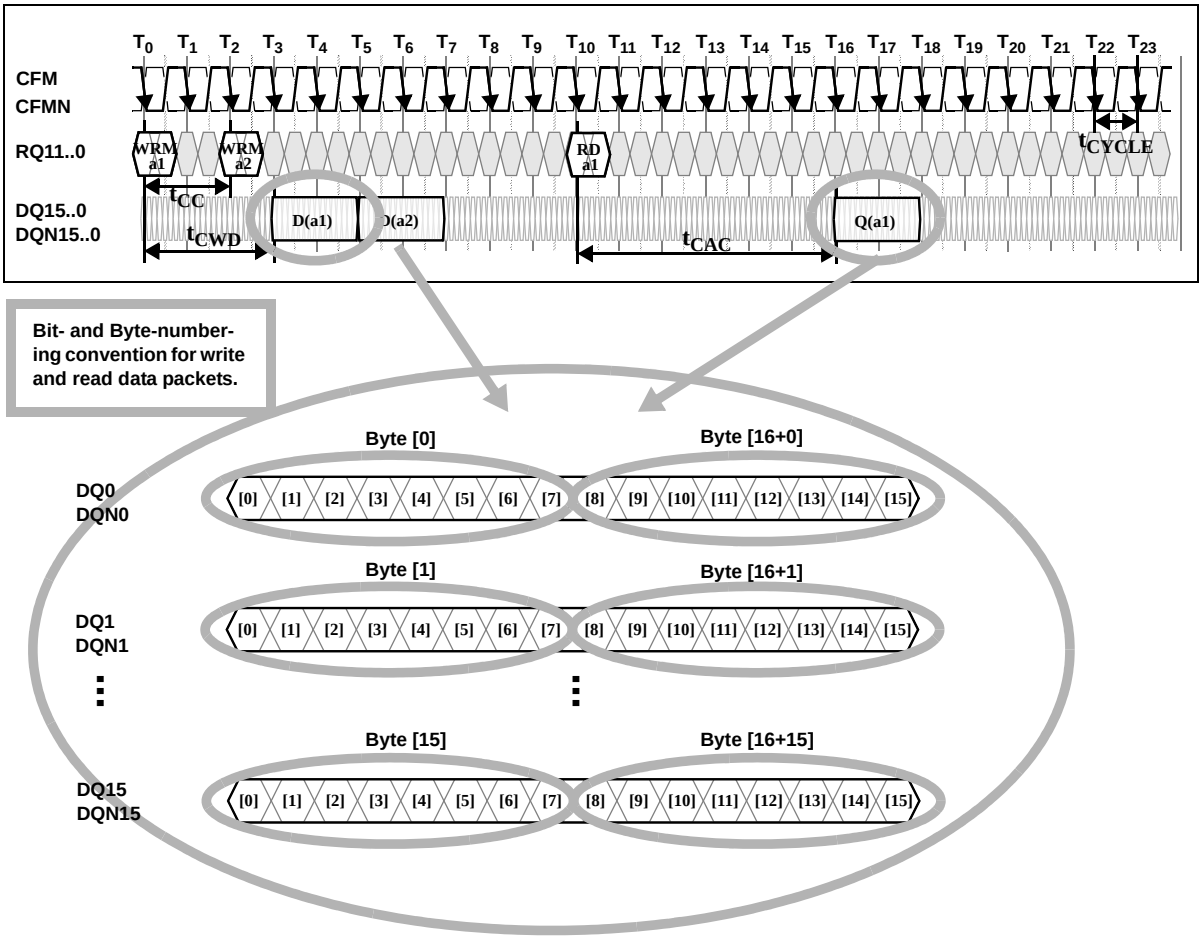
Note that other systems might use a data transfer size that is different than the 64 bytes per t_{CC} interval per RQ bus that is used in the example in Figure 51.

Figure 52 shows the timing of two successive WRM commands in COLM packets. The timing is identical to that of two successive WR commands in COL packets. The one difference is that the COLM packet includes a M[7:0] field that indicates the reserved bit pattern (for the eight bits of each byte) that indicates that the byte is not to be written. This requires that the alignment of bytes within the data packet be defined, and also that the bit numbering within each byte be defined (note that this was not necessary for the unmasked WR command). In the figure, bytes are contained within a single DQ/DQN pin pair - this is necessary so the dynamic width feature can be supported. Thus, each pin pair carries two bytes of each data packet. Byte[0] is transferred earlier than byte[1], and bit[0] of each byte (corresponding to M [0]) is transferred first, followed by the remaining bits in succession).

Figure 52 : Write-Masked (WRM) Transaction Example



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Multiple Bank sets and the ERAW Feature

Figure 55 shows a block diagram of a XDR DRAM in which the banks are divided into two sets (called the even bank set and the odd bank set) according to the least-significant bit of the bank address field. This XDR DRAM supports a feature called “Early Read After Write” (hereafter called “ERAW”)

The logic that accepts commands on the RQ11...0 signals is capable of operating these two bank sets independently. In addition, each bank set connects to its own internal “S” data bus (called S0 and S1). The receive interface is able to drive write data onto either of these internal data buses, and the transmit interface is able to sample read data from either of these internal data buses. These capabilities will permit the delay between a write column operation and a read column operation to be reduced, thereby improving performance.

Figure 53 shows the timing previously presented in Figure12, but with the activity on the internal S data bus included. The write-to-read parameter $t_{\Delta WR}$ ensures that there is adequate turnaround time on the S bus between D (a2) and Q (c1).

When ERAW is supported with odd and even bank sets, the $t_{\Delta WR,MIN}$ parameter must be obeyed when the write and read column operations are to the same bank set, but a second parameter $t_{\Delta WR-D}$ permits earlier column operations to the opposite bank set. Figure54 shows how this is possible because there are two internal data buses S0 and S1. In this example, the four columns read operations are made to the same bank Bb, but they could use different banks as long as they all belonged to the bank set that was different form the bank set containing Ba (for the column write operations).

Figure 53 : Write/Read Interaction - No ERAW Feature

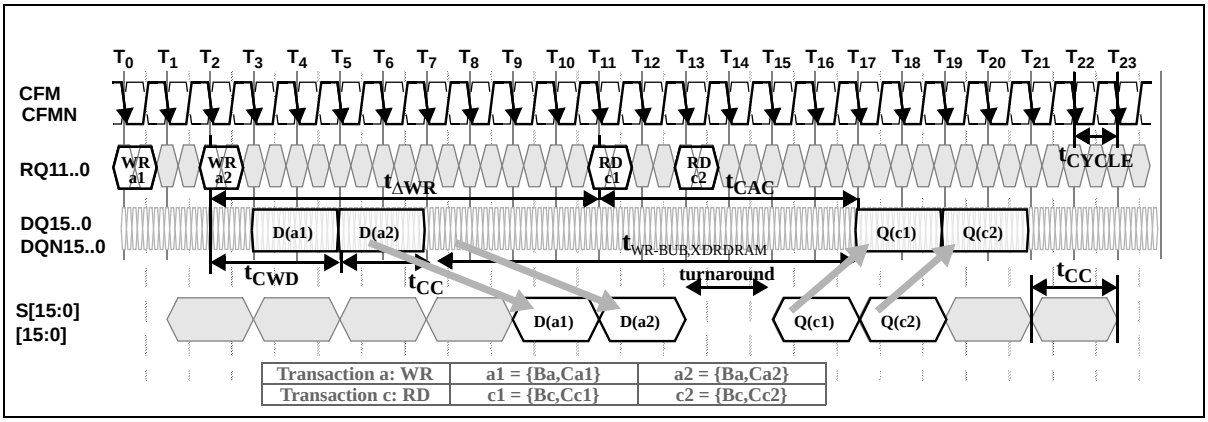

Figure 54 : Write/Read Interaction - ERAW Feature

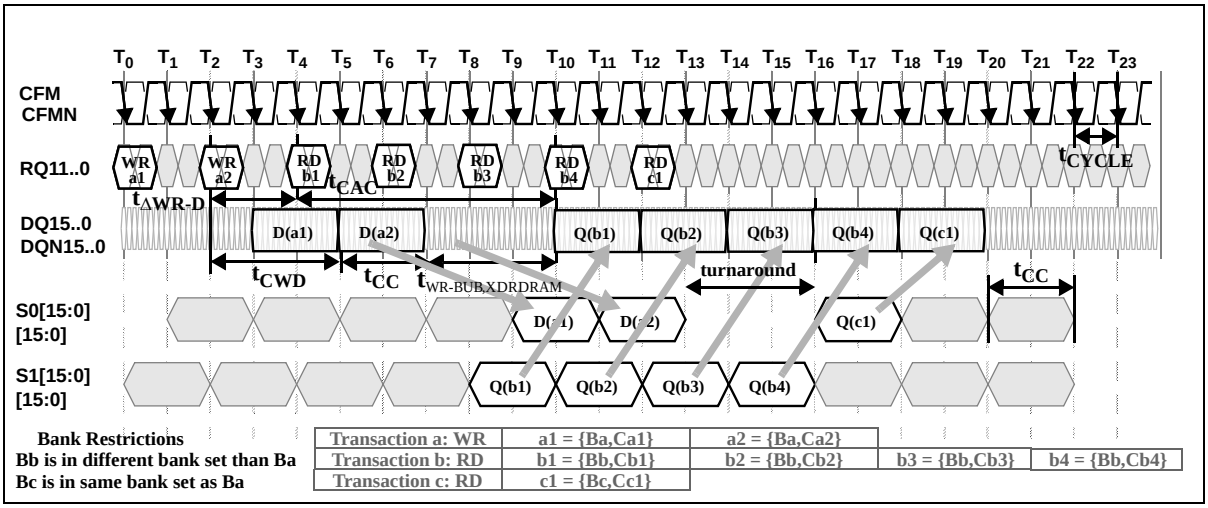

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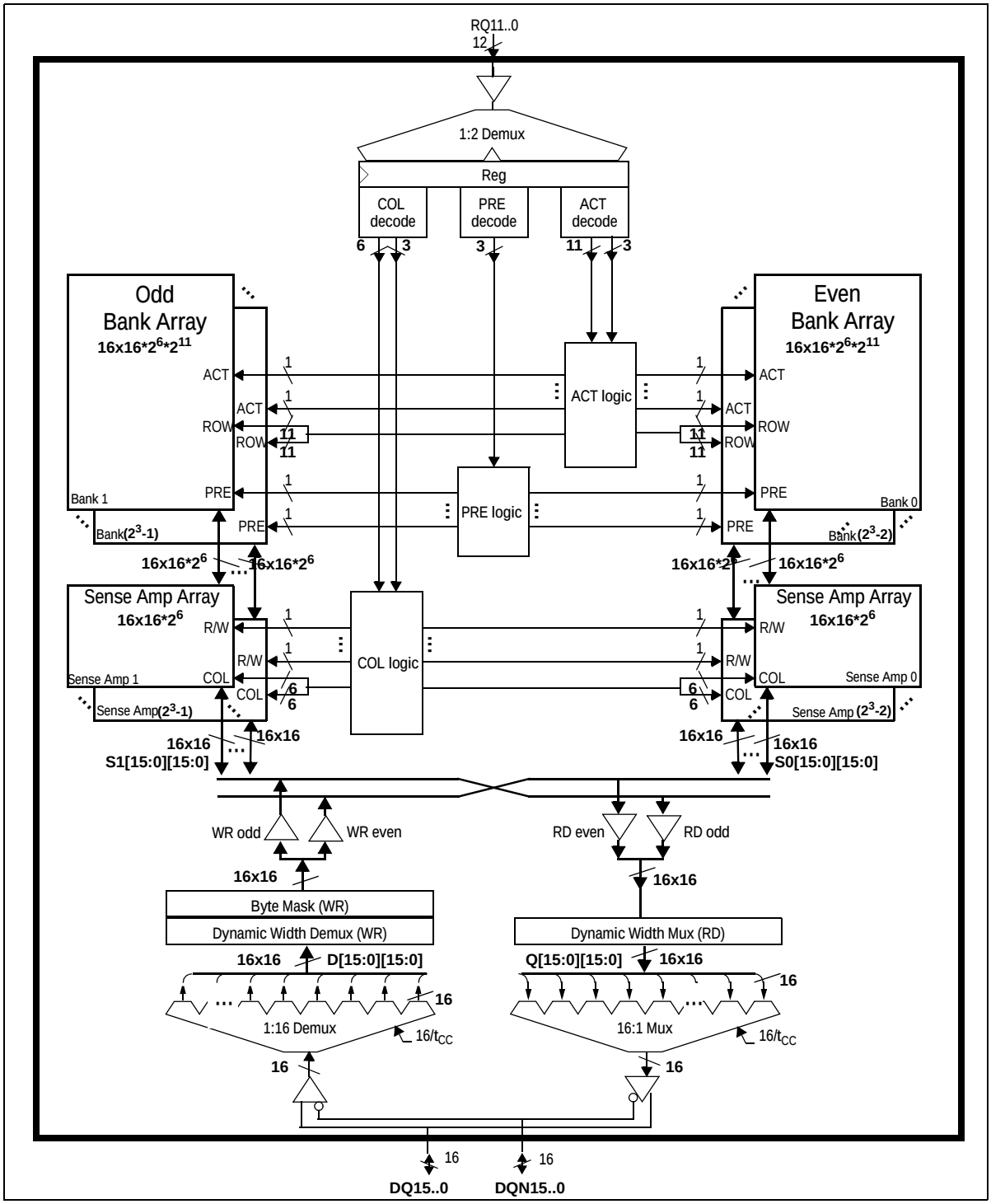
Figure 55 : XDR DRAM Block Diagram with Bank Sets



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Simultaneous Activation

When the XDR DRAM supports multiple bank sets as in Figure 55, another feature may be supported, in addition to ERAW. This feature is simultaneous activation, and the timing of several cases is shown in Figure 56.

The t_{RR} parameter specifies the minimum spacing between packets with activation commands in XDR DRAMs with a single bank set, or between packets to the same bank set in a XDR DRAM with multiple bank sets. The t_{RR-D} parameter specifies the minimum spacing between packets with activation commands to different bank sets in a XDR DRAM with multiple bank sets.

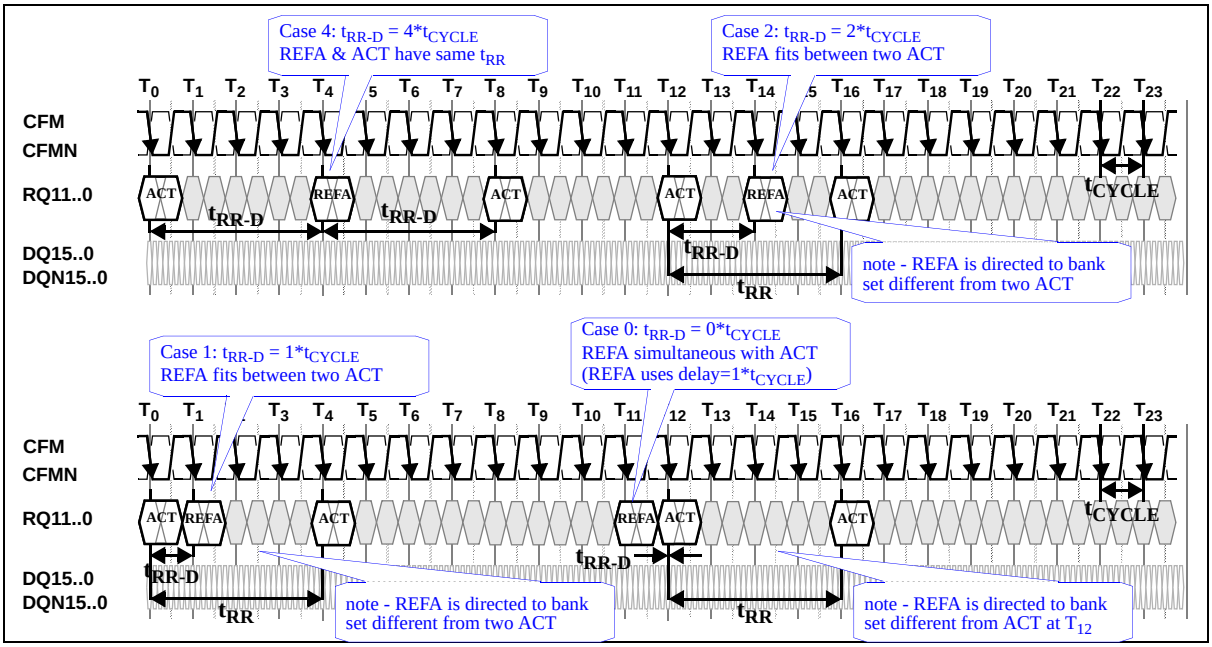
In Figure 56, Case 4 shows an example when both t_{RR} and t_{RR-D} must be at least $4*t_{CYCLE}$. In such a case, activation commands to different bank sets satisfy the same constraint as activation commands to the same bank set.

In Figure 56, Case 2 shows an example when t_{RR} must be at least $4*t_{CYCLE}$ and t_{RR-D} must be at least $2*t_{CYCLE}$. In such a case, an activation command to one bank set may be inserted between two activation commands to a different bank set.

In Figure 56, Case 1 shows an example when t_{RR} must be at least $4*t_{CYCLE}$ and t_{RR-D} must be at least $1*t_{CYCLE}$. As in the previous case, an activation command to one bank set may be inserted between two activation commands to a different bank set. In this case, the middle activation command will not be symmetrically placed relative to the two outer activation commands.

In Figure 56, Case 0 shows an example when t_{RR} must be at least $4*t_{CYCLE}$ and t_{RR-D} must be at least $0*t_{CYCLE}$. This means that two activation commands may be issued on the same CFM clock edge. This is only possible by using the delay mechanism in one of the two commands. See “Dynamic Request Scheduling” on page 18. In the example shown, the packet with the REFA command is received one cycle before the command with the ACT command, and the REFA command includes a one cycle delay. Both activation commands will be issued internally to different bank sets on the same CFM clock edge.

Figure 56 : Simultaneous Activation — t_{RR-D} Cases



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Simultaneous Precharge

When the XDR DRAM supports multiple bank sets as in Figure55, another feature may be supported, in addition to ERAW. This feature is simultaneous precharge, and the timing of several cases is shown in Figure57.

The t_{PP} parameter specifies the minimum spacing between packets with precharge commands in XDR DRAMs with a single bank set, or between packets to the same bank set in a XDR DRAM with multiple bank sets. The t_{PP-D} parameter specifies the minimum spacing between packets with precharge commands to different bank sets in a XDR DRAM with multiple bank sets.

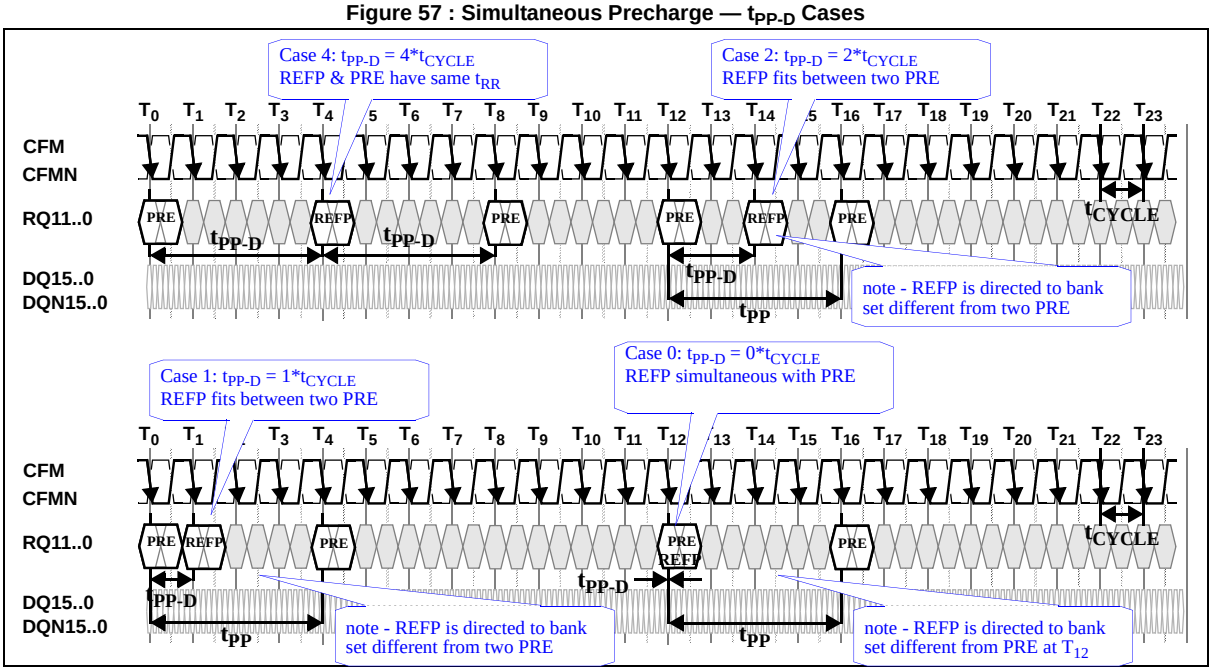
In Figure57, Case4 shows an example when both t_{PP} and t_{PP-D} must be at least $4*t_{CYCLE}$. In such a case, precharge commands to different bank sets satisfy the same constraint as precharge commands to the same bank set.

In Figure57, Case2 shows an example when t_{PP} must be at least $4*t_{CYCLE}$ and t_{PP-D} must be at least $2*t_{CYCLE}$. In such a case, a precharge command to one bank set may be inserted between two precharge commands to a different bank set.

In Figure57, Case1 shows an example when t_{PP} must be at least $4*t_{CYCLE}$ and t_{PP-D} must be at least $1*t_{CYCLE}$. As in the previous case, a precharge command to one bank set may be inserted between two precharge commands to a different bank set. In this case, the middle precharge command will not be symmetrically placed relative to the two outer precharge commands.

In Figure57, Case0 shows an example when t_{PP} must be at least $4*t_{CYCLE}$ and t_{PP-D} must be at least $0*t_{CYCLE}$. This means that two precharge commands may be issued on the same CFM clock edge. This is only possible by using the delay mechanism in one of the two commnads. See “Dynamic Request Scheduling” on page 18. It is also possibly by taking advantage of the fact that two independent precharge commands may be encoded within a single ROWP packet. In the example shown, the ROWP packet contains both a REFP command and a PRE command. Both precharge commands will be issued internally to different bank sets on the same CFM clock edge.

Figure 57 : Simultaneous Precharge — t_{PP-D} Cases



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Operating Conditions

Electrical Conditions

Table13 summarizes all electrical conditions (temperature and voltage conditions) that may be applied to the memory component. The first section of parameters is concerned with absolute voltage, storage and operating temperatures, and the power supply, reference, and termination voltage.

The second section of parameters determines the input voltage levels for the RSL RQ signals. The high and low voltages must satisfy a symmetry parameter with respect to the $V_{REF, RSL}$.

The third section of parameters determines the input voltage levels for the RSL SI(serial interface) signals. The high and low voltages must satisfy a symmetry parameter with respect to the $V_{REF, RSL}$.

The fourth section of parameters determines the input voltage levels for the CFM clock signals. The high and low voltages are specified by a common-mode value and a swing value.

The fifth section of parameters determines the input voltage levels for the write data signals on the DRSL DQ pins. The high and low voltages are specified by a common-mode value and a swing value.

Table 13 : Electrical Conditions

Symbol	Parameter	Minimum	Maximum	Unit
$V_{IN,ABS}$	Voltage applied to any pin (except V_{DD}) with respect to GND	- 0.3	1.5	V
$V_{DD,ABS}$	Voltage on V_{DD} with respect to GND	- 0.5	2.3	V
T_{STORE}	Storage temperature	- 50	100	°C
T_J	Junction temperature under bias during normal operation	100		°C
V_{DD}	Supply voltage applied to V_{DD} pins during normal operation	1.8 - 0.09	1.8 + 0.09	V
$V_{REF,RSL}$	RSL - Reference voltage applied to V_{REF} pin[a]	$V_{TERM,RSL}$ - 0.450 - 0.025	$V_{TERM,RSL}$ - 0.450 + 0.025	V
$V_{TERM,DRSL}$	DRSL - Termination voltage applied to V_{TERM} pins	1.2 - 0.06	1.2 + 0.06	V
$V_{IL,RQ}$	RSL RQ inputs -low voltage	$V_{REF,RSL}$ - 0.45	$V_{REF,RSL}$ - 0.15	V
$V_{IH,RQ}$[b]	RSL RQ inputs -high voltage	$V_{REF,RSL}$ + 0.15	$V_{REF,RSL}$ + 0.45	V
$R_{A,RQ}$	RSL RQ inputs - data asymmetry: $R_{A,RQ} = (V_{IH,RQ}-V_{REF,RSL})/(V_{REF,RSL}-V_{IL,RQ})$	TBD	TBD	V
$V_{IL,SI}$	RSL Serial Interface inputs -low voltage	$V_{REF,RSL}$ - 0.45	$V_{REF,RSL}$ - 0.20	V
$V_{IH,SI}$[b]	RSL Serial Interface inputs -high voltage	$V_{REF,RSL}$ + 0.20	$V_{REF,RSL}$ + 0.45	V
$R_{A,SI}$	RSL Serial Interface inputs - data asymmetry: $R_{A,SI} = (V_{IH,RQ}-V_{REF,RSL})/(V_{REF,RSL}-V_{IL,RQ})$	TBD	TBD	V
$V_{ICM,CFM}$	CFM/CFMN input - common mode: $V_{ICM,CTM} = (V_{IH,CFM}{}^{b}+V_{IL,CTM})/2$	$V_{TERM,DRSL}$-0.150	$V_{TERM,DRSL}$-0.075	V
$V_{ISW,CFM}$	CFM/CFMN input - high-low swing: $V_{ISW,CFM} = (V_{IH,CTM}{}^{b} - V_{IL,CTM})$	0.15	0.30	V
$V_{ICM,DQ}$	DRSL DQ inputs - common mode: $V_{ICM,DQ} = (V_{IH,DQ}{}^{b}+V_{IL,DQ})/2$	$V_{TERM,DRSL}$-0.150	$V_{TERM,DRSL}$-0.025	V
$V_{ISW,DQ}$	DRSL DQ inputs - high-low swing: $V_{ISW,DQ} = (V_{IH,DQ}{}^{b} - V_{IL,DQ})$	0.05	0.30	V

a. $V_{TERM,RSL}$ is typically 1.2V±0.06V. It connects to the RSL termination components, not to this DRAM component.
b. V_{IH} is typically equal to $V_{TERM,RSL}$ or $V_{TERM,DRSL}$ (whichever is appropriate) under DC conditions in a system.

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Timing Conditions

Table14 summarizes all timing conditions that may be applied to the memory component. The first section of parameters is concerned with parameters for the clock signals. The second section of parameters is concerned with parameters for the request signals. The third section of parameters is concerned with parameters is concerned with parameters for the write data signals. The fourth section of parameters is concerned with parameters for the serial interface signals. The fifth section is concerned with all other parameters, including those for refresh, calibration, power state transitions, and initialization.

Table 14 : Timing Conditions

Symbol	Parameter and Other Conditions	Minimum	Maximum	Units	Figure(s)
t_{CYCLE} or $t_{CYC,CTM}$	CFM RSL clock - cycle time -4000 -3200 -2400	2.00 2.50 3.33	3.83 3.83 3.83	ns ns ns	Figure 58
$t_{R,CFM}$, $t_{F,CFM}$	CFM/CFMN input - rise and fall time - use minimum for test.	0.08	0.20	t_{CYCLE}	Figure 58
$t_{H,CFM}$, $t_{L,CFM}$	CFM/CFMN input - high and low times	40%	60%	t_{CYCLE}	Figure 58
$t_{R,RQ}$, $t_{F,RQ}$	RSL RQ input - rise/fall times (20% - 80%) - use minimum for test.	0.08	0.26	t_{CYCLE}	Figure 59
$t_{S,RQ}$, $t_{H,RQ}$	RSL RQ input to sample points (set/hold) @ 2.50 ns > $t_{CYCLE} \geq$ 2.00 ns @ 3.33 ns > $t_{CYCLE} \geq$ 2.50 ns @ 3.83 ns $\geq t_{CYCLE} \geq$ 3.33 ns	tbd 0.200 tbd	- - -	ns ns ns	Figure 59
$t_{IR,DQ}$, $t_{IF,DQ}$	DRSL DQ input - rise/fall times (20% - 80%) - use minimum for test.	0.020	0.074	t_{CYCLE}	Figure 60
$t_{S,DQ}$, $t_{H,DQ}$	DRSL DQ input to sample points (set/hold) @ 2.50 ns > $t_{CYCLE} \geq$ 2.00 ns @ 3.33 ns > $t_{CYCLE} \geq$ 2.50 ns @ 3.83 ns $\geq t_{CYCLE} \geq$ 3.33 ns	tbd 0.065 tbd	- - -	ns ns ns	Figure 60
$t_{DOFF,DQ}$	DRSL DQ input delay offset (fixed) to sample points	-0.08	+0.08	t_{CYCLE}	Figure 60
$t_{CYC,SCK}$	Serial Interface SCK input - cycle time	20	-	ns	Figure 62
$t_{R,SCK}$, $t_{F,SCK}$	Serial Interface SCK input - rise and fall times	-	5.0	ns	Figure 62
$t_{H,SCK}$, $t_{L,SCK}$	Serial Interface SCK input - high and low times	40%	60%	$t_{CYC,SCK}$	Figure 62
$t_{IR,SI}$, $t_{IF,SI}$	Serial Interface CMD,RST,SDI input - rise and fall times	-	5.0	ns	Figure 62
$t_{S,SI}$,$t_{H,SI}$	Serial Interface CMD,SDI input to SCK clock edge - set/hold time	5	-	ns	Figure 62
$t_{DLY,SI-RQ}$	Delay from last SCK clock edge for register write to first CFM edge with RQ packet containing a command which uses the value in the register. Also, delay from first CFM edge with RQ packet containing a command which modifies register value to the first SCK clock edge for register read to this register.	10	-	$t_{CYC,SCK}$	-
t_{REF}	Refresh interval. Every row of every bank must be accessed at least once in this interval with a ROW-ACT, ROWP-REF or ROWP-REFI command.	-	16	ms	Figure 44
$t_{REFA-REFA,AVG}$	Average refresh command interval. ROWP-REFA or ROWP-REFI commands must be issued at this average rate. This depends upon t_{REF} and the number of banks and the number of rows: $t_{REFI} = t_{REF}/(N_B*N_R) = t_{REF}/(2^3*2^{11})$.	$t_{REFA-REFA,AVG}$ = 488		ns	-
$N_{REFA,BURST}$	Refresh burst limit. The number of ROWP-REFA or ROWP-REFI commands which can be issued consecutively at the minimum command spacing.	-	128	commands	-
$t_{BURST-REFA}$	Refresh burst interval. The interval between a burst of $N_{REFA,BURST,MAX}$ ROWP-REFA or ROWP-REFI commands and the next ROWP-REFA or ROWP-REFI command.	-	TBD	t_{CYCLE}	-
$t_{COREINIT}$	Interval needed for core initialization after power is applied.	-	1.5	ms	-
t_{CALC}	Current calibration interval	-	100	ms	Figure 45
$t_{CMD-CALC}$, $t_{CMD-CALZ}$	Delay between packet with any command and CALC/CALZ packet w/ PRE or REFP command w/ any other command	4 16	- -	t_{CYCLE}	Figure 45
t_{CALCE}, t_{CALZE}	Delay between CALC/CALZ packet and CALE packet	12	-	t_{CYCLE}	Figure 45
$t_{CALE-CMD}$	Delay between CALE packet and packet with any command	24	-	t_{CYCLE}	Figure 45
$t_{CMD-PDN}$	Last command before PDN entry	16	-	t_{CYCLE}	Figure 46
$t_{PDN-CFM}$	RSL CFM/CFMN and V_{TERM} stable after PDN entry	16	-	t_{CYCLE}	Figure 46
$t_{CFM-PDN}$	RSL CFM/CFMN and V_{TERM} stable before PDN exit	16	-	t_{CYCLE}	Figure 46
$t_{PDN-CMD}$	First command after PDN exit (includes lock time for CFM/CFMN)	4096	-	t_{CYCLE}	Figure 46

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Operating Characteristics

Electrical Characteristics

Table15 summarizes all electrical parameters (temperature, current and voltage) that characterize this memory component. The only exception is the supply current values(I_{DD}) under different operating conditions covered in the Supply Current Profile section.

The first section of parameters is concerned with the thermal characteristics of the memory component.

Ther second section of parameters is concerned with the current needed by the RQ pins and V_{REF} pin.

The third section of parameters is concerned with the current needed by the DQ pins and voltage levels produced by the DQ pins when driving read data. This section is also concerned with the current needed by the V_{TERM} pin, and with the resistance levels produced for the internal termination components that attach to the DQ pins.

The fourth section of parameters determines the output voltage levels and the current needed for the serial interface signals.

Table 15 : Electrical Characteristics

Symbol	Parameter	Minimum	Maximum	Units
Θ_{JC}	Junction-to-case thermal resistance	-	TBD	°C/Watt
$I_{I,RSL}$	RSL RQ or Serial Interface input current @ (V_{IN}= $V_{IH,RQ,MAX}$)	-10	10	uA
$I_{REF,RSL}$	$V_{REF,RSL}$ current @ $V_{REF,RSL,MAX}$ flowing into V_{REF} pin	-10	10	uA
$V_{OSW,DQ}$	DRSL DQ outputs - high-low swing: $V_{OSW,DQ}$=($V_{IH,DQ}$-$V_{IL,DQN}$) or ($V_{IH,DQN}$-$V_{IL,DQ}$) (See Figure 27) ODF = 00 ODF=01 ODF=10 ODF=11	0.225 TBD TBD TBD	0.350 TBD TBD TBD	V
$R_{TERM,DQ}$	DRSL DQ outputs - termination resistance	40.0	60.0	Ω
$V_{OL,SI}$	RSL serial interface SDO output - low voltage	0.0	0.25	V
$V_{OH,SI}$	RSL serial interface SDO output - high voltage	$V_{TERM,RSL}$ - 0.25	$V_{TERM,RSL}$	V

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Supply Current Profile

In this section, Table16 summarizes the supply current (I_{DD}) that characterizes this memory component. This parameter is shown under different operating conditions.

Table 16 : Supply Current Profile

Symbol	Power State and Steady State Transaction Rates	Maximum @t_{CYCLE}= 2.00 ns	Maximum @t_{CYCLE}= 2.50 ns	Maximum @t_{CYCLE}= 3.33 ns	Units
$I_{DD,PDN}$	Device in PDN, self-refresh enabled. [a]	TBD	9500	TBD	uA
$I_{DD,STBY}$	Device in STBY. This is for a device in STBY with no packets on the Channel[a]	TBD	340	TBD	mA
$I_{DD,REF}$	Device in STBY and refreshing rows at the $t_{REF,MAX}$ period.[a]	TBD	-	TBD	mA
$I_{DD,WR}$	ACT command every t_{RR}, PRE command every t_{PP}, WR command every t_{CC}.[a]	TBD	1120	TBD	mA
$I_{DD,RD}$	ACT command every t_{RR}, PRE command every t_{PP}, RD command every t_{CC}[a,b]	TBD	1200	TBD	mA
$I_{TERM,DRSL,NONE}$	No RD nor WR commands issued. [c]	TBD	35	TBD	mA
$I_{TERM,DRSL,RD}$	RD command every t_{CC}.[c]	TBD	100	TBD	mA
$I_{TERM,DRSL,WR}$	WR command every t_{CC}.[c]	TBD	200	TBD	mA

a. I_{DD} current @ $V_{DD,MAX}$ flowing into V_{DD} pins

b. This does not include the $I_{OL,DQ}$ sink current. The device dissipates $I_{OL,DQ} \cdot V_{TERM,DQ}$ in each DQ/DQN pair when driving data.

c. $I_{TERM,DRSL}$ current @ $V_{TERM,DQ,MAX}$ flowing into V_{TERM} pins

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Timing Characteristics

Table 17 summarizes all timing parameters that characterize this memory component. The only exceptions are the core timing parameters that are speed-bin dependent. Refer to the Timing Parameters section for more information.

The first section of parameters pertains to the timing of the DQ pins when driving read data.

The second section of parameters is concerned with the timing for the serial interface signals when driving register read data.

The third section of parameters is concerned with the time intervals needed by the interface to transition between power states.

Table 17 : Timing Characteristics

Symbol	Parameter and Other Conditions	Minimum	Maximum	Units	Figure(s)
$t_{Q,DQ}$	DRSL DQ output delay (variation across 16 Q bits on each DQ pin) from drive points - output delay @ 2.50 ns > $t_{CYCLE} \geq$ 2.00 ns @ 3.33 ns > $t_{CYCLE} \geq$ 2.50 ns @ 3.83 ns $\geq t_{CYCLE} \geq$ 3.33 ns	tbd -0.065 tbd	tbd +0.065 tbd	ns ns ns	Figure 61
$t_{QOFF,DQ}$	DRSL DQ output delay offset (a fixed value for all 16 Q bits on each DQ pin) from drive points - output delay	0.00	+0.20	t_{CYCLE}	Figure 61
$t_{OR,DQ}$, $t_{OF,DQ}$	DRSL DQ output - rise and fall times (20%-80%).	0.02	0.04	t_{CYCLE}	Figure 61
$t_{Q,SI}$	Serial SCK-to-SDO output delay @ $C_{LOAD,MAX}$ = 15 pF	2	15	ns	Figure 63
$t_{P,SI}$	Serial SDI-to-SDO propagation delay @ $C_{LOAD,MAX}$ = 15 pF	-	15	ns	Figure 63
$t_{OR,SI}$, $t_{OF,SI}$	Serial SDO output rise/fall (20%-80%) @ $C_{LOAD,MAX}$ = 15 pF	-	10	ns	Figure 63
$t_{PDN-ENTRY}$	Time for power state to change after PDN entry	-	16	t_{CYCLE}	Figure 46
$t_{PDN-EXIT}$	Time for power state to change after PDN exit	0	-	t_{CYCLE}	Figure 46

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Timing Parameters

Table18 summarizes the timing parameters that characterize the core logic of this memory component.. These timing parameters will vary as a function of the component's speed bin. The four sections deal with the timing intervals between packets with, respectively, row-row commands, row-column commands, column-column commands, and column-row commands.

Table 18 : Timing Parameters

Symbol	Parameter and Other Conditions		Min (A)	Min (B)	Min (C)	Units	Figure(s)
t_{RC}	Row-cycle time: interval between successive ROWA-ACT or ROWP-REFA or ROWP-REFI activate commands to the same bank.	t_{RC} $t_{RC-R, 2tCC} = t_{RCD-R} + t_{CC} + t_{RDP} + t_{RP}$[a] $t_{RC-W, 2tCC, noERAW} = t_{RCD-W} + t_{CC} + t_{WRP} + t_{RP}$[a] $t_{RC-W, 2tCC, ERAW} = t_{RCD-W} + t_{CC} + t_{WRP} + t_{RP}$[a]	16 16 19 23	20 20 24 28	24 24 24 28	t_{CYCLE}	Figure 4 - Figure 7
t_{RAS}	Row-asserted time: interval between a ROWA-ACT or ROWP-REFA or ROWP-REFI activate command and a ROWP-PRE or ROWP-REFP precharge command to the same bank. Note that $t_{RAS,MAX}$ is 64 us for all timing bins.		10	13	17	t_{CYCLE}	Figure 4 - Figure 7
t_{RP}	Row-precharge time: interval between a ROWP-PRE or ROWP-REFP precharge command and a ROWA-ACT or ROWP-REFA or ROWP-REFI activate command to the same bank.		6	7	7	t_{CYCLE}	Figure 4 - Figure 7
t_{PP}	Precharge-to-precharge time: interval between successive ROWP-PRE or ROWP-REFP precharge commands to different banks.	t_{PP} t_{PP-D}[b]	4 1	4 1	4 1	t_{CYCLE}	Figure 4 - Figure 7
t_{RR}	Row-to-row time: interval between ROWA-ACT or ROWP- REFA or ROWP-REFI activate commands to different banks.	t_{RR} t_{RR-D}[c]	4 4	4 4	4 4	t_{CYCLE}	Figure 4 - Figure 7
t_{RCD-R}	Row-to-column-read delay: interval between a ROWA-ACT activate command and a COL-RD read command to the same bank.		5	7	7	t_{CYCLE}	Figure 4 - Figure 7
t_{RCD-W}	Row-to-column-write delay: interval between a ROWA-ACT activate command and a COL-WR or COL-WRM write command to the same bank.		1	3	3	t_{CYCLE}	Figure 4 - Figure 7
t_{CAC}	Column access delay: interval from COL-RD read command to Q read data		6	7	7	t_{CYCLE}	Figure 10
t_{CWD}	Column write delay: interval from a COL-WR or COLM-WRM write command to D write data.		3	3	3	t_{CYCLE}	Figure 9
t_{CC}	Column-to-column time: interval between successive COL-RD commands, or between successive COL-WR or COLM-WRM commands.		2	2	2	t_{CYCLE}	Figure 4 - Figure 7
$t_{RW-BUB, XDRDRAM}$	Read-to-write bubble time: interval between the end of a Q read data packet and the start of D write data packet (the end of a data packet is the time interval t_{CC} after its start).		3	3	3	t_{CYCLE}	Figure 13
$t_{WR-BUB, XDRDRAM}$	Write-to-read bubble time: interval between the end of a D writed data and the start of Q read data packet (the end of a data packet is the time interval t_{CC} after its start).		3	3	3	t_{CYCLE}	Figure 13
$t_{\Delta RW}$	Read-to-write time: interval between a COL-RD read command and a COL-WR or COLM-WRM write command.[d]		8	9	9	t_{CYCLE}	Figure 12
$t_{\Delta WR}$	Write-to-read time: interval between a COL-WR or COLM-WRM write command and a COL-RD read command.	$t_{\Delta WR}$ $t_{\Delta WR-D}$[e]	9 2	10 2	10 2	t_{CYCLE}	Figure 12
t_{RDP}	Read-to-precharge time: interval between a COL-RD read command and a ROWP-PRE precharge command to the same bank.		3	4	4	t_{CYCLE}	Figure 4 - Figure 7
t_{WRP}	Write-to-precharge time: interval between a COL-WR or COLM-WRM write command and a ROWP-PRE precharge command to the same bank.		10	12	12	t_{CYCLE}	Figure 4 - Figure 7
t_{DR}	Write data-to-read time: interval between the start of D write data and a COL-RD read command to the same bank.		6	7	7	t_{CYCLE}	Figure 12
t_{DP}	Write data-to-precharge time: interval between D write data and ROWP-PRE precharge command to the same bank.		7	9	9	t_{CYCLE}	Figure 9
$t_{LRRn-LRRn}$	Interval between ROWP-LRRn command and a subsequent ROWP-LRRn command. [f]		16	20	24	t_{CYCLE}	Table5
$t_{REFx-LRRn}$	Interval between ROWP-REFx command and a subsequent ROWP-LRRn command.		16	20	24	t_{CYCLE}	Table5
$t_{LRRn-REFx}$	Interval between ROWP-LRRn command and a subsequent ROWP-REFx command.		16	20	24	t_{CYCLE}	Table5

a. The $t_{RC,MIN}$ parameter is applicable to all transaction types (read, write, refresh, etc.). Read and write transactions may have an additional limitation, depending upon how many column accesses (each requiring t_{CC}) are performed in each row access (t_{RC}). The table lists the special cases ($t_{RC-R, 2tCC}$, $t_{RC-W, 2tCC, noERAW}$, $t_{RC-W, 2tCC, ERAW}$) in which two column accesses are performed in each row access. Note that $t_{RC-W, 2tCC, ERAW}$ uses a relaxed value of t_{RCD-W} that is equal to $t_{RCD-R,MIN}$. All other parameters are minimum.

b. t_{PP-D} is the t_{PP} parameter for precharges to different bank sets. See "Simultaneous Precharge" on page 53.

c. t_{RR-D} is the t_{RR} parameter for activates to different bank sets. See "Simultaneous Activation" on page 52.

d. See "Propagation Delay" on page 27.

e. $t_{\Delta WR-D}$ is the $t_{\Delta WR}$ parameter for write-read accesses to different bank sets. See "Multiple Bank Sets and the ERAW Feature" on page 50. Also, note that the value of $t_{\Delta WR-D}$ may not take on the values {3,5,7} within the range{$t_{\Delta WR-D,MIN}$, ... $t_{\Delta WR,MIN}$-1}. t_{DWR-D} may assume any value $\geq t_{\Delta WR,MIN}$.

f. ROWP-LRRn includes the commands {ROWP-LRR0,ROWP-LRR1,LOWP-LRR2}, ROWP-REFx includes the commands {ROWP-REFA,ROWP-REFI, LOWP-REFP},

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Receive/Transmit Timing

Clocking

Figure58 shows a timing diagram for the CFM/CFMN clock pins of the memory component. This diagram represents a magnified view of these pins. This diagram shows only one clock cycle.

CFM and CFMN are differential signals: one signal is the complement of the other. They are also high-true signals - a low voltage represents a logical zero and a high voltage represents a logical one. There are two crossing points in each clock cycle. The primary crossing point includes the high-voltage-to-low-voltage transition of CFM (indicated with the arrowhead in the diagram). The secondary crossing point includes the low-voltage-to-high-voltage transition of CFM. All timing events on the RSL signals are referenced to the first set of edges.

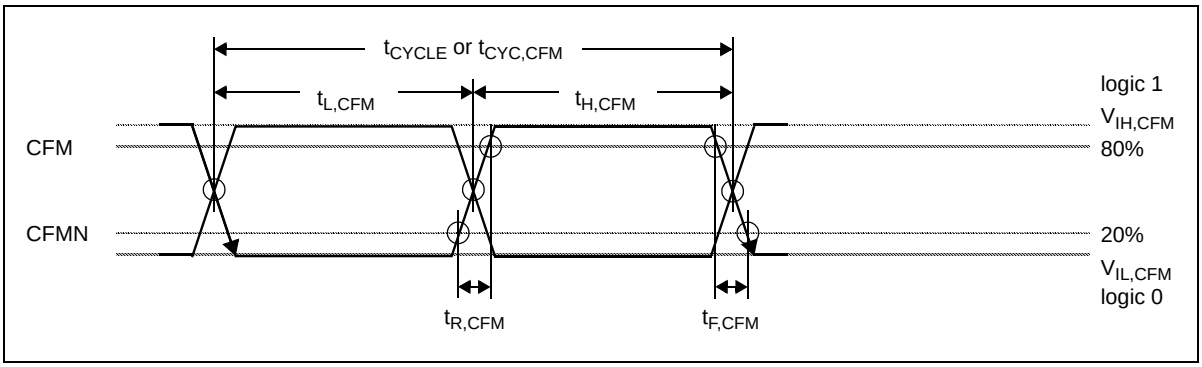
Timing events are measured to and from the crossing point of the CFM and CFMN signals. In the timing diagram, this is how the clock-cycle time (t_{CYCLE} or $t_{CYC, CFM}$), clock-low time ($t_{L, CFM}$) and clock-high time ($t_{H, CFM}$) are measured.

Because timing intervals are measured in this fashion, it is necessary to constrain the slew rate of the signals. The rise ($t_{R, CFM}$) and fall time ($t_{F, CFM}$) of the signals are measured from the 20% and 80% points of the full-swing levels.

20% = V_{IL}, CFM + 0.2*(V_{IH}, CFM - V_{IL}, CFM)

80% = V_{IL}, CFM + 0.8*(V_{IH}, CFM - V_{IL}, CFM)

Figure 58 : Clocking Waveforms



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RSL RQ Receive Timing

Figure59 shows a timing diagram for the RQ11...0 request pins of the memory component. This diagram represents a magnified view of the pins and only a few clock cycle (CFM and CFMN are the clock signals). Timing events are measured to and from the primary CFM/CFMN crossing point in which CFM makes its high-voltage-to-low-voltage transition. The RQ11...0 signals are low-true: a high voltage represents a logical zero and a low voltage represents a logical one. Timing events on the RQ11... 0 pins are measured to and from the point that the signal reaches the level of the reference voltage $V_{REF, RSL}$.

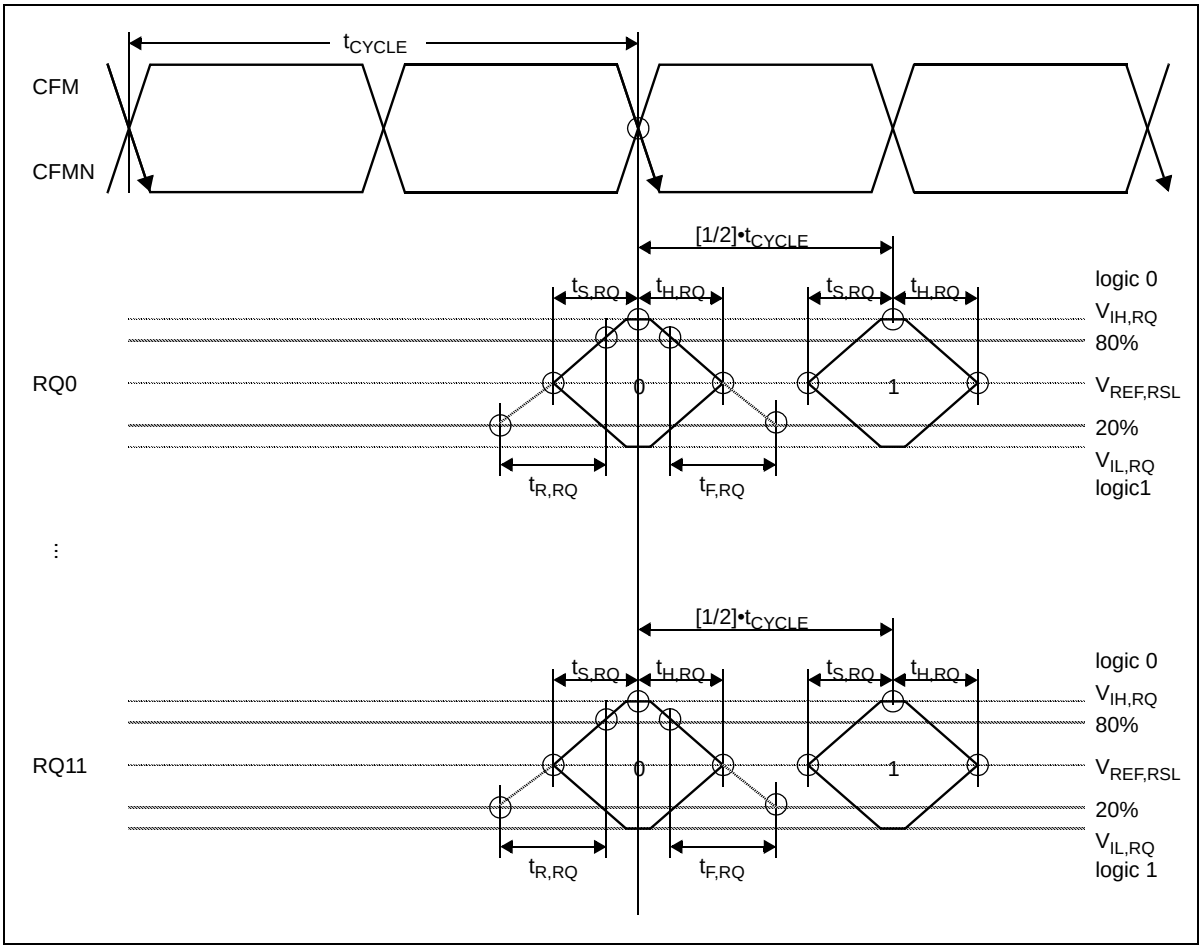
Because timing intervals are measured in this fashion, it is necessary to constrain the slew rate of the signals. The rise ($t_{R, RQ}$) and fall time ($t_{F, RQ}$) of the signals are measured from the 20% and 80% points of the full-swing levels.

20% = $V_{IL, RQ}$ + 0.2*(V_{IH}, RQ - $V_{IL, RQ}$)

80% = $V_{IL, RQ}$ + 0.8*(V_{IH}, RQ - $V_{IL, RQ}$)

There are two data receiving windows defined for each RQ11...0 signal. The first of these (labeled “0”) and a set time, $t_{S,RQ}$, and a hold time, $t_{H,RQ}$, measured around the primary CFM/CFMN crossing point. The second (labeled “1”) has a set time ($t_{S, RQ}$) and a hold time ($t_{H, RQ}$) measured around a point 0.5*t_{CYCLE} after the primary CFM/CFMN crossing point.

Figure 59 : RSL RQ Receive Waveform



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DRSL DQ Receive Timing

Figure60 shows a timing diagram for receiving write data on the DQ/DQN data pins of the memory component. This diagram represents a magnified view of the pins and only a few clock cycles are shown (CFM and CFMN are the clock signals). Timing events are measured to and from the primary CFM/CFMN crossing point in which CFM makes its high-voltage-to-low -voltage transition. The DQ15...0/DQN15...0 signals are high-true: a low voltage represents a logical zero and a high voltage represents a logical one. They are also differential - timing events on the DQ15...0/DQN15... 0 pins are measured to and from the point that each differential pair crosses.

Because timing intervals are measured in this fashion, it is necessary to constrain the slew rate of the signals. The rise time ($t_{IR, DQ}$) and fall time ($t_{IF, DQ}$) of the signals are measured from the 20% and 80% points of the full-swing levels.

20% = $V_{IL, DQ} + 0.2*(V_{IH, DQ} - V_{IL, DQ})$

80% = $V_{IL, DQ} + 0.8*(V_{IH, DQ} - V_{IL, DQ})$

There are 16 data receiving windows defined for each DQ15...0/DQN15... 0 pin pair. The receiving windows for a particular DQi/DQNi pin pair is referenced to an offset parameter $t_{DOFF,DQi}$ (the index “i” may take on the values {0, 1, .. , 15} and refers to each of the DQ15... 0/DQN15... 0 pin pairs).

The $t_{DOFF,DQi}$ parameter determines the time between the primary CFM/CFMN crossing point and the offset point for the DQi/DQNi pin pair. The 16 receiving windows are placed at times $t_{DOFF,DQi} + (j/8)*t_{CYCLE}$ (the index “j” may take on the values {0, 1, .. , 15} and refers to each of the receiving windows for the DQi/DQNi pin pair).

The offset values $t_{DOFF,DQi}$ for each of the 16 DQi/DQNi pin pairs can be different. However, each is constrained to lie inside the range {$t_{DOFF,MIN}$, $t_{DOFF,MAX}$}. Furthermore, each offset value $t_{DOFF,DQi}$ is static and will not change during system operation. Its value can be determined at initialization.

The 16 receiving windows (j = 0 ... 15) for the first pair DQ0/DQN0 are labeled “0” through “15”. Each window has a set time ($t_{S, DQ}$) and a hold time ($t_{H, DQ}$) measured around a point $t_{DOFF,DQ0} + (j/8) *t_{CYCLE}$ after the primary CFM/CFMN crossing point.

The 16 receiving windows (j = 0 ... 15) for the each of the other pairs DQi/DQNi are also labeled “0” through “15”. Each window has a set time ($t_{S, DQ}$) and a hold time ($t_{H, DQ}$) measured around a point $t_{DOFF,DQi} + (j/8)*t_{CYCLE}$ after the primary CFM/CFMN crossing point.

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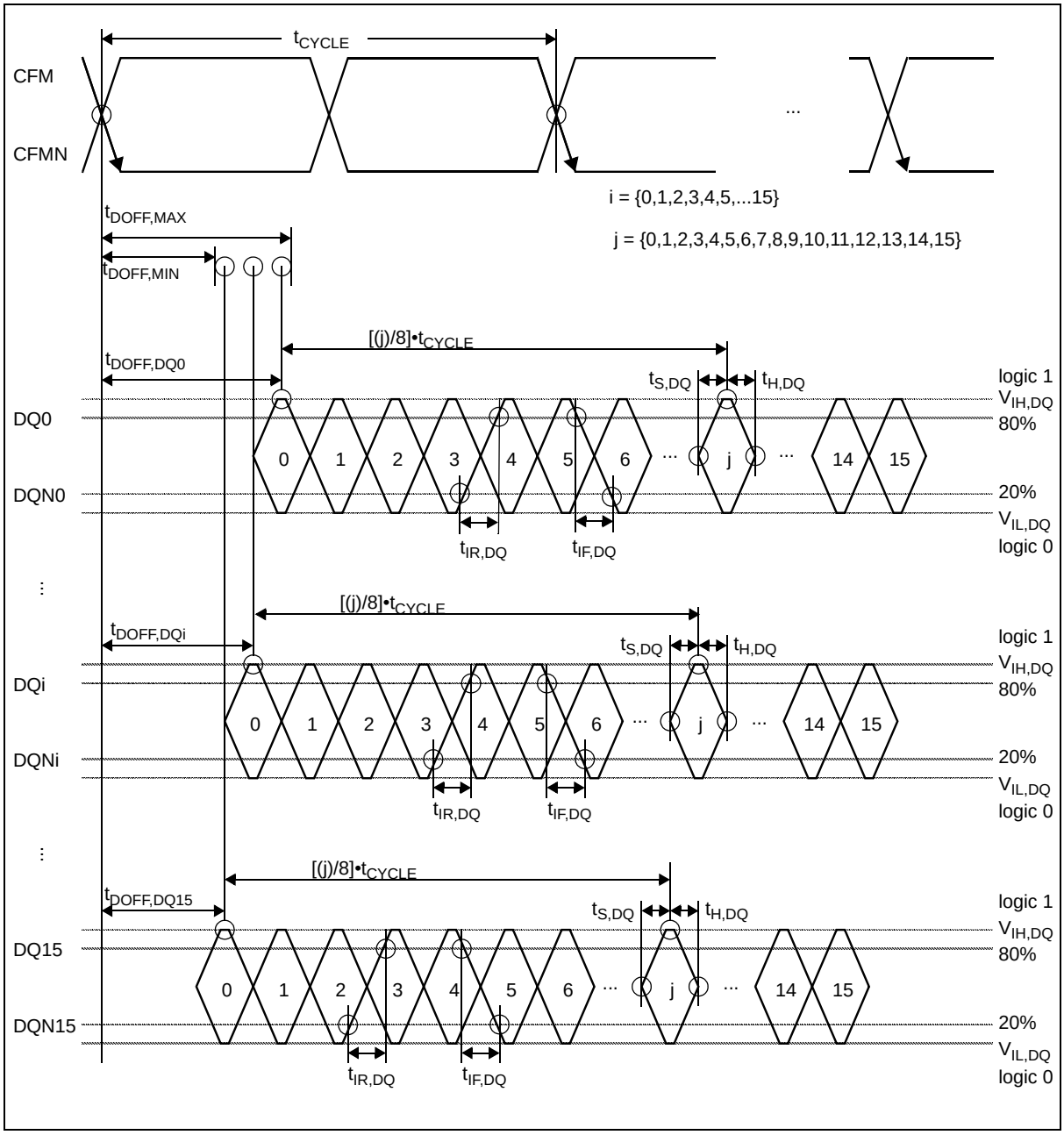
Figure 60 : DRSL DQ Receive Waveforms



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DRSL DQ Transmit Timing

Figure61 shows a timing diagram for transmitting read data on the DQ15...0/DQN15...0 data pins of the memory component. This diagram represents a magnified view of these pins and only a few clock cycles are shown (CFM and CFMN are the clock signals). Timing events are measured to and from the primary CFM/CFMN crossing point in which CFM makes its high-voltage-to-low-voltage transition. The DQ15...0/DQN15...0 signals are high-true: a low voltage represents a logical zero and a high voltage represents a logical one. They are also differential - timing events on the DQ15...0/DQN15...0 pins are measured to and from the point that each differential pair crosses.

Because timing intervals are measured in this fashion, it is necessary to constrain the slew rate of the signals. The rise ($t_{OR, DQ}$) and fall time ($t_{OF, DQ}$) of the signals are measured from the 20% and 80% points of the full-swing levels.

20% = $V_{OL, DQ} + 0.2*(V_{OH, DQ} - V_{OL, DQ})$

80% = $V_{OL, DQ} + 0.8*(V_{OH, DQ} - V_{OL, DQ})$

There are 16 data transmit windows defined for each DQ15...0/DQN15...0 pin pair. The transmitting windows for a particular DQi/DQNi pin pair is referenced to an offset parameter $t_{QOFF,DQi}$ (the index “i” may take on the values {0, 1, .., 15} and refers to each of the DQ15... 0/DQN15...0 pin pairs).

The $t_{QOFF,DQi} + t_{Q,DQ,MAX}$ expression determines the time between the primary CFM/CFMN crossing point and the offset point for the DQi/DQNi pin pair.

The offset values $t_{QOFF,DQi}$ for each of the 16 DQi/DQNi pin pairs can be different. However, each is constrained to lie inside the range {$t_{QOFF,MIN}$, $t_{QOFF,MAX}$}. Furthermore, each offset value $t_{QOFF,DQi}$ is static; its value will not change during system operation. Its value can be determined at initialization time.

The 16 transmit windwos (j = 0 ... 15} for the first pair DQ0/DQN0 are labeled “0” through “15”. Each window begins at the time ($t_{QOFF,DQ0} + t_{Q,DQ,MAX} +((j+0.5)/8)*t_{CYCLE}$) and ends at the time ($t_{QOFF,DQ0} + t_{Q,DQ,MIN} +((j+1.5)/8)*t_{CYCLE}$) measured after the primary CFM/CFMN crossing point.

Note that when no read data is to be transmitted on the DQ/DQN pins(and no other component is transmitting on the external DQ/DQN wires), then the voltage level on the DQ/DQN pins will follow the voltage reference value VTERM,DRSL on the VTERM pin. The logical value of each DQ/DQN pin pair in this no-drive state will be “1/1”; when read data is driven, each DQ/DQN pin pair will have either the logical value of “1/0” or “0/1”.

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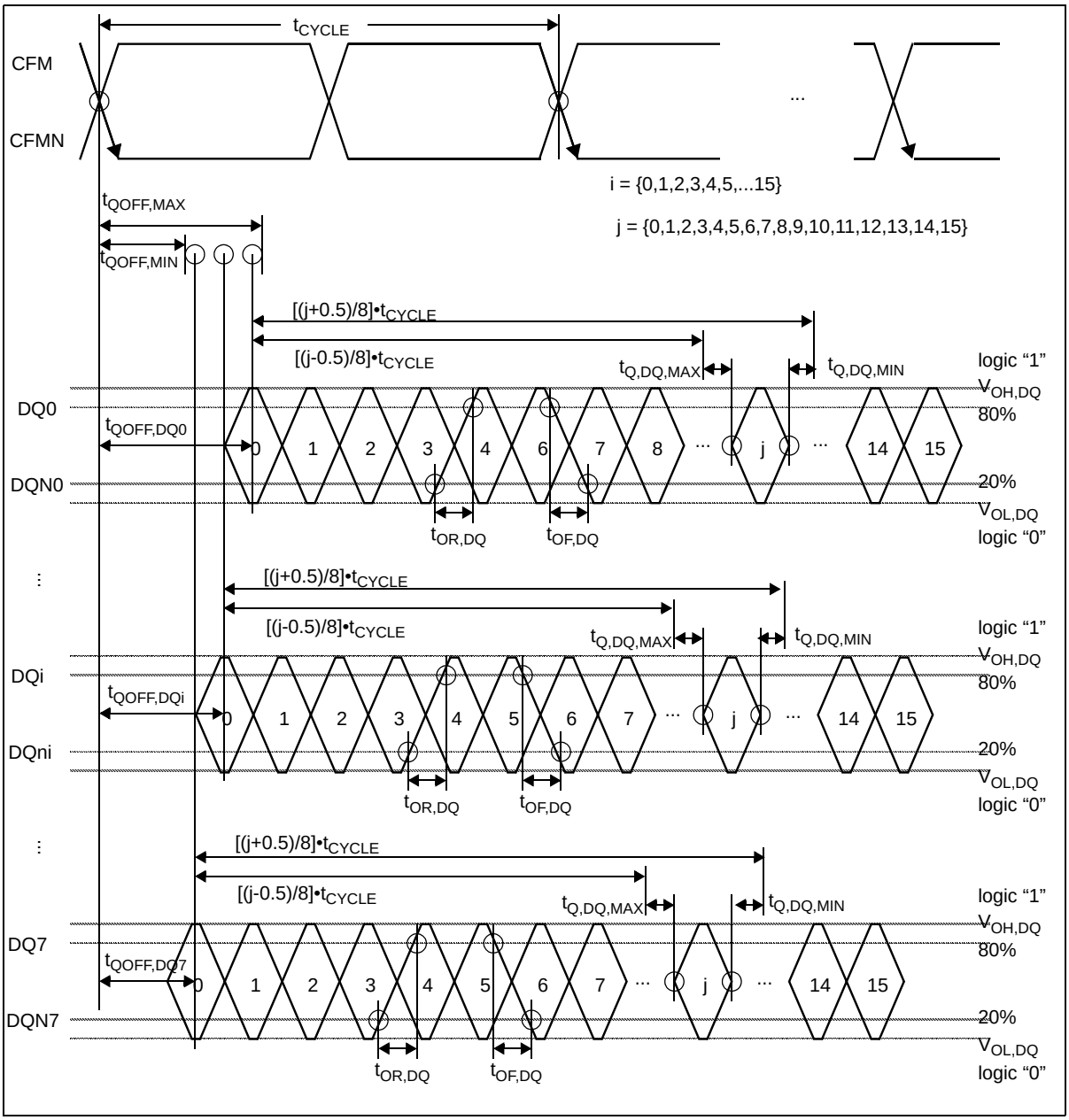
Figure 61 : RSL DQ Transmit Waveforms



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Serial Interface Receive Timing

Figure62 shows a timing diagram for the serial interface pins of the memory component. This diagram represents a magnified view of the pins only a few clock cycles.

The serial interface pins carry low-true signals: a high voltage represents a logical zero and a low voltage represents a logical one. Timing events are measured to and from the $V_{REF,RSL}$ level. Because timing intervals are measured in this fashion, it is necessary to constrain the slew rate of the signals. The rise time ($t_{R,SCK}$ and $t_{RI,SI}$) and fall time ($t_{F,SCK}$ and $t_{IF,SI}$) of the signals are measured from the 20% and 80% points of the full-swing levels.

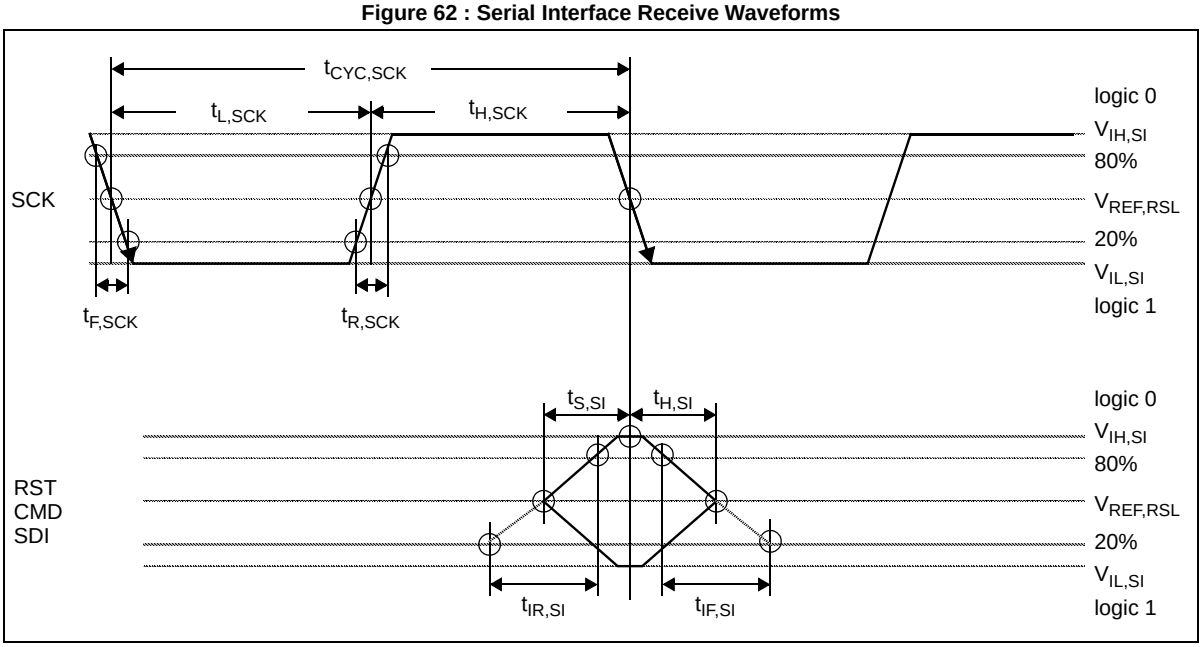
20% = $V_{IL,SI}$ + 0.2 *($V_{IH,SI}$ - $V_{IL,SI}$)

50% = $V_{IL,SI}$ + 0.5 *($V_{IH,SI}$ - $V_{IL,SI}$)

80% = $V_{IL,SI}$ + 0.8 *($V_{IH,SI}$ - $V_{IL,SI}$)

There is one receiving window defined for each serial interface signal (RST, CMD and SDI pins). This window has a set time ($t_{S,RQ}$) and a hold time ($t_{H,RQ}$) measured around the falling edge of the SCK clock signal.

Figure 62 : Serial Interface Receive Waveforms



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Serial Interface Transmit Timing

Figure63 shows a timing diagram for the serial interface pins of the memory component. This diagram represents a magnified view of the pins and only a few clock cycles are shown.

The serial interface pins carry low-true signals: a high voltage represents a logical zero and a low voltage represents a logical one. Timing events are measured to and from the $V_{REF,RSL}$ level. Because timing intervals are measured in this fashion, it is necessary to constrain the slew rate of the signals. The rise time ($t_{OR,SI}$) and fall time ($t_{OF,SI}$) of the signals are measured from the 20% and 80% points of the full-swing levels.

20% = $V_{OL,SI}$ + 0.2*($V_{OH,SI}$ - $V_{OL,SI}$)

50% = $V_{OL,SI}$ + 0.5*($V_{OH,SI}$ - $V_{OL,SI}$)

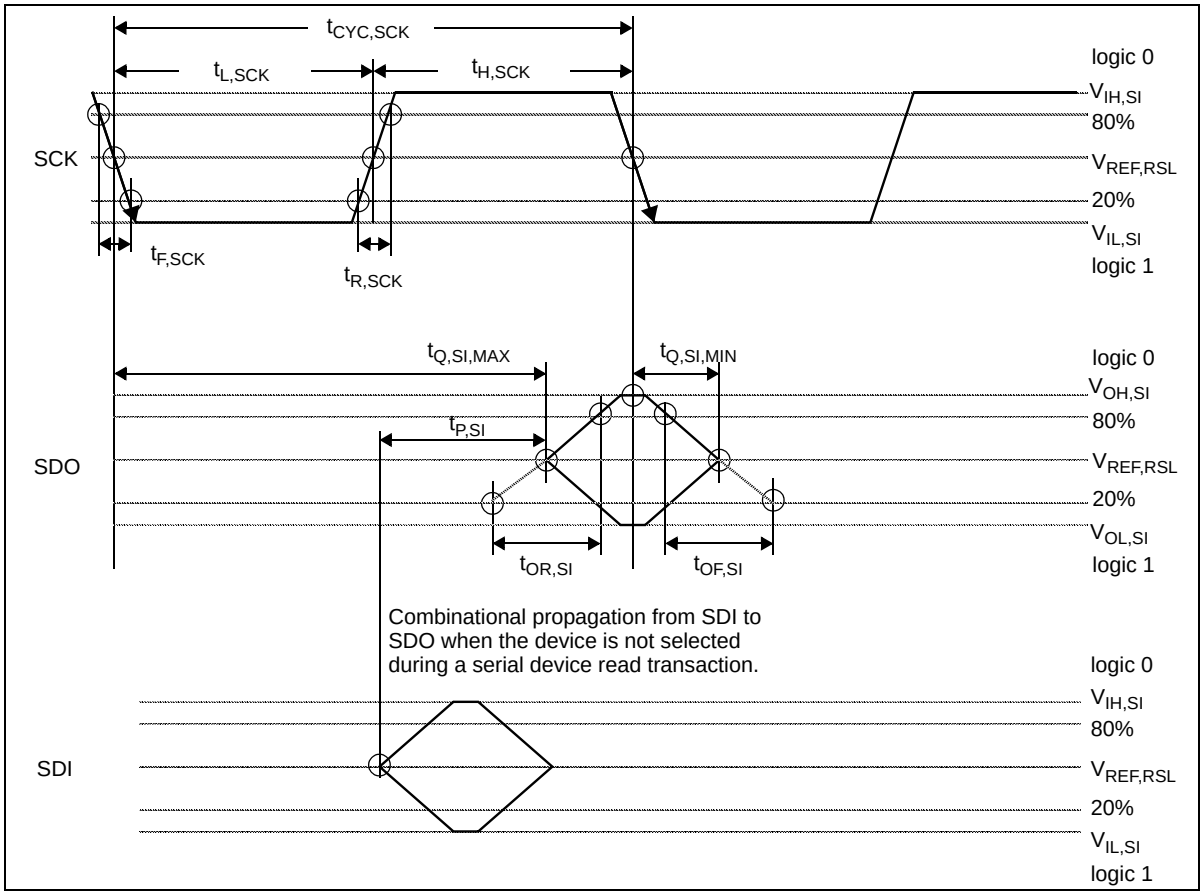
80% = $V_{OL,SI}$ + 0.8*($V_{OH,SI}$ - $V_{OL,SI}$)

There is one transmit window defined for the serial interface data signal (SDO pins). This window has a maximum delay time ($t_{Q,SI,MAX}$) from the falling edge of the SCK clock signal and a minimum delay time ($t_{Q,SI,MIN}$) from the next falling edge of the SCK clock signal.

When the memory component is not selected during a serial device read transaction, it will simply pass the information on the SDI input to the SDO output. This combinational propagation delay parameter is $t_{P,SI}$. The $t_{CYC,SCK}$ will need to be increased during a serial read transaction (relative to the $t_{CYC,SCK}$ value for a serial write transaction) because of the accumulated propagation delay through all of the XDR DRAM devices on the serial interface.

During Initialization, when the serial identification is determined, the SDI-to-SDO path is registered, so the $t_{CYC,SCK}$ value can be set to the same value as for serial write transactions. See “Initialization” on page42.

Figure 63 : Serial Interface Transmit Waveforms



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Package Description

Package Parasitic Summary

Table19 summarizes inductance, capacitance, and resistance values associated with each pin group for the memory component. Most of the parameters have maximum values only, however some have both maximum and minimum values.

The first group of parameters are for the CFM/CFMN clock pair pins. They include inductance, capacitance, and resistance values.

The second group of parameters are for the RQ request pins. They include inductance, mutual inductance, capacitance, and resistance values. There are also limits on the spread in inductance and capacitance values allowed in any one memory component.

The third group of parameters are specific to the DQ data pins and include inductance, mutual inductance, capacitance, and resistance values. There are limits on the spread in inductance and capacitance values allowed in any one memory component.

The fourth group of parameters are for the serial interface pins. They include inductance and capacitance values.

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Table 19 : Package RSL Parasitic Summary

Symbol	Parameter and Other Conditions		Minimum	Maximum	Units
L_{VTERM}	V_{TERM} pin - effective input inductance per four bits		-	2.2	nH
$L_{I,CFM}$	CFM/CFMN pins - effective input capaciance[b]	-2400 -3200 -4000	- - -	tbd 5.0 tbd	nH
$C_{I,CFM}$	CFM/CFMN pins - effective input capaciance[b]	-2400 -3200 -4000	- 1.8 -	tbd 2.4 tbd	pF
$R_{I,CFM}$	CFM/CFMN pins - effective input resistance		4	15	Ω
$L_{I,RQ}$	RSL RQ pins - effective input inductance[b]	-2400 -3200 -4000	- - -	tbd 5.0 tbd	nH
$C_{I,RQ}$	RSL RQ pins - effective input capacitance[b]	-2400 -3200 -4000	tbd 1.8 tbd	tbd 2.4 tbd	pF
$R_{I,RQ}$	RSL RQ pins - effective input resistance		4	15	Ω
$L_{12,RQ}$	Mutual inductance between adjacent RSL RQ signals		-	0.6	nH
$\Delta L_{I,RQ}$	Difference in $L_{I,RQ}$ between any RSL RQ pins of a single device		-	1.8	nH
$\Delta C_{I,RQ}$	Difference in C_I between CFM/CFMN average and RSL RQ pins of single device		-0.06	+0.06	pF
$Z_{PKG,DQ}$	DRSL DQ pins - package differential impednce note - package trace length should be less than 10mm long.	-2400 -3200 -4000	tbd 70 tbd	tbd 130 tbd	Ω
$C_{I,DQ}$	DRSL DQ pins - effective input capacitance[a]	-2400 -3200 -4000	- - -	tbd 2.0 tbd	pF
$\Delta C_{I,DQ}$	Difference in C_I between DQi and DQNi of each DRSL pair[a]	-2400 -3200 -4000	- - -	tbd 0.06 tbd	pF
$R_{I,DQ}$	DRSL DQ pins - effective input resistance		4	25	Ω
$L_{I,SI}$	Serial Interface effective input inductance		-	8.0	nH
$C_{I,SI}$	Serial Interface effective input capacitance RST, SCK, CMD SDI,SDO		 1.7 -	 3.0 7.0	 pF pF

a. This is the effective die input capacitance, and does not include package capacitance.

b. CFM/RQ/SI should include package capacitance/Impedance, only DQ deos not include pacage capacitance. This value is a combination of the device I/O circuitry and package capacitance&inductance

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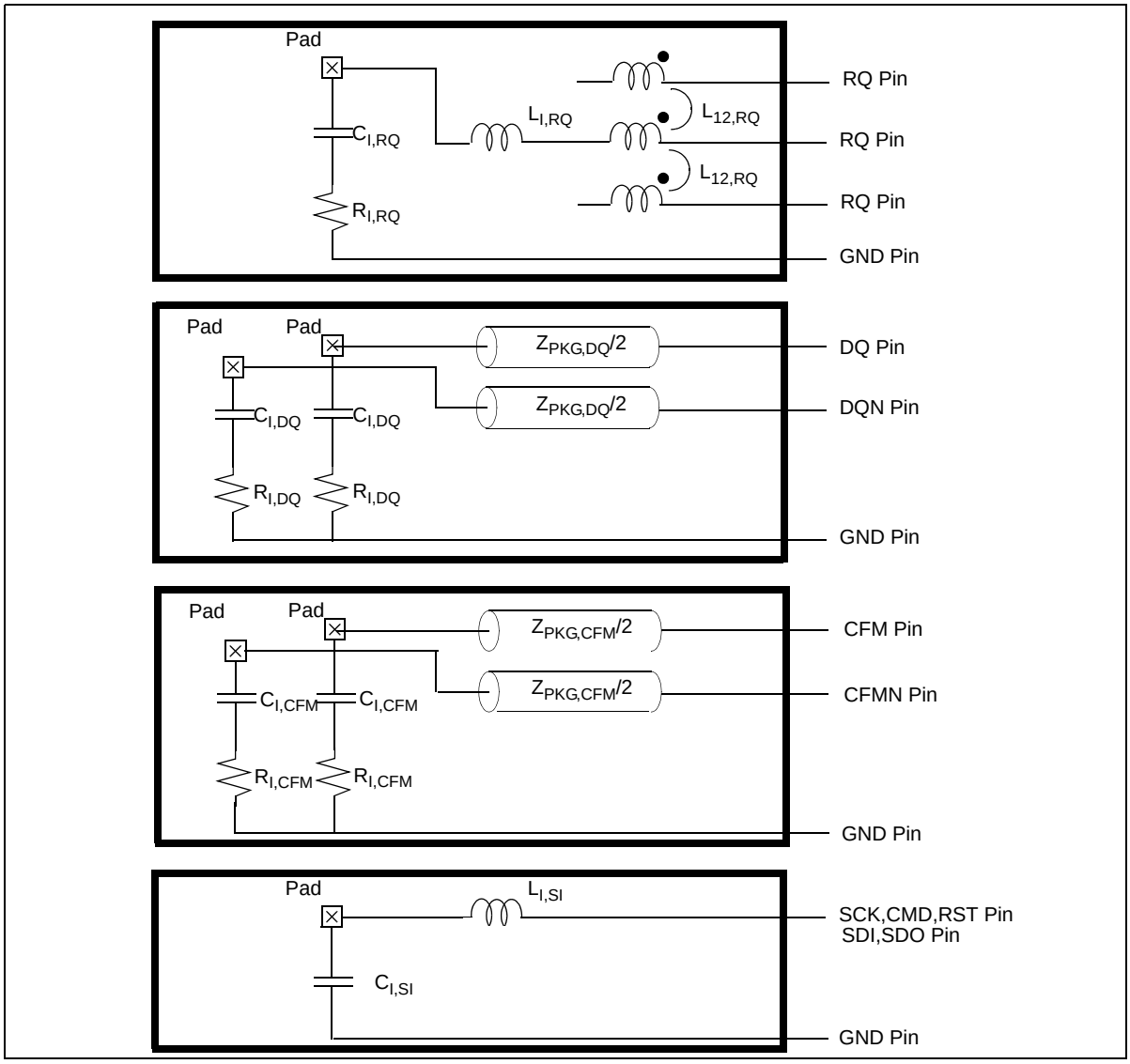
Figure 64 : Equivalent Circuits for Package Parasitic



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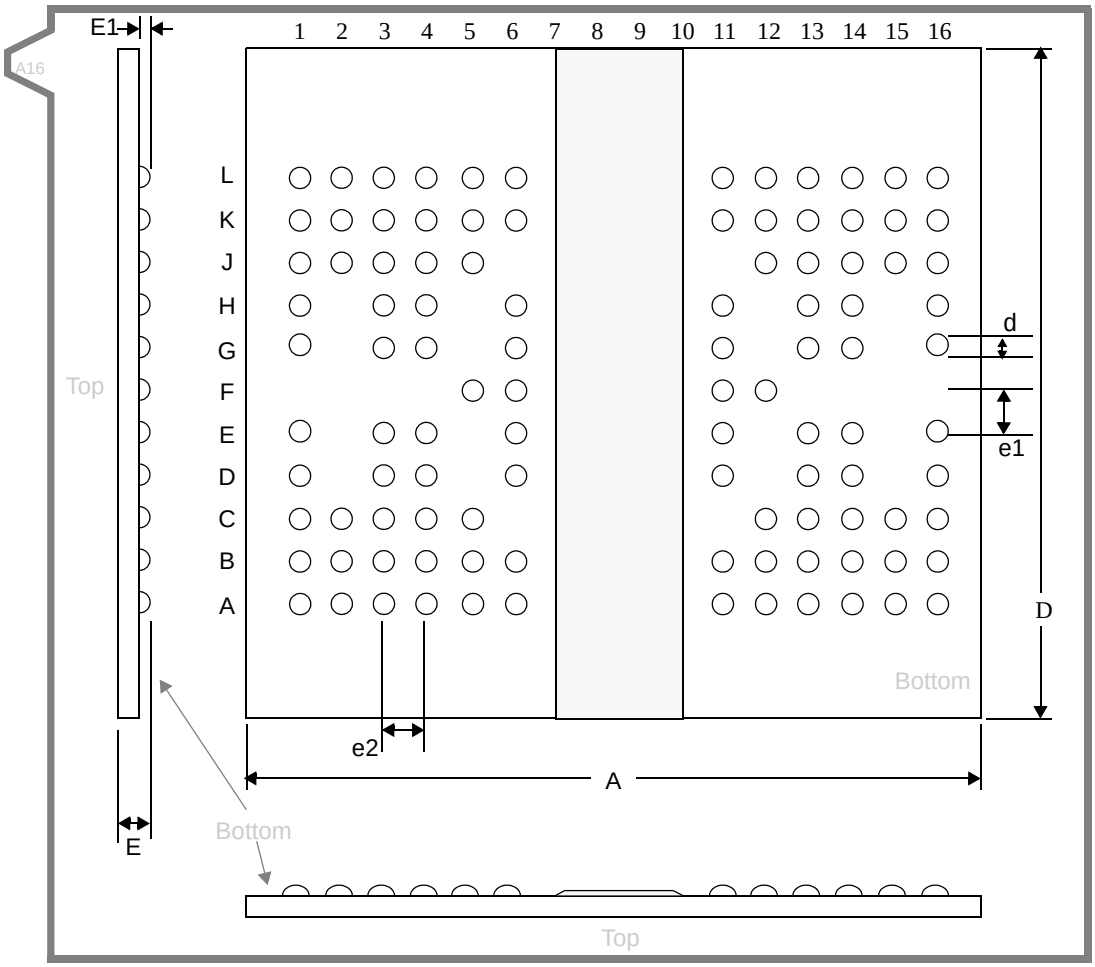
Package Mechanical Drawing

Figure65 illustrates the XDR DRAM device package and Table20 summarizes the mechanical parameters for that package.

Table 20 : XDR DRAM Package Mechanical Parameters

Symbol	Parameter	Min	Max	Unit	Symbol	Parameter	Min	Max	Unit
e1	Ball pitch (x-axis)	1.27	1.27	mm	E	Package total thickness	0.93	1.13	mm
e2	Ball pitch (y-axis)	0.80	0.80	mm	E1	Ball height	0.30	0.40	mm
A	Package body length	13.9	14.1	mm	d	Ball diameter	0.40	0.50	mm
D	Package body width	14.4	14.6	mm					

Figure 65 : XDR DRAM Package Mechanical Drawing (Bottom View)



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