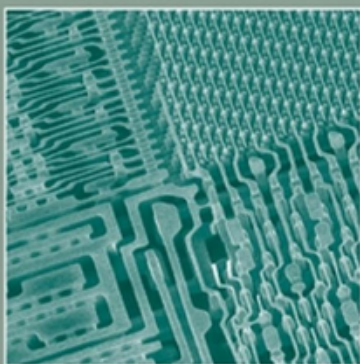
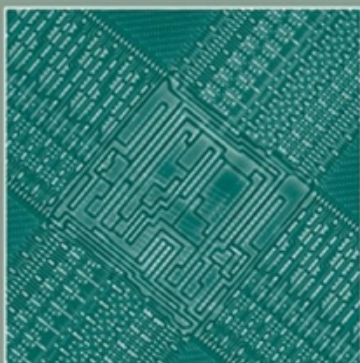
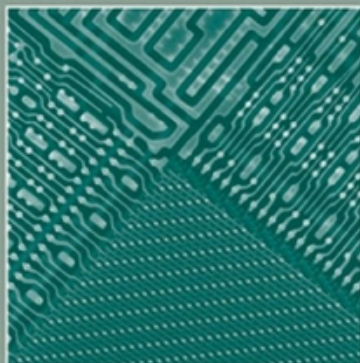


DRAM

CIRCUIT DESIGN

Fundamental and High-Speed Topics



Brent Keeth • R. Jacob Baker
Brian Johnson • Feng Lin

IEEE Press Series on Microelectronic Systems
Stuart K. Tewksbury and Joe E. Brewer, Series Editors

Netlist EX2032
Samsung v Netlist
IPR2023-00454

© 2023 IEEE

Copyright © 2008 by the Institute of Electrical and Electronic Engineers, Inc. All rights reserved.

Published by John Wiley & Sons, Inc., Hoboken, New Jersey.

Published simultaneously in Canada.

No part of this publication may be reproduced, stored in a retrieval system, or transmitted in any form or by any means, electronic, mechanical, photocopying, recording, scanning, or otherwise, except as permitted under Section 107 or 108 of the 1976 United States Copyright Act, without either the prior written permission of the Publisher, or authorization through payment of the appropriate per-copy fee to the Copyright Clearance Center, Inc., 222 Rosewood Drive, Danvers, MA 01923, (978) 750-8400, fax (978) 750-4470, or on the web at www.copyright.com. Requests to the Publisher for permission should be addressed to the Permissions Department, John Wiley & Sons, Inc., 111 River Street, Hoboken, NJ 07030, (201) 748-6011, fax (201) 748-6008, or online at <http://www.wiley.com/go/permission>.

Limit of Liability/Disclaimer of Warranty: While the publisher and author have used their best efforts in preparing this book, they make no representations or warranties with respect to the accuracy or completeness of the contents of this book and specifically disclaim any implied warranties of merchantability or fitness for a particular purpose. No warranty may be created or extended by sales representatives or written sales materials. The advice and strategies contained herein may not be suitable for your situation. You should consult with a professional where appropriate. Neither the publisher nor author shall be liable for any loss of profit or any other commercial damages, including but not limited to special, incidental, consequential, or other damages.

For general information on our other products and services or for technical support, please contact our Customer Care Department within the United States at (800) 762-2974, outside the United States at (317) 572-3993 or fax (317) 572-4002.

Wiley also publishes its books in a variety of electronic formats. Some content that appears in print may not be available in electronic format. For information about Wiley products, visit our web site at www.wiley.com.

Wiley Bicentennial Logo: Richard J. Pacifico

Library of Congress Cataloging-in-Publication Data is available.

ISBN 978-0-470-18475-2

Printed in the United States of America.

10 9 8 7 6 5 4 3 2 1

Netlist EX2032

Samsung v Netlist

IPR2023-00454

righted material

Contents

Preface	xi
----------------------	----

Chapter 1 An Introduction to DRAM

1.1 DRAM Types and Operation	1
1.1.1 The 1k DRAM (First Generation)	1
1.1.2 The 4k–64 Meg DRAM (Second Generation)	7
1.1.3 Synchronous DRAM (Third Generation)	15
1.2 DRAM Basics	22
1.2.1 Access and Sense Operations	24
1.2.2 Write Operation	28
1.2.3 Opening a Row (Summary)	29
1.2.4 Open/Folded DRAM Array Architectures	31

Chapter 2 The DRAM Array

2.1 The Mbit Cell	33
2.2 The Sense Amp	44
2.2.1 Equilibration and Bias Circuits	44
2.2.2 Isolation Devices	46
2.2.3 Input/Output Transistors	46
2.2.4 Nsense and Psense Amplifiers	47
2.2.5 Rate of Activation	49
2.2.6 Configurations	49
2.2.7 Operation	52
2.3 Row Decoder Elements	54
2.3.1 Bootstrap Wordline Driver	55
2.3.2 NOR Driver	57
2.3.3 CMOS Driver	58

2.3.4 Address Decode Tree	58
2.3.5 Static Tree	59
2.3.6 P&E Tree	59
2.3.7 Predecoding	60
2.3.8 Pass Transistor Tree	61
2.4 Discussion	61

Chapter 3 Array Architectures

3.1 Array Architectures	65
3.1.1 Open Digitline Array Architecture	65
3.1.2 Folded Array Architecture	75
3.2 Design Examples: Advanced Bilevel DRAM Architecture ...	83
3.2.1 Array Architecture Objectives	84
3.2.2 Bilevel Digitline Construction	85
3.2.3 Bilevel Digitline Array Architecture	88
3.2.4 Architectural Comparison	93

Chapter 4 The Peripheral Circuitry

4.1 Column Decoder Elements	99
4.2 Column and Row Redundancy	102
4.2.1 Row Redundancy	104
4.2.2 Column Redundancy	107

Chapter 5 Global Circuitry and Considerations

5.1 Data Path Elements	111
5.1.1 Data Input Buffer	111
5.1.2 Data Write Muxes	115
5.1.3 Write Driver Circuit	116
5.1.4 Data Read Path	118
5.1.5 DC Sense Amplifier (DCSA)	119
5.1.6 Helper Flip-Flop (HFF)	121
5.1.7 Data Read Muxes	122
5.1.8 Output Buffer Circuit	124
5.1.9 Test Modes	125
5.2 Address Path Elements	126
5.2.1 Row Address Path	126
5.2.2 Row Address Buffer	127
5.2.3 CBR Counter	127
5.2.4 Predecode Logic	128
5.2.5 Refresh Rate	128
5.2.6 Array Buffers	130
5.2.7 Phase Drivers	131

5.2.8 Column Address Path	131
5.2.9 Address Transition Detection	132
5.3 Synchronization in DRAMs	135
5.3.1 The Phase Detector	137
5.3.2 The Basic Delay Element	137
5.3.3 Control of the Shift Register	138
5.3.4 Phase Detector Operation	139
5.3.5 Experimental Results	140
5.3.6 Discussion	142

Chapter 6 Voltage Converters

6.1 Internal Voltage Regulators	147
6.1.1 Voltage Converters	147
6.1.2 Voltage References	148
6.1.3 Bandgap Reference	153
6.1.4 The Power Stage	154
6.2 Pumps and Generators	158
6.2.1 Pumps	158
6.2.2 DVC2 Generator	165
6.3 Discussion	165

Chapter 7 An Introduction to High-Speed DRAM

7.1 The Performance Paradigm	167
7.2 Performance for DRAM Memory Devices	169
7.3 Underlying Technology Improvements	171

Chapter 8 High-Speed Die Architectures

8.1 Introduction: Optimizing DRAM Architecture for High Performance	173
8.2 Architectural Features: Bandwidth, Latency, and Cycle Time	175
8.2.1 Architectural Limiters: The Array Data Path	176
8.2.2 Architectural Limiters: The Read Data Path	183
8.2.3 Architectural Limiters: Latency	186
8.3 Conclusion: Designing for High Performance	190

Chapter 9 Input Circuit Paths

9.1 Introduction	193
9.2 Input Receivers	196
9.3 Matched Routing	200
9.4 Capture Latches	203
9.5 Input Timing Adjustments	206
9.6 Current Mode Logic (CML)	212

Chapter 10 Output Circuit Paths

10.1 Transmission Line, Impedance, and Termination.....	220
10.2 Impedance Control	224
10.3 Simultaneous Switching Noise (SSN)	230
10.4 Signal Return Path Shift (SRPS).....	238
10.5 Electrostatic Discharge (ESD)	242
10.6 Parallel-to-Serial Conversion	244
10.7 Emerging Memory I/O Features.....	248

Chapter 11 Timing Circuits

11.1 Introduction.....	251
11.2 All-Digital Clock Synchronization Design.....	254
11.2.1 Timing Analysis	255
11.2.2 Digital Delay Line.....	259
11.2.3 Phase Detector (PD)	267
11.2.4 Test and Debug	273
11.2.5 Dual-Loop Architecture	274
11.3 Mixed-Mode Clock Synchronization Design	275
11.3.1 Analog Delay Line	276
11.3.2 Charge-Pump Phase Detector (CPPD)	283
11.3.3 Dual-Loop Analog DLL	286
11.3.4 Mixed-Mode DLL and Its Applications	289
11.4 What's Next for Timing	291

Chapter 12 Control Logic Design

12.1 Introduction.....	295
12.2 DRAM Logic Styles	298
12.2.1 Process Limitations	298
12.2.2 Array Operation.....	301
12.2.3 Performance Requirements	304
12.2.4 Delay-Chain Logic Style.....	306
12.2.5 Domino Logic	309
12.2.6 Testability	314
12.3 Command and Address Control	317
12.3.1 Command Decoder	318
12.3.2 Read and Write Data Address Registers	324
12.3.3 Column Access Control.....	328
12.4 Write Data Latency Timing and Data Demultiplexing.....	330
12.4.1 Write Latency Timing.....	332
12.4.2 Write Data Demultiplexing.....	338
12.5 Read Data Latency Timing and Data Multiplexing	346
12.5.1 Read Data FIFO.....	350

12.5.2 Read Latency (CL) Tracking	359
12.6 Comments on Future Direction for DRAM Logic Design ...	367
Chapter 13 Power Delivery	
13.1 Power Delivery Network Design	373
13.2 Device/Package Co-design	376
13.3 Full-Chip Simulations	380
Chapter 14 Future Work in High-Performance Memory	385
Appendix.	391
Glossary	407
Index	413

An Introduction to DRAM

Dynamic random access memory (DRAM) integrated circuits (ICs) have existed for more than thirty years. DRAMs evolved from the earliest kilobit (Kb) generation to the gigabit (Gb) generation through advances in both semiconductor process and circuit design technology. Tremendous advances in process technology have dramatically reduced feature size, permitting ever higher levels of integration. These increases in integration have been accompanied by major improvements in component yield to ensure that overall process solutions remain cost-effective and competitive. Technology improvements, however, are not limited to semiconductor processing. Many of the advances in process technology have been accompanied or enabled by advances in circuit design technology. In most cases, advances in one have enabled advances in the other. In this chapter, we introduce some fundamentals of the DRAM IC, assuming that the reader has a basic background in complementary metal-oxide semiconductor (CMOS) circuit design, layout, and simulation [1].

1.1 DRAM TYPES AND OPERATION

To gain insight into how modern DRAM chips are designed, it is useful to look into the evolution of DRAM. In this section, we offer an overview of DRAM types and modes of operation.

1.1.1 The 1k DRAM (First Generation)

We begin our discussion by looking at the 1,024-bit DRAM (1,024 x 1 bit). Functional diagrams and pin connections appear in Figure 1.1 and Figure 1.2, respectively. Note that there are 10 address inputs with pin labels R_1 – R_5 and C_1 – C_5 . Each address input is connected to an on-chip

address input buffer. The input buffers that drive the *row* (*R*) and *column* (*C*) decoders in the block diagram have two purposes: to provide a known *input capacitance* (C_{IN}) on the address input pins and to detect the input address signal at a known level so as to reduce timing errors. The level V_{TRIP} , an idealized trip point around which the input buffers slice the input signals, is important due to the finite transition times on the chip inputs (Figure 1.3). Ideally, to avoid distorting the duration of the logic zeros and ones, V_{TRIP} should be positioned at a known level relative to the maximum and minimum input signal amplitudes. In other words, the reference level should change with changes in temperature, process conditions, *input maximum amplitude* (V_{IH}), and *input minimum amplitude* (V_{IL}). Having said this, we note that the input buffers used in first-generation DRAMs were simply inverters.

Continuing our discussion of the block diagram shown in Figure 1.1, we see that five address inputs are connected through a decoder to the 1,024-bit memory array in both the row and column directions. The total number of addresses in each direction, resulting from decoding the 5-bit word, is 32. The single memory array is made up of 1,024 memory elements laid out in a square of 32 rows and 32 columns. Figure 1.4 illustrates the conceptual layout of this memory array. A memory element is located at the intersection of a row and a column.

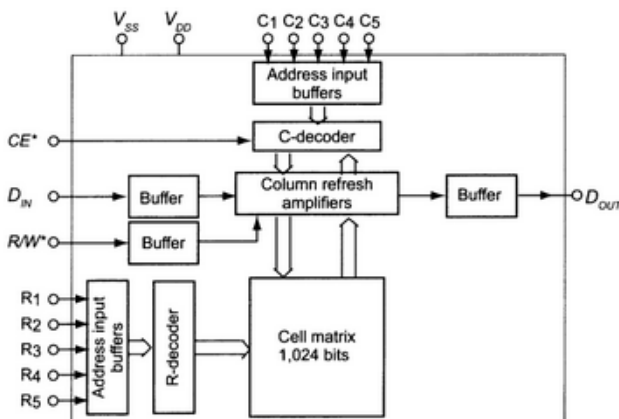


Figure 1.1 1,024-bit DRAM functional diagram.

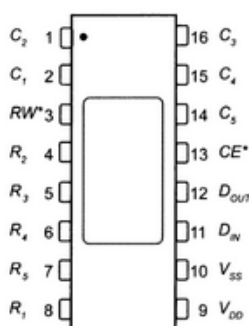


Figure 1.2 1,024-bit DRAM pin connections.

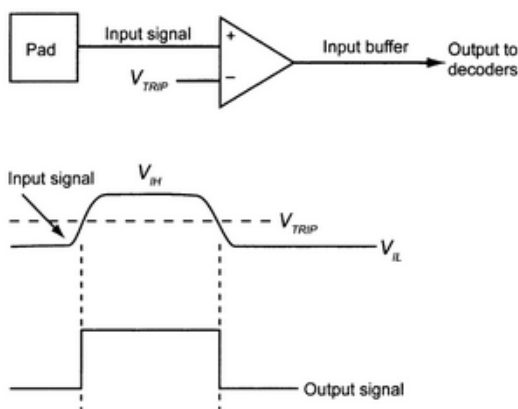


Figure 1.3 Ideal address input buffer.

By applying an address of all zeros to the 10 address input pins, the memory data located at the intersection of row0, $RA0$, and column 0, $CA0$, is accessed. (It is either written to or read out, depending on the state of the R/W^* input and assuming that the CE^* pin is LOW so that the chip is enabled.)

It is important to realize that a single bit of memory is accessed by using both a row and a column address. Modern DRAM chips reduce the number of external pins required for the memory address by using the same pins for both the row and column address inputs (*address multiplexing*). A clock signal *row address strobe* (RAS^*) strobes in a row address and then, on the same set of address pins, a clock signal *column address strobe* (CAS^*) strobes in a column address at a different time.