

1 UNITED STATES PATENT AND TRADEMARK OFFICE
2 BEFORE THE PATENT TRIAL AND APPEAL BOARD
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5 SAMSUNG ELECTRONICS CO., LTD.,
6 Petitioner
7 v.
8 NETLIST, INC.,
9 Patent Owner
10 -----

11
12 Case No. IPR2023-00454

13 Patent No. 11,093,417

14 - and -

15 Case No. IPR2023-00455

16 Patent No. 9,858,215
17

18 REMOTE DEPOSITION

19 DR. ANDREW WOLFE
20
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22
23

24 DATE TAKEN: NOVEMBER 5, 2023

REPORTED BY: RENEE HARRIS, CSR, CCR, RPR

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5 SAMSUNG ELECTRONICS CO., LTD.,
6 Petitioner

7 v.

8 NETLIST, INC.,
9 Patent Owner
10

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12 Case No. IPR2020-01624

13 Patent No. 6,975,132
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17 Remote Deposition of DR. ANDREW WOLFE, the
18 witness herein, at 9:02 Pacific Daylight Time, on
19 Saturday, November 5, 2023, appearing remotely
20 from Santa Clara, California before Renee Harris,
21 California Certified Shorthand Reporter No. 14168,
22 New Jersey Certified Court Reporter No.
23 30XI00241200, and Registered Professional
24 Reporter.
25

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PREVIOUSLY MARKED EXHIBITS REFERENCED

EXHIBIT NO.	DESCRIPTION
1001	U.S. Patent No. 9,858,215
1001	U.S. Patent No. 9,858,215
1001	U.S. Patent No. 11,093,417
1003	Declaration, Dr. Wolfe, '215
1003	Declaration, Dr. Wolfe, '417
1062	JEDEC JESD21-C design specification for DDR SDRAM RDIMM (January 2002)
1064	JEDEC JESD79-2 DDR2 standard (September 2003)
1071	U.S. Patent No. 7,363,422 (Perego)
1072	U.S. Patent No. 7,155,627 (Matsui)
1073	U.S. Patent No. 2006/0277355 (Ellsberry)
1074	U.S. Patent No. 7,024,518 (Halbert)

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SANTA CLARA, CALIFORNIA;
SATURDAY, NOVEMBER 5, 2023, 9:02 A.M.;

DR. ANDREW WOLFE,
called as a witness and having been first duly
sworn by the Certified Shorthand Reporter, was
examined and testified as follows:

EXAMINATION

BY MR. WARRICK:

Q. Good morning, Dr. Wolfe.

I believe you said you have access to the
exhibits. I'd like to start off with your
declaration in the IPR dealing with the '417
patent. It should be Exhibit 1003. Note the '417
patent in the title.

Do you see that?

A. I do.

Q. And if you could go to paragraph 126 in
there, please. It's on page 104.

A. Yes.

Q. And could you just read for us paragraph
126. It's short.

A. "In my opinion, a Skilled Artisan would
have understood that the term 'rank' refers to an

1 independent set of one or more memory devices on a
2 memory module that act together in response to
3 command signals, including chip select signals, to
4 read or write the full bit-width of the memory
5 module."

6 Q. Thank you.

7 And that is the construction that you've
8 endorsed for the term "rank" in the '417 patent;
9 correct?

10 A. Correct.

11 Q. And that's also the construction you've
12 endorsed for the '215 patent; correct?

13 A. Correct.

14 Q. I'd like to spend a little bit of time
15 with this. Starting with the words "act
16 together," could you explain to me what you mean
17 in your proposed construction by saying that the
18 memory devices must "act together"?

19 A. Well, you need to read it in context.
20 Since a rank can be one or more memory devices,
21 "act together" means that they are not responding
22 independently, separately to command signals.
23 Which, of course, if you only have one, is natural
24 and would always happen. And if you have more
25 than one, you would have to configure the memory

1 devices so that they respond together to command
2 signals.

3 Q. When you say "respond together," I guess
4 I'm not sure what that means beyond "act
5 together."

6 Does that -- does that mean they have to
7 respond at the same time? Does it mean something
8 more than that?

9 A. I think to a skilled artisan they would
10 interpret that in a reasonable manner. So it does
11 not have -- nothing -- no two things ever happen
12 at the exact same instant in time. That's the
13 world we live in. But they would respond in
14 approximately the same time. They would attempt
15 to respond in the same time. And they would
16 respond in a coordinated way.

17 I mean, the -- again, a person of
18 ordinary skill would use the rank to describe
19 something that's ordinarily and commonly done, not
20 to try to bizarrely limit the field through their
21 use of that word. It's a word that -- that was
22 not created as part of a standards effort or as
23 part of a definitional effort. It was a
24 descriptive word that grew among practitioners to
25 describe the ordinary way that they did things.

1 And when they connected one or more
2 memory devices in a way that those memory devices
3 would respond together to command signals, while
4 some other memory devices, one or more, in a
5 different rank, might respond separately to
6 command signals, the word "rank" was used to
7 distinguish one set of one or more memory devices
8 from another set of one or more memory devices.

9 Q. Dr. Wolfe, do you disagree that the term
10 "rank" arose out of the JEDEC standards and
11 related proceedings?

12 A. I believe I do, depending by what you
13 mean by "arose out of."

14 My recollection and my understanding is
15 that because at that time, there were two slightly
16 different memory organizations or structures that
17 were being referred to as "banks" during the late
18 '70s through the '90s, that some engineers at
19 certain companies started to distinguish those by
20 calling groups of memory cells on a chip a "bank"
21 and calling groups of memory cells that were
22 distinguishing between chips a "rank."

23 And when JEDEC began to update their
24 standards, some of that vocabulary migrated from
25 common usage into the JEDEC standard.

1 Q. So you agree that a "bank" and a "rank"
2 are different terms; they don't mean the same
3 thing?

4 MR. CHANDLER: Object to form.

5 THE WITNESS: It depends under what
6 context and what time. Certainly, what today
7 most people would call a "rank," when I
8 started developing computer systems, most
9 people called a "bank." And even today, some
10 of us who are older will often refer to the
11 structure that many people call a "rank"
12 today as a "bank" because historically the
13 term was used for that structure of one or
14 more memory devices on a memory module that
15 act together.

16 That term "rank" is -- and the term
17 "bank" can also in certain contexts used to
18 refer to sets of memory modules in certain
19 computing systems.

20 So you really have to look at the context
21 and the time frame.

22 BY MR. WARRICK:

23 Q. But you would agree that the term "bank"
24 does not imply a rank; right?

25 MR. CHANDLER: Objection. Form.

1 THE WITNESS: Again, it depends on the
2 context, and it depends on the time frame.

3 BY MR. WARRICK:

4 Q. Let me put it differently.

5 It sounds like from what you've said that
6 something that fits your understanding of a rank
7 may also qualify as a bank; right?

8 A. It depends on the context and a time
9 frame.

10 Q. But a set of memory devices that qualify
11 as a "bank" with a "b" are not necessarily a
12 "rank" with an "r"; correct?

13 MR. CHANDLER: Objection. Form.

14 THE WITNESS: It depends on the context
15 and a time frame.

16 BY MR. WARRICK:

17 Q. Is there a situation where the term
18 "bank" necessarily implies a rank, to your
19 knowledge?

20 A. I don't know what you mean by
21 "necessarily implies." But I certainly could read
22 descriptions of computer systems in the mid-'80s
23 or early '90s that used the term "bank" to refer
24 to what in certain JEDEC standards is today called
25 a "rank."

1 Q. I want to go back to something you said
2 earlier about your construction of rank.

3 You said that the memory devices would
4 respond in a coordinated way.

5 When you say a "coordinated way," does
6 that mean that there is some type of communication
7 between the memory devices on the memory module?

8 MR. CHANDLER: Objection. Form.

9 THE WITNESS: Not necessarily and not
10 commonly, no.

11 BY MR. WARRICK:

12 Q. So what does it mean, in your view, for
13 the memory devices to respond in a "coordinated
14 way"?

15 A. Each memory device might have a different
16 role. For example, one memory device might have
17 to output Bits 0 through 3 while another memory
18 device is outputting Bits 4 through 7.

19 So they are not doing exactly the same
20 thing, but they are working in coordination in
21 response to the same command signals, responding
22 at approximately the same time, in order to
23 provide Bits 0 through 7 together.

24 Q. So memory devices that are responding to
25 the same command signals and responding at

1 approximately the same time qualify as a rank in
2 your view?

3 A. No. I've given a complete definition.
4 And again, that's with respect to these patents,
5 the way the word "rank" is used in these patents,
6 in the context of these patents. And the
7 definition would be read by a person of ordinary
8 skill applying some common sense.

9 So one or more memory devices on a memory
10 module act together in response to command
11 signals, including chip select signals, to read or
12 write the full width of the memory module is
13 something that is ordinarily and commonly called a
14 "rank" in the industry at the time of these
15 patents.

16 Q. Well, you mentioned earlier that your
17 construction was specific to the context of these
18 patents that are at issue in these two IPRs.

19 How does that definition differ from what
20 you would called the ordinary understanding in the
21 art of the term "rank"?

22 A. It is an ordinary understanding in the
23 art of the term "rank." Like many words, "rank"
24 can mean different things in different contexts.
25 It doesn't always have to refer to memories. It

1 can refer to people. You know, it's a word that
2 can have different meanings.

3 And in the context of memory of modules,
4 this is the ordinary meaning.

5 Q. Your construction also includes the term
6 "independent set." Can you explain for me what
7 you mean by an "independent set" of memory
8 devices.

9 A. It's really just what I said before, is
10 that it would be common in a computer system that
11 you would have one or more memory devices that are
12 acting together and that also have one or more
13 memory devices that are acting separately.

14 So when I use the word "independent," I'm
15 identifying that a rank is the one or more memory
16 devices that work together, as distinct from
17 another rank, which would be the other one or more
18 memory devices that operate separately.

19 So those two ranks are operating
20 independently from each other in the sense that
21 they are not responding at the same time to the
22 same command signals.

23 Q. So in your view, does the -- does the
24 rank have anything to do with how the memory
25 devices are physically connected in the memory

1 system?

2 A. Well, in practice, the way that memory
3 devices respond to signals always has to do with
4 how they are physically connected.

5 Q. But assuming they are connected such that
6 they can respond to signals, say, from a
7 controller or a buffer and they can do so in what
8 you call a "coordinated way," that would qualify
9 as a rank under your construction, regardless of
10 how they are specifically connected; correct?

11 MR. CHANDLER: Objection. Form.

12 THE WITNESS: I don't know. You'd have
13 to show me an example. You know, typically,
14 if you move the connections around to a
15 memory system, it will respond differently.
16 So you would have to re-analyze it.

17 BY MR. WARRICK:

18 Q. But if they respond in approximately the
19 same time in response to the same command signals,
20 then those memory devices would be a rank, under
21 your view; correct?

22 MR. CHANDLER: Objection. Form.

23 THE WITNESS: Well, in this case, we are
24 talking about the meaning of the term "rank"
25 with respect to memory modules, so they would

1 have to be on a memory module.

2 BY MR. WARRICK:

3 Q. Okay. So assuming they are on the memory
4 module and they are responding at approximately
5 the same time to the same command signals, then
6 those memory devices would be a rank, under your
7 proposed construction in this case?

8 MR. CHANDLER: Object to form.

9 THE WITNESS: Not necessarily. You're
10 leaving out part of my construction. It
11 would have to be -- to respond together to
12 command signals, including chip select
13 signals, to read or write the full bit width
14 of the memory module.

15 BY MR. WARRICK:

16 Q. Okay. So maybe we can try this
17 differently.

18 If a set of memory devices are on the
19 memory module and they respond in approximately
20 the same time to the same command signals,
21 including chip select signals, to read or write
22 the full bit width of the memory module, then that
23 would fit your definition of a "rank," at least
24 for purposes of these patents; correct?

25 A. In an ordinary situation, it would be.

1 If you're trying to describe something that's
2 strange or unusual, I would have to see it to --
3 to know.

4 Again, these are -- these constructions
5 are intended to be understood by a reasonable
6 person who is familiar with the art.

7 Q. But, Dr. Wolfe, you do understand that in
8 proceedings like in inter partes review proceeding
9 before the Patent and Trademark Office, the claim
10 constructions, in part, are to assist the
11 administrative patent judges in understanding the
12 meaning of the patents; isn't that right?

13 MR. CHANDLER: Objection.

14 THE WITNESS: I do understand that, and
15 that is the intent here.

16 BY MR. WARRICK:

17 Q. And those administrative patent judges
18 are not always persons of ordinary skill in the
19 relevant art; correct?

20 A. That's correct. And they will be
21 assisted by experts in applying this construction
22 to the evidence. And -- but they are, I do
23 believe, reasonable people.

24 Q. Dr. Wolfe, taking a step back, you
25 understand -- strike that.

1 Can you state your full name so we have
2 it on the record, please.

3 A. Andrew Wolfe.

4 Q. And, Dr. Wolfe, you are testifying as an
5 expert on behalf of the petitioner in these two
6 IPRs; correct?

7 A. Yes. If we're talking about the same two
8 IPRs, yes.

9 Q. Well, to be specific, IPR2023-454
10 involving the '417 patent and IPR2023-455, which
11 involves the '215 patent.

12 A. Those are the IPRs that I'm here to
13 testify about today.

14 Q. And you're testifying on behalf of
15 Samsung Electronics Company; correct?

16 A. I believe that's the correct name of the
17 entity, yes.

18 Q. And you understand you are under oath
19 today?

20 A. I do.

21 Q. Any reason that you cannot give full,
22 accurate, and truthful testimony today?

23 A. No. I have been struggling with
24 bronchitis. If it flares up, I may need a break,
25 but it should not affect any of my answers.

1 Q. Well, if you need a break, let me know.
2 I just ask, as I suspect you're familiar, that if
3 there's a pending question that you answer it
4 first, and then we can take a break.

5 A. I will do my best.

6 Q. Let's take a look at the -- I'm sorry?

7 A. I didn't say anything.

8 Q. I'd like to look at the Perego patent.
9 It should be in your folder as Exhibit 1071.

10 A. Okay.

11 Q. Great.

12 And let's go to Figure 4B on page 9 of
13 Perego.

14 A. Okay.

15 Q. And first of all, you -- you recognize
16 this document, don't you, Dr. Wolfe?

17 A. I do.

18 Q. This is one of the patents that you are
19 alleging is a prior art that, in combination with
20 other art, renders obvious the claims of the '417
21 and '215 patents?

22 A. Yes.

23 Q. So looking at Figure 4B of Perego, is it
24 possible for you to tell me based solely on that
25 figure how many ranks there are?

1 MR. CHANDLER: Objection. Form.

2 THE WITNESS: I wouldn't even try to do
3 that. Why would I try to interpret a figure
4 in a patent without reading a description of
5 it? That wouldn't make any sense.

6 BY MR. WARRICK:

7 Q. Fair enough.

8 So just -- so -- just so we are on the
9 same page, you would have to read the accompanying
10 description to understand how many ranks are
11 depicted in Figure 4B of Perego; right?

12 A. I don't know if you would or if you
13 wouldn't, but in a proceeding like this, it would
14 be imprudent to attempt to interpret a document
15 without reading it in the context of the reference
16 as a whole.

17 Q. Now, you have read the entirety of the
18 Perego reference; correct?

19 A. Yes.

20 Q. Having read it, how many -- how many
21 ranks do you believe exist in Figure 4B of Perego?

22 A. I believe there's two; and I've indicated
23 that on page 155 of my declaration.

24 MR. CHANDLER: And for clarity, you know,
25 there are two IPRs. Be sure the question and

1 answers refer to the specific IPR that you're
2 referring to for an exhibit.

3 MR. WARRICK: Sure.

4 BY MR. WARRICK:

5 Q. Just so we're clear, when I'm asking
6 questions about references such as Perego, my
7 understanding is that your answers would be
8 equally applicable in either IPRs; is that fair,
9 Dr. Wolfe?

10 A. It depends on the question.

11 Q. So would you interpret Perego differently
12 depending on the patent that it's being asserted
13 against?

14 A. Not in terms of what it discloses; but in
15 terms of how it applies to claim language, I
16 might.

17 Q. Okay. You mentioned paragraph -- page
18 155 of your declaration.

19 Were you referring to your declaration in
20 the '417 patent IPR?

21 A. Yes.

22 Q. And on page 155 of that declaration,
23 you've added color-coding to Figure 4B; correct?

24 A. Correct.

25 Q. And that's not part of the original

1 reference; correct?

2 A. The color-coding is not.

3 Q. Now, in your color-coding, the memory
4 devices across the top of Figure 4B you've
5 characterized as one rank, and the ones on the
6 lower half of Figure 4B you've characterized as a
7 separate rank; correct?

8 A. Correct.

9 Q. And is that because they are on separate
10 channels?

11 MR. CHANDLER: Objection. Form.

12 THE WITNESS: I don't understand the
13 question. Is what because they are on
14 separate channels?

15 BY MR. WARRICK:

16 Q. Your characterization of Figure B as
17 showing two ranks.

18 MR. CHANDLER: Objection. Form.

19 THE WITNESS: It's because of the way
20 that they operate as described by Perego; and
21 more specifically, how a person of ordinary
22 skill would understand them to operate if, as
23 Perego suggests, DDR2 memory devices were
24 used in an embodiment.

25 ///

1 BY MR. WARRICK:

2 Q. But if we were to use Perego as depicted
3 in Figure 4B -- well, back up. Strike that.

4 The memory devices depicted in Figure 4B
5 are not SDRAM devices; correct?

6 MR. CHANDLER: Objection. Form.

7 THE WITNESS: I don't think I would
8 necessarily agree. Perego explains that his
9 teachings that he's explaining with respect
10 to the figures can be used with different
11 kinds of memory, and he specifically mentions
12 DDR2.

13 BY MR. WARRICK:

14 Q. But as depicted in Figure 4B with the
15 particular command signals shown, would that not
16 be more consistent with a Rambus-style memory
17 device?

18 A. Not if one were to re- -- interpret it as
19 a person of ordinary skill in the context of
20 Perego as a whole.

21 If one were to look at it quite
22 literally, there are certain symbols there that
23 are indicative of Rambus memory devices, but
24 there's a clear explanation in Perego that they
25 can be interpreted more broadly and that a person

1 of ordinary skill in the art would understand how
2 to substitute signals from, for example, a JEDEC
3 spec.

4 Q. But any modifications you would have to
5 make to accommodate a JEDEC spec memory device in
6 place of a Rambus-style memory device are not
7 depicted in Figure 4B; correct?

8 MR. CHANDLER: Objection. Form.

9 THE WITNESS: I think it depends on what
10 you mean by "depicted."

11 I mean, for example, my recollection is
12 that there are RQ signals, perhaps, and DQ
13 signals in a JEDEC standard.

14 But in any case, it doesn't matter,
15 because the figures are directed towards a
16 person of ordinary skill who is given the
17 guidance that the memory type can be
18 substituted.

19 BY MR. WARRICK:

20 Q. There's no chip select signal, for
21 example, shown in Figure 4B of Perego?

22 MR. CHANDLER: Objection. Form.

23 THE WITNESS: I think there is a chip
24 select signal. There's not a separate chip
25 select wire. But a person familiar with the

1 Rambus spec would understand that there is a
2 chip select signal.

3 BY MR. WARRICK:

4 Q. There's no chip select signal disclosed
5 in the Perego reference; correct?

6 MR. CHANDLER: Object to form.

7 THE WITNESS: I disagree. There's no --
8 first place, as I said, the Perego reference
9 refers to the Rambus embodiments; person of
10 ordinary skill in the art would understand
11 where chip select signals are present in a
12 Rambus embodiment, in some of the packetized
13 signals that travel over the illustrated
14 lines.

15 And Perego also explains to the reader
16 that alternative signaling protocols can be
17 used, including DDR, which a person of
18 ordinary skill in the art would understand
19 has chip select signals; or if they did not
20 understand that for some reason, would go to
21 the standard and would see that there are
22 chip select signals.

23 BY MR. WARRICK:

24 Q. When you're talking about the standard,
25 are you referring to JESD79-2?

1 A. Yes. As of September 2003.

2 Q. And that's the standard for DDR2 memory
3 devices; correct?

4 A. It is the standard for at least certain
5 DDR2 memory devices.

6 Q. It's not the standard for a JEDEC-style
7 memory bus; correct?

8 MR. CHANDLER: Objection. Form.

9 THE WITNESS: I'm not sure what you're
10 trying to say, but I -- it is the standard
11 for a JEDEC-style memory component, which
12 could connect to a DDR2 memory bus.

13 BY MR. WARRICK:

14 Q. But it's not the standard for a DDR2
15 memory bus; correct?

16 MR. CHANDLER: Objection. Form.

17 THE WITNESS: I don't know what you mean
18 by a "DDR2 memory bus." I'm not familiar
19 with that being a defined term of art. But
20 certainly a reasonable person could use that
21 descriptively to refer to the pins of DDR2
22 memory devices.

23 BY MR. WARRICK:

24 Q. Looking back at Figure 4B of Perego, am I
25 correct that there are two clock signals shown?

1 A. There are more than two clock signals
2 shown.

3 Q. Am I correct there are two types of clock
4 signals shown in Figure 4B, CFM and CTM?

5 A. Depends on how -- depends on how you're
6 using the term.

7 In a Rambus protocol, those are clock
8 lines, and they could have a variety of different
9 kinds of signals on them.

10 Q. Figure 4B has -- depicts two channels;
11 correct?

12 MR. CHANDLER: Objection to form.

13 THE WITNESS: Now, I believe that -- let
14 me see what it says in the patent. I don't
15 think that's right.

16 BY MR. WARRICK:

17 Q. How many channels are depicted in Figure
18 4B of Perego?

19 A. Figure 4B is described as a quad-channel
20 module. So four.

21 Q. And in each of the four channels in
22 Figure 4B, there's a CFM line and a CTM line;
23 correct?

24 A. In a Rambus embodiment, that would be
25 true.

1 Q. And those lines carry two clock signals;
2 correct?

3 MR. CHANDLER: Objection. Form.

4 THE WITNESS: Again it depends what your
5 context is in talking about signals. But at
6 any one time, they would carry two clock
7 signals. A CFM line would carry a clock
8 signal, and a CTM line could carry a clock
9 signal, in a Rambus embodiment, at any one
10 time.

11 BY MR. WARRICK:

12 Q. Are you aware of any other types of
13 signals that would be carried on a CFM or CTM line
14 on a memory module?

15 A. I don't recall the entirety of the Rambus
16 protocol off the top of my head. I believe it's
17 hundreds of pages.

18 So I don't know the answer without
19 referring to the documentation.

20 Q. But as you sit here, you're not aware of
21 any other types of signals that would be conveyed
22 on CFM or CTM lines; correct?

23 A. I don't know one way or the other without
24 looking at the documentation.

25 Q. Do DDR2 memory devices require CFM and

1 CTM signals?

2 MR. CHANDLER: Object to form.

3 THE WITNESS: Not under those names, but
4 they do require clocking signals in two
5 different directions. That's why a person of
6 ordinary skill would rely on their knowledge
7 of JEDEC Standard 79-2 in order to build a
8 DDR embodiment.

9 BY MR. WARRICK:

10 Q. So a DDR2 SDRAM memory device requires
11 two clock signals, in your view?

12 MR. CHANDLER: Objection to form.

13 THE WITNESS: Again, it depends on how
14 one defines "clock signal." But there are a
15 clock and a clock bar signal provided to the
16 DDR2 memory devices. In addition, there are
17 clocking signals that are referred to as
18 "strokes," that are used to clock data in and
19 out of the chip; and there are a number of
20 those.

21 BY MR. WARRICK:

22 Q. Perego describes an ability to access the
23 various memory devices independently; isn't that
24 right?

25 A. Are you referring to a specific statement

1 in Perego? I don't remember the entirety of the
2 text.

3 Q. Well, in general, Perego describes, for
4 example, a point-to-point topology; correct?

5 A. Perego describes a point-to-point
6 topology for Rambus embodiments. He doesn't limit
7 his invention in any way to a point-to-point
8 topology. And, in fact, by explaining that his
9 invention can be built with DDR2, he specifically
10 informs a reader that a point-to-point topology is
11 not necessary.

12 Q. But variable bit widths are central to
13 the types of memory modules described in Perego;
14 correct?

15 MR. CHANDLER: Objection. Form.

16 THE WITNESS: I wouldn't say that. I
17 would say that configureable bit widths are a
18 feature of his invention but not a required
19 feature of his disclosure.

20 BY MR. WARRICK:

21 Q. Let me ask this: To the extent that, in
22 your view, there are two ranks depicted in Figure
23 4B of Perego, is the bit width of those ranks
24 fixed?

25 MR. CHANDLER: Object to form.

1 THE WITNESS: It can be. Perego gets
2 configured to a specific bit width, and an
3 embodiment of Perego could have one or more
4 bit widths. A person of ordinary skill would
5 understand it to be that broad. A person of
6 ordinary skill would not look at Figure 4B
7 and read the description with respect to
8 Figure 4B and say, "I can only build that
9 kind of a DIMM if it has multiple bit widths
10 available."

11 BY MR. WARRICK:

12 Q. Each memory device in Figure 4B has a
13 fixed bit width, though; correct?

14 A. Again, it would depend on the
15 embodiments. But in the common embodiments, yes,
16 each memory device in Figure 4B would have a fixed
17 bit width.

18 Q. And so when you say that Perego could
19 configure ranks with different bit widths, it
20 would do that by including different numbers of
21 the memory devices from the module?

22 A. I don't think that's what I said.

23 Q. Then how would Perego configure
24 different -- strike that.

25 How would Perego configure ranks with

1 different bit widths?

2 A. There's an example shown in Figure 5C of
3 how a set of multiplexers can be used to change
4 the bit width configuration of the module. But,
5 again, it's a feature; it's not necessary to the
6 operation of the module.

7 Q. In your view, though, a rank will always
8 have a bit width; correct?

9 A. Again, I -- you know, I -- it's not
10 critical to the definition, but normally a rank
11 would have a bit width.

12 Q. And that bit width is tied to the number
13 and size of memory devices within the rank;
14 correct?

15 A. No. No. More than that, because you can
16 have two different memories of the same size, and
17 you can have the same number of memories, each of
18 which is the same size, but those memories have
19 different bit widths; that -- anybody who looks at
20 a JEDEC standard would understand that, that
21 memories of the same size are often available on
22 the market at a variety of bit widths.

23 Q. Under -- understood. Let me ask a better
24 question.

25 The bit width of a rank is tied to the

1 number and bit widths of the memory devices within
2 the rank; correct?

3 A. In general. Again, people use these
4 words with common sense. If occasionally you were
5 to only access a portion of a rank, and that was a
6 capability that you had, a person of ordinary
7 skill in the art would not stop calling that a
8 rank.

9 Q. And you've said earlier that Perego
10 allows you to configure the ranks; correct?

11 MR. CHANDLER: Object to form.

12 THE WITNESS: That is a feature of some
13 of his embodiments.

14 BY MR. WARRICK:

15 Q. And so for example, in Perego, you can
16 choose how many of the memory devices will
17 participate in a given rank; yes?

18 MR. CHANDLER: Object to form.

19 THE WITNESS: It's the interface that it
20 is configurable with. I don't think I've
21 considered whether or not the ranks can be
22 configured, because, again, it's irrelevant,
23 because Perego doesn't require you to have
24 variable-size ranks. It certainly discloses
25 fixed-size ranks.

1 I, right now, am not seeing rank
2 reconfiguration. It was the interface that
3 can be reconfigured.

4 BY MR. WARRICK:

5 Q. Well, let me ask this, then: Does Figure
6 4B necessarily depict two and only two ranks?

7 MR. CHANDLER: Object to form.

8 THE WITNESS: As described in the text,
9 it does. For -- for one embodiment described
10 in the text, it literally has two ranks.
11 Whether someone could use the same figure
12 with different text to describe something
13 else, I haven't considered that.

14 BY MR. WARRICK:

15 Q. But in your -- under your proposed
16 construction, there's nothing about the location
17 of the individual memory devices on the module
18 that determines which rank they can be a part of;
19 correct?

20 MR. CHANDLER: Object to form.

21 THE WITNESS: If by "location" you mean
22 their physical placement without respect to
23 their connectivity, I think that's correct.

24 It's the connectivity and operation of
25 memory devices that would lead a person of

1 ordinary skill to determine what rank they
2 are were in -- they are in.

3 BY MR. WARRICK:

4 Q. Now, if we look at Figure 4A, which is on
5 the same page of the Perego reference, Exhibit
6 1071.

7 Do you see that?

8 A. I do.

9 Q. And you've also referenced that in your
10 declaration for the '417 patent, on page 154 of
11 your declaration; correct?

12 A. Correct.

13 Q. And in your declaration, you've also
14 color-coded Figure 4A with colors that aren't from
15 the original reference; right?

16 A. Correct.

17 Q. And am I correct that through your
18 color-coding and related text, it's your view that
19 Figure 4A depicts two ranks?

20 A. In --

21 MR. CHANDLER: Objection --

22 THE WITNESS: -- a two-channel
23 embodiment, the Figure 4A, that would be
24 correct.

25 ///

1 BY MR. WARRICK:

2 Q. Now, as between Figures 4A and 4B of
3 Perego, both include channels 415a and 415b;
4 correct?

5 A. They both include channels that are
6 called 415a and 415b. But in the context of the
7 text, I'm not sure we should assume that they are
8 identical across the embodiments.

9 Q. So in your view, in Figure 4B, channels
10 415a and 415b are both part of the same rank,
11 unlike Figure 4A; is that right?

12 A. It's not really a question of in my view.
13 It's a question of what Perego says.

14 Perego says that in 4A you can have an
15 embodiment where both channels are in the same
16 rank or where the channels are in two different
17 ranks. Actually, it says you can either have one
18 channel or two channels there, as well.

19 In 4B, it tells us that there are two
20 ranks and with four channels, that -- that the
21 channels are being paired in that particular
22 situation.

23 Q. Can you point me to -- to where
24 specifically Perego draws that distinction?

25 A. I'm not sure what you mean by "that

1 distinction."

2 Q. The distinction between the alleged ranks
3 in Figure 4B versus 4A in the context of channels
4 415a and 415b.

5 A. Again, one has to read Perego in its
6 whole context, where it does tell us we can have
7 DDR2 embodiments.

8 Q. Well, you indicated earlier that Perego
9 tells us that Figure 4B includes four channels and
10 two ranks; yes?

11 A. Yes. That's primarily described in an
12 embodiment that's described in Column 10, lines 32
13 through 47.

14 Q. So Column 10, starting at line 32 of
15 Perego, talks about "alternate embodiments";
16 correct?

17 A. Yes.

18 Q. And specifically, it says, [as read]:

19 "...channels 415a and b may operate
20 simultaneously with channels 415c and
21 415d..."?

22 A. Yes.

23 Q. And what does that mean, in your view,
24 that they operate simultaneously?

25 A. I read it to mean that channels a and b

1 are operating together; and that channels c and d
2 are operating together; that each is operating as
3 a rank.

4 Q. But it's an alternate embodiment, so they
5 could also operate independently, in your view?

6 MR. CHANDLER: Object to form.

7 THE WITNESS: Perhaps the -- this patent
8 can disclose multiple embodiments.
9 There's -- there's nothing in my opinion that
10 says that every embodiment of Perego
11 discloses the claims, only that there are
12 disclosed embodiments that disclose the
13 claims.

14 BY MR. WARRICK:

15 Q. But Perego discloses the flexibility
16 that, for example, the modules shown in Figure 4B
17 could include more than two ranks; yes?

18 A. A person of ordinary skill could make
19 lots of modifications to Perego based on its
20 teachings, but that doesn't impact my opinion.

21 Q. Could, for example, the four memory
22 devices -- devices closest to the buffer in 4B be
23 configured as a single rank?

24 MR. CHANDLER: Objection to form.

25 THE WITNESS: I'm not sure which ones

1 you're talking about.

2 BY MR. WARRICK:

3 Q. So in Figure 4B, you see a buffer in the
4 center; correct?

5 A. Yes.

6 Q. And we see rows of memory devices on the
7 top half of Figure 4B and rows of memory devices
8 on the lower half; yes?

9 A. Yes.

10 Q. So my question is: Could you configure a
11 rank to include the two memory devices immediately
12 to the left of the buffer as well as the two
13 memory devices to the immediate right of the
14 buffer?

15 MR. CHANDLER: Object to form.

16 THE WITNESS: I suppose a person of
17 ordinary skill in the art would know how to
18 make the appropriate modifications to do
19 that, but I don't see that taught anywhere in
20 Perego.

21 BY MR. WARRICK:

22 Q. But it could be done using the -- the
23 system disclosed in Perego is what you're saying?

24 MR. CHANDLER: Object to form.

25 THE WITNESS: Using a modification of the

1 system -- of what's taught in Perego, I think
2 it could be done.

3 Memory systems are very, very flexible.
4 There's a lot of things that could be done
5 that are within the skill of a person of
6 ordinary skill in the art.

7 BY MR. WARRICK:

8 Q. Going back to Perego's description in
9 Column 10, starting at line 32, where it says,
10 "...channels 415a and 415b may operate
11 simultaneously with channels 415c and 415d,"
12 does "simultaneously" mean in response to the
13 same memory request?

14 A. I don't believe that's what's indicated
15 here.

16 Q. So you think it's talking about
17 "simultaneously" in response to different memory
18 requests?

19 MR. CHANDLER: Object to form.

20 THE WITNESS: I believe that what that's
21 saying is that a and b would operate
22 simultaneously and that c and d would operate
23 simultaneously.

24 BY MR. WARRICK:

25 Q. Well, assuming that's correct, does that

1 mean that Channels 415a and 415b would operate
2 simultaneously in response to the same memory
3 command?

4 A. The same host command, yes.

5 Q. When you say a "host command," do you
6 mean the command originating from the buffer?

7 MR. CHANDLER: Objection.

8 THE WITNESS: In a DDR2 embodiment, that
9 would be true, yes.

10 BY MR. WARRICK:

11 Q. Well, going back to that, we discussed
12 earlier that in Figure 4B, each channel includes
13 two clock lines, CFM and CTM; right?

14 A. In a Rambus embodiment, that would be the
15 case.

16 Q. Well, in -- in Figure 4B, as it is shown
17 in Perego, that's what's depicted; correct?

18 MR. CHANDLER: Objection. Form.

19 THE WITNESS: Again, that's what's
20 literally depicted, but a person of ordinary
21 skill reading the patent would understand
22 that those are exemplary signals, not
23 limiting.

24 BY MR. WARRICK:

25 Q. Well, just so I understand, what you're

1 saying is that a person of ordinary skill, in your
2 view, would be able to modify the embodiments of
3 Perego, including the embodiment depicted in 4B.

4 Am I understanding you correctly?

5 A. No, not really.

6 What I'm saying is that Perego
7 specifically says that various kinds of memory can
8 be used in his embodiments, including DDR2; and
9 that a person of ordinary skill would understand
10 that when Perego, in that context, illustrates a
11 set of input sig- -- and output signals to a
12 memory device, that that's exemplary and that they
13 are expected to understand that that would be
14 substituted, under Perego's teachings, for the
15 appropriate memory signals for the device that
16 you're using in the embodiment.

17 Q. And Figure 4B, to use your word, is
18 exemplary; correct?

19 A. It is -- yes, it is exemplary.

20 Q. And in the example of Figure 4B, each
21 channel includes two clock signal lines, CFM and
22 CTM; correct?

23 A. That is literally what's depicted.

24 But as I explained, a person of ordinary
25 skill would understand that any set of appropriate

1 memory control signals can be used there.

2 Q. Now, a DDR2 memory device would not be
3 used with two clock signal lines, CFM and CTM,
4 would it?

5 MR. CHANDLER: Objection to form.

6 THE WITNESS: Not with two clock signal
7 name -- lines that have those names. It
8 instead would use the clock signal lines that
9 are appropriate to DDR2, as explained in
10 Exhibit 1064.

11 BY MR. WARRICK:

12 Q. And Exhibit 1064 is the DDR2
13 specification; correct?

14 A. Correct.

15 Q. But the example depicted in Figure 4B of
16 Perego is showing a Rambus-style memory
17 architecture if you interpret it literally;
18 correct?

19 MR. CHANDLER: Objection. Form.

20 THE WITNESS: If you interpret it
21 literally, it is illustrating the Rambus
22 signal names.

23 But as I said, Perego is very clear in
24 expressing to a person of ordinary skill that
25 other kinds of memory modules or memory

1 devices can be used as well.

2 BY MR. WARRICK:

3 Q. Now, you can't just swap out each of the
4 Rambus-style memory devices in Figure 4B for DDR2
5 memory devices and have a working memory module,
6 can you?

7 MR. CHANDLER: Object to form.

8 THE WITNESS: It depends what you mean by
9 "just swap out." You can't just physically
10 remove one and replace it with the other.

11 But as a person of ordinary skill, it
12 would not require any invention to replace
13 one with the other. I would simply follow
14 the specifications.

15 BY MR. WARRICK:

16 Q. And when you say "the specifications,"
17 what specifications are you referring to?

18 A. Generally, Exhibit 1064. But in
19 practice, I would also obtain the specifications
20 for the particular brand of memory devices that I
21 was using to see if they deviate in any way from
22 Exhibit 1064.

23 Q. You would also have to make modifications
24 to the memory channels; correct?

25 MR. CHANDLER: Objection to form.

1 THE WITNESS: "Memory channel" is really
2 just a description of the interconnect for
3 the memory.

4 So a person of ordinary skill would
5 ordinarily -- when changing out one memory
6 type for another, would change the
7 connectivity to match the specifications for
8 the desired memory type. And just by
9 changing the connectivity and the behavior of
10 the interface to match the documented
11 specification, one would be changing the
12 channel.

13 BY MR. WARRICK:

14 Q. And when you say "changing the
15 interface," that would include, for example,
16 changing the CFM and CTM lines depict -- depicted
17 in Figure 4B; correct?

18 MR. CHANDLER: Objection. Form.

19 THE WITNESS: Those particular names are
20 specific to the Rambus interface. They would
21 be substituted by the specific names and
22 specific interconnect wires that are
23 disclosed in Exhibit 1064. That's an
24 ordinary thing to do.

25 ///

1 BY MR. WARRICK:

2 Q. You would also, for example, have to add
3 chip select lines; correct?

4 MR. CHANDLER: Objection. Form.

5 THE WITNESS: You would make the
6 interface compatible with the JEDEC
7 specification in Ex. 1064, that includes a
8 number of lines that are described on page 6
9 of JEDEC standard 79-2.

10 You would simply substitute one
11 well-known interface for another.

12 BY MR. WARRICK:

13 Q. Are you characterizing Perego as a
14 well-known interface?

15 A. No. I'm characterizing the DDR2 device
16 interconnect interface and the Rambus device
17 interconnect interface as well-known interfaces.

18 Q. And one of the changes you would have to
19 make is to add chip select lines in order to be
20 compliant with the JEDEC standard for DDR2;
21 correct?

22 MR. CHANDLER: Objection. Form.

23 THE WITNESS: Chip select lines are one
24 of the aspects of the DDR2 standard.

25 And if you substituted one well-known

1 standard for another, you would have to
2 remove all of the connections from the first
3 standard and replace them with all of the
4 connections from the second standard.

5 BY MR. WARRICK:

6 Q. And that would include chip select lines
7 that are not depicted in Figure 4B; correct?

8 MR. CHANDLER: Object to form.

9 THE WITNESS: The JEDEC connections are
10 not literally depicted in Figure 4B. But as
11 we've discussed a number of times, Perego
12 informs a person of ordinary skill in the art
13 that they can be used as an alternative to
14 the Rambus interconnect.

15 MR. CHANDLER: Phil, whenever it's a good
16 time for a break -- we've been going about an
17 hour -- so that we can sequence this to get
18 three sessions before lunch if possible.

19 MR. WARRICK: Yes.

20 BY MR. WARRICK:

21 Q. Dr. Wolfe, would you mind if I ask just a
22 couple more questions and then we take a break?

23 A. That's fine.

24 Q. I just want to make sure I understand.
25 From your explanation, Figure 4B is depicting a

1 well-known Rambus-style interface between the
2 buffer and the memory devices; yes?

3 A. That Figure 4B literally illustrates a
4 well-known Rambus-style interface between the
5 buffer and the memory devices. And Perego
6 elsewhere explains that other memory interfaces
7 can be used instead.

8 Q. And if you were to use DDR2 memory
9 devices in Figure 4B of Perego, you would also
10 have to change the interconnects between those
11 devices and the buffer; correct?

12 MR. CHANDLER: Objection. Form.

13 THE WITNESS: You would replace the
14 well-known Rambus interface with the
15 well-known DDR2 interface.

16 BY MR. WARRICK:

17 Q. And isn't it correct you would also have
18 to make changes to the design of the buffer in
19 Figure 4B of Perego if you substituted DDR2 memory
20 devices?

21 A. Correct. You would -- you would take
22 aspects of the buffer that were designed to be
23 compliant with the public Rambus standard, and you
24 would change them to be compliant with the public
25 DDR2 standard.

1 MR. WARRICK: Okay. We can take a break.

2 MR. CHANDLER: Five minutes is fine here.

3 (Short break taken.)

4 THE WITNESS: Can I clarify one of my
5 prior answers?

6 BY MR. WARRICK:

7 Q. What answer is that, Dr. Wolfe?

8 A. You asked me a number of questions about
9 whether or not the illustration on Figure 4B was
10 literally Rambus. And now that I've had another
11 chance to look at the patent, at the end of the
12 description at the bottom of Column 9 and the top
13 of Column 10, it's pretty clear that one's
14 intended to interpret those labels more broadly
15 than Rambus. Specifically, the RQ control lines
16 are described as that they can be individual
17 control lines, including row address strobe,
18 column address stroke, etc., which are DDR-style
19 signals.

20 And, in fact, if you go on to the rest of
21 that paragraph, it points one to Figure 6A, where
22 it says that you can have individual device-select
23 lines as well, which would be chip selects.

24 Q. So just to be clear, you're talking about
25 the paragraph that spans the bottom of Column 9

1 and the top of Column 10 in Perego?

2 A. Generally. It's actually from about line
3 34 in Column 9 through line 4 in Column 10.

4 Q. Well, in Column 9, starting around line
5 58, it talks about the control lines, which I
6 think you referenced earlier, RQ.

7 And that's in the context of alternate
8 embodiments; correct?

9 A. Yes. But also it's part of a section
10 that talks about being -- with reference to
11 Figures 4A, 4B, and 4C.

12 Q. And that particular paragraph references
13 6A, as you mentioned, as depicting one such
14 alternate embodiment; right?

15 A. Later in the paragraph, it does.

16 Q. So again, Figure 4A -- 4 -- strike that.

17 Figure 4B of Perego is one example and
18 what you are highlighting to me as text in Perego
19 talking about other embodiments; correct?

20 A. My understanding in context would be that
21 that's intended to describe the range of
22 embodiments that are represented by Figures 4A,
23 4B, and 4C.

24 Q. And, Dr. Wolfe, we just came back from a
25 brief break.

1 Did you have discussions with counsel
2 during that break?

3 A. I did not communicate with anyone in any
4 way during the break.

5 Q. Okay. So going back to your proposed
6 construction for rank in the context of the '417
7 and '215 patents. We had been looking at that
8 earlier in paragraph 126 of your '417 patent
9 declaration, for example.

10 Do you recall that?

11 A. Yes.

12 Q. And part of your construction is that the
13 memory devices act together to read or write the
14 full bit width of the memory module; correct?

15 A. That one or more memory devices act
16 together to read or write the full bit width of
17 the memory module. In the context of memory
18 modules, I believe that's correct.

19 Q. And, in your view, how does one know the
20 full bit width of the memory module?

21 A. It's defined by the design.

22 Q. Is it a fixed number for any given memory
23 module?

24 MR. CHANDLER: Objection. Form.

25 THE WITNESS: I wouldn't say that it's

1 not possible to have a configureable memory
2 module, but once the module's been figured,
3 the full bit width, I think, is a -- is
4 established.

5 Now, as I mentioned, sometimes computer
6 systems will perform a partial read and
7 write. That doesn't change what we mean when
8 we use the word "rank."

9 BY MR. WARRICK:

10 Q. When you say "a partial read and write,"
11 do you mean a read or write that involves less
12 than all of the memory devices within a given
13 rank?

14 MR. CHANDLER: Objection. Form.

15 THE WITNESS: In some computer systems,
16 that is a capability, that a rank can read or
17 write some or all of its bits. People would
18 still ordinarily call that a "rank," even --
19 even if not every single memory transaction
20 used every bit.

21 BY MR. WARRICK:

22 Q. You mentioned that some memory modules
23 could be configured in terms of the bit width of
24 the module.

25 Is Perego describing such a system?

1 A. Perego has a configurable interface. I
2 don't think the sizes of ranks are configurable.
3 But it's the interface width. It's not the size
4 of the memory module transaction.

5 But again, I haven't relied on the
6 configurability. Perego clearly defines -- or
7 clearly describes modules which have been
8 pre-configured to have the width of the memory
9 module be equal to the width of the rank.

10 Q. So backing up, what I'm asking about
11 right now is the bit width of the module itself
12 separate from the bit width of any ranks within
13 it.

14 And what I'm asking is, how does one know
15 the bit width for a given memory module?

16 MR. CHANDLER: Object to form.

17 THE WITNESS: In practice, one would read
18 the specifications of how it -- how it
19 operates.

20 BY MR. WARRICK:

21 Q. Is it tied to the maximum number of bits
22 that could be output from the memory module
23 simultaneously?

24 A. Again, we have to look at it in context.
25 But typically the maximum number of bits in a

1 particular configuration would be the bit width of
2 the module.

3 Q. Having reviewed Perego, do you have a
4 view on the full bit width of the memory module
5 depicted in Figure 4B?

6 A. I don't think it's restricted in any way.
7 One would make it -- I mean, in one illustration
8 of the example, in 4B, it's 16 bits.

9 But again, if you read the text, it's
10 clear that one can pick any number of bits up to
11 and including the bit width of a rank.

12 Q. It can't be more than the bit width of a
13 rank?

14 MR. CHANDLER: Objection. Form.

15 THE WITNESS: Perhaps it can. Again, I
16 didn't have to consider all those cases
17 because it clearly discloses that it can be
18 the bit width of a rank. And that's the only
19 embodiment that one needs to understand that
20 the asserted claims are obvious -- or the
21 challenged claims are obvious.

22 BY MR. WARRICK:

23 Q. So under your proposed construction,
24 memory devices that are acting together to read or
25 write less than the full bit width of a memory

1 module would not be a rank; correct?

2 MR. CHANDLER: Objection. Form.

3 THE WITNESS: Again, I think it would
4 be -- a person of ordinary skill would use
5 common sense. The fact that in one memory
6 transaction only a portion of the memory
7 module bit width was used would not make that
8 memory stop being a rank. If it had the
9 ordinary capability to read and write the
10 full bit width of the memory module in
11 response to command signals, including chip
12 select signals, then a person of ordinary
13 skill would understand that to be a rank.

14 The fact that it could potentially do
15 other things, as well, would not make it stop
16 being a rank.

17 BY MR. WARRICK:

18 Q. What about memory devices that act
19 together to read or write more than the full bit
20 width of the memory module, would those not
21 qualify as a rank under your definition?

22 A. I'd have to look at a particular design,
23 but I think that they probably would be a rank.

24 Q. Well, for example, if Figure 4B, if we
25 assume that it depicts a module with a full bit

1 width of 16, and you have memory devices within 4B
2 that act together to read or write 32 bits, that
3 wouldn't be a rank under your definition, would
4 it?

5 MR. CHANDLER: Objection. Form.

6 THE WITNESS: Again, that's not an
7 embodiment that I relied on. But I think a
8 rank can be bigger than the interface and
9 still be a rank.

10 Again, you know, a person of ordinary
11 skill in the art doesn't use the term in some
12 prosecutorial manner, where it's trying to --
13 to do more than -- than assist a person in
14 understanding the art.

15 What we're trying to do is distinguish
16 the memory devices that are accessed together
17 to provide a read or a write from the ones
18 that are accessed separately to provide a
19 read or a write.

20 BY MR. WARRICK:

21 Q. And I believe you said earlier today that
22 when you say "access together," you mean at
23 approximately the same time and in response to the
24 same command signals; yes?

25 A. Yes. In the way that an ordinary person

1 of skill would understand being accessed together
2 in a memory system so that within reasonable
3 engineering parameters they are responding at the
4 same time.

5 Q. Now, the bit width of the memory module
6 is tied to the buffer data path width; am I right
7 about that?

8 MR. CHANDLER: Objection. Form.

9 THE WITNESS: I'm not sure what context
10 you're speaking in.

11 BY MR. WARRICK:

12 Q. In the context of Figure 4B in Perego,
13 for example.

14 A. Ask me one more time, please.

15 Q. Well, in Figure 4B of Perego, the buffer
16 has a data path width; correct?

17 MR. CHANDLER: Objection. Form.

18 THE WITNESS: I'm not exactly sure what
19 you're referring to. The width of which
20 particular set of signals?

21 BY MR. WARRICK:

22 Q. Well, let's look at -- towards the bottom
23 of Figure 4B, you see some up and down arrows and
24 the number 16?

25 A. Yes.

1 Q. Is that referring to the number of pins
2 or lines connected to the buffer?

3 A. In an exemplary embodiment, yes; the
4 number of -- of data pins that are connected in an
5 exemplary embodiment of Figure 4B.

6 Q. And so 16 pins, would that imply a 16-bit
7 memory module bit width?

8 A. In an exemplary embodiment, yes.

9 Q. And is it true that the memory module bit
10 width could also be greater than 16 in that
11 context if you had a serialization ratio greater
12 than 1:1?

13 MR. CHANDLER: Object to form.

14 THE WITNESS: It depends how you're
15 defining "bit width of the module."

16 Again, Perego doesn't intend to be
17 limiting. He describes a variety of
18 different interface widths that can be
19 implemented.

20 BY MR. WARRICK:

21 Q. Well, let's bring it back to your
22 proposed construction, because what I really want
23 to understand, Dr. Wolfe, is what you mean in your
24 proposed construction by the "full bit width of
25 the memory module."

1 Perego is one example. But generally,
2 for your construction, how do we determine the
3 full bit width of a memory module?

4 A. It's usually, as I said, defined for the
5 memory module; but it would typically be defined
6 as the size of a standard read or write operation
7 to that module.

8 Q. And is the size of a standard read or
9 write operation for a given module tied to the
10 number of contacts on the module used for data?

11 MR. CHANDLER: Objection. Form.

12 THE WITNESS: In the most common cases,
13 it is, but I don't know that it necessarily
14 needs to be.

15 BY MR. WARRICK:

16 Q. I want to go back to this concept in your
17 proposed construction of memory devices acting
18 together.

19 And if we look at Figure 4B of Perego as
20 an example, your view is that all of the memory
21 devices across the top of Figure 4B that are
22 connected to Channels 415c and 415d comprise one
23 rank; correct?

24 A. Yes, in certain disclosed embodiments.

25 Q. And that is in part because, in your

1 view, those memory devices act together in
2 response to command signals to read or write the
3 full bit width of the memory module?

4 A. Yes. Again, in certain embodiments.

5 Q. Now, in Figure 4A on the other hand, in
6 your view, each rank has half the number of memory
7 devices as the ranks you identified in Perego 4B;
8 correct?

9 MR. CHANDLER: Object to form.

10 THE WITNESS: In certain exemplary
11 embodiments, yes.

12 BY MR. WARRICK:

13 Q. Now, does it follow that in those
14 embodiments the full bit width of the memory
15 module in Figure 4A is less than the full bit
16 width of a memory module in Figure 4B?

17 A. Not necessarily. The individual memory
18 devices can be twice as wide.

19 Q. You mentioned earlier that there's this
20 concept of partial reads and writes; is that
21 right?

22 A. In some commercial systems.

23 Q. If we look at Figure 4B and the memory
24 devices that are connected to Channels 415c and
25 415d, if half of those devices, for example, the

1 memory devices on Channel 415c, are acting
2 together to read or write the full bit width of
3 the memory module, does that become a separate
4 rank?

5 MR. CHANDLER: Objection. Form.

6 THE WITNESS: I don't know. That's not
7 the embodiment I relied on. So I would have
8 to look at what changes you're actually
9 proposing in detail.

10 BY MR. WARRICK:

11 Q. Well, I'm just asking, Dr. Wolfe, if
12 those four memory devices on the upper left of
13 Figure 4B, connected to Channel 415c, act together
14 to read or write the full bit width of the memory
15 module, then that would be a "rank" under your
16 understanding of the term; yes?

17 MR. CHANDLER: Objection. Form.

18 THE WITNESS: That would be a different
19 embodiment than the one I relied on. It
20 would operate differently, and I would have
21 to understand how it operated in detail.

22 BY MR. WARRICK:

23 Q. Now, Perego is titled "Configurable Width
24 Buffered Module"; correct?

25 A. Correct.

1 Q. What does that mean in the context of
2 Perego, to have a configurable width buffered
3 module?

4 A. That means that in addition to disclosing
5 rank multiplication, Perego also discloses, as
6 illustrated in Figure 5C, that one feature of his
7 module is that the interface width can be
8 configured to more than one different option in
9 some embodiments.

10 Q. When you say the "interface width," are
11 you describing the width of the interface into the
12 buffer or from the buffer to the memory devices?

13 A. In the interface, as what's shown as
14 Interface 596 on Figure 5B, for example.

15 Q. And so Perego has a configurable
16 serialization circuit that's capable of varying
17 the data path width; is that right?

18 MR. CHANDLER: Object to form.

19 THE WITNESS: In some of his embodiments,
20 he does.

21 BY MR. WARRICK:

22 Q. Going back to Figure 4B of Perego, I
23 think I understood from you earlier that all of
24 the memory devices connected to Channel 415a and
25 415b comprise one rank; is that right?

1 A. In at least one embodiment, that would be
2 true.

3 Q. So in that embodiment, they would operate
4 simultaneously to satisfy a single memory read or
5 write command; correct?

6 A. Correct.

7 Q. And those eight memory devices in that
8 embodiment would be working together to output
9 data to -- 16 bits of data on the DQ lines?

10 MR. CHANDLER: Objection. Form.

11 THE WITNESS: No. This -- this Figure 4A
12 is not -- 4B or is not limited to 16 bits.

13 Could be 32 bits or 64 bits or 128 bits.

14 Those are all disclosed in Perego.

15 BY MR. WARRICK:

16 Q. But literally Figure 4B shows a bit width
17 of 16; correct?

18 A. It's literally what's shown in the
19 example. But again, the content -- the patent
20 itself tells you that that's not a limitation of
21 Figure 4B.

22 Q. So in that context of an example that has
23 a 16-bit width memory module, the eight memory
24 devices connected to Channels 415a and 415b are
25 working together to output 16 bits of data;

1 correct?

2 MR. CHANDLER: Object to form.

3 THE WITNESS: There would be no reason to
4 limit it to 16 bits. But if one were to
5 choose to limit the buffer-to-host connection
6 to 16 bits and to decide that there were
7 eight module memory devices in each rank,
8 then they would work together to supply 16
9 bits.

10 BY MR. WARRICK:

11 Q. You mentioned the concept of rank
12 multiplication a minute ago.

13 A. Yes.

14 Q. It's your contention that Perego
15 discloses rank multiplication.

16 Am I understanding that correctly?

17 A. I don't recall if I reached that
18 conclusion.

19 Q. Well, let me ask you, then. Do you
20 have -- have you offered an opinion in this -- in
21 these proceedings about whether or not Perego
22 discloses rank multiplication?

23 A. Yeah. Paragraph 241 of my '417
24 declaration, I did conclude that, "Perego teaches
25 that the 'logic' in the buffer device can perform

1 'rank multiplication'..."

2 Q. So, to me, that sounds a little bit
3 different.

4 I see in paragraph 241 of your '417
5 patent declaration, "Perego teaches that the
6 'logic' in the buffer device can perform 'rank
7 multiplication'..."

8 Do the words "rank multiplication" appear
9 in Perego?

10 A. Not that I can recall.

11 Q. For that matter, does the term "rank"
12 appear in the Perego reference?

13 A. I don't recall the term being used, but
14 the concept is there.

15 Q. So if, in your view, Perego is disclosing
16 rank multiplication, am I understanding correctly
17 that Perego can present fewer ranks than actually
18 exist as physical ranks?

19 A. I'm not sure what it means to -- I don't
20 even remember the word you used.

21 Did you say "present ranks"? Is that the
22 term you used?

23 Q. Yes.

24 A. I'm not sure I know what it means to
25 "present ranks."

1 It can --

2 Q. Let me ask this, then. Can Perego, in
3 your view of what you're describing as the rank
4 multiplication disclosed in Perego, make more than
5 one physical rank appear as only one rank to the
6 rest of the system?

7 A. In essence, yes. Because what it can do
8 is it can take a memory request that is too large
9 to be serviced by one physical rank and have it
10 serviced by two physical ranks in a way that the
11 original host can't tell the difference.

12 Q. And it's your view that that concept is
13 disclosed by Perego?

14 A. Yes.

15 Q. So would an example of that be, in Figure
16 4B, Perego making what you call the two ranks
17 appear as just a single rank to the memory
18 controller?

19 MR. CHANDLER: Object to form.

20 THE WITNESS: If by the "memory
21 controller," you mean the memory controller
22 in an external host, essentially, yes.

23 BY MR. WARRICK:

24 Q. I want to go back to the example we were
25 discussing in Figure 4B, where I asked about the

1 context of the module bit width being 16 and the
2 eight memory devices on Channels 415a and 415b
3 working together to output 16 bits.

4 Do you recall that?

5 A. I recall the question.

6 Q. So in that example, just so I understand,
7 is it correct that each of those eight memory
8 devices would be outputting two bits each?

9 MR. CHANDLER: Object to form.

10 THE WITNESS: In that example, that would
11 be the case.

12 But again, there is nothing special about
13 those numbers with respect to 4B.

14 A person of ordinary skill in the art who
15 implemented Figure 4B in light of the JEDEC
16 standard in Exhibit 1064 would likely choose
17 different specific values.

18 BY MR. WARRICK:

19 Q. In Figure 4B of Perego, does the bit
20 width of the memory module change depending on how
21 many of the channels are working together?

22 MR. CHANDLER: Object to form.

23 THE WITNESS: I don't believe so. I
24 believe that it's just the interface -- if
25 we're talking about the same bit width of the

1 module, I believe it's only the interface
2 that changes.

3 BY MR. WARRICK:

4 Q. If all 16 memory devices depicted in
5 Figure 4B of Perego are operating simultaneously
6 to read or write the full bit width of the module,
7 does that mean that there would be just a single
8 rank in that example?

9 A. I don't believe I -- I don't recall
10 seeing a description of such an embodiment in
11 Perego.

12 Q. Am I correct that Perego has the
13 flexibility to configure a rank in that way?

14 A. I'm not sure what you're asking.
15 Certainly, you can have a single-rank embodiment
16 of Figure 4A; that is described in Perego. But I
17 don't believe that a single-rank embodiment of 4B
18 is actually described in Perego.

19 Q. What I ask is whether Perego would permit
20 a skilled artisan to configure a single-rank
21 embodiment in the context of Figure 4B.

22 A. I don't know. I haven't considered that.
23 I -- I relied on the two-bank -- or the two-rank
24 embodiment that was actually described in Perego.

25 Q. When Perego is allegedly performing rank

1 multiplication, in your view, and it's making two
2 physical ranks appear as one rank to the external
3 memory controller, what differentiates those two
4 ranks such that they are not really just one
5 larger rank?

6 A. I think in that particular case, they
7 would be accessed by different control signals at
8 different times.

9 Q. You said a minute ago that you hadn't
10 contemplated the possibility of a single-rank
11 embodiment in the context of Perego 4B. But if we
12 were to change Figure 4B from a 16-bit memory
13 module to a 64-bit memory module, would that imply
14 a single-rank embodiment, all else being equal?

15 A. I don't know what you mean by "all else
16 being equal." I would not do it that way. If I
17 were to make a 64-bit-wide host interface on an
18 embodiment of 4B, and I would do that using DDR2
19 interfaces, as I've suggested, I would use 8-by-8
20 chips in each rank to provide a 64-bit response.

21 Q. So let's say you did use eight-bit memory
22 devices; and in total in Figure B there are 16 of
23 them; and let's assume that the context is a
24 128-bit module width. Would that be a single-rank
25 example?

1 A. It might be. But again, that's not
2 really following what's taught about Figure 4B.
3 If I were using by-8 chips, I would put 16 in each
4 rank to get 128-bit host interface, or I would use
5 8-by-16 chips if I wanted each rank to provide 128
6 bits to 128-bit interface.

7 So that's the natural conclusion that I
8 would reach in implementing Figure 4B in a JEDEC
9 DDR2-compliant environment.

10 Could a person of ordinary skill do other
11 things? Yes, probably.

12 Q. So memory devices on separate channels
13 can act together to respond to command signals to
14 read or write the full width -- bit width of the
15 memory module; correct?

16 A. Depending on how you define a channel.
17 If you define that as a set of wires, then yes,
18 that's correct, as long as the signals are
19 duplicated across both sets of wires -- or
20 specifically the control signals are duplicated
21 across both sets of wires.

22 Q. So for example, in Perego 4B, in your
23 understanding, the memory devices connected to
24 Channels 415c and 415a could act together to form
25 a single rank?

1 MR. CHANDLER: Objection. Form.

2 THE WITNESS: Not consistently with the
3 description of Perego. A person of ordinary
4 skill could probably modify it that way. But
5 in Perego -- the way it's described in
6 Perego, my understanding is that it's 415c
7 and 415d that would have duplicate control
8 signals and 415a and 415b that would have
9 duplicate control signals.

10 BY MR. WARRICK:

11 Q. Are you saying it's not disclosed in
12 Perego that one could send the same control
13 signals to the memory devices on Channels 415c and
14 415a in Figure 4B?

15 A. I don't recall that disclosure. But
16 again, it's not really relevant to my conclusions,
17 because whether or not someone could do something
18 different in Perego doesn't have anything to do
19 with what it discloses with respect to the claims.

20 Q. Is that an important distinction?

21 A. Is what an important distinction?

22 Q. Between what Perego actually discloses
23 and what someone theoretically could do in view of
24 the disclosure.

25 A. Both are valuable in assessing

1 obviousness. But once one has concluded that
2 Perego discloses or renders obvious the claims,
3 it's not necessary to make a determination as to
4 whether or not other things are also obvious.

5 Q. In Perego, if you could look, please, at
6 Column 15, around line 45, there's a reference to:

7 "...grouping memory devices into multiple
8 independent target subsets (i.e. more
9 independent banks)."

10 Do you see that?

11 A. That's the paragraph that starts at line
12 31?

13 Q. Correct.

14 A. Let me read it, please.

15 Okay.

16 Q. You've read the -- the paragraph in
17 Column 15?

18 A. Yes.

19 Q. So I'm specifically interested in the
20 last sentence of that paragraph, Column 15, lines
21 43 to 45.

22 It talks about "...grouping memory
23 devices into multiple independent target
24 subsets (i.e. more independent banks)."

25 Do you see that?

1 A. Yes.

2 Q. Is Perego referencing ranks in that
3 discussion, in your view?

4 A. Yes.

5 Q. So your understanding is that grouping --
6 the reference to "grouping memory devices into
7 multiple independent target subsets," is, in fact,
8 grouping memory devices into "ranks," under your
9 understanding of that term?

10 MR. CHANDLER: Object to form.

11 THE WITNESS: Yes. Under some
12 conditions, that would be true.

13 It's important to understand that -- that
14 this entire paragraph is both conditional and
15 permissive.

16 But I do believe that he's discussing the
17 possibility of, in some cases, increasing the
18 number of ranks.

19 BY MR. WARRICK:

20 Q. What's your understanding of what Perego
21 means by a "more independent bank"?

22 MR. CHANDLER: Objection to form.

23 THE WITNESS: My understanding is that
24 he's saying that there could be alternative
25 embodiments that have more ranks than the

1 embodiment that he's previously described,
2 under certain conditions and if one chooses.

3 BY MR. WARRICK:

4 Q. Is Perego referencing a rank, in your
5 view, when it says "independent banks"?

6 A. I think broadly he is -- is talking about
7 the same general concept.

8 Q. Generally speaking, if multiple memory
9 devices output data that collectively is part of a
10 single memory device transfer operation, is that
11 potentially a "rank," under your understanding of
12 the term?

13 MR. CHANDLER: Object to form.

14 THE WITNESS: Can I hear that one more
15 time?

16 BY MR. WARRICK:

17 Q. Yes.

18 Generally speaking, if multiple memory
19 devices output data that is part of a single
20 memory device transfer operation, is that
21 potentially a "rank," under your understanding of
22 the term?

23 MR. CHANDLER: Objection. Form.

24 THE WITNESS: I think that could be a
25 rank, depending on other factors.

1 Again, a person of ordinary skill in the
2 art is really trying to make a determination
3 of whether or not their memory chips are in
4 the same rank or in different ranks.

5 They are not trying to, in some
6 hypercritical way, define a "rank" so
7 narrowly that -- that something that operates
8 essentially like a rank is excluded because
9 of some minor technicality.

10 BY MR. WARRICK:

11 Q. So a "rank" is a flexible concept, under
12 your understanding, in this context?

13 MR. CHANDLER: Objection. Form.

14 THE WITNESS: No. I think in this
15 context, it's a descriptive term that helps
16 us to understand whether or not memory
17 devices are activated together or separately.

18 BY MR. WARRICK:

19 Q. When you --

20 MR. CHANDLER: Sorry. I was just going
21 to say, you know, if we want to have a third
22 session before lunch, we should probably take
23 a break whenever is convenient.

24 MR. WARRICK: Okay. I think we would be
25 near a good stopping point soon.

1 BY MR. WARRICK:

2 Q. Dr. Wolfe, you said that -- you
3 referenced memory devices being activated together
4 or separately in your last answer?

5 A. Right.

6 Q. What do you mean by "activated"?

7 A. Responding to control signals, including
8 a chip select.

9 Q. You mean "activated," in your view, is
10 distinct from responding to a read or write
11 command; is that right?

12 MR. CHANDLER: Objection. Form.

13 THE WITNESS: No. It's simply a word
14 that I used to mean "responding to a read or
15 write command."

16 BY MR. WARRICK:

17 Q. So you were not referencing, for example,
18 the concept of row activation?

19 A. No.

20 Q. In your view, does row activation play
21 any role in the configuring of a rank?

22 MR. CHANDLER: Objection to form.

23 THE WITNESS: Not necessarily. It would
24 be common to have all of the devices in a
25 rank respond together to a row activation and

1 devices in a different rank have a separate
2 row activation, but it's not definitional.

3 BY MR. WARRICK:

4 Q. Does a memory device have to be activated
5 before it can respond to read or write memory
6 commands?

7 MR. CHANDLER: Objection. Form.

8 THE WITNESS: Not in general. But DDR2
9 DRAM devices do.

10 MR. WARRICK: Okay. I think we could
11 take a break here. Is five minutes good
12 again?

13 MR. CHANDLER: Sure. Good for me.

14 MR. WARRICK: All right.

15 (Short break taken.)

16 BY MR. WARRICK:

17 Q. Dr. Wolfe, before the break, we were
18 talking about row activation, and you noted that
19 in DDR2 SDRAM implementations and embodiments,
20 there has to be a row activation command before
21 reads and writes can be performed; is that
22 accurate?

23 A. Correct.

24 Q. And in the example of Perego, the buffer
25 will select the target subset channels based on

1 address bits; is that right?

2 MR. CHANDLER: Object to form.

3 THE WITNESS: Looking at something
4 particular in Perego?

5 BY MR. WARRICK:

6 Q. Perego generally. Just based on the
7 disclosures of Perego.

8 A. I think it can select based on address
9 bits.

10 Q. So in Perego, is it correct that all of
11 the memory devices in the possible target subset
12 channels have to be activated together?

13 MR. CHANDLER: Object to form.

14 THE WITNESS: If in an embodiment of
15 Perego you're going to have multiple memory
16 devices respond to the same read or write
17 operation, they both need to have the same
18 row activated. Normally you would do that
19 together, but they could be done
20 sequentially.

21 BY MR. WARRICK:

22 Q. Does Perego disclose selecting target
23 subsets based on anything other than address bits?

24 A. I don't recall it explicitly saying that,
25 but it also doesn't in any way limit it to the

1 address bits. And a person of ordinary skill,
2 when looking at the JEDEC standard in Exhibit
3 1064, would understand that you can select
4 portions of memory or memory devices from a set
5 using either address bits or bank address inputs.

6 Bank address inputs are essentially
7 simply extended address bits for many purposes.

8 Q. Okay. So let's consider the example of
9 having two channels and each is a possible target
10 subset. In that case, is it correct that you have
11 to send an activation command to all of the DRAMs
12 on all of the target subset channels?

13 MR. CHANDLER: Objection. Form.

14 THE WITNESS: If you're using a DDR2
15 implementation, you need to activate rows
16 before you read or write them in all cases.

17 BY MR. WARRICK:

18 Q. And so my question is, in that context of
19 a DDR2 implementation, if you have two channels
20 that are potential target subsets, you would need
21 to activate the rows in all of those memory
22 devices in both channels; correct?

23 MR. CHANDLER: Objection. Form.

24 THE WITNESS: Not clear to me what
25 you're -- how you're using the word "target

1 subsets" in the question.

2 BY MR. WARRICK:

3 Q. In the context of the Perego disclosure
4 we had been looking at before the break, in Column
5 15, about multiple independent target subsets.

6 A. Well, again, that's only one permitted
7 embodiment of Perego. If you want to access a row
8 across a group of memory devices, the same row
9 needs to be activated in each memory device that
10 you're going to access using the signal read or
11 write command.

12 Q. Can we look at the abstract of Perego for
13 a minute?

14 A. Okay.

15 Q. And the third sentence of the abstract,
16 I'm going to read, if you could follow along with
17 me.

18 It says, "The configurable width buffer
19 device includes a interface and a configurable
20 serialization circuit capable of varying a data
21 path width or a number of contacts used at the
22 interface of the configurable width buffer device
23 in accessing the at least one memory device."

24 Did I read that correctly?

25 A. Yes.

1 Q. And based on that disclosure in the
2 abstract, is it correct that Perego permits
3 configuration of both the data path and the
4 contacts of the interface?

5 MR. CHANDLER: Object to form.

6 THE WITNESS: In some embodiments, Perego
7 permits that. In other embodiments, he talks
8 about a one-to-one serialization ratio and he
9 talks about determining the configuration and
10 manufacturing time.

11 BY MR. WARRICK:

12 Q. Can we look at Column 21, please, of
13 Perego, and the paragraph that starts on line 16
14 of Column 21.

15 A. Okay.

16 Q. So again, specifically, the first
17 sentence, starting on line 16 of Column 21 of
18 Perego, says [as read]: "Any number of channels
19 415a through 415d, for example; two Channels 415c
20 and 415d may transfer information simultaneously
21 and the memory devices on the other two channels
22 415a and 415b remain in a ready or standby state
23 until called upon to perform memory access
24 operations."

25 Did I read that correctly?

1 A. I believe so.

2 Q. Am I -- is it your understanding of that
3 disclosure that if two channels in Perego are
4 transferring information simultaneously, the other
5 channels are in a ready or standby state at that
6 time?

7 MR. CHANDLER: Objection. Form.

8 THE WITNESS: My understanding is that
9 that's permitted. This is all permissive
10 language.

11 I think this is supportive of a two-rank
12 configuration of Figure 4B in which channels
13 4c and 4d are accessed together and 4a and 4b
14 are waiting for the next access.

15 BY MR. WARRICK:

16 Q. Now, am I correct that that example is
17 the partial rank access that you were describing
18 earlier today?

19 A. No. In that case, there's a full rank, c
20 and d, that's being accessed, and a second rank, a
21 and b, that's not being accessed.

22 Q. Can we look for a second at paragraph 269
23 of your declaration for the '417 patent.

24 Do you have that in front of you?

25 A. Yes.

1 Q. And in paragraph 269 of your declaration,
2 in the prior paragraph, you reference the same
3 portion of Perego that we were just reading, but
4 you reference the concept of keeping channels "in
5 a ready or standby state."

6 Is that different than keeping the
7 devices on the channels in a ready or standby
8 state?

9 A. It would be slightly different, but they
10 are intended to describe the same operation. When
11 the devices are in a standby state, one would
12 describe the channel as being in a standby state.

13 Q. And when you say that, are you saying
14 that specifically for the context of Perego or as
15 a more general matter for memory devices?

16 A. I think in general, if all of the devices
17 connected to a channel are in a standby state, a
18 person of ordinary skill would -- might say that
19 that channel is in a standby state.

20 Q. Are you aware of a separate concept in
21 the memory art of having a channel in a ready or
22 standby state as distinct from the memory devices
23 on the channel being in that state?

24 MR. CHANDLER: Object to form.

25 THE WITNESS: I can't recall seeing that

1 formally. But I think less formally, one
2 might use the descriptive term that a channel
3 is in a standby state to mean that all the
4 devices on the channel, including the host,
5 are in a standby -- well, in this case,
6 "host" might be misleading.

7 That all the devices connected to the
8 channel, whether they be memory devices or
9 control devices, are in a standby state,
10 where, at least hypothetically, individual
11 devices on a channel can be in a standby
12 state while other devices are not.

13 BY MR. WARRICK:

14 Q. Going back to the sentence that we
15 started with on Column 21 of Perego, starting on
16 line 16, I just want to make sure I understand the
17 partial rank access concept that you've mentioned
18 a couple of times today.

19 I believe you said just a few minutes ago
20 that you understand this sentence to be talking
21 about one rank, including two channels, to be
22 transferring information while another rank,
23 including the other two channels, being in this
24 standby state; is that right?

25 A. That's my understanding of the example in

1 Column 1 -- I'm sorry.

2 That's my understanding of the example in
3 Column 21 starting at line 16.

4 Q. So what I'd like to understand is how is
5 that different than having a single rank,
6 including all four channels, that's being
7 partially accessed?

8 A. Because there's no capability described
9 here that -- that all four channels can respond to
10 a single request.

11 Again, in a -- in a basic memory system,
12 if we have a 32-bit memory system, in some memory
13 systems that are commercially used, there is an
14 additional capability to only write 8 bits out of
15 the 32. But a person of ordinary skill would not
16 describe that as no longer being a 32-bit memory
17 interface just because it has that additional
18 capability.

19 This is not being described as an
20 additional capability of a larger interface. This
21 is being described as its primary mode of
22 operation, that channels a and b operate together
23 in response -- in response to a memory access
24 operation, and Channels c and d can operate
25 together in response to a different memory

1 operation.

2 Q. Maybe it would be simpler if we looked at
3 Figure 4A of Perego.

4 And as I understood you earlier today,
5 Dr. Wolfe, you indicated that the embodiment
6 depicted in 4A could include either one rank or
7 two ranks; is that right?

8 A. No. I said that the patent describes a
9 one-rank embodiment of Figure 4A, and the patent
10 also describes a two-rank embodiment of Figure 4A.

11 Q. So as between those two embodiments, what
12 is the distinction, in your view, between the
13 two-rank embodiment and a partial access of the
14 one-rank embodiment that involves only one of the
15 channels?

16 A. Well, we don't know that there is a
17 partial access capability in any of these
18 embodiments. They are not described in Perego,
19 and they may not exist.

20 So the primary difference would be that
21 in normal operation a one-rank embodiment would
22 access all eight memory devices, and a two-rank
23 embodiment would either access the four memory
24 devices on the left or alternatively access the
25 four memory devices on the right.

1 In a two-rank embodiment, one could
2 either access the four on the left or the four on
3 the right. In normal operation, in a one-rank
4 embodiment, all eight would be accessed.

5 Now, independent of any of the teachings
6 of Perego, if in addition to having the capability
7 of having one rank access all eight you had the
8 capability to only access one memory device, a
9 person of ordinary skill would no -- wouldn't say,
10 "Well, that's no longer a one-rank because it has
11 an additional capability," because a basic read
12 operation would access every memory device.
13 That's what makes it one rank.

14 Q. Just so I understand, your view is that
15 Perego does not disclose a partial access
16 capability?

17 A. I don't recall seeing one with respect to
18 a single-rank embodiment of Figure 4A.

19 Q. Do you recall seeing one in connection
20 with any embodiments of Perego?

21 A. Not off the top of my head.

22 Q. Let's look, if we could, at paragraph 48
23 of your declaration in connection with the '417
24 patent.

25 Do you have that in front of you?

1 A. I do. It's long, but I have the two
2 pages in front of me.

3 Q. And in this portion of your declaration,
4 you're describing your view of the person of
5 ordinary skill in the art in the context of the
6 '417 patent; correct?

7 A. Yes.

8 Q. And am I right that you propose the same
9 person of ordinary skill in the art in your
10 declaration for the '215 patent?

11 A. Let me look exactly. They are very
12 similar, but I don't recall if they are exactly
13 the same. The dates may differ a little bit.

14 It appears to be the same.

15 Q. And just so it's clear, I suppose that
16 that is also Exhibit 1003 but Exhibit 1003 from
17 the '215 patent IPR.

18 In this paragraph, you indicate that the
19 hypothetical person of ordinary skill in the art
20 "would have been familiar with various standards
21 of the day including the JEDEC industry
22 standards."

23 That's your view; correct?

24 A. Yes.

25 Q. And would be it fair to say that that

1 familiarity with various standards of the day
2 would also extend to Rambus-style DRAMs?

3 A. I'm not quite sure what you mean by
4 "Rambus-style," but the public Rambus
5 specifications would be known.

6 Q. Okay. And that would include
7 specifications for XDR, for example?

8 MR. CHANDLER: Objection to form.

9 THE WITNESS: I don't remember the exact
10 date for XDR. There were a number of Rambus
11 standards.

12 BY MR. WARRICK:

13 Q. But, in your view, those would also be
14 known to the person of ordinary skill in the art
15 in the context of the '417 and the '215 patents?

16 A. The publicly disclosed Rambus standards
17 at the time would also be known to -- by a person
18 of ordinary skill in the art.

19 Q. I would like to talk for a little bit --
20 or more precisely ask you some questions about CAS
21 latency. And perhaps we could start by just
22 asking you to explain your understanding of CAS
23 latency in the concept of memory modules.

24 A. The exact details of what CAS latency
25 means has varied from memory generation to memory

1 generation. But "CAS" stands for "column address
2 strobe." In early memories, it literally was a
3 pulse that was used to capture the column address
4 from the memory controller to the memory devices.
5 In more recent memory technologies, it was a
6 control signal or a command that was used to
7 indicate that on a specific clock cycle the column
8 address should be captured by memory devices.

9 In general, the CAS signal, in whatever
10 form that it had, was used to indicate the timing
11 of the arrival of the column address information.

12 Now, sometimes the term is used, a little
13 bit sloppily, to refer to the CAS-to-data-delay
14 value that is also a property of various memory
15 technologies.

16 Q. So your answer described various
17 different potential interpretations of the term
18 "CAS latency," depending on context. I think
19 maybe it would be helpful for us to talk about the
20 '417 and '215 patents specifically.

21 Both the '417 and the '215 patent claims
22 reference the overall CAS latency of the memory
23 module.

24 And what is your understanding of that
25 particular term in the context of the '417 and

1 '215 patents?

2 A. So there seems to be a presumption that
3 there's only one in the claim, which is not
4 necessarily true in certain memory technologies.

5 Typically, there's a read-latency, which
6 is a function -- which is described often as a CAS
7 latency for reads. And that is the amount of
8 time, again, depending on the technology, from the
9 CAS signal until data starts being returned from
10 the memory module to the host.

11 In a synchronous memory, it would be
12 defined in clock cycles or half-clock cycles. In
13 an asynchronous memory, it would be defined in a
14 time unit, like nanoseconds.

15 Oftentimes, there's a different latency
16 for a write operation that would describe how long
17 after the CAS signal the host should send data.

18 And on some memory technologies, the read
19 CAS latency and the write CAS latency are the
20 same; and in some memory technologies, they are
21 different by a known amount; and in some memory
22 technologies, they are different by a configurable
23 amount.

24 By "known," I guess I mean
25 "predetermined."

1 Q. In the context of DDR or DDR2 SDRAMs --
2 well, first, those are synchronous; correct?

3 A. DDR and DDR2 JEDEC-compliant DRAMs are
4 synchronous DRAMs.

5 Q. And in DDR and DDR2 SDRAMs, the CAS
6 control signal that you mentioned in a prior
7 answer is an integral part of the command bus to
8 the SDRAMs; correct?

9 MR. CHANDLER: Objection. Form.

10 THE WITNESS: I don't know what you mean
11 by "integral," but it is a part of the
12 normally used command bus.

13 BY MR. WARRICK:

14 Q. In your view, could you have a
15 JEDEC-compliant DDR or DDR2 implementation without
16 the CAS control signal being part of the command
17 bus?

18 MR. CHANDLER: Objection. Form.

19 THE WITNESS: There's a variety of JEDEC
20 specifications. The DDR memory chip device
21 requires a CAS signal, and the standard JEDEC
22 DDR2 DIMMs also require a CAS control signal.

23 BY MR. WARRICK:

24 Q. So if the DDR or DDR2 memory devices
25 require a CAS signal, does it not follow that that

1 signal has to be delivered to the memory devices
2 through the interface?

3 MR. CHANDLER: Objection. Form.

4 THE WITNESS: You can have chips in
5 between and still be JEDEC compliant. But
6 there are two different places where CAS
7 signals are required. Their specifications
8 are described within each corresponding JEDEC
9 specification. And in a simple, unbuffered
10 DIMM, it would be common to directly connect
11 them.

12 BY MR. WARRICK:

13 Q. So is it correct that an SDRAM will look
14 at the CAS latency -- I'm sorry. Start over.

15 Is it correct that the SDRAM, in the
16 context of DDR or DDR2, will look at the CAS
17 command signal potentially in combination with
18 other command bus signals to determine the timing
19 of operations?

20 MR. CHANDLER: Objection to form.

21 THE WITNESS: For some operations, that
22 is correct, with respect to the CAS signal
23 that is coming into that particular chip.

24 BY MR. WARRICK:

25 Q. I want to go back to this language that's

1 in the claims of both the '417 and the '215
2 patents, of the overall CAS latency of the memory
3 module. And I just want to make sure I understand
4 your view of what that means in -- in the context
5 of those two patents. And if you think it's
6 different for the patents, feel free to respond
7 separately.

8 A. So again, the patents seem to be written
9 based on an assumption that there's a single CAS
10 latency for the module -- the memory module and a
11 single CAS latency for each memory device, which
12 may not be the case in certain real-world
13 technologies.

14 But the way I would interpret it in the
15 claims is that the CAS latency of the memory
16 device, again, corresponding to the memory
17 device's specification -- you would look at it in
18 the context of the memory device's specification.
19 But in general, it's the amount of time -- in the
20 context of a read operation, it would be the
21 number of clock cycles between the assertion of
22 the CAS signal and the return of data.

23 So in the case of the memory device, it
24 would be the number of clock cycles between the
25 assertion of the CAS signal at the memory device

1 and the return of data from the memory device in
2 response to that particular transaction.

3 In the case of the module, it would be
4 the number of clock cycles between the assertion
5 of the CAS signal at the input to the module and
6 the return of data corresponding to that CAS
7 signal at the output of the module. And there
8 would be a similar definition for write
9 operations, but they would involve when data is
10 provided to the module and to the chip rather than
11 returned from the module or from the chip.

12 Q. So when you were talking about the memory
13 device in your last answer, are you referring to
14 the parts of the claims in both the '215 and '417
15 patents that talk -- that discuss the actual
16 operational CAS latency of each of the memory
17 devices?

18 A. Yes. That's generally what I was
19 referring to.

20 Q. Okay. And in both of your definitions
21 for "CAS latency of the memory device" or "the
22 module," you reference the assertion of the CAS
23 signal?

24 A. Yes.

25 Q. Is that distinct from the presentation of

1 the column access command, i.e., a read or a write
2 command?

3 MR. CHANDLER: Objection. Form.

4 THE WITNESS: I believe -- I believe that
5 it can be. There are read and write commands
6 that can happen in DDR2 separately from a CAS
7 assertion.

8 BY MR. WARRICK:

9 Q. When you say a "CAS assertion," could you
10 just explain to me what you mean by that term.

11 A. So it's a term of art. It means that the
12 CAS signal is set at a voltage level that
13 indicates that it is present.

14 So in particular, in DDR2, the actual
15 signal is not CAS. The actual signal is CAS bar.
16 And it is asserted, meaning the end device is to
17 understand that it is time for a column address
18 strobe when it has the value of zero; and it is
19 unasserted, meaning essentially it's not being
20 communicated, when it has the value of one.

21 So to avoid confusion between it being
22 there and it not being there, we talked about it
23 being asserted when it's there, even if that's a
24 zero voltage.

25 Q. So am I correct that in the context of

1 DDR2, a read or a write command is really defined
2 by the states of various -- including CAS --

3 A. I'm sorry. I didn't hear the entire
4 question. Sorry about that.

5 Q. I'll restate.

6 There are various states that
7 collectively define commands such as read or write
8 in the context of DDR2; correct?

9 MR. CHANDLER: Objection. Form.

10 THE WITNESS: What do you mean by
11 "read" -- I'm sorry. What do you mean by
12 "states"?

13 BY MR. WARRICK:

14 Q. Maybe it would help if we go to Exhibit
15 1064, which is the JEDEC DDR2 specification.

16 A. Yes.

17 Q. If we go to page 49, that's -- Table 10
18 is a "Command truth table"?

19 A. Yes.

20 Q. And, for example, NOTE 1 of Table 10
21 says, "All DDR2 SDRAM commands are defined by
22 states of CS, RAS, CAS, WE and CKE..."?

23 A. Yes. That's not a -- not a conventional
24 use of the word "states," but it is understandable
25 by a person of ordinary skill in the art.

1 Q. And it's that collection of states, as
2 described in Table 10, anyway, that define the
3 read and write commands; correct?

4 A. It defines the presence of a read or
5 write command, yes.

6 Q. So a CAS signal alone does not cause a
7 column access operation; correct?

8 MR. CHANDLER: Object to form.

9 THE WITNESS: Well, I believe it may
10 cause a column access but not necessarily a
11 read or a write.

12 I guess in the case of the extended mode
13 register set operation, then there's probably
14 no column access. That's probably a special
15 case.

16 BY MR. WARRICK:

17 Q. But a CAS state alone does not trigger a
18 read or write operation; correct?

19 MR. CHANDLER: Objection. Form.

20 THE WITNESS: Not alone. It requires
21 certain other signals to have certain other
22 values.

23 BY MR. WARRICK:

24 Q. So what I want to make sure I understand
25 is that in an earlier answer, you were describing

1 your understanding of these CAS latency terms in
2 the '417 and '215 patents either for a memory
3 device or for the module as a whole. And in that
4 answer, you were referring to the timing of the
5 CAS assertion.

6 And I'm trying to understand what you
7 mean by that; if you're saying that the CAS
8 latency timing begins when the CAS state first
9 takes on a particular value. Is that what you're
10 saying?

11 A. Well, in the first place, "CAS latency"
12 is defined for each memory technology; right?
13 There's not a single definition that applies
14 across the industry, and it's just been sloppily
15 claimed.

16 But if we do our best to understand what
17 it means and assume that it refers to the common
18 technologies of the day, the CAS latency is
19 exactly the way I defined it for transactions that
20 are properly formed.

21 If you misform a read or a write
22 operation, which means that they are not really a
23 read operation -- write operation, and assert CAS,
24 then the data will not be returned.

25 Q. If you could look specifically at Claim 1

1 of the '417 patent.

2 A. Okay.

3 Q. The end of Claim 1 of the '417 patent
4 states:

5 "...wherein data transfers through the
6 circuitry are registered for an amount of
7 time delay such that the overall CAS latency
8 of the memory module is greater than an
9 actual operational CAS latency of each of the
10 memory devices."

11 Do you see that?

12 A. Yes.

13 Q. What's your understanding of data
14 transfers through the circuitry being registered
15 for an amount of time delay?

16 A. So I think that this is intended to talk
17 about a clocked system. That's why things are
18 being registered. "Registered" means being stored
19 in a register, stored in a -- in a data storage
20 element. And the amount of time delay in the
21 context of -- of a registered system, the most
22 reasonable interpretation of that would be that it
23 would be some number of clock cycles, one or more.

24 And what it's saying is that if you delay
25 the response of the memory module by one or more

1 cycles over and above the response time of the
2 chip, then the CAS latency, which is a descriptor
3 of the response delay, would increase by that same
4 amount.

5 Q. When you say the "CAS latency" would
6 increase by the same amount, you're referring to
7 the CAS latency of the memory module; correct?

8 A. Correct.

9 So if there is a delay -- a time delay
10 between the memory device response and the memory
11 module response, then the CAS latency of the
12 module will be greater than the amount of that
13 delay in the CAS latency of the device. I mean,
14 it's almost a tautology.

15 Q. Does Perego, in your view, disclose
16 registering data transfers for this type of time
17 delay such that one or more clock cycles are being
18 added to the CAS latency of the module?

19 MR. CHANDLER: Object to form.

20 THE WITNESS: I think it does. Perego
21 discloses that its data output is registered.
22 And a person of ordinary skill would
23 understand that when you delay the output
24 from a device or from a system by registering
25 it, you need to increase any descriptors of

1 that delay by the amount of the delay. You
2 can't delay something and not have it be
3 delayed.

4 BY MR. WARRICK:

5 Q. Am I to understand you correctly, that by
6 registering the output, you are necessarily
7 delaying the output?

8 A. When you register it in the ordinary
9 manner, where it is going to exit the register in
10 a subsequent clock to when it enters the register,
11 which is what would ordinarily happen and what is
12 described in Perego, you are necessarily delaying
13 it with respect to the non-registered alternative.

14 Q. I assume, Dr. Wolfe, that you're familiar
15 with what a latch is?

16 A. Yes.

17 Q. How is a latch different from a register?

18 A. A latch can be used with different
19 clocking structures. And with a latch, rather
20 than delaying -- well, I shouldn't say that.

21 Rather than delaying the output from a
22 full -- by a full clock cycle, you can merely
23 delay by a propagation delay, which could be less
24 than a full clock cycle, and then you retain that
25 value.

1 Q. And when you were describing Perego
2 earlier, you were talking about a register as
3 distinct from a latch; is that right?

4 MR. CHANDLER: Objection. Form.

5 THE WITNESS: Yes. I think that that's a
6 disclosed embodiment. And because there's no
7 disclosure in Perego of slowing down the
8 clock or anything like that. And if you had
9 a latch, in Perego's system, you would need
10 to slow it down.

11 So I think that whether or not Perego
12 explicitly describes using a register, it can
13 use -- it would be obvious to a person of
14 ordinary skill to build a registered DIMM
15 using Perego's technique in order to maintain
16 the data rate, especially in the context of a
17 DDR2 implementation.

18 BY MR. WARRICK:

19 Q. Right.

20 So that would be different than being
21 expressly disclosed in Perego; right?

22 MR. CHANDLER: Objection to form.

23 BY MR. WARRICK:

24 Q. Let me restate.

25 Dr. Wolfe, Perego does not expressly

1 disclose registering the data output as distinct
2 from using latches; correct?

3 MR. CHANDLER: Object to form.

4 THE WITNESS: Not explicitly. But what
5 it does describe is generating clocks, clock
6 alignment, to use the latches in a way so
7 there is still a delay in the way that there
8 wouldn't be with a register. And that's why
9 it would be obvious to a person of ordinary
10 skill to use a register, as well.

11 BY MR. WARRICK:

12 Q. If we look at Figure 5C of Perego, do you
13 see there are a series of boxes labeled 597f
14 through 597m?

15 Do you see those?

16 A. I do.

17 Q. And towards the bottom of Column 17 of
18 Perego, it's describing Figure 5C, and it
19 references Output Latches 597f through m?

20 A. Correct.

21 Q. So that we are on the same page, 597f
22 through m in Figure 5C of Perego are latches;
23 correct?

24 A. They are. In that embodiment, they are
25 latches.

1 Q. And it's data that's flowing through
2 those latches; correct?

3 A. In those embodiments, that's correct. Of
4 course, in a DDR2 embodiment, you would also have
5 to deal with strobes, which would not be able to
6 be latched.

7 Q. And just to be clear, Perego itself does
8 not expressly disclose adding an additional clock
9 cycle such that the CAS latency of the module is
10 greater than the CAS latency of the individual
11 memory devices; correct?

12 MR. CHANDLER: Object to form.

13 THE WITNESS: It's not that narrow, but
14 it shows adding the latches, which would add
15 a delay. When you're adding a delay, you
16 either have to have the same number of clock
17 cycles with each clock cycle being longer;
18 that would increase the CAS latency; or you
19 have to have more clock cycles with them
20 being the same size; that would also increase
21 the CAS latency.

22 BY MR. WARRICK:

23 Q. And what about Exhibit 1064, the JEDEC
24 DDR2 specification, does that expressly disclose
25 adding additional clock cycle?

1 A. It discloses the timing in such a way
2 that a person of ordinary skill in the art would
3 know that you either need to -- if you add delay
4 to a memory device -- again, 1064 is just a device
5 specification. It's not the module specification.

6 But if you read this in -- if you read
7 this in conjunction with the module specification,
8 what you'll see is that you can't simply add
9 delay; that if you are going to have to add delay,
10 you would have to use a registered module, which
11 would need a longer CAS; or you would need to slow
12 down the clock cycle, as is shown on page 64,
13 where it shows the various timings; and there, you
14 can keep the number of clock cycles.

15 So for example, it shows that if you run
16 something at 533 rates, you might have a CAS
17 latency of 3, with each cycle being longer; or if
18 you ran a chip at 667 rates, the CAS latency might
19 be 4, with each being shorter.

20 But in either case, you've got to have a
21 certain amount of time involved in order for the
22 device to work.

23 Q. You mentioned a registered module, but
24 isn't it correct that a JEDEC-registered DIMM does
25 not add any delay to the data path?

1 A. I don't think that's true. I think
2 that -- I don't think you can build a registered
3 DIMM that responds in the same amount of time as
4 the underlying memory chip. That just doesn't
5 seem possible. It may be documented in different
6 ways. It may be that the memory controller,
7 knowing that it's using a registered DIMM, adds
8 that extra clock of latency on its own, but the
9 latency is still there.

10 Q. But a JEDEC-registered DIMM only delays
11 the control and address path, which are separate
12 from the data path; correct?

13 A. It depends which JEDEC standards you're
14 looking at. If you're looking at, for example, a
15 fully buffered DIMM, it does both.

16 Q. You referenced a module specification a
17 minute ago.

18 A. Yes.

19 Q. Were you referencing a particular module
20 specification?

21 A. No. Depending on what kind of module you
22 wanted to build, you would pick the right module
23 specification. There have been several of them, I
24 believe, with each generation of -- of DIMM.

25 Q. Exhibit 1064, which is the JEDEC DDR2

1 SDRAM specification, that's not a module
2 specification; correct?

3 MR. CHANDLER: Objection. Form.

4 THE WITNESS: Exhibit 1064 is a device
5 specification.

6 BY MR. WARRICK:

7 Q. And a device specification is distinct
8 from a module specification; correct?

9 MR. CHANDLER: Object to form.

10 THE WITNESS: In the JEDEC form, although
11 there is data in a device specification that
12 would be informative to a module designer.

13 BY MR. WARRICK:

14 Q. And what is the JEDEC specification for a
15 DDR2 module?

16 A. As I said, I believe there are a variety
17 of them.

18 Q. Are any of them referenced in the Perego
19 reference?

20 A. I don't recall. Let me look.

21 There are several of them in the IDS.

22 Q. Can you give me an example, please.

23 A. I see JEDEC Standard 21C, and I also see
24 the JEDEC FB-DIMM specification.

25 Q. Now, earlier, another concept you

1 referenced from one of your answers was a fully
2 buffered DIMM?

3 A. Yes.

4 Q. Did those exist at the time of the
5 priority date for the '417 patent?

6 MR. CHANDLER: Objection. Form.

7 THE WITNESS: I don't know. I'm familiar
8 with the specification being published in
9 2006, but I don't know when they were first
10 known in the industry.

11 BY MR. WARRICK:

12 Q. Does your declaration in the '417 patent
13 IPR reference fully buffered DIMMs?

14 A. No.

15 Q. Does your declaration in connection with
16 the '215 patent IPR reference fully buffered
17 DIMMs?

18 A. I don't see a reference right now.

19 Q. Okay. I'm on the East Coast, but I
20 know -- I understand you're on the West Coast; so
21 it's probably getting close to lunchtime for some
22 folks. We could either break now, or I could go
23 for another five or ten minutes.

24 Dr. Wolfe, what's your preference?

25 A. Another five or ten minutes is fine.

1 Q. Okay. Are you familiar, Dr. Wolfe, with
2 the concept of additive latency?

3 A. Yes. But again, each generation has a
4 slightly different definition.

5 Q. Well, so, I mean, for example, we could
6 look at Exhibit 1064, the DDR2 spec.

7 A. Yes.

8 Q. And if we look at page 14, there's a
9 reference to "Additive Latency" there in the
10 figure.

11 A. There is.

12 Q. Do you have an understanding of what
13 additive latency is in the context of DDR2?

14 A. Generally. I've only had to understand
15 it to the extent that it's applied to issues that
16 I've been interested in. And, of course, these
17 are very complicated specifications, but I think I
18 understand at least most of what it does.

19 Q. Is it correct that additive latency is a
20 subset of the operational CAS latency of each
21 memory device?

22 A. Depends what you mean by "operational CAS
23 latency." In DDR2, for ordinary read and write
24 operations, the read latency is calculated based
25 on the CAS latency plus the additive latency.

1 The write operation -- the write latency
2 is calculated based on the additive latency plus
3 the CAS latency minus an offset.

4 I believe there are other less common
5 functions in which the CAS latency is used without
6 the additive latency. And of course, the additive
7 latency can always be set to zero and, in fact,
8 commonly is, in which case it's irrelevant.

9 Q. Understood.

10 But my question is: To the extent there
11 is a non-zero additive latency, that is a subset
12 of the memory device CAS latency; correct?

13 MR. CHANDLER: Objection to form.

14 THE WITNESS: No, it's not correct. The
15 previous explanation is how it works.

16 BY MR. WARRICK:

17 Q. Well, in your answer that you're
18 referencing, you distinguish between CAS latency
19 for reads and writes; correct?

20 MR. CHANDLER: Objection to form.

21 THE WITNESS: No, I don't think I did.

22 BY MR. WARRICK:

23 Q. So in your prior answer, you referenced
24 read latency and write latency as two distinct
25 concepts; correct?

1 A. Two distinct values that are specified in
2 Exhibit 1064.

3 Q. So your understanding of the read latency
4 is the CAS latency plus the additive latency; is
5 that right?

6 MR. CHANDLER: Object to form.

7 THE WITNESS: That's how it's defined in
8 Exhibit 1064 for ordinary read operations.

9 BY MR. WARRICK:

10 Q. And that is the read latency of the DDR2
11 memory device; correct?

12 A. Correct. Exhibit 1064 is a specification
13 for a DDR2 memory device.

14 Q. And based on your prior answer, the write
15 latency is the additive latency plus the CAS
16 latency minus an offset; is that right?

17 MR. CHANDLER: Object to form.

18 THE WITNESS: That is correct for the
19 memories described in Exhibit 1064 with
20 respect to an ordinary write operation.

21 BY MR. WARRICK:

22 Q. So in the context of DDR2, which was
23 described in Exhibit 1064, that write latency is
24 the write latency of the DDR2 memory device;
25 correct?

1 A. The write latency defined in Exhibit 1064
2 is the write latency of a particular DDR2 memory
3 device.

4 MR. WARRICK: I think I'm at a good
5 stopping point there. So if it's fine with
6 everyone, we can take a break. I'm flexible
7 on timing.

8 Dr. Wolfe, do you have a preference?

9 THE WITNESS: 40, 45 minutes would be
10 good.

11 MR. WARRICK: 45 minutes is fine if that
12 works for everyone else.

13 MR. CHANDLER: Okay. So 1:10 p.m.

14 (Short break taken.)

15 BY MR. WARRICK:

16 Q. All right. Dr. Wolfe, welcome back.

17 Before we took a break, we were talking
18 about CAS latency, and I would like to circle back
19 to that for a few questions more.

20 We talked about the fact that the '417
21 and '215 patent claims include this phrase [as
22 read]: "Actual operational CAS latency of a
23 memory device."

24 And I don't know that we had a clear
25 answer from you as to whether you have a view on

1 the meaning of that particular phrase.

2 A. Clearly, it refers to the CAS latency of
3 a memory device independently of whether or not
4 it's been used an a memory module or any
5 particular type of module. As we discussed
6 before, it's somewhat awkward in that it kind of
7 makes an assumption that there's a single CAS
8 latency.

9 But other than that, I've simply assumed
10 for purposes of my opinions that it refers to the
11 documented CAS latency of the particular memory
12 device that one would use in an implementation.

13 Q. So for a read operation, for example,
14 under your understanding, would the actual
15 operational CAS latency of a memory device include
16 the additive latency plus the CAS latency?

17 A. I wouldn't read it that way since there's
18 no discussion of additive latency in the -- in the
19 '417 patent. But since the additive latency can
20 be zero, and often is, in some cases, they could
21 be the same.

22 Q. And did I understand you correctly
23 earlier today that read latency is the delay
24 between when the memory device receives a read
25 command and when it outputs the requested data?

1 A. In DDR2 memory devices compliant with
2 Exhibit 1064, read latency is the number of clocks
3 between the provision of the CAS signal assertion
4 to the memory device and the beginning of
5 providing data in response to that CAS signal.

6 Q. Okay. So let's shift gears a little bit.
7 So I want to stick with Perego, though. So if we
8 could turn to that. And let's start at Figure 5A
9 in Perego, Exhibit 1071.

10 A. Okay.

11 Q. And what does Figure 5A represent?

12 A. A block diagram of a buffer device
13 according to another embodiment of the present
14 invention.

15 Q. And you see a box within 5A labeled 560?

16 A. Yes.

17 Q. And it's also labeled "OPTIONAL DATA
18 CACHE & TAGS"; correct?

19 A. Yes.

20 Q. How does the cache, if it is present,
21 affect the operation of the module?

22 A. Well, I didn't have to consider that
23 since it's optional. So it's taught as being
24 either present or not present. So I did not
25 analyze that particular case.

1 Q. If you look at Column 12, lines 4 through
2 9 of Perego, it indicates that, "Employing a cache
3 560 may improve memory access time by providing
4 storage of most frequently referenced data and
5 associated tag addresses with lower access latency
6 characteristics than those of the memory devices."

7 A. I see that.

8 Q. And if that's true, how would the
9 presence of such a cache affect the operation of
10 the Perego memory module?

11 MR. CHANDLER: Objection to form.

12 THE WITNESS: Again, Perego discloses
13 embodiments without a cache, and that's what
14 I relied on. But if a cache were present,
15 then it's possible that some portion of
16 memory reads and writes could be directed to
17 the cache rather than the memory devices.

18 BY MR. WARRICK:

19 Q. So when there's a read request, for
20 example, the data can come from either the memory
21 devices or it could come from this data cache;
22 correct?

23 MR. CHANDLER: Objection to form.

24 THE WITNESS: In certain embodiments that
25 I did not rely on, that's correct.

1 BY MR. WARRICK:

2 Q. In Figure 5A, within 560, there's another
3 box labeled 565?

4 A. Correct.

5 Q. Do you know what that is?

6 A. Computation Block 565. And it's rather
7 broad as to what it can comprise. Again, it's
8 optional.

9 Q. And there's also a Box 550 labeled "WRITE
10 BUFFER" in Figure 5A of Perego?

11 A. I see that.

12 Q. And if you look at Column 12, roughly
13 lines 9 through 12, there's some description of
14 that?

15 A. Yes.

16 Q. Or 12 through 19 -- or 9 through 12. I'm
17 sorry. Or no --

18 A. This section goes through 19.

19 Q. Yes. Thank you. I'm sorry. I misspoke.
20 Referencing that discussion in Column 12,
21 how does the write buffer affect the operation of
22 the module?

23 A. The write buffer is described here as an
24 ordinary write buffer, as was known in the prior
25 art. It is also optional. It is only present in

1 certain embodiments.

2 But if it was present, it would have the
3 capability to, at times, defer writing certain
4 data into memory until a later time.

5 Q. Does Perego say the write buffer is
6 optional?

7 A. He says it's only in some embodiments.
8 So that would mean that it's not in all
9 embodiments.

10 Q. Going back to the data cache, 560, is it
11 correct that if in response to a read request, the
12 data is delivered from the cache rather than the
13 memory devices, it will be delivered sooner than
14 if it had come from the memory devices?

15 MR. CHANDLER: Objection. Form.

16 THE WITNESS: Again, the cache is
17 optional. It's not the embodiment that I
18 relied on.

19 If that were the case, again, it would
20 depend on design details. But presumably one
21 would only use the cache if it returned data
22 sooner than the memory devices. It would be
23 a special case, again, in that optional
24 configuration.

25 ///

1 BY MR. WARRICK:

2 Q. All right. Could we -- could you turn,
3 please, Dr. Wolfe, to Exhibit 1062.

4 A. Sure. That's the '417?

5 Q. Yes. Well, I believe it's actually the
6 same exhibit in both IPRs.

7 A. Okay.

8 Q. And you recognize that document?

9 A. Yes.

10 Q. What's Exhibit 1062?

11 A. Exhibit 1062 is the registered DIMM
12 specification for DDR not DDR2 memories.

13 Q. And you're familiar with this
14 specification?

15 A. Generally. It's got thousands of
16 parameters. I don't know them all. But I have
17 used it before.

18 Q. And you cited it in your declarations;
19 correct?

20 A. Yes.

21 Q. Do any of the modules disclosed in this
22 specification include a cache?

23 A. In the same manner as in Perego?

24 Q. Well, I guess we could start with at all,
25 first.

1 A. The way that a person of ordinary skill
2 would normally define a "cache," no.

3 Q. And do any of the modules disclosed in
4 Exhibit 1062 disclose a cache that is similar to
5 the one disclosed in Perego in Figure 5A?

6 A. No. Again, I think that's why Perego
7 makes it optional, is that would have been unusual
8 to include it on a memory module at that time.

9 Q. Do any of the modules disclosed in
10 Exhibit 1062 include a write buffer?

11 A. Not that I'm aware of. Again, by the
12 time of Exhibit 1062, although it was known to put
13 a cache or a write buffer on a memory module, it
14 was not very efficient to do it that way.

15 So that's, again, that's why I believe
16 Perego made it optional; both the cache and the
17 write buffer, by 2002, would most commonly be
18 placed closer to the processor than the memory
19 module.

20 Q. What about a computational engine? Any
21 of the modules in Exhibit 1062 disclose that?

22 A. No. Again, that's probably why it's
23 optional in Perego, is that it would have been
24 unusual.

25 Q. In Exhibit 1062, the JEDEC specification,

1 is it correct that the delay in cycles between a
2 column access command and the data is fixed based
3 on the particulars of the DRAMs present on the
4 module?

5 MR. CHANDLER: Objection. Form.

6 THE WITNESS: It is fixed based on the
7 DRAM -- well, no, that's not the case. It
8 depends what speed you're running the device
9 at.

10 BY MR. WARRICK:

11 Q. For any given speed is that a true
12 statement?

13 MR. CHANDLER: Objection. Form.

14 THE WITNESS: No. I believe it's still
15 configurable.

16 BY MR. WARRICK:

17 Q. And how would you configure that within
18 the context of Exhibit 1062?

19 A. I don't have the DDR memory spec in front
20 of me, but I believe that there was a
21 configuration register that would be programmable
22 on each of the devices.

23 Q. So is it your view that according to the
24 JEDEC spec there can be variability in the timing
25 of data relative to the commands?

1 MR. CHANDLER: Objection. Form.

2 THE WITNESS: I'm not sure what you mean
3 by "variability," but not every system needs
4 to set the cache latency for particular
5 devices the same way.

6 BY MR. WARRICK:

7 Q. Well, you used the word "configurability"
8 earlier.

9 Maybe a better question is: In your
10 view, there's configurability within the timing of
11 the data relative to the commands in the modules
12 defined in Exhibit 1062?

13 MR. CHANDLER: Objection. Form.

14 THE WITNESS: Yes, they can be
15 configured.

16 BY MR. WARRICK:

17 Q. Is it correct that in the modules defined
18 in Exhibit 1062, the memory controller will know
19 when read data will be returned to it?

20 MR. CHANDLER: Objection. Form.

21 THE WITNESS: In operation it will, yes.

22 BY MR. WARRICK:

23 Q. Is it fair to say the controller is in
24 complete command of the module in terms of the
25 timing?

1 MR. CHANDLER: Objection. Objection to
2 form.

3 THE WITNESS: No. I think that's a
4 stretch. I think that it would be
5 compatible. Because the module is compliant
6 with a standard, it would be able to predict
7 the behavior of the module once the module
8 has been configured.

9 BY MR. WARRICK:

10 Q. So in the Perego embodiments that include
11 the data cache, they are very different than the
12 JEDEC modules defined in the specification of
13 Exhibit 1062; correct?

14 A. Well, I didn't rely on the embodiments
15 that include the data cache. It's optional. I
16 wouldn't say they were very different. I would
17 say they have an additional feature that's not
18 present in 1062 if the optional data cache is --
19 is included in Perego.

20 But it need not be.

21 Q. And we can look at Figure 5B of Perego.
22 And you see, you have the Interface 596
23 towards the bottom of Figure 5B?

24 A. I see that.

25 Q. Is there any indication that the

1 character or capabilities of that Memory Bus
2 Interface 596 or the memory bus depend on whether
3 or not the cache is present?

4 A. I don't recall Perego being specific
5 about it one way or the other.

6 Again, Perego's very open-ended in
7 explaining that all kind of memory interfaces can
8 be used there, including standard memory
9 interfaces.

10 Q. Well, let me ask this: In embodiments of
11 Perego that do include the data cache, in the
12 circumstance where there is a cache hit, it's
13 correct that the data will be returned more
14 quickly than the memory controller would expect,
15 compared to a module that does not have such a
16 cache?

17 MR. CHANDLER: Objection. Form.

18 THE WITNESS: One would expect that if
19 someone chose to use a data cache -- which,
20 again, I did not rely on any embodiments with
21 the data cache on the memory module. But if
22 one chose to use that embodiment, presumably
23 one would choose to use an interface that
24 could receive the results back at different
25 times, because there would be no point in

1 using an optional data cache unless one could
2 take advantage of the improved speed.

3 So one would choose, in that particular
4 circumstance, a host interface that could
5 recognize that particular situation.

6 BY MR. WARRICK:

7 Q. And just so we're clear, the write
8 buffer, unlike the data cache of Perego, is not an
9 optional feature; correct?

10 MR. CHANDLER: Objection. Form.

11 THE WITNESS: It clearly is, because
12 Perego teaches that some embodiments have the
13 write buffer and other embodiments don't.

14 BY MR. WARRICK:

15 Q. The write buffer, however, is not
16 described as optional in the context of the
17 embodiments of Figures 5A or Figure B of Perego;
18 correct?

19 A. I think it is. The patent refers you to
20 those figures and then says that in some
21 embodiments the write buffer is present. It
22 doesn't say embodiments other than 5A and 5B. I
23 think a person of ordinary skill would understand
24 that as being a completely optional feature.

25 And even if Perego hadn't stated it, a

1 person of ordinary skill in the art would
2 understand that in this particular environment, a
3 write buffer would be optional.

4 Q. You would agree at minimum, though, that
5 the Write Buffer 550 in Figure 5A is not labeled
6 as optional in the same manner as Data Cache 560;
7 correct?

8 MR. CHANDLER: Object to form.

9 THE WITNESS: It's not labeled that way
10 on the drawing. It doesn't say the word
11 "optional." It's a smaller box. But it's
12 clear from the text that it is optional and
13 that the signals to it are optional. They
14 are actually even described as optional.

15 BY MR. WARRICK:

16 Q. Let's talk about the '215 patent, if we
17 could. That is Exhibit 1001 from the '215
18 patent's IPR.

19 A. Okay.

20 Q. And if we look at Claim 1 of the '215
21 patent, you'll see one of the elements begins
22 with:

23 "A register coupled to the print -- to
24 the printed circuit board and configured to
25 receive and buffer first command and address

1 signals."

2 Do you see that?

3 A. I see that.

4 Q. Now, Perego does not disclose this
5 register in Claim 1 of the '215 patent, does it?

6 A. I think a person of ordinary skill would
7 understand Buffer Device 350 to include a
8 register.

9 Q. Did you express that view in your
10 declaration for the '215 patent IPR?

11 A. Yes. Paragraphs 251, 252.

12 All the way through somewhere around 255
13 or 256.

14 Q. Can you point me to where you
15 specifically offer the view that the Buffer 350
16 from Perego includes a register.

17 A. Paragraph 251. "Perego discloses that a
18 'register' in its buffer device (e.g., 350) is
19 coupled to the printed circuit board..."

20 And then it goes on from there.

21 And then in particular, at the end of
22 paragraph 254, I quote the portion of Perego where
23 it explains that [as read]:

24 "...buffers disposed on conventional
25 DIMM modules are employed to buffer or

1 register control signals or address
2 signals.'"

3 Q. Is there a difference, in your view,
4 between a buffer and a register?

5 A. There can be in different contexts. But
6 I believe in this context, especially in light of
7 Perego's disclosure in Column 6, that he is
8 expressing the view that his buffer can be a
9 register.

10 Q. Turning back to Perego, we discussed the
11 fact earlier that Perego describes a configurable
12 width module; correct?

13 A. Right. Perego does describe that some of
14 his embodiments have configurable width modules
15 that can be configured in various ways.

16 Q. Can you have a configurable bit width
17 module that is compliant with JEDEC
18 specifications?

19 A. I would think so, because if you read
20 Perego, he indicates that one of the ways of
21 configuring it is to have a resistor or a jumper
22 that's installed at manufacture time that
23 configures it to a fixed bit width. In that case,
24 I think it can certainly be JEDEC compliant.

25 Q. Well, in that case, if you have something

1 that's constraining an embodiment of Perego to a
2 fixed bit width, it's no longer a configurable bit
3 width module; correct?

4 MR. CHANDLER: Objection. Form.

5 THE WITNESS: It's a matter of semantics.
6 You know, I mean, it's what Perego calls a
7 variable -- a configurable bit width module.

8 But I would agree that once it's been
9 configured, especially if it's been
10 configured at manufacturing time, then a
11 reasonable person might no longer treat it as
12 configurable. But that's exactly what's
13 described in Column 16 of Perego.

14 BY MR. WARRICK:

15 Q. Are you aware of any JEDEC-compliant
16 memory modules that have configurable bit width?

17 A. I can't point you to one off the top of
18 my head, but I'm quite certain they are out there.
19 I'm also completely certain that they are out
20 there.

21 For example, there are modules that --
22 that work at 64 or 72 bits.

23 Q. And in that particular context, is that a
24 function of whether or not error correction is
25 being employed?

1 A. In many cases, that would be the reason
2 but not necessarily.

3 Q. We discussed earlier that some of the
4 figures in Perego depict what you would describe,
5 I believe, as a well-known Rambus memory bus; is
6 that right?

7 MR. CHANDLER: Objection. Form.

8 THE WITNESS: Yes. That would be my
9 understanding.

10 BY MR. WARRICK:

11 Q. And a Rambus bus is very different than a
12 JEDEC SDRAM bus; correct?

13 MR. CHANDLER: Objection. Form.

14 THE WITNESS: Depends what you mean by
15 "very different."

16 My recollection is that Rambus thought
17 there were enough similarities to file a few
18 dozen lawsuits.

19 BY MR. WARRICK:

20 Q. Do you view a Rambus bus and a JEDEC
21 SDRAM bus as similar?

22 A. Again, I haven't tried to do that
23 comparison, but my understanding is there are some
24 features that are quite similar and some features
25 that are quite different.

1 Q. Is it true a Rambus bus is generally
2 narrower than a JEDEC bus?

3 A. Debatable. A number of people would say
4 that's why it failed; that in practice, in order
5 to get equivalent performance, by the time you set
6 up multiple channels of Rambus memory in a device,
7 you would typically have the same number of wires
8 as if you set up a single, wider DDR bus. It's
9 just a question of the details of how those wires
10 are behaving.

11 Q. A Rambus uses a packet protocol, doesn't
12 it?

13 MR. CHANDLER: Objection to form.

14 THE WITNESS: A direct Rambus certainly
15 used a packet protocol for certain functions,
16 as did the later fully buffered modules in
17 DDR.

18 BY MR. WARRICK:

19 Q. The DDR and DDR2 specifications we've
20 looked at today, however, do not include a packet
21 protocol; correct?

22 A. Depends how you define a "packet
23 protocol." There certainly are packetized bursts
24 of data that are sent, but it's not packetized
25 control or address protocol in the same way as

1 Rambus.

2 Again, I think that's why Perego made it
3 clear that there were various kinds of memory that
4 would work with his invention.

5 Q. So I don't know if this is what you're
6 referring to, but Column 8, lines 1 through 9, of
7 Perego mentions several different types of memory
8 devices and claims that those could be used within
9 the modules it discloses.

10 A. More specifically within the described
11 embodiments.

12 Q. So for example, Column 8 of Perego
13 mentions DDR. It also mentions XDR, SRAM, FRAM,
14 MRAM, Flash, ROM.

15 Those various types of memory devices are
16 not freely interchangeable, are they?

17 A. Depends what you mean by "freely
18 interchangeable." You cannot remove one and
19 replace it with another in certain cases, but a
20 person of ordinary skill would know how to
21 redesign an interface using routine methods to
22 replace one with another; and they are all
23 designed to speak to a microprocessor.

24 Q. And we discussed earlier that in Perego,
25 if you were to use JEDEC-compliant DDR2 memory

1 devices, you would, in fact, have to modify other
2 parts of the memory module to make it work;
3 correct?

4 MR. CHANDLER: Object to form.

5 THE WITNESS: Yes. You would need to
6 make modifications at the detail level that
7 are routine within the industry.

8 BY MR. WARRICK:

9 Q. When you say "routine within the
10 industry," are you referring to others who have
11 modified a Rambus bus module to use JEDEC SDRAM
12 memory devices?

13 A. No. Because, again, Perego tells us that
14 his embodiments are compatible with DDR. A person
15 of ordinary skill would know how to build a memory
16 interface for a variety of different known memory
17 types by following the specifications.

18 And there's no reason, in view of Perego,
19 why they would necessarily need to use a
20 Rambus-compatible memory interface. Perego
21 teaches that the interface need not be a
22 Rambus-compliant interface, either.

23 So a person of ordinary skill would be
24 fluent in designing memory controllers and memory
25 interfaces and would be able to take the teachings

1 of Perego and use them for at least any of the
2 recited types of memory.

3 Q. Well, I believe you stated earlier that
4 in order to use DDR2 devices with Perego, you
5 would you need to make changes to the interface,
6 as well as the buffer device of Perego; is that
7 right?

8 A. No. If that's what I said, I
9 misunderstood the question.

10 I thought you asked me, if one were to
11 take a Perego embodiment that used Rambus and
12 replace that with DDR, would you need to make
13 changes? In that case, you would need to make
14 some changes, but they are changes that are
15 routine.

16 You could not implement Perego using
17 Rambus without looking up the Rambus spec, and you
18 could not implement Perego with DDR or DDR2
19 without looking up the corresponding specs.
20 There's too much detail to be able to do it
21 without using the public specifications.

22 Q. So I think I understand your view that
23 someone of ordinary skill in the art would be able
24 to construct either a Rambus interface or a
25 JEDEC-style interface and that that would be

1 routine.

2 I just want to be clear, are you saying
3 it's also routine to adapt a Rambus interface to
4 work with DDR2 memory devices?

5 A. I don't think Perego requires that in any
6 way, but I think Perego teaches it. So together
7 with the teachings of Perego, I think it would be
8 routine.

9 Q. Are you aware of anyone doing that?

10 A. Well, it only would have been interesting
11 in 2006. So I don't recall whether anybody did it
12 back then. Maybe even earlier, starting in maybe
13 '99 through 2007. I don't recall whether or not
14 anybody did it then, but --

15 Q. You're not aware of anyone?

16 A. Not off the top of my head. But again,
17 that would have -- that would have been primarily
18 for economic reasons that DDR memory was just
19 cheaper. And most manufacturers, particularly PC
20 manufacturers, would -- would provide you your
21 choice of a Rambus or DDR memory controller.

22 Q. If we started with one of the Rambus
23 modules of Perego and substituted DDR2 memory
24 devices and then made the changes to the interface
25 and the buffer that you referenced earlier would

1 be necessary, or a working module, what aspects of
2 Perego would be left in such a device?

3 MR. CHANDLER: Objection. Form.

4 THE WITNESS: Well, I'm not sure anybody
5 would ever need to go through that process,
6 because Perego teaches you how to directly
7 implement his -- his invention with a variety
8 of memory types.

9 But if you decided to take Perego and
10 implement it with a non-Rambus memory type,
11 as is taught, you would still have, perhaps,
12 factory configurability. You would have --
13 perhaps have the ability to have a buffer
14 that performs rank multiplication across two
15 different ranks. So there would be a number
16 of advantages.

17 BY MR. WARRICK:

18 Q. Would you still have a configurable width
19 buffer?

20 A. It depends on what time. Again, that's a
21 feature that he teaches. But he also teaches that
22 it can be fixed at manufacturing time.

23 Q. But if you took the Rambus embodiment
24 and, again, substituted the DDR2 memory devices
25 and made the necessary changes to the interface

1 and buffer to work with those devices, would you
2 still have a configurable bit width buffer?

3 A. Well, again, I'm not sure why you would
4 do that rather than applying the teachings of
5 Perego directly to DDR as he suggests.

6 But if you did go through that process, I
7 think you could certainly still have a
8 configurable bit width buffer, because you
9 could -- you could configure it in different ways,
10 as suggested by Perego.

11 I don't know that -- I mean, I haven't
12 relied on that kind of embodiment. I've relied on
13 the embodiment that's taught, in which you would
14 fix the bit width at manufacturing time.

15 Q. Just so we're all on the same page, can
16 you refer me to the particular part of Perego
17 you're referencing when you talk about fixing the
18 bit width at manufacturing time?

19 A. Column 16, lines 53 through 65. It talks
20 about [as read]:

21 "...state storage -- various types of
22 state storage are possible, including but not
23 limited to manual jumpers and switch settings
24 and module presence detection or type
25 detection mechanisms. The latter class may

1 include pull-up or pull-down resistor
2 networks" -- which one would provide at
3 manufacturing time - "tied to a particular
4 logic value (high or low), which may change
5 state when a module is added or removed from
6 the system."

7 And again, that is all permissive
8 language. So it certainly could be fixed as well.

9 Q. And am I understanding you correctly that
10 this embodiment of Perego -- or should I say
11 embodiments of Perego that include this permissive
12 feature of fixing the bit width at manufacturing,
13 those are the only embodiments in Perego on which
14 you rely?

15 MR. CHANDLER: Objection. Form.

16 THE WITNESS: No. I relied on all the
17 teachings of Perego. But certainly Perego
18 talks about embodiments with a serialization
19 ratio of one-to-one, either factory fixed or
20 in operation as configured at run time, and I
21 think either of those would make the '215
22 obvious, and the '417.

23 BY MR. WARRICK:

24 Q. So is it fair to say that you're only
25 relying on Perego embodiments that, in your view,

1 include a fixed width module?

2 MR. CHANDLER: Objection to form.

3 THE WITNESS: I mean, there's 800 pages
4 in the report. We would have to go through
5 and look at every dependent claim.

6 But for the independent claims, the
7 one-to-one operation is enough to make the
8 independent claims obvious.

9 BY MR. WARRICK:

10 Q. I want to go back to the modifications
11 that would be necessary for Perego to utilize DDR2
12 memory devices, which I believe you indicated
13 would be routine, in your view --

14 A. No, that's wrong. I never said it would
15 require modifications to Perego to use DDR2.

16 What you asked me is if you implemented
17 Perego with Rambus first and then switched to
18 DDR2, would you need to make modifications; and
19 you would.

20 But Perego teaches you how to make DDR2
21 embodiments. You would not need to modify Perego
22 to make DDR2 embodiments.

23 Q. So I understand there are portions of
24 Perego that indicate that one could use different
25 types of memory devices. And, for example, we had

1 looked at Column 8 a few minutes ago, which
2 mentioned a lot of those devices.

3 But it's your view that Perego also
4 teaches a person of ordinary skill how to
5 implement a Perego module using DDR2 specifically?

6 A. Yes, based on a person of ordinary skill
7 in the art's existing knowledge of DDR2. Perego
8 is explicit that none of the things that he shows
9 in an exemplary way are limiting. He talks about
10 how you could have point-to-point links or bus
11 topologies. He's clearly not limiting it to an
12 RDRAM. He talks about different kinds of control
13 signals, including individual selects, again,
14 helping someone to understand how they would
15 implement it with a DDR.

16 So as a person of ordinary skill reading
17 this disclosure with Perego's additional
18 disclosures that the features that are
19 Rambus-specific are not limiting, would understand
20 how to apply these concepts in a DDR2
21 implementation, based on what Perego teaches.

22 Q. Well, you would agree that not limiting
23 the scope of what's described in Perego is not the
24 same thing as teaching someone how to construct a
25 particular embodiment for a particular type of

1 memory device; right?

2 MR. CHANDLER: Object to form.

3 THE WITNESS: It's not the same, but it's
4 also not what I said.

5 A person of ordinary skill would already
6 know how to build the individual components
7 that are DDR2-specific, how to build
8 DDR-specific -- -2-specific interface; what
9 DDR2 control signals look like; what DDR2
10 timing looks like.

11 And Perego specifically tells the reader
12 that that's within the scope of this
13 invention. So therefore, when Perego uses an
14 example, the person of ordinary skill would
15 apply that example to their existing
16 knowledge and not try to interpret Perego's
17 example as limiting the embodiments or
18 instructing the reader not to apply that
19 existing knowledge that's already been
20 suggested.

21 BY MR. WARRICK:

22 Q. I apologize if you can hear the noise. I
23 am in Washington, D.C., at our office, and there
24 seems to be some sort of --

25 A. We're not hearing it.

1 MR. CHANDLER: I don't hear. It just
2 you. No protesters.

3 MR. WARRICK: Okay. It's a common event
4 here. It's a hazard of the location.

5 BY MR. WARRICK:

6 Q. Okay. So, Dr. Wolfe, I understand you to
7 be saying that a person of skill would know how to
8 build a system that would work with these
9 different types of memory devices; and that Perego
10 indicates to such a person that any number of
11 memory devices could be used; and that generally,
12 a skilled artisan would know how to construct a
13 system according to Perego that would work with
14 those different types of memory devices.

15 Is that a fair summary?

16 A. I think that's generally correct, yes.

17 Q. But is there anything in Perego that
18 specifically teaches a person of ordinary skill
19 how to implement its modules with DDR2 memory
20 devices specifically?

21 A. Yes. At the level of instruction that a
22 person of ordinary skill needs, simply describing
23 where the interfaces are, what order things happen
24 in, how things are generally interconnected, is
25 enough. It's not necessary for a person of

1 ordinary skill to list out the signals. It's not
2 necessary for Perego to repeat the contents of
3 Exhibit 1064 to a person of ordinary skill,
4 because that's already within their knowledge.

5 Q. Now, Exhibit 1064 is the specification
6 for the memory devices themselves; correct?

7 A. Correct.

8 Q. Not for the JEDEC DIMM?

9 A. No. But they would convey a lot of
10 operational details. There are other JEDEC
11 compliance factors, like pin capacitance and such,
12 that would be specific to some other
13 specification.

14 Q. Well, there are some key aspects of a
15 DDR2 or a DDR-compliant module that are not
16 disclosed in Perego, such as chip select signals;
17 correct?

18 MR. CHANDLER: Objection. Form.

19 THE WITNESS: Well, it does disclose that
20 you can have individual select signals to the
21 individual devices.

22 It also points to DDR, which any person
23 of ordinary skill would understand requires a
24 chip select signal.

25 ///

1 BY MR. WARRICK:

2 Q. But a DDR memory device requires a chip
3 select signal; correct?

4 A. It does. But also, DDR-compliant DIMMs
5 all have chip select signals.

6 Q. And, in fact, they require chip select
7 lines as well; correct?

8 A. DDR-compliant DIMMs do have chip select
9 lines.

10 Q. And those chip select lines are not
11 disclosed in Perego; correct?

12 MR. CHANDLER: Objection. Form.

13 THE WITNESS: It talks about individual
14 module control lines in Column 1, with
15 respect to a conventional memory system. I
16 think it's disclosed there.

17 I think it -- the RQ scroll lines, it
18 says, may comprise individual control lines,
19 including selection lines.

20 And if we look at the figures in Perego,
21 it describes the external connections as RQ
22 lines.

23 So I do think it's disclosed.

24 BY MR. WARRICK:

25 Q. But you would have to agree that chip

1 select lines are not expressly disclosed in
2 Perego; correct?

3 A. It says the control lines RQ can have
4 individual device select lines.

5 As a person of ordinary skill, I would
6 understand those to be chip select lines.

7 MR. CHANDLER: Whenever is convenient.
8 It's been about an hour.

9 MR. WARRICK: Yeah, we can pause here,
10 and maybe this commotion will die down by the
11 time we come back.

12 (Short break taken.)

13 BY MR. WARRICK:

14 Q. Dr. Wolfe, before, we were talking about
15 the teachings of the Perego reference and
16 specifically the possibility of using different
17 types of memory devices with Perego.

18 And we had referenced Column 8, which
19 discloses DDR, along with several other types of
20 memory devices.

21 And I believe it was your opinion that
22 any of those could be used with Perego, in view of
23 the knowledge of the skilled artisan; is that
24 right?

25 A. Yes, in at least some embodiments of

1 Perego; but specifically DDR, which is listed in
2 that first category, along with direct Rambus.

3 Q. Is it the case that even with something
4 like flash memory, that a skilled artisan would be
5 able to incorporate that into Perego as a routine
6 matter?

7 A. Yes. The -- there would be more
8 differences between a flash memory implementation
9 and a Rambus implementation than between a DDR
10 implementation and a Rambus implementation.

11 But this has to all be considered from
12 the perspective of a person of ordinary skill in
13 the art, who, by this time, you know, the art of
14 interfacing memories to microprocessors is
15 certainly more than 30 years old and was quite
16 broad.

17 Q. Before the break, we were talking about
18 chip select signals and chip select lines.

19 And you agree that those are necessary
20 for a DDR2 implementation of Perego; correct?

21 MR. CHANDLER: Objection. Form.

22 THE WITNESS: An implementation of Perego
23 using JEDEC-compliant DDR chips would have
24 chip select lines.

25 ///

1 BY MR. WARRICK:

2 Q. Now, in Perego, I would like to look
3 specifically at Column 10; and Column 10, lines 63
4 through 67. It's at the bottom of Column 10.

5 And Perego says, "Different types of
6 memory devices may be included on different
7 modules within a memory system, by employing
8 buffer device 405 to translate protocols employed
9 by controller 310 to the protocol utilized in a
10 particular memory device implementation."

11 Did I read that correctly?

12 A. I believe so.

13 Q. So is this part of the -- I'll rephrase.

14 Is this the teaching of Perego that you
15 referenced earlier when you discussed Perego
16 teaching the skilled artisan how to incorporate
17 DDR2?

18 A. No. Perego teaches that DDR2 can be used
19 generally, but he also teaches that in some
20 embodiments one can choose a different protocol
21 for the host interface than one does for the
22 individual device interface. It teaches them
23 both.

24 Q. Would you agree this would be a simpler
25 modification of Perego than modifying the entire

1 module to use DDR2?

2 MR. CHANDLER: Objection. Form.

3 THE WITNESS: It's not necessary to
4 modify the module to use DDR2; only to
5 implement it that way, as Perego teaches.

6 BY MR. WARRICK:

7 Q. Is there any disclosure in Perego that
8 teaches you how to perform the translations that
9 are described at the bottom of Column 10?

10 MR. CHANDLER: Objection. Form.

11 THE WITNESS: Not specifically.
12 Translating from one memory protocol to
13 another is not required by Perego, but it
14 would be within the skill of a person of
15 ordinary skill in the art.

16 BY MR. WARRICK:

17 Q. So, in your view, a person of skill in
18 the art could take an incoming signal to the
19 Perego buffer that is not JEDEC-compliant and then
20 translate that into the signals necessary for a
21 DDR2 memory device?

22 MR. CHANDLER: Objection to form.

23 THE WITNESS: A person of ordinary skill
24 in the art could do that, but that's not
25 necessary in order to implement Perego with

1 DDR2.

2 BY MR. WARRICK:

3 Q. But that's what this particular
4 embodiment is describing in Perego; correct?

5 A. That is within the scope of that one
6 particular embodiment discussed in that one
7 particular paragraph.

8 Q. And in that embodiment, the buffer of
9 Perego would not receive chip select signals, for
10 example, from the memory controller; correct?

11 MR. CHANDLER: Object to form.

12 THE WITNESS: I disagree. The Rambus
13 protocol, for example, does include chip
14 select signals. They are simply multiplexed
15 on to the same wires as other signals, in a
16 packetized form.

17 BY MR. WARRICK:

18 Q. Now, Column 9 of Perego talks about
19 "control lines (RQ)."

20 And it says they "...may comprise
21 individual control lines, for example, row
22 address strobe, column address strobe, etc.,
23 and address lines."

24 I believe you referenced that earlier?

25 A. Yes.

1 Q. And Perego, in that context, is referring
2 to the interface between the buffer and the memory
3 devices; correct?

4 A. I don't know -- I don't know why we would
5 assume that. He has two different place where --
6 places where he uses the label "RQ."

7 Q. That same paragraph in Perego discusses
8 the need in some cases to "increase the number of
9 parallel signal connection paths"; correct?

10 A. In some cases, yes.

11 Q. And Perego says that that would increase
12 the "system layout resource requirements"; right?

13 A. With respect to a narrow packet protocol
14 approach, not necessarily with respect to other
15 approaches.

16 Q. Would you agree that system layout
17 resource requirements would be a factor when one
18 is deciding how to implement a memory module?

19 A. It could be a factor. But we know both
20 at that time and prior and subsequently, the vast
21 majority of -- the majority of the market chose to
22 use parallel signal connection paths and not a
23 narrow packet protocol approach.

24 Q. You mentioned earlier that Rambus
25 included chip select signals.

1 Did I read that correctly?

2 A. It does include chip select signals in --
3 in its packetized information. And, in fact,
4 Figure 6A essentially confirms that, if we assume
5 that it can describe a Rambus-like implementation,
6 because we see the packetized information coming
7 in on 620a and then being distributed as chip
8 select signals on 633a and 633b.

9 Q. But Rambus does not include chip select
10 lines; correct?

11 MR. CHANDLER: Objection to form.

12 THE WITNESS: Rambus protocols at that
13 time did not include distinct chip select
14 wires, as far as I know.

15 But at the same time, Columns 9 and 10 do
16 teach that they could be used in that kind of
17 an environment.

18 BY MR. WARRICK:

19 Q. Going back to your proposed claim
20 construction for the term "rank" in the '417 and
21 '215 patents, one thing we didn't discuss earlier
22 specifically is the fact that it includes chip
23 select signals.

24 And specifically, again, your proposed
25 construction is "...an independent set of one

1 or more memory devices on a memory module
2 that act together in response to command
3 signals, including chip select signals, to
4 read or write the full bit-width of the
5 memory module"; correct?

6 A. Yes.

7 Of course, it's important to understand
8 that when we talk about chip select signals, a
9 rank select signal is often called a chip select
10 signal, in practice, in the industry. A chip
11 select signal is not limited to selecting a single
12 chip.

13 Q. So under your construction, for a set of
14 memory devices to constitute a rank, is it
15 necessary for a chip select signal to be applied
16 to all of those devices?

17 A. They all need to know that it's their
18 turn to respond. So there would need to be a chip
19 select signal or some equivalent.

20 Q. And is it correct that all the memory
21 devices within a given rank have to have the same
22 chip select signals applied to them?

23 A. No. They just need corresponding chip
24 select signals. If you replicate a signal or
25 something else similar that tells them all that

1 they need to respond at the same time, they are
2 still a rank.

3 Q. So why -- why are chip select signals a
4 part of your proposed construction for these two
5 patents?

6 A. Again, I'm trying to describe the way
7 the -- the way the word "rank" is ordinarily used
8 in the context of these patents with a memory
9 module.

10 And part of that ordinary meaning with
11 respect to this patent is that the chips respond
12 together or perform a write operation together
13 when they are told it's their turn and not at some
14 random time. So I was trying to describe that.

15 And again, that's consistent with what
16 the '417 patent says.

17 Q. Are you aware of examples where different
18 memory devices within the same rank receive
19 different chip select signals?

20 A. It depends what you mean by "different
21 chip select signals." It's certainly true that
22 when a rank gets large, it is common to replicate
23 the chip select signals so that there are a bunch
24 that all operate at the same time.

25 Q. If you had two groups of memory devices

1 that are supplied with different chip select
2 signals, then those devices would not be
3 considered to be part of the same rank, would
4 they?

5 A. Depends what you mean by "different chip
6 select signals." Certainly, the way that I
7 described before, they would.

8 If they never operate together in
9 response to command signals, then they would not
10 be in the same rank.

11 Q. But, in your view, they would not
12 necessarily have to receive -- I'll rephrase that.

13 In your view, the memory devices within a
14 rank do not necessarily have to receive the same
15 chip select signals in order to be part of the
16 same rank?

17 MR. CHANDLER: Objection to form.

18 THE WITNESS: Again, it depends how
19 you're defining those words. They have to
20 receive corresponding chip select signals so
21 that they know that they are being selected
22 at the same time. But they don't -- there
23 doesn't need to be one physical wire
24 connecting them all. Chip select signal can
25 be replicated.

1 BY MR. WARRICK:

2 Q. And are the replicated chip select
3 signals identical to the original chip select
4 signals?

5 A. They are identical enough for their
6 suited purpose.

7 Q. And so memory devices within a rank would
8 have to receive chip select signals that have at
9 least that degree of identity; correct?

10 A. No. I mean, again, the purpose of the
11 word "rank" is to help a person of ordinary skill
12 identify which devices are in the same rank and
13 which devices are in different ranks.

14 And the ones that are acting together in
15 response to command signals, including chip select
16 signals, to read or write the full bit width of
17 the memory module, are the ones that are in the
18 same rank.

19 And if they are acting together in
20 response to the chip select signals, to read or
21 write the full bit width of the memory module,
22 then they are in the same rank, even if there are
23 tiny differences between copies of the chip select
24 signals.

25 Q. I believe in your declaration for the

1 '417 patent, Dr. Wolfe, you indicated that for
2 Ellsberry, the separate reference, the individual
3 memory devices could receive something different
4 than a chip select signal to indicate whether or
5 not they are participating in a rank; is that
6 fair?

7 MR. CHANDLER: Objection to form.

8 THE WITNESS: The particular portion of
9 my declaration that you're referring to?

10 BY MR. WARRICK:

11 Q. Just a second. I apologize. I think I
12 have a mistake in my notes. Let me ask you more
13 generally, though.

14 For Ellsberry, does Ellsberry include
15 chip select signals?

16 A. I don't recall off the top of my head.
17 I'd have to go through my -- my report.

18 Q. Okay --

19 A. But again, I didn't rely on Ellsberry
20 alone. So I only relied on Ellsberry in
21 combination with Perego and JEDEC, and they both
22 disclose chip select signals.

23 Q. So are you saying you did not rely on
24 Ellsberry for the disclosure of chip select
25 signals?

1 A. No. I just said I don't recall if I also
2 rely on Ellsberry for the disclosure of chip
3 select signals.

4 But they are disclosed in the two base
5 references, as well.

6 Ellsberry is 1073?

7 Q. Correct. And it should be in the Exhibit
8 Share, as well.

9 A. I mean, Ellsberry definitely has chip
10 select signals.

11 Q. And, my question, then, is: Do the chip
12 select signals in Ellsberry play a role in which
13 memory devices participate in a given rank?

14 A. Yes. In Ellsberry alone, that would be
15 true.

16 Q. What about the no-operation function?

17 A. Ellsberry -- Ellsberry also teaches that
18 one can use a no-op command as a rank select.

19 Q. So your understanding is that Ellsberry
20 could use either a chip select or a no-op command
21 for rank selection?

22 A. My understanding is that that's what a
23 person of ordinary skill would understand with
24 respect to Ellsberry.

25 Q. In your declaration, you cited a textbook

1 that describes ranks as including memory devices
2 that operate in lockstep.

3 Do you agree that memory devices within a
4 rank have to operate in lockstep with each other?

5 A. Do you recall the exhibit number?

6 Q. It's in -- if you look at your '417
7 patent declaration at paragraph 128, it references
8 Exhibit 1070.

9 A. I think it was around page 9; is that
10 right?

11 Q. It's page 104, paragraph 128 of the '417.

12 A. The page in the reference -- I want to
13 make sure I get the exact language out of the
14 book -- page 6.

15 Q. So what I'm referencing, if you look at
16 your declaration, it has a quote --

17 A. Oh, page 413.

18 Q. 413 from Exhibit 1070. And you have it
19 quoted in a parenthetical.

20 The quote is, "Essentially a rank of
21 memory is a 'bank' of one or more DRAM devices
22 that operate in lockstep in response to a given
23 command"?

24 A. Right. And that's what's important, if
25 it says, "one or more DRAM devices."

1 So, yes, the "one or more DRAM devices"
2 have to operate in lockstep. But clearly that can
3 be either one or more.

4 Q. So I want to circle back to the "one or
5 more." But, first, operating in lockstep, that is
6 equivalent to the "acting together" portion of
7 your proposed construction of the term "rank"?

8 A. Yes. It does say in "a given command."
9 So my "acting together" is specific to the read
10 and write commands.

11 Q. Understood.

12 Now, in terms of "one or more," does
13 Perego disclose a memory module with only a single
14 memory device per rank?

15 MR. CHANDLER: Objection. Form.

16 THE WITNESS: It certainly seems to claim
17 one. I don't see anything in the claim that
18 requires multiple memory devices in a rank.

19 BY MR. WARRICK:

20 Q. But do any of the embodiments described
21 in the specification of Perego include only a
22 single memory device per rank?

23 MR. CHANDLER: Objection to form.

24 THE WITNESS: I don't recall. It was
25 certainly nothing that -- I mean, the

1 abstract says that the buffer device is
2 coupled to at least one memory device.

3 The first line of the "DETAILED
4 DESCRIPTION" says, [as read]: "...one or
5 more memory -- semiconductor memory devices
6 coupled to a buffer device."

7 BY MR. WARRICK:

8 Q. But of the specific embodiments
9 described, do any of them include only a single
10 memory device per rank?

11 MR. CHANDLER: Objection to form.

12 THE WITNESS: Column 7, line 62, in
13 describing the Figure 3C embodiment, it says
14 that you can access data from one or more of
15 the memory devices.

16 I mean, it's pretty consistent that
17 Perego doesn't care whether you have one or
18 more memory devices in a rank, either in his
19 abstract or his specification body or his
20 claims.

21 BY MR. WARRICK:

22 Q. But you agree that there's not a specific
23 embodiment described that shows one memory device
24 per rank; correct?

25 MR. CHANDLER: Objection to form.

1 THE WITNESS: I just told you Figure 3C
2 is described as having at least one memory
3 device, both at Column 7, line 63, and again
4 at line 67.

5 Column 12, line 16, again, with respect
6 to an embodiment, refers to [as read], "at
7 least one memory device over an interface."

8 Column 15, line 1, it talks about having
9 an embodiment with "one or more memory
10 devices."

11 And again, later in that paragraph.

12 BY MR. WARRICK:

13 Q. I think that's slightly different from
14 what I'm asking. But I think it's best that we
15 move on.

16 Sticking with Perego, though, I think we
17 covered earlier that Perego teaches using address
18 signals to select specific signal lines for
19 responding to a read or write command; is that
20 right?

21 MR. CHANDLER: Objection. Form.

22 THE WITNESS: It does describe that with
23 respect to the specific embodiments, yes,
24 person of -- but it's permissive.

25 ///

1 BY MR. WARRICK:

2 Q. So in that context, is it correct that
3 not all the devices within the rank need to
4 participate in responding to a read or write
5 command?

6 A. I don't know what you mean by they "need
7 to," but in a straightforward, ordinary
8 embodiment, they would.

9 Q. Well, is it possible, for example, in
10 that case, for all of the devices within the rank
11 to receive a low chip select signal, and then the
12 address signals would specify which devices would
13 provide a data burst?

14 A. No. It just doesn't work that way.

15 Q. Let's look at Halbert for a few minutes,
16 if we could. That's Exhibit 1078. It should also
17 be in the Exhibit Share.

18 A. Okay.

19 Q. And you're familiar with this document as
20 well?

21 A. Yes.

22 Q. And Figure 4 in Halbert is an embodiment
23 of the alleged invention of Halbert; correct?

24 A. It's a block diagram for a memory module,
25 according to one embodiment of the invention.

1 Q. Okay. And Figures 5 and 6 show the
2 operation of that embodiment; correct?

3 A. Yes, under certain circumstances.

4 Q. Now, looking at Figure 4 of Halbert -- in
5 the upper right corner within what's labeled a
6 "MEMORY DEVICE ARRAY," we have "Rank 140" and
7 "Rank 142"?

8 A. Yes.

9 Q. And those together form the memory device
10 array, correct, in Halbert?

11 A. Yes.

12 Q. And the memory device array in Figure 4
13 of Halbert is presented with an address and
14 command bus, specifically RADD/RCMD, from the
15 module controller; correct?

16 A. Yes.

17 Q. And as a result of being presented with a
18 common command and address bus, specifically
19 RADD/RCMD, do you agree that Rank 140 and Rank 142
20 operate in lockstep with each other?

21 MR. CHANDLER: Objection. Form.

22 THE WITNESS: Sometimes they do, and
23 sometimes they don't. If you look at Figure
24 6, you can see a situation where they are not
25 in lockstep.

1 BY MR. WARRICK:

2 Q. Would you call the memory device array of
3 Halbert a single rank?

4 MR. CHANDLER: Objection. Form.

5 THE WITNESS: No. I think they receive
6 separate control signals.

7 BY MR. WARRICK:

8 Q. And what's your basis for saying that?

9 A. They are selected based on -- well, let
10 me check here.

11 No, actually, that happens elsewhere.

12 I do think in the way that I've defined
13 "rank," those would be separate -- those would be
14 a single rank. This particular patent has its own
15 definition of "rank."

16 Q. Right. I should have clarified. I meant
17 according to your proposed construction of "rank."

18 And so if I understand you correctly,
19 you're saying you do think that the memory device
20 array of Halbert Figure 4 is a "rank," according
21 to your construction?

22 MR. CHANDLER: Objection. Form.

23 THE WITNESS: Yes.

24 BY MR. WARRICK:

25 Q. Now, if we look at the specification in

1 Column 4, it indicates that each of the memory
2 devices, which it calls "ranks 140 and 142," are
3 each capable of performing m-bit-wide data
4 transfers?

5 That's Column 4, around line 54.

6 A. Yes.

7 Q. And if you look a little bit further
8 down, also describing Figure 4 in Column 4, around
9 line 62, it describes [as read]: "An m-bit-wide
10 path through buffer 122 that receives and drives
11 data signals DQ on the system memory data bus."

12 So in view of those disclosures, am I
13 correct that the Halbert Figure 4 has an
14 m-bit-wide data path, but that the memory device
15 array can return, effectively, 2 m data bits?

16 A. Yes.

17 MR. CHANDLER: Objection to form.

18 BY MR. WARRICK:

19 Q. So in view of your proposed construction,
20 which requires memory devices, among other things,
21 to act together in response to command signals to
22 read or write the full bit width of the memory
23 module, isn't the memory device array actually
24 reading or writing double the full width -- bit
25 width of the memory module?

1 MR. CHANDLER: Objection to form.

2 THE WITNESS: It's still doing the full
3 width of the memory module. I mean, we would
4 still call it a "rank" because it's doing the
5 full width of the memory module.

6 Again, the point there is to distinguish
7 it from something that can't do the full
8 width of the memory module.

9 BY MR. WARRICK:

10 Q. So a set of memory devices that -- that
11 output something greater than the whole bit width
12 of the memory module can still constitute a rank,
13 in your view?

14 MR. CHANDLER: Objection. Form.

15 THE WITNESS: If it meets the other
16 criteria and it's supplying the full width of
17 the memory module, then I think it meets the
18 construction.

19 BY MR. WARRICK:

20 Q. Going back to Figure 6, you mentioned
21 that -- that they are not in lockstep in certain
22 aspects of Figure 6.

23 Can you just identify for me which
24 portions of Figure 6 you're relying on.

25 A. Yeah. I think I was a little bit off

1 there. The data returned is returned to the host
2 in two pieces out of step, but it does come out of
3 the array in lockstep.

4 MR. WARRICK: Okay. All right. Could we
5 take a brief break, just, say, five minutes.

6 (Short break taken.)

7 BY MR. WARRICK:

8 Q. All right. Dr. Wolfe, if we could go to
9 your declaration -- and we could go to your
10 declaration for the '417 patent, to paragraph 65.

11 Do you have that in front of you?

12 A. Yes.

13 Q. And this is in a portion of your
14 declaration addressing the '087 provisional, which
15 is one of the applications to which the '417
16 patent claims priority; correct?

17 A. Yes.

18 Q. Now, in paragraph 65 of your declaration,
19 could you read the second sentence for me, please.

20 A. "For example, a Skilled Artisan would
21 have understood that, for DDR SDRAM devices, a
22 data transfer is preceded by a 'preamble' on the
23 DQS stroke lines, and the data transfer through
24 the buffer can be controlled in response to such
25 preambles."

1 Q. Thank you.

2 I'd like to ask you some questions about
3 that.

4 Specifically, is it your view that the
5 data transferred through the buffer could be
6 controlled in response to such preambles?

7 A. I think it could. But I think a better
8 way to say it would be -- "could be controlled to
9 manage such preambles."

10 Q. I'm sorry. I'm not sure if I follow,
11 Dr. Wolfe. You're saying that the -- maybe if you
12 could just restate.

13 What I was trying to understand is
14 whether the preambles could control the data
15 transfer through the buffer.

16 A. I think they could, but I don't think
17 that's what I was trying to say here.

18 I think what I was trying to say here is
19 that there could be data buffer control signals to
20 control the buffer during the time when those
21 preambles are present.

22 Q. So I was just re-reading your answer,
23 Dr. Wolfe, in an effort to understand.

24 You said, "I think what I was trying to
25 say here is that there could be data buffer

1 control signals to control the buffer during the
2 time when those preambles are present."

3 So that is different than the preambles
4 controlling the data transfer through the buffer;
5 correct?

6 MR. CHANDLER: Objection. Form.

7 THE WITNESS: It is. As I said, I think
8 the preambles could control it in some cases,
9 but that wasn't what I was trying to say
10 here.

11 I think what I was trying to say is the
12 data transfer through the buffer can be
13 controlled to respond to such preambles, not
14 in response to such preambles. I think that
15 would be clearer.

16 BY MR. WARRICK:

17 Q. Bear with me just a minute, if you would,
18 please.

19 All right. Let's go back to Exhibit
20 1064, if we could, please, the JEDEC DDR2
21 standard.

22 A. Okay.

23 Q. And actually, before we do that, just to
24 clarify. The same discussion about the '087
25 provisional is also contained in your declaration

1 pertaining to the '215 patent; correct?

2 A. That's my recollection.

3 Q. Okay. And so your answers to these
4 recent questions, would they apply equally to the
5 discussion in your '215 patent declaration?

6 A. Yes.

7 Q. So turning to Exhibit 1064, I'd like to
8 go specifically to page 26.

9 A. Okay.

10 Q. And on page 26, there is Figure 23.
11 Do you see that?

12 A. Yes.

13 Q. And I believe that Figure 23 was also
14 referenced in that same paragraph of your
15 declaration?

16 A. Yes.

17 Q. And --

18 A. And also Figure 29.

19 Q. Am I correct that Figure 23 in Exhibit
20 1064 shows the timing for data transfers that
21 result from a read operation in DDR2?

22 A. Yes. But it should probably be read or
23 viewed in conjunction with 25, 26, and 27, to
24 understand some of the context.

25 Q. Are you referring to Figures 25, 26, and

1 27?

2 A. Yes.

3 Q. Okay. So in Figure 23 of Exhibit 1064,
4 the preamble that we were discussing earlier from
5 your declaration, is the period while DQS is low
6 prior to the first rising transition on DQS that
7 accompanies the first piece of data, the burst; is
8 that right?

9 A. Generally, yes, the rising edge of DQS
10 slightly precedes the first piece of data; but
11 that's generally correct.

12 Q. And in Figure 23, tRPRE indicates the
13 duration of the preamble; yes?

14 A. Generally. We'd have to look at the
15 definition to see if it's a minimum, maximum, or
16 typical duration.

17 Q. And because Figure 23 illustrates read
18 data timing, in Figure 23, CK, which is the
19 differential clock, is an input to a DDR2 SDRAM,
20 and DQS and DQ are outputs from the DDR2 SDRAM in
21 response to a read command; correct?

22 MR. CHANDLER: Objection to form.

23 THE WITNESS: I think that's generally
24 correct.

25 ///

1 BY MR. WARRICK:

2 Q. And if we look specifically at the DQS
3 signal trace in Figure 23, the SDRAM drives DQS to
4 a low voltage during the preamble; and then after
5 the preamble, the SDRAM alternates between driving
6 the DQS signal line to a high voltage and to a low
7 voltage, as the burst is output from the SDRAM; is
8 that right?

9 A. Correct.

10 Q. And remaining with Figure 23, before the
11 preamble, and after -- strike that.

12 In Figure 23, Dr. Wolfe, following the
13 end of the burst, the diagram shows that the DQS
14 signal trace is at an intermediate level.

15 Do you see that?

16 A. No. That's a misinterpretation.

17 Q. Okay. In what way?

18 A. That's to represent that in this
19 particular case, where there -- where there is no
20 immediate subsequent transaction, it would return
21 to a -- I believe, to a high impedance level.

22 Q. Okay. So am I understanding correctly
23 that when we see the DQS on the right side of
24 Figure 23 represented by a flat line, that's
25 representing a high impedance state?

1 MR. CHANDLER: Objection. Form.

2 THE WITNESS: In this diagram, I believe
3 that's correct.

4 BY MR. WARRICK:

5 Q. And when DQS is in that state, the SDRAM
6 isn't driving it high or low. It's just not being
7 driven at all; correct?

8 A. Not being driven by the SDRAM. It could
9 be being driven by something else.

10 Q. Okay.

11 A. Including another SDRAM.

12 Q. So just to make sure I have this correct,
13 in Figure 23, when we see DQS on the right side of
14 the figure in what appears to be a flat line, it's
15 not showing a voltage that's, for example, halfway
16 between the VSS and VDD; it's not showing the
17 voltages at half VDD; but only that the DQS output
18 driver of the SDRAM is in a high impedant state.

19 Do I have that right?

20 A. Yes, I believe that's correct.

21 MR. WARRICK: All right, Dr. Wolfe. I
22 don't believe I have any further questions
23 for you at the moment.

24 Turn it over if Counsel has any redirect.

25 MR. CHANDLER: We'll go off the record.

1 But before we do that, to be clear, I mean,
2 this was a separate two days for both IPRs.
3 And so you're finished with your direct for
4 both IPRs now; you're turning over to me for
5 any redirect on both IPRs; is that correct?

6 MR. WARRICK: That's correct.

7 MR. CHANDLER: Okay. Yeah. Why don't we
8 go off the record; and maybe ten minutes.
9 I'll check my notes.

10 MR. WARRICK: Okay.

11 (Short break taken.)

12 EXAMINATION

13 BY MR. CHANDLER:

14 Q. To start, I want to follow up on some
15 questions at the beginning about the claim
16 construction for rank. And there was a colloquy
17 where -- the following question and answer, which
18 I'll try to put in the chat. I'll also read it to
19 you. But sometimes -- maybe I can't put it in the
20 chat. That's fine. I'll read it to you slowly,
21 and then I'll ask my question.

22 So this is just an earlier question and
23 answer to refresh your recollection about the part
24 of the testimony that I'm asking about.

25 So Netlist's counsel asked you:

1 "So maybe we can try this differently.
2 If a set of memory devices are on the memory
3 module and they respond in approximately the
4 same time to the same command signals,
5 including chip select signals, to read or
6 write the full bit width of the memory
7 module, then that would fit your definition
8 of a 'rank,' at least for purposes of these
9 patents; correct?

10 "ANSWER: In an ordinary situation, it
11 would be. If you're trying to describe
12 something that's strange or unusual, I would
13 have to see it to know.

14 "Again, these are -- these constructions
15 are intended to be understood by a reasonable
16 person who is familiar with the art."

17 So do you have that question and answer
18 in mind for my follow-up question and answer?

19 A. Yes.

20 Q. So my question is simply, when you were
21 asked if a set of memory devices fits your
22 definition of "rank," where your definition of
23 "rank" is one or more memory devices, were you
24 trying to change your claim construction for rank?

25 MR. WARRICK: Objection. Form.

1 THE WITNESS: No. You can have one thing
2 in a set. But -- technically, you can have
3 zero things in a set, but you can't have zero
4 things that respond in the way the rest of
5 that question said.

6 BY MR. CHANDLER:

7 Q. And at any point in response to the
8 questions from Netlist's counsel, were you trying
9 to change your construction for rank that appears
10 in your expert declarations?

11 MR. WARRICK: Objection to form.
12 Leading.

13 THE WITNESS: No. That -- that is the
14 correct construction with respect to these
15 patents.

16 BY MR. CHANDLER:

17 Q. Okay. I want to go to a different
18 colloquy now, about Perego.

19 And, you know, to the extent it helps,
20 I'll put the time stamp for the previous colloquy,
21 which was -- it looks like it started at 9:00
22 a.m., 18 minutes and 32 seconds.

23 So I'll just put that in the record to
24 help us try to find it later on.

25 Now I want to move to a different

1 colloquy about Perego, where the time stamp, at
2 least in the rough, is 11:00 a.m., 17 minutes and
3 9 seconds. And again, I'll read you the question
4 and answer that I'm trying to follow up on, and
5 then we'll ask my follow-up question.

6 So counsel for Netlist asked you [as
7 read]:

8 "Question: Does Perego disclose
9 selecting target subsets based on anything other
10 than address bits?

11 "Answer: I don't recall it explicitly
12 saying that, but it also doesn't in any way limit
13 it to the address bits. And a person of ordinary
14 skill, when looking at the JEDEC standard Exhibit
15 1064, would understand that you can select
16 portions of memory or memory devices from a set
17 using either address bits or bank address inputs.

18 "Bank address inputs are essentially
19 simply extended address bits for many purposes."

20 Do you remember that question and answer?

21 A. Yes.

22 Q. So my follow-up question is, when
23 performing rank multiplication with Perego, would
24 that be performed only with address bits and with
25 nothing else?

1 MR. WARRICK: Objection. Form.

2 THE WITNESS: No. You still need to send
3 the proper commands, and you still need to
4 select the proper chips with the proper chip
5 select values.

6 BY MR. CHANDLER:

7 Q. And so in Perego -- if you look at Column
8 15, line 37 to 40 -- and let me know when you have
9 that in front of you.

10 A. I do.

11 Q. In Perego at Column 15, line 37 to 40,
12 where there's a discussion of "...the target
13 subset of secondary channel signal lines may be
14 selected via address bits provided as part of the
15 primary channel request," in that example, would
16 it be only the address bits that would be used --
17 or would it be used in conjunction with something
18 else? And in which case, what would the
19 "something else" be?

20 MR. WARRICK: Objection. Form.

21 THE WITNESS: No. As I explained before,
22 you can't use address bits to get some
23 devices to respond and other devices not to
24 respond. You have to use commands and chip
25 selects to get that to happen.

1 Otherwise, you would just get -- all the
2 chips would respond; they would just respond
3 from different addresses. And that would
4 cause collisions and wouldn't perform rank
5 multiplication in the way that's described in
6 these examples.

7 BY MR. CHANDLER:

8 Q. Could you turn to the '215 and '417
9 patents, and --

10 A. One at a time.

11 Q. I have a question about both of them.

12 And maybe as a preliminary matter, is it
13 correct that the figures and specifications of the
14 '215 and '417 are substantially similar, if not
15 identical?

16 A. As far as I can tell, yes.

17 Q. So my question is for both patents.

18 Do the '215 and '417 patents refer to
19 FB-DIMMs?

20 A. They do. We talked about before that
21 they show up in the IDS; but also in the text --
22 let's see. In the '215, I see it in Column 21,
23 line 17. '417, I see it at Column 23, line 32.

24 Q. Do you believe that at the time of the
25 '215 and '417 patents that FB-DIMMs were known to

1 a person of ordinary skill in the art?

2 MR. WARRICK: Objection. Form. Leading.

3 THE WITNESS: I think they were.

4 BY MR. CHANDLER:

5 Q. Follow up on a different colloquy. Try
6 to be precise. And actually -- so I'm going to
7 follow up on some questions about Halbert. And it
8 spans a few questions, so I won't give you a
9 specific question to start with.

10 Could you pull up the Halbert reference?
11 Let me know when you have it. I think it was --

12 A. 1078? I've got it.

13 Q. Yeah. I think 1078 was the version that
14 Netlist's counsel was asking you questions about.
15 I think there's also the Halbert publication
16 that's an exhibit, which has the same disclosure,
17 but we'll stick with 1078.

18 Let me know when you have it.

19 A. Yes.

20 Q. So in Column 4 of Exhibit 1078, starting
21 at line 57, do you see Halbert teaches that,
22 "Generally, multiple ranks will receive the same
23 address and commands, and will perform memory
24 operations with the interface circuit
25 concurrently"?

1 A. I see that.

2 Q. In your opinion, is Halbert limited in
3 its teachings to only that specific example, where
4 multiple ranks receive -- receive the same address
5 and commands and perform memory operations with
6 the interface circuit concurrently?

7 MR. WARRICK: Objection. Form. Leading.

8 THE WITNESS: I don't think so. I think
9 that's why I was a little bit confused
10 before. I think that memory device array can
11 be a single rank when it does receive the
12 same address and commands.

13 But Halbert seems to explain that not all
14 embodiments do that. And if they receive
15 different commands and different -- in
16 particular, then they would be two ranks.

17 BY MR. CHANDLER:

18 Q. Would you turn to your '417 expert
19 declaration marked as Exhibit 1003 and go to page
20 149. And let me know when you're there.

21 A. I am there.

22 Q. And just to make it simpler, can you also
23 at the same time pull up your other expert
24 declaration from the '215 IPR marked as Exhibit
25 1003 and go to page 152 of that expert

1 declaration.

2 A. Okay.

3 Q. And do you see on page 149 of Exhibit
4 1003 in the '417 IPR and also page 152 of
5 Exhibit 1003 of the '215 IPR you have an annotated
6 version of Figure 4 of Halbert that shows Rank 140
7 in green and Rank 142 in blue?

8 A. Yes.

9 Q. For clarity, can Rank 140 in Halbert and
10 Rank 142 in Halbert, in at least some embodiments,
11 be two separate ranks?

12 MR. WARRICK: Objection. Form. Leading.

13 THE WITNESS: Yes. That's what I was
14 indicating in these sections of the report.

15 MR. CHANDLER: Okay. Nothing further
16 from me.

17 And as a reminder, we would like the
18 final by Friday, November 10, and the
19 opportunity to review and make any
20 corrections.

21 MR. WARRICK: Okay. If we could get the
22 final by the 10th, as well, that would be
23 good.

24 (TIME 4:21 p.m.)

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DECLARATION UNDER PENALTY OF PERJURY

I, DR. ANDREW WOLFE, do hereby certify
under penalty of perjury that I have read the
foregoing transcript of my deposition taken
on NOVEMBER 5, 2023; that I have made such
corrections as appear noted herein; that my
testimony as contained herein, as corrected,
is true and correct.

DATED this day of ,
2023, at .

DR. ANDREW WOLFE

1 STATE OF CALIFORNIA)
2 (ss.
3 COUNTY OF LOS ANGELES)

4 I, RENEE HARRIS, do hereby certify that I
5 am a licensed Certified Shorthand Reporter, duly
6 qualified and certified as such by the State of
7 California;

8 That prior to being examined, the witness named
9 in the foregoing deposition was by me duly sworn
10 to testify to tell the truth, the whole truth, and
11 nothing but the truth;

12 That the said deposition was by me recorded
13 stenographically;

14 And the foregoing pages constitute a full,
15 true, complete and correct record of the testimony
16 given by the said witness;

17 That I am a disinterested person, not
18 being in any way interested in the outcome of said
19 action, or connected with, nor related to any of
20 the parties in said action, or to their respective
21 counsel, in any manner whatsoever.

22 DATED: 11/10/2023



23
24 Renee Harris, CSR, CCR, RPR
CA CSR No. 14168,
25 NJ CRR No. 30XI00241200

1 THEODORE W. CHANDLER, ESQ.

2 ted.chandler@bakerbotts.com

3 November 10, 2023

4 RE: SAMSUNG ELECTRONICS CO. vs. NETLIST, INC.

5 November 5, 2023, DR. ANDREW WOLFE, JOB NO. 6294218

6 The above-referenced transcript has been
7 completed by Veritext Legal Solutions and
8 review of the transcript is being handled as follows:

9 — Per CA State Code (CCP 2025.520 (a)-(e)) - Contact Veritext
10 to schedule a time to review the original transcript at
11 a Veritext office.

12 — Per CA State Code (CCP 2025.520 (a)-(e)) - Locked .PDF
13 Transcript - The witness should review the transcript and
14 make any necessary corrections on the errata pages included
15 below, notating the page and line number of the corrections.
16 The witness should then sign and date the errata and penalty
17 of perjury pages and return the completed pages to all
18 appearing counsel within the period of time determined at
19 the deposition or provided by the Code of Civil Procedure.

20 — Waiving the CA Code of Civil Procedure per Stipulation of
21 Counsel - Original transcript to be released for signature
22 as determined at the deposition.

23 — Signature Waived - Reading & Signature was waived at the
24 time of the deposition.

25

Page 184

1 _X_ Federal R&S Requested (FRCP 30(e)(1)(B)) - Locked .PDF
2 Transcript - The witness should review the transcript and
3 make any necessary corrections on the errata pages included
4 below, notating the page and line number of the corrections.
5 The witness should then sign and date the errata and penalty
6 of perjury pages and return the completed pages to all
7 appearing counsel within the period of time determined at
8 the deposition or provided by the Federal Rules.
9 ___ Federal R&S Not Requested - Reading & Signature was not
10 requested before the completion of the deposition.

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.,

Petitioner,

v.

NETLIST, INC.,

Patent Owner.

IPR2023-00454
Patent 11,093,417

**ERRATA TO THE DEPOSITION OF
ANDREW WOLFE (NOVEMBER 4, 2023)**

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.,

Petitioner,

v.

NETLIST, INC.,

Patent Owner.

IPR2023-00455

Patent 9,858,215

**ERRATA TO THE DEPOSITION OF
ANDREW WOLFE (NOVEMBER 4, 2023)**

I, ANDREW WOLFE, have read the transcript of my deposition taken on November 4, 2023. Listed below are changes to the transcript that I wish to make and the reasons for making them:

<u>Page:Line</u>	<u>Now Reads</u>	<u>Should Read</u>	<u>Reason for Change</u>
1:24 2:19 5:2	November <u>5</u> , 2023	November <u>4</u> , 2023	My deposition was on Saturday, November 4, 2023, not November 5th.
2:12–:13	<u>Case No. IPR2020-01624</u> <u>Patent No. 6,975,132</u>	<u>Case No. IPR2023-00454</u> <u>Patent No. 11,093,417</u> <u>- and -</u> <u>Case No. IPR2023-00455</u> <u>Patent No. 9,858,215</u>	Typographical error. See 1:12–:16.

<u>Page:Line</u>	<u>Now Reads</u>	<u>Should Read</u>	<u>Reason for Change</u>
15:18–16:6	Q. If a set of memory devices are on the memory module and they respond in approximately the same time to the same command signals, including chip select signals, to read or write the full bit width of the memory module, then that would fit your definition of a "rank," at least for purposes of these patents; correct? A. In an ordinary situation, it would be. If you're trying to describe something that's strange or unusual, I would have to see it to -- to know. Again, these are -- these constructions are intended to be understood by a reasonable person who is familiar with the art.	[see note]	No change, but this was further clarified at 174:20–175:15.
29:16–:19	I would say that <u>configureable</u> bit widths are a feature of his invention but not a required feature of his disclosure.	I would say that <u>configurable</u> bit widths are a feature of his invention but not a required feature of his disclosure.	Typographical error

<u>Page:Line</u>	<u>Now Reads</u>	<u>Should Read</u>	<u>Reason for Change</u>
32:9–:13	Q. And you've said earlier that Perego allows you to configure the ranks; correct? MR. CHANDLER: Object to form. THE WITNESS: That is a feature of some of his embodiments.	[see note]	This was clarified in the next question and answer. See 32:15–:22 (“It's the interface that it is configurable width. I don't think I've considered whether or not the ranks can be configured....”).
32:19–:20	It's the interface that it is configurable <u>with</u> .	It's the interface that it is configurable <u>width</u> .	Typographical error
41:10–:12	Perego, in that context, illustrates a set of <u>input sig- --</u> and output signals to a memory device	Perego, in that context, illustrates a set of <u>input signals</u> and output signals to a memory device	Typographical error

42:15–47:25	Q. But the example depicted in Figure 4B of Perego is showing a Rambus-style memory architecture if you interpret it literally; correct? MR. CHANDLER: Objection. Form. THE WITNESS: If you interpret it literally, it is illustrating the Rambus signal names.... Q...From your explanation, Figure 4B is depicting a well-known Rambus-style interface between the buffer and the memory devices; yes? A. That Figure 4B literally illustrates a well-known Rambus-style interface between the buffer and the memory devices. And Perego elsewhere explains that other memory interfaces can be used instead. Q. And if you were to use DDR2 memory devices in Figure 4B of Perego, you would	[see note]	No change, but this was further clarified at 48:4–49:23, 133:3–:21, 134:22–135:8, 135:23–136:5, 138:10–140:20, 146:24–147:5.
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<u>Page:Line</u>	<u>Now Reads</u>	<u>Should Read</u>	<u>Reason for Change</u>
	also have to change the interconnects between those devices and the buffer; correct? MR. CHANDLER: Objection. Form. THE WITNESS: You would replace the well-known Rambus interface with the well-known DDR2 interface. Q. And isn't it correct you would also have to make changes to the design of the buffer in Figure 4B of Perego if you substituted DDR2 memory devices? A. Correct. You would -- you would take aspects of the buffer that were designed to be compliant with the public Rambus standard, and you would change them to be compliant with the public DDR2 standard.		
48:18	column address <u>stroke</u>	column address <u>strobe</u>	Typographical error

<u>Page:Line</u>	<u>Now Reads</u>	<u>Should Read</u>	<u>Reason for Change</u>
50:25–51:4	I wouldn't say that it's not possible to have a <u>configureable</u> memory module, but once the module's been <u>figured</u> , the full bit width, I think, is a -- is established.	I wouldn't say that it's not possible to have a <u>configurable</u> memory module, but once the module's been <u>configured</u> , the full bit width, I think, is a -- is established.	Typographical errors
53:18–:21	And that's the only embodiment that one <u>needs to</u> understand that the asserted claims are obvious -- or the challenged claims are obvious.	And that's the only embodiment that one <u>needs, to</u> understand that the asserted claims are obvious -- or the challenged claims are obvious.	Typographical error
62:18–:21	It's literally what's shown in the example. But again, the <u>content</u> -- the patent itself tells you that that's not a limitation of Figure 4B.	It's literally what's shown in the example. But again, the <u>context</u> -- the patent itself tells you that that's not a limitation of Figure 4B.	Typographical error
68:19–:20	I would use <u>8-by-8</u> chips in each rank to provide a 64-bit response.	I would use <u>eight x8</u> chips in each rank to provide a 64-bit response.	Typographical error
69:3–:6	If I were using <u>by-8</u> chips, I would put 16 in each rank to get 128-bit host interface, or I would use <u>8-by-16</u> chips if I wanted each rank to provide 128 bits to 128-bit interface.	If I were using <u>x8</u> chips, I would put 16 in each rank to get 128-bit host interface, or I would use <u>eight x16</u> chips if I wanted each rank to provide 128 bits to 128-bit interface.	Typographical errors

<u>Page:Line</u>	<u>Now Reads</u>	<u>Should Read</u>	<u>Reason for Change</u>
76:24–78:1	Q. And in the example of Perego, the buffer will select the target subset channels based on address bits; is that right? A. I think it can select based on address bits. Q. Does Perego disclose selecting target subsets based on anything other than address bits? A. I don't recall it explicitly saying that, but it also doesn't in any way limit it to the address bits.	[see note]	No change, but this was further clarified at 160:16–161:14, 176:22–178:6.
79:7–:11	If you want to access a row across a group of memory devices, the same row needs to be activated in each memory device that you're going to access using the <u>signal</u> read or write command.	If you want to access a row across a group of memory devices, the same row needs to be activated in each memory device that you're going to access using the <u>single</u> read or write command.	Typographical error

<u>Page:Line</u>	<u>Now Reads</u>	<u>Should Read</u>	<u>Reason for Change</u>
80:7–:10	In other embodiments, he talks about a one-to-one serialization ratio and he talks about determining the configuration <u>and</u> manufacturing time.	In other embodiments, he talks about a one-to-one serialization ratio and he talks about determining the configuration <u>at</u> manufacturing time.	Typographical error
81:11–:14	I think this is supportive of a two-rank configuration of Figure 4B in which <u>channels 4c and 4d</u> are accessed together and <u>4a and 4b</u> are waiting for the next access.	I think this is supportive of a two-rank configuration of Figure 4B in which <u>channels 415c and 415d</u> are accessed together and <u>415a and 415b</u> are waiting for the next access.	Misspoke. See 80:16–81:1.
95:21–:24	So to avoid confusion between it being there and it not being there, we <u>talked</u> about it being asserted when it's there, even if that's a zero voltage.	So to avoid confusion between it being there and it not being there, we <u>talk</u> about it being asserted when it's there, even if that's a zero voltage.	Typographical error

<u>Page:Line</u>	<u>Now Reads</u>	<u>Should Read</u>	<u>Reason for Change</u>
100:9–:13	So if there is a delay - - a time delay between the memory device response and the memory module response, then the CAS latency of the module will be greater <u>than</u> the amount of that delay in the CAS latency of the device.	So if there is a delay - - a time delay between the memory device response and the memory module response, then the CAS latency of the module will be greater <u>by</u> the amount of that delay in the CAS latency of the device.	Typographical error
102:25–:10	Q....Dr. Wolfe, Perego does not expressly disclose registering the data output as distinct from using latches; correct? MR. CHANDLER: Object to form. THE WITNESS: Not explicitly. But what it does describe is generating clocks, clock alignment, to use the latches in a way so there is still a delay in the way that there <u>wouldn't</u> be with a register. And that's why it would be obvious to a person of ordinary skill to use a register, as well.	Q....Dr. Wolfe, Perego does not expressly disclose registering the data output as distinct from using latches; correct? MR. CHANDLER: Object to form. THE WITNESS: Not explicitly. But what it does describe is generating clocks, clock alignment, to use the latches in a way so there is still a delay in the way that there <u>would</u> be with a register. And that's why it would be obvious to a person of ordinary skill to use a register, as well.	Typographical error

<u>Page:Line</u>	<u>Now Reads</u>	<u>Should Read</u>	<u>Reason for Change</u>
107:25– 108:10	Q. Now, earlier, another concept you referenced from one of your answers was a fully buffered DIMM? A. Yes. Q. Did those exist at the time of the priority date for the '417 patent? MR. CHANDLER: Objection. Form. THE WITNESS: I don't know. I'm familiar with the specification being published in 2006, but I don't know when they were first known in the industry.	[see note]	No change, but this was further clarified at 178:17–179:3.
113:2–:5	it refers to the CAS latency of a memory device independently of whether or not it's been used <u>an</u> a memory module or any particular type of module	it refers to the CAS latency of a memory device independently of whether or not it's been used <u>in</u> a memory module or any particular type of module	Typographical error
118:11–:12	Exhibit 1062 is the registered DIMM specification for <u>DDR not DDR2 memories.</u>	Exhibit 1062 is the registered DIMM specification for <u>DDR, not DDR2, memories.</u>	Typographical error

<u>Page:Line</u>	<u>Now Reads</u>	<u>Should Read</u>	<u>Reason for Change</u>
121:3–:5	not every system needs to set the <u>cache</u> latency for particular devices the same way	not every system needs to set the <u>CAS</u> latency for particular devices the same way	Typographical error
131:24– 132:7	Q. And we discussed earlier that in Perego, if you were to use JEDEC-compliant DDR2 memory devices, you would, in fact, have to modify other parts of the memory module to make it work; correct? MR. CHANDLER: Object to form. THE WITNESS: Yes. You would need to make modifications at the detail level that are routine within the industry.	[see note]	No change, but this was further clarified at 133:3–134:8.
138:3–:4	there's 800 pages in the <u>report</u>	there's 800 pages in the <u>reports</u>	Typographical error
143:17	RQ <u>scroll</u> lines	RQ <u>control</u> lines	Typographical error
157:24–:25	And that's what's important, <u>if</u> it says, "one or more DRAM devices."	And that's what's important, <u>is</u> it says, "one or more DRAM devices."	Typographical error

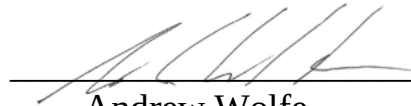
<u>Page:Line</u>	<u>Now Reads</u>	<u>Should Read</u>	<u>Reason for Change</u>
160:16–:24	Q....Sticking with Perego, though, I think we covered earlier that Perego teaches using address signals to select specific signal lines for responding to a read or write command; is that right? MR. CHANDLER: Objection. Form. THE WITNESS: It does describe that with respect to the specific embodiments, yes, person of -- but it's permissive.	[see note]	No change, but this was further clarified at 161:9–:14, 176:22–178:6.
163:18–:23	Q....And so if I understand you correctly, you're saying you do think that the memory device array of Halbert Figure 4 is a "rank," according to your construction? MR. CHANDLER: Objection. Form. THE WITNESS: Yes.	[see note]	No change, but this was further clarified at 179:20–181:14.
166:23	DQS <u>stroke</u> lines	DQS <u>strobe</u> lines	Typographical error

<u>Page:Line</u>	<u>Now Reads</u>	<u>Should Read</u>	<u>Reason for Change</u>
172:18	high <u>impedant</u> state	high <u>impedance</u> state	Typographical error

I hereby certify that the transcript of my deposition on November 4, 2023, as corrected above, is a true and accurate transcription of my testimony.

I, Andrew Wolfe, do hereby declare and state, that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, under Section 1001 of Title 18 of the United States Code.

Executed on: December 5, 2023



 Andrew Wolfe