

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.

Petitioner,

v.

NETLIST, INC.,

Patent Owner

IPR2023-00455

Patent 9,858,215

IPR2023-201428
Patent 8,787,060

IPR2023-00454
Patent 11,093,417

Remote video-recorded deposition of

STEVEN PRZYBYLSKI, PH.D.,

Volume 1

REPORTED BY:

Gail L. Inghram Verbano:

Registered Diplomate Reporter,

Certified Realtime Reporter,

Certified Shorthand Reporter-CA (No. 8635)

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8 SAMSUNG ELECTRONICS CO., LTD.

9 Petitioner,

10 v.

11 NETLIST, INC.,

12 Patent Owner
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16 WHEREUPON, the remote
17 video-recorded deposition of STEVEN PRZYBYLSKI,
18 Ph.D., Volume 1, was held via Zoom
19 videoconferencing, on Thursday, February 15,
20 2024, beginning at approximately 8:07 a.m., the
21 proceedings being recorded stenographically by
22 Gail Inghram Verbano, Registered Diplomate
23 Reporter, Certified Realtime Reporter,
24 Certified Shorthand Reporter-CA (No. 8635), and
25 transcribed under her direction.

A P P E A R A N C E S

A P P E A R A N C E S:

On behalf of Samsung:

THEODORE W. CHANDLER, ESQ.

ted.chandler@bakerbotts.com

FERENC PAZMANDI, ESQ.

ferenc.pazmandi@bakerbotts.com

BAKER BOTTS, LLP

101 California Street, Suite 3200

San Francisco, California 94111-5802

415.291.6259

On behalf of Netlist, Inc.:

PHILIP WARRICK, ESQ.

pwarrick@irell.com

IRELL & MANELLA, LLP

1800 Avenue of the Stars, Suite 900

Los Angeles, California 90067-4276

310.277.1010

ALSO PRESENT:

DANA BACHMAN, Legal Videographer

C O N T E N T S

EXAMINATION OF:

PAGE

STEVEN PRZYBYLSKI, Ph.D.

By Attorney Chandler8

E X H I B I T S

NUMBER:

PAGE

Exhibit 1096 Redline comparison of the14

Declarations of Dr. Przybylski

Exhibit 1097 Second of edition of textbook167

by S. Przybylski, "New DRAM
Technologies: A Comprehensive
Analysis of the New
Architectures" (451 pages)

Exhibit 1103 PowerPoint presentation re:63

Netlist's Technology Tutorial,
5-8-17 (CDX-200.1 to 200.11)

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E X H I B I T S (Cont'd)

NUMBER	PAGE
Exhibit 1104 JEDEC Standard for DDR SDRAM,	77
JESD79D, January 2004	
(86 pages)	
Exhibit 1106 JEDEC Standard 21-C for DDR	79
SDRAM (36 pages)	

(Exhibits 1098 through 1102 not
identified.)

PREVIOUSLY MARKED EXHIBITS REFERENCED:

NUMBER	PAGE
Exhibit 1001	9
Exhibit 1005	254
Exhibit 1060	45
Exhibit 1062	46
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Exhibit 1069	193
Exhibit 1070	100

1	Exhibit 1071	36
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7	Exhibit 2020	70
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Thursday, February 15, 2024; 8:07 a.m.

- - -

THE VIDEOGRAPHER: Good morning.

We're now on the record at 8:07 a.m. Pacific
Time on February 15th, 2024.

This begin the video-conferenced
deposition of Steven Przybylski, taken in the
matter of Samsung Electronics Company, Ltd.,
versus Netlist, Incorporated, filed before the
Patent Trial and Appeal Board, Case Number
IPR2023-00454 and IPR2023-00455.

My name is Dana Bachman. I'm
your videographer today. Our court reporter is
Gail Verbano. We are both representing Esquire
Deposition Solutions.

Will everyone present please
identify themselves, beginning with our witness,
Mr. Przybylski.

DR. PRZYBYLSKI: Steven
Przybylski.

THE VIDEOGRAPHER: Thank you.
Counsel, please.

ATTORNEY CHANDLER: Good morning.
This is Theodore Chandler from Baker Botts on
behalf of the Petitioner, Samsung Electronics

1 Co., Ltd. And with me is my colleague
2 Dr. Ferenc Pazmandi.

3 ATTORNEY WARRICK: Philip Warrick
4 with Irell & Manella on behalf of Patent Owner
5 Netlist, Inc. And with me is Dr. Anita Zhong,
6 also with Irell & Manella.

7 THE VIDEOGRAPHER: Thank you very
8 much.

9 Madam Reporter, would you please
10 swear in our witness.

11
12 WHEREUPON,

13 STEVEN PRZYBYLSKI, Ph.D.,
14 being first duly sworn or affirmed to testify to
15 the truth, the whole truth, and nothing but the
16 truth, was examined and testified as follows:

17
18 EXAMINATION

19 BY ATTORNEY CHANDLER:

20 Q. Good morning. Please state your
21 name for the record and spell your last name.

22 A. Steven Przybylski,
23 P-R-Z-Y-B-Y-L-S-K-I.

24 Q. What do you do for a living,
25 Dr. Przybylski?

1 A. I am an intellectual property
2 consultant, principally.

3 Q. Dr. Przybylski, were you retained
4 by Netlist to provide opinions in this case
5 related to Netlist's '417 patent?

6 A. Yes.
7 (Exhibit Number 1001 was previously
8 marked for identification.)

9 BY ATTORNEY CHANDLER:

10 Q. And the '417 patent is marked as
11 Exhibit 1001 in IPR2023-00454 and is U.S. Patent
12 Number 11,093,417; correct?

13 A. Correct. Technically, I'm not
14 retained by Netlist but through an intermediary,
15 but it doesn't make any real difference.

16 Q. Dr. Przybylski, were you also
17 retained by Netlist, at least indirectly, to
18 provide opinions in this case related to
19 Netlist's '215 patent?

20 A. Yes.

21 Q. And the '215 patent is marked as
22 Exhibit 1001 in IPR2023-00455 and is U.S. Patent
23 Number 9,858,215; correct?

24 A. Yes.

25 Q. The '417 and '215 patents are

1 related to each other and have substantially the
2 same figures and written description; correct?

3 ATTORNEY WARRICK: Objection;
4 form.

5 THE WITNESS: Yes, that's
6 correct.

7 BY ATTORNEY CHANDLER:

8 Q. Given that this is a remote
9 deposition, meaning that we're not in the same
10 physical room together, there are a few
11 questions I need to ask, starting with where are
12 you physically located right now during this
13 deposition?

14 A. Ann Arbor, Michigan.

15 Q. Is there anyone else in the room
16 with you right now?

17 A. No.

18 Q. Given that I cannot see the room
19 that you are in, will you please let us know if
20 someone enters the room that you're in at any
21 time before this deposition ends?

22 A. I will do so.

23 Q. Dr. Przybylski, did you bring
24 anything with you to your deposition today?

25 A. I have clean copies -- hard

1 copies of the two declarations from the two
2 IPRs.

3 (Exhibit Number 2024 was previously
4 marked for identification.)

5 BY ATTORNEY CHANDLER:

6 Q. Marked as Exhibit 2024 in each
7 IPR?

8 A. Correct.

9 Q. And is there anything on your
10 computer related to these IPRs in front of you?

11 A. On the screen, you mean?

12 Q. Correct.

13 A. I have the Zoom that's going on.
14 You also bade me to download redlines, and I
15 have one of those two visible to me right now.

16 Q. Okay.

17 A. I also have a window -- Explorer
18 window up where it's showing the folder in which
19 that downloaded redline exists.

20 Q. Given that I cannot see whether
21 you have anything in front of you, will you
22 please let us know if you or anyone else puts
23 anything in front of you at any time before this
24 deposition ends?

25 A. Of course.

1 Q. I will take breaks throughout
2 your deposition, but I want to remind you that
3 during those breaks, under the rules of the
4 PTAB, you should not consult with your counsel
5 about the substance of your testimony.

6 Do you understand?

7 A. I do.

8 Q. During deposition, I would ask
9 that you do not look things up on the internet
10 or do other things on your computer or your
11 phone that we cannot see on the camera.

12 Do you understand?

13 A. I do.

14 Q. And you also understand that
15 during your deposition, you should not be
16 emailing or texting with other people?

17 A. Of course.

18 Q. Approximately how many times have
19 you been deposed before?

20 A. Somewhere between 15 and 20.

21 Q. Do you have any questions for me
22 about the procedure for today's deposition?

23 A. Not at this time.

24 Q. My questions to you today are
25 intended to cover your opinions in both

1 IPR2023-00454 and IPR2023-00455.

2 Understood?

3 A. Yes.

4 Q. And unless you tell me otherwise,
5 I will understand your answers to my questions
6 to apply equally to both IPRs.

7 Is that fair?

8 A. So is it your intent, then, to
9 bounce back and forth between the two IPRs or to
10 deal with one and then the other?

11 Q. To cover both at the same time.

12 A. Okay. I understand.

13 ATTORNEY WARRICK: Counsel, I
14 would just ask on the record that you be clear
15 when you're asking questions that are specific
16 to one patent or the other, given that they are
17 distinct patents with different claim language,
18 among other things.

19 BY ATTORNEY CHANDLER:

20 Q. So, Dr. Przybylski, again, to be
21 clear, unless I state otherwise, my questions
22 are intended to cover both patents and both IPRs
23 at the same time.

24 Understood?

25 A. Understood. I will endeavor to

1 refer to both declarations in parallel in order
2 to make sure I'm answering for both IPRs.

3 (Whereupon, Exhibit Number 1096 in both
4 IPRs was marked for identification and
5 is attached hereto.)

6 BY ATTORNEY CHANDLER:

7 Q. And to that end, I have marked a
8 new exhibit numbered 1096 in each IPR, which
9 I've uploaded into the chat so that everyone can
10 have a copy. And Exhibit 1096 in both IPRs is a
11 computer-generated redline comparing your
12 declaration in IPR2023-00454, marked as
13 Exhibit 2024 to your declaration, and
14 IPR2023-00455, marked as Exhibit 2024.

15 Do you understand?

16 A. Are you representing that those
17 two files are identical?

18 Q. The two Exhibit 1096 files are
19 identical except for the stamp on the bottom
20 right that provides the IPR number.

21 A. And they both are a redline of
22 the '417 showing the changes for the '215.

23 Is that accurate?

24 Q. Correct.

25 A. Understood.

1 Q. As shown in the redline marked as
2 Exhibit 1096, there are many paragraphs in your
3 declaration marked as Exhibit 2024 in
4 IPR2023-00454 that are substantively identical
5 to your declaration marked as Exhibit 2024 in
6 IPR2023-00455.

7 Is that fair?

8 ATTORNEY WARRICK: Objection;
9 form.

10 THE WITNESS: Yes, that's fair.

11 I will note that there are -- can
12 you look at page 21 of 225 in the redline
13 document. It's not rendering properly for me.
14 Is that also on your end?

15 BY ATTORNEY CHANDLER:

16 Q. Yes. So to be clear, it's a
17 computer-generated redline, and computers are
18 not imperfect.

19 A. Tell me about it.

20 Okay. So I will -- where coming
21 across those issues, I will be referring to the
22 master documents, the declarations, to
23 understand exactly what's -- what the redline is
24 trying to convey.

25 Q. Fair enough.

1 And that's what I was going to
2 get at, which is, if it's helpful to you during
3 the deposition today, please feel free to use
4 Exhibit 1096 if you need to find the
5 corresponding paragraph number in your other
6 declaration. For example, towards the end of
7 your declaration, the paragraph numbering
8 between the two declarations starts to diverge,
9 even though there are still many paragraphs
10 toward the end of your declaration that are
11 substantively identical.

12 Understood?

13 A. I see that, yes.

14 ATTORNEY WARRICK: Counsel, I
15 just want to state for the record that, based on
16 at least page 21, as identified by the witness,
17 this is not a completely accurate redline of the
18 two declarations.

19 BY ATTORNEY CHANDLER:

20 Q. Dr. Przybylski, in general, to be
21 clear, I'll be asking you questions today that
22 are not unique to one IPR or the other IPR and,
23 instead, are relevant to both IPRs.

24 Understood?

25 A. Yes, understood.

1 Q. What did Netlist ask you to do in
2 this matter?

3 ATTORNEY WARRICK: Objection;
4 form.

5 THE WITNESS: Attorneys for
6 Netlist asked me to review the IPRs and the
7 documents therein and to formulate opinions
8 vis-a-vis the assertions made therein and in the
9 declarations associated with them.

10 BY ATTORNEY CHANDLER:

11 Q. And when you say "review the
12 IPRs," are you referring to the petition that
13 was filed in each IPR, or to something else?

14 A. To the petitions, yes -- and, as
15 I mentioned, the declarations and the exhibits
16 attached thereto.

17 Q. Did anyone help you with your
18 work in these two IPRs?

19 ATTORNEY WARRICK: Objection;
20 form.

21 THE WITNESS: To the extent that
22 I did communicate with counsel for Netlist on
23 the work as it was progressing.

24 BY ATTORNEY CHANDLER:

25 Q. And when you say "counsel for

1 Netlist," are you referring to the lawyers at
2 Irell & Manella or to someone else?

3 A. Yes, to those two.

4 Q. And to be clear, when you say
5 "those two," you're referring to the lawyers at
6 the law firm named Irell & Manella?

7 A. Yes, correct.

8 Q. What did you do to prepare for
9 today's deposition?

10 A. I reviewed my declaration and
11 the -- some of the principal references referred
12 to in the petition. Those are the -- I did also
13 glance at the petitions and declarations but not
14 to review them in detail.

15 Q. And to be clear, you referred to
16 your declaration in the singular; but you
17 actually have two declarations, one for each
18 IPR. Those declarations overlap, but they're
19 not entirely identical to each other; correct?

20 A. Correct.

21 Q. And did you meet with anyone in
22 preparation for today's deposition?

23 A. Yes.

24 Q. And who attended that meeting?

25 A. Philip Warrick and Annita Zhong.

1 Q. Anyone else?

2 A. No.

3 Q. And when was that meeting, and
4 how long was it?

5 A. We had three meetings over the
6 course of the last several days this week.

7 Q. And for approximately how many
8 hours did you meet to prepare for today's
9 deposition?

10 A. For the meetings per se, they
11 were on the order of about four hours total, I
12 would say.

13 Q. And did you also prepare on your
14 own time by yourself for today's deposition?

15 A. Yes, I did.

16 Q. And for approximately how long?

17 A. Preparation in earnest began last
18 Friday through the weekend and through the first
19 part of this week. So I would say probably
20 around 10 hours or so, maybe a little bit more.
21 I don't know.

22 Q. So within the last two to three
23 weeks, approximately how many hours in total
24 have you spent preparing for today's deposition?

25 A. My answer was for the total

1 amount.

2 Q. So in the last two to three
3 weeks, you believe you spent a total of about 10
4 hours preparing for today's deposition,
5 including both time spent preparing on your own
6 and time spent meeting with the lawyers at
7 Irell & Manella; is that correct?

8 ATTORNEY WARRICK: Objection;
9 form.

10 THE WITNESS: It's probably a
11 little bit more in that counting the meetings
12 with the attorneys from Irell; so call it 15
13 hours approximately. Maybe a little bit more.

14 BY ATTORNEY CHANDLER:

15 Q. So in the past two to three
16 weeks, you believe you spent a total of
17 approximately 15 hours preparing for today's
18 deposition.

19 Is that fair?

20 A. That's fair. I'd have to review
21 my notes to get a more accurate number, but
22 that's a good estimate as we stand right here.

23 Q. As part of your work for Netlist
24 on this matter, did you personally talk to
25 anyone else, such as the inventors or anyone

1 else with experience in the field?

2 A. I don't recall any other meetings
3 other than with the attorneys at Irell.

4 Q. How much are you charging per
5 hour for your time spent on these two IPRs?

6 A. My billing rate for these IPRs is
7 \$550 an hour.

8 Q. In total, approximately how many
9 hours have you spent working as an expert in
10 these two IPRs?

11 A. Including the creation of the
12 declarations, you mean --

13 Q. Yes.

14 A. -- and the preparation for this
15 deposition?

16 Q. Correct.

17 A. The creation of the declarations
18 was a while ago. I don't remember exactly how
19 long -- how much time, but that's -- for the two
20 IPRs together, it was probably on the order of
21 100 hours or so. I don't know. Don't remember
22 well.

23 Q. And approximately how much in
24 total have you billed for the time you have
25 spent working as an expert in these two IPRs?

1 A. That would be the hours spent
2 multiplied by 550, so presumably that's
3 somewhere around \$50,000. But, again, I don't
4 have my invoices in front of me.

5 Q. Aside from these two IPRs, are
6 there other matters where you are engaged by
7 Netlist, either directly or indirectly, to
8 provide expert opinions?

9 ATTORNEY WARRICK: Objection;
10 form and scope.

11 THE WITNESS: Yes.

12 BY ATTORNEY CHANDLER:

13 Q. And could you summarize those
14 other matters.

15 ATTORNEY WARRICK: Same
16 objections.

17 THE WITNESS: There are
18 additional IPRs that I have offered declarations
19 in that are -- my involvement in those have
20 concluded.

21 BY ATTORNEY CHANDLER:

22 Q. Anything else related to Netlist
23 besides the other IPRs that have concluded?

24 A. I believe I offered a claim
25 construction opinion, but that was like two

1 years ago.

2 Q. Anything else?

3 A. Not that I can recall.

4 Q. And the other IPRs where you were
5 engaged by Netlist, either directly or
6 indirectly, what was the general subject matter
7 of those patents?

8 ATTORNEY WARRICK: Objection;
9 form, scope.

10 THE WITNESS: They were IPRs
11 related to other Netlist patents.

12 BY ATTORNEY CHANDLER:

13 Q. And were those other Netlist
14 patents related to the '417 and '215 patents in
15 these IPRs?

16 ATTORNEY WARRICK: Objection;
17 form.

18 THE WITNESS: Well, they're
19 related in that they have common ownership.
20 There are certainly concepts that were common to
21 both, but I don't recall specifically whether
22 the claims overlapped substantially or whether
23 the specifications were identical.

24 There are also pieces of prior
25 art that were common across some of these other

1 cases.

2 BY ATTORNEY CHANDLER:

3 Q. And the other IPRs that you're
4 referring to, were those other IPRs related to
5 each other?

6 ATTORNEY WARRICK: Objection to
7 form.

8 THE WITNESS: Again, they were
9 related to each other based on common ownership.
10 At least two were related to the same patent.
11 Beyond that, I have no specific recollection.

12 BY ATTORNEY CHANDLER:

13 Q. Before this case, when did you
14 first do any work for Netlist? Approximately
15 what time frame?

16 A. I don't recall any engagement for
17 Netlist prior to the immediately precursor IPRs
18 that we just discussed.

19 Q. And so approximately when did you
20 first do any work for Netlist, to your
21 recollection?

22 A. So to my best recollection today
23 is that it would be somewhere in the 2001 -- I'm
24 sorry -- 2021 time frame -- yeah, approximately.

25 Q. Before you were first engaged by

1 Netlist around the year 2021, were you familiar
2 with Netlist as a company?

3 A. Yes.

4 Q. How so?

5 A. As an expert in the DRAM field,
6 I'm aware of lots of activities within that
7 whole industry; and Netlist has certainly been a
8 participant in that over the years.

9 Q. And could you be more specific as
10 to what you recall or knew about Netlist before
11 you were first engaged by Netlist as an expert
12 around the year 2021.

13 ATTORNEY WARRICK: Objection;
14 form.

15 THE WITNESS: I was aware that
16 they participated in the development of novel
17 memory modules, and I believe they directly sold
18 those as well. But I don't know if that was
19 only indirectly or whether it was licensing.

20 BY ATTORNEY CHANDLER:

21 Q. And did you develop that
22 awareness of Netlist as a participant in the
23 industry or as a professor or as a participant
24 in the standards-setting organization? What was
25 the sort of context of your awareness?

1 ATTORNEY WARRICK: Objection;
2 form.

3 THE WITNESS: Principally, as an
4 industry expert that consulted and taught and
5 wrote about the industry.

6 BY ATTORNEY CHANDLER:

7 Q. Before you were first engaged by
8 Netlist around the year 2021, did you know any
9 of the named inventors on the '417 and '215
10 patents identified as Jeffrey C. Solomon and
11 Jayesh R. Bhakta?

12 A. No, I have no recollection of
13 ever having encountered them personally.

14 Q. Do you own any Netlist stock or
15 stock options?

16 A. No.

17 Q. Is your compensation in this case
18 contingent in any way on the outcome of the
19 case?

20 A. No.

21 Q. Are your expert declarations,
22 marked as Exhibit 2024 in these two IPRs,
23 complete? Meaning do they provide a complete
24 statement of all the opinions you intend to
25 express in these IPRs, along with the basis and

1 reasons for those opinions?

2 ATTORNEY WARRICK: Objection;
3 form.

4 THE WITNESS: Yes, they include
5 all of my opinions. The basis for those
6 opinions includes my knowledge as an industry
7 expert, not all of which is written down within
8 the four corners of the declarations.

9 BY ATTORNEY CHANDLER:

10 Q. Are your expert declarations
11 marked as Exhibit 2024 in these two IPRs
12 accurate, meaning they do not have any mistakes
13 as far as you know?

14 A. I certainly encountered the usual
15 number of typographical and other proofreading
16 errors, but nothing of substance.

17 Q. Do you have any present plans to
18 correct or supplement your expert declarations,
19 marked as Exhibit 2024 in these two IPRs?

20 A. No, I have no plans as of this
21 moment.

22 Q. Please look at your CV at the end
23 of your declarations marked as Exhibit 2024 in
24 the two IPRs, and let me know when you're ready
25 to proceed.

1 A. I have in front of me Appendix A
2 of the '0455 IPR -- i.e., attached to the --
3 related to the '215 patent.

4 Q. And as shown in Exhibit 1096,
5 your CV appears to be the same in both of your
6 expert declarations, marked as Exhibit 2024;
7 correct?

8 A. Yes, that is correct.

9 Q. Your CV at the end of your expert
10 declarations, marked as Exhibit 2024 in both
11 IPRs, does not list any of your prior expert
12 testimony; correct?

13 A. That's correct.

14 Q. Why not?

15 A. It is just not part of my CV that
16 I normally keep and distribute.

17 Q. Do you have a list of your prior
18 expert engagements in which you were either
19 deposed or testified at trial?

20 A. I have an informal running list,
21 yes.

22 Q. And do you have access to that
23 now?

24 ATTORNEY WARRICK: Objection;
25 form.

1 THE WITNESS: I don't have a hard
2 copy of it, no.

3 BY ATTORNEY CHANDLER:

4 Q. But on your computer you have
5 access to such a list; correct?

6 ATTORNEY WARRICK: Objection;
7 form.

8 THE WITNESS: Yes.

9 BY ATTORNEY CHANDLER:

10 Q. Could you please summarize for us
11 your prior expert engagements in which you were
12 either deposed or testified at trial.

13 A. So I have been involved in
14 litigation support generally for quite a long
15 while and have been engaged in upwards of 50
16 different matters, of which I have offered
17 testimony in approximately 20 of them and been
18 deposed on either a -- for an IPR or for
19 infringement or invalidity on the order of 15 to
20 20 times, sometimes multiple times per
21 engagement; and have appeared at ITC hearings.
22 And that is an accurate summary.

23 Q. Do you have access to a list of
24 the cases in which you were engaged as an expert
25 and either deposed or testified at trial?

1 ATTORNEY WARRICK: Objection;
2 form.

3 THE WITNESS: I don't keep track
4 of case identifiers. I do keep track of
5 participants.

6 BY ATTORNEY CHANDLER:

7 Q. Sure.

8 So starting with the most recent
9 time frame, can you just go back chronologically
10 and tell us the case participants in which you
11 were the expert and the name of your client.

12 A. I'll have to bring up the file to
13 answer that question.

14 ATTORNEY WARRICK: Counsel, I
15 just want to say, to the extent you're asking
16 the witness to go searching for files, that's
17 not necessarily -- first of all, that's not the
18 same as bringing documents to a deposition and
19 should not be construed as a waiver of any sort
20 of protections that might apply to those
21 documents.

22 BY ATTORNEY CHANDLER:

23 Q. So, Dr. Przybylski, are you able
24 to answer the question?

25 A. I am bringing up my list for --

1 so I can answer your question.

2 Okay. So repeat your question,
3 please.

4 Q. Starting from today and going
5 back chronologically, can you tell us the case
6 participants in which you're the expert and the
7 name of your client?

8 And to keep things orderly, why
9 don't we only take a few years at a time. So I
10 don't need you to tell me your whole life's
11 story, but let's go back in time as to who
12 you've been engaged as an expert by and what the
13 case was and whether you were deposed or
14 testified at trial in that case.

15 A. Okay. So testifying experience
16 most recently is Nelson Bumgardner Conroy PC,
17 and that was Xueshan v. Renaissance.

18 Most recent after that was
19 Freitas & Weinberg LLP. That was in the --
20 offered a claim construction declaration.

21 Prior to that, the client was
22 Amin Turocy & Watson, LLP.

23 Q. For clarification, so, for
24 example, in the claim construction declaration
25 that you offered, who was the party that you

1 offered the claim construction for and who was
2 the opposing party?

3 A. That was Polaris Innovations,
4 Inc., v. Xilinx.

5 Q. Okay.

6 A. Prior to that was -- as I said,
7 Amin, Turocy & Watson, LLP, representing AusTech
8 Computer International and AusTech -- I'm
9 sorry -- and Asus Computer, Inc., and this was
10 offering a rebuttal expert report.

11 Prior to that --

12 Q. And when you say "prior to that,"
13 it would be helpful if you give an approximate
14 time frame. I understand cases --

15 A. We're in 2001 -- I'm sorry.
16 2021-2022 time frame.

17 Q. Uh-huh.

18 A. The Fabricant LLP. Rampart Asset
19 Management, LLC, was the party involved versus
20 NXP. And I offered a claim construction
21 declaration in that matter.

22 Prior to that was Skiermont Derby
23 LLP for Micron, offering a claim construction
24 declaration and four IPR declarations and
25 corresponding depositions.

1 Q. And to be clear, was the client
2 Micron or was the adverse party Micron?

3 A. The adverse party was Micron.

4 Q. And who was the client?

5 A. Netlist. I thought I said that.
6 Perhaps I didn't.

7 Q. Okay. Before that?

8 A. Prior to that, the client was
9 Venable LLP. The client that I was working for
10 was HD Silicon Solutions LLP -- no. I'm sorry.

11 That one I believe was --
12 Microchip Technology was the party I was working
13 for, and HD Silicon Solutions was the adverse
14 party. And there were seven IPRs in that
15 engagement.

16 Q. And approximately what time
17 frame?

18 A. 2021 to 2022.

19 Q. Okay.

20 A. You want me to keep going?

21 Q. Yeah, why don't you keep going
22 back until at least 2018.

23 A. Okay. There's only a few more to
24 get to that time frame.

25 The previous one to that, I

1 think, is Freitas & Weinberg LLP for Aquila
2 Innovations versus AMD, Inc., total of six IPRs,
3 with declarations and depositions accordingly.

4 Prior to that was DLA Piper,
5 representing Toyota Motor Corporation, et al.,
6 versus Broadcom. That was an ITC matter. So it
7 was involving -- I was a testifying expert on
8 domestic industry, my expert report, deposition
9 and at hearing.

10 And prior to that were before
11 2018.

12 Q. I apologize. Could you actually
13 go back to 2016. My mistake.

14 A. 2016.

15 So prior to that was Laurence &
16 Phillips LLP -- IP Law LLP for Polaris versus
17 NVIDIA, eight IPRs in that engagement,
18 corresponding declarations and depositions.

19 And that's the list of my current
20 file. I'd have to go find another file to go
21 beyond that. That was for 2017 and 2018. Is
22 that adequate?

23 Q. For now.

24 Why don't you go ahead and put
25 that aside, and let me know when you're ready

1 for the next question.

2 A. I have closed that window.

3 Q. Dr. Przybylski, have you
4 carefully read Netlist's '417 and '215 patents
5 marked as Exhibit 1001 in each of the IPRs?

6 A. Not recently, no.

7 Q. But in the past?

8 A. It depends on what you mean by
9 "carefully." Certainly there are aspects of it
10 that I paid closer attention to than others, but
11 I did read them to some degree of thoroughness.

12 Q. Did you read them completely?

13 A. I would say I scanned them
14 completely. I read portions of them completely.

15 Q. Do you believe that you
16 understand the '417 and '215 patents in these
17 IPRs?

18 A. Do I understand the disclosure of
19 the specifications? Yes, I do.

20 Q. Do you believe you understand the
21 figures of the '417 and '215 patents?

22 A. You want me to review a specific
23 figure?

24 Q. No. I'm just asking you, when
25 you did review Netlist '417 and '215 patents in

1 the past, do you believe that you understood the
2 figures of the '417 and '215 patents?

3 A. With your permission, I'll pull
4 up the '417 patent and quickly look at the
5 figures to make sure I can answer that
6 accurately.

7 Is that all right?

8 Q. Sure.

9 A. Yes, I understand the figures of
10 the '417 and '215 patents.

11 Q. And do you believe that you
12 understand the claims at the end of the '417 and
13 '215 patents marked as Exhibit 1001 in these two
14 IPRs?

15 ATTORNEY WARRICK: Objection;
16 form.

17 THE WITNESS: Yes, I understand
18 all of the terms that are in the various
19 elements of the claims of those two patents.

20 (Exhibit Number 1071 was previously
21 marked for identification.)

22 BY ATTORNEY CHANDLER:

23 Q. Please turn to Exhibit 1071,
24 which is the same exhibit in both IPRs, and let
25 me know when you're there.

1 A. 1071. Hold on. Is that one of
2 the ones you put in chat?

3 Q. You know, I thought I did, but
4 now that I'm looking --

5 A. There it is. 1071, yes. I'm
6 just going to pull it off of chat rather than
7 trying to -- so that's Perego; right?

8 Q. Yes. Yes.

9 A. I have 7,363,422 to Perego up on
10 one of my screens.

11 Q. Dr. Przybylski, have you
12 carefully read the Perego prior art reference
13 marked as Exhibit 1071 in both IPRs?

14 A. Yes.

15 Q. And do you believe that you
16 understand the Perego reference marked as
17 Exhibit 1071 in both IPRs?

18 A. Yes.

19 (Exhibit Number 1064 was previously
20 marked for identification.)

21 BY ATTORNEY CHANDLER:

22 Q. Please turn to Exhibit 1064,
23 which is the same in both IPRs, and let me know
24 when you're there.

25 A. 1064.

1 Q. It should be in the chat as well.

2 A. Yes. Sorry. I spoke over you.

3 I'm downloading it now.

4 So I have JEDEC standard JEDS79-2
5 from September 2003 in front of me.

6 Q. So, Dr. Przybylski, have you
7 carefully read the JESD79-2 JEDEC standard from
8 September 2003 marked as Exhibit 1064 in both
9 IPRs?

10 A. Have I read all of it? No, I've
11 never read every single word of this standard.
12 I certainly have been familiar with it since
13 before it was introduced, but -- and I'm very
14 familiar with its contents; but every footnote
15 of every figure, no.

16 Q. And when you say that you were
17 familiar with it since before it was introduced,
18 what do you mean by that?

19 A. The DDR2 standard was discussed
20 in the industry prior to its being issued
21 formally by JEDEC and the EIA. So I was aware
22 of its imminent arrival.

23 Q. Were you a member of JEDEC at
24 that time?

25 A. No. JEDEC's members are

1 companies, not individuals.

2 Q. And what were you doing at that
3 time that the DDR2 standard was being discussed
4 in the industry? Were you teaching or
5 consulting or what were you doing?

6 A. I was consulting and staying
7 current with developments in the industry
8 generally.

9 Q. And if you weren't a member of
10 JEDEC at the time and you were consulting, how
11 did you become aware of the development of the
12 DDR2 standard before it was finalized in
13 September of 2003?

14 A. I don't know if there were press
15 reports or not. I have no recollection of that.
16 But certainly with -- in conversation with
17 individuals -- again, not able to recall
18 specific ones; but, in general, the next
19 generation of standard SDRAMs is that its coming
20 is -- is known within the industry, and it's not
21 a secret process.

22 The deliberations are secret and
23 the voting is within the companies, but people
24 talk.

25 Q. And what type of consulting were

1 you doing in the early 2000s?

2 A. Certainly throughout the 1990s
3 and into the 2000s, I was working with
4 semiconductor vendors and systems companies to
5 understand the DRAM marketplace and the changes
6 that were happening within it across the main
7 memory and other -- as applicable to systems
8 that are PC servers and embedded systems.

9 (Exhibit Number 1073 was previously
10 marked for identification.)

11 BY ATTORNEY CHANDLER:

12 Q. Could you please turn to
13 Exhibit 1073, which is the same in both IPRs,
14 and let me know when you have it up on the
15 screen. It's in the chat for everyone's ease of
16 reference.

17 A. I have U.S. Patent Application
18 Publication US 2006/0277355 to Mark Ellsberry in
19 front of me.

20 Q. Dr. Przybylski, have you
21 carefully read the Ellsberry prior art reference
22 marked as Exhibit 1073 in both IPRs?

23 A. Yes, but not recently.

24 Q. Do you believe that you
25 understand the Ellsberry prior art reference

1 marked as Exhibit 1073 in both IPRs?

2 A. Yes.

3 (Exhibit Number 1078 was previously
4 marked for identification.)

5 BY ATTORNEY CHANDLER:

6 Q. Please turn to Exhibit 1078,
7 which is the same in both IPRs, and let me know
8 when you're there. There should be a copy in
9 the chat for everyone's ease of reference.

10 A. There it is.

11 So now I have U.S. Patent
12 7,024,518, to John Halbert, et al., in front of
13 me.

14 Q. Dr. Przybylski, have you
15 carefully read the Halbert prior art reference
16 marked as Exhibit 1078 in both IPRs?

17 A. Yes, but not recently.

18 Q. Do you believe that you
19 understand the Halbert prior art reference
20 marked as Exhibit 1078 in both IPRs?

21 A. Yes.

22 Q. Have you known John Halbert at
23 Intel?

24 A. I don't believe I've ever met
25 him.

1 Q. Have you known Mark Ellsberry,
2 the first named inventor on Exhibit 1073?

3 A. That name is very familiar to me.
4 I believe I've crossed paths with him sometime
5 in the 1990s. But, again, the context I
6 wouldn't recall.

7 Q. Have you known Richard Perego,
8 Fred Ware or Ely Tsern from Rambus, the named
9 inventors on Exhibit 1071?

10 A. I've met Fred Ware on a couple of
11 occasions. The others -- let me see. I don't
12 believe I've met Richard Perego or Ely Tsern.

13 (Exhibit Number 1082 was previously
14 marked for identification.)

15 BY ATTORNEY CHANDLER:

16 Q. Please turn to Exhibit 1082,
17 which is the same in both IPRs, and let me know
18 when you have it on your screen. There should
19 be a copy in the chat for everyone's ease of
20 reference.

21 A. I have U.S. Patent application
22 publication 2003/0039151 in front of me.

23 Q. Dr. Przybylski, have you
24 carefully read the Matsui prior art reference,
25 marked as Exhibit 1082 in both IPRs?

1 A. Yes, but not recently.

2 Q. Do you believe that you
3 understand the Matsui prior art reference marked
4 as Exhibit 1082 in both IPRs?

5 A. I certainly did when I was
6 reviewing it for the purposes of the
7 declaration. I presume that hasn't changed
8 since then.

9 (Exhibit Number 1072 was previously
10 marked for identification.)

11 BY ATTORNEY CHANDLER:

12 Q. Please turn to Exhibit 1072,
13 which is the same in both IPRs, and let me know
14 when you're there.

15 It looks like there's a copy in
16 the chat for everyone's convenience.

17 A. This is U.S. Patent 7,155,627 to
18 Matsui. I have that in front of me.

19 Q. Dr. Przybylski, have you
20 carefully read the Matsui prior art patent
21 marked as Exhibit 1072 in both IPRs?

22 A. This one is less familiar to me,
23 so it was not something I reviewed in great
24 detail when preparing the declarations.

25 Q. Do you believe that you

1 understand the Matsui prior art patent marked as
2 Exhibit 1072 in both IPRs?

3 A. I believe that if I reviewed it,
4 again, in detail, I would be able to understand
5 it, yes. But exactly what it's teaching, I
6 don't have in front of mind right now.

7 (Exhibit Number 1079 was previously
8 marked for identification.)

9 BY ATTORNEY CHANDLER:

10 Q. Please turn to Exhibit 1079,
11 which is the same in both IPRs, and let me know
12 when you have it in front of you. There is a
13 copy of it in the chat for everyone's
14 convenience.

15 A. I have in front of me U.S. Patent
16 application publication 2006/0117152 to Amidi in
17 front of me.

18 Q. Dr. Przybylski, have you
19 carefully read the Amidi prior art reference
20 marked as Exhibit 1079 in both IPRs?

21 A. I don't believe I've read it
22 carefully. I did review it in -- briefly when
23 preparing my declaration, but that was a while
24 ago. I have not reviewed it recently.

25 Q. Do you believe that you

1 understand the Amidi prior art reference marked
2 as Exhibit 1079 in both IPRs?

3 A. I don't recall specifically what
4 it's teaching, but I do firmly believe that on
5 reviewing it, I would understand it.

6 (Exhibit Number 1060 was previously
7 marked for identification.)

8 BY ATTORNEY CHANDLER:

9 Q. Please turn to Exhibit 1060,
10 which is the same in both IPRs, and let me know
11 when you have it in front of you. There is a
12 copy of it in the chat for everyone's
13 convenience.

14 A. I have in front of me JEDEC
15 standard, JESD79 from June 2000 related to
16 double data rate, DDR, SDRAMs.

17 Q. Dr. Przybylski, have you
18 carefully read the JESD79 standard for DDR
19 SDRAMs dated June 2000 marked as Exhibit 1060 in
20 both IPRs?

21 A. As with the previous JEDEC
22 standard, I wouldn't say that I read every
23 footnote of every figure, but I certainly
24 understand the design and operation of DDR
25 SDRAMs as specified by this standard.

1 Q. So to be clear, do you believe
2 that you understand the JESD79 JEDEC standard
3 for DDR SDRAMs dated June 2000 marked as
4 Exhibit 1060 in both IPRs?

5 A. Yes.
6 (Exhibit Number 1062 was previously
7 marked for identification.)

8 BY ATTORNEY CHANDLER:

9 Q. Please turn to Exhibit 1062,
10 which is the same in both IPRs, let me know when
11 you have it in front of you. There's a copy in
12 the chat for everyone's convenience.

13 A. I have in front of me a portion
14 of JEDEC standard now called JESD21-C, a portion
15 totaling 82 pages, beginning at page 4.20.4-1.

16 Q. Dr. Przybylski, have you
17 carefully read the JEDEC21-C prior art reference
18 marked as Exhibit 1062 in both IPRs?

19 A. Again, it's pretty duplicative
20 across the different versions of the RDIMM
21 standard that's being specified here, so not
22 every page has been examined carefully. But I
23 certainly do understand the structure and
24 operation of the RDIMMs that are specified here.

25 Q. So to be clear, do you believe

1 that you understand the JEDEC21-C prior art
2 reference marked as Exhibit 1062 in both IPRs?

3 A. Yes.

4 ATTORNEY CHANDLER: All right.
5 How about we -- we've been going about an hour,
6 so how about we take a break. Go off the
7 record.

8 THE WITNESS: Very good. How
9 long?

10 ATTORNEY CHANDLER: Ten minutes?

11 THE WITNESS: Ten minutes.

12 THE VIDEOGRAPHER: Off the record
13 at 9:04 a.m. Pacific Time.

14 (Recess taken from 9:04 a.m. to
15 9:16 a.m.)

16 THE VIDEOGRAPHER: On the record
17 at 9:16 a.m. Pacific Time.

18 BY ATTORNEY CHANDLER:

19 Q. Dr. Przybylski, are there any
20 corrections or clarifications you'd like to make
21 to your answers so far?

22 A. Not at this time.

23 Q. And just to confirm, during the
24 break, did you consult with anyone?

25 A. Mr. Warrick called me just to

1 make sure everything was going smoothly on my
2 end. I said "yes," and that was the extent of
3 the call.

4 Q. Understood.

5 And are you ready to proceed?

6 A. I am.

7 Q. Dr. Przybylski, I'd like to ask
8 you some questions about the hypothetical person
9 of ordinary skill in the art, starting with the
10 relevant time frame for such a person.

11 So do you have that in mind? And
12 then I'll ask you some more specific questions.

13 A. So I'm turning to page 46 of my
14 declaration for the '417, where that subject
15 matter is addressed.

16 Q. That's fine. And I think as
17 shown in Exhibit 1096, this section of your
18 declaration is the same in both IPRs. But go
19 ahead and get oriented and let me know when
20 you're ready to proceed.

21 A. Yes, I see those sections are
22 essentially the same within the two
23 declarations; and I have, as I said, the '417 in
24 front of me.

25 Q. In the section that you are

1 referring to in your two expert declarations
2 marked as Exhibit 2024 are paragraphs 66 through
3 72 where you discuss the person of ordinary
4 skill in the art; correct?

5 A. Yes. Those are the paragraphs
6 relating to that topic.

7 Q. Now, Samsung's expert, Dr. Wolfe,
8 has taken the position that the effective filing
9 date for the '417 and '215 patents is no earlier
10 than July 1st, 2005.

11 I understand that you contend
12 that the claims in the '417 and '215 patents are
13 entitled to a priority date of at least
14 January 19th, 2005, which is the filing date
15 of the '087 provisional application; but in
16 paragraph 72 of your expert declarations marked
17 as Exhibit 2024, you refer to the 2004 to 2005
18 time frame when discussing the person of
19 ordinary skill in the art.

20 Do you see that?

21 A. I see paragraph 72 begins. I
22 note that in the 2024-2025 time frame,
23 et cetera, yes.

24 Q. To be clear, it's not 2024-2025.

25 A. I'm sorry.

1 Q. 2004 through 2005.

2 A. My apologies. Yes, 2004 to 2005.

3 Q. Okay. Unless stated otherwise,
4 can you please answer my questions today from
5 the perspective of a person of ordinary skill in
6 the art in the 2004 to 2005 time frame?

7 ATTORNEY WARRICK: Objection;
8 form.

9 THE WITNESS: To the best of my
10 ability, I will try to be clear, about the
11 perspective from which I'm answering your
12 questions.

13 BY ATTORNEY CHANDLER:

14 Q. And just so I'm clear, the --
15 please understand that my questions are intended
16 to be asked with respect to the person of
17 ordinary skill in the art in the 2004 to 2005
18 time frame.

19 Understood?

20 A. I understand.

21 ATTORNEY WARRICK: Objection;
22 form.

23 Counsel, Dr. Przybylski is here
24 as an expert, which is his role in these
25 proceedings; and so I would ask that you be

1 specific if you're going to ask him about the
2 perspective of the hypothetical person of
3 ordinary skill in the art.

4 BY ATTORNEY CHANDLER:

5 Q. Dr. Przybylski, did you answer my
6 question by saying, "I understand"? Did I hear
7 that correctly?

8 A. Yes, I understand that that's the
9 perspective on which you will generally be
10 asking questions, but not -- not necessarily all
11 questions.

12 ATTORNEY CHANDLER: And,
13 Mr. Warrick, I would like to remind you that on
14 pages 127 to 130 of the Consolidated Trial
15 Practice Guide dated November 2019, speaking
16 objections are strictly prohibited.

17 Understood?

18 ATTORNEY WARRICK: I am familiar
19 with the Practice Guide.

20 BY ATTORNEY CHANDLER:

21 Q. Dr. Przybylski, could you please
22 answer my questions today in a way that is
23 consistent with the ordinary and accustomed
24 meaning of words to a person of ordinary skill
25 in the art in the 2004 to 2005 time frame?

1 ATTORNEY WARRICK: Objection;
2 form.

3 THE WITNESS: I would endeavor to
4 do that or to be clear when I'm not doing that,
5 to the best of my ability.

6 BY ATTORNEY CHANDLER:

7 Q. Could you please turn toward the
8 beginning of your expert declaration marked as
9 Exhibit 2024 to the section titled "Technology
10 Background," which spans paragraphs 12 through
11 57, and let me know when you're there.

12 And while you're doing that, I'll
13 note that Exhibit 1096 indicates that the
14 substance of paragraphs 12 through 57 is
15 substantially the same in both of your expert
16 declarations.

17 A. Yes. I see that there are some
18 differences between those -- in those paragraphs
19 between those declarations, but they do not have
20 a great deal of substance to them.

21 I am currently looking at page 7
22 of my '417 declaration.

23 Q. And paragraphs 12 through 57 of
24 your expert declarations marked as Exhibit 2024
25 provide a technology background for purposes of

1 these IPRs?

2 A. That is the heading for this
3 section, "Technology Background," yes.

4 Q. In your opinion, are the
5 background technologies summarized in
6 paragraphs 12 through 57 of your expert
7 declaration marked as Exhibit 2024 something
8 that a person of ordinary skill in the art
9 would have known about?

10 A. Yes, I think generally that is an
11 accurate statement.

12 Q. In your opinion, would a person
13 of ordinary skill in the art reading the
14 contents of the Perego reference, marked as
15 Exhibit 1071, have known about the background
16 technologies summarized in paragraphs 12 through
17 57 of your expert declarations marked as
18 Exhibit 2024?

19 A. I think I answered the previous
20 question by saying that, yes, a person of
21 ordinary skill in that time frame would be
22 familiar with this material, regardless of
23 whether they're reading Perego or not.

24 Q. In your opinion, would such a
25 person of ordinary skill in the art have taken

1 into consideration the background technologies
2 summarized in paragraphs 12 through 57 of your
3 expert declaration marked as Exhibit 2024 when
4 trying to understand the contents of the Perego
5 reference marked as Exhibit 1071?

6 ATTORNEY WARRICK: Objection;
7 form.

8 THE WITNESS: I'm not sure what
9 you mean by "taking into account." It's -- this
10 background technology that I refer to is
11 something that a person of ordinary skill would
12 be familiar with while reading Perego or
13 otherwise. To the extent that they're taking
14 any of it in particular into account, I'm not --
15 have not rendered an opinion on that.

16 BY ATTORNEY CHANDLER:

17 Q. In your opinion, would a person
18 of ordinary skill in the art have taken into
19 consideration the background technologies
20 summarized in paragraphs 12 through 57 of your
21 expert declaration marked as Exhibit 2024 when
22 trying to understand the contents of the '417
23 and '215 patent applications?

24 ATTORNEY WARRICK: Objection;
25 form.

1 THE WITNESS: Again, this
2 background material is something that a person
3 of ordinary skill would have been generally
4 familiar with. I do not know specifically what
5 aspects of that they would necessarily have to
6 call on in order to understand the patents at
7 issue here.

8 BY ATTORNEY CHANDLER:

9 Q. In your opinion, is the
10 technology background summarized in paragraphs
11 12 through 57 of your expert declaration marked
12 as Exhibit 2024 relevant to the field of art for
13 the '417 and '215 patents?

14 ATTORNEY WARRICK: Objection;
15 form.

16 THE WITNESS: The technology
17 background is there principally to help the
18 board understand the technologies at issue here.
19 They do -- the content of that section does
20 generally relate to the subject matter of the
21 '417 and the '215 and the prior art references
22 cited by the petitions.

23 Beyond that, I have nothing
24 further to add.

25 ///

1 BY ATTORNEY CHANDLER:

2 Q. Please turn to paragraph 32 of
3 your expert declarations marked as Exhibit 2024.
4 Let me know when you're there.

5 And while you're doing that, I'll
6 note that Exhibit 1096 indicates that the
7 substance of paragraph 32 is the same in both of
8 your expert declarations.

9 A. I am at paragraph 32.

10 Q. In paragraph 32 of your expert
11 declarations marked as Exhibit 2024, you
12 referred to DIMMs, UDIMMs and RDIMMs; correct?

13 A. I don't actually call them
14 RDIMMs. I called them registered DIMMs at the
15 top of page 23 of my '417 declaration.

16 But that minutia apart, that is
17 generally true. I referred to DIMMs, UDIMMs or
18 unbuffered DIMMs and registered DIMMs in that
19 paragraph.

20 Q. And to be clear, registered DIMMs
21 are commonly referred to by persons of ordinary
22 skill in the art as RDIMMs; correct?

23 A. Yes. There are many acronyms
24 that are very similar in this whole art, but
25 RDIMM is one that is principally used to refer

1 to JEDEC standardized, registered DIMMs.

2 Q. In your opinion, would a person
3 of ordinary skill in the art have known about
4 DIMMs, UDIMMs and RDIMMs?

5 A. Yes. It's within the scope of
6 knowledge or familiarity of a person of ordinary
7 skill to at least be familiar with those types
8 of memories and, generally speaking, what they
9 are about.

10 Q. And could you pull up the '417
11 and '215 patents marked as Exhibit 1001. And in
12 the '417 patent, go to Column 6 starting around
13 line 46. And let me know, and I'll point you to
14 the similar location in the other patent.

15 A. All right. So I have the '417
16 up, Column 6.

17 Do you want me to talk about this
18 first, or do you want me to bring up the other
19 one in parallel?

20 Q. I'll -- let's bring up the other
21 one in parallel because the specifications of
22 the two patents are the same, so I want to cover
23 both patents at the same time.

24 A. Sure.

25 Q. So in the '215 patent, the

1 corresponding text starts at Column 5, line 66.

2 A. Give me a second to bring that
3 one up, please.

4 Did you put the '215 in chat? I
5 didn't believe we actually pulled that one down?

6 Oh, I see. They're both there.
7 That's the '417. That's the '215. Okay.

8 Q. So do you have in front of you
9 the '417 patent, Column 6, line 46, and then
10 also '215 patent at Column 5, line 66?

11 A. Just getting there with respect
12 to the '215. Half a second more.

13 Yes, I have both of them up in
14 front of me now.

15 Q. And the '417 and '215 patents
16 both refer to DIMMs, UDIMMs and RDIMMs; correct?

17 A. Among others, yes.

18 Q. The '417 and '215 patents also
19 refer to other types of memory modules, such as
20 SO-DIMMs, FB-DIMMs, and RBDIMMs; correct?

21 A. Yes, they do.

22 Q. In your opinion, would a person
23 of ordinary skill in the art have known about
24 SO-DIMMs, FB-DIMMs and RBDIMMs?

25 A. SO-DIMMs, certainly. They were

1 relatively common and important. FB-DIMMs are
2 much rarer and would -- a POSITA in that time
3 frame might not have had any familiarity with
4 FB-DIMMs as a course of their employment.

5 Similarly, RBDIMMs are -- I'm not
6 familiar exactly with what that is referring to.
7 It's not a JEDEC standardized DIMM, so -- that
8 I'm familiar with.

9 Q. So if I understand correctly,
10 SO-DIMMs and FB-DIMMs were known, but SO-DIMMs
11 were more widely known than FB-DIMMs? Would
12 that be fair?

13 ATTORNEY WARRICK: Objection;
14 form.

15 THE WITNESS: That's not quite
16 what I said. I think that a POSITA in 2004-2005
17 would not necessarily have had any exposure to
18 FB-DIMMs. They would have had some exposure,
19 most likely, with SO-DIMMs.

20 I'm not even familiar when the
21 FB-DIMMs were formally standardized. I think it
22 was after this time frame. I'm not sure.

23 BY ATTORNEY CHANDLER:

24 Q. The inventors of the '417 and
25 '215 patents knew about FB-DIMMs; correct? They

1 put it in their patent application.

2 ATTORNEY WARRICK: Objection;
3 form.

4 THE WITNESS: Yes, they did
5 mention them in Columns 5 and 6 respectively.
6 But, again, what I said is I don't know formally
7 when those standards were issued by JEDEC.

8 BY ATTORNEY CHANDLER:

9 Q. Were SO-DIMMs and FB-DIMMs known
10 by the time of the '417 and '215 patents,
11 regardless of whether JEDEC had formally issued
12 standards for them?

13 ATTORNEY WARRICK: Objection;
14 form.

15 THE WITNESS: In the time frame
16 2004-2005, I don't know whether they were
17 known -- FB-DIMMs were known at that time or
18 not.

19 BY ATTORNEY CHANDLER:

20 Q. But they were known to the
21 inventors?

22 ATTORNEY WARRICK: Objection to
23 form.

24 THE WITNESS: I don't know at
25 what point in the prosecution history those

1 particular references were added to the
2 specification or whether it was a result of a --
3 the initial filings or whether those particular
4 references were added later. I'm just not
5 familiar.

6 BY ATTORNEY CHANDLER:

7 Q. Do you have patents yourself?

8 A. Yes.

9 Q. And you understand that once a
10 patent application is filed, it's not permitted
11 to add to the patent specification; correct?

12 ATTORNEY WARRICK: Objection;
13 form.

14 THE WITNESS: There are
15 provisional applications from which priority is
16 given; and then there are the full,
17 nonprovisional applications that are a more
18 complete description of the subject matter of
19 the invention. So there is a clear difference
20 between those two, at least.

21 BY ATTORNEY CHANDLER:

22 Q. You provided the opinion that the
23 '417 and '215 patents are entitled to a priority
24 date of January 19th, 2005.

25 As of that date, January 19th,

1 2005, in your opinion, do the claims of the '417
2 and '215 patents cover memory modules that are
3 either SO-DIMMs or FB-DIMMs?

4 ATTORNEY WARRICK: Objection;
5 form.

6 BY ATTORNEY CHANDLER:

7 Q. Or do you not know?

8 A. Whether -- by "covered," do you
9 mean that those types of modules infringe those
10 claims? Is that what you're meaning?

11 Q. Well, it's usually, rather than
12 the word "infringe," we would say are
13 "embodiments." So could an SO-DIMM or an
14 FB-DIMM embody the claims of the '417 and '215
15 patents as of January 19th, 2005, the date
16 that you say the claims are entitled to a
17 priority date of?

18 ATTORNEY WARRICK: Objection;
19 form.

20 THE WITNESS: That's not a
21 terminology that I'm familiar with. I think
22 that it -- the way that it would normally be
23 expressed is: Are those types of modules within
24 the scope of the claims at issue? And that's
25 not a subject of my opinions in this matter.

1 BY ATTORNEY CHANDLER:

2 Q. It's a little bit different, so I
3 want to just be clear about this.

4 So when you provided the opinion
5 that the claims were entitled to a priority date
6 of January 19th of 2005, you were indicating
7 that there was support in the specification for
8 those claims.

9 And my question is: Is there
10 support in the specification for the claims of
11 the '417 and '215 patents, as of January 19th,
12 2005, with respect to an SO-DIMM or an FB-DIMM
13 that practices the claims or embodies the
14 claims?

15 ATTORNEY WARRICK: Objection;
16 form.

17 THE WITNESS: That's not
18 something I've opined on, and I don't know that
19 off the top of my head, sitting here today.

20
21 ATTORNEY CHANDLER: I'd like to
22 introduce a new exhibit in the chat, which I'll
23 mark as Exhibit 1103.

24 ///

25 ///

1 (Whereupon, Exhibit Number 1103 in both
2 IPRs was marked for identification and
3 is attached hereto.)

4 BY ATTORNEY CHANDLER:

5 Q. It should be coming to everyone.
6 It's the same document in both IPRs. I've
7 provided two copies. The only difference in the
8 two copies is the case number in the stamp in
9 the bottom right.

10 Please let me know when you have
11 Exhibit 1103 in front of you.

12 A. I have Netlist Technology
13 Tutorial dated May 8th, 2017.

14 Q. Correct. Exhibit 1103 is the
15 technology tutorial prepared by Netlist.

16 Have you seen Exhibit 1103
17 before?

18 A. I've seen the cover page before.
19 I have not reviewed it in detail, no.

20 Q. Please turn to page 2 of
21 Exhibit 1103, and let me know when you're there.

22 A. I am at page 2.

23 Q. Does page 2 of Exhibit 1103 show
24 a picture of a DIMM, which is to say a dual
25 in-line memory module?

1 A. It appears to show a memory
2 module that it's claiming is a DIMM. It's not
3 clear whether that's a JEDEC standardized DIMM.
4 It appears not to be, but I don't know for a
5 fact one way or the other. It has the right
6 form factor to be a considered a DIMM in the
7 most general understanding of that term.

8 Q. Does page 3 of Exhibit 1103 show
9 a DIMM memory module at the bottom?

10 A. Yes. This appears to be a
11 Samsung-manufactured DIMM. It looks like an
12 RDIMM, but I don't know for a fact. I'd have to
13 look up the product numbers to be sure exactly
14 what it is.

15 Q. Do you agree that SDRAM memory
16 devices emerged in the 1990s and have been
17 standardized by JEDEC?

18 A. Have to be careful with regard to
19 the term "SDRAM," because sometimes it's
20 referring just to any variety of synchronous
21 DRAM. So synchronous with a small s.

22 If it's a JEDEC standardized
23 device, it's all caps, and the S is standing for
24 synchronous with a capital S. And those are the
25 devices that are standardized by JEDEC.

1 There are a great many
2 nonstandardized, small s, synchronous, dynamic
3 random-access memories that are not covered by
4 JEDEC standards.

5 Q. Do you agree that SDRAM, all
6 caps, has evolved in several generations,
7 including DDR and DDR2?

8 ATTORNEY WARRICK: Objection;
9 form; also scope as to the question and as to
10 the exhibit, 1103.

11 THE WITNESS: Yes. There are --
12 have been a number of SDRAM standards developed
13 by JEDEC, one of which is called DDR SDRAM,
14 short for double data rate synchronous dynamic
15 random-access memory, as well DDR2 and so forth.

16 ATTORNEY CHANDLER: And I'll note
17 for the court reporter, I said D -- as in dog.
18 (Incidental comments made off the
19 stenographic record.)

20 THE WITNESS: We'll be saying
21 "DDR" a lot.

22 BY ATTORNEY CHANDLER:

23 Q. Dr. Przybylski, DDR and DDR2 were
24 JEDEC standards that a person of ordinary skill
25 in the art knew about by the time of the '417

1 and '215 patents; correct?

2 A. Again, you have to be careful
3 with the terminology, because DDR, standing for
4 double data rate, applies to many different
5 contexts. To be clear that you're talking about
6 the JEDEC standard, you should say DDR SDRAM
7 JEDEC standard.

8 Q. So to be clear, the DDR SDRAM
9 JEDEC standard and DDR2 SDRAM JEDEC standard
10 were known to a person of ordinary skill in the
11 art by the time of the '417 and '215 patents;
12 correct?

13 ATTORNEY WARRICK: Objection;
14 form.

15 THE WITNESS: Yes. We looked at
16 JEDEC standardizing documents that predate the
17 2004-2005 time frame that we're talking about
18 and so that they -- a POSITA in that time frame
19 would have been familiar with them.

20 BY ATTORNEY CHANDLER:

21 Q. For example, please turn back to
22 Exhibit 1060, the JEDEC JESD79 standard for DDR
23 SDRAM dated June 2000. Let me know when you
24 have it in front of you.

25 A. I have the cover page of that in

1 front of me.

2 Q. You do not dispute that a person
3 of ordinary skill in the art would have known
4 about the JEDEC JESD79 standard for DDR SDRAM
5 dated June 2000 marked as Exhibit 1060 in both
6 IPRs; correct?

7 ATTORNEY WARRICK: Objection to
8 form.

9 THE WITNESS: I do not dispute
10 that.

11 BY ATTORNEY CHANDLER:

12 Q. And please turn to Exhibit 1062.
13 Let me know when you have that in front of you.

14 A. I have the first page of
15 Exhibit 1062 in front of me.

16 Q. You do not dispute that a person
17 of ordinary skill in the art would have known
18 about the JEDEC JESD21-C design specification
19 for DDR SDRAM registered DIMM dated January 2002
20 marked as Exhibit 1062 in both IPRs; correct?

21 ATTORNEY WARRICK: Objection;
22 form.

23 THE WITNESS: Again, you have to
24 be careful with terminology, because the JEDEC
25 Standard 21-C is about 3,000 pages in total.

1 What this exhibit is, is one small portion of
2 that overall standard, the design specification
3 for PC2100 and PC1600 DDR SDRAM registered DIMMs
4 dated January 2002.

5 BY ATTORNEY CHANDLER:

6 Q. And you do not dispute that a
7 person of ordinary skill in the art would have
8 known about that, which is marked as
9 Exhibit 1062 in both IPRs; correct?

10 ATTORNEY WARRICK: Objection;
11 form.

12 THE WITNESS: I do not dispute
13 that.

14 BY ATTORNEY CHANDLER:

15 Q. Please turn to Exhibit 1064. Let
16 me know when you have it in front of you.

17 A. I have the first page of the
18 JEDEC standard JESD79-2 for DDR2 SDRAM
19 specification dated September 2003 in front of
20 me.

21 Q. And you do not dispute that a
22 person of ordinary skill in the art would have
23 known about that standard, which is marked as
24 Exhibit 1064 in both IPRs; correct?

25 ATTORNEY WARRICK: Objection;

1 form.

2 THE WITNESS: I do not dispute
3 that.

4 (Exhibit Number 2020 was previously
5 marked for identification.)

6 BY ATTORNEY CHANDLER:

7 Q. Take a look at Exhibit 2020,
8 which I'll put in the chat. It was previously
9 marked by Netlist, but I'll try to put it in the
10 chat for everyone's ease of reference. It's the
11 same exhibit in both IPRs. And let me know when
12 you have it.

13 A. It has not shown up for me yet.

14 Oh, 2020, here we go.

15 I have in front of me the first
16 page of Exhibit 2020 titled "JEDEC Standard for
17 DDR2 SDRAM Specification," Standard Number
18 JESD79-2B, dated January 2005.

19 Q. And you do not dispute that a
20 person of ordinary skill in the art would have
21 known about that JEDEC standard marked as
22 Exhibit 2020 in both IPRs; correct?

23 ATTORNEY WARRICK: Objection;
24 form.

25 THE WITNESS: This standard was

1 publicized in 2005. The time frame that we're
2 generally discussing is 2004-2005. So certainly
3 by the end of that time frame, this particular
4 revision of the JESD79-2 standard would have
5 become into the general knowledge of a POSITA at
6 that time -- in that time frame.

7 (Exhibit Number 2031 was previously
8 marked for identification.)

9 BY ATTORNEY CHANDLER:

10 Q. Please take a look at
11 Exhibit 2031 that you cited in your declaration.
12 And I'll also put a copy in the chat for ease of
13 reference. It's the same exhibit in both IPRs.
14 Let me know when you have it in front of you.

15 A. Downloading now.

16 Okay. I'm looking at JEDEC
17 Standard Number 21-C, page 4 dash -- sorry --
18 page 4.1.2.10-1. The first page of "Appendix X:
19 Specific SPDs for DDR2 SDRAMs."

20 Q. And you cited Exhibit 2031 in
21 your declarations marked as Exhibit 2024;
22 correct?

23 A. Yes. I see at least one
24 reference to Exhibit 2031 on page 46 of my '417
25 declaration.

1 Q. And you do not dispute that a
2 person of ordinary skill in the art would have
3 known about the JEDEC standard for specific SPDs
4 for DDR2 SDRAM, marked as Exhibit 2031 in both
5 IPRs; correct?

6 ATTORNEY WARRICK: Objection;
7 form.

8 THE WITNESS: This standard was
9 made public with Release 13 of JEDEC Standard
10 21-C. There's no specific date on it that I see
11 at the top. So without referring specifically
12 to the release notes for Release 13, can't say
13 precisely when this becomes into the public
14 domain.

15 We may be able to determine that
16 from looking at the standard for the DIMM that
17 you're saying with the DDR2 SDRAM DIMMs and see
18 if it refers to this particular standard.

19 BY ATTORNEY CHANDLER:

20 Q. And did you review the standard
21 for DDR2 DIMMs -- you just referred -- I'm
22 trying to understand.

23 Did you review the standard that
24 you just referred to in your last answer?

25 A. In my last answer, I referred

1 generically to DDR2 SDRAM DIMM standards, of
2 which there are several; and I didn't refer to
3 any one in particular.

4 Q. Explain your last answer a little
5 bit more, then.

6 A. I'm sorry. Was that a question?

7 Q. Yes. Could you please clarify
8 what you were trying to convey with your last
9 answer, then.

10 ATTORNEY WARRICK: Objection;
11 form.

12 THE WITNESS: My last answer was
13 the one where I was referring to the plurality
14 of DDR2 SDRAM DIMM standards. Is that the
15 question that you want me to clarify -- the
16 answer that you want me to clarify? I'm really
17 quite confused at this point.

18 BY ATTORNEY CHANDLER:

19 Q. I was just trying to understand
20 what you were trying to convey with respect to
21 my question of whether a person of ordinary
22 skill in the art would have known about
23 Exhibit 2031, which you cited in your expert
24 declarations.

25 ATTORNEY WARRICK: Objection;

1 form.

2 THE WITNESS: My first answer
3 with regard to that is that we don't have in
4 front of us documentation of when Release 13 was
5 made public. So we can't say with certainty
6 whether a POSITA of the 2004-2005 time frame
7 would have access to this particular Appendix X.

8 BY ATTORNEY CHANDLER:

9 Q. I guess I'm a little confused,
10 then. Why were you citing Exhibit 2031 in your
11 expert declarations marked as Exhibit 2024?

12 And the related question is: Do
13 you believe a person of ordinary skill in the
14 art would know about Exhibit 2031?

15 (Interruption by the court reporter to
16 clarify the record.)

17 BY ATTORNEY CHANDLER:

18 Q. And a related question is: Do
19 you believe a person of ordinary skill in the
20 art would have known about Exhibit 2031?

21 ATTORNEY WARRICK: Objection;
22 form.

23 THE WITNESS: So there's two
24 questions pending. Can we deal with one at a
25 time, please.

1 BY ATTORNEY CHANDLER:

2 Q. Sure.

3 A. So with regard to my citation to
4 Exhibit 2023 --

5 Q. No. 2031.

6 A. 2031 -- oh, I'm sorry. Yes. My
7 apologies. Look at the wrong thing.
8 2031.

9 I at least refer to it in the --
10 in context of paragraph 65 of my '417
11 declaration where I'm using it to support the
12 idea that the Court's construction of rank is
13 not consistent with the plain and ordinary
14 meaning, as captured by this section of
15 JESD21-C.

16 Q. And you cite Exhibit 2031
17 elsewhere in your declaration as well; correct?

18 A. I'm checking.

19 I see a reference to that
20 exhibit in paragraph 182.

21 Q. And also the next paragraph as
22 well; right?

23 A. Yes, but not by number there; in
24 paragraph 183, yes.

25 Q. So getting back to my original

1 question, in your opinion would a person of
2 ordinary skill in the art have known about the
3 JEDEC standard marked as Exhibit 2031 in both
4 IPRs?

5 ATTORNEY WARRICK: Objection;
6 form.

7 THE WITNESS: I believe that a
8 person of ordinary skill would be familiar with
9 generally the concept of SPDs, determining -- or
10 helping the memory controller understand the
11 nature and characteristics of the module it's
12 controlling.

13 I, again, I don't have a specific
14 date in front of me for this particular
15 revision. So without that, can't know for sure
16 whether it falls within the specified time frame
17 or not.

18 BY ATTORNEY CHANDLER:

19 Q. But at least when you were
20 preparing your expert declarations marked as
21 Exhibit 2024, you thought that it was reasonable
22 to cite to Exhibit 2031 for purposes of claim
23 construction of the '417 and '215 patents and
24 also for purposes of understanding the Perego
25 prior art reference; correct?

1 ATTORNEY WARRICK: Objection;
2 form.

3 THE WITNESS: I did, in fact,
4 cite to this document in both those portions of
5 my declaration, yes.

6 (Whereupon, Exhibit Number 1104 in both
7 IPRs was marked for identification and
8 is attached hereto.)

9 ATTORNEY CHANDLER: I'd like to
10 mark a new exhibit, which will be Exhibit 1104,
11 same document in both IPRs, only difference
12 being the case number stamped in the bottom
13 right. I'll put copies of Exhibit 1104 in the
14 chat.

15 Again, the two copies are the
16 same, so you're welcome to open either one.
17 Just let me know when you have it on your
18 screen.

19 THE WITNESS: I am looking at the
20 cover page of "JEDEC Standard, JESD79D" from
21 January 2004, "Double Data Rate (DDR), SDRAM
22 Specification."

23 BY ATTORNEY CHANDLER:

24 Q. And you do not dispute that a
25 person of ordinary skill in the art would have

1 known about the JESD79D standard for DDR SDRAM
2 marked as Exhibit 1104 in both IPRs; correct?

3 ATTORNEY WARRICK: Objection;
4 form. Also objection; scope, as to the question
5 and the exhibit, 1104.

6 THE WITNESS: No, I don't dispute
7 that. We've already seen JESD79 from the year
8 2000, if I remember correctly. And this is just
9 a revision of that original specification
10 standard.

11 BY ATTORNEY CHANDLER:

12 Q. And, in fact, if you search the
13 '417 and '215 patents for "79D," you'll see the
14 patents incorporate by reference the JEDEC
15 standard JESD79D, which I've now marked as
16 Exhibit 1104; correct?

17 A. I don't know that off the top of
18 my head. If you want to point me to a column
19 and line number, then we can confirm that.

20 Q. Sure. The fastest thing is just
21 search for "79D"; or if you want to scroll, go
22 to Column 23 of the '417 patent, line 52; or you
23 can go to Column 21 of the '215 patent, line 37
24 or so.

25 A. Yes. At least in the '417, it's

1 incorporated by reference, as you said.

2 Q. And also the '215 patent,
3 Column 21, line 37, 38, around there? The
4 JESD79D standards incorporate by reference the
5 same standard that I marked as Exhibit 1104;
6 correct?

7 A. I will make a note that the
8 specification of the '417 and, presumably, the
9 '215 have the date wrong for that particular
10 standard. They show it as February of 2004.
11 But on the cover sheet, it -- it's listed as
12 January. So I don't know why that error is
13 there, but just noting it for the record.

14 (Whereupon, Exhibit Number 1106 in both
15 IPRs was marked for identification and
16 is attached hereto.)

17 ATTORNEY CHANDLER: Let me mark
18 another exhibit. It will be 1106. Again, it
19 will be the same document in both IPRs, the only
20 difference being the case number that's stamped
21 in the bottom right. I've put both copies of
22 Exhibit 1106 in the chat.

23 BY ATTORNEY CHANDLER:

24 Q. Please let me know when you have
25 Exhibit 1106 open.

1 A. I am looking at JEDEC Standard
2 21-C, page 4.1.2.4-1, which is the first page of
3 Appendix D of that -- of some larger portion of
4 that standard.

5 Q. And Exhibit 1106 is similar to
6 Exhibit 2031 that we looked at earlier and that
7 you cited in your expert declarations; however,
8 Exhibit 1106 is for DDR SDRAM; whereas,
9 Exhibit 2031 that you cited is for DDR2 SDRAM;
10 correct?

11 ATTORNEY WARRICK: Objection;
12 form. Also, objection; scope as to the question
13 and the exhibit, 1106.

14 THE WITNESS: Can you repeat the
15 question, please. I lost it in the objection.
16 BY ATTORNEY CHANDLER:

17 Q. Exhibit 1106 is similar to
18 Exhibit 2031 that we looked at earlier and that
19 you cited in your expert declaration; however,
20 Exhibit 1106 is for DDR SDRAM; whereas,
21 Exhibit 2031 that you cite is for DDR2 SDRAM;
22 correct?

23 ATTORNEY WARRICK: Same
24 objections.

25 THE WITNESS: These two documents

1 are, in fact, similar. They have -- principally
2 consist of a table with similar but not
3 identical elements within them, or at least the
4 name has changed over time. But -- yeah, so
5 you're correct in that they are similar.

6 BY ATTORNEY CHANDLER:

7 Q. And both the '417 and '215
8 patents refer to the SPD, which refers to serial
9 presence detect; correct? For example, the
10 bottom of Column 19 of the '417 patent and the
11 bottom half of Column 17 of the '215 patent.

12 A. Yes. I see in the '417
13 Column 19, starting at line 56, that memory
14 modules typically include a serial presence
15 detect device 240; and then it goes on to
16 describe how it's effected and what it
17 characterizes.

18 Q. And there's a corresponding
19 disclosure in the '215 patent starting in the
20 middle of Column 17 and carrying over to the
21 next column; correct?

22 A. 17.

23 Yes, the disclosures appear to be
24 identical.

25 Q. In the discussion of the SPD in

1 the '417 and '215 patents, there's reference to
2 various bytes, such as byte 3, defining the
3 number of row address bits, byte 4, defining the
4 number of column address bits, et cetera; is
5 that correct?

6 A. Yes. That's how it's described
7 in the specification of the '417 and '215.

8 Q. And Exhibit 1106 provides the --
9 the corresponding information about those bytes;
10 correct?

11 ATTORNEY WARRICK: Objection;
12 form.

13 THE WITNESS: Byte 3 --
14 (Witness reviews document.)

15 So there are some differences
16 between how the fields of the SPD are described
17 in the specifications of the '417 and '215
18 relative to their textual descriptions in
19 Exhibit 1106. But there -- at least to the
20 extent that I've reviewed, they are referring to
21 the same general concepts.

22 Good time for another break?

23 BY ATTORNEY CHANDLER:

24 Q. Almost.

25 Do you believe a person of

1 ordinary skill in the art would be familiar
2 with the --

3 A. I'm sorry.

4 Q. Do you believe a person of
5 ordinary skill in the art would be familiar with
6 Exhibit 1106 in both IPRs?

7 ATTORNEY WARRICK: Objection;
8 form.

9 THE WITNESS: Well, again, we
10 don't have a date related to Release 11 of JEDEC
11 Standard 21-C, which would clarify exactly when
12 this became into the public domain; but it is
13 highly likely that a POSITA, as of 2004-2005,
14 would be familiar with at least the existence,
15 if not the details, of Exhibit 1106.

16 ATTORNEY CHANDLER: Why don't we
17 go ahead and take a break.

18 THE WITNESS: Very good. Ten
19 minutes again?

20 ATTORNEY CHANDLER: Sure.

21 THE VIDEOGRAPHER: Off the record
22 at 10:17 a.m. Pacific Time.

23 (Recess taken from 10:17 a.m. to
24 10:28 a.m.)

25 THE VIDEOGRAPHER: On the record

1 at 10:28 a.m. Pacific Time.

2 BY ATTORNEY CHANDLER:

3 Q. Please turn to page 4 of
4 Exhibit 1103, and let me know when you're there.

5 A. 1103. We're referring back to
6 the tutorial; correct?

7 Q. Yes.

8 A. And page 4?

9 Q. Yes.

10 A. "SDRAM Fundamentals"; correct?

11 Q. Yes.

12 A. Very good.

13 Q. Do you agree that a given SDRAM
14 memory device contains several sections called
15 banks, with a B, as in boy?

16 ATTORNEY WARRICK: Objection;
17 form, scope.

18 THE WITNESS: You're referring
19 specifically to JEDEC standardized SDRAMs?

20 BY ATTORNEY CHANDLER:

21 Q. As an example, yes.

22 ATTORNEY WARRICK: Same
23 objections.

24 THE WITNESS: Yes, JEDEC
25 standardized SDRAMs include sections called

1 banks.

2 BY ATTORNEY CHANDLER:

3 Q. With a B, as in boy; correct?

4 A. Correct.

5 Q. And do you agree that each bank
6 with an SDRAM memory device consists of rows and
7 columns of memory?

8 ATTORNEY WARRICK: Objection;
9 form, scope.

10 THE WITNESS: Yes, generally
11 speaking, DRAMs are logically organized into
12 banks containing rows and columns.

13 BY ATTORNEY CHANDLER:

14 Q. Do you believe a person of
15 ordinary skill in the art would have known what
16 is shown here on page 4 of Exhibit 1103?

17 ATTORNEY WARRICK: Objection;
18 form, scope.

19 THE WITNESS: In the time frame
20 we're talking about, 2004-2005, I believe that a
21 POSITA would generally be familiar with the
22 internal logical structure of DRAMs generally
23 and JEDEC standardized SDRAMs in particular.

24 BY ATTORNEY CHANDLER:

25 Q. And you used the term "POSITA,"

1 which is an abbreviation for a person of
2 ordinary skill in the art; correct?

3 A. Are you okay with my using the
4 acronym?

5 Q. I am. I just want to make clear
6 that we're referring to the same thing.

7 A. Yes, we are.

8 Q. Turning to page 5 of
9 Exhibit 1103 -- let me know when you have that
10 in front of you.

11 A. Page 5, yes.

12 Q. Do you agree that a rank, with an
13 R, is a set of DRAMs that are written to or read
14 from together?

15 ATTORNEY WARRICK: Objection;
16 form, scope.

17 THE WITNESS: That's not one of
18 the constructions that's being considered in
19 this particular set of IPRs, but it's a
20 colloquial understanding for the purposes of
21 this technology overview.

22 In the context of DIMM that's
23 shown in the bottom half of that figure, it
24 illustrates two ranks of memory devices that
25 are, in fact, read or written together.

1 BY ATTORNEY CHANDLER:

2 Q. Is it common for a rank of memory
3 devices to be written to or read from together?

4 ATTORNEY WARRICK: Objection;
5 form.

6 THE WITNESS: It's -- yes, it's
7 common that that is how the DRAMs in a rank are
8 used. It is not exclusively how they're used,
9 in particular with regard to certain memory
10 structures. Certain DIMM types, you could have
11 partial rank reads and writes.

12 BY ATTORNEY CHANDLER:

13 Q. Could you explain that a little
14 bit more, what you're referring to.

15 A. If you wish to write less than 64
16 bits at a time -- in other words, to only
17 involve a subset of the DRAMs in a rank -- you
18 can do that. There are mechanisms in place
19 within the JEDEC standardized DIMMs in
20 particular. And so you can write them all
21 together, but you don't have to.

22 Q. And at a high level, what is the
23 mechanism that you're referring to in the JEDEC
24 standard that permits writing to less than the
25 full rank of memory devices?

1 A. The way it's implemented within
2 the JEDEC standardized DRAMs and DIMMs, there is
3 a write mask feature that facilitates that
4 functionality.

5 Q. When the write mask feature is
6 being used, would it still be common to refer to
7 all of the DRAMs that together form the width of
8 the memory module to refer to those as a rank,
9 even if in a given write operation, the mask
10 results in only a subset of those DRAMs being
11 written to?

12 ATTORNEY WARRICK: Objection;
13 form.

14 THE WITNESS: Yes, because the
15 JEDEC standard -- certain -- certain of the
16 JEDEC standards refer to those collections of
17 DRAMs as "ranks." So a POSITA looking to the
18 standard for the meaning of the terminology in
19 that context, those collections of 8 DRAMs are
20 referred to formally as a rank in that context.

21 BY ATTORNEY CHANDLER:

22 Q. In the example where a mask is
23 being used as part of a write command such that
24 only a subset of the memory devices in a rank
25 actually write the data to memory, am I correct

1 that all of the memory devices in the rank
2 receive the write command; but in addition to
3 that, there's a subset of the memory devices
4 that receive the mask, and it's the mask that
5 results in only a subset of the memory devices
6 in the rank actually writing the data to memory?
7 Is that a generally fair description?

8 ATTORNEY WARRICK: Objection;
9 form.

10 THE WITNESS: Generally speaking,
11 in the context of the JEDEC standardized SDRAMs
12 and the DIMMs that use them, that is an accurate
13 description of how partial word writes are
14 implemented.

15 BY ATTORNEY CHANDLER:

16 Q. Do you agree that a rank of DRAMs
17 share all of the command and address input
18 signals, including the chip-select signal?

19 ATTORNEY WARRICK: Objection;
20 form.

21 THE WITNESS: Again, within the
22 scope of these JEDEC standardized SDRAMs and
23 module types, that is accurate, again, in that
24 context.

25 ///

1 BY ATTORNEY CHANDLER:

2 Q. And that context would include
3 the JEDEC standard for DDR SDRAM and DDR2 SDRAM;
4 correct?

5 A. We would have to look at specific
6 module types -- there are actually a great many
7 different types of DDR2 SDRAM modules. I'm not
8 sure all of them implement partial word reads
9 and writes in that same fashion.

10 This particular picture shows
11 a -- what would be called a UDIMM. And in the
12 context of a UDIMM, that is accurate.

13 Q. Is it also accurate in the
14 context of an RDIMM?

15 A. Okay. So I've lost track of what
16 the original thing we're talking about is. So
17 could you repeat the question with the preamble.

18 Q. Do you agree that a rank of
19 DDR SDRAMs, whether in an UDIMM or an RDIMM,
20 share all of the same command and address input
21 signals, including the chip-select signal?

22 ATTORNEY WARRICK: Objection;
23 form.

24 THE WITNESS: So the question
25 changed from DDR2 to DDR. Is your intent to ask

1 about DDR?

2 BY ATTORNEY CHANDLER:

3 Q. We can start with DDR1 SDRAM, but
4 I'm also interested in DDR2 SDRAM to the extent
5 you think there's a difference in the answer to
6 my question.

7 A. Okay. And just as an aside, with
8 regard to terminology, there's really no such
9 thing as DDR1. It is an error that some people
10 persist in using. But the standards are DDR,
11 DDR2 and so forth.

12 Anyways, so let's --

13 Okay. So looking at
14 Exhibit 1062, which is the DDR SDRAM RDIMM
15 standard, Version 1.3, January 2002, we see
16 that -- for example, on page 11, we have the --
17 the commands going to all of the devices and the
18 single chip-select, which is S0 going into the
19 register and chip-select RS0 becoming
20 chip-select going to the SDRAM.

21 So in this particular module, for
22 example, that your statement is accurate.

23 Q. And for clarity, you were looking
24 at the register on the bottom left of page 11 of
25 Exhibit 1062; is that correct?

1 A. Yes. That is the register that
2 gives the registered DIMM its name.

3 Q. Could you turn back to
4 Exhibit 1103, page 5, and let me know when you
5 have it in front of you.

6 A. I am back at page 5, yes.

7 Q. Do you agree that the DRAMs in a
8 rank will respond to commands together and
9 provide data to the full width of the module?

10 ATTORNEY WARRICK: Objection;
11 form.

12 THE WITNESS: So each of the
13 DRAMs respond to their command and chip-select
14 signals. To the extent that a particular memory
15 module has those signals shared amongst all of
16 the DRAMs in a rank, then that would be true.

17 Your language is a little bit
18 imprecise, because togetherness implies a
19 temporal togetherness; and that's not always the
20 case with regard to, in particular, later
21 iterations of JEDEC standardized DIMMs.

22 BY ATTORNEY CHANDLER:

23 Q. And when you are talking about
24 later iterations of JEDEC standardized DIMMs,
25 are you talking about after 2005?

1 A. Yes. They would be after 2005.

2 Q. So to be clear, again, just for
3 clarity, in general, my questions are intended
4 to be asked with respect to the time frame
5 2004-2005, from the perspective of a person of
6 ordinary skill in the art.

7 Understood?

8 A. Understood, yes.

9 So with regard to the DDR2
10 SDRAM-based DIMMs that are standardized by
11 JEDEC, the DRAMs on the DIMM within a single
12 rank are operating slightly out of phase with
13 each other, but not substantially so that it is
14 an issue for the lower frequencies that are at
15 play in that generation of memories and modules.

16 Q. On page 5 of Exhibit 1103, do you
17 see the last bullet point says, "Need 8 DRAMs in
18 a rank to provide the 64 bits at once"?

19 A. I see that bullet.

20 Q. Do you believe that statement is
21 generally accurate, taking into account that the
22 time frame of "at once" may not be precisely at
23 once down to the zillionth of a second, but
24 would be "at once" given the clock frequencies
25 of the memory modules of the day?

1 ATTORNEY WARRICK: Objection;
2 form, scope.

3 THE WITNESS: Yes. It is a
4 tutorial and, thus, speaks in generalities. And
5 so I do not take exception with what the bullet
6 point is trying to teach.

7 BY ATTORNEY CHANDLER:

8 Q. Now, in your expert declarations
9 marked as Exhibit 2004, you have offered the
10 opinion that the term "rank," with an R,
11 requires more than one memory device; correct?

12 ATTORNEY WARRICK: Objection;
13 form.

14 THE WITNESS: In my paragraph 61
15 of the declaration for the '417, I say that
16 Netlist, in contrast, proposed that a rank is a
17 predetermined group of memory devices on a
18 memory module that can send or receive a fixed
19 number of data bits via a fixed-width data bus
20 in response to read or write commands and
21 independently from other memory devices on the
22 memory module.

23 That is -- there are, in fact,
24 three different proposed constructions at play
25 here, and that is the one that Netlist has

1 proposed.

2 BY ATTORNEY CHANDLER:

3 Q. And do you agree with Netlist's
4 proposed construction --

5 A. It's not --

6 Q. -- for the term "rank," with an
7 R?

8 A. It's a fine construction. I've
9 been asked to apply it in this declaration, and
10 I have done so.

11 Q. In the context of the '417 and
12 '215 patents, in your opinion, does the term
13 "rank," with an R, require more than one memory
14 device to be in the rank?

15 ATTORNEY WARRICK: Objection;
16 form, scope.

17 THE WITNESS: Give me a second.
18 (Witness reviews document.)

19 In the context of at least the
20 '417, the ranks as they are claimed require a
21 plurality of memory devices within an N-bit-wide
22 rank.

23 BY ATTORNEY CHANDLER:

24 Q. What about the context of the
25 '215 patent?

1 ATTORNEY WARRICK: Same
2 objections.

3 THE WITNESS: Too many PDFs open.
4 (Witness reviews document.)

5 In the context of the '215, the
6 plurality of ranks that are claimed in Claim 1
7 require at least one memory device in each rank.

8 With regards to the construction
9 that Netlist is proposing, that would still
10 require a plurality of memory devices that -- in
11 the rank.

12 BY ATTORNEY CHANDLER:

13 Q. In your opinion, in the context
14 of the '215 patent, can a rank, with an R,
15 include just one memory device?

16 ATTORNEY WARRICK: Objection;
17 form, scope.

18 THE WITNESS: Not according to
19 the construction proposed by Netlist.

20 BY ATTORNEY CHANDLER:

21 Q. And that was not my question. My
22 question is whether, in your opinion, in the
23 context of the '215 patent, can a rank, with
24 an R, include just one memory device?

25 ATTORNEY WARRICK: Same

1 objections.

2 THE WITNESS: In my opinion, the
3 term "rank" is used and misused in a variety of
4 different ways and a variety of different
5 contexts, both in the time frame 2004-2005 in
6 particular, since it was still a -- the term was
7 only a decade old at that time. And so there
8 is -- without the benefit of a proposed
9 construction, it's difficult to say what a
10 POSITA would have understood in that time frame
11 as whether or not it's limited to one or two --
12 whether -- I'm sorry -- whether a rank can have
13 a single memory device or it necessarily has to
14 have a plurality of memory devices.

15 Certainly in that time frame and
16 with the memory device -- devices that were
17 common at the day, all ranks, as the term was
18 used, would have involved more than one memory
19 device. That would have been the context that a
20 POSITA would have used in order to understand
21 what the term means.

22 BY ATTORNEY CHANDLER:

23 Q. So is it fair to say that your
24 opinion is that in the context of the '417 and
25 '215 patents, a person of ordinary skill in the

1 art would understand the term "rank," with an R,
2 to require more than one memory device?

3 ATTORNEY WARRICK: Objection;
4 form, scope.

5 THE WITNESS: Yes. It is my
6 opinion that a POSITA in 2004-2005 would
7 understand that ranks include more than one
8 memory device.

9 BY ATTORNEY CHANDLER:

10 Q. And not just include more than
11 one memory device, but must have more than one
12 memory device.

13 So to be clear, the -- the
14 dispute is whether a rank can only have one
15 memory device. I think everyone agrees that a
16 rank can have more than one memory device. The
17 issue is whether a rank can have just one memory
18 device.

19 What's your opinion on that
20 question with respect to the '417 and '215
21 patents?

22 ATTORNEY WARRICK: Objection;
23 form, scope.

24 THE WITNESS: It's -- my opinion
25 is not what's relevant here. It's -- you've

1 instructed me to answer in the context of what a
2 POSITA would understand in 2004-2005.

3 In that context, a POSITA would
4 not have encountered anything called a rank with
5 less -- with only a single memory device. So it
6 would have been a significant leap on the part
7 of a POSITA to think that there might be
8 something called a rank that only had one -- it
9 would be outside of his or her experience.

10 BY ATTORNEY CHANDLER:

11 Q. And you're sure about that?

12 ATTORNEY WARRICK: Objection;
13 form.

14 THE WITNESS: Based on my review
15 of the documents of the day that are at -- in
16 the record of this -- these IPRs, that is my
17 considered opinion.

18 BY ATTORNEY CHANDLER:

19 Q. In forming your opinion in these
20 IPRs as reflected in your expert declaration
21 marked as Exhibit 2024, did you use the
22 understanding of the term "rank" as we just
23 discussed in which a rank requires more than one
24 memory device?

25 ATTORNEY WARRICK: Objection;

1 form.

2 THE WITNESS: In drafting these
3 declarations, I considered the proposed
4 constructions by the parties and by the board
5 and outlined my thoughts about them and then
6 principally used the Netlist proposed
7 construction as indicated by counsel.

8 BY ATTORNEY CHANDLER:

9 Q. And to be clear, Netlist proposed
10 construction requires more than one memory
11 device in a rank; correct?

12 A. To be clear, it says that a rank
13 is a predetermined group of memory devices on a
14 memory module.

15 So in that context, yes.

16 (Exhibit Number 1070 was previously
17 marked for identification.)

18 ATTORNEY CHANDLER: I'm going to
19 put Exhibit 1070 in the chat. It's the same
20 exhibit in both IPRs. It's been marked
21 previously, but I'll just put it in the chat for
22 ease of reference.

23 BY ATTORNEY CHANDLER:

24 Q. Please open it up and let me know
25 when you have it open, and you can go to

1 page 413 of Exhibit 1070.

2 A. So I have the cover page of
3 "Memory Systems, Cache, DRAM, Disk" by Jacob,
4 Ng, and Wang.

5 Q. And have you seen the Jacob
6 textbook marked as Exhibit 1070 before?

7 A. Yes.

8 Q. And were you familiar with the
9 Jacob textbook marked as Exhibit 1070 before you
10 were engaged by Netlist in around the year 2021?

11 A. Yes.

12 Q. In what context were you familiar
13 with the Jacob textbook marked as Exhibit 1070?

14 A. I generally buy all memory
15 subsystem books that come on the market that I
16 become aware of. This one was published in
17 2008, I believe, so in that time frame. And so
18 I probably purchased my copy in that time frame
19 as well -- yes, copyright 2008.

20 Q. Please turn to page 413 of
21 Exhibit 1070, and let me know when you're there.
22 If you're using Adobe Acrobat, you can type
23 control, shift, N, type in 413, press enter, and
24 it should jump right there.

25 A. I'm on page 413.

1 Q. Now, you understand that
2 Professor Jacob, as shown on Exhibit 413 as
3 Exhibit 1070, has defined the term "rank" as
4 including one or more DRAM devices, contrary to
5 Netlist's proposed construction of "rank" that
6 requires more than one memory device; correct?

7 ATTORNEY WARRICK: Objection;
8 form.

9 THE WITNESS: So reading from
10 page 413, the authors say, "Essentially, a rank
11 is -- a rank of memory is a 'bank' of one or
12 more DRAM devices that operating in lockstep in
13 response to a given command."

14 BY ATTORNEY CHANDLER:

15 Q. Do you agree with that sentence
16 in Exhibit 1070, page 413?

17 A. I think that it is not a good
18 sentence. It's internally inconsistent in that
19 if you have two things operating in lockstep,
20 they are necessarily more than one of them.

21 So it's not a good sentence that
22 I would agree with.

23 Q. To be clear, you disagree with
24 Professor Jacob's statement on page 413 as well
25 as page 414 of Exhibit 1070 that a rank can have

1 just one memory device?

2 ATTORNEY WARRICK: Objection;
3 form.

4 THE WITNESS: We're on page 414,
5 are you referring to?

6 BY ATTORNEY CHANDLER:

7 Q. The end of the first full
8 paragraph on the left above the heading 10.2.3.

9 A. So as of 2008 and in the context
10 of embedded systems that do not use memory
11 modules, that statement on page 414 has
12 validity.

13 However, when you ask me in the
14 context of a POSITA in 2004-2005, whether one
15 device can operate in lockstep with itself and
16 only itself, there become problems. And the
17 distinction that the authors make here between
18 the two uses on page 413 and 414 are at tension
19 with each other.

20 And so I remain of the opinion
21 that a POSITA, in 2004-2005 in the context of
22 the JEDEC standardized modules, would understand
23 a rank to have more than one device.

24 Q. Are the '417 and '215 patents
25 limited to JEDEC standardized modules?

1 ATTORNEY WARRICK: Objection;
2 form.

3 THE WITNESS: So the scope of the
4 claims of these patents are not limited to JEDEC
5 standardized modules.

6 BY ATTORNEY CHANDLER:

7 Q. So I want to focus on this
8 question of whether a rank can have just one
9 memory device or whether it requires more than
10 one memory device. So it's a pretty simple sort
11 of mathematical question. Like, is one memory
12 device sufficient to be a rank, or do there need
13 to be two or more memory devices?

14 Do you understand the issue that
15 I'm focused on?

16 A. Yes, I do.

17 Q. At the time of the Jacob book in
18 2008, do you believe a rank could have just one
19 memory device?

20 ATTORNEY WARRICK: Objection;
21 form, scope.

22 THE WITNESS: So in this case
23 particularly, you're not asking me to answer in
24 the context of a POSITA of 2004-2005; is that
25 accurate?

1 BY ATTORNEY CHANDLER:

2 Q. Correct. And just so you
3 understand where I'm going to go with the next
4 question -- I'm trying to understand, is there
5 some change in the meaning of "rank" from
6 2004-2005 to 2008? And I'm also interested in a
7 little bit before 2004-2005, whether there was
8 some change in the meaning of the term "rank."

9 But to start, let's just start
10 with 2008, since we've got the Jacob textbook.
11 And he says pretty clearly that a rank can have
12 just one memory device.

13 Is that consistent with your
14 understanding of the term "rank" in the year
15 2008, that it could have just one memory device?

16 ATTORNEY WARRICK: Objection;
17 form, scope.

18 THE WITNESS: Again, this is not
19 something that I've really dealt with in my
20 declaration, since I've been using the proposed
21 constructions by the parties as directed to by
22 staff -- by counsel, rather.

23 The important point with regard
24 to your underlying question is that Jacob's
25 context, specifically on page 414, is embedded

1 systems, which have sometimes as few as a single
2 memory device; but the context for all of your
3 other questions of a POSITA in 2004-2005,
4 thinking about memory modules with ranks on
5 them, the concept of a single memory device rank
6 would be completely foreign to that POSITA.

7 BY ATTORNEY CHANDLER:

8 Q. And is there something special in
9 the answer you just gave me about the term
10 "rank" in the year 2004 and 2005, or would your
11 answer be the same with respect to the
12 understanding of a person of ordinary skill in
13 the art in the year 2000 or the year 1995, for
14 example?

15 ATTORNEY WARRICK: Objection;
16 form.

17 THE WITNESS: So you're asking
18 me -- a POSITA in an earlier time frame, what
19 would they think?

20 BY ATTORNEY CHANDLER:

21 Q. Yes. I'm trying to understand
22 whether you're suggesting that the term "rank,"
23 with an R, changed its meaning over time as you
24 go from 1995 to 2000 to 2005 to, you know, 2008
25 and so forth; or whether the term "rank," with

1 an R, had the same meaning throughout that time
2 frame.

3 ATTORNEY WARRICK: Objection;
4 form.

5 THE WITNESS: There was no change
6 to the meaning as understood by a POSITA for all
7 of those previous time frames that you're
8 considering in the context of memory modules
9 containing synchronous DRAMs.

10 BY ATTORNEY CHANDLER:

11 Q. Okay. Could you turn to page 6
12 of Exhibit 1103 and let me know when you're
13 there.

14 A. 1106?

15 Q. No. Exhibit 1103, which is the
16 tutorial, and then on page 6. And let me know
17 when you're there.

18 A. I apologize.

19 Tutorial, page 6, I am there.

20 Q. Do you believe a person of
21 ordinary skill in the art would have known about
22 the DQS, data strobe signal, and the DQ, data
23 signal?

24 ATTORNEY WARRICK: Objection;
25 form, scope.

1 (Witness reviews document.)

2 THE WITNESS: Yes, in the context
3 of a POSITA in 2004-2005, they would certainly
4 have been familiar with the concept of a
5 bidirectional data line, DQ; and in the context
6 of a DDR2 memory, they would be familiar with
7 the idea of a data strobe signal, DQS.

8 BY ATTORNEY CHANDLER:

9 Q. And the DQS, strobe signal, was
10 also used with DDR SDRAM memory; correct?

11 A. Let me be double-check. I
12 believe that's true, but let me double-check.
13 DDR.

14 Q. That's shown, for example, on
15 Exhibit 1060, page 7, about two-thirds down.

16 A. I looked at the standard. And
17 for DDR SDRAMs, DQS was not differential, so
18 this figure would not apply. But the concept of
19 a data strobe signal would apply, yes.

20 Q. And so when you use the term
21 "differential," you're referring to the idea
22 shown on page 6 of Exhibit 1103 that you could
23 have a DQS strobe signal and a DQS-bar strobe
24 signal that's essentially the opposite?

25 Is that fair?

1 ATTORNEY WARRICK: Objection;
2 form, scope.

3 THE WITNESS: I would take
4 exception to the word "could." Certainly most
5 of the -- I believe the DDR2 required both to be
6 present, but I'm not 100 percent sure of that.
7 Certainly the DDR did not have the complementary
8 signal line.

9 BY ATTORNEY CHANDLER:

10 Q. Why don't you put it in your own
11 words, the distinction you're trying to draw
12 with respect to the DQS strobe signal for DDR
13 SDRAM versus DDR2 SDRAM.

14 A. So if we look at Exhibit 1104,
15 which is the DDR standard, and we look at the
16 page 1 of that standard, it talks about a DQS
17 signal. But there's no reference in that
18 standard to DQS-bar. So the -- in that
19 generation of SDRAMs, the DQS was single-ended,
20 is the terminology that we use.

21 In contrast, in the DDR2
22 standard, Exhibit 1064, we see, for example, on
23 page 6 of that standard that DQS and DQS-bar are
24 both defined and are -- and so the figure of the
25 tutorial, page 6, applies to DDR2 but not to DDR

1 SDRAMs.

2 Q. And do you believe a person of
3 ordinary skill in the art would have known the
4 information you just gave me in your last
5 answer?

6 A. The information that I gave you
7 in my last answer comes straight from the
8 standards, which we have previously determined
9 would be within the knowledge set of -- or at
10 least the familiarity set of a POSITA in
11 2004-2005.

12 Q. Looking at page 7 of
13 Exhibit 1103, do you agree page 7 of 1103
14 illustrates an unbuffered DIMM, also known as a
15 UDIMM?

16 ATTORNEY WARRICK: Objection;
17 form, scope.

18 THE WITNESS: Yes, but this is
19 not a DDR2 UDIMM or a DDR UDIMM?

20 BY ATTORNEY CHANDLER:

21 Q. And why do you say that?

22 A. Because I know what the clock and
23 command and address topology indicates, that
24 this is the topology that is present in DDR3
25 UDIMMs, not in DDR2 UDIMMs.

1 Q. And how would the topology of a
2 DDR2 UDIMM differ from what's shown on page 7 of
3 Exhibit 1103?

4 ATTORNEY WARRICK: Objection --
5 sorry. Objection; form, scope.

6 (Witness reviews document.)

7 THE WITNESS: So which exhibit
8 is -- okay. So this is the RDIMM.

9 Exhibit 1062 is the JEDEC
10 standard for DDR SDRAM RDIMMs, not DDR2, but the
11 same ideas will apply.

12 For example, if you look at
13 page 64 of that standard, it shows you the
14 prescribed topology of address and control
15 signals for raw cards A and B, but it applies
16 equally for the other variants of this standard.
17 So this does not include a fly-by, as the
18 topology that's shown in the tutorial, page 6 or
19 7, whichever it was we were looking at. And
20 this tree-like topology was the norm for the
21 earlier generations of JEDEC standardized
22 modules.

23 BY ATTORNEY CHANDLER:

24 Q. Turning back to page 7 of
25 Exhibit 1103, do you believe a person of

1 ordinary skill in the art would have known about
2 UDIMM memory modules in general?

3 ATTORNEY WARRICK: Objection;
4 form, scope.

5 THE WITNESS: I believe we have
6 an exhibit that is a UDIMM standard for DDR2.
7 Is that accurate?

8 BY ATTORNEY CHANDLER:

9 Q. I'm not sure that we do.

10 A. In the record?

11 Well, certainly we've identified
12 UDIMM in the specification of the patents at
13 issue here and have acknowledged that UDIMM is
14 one of the acronyms that a POSITA would have
15 known about in 2004-2005 in the context of a DDR
16 SDRAM UDIMM or a DDR2 SDRAM UDIMM.

17 Q. And how would you --

18 A. Perhaps not the latter.

19 I think we -- we'd have to go
20 back and check the record of this deposition to
21 see if we established that for DDR2 UDIMMs. But
22 certainly with regard to DDR SDRAM UDIMMs, it
23 was within the experience of and knowledge of a
24 POSITA in 2004-2005. I apologize for not ending
25 that answer cleanly.

1 Q. How would you explain to a
2 layperson what a UDIMM memory module is?

3 A. As shown in page 7, the figure on
4 page 7, a UDIMM is a DIMM, so it's a dual
5 in-line memory module, that's standardized by
6 JEDEC that includes DRAMs of the appropriate
7 generation and no other substantial integrated
8 circuits, excluding, of course, the SPD device,
9 if that's on there as well, but not shown in
10 this particular figure.

11 Q. And you're referring to page 7 of
12 Exhibit 1103; correct?

13 A. I am.

14 Q. So page 7 of Exhibit 1103 shows a
15 memory controller at the bottom sending DQ and
16 DQS signals to the memory devices on the module
17 as well as address commands and clock signals to
18 the memory devices on the memory module.

19 Is that a fair summary?

20 ATTORNEY WARRICK: Objection;
21 form, scope.

22 THE WITNESS: That does describe
23 what is shown on page 7 of Exhibit 1103.

24 BY ATTORNEY CHANDLER:

25 Q. And is it generally fair to say

1 that with a UDIMM memory module, the memory
2 controller sends data signals, address signals,
3 command signals and clock signals directly to
4 the DRAM memory devices without any intermediary
5 integrated circuits along the way?

6 ATTORNEY WARRICK: Objection;
7 form.

8 THE WITNESS: I'll take exception
9 to the characterization, as indicated in this
10 figure, that the memory controller sends DQ and
11 DQS. It, in fact, sends and receives DQ and
12 DQS. And there are other aspects to the UDIMM
13 interface that are -- that ignored, both in this
14 figure and in your characterization, that are
15 not central to the essential understanding of
16 what a UDIMM is.

17 BY ATTORNEY CHANDLER:

18 Q. So, in your words, what is sort
19 of central to the essential understanding of
20 what a UDIMM is, then?

21 ATTORNEY WARRICK: Objection;
22 form.

23 THE WITNESS: I think I answered
24 that a couple of questions ago; that the UDIMM
25 has on it the DRAMs and perhaps the NSPE device

1 but no additional integrated circuits.

2 BY ATTORNEY CHANDLER:

3 Q. If I understand the clarification
4 that you are trying to make to my question, with
5 a UDIMM, the memory controller can both send and
6 receive DQ and DQS signals directly with the
7 memory devices and can also send address command
8 and clock signals directly to memory devices.

9 Is that fair?

10 ATTORNEY WARRICK: Objection;
11 form.

12 THE WITNESS: I think that's
13 fair, yes. I think you accurately summarized
14 the previous answer.

15 BY ATTORNEY CHANDLER:

16 Q. Do you agree that page 8 of
17 Exhibit 1103 illustrates a registered DIMM, also
18 known as RDIMM?

19 ATTORNEY WARRICK: Objection;
20 form, scope.

21 THE WITNESS: Yes. Page 8 of
22 Exhibit 1103 shows a figure that's labeled
23 "RDIMM."

24 BY ATTORNEY CHANDLER:

25 Q. And how would you explain to a

1 layperson what an RDIMM memory module is?

2 A. In general, a JEDEC standardized
3 RDIMM includes a register for the address and
4 command fields or signals in addition to the
5 DRAMs on the module.

6 Q. And the register you're referring
7 to is the box labeled "Register" shown in the
8 middle of page 8 of Exhibit 1103.

9 Is that fair?

10 A. Yes, that's true. And we also
11 saw an RDIMM in the figure we referenced -- or
12 the exhibit we referenced a few minutes ago,
13 which was an actual JEDEC standardized RDIMM in
14 its full glory.

15 Q. Okay. Is it fair to say that an
16 RDIMM does not register or buffer the DQ and DQS
17 signals; instead, it only registers the address
18 command and clock signals going to the memory
19 devices?

20 ATTORNEY WARRICK: Objection;
21 form.

22 THE WITNESS: Certainly the RDIMM
23 that's shown on page 8 of Exhibit 1103 does not
24 have anything along the DQ or DQS paths between
25 the memory controller and the DRAMs. And we saw

1 comparable organization when we looked at the
2 DDR2 RDIMM exhibit earlier.

3 BY ATTORNEY CHANDLER:

4 Q. Can the same type of memory
5 devices be used on both the UDIMM memory module
6 and an RDIMM memory module?

7 ATTORNEY WARRICK: Objection;
8 form.

9 BY ATTORNEY CHANDLER:

10 Q. For example, DDR SDRAM memory
11 devices or DDR2 SDRAM memory devices?

12 A. So if you look at the standards
13 for a DDR2 UDIMM module and a DDR2 RDIMM module,
14 you'll see that they specify the use of the same
15 types of DDR2 SDRAMs, all standardized by JEDEC.
16 And we can look at those specific standards to
17 confirm that, if you so choose.

18 Q. I just want to be clear at a high
19 level. It's not like JEDEC has one standard for
20 DDR memory devices that are intended for a UDIMM
21 and a different standard for DDR memory devices
22 intended for an RDIMM; instead, JEDEC has one
23 standard for the memory device; and that same
24 memory device may be used on different types of
25 memory modules. Maybe it's a UDIMM. Maybe it's

1 an RDIMM. Maybe it's something else.

2 Is that fair?

3 ATTORNEY WARRICK: Objection;
4 form.

5 THE WITNESS: JEDEC has
6 standardized SDRAMs of different flavors. It's
7 also standardized modules that use those DRAMs
8 that are standardized. So the -- and the names
9 of the module standards indicate which type of
10 DRAMs are applicable for use in those modules.
11 Not all DDR SDRAMs are usable within a
12 particular DDR2 UDIMM, but some are. And
13 certainly there are other nonstandardized memory
14 configurations, proprietary memory
15 configurations that also use JEDEC standardized
16 DRAMs.

17 But, in general, your assertion
18 is accurate, that the generations of modules and
19 the generations of SDRAMs, both as standardized
20 by JEDEC, go hand in hand.

21 BY ATTORNEY CHANDLER:

22 Q. So to take a concrete example,
23 Exhibit 1060 is the JEDEC standard for the DDR
24 SDRAM memory device.

25 A. Yes.

1 Q. And there's only one JEDEC
2 standard for DDR SDRAM memory devices. It's not
3 like you've got one JEDEC standard for DDR SDRAM
4 memory devices intended for a UDIMM and a
5 different JEDEC standard for DDR SDRAM memory
6 devices intended for RDIMMs.

7 Instead, there's just one JEDEC
8 standard for DDR SDRAM memory devices, and those
9 memory devices may find themselves in a variety
10 of different types of memory modules; is that
11 fair?

12 ATTORNEY WARRICK: Objection;
13 form.

14 THE WITNESS: So if you look at
15 page 1 of the DDR SDRAM specification JESD79,
16 you'll see that it doesn't define one DRAM. It
17 defines a whole family of DRAMs. Some of that
18 family will find reference to them in the -- the
19 DDR UDIMM standard.

20 Others may or may not. We'd have
21 to check to see exactly which of these plurality
22 of defined DDR SDRAMs are acceptable or are
23 usable in specific DDR RDIMM modules.

24 So, yes, there's one SDRAM
25 standard that feeds into or is referenced by

1 both the UDIMM and the RDIMM standards, but not
2 every DDR SDRAM may have a home in any one
3 particular type of module.

4 BY ATTORNEY CHANDLER:

5 Q. And the answer you just gave, it
6 also applies to DDR2 memory devices and the
7 JESD79-2 standard that we looked at marked as
8 Exhibit 1064; correct?

9 A. Yes. That's a general
10 characterization of how JEDEC goes about
11 standardizing things.

12 Q. If you look back at the tutorial
13 marked as Exhibit 1103 and sticking on page 8,
14 for example, how would you explain to a
15 layperson what the memory controller is, which
16 is indicated at the bottom of that figure?

17 ATTORNEY WARRICK: Objection;
18 form, scope.

19 THE WITNESS: Well, in this
20 figure of Exhibit 1103, page 8, the memory
21 controller is the circuitry that controls the
22 memory that is on the RDIMM. It's -- the memory
23 is not -- only responds to commands that are
24 provided to it; and it is the memory control
25 that is responsible for controlling the memories

1 according to the standard that they comply with
2 and to send data and to receive data when
3 appropriate.

4 BY ATTORNEY CHANDLER:

5 Q. And at the time frame of the '417
6 and '215 patents, were there certain companies
7 that typically manufactured memory controllers
8 that you were familiar with?

9 ATTORNEY WARRICK: Objection to
10 form.

11 THE WITNESS: In the 2004-2005
12 time frame, memory controllers were either
13 designed and sold independently or part of a
14 chipset or were designed and sold as a design
15 that was then licensed and then used by other
16 companies.

17 So there are a wide variety of
18 companies that participate in the memory
19 controller side of the entire DRAM community.

20 BY ATTORNEY CHANDLER:

21 Q. Did you have familiarity with
22 memory controllers at the time of the '417 and
23 '215 patents?

24 A. Oh, certainly.

25 Q. And what memory controllers were

1 you most familiar with at that time frame?

2 A. That was, what? 20 years ago.
3 So I would be hard-pressed to remember specific
4 part numbers.

5 But certainly, you know, Intel
6 was a dominant force in architecting PCs in that
7 time frame. And so their memory controllers
8 that they put into their northbridge devices or
9 hub devices were ones that I was specifically
10 familiar with.

11 Q. Were you familiar with memory
12 controllers at the time of the '417 and '215
13 patents that were compatible with either a UDIMM
14 memory module or an RDIMM memory module? In
15 other words, the purchaser of the computer could
16 later decide whether to plug in a UDIMM memory
17 module or an RDIMM memory module; and either
18 way, the memory controller would still work? Is
19 that something that you were familiar with?

20 A. Again, that's 20 years ago. I
21 don't have a specific recollection of such a
22 memory controller that was ambidexterous with
23 regard to UDIMMs and RDIMMs.

24 Q. What do you believe a person of
25 ordinary skill in the art would have known about

1 that question?

2 ATTORNEY WARRICK: Objection;
3 form.

4 THE WITNESS: Again, that's
5 outside the scope of the questions I had to
6 consider for these declarations. I'm not
7 familiar with any particular memory controllers
8 that would have that characteristic, so I am not
9 confident that a POSITA would either.

10 So, again, the passage of time
11 makes answering that question difficult.

12 BY ATTORNEY CHANDLER:

13 Q. Let me ask the opposite.

14 Are you familiar with any memory
15 controllers at the time of the '417 and '215
16 patents which would only work with a UDIMM but
17 not work with an RDIMM or, conversely, would
18 only work with an RDIMM and wouldn't work with a
19 UDIMM?

20 A. Yeah. That was the norm.

21 Q. Could you turn to page 9 of
22 Exhibit 1103 and let me know when you're there.

23 A. "Fully-Buffered DIMM," yes.

24 Q. Does page 9 of Exhibit 1103
25 illustrate a fully buffered DIMM, also known as

1 an FB-DIMM?

2 ATTORNEY WARRICK: Objection;
3 form, scope.

4 THE WITNESS: Again, looking at
5 page 9 of Exhibit 1103, it is labeled
6 "Fully-Buffered-DIMM" and shows a box labeled
7 such.

8 BY ATTORNEY CHANDLER:

9 Q. How would you explain to a
10 layperson what an FB-DIMM memory module is?

11 A. So as illustrated in this figure
12 on page 9, the essential aspect of an FB-DIMM
13 that you would try to convey to a layperson is
14 that there is an AMB chip on the FB-DIMM that
15 couples address command and data between the
16 memory controller and the individual DRAMs on
17 that module.

18 Q. And what -- what does AMB stand
19 for?

20 A. I think it stands for advanced
21 memory buffer, but we'd have to look at the
22 standard defining it to be certain.

23 Q. What's the benefit of buffering
24 the data lines on the memory module?

25 ATTORNEY WARRICK: Objection;

1 form.

2 THE WITNESS: You're referring to
3 in general or in the context of FB-DIMMs in
4 particular?

5 BY ATTORNEY CHANDLER:

6 Q. Really, in general. If you want
7 to answer in the context of the FB-DIMM in
8 particular, I'll take it. But let's start with
9 in general.

10 A. So if you --

11 ATTORNEY WARRICK: Same
12 objection.

13 THE WITNESS: Let's go back to
14 page -- page 5 of 1103, which just takes the
15 address and command aspect of the DIMM out of
16 the question -- it doesn't show that at all. It
17 just shows two ranks.

18 But the principal characteristic
19 that this figure does show is that the DQ
20 signals communicate data and the DQS signals for
21 the data strobe, communicates those signals
22 between the memory controller and a plurality of
23 DRAMs in a typical memory system.

24 And so that topology makes it
25 difficult to run the DQ signals at high

1 frequency. So buffering the DQ signals on the
2 memory module is one solution to solving that
3 essential problem with the JEDEC style of
4 memory -- memory module and memory system.

5 BY ATTORNEY CHANDLER:

6 Q. And is the answer you just gave
7 me something that you think the person of
8 ordinary skill in the art would have known at
9 the time?

10 As a reminder, I mean, Perego
11 has a buffer --

12 A. Yeah, right. So the -- in the
13 context of the JEDEC standardized modules, the
14 answer, I think, is no. But with -- in the
15 context of the prior art generally and the
16 references in -- in the record here, I think
17 that that -- the existence of buffers between
18 the memory controller and the DRAMs on the DQ
19 lines would have been something that a POSITA
20 would have been generally familiar with as a
21 possibility in the 2004-2005 time frame.

22 ATTORNEY WARRICK: Counsel,
23 sorry. Sorry to interrupt. I don't know if it
24 would be approaching a good time for a break.
25 We've been going over an hour.

1 ATTORNEY CHANDLER: Soon.

2 BY ATTORNEY CHANDLER:

3 Q. Dr. Przybylski, do you believe a
4 person of ordinary skill in the art would have
5 understood, as you said a moment ago, that
6 putting the buffer on the data lines may permit
7 the DQ data signals to run at a higher
8 frequency?

9 ATTORNEY WARRICK: Objection;
10 form.

11 THE WITNESS: I think that that's
12 not quite accurate, because the -- in the
13 context of any specific module, the operating
14 frequency is specified as part of the definition
15 of that module; but the POSITA would have been
16 aware that some memory standards in the pantheon
17 of memory standards and module standards at play
18 in 2004-2005, that ones with -- that took into
19 account signal integrity and signal topology are
20 able to provide higher bandwidth or performance
21 than ones that do not.

22 BY ATTORNEY CHANDLER:

23 Q. How would you explain to a
24 layperson why a buffer on the data line may
25 permit higher bandwidth or performance as

1 compared to a memory module that does not have a
2 buffer on the data line.

3 ATTORNEY WARRICK: Objection;
4 form.

5 THE WITNESS: That's very
6 difficult to do for a layperson without going
7 into a significant amount of electronics and
8 signal integrity issues. But -- so I will try
9 not to do that.

10 BY ATTORNEY CHANDLER:

11 Q. But do you think a person of
12 ordinary skill in the art would understand that
13 a buffer on the data line may permit higher
14 bandwidth or performance as compared to a memory
15 module that did not have a buffer on the data
16 line?

17 ATTORNEY WARRICK: Objection;
18 form.

19 THE WITNESS: We'd have to look
20 at a particular example to understand what a
21 POSITA would or would not have understood about
22 that. In terms of a general concept, a POSITA
23 would understand that some memory devices, some
24 memory module topologies are able to run much
25 faster than others. And to the extent that

1 buffering plays a role in that, a POSITA may or
2 may not have had the insight to come to that
3 conclusion.

4 BY ATTORNEY CHANDLER:

5 Q. In your declaration as well as
6 the prior art references, there's reference to
7 the concept of a load on a electrical line.

8 Are you familiar with the concept
9 of a load?

10 A. Yes.

11 Q. How would you explain what that
12 is?

13 A. A load is a weight, an electrical
14 weight. It's a signal that, in conveying
15 information from one point to another, has at
16 its destination a receiver that will present to
17 the signal a resistance or capacitance or
18 inductance that influences the communication of
19 that information.

20 Q. And you believe a person of
21 ordinary skill in the art would have known what
22 you just told me in your last answer?

23 ATTORNEY WARRICK: Objection;
24 form.

25 THE WITNESS: In general, yes.

1 Its -- as its applicability to memory modules
2 and buffering of DQ in particular, that's a
3 different question that I did not seek to
4 address in my declarations.

5 BY ATTORNEY CHANDLER:

6 Q. What impact does a higher
7 electrical load have on data signals that are
8 being transmitted to and from a memory
9 controller?

10 ATTORNEY WARRICK: Objection;
11 form.

12 THE WITNESS: Again, that's a
13 question that requires a substantial amount of
14 electronics and math to answer properly. Just
15 say that higher loads are more challenging and
16 have negative impacts.

17 BY ATTORNEY CHANDLER:

18 Q. To be clear, was your answer
19 that -- that, in general, higher loads are more
20 challenging and have negative impacts?

21 A. In general, yes, but it's all
22 extremely context-specific.

23 Q. And what impact does a buffer on
24 the data lines have with respect to loads on the
25 data signals?

1 ATTORNEY WARRICK: Objection;
2 form.

3 THE WITNESS: Again, within the
4 context of 2004-2005 and the knowledge and
5 experience of a POSITA, the general idea that
6 reducing or otherwise managing loads to minimize
7 their impact on data communications is a good
8 thing.

9 BY ATTORNEY CHANDLER:

10 Q. Now, I've been sometimes told
11 that there can be too much of a good thing.

12 And so if you look at the
13 tutorial, Exhibit 1103, and you look at pages 7,
14 8 and 9, a UDIMM doesn't buffer any of the
15 signals; an RDIMM buffers the address command
16 and clock signals, but not the data signals; and
17 an FB-DIMM buffers all -- all of the signals.
18 Right?

19 ATTORNEY WARRICK: Objection;
20 form, scope.

21 THE WITNESS: Again, in the
22 context of these figures at this time, that is
23 an accurate assessment. However, as an example
24 of how context-sensitive this is, the DDR3 UDIMM
25 with its unique topology would generally provide

1 in small- to medium-sized memory systems better
2 performance than the comparable RDIMM.

3 So it is very difficult to
4 generalize across time and across DRAM standards
5 and across module standards.

6 BY ATTORNEY CHANDLER:

7 Q. That's what I wanted to get at,
8 which is, there is some trade-off to whether you
9 include a buffer on the signal line; it's not
10 always going to be better; right?

11 ATTORNEY WARRICK: Objection;
12 form.

13 THE WITNESS: What do you mean by
14 "better"? There's better in terms of
15 performance. There's better in terms of
16 reliability. There's better in terms of cost.
17 So there's -- engineering is the art of the
18 trade-off.

19 BY ATTORNEY CHANDLER:

20 Q. If you include a buffer on the
21 data line of a memory module, would that buffer
22 normally add a latency to the data signal as it
23 passes through the buffer?

24 ATTORNEY WARRICK: Objection;
25 form.

1 THE WITNESS: Inevitably, there's
2 some delay, depending on the type of buffer and
3 its characteristics internally. It can be very
4 small or it can be substantial. It all depends,
5 again, on the unique characteristics of the
6 circumstance we're talking about.

7 BY ATTORNEY CHANDLER:

8 Q. For example, is it possible that
9 if you put a buffer on a data line, that the
10 buffer could add a latency of one clock cycle?

11 ATTORNEY WARRICK: Objection;
12 form.

13 THE WITNESS: To what?

14 BY ATTORNEY CHANDLER:

15 Q. To what would have existed if the
16 buffer had not been put on the data line.

17 A. So specifically --

18 ATTORNEY WARRICK: Objection;
19 form.

20 THE WITNESS: We're specifically
21 talking about data lines at this point?

22 BY ATTORNEY CHANDLER:

23 Q. Yes.

24 A. Okay. So in the context of
25 2004-2005 and the knowledge of a POSITA, I think

1 a POSITA would understand that a -- a buffer
2 generally could add a small amount or a larger
3 amount of latency, and depending on what's
4 inside of it.

5 So -- and that would apply to
6 data as well as anything else that the POSITA is
7 dealing with.

8 Q. And within the range of latencies
9 created by the data buffer, which you
10 characterize as between a small amount and a
11 large amount, the latency could be, for example,
12 one clock cycle. That would be within the range
13 of reasonable possibilities; is that fair?

14 ATTORNEY WARRICK: Objection;
15 form.

16 THE WITNESS: Again, for a POSITA
17 in 2004 to 2005, it would recognize that a
18 buffer or a buffer with a register or whatever
19 is being in the path of the communication of a
20 signal, the amount of that delay depends on the
21 characteristics and nature of the buffer and the
22 entire clocking and paradigm that's at play. So
23 this is not an idea that's unique to memory
24 modules or memory systems, but it's a general
25 concept.

1 BY ATTORNEY CHANDLER:

2 Q. Was it common for a register for
3 a buffer to delay a signal by one clock cycle?

4 ATTORNEY WARRICK: Objection to
5 form.

6 THE WITNESS: There are --

7 ATTORNEY WARRICK: Objection;
8 form.

9 THE WITNESS: There are many
10 examples of a register or buffer that includes a
11 cycle of delay. There are many examples that
12 include many cycles of delay; and there are
13 examples that have fractions of a cycle of
14 delay.

15 Again, it all depends on the
16 context and of the nature of the buffer that's
17 in the signal path.

18 ATTORNEY WARRICK: Counsel, I
19 suggest again that it might be a good time for a
20 break.

21 THE WITNESS: It's been an hour
22 and a half, so let's -- I would appreciate a
23 break.

24 ATTORNEY CHANDLER: Let me --
25 just a few more questions. I want to sort of

1 wrap this up on this question.

2 BY ATTORNEY CHANDLER:

3 Q. Let's take the example of a data
4 buffer that adds a latency of one clock cycle to
5 the data signal on the memory module.

6 Do you have that in your mind?

7 A. Yes.

8 Q. As a layperson, to me it's a
9 little bit counterintuitive as to why you would
10 want to put a data buffer on a memory module if
11 that data buffer is going to delay the signal by
12 one clock cycle. And yet if I understand your
13 earlier testimony, there's situations in which
14 the data buffer can improve performance.

15 So how would you explain to me
16 why adding a data buffer, which delays the data
17 signal by one clock cycle, actually improves the
18 performance of the memory module?

19 ATTORNEY WARRICK: Objection;
20 form.

21 THE WITNESS: Well, let's say you
22 have two cars, a Ferrari and a Volkswagen
23 Beetle.

24 The Ferrari takes ten minutes to
25 warm up before you get to drive it; but once

1 you're driving, you're going faster. So
2 depending on how far you're going, either the
3 Volkswagen Beetle or the Ferrari will get there
4 faster.

5 It's the same sort of trade-offs
6 that exist in the digital world, where the
7 trade-off between operating frequency and
8 latency is very poignant, and different
9 solutions make sense in different domains for
10 different types of memory systems, for different
11 types of modules and different system types.

12 ATTORNEY CHANDLER: Why don't we
13 take a break.

14 THE VIDEOGRAPHER: Off the record
15 at 11:57 a.m. Pacific Time.

16 (Luncheon recess taken from 11:57 a.m.
17 to 12:48 p.m.)
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P R O C E E D I N G S
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THE VIDEOGRAPHER: On the record
at 12:48 p.m. Pacific Time.

EXAMINATION (Cont'd)

BY ATTORNEY CHANDLER:

Q. Dr. Przybylski, are there any
clarifications or corrections you'd like to make
to any of your testimony from before lunch?

A. Not at this time, no.

Q. Could you please turn to
paragraph 66 of your expert declarations marked
as Exhibit 2024, and let me know when you're
there. And while you're doing that, I'll note
that Exhibit 1096 indicates that the substance
of paragraph 66 is the same in both of your
expert declarations.

A. Okay. I'm there.

Q. In paragraph 66 of your expert
declarations marked as Exhibit 2024, you quote
Dr. Wolfe's opinion about the person of ordinary

1 skill in the art, sometimes referred to as a
2 skilled artisan or a POSITA; correct?

3 A. Yes, I do quote Dr. Wolfe.

4 Q. Dr. Wolfe provided the opinion
5 that a skilled artisan would have:

6 "An advanced degree in
7 electrical or computer engineering
8 and at least two years working in
9 the field; or a bachelor's degree in
10 such engineering disciplines and at
11 least three years working in the
12 field. Additional training can
13 substitute for educational or
14 research experience and vice versa."

15 Did I read that accurately?

16 A. I believe so.

17 Q. Do you dispute that part of
18 Dr. Wolfe's opinion about a person of ordinary
19 skill in the art that I just read?

20 A. I don't dispute it. I've
21 accepted it as is.

22 Q. Dr. Wolfe continued by stating:

23 "Such a hypothetical person
24 would have been familiar with
25 various standards of the day,

1 including the JEDEC industry
2 standards."

3 Did I read that accurately?

4 A. Yes.

5 Q. Do you dispute that part of
6 Dr. Wolfe's opinion about a person of ordinary
7 skill in the art that I just read?

8 A. Give me a second.

9 (Witness reviews document.)

10 No. Reading from my paragraph
11 68, I say:

12 "I believe a POSITA here
13 would be knowledgeable about the
14 operation of standardized DRAM and
15 SDRAM memory devices and memory
16 modules, including those
17 commercially available devices and
18 how those devices and modules
19 interacted with memory controllers
20 of a computer system."

21 Q. Dr. Wolfe goes on to state:

22 "Specifically, he or she
23 would have been knowledgeable about
24 the JEDEC DDR and DDR2 SDRAM
25 standards used to standardize the

1 functioning of memory devices and
2 the JEDEC21-C standard used to
3 standardize different possibilities
4 for the physical layout of memory
5 devices on a module as well as
6 difference possibilities for density
7 and organization of the memory
8 devices to achieve a given memory
9 capacity."

10 Did I read that accurately?

11 A. You did.

12 Q. Do you dispute that part of
13 Dr. Wolfe's opinion about the person of ordinary
14 skill in the art that I just read?

15 A. As we discussed at the very
16 outset of today's deposition, the JESD21-C
17 standard is a huge amalgamation of many, many
18 standards, only some of which are related to
19 memory devices and -- and memory modules.

20 And so that statement is overly
21 broad. But given that caveat, there's -- I have
22 no dispute with it.

23 Q. Dr. Wolfe goes on to state that a
24 skilled artisan:

25 "Would also have been

1 familiar with the structure and
2 operation of circuitry used to
3 access and control computer
4 memories, including sophisticated
5 circuits such as ASICs
6 (application-specific integrated
7 circuits) and CPLDs (complex
8 programmable logic devices) and more
9 low-level circuits such as tristate
10 buffers, flip-flops and registers."

11 Did I read that accurately?

12 A. Yes.

13 Q. Do you dispute that part of
14 Dr. Wolfe's opinion about the person of ordinary
15 skill in the art that I just read?

16 A. I don't have any difficulty with
17 it.

18 Q. Could you turn to paragraph 68 of
19 your expert declarations marked as Exhibit 2024.
20 Let me know when you're there. And, again, I
21 believe Exhibit 1096 indicates that paragraph 68
22 is substantively the same in both of your expert
23 declarations.

24 A. I'm looking at 68.

25 Q. In paragraph 68 of your expert

1 declarations marked as Exhibit 2024, you
2 indicate that Dr. Wolfe provided the opinion
3 that a person of ordinary skill in the art would
4 be knowledgeable about the design and operation
5 of standardized DRAM and SDRAM memory devices
6 and memory modules and how they interacted with
7 the memory controller of a computer system.

8 Did I read the portion of your
9 paragraph 68 accurately?

10 A. Yes.

11 Q. That portion of Dr. Wolfe's
12 opinion is the only part of Dr. Wolfe's opinion
13 about the person of ordinary skill in the art
14 that you specifically disagreed with in your
15 expert declarations marked as Exhibit 2024; is
16 that fair?

17 A. Specifically with regard to the
18 DRAM internals and the ability to create a new
19 DRAM device, yes.

20 Q. And that's what I want to follow
21 up on.

22 It's your opinion that a person
23 of ordinary skill in the art would not be
24 knowledgeable about the design of memory devices
25 or memory modules; instead, in your opinion, a

1 person of ordinary skill would be knowledgeable
2 about the operation of standardized DRAM and
3 SDRAM memory devices and memory modules,
4 including those commercially available devices
5 and how these devices and modules interacted
6 with memory controllers of a computer system.

7 Is that a fair summary?

8 ATTORNEY WARRICK: Objection;
9 form.

10 THE WITNESS: Yes. As I've
11 indicated in that section of my report, I view
12 the design of memory devices and the use of
13 memory devices in memory systems as being two
14 separate fields of art and that the POSITA in
15 this case is familiar with the latter and not
16 with the former.

17 BY ATTORNEY CHANDLER:

18 Q. And then in paragraph 70 of your
19 expert declarations marked as Exhibit 2024, you
20 state that:

21 "With this restriction to the
22 scope of knowledge and experience of
23 a POSITA, I apply Samsung's proposed
24 level of knowledge in my analysis."

25 Is that correct?

1 A. That's what paragraph 70 says,
2 yes.

3 Q. And so do I understand correctly
4 that all of your opinions in your declarations
5 marked as Exhibit 2024 are based on Samsung's
6 proposed level of skill in the art with the one
7 restriction we just discussed, which is that, in
8 your opinion, a person of ordinary skill in the
9 art would not be knowledgeable about the design
10 of memory devices and memory modules?

11 A. As far as the knowledge of a
12 POSITA in 2004-2005, they know how to use the
13 DRAMs. They knew a little bit about the
14 organization of and the logical specification of
15 the DRAMs, but they know very little about
16 what's going on under the hood, so to speak.

17 Q. In paragraph 72 of your expert
18 declarations, marked as Exhibit 2024, you state
19 that the "Vast majority of the DRAM devices and
20 modules sold would have been compliant with one
21 of the JEDEC standards."

22 Did I read that accurately?

23 A. Yes.

24 Q. I have seen estimates that around
25 90 percent of the DRAM memory devices sold in

1 this time frame complied with the JEDEC
2 standards for DDR or DDR2 memory devices.

3 Does that sound like a reasonable
4 estimate to you?

5 A. 90 percent for those two
6 standards in particular?

7 Q. Yes. For the --

8 A. Or 90 percent for all JEDEC
9 standard DRAMs?

10 Q. Well, why don't you tell me what
11 you think is reasonable and what you intended by
12 the phrase "the vast majority."

13 A. Well, certainly I did not have
14 access to market data from that time frame
15 anymore. So it was based on my understanding of
16 what the market conditions were in 2004-2005. I
17 don't feel comfortable putting a particular
18 number on it, whether it's 90 percent for those
19 two DRAM types or if it's 95 for those two DRAM
20 types or 98 for all JEDEC-defined SDRAMs. I
21 don't have any data. So I'm comfortable with
22 saying that the vast majority, like more than
23 75 percent; but specifically how much more, I do
24 not know.

25 Q. In paragraph 71 of your expert

1 declarations marked as Exhibit 2024, you refer
2 to "commercially available memory devices."

3 In forming your opinions, did you
4 assume that a person of ordinary skill in the
5 art would be familiar only with commercially
6 available memory devices?

7 A. Not explicitly. However, a
8 POSITA in 2004-2005 would not have had enough
9 time to really come to -- come in contact with
10 any noncommercially available DRAM devices
11 except possibly ones that are written about in
12 papers here and there that they might have come
13 in contact with. But certainly the principal
14 frame of reference for a POSITA's thinking about
15 these things would have been the commercially
16 available devices and modules.

17 Q. In paragraph 69 of your expert
18 declarations marked as Exhibit 2024, you cite to
19 Exhibit 1070, the textbook by Professor Jacob
20 that we looked another a little bit earlier, to
21 support your opinion that a person of ordinary
22 skill in the art would not be knowledgeable
23 about the internal operation or structure of
24 memory devices; correct?

25 A. Yes. We'd have to look at those

1 pages, 316, 317, to be clear. But that is what
2 I do say in that paragraph.

3 Q. You state that in the Jacob
4 textbook marked as Exhibit 1070, there are 285
5 pages about the design and operation of memory
6 systems using DRAMs, of which only two pages and
7 one figure describe the internal operation and
8 structure of a DRAM in the most superficial
9 manner; correct?

10 A. Those are my words, yes.

11 Q. And the 285 pages that you're
12 referring to are pages 315 through 598 of
13 Exhibit 1070, which is Chapters 7 through 15 in
14 Part 2 of the textbook; is that fair?

15 A. I don't have the specific page
16 numbers listed there in that paragraph. I'm
17 happy to take your word for it, if that -- the
18 page numbers that you outlined total 285.

19 Q. So if you open Exhibit 1070 and
20 you go to the table of contents on page
21 Romanette xiii, you see that there's Part II
22 DRAMs starting on page 313 with Chapter 7 and
23 that Part II runs through Chapter 15 that ends
24 on page 598; correct?

25 A. Yes, I see that.

1 Q. Could you turn to page 353 of the
2 Jacob textbook marked as Exhibit 1070. This is
3 the start of Chapter 8. And let me know when
4 you're there.

5 A. Page 353, Chapter 8.

6 Q. And Chapter 8 runs through
7 page 376; correct?

8 A. Yes.

9 Q. Chapter 8 of the Jacob textbook
10 marked as Exhibit 1070, starting on page 353 and
11 ending on page 376, describes the internal
12 operation and structure of DRAM memory devices;
13 correct?

14 A. Generally speaking, that's true.
15 So I was clearly in error when I said the two
16 pages in one figure.

17 Q. A person of ordinary skill in the
18 art would have been familiar with the general
19 information contained in Chapter 8 of the Jacob
20 textbook marked as Exhibit 1070 about the
21 internal operation and structure of DRAM memory
22 devices; correct?

23 A. No, I wouldn't necessarily go
24 that far. This textbook was written and
25 released in 2008. Prior to this textbook, there

1 were separate textbooks about the DRAM internals
2 and textbooks and papers about the internals
3 and -- so that it's a leap to say that a POSITA
4 in 2004-2005 would be familiar with all of the
5 contents of Chapter 8.

6 Q. Well, to be clear, you're the one
7 that cited to Exhibit 1070 in your expert
8 declarations marked as Exhibit 2024; correct?

9 A. I did.

10 Q. And also to be clear, you would
11 agree now that a person of ordinary skill in the
12 art would have been familiar with information
13 about the internal operation and structure of
14 DRAM memory devices; correct?

15 ATTORNEY WARRICK: Objection;
16 form.

17 THE WITNESS: My principal
18 argument is that the design of DRAMs and the
19 design of memory system using DRAMs are two
20 separate bodies of art and that the POSITA that
21 we are considering here with relatively little
22 experience and the experience being principally
23 related to the design of memory systems would
24 not be necessarily familiar with all of the
25 material of Chapter 8.

1 BY ATTORNEY CHANDLER:

2 Q. Turn to page 355 of Exhibit 1070,
3 the textbook that you cited in your expert
4 declarations, and let me know when you're there.

5 A. 355?

6 Q. Yes.

7 A. Section 8.2, "DRAM Storage
8 Cells"?

9 Q. Yes.

10 In your opinion, would a person
11 of ordinary skill in the art have been familiar
12 with the DRAM storage cells internal to the
13 memory devices?

14 A. At a fundamental level, the 1T1C
15 storage cell is the basis for DRAMs, yes, they'd
16 be familiar with it because they would be
17 cognizant that these storage cells need to be
18 refreshed.

19 Q. Turn to page 358 of Exhibit 1070.
20 Let me know when you're there.

21 A. I'm at 358.

22 Q. In your opinion, would a person
23 of ordinary skill in the art have been familiar
24 with the concept of RAM array structures
25 internal to the memory device?

1 A. In my opinion, a person of
2 ordinary skill would have been aware of RAM
3 array structures at the level of detail
4 articulated by Figure 8.7 on page 359, that the
5 memory storage cells are logically arranged into
6 rows and columns and that word lines and bit
7 lines are what are used to access the -- to
8 perform activates and then reads and write
9 commands; but above and beyond that, I'm not
10 confident of that.

11 Q. Turn to page 366 of Exhibit 1070.
12 Let me know when you're there.

13 A. Which page? I'm sorry.

14 Q. 366.

15 A. 366.

16 I'm there.

17 Q. In your opinion, would a person
18 of ordinary skill in the art have been familiar
19 with decoders internal to the memory device?

20 A. A person of ordinary skill would
21 know that there were decoders in there, because
22 the row and column addresses need to get decoded
23 into individual word lines and collections of
24 bit lines; but their specific characteristics
25 and certainly the whole topic of redundancy

1 would have been beyond them.

2 Q. Turn to page 368 of Exhibit 1070.

3 Let me know when you're there.

4 A. Yes.

5 Q. In your opinion, would a person
6 of ordinary skill in the art have been familiar
7 with control logic internal to the memory
8 device?

9 A. Again, within the context of a
10 POSITA of 2004-2005, principally concerned with
11 SDRAMs of different varieties standardized by
12 JEDEC, would have been cognizant of control
13 logic as depicted in Figure 8.18, which is
14 control logic for a synchronous DRAM, because
15 that sort of figure exists in the data sheets
16 for those commercially available DRAMs. So to
17 that level, yes.

18 Q. Please turn to page 372 of
19 Exhibit 1070. Let me know when you're there.

20 A. I'm at page 372.

21 Q. In your opinion, would a person
22 of ordinary skill in the art have been familiar
23 with data I/O structures internal to the memory
24 device?

25 A. Again, if you look at the next

1 page, page 373, there is a drawing of a data I/O
2 structure from a DDR SDRAM. This figure is
3 duplicated by and large in the data sheets for
4 DDR SDRAMs. And so our person of ordinary skill
5 as of 2004-'5 would be familiar with this level
6 of the I/O structures.

7 Q. In your opinion, would a person
8 of ordinary skill in the art have been familiar
9 with DRAM device packaging?

10 A. Again, the JEDEC standards for
11 the DRAMs specify the device -- the packages
12 that each is to be packaged in and delivered in,
13 including the pin-outs. And so the -- the
14 person of ordinary skill might not be familiar
15 with the historical DIP and SOJ packages that
16 are shown in Figure 8.22 but would be
17 comfortable with the TSOP and BGA -- not BGA --
18 the TSOP packages that were common in 2004 and
19 2005.

20 Q. Please turn to page 457 of
21 Exhibit 1070 and let me know when you're there.

22 A. 457, so going backwards?

23 Q. No. Forwards, 457.

24 A. 457. I'm sorry. My apologies.

25 457.

1 Q. It's the start of Chapter 12.
2 Just let me know when you're there.

3 A. Yes.

4 Q. Chapter 12 of the Jacob textbook
5 marked as Exhibit 1070, starting on page 457,
6 describes the evolutionary developments of DRAM
7 device architecture; correct?

8 A. Yes. That's a terminology I
9 introduced.

10 Q. And a person of ordinary skill in
11 the art would have been familiar with the
12 evolutionary developments of DRAM device
13 architecture up to the 2004 and 2005 time frame;
14 correct?

15 A. Given that we are assuming that
16 our POSITA entered the workforce around
17 2001-ish/2002-ish and entered school in the late
18 1990s, their familiarity with the ancient
19 history of the field is not something we can
20 rely on.

21 Q. In forming your opinions in your
22 expert declaration marked as Exhibit 2024, did
23 you consider whether the hypothetical person of
24 ordinary skill in the art is knowledgeable about
25 all of the prior art in the field of the '417

1 and '215 patents? Or did you limit the
2 hypothetical person of ordinary skill in the art
3 to only what existed between the late 1990s and
4 2004 to 2005?

5 ATTORNEY WARRICK: Objection;
6 form.

7 THE WITNESS: My process was to
8 rebut the arguments in the petitions and the
9 corresponding declarations. To the extent that
10 there was need to consider that particular
11 aspect of a POSITA's knowledge, I would have
12 done so; but I don't recall any circumstances
13 where that came into play.

14 BY ATTORNEY CHANDLER:

15 Q. Turn to page 458 of Exhibit 1070,
16 and there's a Figure 12.1 at the top. Let me
17 know when you have that in front of you.

18 A. I have 458 up.

19 Q. So page 458 of Exhibit 1070 at
20 the top and Figure 12.1 refers to different
21 types of memory devices, including SDRAMs, DDR
22 SDRAMs, and different Rambus DRAMs; correct?

23 A. Are you reading from the text or
24 from the figure?

25 Q. I'm looking at the figure.

1 A. I don't see any reference to
2 Rambus DRAMs in the figure.

3 Q. In the upper right.

4 A. Oh, D-RD and XDR. You're right,
5 yes.

6 Q. And a person of ordinary skill in
7 the art --

8 A. So what's the question now again,
9 please?

10 Q. Simply that Figure 12.1 on the
11 top of page 458 of Exhibit 1070 refers to
12 different types of memory devices, including
13 SDRAMs, DDR SDRAMs and different Rambus DRAMs;
14 correct?

15 A. Yes. Once you recognize that
16 D-RD and XDR refer to Rambus DRAMs, yes.

17 Q. And, in your opinion, a person of
18 ordinary skill in the art would have been
19 familiar with SDRAMs, DDR SDRAMs and Rambus
20 DRAMs; correct?

21 A. Yes, and probably the GDDR
22 graphics DRAMs as well, but those have not come
23 into play in this matter.

24 Q. Turn to page 465 of Exhibit 1070.
25 Let me know when you're there.

1 A. Yes.

2 Q. As we've discussed, a person of
3 ordinary skill in the art would have been
4 familiar with SDRAMs, with a capital S; correct?

5 A. Yes.

6 Q. As shown, for example, on
7 page 467 of Exhibit 1070 in Figure 12.10 at the
8 top, a person of ordinary skill in the art would
9 have known about SDRAM device architecture with
10 four banks; correct?

11 A. Yes.

12 ATTORNEY WARRICK: Objection to
13 form.

14 THE WITNESS: This represents the
15 logical presentation of the memory device to the
16 outside world.

17 BY ATTORNEY CHANDLER:

18 Q. Please turn to page 471 of
19 Exhibit 1070. Let me know when you're there.

20 A. 471, yes.

21 Q. And there's a leaf blower
22 outside. Is it bothering you? Do you hear it?

23 A. You're cutting out once in a
24 while as a result, but not much.

25 Q. A person of ordinary skill in the

1 art would have been familiar with DDR SDRAMs;
2 correct?

3 A. We did verify this morning that
4 the DDR SDRAM standard, the first one became
5 public in 2005, I think. What did we see?

6 Q. It was 2000 for DDR and then 2003
7 for DDR2; correct?

8 A. Right. And then 79-B2 -- 2B --
9 sorry -- was January 20th, 2005, so, yes.

10 Q. And then if you turn to page 474
11 of Exhibit 1070, you agree a person of ordinary
12 skill in the art would have been familiar with
13 DDR2 SDRAMs; correct?

14 A. To the extent that they were
15 referenced in other documents, yes. I think we
16 were not clear whether the -- right. So the --
17 I'm sorry. So the DDR2 SDRAMs were early
18 enough. So, yes.

19 Q. And then if you turn to page 475
20 of Exhibit 1070, do you agree a person of
21 ordinary skill in the art would have been
22 familiar with some of the protocol and
23 architectural differences between DDR SDRAMs and
24 DDR2 SDRAMs?

25 ATTORNEY WARRICK: Objection;

1 form.

2 THE WITNESS: Yes. Those are the
3 difference that would have -- are essential to
4 building memory systems and memory modules out
5 of these devices. So the protocol and
6 architectural differences are principally what
7 the POSITA of 2004-2005 is concerned with.

8 BY ATTORNEY CHANDLER:

9 Q. It you turn to page 477 of
10 Exhibit 1070, do you agree that a person of
11 ordinary skill in the art would have been
12 generally familiar with the scaling trends of
13 DDR and DDR2 SDRAM memory devices?

14 ATTORNEY WARRICK: Objection;
15 form.

16 (Witness reviews document.)

17 THE WITNESS: Some of the content
18 of Section 12.3.6 relating to the evolution of
19 the JEDEC standard DRAMs would have been known
20 to a POSITA of 2004-2005.

21 BY ATTORNEY CHANDLER:

22 Q. And if you look at page 480 of
23 Exhibit 1070, do you agree a person of ordinary
24 skill in the art would have been familiar with
25 Rambus DRAMs?

1 A. Yes.

2 Q. And, for example, as shown on
3 page 482 of Exhibit 1070 and Figure 12.24, a
4 person of ordinary skill in the art would have
5 been generally familiar with the internal bank
6 architecture of a Rambus direct RDRAM device; is
7 that fair?

8 ATTORNEY WARRICK: Objection;
9 form.

10 THE WITNESS: Certainly would be
11 generally aware that there was a plurality of
12 ranks -- of banks -- sorry, my apologies. And
13 that is a distinction between the JEDEC
14 standardized devices and the Rambus devices.

15 And, again, this is a logical
16 representation of the internal architecture of
17 those devices. And so the -- it is the general
18 purview of what a POSITA would be familiar with
19 to some extent.

20 BY ATTORNEY CHANDLER:

21 Q. Please look back at your expert
22 declaration marked as Exhibit 2024, specifically
23 paragraphs 5 through 11. Let me know when
24 you're there.

25 And while you're doing that, I'll

1 note that Exhibit 1096 shows that the substance
2 of paragraphs 5 through 11 is the same in both
3 of your expert declarations.

4 A. I am there.

5 Q. Starting with paragraph 5 of your
6 expert declarations marked as Exhibit 2024, you
7 describe your qualifications and experience
8 relevant to these IPRs; correct?

9 A. Referring to Appendix A, yes.

10 Q. And you consider yourself
11 qualified to provide expert opinions in these
12 IPRs; correct?

13 A. Yes.

14 Q. Do you consider Samsung's expert,
15 Dr. Wolfe, to be qualified to provide expert
16 opinions in these IPRs concerning the '417 and
17 '215 patents?

18 A. That's not a question that I've
19 been asked to opine on.

20 Q. But I'm asking you.

21 A. I haven't reviewed his CV
22 recently, so I don't know.

23 Q. Do you know Dr. Wolfe?

24 A. I have had occasion to bump into
25 him from time to time over the years, yes.

1 Q. Would you consider him, based on
2 your interaction with him, to be an expert with
3 respect to the fields of the '417 and '215
4 patents?

5 ATTORNEY WARRICK: Objection;
6 form.

7 THE WITNESS: Again, I haven't
8 reviewed his detailed work experience and
9 qualifications that relate to memory subsystems
10 in particular, so I don't know.

11 BY ATTORNEY CHANDLER:

12 Q. Have you heard of Dr. Michael
13 Brogioli?

14 A. I do not know the man, no.

15 Q. Do you consider Professor Bruce
16 Jacob to be an expert in the field of the '417
17 and '215 patents, the author of the textbook
18 marked as Exhibit 1070?

19 ATTORNEY WARRICK: Objection;
20 form.

21 THE WITNESS: Yes. He's
22 certainly quite knowledgeable in this field.

23 BY ATTORNEY CHANDLER:

24 Q. In paragraph 9 of your expert
25 declarations marked as Exhibit 2024, you state

1 that you worked on cache hierarchies; correct?

2 A. Yes.

3 Q. Did the cache hierarchies that
4 you worked on use memory modules?

5 A. My doctoral dissertation involved
6 cache memory design and main memory design.
7 Modules were a level of conceptual detail below
8 it, which I was working on.

9 Q. Can you explain that a little bit
10 more, what you mean by "level of conceptual
11 detail below."

12 A. The simulations that I was doing
13 with regard to main memory performance did not
14 capture whether a particular style of main
15 memory was in one form of module or another.

16 In that time frame, all of the
17 DRAMs that were commercially available were all
18 asynchronous and the modules were basically all
19 unbuffered DIMMs. So there was no issue with
20 regard to whether the memory systems I was
21 simulating used one variety of module or
22 another.

23 Q. But focusing on the cache
24 hierarchies, what kind of memories -- what kind
25 of memory modules, if any, were involved in the

1 cache hierarchies that you were working on?

2 A. So the cache hierarchies in that
3 era were all SRAM-based.

4 Q. And were those cache hierarchies
5 that were SRAM-based organized on to a memory
6 module?

7 A. They could have been. It was
8 not -- again, it was not part of the -- it was
9 not one of the dimensions that I was
10 investigating.

11 Q. And what is an SRAM memory
12 device?

13 A. Stands for static random-access
14 memory.

15 Q. Were SRAM memory devices known
16 and commercially available before the 2004-2005
17 time frame?

18 A. Yes.

19 Q. And is an SRAM memory device
20 different from a DRAM memory device?

21 A. Yes.

22 Q. In paragraph 9 of your expert
23 declaration marked as Exhibit 2024, you also
24 state that you worked on MIPS computer systems,
25 M-I-P-S; correct?

1 A. Correct.

2 Q. Did the MIPS computer systems
3 that you worked on use memory modules?

4 A. Yes, they did.

5 Q. Did the MIPS computer systems
6 that you worked on use DRAM memory devices?

7 A. Yes.

8 Q. And what kind of DRAM memory
9 devices?

10 A. In that era, again, we were
11 pre-SDRAM. And so we were all dealing with fast
12 page mode devices.

13 (Interruption by the court reporter to
14 clarify the record.)

15 BY ATTORNEY CHANDLER:

16 Q. In paragraph 11 of your expert
17 declarations marked as Exhibit 2024, you
18 mentioned that you wrote and revised a book
19 entitled "New DRAM Technologies: A
20 Comprehensive Analysis Architectures"; correct?

21 A. Yes; two editions of it.

22 Q. And to what extent is that book
23 that you wrote relevant to your qualifications
24 for being an expert in these IPRs?

25 A. That book analyzed not just

1 SDRAMs but all of the variety of DRAM
2 architectures, both internally and externally,
3 all those architectures that were available in
4 the early 1990s through the -- the second
5 edition came out in the later half of the 1990s.
6 And so it's presented for the reader how these
7 devices differed internally and how their
8 interfaces were different at a very granular
9 level, and then explored how their performances
10 in systems varied as a result of their different
11 characteristics.

12 Q. And that's relevant to these
13 IPRs?

14 A. Yes.

15 (Whereupon, Exhibit Number 1097 in both
16 IPRs was marked for identification and
17 is attached hereto.)

18 ATTORNEY CHANDLER: I'd like to
19 mark a new exhibit, which will be 1097. It's
20 the same document in both IPRs, the only
21 difference being the stamp in the bottom right,
22 the case number.

23 I put it in the chat for
24 everyone's convenience.

25 BY ATTORNEY CHANDLER:

1 Q. Please let me know when you have
2 Exhibit 1097 open.

3 A. I got the whole thing, yes.

4 Q. Do you recognize the cover of
5 Exhibit 1097 as the cover of the second edition
6 of your book entitled "New DRAM Technologies: A
7 Comprehensive Analysis of the New
8 Architectures"?

9 A. Yes.

10 Q. And did you write this book
11 marked as Exhibit 1097 yourself?

12 A. Yes.

13 Q. Please turn to page 41 of
14 Exhibit 1097, which is Chapter 3 of your book,
15 and let me know when you're there.

16 A. I'm at Chapter 3.

17 Q. Do you believe a person of
18 ordinary skill in the art would have known about
19 DRAM basics as explained starting on page 41 of
20 your book marked as Exhibit 1097?

21 ATTORNEY WARRICK: Objection;
22 form.

23 THE WITNESS: The POSITA that
24 we've been discussing vis-à-vis 2004 and 2005
25 would have been familiar with some of the topics

1 in my Chapter 3, just as we reviewed Jacob's
2 book from 2008, and that some of the topics
3 related to the DRAM internals would have been
4 within the purview of such a POSITA.

5 But I think there are some
6 aspects that are in my Chapter 3 that would not
7 necessarily have been at the fingertips of our
8 POSITA.

9 BY ATTORNEY CHANDLER:

10 Q. Please turn to page 69 of
11 Exhibit 1097, which is the start of Chapter 4,
12 and let me know when you're there.

13 A. I'm there.

14 Q. Do you believe a person of
15 ordinary skill in the art would have known about
16 single in-line memory modules, or SIMMs?

17 ATTORNEY WARRICK: Objection;
18 form.

19 THE WITNESS: Again, by the time
20 we were in the 2000s, which is when our POSITA
21 is learning about these things, SIMMs are no
22 longer being used and we are purely in the
23 domain of DIMMs and other more-advanced memory
24 module structures. So they may or may not be
25 familiar with the prior generations of modules.

1 BY ATTORNEY CHANDLER:

2 Q. Well, to be clear, a person of
3 ordinary skill had to go to college and get the
4 equivalent of an advanced degree, and as part of
5 that training, they would have been taught about
6 SIMMs; correct?

7 A. Maybe. Maybe not.

8 Again, the transition from SIMMs
9 to DIMMs happened in -- if I recall correctly,
10 it was in the middle 1990s. So after this
11 edition came out -- at least I think so. We'd
12 have to go back and check the dates on various
13 standards.

14 But, you know, the -- our POSITA
15 may be familiar with SIMMs, maybe not. I don't
16 know. It -- it certainly didn't come up with
17 regard to my opinions in this matter.

18 Q. The '417 and '215 patents
19 specifically refer to SIMMs as within the scope
20 of the memory modules that the '417 and '215
21 patents relate to; right?

22 ATTORNEY WARRICK: Objection;
23 form.

24 BY ATTORNEY CHANDLER:

25 Q. As shown, for example, in

1 Column 6 of the '417 patent at line 45, and also
2 shown, for example, in Column 5 of the
3 '215 patent at line 65; correct?

4 A. Yeah, that's true.

5 Q. Turning back to your book marked
6 as Exhibit 1097, you discuss SIMMs starting on
7 page 70; correct?

8 A. Correct.

9 Q. And then, for example, on page 71
10 of your book marked as Exhibit 1097, you show a
11 figure at the top of the page of a standard
12 30-pin SIMM; correct?

13 A. That's what the caption of
14 Figure 4-1 indicates.

15 Q. You think a person of ordinary
16 skill in the art would have known about standard
17 30-pin SIMMs?

18 A. Possibly. It's -- again, since
19 we're dealing with someone who came out of
20 school in the early 2000s, perhaps or perhaps
21 not. I mean, it's -- there were certainly
22 enough textbooks in that time frame that talked
23 about SIMMs, so it's quite plausible that they
24 would have.

25 Q. You state on page 71 of your book

1 marked as Exhibit 1097 that the most common SIMM
2 memory modules were x8 and x9 organizations;
3 correct?

4 A. And also x32 and x36 on larger
5 ones.

6 Q. And even though we're pronouncing
7 it "by 8," it's written lowercase x and then the
8 number 8; correct?

9 A. Well, technically, it's a
10 multiplication symbol. But if we don't have
11 access to that, we use a lowercase x, yes.

12 Q. And what does x8 and x9 mean?

13 A. So with regard to my Figure 3-8
14 showing a 512Kx8 DRAM on page 56 of the new DRAM
15 technologies, Version 2, it shows 8 DQ signals
16 exhibiting the DRAM. So the x8 means 8 DQ
17 signals.

18 Q. Please turn to page 129 of
19 Exhibit 1097. Let me know when you're there.

20 A. 129, you said?

21 Q. Yes.

22 A. Chapter 5?

23 Q. Yes.

24 A. I'm there.

25 Q. Starting on page 129 of your book

1 marked as Exhibit 1097, you describe new DRAM
2 architectures; correct?

3 A. Yes.

4 Q. And do you believe a person of
5 ordinary skill in the art would have known about
6 the new DRAM architectures described in your
7 book marked as Exhibit 1097 starting on page
8 129?

9 ATTORNEY WARRICK: Objection;
10 form.

11 (Witness reviews document.)

12 THE WITNESS: So Chapter 5 begins
13 with a discussion of improvements to the
14 existing interface and talks about new packaging
15 varieties and new organizations and then gets
16 into some of the new architectures that were
17 becoming -- or being proposed as architectures
18 that -- to replace the fast page mode and burst
19 EDO architectures that were common in the early
20 half of that decade. Some of these caught on;
21 some of them fell by the wayside.

22 I think a POSITA in the mid 2000s
23 would certainly have heard of some of these, but
24 not all of them.

25 For example, on page 152, we -- I

1 categorize synchronous DRAMs in the collection
2 of DRAMs that are new, as they were in 1994 and
3 1996. So, obviously, the POSITA in 2004-2005
4 would have been familiar with these; but some of
5 the other ones never got any commercial traction
6 and fell by the wayside. Similarly for the
7 revolutionary approaches in Section 5.6.

8 BY ATTORNEY CHANDLER:

9 Q. Please turn to page 157 of your
10 book marked Exhibit 1097. Let me know when
11 you're there.

12 A. I am there.

13 Q. Starting on page 157 of your book
14 marked as Exhibit 1097, you describe
15 conventional alternatives to DRAM memory
16 devices; correct?

17 A. "Conventional" being the DRAM
18 architectures that were in place or just minor
19 modifications to the DRAMs that were in place in
20 around 1993-1994.

21 Q. A person of ordinary skill in the
22 art would have known about conventional
23 alternatives, such as EDO DRAMs, as described in
24 your book marked as Exhibit 1097; correct?

25 ATTORNEY WARRICK: Objection;

1 form.

2 THE WITNESS: They may have heard
3 the term, but they would never have had an
4 opportunity to design with them.

5 BY ATTORNEY CHANDLER:

6 Q. Please turn to page 171 of your
7 book marked Exhibit 1097. Let me know when
8 you're there.

9 A. Chapter 7, Evolutionary
10 Approaches -- Alternatives, rather?

11 Q. Yes. Starting on page 171 of
12 your book marked as Exhibit 1097, you describe
13 evolutionary alternatives to DRAM, such as
14 synchronous DRAMs; correct?

15 A. Yes. The synchronous DRAMs that
16 were coming into the fore in the mid 1990s I
17 categorized as evolutionary.

18 Q. And as we've discussed, a person
19 of ordinary skill in the art would have known
20 about these evolutionary alternatives to DRAM at
21 the time, such as synchronous DRAM; correct?

22 A. But the synchronous DRAMs that I
23 address in my book predate the DDR and DDR2
24 DRAMs -- SDRAMs that are at issue in this
25 matter.

1 The previous version, which came
2 to be known as SDR SDRAMs are -- had a
3 relatively short lifespan because of some issues
4 with them; and so a POSITA probably would have
5 heard of SDR SDRAMs, but maybe not.

6 Q. But, again, the '417 and '215
7 patents specifically refer to RAM, DRAM, SDRAM,
8 SDR, DDR, and DDR2, correct, as shown, for
9 example, in Column 6 of the '417 patent around
10 lines 51 through 55 and also Column 6 of the
11 '215 patent around lines 4 through 8; correct?

12 A. Yes. It does mention SDR as one
13 of the varieties of SDRAMs there, yes.

14 Q. And also DRAM and RAM, even older
15 technologies; correct?

16 A. Well, "RAM" is a general term
17 referring to all random-access memory, so
18 including SRAMs and DRAMs and so that's a
19 generic placeholder.

20 Then it refers to DRAMs, which,
21 again, is generic, not specifically referring to
22 the previous generations. And then SDRAMs in
23 its varieties being an example of DRAMs, DRAMs
24 being an example of RAMs. That's how I
25 interpret that sentence.

1 Q. Do you interpret the '417 and
2 '215 patents as limiting themselves to memory
3 devices that are SDRAM and newer, or do you
4 interpret the disclosure of the '417 and '215
5 patent as trying to be broader and encompassing
6 older generations of memory devices as well?

7 ATTORNEY WARRICK: Objection;
8 form.

9 THE WITNESS: So the disclosure
10 of the '417 only mentions by name in this
11 sentence the SDR -- I'm sorry -- the SDRAMs in
12 its various flavors, including SDR SDRAMs.

13 It doesn't mention by name that I
14 can find here any of the names of the previous
15 generations of memory architecture with the
16 exception of the reference to SIMMs in the
17 previous paragraph.

18 So with regard to the disclosure
19 of the specification, there is a failure to
20 disclose anything other than those more recent
21 architectures in this portion of the
22 specification. So there's no mention of fast
23 page mode or EDO or any of the other
24 architectures that, for example, I enumerate in
25 the new DRAM technologies book.

1 BY ATTORNEY CHANDLER:

2 Q. Starting on page 204 of your book
3 marked as Exhibit 1097, you have a section
4 numbered 7.4 devoted to synchronous SDRAMs, also
5 known as SDRAMs with a capital S; correct?

6 A. Sorry. What was the page number
7 again?

8 Q. 204.

9 A. 204.

10 Yes, I see that section.

11 Q. And you indicate that JEDEC,
12 specifically the JC42.3 committee, developed
13 standards for SDRAMs; correct?

14 A. I'm sorry. Repeat the question.

15 Q. You indicate on page 204 of your
16 book marked as Exhibit 1097 that JEDEC,
17 specifically the JC42.3 committee of JEDEC,
18 develops standards for SDRAMs; is that correct?

19 A. Yes. So in that first paragraph
20 of Section 7.4, I do note that the JC42.3
21 standards committee is working on a proposed
22 standard for SDRAMs.

23 Q. And did you personally ever
24 participate in the JEDEC JC42.3 committee?

25 A. As I mentioned earlier, the

1 members of JEDEC are companies, not individuals.
2 Some of my clients in that period were members
3 of that committee and other committees, and I
4 would occasionally participate as a guest of one
5 of those clients. But I was not a voting member
6 or anything like that.

7 Q. So even though you were not a
8 member of JEDEC, you attended some meetings of
9 the JEDEC JC42.3 committee during the
10 standardization process for SDRAMs; is that
11 fair?

12 A. I don't recall which versions of
13 the SDRAM standards I was -- I attended. I only
14 attended a couple of meetings of JEDEC, because,
15 as I said, I myself was not a member and could
16 only attend as a guest of another member.

17 So I think that answered your
18 question.

19 Q. Please turn to page 242 of your
20 book. Let me know when you're there.

21 A. I am at 242.

22 Q. On page 242 of your book marked
23 as Exhibit 1097, you list out some of the
24 strengths and weaknesses of SDRAMs; correct?

25 ATTORNEY WARRICK: Objection;

1 form.

2 THE WITNESS: Yes. This
3 specifically is for the SDR variety of SDRAMs.

4 BY ATTORNEY CHANDLER:

5 Q. And do you believe a person of
6 ordinary skill in the art would have known about
7 the strengths and weaknesses of SDRAMs, as
8 listed on page 242 of your book marked as
9 Exhibit 1097?

10 ATTORNEY WARRICK: Objection;
11 form.

12 THE WITNESS: Certainly by the
13 time we reach 2004 and 2005 and the subsequent
14 versions of SDRAMs standardized by JEDEC, most
15 of -- or some of these weaknesses have
16 dissipated, are no longer in play. So they
17 would not necessarily be front of mind for a
18 POSITA in 2004-2005.

19 And certainly -- you know, of the
20 five weaknesses there, the middle three would
21 certainly be something a POSITA would be aware
22 of; the first and the last, probably not.

23 BY ATTORNEY CHANDLER:

24 Q. With respect to the strengths of
25 SDRAMs listed on page 242 of your book marked as

1 Exhibit 1097, did those strengths remain true in
2 the 2004-2005 time frame?

3 ATTORNEY WARRICK: Objection;
4 form.

5 THE WITNESS: It mentions there a
6 dual-bank architecture. By the time we're in
7 the mid-2000s, we migrated beyond dual-bank to
8 quad-bank and higher-bank counts for some of the
9 other memory types. So that would be no longer
10 precisely accurate.

11 And so with regard to the first
12 strength, it says, "Likely to become a commodity
13 part."

14 By 2004 and '5, it is -- the
15 JEDEC standardized DRIMMS sic are the commodity
16 parts, so that's modified over time. And the
17 commodity marketplace does provide for
18 interchangeable parts across vendors. And the
19 other strengths, including, obviously, the DIMM
20 standard, became a significant strength over
21 time as well.

22 BY ATTORNEY CHANDLER:

23 Q. So would it be fair to say both
24 at the time of your book marked as Exhibit 1097,
25 which is around 1996, as well as the time of the

1 '417 and '215 patents in the 2004-2005 time
2 frame, that a person of ordinary skill in the
3 art knew that strengths of DDR SDRAMs and DDR2
4 SDRAMs included that they were standardized by
5 JEDEC; they were commodity parts; they were
6 interchangeable parts; and that high bandwidth
7 was possible?

8 ATTORNEY WARRICK: Objection;
9 form.

10 THE WITNESS: Yes. However, what
11 constitutes high bandwidth in 2000 -- I'm
12 sorry -- 1996 is different than what passes for
13 high bandwidth in 2004 and '5. But, generally
14 speaking, that's true.

15 BY ATTORNEY CHANDLER:

16 Q. Please turn to page 259 of your
17 book. Let me know when you're there.

18 A. I'm there.

19 ATTORNEY CHANDLER: And I should
20 ask -- we've been going a little bit more than
21 an hour -- if you want to take a break now or if
22 you want to keep going through your book.

23 THE WITNESS: Yes, let's take a
24 break.

25 ATTORNEY CHANDLER: Okay.

1 THE VIDEOGRAPHER: Off the record
2 at 2:00 p.m. Pacific Time.

3 (Recess taken from 2:00 p.m. to
4 2:11 p.m.)

5 THE VIDEOGRAPHER: On the record
6 at 2:11 p.m. Pacific Time.

7 BY ATTORNEY CHANDLER:

8 Q. Dr. Przybylski, starting at on
9 259 of your book marked as Exhibit 1097, you
10 describe what you characterize as revolutionary
11 alternatives to DRAM, such as Rambus DRAMs;
12 correct?

13 A. Yes.

14 Q. And a person of ordinary skill in
15 the art would have known about these so-called
16 revolutionary alternatives to DRAM, such as
17 Rambus DRAMs; correct?

18 ATTORNEY WARRICK: Objection;
19 form.

20 THE WITNESS: The Rambus DRAMs
21 that I talked at length about in this chapter
22 predate the versions of Rambus memory devices
23 that are at issue in this matter, which were the
24 direct and the XDR generations.

25 This device here is -- did not

1 survive very long, and so the specifics of this
2 particular Rambus device probably would not be
3 something that a POSITA of 2004-2005 would have
4 had contact with.

5 BY ATTORNEY CHANDLER:

6 Q. But it was described in your
7 book, and a person of ordinary skill in the art
8 had access to your book; correct?

9 A. The distribution of the book was
10 pretty limited to various companies and a few
11 libraries. But as far as whether a POSITA in
12 2004-2005 would have had access to this
13 limited-edition book from a decade earlier, not
14 at all clear to me.

15 Q. Well, it's also described in
16 Professor Jacob's book and his paper from 2002;
17 correct?

18 ATTORNEY WARRICK: Objection;
19 form.

20 THE WITNESS: What was described?

21 BY ATTORNEY CHANDLER:

22 Q. Rambus DRAMs, including the
23 version that you're talking about, starting on
24 page 259 of Exhibit 1097; right?

25 A. Yes. There's some overlap

1 between this particular device, and it is
2 mentioned in passing in Jacob's article.

3 Q. Turn to page 305 of your book
4 marked as Exhibit 1097. Let me know when you're
5 there.

6 A. Page 305?

7 Q. Yes.

8 A. I'm there.

9 Q. On page 305 of your book marked
10 as Exhibit 1097, you list strengths and
11 weaknesses of Rambus DRAMs; correct?

12 A. I do.

13 Q. For example, some of the listed
14 weaknesses of Rambus DRAMs include "high
15 latency," "limited parallelism," and "not an
16 evolutionary technology"; correct?

17 ATTORNEY WARRICK: Objection;
18 form.

19 THE WITNESS: Yes, those are
20 things that I mention.

21 BY ATTORNEY CHANDLER:

22 Q. You also mention that another
23 weakness of Rambus DRAM was a "negative industry
24 perception of the royalty structure."

25 Could you explain that a little

1 bit more.

2 A. So the JEDEC committees were
3 working to standardize DRAM interfaces and
4 module interfaces.

5 Rambus had a different business
6 model, which involved designing memory devices
7 and modules and then licensing those designs to
8 semiconductor manufacturers; and there was, at
9 the time, a significant perception that the
10 Rambus royalty structure was going to be
11 detrimental to the industry.

12 Q. And did that negative perception
13 of the royalty structure of Rambus memory
14 devices persist through the 2004-2005 time
15 frame?

16 A. To some extent. I don't remember
17 the details. But by the time we were dealing
18 with XDR and direct Rambus, there was still some
19 concern about the price comparison between
20 Rambus DRAMs and, for example, the SDRAMs of the
21 day. And so it was an issue to some extent.
22 It's hard to quantify how much of an issue it
23 was.

24 Q. If I understand correctly, would
25 it be fair to say that the SDRAM memory devices

1 in the 2004 and 2005 time frame, including SDR,
2 DDR and DDR2, did not have a negative industry
3 perception with respect to any royalty
4 structures?

5 A. Not with regard to --

6 ATTORNEY WARRICK: Objection to
7 form.

8 THE WITNESS: There was not a
9 negative perception with regard to a royalty
10 structure, because although there was a lot of
11 cross-licensing with royalties amongst the
12 companies involved in the DRAM industry, it
13 wasn't of the same style and business model that
14 Rambus had.

15 There were other issues with the
16 JEDEC standardized memory modules that resulted
17 in negative perceptions of other varieties not
18 specifically about the royalty structure that I
19 mentioned here for Rambus.

20 BY ATTORNEY CHANDLER:

21 Q. If I understand your earlier
22 testimony, by the 2004-2005 time frame, the vast
23 majority of memory devices were JEDEC standard
24 SDRAM types of memory devices; correct?

25 A. Yes, that was my testimony.

1 Q. And -- but at the time of your
2 book marked as Exhibit 1097, the mid 1990s, it
3 sounds like back then you were writing a book
4 because perhaps it was not quite clear at that
5 point in time whether the Rambus DRAMs or the
6 JEDEC DRAMs or perhaps even another type of
7 memory device would win out in popularity.

8 Is that fair?

9 ATTORNEY WARRICK: Objection;
10 form.

11 THE WITNESS: Yes, there was a
12 great deal of uncertainty. Between 1992 or so
13 and 1997, there were probably 15 or 20 different
14 proposals for different DRAM architectures of
15 various sorts.

16 Everyone knew that what the
17 industry had been doing vis-a-vis the fast page
18 mode devices, which had been the staple for a
19 decade, was no longer adequate. But it was not
20 at all clear what direction the industry should
21 go in, and that was the motivation for the book.

22 BY ATTORNEY CHANDLER:

23 Q. But by the 2004 to 2005 time
24 frame, if I understand your testimony correctly,
25 it sounds like the JEDEC SDRAM memory devices

1 had proven themselves the most popular and
2 widely accepted; and the Rambus DRAM memory
3 devices were not nearly as popular by that time
4 frame.

5 Is that fair?

6 A. By that time frame, that's fair.
7 Technically, the Rambus memory architectures
8 were still superior to the SDRAMs vis-a-vis
9 bandwidth in particular; but from a commercial
10 perspective, you're correct.

11 Q. Please turn to page 337 of your
12 book marked as Exhibit 1097. Let me know when
13 you're there.

14 A. "Chip-Level Comparison." I am
15 there.

16 Q. A person of ordinary skill in the
17 art would have known about the chip-level
18 comparison of the different types of DRAM
19 described in your book in Chapter 9 starting on
20 page 337 in Exhibit 1097.

21 Is that fair?

22 ATTORNEY WARRICK: Objection;
23 form.

24 THE WITNESS: Certainly, a POSITA
25 in 2004-2005 would have been keenly aware that

1 the interfaces for these different memory types
2 were all different and not interchangeable; and
3 to the extent that, consequently, the POSITA
4 would understand that a chip-level comparison of
5 those interfaces would be required in order to
6 make any sort of decision between one or another
7 or how to use one or another, so in that
8 respect, yes.

9 Having a comprehensive
10 comparison, as I lay out in Chapter 9, of all of
11 the different varieties, that would probably be
12 not something a POSITA would have had the time
13 or inclination to prepare themselves.

14 BY ATTORNEY CHANDLER:

15 Q. Please turn to page 353 of
16 Exhibit 1097. Let me know when you're there.

17 A. System-Level Comparison, I am
18 there.

19 Q. A person of ordinary skill in the
20 art would have known about the system-level
21 comparison of different types of DRAM as
22 described in Chapter 10 of your book starting on
23 page 353 of Exhibit 1097; correct?

24 ATTORNEY WARRICK: Objection;
25 form.

1 THE WITNESS: Generally speaking,
2 to the same extent as we discussed for the
3 chip-level comparison, the -- a POSITA would,
4 again, be looking at a system-level comparison
5 for understanding the relative merits of
6 different DRAM architectures.

7 BY ATTORNEY CHANDLER:

8 Q. All right. Please go pretty much
9 towards the end of Exhibit 1097 and sort of back
10 up to page 809 and let me know when you're
11 there.

12 A. 809.

13 Yes.

14 Q. Starting on page 809 of your book
15 marked as Exhibit 1097, you include a copy of a
16 Rambus DRAM data sheet that runs through
17 page 840 of your book; correct?

18 A. Yes.

19 Q. On page 821 of your book marked
20 as Exhibit 1097, you provide a description of
21 the registers used by a Rambus DRAM to store
22 configuration information; is that correct?

23 A. I'm sorry. Which page was that?

24 Q. 821.

25 A. Yes. I list -- the data sheet

1 that I copied into the book with permission of
2 Rambus does list the register types, yes.

3 Q. So, for example, as shown in
4 Table 7 on page 821 of Exhibit 1097, the
5 register 0 of a Rambus DRAM stores the device
6 type; correct?

7 A. That's what it says there.

8 Q. Register 1 of a Rambus DRAM
9 stores the device ID, which is used to specify
10 the base address for the memory device; correct?

11 A. That's what it says.

12 Q. Register 2 of a Rambus DRAM
13 stores the delay, which is used to specify the
14 CAS timing parameters; correct?

15 ATTORNEY WARRICK: Objection;
16 form.

17 THE WITNESS: CAS timing
18 parameters, register 2; yes.

19 BY ATTORNEY CHANDLER:

20 Q. And there are a number of other
21 registers listed in Table 7 on page 821 of your
22 book marked as Exhibit 1097; correct?

23 A. Yes. They're all listed there.

24 Q. On page 822 of Exhibit 1097, the
25 data sheet provides more detail about some of

1 the registers that were listed on the previous
2 page in Table 7; correct?

3 A. It appears that way, yes.

4 Q. For example, at the top of page
5 822 of Exhibit 1097, it shows that the device ID
6 field in register 1 of a Rambus DRAM as compared
7 to address 35:21 of a request packet to
8 determine if that particular memory device has
9 been selected; correct?

10 ATTORNEY WARRICK: Objection;
11 form.

12 THE WITNESS: That's what it says
13 there, yes.

14 BY ATTORNEY CHANDLER:

15 Q. As another example in the middle
16 of page 822 of Exhibit 1097, it shows that the
17 delay register 2 of a Rambus DRAM includes a
18 byte 1 that sets a read delay that is normally
19 7-bus clocks, and it also includes a byte 3 that
20 sets a right delay that is normally 1-bus clock;
21 correct?

22 A. Right. And, again, all of this
23 stuff is for the 16-megabit base, I believe,
24 RDRAM.

25 ///

1 (Exhibit Number 1069 was previously
2 marked for identification.)

3 BY ATTORNEY CHANDLER:

4 Q. All right. Could you pull up
5 Exhibit 1069, which I might not have previously
6 put in the chat, so let me just put it in there.
7 May be duplicative, but it's the --

8 A. I don't have that up, so it will
9 be helpful.

10 Q. It's the same exhibit in both
11 IPRs, and it's the paper written by
12 Professor Jacob in 2002. It's in the chat. Let
13 me know when it up on your screen.

14 A. I have that up on my screen.

15 Q. And have you reviewed
16 Exhibit 1069, Professor Jacob's article about
17 "Synchronous DRAM Architectures," dated
18 December 10th, 2002?

19 A. I have read it all in past -- in
20 the past. In this matter, I reviewed portions
21 of it more extensively than other portions.

22 Q. All right. Please turn to page 2
23 of Exhibit 1069 and carrying over to page 3
24 where Professor Jacob discusses chip-select
25 signals, and let me know when' you're there.

1 A. I'm on page 2.

2 Q. Professor Jacob explains on the
3 bottom right of page 2 of Exhibit 1069 in the
4 third sentence that "The chip-select bus
5 contains a separate wire for every rank of DRAM
6 in the system."

7 Correct?

8 A. And this is in the context of
9 JEDEC-style organizations that he's referring to
10 in the previous paragraph; yes.

11 Q. Is the description by
12 Professor Jacob of the chip-select signal on the
13 bottom right of page 2 of Exhibit 1069
14 consistent with the understanding of a person of
15 ordinary skill in the art?

16 A. Again, a person of ordinary skill
17 in the art in 2004-2005 would understand that
18 for JEDEC-style organizations being discussed
19 here in this page of Jacob's article, that for a
20 plurality of ranks, there's a separate
21 chip-select for each rank, generally speaking.

22 Q. And at the beginning of that
23 paragraph in the bottom right of page 2,
24 Exhibit 1069, the Professor Jacob states that
25 the chip-select bus is essential in a

1 JEDEC-style memory system; correct?

2 A. Unless you only have one rank.
3 In this case, it's only a single signal. But,
4 yes, if you have a plurality of ranks, you need
5 a plurality of chip-select signals and,
6 therefore, a chip-select signal bus.

7 Q. And do you believe it's
8 consistent with the understanding of a person of
9 ordinary skill in the art that the chip-select
10 bus is essential in a JEDEC-style memory system?

11 ATTORNEY WARRICK: Objection;
12 form.

13 THE WITNESS: Yes. Because
14 JEDEC-style -- JEDEC-defined and standardized
15 SDRAMs have chip-select inputs, you need to have
16 a mechanism for feeding those signals, so it is
17 essential. If you don't have some mechanism for
18 triggering the chip-select inputs of the SDRAMs,
19 they will not operate as you expect.

20 BY ATTORNEY CHANDLER:

21 Q. On page 3 of Exhibit 1069 in the
22 first full sentence, Professor Jacob states:

23 "Even though all DRAMs in the
24 system are connected to the same
25 address and control buses and could,

1 in theory, all respond to the same
2 request at the same time, the
3 chip-select bus prevents this from
4 happening."

5 Did I read that accurately?

6 A. Yes, you did. Yes, you have.

7 Q. Is that description by
8 Professor Jacob consistent with the
9 understanding of a person of ordinary skill in
10 the art with respect to a JEDEC-style memory
11 system?

12 ATTORNEY WARRICK: Objection;
13 form.

14 THE WITNESS: No, not entirely,
15 because clearly there are memory subsystems with
16 modules where all the DRAMs are not connected to
17 the same address and control buses and that
18 there is a -- in some circumstances, a plurality
19 of address and control buses for different
20 ranks. It's highly variable. This is a
21 simplification for the purposes of pedagogy on
22 Dr. Jacob's part.

23 BY ATTORNEY CHANDLER:

24 Q. To be clear, are you saying that
25 in JEDEC-style memory systems, such as DDR and

1 DDR2, that different memory devices get
2 different address lines?

3 A. No, that's not what I said.

4 Q. In the context of JEDEC-style
5 memory systems, do you agree with the first full
6 sentence on page 3 of Exhibit 1069?

7 ATTORNEY WARRICK: Objection;
8 form.

9 THE WITNESS: Again, as I said a
10 moment ago, this sentence is a simplification
11 and generalization for the purposes of pedagogy
12 on Dr. Jacob's part. It is not universally
13 true.

14 BY ATTORNEY CHANDLER:

15 Q. Is it true with respect to DDR
16 SDRAM and DDR2 SDRAM?

17 A. Often but not always.

18 Q. So to be clear, your opinion is
19 that it's typically the case in a JEDEC-style
20 memory system that all the DRAMs in the system
21 are connected to the same address and control
22 buss and could in theory respond to all the same
23 requests at the same time, but the chip-select
24 bus prevents that from happening? Is that a
25 fair summary of your opinion?

1 ATTORNEY WARRICK: Objection;
2 form.

3 THE WITNESS: So, again, talking
4 about what a POSITA would understand in 2004 and
5 2005, a POSITA would understand that, depending
6 on the size of the memory system employing JEDEC
7 standardized memories, you could have a single
8 memory bus -- I'm sorry -- a single control and
9 address bus that wound its way to all of the
10 memory devices; but you could also have a
11 plurality of parallel address and control buses,
12 each of which service a subset of the totality
13 of JEDEC-compliant SDRAMs.

14 BY ATTORNEY CHANDLER:

15 Q. What was the more typical
16 arrangement?

17 A. There was -- it was all a matter
18 of what type of system we're talking about.
19 There was no one typical arrangement.

20 Q. For UDIMMs and RDIMMs, there was
21 no typical arrangement for the address lines,
22 control lines and chip-select lines?

23 ATTORNEY WARRICK: Objection;
24 form.

25 THE WITNESS: That's not what I

1 said.

2 BY ATTORNEY CHANDLER:

3 Q. Were UDIMMs and RDIMMs common
4 examples of memory modules in the 2004-2005 time
5 frame?

6 A. UDIMMs, certainly.
7 RDIMMs, not so much, by my
8 recollection; but, again, we'd have to look at
9 some market data to see.

10 Q. For a single memory module with
11 multiple ranks of memory devices, do you agree
12 with the statement in the first sentence of
13 page 3 of Exhibit 1069?

14 A. That single module --
15 ATTORNEY WARRICK: Objection;
16 form.

17 THE WITNESS: That's a JEDEC
18 standardized module of some type.

19 BY ATTORNEY CHANDLER:

20 Q. I would use Professor Jacob's
21 phrase, which is a JEDEC-style memory system.

22 ATTORNEY WARRICK: Same
23 objection.

24 THE WITNESS: So with that
25 clarification, would you repeat the question,

1 please.

2 BY ATTORNEY CHANDLER:

3 Q. For a single memory module with
4 multiple ranks of memory in a JEDEC-style memory
5 system, do you agree that even though all the
6 DRAMs in the system are connected to the same
7 address and control buses and could in theory
8 all respond to the same requests at the same
9 time, the chip-select bus prevents this from
10 happening?

11 ATTORNEY WARRICK: Objection;
12 form.

13 THE WITNESS: I don't think that
14 question is well phrased, because it's
15 conflating multiple ranks on a JEDEC-style
16 module and then a chip-select bus, which
17 generally would refer to the bus that's outside
18 of the module; but -- so I'm going to stop
19 there.

20 BY ATTORNEY CHANDLER:

21 Q. Okay. I'm using the phrase as in
22 Professor Jacob's paper from 2002, who I believe
23 you said earlier was an expert in the field.

24 A. And he's a professor. So he's
25 teaching here and is not saying things that are

1 necessarily universally true, but we're just
2 saying he's trying to get across a particular
3 point about the function of chip-selects and how
4 they're used in systems. So I do not believe
5 that he's making a general absolute statement
6 about how all memory subsystems using SDRAMs are
7 constructed, one module or multiple modules, one
8 rank or multiple ranks.

9 Q. Let me ask more generally, then.

10 Do you believe a person of
11 ordinary skill in the art would have the general
12 understanding provided by Professor Jacob at the
13 bottom of page 2 of Exhibit 1069, carrying over
14 to the top of page 3, about chip-selects?

15 ATTORNEY WARRICK: Objection;
16 form.

17 THE WITNESS: Yes. Reading
18 Professor Jacob's paper, a POSITA would
19 understand that Dr. Jacob is talking about the
20 function of chip-selects relative to the
21 function of the address and control buses and
22 how together they determine which memories do
23 what in any particular circumstance.

24 BY ATTORNEY CHANDLER:

25 Q. Is it fair to say that Professor

1 Jacob is teaching that it's normal or common for
2 all of the memory devices on a memory module
3 that receive the same address signal and the
4 same command signal, even if those memory
5 devices are in different ranks?

6 A. I think it is understood by a
7 POSITA that that's certainly possible, if not
8 common, but not necessarily true.

9 Q. And what Professor Jacob is
10 teaching in the bottom of page 2, carrying over
11 to the top of page 3 of Exhibit 1069, is even
12 though it's common for all the memory devices to
13 receive the same address and command signals,
14 despite being in different ranks, there is a
15 chip-select wire for each rank of memory devices
16 that enables one rank of memory devices to
17 respond to a read or write command while the
18 other ranks are not selected to respond to the
19 read or write command.

20 Is that a fair summary of what
21 Professor Jacob is trying to teach here with
22 this paper?

23 ATTORNEY WARRICK: Objection;
24 form.

25 THE WITNESS: It's a fair

1 summary. And, in particular, the important
2 aspect is that when there's multiple ranks, one
3 of the chip-selects is active and the others are
4 not active in order to get one rank to perform
5 an operation and the other ranks to not perform
6 the same operation.

7 BY ATTORNEY CHANDLER:

8 Q. Turn to page 7 of Exhibit 1069
9 and let me know when you're there.

10 A. 7? I am there.

11 Q. On page 7 of Exhibit 1069 on the
12 left side starting at Section 1.3, there's a
13 description of contemporary DRAM architectures;
14 including in Section 1.3.1 DDR SDRAMs; and then
15 in 1.3.2, Rambus DRAMs; correct?

16 A. Correct.

17 Q. And in Section 1.3.1 on page 7 of
18 Exhibit 1069, Professor Jacob states that DDR
19 SDRAMs double the bandwidth by transferring data
20 at both edges of the clock; correct?

21 A. Double the data rate relative to
22 SDRAM -- SDRAMs is what's missing from that
23 sentence. And it's relative to both -- it's
24 twice per clock period. The transmission of the
25 data is not relative to the edges of the clock

1 but relative to edges of the data strobe.

2 So, again, for succinctness,
3 Professor Jacob is taking a few liberties with
4 the precision of his statements.

5 Q. And is everything that you just
6 said in your last answer something that you
7 believe a person of ordinary skill in the art
8 would have understood?

9 ATTORNEY WARRICK: Objection to
10 form.

11 THE WITNESS: As we have
12 discussed many times, the -- in 2004 and 2005, a
13 POSITA would have been familiar with double data
14 rate SDRAMs and, therefore -- and how they
15 operate. So, yes.

16 BY ATTORNEY CHANDLER:

17 Q. Professor Jacob goes on to state
18 in the middle of Section 1.3.1 on page 7 of
19 Exhibit 1069, that "DDR DRAM are very similar to
20 single data rate SDRAM in all other
21 characteristics."

22 Correct?

23 A. He does say that. I disagree
24 with it, but he does say that.

25 Q. And then in Section 1.3.2 on the

1 bottom left of page 7 of Exhibit 1069,
2 Professor Jacob discusses Rambus DRAM
3 abbreviated RDRAM; correct?

4 A. That is the first of the three
5 types of Rambus DRAM that he discusses in his
6 paper.

7 Q. And the three types of
8 Rambus DRAM that he discusses in Exhibit 1069
9 are RDRAM, concurrent RDRAM and direct RDRAM;
10 correct?

11 A. That's correct, yes.

12 Q. In Section 1.3.2 at the bottom
13 left of page 7 of Exhibit 1069, Professor Jacob
14 explains that Rambus DRAM:

15 "Does not use dedicated lines
16 for address, control, data and
17 chip-select-select signals -- but,
18 instead, the bus is fully
19 multiplexed, which means that
20 address, control, data, and
21 chip-select-select information all
22 travel over the same set of
23 electrical wires but at different
24 times."

25 Correct?

1 A. That's what he says. I don't
2 think it's particularly accurate.

3 Q. Do you think the description that
4 Professor Jacob provided that I just read from
5 the bottom of page 7 of Exhibit 1069 about
6 Rambus DRAM was consistent with the
7 understanding of a person of ordinary skill in
8 the art?

9 A. No. I think the person of
10 ordinary skill that did happen to know about the
11 original RDRAMs would recognize that there's no
12 chip-select information in that architecture,
13 that everything is address-based.

14 Q. When you say everything is
15 address-based, there are certain address signals
16 that select the chip?

17 A. As we saw it when we looked at
18 the RDRAM data sheet that was attached to my
19 book, we saw that the register defined the base
20 address of -- that a particular RDRAM would
21 respond to.

22 Do you remember that?

23 Q. Yes.

24 A. Okay. So the -- there is no
25 chip-select-select signal as it exists in any of

1 the JEDEC standardized memory devices; instead,
2 there is only the -- the memory controller
3 throws the address out there. And whichever
4 RDRAM matches the address or the -- that the
5 accessed address is within the range of that
6 RDRAM, that RDRAM says, oh, it's for me; I'm
7 going to do something. So there's no
8 chip-select signal, and there's no chip-select
9 information per se in the command packet for
10 that generation of RDRAM.

11 Q. But as indicated by
12 Professor Jacob, and if I understand your
13 explanation correctly, with Rambus DRAM, it's
14 still possible that only a subset of the memory
15 devices are selected to perform a read or write
16 operation; correct?

17 A. There is, in fact, a single one
18 that, if everything is programmed correctly --
19 it's a caveat -- that a single RDRAM will
20 respond to a command, based purely on a decoding
21 of the address and no additional information
22 other than the address.

23 Q. But regardless of whether you
24 call it address or something else, the net
25 result is that one or more chips are selected to

1 perform the memory commands in a Rambus DRAM
2 system; correct?

3 ATTORNEY WARRICK: Objection;
4 form.

5 THE WITNESS: Again, I'm going to
6 take issue with your terminology.

7 The memory device is not selected
8 by the memory controller, as is typical when we
9 use the term "chip-select," as a signal that
10 goes from the memory controller to the
11 individual DRAM or DRAMs.

12 In this case, the DRAM
13 autonomously decides that the transaction that
14 has been requested can only be handled by it.
15 And it's an internal decision based on an
16 address information, which is profoundly
17 different from a chip-select information or --
18 that is being inaccurately called out here by
19 Jacob.

20 BY ATTORNEY CHANDLER:

21 Q. In fairness, the Rambus DRAM are
22 not autonomous. They don't decide on their own
23 whether to --

24 A. Yes, they do. They do. They
25 receive a packet that has a --

1 (Simultaneous cross-talk.)

2 Q. The memory controller determines
3 the address; right? The memory controller says,
4 I want to write to this address.

5 A. Yes, but it doesn't say --

6 ATTORNEY WARRICK: Objection to
7 form.

8 BY ATTORNEY CHANDLER:

9 Q. Go ahead.

10 A. The memory controller doesn't
11 say, I want the third DRAM to respond.

12 It says, I have an address;
13 whoever is responsible for this address, deal
14 with it.

15 Q. But let's back up a little bit.

16 It's the memory controller that
17 programs the registers in the Rambus DRAM memory
18 devices; right?

19 A. Correct.

20 Q. So the memory controller programs
21 the Rambus DRAM memory devices with those
22 registers, and then the memory controller sends
23 out the address information that's going to
24 select one or more of the Rambus DRAM memory
25 devices. So it's the memory controller that is

1 in control; right? It's not like the
2 Rambus DRAMs are totally autonomous; it's the
3 memory controller that's controlling things.

4 A. In this --

5 ATTORNEY WARRICK: Objection;
6 form.

7 THE WITNESS: In this particular
8 architecture, the RDRAMs are essentially
9 autonomous and that when the -- granted, the
10 memory controller has initialized the memory
11 subsystem. And you keep saying "one on more
12 RDRAMs respond." Exactly one RDRAM responds to
13 any transaction on the channel.

14 BY ATTORNEY CHANDLER:

15 Q. The memory controller can program
16 the register in the Rambus DRAM; right? So it's
17 up to the memory controller to decide how those
18 registers in the RD program are programmed and,
19 therefore, how the memory devices will act.

20 The memory devices aren't
21 autonomous in the sense that they can disregard
22 what the memory controller tells them. The
23 memory controller programs them. The memory
24 controller sends the address signal. And then
25 the memory devices are required to follow what

1 the memory controller has done; right?

2 ATTORNEY WARRICK: Objection;
3 form.

4 THE WITNESS: But they're also
5 autonomous in that the memory devices determine
6 when to respond to the request. And there is a
7 profound conceptual difference between an
8 address and the chip-select. And you see that
9 pervasively throughout the JEDEC
10 standardization -- standards for SDRAMs and for
11 all other devices that have chip-select inputs.
12 They were conceptually and temporally -- not --
13 they are conceptually different from addresses.

14 In this case, for the RDRAMs
15 being described in this paragraph, there are no
16 chip-select signals; there's no chip-select
17 signal lines. The memory controller, when it's
18 sending out an address as part of a packet, a
19 command packet, it's not even cognizant of which
20 memory is going to respond, because that's
21 handled a priori in the programming of the
22 registers.

23 So the whole concept of
24 chip-select is dramatically different in this
25 generation of RDRAMs.

1 BY ATTORNEY CHANDLER:

2 Q. In your opinion, but apparently
3 not in the opinion of Professor Jacob. Fair?

4 ATTORNEY WARRICK: Objection;
5 form.

6 THE WITNESS: I don't think this
7 is a matter of opinion. This is a matter of
8 fact. This is exactly how the RDRAMs operate --
9 operated, since they don't exist anymore. And
10 the fact that Jacob has preferred to cast
11 this -- using the language of SDRAMs instead of
12 the language of RDRAMs -- again, is either
13 pedagogical or an error. And you can decide
14 which. But it is, in fact, not accurate.

15 BY ATTORNEY CHANDLER:

16 Q. I want to push back on your
17 statement about Rambus DRAM being autonomous.

18 When you say they're autonomous,
19 the reality is that the memory controller first
20 programs them and the memory controller knows
21 how they're going to act based on that
22 programming. And then the memory controller
23 later will send signals, including address
24 information, and the memory controller knows how
25 the Rambus DRAM will act in response to those

1 signals. And so it's not really fair to say
2 that the memory device is autonomous.

3 A. Well --

4 Q. The memory device is still being
5 controlled by the memory controller, and the
6 memory controller in its own way is able to
7 select the memory devices that it wants.

8 ATTORNEY WARRICK: Objection to
9 form.

10 THE WITNESS: The question is:
11 What do you mean by "autonomous"?

12 If you get into an autonomous
13 vehicle today and you say, "Go home," is the car
14 autonomously taking you home or is it responding
15 to your command?

16 And the same distinction is
17 happening within the Rambus RDRAMs in that the
18 RDRAMs are watching for control packets. When
19 they see a control packet, they look at the
20 address in that control packet and decide
21 whether it's for me or not. That's purely
22 autonomous.

23 If the memory controller sent out
24 an address that was outside of the range of all
25 of the memories on the channel, no one would

1 respond. Nothing would happen.

2 The response to the command
3 packet and the decoding of the address therein
4 and determining what to do and when to do it --
5 that's the critical part here -- is purely
6 localized within the RDRAM. And the memory
7 controller accepts the result. It gets back an
8 indication when that data is going to come back.

9 Or in particular, the memory
10 device can mask the entire transaction and say,
11 I can't do this right now. And if that's not a
12 sign of autonomy, then, you know, I'm not sure
13 what is.

14 BY ATTORNEY CHANDLER:

15 Q. You just referred to a packet.
16 And on page 7 of Exhibit 1069 on the upper
17 right, Professor Jacob also refers to a packet
18 transaction.

19 What's a packet transaction?

20 A. A packet transaction would be a
21 transaction that is initiated by a command
22 packet.

23 Q. Can you explain a little bit
24 more. Seems a bit circular.

25 A. Well, the -- there are

1 transactions. In SDRAMs, transactions are
2 initiated by commands on the command bus and --
3 and the chip-select; and the details of it are
4 determined by the address bus.

5 In Rambus-style memory devices,
6 such as the RDRAM, concurrent RDRAM or direct
7 RDRAM, the control information is not sent over
8 individual wires but are aggregated into
9 multiple time periods over a multiplexed command
10 bus, and they vary between the different Rambus
11 devices and that each signal wire has multiple
12 purposes at different points in time, whether
13 it's command or address or something else,
14 masked in some cases.

15 Q. Are the packet transactions used
16 by Rambus memory devices transmitted on
17 electrical wires using signals?

18 ATTORNEY WARRICK: Objection;
19 form.

20 THE WITNESS: Yes.
21 BY ATTORNEY CHANDLER:

22 Q. On page 7 of Exhibit 1069, in
23 both the heading 1.3.2 that we looked at as well
24 as the text, there are those three different
25 types of Rambus DRAM: The original RDRAM,

1 concurrent RDRAM and direct RDRAM.

2 And my question is: In your
3 opinion, would a person of ordinary skill in the
4 art have known about those three different types
5 of Rambus memory devices?

6 A. By 2004-2005, the original RDRAM
7 was long gone. The concurrent RDRAM was also
8 gone, and direct RDRAM was the principal Rambus
9 device that was in the marketplace. And there's
10 also the XDR RDRAMs that were also in the
11 marketplace that's referred to in, I believe,
12 one of the patents at issue here. Let me
13 double-check that.

14 I think it's Perego that refers
15 extensively to XDR.

16 Q. On page 7 of Exhibit 1069 on the
17 right side in the middle paragraph,
18 Professor Jacob explains that the original
19 Rambus DRAM design was changed because it did
20 not have separate segments of the bus dedicated
21 to separate functions and, thus, it was not
22 considered well suited to the TC main memory
23 market; correct?

24 A. Yes, it says that.

25 Q. Is that consistent with your

1 understanding?

2 A. Well, he's citing my work. So,
3 presumably, he found it somewhere in there.

4 The original base RDRAM, the
5 autonomy of the DRAMs was difficult to control
6 by the memory controller, and the scheduling of
7 the bus was very challenging. So in that sense,
8 he is accurate with regard to the original
9 RDRAM.

10 Q. And then Professor Jacob goes on
11 to explain on the right side of page 7 of
12 Exhibit 1069, in the second paragraph, that the
13 next generation of Rambus memory called
14 concurrent RDRAM had a "bus that was divided
15 into separate address, command and data segments
16 reminiscent of a JEDEC-style DRAM organization."

17 Correct?

18 A. I don't think that that's an
19 accurate characterization of "concurrent." I
20 think it's another instance where he's made a
21 mistake, but we'd have to look at a concurrent
22 RDRAM data sheet to verify that.

23 Q. In concurrent RDRAM, the width of
24 the data bus segment was 1 byte, or 8 bits;
25 correct?

1 A. 8 or 9 bits; yes.

2 Q. And then Professor Jacob goes on
3 to explain on the bottom right paragraph of
4 page 7 of Exhibit 1069, that the next generation
5 of Rambus DRAM called direct RDRAM, increased
6 the width of the data segment of the bus to 2
7 bytes, or 16 bits; but the segments remained
8 separate and dedicated similar to a JEDEC-style
9 organization.

10 Correct?

11 A. Which paragraph are you reading
12 from? The last paragraph on page 7? Right.

13 Q. Yes.

14 A. Let me read that again.

15 (Witness reviews document.)

16 Yeah, so this paragraph or this
17 portion of this paragraph explicitly
18 mischaracterizes the direct RDRAM control
19 structure and that the -- it calls the address
20 segment 5 bits and the control segment 3 bits.
21 That's completely inaccurate.

22 In fact, the control portion of
23 the direct RDRAM architecture has 3 bits for
24 column commands, including column commands and
25 column addresses, and 3 bits for row commands

1 and row addresses.

2 So his characteristics of those
3 5-bits and 3-bit segments, as being for address
4 of control, that's just flat-out inaccurate.
5 Not a matter of interpretation or pedagogy.

6 Q. A person of ordinary skill in the
7 art knew about Rambus direct RDRAM; correct?

8 A. We have agreed that based on the
9 timing and the reference in, for example,
10 Perego, that, yes, a POSITA in 2004-2005 would
11 have familiarity with direct RDRAM.

12 Q. Could you turn back to
13 Exhibit 1070, the Jacob textbook, and go to
14 page 21. Let me know when you're there.

15 A. Okay. Which page again, please?

16 Q. 21.

17 A. At the very beginning?

18 Q. Yes.

19 A. I'm on page 21.

20 Q. On page 21 of Exhibit 1070,
21 Professor Jacob compares SDRAM and Rambus
22 architectures both in the figure at the bottom
23 of the page as well as in the text starting at
24 the bottom left and carrying over to the right
25 side of the page; correct?

1 A. Does appear that way.

2 Q. And as shown on the left side of
3 the figure on page 21 of Exhibit 1070, an
4 example of SDRAM is DDR memory, which, as we
5 discussed, had been standardized by JEDEC;
6 correct?

7 A. That's how he's labeled it, yes.

8 Q. Professor Jacob explains on the
9 right side on page 21 of Exhibit 1070 that
10 Rambus uses fewer address and command pins than
11 SDRAM and, thus, incurs an additional latency at
12 the command level; correct?

13 A. That's what he says.

14 Q. And a person of ordinary skill in
15 the art would have understood that about the
16 Rambus architecture; correct?

17 A. No, I don't think a POSITA in
18 2004-2005 would recognize that the delay from
19 the first portion of a command arriving at a
20 DRAM on a direct RDRAM channel to the last
21 portion of that command arriving on the same
22 portion or the same column or row command bus
23 constitutes a -- an additional latency.

24 Q. Dr. Jacob explains on the right
25 side of page 21 of Exhibit 1070 that Rambus's

1 longer channel results in longer read command
2 latencies and longer bus turnaround times;
3 correct?

4 A. There is a longer -- let me
5 restart that answer.

6 The appropriate comparison is the
7 maximum length of the direct RDRAM channel. And
8 the longest signal trace length in a memory --
9 JEDEC SDRAM-compliant multimodule memory
10 implementation, as shown in Figure 0v.7 on the
11 left-hand side.

12 In fact, four DDR SDRAMs, the
13 maximum signal path length for address is going
14 to be shorter than the maximum channel length
15 for a direct RDRAMs; but in direct RDRAM
16 systems, if you don't have a full-length
17 channel, you don't suffer this problem. And
18 most direct RDRAM channels would have been
19 significantly shorter than the maximum length.

20 So the comment with regard to
21 longer read command latencies is not universally
22 true and, in fact, most often not true.

23 The longer bus turnaround times
24 is also inaccurate, because in the direct -- in
25 the SDRAM and DDR SDRAM memory systems, the

1 clock cycle is very much longer. So a single
2 cycle of bus turnaround time is much longer than
3 a comparable turnaround time on the direct
4 channel.

5 So both halves of this sentence
6 are, again, sometimes true -- in the worst case,
7 probably true -- but in the typical case, not
8 likely to be true.

9 So, again, from a pedagogical
10 perspective, the sentence is not false; but it
11 is a simplification of the reality of the
12 situation.

13 Q. In the figure on the bottom of
14 page 21 of Exhibit 1070, Professor Jacob
15 compares a JEDEC-style memory system on the left
16 with 8 memory devices to a Rambus memory system
17 on the right is 8 memory devices; right?

18 A. Yes, it does.

19 Q. And Professor Jacob teaches that
20 the JEDEC-style memory system on the left has a
21 short and wide channel; whereas, in comparison,
22 the Rambus-style memory system on the right has
23 a long and narrow channel; correct?

24 A. He says that, but it's not
25 precisely accurate. The length of the signal

1 lines for the command and address and
2 chip-select on the memory system on the left,
3 the SDRAM memory system, is the full width of
4 the module plus the length of the trace from the
5 controller to the start of the module, which in
6 contrast for the Rambus style -- for the direct
7 Rambus memory system, the maximum length of the
8 channel is two module lengths.

9 And these modules are the same
10 size, because the RIMMs, which are the Rambus
11 module, are the same width as the DIMMs -- the
12 DDR and SDRAM DIMMs that were in place at the
13 time.

14 So the difference in the trace
15 length between -- the worst-case trace length
16 between these two examples is relatively small.
17 And certainly if you end up with a single-module
18 memory system, in both cases, the Rambus-style
19 architecture will be better. It will have a
20 shorter worst-case signal path length.

21 Q. But most computers have at least
22 two memory slots or two memory modules; right?

23 A. "Most" is a, I think, an
24 overgeneralization, particularly since the
25 Rambus -- direct Rambus memory systems, the

1 memory controllers for that typically had a
2 single controller for each module, which was
3 practical, because the total number of signals
4 was very much smaller.

5 So for the same number of pins on
6 the controller, you could have two Rambus
7 channels in fewer pins than you had one x64
8 SDRAM memory system as per the figure on the
9 left of Figure 0.v.7.

10 So for most -- it's actual
11 circumstances where the apples-to-apples
12 comparison is a comparable number of pins on the
13 controller; the direct Rambus JEDEC-style memory
14 system is preferred, has shorter maximum signal
15 lengths.

16 And in that respect, Jacob's
17 sentence in the middle of the right column of
18 page 21 is not accurate for most cases. It's
19 pedagogically a reasonable thing to teach, but
20 it's not necessarily accurate.

21 Can we take a break, please?

22 Q. Can you go a few more minutes so
23 we can sort of finish the discussion on this
24 page, or do you want to take a break right now?

25 A. It's been almost an hour and a

1 half, so I would prefer we -- if it's one more
2 question, go for it. If it's more than one, we
3 should stop.

4 ATTORNEY CHANDLER: I won't make
5 any promises, so let's take a break.

6 THE WITNESS: Okay. Break it is.
7 Ten minutes, please.

8 THE VIDEOGRAPHER: Off the record
9 at 3:21 p m. Pacific Time.

10 (Recess taken from 3:21 p.m. to
11 3:35 p.m.)

12 THE VIDEOGRAPHER: On the record
13 at 3:35 p.m. Pacific Time.

14 THE WITNESS: May I add a
15 sentence to my last answer?

16 BY ATTORNEY CHANDLER:

17 Q. Yes. And I was actually going to
18 ask you more generally if there are any
19 corrections or clarifications you'd like to make
20 to any of your testimony earlier today to far.

21 A. So not generally. But with
22 regard to this last interchange about Jacob's
23 writing, it's really difficult to make real
24 apples-and-apples comparisons across memory
25 types. And I'm not criticizing Jacob for making

1 these bold generalizations, because he's writing
2 a textbook.

3 But when we're doing -- in this
4 venue when we are trying to be as precise as
5 possible, it's important to really try hard to
6 think about what the proper comparison really
7 is.

8 And I'm sure you'd find it in my
9 own writing if you looked hard enough where in
10 order to fit into a reasonable-sized-length
11 article, you make some statements that are true
12 most of the time or even some of the time or
13 that get a particular point across.

14 But here when you're asking me
15 questions about a comparison between an SDRAM
16 and a direct Rambus memory system, it's a very
17 complicated comparison. That's all.

18 Q. Would it be fair to say that a
19 person of ordinary skill in the art would
20 understand the trade-offs between a DDR memory
21 system and a Rambus memory system, as
22 summarized, for example, on page 21 of the Jacob
23 textbook marked as Exhibit 1070?

24 ATTORNEY WARRICK: Objection;
25 form.

1 THE WITNESS: A person of
2 ordinary skill in 2004-2005 on first blush would
3 understand some of these trade-offs; and as a
4 detailed comparison was undertaken towards a
5 specific design, the trade-offs would clarify
6 and become more nuanced.

7 So the trade-offs expressed here
8 by Jacob on page 21 are a very high level and
9 not necessarily accurate in most or even many
10 circumstances.

11 BY ATTORNEY CHANDLER:

12 Q. On page 21 of Exhibit 1070, is it
13 fair to say that one of the trade-offs that
14 Professor Jacob is trying to convey is that a
15 DDR memory system as shown in the bottom left
16 has what he would characterize as a short and
17 wide channel; whereas, a Rambus-style memory
18 system, as illustrated on the right, has what he
19 would characterize as a long and narrow channel?

20 At a high level, do you think a
21 person of ordinary skill in the art would
22 understand that difference between a DDR-type
23 memory system and a Rambus-type memory system?

24 A. Yes. A person of ordinary skill
25 in the art would understand that the topologies

1 are dramatically different, but that person of
2 ordinary skill would also recognize that an
3 SDRAM memory system of the style shown on the
4 left consumes about 120 pins on the controller;
5 whereas, at Rambus-style architecture on the
6 right consumes about 30 pins.

7 And, therefore, if your
8 particular design has a shortage of pins or if
9 the cost of the pins is factored into the
10 equation, it completely upsets that simplistic
11 comparison that Jacob undertakes here.

12 Q. In fairness, on the right side of
13 page 21 of Exhibit 1070, about -- several
14 sentences up from the bottom, Jacob explains
15 that the width and depth of the memory channels
16 impact the bandwidth, the latency, the pin count
17 and various cost components of the respective
18 memory systems; correct?

19 A. But what he doesn't say is that
20 the consequence of those parameters being
21 different means that his previous statement is
22 not accurate all the time.

23 Q. Would it be fair to say a person
24 of ordinary skill in the art would understand
25 that if you change the width and depth of the

1 memory channels, that there will be impacts on
2 bandwidth, latency, pin count and cost
3 components of the memory system?

4 ATTORNEY WARRICK: Objection;
5 form.

6 THE WITNESS: Yes. A POSITA
7 reading this entire section would understand
8 that the entire trade-off is complicated and
9 relies on a great many factors and that
10 generalizations, such as about the longer
11 channel, doesn't necessarily hold in their
12 particular case.

13 So, again, you can't rely on just
14 one sentence within a longer section about this
15 comparison.

16 BY ATTORNEY CHANDLER:

17 Q. On page 23 of Exhibit 1070 in the
18 table in the middle of the page labeled
19 Table 0v.3, Professor Jacob provides the
20 comparison of SDRAM, DDR SDRAM and direct
21 Rambus DRAM memory systems; correct?

22 A. Yes, I see that.

23 Q. And in this comparison on page 23
24 of Exhibit 1070, the DDR memory system in the
25 second row had a better peak bandwidth than the

1 direct Rambus DRAM memory system; correct?

2 A. That's what he shows here, yes.

3 Q. And the DDR memory system in this
4 table on page 23 of Exhibit 1070 has a sustained
5 bandwidth that's nearly identical to that of the
6 direct Rambus DRAM system -- DRAM system;
7 correct?

8 A. But, again, consuming or
9 utilizing a great many more pins on the memory
10 controller. I'm not sure where he got the 117
11 number for the direct Rambus. It's not at all
12 what I remember, but I'll take his word for it
13 for now.

14 Q. And do you believe a person of
15 ordinary skill in the art would have known about
16 these types of comparisons of DDR memory systems
17 to Rambus-style memory systems?

18 ATTORNEY WARRICK: Objection;
19 form.

20 THE WITNESS: I'm sorry. I was
21 trying to digest the table. Would you please
22 repeat the question for me.

23 BY ATTORNEY CHANDLER:

24 Q. Do you believe a person of
25 ordinary skill in the art would have known about

1 these types of comparisons of DDR memory systems
2 to Rambus-style memory systems along the lines
3 of what's shown in the table on the middle of
4 page 23 on Exhibit 1070?

5 ATTORNEY WARRICK: Objection;
6 form.

7 THE WITNESS: So certainly a
8 POSITA in 2004-2005 embarking on a specific
9 design where the choice of memory type was a
10 decision to be made would go through an
11 exhaustive comparison, much more detailed than
12 would be shown here in Table 0v.3 to fully
13 understand for the particular design being
14 undertaken what the bandwidth, cost and power,
15 for example, trade-offs would be and physical
16 area as well, obviously.

17 (Exhibit Number 2025 was previously
18 marked for identification.)

19 BY ATTORNEY CHANDLER:

20 Q. Could you please pull up
21 Exhibit 2025, which -- I don't think we've
22 talked about before, and I don't think I've put
23 in the chat before.

24 So let me go ahead and just put
25 it in the chat, even if this may be redundant,

1 so that you can see it. And let me know when
2 you have it up on your screen.

3 A. I have it on my screen.

4 Q. Have you reviewed Exhibit 2025
5 before, the Rambus direct RDRAM data sheet?

6 A. There was certainly -- there was
7 certainly a time when I knew it very well. I
8 have looked at parts of it relatively recently,
9 but I haven't studied it carefully in the last
10 week.

11 Q. On page 3 of Exhibit 2025, which,
12 to be clear, is the same exhibit in both IPRs,
13 Table 1, provides the pin description for a
14 Rambus direct RDRAM memory device; correct?

15 A. It's -- Table 1 is described as
16 "Pin Descriptions."

17 Q. And you see in the middle of
18 Table 1 of Exhibit 2025, there's a row for DQA;
19 and then at the bottom, there's a row for DQB;
20 and then directly above that, there are some
21 rows for RQ.

22 A. Yes.

23 Q. The Rambus direct RDRAM memory
24 device had dedicated data lines for the data
25 signals DQA and for the data signals DQB;

1 correct?

2 A. That's what this table shows.

3 Q. And then separate and apart from
4 the DQA and DQB data lines, the Rambus direct
5 RDRAM memory devices also had dedicated lines
6 for RQ0 through RQ7, which carried the signals
7 containing address and control information;
8 correct?

9 A. What this table shows is that
10 those RQ0 to RQ7 are conceptually divided into
11 two portions, one for row axes and the other
12 for column axes, as we discussed before the
13 break.

14 Q. RQ0 through RQ7 are separate
15 lines from DQA and DQB; correct?

16 A. Yes, they are.

17 Q. And RQ0 through RQ7, just to
18 treat them as a group -- I understand that there
19 may be a subdivision; but if you take RQ0
20 through RQ7 as a group, they would carry the
21 signals containing address and control
22 information; correct?

23 A. Yes. Those eight signal lines
24 carry all address and control information for
25 row axes and column axes respectively.

1 Q. And to be clear, then, the Rambus
2 direct DRAM memory devices do not have dedicated
3 address lines for address signals in the way
4 that a JEDEC-style memory system would have;
5 correct?

6 A. That's correct. The -- on the
7 RQ0 to RQ4 and RQ5 through RQ7, there are
8 packets of command -- command packets, which
9 include command op codes and addresses for the
10 corresponding row and column axes.

11 Q. The Rambus direct DRAM memory
12 devices do not have dedicated control lines for
13 control signals in contrast, for example, for
14 the JEDEC-style memory system?

15 A. The lines -- the traces on the
16 channel are -- carry both control and address on
17 each of them.

18 Q. So, for example, the DDR memory
19 device would have a pin dedicated to a row
20 address strobe signal while a Rambus direct DRAM
21 does not; correct?

22 A. You have to be careful, because
23 for the JEDEC standardized, SDRAMs of all
24 varieties, we have signal names that are
25 archaic, persisting in the definition of the

1 memory device. So when you refer to a row
2 address signal, that is the name of one signal
3 in the command bus. And it by itself doesn't
4 signify anything in particular; just like RQ7
5 doesn't signify anything in particular by
6 itself, the same idea applies to the JEDEC
7 standardized memory devices as well.

8 Q. And just to be clear, I think you
9 said "row address signal," and I think my
10 question was --

11 A. I misspoke. Row address -- the
12 RAS signal, row address, which is a -- it's not
13 called that anymore, but its history is that it
14 came from a row address strobe signal that had
15 that name. It got, over the decades, turned
16 into an acronym, RAS; and that name, RAS,
17 persists even though it's one bit of a command.

18 So I apologize if I misspoke with
19 the first answer.

20 Q. All right. So to be clear, a DDR
21 memory device has a pin dedicated to a RAS
22 signal and has a pin dedicated to a CAS signal;
23 whereas, a Rambus direct DRAM does not; is that
24 fair?

25 A. That is fair.

1 Q. Could you pull up Exhibit 1064
2 which is the JESD79-2 standard for DDR2 SDRAMs
3 that we've discussed a little bit, and let me
4 know when you have it in front of you.

5 A. I'm sorry. I missed the exhibit
6 number, please.

7 Q. 1064.

8 A. 1064. There it is.

9 Q. This is the JESD79-2 standard for
10 DDR2 SDRAMs, dated September 2003.

11 Do you have it in front of you?

12 A. I do.

13 Q. On page 6 of Exhibit 1064 is a
14 table under the heading "Package Pinout &
15 Addressing, Input/Output Functional
16 Description."

17 Correct?

18 A. Yes.

19 Q. And starting with the first line
20 on page 6 of Exhibit 1064, CK and CK-bar are
21 differential clock inputs for DDR2 memory
22 devices; correct?

23 A. Yes.

24 Q. With DDR2 memory devices, all
25 address and control input signals are sampled on

1 the crossing of CK and CK-bar; correct?

2 A. That's what it says, yes.

3 Q. And a person of ordinary skill in
4 the art would know and understand that; correct?

5 A. Yes.

6 Q. More generally, as I think we've
7 discussed, but just to be clear, would it be
8 fair to say that a person of ordinary skill in
9 the art would know and understand what's on
10 page 6 of Exhibit 1064 in this table that
11 provides the input/output functional description
12 for DDR2 memory devices?

13 ATTORNEY WARRICK: Objection;
14 form.

15 THE WITNESS: So this describes
16 all the pins; it doesn't really describe the
17 full functional description of the memory
18 device. But that aside, the textual
19 explanations would be clear to a POSITA of the
20 2004-2005 time frame, and they would have no
21 difficulty in understanding what each of these
22 signals of the SDRAM are for.

23 BY ATTORNEY CHANDLER:

24 Q. A couple of lines down on page 6
25 of Exhibit 1064 is a row for the chip-select

1 input, abbreviated CS; correct?

2 A. Yes, I see that.

3 Q. And for DDR2 memory devices, the
4 chip-select input provides for external rank
5 selection on systems with multiple ranks;
6 correct?

7 A. That's what it says.

8 Q. And for DDR2 memory systems, the
9 chip-select input is considered part of the
10 command code; correct?

11 A. Yes, that's what it says.

12 Q. A little bit further below that
13 on page 6 of Exhibit 1064 are other command
14 inputs called RAS, CAS and WE, which along with
15 the chip-select, define the command being
16 entered into the DDR2 memory device when the
17 clock signals cross; is that fair?

18 A. We wouldn't wall it "WE." We'd
19 call it "write enable." But sure. Go ahead.

20 Q. So is it correct that as shown on
21 page 6 of Exhibit 1064, the other command inputs
22 called RAS, CAS and write enable, along with the
23 chip-select, define the command being entered
24 into the DDR2 memory devices when the clock
25 cycles cross?

1 A. Yes, that's generally true.

2 Q. And RAS, I think you said
3 earlier, stands for row address strobe, at least
4 historically; is that correct?

5 A. Historically. Presently, it
6 doesn't anymore; it's just called RAS and CAS
7 and write enable.

8 But as it says here, they are all
9 part of a command bus; and their historical
10 meaning of row address strobe and column address
11 strobe and write enable have been lost to
12 antiquity.

13 Q. Now, page 6 of Exhibit 1064 lists
14 a number of other signals received by a DDR2
15 memory device that do not define the command;
16 correct?

17 A. Yes, that's correct.

18 Q. For example, a DDR2 memory device
19 receives an ODT signals, which stands for on-die
20 termination, but that signal is not used to
21 define the command; correct?

22 A. That's correct. It does not
23 contribute to the definition of the command; but
24 it is a command signal -- it is a control
25 signal; it's not a data signal.

1 Q. DDR2 memory devices also receive
2 the DM signal which stands for data mask. And
3 that's another example of a signal that's not
4 used to define the command; correct?

5 A. Yes.

6 Q. DDR2 memory devices receive DQ
7 data signals and DQS strobe signals, but those
8 signals are not used to define the command;
9 correct?

10 A. Yes, that's correct.

11 Q. In the middle of page 6 of
12 Exhibit 1064, there's a row for bank address
13 inputs, labeled BA0 to BA2; correct?

14 A. Correct.

15 Q. The BA0 to BA2 pins can receive
16 bank address signals defining which bank inside
17 of a DDR2 memory device that a read or write
18 command applies to.

19 Is that fair?

20 A. It's not precisely how it's
21 worded but, yes, it's accurate.

22 Q. And then for mode register set
23 commands, the same BA0 to BA2 pins can also
24 carry information determining which of the mode
25 registers inside the DDR2 memory device are

1 accessed.

2 Is that fair?

3 A. Accessed as in being written;
4 yes.

5 Q. And then a little further down on
6 page 6 of Exhibit 1064, there are individual
7 address inputs, A0 to A15, for the DDR2 memory
8 device; and those address inputs, A to 015, are
9 separate from the BA0 to BA2 bank address
10 inputs; correct?

11 A. Correct. And the address bits
12 convey data that's going into the mode
13 registers; and they also convey some control
14 information, such as the precharge bit.

15 Q. So you're referring to the line
16 that's labeled A10 and in certain circumstances,
17 carry a precharge command for DDR2 memory
18 devices; correct?

19 A. It's more of a precharge modifier
20 to a read or write command as opposed to a
21 command in its own right. So it's a nuanced
22 difference. Perhaps a difference without a
23 distinction -- I don't know -- or the vice
24 versa.

25 Q. And the address inputs A0 to A15

1 can carry either row address or column address
2 for the DDR2 memory devices, depending on the
3 type of command.

4 Is that fair?

5 A. Yes. And elsewhere there is a
6 command truth table that specifies exactly for
7 each memory type -- for each size and width of
8 memory, which pins are carrying which piece of
9 information for row axes and column axes.

10 Q. The next row down on page 6 of
11 Exhibit 1064 shows that for DDR2 memory devices,
12 there are also data input/output lines labeled
13 DQ, which are separate from the address and
14 control lines; correct?

15 A. Yes, they are separate.

16 Q. And the next row down on page 6
17 of Exhibit 1064 shows that DDR2 memory devices
18 also have DQS strobe lines; correct?

19 A. Yes, they do.

20 Q. Now, we talked a little bit
21 earlier about single data rate SDRAMs, and those
22 older single data rate SDRAMs do not have DQS
23 strobe signals; correct?

24 A. That's correct. That's a very
25 important addition between SDR and DDR -- SDRAM.

1 Q. And the purpose of the DQS strobe
2 signal for DDR2 memory devices is to indicate to
3 the recipients that the data signal is present
4 and valid. Is that fair?

5 A. Where are you getting the invalid
6 part?

7 Q. From our friend, Professor Jacob,
8 Exhibit 1069, page 2, note 2.

9 A. Okay. So, again, a pedagogical
10 simplification. The DQS indicates when to try
11 and capture the data. It doesn't guarantee that
12 the data is, in fact, valid and have sufficient
13 signal integrity to be captured.

14 If everything is designed
15 properly, the two are synonymous; but it is the
16 definition of the DQS signal that now is when
17 you should try to capture it. Or that's at
18 least the case for write data for the DRAMs, for
19 the phase of the signal is different for read
20 data.

21 Q. The DQS strobe signal travels
22 from the source to the destination along with
23 the data signal; correct?

24 A. Yes. And there are rules about
25 how different those trace lengths can be.

1 Q. The DQS strobe signal for DDR2
2 memory devices has a preamble; correct?

3 A. If we want to pull up one of the
4 timing diagrams, we could talk more precisely
5 about the relative location of edges on DQS
6 relative to data.

7 Q. Sure. How about if you look at
8 page 60 of Exhibit 10 -- I'm sorry. Not
9 page 60 -- page 26 of Exhibit 1064.

10 A. "Data Output (Read) Timing."
11 So that these are signals being
12 output by the SDRAM, the DDR SDRAM in this
13 cease, DDR2 SDRAM in this case. Sorry.

14 Q. So a person of ordinary skill in
15 the art would understand that DQS strobe signals
16 have a preamble; correct?

17 A. Yes, and the different versions
18 of the JEDEC standards define the preamble
19 differently.

20 Q. The preamble for the DQS strobe
21 signal is transmitted before the actual data
22 signals; correct?

23 A. Again, it depends on whether
24 you're talking about reads or writes and whether
25 the recipient is the memory controller or the

1 DRAM. But that is, again, a statement that is
2 probably pedagogically accurate, if not
3 precisely accurate in every respect.

4 Q. To be clear, the word "preamble"
5 is referring to the beginning.

6 Is that fair?

7 A. Yes, and the start of the
8 preamble is always before the start of the first
9 data, regardless of whether it's read data or
10 write data. But it's not always all the way
11 before.

12 Q. The preamble for the DQS strobe
13 signal lasts approximately one full clock cycle,
14 according to DDR2 standard.

15 Is that fair?

16 A. We would have to look at the
17 specification for TRPRE, which is the specified
18 time for the preamble from its formal start to
19 the first rise in transition of DQS; but this
20 figure would indicate that it's approximately
21 one full cycle. It could be slightly less or
22 slightly more, depending on how the TRPRE is
23 defined.

24 Q. And if you search for TRPRE, you
25 will see on page 65 of Exhibit 1064 that the

1 preamble for the DQS strobe signal for a read is
2 specified to be between 0.9 and 1.1 clock
3 cycles; correct?

4 A. Exactly. So it could be slightly
5 less; it could be slightly more.

6 Q. And during the length of the
7 preamble of the DQS strobe signal, which, as
8 just discussed, will be approximately one full
9 clock cycle, the DQS signal is driven low while
10 the DQS-bar signal is driven high; correct?

11 A. In Figure 23, based on read
12 data -- in other words, data coming out of the
13 DRAMs -- the DRAM drives DQS low and DQS-bar
14 high for the bulk of the preamble period.

15 Q. And would that also be true in
16 the right direction, that you have a preamble of
17 the DQS strobe signal that's approximately one
18 clock cycle long where the DQS signal is low and
19 the DQS-bar signal is high?

20 A. If you look at Figure 29 of that
21 DDR2 JEDEC standard, you see that the DQS
22 signals are defined differently for write data
23 than for read data.

24 Q. But is it still the case that for
25 write data, there's a preamble to the DQS strobe

1 signal where the DQS signal is driven low and
2 the DQS-bar signal is driven high?

3 A. What Figure 29 is depicting is
4 that in order for the DRAM to be guaranteed to
5 capture the data, the DQS signal has to be
6 stable in its preamble state for a given period
7 of time prior to the first rising edge of DQS
8 and the first falling edge of DQS-bar.

9 Q. And so, for example, in Figure 30
10 of the DDR2 standard on page 30 of Exhibit 1064,
11 we see a preamble for the DQS strobe signal
12 where DQS is low for approximately one clock
13 cycle, while DQS-bar is high for approximately
14 one clock cycle before the first piece of write
15 data.

16 Is that a fair description of
17 what's shown in Figure 30?

18 A. That's shown in Figure 30. If we
19 look at page 65 again, we see that the write
20 preamble is necessarily more than one-quarter
21 clock cycle. It can be any amount of time
22 longer than that.

23 Q. So for both a read command and a
24 write command in the -- to a DDR2 or from a
25 DDR2, memory system that will be a DQS strobe

1 signal with a preamble of a certain length where
2 the DQS signal is low and the DQS-bar signal is
3 high; is that fair?

4 ATTORNEY WARRICK: Objection;
5 form.

6 THE WITNESS: Yes; otherwise,
7 it's not guaranteed that the DRAM for write data
8 will be able to capture the -- the data
9 properly. And for read data, it's saying that
10 the DRAM will provide enough of a preamble that
11 will allow the memory controller to find the
12 center of the data eye.

13 BY ATTORNEY CHANDLER:

14 Q. Please turn to page 12 of
15 Exhibit 1064. Let me know when you're there.

16 A. I'm on page 12.

17 Q. As shown on page 12 of
18 Exhibit 1064, DDR2 memory devices include
19 registers, one of which is called the mode
20 register; correct?

21 A. I think that -- yes, it refers to
22 this particular register as the mode register;
23 and the other one is called the extended mode
24 register.

25 So the term "mode register"

1 refers specifically to this register, even
2 though both registers are, in fact, mode
3 registers.

4 Q. The mode register of the DDR2
5 memory device is normally programmed during
6 initialization; and the programmed values can
7 then be used during normal operation.

8 Is that fair?

9 A. It's stronger than that. It's
10 required to be set during initialization.

11 Q. The values for the mode register
12 are carried by the address lines going to the
13 DDR2 memory device; correct? During the
14 initialization process.

15 A. When --

16 ATTORNEY WARRICK: Objection;
17 form.

18 THE WITNESS: When the command
19 bus indicates a mode register set command, the
20 bank address bits show which mode register of
21 the two is being programmed, per the box in the
22 lower left corner of figure on page 12; and the
23 other contents of the fields of the mode
24 register are provided on address A0 through A12
25 is the last one that's useful. The rest are

1 reserved for future use.

2 BY ATTORNEY CHANDLER:

3 Q. For example, CAS latency can be
4 programmed in the mode register of a DDR2 memory
5 device during initialization; correct?

6 A. The CAS latency has to be
7 programmed during the initialization phase of --
8 it's getting the memory system and the SDRAMs
9 functional and operational.

10 Q. And how would you explain what
11 CAS latency is?

12 A. It is defined within the four
13 corners of the standard.

14 Q. And can you explain that a little
15 more.

16 A. There are figures and tables that
17 show what the CAS latency is relative to
18 commands and data for -- and its applicability
19 for reads and writes. And then -- yeah.

20 Q. On page 12 of Exhibit 1064,
21 there's a table on the right that's labeled "CAS
22 Latency." And there are different rows; and the
23 column labeled "Latency" says "2(Optional), and
24 then there's a row for 3, a row for 4 and a row
25 for 5; correct?

1 A. That's what the table says, yes.

2 Q. And in the context of CAS
3 latency, does the 2, 3, 4 and 5, refer to clock
4 cycles?

5 A. Yes. In DDR2, the latency is
6 measured in clock cycles. But we can refer to
7 the timing diagrams, to be clear about that.

8 Q. And so, for example, on page 24
9 of Exhibit 1064, there's a timing diagram that
10 gives an example of CAS latency and additive
11 latency and how they relate to read latency as
12 well as write latency; is that fair?

13 A. Yes. To be specific, AL refers
14 to additive latency; CL refers to CAS latency;
15 RL refers to the total read latency; and WL
16 refers to the write latency -- all from within
17 that figure.

18 Q. And in the text above that
19 figure, the -- on page 24 of Exhibit 1064, the
20 DDR2 standard specifies that the read latency is
21 defined as additive latency plus CAS latency;
22 correct?

23 A. The exact language there is that
24 the read latency is controlled by the sum of AL
25 and CL. So it's a nuance.

1 Q. I'm looking at the language three
2 lines up: Read latency is defined as the sum of
3 additive latency because CAS latency -- and it
4 has a little equation, "RL=AL+CL"; correct?

5 A. Oh, I see, down towards the
6 bottom of that paragraph. Let me read that.

7 Yes, that's what it says there
8 on that last three lines of that paragraph.

9 Q. And then write latency,
10 abbreviated WL, is defined as read latency minus
11 1; correct?

12 A. Yes. For DDR2 SDRAMs, that is
13 how it's defined. All SDRAM -- all DDR2 SDRAMs
14 expect write data then and will deliver read
15 data correspondingly.

16 Q. On page 14 of Exhibit 1064, we
17 can see that DDR2 memory devices also include
18 another register called the extended mode
19 register; correct?

20 A. Yes, they do.

21 Q. And the extended mode register in
22 DDR2 memory device is used to specify the value
23 for the additive latency; correct?

24 A. That is one of the things that is
25 set via the extended mode register, yes.

1 Q. And the additive latency can be 0
2 clock cycles, or 1, 2, 3 or 4 clock cycles;
3 correct?

4 A. That is what the table on page 14
5 specifies.

6 Q. And so under the DDR2 standard,
7 it's possible to set the additive latency to be
8 0, in which case the CAS latency is what would
9 impact the read latency and the write latency;
10 correct?

11 A. Well, the CAS latency, as
12 specified in the mode register, always impacts
13 the read latency and the write latency. If you
14 happen to set the additive latency to 0, the CAS
15 latency is the only thing that's determining
16 what the read latency and the write latency are.

17 (Exhibit Number 1005 was previously
18 marked for identification.)

19 BY ATTORNEY CHANDLER:

20 Q. Could you pull up Exhibit 1005.
21 And, again, I'm not sure if we talked about it
22 before, so I'll just put it in the chat for ease
23 of reference.

24 A. It's not up, so I presume we have
25 not looked at it yet.

1 Q. Yeah. Let me know when you have
2 it on the screen. It's the '087 provisional.

3 A. I have that provisional up.

4 Q. All right. Have you reviewed
5 Exhibit 1005, the provisional application
6 60/645087, which has been referred to as the
7 '087 provisional?

8 A. Yes, I have.

9 Q. The '087 provisional, marked as
10 Exhibit 1005, is the only provisional
11 application that you formed an opinion about
12 with respect to whether it provides support for
13 the claims of the '417 and '215 patents;
14 correct?

15 ATTORNEY WARRICK: Objection;
16 form.

17 THE WITNESS: My task was to
18 rebut the arguments relative to the '087
19 provisional that were in the petition and
20 declaration, and I did that. It was not
21 necessary for me to do anything more vis-a-vis
22 rebutting those arguments.

23 BY ATTORNEY CHANDLER:

24 Q. In your expert declaration marked
25 as Exhibit 2024, in Footnote 2, paragraph 81 of

1 the '417 IPR and the paragraph 34 84 the '215
2 IPR, you state that you were asked only to
3 render an opinion on Petitioner's arguments
4 regarding the '087 provisional; correct?

5 A. What page are you on again,
6 please?

7 Q. It's paragraph 81.

8 A. Paragraph 81. All right.

9 Q. And then --

10 A. And there's the Footnote 2. Yes,
11 I see Footnote 2.

12 Q. So to be clear, it's only the
13 '087 provisional marked as Exhibit 1005 that you
14 provide any opinions about with respect to
15 whether any of the provisionals provide support
16 for the claim for the '417 and '215 patents;
17 correct?

18 ATTORNEY WARRICK: Objection;
19 form.

20 THE WITNESS: Turning to
21 paragraph 92 of my declaration that's for the
22 '417, I say that:

23 "I understand that Petitioner
24 has not identified any other
25 limitations of the '417 patent

1 allegedly not supported by the '087
2 provisional. I take that to mean
3 that Dr. Wolfe and Petitioner
4 concede that the '087 provisional
5 provides support for the other
6 limitations.

7 "Nevertheless, for
8 completeness, I following the follow
9 exemplary citations in the following
10 claim chart for the remaining
11 limitations and -- when viewed
12 through the eyes of a POSITA and the
13 knowledge of the state of the art,
14 including translation JEDEC
15 standards -- indicate that the
16 inventors had possession of the
17 claimed subject matter."

18 And in that following table, I do
19 refer to other citations other than
20 Exhibit 1005. I would have to go back and see
21 which of those are provisional applications and
22 which of those are other documents that a POSITA
23 would have access to.

24 BY ATTORNEY CHANDLER:

25 Q. So I guess I'm a little confused

1 by your Footnote 2 as well as the table that you
2 just cited where you cite to things other than
3 Exhibit 1005.

4 So is it your opinion that there
5 are other provisionals other than Exhibit 1005
6 that provide support for all the claims of the
7 '417 and '215 patents?

8 ATTORNEY WARRICK: Objection;
9 form.

10 THE WITNESS: I would have to
11 review those provisionals to identify the
12 support that you're suggesting.

13 BY ATTORNEY CHANDLER:

14 Q. And to be clear, I'm not
15 suggesting. I'm trying to ask you if you're
16 trying to offer an opinion that there's more
17 than just Exhibit 1005 that provides support for
18 all of the claims of the '417 and '215 patents.

19 So what are your opinions? Are
20 they that it's only Exhibit 1005 that you're
21 relying on to provide support? Or are you
22 trying to say that it's Exhibit 1005 plus other
23 provisionals? Or are you trying to say that
24 there are other provisionals besides
25 Exhibit 1005 that provide support for the claims

1 of the '417 and '215 patents?

2 ATTORNEY WARRICK: Objection;
3 form.

4 THE WITNESS: So what I'm saying
5 in that footnote and in that section of the
6 declaration is that, by looking at the '087
7 provisional by itself, I've rebutted all of the
8 arguments presented in the petition and
9 Dr. Wolfe's declaration vis-a-vis the '087 not
10 providing support; and I'm saying that it does
11 supply adequate support for all of those
12 arguments that were presented in the petition.

13 I'm also providing additional
14 support for the various claim elements in other
15 references, but those are not necessary in order
16 to rebut the arguments in the petition.

17 BY ATTORNEY CHANDLER:

18 Q. I understand the point you're
19 providing about the '087 provisional and that,
20 in your opinion, Exhibit 1005 is sufficient to
21 provide support for all the claims. And I'll
22 ask questions about that in a little bit.

23 But I'm still a little confused
24 by your statement that you're providing
25 additional support for various claim elements

1 and other references.

2 Are you suggesting that those
3 other references are sufficient to support the
4 claims? Or are you just pointing to other
5 examples and other references where, you know,
6 certain elements may be present but not
7 necessarily support for the entire claim
8 language?

9 ATTORNEY WARRICK: Objection;
10 form.

11 THE WITNESS: So, again, what I
12 am saying is that the '087 by itself rebuts the
13 arguments in the petition and that if that's
14 inadequate for the board to find support for all
15 of the claim elements, I'm providing this
16 additional support across multiple references
17 to -- that might help them come to a conclusion
18 that the inventors had full support for the
19 claims, as drafted.

20 BY ATTORNEY CHANDLER:

21 Q. And all of what you just
22 described is in the table which -- on
23 Exhibit 2024 of IPR 2023-00454, runs from pages
24 62 through 64; and in IPR2023-00455, runs from
25 pages 58 through 61; correct?

1 A. Correct. Those are the pages on
2 which those tables exist.

3 Q. And there's nothing besides those
4 tables that you're pointing to with respect to
5 this notion of additional support in other
6 references that might help the board come to the
7 conclusion that the inventors had full support
8 of the claims; is that fair?

9 A. Correct. I mean, the bulk of the
10 section is specifically rebutting the arguments
11 in the petition, and that is done solely with
12 the '087 provisional. And the table is
13 additional support, generally speaking.

14 Q. Turning back to Exhibit 1005, the
15 '087 provisional, that provisional has only one
16 figure shown on page 10 of the Exhibit 1005;
17 correct?

18 A. Yes. There's only one figure
19 labeled "Block Diagram: Blank Buffered DIMM
20 Memory Sub-system."

21 Q. The figure in the '087
22 provisional on page 10 of Exhibit 1005 is a
23 block diagram in which a block of rank buffered
24 DIMM logic, abbreviated RBDL, is shown in the
25 middle of the figure; correct?

1 A. Yes, it's generally in the middle
2 of the figure.

3 Q. The figure in the '087
4 provisional on page 10 of Exhibit 1005 shows
5 that the block of rank buffered DIMM logic only
6 receives from the memory controller on the left
7 data signals DQ0 through DQ63, data strobe
8 signals DQS0 through DQS7; a chip-select signal
9 cs#; and address and control signals identified
10 as ad & ctl; correct?

11 ATTORNEY WARRICK: Objection;
12 form.

13 THE WITNESS: Yeah, I'm not sure
14 the cs signal is necessarily viewed by the
15 POSITA as a single signal or a bus of signals.
16 But that -- other than that quibble, your
17 recitation of the names attached to the lines
18 and buses is accurate.

19 BY ATTORNEY CHANDLER:

20 Q. And then the figure in the '087
21 provisional on page 10 of Exhibit 1005 shows on
22 the right side two ranks of memory, each of
23 which receive a similar set of signals from the
24 block of rank buffered DIMM logic; correct?

25 ATTORNEY WARRICK: Objection;

1 form.

2 THE WITNESS: The names are
3 different with regard to rcs0# and rcs1#; but
4 they are, in fact, similar.

5 BY ATTORNEY CHANDLER:

6 Q. The figure in the '087
7 provisional on page 10 of Exhibit 1005 does not
8 show any of the internal structure of the block
9 of rank buffered DIMM logic; correct?

10 A. The figure does not, but the text
11 does speak to some of its internal structure.

12 Q. Paragraph 5 of the '087
13 provisional marked as Exhibit 1005 refers to a
14 multiplexer/demultiplexer; correct?

15 A. Yes, it does.

16 Q. But that paragraph does not
17 mention any control signals for that
18 multiplexer/demultiplexer; correct?

19 A. It doesn't mention control
20 signals for the multiplexer/demultiplexer, but
21 that doesn't mean those signals are not inherent
22 in -- in that any multiplexer/demultiplexer
23 needs to have control signals to determine its
24 behavior.

25 Q. Paragraph 8 of the '087

1 provisional, marked as Exhibit 1005, also refers
2 to a multiplexer/demultiplexer; correct?

3 A. There it's specifically called
4 the data path multiplexer/demultiplexer, as it
5 is in paragraph 5 also, by the way. So it's the
6 same thing. And it's a
7 multiplexer/demultiplexer in the data path
8 between the memory controller and the ranks on
9 the module.

10 Q. But that paragraph also does not
11 mention any control signals for the
12 multiplexer/demultiplexer; correct?

13 A. Again, it doesn't have to because
14 any multiplexer/demultiplexer necessarily has to
15 have control signals in order to have its
16 behavior determined.

17 Q. Paragraph 17 of the '087
18 provisional marked as Exhibit 1005 also refers
19 to a multiplexer/demultiplexer; correct?

20 A. Where in that paragraph?

21 Oh, there it is, yes.

22 Here it's the
23 multiplexer/demultiplexer, presumably referring
24 back to the same data path,
25 multiplexer/demultiplexer of the previous

1 paragraphs, yes.

2 Q. And, again, that paragraph does
3 not mention any control signals for the
4 multiplexer/demultiplexer; correct?

5 A. And, again, it doesn't need to,
6 because any multiplexer/demultiplexer
7 necessarily has to have control signals in order
8 to determine its behavior in real time.

9 Q. In the '087 provisional marked as
10 Exhibit 1005, neither paragraph 5 nor 8 nor 17
11 tell you which control signals or any other
12 signals to use as inputs to the
13 multiplexer/demultiplexer -- the control
14 multiplexer/demultiplexer; correct?

15 ATTORNEY WARRICK: Objection to
16 form.

17 (Interruption by the court reporter to
18 clarify the record.)

19 BY ATTORNEY CHANDLER:

20 Q. In the '087 provisional marked as
21 Exhibit 1005, neither paragraph 5 nor 8 nor 17
22 tell you which control signals or other signals
23 to use as inputs to the
24 multiplexer/demultiplexer to control the
25 multiplexer/demultiplexer; correct?

1 ATTORNEY WARRICK: Objection;
2 form.

3 THE WITNESS: So I cover this in
4 detail in paragraph 82 of my declaration, where
5 I list all of the implications of the figure and
6 those paragraphs in the provisional '087 and
7 what a POSITA of our time period would
8 understand from that disclosure.

9 And, in particular, in the --
10 reading from Item 5 of that list in that
11 paragraph, the claimed circuitry is at least
12 part of said multiplexer/demultiplexer, which a
13 POSITA would understand necessarily would
14 receive control signals from the command decode
15 circuitry and would understand necessarily that
16 the module described in the '087 provisional
17 would receive commands from the external memory
18 controller and would decode that -- and would
19 include command decode circuitry to interpret
20 those commands and so forth.

21 In particular, I will note in
22 addition that a POSITA reading the phrase "data
23 path multiplexer/demultiplexer" would understand
24 what a multiplexer/demultiplexer is and that
25 they would necessarily be control signals that

1 determine which path is being selected and which
2 direction the multiplexer/demultiplexer is
3 sending data. So in total, it's clear that the
4 data buffer control signals are supported by the
5 '087 provisional.

6 ATTORNEY CHANDLER: Could we go
7 off the record? But don't run away because I
8 want to talk about tomorrow.

9 THE VIDEOGRAPHER: Off the record
10 at 4:43 p.m. Pacific Time.

11 (Recess taken from 4:43 p.m. to
12 4:48 p.m.)

13 THE VIDEOGRAPHER: On the record
14 at 4:48 p.m. Pacific Time.

15 ATTORNEY CHANDLER: Dr.
16 Przybylski, as discussed, let's reconvene
17 tomorrow at 7:00 a.m. Pacific, 10:00 a.m.
18 Eastern, for the continuation of my questioning
19 of you in both IPRs. And as a reminder, under
20 the PTAB rules, you're not permitted to discuss
21 the substance of anything with your counsel
22 overnight.

23 THE WITNESS: I understand.

24 THE VIDEOGRAPHER: Counsel, would
25 you like us to conclude the video deposition at

1 this point?

2 ATTORNEY CHANDLER: I'd like to
3 recess until tomorrow morning.

4 THE COURT REPORTER: While we're
5 still on the record, do you both want rough
6 drafts tonight?

7 ATTORNEY CHANDLER: Sure, I'll
8 take a rough draft. And just so you have it, I
9 would like the final drafts one week later from
10 today, so Thursday, February 22nd.

11 THE COURT REPORTER: Okay.
12 Mr. Warrick?

13 THE VIDEOGRAPHER: Counsel, does
14 anyone need a copy of the video?

15 ATTORNEY CHANDLER: Phil, go
16 ahead.

17 ATTORNEY WARRICK: I do not need
18 the video. The rough would be great. And I
19 guess I don't know -- what's the normal
20 turnaround on the final transcript?

21 THE COURT REPORTER: Two weeks.
22 It's usually two weeks from today.

23 ATTORNEY WARRICK: That's fine.

24 THE VIDEOGRAPHER: All right.

25 This concludes Volume 1 of the deposition of

1 Steven Przybylski. We're off the video record
2 at 4:49 p.m. Pacific Time on February 15, 2024.
3 (Whereupon, at 4:49 p.m. the
4 proceedings adjourned.)
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INSTRUCTIONS TO DEPONENT

After reading this volume of
your deposition, indicate any corrections or
changes to your testimony and the reasons
therefor on the Errata Sheet supplied to you
and sign it. DO NOT make marks or notations on
the transcript volume itself.

E R R A T A

I wish to make the following
changes, for the following reasons:

Page Line

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C E R T I F I C A T I O N

I hereby certify that I have
read the foregoing transcript of my deposition
testimony, and that my answers to the questions
propounded, with the attached corrections or
changes, if any, are true and correct.

STEVEN PRZYBYLSKI, PH.D.

CERTIFICATE OF SHORTHAND REPORTER

I, Gail Inghram Verbano,
Registered Diplomate Reporter, Certified
Realtime Reporter, Certified Shorthand Reporter
(CA) and Notary Public, the officer before whom
the foregoing proceedings were taken, do hereby
certify that the foregoing transcript is a true
and correct record of the proceedings; that
said proceedings were taken by me
stenographically and thereafter reduced to
typewriting under my supervision; and that I am
neither counsel for, related to, nor employed
by any of the parties to this case and have no
interest, financial or otherwise, in its
outcome.


Gail Inghram Verbano, CSR, RDR, CRR
CA-CSR No. 8635

1 UNITED STATES PATENT AND TRADEMARK OFFICE

2
3 BEFORE THE PATENT TRIAL AND APPEAL BOARD

4
5 SAMSUNG ELECTRONICS CO., LTD.

6 Petitioner,

7 v.

8 NETLIST, INC.,

9 Patent Owner

10
11 IPR2023-00455

12 Patent 9,858,215

13
14 IPR2023-201428
15 Patent 8,787,060

16 IPR2023-00454
17 Patent 11,093,417

18 Remote video-recorded deposition of

19 STEVEN PRZYBYLSKI, PH.D.

20 Volume 2

21
22
23 REPORTED BY:

24 Gail L. Inghram Verbano:

25 Registered Diplomate Reporter,

Certified Realtime Reporter,

Certified Shorthand Reporter-CA (No. 8635)

1
2 UNITED STATES PATENT AND TRADEMARK OFFICE

3
4 BEFORE THE PATENT TRIAL AND APPEAL BOARD

5
6 SAMSUNG ELECTRONICS CO., LTD.

7 Petitioner,

8 v.

9 NETLIST, INC.,

10 Patent Owner

11
12
13
14
15 WHEREUPON, the remote
16 video-recorded deposition of STEVEN PRZYBYLSKI,
17 Ph.D., Volume 2, was held via Zoom
18 videoconferencing on Friday, February 16,
19 2024, beginning at approximately 6:59 a.m.
20 Pacific Time, the proceedings being recorded
21 stenographically by Gail Inghram Verbano,
22 Registered Diplomate Reporter, Certified
23 Realtime Reporter, Certified Shorthand
24 Reporter-CA (No. 8635), and transcribed under
25 her direction.

A P P E A R A N C E S

A P P E A R A N C E S:

On behalf of Samsung:

THEODORE W. CHANDLER, ESQ.

ted.chandler@bakerbotts.com

FERENC PAZMANDI, ESQ.

ferenc.pazmandi@bakerbotts.com

BAKER BOTTS, LLP

101 California Street, Suite 3200

San Francisco, California 94111-5802

415.291.6259

On behalf of Netlist, Inc.:

PHILIP WARRICK, ESQ.

pwarrick@irell.com

IRELL & MANELLA, LLP

1800 Avenue of the Stars, Suite 900

Los Angeles, California 90067-4276

310.277.1010

ALSO PRESENT:

DANA BACHMAN, Legal Videographer

- - -
I N D E X
- - -

EXAMINATION OF:	PAGE
STEVEN PRZYBYLSKI, PH.D.,	
By Attorney Chandler	280
By Attorney Warrick	447
By Attorney Chandler	468

E X H I B I T S

NUMBER	PAGE
(Exhibits 1107 through 1112 not identified.)	
Exhibit 1113 U.S. Patent Number 7,002,378 re: IPR2022-01428 and IPR2022-01428 (9 pages)	292

PREVIOUSLY MARKED EXHIBITS REFERENCED:	PAGE
Paper 1	427
Exhibit 1012	484

DEPOSITION SUPPORT INDEX

QUESTIONS INSTRUCTED NOT TO ANSWER:

PAGE LINE

(None)

REQUEST FOR PRODUCTION OF DOCUMENTS

PAGE LINE

(None)

STIPULATIONS

PAGE LINE

(None)

QUESTIONS MARKED

PAGE LINE

(None)

REPORTER'S NOTE:

QUOTATION MARKS ARE USED FOR CLARITY AND DO NOT
NECESSARILY REFLECT A DIRECT QUOTE.

1 Friday, February 16, 2024; 6:59 a.m.

2 - - -

3
4 THE VIDEOGRAPHER: Good morning.

5 We're now on the record. It's 6:59 a.m. Pacific
6 Time on February 16th, 2024.

7 This begins the video conferenced
8 deposition of Steven Przybylski, Volume 2, taken
9 in the matter of Samsung Electronics Co., Ltd.
10 versus Netlist Incorporated, filed before the
11 Patent Trial and Appeal Board; Case Numbers
12 IPR2023-00454, and IPR2023-00455.

13 My name is Dana Bachman. I'm
14 your videographer today. Our court reporter is
15 Gail Verbano. We are both representing Esquire
16 Deposition Solutions.

17 Will everyone present please
18 identify themselves beginning with our witness,
19 Mr. Przybylski.

20 THE WITNESS: Steven Przybylski.

21 THE VIDEOGRAPHER: Thank you.
22 Counsel, please.

23 ATTORNEY CHANDLER: Good morning.
24 Theodore Chandler from Baker Botts on behalf of
25 the Petitioner Samsung Electronics Co., Ltd.,

1 and with me is my colleague, Dr. Ferenc
2 Pazmandi.

3 ATTORNEY WARRICK: Phillip
4 Warrick with Irell & Manella on behalf of patent
5 owner Netlist, Inc.

6 THE VIDEOGRAPHER: Thank you.
7 Madam Court Reporter, would you
8 please re-swear our witness.

9
10 WHEREUPON,

11 STEVEN PRZYBYLSKI, PH.D.,
12 being first duly resworn or reaffirmed to testify
13 to the truth, the whole truth, and nothing but
14 the truth, was examined and testified further as
15 follows:

16
17 EXAMINATION (Cont'd)
18 BY ATTORNEY CHANDLER:

19 Q. Dr. Przybylski, do you have any
20 clarifications or corrections to your previous
21 testimony so far?

22 A. I would like to add something to
23 our discussion at the end of yesterday with
24 regard to the chapter -- the overview chapter in
25 the Jacob textbook where we were looking at the

1 tables that compared direct Rambus and DDR SDRAM
2 on page 23 of Exhibit 1070, if I may.

3 Q. Okay.

4 A. At the time yesterday I was
5 skeptical of some of the numbers in that
6 comparison table, and I was incredulous, in
7 particular, about the 117-pin count per channel
8 for the direct Rambus in Table 0V.3.

9 It didn't look right, so I
10 checked some of the other references in the
11 record here. And, in particular, the article
12 Exhibit 2001, by Richard Crisp shows the -- what
13 the interface looks like on the memory
14 controller and says that the proper number there
15 is, I think, 65 or so -- I'm sorry -- 76 or
16 something. In the low 70s. We can pull that up
17 if you would like. It's up to you.

18 And so that number is wrong in
19 this table. There's no explanation as to how
20 the authors got to 117.

21 The operating frequency is also
22 at 600 megahertz, whereas the data sheets show
23 it going up to 800 megahertz.

24 So this -- this comparison is
25 not -- at least there's questions about it. And

1 I think I would beseech the board to be careful
2 with regard to using Jacob's work in comparisons
3 of the DDR JEDEC -- DRR SDRAM and JEDEC
4 standardized memory subsystems and the direct
5 Rambus. There's significant questions there
6 between the -- what -- the analysis that he
7 does. That's all.

8 Q. Do you agree that DDR SDRAM, at a
9 given operating frequency, could have a peak
10 bandwidth greater than the peak bandwidth for
11 Rambus memory?

12 A. I think that in this table, the
13 peak bandwidth of the direct Rambus is listed
14 based on a 600 megahertz operating frequency.
15 And if the data sheets are to be believed, then
16 the peak operating frequency is 800, not 600.
17 So that, in this case, the peak bandwidth of a
18 single channel of Rambus -- direct Rambus DRAM
19 would be greater than that -- what's shown as
20 the peak bandwidth.

21 Or the peak bandwidth would at
22 least be comparable, I think, probably -- 6 to
23 8 --

24 Yeah, it would be the same in the
25 two. But then if you normalize it on a per-pin

1 basis for the controller, the peak bandwidth for
2 the direct Rambus apples-to-apples comparison
3 would be another 50 percent higher than this.

4 So under that analysis, the peak
5 bandwidth of direct Rambus would be
6 substantially greater than that of a direct
7 SDRAM memory subsystem.

8 Q. The operating frequency of DDR
9 has continued to increase, right, such that it's
10 much faster than 200 megahertz today?

11 A. Well, the operating frequency of
12 DDR hasn't gone up. There are subsequent
13 generations of SDRAMs that operate at higher
14 frequency, but I don't know if JEDEC has changed
15 the specification of DDR SDRAM as cited in this
16 table to above the 200 megahertz operating
17 frequency listed here.

18 Q. But the way JEDEC works is that
19 by the 2004 to 2005 time frame, the DDR2
20 specification had been published and finalized,
21 and it provided for speeds that were much faster
22 than the prior generation of the specification
23 DDR -- sometimes referred to as DDR1; and
24 furthermore, the 2004-2005 time frame, JEDEC was
25 already thinking about and working on the next

1 generation of the standard DDR3, which would
2 have even faster speeds than DDR2, and even
3 faster or greater bandwidth; right?

4 Isn't that the way JEDEC was
5 working and continues to work today?

6 ATTORNEY WARRICK: Objection;
7 form.

8 THE WITNESS: Yes, JEDEC aims for
9 about a factor of two performance increase per
10 generation of standard, and then going up from
11 there.

12 But no one stands still; right?
13 The direct Rambus, as compared in this table
14 is -- had follow-ons, as we know with the XDR
15 and other high-performance memory sub systems.
16 Ultimately, the JEDEC way of doing things, from
17 a business perspective and a industry/community
18 perspective, won out, and we all now use JEDEC
19 standardized memories for essentially
20 everything.

21 And -- but my point is that this
22 particular table and the other analyses we've
23 seen from these authors does not appear to
24 appropriately capture the comparison as of -- as
25 it's portrayed in this table.

1 BY ATTORNEY CHANDLER:

2 Q. But my point is that, by
3 2004-2005, there was a recognition in the
4 industry that Rambus was not going to be some
5 revolutionary new technology that could leapfrog
6 the JEDEC DDR approach that, by 2004-2005, the
7 writing was on the wall that the JEDEC DDR
8 approach had won out and would continue to win
9 out because it was at least comparable in
10 performance to the Rambus approach and it had
11 all the advantages of cost and widespread
12 adoption. Isn't that fair?

13 ATTORNEY WARRICK: Objection;
14 form.

15 THE WITNESS: But I would say,
16 having lived through that period as a consultant
17 following the industry very closely, it was the
18 latter set of characteristics, the business side
19 of things, that were ultimately the reason why
20 we're not using Rambus DRAMs today for anything
21 of note, and that the DRAM manufacturers and
22 principal system vendors, you know, decided to
23 adopt and use the SDRAMs as being adequate for
24 the different applications even though, as shown
25 by this table, that the direct or -- at least

1 the revision of this table that was more
2 accurate -- but the direct RDRAM still had
3 superior performance over the DDR during the
4 time frame when that -- there was uncertainty
5 about which way the industry was going to go.

6 But you're absolutely correct
7 that the industry did select the JEDEC approach
8 and reject the Rambus approach.

9 BY ATTORNEY CHANDLER:

10 Q. And that was known by the
11 2004-2005 time frame?

12 A. Yeah. It was clear earlier than
13 that even that it was not going to become the
14 mainstream memory type for PCs and servers, at
15 least.

16 Q. Could you turn back to your
17 expert declarations marked as Exhibit 2024. And
18 the chat has been cleared out. I'm hoping you
19 still have everything on your screen, but if you
20 need anything from the chat, let me know, and I
21 can drop it in if that's more efficient.

22 A. So I walked away from my computer
23 last night and have returned to it, so all of
24 the PDFs that I opened are still open.

25 Q. Good. We'll pick up where we

1 left off.

2 So open -- turn to paragraph 88
3 of your first expert declaration, paragraph 91
4 of your second expert declaration, and those
5 paragraphs begin with the words:

6 "Therefore, at least some of
7 the time, there is no discernible
8 transition in the voltage on the DQS
9 signal at the start of the
10 preamble."

11 Do you see that?

12 A. I do.

13 Q. So in your opinion, for at least
14 some of the time there's no discernible
15 transition in the voltage on the DQS signal at
16 the start of the preamble; correct?

17 A. Yes. The start of the preamble
18 is not discernible by the receiver of the DQS
19 and the DQ signals, and so it's not a reliable
20 indicator of anything. It's just shown in the
21 standard to specify the minimum length of the
22 preamble that's a requirement to ensure that the
23 rising edge is captured -- is useable properly
24 by the receiver.

25 Q. There's a little ambiguity in my

1 mind as to what you're saying in the sentence
2 where you say there's "no discernible transition
3 at the start of the preamble."

4 The word "start" could be
5 referred to the very first moment in time where
6 the signal drops low; or the word "start" could
7 be referring to the first time period of the
8 preamble where the signal is low for a certain
9 amount of time.

10 What did you mean?

11 A. If we look at the JEDEC standard,
12 for reads and writes it specifies either a
13 minimum length or a bounds -- a minimum length
14 of a preamble on outbound DQS from the DRAM's
15 perspective or a requirement for an inbound DQS.
16 And by "start of the preamble," I was referring
17 to the standard specified minimum time.

18 So, for example, on inbound DQS
19 signals to the SDRAM, the formal start of the
20 preamble is somewhere between .9 and 1.1 clock
21 cycles ahead of the first transition on DQS. So
22 that would be what I refer to as the start of
23 the preamble, regardless of whether there's an
24 actual voltage transition there.

25 Q. I'm still a little unclear as to

1 what you're saying. And maybe it would help for
2 us to both look at a picture together.

3 So could you turn to the DDR2
4 standard, Exhibit 1064, and go to page 26, as an
5 example, and let me know you're there.

6 A. 1064, page what again, please?

7 Sorry.

8 Q. 26.

9 A. 26, thank you.

10 So this is the data outbound read
11 timing, and so it specifies the DRAM's behavior
12 on a read as a result of executing a read
13 command.

14 Q. On page 26 of Exhibit 1064 in
15 Figure 23 there's a preamble to the DQS strobe
16 signal; correct?

17 A. Yes. It does specify that the
18 DRAM will guarantee that DQS is low for between
19 .9 and 1.1 cycles ahead of the first rising edge
20 of DQS.

21 Q. And the recipient of the preamble
22 of the DQS strobe signal is able to discern that
23 what it is receiving is, in fact, the preamble;
24 correct?

25 A. No. That's not how it works.

1 Because the DQS could be low to
2 start with, before the first time period shown
3 here, there is nothing on that signal trace in
4 terms of a voltage change that would indicate to
5 the receiver that it is, in fact, in a preamble.

6 It's -- go ahead.

7 Q. To be clear, so you're not
8 relying solely on the lack of a discernible
9 transition from when the line is drawn in the
10 middle to where the line drops low; you're
11 saying that even when the line for the DQS
12 strobe signal is low for up to a full clock
13 cycle, that that is not discernible as a
14 preamble either; is that fair?

15 A. Yes. The purpose of the preamble
16 is to make sure that there is no false
17 transitions on DQS in advance of the first real
18 transition, and it's only the transitions that
19 signify the beginning of -- in the case of a
20 read transaction, the beginning of the first bit
21 period on the DQs.

22 It does -- if you don't have a
23 transition, there's nothing to detect in this
24 sense. There -- if -- if the voltage on the DQS
25 has been low for 15 clock cycles, it's not the

1 preamble of anything in particular, but the
2 receiver and the memory controller can't use the
3 fact that it's low to do anything. It's just
4 make the -- the specification is saying that it
5 has to be low for a clock cycle plus or minus
6 ahead of the first transition in order to make
7 sure that the first transition is clean.

8 Q. So in your opinion, a person of
9 ordinary skill in the art would not be trying to
10 detect the preamble itself? Is that sort of the
11 basis for your opinion in your declaration,
12 starting on paragraph 88 of the '417 IPR and
13 paragraph 91 of the '215 IPR?

14 ATTORNEY WARRICK: Objection;
15 form.

16 THE WITNESS: Much stronger than
17 that. It's not that he wouldn't try to; it's
18 that he can't. There's nothing to grab onto to
19 say "I'm in the preamble now."

20 Because this -- the signal is
21 unchanged, for example, for a long period of
22 time in advance of this actual transaction on
23 the DQ and DQS signals, and you're not in the
24 preamble for many, many cycles. The preamble is
25 defined as that last cycle in advance.

1 But you can't -- as the receiver,
2 you can't do anything as a result of being in,
3 quote, the preamble, unquote. The period of
4 time when the receiver -- when the transmitter,
5 the DRAM in this case, is actively driving it
6 low as opposed to it just happening to be low.
7 So that the -- the transition on DQS, which is
8 the actual point that we're interested in, that
9 that's clean and discernible.

10 (Whereupon, Exhibit Number 1113 in both
11 IPRs was marked for identification and
12 is attached hereto.)

13 BY ATTORNEY CHANDLER:

14 Q. I'd like to mark a new exhibit,
15 which will be 1113 in both IPRs. It's the same
16 document, the only difference being the stamp in
17 the bottom right with the case number.

18 I've dropped the exhibit into the
19 chat. Please go ahead and open up Exhibit 1113
20 and let me know when you have it in front of
21 you.

22 A. I'm looking at patent 7,002,378
23 to Srikanth.

24 Q. Yes. Exhibit 1113 is U.S. Patent
25 Number 7,002,378 to Srikanth at Intel, filed on

1 December 29th, 2000; correct?

2 A. The priority is -- yes. Item 22
3 on the front page says filed December 29th,
4 2000.

5 Q. And then just below that it says
6 that it was published on the 4th of July 2022;
7 correct?

8 A. Yes. Item 65 says, "Prior
9 publication date, U.S.," et cetera, "July 4th,
10 2002."

11 Q. And as shown in the title of this
12 patent, marked as Exhibit 1113, as well as the
13 abstract, this patent teaches a technique for
14 detecting a valid data strobe; correct?

15 A. That is the title of this patent,
16 yes.

17 Q. And then turn to Column 1 of the
18 patent marked as Exhibit 1113.

19 A. Yes, I'm at Column 1.

20 Q. The first sentence of this patent
21 marked as Exhibit 1113, Column 1, line 5 teaches
22 continuously monitoring a data strobe signal and
23 detecting when it indicates valid data is
24 available; correct?

25 ATTORNEY WARRICK: Objection;

1 form.

2 (Witness reviews document.)

3 THE WITNESS: You're talking
4 about the field?

5 BY ATTORNEY CHANDLER:

6 Q. Yes.

7 A. Column 1, lines 4 through 10;
8 right?

9 Q. Yes.

10 A. I don't see the word "available"
11 there.

12 "The present invention
13 relates to a valid data strobe
14 detection technique and to -- more
15 particularly to a technique for
16 continuously monitoring the data
17 strobe signal from a
18 double-data-rate synchronous DRAM,
19 for example, for validating the
20 strobe signal for subsequent use."

21 That's what it says.

22 Q. Turn to Column 3 of the patent
23 marked as Exhibit 1113 and go to the start
24 paragraph starting around line 47. Let me know
25 when you're there.

1 A. Line 47 starting, "A typical
2 strobe waveform."

3 Q. And you may want to just briefly
4 look at Figure 2, and let me know when you're
5 ready.

6 A. So I looked at Figure 2.

7 Q. So in Column 3 starting around
8 line 47 of Exhibit 1113, there's a discussion of
9 Figure 2 and a read preamble; correct?

10 A. Yes. It says a "minimum read
11 preamble period would be equal to nine
12 nanoseconds." That's in the middle of that
13 paragraph, yes.

14 Q. Exhibit 1113 teaches that the
15 read preamble may be set equal to 0.9 to 1.1
16 clock periods, and that read preamble period may
17 be used in accordance with the JEDEC
18 specifications for validating the read preamble;
19 correct?

20 A. Yeah, I think we would have to be
21 very careful of what he means by "validating"
22 the preamble," but those are the words there.

23 Q. And then in the next paragraph of
24 Column 3 of Exhibit 1113, towards the end of the
25 paragraph at the bottom of the column, the

1 inventors at Intel teach that when the DQS
2 strobe signal is low for a certain amount of
3 time, "then a valid read preamble is presumed to
4 have been detected"; correct?

5 ATTORNEY WARRICK: Objection;
6 form.

7 THE WITNESS: Those are the words
8 in Column 3. Again, the -- this solution will
9 detect a valid preamble well in advance of the
10 actual preamble most of the time.

11 So the valid preamble, in the
12 author's own words, is between .9 and 1.1 clock
13 cycles in advance of the first rising edge. And
14 we recognize that the start of the period of
15 time when the voltage on the DQS signal is low
16 can be way in advance of the start of the valid
17 preamble, to use this author's words.

18 So the statement that a valid
19 read preamble is presumed when a low voltage is
20 detected is inaccurate because, by this
21 terminology, they are presuming to detect a
22 valid preamble well in advance of the actual
23 preamble.

24 So there is tremendous tension
25 here between what the author is saying and --

1 and the words he's using about detecting a valid
2 preamble and the reality of the circuitry in a
3 real system. The transition -- the transition
4 from a midpoint to a low can happen at any time
5 in advance of 1.1 cycles ahead of the first
6 rising transition of DQS.

7 So I think that a POSITA reading
8 this paragraph would understand that this author
9 is detecting a valid read preamble well in
10 advance of the actual preamble, as specified in
11 the JEDEC standard.

12 BY ATTORNEY CHANDLER:

13 Q. In the JEDEC standard, as we
14 discussed yesterday, the preamble is required to
15 start between 1.1 and 0.9 clock cycles before
16 the valid data signal?

17 A. That's correct. And, in fact,
18 the -- the -- what is meant by the valid
19 preamble that is between .9 and 1.1 cycles is
20 that the DRAM is driving that signal low during
21 that period. It's not saying anything about any
22 transition at the start of that period or that
23 the DQS signal has not been at a low value for
24 an eternity in advance of that.

25 Q. Both the JEDEC standard that we

1 looked at before, marked as Exhibit 1064, as
2 well this patent, marked as Exhibit 1113,
3 specify that the preamble must start no earlier
4 than 1.1 clock cycles in advance; correct?

5 A. And you have to understand what
6 that means. Per the JEDEC standard, which
7 defines the behavior of the DRAM, the standard
8 says that the DRAM has to drive the DQS low no
9 later than .9 cycles ahead of the first DQS
10 rising transition.

11 It's not saying anything about
12 what is on the DQS signal before that. And I
13 think Dr. Wolfe confirmed that that midpoint
14 indicator on the timing diagram that we looked
15 at previously from the JEDEC standard does
16 not -- only says that it's -- the value of --
17 that the DRAM is not driving the DQS in advance
18 of the start of the preamble.

19 The drivers in the DRAM are in a
20 tri-state mode, not driving high or low. Which
21 means the voltage -- the actual voltage on the
22 DQS signal is -- I don't care as far as the
23 DRAMs are concerned; it's not part of their
24 specification. It could be driven by some other
25 device in terms of a write transaction or some

1 other DRAMs that sharing the DQS line.

2 The standard doesn't -- is only
3 saying what the DRAM will do during the
4 preamble, not what happens before the preamble.
5 And, in fact, this '378 patent is not accurate
6 with regard to the language of the bottom of
7 Column 3, because this author is detecting a
8 valid read preamble potentially well in advance
9 of the actual preamble, as determined by the
10 behavior of the DRAM.

11 Q. But you think the folks at Intel
12 are just wrong when they wrote the patent marked
13 as Exhibit 1113 and that their invention
14 wouldn't work?

15 A. Well, I have not read the entire
16 patent or looked at it in any detail. I don't
17 know exactly what they are claiming to have been
18 their invention. But I do know that the
19 language at the bottom of Column 3, which we've
20 looked at together, is internally inconsistent
21 with the language higher up in Column 3 and more
22 specifically is at odds with the JEDEC standard.

23 Q. Could you turn back to the JEDEC
24 standard marked as Exhibit 1064, page 26, the
25 Figure 23 that we were looking at previously,

1 and let me know when you're there.

2 A. I have that back up in front of
3 me.

4 Q. Did you say that, previously in
5 your answer a moment or two ago, that your
6 understanding of the DQS strobe signal is that
7 before the start of the preamble shown in
8 Figure 23, when the line in the figure for DQS
9 is in the middle, it's not low and it's not
10 high -- did you say that at that point in time
11 the DQS strobe signal would be tri-stated? Or I
12 believe the terminology used sometimes is that
13 the signal would be in a high impedance state?
14 Is that correct?

15 A. You have to be more precise in
16 your language.

17 The drivers are in a tri-state or
18 high impedance mode. The voltage on the signal
19 is indeterminate, is unknowable from the
20 perspective of the SDRAM because that's what
21 this document is about.

22 This document says how the DRAM
23 will behave. Figure 23 is saying that prior to
24 the start of the preamp period -- preamble
25 period, sorry -- the drivers on the DRAM that

1 are driving the DQS signal are in a high
2 impedance state, or tri-state state if you
3 prefer; and that the DRAM is not driving the DQS
4 line to any particular voltage; and that the
5 volt -- the actual voltage on that signal -- and
6 there is one -- is not determined by this DRAM
7 but is determined by something else or something
8 else that happened in the past and that is
9 lingering on that line, because nothing has
10 changed the voltage on that line.

11 Q. But just so I understand, the --
12 according to the JEDEC standard marked as
13 Exhibit 1064, as illustrated on page 26, before
14 the start of the DQS preamble, the DQS line will
15 not be driven by the DRAM, because the DRAM will
16 be in a high impedance state.

17 Is that correct so far?

18 A. So far so good.

19 Q. And then according to the JEDEC
20 standard, no earlier than 1.1 clock cycles
21 before the data the DQS strobe line must go low
22 as part of the preamble?

23 ATTORNEY WARRICK: Objection;
24 form.

25 THE WITNESS: It would be no

1 later than .9. So the -- the DQS is -- I'm
2 sorry. Let me start again.

3 BY ATTORNEY CHANDLER:

4 Q. It's -- between 1.1 and 0.9 clock
5 cycles before the data the DQS strobe signal
6 must go low?

7 ATTORNEY WARRICK: Objection;
8 form.

9 THE WITNESS: Let me say that a
10 little more precisely.

11 What the JEDEC standard says is
12 that the SDRAM is required to drive the DQS
13 signal low, actively drive it to a low voltage,
14 sometime between .9 and 1.1 cycles ahead of the
15 first rising edge of DQS. That's all it says.

16 BY ATTORNEY CHANDLER:

17 Q. But it says a little bit more
18 than that, because not only do you have to drive
19 it low starting 1.1 to 0.9 clock cycles ahead of
20 the data, you have to keep it low for that time
21 period; right?

22 A. You have to actively drive it low
23 for that period of time, starting between --
24 between 1.1 and .9 cycles ahead of the rising
25 edge of DQS. So it can't drive it low more than

1 1.1 cycles in advance, and it has to be driving
2 it low at .9 cycles ahead of the rising DQS
3 signal. The first --

4 (Simultaneous cross-talk.)

5 Q. If we turn back to the Intel
6 patent marked as Exhibit 1113, in Column 3
7 between lines 47 and 67, those inventors are
8 assuming the same setup; correct? That the read
9 preamble will be equal to a period of 0.9 to 1.1
10 clock cycles, as stated in the JEDEC standards;
11 correct?

12 ATTORNEY WARRICK: Objection;
13 form.

14 THE WITNESS: Again, I haven't
15 read this whole patent. I'm really not
16 comfortable interpreting what the mindset of the
17 inventors are or what their actual invention is.

18 I do know that whoever wrote
19 these paragraphs is not being precise about how
20 systems actually work and that the portion at
21 the very bottom of Column 3 that we discussed
22 previously, where it says that a valid read
23 preamble is presumed to have been detected -- I
24 think the word "presumed" here is carrying a lot
25 of weight, because these inventors are presuming

1 to have detected a valid preamble when they are
2 not actually in the preamble of an upcoming
3 transaction.

4 So the -- we have to be very
5 careful about reading the '378 patent in its
6 entirety to understand what exactly they're
7 inventing here and how it relates to the JEDEC
8 standard and how it would actually work in a
9 system.

10 You've only asked me to read, you
11 know, 20 lines in the middle of a patent. I
12 know that these 20 lines are internally
13 inconsistent and inconsistent with the JEDEC
14 standard; and that the word "presumed" to have
15 been detected is very troubling, because you can
16 presume to detect a preamble when you're not
17 actually in a preamble.

18 BY ATTORNEY CHANDLER:

19 Q. I think you said at one point in
20 your last answer that the inventors of
21 Exhibit 1113 were detecting something before the
22 preamble.

23 But to be clear, the bottom of
24 Column 3, the inventors of Exhibit 1113 are
25 talking about detecting the read preamble

1 itself, the read preamble that both they and the
2 JEDEC standard say will be equal to 0.9 to 1.1
3 clock cycles; correct?

4 ATTORNEY WARRICK: Objection;
5 form.

6 THE WITNESS: Again, I haven't
7 read this document. I don't know the invention.
8 I do know that the paragraph that you're asking
9 me to read in isolation does not say that.

10 What they say is that they're
11 presuming that they're in a read preamble when
12 they're not actually in a read preamble.

13 BY ATTORNEY CHANDLER:

14 Q. Let me summarize what I think I'm
15 hearing from you and what I think I'm reading in
16 Exhibit 1113, just to make sure that we're
17 clear.

18 So your opinion was and sounds
19 like still is, that you don't think a preamble
20 for a DQS strobe signal can be detected; whereas
21 the inventors of Exhibit 1113, bottom of
22 Column 3, lines 66 to 67, state that they have a
23 technique where a valid read preamble is
24 presumed to have been detected. Is that fair?

25 ATTORNEY WARRICK: Objection;

1 form.

2 THE WITNESS: Again, I would need
3 to read the entire document to see what actions
4 they take as a result of presuming that they're
5 in a preamble even when they're not in a
6 preamble. Because that's clear from the JEDEC
7 standard and the basic physics of digital
8 systems, that they will be detecting that they
9 are in a preamble based on the voltage on the
10 DQS signal being low for an extended period of
11 time, and they are presuming that they're in a
12 preamble and they're doing some action as a
13 result.

14 But they're not actually in a
15 preamble. It's not a reliable -- the point in
16 time when they're detecting a presumed preamble
17 is well in advance, most of the time, of a
18 actual preamble; because, again, the JEDEC
19 standard specifies the world from the SDRAM's
20 perspective, not from the memory controller's
21 perspective.

22 BY ATTORNEY CHANDLER:

23 Q. But as I listen to your answer,
24 it sounds to me like you are presuming that
25 they're not in a preamble; whereas, when I read

1 Exhibit 1113, Column 3, lines 47 to 67, they're
2 saying they are in a preamble, and this preamble
3 exists from 0.9 to 1.1 clock cycles before the
4 data, and that they have a technique to sample
5 the strobe signal repeatedly in that time frame,
6 and that if they sample it enough times and it's
7 low enough times in a row, then they have a
8 reasonable level of confidence or presumption
9 that this is the true, valid read preamble and
10 not a fluke.

11 Isn't that what they're saying
12 here?

13 ATTORNEY WARRICK: Objection;
14 form.

15 THE WITNESS: I think you are
16 reading a great deal into there that's not
17 actually in those words.

18 They're saying that they're
19 sampling the DQS -- and, again, I need to
20 reiterate that I've not read this document in
21 its entirety, I haven't looked at -- I don't
22 know what they're doing as a result of being in
23 a presumed read preamble.

24 But it's clear from the JEDEC
25 standard, from the DRAM's perspective and the

1 nature of the DQS line and how it's shared
2 amongst reads and writes in multiple DRAMs, that
3 their presumption of being in a preamble is not
4 the same as being in a preamble; that the actual
5 start of the preamble is not reliably
6 detectable.

7 BY ATTORNEY CHANDLER:

8 Q. But let me back up there, because
9 you seem to be putting a lot of the weight on
10 the word "presumption."

11 You're saying their presumption
12 of being in a preamble is not the same as being
13 in a preamble; whereas, when I read
14 Exhibit 1113, their invention, what I take away
15 from it is they have a technique which,
16 according to them, will reliably detect the
17 true, valid read preamble; even if no one is
18 telling them directly that this is the true read
19 preamble, they have a way to figure it out.

20 Isn't that what they are saying?

21 Now, you're pushing back and
22 saying, well, you know, I don't believe that
23 this technique would actually figure out the
24 true preamble. Maybe it's wrong, but what
25 they're teaching is, their technique allows them

1 to detect the actual read preamble. Right?

2 ATTORNEY WARRICK: Objection;
3 form.

4 THE WITNESS: No, that's not what
5 these paragraphs in Column 3 say. And perhaps
6 it's clarified elsewhere within the
7 specification. I don't know. I haven't read
8 the specification.

9 But if you are presuming that
10 you're in a preamble and you're going to
11 continue to presume you're in a preamble for 27
12 cycles, while the signal is low and then at some
13 point -- don't interrupt me, please -- it's --
14 the voltage on the DQS signal is low for 6 or 7
15 samples in a row, they're going to presume
16 they're in a preamble. It's going continue to
17 be low for another 20 cycles. They are going to
18 continue to presume they are in a read preamble.

19 At some point, they're right in
20 that they are in a read preamble and, lo and
21 behold, a rising transition on DQS happens
22 that's used to capture the data.

23 But there -- it -- the underlying
24 question that we haven't answered -- because I
25 haven't read the entire document -- is what do

1 they do as the result of being presumptively in
2 a preamble even when they're not in an actual
3 preamble?

4 BY ATTORNEY CHANDLER:

5 Q. But you keep assuming that this
6 may not be a preamble, and you're changing the
7 assumptions. Because you just said, well, what
8 if it's 20 cycles where it's low; but the JEDEC
9 standard precludes it being from 20 cycles. The
10 JEDEC standard says it can only be low for up to
11 1.1 clock cycles.

12 A. No --

13 ATTORNEY WARRICK: Objection;
14 form.

15 THE WITNESS: That's not what the
16 JEDEC standard says.

17 You have to understand the four
18 corners of the JEDEC standard, which is, the
19 DRAM is not allowed to drive the DQS signal
20 more -- low more than 1.1 cycle ahead of the
21 rising edge of DQS that it will generate, and it
22 has to drive the DQS signal low no less than .9
23 cycles ahead of that transition.

24 The standard says nothing about
25 the voltage on the DQS signal in advance of that

1 beginning of driving the signal by the SDRAM.

2 BY ATTORNEY CHANDLER:

3 Q. So --

4 A. I'm not finished yet.

5 The voltage on the DQS signal is
6 dependent on what's happened before -- a read
7 transaction, a write transaction by this DRAM or
8 some other DRAM. And the standard only says
9 what happens as a result of the DRAM's actions
10 one cycle -- approximately one cycle ahead of
11 when the DRAM is starting to drive data.

12 Q. The DQS strobe signal is driven
13 by the DRAM; right?

14 A. Some of the time, but not all of
15 the times.

16 Q. But the JEDEC standard tells us
17 when the DRAM can and cannot drive the DQ strobe
18 signal; right?

19 ATTORNEY WARRICK: Objection;
20 form.

21 THE WITNESS: And, in particular,
22 as we've reiterated numerous times here already,
23 prior to 1.1 cycles ahead of the rising
24 transition of DQS, the DRAM is explicitly
25 specified not to drive the DQS signal; that the

1 voltage on the DQS signal is dependent not on
2 the behavior of this DRAM but is dependent on
3 what happened before, by something else.

4 BY ATTORNEY CHANDLER:

5 Q. And the "something else" is also
6 governed by the JEDEC standard; right?

7 ATTORNEY WARRICK: Objection;
8 form.

9 THE WITNESS: No. It's --
10 it's -- it --

11 In general, yes, in the sense
12 that the only things in a real system that are
13 driving the DQS system is either a memory
14 controller or a DRAM.

15 The behavior of the memory
16 controller is indirectly specified in that --
17 the behavior of the DQS as its arrived at the
18 DRAM in a write transaction, is specified by the
19 standard; but you could have crazy systems where
20 there's other stuff going on on those lines
21 that's not related to the memory system. It's
22 plausible, given the standard.

23 The standard only cares about how
24 you stimulate the DRAM and what it's going to do
25 as a result. The system designer is free to do

1 anything else.

2 BY ATTORNEY CHANDLER:

3 Q. That's not entirely fair, because
4 every DRAM needs to comply with the JEDEC
5 standard. The JEDEC standard says, when your
6 turn is up, you need to tri-state and stop
7 driving the DQS strobe signal, let someone else
8 take a turn; right?

9 ATTORNEY WARRICK: Objection;
10 form.

11 THE WITNESS: Or you could have
12 another turn next yourself.

13 The -- that Figure 23 of the
14 JEDEC DDR2 standard that we were looking at
15 before -- which exhibit was that? 1064.

16 So what it says is that at the
17 end of the burst read transaction, that the DRAM
18 has to tri-state its drivers at the end, and it
19 specifies a time after the last falling edge of
20 DQS, at which point it has to stop driving the
21 signal.

22 The voltage on the line will not
23 change until something else drives it again. So
24 it will stay low indefinitely, because it's low
25 just before the tri-state period, and

1 it's -- you know, the signals have capacitance,
2 they have inertia as far as the voltage is
3 concerned.

4 So this DRAM is driving the DQS
5 signal low during the last bit period. It's
6 saying, I'm not driving it anymore. The voltage
7 is going to stay low until something else,
8 perhaps this DRAM again, in another read
9 transaction, drives it to a different state
10 again.

11 BY ATTORNEY CHANDLER:

12 Q. The controller --

13 A. Not necessarily the controller.

14 Q. No, I was starting a new
15 sentence.

16 The memory controller -- the
17 memory controller tells each rank of DRAM when
18 to perform a read command and, therefore, when
19 to drive the DQS strobe signal; correct?

20 ATTORNEY WARRICK: Objection;
21 form.

22 THE WITNESS: Yes, essentially.

23 BY ATTORNEY CHANDLER:

24 Q. So the memory controller has a
25 hand in what's happening on the DQS strobe

1 signal; correct?

2 A. And, in fact, most memory
3 controllers know when to expect a memory
4 transaction incoming from a DRAM and don't
5 employ any technique such as described within
6 the '378 patent. They don't need to detect the
7 preamble, per se, because they know when it's
8 coming. They know when approximately -- when
9 the first rising edge is going to be.

10 Q. But to be clear, the JEDEC
11 standard required a preamble. That's an
12 important part of the standard; right?

13 A. Yes, it does.

14 ATTORNEY WARRICK: Objection to
15 form.

16 Sorry, Dr. Przybylski, just make
17 sure to give me a chance to interject if
18 necessary.

19 THE WITNESS: My apologies. I'm
20 getting too wrapped up in this.

21 ATTORNEY CHANDLER: My apologies
22 as well.

23 ATTORNEY WARRICK: It's exciting
24 subject matter.

25 THE WITNESS: Well, it's --

1 there's subtly here that's important for this
2 situation, because the -- Dr. Wolfe said some
3 things in his declaration and repeated in the
4 petition that are not accurate and that your --
5 vis-a-vis the behavior of the DQS signal and the
6 DRAMs at issue here. And it's important that
7 the Board understand what's really being
8 specified by the standard and how the systems
9 really work.

10 Go ahead.

11 BY ATTORNEY CHANDLER:

12 Q. It's also important for the Board
13 to understand what a person of ordinary skill in
14 the art at the time would have understood. And
15 contemporaneous patents, such as Exhibit 1113,
16 are reasonable evidence of what was understood
17 at the time; correct?

18 ATTORNEY WARRICK: Objection;
19 form.

20 THE WITNESS: Yes. And you have
21 to make sure your understanding of these
22 references are consistent with reality.

23 And so when the authors of the
24 '378 say, "We presume we're in a read preamble,"
25 is not the same as saying, "We know we're in a

1 preamble."

2 BY ATTORNEY CHANDLER:

3 Q. Again, I think you're drawing a
4 distinction between presuming to be in a
5 preamble and knowing to be in a preamble, when
6 it sounds like they're just shades of gray,
7 which is, you're assuming that knowing that
8 you're in a preamble is 100 percent certainty;
9 whereas, the inventors of Exhibit 1113 have come
10 up with the technique -- they used the word
11 "presumed," but they're using the word
12 "presumed" to indicate a sufficiently reliable
13 method where it may not be 100 percent certainty
14 but it's some very close level of certainty that
15 they're able to accomplish detecting, with a
16 reasonable amount of certainty, the read
17 preamble.

18 Is that fair?

19 ATTORNEY WARRICK: Objection;
20 form.

21 THE WITNESS: Apologies.

22 No, that's not fair, because we
23 haven't reviewed the entire patent. We don't
24 know what they're doing as a result of this
25 presumption. In fact, the probability that

1 their initial presumptive detection is an actual
2 preamble is extremely low. Because of the
3 electrical behavior of the DQS line, as we've
4 described together over the last ten minutes or
5 so, the DQS signal will stay low after the end
6 of one transaction.

7 So if you're a memory controller
8 and you've just received a read transaction, the
9 DQS signal is low; the next read transaction,
10 for example, might be 20 clock cycles later, the
11 technique of the '379 as it's articulated in the
12 bottom of Column 3 -- and, again, I haven't read
13 the entire thing -- it will immediately start
14 registering a presumed preamble, immediately
15 after the end of the last read transaction and
16 will continue to presume to be in a read
17 transaction throughout that 20-cycle period
18 until the actual rising edge of the next read
19 transaction from this -- the same DRAM for a
20 different DRAM.

21 So the probability that the
22 presumption of being in a read preamble is
23 actually in a read preamble is very low,
24 depending on the actual utilization of the
25 memory bus.

1 BY ATTORNEY CHANDLER:

2 Q. I think we discussed earlier that
3 Intel was one of the companies that made memory
4 controllers; right?

5 A. Yes.

6 Q. They made a lot of memory
7 controllers in the early 2000s; right?

8 A. Very successfully, yes.

9 Q. And it's the memory controller
10 for a read command that needs to detect the
11 preamble of the DQS strobe signal -- in other
12 words, it's Intel product that needs to detect
13 when there's a read command that has a DQS
14 preamble; correct?

15 A. No.

16 ATTORNEY WARRICK: Objection;
17 form.

18 THE WITNESS: No. That's not --
19 that is, in fact, not how it works.

20 What the memory controller has to
21 do is detect the rising edge of DQS at the end
22 of the preamble and use that to capture the
23 data.

24 The purpose of the preamble is to
25 ensure that the rising edge of DQS that

1 signifies the first piece of data is clean and
2 valid. That's the only purpose of the preamble.

3 And that's why the preamble is
4 specified to be of different lengths, inbound
5 and outbound, because the start of the preamble
6 is not significant. It's just saying that the
7 DRAM manufacturers are necessarily going to
8 drive the DQS low for one cycle ahead of the
9 rising edge of DQS, in order to ensure that --
10 at the other end -- at the memory controller,
11 the rising edge of DQS will be clean and useable
12 to capture the data.

13 BY ATTORNEY CHANDLER:

14 Q. Intel makes the memory
15 controllers that receive the DQS strobe signal
16 on a read command; correct?

17 ATTORNEY WARRICK: Objection;
18 form.

19 THE WITNESS: Yes. All memory
20 controllers have to receive the DQS signal in
21 order to receive the rising and falling edges
22 that signify the transmission of data.

23 BY ATTORNEY CHANDLER:

24 Q. In the patent by Intel, marked as
25 Exhibit 1113, in Column 1, line 56 through 59,

1 the inventors state there is a need for a
2 technique which can identify a valid read
3 preamble; correct?

4 A. Where are you reading again,
5 please? Column 1 what?

6 Q. Line 56 through 59 or so.

7 The inventors at Intel, the
8 company that makes the memory controller that
9 received the read commands and receives the DQS
10 strobe signal from the read command state in
11 Column 1 starting around line 56 of
12 Exhibit 1113, "There is a need for a technique
13 which can identify a valid read preamble";
14 correct?

15 A. Those are the words in that short
16 snippet of Column 1. We don't know what that
17 need is. It may be a need specific to the
18 internals of their particular memory controller.

19 What I'm saying is that the JEDEC
20 standard specifies the read preamble in terms of
21 the DRAM's behavior in order to make sure that
22 the rising edge of DQS is cleanly discernible in
23 order to use it to capture the data. Certainly
24 there are many memory controllers out there that
25 don't detect a preamble in order to do anything

1 in particular; they just wait for the DQS and
2 they capture the data as a result.

3 So the authors of the '317 saying
4 there's a need to do that is at odds with -- let
5 me start that sentence again.

6 The fact that the authors of the
7 '378 are saying that they have a need specific
8 to their design to detect the start of a
9 preamble is not the same as saying that all
10 memory controllers need to detect the start of a
11 preamble. In fact, that's not the case.

12 Q. I understand your opinion that
13 you believe it's not possible to discern the
14 preamble of the DQS strobe signal; but these
15 inventors at Intel, in Exhibit 1113, state that
16 there's a need to identify a valid read
17 preamble, and they purport to disclose a
18 technique for doing that. So there's a little
19 disagreement between you and your opinion and
20 what's being disclosed in Exhibit 1113.

21 A. I think --

22 ATTORNEY WARRICK: Objection to
23 form.

24 BY ATTORNEY CHANDLER:

25 Q. Is that fair?

1 A. No, I don't think that's fair,
2 because the way that these DQS signals operate
3 in a signal -- in a system is not a matter of
4 opinion; it's a matter of fact. And the fact --
5 and that the authors of this patent have said
6 they have a need to do something doesn't alter
7 those facts.

8 And the fact -- and then later in
9 Column 3 where they say, well, we can detect
10 that the signal is low and we're going to
11 presume that that is, in fact, a preamble and
12 perhaps do something as a result of that
13 presumption is not inconsistent with the reality
14 of the DQS signal and the JEDEC standards, which
15 says that the DQS is continuously low between
16 transactions most of the time except for -- you
17 know, for extremely low -- long periods of
18 idleness, the voltage on the DQS signal may
19 drift.

20 But in any reasonably busy memory
21 system, the DQS will be low continuously between
22 memory transactions; and the technique that is
23 articulated at the bottom of Column 3 of the
24 '378 patent will continuously indicate a
25 presumption of a preamble in advance of the

1 actual preamble.

2 The memory controller knows when
3 the actual preamble is approximately going to
4 show up; but they're doing this presumptive
5 preamble well in advance of that.

6 Or at least we believe so.

7 Again, I haven't read the whole thing. Maybe
8 they're qualifying it by when they expect the
9 preamble to show up in their memory controller,
10 because they know what the read latencies are
11 and they know what the -- what the general
12 structure of the memory system is.

13 So I think when you try and
14 rationalize their words with the reality of
15 memory systems, you understand that their
16 presumption of being in a preamble is different
17 and not the near 100 percent that you wish, but
18 that it is an indication that we're between two
19 transactions and that there will be another one
20 coming sometime.

21 Q. Everything you just said, that's
22 not anywhere in Exhibit 1113; right?

23 A. That's -- what I just said is a
24 natural consequence of 1064 and 1113 taken
25 together, because they relate to each other;

1 right? The -- this is specifically about DDR
2 SDRAMs, which, I think, is what you were having
3 me look at. 1064 is DDR2.

4 So, again, we have a little
5 disconnect there, but the basic physics of DQS
6 signals doesn't change.

7 The JEDEC standard and physics
8 says what goes on on the DQS signal at the
9 memory controller during the read transactions.
10 You have to read the '378 in light of that
11 reality, and that's what a POSITA would be able
12 to do.

13 ATTORNEY WARRICK: Could I
14 suggest this may be a good time for a break?
15 We've been going well over an hour.

16 THE WITNESS: I agree.

17 ATTORNEY CHANDLER: Almost. Let
18 me just -- follow up.

19 BY ATTORNEY CHANDLER:

20 Q. Do you agree with the statement
21 in Column 1 of Exhibit 1113 starting at line 60
22 that the existing DDR SDRAM protocol does not
23 provide a feedback to the memory controller
24 indicating when to look for the data strobe?

25 A. So reading the entire paragraph

1 that that one sentence is a part of, or at least
2 the following sentences, it goes on to say,
3 "rather the memory controller launches a read
4 command and then somehow knows -- somehow
5 identifies the arrival of the DQS signal."

6 In fact, the memory controller
7 knows, based on the programs read latency of the
8 DRAMs approximately when the DQS is going to be
9 arriving.

10 So it's clear that -- from the
11 perspective of the authors of the '378 patent
12 that their memory controller is not using all of
13 the information at its disposal to know when to
14 expect data to return. Because as you've noted,
15 the memory controller knows all that stuff.
16 It's the -- it's in charge.

17 So for some reason, they've --
18 the context of their invention and their memory
19 controller is that the memory controller is
20 going to presume to be in a preamble well in
21 advance of an actual preamble and then somehow
22 be ready for a DQS signal arriving at some
23 random time; but, in fact, it's not at a random
24 time and the memory controller knows when it's
25 going to be coming, approximately.

1 So, again, you have to read the
2 '378 as a POSITA would in the context of the
3 JEDEC standard and the reality of memory
4 subsystems to understand what the authors of the
5 '378 are actually saying.

6 Q. But is it correct that in a DDR
7 SDRAM system, there's not some separate signal
8 that tells the recipient, such as the memory
9 controller in this situation, when to look for
10 the data strobe?

11 ATTORNEY WARRICK: Objection;
12 form.

13 THE WITNESS: Yes, that's true;
14 there is no such signal. And you have to ask
15 why, is there no such signal?

16 If there was a need -- a
17 pervasive need for such a signal, the JEDEC
18 committee would have put it in. But there isn't
19 one, because the memory controller knows when
20 the data is going to be coming back, modulus the
21 transmission delays along the signal lines.

22 So the memory controller knows
23 when it sent the read command. It knows what
24 the read latency of these DRAMs is. It knows
25 how -- in the DDR world, less so.

1 But it -- it knows roughly the
2 time delay associated with communicating with
3 the DRAMs, and so it knows approximately when to
4 expect a DQS rising edge, signifying the return
5 of the data that it asked for.

6 Go ahead.

7 BY ATTORNEY CHANDLER:

8 Q. You say the memory controller
9 knows approximately when the strobe and then the
10 data should arrive.

11 But the whole point of
12 Exhibit 1113 is that knowing approximately when
13 the strobe and when the data is going to arrive
14 isn't good enough, because we're starting to get
15 at higher speeds; and at the bottom of Column 1,
16 top of Column 2 what the inventors are talking
17 about is that there's going to be uncertainty
18 due to flight time and other routing of the
19 signals. And so you can't count on when the
20 strobe and the data is supposed to arrive; you
21 can't count on approximately when it's going to
22 arrive. They are proposing a technique that
23 doesn't rely on any of that, but instead relies
24 on when the strobe itself has a preamble that
25 arrives. Isn't that correct?

1 ATTORNEY WARRICK: Objection;
2 form.

3 THE WITNESS: No, that's not
4 correct. Because the -- let me read.

5 (Witness reviews document.)

6 The uncertainty that's talked
7 about and the variance that's talked about in
8 the following paragraphs of the background of
9 the '378 patent -- which, again, I haven't read
10 in its entirety -- is on the order of a fraction
11 of a clock cycle. Because in the DDR SDRAM
12 generation, the operating frequencies were low
13 by today's comparisons, and so the flight time
14 delays are fractions of a cycle and not multiple
15 cycles.

16 In contrast, their technique for
17 presumptively detecting a preamble has many,
18 many cycles of uncertainty between the
19 presumptive preamble and the actual preamble.

20 So, in fact, their technique will
21 have some value for them. It is not universal.
22 If this missing wire was important, it would
23 have been included in this SDRAM standard and
24 all subsequent SDRAM standards; but, in fact,
25 there are sufficient techniques, including the

1 memory controller knowing how many cycles of
2 latency it programmed the SDRAMs to have, so
3 that the -- for most memory controllers, there
4 is no need to presumptively try and determine
5 whether you're in a preamble or not.

6 BY ATTORNEY CHANDLER:

7 Q. So, in your opinion, the
8 controller will know, for the read command,
9 approximately when the strobe signal and the
10 data signal should arrive; correct?

11 ATTORNEY WARRICK: Objection;
12 form.

13 THE WITNESS: The memory
14 controller will know in which cycle the data is
15 going to come back. The actual phase
16 relationship between the rising edge of the DQS
17 signal indicating the start of the first piece
18 of data on the DQ lines and the memory
19 controller's clock signal, that phase
20 relationship, will vary from instance to
21 instance, from one memory system design to
22 another, from one DRAM to another, from one rank
23 to another. But that's all a fraction of a
24 cycle.

25 The memory controller can know,

1 and does know in most cases, which cycle the
2 data is going to come back in, particularly in
3 the DDR SDRAM regime.

4 BY ATTORNEY CHANDLER:

5 Q. So, in your opinion, a memory
6 controller will know approximately when the
7 strobe and data signals will arrive within
8 approximately one clock cycle; and then
9 Exhibit 1113 teaches that it's possible to
10 detect whether that strobe signal is a preamble
11 by repeatedly sampling the signal to see if it's
12 low for a certain amount of time. Is that fair?

13 ATTORNEY WARRICK: Objection;
14 form.

15 THE WITNESS: No, that's not
16 fair. There are a couple of inaccuracies in
17 that long question.

18 The first was that the cycle in
19 which the data is coming back is not
20 approximately known; it's precisely known. The
21 only uncertainty or variability, to use the
22 language at the top of Column 2 of the '378
23 patent -- which again I haven't read in its
24 entirety -- is only related to flight time
25 delays between the memory controller and the

1 DRAM, and those in the DDR regime are a fraction
2 of a cycle.

3 So the memory controller knows
4 which cycle the data is going to be coming back
5 in. Precisely when in that cycle is the
6 variability.

7 In contrast, the technique of the
8 '378 patent is about presumptively detecting a
9 preamble way, way in advance of that.

10 For some reason that's known to
11 these inventors, they had a need for it.
12 Most -- every other memory controller that I've
13 looked at or had exposure to in detail doesn't
14 do this. There's no need -- presumptive need or
15 universal need to do this. If there was, this
16 signal that they're referring to -- that they're
17 feeling a lack of would have been included by
18 JEDEC.

19 And Intel is a JEDEC member, by
20 the way. So if the memory controller designers
21 at Intel said, hey, we need this signal that's
22 missing, Intel would have ensured that it was
23 part of the standard.

24 The standard is complete and
25 adequate in its own right, as verified by

1 Intel's votes on the matter.

2 And so you're inferring a great
3 detail about the fact that these guys are
4 employed by Intel. They have a particular need
5 for their particular memory controller to do
6 something presumptively. It's not universal.

7 BY ATTORNEY CHANDLER:

8 Q. Do you agree that adding a pin to
9 a controller would increase costs, and that,
10 oftentimes, companies like Intel and
11 organizations like JEDEC will avoid adding a pin
12 in a signal if they have another way to get the
13 job done that doesn't require the additional pin
14 and additional signal?

15 ATTORNEY WARRICK: Objection;
16 form.

17 THE WITNESS: That's a generally
18 true statement.

19 With regard to this situation,
20 the counter example is that the DQS signals were
21 added because they were required. They needed
22 to be added to make the systems work at high
23 frequency, relative to the previous generations
24 of DRAMs.

25 So the JEDEC committee, including

1 Intel, knew that the standard that they created
2 with the -- with the behavior of the DQS signal
3 as from the DRAM's perspective was sufficient to
4 facilitate accurate capturing of data. And
5 there was no need for this additional line
6 because they recognized that the memory
7 controllers knew when the data was coming back,
8 and there was no need to presumptively, well in
9 advance of an actual preamble say, oh, we might
10 be in a preamble now; we might be in a preamble
11 now; we might be in a preamble -- for cycles and
12 cycles on end before the actual preamble.

13 What the authors of the '378 are
14 doing as a result of that presumption is not
15 clear, because I haven't read the whole thing.
16 It may be trivial. It may be something unique
17 to their particular memory controller. But
18 regardless, it's this -- this presumed need is
19 specific to them and not a universal
20 characteristic of DDR SDRAM memory systems.

21 And we really should take a break
22 at this point.

23 BY ATTORNEY CHANDLER:

24 Q. Do you think a person of ordinary
25 skill in the art would have known about

1 Exhibit 1113 -- is it fair to say it's in the
2 prior art?

3 ATTORNEY WARRICK: Objection;
4 form.

5 THE WITNESS: It is fair to say
6 it was published in advance of the 2004-2005
7 time frame that we are focusing on.

8 ATTORNEY CHANDLER: Okay, let's
9 take a break.

10 THE VIDEOGRAPHER: Off the record
11 at 8:26 a.m. Pacific Time.

12 (Recess taken from 8:26 a.m. to
13 8:37 a.m.)

14 THE VIDEOGRAPHER: On the record
15 at 8:37 a.m. Pacific Time.

16 BY ATTORNEY CHANDLER:

17 Q. Please pull up the '417 and '215
18 patents marked as Exhibit 1001, and let me know
19 when you have them.

20 A. I have the '417 up.

21 Q. And go ahead and pull up the '215
22 as well. We'll cover them both at the same
23 time.

24 A. Okay, hold on.

25 Q. Then you can go to Column 1 of

1 both to start.

2 A. Okay. I'm looking at Column 1 of
3 both of '417 and '215.

4 Q. In Column 1 of both the '417 and
5 '215 patents, toward the middle of the column
6 there's the field of invention, which indicates
7 that the '417 and '215 patents relate "generally
8 to memory modules of a computer system";
9 correct?

10 A. The field of the invention of
11 both patents is:

12 "Relates generally to memory
13 modules of a computer system, and
14 more specifically to devices and
15 methods for improving the
16 performance, the memory capacity, or
17 both, of memory modules."

18 Q. The '417 and '215 patents are not
19 limited to JEDEC-compliant memory systems;
20 correct?

21 ATTORNEY WARRICK: Objection;
22 form.

23 THE WITNESS: You're referring to
24 the scope of the claims and what that is, I
25 think that's outside of -- I haven't made any

1 opinions about infringement or the scope of the
2 claims.

3 BY ATTORNEY CHANDLER:

4 Q. But the scope of the claims is
5 the same whether we're talking about
6 infringement or invalidity; right?

7 A. Yes, the scope of the claims is
8 the scope of the claims. It's a matter --
9 the -- my opinions have been to rebut the
10 arguments of the petition and the corresponding
11 declaration that seek to invalidate those
12 claims.

13 Q. Let's start with the
14 specification of the '417 and '215 patents.

15 Nothing in the specification of
16 the '417 and '215 patents limits those patents
17 to JEDEC-compliant memory systems; correct?

18 ATTORNEY WARRICK: Objection;
19 form.

20 THE WITNESS: There are certain
21 embodiments that relate to JEDEC standardized
22 devices of modules. I don't know whether they
23 are, in fact, limiting or not to that specific
24 set of embodiments. That's not something that
25 I've opined on.

1 BY ATTORNEY CHANDLER:

2 Q. So you have not offered the
3 opinion that either the claims or the
4 specification of the '417 and '215 patents are
5 limited to JEDEC-compliant memory systems; is
6 that fair?

7 A. Let me review my declaration.
8 (Witness reviews document.)

9 In looking at Section 6 of my
10 declarations vis-a-vis the '417 and '215
11 patents, I'm not seeing an opinion that relates
12 to whether anything in the specification is
13 formally limiting the scope of the claims to
14 JEDEC-compliant memories and modules.

15 Q. Please turn to Figure 1 of the
16 '417 and '215 patents marked as Exhibit 1001.
17 Let me know you're there.

18 A. Yes, I'm looking at Figure 1 in
19 both patents.

20 Q. Figure 1 of the '417 and '215
21 patents, marked as Exhibit 1001, shows a memory
22 module 10, which is the big dashed box,
23 including memory devices 30 on the left and a
24 buffer circuit 40 in the middle; correct?

25 ATTORNEY WARRICK: Objection;

1 form.

2 THE WITNESS: Yes, that's
3 generally accurate.

4 BY ATTORNEY CHANDLER:

5 Q. Please turn to Column 6 of the
6 '417 patent starting around line 43, and the
7 corresponding location in the '215 patent is
8 Column 5 starting around line 63. And let me
9 know when you're there.

10 A. I have those columns up in front
11 of me.

12 Q. The '417 and '215 patents teach
13 that memory modules 10, "compatible with
14 embodiments described herein, include, but are
15 not limited to," and then there's a list of
16 different types of memory modules; correct?

17 A. Yes, those are the words of
18 Column 6 of the '417.

19 Q. And then a little bit further
20 below that, the '417 and '215 patents teach that
21 memory devices 30 "compatible with embodiments
22 described herein, include, but are not limited
23 to," and then it goes onto list various types of
24 memory devices; correct?

25 A. Yes, in Column 6 of '417 it does

1 list a variety of JEDEC standardized memory
2 devices and refers to them with regard to some
3 embodiments.

4 Q. The '417 and '215 patents
5 explicitly do not limit either the memory module
6 or the memory devices to any particular JEDEC
7 standard or to JEDEC at all; correct?

8 ATTORNEY WARRICK: Objection;
9 form.

10 THE WITNESS: The patent does
11 refer to the JEDEC standards specifically in
12 some places. It does, as you indicated,
13 indicate that the modules and the memories are
14 not limited to the one specifically listed. It
15 could include others as well.

16 BY ATTORNEY CHANDLER:

17 Q. Please turn to Column 23 of the
18 '417 patent, starting around line 22, and the
19 corresponding language in the '215 patent is in
20 Column 21 starting around line 8. And let me
21 know when you're there.

22 A. I'm look at including 23 of the
23 '417.

24 Q. And do you have the '215 around
25 Column 21 as well?

1 A. Let me look at 21. They're
2 identical?

3 Q. Yes. I mean, they're identical
4 as far as I can see.

5 A. Yes, they both have a paragraph
6 starting, "In certain embodiments utilizing
7 memory density multiplication embodiments," yes.

8 Q. Are you familiar with the concept
9 of rank multiplication?

10 A. Generally yes; and as it's
11 described within this patent specification, yes.

12 Q. The '417 and '215 patents
13 disclose a buffer circuit 40 with translation
14 logic for performing what's commonly known as
15 rank multiplication; is that fair?

16 ATTORNEY WARRICK: Objection;
17 form.

18 THE WITNESS: So the last
19 sentence of that paragraph in Column 23 of the
20 '417 beginning at line 32 of that column says:

21 "Furthermore, in certain
22 embodiments, the translation logic
23 equations vary depending on whether
24 the implementation multiplies memory
25 devices per rank or multiplies the

1 number of ranks per memory module."

2 So to that extent, for certain
3 embodiments, they do claim rank multiplication
4 as a part of the logic -- the translation logic.
5 BY ATTORNEY CHANDLER:

6 Q. And the two sentences before what
7 you are reading -- for example, Column 23 of the
8 '417 patent starting at line 26 -- is discussion
9 of circuit 40 using translation logic to perform
10 what we commonly refer to now as rank
11 multiplication; correct?

12 ATTORNEY WARRICK: Objection;
13 form.

14 THE WITNESS: I think the
15 sentence that I read was the end of that
16 paragraph more accurately summarizes the idea
17 that the memory devices 10 can include, in
18 certain embodiments, implementations of a rank
19 multiplication of the number of ranks, which is
20 what we would call rank multiplication, or --

21 BY ATTORNEY CHANDLER:

22 Q. And --

23 A. Yeah, go ahead.

24 Q. Do you understand the concept of
25 a density transition bit?

1 A. Yes, the term "density transition
2 bit" occurs in several places in the
3 specification of the '417 and '215. I think it
4 is not a term that has a lot of use, if any use,
5 outside of the specification.

6 But within the context of this
7 specification, it's clear what the inventors
8 mean by it.

9 Q. And what's the relationship, in
10 the '417 and '215 patents, between the density
11 transition bit and rank multiplication?

12 A. Reading from the Column 24 of the
13 '417, it says that the "Table 4 lists the
14 corresponding density transition bits for the
15 density transitions between DDR2 memory
16 densities of Table 3."

17 So they are identifying in
18 Table 4 which address or bank bits change in
19 terms of the width of the various fields between
20 one density of memory device and another; and
21 that has bearing on their rank multiplication
22 implementation.

23 Q. At the top of Column 23 of the
24 '417 patent it states:

25 "The term 'density transition

1 bit' is used to refer to the
2 additional address signal bit which
3 is used to access the additional
4 memory by selecting which rank of
5 memory devices is enabled for a read
6 or write transfer operation."

7 Correct?

8 A. So what line did you start
9 reading at on 23? Or you were paraphrasing not
10 reading; correct?

11 Q. No, I was reading starting around
12 line 7 of 23 of the '417 patent.

13 A. Okay, let me find that exactly.
14 Oh, I see where it is. Okay.
15 Just one moment, please. [Reading sotto voce].
16 Yeah, so you accurately read that
17 portion of the Column 23.

18 Q. So how is the density transition
19 bit used to perform rank multiplication? How
20 does it work?

21 ATTORNEY WARRICK: Objection;
22 form.

23 THE WITNESS: In brief the --
24 when using smaller devices to simulate larger
25 devices, the address bits that are different

1 between -- in terms of the width of the row or
2 bank addresses that are different between the
3 two densities are the ones that need to be --
4 that play an important role in the simulation of
5 a larger density by two smaller densities
6 devices, which is the central idea of rank
7 multiplication.

8 BY ATTORNEY CHANDLER:

9 Q. And then turning back to line
10 22 -- or the paragraph beginning at line 22 of
11 Column 23 of the '417 patent, as well as in the
12 '215 patent it's the paragraph starting at line
13 8 of Column 21.

14 The buffer circuit 40 has
15 translation logic for performing rank
16 multiplication using the density transition bit;
17 correct?

18 ATTORNEY WARRICK: Objection;
19 form.

20 THE WITNESS: First of all, 40 is
21 just the circuit, it's not called the buffer
22 circuit, which -- just for precision.

23 Yes, it says, starting at line
24 26:

25 "The circuit 40 of certain

1 embodiments utilize the implied --
2 utilizes implied translation logic
3 equations having variations
4 depending on whether the density
5 transition bit is a row or a column
6 or internal bank address bit."

7 So the specific density
8 transition bit for different density transitions
9 is a factor in circuit 40's translation logic
10 equations.

11 BY ATTORNEY CHANDLER:

12 Q. In the '417 and '215 patents, the
13 translation logic in circuit 40 will receive
14 chip-select signals and address signals;
15 correct?

16 ATTORNEY WARRICK: Objection;
17 form.

18 THE WITNESS: If we refer back to
19 Figure 1 of the two patents, it shows that
20 between the circuit 40 and the -- I think the
21 controller 20, there are address and control and
22 chip-select signals indicated.

23 BY ATTORNEY CHANDLER:

24 Q. And so what signals are used to
25 perform rank multiplication? How are they used?

1 So what are the inputs, the translation logic in
2 circuit 40, and what's the output? What are you
3 trying to accomplish?

4 ATTORNEY WARRICK: Objection;
5 form.

6 THE WITNESS: The goal of rank
7 multiplication is, as I noted earlier, to make
8 lower density memory devices that are available
9 and cost-effective appear to be a larger density
10 device that may be less cost-effective at the
11 present time, at the point of decision of an
12 engineer making selections of memory density
13 devices. So that's the purpose of rank
14 multiplication.

15 It's based on the addresses, and
16 there is -- the addresses in and the addresses
17 out such that the memory controller perceives
18 one set of memory devices, even though that is a
19 deception on the part of the circuit 40.

20 BY ATTORNEY CHANDLER:

21 Q. And what happens with respect to
22 the number of chip-select signals when you're
23 performing rank multiplication?

24 ATTORNEY WARRICK: Objection;
25 form.

1 THE WITNESS: For the embodiments
2 utilizing rank multiplication, there would be a
3 change in the number of chip-select signals, as
4 we see in some of the figures -- for example,
5 in -- starting at Figure 9, you see examples of
6 different embodiments with different numbers of
7 chip-selects coming into the module and
8 different numbers of ranks being controlled by
9 circuit 40.

10 BY ATTORNEY CHANDLER:

11 Q. Figure 1 shows that as well;
12 correct?

13 A. Figure 1 is less precise. It
14 doesn't -- it shows chip-select signals going to
15 the different ranks 32 from circuit 40; and it
16 shows at least some chip-select signals between
17 memory controller 20 and circuit 40.

18 Some of the later figures are
19 more precise with regard to exactly how many
20 chip-select signals are received by the module
21 10 from the memory controller and how many
22 chip-selects are generated towards the ranks
23 within the module 10.

24 Q. Figure 1 in the '417 and '215
25 patents shows twice as many chip-select signals

1 being output by circuit 40 compared to the
2 number of chip-select signals being input to the
3 circuit 40; correct?

4 ATTORNEY WARRICK: Objection;
5 form.

6 THE WITNESS: I don't think that
7 the illustration of Figure 1 necessarily shows
8 rank multiplication. If I'm reading from
9 Column 6 of the '215 beginning at line 30 -- no,
10 not line 30, sorry.

11 Yes, I'm sorry. Reading '215
12 starting Column 6, line 30:

13 "In certain embodiments, the
14 plurality of memory devices 30 are
15 arranged in a first number of ranks.
16 For example, in certain embodiments,
17 the memory devices 30 are arranged
18 in two ranks, schematically
19 illustrated in Figure 1. In other
20 embodiments, memory devices are
21 arranged in four ranks."

22 So that limited description of
23 Figure 1 does not imply that the number of ranks
24 is different. And under that portion of
25 Column 6, you would understand that there are

1 more than one chip-selects coming into --
2 potentially, at least, into circuit 40.

3 BY ATTORNEY CHANDLER:

4 Q. I understand that there may be
5 more than one chip-select being input to
6 circuit 40.

7 My question is: Circuit 40 in
8 Figure 1 doubles the number of chip-selects;
9 right?

10 ATTORNEY WARRICK: Objection;
11 form.

12 THE WITNESS: I don't think that
13 the embodiment of Figure 1 is necessarily
14 performing rank multiplication, since elsewhere
15 it said that only in certain embodiments are we
16 having rank multiplication and that the
17 embodiment of Figure 1 is not limited to that
18 circumstance.

19 And so it does not necessarily
20 change the number of chip-selects.

21 BY ATTORNEY CHANDLER:

22 Q. And I'm focused on the discussion
23 in Column 23 of the '417 patent and Column 21 of
24 the '215 patent where circuit 40, as we
25 discussed earlier, does perform rank

1 multiplication using translation logic based on
2 the density transition bit. And what I'm trying
3 to understand from you is: How does that work?

4 ATTORNEY WARRICK: Objection;
5 form.

6 THE WITNESS: In the embodiments
7 that include a circuit 40 that include -- or
8 that implement rank multiplication, there would
9 be a change -- let me start again. My
10 apologies.

11 In at least some embodiments that
12 implement rank multiplication that include a
13 circuit 40, there would be a change in the
14 number of chip-selects, as the address
15 translation is performed to implement the
16 address -- the rank multiplication. I don't
17 believe that all implementations -- all
18 embodiments involving a circuit 40 necessarily
19 include that feature.

20 BY ATTORNEY CHANDLER:

21 Q. And when you say "that feature,"
22 you're referring to rank multiplication?

23 A. Yes, I am.

24 Q. All right. Sticking with the
25 embodiment of circuit 40, as shown, for example,

1 in Figure 1 of the '417 and '215 patents where
2 there is translation logic for performing rank
3 multiplication, what are the necessary inputs?
4 How does the logic work, and then what's the
5 output?

6 ATTORNEY WARRICK: Objection;
7 form.

8 THE WITNESS: Well, the
9 implementation of rank multiplication in all of
10 the embodiments of these patents span a variety
11 of different implementations depending on which
12 density transition they're talking about, as
13 articulated in Tables 3 and 4 of the
14 specifications.

15 Yeah, 3A, 3B and 4.

16 And so, for example, in the
17 embodiment of Figure 10A there's a change in the
18 row address bits but not of the chip-select
19 bits. And Figure 10B illustrates exactly how
20 that is going to be affected.

21 And then there are other
22 implementations described in subsequent figures.
23 So it's hard to summarize all of the inputs and
24 all of the outputs for the rank multiplication
25 because it varies according to the density

1 transition being considered.

2 BY ATTORNEY CHANDLER:

3 Q. I was asking about Figure 1 in
4 the embodiment of circuit 40 where the
5 translation logic performs rank multiplication
6 using the density transition bit.

7 And in Figure 1 there's twice the
8 number of chip-select signals coming out of
9 circuit 40 as coming in. And I'm trying to
10 understand from you how that works: What are
11 the necessary inputs to the translation logic,
12 what does the translation logic do to perform
13 rank multiplication, and then what are the
14 outputs?

15 ATTORNEY WARRICK: Objection;
16 form.

17 THE WITNESS: I don't believe
18 that the Figure 1 shows only rank multiplication
19 embodiments. It's a generic figure that is
20 applicable to many embodiments within the
21 specification.

22 One of the embodiments that I
23 talked about that conforms to the general rubric
24 of Figure 1, which is exemplified -- explained
25 in more detail with regard to Figure 10, has no

1 change in the number of chip-selects.

2 Others would necessarily have a
3 change in the number of chip-selects depending
4 on the address -- the density transition that's
5 being manipulated and what the density
6 transition bit is for that indication -- for
7 that particular transition. Again, it varies
8 depending on the embodiments.

9 And, for example, if we look at
10 Column 25 of the '215, it refers to an
11 embodiment with a circuit 40, one particular
12 circuit 40, where there is a piece of Varilog
13 code that's quite long that implements, in part,
14 the memory density multiplication from
15 256 megabytes to 512 megabytes of a DDR2 SDRAM
16 device, and it describes how the CAS signals are
17 changed.

18 We can go through that Varilog
19 line by line if you want. I'm not sure that
20 would be productive.

21 BY ATTORNEY CHANDLER:

22 Q. In the embodiment of circuit 40
23 in Figure 1 of the '417 and '215 patents, where
24 circuit 40 is using translation logic to perform
25 rank multiplication, is an example of rank

1 multiplication where there is one chip-select
2 signal coming in to circuit 40 and two
3 chip-selects coming out? Would that be an
4 example of rank multiplication?

5 ATTORNEY WARRICK: Objection;
6 form.

7 THE WITNESS: So to be clear,
8 circuit 40 is indicative of a wide variety of
9 different implementations, some of which do rank
10 multiplication, some of which do not.

11 For example, in Figures 3 and
12 4 --

13 BY ATTORNEY CHANDLER:

14 Q. But to be clear, I'm focusing on
15 the embodiment where circuit 40 does perform
16 rank multiplication.

17 I understand your point that
18 circuit 40 in other embodiments doesn't. But as
19 I think I've been clear, but I just want to make
20 clear, let's focus on the embodiment of
21 circuit 40 that is performing rank
22 multiplication. Understood?

23 A. Okay. So as long as we are
24 stipulating that the circuit 40 embodies many --
25 includes many embodiments, some of which do rank

1 multiplication and some of which do not.

2 Given that stipulation, the --
3 where there is a change in the number of
4 chip-selects as a result of rank multiplication,
5 the new chip-selects would be determined based
6 on the row and bank address bits, or the density
7 transition bit, in particular, for the density
8 transition being implemented in that embodiment.

9 Q. In that embodiment, does the
10 translation logic of circuit 40 generate
11 additional chip-select signals based on the
12 density transition bit which is either the
13 address signal or the bank address signal?

14 ATTORNEY WARRICK: Objection
15 form.

16 THE WITNESS: Yes, according to
17 Table 3B, which enumerates the JEDEC
18 standardized densities for the DDR2 SDRAMs, it
19 indicates that, from one density to another, we
20 have either a change in the number of row
21 address bits or the number of bank address bits;
22 and according to Table 4, it indicates which
23 bits, in particular, are significant with regard
24 to the change in density, and those are the ones
25 that would be utilized in implementing rank

1 multiplication in those specific embodiments.

2 BY ATTORNEY CHANDLER:

3 Q. Turning back to the same
4 paragraph that we've been focused on for a
5 little bit now, which is Column 23 of the '417
6 patent starting at line 22, and Column 21 of the
7 '215 patent starting at line 8.

8 The '417 and '215 patents teach,
9 in the next sentence, that the translation logic
10 equations of certain embodiments vary depending
11 on the type of memory module 10 -- for example,
12 UDIMM, RDIMM, FB-DIMM, et cetera; correct?

13 ATTORNEY WARRICK: Objection;
14 form.

15 THE WITNESS: So reading from
16 Column 23, starting at line 29, the text of the
17 specification is:

18 "In addition, the translation
19 logic equations of certain
20 embodiments vary depending on the
21 type of memory module 10 (e.g.,
22 UDIMM, RDIMM, FB-DIMM, et cetera.)"

23 BY ATTORNEY CHANDLER:

24 Q. And as we discussed earlier, the
25 '417 and '215 patents are not limited to

1 particular types of memory modules; correct?

2 ATTORNEY WARRICK: Objection;
3 form.

4 THE WITNESS: Yes, we did have
5 questions and answers about that earlier.

6 BY ATTORNEY CHANDLER:

7 Q. And at the time of the '417 and
8 '215 patents, Rambus-style memory modules were
9 known to a person of ordinary skill in the art;
10 correct?

11 A. Yes. We addressed that question
12 yesterday.

13 Q. And nothing in the '417 and '215
14 patents says that the claimed inventions do not
15 work with memory modules that use a Rambus-style
16 protocol to communicate with the host computer;
17 right?

18 ATTORNEY WARRICK: Objection;
19 form.

20 THE WITNESS: Well, certainly the
21 concept of rank multiplication doesn't work
22 within a Rambus-style -- for example,
23 specifically a direct Rambus-style memory
24 module, since there's no memory controller -- no
25 buffer or translation circuitry on such a module

1 to effect a rank multiplication even if you
2 wanted to do that.

3 There's no -- the way that the
4 direct Rambus channel is architected, there's no
5 advantage to trying to fool the memory
6 controller into thinking it's got one density
7 when it's actually got a different density under
8 its control.

9 BY ATTORNEY CHANDLER:

10 Q. But let me make sure I understand
11 what you're saying, because I thought the
12 benefit of rank multiplication is that sometimes
13 lower-density memory devices could be a lot
14 cheaper than higher-density memory devices.

15 So far am I correct there?

16 A. The premise of rank
17 multiplication is that sometimes the cost per
18 bit of a lower-density device is, for a period
19 of time, lower than the cost per bit of a
20 higher-density design; yes.

21 In a direct Rambus-style memory
22 system, you just go ahead and use the
23 lower-density devices. There's no need to fool
24 the memory controller into thinking that they
25 are higher-density devices under its control.

1 There's no advantage to doing that.

2 Q. Hold on. You're assuming that
3 it's a Rambus memory system with Rambus memory
4 devices.

5 Let's focus on the reality of the
6 time frame, which is, in 2004 and 2005, as we
7 discussed earlier, the most popular types of
8 memory devices were DDR memory devices; correct?

9 A. In that time frame, that's true.

10 Q. So does the invention of the '417
11 and '215 patent exclude the possibility of a
12 memory module with low-density DDR memory
13 devices, that includes a circuit 40 translation
14 logic for performing rank multiplication,
15 connected to a Rambus-style communication
16 protocol to the host computer?

17 ATTORNEY WARRICK: Objection;
18 form.

19 BY ATTORNEY CHANDLER:

20 Q. Is there anything in the '417 and
21 '215 patent that says our invention doesn't work
22 with that?

23 ATTORNEY WARRICK: Objection;
24 form.

25 THE WITNESS: There's nothing in

1 the '417 patent that I'm aware of that would
2 suggest to a POSITA that that sort of hybrid
3 system would make sense with the assumption that
4 you're trying to fool the memory controller into
5 believing that it's controlling a different type
6 of memory than it actually is, regardless of --

7 When you say that it's connected
8 over a direct Rambus-style interface with a
9 direct -- an actual direct Rambus channel and
10 its protocol, there is any motivation for doing
11 the rank multiplication that's described within
12 the '417 vanishes.

13 So the hypothetical embodiment
14 that you're suggesting would not make any sense
15 to a POSITA.

16 BY ATTORNEY CHANDLER:

17 Q. The '417 and '215 patents teach
18 performing rank multiplication with an
19 FB-DIMM-type memory module; correct?

20 ATTORNEY WARRICK: Objection;
21 form.

22 THE WITNESS: I'm sorry. Repeat
23 your question, please.

24 BY ATTORNEY CHANDLER:

25 Q. The '417 and '215 patents teach

1 performing rank multiplication with an
2 FB-DIMM-type memory module; correct? As an
3 example.

4 ATTORNEY WARRICK: Objection to
5 form.

6 THE WITNESS: Is there -- is
7 there a particular portion of the specification
8 that teaches that that you would like me to
9 read?

10 BY ATTORNEY CHANDLER:

11 Q. The same one that we've been
12 looking at, which is Column 23, of the '417
13 patent starting at paragraph around line 22, and
14 then the '215 patent Column 21 paragraph
15 starting on line -- around line 8.

16 A. So yes, FB-DIMMs are listed in
17 that list of module types at line 32 of
18 Column 23 of the '417.

19 There are no specifics or more
20 elaborated embodiments that are specifically
21 related to FB-DIMMs that I'm aware of.

22 Q. But nothing in the '417 and '215
23 patent says don't perform rank multiplication
24 with an FB-DIMM. To the contrary, the '417 and
25 '215 patents specifically list FB-DIMM as a

1 memory module that's compatible with the
2 disclosed inventions; correct?

3 ATTORNEY WARRICK: Objection;
4 form.

5 THE WITNESS: There is the
6 implication that, within the context of an
7 FB-DIMM -- i.e., with an FB-DIMM channel in and
8 memory devices organized on that channel -- can
9 be -- can make use of the address -- the
10 translation logic equations that it's talking
11 about throughout the specification.

12 BY ATTORNEY CHANDLER:

13 Q. Could we turn to the Perego
14 reference marked as Exhibit 1071, which I
15 believe I put in the chat yesterday. If you
16 need it again in the chat, let me know.

17 A. It's still up.

18 Q. Have you reviewed Exhibit 1071,
19 the Perego reference?

20 A. Yes, I have.

21 Q. And did you review it thoroughly?

22 ATTORNEY WARRICK: Objection to
23 form.

24 (Interruption by the court reporter to
25 clarify the record.)

1 ATTORNEY CHANDLER: And I'm not
2 sure I heard the answer.

3 THE WITNESS: I said, "I believe
4 so."

5 BY ATTORNEY CHANDLER:

6 Q. Please turn to Figure 2A of the
7 Perego reference marked as Exhibit 1071, and let
8 me know when you're there.

9 A. I'm looking at Figure 2A of the
10 Perego reference.

11 Q. Figure 2A of the Perego reference
12 marked as Exhibit 1071 discloses a memory system
13 that was known in the prior art, as indicated
14 under the text Figure 2A; correct?

15 A. Yes, Figure 2A refers
16 specifically to an S-RIMM module, which was a
17 real proposal of Rambus in the time frame of the
18 DDR -- I'm sorry -- direct Rambus transition.

19 Q. Figure 2A of the Perego reference
20 marked as Exhibit 1071 shows multiple memory
21 modules where each module has synchronous DRAM
22 devices on it, as indicated on the upper right
23 of the figure; correct?

24 A. Yes. So this figure shows a
25 Rambus channel connecting three memory modules,

1 each of which have a memory translator hub, MTH,
2 on an S-RIMM module using synchronous DRAMs.

3 Q. And are synchronous DRAMs
4 sometimes referred to as "SDRAM" for short?

5 A. Yes. SDRAMs for short refer to,
6 as we've talked about at length, a plurality of
7 different standardized memory devices, as
8 dictated by JEDEC.

9 Q. And the SDRAM memory devices
10 shown in Figure 2A of the Perego reference
11 marked as Exhibit 1071, those are not what we
12 would refer to as Rambus memory devices;
13 correct?

14 A. Correct.

15 Q. Instead, as I think you said just
16 a moment ago, SDRAM memory devices were
17 standardized by JEDEC. And at this time frame,
18 DDR SDRAM memory devices were common; correct?

19 A. In our time frame of 2004-2005,
20 yes, the synchronous DRAMs were common.

21 Q. And specifically, the DDR SDRAMs
22 were common and had been standardized as of
23 2000; correct?

24 A. DDR SDRAMs were standardized
25 before 2004-2005, yes.

1 Q. And specifically, the first DDR
2 SDRAM standard was finalized in 2000, as shown,
3 for example, by Exhibit 1060; and then the DDR2
4 standard was finalized by 2003, as shown, for
5 example, by Exhibit 1064; correct?

6 A. Yes. The original DDR SDRAM
7 is -- yes, June of 2000 is the date on the cover
8 of that, as you said.

9 Q. In Figure 2A of the Perego
10 reference marked as Exhibit 1071, the memory
11 modules are connected to a Rambus channel, even
12 though the memory devices are not Rambus memory
13 devices, they're SDRAM memory devices,
14 standardized by JEDEC; correct?

15 A. Yes, a I described a couple of
16 questions ago, Figure 2A shows a Rambus channel
17 connecting three modules, each of which has a
18 memory translator hub, MTH, controlling a rank
19 of synchronous DRAMs, which could be understood
20 by a POSITA to be the DDR-type, but not
21 necessarily.

22 Q. I apologize. There's some
23 gardening tools or something outside my window.
24 Is it -- and I never know if it gets picked up
25 by the microphone.

1 Do you hear it or is it making me
2 cut out?

3 A. It's -- I'm not hearing it, but
4 you are cutting out a bit. Maybe we can a short
5 break now and resume after they've moved on.

6 ATTORNEY CHANDLER: Yeah, why
7 don't we go ahead and do that.

8 ATTORNEY WARRICK: Okay.

9 ATTORNEY CHANDLER: Thanks.

10 THE VIDEOGRAPHER: Off the record
11 at 9:35 a.m. Pacific Time.

12 (Recess taken from 9:35 a.m. to
13 9:52 a.m.)

14 THE VIDEOGRAPHER: On the record
15 at 9:52 a.m. Pacific Time.

16 BY ATTORNEY CHANDLER:

17 Q. Please turn to Column 10 of the
18 Perego reference marked as Exhibit 1071, and
19 look at the paragraph starting around line 54.
20 Let me know when you're there.

21 A. I'm on Column 10.

22 Q. Down in the bottom right line,
23 54?

24 A. Yes.

25 Q. The Perego marked as Exhibit 1071

1 discloses embodiments using SDRAM and DDR2;
2 correct?

3 A. What Column 10, starting at line
4 54 says is that:

5 "In one embodiment, memory
6 devices 410a through 410h are Rambus
7 DRAMs, operating at a data rate of
8 1066 megabits per second. Other
9 memory devices may be implemented on
10 module 400, for example
11 double-data-rate 2 (DDR2) DRAM
12 devices and synchronous DRAM (SDRAM)
13 devices."

14 Q. And so if you turn to Figure 4 of
15 Perego, Figures 4A and 4B, Perego is teaching,
16 in the paragraph that we just looked at, that
17 those memory devices, in Figures 4A, 4B and 4C
18 could be Rambus memory devices or they could be
19 DDR2 memory devices.

20 Is that fair?

21 ATTORNEY WARRICK: Objection;
22 form.

23 THE WITNESS: What I interpret
24 the Figure 4, in its three subfigures in
25 conjunction with that paragraph we just read, is

1 that the modules depicted in 4A, 4B and 4C use a
2 Rambus-style -- a direct Rambus channel for each
3 of 405 -- I'm sorry -- 415a through -- a and b
4 in the case of Figure 4A; and, therefore, those
5 memory devices in that illustration are direct
6 Rambus RDRAMs.

7 The subsequent sentence of that
8 paragraph in Column 10 indicates that you could
9 build a device like this with SDRAMs but it
10 wouldn't be this exact device.

11 BY ATTORNEY CHANDLER:

12 Q. And then the paragraph that we're
13 looking at, at the bottom of Column 10 of the
14 Perego reference marked as Exhibit 1071,
15 indicates, at the very bottom of Column 10, that
16 buffer device 405 can translate protocols
17 employed by controller 310 to the protocol
18 utilized in a particular memory device
19 implementation, which, as we discussed, may be a
20 Rambus memory device or may be a DDR2 memory
21 device.

22 Is that fair?

23 A. So reading continuing from where
24 I left off, says as you say:

25 "Utilizing buffer device 405

1 between the memory devices and the
2 controller in accordance with the
3 present invention may feasibly
4 render the type of memory device
5 transparent to the system.

6 Different types of memory devices
7 may be included on different modules
8 within a memory system by employing
9 memory buffer device 405 to
10 translate protocols employed by the
11 controller and the protocols
12 utilized by the particular memory
13 device implementations."

14 So, yes, this idea that the
15 buffered device on the modules can translate
16 protocols and provide for a unique level of
17 multi-device-type flexibility within a single
18 memory system is -- is unique and important.

19 Q. I don't know what you have in
20 front of you right now, but I want to look at
21 Figure 4B, and then I also want to talk about --
22 a little further up in Column 10. So maybe just
23 look at Figure 4B and then turn back to
24 Column 10 and let me know when you're ready.

25 A. Okay.

1 So I've looked at Figure 4B. It
2 shows a module 450 that has a buffer 405 and
3 four direct Rambus channels, and a total of 16
4 Rambus -- direct Rambus RDRAMs, all connected to
5 a Rambus -- a direct Rambus channel at the
6 bottom.

7 So turning back, as you asked,
8 to Column 10. I'm now ready to consider
9 Column 10.

10 Q. Column 10 of the Perego reference
11 marked as Exhibit 1071, starting around line 22,
12 talks about Figure 4B; correct?

13 A. Yes. Starting at line 22 it
14 says, "Figure 4B illustrates a quad-channel
15 module 450 with channels 415a to 415d."

16 Q. So Figure 4B of the Perego
17 reference marked as Exhibit 1071 shows the
18 buffer 405 communicating with the memory devices
19 via four channels labeled 415a, 415b, 415c and
20 415d; correct?

21 A. Yes. 415a through 415d are
22 Rambus-style channels, RDRAM -- direct RDRAM
23 channels.

24 Q. And then Column 10 of the Perego
25 reference marked as Exhibit 1071, a little bit

1 below line 22 goes onto explain that the
2 channels in Figure 4B may operate in pairs;
3 correct?

4 A. Are you referring to the text at
5 line 31 in particular, or is there something
6 else you want me to look at?

7 Q. It's a little bit further up,
8 around line 25 where -- I mean, it is -- it is
9 related to that. But it indicates 415c and 415d
10 can be routed in parallel with 415a and 415b.
11 And then, as you say down in 31 and -- lines 31
12 and 32 of Column 10, there's a discussion that
13 channels 415a and 415b may operate
14 simultaneously with 415c and 415d.

15 A. Yes. So to read it in its
16 entirety, starting at line 32, it says:

17 "In alternative embodiments,
18 channels 415a and 415b may operate
19 simultaneously with channels 415c
20 and 415d to realize greater
21 bandwidth."

22 Q. So does Perego marked as
23 Exhibit 1071 teach that in Figure 4B, that one
24 embodiment is you have four separate independent
25 channels; another embodiment is two channels

1 working together at a given time; and then a
2 third embodiment is all four channels working
3 together at the same time?

4 Is that a fair understanding of
5 what Perego is disclosing in Column 10 of
6 Exhibit 1071?

7 ATTORNEY WARRICK: Objection;
8 form.

9 THE WITNESS: The principal
10 motivation for the structure of Figure 4B is
11 given in terms of capacity and the number of
12 memory devices that's articulated in lines 26
13 through 31 of Column 10.

14 It also subsequently talks about
15 operating pairs of channels together, or pairs
16 of pairs operating together.

17 BY ATTORNEY CHANDLER:

18 Q. I'm a little unclear if you're
19 agreeing or disagreeing with --

20 A. I'm just reading the text of the
21 patent.

22 I'm not seeing any reference to
23 an embodiment in which there are two channels
24 415a and 415d, where those are operating
25 independently. But if you have such a

1 citation --

2 Q. I thought I heard you say a and d
3 like "dog"; whereas, I think my question was a
4 and b like "boy."

5 A. I meant -- I meant to say b like
6 "boy."

7 I'm not reading anything that
8 suggests that 415a and 415b, where they both
9 exist on the module, operating independently,
10 that they are essentially two halves of one
11 pair. But if there's some -- if I've missed
12 something, then please point me to it.

13 Q. Well, there's Figure 4B, there's
14 Column 10 that we've been looking at, and
15 there's knowledge of person of ordinary skill in
16 the art.

17 And what I'm trying to understand
18 is: Is your opinion that Figure 415b is limited
19 to only a certain use of the four channels; or
20 does Column 10, along with the knowledge of a
21 person of ordinary skill in the art, teach that
22 those four channels may be used independently;
23 or alternatively, in a different embodiment, may
24 be used simultaneously?

25 ATTORNEY WARRICK: Objection;

1 form.

2 THE WITNESS: My interpretation
3 of the disclosure of Column 10 vis-a-vis
4 Figures -- 4B in particular, is that when there
5 are four channels, they operate all together to
6 provide greater bandwidth. And that's why you
7 have multiple channels, as opposed to more
8 devices on a single channel, or a pair of
9 channels 415a and 415b.

10 So there is both the advantage of
11 increased capacity beyond what a single pair of
12 direct Rambus channels can support; and in
13 additionally, there is the advantage of
14 simultaneous operation, per line 31, 32 of
15 Column 10.

16 BY ATTORNEY CHANDLER:

17 Q. I want to make sure I understand.

18 At one extreme in implementation
19 of Figure 4B there could just be one memory
20 device with one channel dedicated to that memory
21 device.

22 Is that fair? It's taught, for
23 example, at Column 10, line 18 or so?

24 ATTORNEY WARRICK: Objection;
25 form.

1 THE WITNESS: Yes, Column 15 and
2 16 of Column 10, referring to Figure 4A, says
3 that you can have a single channel 415a, or it
4 can be organized as a pair of channels 415a and
5 415b.

6 BY ATTORNEY CHANDLER:

7 Q. And then are you limited to --
8 going in the other direction, are you limited to
9 just the pair of channels 415a or 415b, or can
10 you actually have four channels all working
11 together?

12 A. With regard to the embodiment
13 depicted in Figure 4B, there are four channels
14 that are working together, at least in that
15 alternative embodiment, yes.

16 Q. And the Perego reference marked
17 as Exhibit 1071 teaches that the memory devices
18 in Figures 4A, 4B, 4C may be DDR2 memory
19 devices; correct?

20 ATTORNEY WARRICK: Objection;
21 form.

22 THE WITNESS: No. It's saying
23 that you could design something comparable to
24 the embodiments of Figure 4A through 4C that use
25 DDR SDRAMs.

1 But the memory -- the buffer
2 device would have to be different. The signal
3 names would be different. The signal topologies
4 would be different. There would be little in
5 common between such a -- the actual -- the
6 depiction of Figures 4A and 4B to a comparable
7 device with a different buffer circuit that
8 provide -- that interfaces with double-data-rate
9 DDR2 SDRAMs.

10 BY ATTORNEY CHANDLER:

11 Q. But the Perego reference marked
12 as Exhibit 1071, you agree, does disclose an
13 embodiment where the memory module has memory
14 devices that are DDR memory devices; correct?

15 ATTORNEY WARRICK: Objection;
16 form.

17 THE WITNESS: Yes, the disclosure
18 at the bottom of Column 10 says that although
19 the depicted devices 410a through 410h are
20 direct Rambus memory devices, you could build
21 something comparable of the same general
22 structure with a memory translation buffer
23 device to translate the primary channel protocol
24 to a DDR2 SDRAM protocol in order to effect a
25 plurality of memory types within a single memory

1 system.

2 BY ATTORNEY CHANDLER:

3 Q. Okay. I want to ask about a
4 different aspect of Perego, so to avoid
5 confusion, I'm not going to be talking about the
6 memory devices. Instead, I want to talk about
7 the communications between the memory module and
8 the host computer.

9 Do you understand what I'm
10 focused on now?

11 A. Yes. That generally goes by the
12 name of "the primary channel and the protocol
13 thereon," within the disclosure of Perego.

14 Q. In your opinion, can the memory
15 modules disclosed by Perego in Exhibit 1071 be
16 used with the host computer that uses a
17 JEDEC-style bus for address control and data
18 signals between the host computer and the memory
19 module?

20 ATTORNEY WARRICK: Objection;
21 form.

22 THE WITNESS: Perego discloses a
23 principal embodiment of a point-to-point link
24 between the memory controller and the memory
25 modules such that there's a single module at the

1 end of each point-to-point link.

2 It also discloses some details
3 about how that primary channel in a
4 point-to-point configuration can be effected,
5 either multiplexed or not.

6 It also discusses, in a couple of
7 places, the potential of using a bus structure
8 instead of a point-to-point structure, and that
9 would be something similar to the embodiment of
10 Figure 2A.

11 But in no case is there an
12 implication that it's a JEDEC-style, as you say,
13 not conforming with any JEDEC standard, as the
14 implementation of the primary channel that I'm
15 aware of.

16 BY ATTORNEY CHANDLER:

17 Q. So to be clear, your opinion is
18 that the Perego reference marked as Exhibit 1071
19 never disclosed any memory module that
20 communicates with the host computer using a
21 JEDEC-style bus for address control and data
22 signals going between the host computer and the
23 memory module.

24 Is that fair?

25 A. Is there something that you want

1 to point me to within Perego that would suggest
2 that?

3 Q. No, I want your opinion.

4 A. So far we've looked at the bottom
5 portion of Column 10, which talks about the
6 memory devices being consistent with the use of
7 JEDEC-style -- JEDEC standardized memory
8 devices. I've talked a bit about the range of
9 embodiments of the primary channel.

10 I've not talked at all about the
11 use of a JEDEC standardized primary channel.

12 Q. So in informing your opinions in
13 your declaration marked as Exhibit 2024, you did
14 not talk about or form any opinions on the
15 assumption that the Perego reference marked as
16 Exhibit 1071 discloses a primary channel that's
17 a JEDEC-style bus, meaning that the address data
18 control signals between the host computer and
19 the memory module would be a JEDEC-style bus.

20 Is that fair?

21 ATTORNEY WARRICK: Objection;
22 form.

23 THE WITNESS: What exactly do you
24 mean by "a JEDEC-style bus"?

25 ///

1 BY ATTORNEY CHANDLER:

2 Q. Well, I was trying to use your
3 language. But what was the term that you were
4 using to refer to the communications between the
5 host computer and the memory module that comply
6 with the JEDEC standard?

7 A. I believe I used the phrase
8 "JEDEC standardized primary channel," but the
9 court reporter could confirm that, perhaps.

10 Q. Do you understand -- when I say
11 "JEDEC-style bus" to refer to address signals,
12 control signals and data signals going between
13 the host computer and the memory module, is that
14 understandable to you?

15 A. For me, "JEDEC-style" would
16 include more than just that. Those three
17 elements being separate is not restricted to
18 JEDEC standardized devices or modules.

19 So when you use "JEDEC-style,"
20 there's more baggage that goes along with that
21 terminology than just the separation of address
22 control and data.

23 Q. Can you explain that a little bit
24 more, what you're trying to say.

25 A. Well, if you look at the JEDEC

1 standardized modules that used DDR2 SDRAMs, for
2 example, there is a lot to the standard of the
3 module and the constituent SDRAMs that make it
4 JEDEC-style, in my view.

5 For example, the use of DQS
6 signals, the use of chip-select signals and so
7 forth, the ODT functionality, all of the
8 features that are within those standards that
9 make for a complete embodiment and useable
10 memory module, all of that comes along with the
11 moniker of "JEDEC-style."

12 So I think it's much more than
13 just the multiplexing or the non-multiplexing of
14 address control and data.

15 Q. Okay. So with that understanding
16 of "JEDEC-style bus," the first question, just
17 to be clear, is: At the time of Perego,
18 JEDEC-style buses were known; correct?

19 A. Correct. As defined then, yes.

20 Q. And in your expert opinion marked
21 as Exhibit 2024, you base your opinions on the
22 assumption that the Perego reference marked as
23 Exhibit 1071 does not disclose memory modules
24 that communicate with the host computer using a
25 JEDEC-style bus; correct?

1 ATTORNEY WARRICK: Objection;
2 form.

3 THE WITNESS: Given the
4 understanding of "JEDEC-style bus," as we've
5 just agreed to, involving more than just
6 demultiplexing address data and control, it's --
7 I want to review my declaration, but it's my
8 understanding, before I do so, that I'm not
9 aware of any embodiments of Perego that use a
10 JEDEC-style primary channel.

11 BY ATTORNEY CHANDLER:

12 Q. And when you say "primary
13 channel," you're referring to the communications
14 between the memory module and the host computer?

15 A. Yes, that's the -- using "primary
16 channel" to refer to that communication path as
17 it's used in Perego.

18 Q. In your opinions in your
19 declaration marked as Exhibit 2024, you
20 concluded that the memory modules disclosed by
21 Perego would use a Rambus protocol for
22 communications between the memory module and the
23 host computer, which I understand you refer to
24 as "the primary channel"; is that correct?

25 ATTORNEY WARRICK: Objection;

1 form.

2 THE WITNESS: There are certainly
3 specific embodiments within Perego -- for
4 example, the embodiments of Figures 4A, B and C,
5 where the channel is, through the signal names,
6 indicated to be a direct Rambus channel.

7 For other embodiments, such as
8 those of -- let's see.

9 So the embodiments that utilize
10 the buffer of Figure 5B with its configurable
11 width interface, a POSITA would recognize that
12 as referring to an XDR-style memory module --
13 sorry primary channel that incorporates that
14 variable width capacity or feature.

15 BY ATTORNEY CHANDLER:

16 Q. And your opinion is that
17 Figure 5B of Perego and Figures 4A through C of
18 Perego marked as Exhibit 1071 do not use a
19 primary channel that's a JEDEC-style bus for
20 communications between the host computer and the
21 memory module; correct?

22 A. That is -- I believe that is what
23 I said, yes.

24 Q. And that was the understanding
25 that you used in forming your opinions in your

1 expert declarations, marked as Exhibit 2024?

2 A. In part, yes. Obviously, I
3 relied on a lot of stuff in forming my opinions,
4 but that's one aspect of it.

5 Q. Please pull up the Ellsberry
6 reference marked as Exhibit 1073.

7 A. Yes, I'm looking at 1073.

8 Q. And have you reviewed the
9 Ellsberry referenced marked as Exhibit 1073 in
10 both IPRs?

11 A. Not in detail recently; but
12 previously, for preparing the declaration, I
13 have.

14 Q. So, for example, in paragraph 199
15 of your expert declaration, marked as
16 Exhibit 2024 in the '417 IPR, you referred to
17 Ellsberry; and the corresponding cite for the
18 other expert declaration is paragraph 204.

19 A. 199 of the '417, is that what you
20 said?

21 Q. Yeah, and paragraph 204 of the
22 '215 declaration marked as Exhibit 2024.

23 A. Let me read that paragraph to
24 refresh my memory.

25 (Witness reviews document.)

1 Is there a question pending?

2 Q. Are you ready to proceed?

3 A. Yes.

4 Q. In your opinion, Figure 10 of the
5 Ellsberry discloses a x8 module of fixed width
6 and singular memory type with two ranks;
7 correct?

8 A. That's what I say in Figure -- in
9 paragraph 199.

10 You could view Figure 10 as also
11 showing a part of a wider module, as shown, for
12 example, in Figure 5 of Perego. I don't
13 believe -- I'd have to look at the text with
14 regard to Figure 10 to confirm that, but I can
15 do that if you would like.

16 Q. But in your opinion, Figure 10 of
17 Ellsberry discloses an embodiment of a x8
18 module -- which is to say an 8-bit-wide
19 module -- with two ranks; correct?

20 I think I understood you to say
21 just a moment ago that Figure 10 is also
22 compatible with other types of modules. But
23 focusing on the example you're discussing here
24 in your expert declaration marked as
25 Exhibit 2024, your opinion is that Figure 10 of

1 Ellsberry discloses an embodiment of a x8
2 module, which is to say an 8-bit-wide module,
3 with two ranks; is that correct?

4 A. I'm just reviewing the text of
5 Ellsberry vis-a-vis Figure 10, so give me a
6 second.

7 (Witness reviews document.)

8 Do you know where in Ellsberry
9 it talks about Figure 10 in particular?

10 Q. Well, you cite to paragraph 53 of
11 Exhibit 1073.

12 A. Okay, let me look at 53. Yes,
13 that's ...

14 That seems to be the only
15 reference to Figure 10 within the specification
16 of Ellsberry.

17 (Witness reviews document.)

18 Q. Are you waiting for me?

19 A. No, I'm trying to find additional
20 insight in Ellsberry for the disclosure of
21 Figure 10.

22 There is a reference to it in
23 paragraph 21 that refers to Figures 10, 11, 12
24 and 13 as illustrating different configurations
25 of memory modules, e.g., DIMMs.

1 A POSITA reading that would
2 understand that there's two ways to interpret
3 Figure 10, either as an 8-bit-wide module, which
4 doesn't make a lot of sense in the time frame
5 we're talking about, or as a portion of a wider
6 structure. Typically -- DIMMs are typically 64
7 bits wide, so a POSITA might view it either way.

8 Q. All right. Let's stick with the
9 way disclosed in your expert declaration marked
10 as Exhibit 2024, which is that Figure 10 of
11 Ellsberry discloses an 8-bit-wide memory module
12 with two ranks.

13 Understood?

14 A. Technically, that's all that's
15 visible within Figure 10, yes.

16 Q. In that embodiment of Figure 10
17 of the Ellsberry reference marked as Exhibit
18 1073, the two ranks are denoted as 1006 and
19 1008; is that correct?

20 A. In paragraph 53 of Ellsberry, it
21 calls them banks, not ranks.

22 But other than that, yes, it --
23 the exact term -- language of paragraph 53 is:

24 "Figure 10 illustrates a
25 single chip-select memory

1 configuration in which one control
2 unit 1002 and one bank switch 1004
3 are used to control two memory banks
4 1006 and 1008, each memory bank
5 having two memory devices 1010 and
6 1012 in separate data buses 1014 and
7 1016."

8 Q. The two ranks that you were
9 referring to in your expert declaration marked
10 as Exhibit 2024 are those identified as 1006 and
11 1008 in Figure 10 of the Ellsberry reference
12 marked as Exhibit 1073; correct?

13 A. Yes, which Ellsberry refers to as
14 "banks."

15 Q. And on that issue of banks versus
16 ranks, you understand that there was a change in
17 terminology where originally the word "banks"
18 with a B was used more broadly to refer to
19 different types of things, one of which we now
20 more commonly refer to as rank with an R;
21 correct?

22 ATTORNEY WARRICK: Objection;
23 form.

24 THE WITNESS: Yes, I am familiar
25 with the transition of the terminology from

1 "banks" to "ranks," since I initiated it.

2 BY ATTORNEY CHANDLER:

3 Q. And in what year did you initiate
4 it?

5 A. The -- it was in the 1996 time
6 frame. We looked at my "New DRAM Technologies"
7 report yesterday. It was in the creation of
8 that report that I recognized the need for a new
9 term, and I started using it in my talks and
10 writings. And it was, over time, accepted and
11 propagated through the industry, although
12 clearly, as far as Ellsberry is concerned, they
13 didn't quite get the message.

14 Q. Well, to be fair to Ellsberry, in
15 the original DDR SDRAM standard it uses the term
16 "bank with a B; and then it was in the next
17 version of the standard, the DDR2 standard, that
18 JEDEC at least transitioned to using the term
19 "rank" with an R; correct?

20 A. Yes. It took time for the
21 industry to recognize the value of having two
22 separate terms.

23 Q. But it's not just that it took
24 time for the industry; it's that the DDR
25 standard -- which still exists today, right? --

1 says "bank" with a B, and it used it in the way
2 that the DDR2 standard says "rank" with an R;
3 correct?

4 A. Yes, because it predated -- the
5 creation of the DDR standard predated the more
6 widely -- wider acceptance of the term "rank" to
7 mean what it does today.

8 Q. And the DDR -- the DDR standard
9 still exists? There are still DDR memory
10 devices; right?

11 A. You can still buy them and the
12 standard still is valid. They obviously -- not
13 in their interest to go back and change the
14 terminology of an existing standard. That would
15 just create confusion.

16 Q. So in fairness to Ellsberry, when
17 Ellsberry wrote "bank" with a B, that was the
18 terminology that was correctly used in the DDR
19 standard.

20 Now, Ellsberry also refers to
21 DDR2. In that context, "rank" with an R would
22 be the terminology used, and a person of
23 ordinary skill in the art would understand all
24 of that; correct?

25 A. Yeah. A person of ordinary skill

1 in the art at the time of 2004-2005 would
2 appreciate that there are still references out
3 there that are using "bank" where more properly
4 "rank" might have been used.

5 Q. And this transition of
6 terminology from "bank" with a B to "rank" with
7 an R, that's discussed, for example, in the
8 Jacobs textbook that we looked at previously,
9 Exhibit 1070, on page 413; correct?

10 A. You want me to pull it up and
11 confirm that?

12 Q. Sure. Just look at it quickly.
13 I'm pretty sure he's talking about the same
14 thing you're talking about, but why don't you go
15 ahead and double-check.

16 A. What was the page number again?

17 Q. 413.

18 A. There we go, yeah, sorry. I was
19 on 14.

20 Yes, we discussed this
21 yesterday, and it is about the term "rank" and
22 how it's changed over -- from "bank" to "rank"
23 over time.

24 Q. And in the figure on page 413 of
25 Exhibit 1070 on the right-hand side, Jacob

1 crosses out "bank" and puts an arrow to "rank";
2 correct?

3 On the right-hand side, do you
4 see that big X over the word "bank"?

5 A. Yes, that is what he depicts in
6 the figure. He doesn't really describe what
7 he's doing there in the text, but that is
8 exactly what he has done in the figure, crossing
9 out the word "bank" and an arrow pointing to the
10 word "rank."

11 Q. So turning back to Figure 10 of
12 Ellsberry in Exhibit 1073, there are two
13 ranks -- using the term "rank" as we currently
14 understand it -- and those are identified as
15 1006 and 1008; correct?

16 A. My recollection is that Ellsberry
17 accesses one of its banks at a time. Each
18 transaction goes to one bank or the other bank,
19 and that would make them ranks. If I'm
20 incorrect about that, then they would together
21 be a single rank, per the normal usage of that
22 term.

23 But that's my understanding,
24 sitting here today.

25 Q. The two ranks that you were

1 referring to in your expert declaration marked
2 as Exhibit 2024 are 1006 and 1008 in Figure 10
3 of the Ellsberry reference marked as
4 Exhibit 1073; and we can see that 1006 gets
5 chip-select signal CS0A, and rank 1008 gets a
6 different chip-select signal, CS0B; correct?

7 A. Yes, that's what's shown in
8 Figure 10.

9 Q. And then Figure 10 of the in
10 Ellsberry reference marked as 1073 shows that
11 rank 1006 has a data bus 1016, and then rank
12 1008 has a different data bus 1014; correct?

13 A. Correct. They are two separate
14 data busses -- actually, 10 -- the arrows point
15 to the DQS of one half and the DQA of the other.
16 So let me double-check the text to see if it
17 clarifies.

18 I doubt -- it refers to -- in
19 figure -- I'm sorry -- in paragraph 53, that
20 data buses 1014 and 1016 come from the two banks
21 of memory devices 1010 and 1012.

22 Q. In Figure 10 of the Ellsberry
23 reference marked as Exhibit 1073, data bus 1016
24 is 8 bits wide and connected to switch ASIC
25 1004, and Exhibit 10 -- sorry -- data bus 1014

1 is also 8 bits wide and is also connected to the
2 switch ASIC 1004; correct?

3 A. Yes. The data buses include both
4 data signals and DQS signals in both cases, yes.

5 Q. And then in Figure 10 of the
6 Ellsberry reference marked as Exhibit 1073, on
7 the left side of the switch ASIC 1004 there's
8 another data bus that's only 8 bits wide;
9 correct?

10 A. Yes. The data bus on the left
11 side of the switch ASIC has a data bus that's
12 listed as a 8-bit-wide, DQ0 through 7, and DQS0
13 and DQS1. It's -- the data portion of that is
14 divided into two halves, because there are
15 separate DQS signals for the top and half
16 nibbles of that byte.

17 Q. And so in summary, in Figure 10
18 of the Ellsberry reference marked as Exhibit
19 1073, the switch ASIC 1004 has an 8-bit data bus
20 on the left side of the figure, but then on the
21 right side of the figure has got two separate
22 8-bit data buses; correct?

23 A. Yes, where the data buses include
24 DQs and DQs, yes.

25 It's been about an hour since

1 we've been going. Can we have another break,
2 please?

3 ATTORNEY CHANDLER: Sure, yeah.
4 Just a few minutes.

5 THE WITNESS: Okay.

6 THE VIDEOGRAPHER: I'm sorry,
7 Counsel. Did you want to break now?

8 ATTORNEY CHANDLER: Yeah, just
9 for a few minutes.

10 THE VIDEOGRAPHER: Off the record
11 at 10:47 a.m. Pacific Time.

12 (Recess taken from 10:47 a.m. to
13 10:54 a.m.)

14 THE VIDEOGRAPHER: On the record
15 at 10:54 a.m. Pacific Time.

16 BY ATTORNEY CHANDLER:

17 Q. Do you have Figure 10 of
18 Ellsberry marked as Exhibit 1073 in front you?

19 A. Yes, I do.

20 Q. Are you familiar with the concept
21 of a data collision?

22 A. Generally, yes.

23 Q. How would you explain what a data
24 collision is?

25 A. A data collision, generally

1 speaking, is when two drivers on a single wire
2 are trying to communicate simultaneously and,
3 thereby, neither of them getting their message
4 across.

5 Q. In Figure 10 of the Ellsberry
6 reference, marked as Exhibit 1073, if the switch
7 ASIC were to be operated incorrectly or unwisely
8 such that it were to receive read data from rank
9 1006 at the same time that it receives data from
10 rank 1008 and if it were to try to drive the
11 data from both 1006 and 1008 onto the data bus
12 to the left of switch ASIC 1040, is that an
13 example of something that could result in a data
14 collision?

15 ATTORNEY WARRICK: Objection;
16 form.

17 THE WITNESS: Well, first of all,
18 it would be the control unit ASIC that would be
19 misbehaving if that were to happen, not
20 necessarily the switch ASIC of Figure 10.

21 It's not really a data collision
22 in the same sense that I articulated it with two
23 drivers on a single wire. It's more of a matter
24 of -- there -- the switch ASIC being unable to
25 select both pieces of data simultaneously to

1 drive onto a single wire or bus on the other
2 side of its multiplexing function.

3 BY ATTORNEY CHANDLER:

4 Q. So if I understand you correctly,
5 in Figure 10 of the Ellsberry reference marked
6 as Exhibit 1073, the control ASIC on the bottom
7 left of the figure controls the switch ASIC on
8 the upper left of the figure; correct?

9 A. There is a connection between the
10 two shown, which a POSITA would understand to be
11 a -- how control information is sent from the
12 control units to the switch ASIC. A POSITA
13 might reasonably assume that that control tells
14 the switch ASIC which of the two data buses is
15 to be driven at a given point in time onto or
16 from the ASIC DQs on the other side.

17 So if there is an error here,
18 it's on the part of the control unit, and the
19 switch ASIC would just do what it's told:
20 Select one or the other, but it could not select
21 both at the same time, for obvious reasons.

22 Q. So to avoid a data collision in
23 Figure 10 of the Ellsberry reference marked as
24 Exhibit 1073, the control ASIC needs to send
25 control signals to the switch ASIC to operate

1 the switch ASIC in the proper manner to avoid a
2 data collision.

3 Is that fair?

4 ATTORNEY WARRICK: Objection to
5 form.

6 THE WITNESS: Again, I don't
7 think you're using "data collision" the same way
8 that I was, and I don't find that word within
9 Ellsberry. So it's -- I'm confused as to why
10 you continue to call this a data collision
11 scenario.

12 BY ATTORNEY CHANDLER:

13 Q. The switch ASIC in Ellsberry
14 receives a signal and then drives it out the
15 other side of the switch ASIC; correct?

16 A. That's a simplistic and narrow
17 view of what the switch ASIC does, but that's a
18 first step in describing its functionality.

19 Q. And in particular, sticking with
20 Figure 10 of the Ellsberry reference marked as
21 Exhibit 1073, the switch ASIC has a total of 16
22 DQ data lines coming into it and only 8 DQ data
23 lines going out of it, and each one of the 16 DQ
24 data lines coming into the switch ASIC has a
25 driver; correct?

1 ATTORNEY WARRICK: Objection;
2 form.

3 THE WITNESS: The drivers are on
4 the DRAMs or on the ASIC? I'm sorry, I didn't
5 follow your question.

6 BY ATTORNEY CHANDLER:

7 Q. Both.

8 So there's 16 DQ data lines
9 coming into the switch ASIC. Those signals are
10 driven by the DRAMs. But then once those 16
11 data signals are inside the switch ASIC, each
12 one of those 16 data lines has a driver ready
13 and able to drive that signal out to the left of
14 the switch ASIC, shown in Figure 10 of
15 Exhibit 1073; correct?

16 A. Yes. So wherever there is a data
17 flow on a signal wire, there is a driver to
18 effectuate that.

19 The fact that you have more DQs
20 on one side of the switch ASIC than on the other
21 means that either one or the other is used at a
22 time, sequentially, or there is some form of
23 frequency multiplication going on that allows
24 both to be interleaved within a single data
25 burst, as you see in the Halbert reference, for

1 example.

2 Q. But sticking with the Ellsberry
3 reference, Figure 10 of Exhibit 1073, if all 16
4 drivers in the switch ASIC were to drive data at
5 the same time onto the 8 data lines coming out
6 to the left of the switch ASIC, that would cause
7 a collision; right?

8 ATTORNEY WARRICK: Objection;
9 form.

10 THE WITNESS: It's -- that's an
11 inaccurate use of the word "collision" as it's
12 normally understood by a POSITA in that you
13 don't -- what you're describing is a -- the
14 inability of the switch ASIC to drive two bits
15 onto one line at the same time, which is
16 generally true although not universally true.

17 In this case, if both banks of
18 DRAMs are trying -- have been told to output
19 devices simultaneous -- I'm sorry -- have been
20 told by the control unit ASIC to output read
21 data at the same time towards the switch ASIC,
22 either the switch ASIC is going to ignore one of
23 the two or it has some mechanism for
24 interleaving the two temporally within the
25 burst. And that -- I don't see any -- not

1 sufficiently familiar with Ellsberry to say that
2 that's ruled out, but that's not how a normal
3 JEDEC-compliant DIMM would operate.

4 So it's not a data collision as
5 it is normally understood.

6 BY ATTORNEY CHANDLER:

7 Q. But the reason there's no data
8 collision in Figure 10 of the Ellsberry
9 reference marked as Exhibit 1073 is because the
10 control unit ASIC at the bottom properly
11 controls the switch ASIC; is that fair?

12 ATTORNEY WARRICK: Objection;
13 form.

14 THE WITNESS: There is -- there
15 would be no collisions within the operation of
16 the embodiment of Figure 10 provided the switch
17 ASIC is not trying to write write data at the
18 same time that either of the banks is trying to
19 write read data onto data buses 1016 or 1014.

20 That would be a description of a
21 collision where two drivers are trying to drive
22 something onto the same wires at the same time.

23 BY ATTORNEY CHANDLER:

24 Q. And let me put it this way.

25 I'm not saying a person of

1 ordinary skill in the art would do this, but
2 just to understand the importance of the control
3 unit ASIC in Figure 10 of Exhibit 1073, if we
4 wanted to, we could program that control unit
5 ASIC in Figure 10 of Exhibit 1073 to cause a
6 collision; right?

7 ATTORNEY WARRICK: Objection;
8 form.

9 THE WITNESS: Presumably, yes.
10 But if the control unit ASIC simultaneously
11 caused the ASIC -- switch ASIC to believe that a
12 write was happening and that it should drive
13 whatever it received on its ASIC DQ signals and
14 to drive them onto one or the other or both,
15 conceivably, of the data buses 1016 and 1014,
16 and simultaneously told the banks of DRAMs
17 1006 -- I'm sorry -- 1006 and 1008 to
18 simultaneously drive write -- read data onto
19 those same data buses, that would be causing a
20 data collision on those data buses, and that
21 would not yield proper operation of either the
22 reads or the writes.

23 BY ATTORNEY CHANDLER:

24 Q. And another example of proper
25 operation, which you wouldn't want to do but in

1 theory could happen is if the control unit ASIC
2 were programmed in a certain way, in Figure 10
3 of Exhibit 1073, the control until ASIC could
4 tell the switch ASIC to simultaneously drive 16
5 data lines out to the left of the switch ASIC
6 onto 8 data lines, and the result would be
7 nothing useable to the recipient.

8 Is that fair?

9 ATTORNEY WARRICK: Objection;
10 form.

11 THE WITNESS: I think your
12 statement precluding your question is not well
13 formed, because unless we're talking about a
14 multi-valued communication system, you can't
15 drive 2 bits onto one line in a
16 binary-communication setup. So the -- unless
17 there's some frequency multiplication going on
18 here, the -- you can't drive 2 bits onto one
19 line at the same time. The driver just is
20 unable to do that. It's -- and so your -- your
21 hypothetical is nonsensical in that sense.

22 Also, it's not a matter of
23 programming the control unit ASIC; it's matter
24 of designing it with a flaw. It's not likely to
25 be a highly programmable unit.

1 BY ATTORNEY CHANDLER:

2 Q. You said just a moment ago you
3 can't drive 2 bits onto one line at the same
4 time. And I understand that you wouldn't want
5 to do that, but I'm a little confused by your
6 suggestion that it can't be done.

7 I mean, I can have one wire with
8 two drivers both pointed on to the wire, and
9 they could both drive at the same time and that
10 would cause a collision; right?

11 A. That is what I've been describing
12 as a collision: Two things driving onto one
13 wire at the same time.

14 That's different from one driver
15 driving 2 bits at the same time, which is what
16 your previous hypothetical described, where you
17 had -- you were trying to get the ASIC switch to
18 drive 16 bits of data onto 8 bits of data bus.
19 And that is possible, certainly, within the
20 context of different nonbinary communication
21 systems, or in the context of transmission line
22 communication systems, where you have bits
23 flowing past each other on the same wire without
24 there being a problem associated with the
25 communication therein.

1 But in regard to memory
2 subsystems of the type that we're talking about
3 here, in the time frame we're talking about
4 here, the -- that's not typically possible.

5 Q. Take a look at Figure 4 of the
6 Ellsberry reference marked as Exhibit 1073.

7 A. Figure 4.

8 Q. Looking at Figure 4 do you see in
9 Figure 4 that there are two read drivers, one in
10 box 402 and the other in box 404?

11 A. Yes.

12 Q. If we turned on those two read
13 drivers 402 and 404 at the same time, is it fair
14 to conclude that a collision may result?

15 A. Yes.

16 ATTORNEY WARRICK: Objection to
17 form.

18 THE WITNESS: Yes, if there was a
19 circumstance where they both were driving
20 different bits of information at the same time,
21 then that would represent a collision on the DQ
22 line shown there.

23 However, the decode -- config
24 decode and the read/write logic in boxes 406 and
25 408 would be designed to not do that and to

1 drive -- have either one or the other driver
2 drive data at a time.

3 It's also unlikely that you would
4 implement it this way, since the drivers in the
5 read buffers of 402 and 404 are large and
6 expensive circuits, and you provide the
7 multiplexing functionality upstream from that.

8 But conceptually, this is a
9 reasonable interpretation of what's going on.

10 BY ATTORNEY CHANDLER:

11 Q. So turn back to Figure 10 of the
12 Ellsberry reference marked as Exhibit 1073.

13 Do you have that in front of you?

14 A. I'm back at 10.

15 Q. In theory, the switch ASIC in
16 Figure 10 of Exhibit 1073 could have 16 read
17 drivers all driving at the same time onto the
18 8-bit data bus coming out to the left of the
19 switch ASIC, and in that situation there would
20 be some collisions.

21 Is that fair?

22 ATTORNEY WARRICK: Objection;
23 form.

24 THE WITNESS: There -- if you
25 have 16 read drivers connected in pairs to 8

1 lines, and you -- and the control functionality
2 within the switch ASIC was flawed and caused
3 both of a pair of read drivers, in your
4 hypothetical, to drive simultaneously onto a
5 single wire, that would constitute a collision
6 on that bus, if the bits were different.

7 BY ATTORNEY CHANDLER:

8 Q. And so to avoid a data collision
9 in Figure 10 of the Ellsberry reference marked
10 as Exhibit 1073, the control unit and the switch
11 ASIC need to operate properly with correct
12 timing and correct direction so that only 8 of
13 the 16 read drivers and the switch ASIC are
14 driving read data out to the left onto the 8-bit
15 data bus; is that fair?

16 ATTORNEY WARRICK: Objection;
17 form.

18 THE WITNESS: Again, and that's
19 true in the context of DDR SDRAMs and DDR SDRAM
20 modules.

21 There are communication systems
22 where you can drive different drivers
23 simultaneously without error, either through an
24 open collector-type system or, as I said, with a
25 transmission line, but that would involve

1 transmitters at different locations.

2 But certainly with regard to an
3 open collector communication system or signaling
4 system, there would be no collision. It
5 would -- per se, that would be a different
6 function for that -- the effect of the wire and
7 the two drivers happening -- driving
8 simultaneously.

9 So, in short, a collision is not
10 strictly necessary, but in the context of this
11 particular figure and the DDR SDRAMs, a
12 collision would happen in that circumstance.

13 BY ATTORNEY CHANDLER:

14 Q. And this particular figure, being
15 Figure 10 of the Ellsberry reference marked as
16 Exhibit 1073?

17 A. The Figure 10 of 1073, if
18 implemented according to the structure of
19 Figure 4, which as I noted is not practical, but
20 which is conceptual in this case, if that
21 conceptual implementation of a pair of drivers
22 per bit line was implemented in Figure 10, then
23 yes, under that contrived circumstance, there
24 would be a collision.

25 Q. And I think you said a moment ago

1 something about open collector-type system.

2 A. Yes.

3 Q. To be clear, DDR memory devices
4 do not use open collector for the data signals;
5 correct?

6 A. Yes, that -- I did indicate that
7 in my answer.

8 Q. So do you agree that DDR memory
9 devices do not use open collectors for data?

10 A. DDR SDRAMs do not use open
11 collector drivers; correct.

12 Q. And Figure 10 of the Ellsberry
13 reference marked as Exhibit 1073, the address
14 and control signals AC and CS go to the control
15 ASIC 1002 at the bottom; correct?

16 A. Yes, the control unit ASIC is
17 marked as unit number 1002, and it has AC and CS
18 inputs on its left-hand side.

19 Q. And the switch ASIC 1040 in
20 Figure 10 of the Ellsberry reference marked as
21 Exhibit 1073 does not receive the address and
22 control signals AC and CS from the memory
23 controller; correct?

24 A. In this figure, Figure 10, the
25 exact form of the information communicated

1 between the control unit ASIC and the switch
2 ASIC is not presented or described. So it's
3 plausible that the chip-selects and the address
4 and control information is just forwarded to the
5 switch ASIC and it determines what's going on;
6 or alternatively, the control unit is doing some
7 pre-decode and sending a different but
8 equivalent sets of information from the control
9 unit ASIC to the switch ASIC.

10 Q. But either way, the address and
11 control signals AC and CS, they first go to the
12 control unit 1002 in Figure 10 of the Ellsberry
13 reference marked as Exhibit 1073; correct?

14 A. Yes. Figure 10 illustrates the
15 AC and CS inputs to the control unit Item 1002
16 and not such inputs to the switch ASIC 1004 and
17 only the ASIC pipe connections between those two
18 units.

19 Q. And the control unit -- or,
20 rather, control unit ASIC 1002 -- would be able
21 to determine, from the address and control
22 signals, which rank of memory would need to
23 output data to the switch ASIC; correct?

24 A. Is there a particular paragraph
25 or set of paragraphs in the specification of

1 Ellsberry that deals with the functionality of
2 the control unit ASIC that I should review?

3 Q. I'm basing this on your opinions
4 and your previous review of how things work.

5 A. Then I should take some time to
6 study this reference a little bit longer then;
7 because there are different ways it might be
8 done, and I don't remember off the top of my
9 head today exactly what Ellsberry says about the
10 operation of control unit ASIC.

11 Do you want me to do that?

12 Q. Respectfully, you spent over 15
13 hours preparing for this deposition; right?

14 ATTORNEY WARRICK: Objection;
15 form.

16 THE WITNESS: As I indicated, I
17 had not spent much of that time looking at
18 Ellsberry. So I am not as familiar with it as I
19 have been with some of the other references that
20 you have put in front of me.

21 BY ATTORNEY CHANDLER:

22 Q. Ellsberry was one of the
23 references used in the grounds of both
24 petitions; correct?

25 A. That is correct.

1 Q. Then it is a reference that you
2 reviewed and opined on in your expert
3 declarations marked as Exhibit 2024; correct?

4 A. Yes, I did review it and opined
5 on it back when this -- my declaration was
6 drafted, and I have said I have not reviewed it
7 in detail since.

8 Q. Am I correct that in a
9 JEDEC-style memory system, the address and
10 control signals, including the chip-select
11 signal, will tell you which rank of memory needs
12 to output data in response to a read command?

13 A. Certainly, if we bring up a JEDEC
14 standard for a UDIMM multi-rank memory module,
15 we will see that it is the chip-select inputs,
16 called the S inputs, to the modules that
17 determine -- or indicate to the module which of
18 the plurality of ranks are to be involved in the
19 present transaction.

20 Q. And Figure 10 of the Ellsberry
21 reference marked as Exhibit 1073 teaches to a
22 person of ordinary skill that the control unit
23 receives chip-select signals and then outputs
24 chip-select signals, and the two ranks of memory
25 devices receive the output of chip-select

1 signals; correct?

2 A. What's not clear to me without
3 further review is whether this is implementing a
4 JEDEC standardized module or something else with
5 different behavior than what I described
6 pertaining to the UDIMMs that are standardized
7 by JEDEC.

8 Q. Well, Ellsberry marked as Exhibit
9 1073 implements rank multiplication; right?

10 ATTORNEY WARRICK: Objection;
11 form.

12 (Witness reviews document.)

13 BY ATTORNEY CHANDLER:

14 Q. Are you not sure about this? I
15 mean, you did read Ellsberry; right?

16 A. As I said, months ago, when I was
17 preparing the declaration, I did, yes. I'm
18 reading portions of it again now.

19 Q. For example, in the abstract,
20 last sentence, Ellsberry marked as Exhibit 1073
21 teaches "making two smaller-capacity memory
22 devices emulating a single higher-capacity
23 memory device"; correct?

24 A. Yes, the last sentence of the
25 abstract is:

1 "That is, the invention
2 expands the addressable memory banks
3 on a module by making two
4 smaller-capacity memory devices
5 emulate a single higher-capacity
6 memory device."

7 And in the context of the
8 JEDEC -- SDRAM memory systems generally, that
9 is what we call rank multiplication.

10 Q. And, for example, on Figure 7A,
11 7B, 7C, 7D, E and F, Ellsberry teaches the use
12 of what the '417 and '215 patents refer to as a
13 density transition bit, but which Ellsberry
14 labels a physical bank select, in the column
15 second from the right; correct?

16 A. That's what the column second
17 from the right is called, "physical bank select
18 bit." And it refers to a column or row address
19 bit accordingly to -- depending on the
20 configuration specified in the different rows of
21 that table.

22 Q. And that's similar to the density
23 transition bit in the '417 and '215 patents that
24 we looked at a little bit earlier; correct?

25 ATTORNEY WARRICK: Objection;

1 form.

2 THE WITNESS: Similar, yes. I
3 don't know if it's precisely identical in all
4 cases. We'd have to look at the different
5 configurations that are being talked about in
6 the two references. But the general idea
7 appears to be similar.

8 BY ATTORNEY CHANDLER:

9 Q. Turning back to Figure 10 of the
10 Ellsberry reference marked as Exhibit 1073, the
11 control unit ASIC 1002 is going to receive the
12 address and control signals including one
13 chip-select signal; and it can perform rank
14 multiplication, meaning that it will output two
15 chip-select signals, labeled CS0A and CS0B;
16 correct?

17 ATTORNEY WARRICK: Objection;
18 form.

19 BY ATTORNEY CHANDLER:

20 Q. Or are you not sure?

21 A. Repeat the question, please.

22 Q. In Figure 10 of the Ellsberry
23 reference marked as Exhibit 1073, the control
24 unit ASIC 1002 is going to receive an address
25 and control signals including one chip-select

1 signal, and the control unit can perform rank
2 multiplication, meaning that it will output two
3 chip-select signals, labeled CS0A and CS0B;
4 correct?

5 ATTORNEY WARRICK: Objection;
6 form, form.

7 THE WITNESS: Yes, it seems that
8 the control unit ASIC is selecting one of the
9 two banks, as they're referred to here,
10 according to the table of Figure 7.

11 BY ATTORNEY CHANDLER:

12 Q. And again, for clarity, what you
13 just referred to as a bank is what today we
14 would refer to as a rank with an R; correct?

15 A. Generally speaking, that's true.

16 Q. And the control unit in Figure 10
17 of the Ellsberry reference marked as Exhibit
18 1073 will assert one of the two chip-select
19 signals to select one of the two ranks, 1006 or
20 1008, to perform the read operation; correct?

21 A. Yes, that's my understanding,
22 based on my quick review of Ellsberry, that the
23 read or write transactions involve one or the
24 other of Ellsberry's banks 1000- -- in
25 Figure 10, 1006 and 1008.

1 Q. And then the control unit ASIC in
2 Figure 10 of the Ellsberry reference marked as
3 Exhibit 1073 needs to tell the switch ASIC 1004
4 what to do at that point in time to properly
5 drive the read data from the targeted rank onto
6 the 8-bit data bus coming out to the left of the
7 switch ASIC.

8 Is that generally fair, at a high
9 level?

10 ATTORNEY WARRICK: Objection;
11 form.

12 THE WITNESS: Per the disclosure
13 of Figure 10 in particular, where the only
14 connection between those two ASICs is the ASIC
15 pipe and the control information associated with
16 the command and the address, in particular, is
17 presented initially only to the control unit
18 ASIC, it is -- somewhere, either in the switch
19 ASIC or in the control unit ASIC, there is going
20 to be a sequencing that goes on in order to
21 control the data paths within the switch ASIC to
22 do -- and the drivers and the receivers and all
23 the other associated circuitry to effect the
24 proper data transfers into and out of the
25 module.

1 BY ATTORNEY CHANDLER:

2 Q. If you turn to the Halbert
3 reference marked as Exhibit 1078. Let me know
4 when you have it in front of you.

5 A. I have the front page of patent
6 , , to Halbert in front of me.

7 Q. And John Halbert was at Intel;
8 correct?

9 A. At the time it appears to be the
10 case, yes.

11 Q. And did you know any of these
12 named inventors on the Halbert reference marked
13 as Exhibit 1078?

14 A. I have no recollection of having
15 met any of them. So I perhaps did, perhaps did
16 not.

17 Q. And you reviewed the Halbert
18 reference marked as Exhibit 1078; correct?

19 A. Yes.

20 Q. And you believe you understand
21 the Halbert reference --

22 A. Yes.

23 Q. -- marked as Exhibit 1078?

24 A. I do believe I understand the
25 Halbert reference.

1 Q. Take a look at Figure 4 in the
2 Halbert reference as marked as Exhibit 1078.
3 And am I correct it illustrates a memory module
4 100 that is m bits wide? M as in Mary.

5 A. Yes, on Figure 4 of Halbert we
6 have a box around the whole thing, 100; and we
7 have a DQ bus, that is lowercase m bits wide
8 exiting and entering that box 100 on its
9 left-hand side.

10 Q. M as in Mary; right?

11 A. M as in Mary; correct.

12 Q. And in Figure 4 of the Halbert
13 reference marked as Exhibit 1078, the memory
14 module 100 includes, on the right side, two
15 ranks of memory, 140 and 142, each of which is
16 also m bits wide -- M as in Mary; correct?

17 ATTORNEY WARRICK: Objection;
18 form.

19 THE WITNESS: Just as we were
20 struggling with terminology issues with
21 Ellsberry, we have terminology issues here as
22 well.

23 The Halbert calls unit 140 a rank
24 and unit 142 a rank even though they operate
25 together as a 2-m-bit-wide structure, which we

1 would call a single rank consistently with how
2 we've been using the term yesterday and today.

3 BY ATTORNEY CHANDLER:

4 Q. As a technical matter, however,
5 it would be within the skill of a person of
6 ordinary skill in the art to operate rank 140
7 and rank 142 in Figure 4 of Halbert marked as
8 Exhibit 1078 as two separate ranks. If the
9 person of ordinary skill in the art wanted to,
10 they could do that, for example, using two
11 separate chip-select signals; correct?

12 ATTORNEY WARRICK: Objection;
13 form.

14 THE WITNESS: So that would
15 require a modification of the device in multiple
16 respects, and it would be an entirely different
17 disclosure and it would not be satisfying the
18 principal motivation as articulated in Halbert.

19 BY ATTORNEY CHANDLER:

20 Q. Because as a technical matter,
21 it's not that hard to make two ranks operate
22 independently from each other; correct? That
23 was known and done?

24 ATTORNEY WARRICK: Objection;
25 form.

1 THE WITNESS: Two ranks generally
2 operate independently from each other.

3 In this case, they are not
4 independent of each other. If you were to
5 dramatically change the purpose and
6 functionality and timing and everything with
7 respect to the disclosure of Figure 4 of Halbert
8 and how it operates, as illustrated by Figures 5
9 and 6, then, you know, you would have an
10 entirely different device with two ranks and a
11 multiplexer, which would be -- the multiplexer
12 would be irrelevant at that point and you would
13 end up with a standard UDIMM, as defined by
14 JEDEC.

15 BY ATTORNEY CHANDLER:

16 Q. Or you would end up with
17 something like Figure 10 of Ellsberry marked as
18 Exhibit 1073 that we were just looking at;
19 right?

20 ATTORNEY WARRICK: Objection;
21 form.

22 THE WITNESS: Yes. If you make
23 enough changes to Halbert, you end up with
24 something that looks similar to Ellsberry, but
25 without the dual-read drivers that you were

1 insisting upon for inclusion in Ellsberry's
2 ASIC -- data path ASIC in order to get your
3 collisions that you were clearly wanting to
4 establish.

5 BY ATTORNEY CHANDLER:

6 Q. I don't want collisions. I'm not
7 trying to say I want collisions. I was just
8 trying to understand the hypothetical. So I'm
9 not pro-collision.

10 A. Right. So --

11 Q. I'm anti-collision.

12 A. Well, we're not driving
13 autonomous vehicles yet, so -- I'm not in favor
14 of automotive collisions either, and I try to
15 avoid data collisions in my designs as well.

16 But the point being that the data
17 path circuit 120 -- I forget its formal name --
18 hold on.

19 Q. Data interface.

20 A. Data interface circuit. Yes,
21 thank you.

22 So as it's structured, the data
23 interface circuit has a single driver onto the
24 DQ bus that is m bit wide so it cannot have a
25 collision onto that bus, as we had been

1 hypothesizing about Ellsberry.

2 Q. Fair to say there can be a
3 collision within data interface circuit 120. If
4 you are one of those crazy pro-collision types
5 of people, you could have 126 and 128 inside
6 data interface circuit 120, both driving at the
7 same time, and that could cause problems if your
8 MUX/DeMUX isn't doing what it should be doing.

9 I mean, there's all sorts of room
10 for collisions, if that's what you're looking
11 for in life; isn't that fair?

12 ATTORNEY WARRICK: Objection;
13 form. Also scope as to questions regarding data
14 collisions.

15 THE WITNESS: With regard to data
16 collisions, as we agreed, it was defined and
17 used by a POSITA in 2004-2005, you would not
18 have collisions within the data interface
19 circuit 120. The MUX/DeMUX 124 would
20 necessarily select or drive one or the other of
21 the DQ0, DQ1 buses, but those two buses would
22 not be connected physically together in order to
23 cause a data collision -- i.e., the simultaneous
24 driving of a single wire by both register 126
25 and register 128.

1 BY ATTORNEY CHANDLER:

2 Q. And is that arrangement of two
3 drivers connected to a MUX to avoid a data
4 collision, was that a typical arrangement at the
5 time?

6 A. Well, certainly whenever you have
7 a 2-to-1 multiplexing and that is bidirectional,
8 you need a MUX/DeMUX. So this is a circuit that
9 was well known in the art and a POSITA would
10 understand its function and operation.

11 Q. In Figure 4 of the Halbert
12 reference marked as Exhibit 1078, memory module
13 100 includes a data interface circuit 120, which
14 is coupled to rank 140 by an m-bit-wide data bus
15 RQ0, and is also coupled to rank 142 by another
16 m-bit-wide data bus RDQ1; correct? That's
17 literally what's drawn in Figure 4?

18 ATTORNEY WARRICK: Objection;
19 form.

20 THE WITNESS: It's drawn as two
21 separate m-bit-wide buses RDQ0 and RDQ1. But
22 if, for example, you look at Figure 5 and the
23 timing of those two lines, you see that they are
24 effectively two halves of a single 2-m-bit-wide
25 RDQ bus.

1 BY ATTORNEY CHANDLER:

2 Q. In Figure 4 of the Halbert
3 reference marked as Exhibit 1078, the data
4 interface circuit 120 includes data registers
5 126 and 128, multiplexer/demultiplexer 124 and,
6 towards the left, buffer 122; correct?

7 A. Among other things, yes.

8 Q. And those are controlled by
9 control signals coming from the module
10 controller 110 below them in Figure 4; correct?

11 A. Yes, there's a plurality of
12 signals that are shown going from the module
13 controller 110 into the data interface circuitry
14 120 to control its constituent parts.

15 Q. The control signals in Figure 4
16 of the Halbert reference marked as Exhibit 1078
17 coming from the module controller 110 include a
18 DIR signal -- spelled D-I-R -- which determines
19 the direction of the data transfer; a REG_SEL
20 signal, which selects either the data coming
21 from rank 140 or the data coming from rank 142;
22 and RDQS, RDQS0, and RDQS1 signals that control
23 buffer 122, register 126 and register 128;
24 correct?

25 ATTORNEY WARRICK: Objection;

1 form.

2 THE WITNESS: So RDQS0 and RDQS1
3 only control registers 126 and 128. I don't
4 think that's what you said.

5 BY ATTORNEY CHANDLER:

6 Q. RDQS, RDQS0 and RDQS1 --

7 A. I'm sorry. Right, I will -- yes.
8 RDQS controls 122. So your question was well
9 formed.

10 If you would -- I think, the
11 answer is yes, you described that accurately.

12 Q. I want to look at an annotated
13 version of Figure 5 of Halbert which is in the
14 petition. Do you have the petition handy or do
15 you want me to put it in the chat?

16 A. If it's not already open, I would
17 appreciate you put it in the chat, please.

18 ATTORNEY CHANDLER: All right.
19 So I'll put Paper 1 from each IPR into the chat.

20 (Exhibit Number P001 was previously
21 marked for identification.)

22 BY ATTORNEY CHANDLER:

23 Q. All right. So go ahead and open
24 both petitions, and I'll tell you where to go
25 after you got them both open.

1 A. Okay.

2 Q. So in the petition for the '417
3 patent, go to page 126. And then in the
4 petition for the '215 patent, go to page 131.
5 And you should see the same annotated figure in
6 both places. It's an annotation of Figure 5 of
7 the Halbert reference marked as Exhibit 1078.

8 A. And I'm sorry, the page number in
9 the '215 was, again?

10 Q. 131.

11 A. Yes, I see that those figures are
12 identical in the two petitions.

13 Q. And you understand that those
14 figures in the two petitions are taking Figure 5
15 of the Halbert reference marked as Exhibit 1078
16 and then are adding color annotations. So in
17 other words, everything in black and white was
18 from the original Figure 5 of the Halbert
19 reference marked as Exhibit 1078, and everything
20 in color has been added.

21 Understood?

22 A. Yes, I understand that.

23 Q. And you see that there's the
24 label "Module CAS Latency (4.0)" in the
25 annotated figures on page 126 of the '417

1 petition and page 131 of the '215 petition?

2 A. Yes.

3 Q. And then there's also the
4 annotation that says "Memory CAS Latency (2.5)"?

5 A. I see the annotation.

6 Q. Those annotations are they
7 understandable to you, what they're referring
8 to?

9 A. They are referring to temporal
10 differences between different clock edges.

11 Q. Can you explain that a little bit
12 more, what you mean.

13 A. Well, the -- annotation for the
14 module CAS latency is showing the temporal
15 difference between T4 and T8; and the memory CAS
16 latency annotation is showing the temporal
17 difference between T5 and T7n.

18 Q. So at a high level, is it
19 accurate that in the -- in Figure 4 of the
20 Ellsberry reference marked as Exhibit 1073, when
21 you have a read command with the timing as shown
22 in Figure 5, that the memory module receives the
23 read command at time T4 and starts to output the
24 data from the module to the host computer
25 starting at time T8?

1 A. Yes. The R command and RADD
2 buses are captured at T5 by the memory devices
3 in both 140 and 142, and they output their data
4 beginning at T7n for capture at T8.

5 Q. But before T5, the read command
6 is received by the module controller on the
7 memory module at time T4; correct?

8 A. Yes, that's correct. It takes a
9 full cycle, between T4 and T5, for the command
10 and address information to flow through the
11 module controller 110 of Figure 4 of Halbert.

12 Q. So Halbert's memory module
13 receives the read command at time T4, but the
14 memory devices don't get the read command until
15 time T5.

16 Is that fair?

17 A. They don't capture the read
18 command until the rising edge of clock indicated
19 at T5.

20 Q. And so there's a one-clock-cycle
21 delay in the memory module of Halbert marked as
22 Exhibit 1078 between the time when the memory
23 controller sends the read command to the memory
24 module, which is happening around time T4; and
25 the time when the memory devices get the read

1 command, which is going to be around time T5.

2 Is that fair?

3 ATTORNEY WARRICK: Objection;
4 form.

5 THE WITNESS: A more precise
6 formulation of that sentence would be it is one
7 cycle difference between when the memory
8 controller 110 captures the read command and
9 when the DRAMS that are in 140 and 142 together
10 capture the read command at T5.

11 BY ATTORNEY CHANDLER:

12 Q. And then in the Halbert reference
13 marked as Exhibit 1078, after the memory devices
14 capture the read command at time T5, it takes
15 those memory devices 2.5 clock cycles, according
16 to Figure 5, to output the first piece of read
17 data from the memory devices? Is that -- I'm
18 sorry.

19 It takes a total of 2.5 clock
20 cycles from the time the memory devices receive
21 the read command for them to output the read
22 data and for that read data to go through the
23 data interface circuit 120 and to come out the
24 other side off the module; is that correct?

25 ATTORNEY WARRICK: Objection;

1 form.

2 THE WITNESS: I'm sorry --

3 BY ATTORNEY CHANDLER:

4 Q. I'm sorry. I messed it up.

5 A. Yeah, I thought so.

6 Q. There are a lot of arrows.

7 A. There are many.

8 Q. In the DRAM memory devices in the
9 Halbert reference marked as Exhibit 1078, those
10 memory devices, as shown in Figure 5, take 2.5
11 clock cycles from the time the memory device
12 receives the read command until the time that
13 the first piece of data is output from those
14 memory devices.

15 Is that fair?

16 ATTORNEY WARRICK: Objection;
17 form.

18 THE WITNESS: I would use
19 "captures" instead of "receives" because it's
20 clearer and less ambiguous.

21 But -- so if we say it's 2.5 --
22 2-1/2 cycles from when the memory devices in 140
23 and 142 together capture the read command at T5
24 to when the DQS signal is asserted on the MDQS
25 line, indicating the start of the first bit

1 period of the data coming out of those memory
2 devices.

3 BY ATTORNEY CHANDLER:

4 Q. And then after the data first
5 comes out of the memory devices, according to
6 Figure 5 of the Halbert reference marked as
7 Exhibit 1078, there will be an additional delay
8 of approximately 0.5 clock cycles for that data
9 to travel from the right side of the data
10 interface circuit 120 to the left side of the
11 data interface circuit 120, as shown in
12 Figure 4?

13 Is that a fair summary?

14 ATTORNEY WARRICK: Objection;
15 form.

16 THE WITNESS: It's actually less
17 than that, because the data on the RDQ0 and RDQ1
18 buses is not captured until T8, and they -- it
19 flows through the circuit -- data interface
20 circuit 120 very quickly. And it's the -- the
21 strobe on the DQS signal 2, the memory
22 controller is asserted on -- at the same clock
23 edge T8 initiating the output of that first
24 piece of data.

25 So the actual delay through the

1 data interface circuit 120 is, depending on how
2 you count, about a quarter of a cycle from the
3 center of the eye input to the center of the eye
4 on the output.

5 BY ATTORNEY CHANDLER:

6 Q. But the net result, as shown in
7 Figure 5 of the Halbert reference marked as
8 Exhibit 1078, is that the module controller
9 captures the read command at time T4, and it's a
10 total of 4 clock cycles until time T8 that the
11 memory module starts outputting the first piece
12 of read data back to the host computer; correct?

13 A. Yes. The time difference between
14 T4, when the module captures the read command
15 and the rising edge of DQS on the output DQS
16 signal indicating the availability of data A1,
17 is four cycles.

18 Q. And then just focusing on the
19 DRAM memory devices, as we discussed though, the
20 delay from the time that the DRAM memory device
21 captures the read command until the time that it
22 outputs the first piece of read data is 2.5
23 clock cycles, in the Figure 5 of the Halbert
24 reference marked as Exhibit 1078?

25 A. Correct?

1 ATTORNEY WARRICK: Objection;
2 form.

3 THE WITNESS: Yes. What this
4 figure shows is that the time difference between
5 the DRAM capturing the read command and when the
6 rising edge on MDQS, indicating the beginning of
7 the first bit period on the RDQ0 and RDQ 1, is
8 2-1/2 cycles.

9 The difference between the two is
10 one cycle of latency through the memory
11 controller 110, half a cycle of communication
12 delay between the memories and the data
13 interface circuitry 120, and about a quarter of
14 a cycle of latency through the data interface
15 circuitry 120.

16 ATTORNEY WARRICK: Counsel, would
17 it be a good time to perhaps have a longer
18 break? I know it's about noon on the West Coast
19 and later for those of us further east.

20 THE WITNESS: Unless you're about
21 to wrap up entirely. Otherwise, yes, I'd like a
22 lunch break.

23 ATTORNEY CHANDLER: Well, I mean,
24 I heard both of you. Let me at least try to
25 finish up with this figure.

1 BY ATTORNEY CHANDLER:

2 Q. Do you still have the annotated
3 version of Figure 5 of Halbert in front of you?

4 A. Yes, I do.

5 Q. I was trying to listen to your
6 last answer, and I think we agreed that the
7 total there a from start to finish is 4 clock
8 cycles. I guess I was having a little trouble
9 following what you were saying, because it
10 didn't seem to add up to 4.

11 A. So the communication delay
12 between the output of MDQS strobe signal,
13 indicating the start of the data transmission
14 from the DRAM to the data interface circuitry
15 120 is -- and then there's a half-cycle delay
16 between that transition and when the data is
17 actually captured by the data interface circuit
18 120. And then there's a nominal delay within
19 the memory device between when it captures that
20 data and when it immediately starts to send the
21 data.

22 The reason that the totals were
23 slightly more than one cycle is because of the
24 difference between when the DQS signals are
25 asserted for read data and when the center of

1 the eye, indicating where the data is
2 capture-able.

3 But what is clear is that the
4 bulk of the difference between those two
5 annotated times comes from the delay of the
6 command and address through the memory
7 controller 110; and through the communication on
8 the MDQS and RDQ0 and RDQ1 buses and that the
9 amount of delay through the data interface
10 circuit 120 is relatively small.

11 Q. But if you add up all of the
12 delays that you just referred to, it's a total
13 delay of four clock cycles; is that fair?

14 A. That's how we measure latency
15 in -- read latency for JEDEC standard memory
16 devices from the capture of a read command on
17 the rising edge of clock to the rising edge of
18 DQS, indicating the start of a bit period for
19 the first piece of data of a burst.

20 Q. I'm still a little unclear if
21 you're agreeing with me or disagreeing with me.

22 A. I'm agreeing with you that the
23 annotated differences of 4 cycles and 2-1/2
24 cycles correspond to how latencies are measured
25 within JEDEC standardized SDRAMs and SDRAM

1 modules, and that the annotations are for 4
2 cycles and 2-1/2 cycles respectively.

3 Q. And you're referring to the
4 annotation on page 126 of the '417 petition and
5 page 131 of the '215 petition; correct?

6 A. Correct, yes.

7 Q. Netlist did not invent SDRAM
8 memory devices; correct?

9 A. Is this a new topic or just
10 wrapping up?

11 Q. It's wrapping up. Potentially
12 it's not a long series of questions, but, I
13 mean -- unfortunately, I don't -- I don't --
14 it's like 10 questions depending on --

15 ATTORNEY WARRICK: Counsel, I
16 mean, I just want to note we've had several
17 occasions where the witness has asked for a
18 break and --

19 (Simultaneous cross-talk.)

20 ATTORNEY CHANDLER: I'm trying to
21 wrap up.

22 THE WITNESS: If the 10 questions
23 are all of the nature of "Netlist didn't
24 invent," then we can deal with those quickly.
25 If you're going to get into technical details,

1 then we should break for lunch.

2 ATTORNEY CHANDLER: I'm not going
3 to get to the technical details, but,
4 unfortunately, I can't totally control what
5 you're going to tell me.

6 THE WITNESS: No, of course not.

7 BY ATTORNEY CHANDLER:

8 Q. Netlist did not invent SDRAM
9 memory devices; correct?

10 A. I do not know if they were JEDEC
11 members through the development of those
12 standards. If they were, then they had a hand
13 in it. I don't know.

14 Q. Netlist's '417 and '215 patents
15 do not purport to have invented SDRAM memory
16 devices; correct?

17 A. Which variety of SDRAM devices
18 are you talking about?

19 Q. Any variety.

20 A. I'm not aware of any references
21 within the specifications of those patents that
22 would attribute the invention of an SDRAM-style
23 memory to Netlist.

24 Q. Netlist's '417 and '215 patents
25 do not purport to have invented DDR1 or DDR2

1 SDRAM memory devices; correct?

2 A. I'm not aware of any statements
3 to that effect within the specifications of the
4 '417 or '215 patents.

5 Q. Netlist's '417 and '215 patents
6 did not invent ranks of memory devices -- ranks
7 with an R -- correct?

8 A. No. As we've seen many times
9 over the last two days, those concepts date back
10 to the 1990s and before.

11 Q. Netlist's '417 and '215 patents
12 did not invent the memory controller for the
13 computer system; correct?

14 A. Memory controllers have been in
15 existence for as long as there have been
16 memories; and so no, the concept of a memory
17 controller was not invented by Netlist.

18 Q. Netlist did not invent, in the
19 '417 or '215 patents, address signals, control
20 signals or data signals; correct?

21 ATTORNEY WARRICK: Objection;
22 form.

23 THE WITNESS: Those general
24 categories of signal types were not invented by
25 Netlist and have, again, been around as long as

1 there have been memories and memory systems.

2 BY ATTORNEY CHANDLER:

3 Q. Netlist's '417 and '215 patents
4 did not invent chip-select signals; correct?

5 A. Chip-select signals have been
6 associated with memory devices since at least
7 the 1960s, so they are not novel to anything
8 invented in the 2000s.

9 Q. Netlist's '417 and '215 patents
10 did not invent CAS latency; correct?

11 A. CAS latency.

12 So the concept of a CAS latency
13 dates back to the very first DRAMs in the 1960s,
14 so that concept was not novel to Netlist in the
15 2000s.

16 Q. Netlist's '417 and '215 patents
17 did not invent the DIMM memory module or the
18 RDIMM memory module; correct?

19 A. You're referring to the JEDEC
20 standardized UDIMM and RDIMMs in particular?

21 Q. Well, they certainly didn't
22 invent those; right?

23 A. Again, they may have been part of
24 the JEDEC standard-forming procedures or
25 processes for those modules and so may have had

1 a hand in that. They certainly are not claiming
2 to have done so within the specification of the
3 '417 and '215 as such.

4 Q. And Netlist's '417 and '215
5 patents do not purport to have invented buffered
6 memory modules where the data signals are
7 buffered; correct? That was known prior to the
8 '417 and '215 patents?

9 ATTORNEY WARRICK: Objection;
10 form.

11 THE WITNESS: The -- I'm sorry.
12 You're referring to buffered modules in
13 particular or -- just repeat the question,
14 please.

15 BY ATTORNEY CHANDLER:

16 Q. Netlist's '417 and '215 patents
17 do not purport to have invented memory modules
18 with buffers for the data signals; those were
19 known before the '417 and '215 patents; correct?

20 ATTORNEY WARRICK: Objection;
21 form.

22 THE WITNESS: There were modules
23 that included buffers prior to the filing date
24 of the -- or the priority date of the '417 and
25 '215. The specifics of the additional circuitry

1 on the modules is the essential aspect of the
2 novel features -- claimed features of the '417
3 and '215 patents.

4 BY ATTORNEY CHANDLER:

5 Q. And some examples that we've
6 talked about of memory modules with buffers for
7 the data signals include the Perego reference
8 marked as Exhibit 1071, the Ellsberry reference
9 marked as Exhibit 1073, and the Halbert
10 reference marked as Exhibit 1078; correct?

11 A. I take --

12 ATTORNEY WARRICK: Objection;
13 form.

14 THE WITNESS: I take exception
15 with Ellsberry being characterized as prior art.
16 I thought we had gone through the provisional --
17 the arguments about the provisional not
18 supporting all of the claim elements at issue.
19 And if that is, in fact, true, then Ellsberry,
20 by my understanding, today is not prior art.

21 Certainly Halbert, I think if
22 it's prior art, includes a buffer circuit.
23 Perego, if it's a prior art, includes a buffer
24 circuit as well.

25 ///

1 BY ATTORNEY CHANDLER:

2 Q. Putting aside whether or not
3 they're prior art, the Perego reference marked
4 as Exhibit as 1071, the Ellsberry reference
5 marked as Exhibit 1073, and the Halbert
6 reference marked as Exhibit 1078 are all memory
7 modules with buffers for the data signals;
8 correct?

9 ATTORNEY WARRICK: Objection;
10 form.

11 THE WITNESS: Again, I've been --
12 let me start again.

13 Putting aside the issue entirely
14 of which of those are prior art and which of
15 them are not prior art, they all include some
16 degree of circuitry on the data paths of those
17 modules.

18 BY ATTORNEY CHANDLER:

19 Q. Do you have any corrections or
20 clarifications you'd like to make to any of the
21 testimony that you've given to me today or
22 yesterday?

23 A. None that come to mind at
24 present, but we'll see during redirect.

25 ATTORNEY CHANDLER: I'll pass the

1 witness.

2 If we can do this -- if we could
3 go off the record and then, Phil, if you could
4 just put in the chat how long you want me to go
5 away for -- and I realize it may take you a
6 moment to decide that question. But if you
7 could just tell me when you want me to come
8 back, just put it in the chat, and I'll be back.

9 ATTORNEY WARRICK: Well, I mean,
10 I think it would probably make sense for us to
11 plan for a longer break so the folks who want to
12 get food can do so.

13 ATTORNEY CHANDLER: Why don't
14 you --

15 THE VIDEOGRAPHER: Counsel, would
16 you like to go off the record?

17 ATTORNEY CHANDLER: No, I want us
18 all to be on the same wavelength here.

19 Why don't you talk, Phil, to
20 whoever you need to talk to, and then let us all
21 know in the chat how quickly you want us to come
22 back. Because if it's -- you know, I don't want
23 to go away for an hour if you're just going to
24 come back with a couple of questions, so ...

25 ATTORNEY WARRICK: Well, I think

1 it's fair to say between -- it's -- it's not
2 just going to be a couple of questions.

3 ATTORNEY CHANDLER: Okay. So
4 we'll go off the record and you can tell us what
5 time to come back then.

6 ATTORNEY WARRICK: Okay.

7 THE VIDEOGRAPHER: Off the record
8 at 12:18 p.m. Pacific Time.

9 (Luncheon recess taken from 12:18 p.m.
10 to 1:35 p.m.)
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P R O C E E D I N G S
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THE VIDEOGRAPHER: On the record
at 1:35 p.m. Pacific Time.

EXAMINATION

BY ATTORNEY WARRICK:

Q. Dr. Przybylski, do you recall
being asked yesterday various questions by
Petitioner's counsel related to claim
construction?

A. Yes, generally.

Q. And I believe you stated
yesterday that for purposes of your
declarations, Exhibit 2024 in these two IPRs,
that you applied Netlist's proposed claim
construction for the term "rank."

Do you recall that?

A. Yeah, I think I misspoke in that
answer.

Q. What claim construction for the
term "rank" did you apply in your declarations,
both marked 2024 in these IPRs?

1 A. So with regard to, for example,
2 paragraph 165 of my declaration in the '417, I
3 specifically say that I'm applying the
4 Petitioner's proposed construction, not
5 Netlist's.

6 Q. Is that true for the entirety of
7 your declaration in the '417 patent IPR?

8 A. Yes.

9 Q. Is that also the case for your
10 declaration in the '215 patent IPR?

11 A. Yes.

12 Q. And Petitioner's proposed
13 construction -- part of Petitioner's proposed
14 construction, I should say, suggests that a rank
15 could be one or more memory devices; correct?

16 A. I believe that to be the case. I
17 don't remember what paragraph I -- here it is.

18 Paragraph 62 I talk about the
19 Court's construction, and 60 I talk about the
20 Petitioner's construction. "One or more memory
21 devices," yes.

22 Q. And am I correct that in forming
23 your opinions in these IPRs and in preparing the
24 declarations marked 2024 in these two IPRs, that
25 you apply this construction, including the

1 concept that a -- that one on more memory
2 devices on a memory module could constitute a
3 rank?

4 A. Yes. I applied Petitioner's
5 proposed construction in its entirety, which is
6 an independent set of one or more memory devices
7 on a memory module that act together in response
8 to command signals, including chip-select
9 signals, to read or write full-bit width of the
10 memory module.

11 Q. Would your opinions in these two
12 declarations, Exhibit 2024, be different had you
13 applied your personal understanding, as
14 articulated yesterday, that a rank requires a
15 plurality of memory devices?

16 A. No. First of all, that personal
17 understanding was based on the perspective of a
18 POSITA in 2004 and '5.

19 But to answer your question more
20 directly, no, my opinions that the arguments put
21 forward in the petition and declaration are --
22 fail to invalidate or render obvious any of the
23 claims of the -- these two patents would remain
24 the same regardless.

25 Q. And in your declarations, did you

1 provide any opinions regarding claim
2 construction for any terms in the '417 or '215
3 patents?

4 A. No, I did not provide any new
5 claim construction. I list the proposed
6 constructions that are in the record, and I
7 applied Petitioner's -- I did not render an
8 opinion as to which or any of those were a
9 correct construction.

10 Q. Now, yesterday you were also
11 asked some questions about SO-DIMMs.

12 Do you recall that?

13 A. SO-DIMMs were one of the DIMM
14 types that were in the list of -- enumerated
15 DIMM types or memory module types in one of the
16 references.

17 Q. And do you recall also being
18 asked questions yesterday about FB-DIMMs?

19 A. Yes, similarly.

20 Q. Can I have you take a look at the
21 '417 patent, Column 6, beginning around line 43.
22 And this is a paragraph we've looked at both
23 yesterday and today.

24 A. Yes, I have that in front of me.

25 Q. And you'll recall that there is

1 identical text in the '215 patent?

2 A. Yes. Mr. Chandler pointed that
3 out.

4 Q. I'd like to ask you a couple of
5 questions about the sentence that begins around
6 line 43. I'm going to read it:

7 "Furthermore, memory modules
8 10 compatible with embodiments
9 described herein include, but are
10 not limited to, single in-line
11 memory modules (SIMMs), dual in-line
12 memory modules (DIMMs),
13 small-outline DIMMs (SO-DIMMS),
14 unbuffered DIMMS (UDIMMs),
15 registered DIMMs (RDIMMs),
16 fully-buffered DIMMs,
17 (FB-DIMM-DIMMs), rank-buffered
18 DIMMS, (RBDIMMs), mini-DIMMs, and
19 micro-DIMMs."

20 Did I read that correctly?

21 A. Yes, you did.

22 Q. So when the patents say that
23 these various types of memory modules are
24 compatible with embodiments described in the
25 patent specifications, what does that mean to

1 you?

2 A. It means that these style of
3 modules, which are literally compatible with the
4 embodiments disclosed in the specification of
5 the '417 and '215. In other words, if you were
6 to take the SO-DIMM outline and you could create
7 a new module that incorporates features from the
8 specification of the '417 and '215 patents and
9 create a new SO-DIMM, that would not be a
10 standard -- standardized SO-DIMM but would have
11 that form factor, and in that way these module
12 types are compatible with the embodiments
13 disclosed in these specifications.

14 Q. And that's, to be clear, not the
15 same as being an embodiment of the claimed
16 invention; correct?

17 A. No. There are not embodiments
18 that are disclosed that fit any of those
19 physical parameters for the -- or -- of those
20 module types.

21 Q. So, for example, were -- would
22 the POSITA have been aware of any SO-DIMMs at
23 the time of the invention that would constitute
24 embodiments of the '417 or '215 patents' claimed
25 inventions?

1 A. Well, the JEDEC standards for
2 SO-DIMMs have not been brought into the record
3 here. I haven't reviewed those in a long time,
4 but it's my recollection that as of 2004 and
5 2005 there were not any SO-DIMMs with, for
6 example, buffers on the DQ lines, that they were
7 more along the line of UDIMMs, the DRAMS were
8 just connected directly out to the contacts of
9 the SO-DIMMs.

10 Q. And do you understand the claimed
11 inventions of the '215 and '417 patents to
12 require such buffers on the DQ lines?

13 A. Yes. It's -- it's -- there is
14 the -- there are numerous elements within these
15 patents that recite buffers and the like that
16 require circuitry between the DRAMS and the pins
17 of the modules.

18 Q. This portion of the
19 specifications also reference FB-DIMMs. Do you
20 recall when FB-DIMMs were standardized?

21 A. It's my recollection that
22 FB-DIMMs were first standardized in 2007.

23 Q. Now, you have opined that the
24 priority date for the '215 and '417 patents
25 should be at least as early as January of 2005;

1 correct?

2 A. More precisely what I've opined
3 on is that the arguments within the petition and
4 the corresponding declaration that attempt to
5 invalidate or set the priority date of the
6 claims to be after -- some point after the date
7 associated with the '087 provisional are
8 rebutted effectively; and that's so the claims
9 at issue deserve that priority date absent any
10 additional arguments to the contrary.

11 Q. And in that '087 application,
12 from -- that was filed in January of 2005, the
13 inventors did not include all of the same exact
14 text that is included in the specifications of
15 the '417 and '215 patents; right?

16 A. Indeed. That's how provisionals
17 work. You're allowed -- between the provisional
18 and the final application, you're allowed to
19 flesh out and fully teach the invention.
20 There's no expectation that the full text of the
21 patent be present within the provisional.

22 Q. And --

23 ATTORNEY CHANDLER: Phil and
24 Dr. Przybylski, if you could leave time between
25 the question and answer for me to object.

1 I have an objection to that last
2 question that it was leading.

3 THE WITNESS: I will try.

4 BY ATTORNEY WARRICK:

5 Q. Dr. Przybylski, do you recall if
6 the '087 provisional included any disclosures
7 regarding FB-DIMMs?

8 A. I don't recall specifically, but
9 we can check and search for FB-DIMM in there. I
10 don't think there was any -- I don't recall any
11 reference to the FB-DIMMs per se in the '087.

12 Q. And so is it possible that the
13 language regarding FB-DIMMs in the
14 specifications of the '417 and '215 patents was
15 added subsequent to that January 2005
16 provisional application?

17 ATTORNEY CHANDLER: Objection;
18 leading.

19 THE WITNESS: Yeah, it's clear --
20 if the language is not in the provision, it
21 was -- provisional application, it must have
22 been added at some point during the prosecution
23 after that time.

24 BY ATTORNEY WARRICK:

25 Q. What understanding, if any, do

1 you have about the relationship between
2 embodiments that are disclosed in a patent
3 specification and embodiments that are claimed
4 in those patents?

5 A. Not all disclosed embodiments are
6 claimed; not all claims encompass all disclosed
7 embodiments.

8 Q. Now, yesterday you may recall
9 there were questions from Petitioner's counsel
10 regarding Exhibit 2031, which you cited in your
11 declarations.

12 Do you recall that?

13 A. 2031 being Appendix -- Appendix X
14 of -- at -- at Section 4.1.2.10 of JEDEC
15 standard 21-C, Release 13.

16 Q. Yes. And I believe you testified
17 yesterday that you were not aware of the
18 specific publication date of that document,
19 Exhibit 2031; is that right?

20 A. Yes. This document doesn't have
21 a date on it; it only has a release date -- a
22 release number. And Counsel didn't provide any
23 documentation vis-a-vis the date of this -- of
24 Release 13.

25 Q. When you cited Exhibit 2031 in

1 your declarations, Exhibit 2024 in these two
2 IPRs, was it your belief that the cited
3 information reflected the knowledge of a POSITA
4 at the time of the invention?

5 A. Yes. Generally speaking, the
6 idea of SPDs containing information about the
7 modules predates the DDR2 instantiation of that
8 standard, and so it's -- I think I opined to the
9 effect that the -- the idea of SPDs generally
10 and their contents would have been known to a
11 POSITA in the 2004-2005 time frame.

12 Q. And would that include the
13 specific information that you cited in
14 Exhibit 2031 in your declarations in these two
15 IPRs?

16 A. Yes, it would.

17 Q. And is that the case regardless
18 of when Exhibit 2031 was published?

19 A. Yes. Of the -- the two
20 references to 2031 in my declarations, the
21 contents -- the portions that I cite to from
22 2031 would have been in the -- in the knowledge
23 of a POSITA of 2004-2005.

24 Q. I'd like to look at Exhibit 2031
25 if we can. Could you pull that up, please.

1 A. I'm looking at 2031, the first
2 page of it at least.

3 Q. Can you look at page 8, please.

4 A. Page 8.

5 I'm looking at page 8.

6 Q. And on page 8 we have a table
7 that appears to be related to module data width.
8 Is that right?

9 A. Yes. "Byte 6: Model Data Width"
10 is the heading on the top of page 6.

11 Q. And do you recall answering
12 questions yesterday about module data width in
13 the context of the JEDEC21-C standard?

14 A. Generally, yes.

15 Q. And in this table on page 8 of
16 Exhibit 2031, we have various entries with
17 different possible -- with different data width
18 values provided, such as 32, 33, 64, et cetera.
19 Is that right?

20 A. Yes.

21 Q. And some of the lines on this
22 table have dashes rather than a number provided
23 for the data width column of the table.

24 Do you see that?

25 A. I do.

1 Q. Do you know what that indicates?

2 A. The -- only some of the values of
3 the 8-bit field represented by bit 0 through bit
4 7 are allowed; and rather than only listing the
5 allowed ones, the authors of this standard have
6 put in rows of the table with dashes to signify
7 to the reader that there are gaps in the values
8 that are allowed. And any values that are in
9 those gaps are not allowed and, therefore, are
10 indicated as such with dashes.

11 Q. So in light of this table on
12 page 8 of Exhibit 2031 under the JEDEC21-C
13 standard, would a 4-bit module data width be
14 permitted?

15 ATTORNEY CHANDLER: Objection;
16 leading.

17 THE WITNESS: So what this table
18 says is that the SPD does not define a
19 4-bit-width module type. So it's not proper to
20 attempt to identify the module width to be 4
21 bits.

22 BY ATTORNEY WARRICK:

23 Q. What about 8 bits?

24 A. Similarly.

25 Q. Were 4- or 8-bit-width

1 JEDEC-compliant modules known to a POSITA at the
2 time of the invention of the '417 and '215
3 patent?

4 ATTORNEY CHANDLER: Object to
5 form.

6 THE WITNESS: Not DIMMs. There
7 were 8-bit-wide SIMMs that were archaic. I
8 don't even know if they predate JEDEC's
9 involvement in the standardization of modules.
10 They may just have been industry standard
11 without being JEDEC industry standard modules.
12 I don't know that.

13 BY ATTORNEY WARRICK:

14 Q. You also answered questions
15 yesterday regarding the definition of the
16 POSITA, or the person of ordinary skill in the
17 art, for purposes of your declarations related
18 to the '417 and '215 patents.

19 Do you recall that?

20 A. Generally speaking, yes.

21 Q. And I believe at various times
22 you indicated that certain technologies or
23 potential prior art may have predated that
24 hypothetical POSITA by some number of years; is
25 that right?

1 A. Yes, I remember questions along
2 those lines.

3 Q. And how, if at all, did it impact
4 your analysis for purposes of your declarations,
5 Exhibit 2024 in these two IPRs, that any
6 potential prior art may have come -- may have
7 existed in time substantially before the -- let
8 me -- let me rephrase that question. I
9 apologize.

10 How, if at all, did the age of
11 any potential prior art affect your analysis for
12 purposes of your declarations, Exhibit 2024 in
13 these two IPRs?

14 A. I'm not aware of any archaic
15 prior art that was older than the professional
16 experience of a POSITA, as we discussed
17 yesterday, having any impact on the analysis in
18 my declarations.

19 Q. So you did not ignore any prior
20 art by reason of it being too old?

21 A. No.

22 Q. And is it your view that a
23 POSITA, at the time of the invention of the '417
24 and '215 patents, would have ignored any
25 potential prior art by reason of it being too

1 old?

2 A. No. The POSITA would not ignore
3 ideas or prior art because it's too old.

4 Q. Today you were asked questions by
5 Petitioner's counsel about the concept of rank
6 multiplication.

7 Do you recall that?

8 A. Yes.

9 Q. Is it your understanding that the
10 claims of the '417 and '215 patents are directed
11 to the concept of rank multiplication?

12 A. No, I don't think that the
13 independent claims of these patents relate to
14 rank multiplication at all.

15 Q. On the topic of rank
16 multiplication, Petitioner's counsel asked you a
17 lot of questions about Figure 1 of the Perego
18 reference, which is Exhibit 1070.

19 Do you recall that?

20 A. Let me bring up 1070.

21 ATTORNEY CHANDLER: I'm sorry.
22 What figure did you say?

23 ATTORNEY WARRICK: Figure 1.

24 THE WITNESS: 1070 is Jacobs'
25 book.

1 BY ATTORNEY WARRICK:

2 Q. I apologize.

3 A. Perego is 1071.

4 Q. Yeah, I apologize. So strike
5 that.

6 Did not mean Perego.

7 A. You mean the --

8 Q. Of the '417 and '215 patents.

9 A. Yes, that makes more sense.

10 Q. So you recall being asked
11 questions about rank multiplication in the
12 context of Figure 1 of the '417 and '215
13 patents, yes?

14 A. Yes, correct.

15 Q. Is there anything in Figure 1 of
16 the '215 and '417 patents that would be
17 indicative of rank multiplication to a POSITA at
18 the time of the '417 and '215 patent inventions?

19 A. Repeat that back for me, please.

20 Q. Sure.

21 Is there anything in Figure 1 of
22 the '215 and '417 patents that would be
23 indicative of rank multiplication to a POSITA at
24 the time of the inventions?

25 A. To the extent that there's a

1 single chip-select shown going in and a POSITA
2 viewed that as a single chip-select as opposed
3 to a plurality of chip-select signals going in
4 and a plurality of chip-selects going out, that
5 might be indicative of some form of rank
6 multiplication going on. But there are --
7 that's not the only possible interpretation of
8 Figure 1.

9 Q. When you say "a chip-select
10 signal going in," are you referring to a signal
11 being input to what's labeled as 40 in Figure 1?

12 A. Yeah. The -- between memory
13 controller 20 and circuit 40, there's a line
14 that's drawn as bidirectional, labeled CS with a
15 pound sign, CS bar, between those two. That's
16 what I'm referring to.

17 Q. And, in your opinion, how would a
18 POSITA at the time of the invention interpret
19 that CS# label in Figure 1 of the '417 and '215
20 patents?

21 A. There are a range of
22 possibilities. Its bidirectionality would be a
23 point of confusion to a POSITA, because
24 chip-select signals don't generally flow back
25 from a module towards a memory controller. It

1 may be also that the chip-select CS# line could
2 be a chip-select bus, as the address and control
3 lines are obviously buses and are labeled
4 identically.

5 So there are a number of
6 possibilities that would come to mind of a
7 POSITA looking at Figure 1.

8 Q. In your opinion, are there
9 embodiments of the '417 and '215 patents that do
10 not include rank multiplication?

11 A. Yes. As I talk about in
12 paragraph 78 of my '417 declaration, rank
13 multiplication is just one of the ideas found in
14 the specification of the '417 and is generally
15 restricted to a range involving the Verilog
16 examples. But it's not a concept that's found
17 within the claims of the '417 or '215.

18 Q. You were also asked questions
19 today by Petitioner's counsel regarding
20 Rambus-style memory modules and memory devices;
21 is that right?

22 A. Yes.

23 Q. Do the '417 and '215 patents
24 provide any indication to a POSITA at the time
25 of the inventions that the claimed inventions of

1 the '417 and '215 patents could be used in a
2 Rambus-style environment?

3 ATTORNEY WARRICK: Objection;
4 leading.

5 THE WITNESS: No, there's --
6 there's really no suggestion of that within the
7 figures or specification of the '417 or '215.

8 BY ATTORNEY WARRICK:

9 Q. Is there any indication in the --
10 or suggestion in the '417 and '215 patents that
11 embodiments of the claimed inventions could
12 incorporate both JEDEC-style SDRAM memory
13 devices and a Rambus-style primary channel?

14 A. I don't find any support for the
15 idea that embodiments of the '417 and '215
16 could -- would use a Rambus channel of any of
17 the flavors that we are familiar with in this
18 matter. It's all directed towards -- the
19 embodiments are all directed towards variations
20 of the SDRAMs and the other JEDEC standardized
21 devices and modules.

22 Q. You were also asked questions
23 today about the Perego reference, which is
24 Exhibit 1071.

25 A. Yes.

1 Q. Does Perego contain any
2 suggestion to a POSITA that its claimed
3 invention could be implemented with a
4 JEDEC-style primary channel?

5 A. Perego's claims?

6 Q. Correct.

7 A. I have not paid a lot of
8 attention to Perego's claims since it was
9 referenced as prior art. Only to the extent
10 that the claims are part of the original.

11 Q. Let me ask you a better question.
12 Does Perego contain any
13 suggestion to a POSITA that the embodiments
14 disclosed in Perego included a JEDEC-style
15 primary channel?

16 A. In my discussions with
17 Mr. Chandler, we characterized JEDEC-style
18 primary channel as one that not just had
19 separate address control and data signals but
20 which also embodied the other features and
21 aspects of DDR2 SDRAM modules. And as a
22 result -- or with that view of what a
23 JEDEC-style primary channel might be, there is
24 no suggestion within Perego that I'm aware of
25 that suggests a JEDEC-style primary channel.

1 Q. Does Perego provide any
2 suggestion to a POSITA that the disclosed
3 embodiments in Perego could be used with a
4 JEDEC-style primary channel?

5 A. I'm not aware of any such
6 suggestions within the specification of Perego.

7 ATTORNEY WARRICK: I have no
8 further questions at this time.

9 ATTORNEY CHANDLER: Take a break
10 for about ten minutes?

11 ATTORNEY WARRICK: Sure.

12 ATTORNEY CHANDLER: And then I'll
13 have at least some questions.

14 THE VIDEOGRAPHER: Off the record
15 at 2:15 p.m. Pacific Time.

16 (Recess taken from 2:15 p.m. to
17 2:26 p.m.)

18 THE VIDEOGRAPHER: On the record
19 at 2:26 p.m. Pacific Time.

20

21 FURTHER EXAMINATION

22 BY ATTORNEY CHANDLER:

23 Q. Dr. Przybylski, I want to follow
24 up with you first with respect to claim
25 construction for the term "rank." All right?

1 A. Yes.

2 Q. And so you understand there's a
3 disagreement where Samsung has taken the
4 position that "rank" can include one or more
5 memory devices, and Netlist has taken the
6 position that "rank" requires two or more memory
7 devices.

8 Understood?

9 A. Yes.

10 Q. Did I hear you correctly say, in
11 response to questions from Netlist's counsel,
12 that you are not offering any opinion
13 disagreeing with Samsung's proposed claim
14 construction for the term "rank" with respect to
15 Samsung's position that the term "rank" can
16 include just one memory device?

17 A. I've not been instructed to offer
18 any particular opinions with regard to claim
19 construction, so I presented the different
20 alternatives. And as I noted in redirect,
21 the -- I applied Petitioner's construction to
22 the "rank" element of the independent claims.

23 Q. So to be clear, in these IPRs you
24 are not offering any opinions disagreeing with
25 Samsung's proposed construction for the term

1 "rank"; correct?

2 A. I'm not offering any opinions
3 disagreeing or agreeing with Samsung's
4 construction of "rank."

5 Q. Can you pull up the '417 and '215
6 patents again.

7 A. Both or just one?

8 Q. Well, I want to cover both. It's
9 up to you whether you want to look at both or
10 just want to focus on one, with the
11 understanding that the specification in the
12 figures are the same in both.

13 A. All right. I'm looking at the
14 '417 right now.

15 Q. You were asked questions about
16 whether the claims of the '417 and '215 patents
17 concern rank multiplication, by counsel for
18 Netlist.

19 ATTORNEY WARRICK: Objection;
20 form.

21 THE WITNESS: That was a
22 statement or a question?

23 BY ATTORNEY CHANDLER:

24 Q. Do you recall a moment ago being
25 asked by counsel for Netlist about whether or

1 not the claims of the '417 and '215 patents
2 require rank multiplication?

3 A. I remember some questions on
4 redirect about that. I think they were phrased
5 a little bit differently, but yes, I understand
6 what you're talking about.

7 Q. The '417 and '215 patents
8 disclose rank multiplication; correct?

9 A. As I describe in my declaration,
10 the rank multiplication is one of the aspects of
11 the embodiments -- or some of the embodiments of
12 the '417 and '215, but there are other ideas and
13 disclosures and embodiments as well.

14 Q. And I think you said that in your
15 opinion, the independent claims -- or at least
16 some of the independent claims, the '417 and
17 '215 patents do not require rank multiplication;
18 correct?

19 A. There is a single independent
20 claim for the '415. There are --

21 Q. You said '415.

22 A. I apologize. '417. It's been a
23 long two days. My apologies.

24 There's a single independent
25 claim for the '417, and there are only two

1 independent claims for the '215. And it was my
2 answer to counsel that rank multiplication is
3 not a essential feature of either -- of any of
4 those claims.

5 Q. But there's a difference between
6 "essential feature" and whether the claim
7 encompasses rank multiplication; right?

8 ATTORNEY WARRICK: Objection;
9 form.

10 THE WITNESS: "Encompasses" --
11 would you clarify what you mean by
12 "encompasses."

13 BY ATTORNEY CHANDLER:

14 Q. What I'm getting at, and I think
15 you understand, is that the way independent
16 claims work is that they're broader than the
17 dependent claims. So you can have an
18 independent claim in the '417 and '215 patents
19 that covers two embodiments, one of which is
20 rank multiplication, one of which is not; and
21 then there can be dependent claims that further
22 limit the independent claim to one of those two
23 embodiments, such as rank multiplication;
24 correct?

25 A. Yes. That's a general statement

1 of how dependent claims work.

2 Q. And there are at least some
3 dependent claims in the '417 and '215 patents
4 that require rank multiplication; right?

5 ATTORNEY WARRICK: Objection;
6 form.

7 THE WITNESS: You want to point
8 me to a specific dependent claim that we are
9 talking about?

10 BY ATTORNEY CHANDLER:

11 Q. Sure. Look at dependent Claims 9
12 through 11 of the '215 patents.

13 A. I'll bring up the '215, one
14 moment, please.

15 And you said Claim 9?

16 Q. 9, 10, 11.

17 (Witness reviews document.)

18 A. None of these use the word "rank
19 multiplication." You have to -- I haven't
20 looked at these particular claims in a long
21 while, so I'd have to spend some time studying
22 them to understand whether these plurality of
23 different chip-select signals constitute rank
24 multiplication or some broader concept that was
25 also enabled by the specification of these

1 patents.

2 Q. But the point is, you have never
3 offered the opinion and you're not trying to
4 offer the opinion now that the claims of the
5 '417 and '215 patents are somehow such that they
6 do not include rank multiplication; right?

7 ATTORNEY WARRICK: Objection;
8 form.

9 THE WITNESS: I have not offered
10 any opinions as to whether the scope of these
11 claims do or do not include modules that
12 implement rank multiplication.

13 BY ATTORNEY CHANDLER:

14 Q. Could you turn to Column 23 of
15 the '417 patent and Column 21 of the '215
16 patent.

17 A. I have the '215 in front of me.
18 What lines of Column 21?

19 Q. I'll just ask it more generally.
20 It's the same point, which is, in Figure 1 of
21 the '215 and '417 patents, to be clear, that
22 Figure 1 of the '417 and '215 patents can
23 include rank multiplication.

24 Now, you're saying there may be
25 other embodiments where it doesn't have rank

1 multiplication; but the flip side is the patent
2 makes clear that it can implement rank
3 multiplication; correct?

4 A. There are definitely columns that
5 talk about -- and the tables and the like that
6 talk about rank multiplication and how do you
7 implement it vis-a-vis the density transition
8 bits and so forth.

9 Q. And that can all be done in
10 Figure 1 of the '417 and '215 patents; correct?

11 A. Yes. Figure 1 is sufficiently
12 generic that it could show embodiments
13 including -- that include rank multiplication,
14 as well as others that do not.

15 Q. Could you turn to Column 6 of the
16 '417 patent, and I think it's also Column 6 of
17 the '215 patent. Bottom of Column 5, top of
18 Column 6 of the '215 patent. Let me know when
19 you're there.

20 A. You're referring to the load
21 isolation section or something else?

22 I'm looking at the Column 6 of
23 the '417.

24 Q. It's the same section that
25 counsel for Netlist was asking you about. It's

1 talking about all the different types of memory
2 modules and all the different types of memory
3 devices that are compatible with the '417 and
4 '215 patents.

5 A. Yes.

6 Q. So Column 6, lines 43 or so; and
7 then in the '215 patent, Column 5, line 63 or
8 so.

9 A. Yes, I see that section of
10 Column 6 of the '417.

11 Q. And there were some questions
12 that you were asked about SO-DIMM and FB-DIMM
13 and whether those were compatible with the
14 disclosed invention of the '417 and '215
15 patents.

16 Do you recall those colloquies?

17 A. Yes.

18 Q. And your testimony was that an
19 SO-DIMM in the prior art would not satisfy the
20 claimed invention.

21 Instead, if I understand your
22 point correctly, your point was that you could
23 take an SO-DIMM from the prior art and then
24 modify it to practice the inventions disclosed
25 by the '417 and '215 patents.

1 Is that fair?

2 A. I think the essence of my
3 testimony was that these terms refer either to
4 form factors or to JEDEC standardized specific
5 modules.

6 To the extent that this list of
7 buffer types is referring to just the form
8 factors, you could have a POSITA take the
9 inventions of -- or embodiments of the '417 and
10 implement them on a SO-DIMM form factor, for
11 example; but that the standardized SO-DIMMs of
12 the 2004-2005 time frame do not, for example,
13 include buffers on the data paths.

14 Q. Okay. So in your opinion, as of
15 January 19th, 2005, the priority date that you
16 have said applies, in your opinion, a person of
17 ordinary skill in the art would be able to
18 implement rank multiplication on an SO-DIMM; is
19 that correct?

20 ATTORNEY WARRICK: Objection;
21 form.

22 THE WITNESS: SO-DIMMs are
23 constrained in the amount of area that they have
24 on them relative to standard DIMMs; but in
25 theory, that's -- that's generally true.

1 The ...

2 BY ATTORNEY CHANDLER:

3 Q. And to take another example, in
4 your opinion, a person of ordinary skill in the
5 art as of January 19th, 2005, would be able to
6 take a UDIMM, which is to say an unbuffered
7 memory module, and that person could implement
8 rank multiplication on the UDIMM; correct?

9 ATTORNEY WARRICK: Objection;
10 form.

11 THE WITNESS: Given the teachings
12 of the '417 and '215 in front of them, they
13 would have the teaching necessary to implement
14 the rank multiplication units in the circuit 40
15 or 42, et cetera, depending on the particular
16 figures we are talking about. And just as they
17 could in a full-sized DIMM module -- the UDIMMs
18 are the same size, so they would be able to
19 modify a UDIMM to incorporate the additional
20 integrated circuits and other -- and features
21 that are disclosed with the rank multiplication
22 embodiments of the '417 and '215.

23 BY ATTORNEY CHANDLER:

24 Q. And so if you took a UDIMM as of
25 January 19th, 2005, and tried to implement

1 rank multiplication as taught by the '215 and
2 '417 patents, you would need to add buffers to
3 the data lines; is that right?

4 Because those don't exist on a
5 UDIMM; right? There's no buffers on the data
6 lines of a UDIMM, so you would have to add new
7 data buffers to the UDIMM to implement the rank
8 multiplication taught by the '417 and '215
9 patents; correct?

10 A. That would certainly be one way
11 to accomplish the inclusion of rank
12 multiplication features onto a UDIMM. I'm not
13 prepared to say that's the only way. There are
14 certainly figures that suggest that they're not
15 required in the teaching of the '417, but,
16 again, this is not a concept that I've thought a
17 lot about to this point.

18 Q. But, in your opinion, a person of
19 ordinary skill in the art would know how to put
20 data buffers on a UDIMM, and would also know how
21 to put the circuit 40 of the translation logic
22 to implement rank multiplication, as of
23 January 19th, 2005, without any of that
24 Verilog code; correct?

25 ATTORNEY WARRICK: Objection;

1 form.

2 THE WITNESS: I'm sorry. What
3 about the Verilog code? I didn't catch that.

4 BY ATTORNEY CHANDLER:

5 Q. The Verilog code is not something
6 the person of ordinary skill needs, right to
7 implement the rank multiplication? Or do you
8 think they do need it?

9 A. Well, certainly the Verilog code
10 is part of the disclosure of the '417 and
11 includes -- is part of the embodiments of that
12 specification. To the extent --

13 Q. But it's not -- but not -- I'm
14 focused on January 19th, 2005; right? The
15 '087 didn't have any Verilog code.

16 A. I see your point.

17 Yeah, it would be more of a
18 challenge for a POSITA. But I think that a
19 POSITA would be able to re-create that Verilog
20 code from the concepts of a rank multiplication
21 in the context of adding that to a UDIMM.

22 Q. Right. So in your opinion, a
23 person of ordinary skill in the art as of
24 January 19th, 2005, looking at the '087
25 provisional marked as Exhibit 1005 had the skill

1 to take a UDIMM, add data buffers to the data
2 lines, add logic to perform rank multiplication
3 based on the density transition bit, and would
4 have the skill to create the Verilog code to
5 program that logic to operate correctly.

6 Is that fair?

7 ATTORNEY WARRICK: Objection;
8 form.

9 THE WITNESS: I want to pull up
10 the '087. Do you have the exhibit number for
11 that?

12 BY ATTORNEY CHANDLER:

13 Q. 1005.

14 A. There it is. Sorry.

15 Yes, I believe there's
16 sufficient disclosure in the '087 for a POSITA
17 to do that.

18 Q. You were asked some questions
19 about when FB-DIMM was standardized and when it
20 was known.

21 Do you recall those questions?

22 A. In general, yes.

23 Q. I think you said that your
24 recollection is that FB-DIMM was standardized in
25 2007. But clearly the inventors of the '417 and

1 '215 patent were talking about it before 2007;
2 right?

3 ATTORNEY WARRICK: Objection;
4 form.

5 THE WITNESS: What we established
6 was that the '087 provisional application does
7 not mention the FB-DIMMs and that at some point
8 during the provision -- the transformation from
9 the provisional to the final specification,
10 discussion of the FB-DIMMs were added. I do not
11 know at what point in the prosecution of the
12 '417 and '215 that particular language was
13 added.

14 BY ATTORNEY CHANDLER:

15 Q. But you understand that the '417
16 and '215 patents haven't changed with respect to
17 the specification in the discussion of FB-DIMM
18 since the nonprovisional application was filed;
19 right?

20 ATTORNEY WARRICK: Objection;
21 form.

22 THE WITNESS: I'm sorry. I have
23 not looked carefully at the full prosecution
24 history, so I don't know when the last
25 continuation-in-part or the non- -- the -- which

1 version of the -- which application actually
2 contains that language for the first time.

3 BY ATTORNEY CHANDLER:

4 Q. And my point is a little broader
5 than that, which is: Regardless of when FB-DIMM
6 was finally standardized by JEDEC, which may
7 have been in 2007, persons of ordinary skill in
8 the art before that time, they would have known
9 about FB-DIMM and that it was coming; right?

10 A. Not necessarily. The -- it would
11 have been discussed within JEDEC committee
12 meetings prior to that; and senior engineers
13 within the companies participated in the
14 particular JEDEC committee that was thinking
15 about standardizing FB-DIMMs would clearly have
16 been aware of the proposal and the various
17 ballots being voted on with regard to the
18 ultimate standard.

19 But a POSITA outside of that
20 select group would not necessarily have heard
21 the term or been aware of it prior to the
22 release of the standard. Or at least a -- at
23 least of press releases foreshadowing that
24 release.

25 And, again, none of that is in

1 the record here, so we don't know when that
2 happened.

3 (Exhibit Number 1012 was previously
4 marked for identification.)

5 BY ATTORNEY CHANDLER:

6 Q. We'll take a look at
7 Exhibit 1012, which I put in the chat, which is
8 the nonprovisional application filed July 1st,
9 2005.

10 A. This is patent number '386. That
11 one?

12 Q. Yes. And that's part of the
13 priority chain of the family of patents.

14 A. Okay, I have that up.

15 Q. So Exhibit 1012, filed July 1st
16 2005, refers to FB-DIMM in Column 6, line 8 or
17 so; correct?

18 A. Yes. The FB-DIMMs are mentioned
19 there at -- across lines 8 and 9.

20 Q. And the language in Column 6 of
21 Exhibit 1012, from approximately lines 1 through
22 30, about how the memory module is compatible
23 with embodiments described in Exhibit 1012
24 include DIMM, SO-DIMM, FB-DIMM, et cetera,
25 that's the same language that appears in the

1 '417 and '215 patents marked as Exhibit 1001;
2 correct?

3 A. It appears to be. I haven't
4 actually compared them word by word, but the
5 general list is the same, yes.

6 Q. And that's not surprising, that a
7 person of ordinary skill in the art would have
8 known about FB-DIMMs even before JEDEC finished
9 the standards for FB-DIMMs; correct?

10 A. No, my testimony of a few moments
11 ago is that a POSITA would not necessarily have
12 heard of FB-DIMMs well in advance -- certainly
13 years in advance of the release of the standard,
14 unless there was a product that the standard was
15 following in the marketplace -- and I'm
16 certainly not aware of that -- or press accounts
17 that foreshadowed the release of the standard.

18 With this language in the
19 Column 6 of the '386 or the '417 or the '215
20 indicates to me is that most likely Netlist was
21 a member of JEDEC and that the inventors of
22 this -- listed on this patent application were
23 either participating in or were talking with
24 Netlist representatives at the JEDEC meetings
25 and, therefore, were aware of a forthcoming

1 standard that was not yet widely in the public
2 domain.

3 Q. But how can you say it wasn't
4 widely in the public domain when I'm looking at
5 it in a patent application filed July 1st,
6 2005?

7 A. I said not widely in the public
8 domain. Clearly, the inventors had heard the
9 term, may have known more than just the name of
10 it. We don't know.

11 We knew that there was something
12 called FB-DIMM that was being worked on at
13 some -- by someone either in a company somewhere
14 or within JEDEC. We have no knowledge of
15 exactly how that term came to be known by the
16 inventors and put into the language of the
17 specification as of the middle of 2005.

18 Q. So do you disagree with
19 Exhibit 1012 when it says as of July 1st,
20 2005, that a person of ordinary skill in the art
21 could implement rank multiplication in an
22 FB-DIMM?

23 ATTORNEY WARRICK: Objection;
24 form.

25 ///

1 BY ATTORNEY CHANDLER:

2 Q. That's what -- that's what
3 Exhibit 1012 is saying; right? Is "Memory
4 module 10 compatible with embodiments described
5 herein" includes DIMM, SO-DIMM and FB-DIMM.

6 And I'm trying to understand if
7 you're sort of fighting what the inventors are
8 telling us about whether a person of ordinary
9 skill in the art reading this application could
10 actually do what they're saying.

11 A. Well, your previous question --
12 ATTORNEY WARRICK: Objection to
13 form.

14 THE WITNESS: Your previous
15 question was all in the context of UDIMMs, which
16 were, in fact, widely known by POSITAs in the
17 2004-2005 time frame.

18 To the extent that an FB-DIMM was
19 not widely known within -- in July of 2005 and
20 that in only -- and that a POSITA would have
21 only had full access to the details of a -- what
22 an FB-DIMM actually is until later means that
23 the migration of the features of this
24 specification into an FB-DIMM would have
25 required two things: First of all, a knowledge

1 of this specification, and a knowledge of
2 FB-DIMMs.

3 If the latter was not widely
4 known until sometime after 2005, that is when a
5 POSITA would have been able to undertake such a
6 task.

7 BY ATTORNEY CHANDLER:

8 Q. There were a lot of "ifs" in your
9 answer, and so it's a little unclear to me what
10 your position is about whether or not a person
11 of ordinary skill in the art as of July 1st,
12 2005, could have implemented rank multiplication
13 in an FB-DIMM, as stated by Netlist patent
14 marked as Exhibit 1012 in Column 6 line 8.

15 A. What my answer --

16 ATTORNEY WARRICK: Object to
17 form.

18 THE WITNESS: What my answer
19 tried to convey is that if a POSITA in July 2009
20 [sic] had full knowledge of what an FB-DIMM was
21 going to be, then, yes, it would have been
22 possible.

23 But if a POSITA was not aware of
24 what the details of an FB-DIMM were or were
25 going to be at that time, then one half of the

1 equation is not present.

2 BY ATTORNEY CHANDLER:

3 Q. Could a POSITA have joined JEDEC
4 to get information about the FB-DIMM if they
5 didn't have it already?

6 A. No.

7 ATTORNEY WARRICK: Objection to
8 form.

9 THE WITNESS: As we discussed
10 yesterday, the members of JEDEC are companies,
11 and they are bound by nondisclosure agreements.
12 So some random Joe can't walk in off the street
13 and attend a meeting.

14 BY ATTORNEY CHANDLER:

15 Q. Not some random Joe: A person of
16 ordinary skill in the art, which is, you know,
17 the field of art that JEDEC is concerned about.

18 A. Well, with regard to the JEDEC
19 meetings, a POSITA engineer that's relatively
20 green is not necessarily someone that can come
21 in, even as a representative of his parent
22 company, the company that he or she works for.

23 But the -- it is the senior
24 members of the engineering and marketing teams
25 of the member companies that routinely

1 participate in the JEDEC meetings, because it's
2 their expertise that helps direct the
3 standard-setting process.

4 Q. So are you suggesting that the
5 inventors at Netlist, when they disclosed on
6 July 1st, 2005, FB-DIMM in Exhibit 1012, did
7 that violate some JEDEC policy?

8 A. I'm not aware of the specifics of
9 the JEDEC policy with regard to the naming
10 terminology of future standards.

11 There's also the possibility that
12 there is a product or a product plan of some
13 company that was putting that terminology into
14 the public domain with or without disclosing
15 full details of it. We -- we have nothing to go
16 on except for these four words in Column 6.

17 Q. Well, it's not entirely true. I
18 mean, we have the level of ordinary skill in the
19 art to go on; right?

20 A. Yes, but your questions premised
21 around a modification of something. And if you
22 don't know what you're modifying, you can't
23 effect that.

24 So the specification of the '417,
25 '215, et al., teaches the features that are

1 going to be added to something, in your
2 hypothetical; but without -- this specification
3 doesn't tell us about what the FB-DIMM is.

4 It ultimately comes into the
5 public domain clearly when JEDEC standardizes
6 it. And we don't have any information in front
7 of us to help us understand when the details of
8 FB-DIMMs do come into the public domain widely
9 other than the 2007 release of the standard.

10 Q. You were not a member of JEDEC,
11 but you told me that you went to some JEDEC
12 meetings; right?

13 A. I think two, as the guest of a
14 client of mine.

15 Q. Did you sign a nondisclosure
16 agreement when you went to those JEDEC meetings?

17 A. I had nondisclosure agreements
18 with my clients.

19 Q. But not with JEDEC?

20 A. Indirectly so, I guess. But they
21 did not -- there were -- the agreements that I
22 was aware of were between JEDEC and the
23 companies, not specifically with the individual
24 representatives of those companies. So I
25 guess --

1 (Simultaneous cross-talk.)

2 Q. Hold on. There are no
3 nondisclosure agreements in JEDEC.

4 A. I'm sorry?

5 Q. There are no nondisclosure
6 agreements in JEDEC; right?

7 ATTORNEY WARRICK: Objection;
8 form.

9 THE WITNESS: I -- as far as I'm
10 aware -- and, again, I'm not a member of JEDEC
11 and have only observed the process -- is that
12 the proceedings of the meetings are not to be
13 widely disseminated. Whether that's enforced by
14 a nondisclosure agreement or by whatever
15 mechanism the membership meeting agreement for
16 the member companies, I'm not privy to that.
17 BY ATTORNEY CHANDLER:

18 Q. A person of ordinary skill in the
19 art can form their own company and join JEDEC;
20 right?

21 ATTORNEY WARRICK: Objection;
22 form, also scope.

23 THE WITNESS: I don't know what
24 the membership requirements are for joining
25 JEDEC. I have no knowledge about that.

1 BY ATTORNEY CHANDLER:

2 Q. You told me a moment ago that you
3 did know, that -- you said a person can't do it,
4 a company has to do it.

5 A. Well, yes, I know that it's
6 companies, but I don't know if there are any
7 other requirements other than that, or whether,
8 you know, a company that's not actively involved
9 in the industry is -- is invited or is allowed
10 to participate. I don't know. I have no
11 knowledge of that.

12 Q. Isn't it true that basically
13 every company that you've ever heard of is a
14 member of JEDEC, in this field?

15 ATTORNEY WARRICK: Objection;
16 form. Objection; scope.

17 THE WITNESS: No, that's not at
18 all the case, that there are -- there are a
19 large number of companies in this field, and not
20 all of them are JEDEC members. I'm pretty sure
21 of that. I don't know precisely which are and
22 which are not, but the membership list of JEDEC
23 is not in the thousands.

24 BY ATTORNEY CHANDLER:

25 Q. It's in the hundreds though;

1 right?

2 ATTORNEY WARRICK: Same
3 objections.

4 THE WITNESS: I don't know that.
5 I certainly don't know that with regard to the
6 specific committees that are involved for these
7 standards. I would be surprised if it was
8 hundreds. The --

9 BY ATTORNEY CHANDLER:

10 Q. And you know that Rambus was a
11 member of JEDEC; right?

12 A. For a while it was, yes.

13 Q. And Intel was a member of JEDEC?

14 A. I believe so. I don't know for
15 sure, but I presume so.

16 Q. Are you aware of any company that
17 was ever rejected from joining JEDEC?

18 ATTORNEY WARRICK: Objection;
19 form. Objection; scope.

20 THE WITNESS: I have no knowledge
21 about any of that.

22 BY ATTORNEY CHANDLER:

23 Q. To be clear, you are not offering
24 an opinion today that FB-DIMMs were unknown to a
25 person of ordinary skill in the art as of

1 July 1st, 2005; correct?

2 A. No, I'm not forming an opinion to
3 that effect, no.

4 Q. And you're not offering an
5 opinion today that FB-DIMMs were unknown to a
6 person of ordinary skill of the art as of
7 January 19, 2005; correct?

8 A. It's -- my opinions in this
9 matter are related to the validity of these
10 claims and the arguments put forward by the
11 Petitioners and their expert; and I have
12 rebutted those arguments that seek to invalidate
13 the claims in question.

14 I do not offer any opinions
15 outside of those four corners of the task in
16 front of me.

17 Q. So if I understand correctly, you
18 viewed your task as starting with the assumption
19 that the claims were entitled to a priority of
20 January 9th [sic], 2005; and then looking at
21 the arguments presented by the petition and
22 Dr. Wolfe, and responding to those arguments and
23 offering the opinion of whether, in your view,
24 the arguments by the Petitioner and the opinions
25 by Dr. Wolfe were sufficient.

1 ATTORNEY WARRICK: Objection;
2 form.

3 THE WITNESS: I would say it's
4 the other way around.

5 I start the process with an open
6 mind as far as the validity and the valid
7 priority date of the application. I looked at
8 the arguments put forward by -- in the petition.
9 I found them lacking and, therefore, presumed
10 that there is no reason provided in the position
11 [sic] to amend the apparent priority date, per
12 the front page of the patents.

13 BY ATTORNEY CHANDLER:

14 Q. There were some questions about
15 the '417 and '215 patent and Rambus.

16 Do you recall those?

17 A. There were some questions not
18 about Rambus the company but with regard to
19 Rambus channels as -- in general.

20 Q. And by the time of the '417 and
21 '215 patents, Rambus channels, in general, were
22 known to a person of ordinary skill in the art;
23 correct?

24 A. Yes. We came to that conclusion
25 yesterday.

1 Q. And nothing in the '417 and '215
2 patents explicitly excludes Rambus channels from
3 being within the scope of the embodiments of the
4 '417 and '215 patents; correct?

5 ATTORNEY WARRICK: Objection;
6 form.

7 THE WITNESS: Nothing
8 specifically excludes them. But the fact that
9 Rambus rims are not in the list of modular types
10 enumerated is an indicator that at least for the
11 inventors the Rambus channels were not front of
12 mind as far as the implementation space of their
13 invention, that their invention is applicable
14 to.

15 So there's nothing -- there's
16 nothing explicit, but there are indications.
17 BY ATTORNEY CHANDLER:

18 Q. But there are also indications
19 going the other way, and the most notable being
20 that the inventors are very clear that the list
21 of memory modules they say "includes but are not
22 limited to"; right?

23 A. Yes, and so --

24 ATTORNEY WARRICK: Objection;
25 form.

1 THE WITNESS: So it's not
2 explicit.

3 But the fact that they -- out of,
4 you know, 32 pages of specification, they didn't
5 add an additional word about a module type that
6 they were aware of but didn't include with the
7 other module types, that's kind of a strong
8 indication -- although not definitive, I will
9 grant you that -- it's a strong indication as to
10 what the inventors understood to be the
11 applicability of their inventions.

12 BY ATTORNEY CHANDLER:

13 Q. And it may also be a strong
14 indication, by the 2004-2005 time frame, that
15 the vast majority of the industry was using
16 JEDEC-style memory devices and JEDEC-style
17 buses; correct?

18 ATTORNEY WARRICK: Objection to
19 form.

20 THE WITNESS: They did include
21 FB-DIMM, which was not commercially available
22 yet. So the volume is not an idea that clearly
23 played a role in determining what they put in
24 that list and what they didn't.

25 (Simultaneous cross-talk.)

1 (Interruption by the court reporter to
2 clarify the record.)

3 BY ATTORNEY CHANDLER:

4 Q. FB-DIMM was JEDEC; correct?

5 A. But there are other DIMM types in
6 this list that, as far as I know, are not JEDEC.

7 Q. Could you pull up Exhibit 2031,
8 and let me know when you have it.

9 A. I have in front of me
10 Exhibit 2031, which is a portion of Release 13
11 of JEDEC Standard 21-C starting at
12 page 4.1.2.10-1.

13 Q. And counsel for Netlist asked you
14 some questions about page 8 of Exhibit 2031. So
15 if you could go there, let me know when you have
16 it.

17 A. I am looking at page 8.

18 Q. So on page 8 of Exhibit 2031
19 there's a table, and some of the rows of the
20 table have dashes or hyphens; correct?

21 A. Yes. We discussed that.

22 Q. And when I look at the table and
23 I see a row for 0 and then a dash in the next
24 row, and then a row following that for 32, I
25 read that to mean that any value between 0 and

1 32 is permissible.

2 But if I understood your
3 testimony, you're trying to say that all the
4 values between 0 and 32 are impermissible. Is
5 that correct?

6 (Witness reviews document.)

7 A. It is my presumption going into
8 this document, consistent with the other JEDEC
9 documents, that dashes are impermissible values,
10 and there's no language that I see elsewhere
11 within the document that would define it
12 otherwise.

13 So that there are permissible
14 values, and there are other -- some of which are
15 currently used, somewhere are effectively for
16 future expansion; and then there are other
17 values that are impermissible and that are not
18 anticipated to be presently used or ever used in
19 the future.

20 Q. So you've interpreted the dash in
21 Exhibit 2031 as indicating values that are
22 impermissible; correct?

23 A. Yes. In other words, a memory
24 controller reading a particular value out of the
25 SPD encountering a value that is -- that would

1 normally fall into one of the dashed rows would
2 not be required to be able to interpret that
3 value.

4 It's a -- this standard is a
5 listing of what the memory module vendors are
6 allowed to put into the SPD and what the memory
7 controllers are required to be able to interpret
8 as either valid or invalid or -- and
9 correspondingly the dashed lines are outside of
10 that agreement that this standard represents
11 between module makers and systems companies
12 buying them.

13 Q. You sure about that?

14 A. As I said, there's no --I'm not
15 finding any language to dissuade me of that
16 general impression of that's how JEDEC standards
17 are formulated.

18 Q. Please turn to page 13 of
19 Exhibit 2031.

20 You agree that the DRAM memory
21 devices can be x4, x8, x16 or x32; correct?
22 Which is to say a width of 4 bits, 8 bits, 16
23 bits or 32 bits.

24 A. Most of them are, yeah. I think
25 there have been some -- there may have been some

1 in history that are -- have additional bits.
2 Certainly the Rambus-style devices were also in
3 x9 and x18, but I don't know whether there were
4 standardized or nonstandardized SDRAMs that had
5 other widths than that.

6 Q. The table on page 13 of
7 Exhibit 2031 has a dash between 15 and 254; it
8 does not have any row for an SDRAM that's 16
9 bits wide, 18 bits wide, 32 bits wide or 36 bits
10 wide, even though the text on page 13 of
11 Exhibit 2031 makes clear those are all
12 permissible widths; correct?

13 (Witness reviews document.)

14 A. There's something odd about this
15 table, and I don't understand why it's
16 constructed the way it is and why there are not
17 values for x60 and x30 enumerated in the lower
18 portion of the table. I would have expected
19 that to occur. Maybe this was revised in a
20 subsequent release. I don't know.

21 Q. Or maybe dashes don't indicate an
22 impermissible value.

23 A. That's plausible at this point,
24 but, again, I don't know. We'd have to be sure
25 and look at other SPDs documents.

1 I do know that in other JEDEC
2 documents, dashes are generally listed -- values
3 that are not within the agreed-upon set of
4 values that are permitted from either the vendor
5 side or the consumer side. So I do not
6 understand why this table appears to be
7 different.

8 But regardless of what it is --
9 whether it's different or if, as you suggest, my
10 understanding of the table on Figure 8 is
11 inadequate, it still doesn't affect any of my
12 opinions in this matter.

13 Q. Including your opinion that
14 Ellsberry discloses an 8-bit-wide memory module;
15 correct?

16 A. I believe my testimony with
17 regard to Ellsberry is that it's -- the previous
18 figures in Ellsberry show a full 64-bit module
19 with a plurality of slices that were narrower;
20 and that by the time we got to Figure 10, it
21 shows a control unit ASIC, a switch ASIC and 8
22 bits of data to a POSITA that would be what's
23 shown as a complete module x8, but it doesn't
24 make much sense commercially or technically; and
25 instead the Figure 6 of Ellsberry is more

1 indicative of what a full module would look
2 like.

3 So my testimony previously, as I
4 recall it, was that it could be interpreted
5 either way by a POSITA.

6 Q. Including an 8-bit-wide memory
7 module.

8 ATTORNEY WARRICK: Objection;
9 form.

10 THE WITNESS: Again, Figure 10,
11 if viewed by a POSITA as a complete module,
12 would be an 8-bit module. But there are -- by
13 the time we get to 2004-2005, there are no
14 commercially viable 8-bit modules in the
15 marketplace that use JEDEC standard SDRAMs. All
16 of the standardized and high-volume modules of
17 that time frame are x32 or majority are x64.

18 BY ATTORNEY CHANDLER:

19 Q. If I understand your testimony in
20 response to questions from counsel for Netlist,
21 a person of ordinary skill in the art does not
22 forget the earlier prior art; right? They still
23 have in their knowledge prior art that's more
24 than a few years old; correct?

25 A. The -- my testimony with counsel

1 for Netlist was that if there's a piece of prior
2 art that is relevant to an argument that happens
3 to predate the experience of a POSITA, we don't
4 discount that prior art and discard it because
5 it's too old. We still consider it valid prior
6 art.

7 ATTORNEY CHANDLER: Thank you,
8 Dr. Przybylski. No further questions. That
9 concludes the deposition of today and yesterday.
10 Thank you.

11 THE COURT REPORTER: You
12 gentlemen both want your rough drafts again
13 today?

14 ATTORNEY CHANDLER: Yes, please.
15 And just as a reminder, a final draft by
16 Thursday, February 22nd, please.

17 THE WITNESS: Gail, do you need
18 any clarification of unintelligible?

19 THE COURT REPORTER: I don't
20 believe so, but hang on.

21 Mr. Warrick, you want the rough
22 draft today?

23 ATTORNEY WARRICK: Yes, please.

24 THE COURT REPORTER: And do you
25 need regular delivery of the final?

1 ATTORNEY WARRICK: That's fine.

2 THE COURT REPORTER: Okay.

3 THE VIDEOGRAPHER: And Counsel, I
4 apologize but I have to ask again: Does anyone
5 need a copy of the video?

6 ATTORNEY CHANDLER: My answer
7 will be the same unclear answer, which is:
8 Eventually yes, but not right now.

9 THE VIDEOGRAPHER: Perfect.
10 That's fine.

11 Mr. Warrick, sir?

12 ATTORNEY WARRICK: Not at this
13 time.

14 THE VIDEOGRAPHER: Thank you very
15 much.

16 This concludes today's deposition
17 of Steven Przybylski, Volume 2. We're off the
18 video record at 3:29 p.m. Pacific Time on
19 February 16th.

20 (Whereupon, at 3:29 p.m. the
21 proceedings concluded.)
22
23
24
25

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C E R T I F I C A T I O N

I hereby certify that I have
read the foregoing transcript of my deposition
testimony, and that my answers to the questions
propounded, with the attached corrections or
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STEVEN PRZYBYLSKI, PH.D.,

CERTIFICATE OF SHORTHAND REPORTER

I, Gail Inghram Verbano,
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Gail Inghram Verbano, CSR, RDR, CRR
CA-CSR No. 8635