

1 UNITED STATES PATENT AND TRADEMARK OFFICE

2 BEFORE THE PATENT TRIAL AND APPEAL BOARD

3 IPR2022-00615

4 Patent 7,619,912 B2

5
6 SAMSUNG ELECTRONICS CO., LTD.,)
MICRON TECHNOLOGY, INC., MICRON)
7 SEMICONDUCTOR PRODUCTS, INC., and)
MICRON TECHNOLOGY TEXAS LLC,)

8 Petitioner,)

9 vs.)

10 NETLIST, INC.,)

11 Patent Owner.)
12)
13)

14
15 - - - -

16 REMOTE

17 EXPERT WITNESS TESTIMONY OF

18 MICHAEL CHARLES BROGIOLI

19 (Pages 1 - 238)

20 Tuesday, October 3, 2023, 8:01 a.m.

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22
23

24 REPORTED BY: ELAINA BULDA-JONES, CSR 11720
25

APPEARANCES

For SAMSUNG ELECTRONICS CO., LTD., MICRON
TECHNOLOGY, INC., MICRON SEMICONDUCTOR PRODUCTS,
INC., and MICRON TECHNOLOGY TEXAS LLC:

BY: THEODORE W. CHANDLER, ESQ.
BY: FERENC PAZMANDI, ESQ.
Baker Botts LLP
101 California Street, Suite 3200
San Francisco, California 94111-5802
415.291.6259
Ted.chandler@bakerbotts.com
Ferenc.pazmandi@bakerbotts.com

For NETLIST, INC.:

BY: MICHAEL TEZYZAN, ESQ.
Irell & Manella LLP
1800 Avenue of the Stars, Suite 900
Los Angeles, California 90067
310.203.7536
Mtezyan@irell.com

Also present:

Dana Bachmann, videographer

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1 THE VIDEOGRAPHER: Good morning. We're
2 now on the record at 8:01 a.m. Pacific time on
3 October 3rd, 2023.

4 This begins the videoconference deposition
5 of Michael C. Brogioli taken in the matter of
6 Samsung Electronics Company, LTD, et al., versus
7 Netlist Incorporated filed in the U.S. Patent and
8 Trademark Office Patent Trial and Appeal Board.
9 Case number IPR 2022-00615.

08:01

10 My name is Dana Bachmann. I'm your
11 videographer today. Our court reporter is Elaina
12 Bulda-Jones. We're both representing Esquire
13 Deposition Solutions.

08:02

14 Will all present please identify
15 themselves beginning with our witness Mr. Brogioli.

08:02

16 THE WITNESS: Michael Charles Brogioli.

17 THE VIDEOGRAPHER: Thank you.
18 Counsel, please.

19 MR. CHANDLER: Good morning. This is Ted
20 Chandler from the law firm of Baker Botts on behalf
21 of the petitioner Samsung Electronics Co., Limited.
22 And with me is my colleague Dr. Ferenc Pazmandi.

08:02

23 MR. TEZYAN: This is Michael Tezyan of
24 Irell & Manella on behalf of patent owner Netlist.

25 Before we get started I'd just like to

08:02

1 point out, I don't see anything on the realtime
2 right now.

3 (Whereupon, a brief discussion off the
4 record.)

5 THE VIDEOGRAPHER: Off the record at 08:03
6 8:03 a.m. Pacific time.

7 (Whereupon, a brief recess was taken.)

8 THE VIDEOGRAPHER: On the record at
9 8:12 a.m. Pacific time.

10 Madam Reporter, would you kindly swear in 08:12
11 our witness.

12 MICHAEL CHARLES BROGIOLI,
13 called as a witness by the Petitioner herein, being
14 first duly sworn by the Certified Shorthand Reporter
15 was thereupon examined and testified as is
16 hereinafter set forth.

17 EXAMINATION

18 BY MR. CHANDLER:

19 Q. Please state your name for the record.

20 A. Michael Charles Brogioli. 08:13

21 Q. What do you do for a living, Dr. Brogioli?

22 A. I work as an engineering consultant and
23 also as an adjunct professor of electrical and
24 computer engineering.

25 Q. Dr. Brogioli, were you retained by Netlist 08:13

1 to provide opinions in this case related to
2 Netlist's '912 patent?

3 A. Yes, that's correct.

4 Q. And the '912 patent has been premarked as
5 Exhibit 1001 and is U.S. Patent Number 7,619,912,
6 correct?

08:13

7 A. That's correct.

8 (Whereupon, Exhibit 1001, having been
9 previously marked, was referenced.)

10 BY MR. CHANDLER:

08:13

11 Q. Given that this is a remote deposition,
12 meaning we're not in the same physical room
13 together, there are a few questions I need to ask
14 starting with where are you physically located right
15 now during this deposition?

08:14

16 A. I am in Austin, Texas, at a private home
17 office in my home.

18 Q. Is there anyone else in the room with you
19 right now?

20 A. No, there's not.

08:14

21 Q. Given that I cannot see the room that
22 you're in, will you please let us know if someone
23 enters the room you're in at any time before this
24 deposition ends?

25 A. Yes, I will.

08:14

1 Q. Did you bring anything with you to your
2 deposition today?

3 A. No physical materials. I have a copy of
4 my declaration and probably the patent and I think
5 the Perego reference, which I think you've already
6 sent this morning. 08:14

7 Other than that, no, I have nothing with
8 me.

9 Q. Given that I cannot see whether you have
10 anything in front of you, will you please let us
11 know if you or anyone else puts anything in front of
12 you at any time before the deposition ends? 08:14

13 A. Yes.

14 Q. And is there anything on your computer
15 screen right now besides the video feed and the
16 exhibits for this case? 08:15

17 A. No.

18 Q. I will take breaks throughout the
19 deposition. But I want to remind you that during
20 those breaks, you should not consult with your
21 counsel about the substance of your testimony. 08:15

22 Do you understand?

23 A. I do, yes.

24 Q. And during the deposition I'd ask you do
25 not look things up on the internet or do other 08:15

1 things on your computer or your phone that we cannot
2 see on the camera.

3 Do you understand?

4 A. Yes, I do.

5 Q. And you also understand that during your
6 deposition you should not be e-mailing or texting
7 other people?

08:15

8 A. Yes.

9 Q. Approximately how many times have you been
10 deposed before?

08:15

11 A. I think on the range of 45, maybe a little
12 bit more than that.

13 Q. And do you have any questions for me about
14 the procedure for today's deposition?

15 A. Not at this time, no.

08:16

16 Q. What did Netlist ask you to do in this
17 matter?

18 A. As I recall, it was to address certain
19 opinions that I believe Samsung's expert, Dr. Wolfe,
20 had offered in regard to the '912 patent.

08:16

21 Q. Did anyone help you with your work in this
22 matter?

23 A. In forming my opinions, no.

24 Q. What did you do to prepare for today's
25 deposition?

08:16

1 A. I would say fairly standard preparation
2 procedure. I reviewed my declaration, the patent,
3 certain of the references I discuss in my
4 declaration, perhaps portions of Dr. Wolfe's
5 declaration, things of that nature, and also met
6 briefly your -- with counsel, I think it was
7 yesterday.

08:16

8 Q. And who did you meet with?

9 A. It was Michael Tezyan and Annita Zhong.

10 Q. And how long was that meeting?

08:17

11 A. About a half day or so.

12 Q. All right. And then did you also prepare
13 on your own for today's deposition?

14 A. I did, yes.

15 Q. And approximately how many hours have you
16 prepared over the past week or two for today's
17 deposition?

08:17

18 A. So I'll say it will be listed in my
19 invoices. I know I've prepared over this past
20 weekend and perhaps late last week and then had done
21 some preparation some days prior to that. I
22 speculate maybe in the order of 30 or 40 hours,
23 maybe, something in that range, or perhaps a little
24 more than that.

08:17

25 Q. Are there any documents that you reviewed

08:18

1 in preparation for your deposition today that were
2 not already produced as exhibits in the IPR or
3 produced as papers in the IPR?

4 A. Not that I can remember, no. I don't
5 think so.

08:18

6 Q. As part of your work for Netlist on this
7 matter, did you personally talk to anyone outside of
8 the Irell law firm such as the inventors or anyone
9 with expertise in the field?

10 A. No.

08:18

11 Q. How much are you charging Netlist per hour
12 for your time spent on this matter?

13 A. It is \$700 per hour, if I remember
14 correctly.

15 Q. Approximately how many hours have you
16 spent working as an expert for Netlist on the '912
17 patent?

08:18

18 A. That's difficult for me to answer in the
19 sense that, if I recall, I had started doing some
20 preliminary work on this a number of months ago.
21 Maybe even early this year, if not earlier than
22 that. I would have to go back to my invoices on
23 that for you.

08:19

24 Q. Would it be fair to say that you spent
25 time on the '912 patent for both this matter as well

08:19

1 as a corresponding district court action?

2 MR. TEZYAN: Object to form.

3 THE WITNESS: I don't recall. I more
4 specifically recall my work on the '912 relating to
5 this IPR.

08:19

6 BY MR. CHANDLER:

7 Q. Approximately how many hours have you
8 spent working as an expert for Netlist in any matter
9 against Samsung?

10 MR. TEZYAN: Object to form.

08:20

11 THE WITNESS: I -- I don't know. That's
12 tough for me to estimate. But, again, it should be
13 very clearly listed in the invoices.

14 BY MR. CHANDLER:

15 Q. You were the expert at trial against
16 Samsung, correct?

08:20

17 A. That's correct, yes.

18 Q. Would it be fair to say that since 2021
19 you have been paid over \$200,000 by Netlist to work
20 on matters against Samsung?

08:20

21 MR. TEZYAN: Object to form.

22 THE WITNESS: I -- I would point us back
23 to my invoices but that -- that doesn't sound
24 unreasonable to me, given the amount of time I've
25 been working on various -- various matters that were

08:20

1 averse to Samsung.

2 BY MR. CHANDLER:

3 Q. Before this case, when did you first do
4 any work for Netlist?

5 A. I think it was --

08:21

6 Q. If it helps, your declaration,
7 Exhibit 2062, has been put in the chat earlier.
8 (Whereupon, Exhibit 2062, having been
9 previously marked, was referenced.)

10 THE WITNESS: Oh, okay. So it should be
11 on my CV at the very end here. Let me pull that up
12 for you.

08:21

13 So I'm on page 214 of the 225 pages in
14 Exhibit 2062. And at the very bottom there's a
15 Netlist versus SK hynix matter that I began work on
16 in 2016 of that year. And I -- that -- that should
17 be the first time that I did any work relating to
18 Netlist.

08:22

19 BY MR. CHANDLER:

20 Q. And you're referring to ITC investigation
21 number 337-TA-1023?

08:13

22 A. That's correct.

23 Q. Before you were first engaged by Netlist
24 around 2016 or 2017, did you know any of the named
25 inventors on the '912 patent identified as Jayesh R.

08:22

1 Bhakta and Jeffrey C. Solomon?

2 MR. TEZYAN: Object to form.

3 THE WITNESS: I don't recall knowing them
4 or having met them personally. Whether or not I had
5 come across their names prior to that, I don't
6 remember.

08:23

7 BY MR. CHANDLER:

8 Q. Have you ever met any of the named
9 inventors on the '912 patent?

10 A. I don't think so. And the only -- the
11 only reason I say that is when this Netlist and
12 SK hynix trial took place in what was probably 2017,
13 I remember there being various people from Netlist
14 at the time present. I certainly didn't have any
15 conversations of any, you know, technical substance
16 or anything with people but perhaps they were
17 present there.

08:23

18 Q. Is your expert declaration marked as
19 Exhibit 2062 complete, meaning does it provide a
20 complete statement of all the opinions you intend to
21 express in this IPR along with the basis and reasons
22 for those opinions?

08:23

23 MR. TEZYAN: Object to form.

24 THE WITNESS: I would say sitting here
25 today, yes, it does.

08:24

1 BY MR. CHANDLER:

2 Q. Is your expert declaration marked as
3 Exhibit 2062 accurate, meaning it does not have any
4 mistakes as far as you know?

5 A. That's correct, short of maybe a typo or 08:24
6 two. I think I spelled Perego wrong once or twice.

7 Q. Do you have any present plans to correct
8 or supplement your expert declaration marked as
9 Exhibit 2062?

10 A. No, I don't. 08:24

11 Q. And does the CV at the end of your expert
12 declaration marked as Exhibit 2062 list all of your
13 prior expert engagements in which you were either
14 deposed or testified at trial?

15 A. As of the date on this CV, it should, yes. 08:24

16 Q. Have you carefully read Netlist's '912
17 patent marked as Exhibit 1001?

18 A. Yes, I have.

19 Q. Do you believe you understand the '912
20 patent? 08:25

21 A. Yes, and certainly in the context at any
22 of the aspects of it that I discuss in my report,
23 yes.

24 Q. Do you believe you understand the figures
25 of the '912 patent? 08:25

1 A. Yes, I do.

2 Q. And do you believe you understand the
3 claims at the end of the '912 patent?

4 A. The ones that I discuss in my declaration,
5 yes, I do. 08:25

6 Q. So specifically, Claim 16 in the '912
7 patent you understand, correct?

8 A. That's correct.

9 Q. Please turn to Exhibit 1035. Let me know
10 when you're there. 08:25

11 (Whereupon, Exhibit 1035, having been
12 previously marked, was referenced.)

13 THE WITNESS: Okay.

14 BY MR. CHANDLER:

15 Q. Have you carefully read the Perego prior
16 art reference marked as Exhibit 1035? 08:25

17 A. Yes, I have.

18 Q. And do you believe you understand the
19 Perego prior art reference marked as Exhibit 1035?

20 A. I would say yes in -- in terms of the --
21 the aspects of it I discuss in my report, but I have
22 read the entire reference, yes. 08:26

23 Q. Please turn to Exhibit 1036. Let me know
24 when you're there.

25 (Whereupon, Exhibit 1036, having been 08:26

1 previously marked, was referenced.)

2 THE WITNESS: Okay.

3 BY MR. CHANDLER:

4 Q. Have you carefully read the Amidi prior
5 art reference marked as Exhibit 1036?

08:26

6 A. Yes, I have.

7 Q. Do you believe you understand the Amidi
8 prior art reference marked as Exhibit 1036?

9 A. Yes, I do, and I would say certainly in
10 terms of the aspects I discuss in my declaration.

08:26

11 Q. Please turn to Exhibit 1037. Let me know
12 when you're there.

13 (Whereupon, Exhibit 1037, having been
14 previously marked, was referenced.)

15 THE WITNESS: Okay.

08:26

16 BY MR. CHANDLER:

17 Q. Have you carefully read the Ellsberry
18 prior art reference marked as Exhibit 1037?

19 A. Yes, I have.

20 Q. Do you believe you understand the
21 Ellsberry prior art reference marked as
22 Exhibit 1037?

08:27

23 A. Yes, I do, in the context of the aspects I
24 talk about in my declaration, sure.

25 Q. Please turn to Exhibit 1030. Let me know

08:27

1 when you're there.

2 (Whereupon, Exhibit 1030, having been
3 previously marked, was referenced.)

4 THE WITNESS: Okay.

5 BY MR. CHANDLER:

08:26

6 Q. Have you carefully read the JESD79 JEDEC
7 standard marked as Exhibit 1030?

8 A. Yes, I have.

9 Q. Do you believe you understand the JESD79
10 JEDEC standard marked as Exhibit 1030?

08:27

11 A. Yes, I do. And I'd say more specifically
12 the portions I discuss in my declaration.

13 Q. Please turn to Exhibit 1032. Let me know
14 when you're there.

15 (Whereupon, Exhibit 1032, having been
16 previously marked, was referenced.)

08:28

17 THE WITNESS: Okay.

18 BY MR. CHANDLER:

19 Q. Have you carefully read the JEDEC 21-C
20 standard marked as Exhibit 1032?

08:28

21 A. Yes, I have.

22 Q. And do you believe you understand the
23 JEDEC 21-C standard marked as Exhibit 1032?

24 A. Yes, I do. And more specifically,
25 portions I discuss in my declaration.

08:28

1 Q. Please turn to Exhibit 1029. Let me know
2 when you're there.

3 (Whereupon, Exhibit 1029, having been
4 previously marked, was referenced.)

5 THE WITNESS: Okay.

08:26

6 BY MR. CHANDLER:

7 Q. Have you carefully read the JESD79-2 JEDEC
8 standard marked as Exhibit 1029?

9 A. Yes, I have.

10 Q. And do you believe you understand the
11 JESD79-2 JEDEC standard marked as Exhibit 1029?

08:28

12 A. Yes, I do. And specifically portions I
13 discuss in my declaration.

14 Q. Please turn to paragraph 18 of your expert
15 declaration marked as Exhibit 2062. Let me know
16 when you're there. It's on page 8.

08:29

17 A. Okay.

18 Q. At the end --

19 A. Go ahead.

20 Q. -- of paragraph 18 you state that you are
21 applying the level of ordinary skill in the art
22 proposed by Samsung, correct?

08:29

23 A. That's correct.

24 Q. Now, Samsung has taken the position that
25 the effective filing date for Claim 16 of the '912

08:29

1 patent is no earlier than July 1st, 2005, while I
2 understand that you contend Claim 16 is entitled to
3 a priority date in 2004.

4 In paragraph 19 of your declaration, you
5 refer to the, quote, 2004 to 2000 [sic] time frame,
6 end quote, when discussing the person of ordinary
7 skill in the art.

08:29

8 So my question for you is whether there is
9 a material difference in terms of the level of skill
10 between 2004 and 2005, in your opinion?

08:30

11 MR. TEZYAN: Object to form.

12 THE WITNESS: I would say in the context
13 of my declaration, I don't denote a difference
14 between the person of skill in the art in that year
15 or so time frame.

08:30

16 BY MR. CHANDLER:

17 Q. Unless stated otherwise, could you please
18 answer my questions today from the perspective of a
19 person of ordinary skill in the art in the 2004 to
20 2005 time frame?

08:30

21 A. Yes.

22 Q. Could you also please answer my questions
23 today in a way that's consistent with the ordinary
24 and accustomed meaning of words to a person of
25 ordinary skill in the art in the 2004 to 2005 time

08:31

1 frame?

2 A. Yes.

3 MR. CHANDLER: I'd like to introduce a new
4 exhibit. It will be 1103.

5 (Whereupon, Exhibit 1103 was marked for
6 identification.)

7 BY MR. CHANDLER:

8 Q. I'm putting it in the chat and let me know
9 when you have it open.

10 A. Okay.

11 Q. Exhibit 1103 is Netlist's technology
12 tutorial in the case where you were the expert
13 witness in the area of JEDEC standard essential DRAM
14 memory technology related to DIMM, RDIMM, and LRDIMM
15 memory modules, correct?

16 MR. TEZYAN: Object to form.

17 THE WITNESS: I would say my recollection
18 of this reference is a -- it's a technology tutorial
19 that, as I remember, was presented at this hearing
20 in 2017.

21 BY MR. CHANDLER:

22 Q. In ITC investigation number 337-TA-1023,
23 correct?

24 A. That's correct, yes.

25 Q. And in that ITC investigation, you were

1 the expert witness in the area of JEDEC standard
2 essential DRAM memory technology related to DIMM,
3 RDIMM, and LRDIMM memory modules, correct?

4 MR. TEZYAN: Object to form.

5 THE WITNESS: That sounds generally right. 08:32
6 I know I have a description of -- a high level
7 description of my role in my CV. But that sounds
8 like at least somewhat in line with the subject
9 matter I was testifying on.

10 BY MR. CHANDLER: 08:33

11 Q. And you've seen Exhibit 1103 before,
12 correct?

13 A. Yes, I have.

14 Q. Please turn to page 2 of Exhibit 1103 and
15 let me know when you're there. 08:33

16 A. Okay.

17 Q. Does page 2 of Exhibit 1103 show a picture
18 of a DIMM, which is to say a dual in-line memory
19 module?

20 A. It shows in the visualization on the right 08:33
21 component referred to as a memory module. And then
22 the language describing memory modules refers to
23 DIMMs, or dual in-line memory modules, as there's
24 in-line connections on each side of the module.

25 Q. Does page 3 of Exhibit 1103 also show a 08:33

1 DIMM memory module at the bottom?

2 A. Perhaps. I -- I see it's only visualizing
3 one side of a memory module here. I don't see that
4 the slide says "DIMM." But perhaps that's what it
5 is.

08:34

6 Q. Do you agree that SDRAM memory devices
7 emerged in the 1990s and have been standardized by
8 JEDEC?

9 A. That's correct, yes.

10 Q. Do you agree that SDRAM has evolved in
11 several generations including DDR and DDR2 and more
12 recently DDR3 and DDR4?

08:34

13 A. That's right, yes.

14 Q. Do you agree that DDR and DDR2 were JEDEC
15 standards that a person of ordinary skill in the art
16 knew about at the time of the '912 patent?

08:35

17 A. Yes, that sounds right.

18 Q. Could you pull up Exhibit 1029 again.

19 A. Okay.

20 Q. You do not dispute that a person of
21 ordinary skill in the art would have known about the
22 JEDEC standard JESD79-2 marked as Exhibit 1029,
23 correct?

08:35

24 A. That's correct. No, that sounds correct,
25 yes.

08:35

1 Q. And pull up Exhibit 1030 again.

2 A. Okay.

3 Q. You do not dispute that a person of
4 ordinary skill in the art would have known about the
5 JEDEC standard JESD79 marked as Exhibit 1030,
6 correct? 08:35

7 A. No, I don't dispute that.

8 MR. CHANDLER: I want to mark a new
9 exhibit. It will be 1104.

10 (Whereupon, Exhibit 1104 was marked for
11 identification.) 08:36

12 BY MR. CHANDLER:

13 Q. And let me know when you have it open.

14 A. Okay.

15 Q. Exhibit 1104 is the JESD79D JEDEC standard
16 for DDR memory devices dated January 2004, correct? 08:36

17 A. That's correct, yes.

18 Q. And you do not dispute that a person of
19 ordinary skill in the art would have known about the
20 JEDEC standard JESD79D dated January 2004 marked as
21 Exhibit 1104, correct? 08:36

22 A. As of this January 2004 date, yes.

23 Q. And pull up Exhibit 1032, please.

24 A. Okay.

25 Q. You do not dispute that a person of 08:37

1 ordinary skill in the art would have known about the
2 JEDEC standard 21-C marked as Exhibit 1032, correct?

3 A. That's correct, I'm not disputing that.

4 Q. Putting in the chat two exhibits that you
5 had previously marked.

08:37

6 Can you pull up Exhibit 2049 and let me
7 know when you have it open.

8 (Whereupon, Exhibit 2049, having been
9 previously marked, was referenced.)

10 THE WITNESS: Okay.

08:26

11 BY MR. CHANDLER:

12 Q. You do not dispute person of ordinary
13 skill in the art would have known about the JEDEC
14 standard 21-C Revision 1.4 marked as Exhibit 2049,
15 correct?

08:38

16 A. That's correct. I'm not disputing that.

17 Q. And if you turn to Exhibit 2050, let me
18 know when you have that open.

19 (Whereupon, Exhibit 2050, having been
20 previously marked, was referenced.)

08:38

21 THE WITNESS: Okay.

22 BY MR. CHANDLER:

23 Q. You do not dispute that a person of
24 ordinary skill in the art would have known about the
25 JEDEC standard 21-C Revision 1.4 dated February 2002

08:38



1 marked as Exhibit 2050, correct?

2 A. That's correct.

3 Q. All right. Please turn back to
4 Exhibit 1103. Let me know when you're there.

5 A. Okay.

08:38

6 Q. Page 5 of Exhibit 1103 shows an
7 illustration of a DIMM memory module with two ranks
8 labeled "Rank 0" in red and "Rank 1" in green,
9 correct?

10 A. That looks to be what this tutorial slide
11 is illustrating.

08:39

12 Q. Do you agree that a rank is a set of DRAMs
13 that are written to or read from together?

14 MR. TEZYAN: Object to form.

15 THE WITNESS: A rank is a set of DRAMs and
16 they can be written to or read from together, as is
17 described in this slide.

08:39

18 BY MR. CHANDLER:

19 Q. Now, you have offered the opinion in this
20 IPR that the term "rank" requires more than one
21 memory device, correct?

08:40

22 A. That's correct.

23 Q. And you understand that Samsung's expert,
24 Dr. Wolfe, disagrees with you and has offered the
25 opinion that the term "rank" includes one or more

08:40

1 memory devices, correct?

2 A. That's my -- my general recollection, yes.

3 Q. In forming your validity opinions for this
4 IPR, you used your claim construction for rank
5 requiring more than one memory device, not
6 Dr. Wolfe's claimed construction for rank, correct?

08:40

7 MR. TEZYAN: Object to form of the
8 question.

9 THE WITNESS: I would say that I used my
10 definition of a rank throughout my declaration.
11 However, I -- I believe there are certain sections
12 in my declaration where I also address Dr. Wolfe's
13 definition.

08:40

14 BY MR. CHANDLER:

15 Q. And you addressed his definition to
16 disagree with it, correct?

08:41

17 MR. TEZYAN: Object to form.

18 THE WITNESS: I think in certain -- well,
19 yeah, I do disagree with his definition, but I think
20 there are sections of the declaration addressing why
21 certain limitations aren't met even using
22 Dr. Wolfe's definition.

08:41

23 BY MR. CHANDLER:

24 Q. And do you have any particular limitations
25 in mind as what you're referring to?

08:41

1 A. We'd need to go back to the declaration.
2 But one example, as I recall, may be in
3 reference to Perego and the number of -- I think
4 what Dr. Wolfe alleges are DRAM devices per rank not
5 being met. But it should all be in the declaration
6 itself.

08:42

7 Q. Turn to page 7 of Exhibit 1103 and let me
8 know when you're there.

9 Actually, I apologize, stick on page 5 of
10 1103. Do you still have that page in front of you?

08:42

11 A. Okay.

12 Q. Do you agree that at the time of the '912
13 patent, the term "bank" or "physical bank" was
14 sometimes used to mean the same thing as the term
15 "rank"?

08:42

16 MR. TEZYAN: Object to form.

17 THE WITNESS: That in certain references,
18 and I forget the exact -- the exact dates of them,
19 the term "bank" was sometimes used in a similar
20 context to rank. And I believe I -- I talked about
21 that in certain -- at certain points along the way.
22 I believe Dr. Wolfe has as well.

08:43

23 As for the dates of those specific
24 references, I -- I don't recall from memory.

25 BY MR. CHANDLER:

08:43

1 Q. And the term "physical bank" was also used
2 sometimes to mean the same as the term "rank"; is
3 that correct?

4 MR. TEZYAN: Object to form.

5 THE WITNESS: I -- I don't recall if the 08:43
6 physical qualifier was in the reference that I've --
7 I'm recalling from memory. But there was some --
8 there were some examples of the use of "bank" and
9 "rank" used in -- in sort of a less than accurate
10 manner, I would say. 08:44

11 BY MR. CHANDLER:

12 Q. For example, Exhibit 1032 is the
13 JEDEC 21-C standard and it uses the phrase "physical
14 bank." Whereas today we would use the term "rank"
15 to refer to the same concept, correct? 08:44

16 MR. TEZYAN: Object to form.

17 THE WITNESS: I would say the Exhibit 1032
18 uses the phrase "physical bank" at various places.
19 I haven't gone through the reference to see how that
20 relates or doesn't relate to the phrase "rank" 08:44
21 necessarily.

22 BY MR. CHANDLER:

23 Q. Turn to page 7 of Exhibit 1103. Let me
24 know when you're there.

25 A. Okay. 08:44

1 Q. Page 7 of Exhibit 1103 illustrates an
2 unbuffered DIMM, also known as a UDIMM, correct?

3 A. That looks to be what this tutorial slide
4 is illustrating, or aspects of.

5 Q. In your opinion, did a person of ordinary 08:45
6 skill in the art know about UDIMM memory modules?

7 A. As I recall, they would have, yes.

8 Q. In a UDIMM the memory controller directly
9 controls the DRAM memory devices without the use of
10 any buffers on the memory module for any of the 08:45
11 signals from the memory controller, correct?

12 MR. TEZYAN: Object to form.

13 THE WITNESS: I believe what this slide is
14 showing is that the -- in this UDIMM tutorial slide
15 the memory controller's address, command, clock, and 08:46
16 the data lines are DQ, DQS, are communicated between
17 the memory controller and the memory devices
18 themselves. There aren't intermediate components,
19 is what the slide seems to be showing.

20 BY MR. CHANDLER: 08:46

21 Q. And in particular there are no
22 intermediate buffers for those signals on the memory
23 module, correct?

24 A. I -- I don't see that shown in the slide.
25 And that sounds right. 08:46

1 Q. On page 8 of Exhibit 1103, do you agree
2 there is shown a registered DIMM, also known as an
3 RDIMM?

4 A. That's what this high level slide is
5 illustrating aspects of, yes. 08:46

6 Q. In your opinion, did a person of ordinary
7 skill in the art know about RDIMM memory modules?

8 A. Yes, they would have known about JEDEC
9 literature on the RDIMM.

10 Q. An RDIMM memory module has a register on 08:47
11 the memory module for address, command, and clock
12 signals but not the data signals labeled "DQ" or the
13 stroke signals labeled "DQS," correct?

14 A. At a high level, that's correct. And
15 that's also in line with what this slide is showing, 08:47
16 or teaching.

17 Q. Page 9 of Exhibit 1103 illustrates a
18 fully-buffered DIMM, also known as an FBDIMM,
19 correct?

20 A. That's correct. 08:48

21 Q. In your opinion, did a person of ordinary
22 skill in the art know about FBDIMM memory modules?

23 A. I don't recall from memory the date of
24 FB-DIMMs or the material published on them. But
25 what this slide is -- in relation to the various 08:48

1 priority dates we discussed earlier. But this slide
2 is showing aspects of an FBDIMM, or fully-buffered
3 DIMM, and how the various signaling paths work.

4 Q. To refresh your recollection, could you
5 look at the '912 patent column 6, line 2, and let me
6 know when you're there. 08:48

7 A. I am. And I see that it mentions
8 fully-buffered DIMM, or FBDIMM.

9 Q. So in your opinion did a person of
10 ordinary skill in the art know about FBDIMM memory
11 modules? 08:49

12 A. That's correct. That sounds correct, yes.

13 Q. All right. Turning back to page 9 of
14 Exhibit 1103, the AMB on a fully-buffered DIMM
15 buffers all of the signals to and from the memory
16 controller, including data, address, command, and
17 clock signals, correct? 08:49

18 MR. TEZYAN: Object to form.

19 THE WITNESS: I would say in the FBM --
20 oh, I'm sorry -- in the FBDIMM design there is an
21 AMB, or advanced memory buffer, and there are -- the
22 type of information we see here that you just
23 mentioned, address, command, clock, come from the
24 memory controller into that AMB. And then there's
25 various, as we can see, the address, command, and 08:50

1 clock in red, or the data, DQ, DQS, in the orange
2 color going to the DRAM.

3 BY MR. CHANDLER:

4 Q. The AMB also buffers the data and strobe
5 signals coming from the memory controller to the
6 memory module, correct?

08:50

7 A. That the -- those signals also come from
8 the memory controller and go through the AMB in some
9 form, yes.

10 Q. What is the benefit of buffering the data
11 lines on a memory module such as an FBDIMM?

08:50

12 MR. TEZYAN: Objection. Form. And
13 objection relevance.

14 THE WITNESS: So I don't -- depending on
15 the context there may be various benefits in terms
16 of what an implementation requires or a system or a
17 design or...

08:50

18 I don't recall having gone through the
19 FBDIMM specification and pointing out various
20 benefits or drawbacks in my declaration.

08:51

21 BY MR. CHANDLER:

22 Q. Does buffering the data lines on a memory
23 module have the potential to reduce the electrical
24 load?

25 MR. TEZYAN: Same objection to form. And

08:51

1 objection to relevance as well.

2 THE WITNESS: You would have to look at a
3 specific reference to understand -- or a specific
4 scenario in terms of what buffering meant there or
5 how that system was implemented to see the -- what 08:51
6 benefits, if any, were -- were attributed to
7 something like that.

8 BY MR. CHANDLER:

9 Q. The '912 patent teaches using devices on
10 the memory module to buffer the data signal to 08:52
11 isolate the electrical load; is that correct?

12 MR. TEZYAN: Object to form.

13 THE WITNESS: I recall that the '912
14 mentions a concept of buffer in various places. I
15 don't recall addressing the '912's disclosure or not 08:52
16 disclosure of load or electrical load as you're --
17 as you're asking about.

18 I don't recall Dr. Wolfe -- at least
19 addressing opinions of Dr. Wolfe's that relate to
20 that either. 08:52

21 BY MR. CHANDLER:

22 Q. In the '912 patent column 25, lines 31 to
23 32, the '912 patent teaches reducing the load; is
24 that correct?

25 MR. TEZYAN: Object to form. 08:53

1 THE WITNESS: Let me take one second to
2 read it.

3 So it looks like this paragraph is saying
4 that in some of these embodiments the device 120 --
5 the isolation device 120 presents a reduced
6 impedance load to the computer system.

08:54

7 BY MR. CHANDLER:

8 Q. And what's the benefit of reducing the
9 load to the computer system?

10 MR. TEZYAN: Object to form. And to
11 relevance.

08:54

12 THE WITNESS: It looks like this paragraph
13 continues on to state -- roughly line 37 -- the --
14 "where the impedance load of the memory module may
15 otherwise limit the number of ranks or the number of
16 memory devices per memory module."

08:54

17 So it looks like in the context of that
18 sentence it's mentioning that by addressing the load
19 here you may be able to have more memory devices or
20 ranks.

08:55

21 BY MR. CHANDLER:

22 Q. Could you turn to paragraph 5 of your
23 expert declaration marked as Exhibit 2062. Let me
24 know when you're there.

25 A. Okay.

08:55

1 Q. Starting with paragraph 5 of your expert
2 declaration marked as Exhibit 2062 you describe your
3 qualifications and experience relevant to this IPR,
4 correct?

5 A. That's correct.

08:55

6 Q. In paragraph 8 of Exhibit 2062 you mention
7 that you worked for a company named Vicarious
8 Visions in the late 1990s, correct?

9 A. Correct.

10 Q. And page 201 of Exhibit 2062 provides some
11 more detail about your work for Vicarious Visions in
12 1999, correct?

08:55

13 A. That's correct.

14 Q. For example, you "coded innovative, highly
15 optimized assembly routines for real time speech and
16 full motion video on the console's limited Zilog Z80
17 processor resources," correct?

08:56

18 A. That's one of the roles I had, yes.

19 Q. The Zilog Z80 that you were working on had
20 a data bus for communicating with the memory devices
21 that was 8 bits wide, correct?

08:56

22 MR. TEZYAN: Object to form.

23 THE WITNESS: I don't recall specifically.
24 But that sounds reasonable.

25

1 BY MR. CHANDLER:

2 Q. Could you please pull up Exhibit 1034,
3 which I'll put in the chat, and let me know when you
4 have it open.

5 (Whereupon, Exhibit 1034, having been 08:57
6 previously marked, was referenced.)

7 THE WITNESS: Okay.

8 BY MR. CHANDLER:

9 Q. Exhibit 1034 is Professor Jacob's article
10 about synchronous DRAM architectures, correct? 08:57

11 A. Yes, it's one of his papers on -- that --
12 excuse me -- he has titled "Synchronous DRAM
13 Architectures, Organizations, and Alternative
14 Technologies."

15 Q. And you've read Exhibit 2030 -- 1034, 08:57
16 correct?

17 A. Yes, I -- I believe I have.

18 Q. At the bottom of page 2 of Exhibit 1034,
19 on the right, and carrying over to page 3, Professor
20 Jacob describes chip select signals, correct? 08:58

21 A. Let me read the paragraph for you. Okay.

22 It looks like this paragraph is talking
23 about some aspects of what Dr. Jacob is referring to
24 chip select bus or chip select.

25 Q. And is the description provided by 08:59

1 Professor Jacob at the bottom of page 2 of
2 Exhibit 1034, carrying over to page 3, consistent
3 with your understanding of what a person of ordinary
4 skill in the art knew about the chip select bus?

5 MR. TEZYAN: Object to form.

08:59

6 THE WITNESS: I would say in reading this
7 paragraph now, the description of chip select seems
8 in line with what the paper is probably trying to
9 address in terms of things like a JEDEC-style memory
10 system or other aspects of what -- what Professor
11 Jacob is talking about here.

09:00

12 BY MR. CHANDLER:

13 Q. On page 3 of Exhibit 1034 -- I apologize.

14 It's actually, I guess, the bottom of
15 page 2 of Exhibit 1034, Professor Jacob explains
16 that, "The chip select bus contains a separate wire
17 for every rank of DRAM in the system," correct?

09:00

18 A. It looks like -- so I see that sentence.
19 It's about the fourth line down in this paragraph.
20 And it seems to be talking about that, for what
21 Dr. Jacob is referring to as JEDEC style -- in a
22 JEDEC-style memory system within this paragraph.

09:00

23 Q. So in a JEDEC-style memory system, do you
24 agree that it's typical for the chip select bus to
25 contain a separate wire for every rank of DRAM in

09:01

1 the system?

2 MR. TEZYAN: Object to form.

3 THE WITNESS: I don't know that I an
4 formed opinion on that one way or the other in my
5 declaration.

09:01

6 But the concept of a chip select being
7 used for the various memory devices in a rank on a
8 memory module is -- is similar to what we were
9 discussing earlier this morning.

10 BY MR. CHANDLER:

09:01

11 Q. On page 3 of Exhibit 1034, Professor Jacob
12 states, quote, Even though all DRAMs in the system
13 are connected to the same address and control busses
14 and could, in theory, all respond to the same
15 request at the same time, the chip select bus
16 prevents this from happening, end quote.

09:02

17 Did I read that accurately?

18 A. You did.

19 Q. And is that description by Professor Jacob
20 consistent with what you believe a person of
21 ordinary skill in the art would have known at the
22 time for JEDEC-style memory systems?

09:02

23 A. I would say as a high level concept taken
24 in the context of this paragraph, or reference, yes,
25 it's teaching that -- or it seems to be explaining

09:02

1 that there is a same address and control bus and the
2 chip select, just as it says, "in theory, all
3 respond to the same request at the same time, the
4 chip select bus prevents this from happening."

5 So that seems to be, I would say, in line 09:03
6 with various concepts in this paper.

7 Q. Is it conventional for all memory devices
8 on a memory module to receive the same address
9 signals even if those memory devices are in
10 different ranks as suggested here by Professor 09:03
11 Jacob?

12 MR. TEZYAN: Object to form.

13 THE WITNESS: I'm not quite sure I'm
14 following your question.

15 BY MR. CHANDLER: 09:03

16 Q. Is it fair to say Professor Jacob is
17 teaching, at the top of page 3, that normally all
18 memory devices on the memory module receive the same
19 address signals even when those memory devices are
20 in different ranks? 09:04

21 MR. TEZYAN: Object to form.

22 THE WITNESS: So it looks to me the
23 Figure 3, at the top of page 3, is illustrating that
24 each of the memory modules on the right are
25 connected to the same DRAM bus coming from the north 09:04

1 bridge and memory controller and so there would be
2 one set of values on that bus with various other
3 components like memory modules connected to it.

4 BY MR. CHANDLER:

5 Q. Turn to page 9 of Exhibit 1034 and let me 09:05
6 know when you're there.

7 A. Okay.

8 Q. In a JEDEC-style memory module, the
9 address signals go to all the memory devices even if
10 those memory devices are in different ranks, 09:06
11 correct?

12 MR. TEZYAN: Object to form of the
13 question.

14 THE WITNESS: I would need to look at a
15 specific JEDEC reference, but there are address 09:06
16 signals that I recall -- excuse me -- go to -- or
17 each of the DRAM devices, for instance, if they're
18 performing a read command or a write command, are
19 using address signals that they're receiving.

20 In terms of the signaling topology of all 09:06
21 JEDEC memory devices, I don't recall all of that
22 from memory. We'd have to look at a specific
23 reference.

24 BY MR. CHANDLER:

25 Q. So for example, if we look at 09:06

1 Exhibit 1032, the JEDEC 21-C standard, for example,
2 on page 12 of Exhibit 1032, the bottom left shows
3 that all address signals A0 through A13 are sent to
4 all the memory devices D0 through D17, correct, as
5 opposed to, for example, some subset of address
6 lines going to some subset of memory devices and
7 some different subset of address lines going to some
8 different subset of memory devices. Instead, all
9 the address lines go to all the memory devices even
10 if those memory devices are in different ranks,
11 correct?

09:07

09:07

12 MR. TEZYAN: So object to form.

13 THE WITNESS: Give me a second. I was
14 trying to find the page numbers to get to your
15 figure.

09:08

16 And you're on -- just to be clear, you're
17 on page 12 of 82 in the PDF, correct?

18 BY MR. CHANDLER:

19 Q. Yes.

20 So the bottom left of page 12 of
21 Exhibit 1032, as an example, shows that all the
22 address lines A0 through A13 provides address
23 signals to all the memory devices D0 through D17
24 even though some of those memory devices are in
25 different ranks from each other, correct?

09:08

09:08

1 MR. TEZYAN: Object to form.

2 THE WITNESS: So it looks like this page
3 is describing, in the lower left, the register block
4 with the A0 through A13 coming in and it looks like
5 RA0 through RA13 going out. 09:09

6 And after the colon, it shows SDRAMs D0
7 through D17, which seem to be the list of -- of DRAM
8 device square shown in this figure starting with D0
9 in the upper left through D17 I guess on the bottom
10 portion. 09:09

11 BY MR. CHANDLER:

12 Q. And similarly, the RAS, CAS, and WE
13 control signals are sent to all the memory devices
14 D0 through D17 even though some of those memory
15 devices are going to be in a different rank from 09:10
16 each other, correct?

17 MR. TEZYAN: Object to form.

18 THE WITNESS: So I would say and I'll --
19 and I'll -- this will apply to my previous answer,
20 the A0 through A13 address lines come into the 09:10
21 register. It appears that another signal, RA0
22 through RA13, are on the outbound side.

23 When we -- so to your most recent
24 question, still staying on the lower left of this
25 figure, we see what -- what's coming into the 09:10

1 register block as the RAS, R-A-S, C-A-S, and W-E.
2 And there are outbound what look like signals
3 generated here called RRAS, RCAS, and RWE, on the
4 outbound side. But it -- and it illustrates,
5 similar to my previous answer, there's a colon SDRAM
6 D0 through D17 for each of those outbound signals.

09:11

7 BY MR. CHANDLER:

8 Q. So the registered version of the address
9 signals RAS, CAS, and WE is sent to all the memory
10 devices, D0 through D17, even though some of those
11 memory devices will be in different ranks from each
12 other, correct?

09:11

13 MR. TEZYAN: Object to form.

14 THE WITNESS: It looks like it's -- it's
15 showing that the outbound RRAS, for example,
16 outbound from the register, connects to -- if --
17 going on this, the syntax of this figure, the SDRAM
18 D0 through D17.

09:11

19 BY MR. CHANDLER:

20 Q. And turning back to the Jacob paper marked
21 Exhibit 1034, what's shown in the JEDEC standard
22 21-C marked as Exhibit 1032, that we just discussed,
23 is consistent with what Jacob states at the top of
24 page 3 of Exhibit 1034, which is that, "Even though
25 all DRAMs in the system are connected to the same

09:12

09:12

1 address and control busses and could, in theory, all
2 respond to the same request at the same time, the
3 chip select bus prevents this from happening,"
4 correct?

5 MR. TEZYAN: Objection to the form of the 09:13
6 question.

7 THE WITNESS: I'm not -- so that the
8 language of page 3 of Jacob is talking about the
9 DRAMs here connected to a -- DRAMs in the system
10 connected to the same address and control bus. And 09:13
11 that Jacob is saying here that and "could, in
12 theory, all respond to the same request at the same
13 time, the chip select bus prevents this from
14 happening," is -- which I believe Jacob mentions, at
15 least in part, on page 2. 09:13

16 The figure we were just discussing on
17 page 12 of Exhibit 1032, I interpret it as showing
18 various what look like signals that are coming into
19 a register here and then other signals outbound
20 connecting to various SDRAMs. 09:14

21 BY MR. CHANDLER:

22 Q. Including address and control signals,
23 correct?

24 MR. TEZYAN: Object to form.

25 THE WITNESS: That address signals are 09:14

1 part of that, the A0 through A13, it looks like, as
2 well as signals like a write enable, or CAS, for
3 example.

4 BY MR. CHANDLER:

5 Q. And there's also a chip select signal that
6 goes to one rank of memory devices labeled D0
7 through D8 and then there's a different chip select
8 signal that goes to different rank of memory devices
9 labeled D9 through D17, correct?

09:14

10 A. That looks right. The -- the memory
11 devices D0 through D7 are receiving an RS0 signal,
12 or RS0 bar on top, and then the D9 through D16 look
13 like they are connected to the RS1 signal.

09:15

14 Q. And just to be clear, you said D0 through
15 D7, but it's actually D0 through D8. D8 is at the
16 bottom left, correct?

09:15

17 A. That's correct. Thank you.

18 Q. And then the second rank is actually D9
19 through D17, correct?

20 A. That's right.

09:16

21 Q. All right. So turning back to Jacob,
22 page 3 of Exhibit 1034, what Jacob is teaching is
23 that even though the address and control signals can
24 go to all of the DRAM memory devices and, in theory,
25 could all respond to those address and control

09:16

1 signal at the same time as the chip select signal,
2 that prevents that from happening because the chip
3 select signal will select only one rank memory
4 devices at a time to perform a read or write
5 operation, correct?

09:16

6 MR. TEZYAN: Object to form.

7 THE WITNESS: It seems that Jacob is
8 saying in the context of this reference and the --
9 the architecture he's showing in this Figure 3
10 typical PC organization that, quote, in theory, all
11 of these DRAMs all respond to the same request at
12 the same time, the chip select bus prevents this
13 from happening within Jacob.

09:17

14 BY MR. CHANDLER:

15 Q. And also within the JEDEC 21-C standard
16 marked as Exhibit 1032, correct?

09:17

17 MR. TEZYAN: Object to form.

18 THE WITNESS: The figure we're looking at
19 shows a signal used for chip select for various of
20 the DRAM devices. I don't see that this reference
21 uses that language.

09:17

22 BY MR. CHANDLER:

23 Q. But a person of ordinary skill in the art
24 would understand that a conventional JEDEC-style
25 memory module uses a chip select signal as described

09:18

1 by Jacob on pages 2 to 3 of Exhibit 1034; is that
2 fair?

3 MR. TEZYAN: Object to form.

4 THE WITNESS: That a JEDEC-style DRAM
5 memory module may have chip select signal and it 09:18
6 would -- would be intended to or supposed to operate
7 in the manner that the JEDEC reference describes for
8 that version of the standard.

9 BY MR. CHANDLER:

10 Q. And that's what Jacob's describing on 09:18
11 pages 2 to 3 of Exhibit 1034?

12 MR. TEZYAN: Object to form.

13 THE WITNESS: I would say JEDEC -- I'm
14 sorry.

15 Jacob mentions what to me sounds like this 09:18
16 overall PC architecture that's mentioned a lot on
17 page 2 and in this reference for DRAM architectures
18 and alternative technologies has some discussion of
19 a chip select bus and at least one aspect of how
20 that's supposed to interact with the DRAMs in Jacob. 09:19

21 BY MR. CHANDLER:

22 Q. Look at page 7 of Exhibit 1034.

23 A. Okay.

24 Q. On the left side there's a description of
25 contemporary DRAM architectures starting at 09:19

1 Section 1.3, correct?

2 A. Yes.

3 Q. In Section 1.3.1 Professor Jacob describes
4 a double data rate SDRAM, abbreviated DDR SDRAM, and
5 states that DDR doubles the data bandwidth by
6 transferring data at both edges of the clock,
7 correct?

09:19

8 A. That's more or less what it's saying. The
9 sentence is talking about how it -- the DDR is
10 doubling the data rate instead of using a -- sort of
11 a single edge clock. It's going twice as fast,
12 effectively.

09:20

13 Q. Professor Jacob goes on to state that,
14 "DDR DRAM are very similar to single data rate SDRAM
15 in all other characteristics," correct?

09:20

16 A. I see that. I see that sentence, yes.

17 Q. And is that consistent with your
18 understanding?

19 MR. TEZYAN: Object to form.

20 THE WITNESS: I would say as a sort of
21 general concept more or less there are certainly
22 similarities between the two.

09:20

23 BY MR. CHANDLER:

24 Q. In the next section on page 7 of
25 Exhibit 1034, labeled Section 1.3.2, Professor Jacob

09:21

1 describes the Rambus DRAM, abbreviated RDRAM,
2 correct?

3 A. That's correct.

4 Q. In your opinion, did a person of ordinary
5 skill in the art know about Rambus DRAM, abbreviated
6 RDRAM?

09:21

7 A. That sounds right for the then-released or
8 made available Rambus technologies.

9 Q. In Section 1.3.2 of Exhibit 1034, at the
10 bottom left of page 7, Professor Jacob explains that
11 Rambus DRAM does not use dedicated lines for
12 address, control, data, and chip select signals, but
13 instead, the bus is fully multiplexed, which means
14 that address, control, data, and chip select
15 information all travel over the same set of
16 electrical wires but at different times, correct?

09:21

09:22

17 A. I see that sentence, yes.

18 Q. Is that consistent with your understanding
19 of how Rambus DRAM works?

20 A. That I would phrase it that Rambus
21 technology works with a serialized connection
22 incoming that contains various information like
23 address information or data information that is then
24 used by the Rambus device to signal to various
25 memory devices.

09:22

09:23

1 Q. As explained by Professor Jacob at the
2 bottom of page 7 and the top of page 8 of
3 Exhibit 1034, Rambus DRAMs use address, control,
4 data, and chip select information but that
5 information is transmitted using packet
6 transactions, correct? 09:23

7 A. Where are you starting on the bottom of
8 page 7?

9 Q. Just at the very -- maybe it would be
10 easier if you search for the word "packet." 09:24

11 A. Sure.

12 So I'm -- I'm roughly at the top of I
13 guess column 2 on page 7.

14 Q. And that's -- that's what I meant to say.
15 I may have thrown you off by referring to page 8. 09:24

16 So bottom of page 7, top of the second
17 column of page 7.

18 A. Right.

19 So it's talking about in the Rambus-type
20 system that the -- this bus is multiplexed so 09:24

21 there's different information on it at different
22 points in time. In this example, it's a byte wide.
23 And the transactions going over this bus are
24 packet-based. So they're kind of bundles of
25 information that are being communicated back and 09:25

1 forth over this serialized link or interconnect, if
2 you will.

3 Q. And then Professor Jacob goes on to
4 explain, on the right side of page 7 of
5 Exhibit 1034, in the second paragraph, that the
6 later Rambus bus was divided into separate address,
7 command, and data segments reminiscent of a
8 JEDEC-style DRAM organization, correct?

09:25

9 A. About halfway down he states specifically
10 with the introduction of, quote, concurrent RDRAM,
11 end quote, the bus was divided into separate
12 address, command, and data segments reminiscent of a
13 JEDEC-style DRAM organization.

09:25

14 I see that.

15 Q. And in this type of Rambus DRAM called
16 concurrent RDRAM, the width of the data bus segment
17 was one byte, or 8 bits, correct?

09:26

18 A. The -- the data segment remains, yes, a
19 single byte.

20 Q. And in your opinion, did a person of
21 ordinary skill in the art know about concurrent
22 RDRAM?

09:26

23 A. I believe that sounds right. And I
24 believe I talk about concurrent RDRAM in my
25 declaration as well.

09:26

1 Q. And then Professor Jacob goes on to
2 explain, on the bottom right of page 7 of
3 Exhibit 1034, that the next generation of Rambus
4 DRAMs, called direct RDRAM, increase the width of
5 the data segment of the bus to 2 bytes, or 16 bits,
6 but the segments remain separated and dedicated
7 similar to a JEDEC-style organization, correct?

09:27

8 A. This last paragraph in 7 is mentioning the
9 then most recent incarnation called direct RDRAM and
10 that the data segment now is the width of 2 bytes.
11 The address segment changes to 5 bits, so forth.
12 The control segment to 3 bits.

09:27

13 And -- and Dr. Jacob -- or Professor Jacob
14 characterizes it as, "These segments remain
15 separated and dedicated - similar to a JEDEC-style
16 organization."

09:28

17 Q. In your opinion, did a person of ordinary
18 skill in the art know about direct RDRAM?

19 A. I believe so at this point in time. And
20 I -- I also talk about direct RDRAM in my
21 declaration.

09:28

22 MR. CHANDLER: Great.

23 Why don't we take a short break.

24 THE VIDEOGRAPHER: Off the record at
25 9:28 a.m. Pacific time.

09:28

1 (Whereupon, a brief recess was taken.)

2 THE VIDEOGRAPHER: On the record at

3 9:35 a.m. Pacific time.

4 BY MR. CHANDLER:

5 Q. Dr. Brogioli, do you have any corrections
6 or clarifications to make to any of your testimony
7 earlier today?

09:36

8 A. Not that I recall, no.

9 Q. Dr. Brogioli, what is rank multiplication?

10 A. I would say generally it's -- can be
11 thought of as a concept of a host computer or host
12 memory controller perhaps being aware of some number
13 of ranks on a memory module and the memory module
14 actually having more ranks than that. And being
15 able to do interesting things with signaling to
16 address a larger number of ranks or a larger number
17 of DRAM devices to expand the capacity of the
18 module, for example.

09:36

19 Q. You mentioned signaling. What signals are
20 used to perform rank multiplication and how are they
21 used?

09:37

22 MR. TEZYAN: Objection. Form.

23 THE WITNESS: There are probably different
24 references out there that contemplate doing it in
25 different ways. For example, the '912 talks about

09:37

1 various ways of going about performing rank
2 multiplication within that reference.

3 BY MR. CHANDLER:

4 Q. Is one way of performing rank
5 multiplication to generate additional chip select
6 signals for the memory module?

09:37

7 MR. TEZYAN: Objection. Form.

8 THE WITNESS: I would say at a high level
9 that can be a component of certain ways of doing
10 rank multiplication.

09:37

11 BY MR. CHANDLER:

12 Q. And can you give an example of how to do
13 that, how to generate additional chip select signals
14 for the memory module? What signals would you use
15 to do that?

09:38

16 MR. TEZYAN: Objection. Form.

17 THE WITNESS: We would need to look at a
18 specific reference or discussion of a specific
19 module or a way that that reference went about it.
20 The '912, for example, talks about various signaling
21 aspects. Some of the things that are done within
22 that reference.

09:38

23 BY MR. CHANDLER:

24 Q. So can you give an example, from the '912
25 patent if you want, of how rank multiplication

09:38

1 generates additional chip select signals, and in
2 particular, what signals are used to generate the
3 additional chip select signals?

4 MR. TEZYAN: Objection. Form.

5 THE WITNESS: I guess I would point us to 09:39
6 my declaration and if we want to talk about a
7 specific aspect of it.

8 But some of the things that the '912
9 contemplates are using various signals coming in
10 from a host side or host memory controller and then 09:39
11 generating sets of signals that are used to control
12 the DRAM devices in each of the ranks in the memory
13 module of the '912 itself.

14 BY MR. CHANDLER:

15 Q. So if a rank multiplication in the example 09:39
16 of the '912 patent that you have in mind, what
17 signals coming in are used to generate the
18 additional chip select signals going out?

19 A. I guess I'll have to go back to my
20 declaration for you. It's pretty detailed. 09:40

21 So back in the '912 and -- going to my
22 declaration, roughly page 17, talks about the '912
23 and an exemplary memory module. And it shows, at
24 least at very high level, just as I say in 35, a
25 logic element here receiving a set of input control 09:41

1 signals from a computer system that include chip
2 select signals CS0 and CS1 and address signals and
3 bank address signals BA0 to BA sub M.

4 And then talks about how the system --
5 well, from the -- the computer system's perspective, 09:41
6 there's only two ranks here. But that the memory
7 devices are arranged in four ranks and discloses
8 various signaling that goes along with that. It
9 goes into increasing detail later on.

10 Q. If you turn to Exhibit 1036, the Amidi 09:42
11 reference. Let me know when you have it open.

12 A. Okay.

13 Q. The title of Amidi marked as 1036 is,
14 "Transparent Four Rank Memory Module For Standard
15 Two Rank Sub-Systems," correct? 09:42

16 A. That's correct.

17 Q. And the abstract of Amidi marked as
18 Exhibit 1036 states, "A transparent four rank memory
19 module has a front back and a back side. The front
20 side has a third memory rank stacked on a first 09:42
21 memory rank. The back side has a fourth memory rank
22 stacked on a second memory rank." Correct?

23 A. That's correct.

24 Q. And turn to Figure 4A of Amidi.

25 A. Okay. 09:43

1 Q. Figure 4A and 4B on the next page of the
2 Amidi reference marked as Exhibit 1036 disclose a
3 transparent 72-bit registered DDR module with four
4 ranks of memory devices. Labeled at the top of
5 Figure 4A is ranks 0 and 2 on the front side and at
6 the top of Figure 4B as ranks 1 and 3 on the back
7 side of the memory module, correct?

09:43

8 MR. TEZYAN: Objection. Form.

9 THE WITNESS: I see that at least in the
10 language of Amidi's Figure 4A and 4B that the titles
11 are -- well, at the top the title is "Rank 0 & 2."
12 And then 4B, "Rank 1 & 3."

09:43

13 BY MR. CHANDLER:

14 Q. So there are in Figure 4A and 4B four
15 ranks on a transparent 72-bit registered DDR memory
16 module, according to Amidi; is that correct?

09:44

17 MR. TEZYAN: Objection. Form.

18 THE WITNESS: It looks like Amidi is
19 describing Figure 4A and B as -- and I'm on page 2
20 of Amidi -- a diagram schematically illustrating the
21 front side of a transparent 72-bit registered DDR
22 module in accordance with one embodiment of Amidi's
23 present invention.

09:44

24 BY MR. CHANDLER:

25 Q. And there are a total of four ranks in

09:45

1 Figures 4A and 4B, correct?

2 MR. TEZYAN: Objection. Form.

3 THE WITNESS: It looks like that's the way
4 Amidi is at least titling the figures, that there's
5 Rank 0 and 1 -- I'm sorry, Rank 0 and 2 in
6 Figure 4A, and Amidi is saying there's Rank 1 and 3
7 in Figure 4B.

09:45

8 BY MR. CHANDLER:

9 Q. Amidi discloses nine DDR memory devices in
10 each rank where each DDR memory device is x8, or
11 8 bits wide, resulting in a total bit width of
12 72 bits, correct?

09:45

13 A. Amidi paragraph 37, fifth line, sixth line
14 down, "The memory module 400 as illustrated in
15 Figure 4A includes nine 8-bit stacked memory devices
16 404," and it describes I believe previously the
17 72-bit width.

09:46

18 Q. Then nine times eight is 72, so it's
19 consistent with Figure 4A and 4B, correct?

20 A. That sounds right in the D, 8-bit wide
21 times nine of the devices would be 72 bits.

09:46

22 Q. And if you look at with Figures 4A and 4B
23 of Amidi marked as Exhibit 1036 those figures show
24 on the memory module two registers, one on the front
25 side and one on the back side, as well as a CPLD, a

09:47

1 PLL, and an SPD, correct?

2 A. That looks to be the nomenclature Amidi's
3 using, at least in its paragraph 37, yes.

4 Q. And that's what is shown in Figures 4A and
5 4B of Amidi, correct? 09:47

6 A. That those blocks of Amidi are, quote, a
7 register 408, a CPLD 410, a PLL 412, and SPD 414 are
8 shown between those two Figures.

9 Q. Then on the back side there's a second
10 register, 418, shown in Figure 4B, correct? 09:48

11 A. That is correct. There's another block
12 labeled "418" that Amidi shares as a register.

13 Q. Turn to Figure 6A of Amidi. Let me know
14 when you're there.

15 A. Okay. 09:48

16 Q. Figure 6A of Amidi has the title "Row
17 Address Decoding," correct?

18 A. Yes.

19 Q. Figure 6A of Amidi marked as Exhibit 1036
20 shows connections between register 608, PLL 606, and 09:48
21 CPLD 604, correct?

22 MR. TEZYAN: Objection. Form.

23 THE WITNESS: So the Figure 6A of Amidi
24 shows various signals going to the CPLD, signals to
25 a PLL, and then signals to a register. 09:49

1 BY MR. CHANDLER:

2 Q. Figure 6A of Amidi does not expressly show
3 the DDR memory devices in that figure, but the
4 figure tells us at the top left and on the right
5 side of the figure which signals go to the memory
6 devices, correct? 09:50

7 MR. TEZIAN: Objection. Form.

8 THE WITNESS: It's showing at a high level
9 that there are signals up and to the left of
10 Figure 6A and signals roughly on the upper right,
11 that it says "to memory devices." 09:50

12 BY MR. CHANDLER:

13 Q. The PLL on Amidi's memory module is
14 operatively coupled to register 608 and the DDR
15 memory devices but is not operatively coupled to the
16 CPLD 604, correct? 09:51

17 MR. TEZIAN: Objection. Form.

18 THE WITNESS: It looks like I see arrows
19 from block 606, which is the PLL of Figure 6A,
20 pointing to the register and looks like there are
21 some arrows out of the PLL pointing right to memory
22 devices. 09:51

23 The CPLD 604 is, it looks like it's
24 described in paragraph 50 of Amidi, is connected to
25 a CLK0 and CLK0 sub N, or underscore N. 09:52

1 BY MR. CHANDLER:

2 Q. The output of the PLL does not go to the
3 CPLD, correct, in Amidi's memory module?

4 A. I don't see that that is the way that
5 things are visualized in Amidi's Figure 6A. 09:52

6 Q. Are you agreeing with me or disagreeing
7 with me?

8 MR. TEZYAN: Objection. Form.

9 THE WITNESS: That I don't see Figure 6A
10 showing, for example, something outbound from PLL
11 visualized to the CPLD. 09:53

12 BY MR. CHANDLER:

13 Q. Do you agree that the PLL in Amidi does
14 not output signals that go to the CPLD?

15 MR. TEZYAN: Objection. Form. 09:53

16 THE WITNESS: The way paragraph 50 of
17 Amidi is stating it is that the signals sent to PLL
18 606 include CLK0 and CLK0_N. The PLL relays those
19 two signals to register 608 and memory devices 306.

20 I don't see a visualization in Figure 6
21 with outbound arrows from PLL 606 to CPLD 604, for
22 example. 09:54

23 BY MR. CHANDLER:

24 Q. The register on Amidi's memory module
25 receives signals for address, RAS, CAS, WE, BA, and 09:54

1 CKE from the module connector as shown on the left.

2 And the register transmits register
3 versions of those signals to all the DDR memory
4 devices off to the right, correct?

5 MR. TEZYAN: Objection. Form.

09:55

6 THE WITNESS: It looks like the register
7 608 in Amidi has various signals coming in on the
8 left and they're -- the, for instance, ADD, RAS,
9 CAS, et cetera. And then there are signals
10 transmitted on the right-hand side such as rADD, and
11 so forth.

09:56

12 BY MR. CHANDLER:

13 Q. And the signals from the left of the
14 register are coming from the module connector and
15 the signals going out of the register are going to
16 all the memory devices as indicated by those arrows,
17 correct?

09:56

18 A. That seems to be what Amidi is -- is
19 visualizing at a high level in this figure.

20 Q. The CPLD on Amidi's memory module receives
21 two chip select signals labeled CS0 and CS1; a row
22 address signal labeled ADD(N); and command signals
23 labeled RAS, CAS, and WE, correct?

09:56

24 And this is in Figure 6A titled "Row
25 Address Decoding" I'm referring to.

09:57

1 A. It looks like the CPLD 604 -- let me find
2 the exact language in Amidi for you is -- is those
3 signal CS0, CS1, ADD(N). And then the CAS, RAS, and
4 WE, I think were the ones you just asked about. We
5 see those coming in Figure 6A, those arrows pointing
6 upward.

09:57

7 Q. And in Figure 6A, the signal ADD(N) going
8 CPLD is a row address signal, correct, whereas in
9 Figure 6B it's a column address.

10 (Whereupon, a brief discussion off the
11 record.)

09:58

12 MR. TEZYAN: And I'll just object to form.

13 THE WITNESS: That looks to be right. In
14 Amidi's paragraph 21 and 22, it is describing them
15 as Figure 6A for row address decoding and 6B for
16 column address decoding.

09:58

17 BY MR. CHANDLER:

18 Q. The CPLD on Amidi's memory module
19 generates four sets of chip select signals labeled
20 rCS0, rCS1, rCS2, and rSC3 that can be used for the
21 memory devices and ranks 0, 1, 2, and 3,
22 respectively, correct?

09:59

23 MR. TEZYAN: Object to form.

24 THE WITNESS: And paragraph 52 of Amidi
25 states that the CPLD 604 ensures that commands for a

09:59

1 two rank memory module conveyed by the module
2 connector 602 are also perfected on the four rank
3 memory modules. For example, CPLD generates rCS2
4 and rSC3 besides rCS0 and 1, off of CS0 and CS1, and
5 ADD(N) from the memory controller side.

10:00

6 So those upward bound rCSs look to be what
7 Amidi is referring to as chip select. RCS -- rCS0
8 and 1, 2, and 3 are signals coming out from the
9 CPLD.

10 BY MR. CHANDLER:

10:00

11 Q. So the upshot is Amidi generates four chip
12 select signals, rCS0 through rSC3, which can then be
13 sent to four ranks of memory devices 0 through 3; is
14 that fair?

15 MR. TEZIAN: Objection. Form.

10:01

16 THE WITNESS: As I see that that it's
17 referring to the CS0 and CS1 as chip select. And it
18 looks like in the paragraph we were referring to I
19 don't see that Amidi's saying the phrase "chip
20 select." I think we are in paragraph 52 -- 52 of
21 Amidi.

10:02

22 BY MR. CHANDLER:

23 Q. For example, Figure 8 of Amidi shows a
24 chip select coming into the register and then the
25 signaling going out being rCS, indicating it's the

10:02

1 registered version of the chip select signal, and
2 there's four sets, rCS0 through rSC3, correct, on
3 the right side?

4 MR. TEZYAN: Object to form.

5 THE WITNESS: In Figure 8, that -- that 10:02
6 looks to be what's present. It's described as a
7 block diagram. It's showing the CPLD in the four
8 rank DDR memory module. And so on the right-hand
9 side of the block diagram we see, for example, a CS0
10 or CS1 coming in through a MUX block, and then a -- 10:03
11 with other signals, and then the registers 820, 822
12 on the right have an rCS0A or 0B, for example, going
13 out. And we see four of them.

14 BY MR. CHANDLER:

15 Q. Figure 6A of Amidi does not expressly show 10:03
16 the CPLD receiving any bank address signals,
17 correct?

18 A. I would say that the visualization --
19 well, the visualization of Figure A does not
20 specifically delineate bank address signals, 10:03
21 although, as I recall, Amidi is contemplating DRAM.

22 Q. Well, to be clear, in Figure 6A there's
23 the CPLD on the left, and then there's a register on
24 the right. And the register on the right of
25 Figure 6A receives bank address signals labeled BA. 10:04

1 But the CPLD on the left does not receive any bank
2 address signals, according to Figure 6A, correct?

3 A. That appears to be how 6A is visualized,
4 that the CPLD does not explicitly have a BA input
5 line, at least visualized here, whereas the register
6 608 does. 10:04

7 Q. In Figure 8 of Amidi marked as
8 Exhibit 1036, that is a block diagram illustrating
9 the internal circuitry of the CPLD, correct?

10 MR. TEZYAN: Objection. Form. 10:05

11 THE WITNESS: It looks like Figure 8 is
12 intended to schematically illustrate, as -- as Amidi
13 says, schematically illustrate a CPLD in a
14 transparent four rank DDR memory module.

15 So this looks like some of the -- 10:05
16 something that, at least in some embodiments, would
17 reside in Amidi's CPLD.

18 BY MR. CHANDLER:

19 Q. Amidi's CPLD as shown in Figure 8 includes
20 on the left side circuit 804 for detecting load mode
21 register, circuit 806 for detecting auto refresh,
22 and circuit 808 for detecting auto pre-charge,
23 correct? 10:05

24 A. That looks like what Amidi's paragraph 64
25 is saying, that those within Figure 8 are -- or the 10:06

1 CS signal is going to the load mode register --
2 or -- the load mode register auto refresh 806 and
3 the auto pre-charge detect, 808.

4 Q. Amidi's detection circuits 804, 806, and
5 808 do not detect read or write operations, they
6 just detect load mode register, auto refresh, and
7 auto pre-charge, correct?

10:06

8 MR. TEZYAN: Object to form.

9 THE WITNESS: Well, I see that they are
10 called load mode register, auto refresh, and auto
11 pre-charge, and that they are also receiving the WE
12 signal, write enable.

10:06

13 BY MR. CHANDLER:

14 Q. Those circuits are described in
15 paragraph 65 through 67 of Amidi as detecting load
16 mode register, auto refresh, and auto pre-charge,
17 but there's no description of those circuits 804,
18 806, 808 of detecting any other operation such as a
19 read or write operation, correct?

10:07

20 A. Let me take a moment to review.

10:07

21 So it looks like paragraph 65 to 67 are
22 showing the various signals coming into these blocks
23 to detect a certain command, and the three commands
24 appear to be the commands listed in the box. So I
25 don't see that it's saying, for example, a DDR read

10:08

1 command or write command.

2 Q. Amidi's detection circuits 804, 806, and
3 808 only use the signals chip select, abbreviated
4 CS, RAS, CAS, and WE, correct?

5 MR. TEZYAN: Objection. Form. 10:09

6 THE WITNESS: It looks like those are the
7 four signals that are the inputs to each of the --
8 at least visualized in Figure 8, each of the
9 four blocks 804, 806, and 808.

10 BY MR. CHANDLER: 10:09

11 Q. Amidi's detection circuits 804, 806, and
12 808 can detect load mode register, auto refresh, and
13 auto pre-charge operations without using the bank
14 address signals, correct?

15 MR. TEZYAN: Objection. Form. 10:09

16 THE WITNESS: I would say to the extent --
17 well, to the extent Amidi is saying that 804 load
18 mode register, it's saying, quote, This module 804
19 detects load mode register cycle if inputs are
20 asserted properly to indicate load mode register
21 command. 10:10

22 BY MR. CHANDLER:

23 Q. In Figure 8, Amidi detection circuits 804,
24 806, and 808 do not take as an input a bank address
25 signal, correct? 10:10

1 A. I would say Figure 8 does not illustrate
2 bank address signals flowing into blocks 804, 806,
3 or 808.

4 Q. Figure 8 of Amidi illustrates circuits
5 804, 806, and 808 as detecting load mode register, 10:11
6 auto refresh, and auto pre-charge operations without
7 using a bank address signal as an input to those
8 circuits, correct?

9 MR. TEZYAN: Objection. Form.

10 THE WITNESS: I don't see that a bank 10:11
11 address signal is explicitly shown flowing into
12 those blocks 804, 808, and 806.

13 MR. CHANDLER: My realtime stopped
14 working. Why don't we go off the record just for a
15 minute and try to get that fixed and then we'll come 10:11
16 back on.

17 THE VIDEOGRAPHER: Off the record at
18 10:11 a.m. Pacific time.

19 (Whereupon, a brief recess was taken.)

20 THE VIDEOGRAPHER: Mr. Brogioli, are we 10:17
21 ready, sir?

22 (Whereupon, a brief discussion off the
23 record.)

24 THE VIDEOGRAPHER: On the record at
25 10:21 a.m. Pacific time. 10:22

1 BY MR. CHANDLER:

2 Q. Dr. Brogioli, do you have any corrections
3 or clarifications you would like to make to your
4 testimony earlier today?

5 A. Not at this time, no. 10:22

6 Q. Could you turn to the '912 patent marked
7 as Exhibit 1001. Let me know when you have that up.

8 A. Okay.

9 Q. As shown under the heading on the cover
10 page of the '912 patent labeled "Related U.S.
11 Application Data," the '912 patent is related to
12 earlier applications filed on March 7th, 2005;
13 July 15th, 2004; March 5th, 2004; and May 28th,
14 2004, correct? 10:22

15 A. I see those dates, yes. 10:23

16 Q. Please turn to page 36 of your expert
17 declaration marked as Exhibit 2062.

18 A. Okay.

19 Q. And in the footnote there you state that
20 you are only asked to render opinions about the
21 disclosure of the '244 provisional application filed
22 on July 15, 2004, and the '436 patent filed on
23 March 7th, 2005, correct? 10:23

24 A. That's correct.

25 Q. And so to be clear, you're not offering 10:23

1 opinions about whether the '668 application filed on
2 March 5th, 2004, or the '595 application filed on
3 May 28, 2004, provides support for Claim 16 of the
4 '912 patent, correct?

5 MR. TEZYAN: Object to form.

10:24

6 THE WITNESS: I would say that sounds
7 right in the sense that I only recall explicitly
8 having sections or explicitly addressing the '244
9 and the '436.

10 BY MR. CHANDLER:

10:24

11 Q. Could you pull up Exhibit 1005. And I
12 guess I can give it to you and everyone else to make
13 it easy. Let me know when you have it open.

14 (Whereupon, Exhibit 1005, having been
15 previously marked, was referenced.)

10:24

16 THE WITNESS: Okay.

17 BY MR. CHANDLER:

18 Q. Have you carefully reviewed Exhibit 1005,
19 which is the '244 provisional application filed on
20 July 15, 2004?

10:25

21 A. Yes, I have.

22 Q. And do you believe that you understand
23 Exhibit 1005, the '244 provisional application,
24 filed July 15th, 2004?

25 A. I would say in the context of the opinions

10:25

1 I offer about it in my declaration, yes.

2 Q. All right. Could you pull up Exhibit 1009
3 and let me know when you have it open.

4 (Whereupon, Exhibit 1009, having been
5 previously marked, was referenced.)

10:25

6 THE WITNESS: Okay.

7 BY MR. CHANDLER:

8 Q. Have you carefully reviewed Exhibit 1009,
9 the '436 patent, filed on March 7th, 2005?

10 A. Yes, I have.

10:26

11 Q. And do you believe you understand the --
12 Exhibit 1009, the '436 patent, filed on March 7,
13 2005?

14 A. Yes, in the -- in the context of the --
15 the aspects of it I discuss in my declaration.

10:26

16 Q. All right. Please turn back to
17 Exhibit 1005, the '244 provisional application filed
18 July 15, 2004, and let me know when you have that on
19 your screen.

20 A. I do.

10:26

21 Q. The '244 provisional application marked as
22 Exhibit 1005 contains only one figure shown on
23 page 10 of the exhibit, correct?

24 A. That looks correct.

25 Q. In the left middle of Figure 1 of the '244

10:27

1 provisional there is a block called the ASIC
2 decoder, correct?

3 A. That's correct.

4 Q. The ASIC decoder in the '244 provisional
5 shown in Figure 1 has four lines on the left labeled
6 CS0, CS1, AN+1, and the last one is labeled control
7 signals, correct?

10:27

8 A. That's right.

9 Q. According to paragraph 5 of the '244
10 provisional application marked as Exhibit 1005, the
11 ASIC decoder decodes two chip select signals, which
12 in Figure 1 are labeled CS0 and CS1, as well as an
13 address signal, which in Figure 1 is labeled AN+1,
14 and the ASIC decoder uses those input signals to
15 generate four chip select signals, correct?

10:27

16 A. That it decodes two chip select signals
17 and one control signal such as an address signal and
18 converts them into four chip select signals.

10:28

19 And then the last sentence mentions that
20 in certain embodiments it also decodes certain
21 commands such as refresh or pre-charge that require
22 all the ranks of the memory to be active.

10:28

23 Q. And you're talking about the ASIC decoder,
24 right?

25 A. That's right, as described in paragraph 5.

10:29

1 Q. So it's described in paragraph 5, and it's
2 shown in Figure 1 of the '244 provisional, the ASIC
3 decoder receives two chip select signals, CS0 and
4 CS1, and an address signal labeled AN+1, and it
5 converts those into four chip select signals,
6 correct? 10:29

7 MR. TEZYAN: Object to form.

8 THE WITNESS: That looks like what I'm at
9 least in part saying in paragraph 59 of my
10 declaration, that the -- I'm referring to the 10:30
11 highlighted version below on page 38 -- and that
12 it -- "The decoder comprises an ASIC (blue) that,"
13 quote, "decodes two chip select signals and one
14 control signal (such as an address signal) and
15 converts them into four chip select signals." 10:30

16 BY MR. CHANDLER:

17 Q. The four chip select signals illustrated
18 in Figure 1 of the '244 provisional marked as
19 Exhibit 1005 are indicated by the four lines going
20 from the right side of the ASIC decoder to a block 10:31
21 called memory ranks off to the right, correct?

22 A. That looks to be at least part of what
23 Figure 1 is illustrating.

24 Q. And Figure 1 of the '244 provisional
25 application marked as Exhibit 1005 shows that there 10:31

1 are four ranks of memory labeled "Rank 0" through
2 "Rank 3," and each rank receives a respective chip
3 select signal from the ASIC decoder, correct?

4 A. That the decoder in this figure is
5 outputting signals and that those comprise that 10:32
6 second number of chip select signals and that those
7 signals are going to the various ranks.

8 Q. And there are four ranks of memory devices
9 labeled "Rank 0" to "Rank 3" in Figure 1 of the '244
10 provisional application, correct? 10:33

11 A. That looks right, yes.

12 Q. And of each of the four ranks of memory
13 devices in Figure 1 of the '244 provisional receives
14 one of the chip select signals from the ASIC
15 decoder, correct? 10:33

16 MR. TEZYAN: Object to form.

17 THE WITNESS: It looks like of the
18 various -- the chip select signals output by the
19 decoder, they would be going to these various ranks.
20 For example, in Figure 1 of Rank 0 through Rank 3. 10:33

21 BY MR. CHANDLER:

22 Q. And I may have missed the beginning of
23 your answer, but for clarity, each rank of memory
24 devices labeled "Rank 0" through "Rank 3" receives
25 one of the outgoing chip select signals from the 10:34

1 ASIC decoder, correct?

2 A. That looks to be what the Figure 1 is
3 visualizing.

4 Q. On the lower left of Figure 1 of the '244
5 provisional there is a block labeled "Register,"
6 correct?

10:34

7 A. That's right.

8 Q. In Figure 1 of the '244 provisional, and
9 as described in paragraph 9, the register buffers
10 address signals labeled A0 through AN, correct?

10:34

11 MR. TEZYAN: Object to form.

12 THE WITNESS: It says in paragraph 9, "The
13 register buffers address signals (A0 through AN)
14 from a processor (not shown) and send the address
15 signals to the appropriate ranks of memory. The
16 ASIC uses the two chip select signals (CS0, CS1)
17 provided by the processor."

10:35

18 BY MR. CHANDLER:

19 Q. So looking at Figure 1 of the '244
20 provisional, the register receives the address
21 signals A0 to AN. It buffers those address signals
22 and then it sends those signals to the right going
23 to the Rank 0 to Rank 3, correct?

10:35

24 A. That seems to be generally what
25 paragraph 9 is describing.

10:36

1 Q. Figure 1 of the '244 provisional
2 application illustrates only, quote, ranks without
3 showing any individual memory devices in any of the
4 ranks, correct?

5 A. I would say the visualization of Figure 1 10:36
6 and the ranks illustrated within it don't -- I don't
7 see that it explicitly delineates the individual
8 memory devices themselves visually.

9 Q. Paragraph 1 of the '244 provisional 10:37
10 application marked as Exhibit 1005 describes using
11 dynamic random access memory devices, abbreviated
12 DRAM, correct?

13 A. Correct.

14 Q. The '244 provisional application marked as 10:37
15 Exhibit 1005 does not specifically disclose using
16 double data rate, or DDR, memory devices, correct?

17 MR. TEZYAN: Object to form.

18 THE WITNESS: Just flipping back through
19 the document.

20 I don't see that the paragraphs of 10:38
21 Exhibit 1005 mention DDR type DRAM explicitly. It
22 just seems to be mentioning DRAM explicitly.

23 BY MR. CHANDLER:

24 Q. And Figure 1 of the '244 provisional 10:39
25 application also does not specifically refer to DDR

1 memory devices, correct?

2 A. I don't see that Figure 1 itself is
3 explicitly saying DDR type DRAM devices.

4 Q. The '244 provisional application marked as
5 Exhibit 1005 does not specifically disclose data
6 stroke signals, or DQS signals, correct?

10:39

7 MR. TEZYAN: Object to form.

8 THE WITNESS: Well, I would say these are
9 signals that one would appreciate, or one would
10 understand is, are present in DRAM. I don't recall
11 that a specific signal such as DQS itself is
12 explicitly mentioned, you know, in -- in explicit
13 words in these paragraphs, but it's certainly
14 talking about DRAM.

10:40

15 BY MR. CHANDLER:

10:40

16 Q. Not all DRAM uses DQS signals, though,
17 correct?

18 MR. TEZYAN: Object to form.

19 THE WITNESS: I would say that, as we
20 talked about earlier, the DQS is a signal present
21 within JEDEC DRAM, for example.

10:40

22 BY MR. CHANDLER:

23 Q. JEDEC DDR DRAM but not earlier DRAM,
24 correct?

25 MR. TEZYAN: Object to form.

10:40

1 THE WITNESS: I understand the question.

2 I'd have to go back and confirm that for
3 you on early -- earlier generations of the JEDEC
4 specification and the explicit signaling for the
5 memory devices in there. 10:41

6 BY MR. CHANDLER:

7 Q. The '244 provisional application does not
8 specifically disclose or refer to any particular
9 JEDEC standards, correct?

10 MR. TEZYAN: Object to form. 10:41

11 THE WITNESS: I don't see that the
12 paragraphs of the '244 mention a specific JEDEC
13 reference or specific JEDEC reference and revision
14 in the language. They certainly talk about aspects
15 of DRAM and -- and various signaling aspects that 10:42
16 would be generally consistent.

17 BY MR. CHANDLER:

18 Q. Turn to paragraph 11 of the '244
19 provisional. Let me know when you're there.

20 A. Okay. 10:42

21 Q. Paragraph 11 of the '244 provisional
22 application marked as Exhibit 1005 includes Table 1
23 which provides a logic table for the selection of
24 the ranks of memory, correct?

25 A. That looks like the way that it's 10:42

1 described, yes.

2 Q. In Table 1 of the '244 provisional
3 application, the columns CS0, CS1, AN+1, and control
4 describe the inputs to the ASIC decoder shown, for
5 example, in Figure 1. And RS0, RS1, RS2, and RS3
6 are the four chip select signals that are output by
7 the ASIC decoder to Ranks 0 to 3, as shown, for
8 example, in Figure 1; is that correct?

10:43

9 A. One moment to refresh myself.

10 MR. TEZYAN: And I'll just object to form.

10:43

11 THE WITNESS: I'm just flipping back
12 quickly through the section in my report.

13 So I guess it sounds like this is what I'm
14 addressing on page 56 where -- of my declaration.

15 But going back to Table 1 of the '244,
16 the -- I think you were asking about column CS0,
17 CS1, AN+1, and control. And those would be the
18 input signals to the ASIC decoder in Figure 1 of the
19 '244. And then the output signals are the RS0
20 through RS3 columns on the right-hand side.

10:44

21 BY MR. CHANDLER:

22 Q. And those output signals, RS0 through RS3
23 shown in Table 1 of the '244 provisional, are four
24 chip select signals, one for each of the four ranks
25 shown in Figure 1, correct?

10:45

10:45

1 A. They look like they are signals output for
2 each of the four ranks, Rank 0 through Rank 3.

3 Q. And specifically, chip select signals,
4 correct?

5 A. That looks to be in line with the language 10:46
6 of paragraph 5 stating -- paragraph 5 of the '244
7 stating that, "The decoder of certain embodiments
8 comprises an ASIC" -- A-S-I-C -- "that decodes two
9 chip select signals and one control signal (such as
10 an address signal) and converts them into four chip 10:47
11 select signals."

12 Although it seems to be -- the signals in
13 some places are just referred to as RS.

14 Q. And in Table 1 of the provisional
15 application marked as Exhibit 1005, Footnote 1 10:47
16 indicates that the CS0, CS1, RS0, RS1, RS2, and RS3
17 are active low signals, meaning when there's a zero
18 in the table that indicates the signal is active.
19 And if there's a 1 in the table that indicates those
20 signals are inactive; is that correct? 10:47

21 MR. TEZYAN: Objection. Form.

22 THE WITNESS: That it generally means if I
23 want to send the signal to a device to operate in
24 accordance with the signal being enabled or active,
25 for example, in this case, I set it to zero instead 10:48

1 of conversely setting it to a 1.

2 BY MR. CHANDLER:

3 Q. If you compare states 4 and 6 in Table 1
4 of the '244 provisional application, you can see
5 that the input chip select signals CS0 and CS1 have
6 the same values, correct? 10:48

7 A. That's correct.

8 Q. And in states 4 and 6 of Table 1 of the
9 '244 provisional application, the address signal
10 AN+1 can also be the same value in both states 4 and 10:48
11 6, because state 6 does not care about the value of
12 AN+1, correct?

13 MR. TEZYAN: Objection. Form.

14 THE WITNESS: It looks like the X in row 6
15 denotes a don't care condition. Whereas in the AN+1 10:49
16 column for row 4 it is set to low, which is a -- not
17 the active high state.

18 BY MR. CHANDLER:

19 Q. So in both state 4 and state 6 of Table 1
20 the input signals for CS0, CS1, and AN+1 can be the 10:49
21 same values for both state 4 and for state 6,
22 specifically 100, correct?

23 MR. TEZYAN: Objection. Form.

24 THE WITNESS: It looks like for -- yeah,
25 the address, or AN+1, can be zero in state 4 or 10:50

1 don't care in state 6, and then the chip select CS0
2 and CS1 are the same for the two, and then they both
3 also have the active for the control column.

4 BY MR. CHANDLER:

5 Q. But specifically, the don't care in 10:50
6 state 6, or AN+1, means that the value for AN+1 in
7 state 6 can be zero, correct? That's what don't
8 care means, it can be zero or it can be 1, it
9 doesn't matter, either one is okay?

10 MR. TEZYAN: Objection. Form. 10:50

11 THE WITNESS: I guess I would phrase it a
12 little differently, that -- and I don't know that
13 the reference gets into a huge amount of detail on
14 this, but I think what the table is conveying is,
15 for row 6, we simply don't care what the values of 10:51
16 the AN+1 is, one way or the other, whether it's --
17 if it's supposed to be a logical zero or a
18 logical 1, it doesn't matter for row 6.

19 BY MR. CHANDLER:

20 Q. So for states 4 and 6 of Table 1 of the 10:51
21 '244 provisional application, it's possible that the
22 input values for CS0, CS1, and AN+1 are the same for
23 state 4 and for state 6, correct?

24 MR. TEZYAN: Objection. Form.

25 THE WITNESS: I think for those two rows 10:52

1 and for the specific values of CS0, CS1, and AN+1
2 only, it's possible that they can be the same -- the
3 same logical values. Well, in the sense that you
4 don't care what AN+1 is for row 6.

5 BY MR. CHANDLER:

10:52

6 Q. In Table 1 of the '244 provisional, the
7 output of state 4 and state 6 are different from
8 each other, even if the inputs for CS0, CS1, and
9 AN+1 are the same, correct?

10 MR. TEZYAN: Objection. Form.

10:52

11 THE WITNESS: That the outputs RS0 through
12 RS3 differ across those four for what is in row 4
13 and row 6.

14 BY MR. CHANDLER:

15 Q. So for example, the output for state 4 of
16 Table 1 of the '244 provisional shows that only chip
17 select signal RS2 is active low, while the output
18 for state 6 shows that both chip select signals RS2
19 and RS3 are active low, correct?

10:53

20 A. It looks like for row 6, the RS2 and RS3
21 are active low. Whereas for row 4 only the RS2 is
22 in the active low.

10:53

23 Q. And as we discussed earlier, RS2 is the
24 chip select signal that goes to rank 2 in Figure 1,
25 and RS3 is the chip select signal that goes to

10:54

1 Rank 3 in Figure 1 of the '244 provisional
2 application, correct?

3 A. The RS -- RS2 being for a Rank 2 and RS3
4 for a Rank 3.

5 Q. So in states 4 and 6 of Table 1 in the 10:54
6 '244 provisional, since the input signal CS0, CS1,
7 and AN+1 can be the same, that teaches that it's the
8 control column of Table 1 that determines the
9 difference of the output chip select signal RS3,
10 correct? 10:55

11 MR. TEZYAN: Objection.

12 THE WITNESS: No, this --

13 MR. TEZYAN: Form.

14 THE WITNESS: This is somewhat what I'm
15 addressing at the bottom of page 56, that, for 10:55
16 example, in the state 4 we've been talking about,
17 you have one of the four ranks selected in this case
18 of a read command.

19 In state 6, where, as you asked earlier,
20 or as we discussed earlier, the AN+1 signal is in 10:56
21 don't care, this may be an example of performing a
22 refresh command for the control column.

23 But one of them in terms of the logic
24 performed, specifically the state 6, the AN+1 is in
25 a don't care state. 10:56

1 BY MR. CHANDLER:

2 Q. Paragraph 19 of the '244 provisional
3 application describes the control column in -- of
4 Table 1, correct?

5 A. In part. It's talking about the control 10:56
6 column being the various commands that the DRAM's
7 connected to, like activate, read, write, refresh.

8 Q. In state 4 of the '244 provisional
9 application marked as Exhibit 1005 a control command
10 such as read is sent to selected rank only, which, 10:57
11 according to Table 1, is Rank 2, correct?

12 A. That seems to be what paragraph 19, that
13 sentence, is getting at.

14 Q. In state 6 of the '244 provisional
15 application marked as Exhibit 1005, a control 10:57
16 command such as refresh is sent to both Ranks 2 and
17 3, according to Table 1, correct?

18 A. That it says in other -- I'm back in
19 paragraph 19 of the '244 reference.

20 "In other embodiments, the control command 10:58
21 is passed through to both associated ranks (e.g.,
22 table" -- I'm sorry -- "state 6 of Table 1). In
23 such embodiments, the control command (e.g.,
24 refresh) is sent to both DRAM devices to ensure the
25 memory content of the devices remain valid over 10:58

1 time."

2 Q. And in Table 1 of the '244 provisional
3 application for state 6, the two ranks that are
4 shown as receiving the control command, which in
5 this example is refresh, are Ranks 2 and 3, correct,
6 because they have the zeros, which indicates active
7 low?

10:59

8 MR. TEZYAN: Objection. Form.

9 THE WITNESS: That the active low signals
10 for state 6 are going to be the RS2 and RS3.

10:59

11 BY MR. CHANDLER:

12 Q. So putting together, do you agree that in
13 state 6 of the '244 provisional application a
14 control command such as refresh is sent to both
15 Ranks 2 and 3?

10:59

16 A. That it's saying in other embodiments the
17 control command is passed through to both associated
18 ranks, and in such embodiments the control command
19 is sent to both DRAM devices.

20 Q. I'm a little unclear if you're trying to
21 agree with me or disagree with me.

11:00

22 MR. TEZYAN: Objection. Form.

23 BY MR. CHANDLER:

24 Q. Let me ask it this way.

25 In state 6 of the '244 provisional

11:00

1 application, which ranks receive the control
2 command, such as refresh, according to Table 1?

3 A. It looks like --

4 MR. TEZYAN: Objection. Form.

5 THE WITNESS: -- the language of
6 paragraph 19 is stating the control command is sent
7 to both DRAM devices. And the DRAM devices are
8 referring to the prior sentence, where the refresh
9 command is going to the ranks associated in Table 1
10 with RS2 and 3.

11:00

11:01

11 BY MR. CHANDLER:

12 Q. And as we discussed earlier, those would
13 be Ranks 2 and 3 that are associated with chip
14 select signals RS2 and RS3, correct?

15 A. In Table 1, those are the ranks associated
16 with RS2 and RS3.

11:01

17 Q. Please turn to page 46 of your expert
18 declaration marked as Exhibit 2062. Let me know
19 when you're there.

20 A. Okay.

11:01

21 Q. Starting on page 46 of your expert
22 declaration marked as Exhibit 2062, you provide a
23 table supporting your opinion that the '244
24 provisional application marked as Exhibit 1005
25 provides written description support for every

11:02

1 limitation in Claim 16 of the '912 patent, correct?

2 A. That is correct.

3 Q. Please pull up Exhibit 1029, the JEDEC
4 standard for DDR2 memory devices, and go to page 49
5 and let me know when you're there.

11:02

6 A. Did you say page 29?

7 Q. 49.

8 A. 49. Okay.

9 Q. Page 49 of the JEDEC DDR2 standard marked
10 as Exhibit 1029 provides a command truth table,
11 correct?

11:03

12 A. That's correct.

13 Q. A person of ordinary skill in the art
14 would have understood from this table how to use the
15 CKE, clock enable signal; the CS, chip select
16 signal; and the RAS, CAS, and WE signals to identify
17 different commands, correct?

11:03

18 MR. TEZYAN: Object to form.

19 THE WITNESS: That, as the footnote or
20 note 1 talks about, the commands are defined by
21 states of -- the DDR2 specific commands are defined
22 by states, these signals.

11:03

23 BY MR. CHANDLER:

24 Q. And these signals being chip select, RAS,
25 CAS, WE, and CKE, also referred to as clock enable,

11:04

1 correct?

2 A. In terms of the bit -- the bit encoding of
3 various commands that are listed in this table,
4 the -- I think there's 15 in here, commands, total.

5 And then as the other notes say, there's
6 other information that, for example, bank address,
7 that determine other specificity.

11:04

8 Q. But it's the signals CS, RAS, CAS, WE, and
9 clock enable that define the commands as shown on
10 page 49 of Exhibit 1029, correct?

11:05

11 MR. TEZYAN: Object to form.

12 THE WITNESS: I would say in the sense of
13 the four signals that might encode, for example, a
14 read versus a write, or the rows where they're
15 slightly different in terms of the write enable
16 signal. But, again, as the table shows, there is
17 also bank address information and other information
18 associated with the truth table.

11:05

19 BY MR. CHANDLER:

20 Q. For example, on page 49 of Exhibit 1029, a
21 mode register set command is defined by the clock
22 enable signal being high while the chip select, RAS,
23 CAS, and WE signals are all low, correct?

11:05

24 MR. TEZYAN: Object to form.

25 THE WITNESS: You're in the first row.

11:06

1 So the first row is the mode register set
2 or extended mode register set. And here, at least
3 for those four signals, CS, RAS, CAS, and write
4 enable, it's showing what those would be set to for
5 that command. There would be other -- it also shows
6 a BA column, other op code information as well.

11:06

7 BY MR. CHANDLER:

8 Q. So the mode register set command shown on
9 page 49 of Exhibit 1029 is defined by the clock
10 enable signal being high while the chip select, RAS,
11 CAS, and WE signals are all low, correct?

11:06

12 MR. TEZYAN: Object to form.

13 THE WITNESS: I would say in the sense
14 that those signals denote a mode register set versus
15 something that might be a write command or a write
16 with auto pre-charge, but there's also, as the truth
17 table shows for the mode register set, a bank
18 address column in other -- A15 through A0 fields,
19 et cetera.

11:07

20 BY MR. CHANDLER:

11:07

21 Q. On page 49 of Exhibit 1029, the JEDEC DDR2
22 standard, a refresh command, as shown in the second
23 row, is defined by the clock enable signal being
24 high, the chip select, RAS, and CAS signals being
25 low, and the write enable signal being high,

11:07

1 correct?

2 MR. TEZYAN: Object to form.

3 THE WITNESS: That for those signals you
4 just mentioned, those are the high and low values
5 that they would be set to. In the example of a
6 refresh command.

11:08

7 BY MR. CHANDLER:

8 Q. And then if we go down to a write command
9 on page 49 of Exhibit 1029, a write command is
10 defined by the clock enable signal being high, the
11 chip select signal being low, the RAS signal being
12 high, and the CAS and WE signals being low, correct?

11:08

13 MR. TEZYAN: Object to form.

14 THE WITNESS: For the settings of those
15 signals within this table, that looks correct. In
16 addition to the various other BA and A columns,
17 et cetera, on the table.

11:08

18 BY MR. CHANDLER:

19 Q. And if we go down a little bit further to
20 a read command and -- in Exhibit 1029, page 49, the
21 read command is defined by the clock enable signal
22 being high, the chip select being low, the RAS being
23 high, the CAS being low, and the WE signal being
24 high, correct?

11:08

25 MR. TEZYAN: Object to form.

11:09

1 THE WITNESS: I would say in terms of the
2 values, the settings of those -- those values for
3 this command, in addition to the other information
4 that's shown in the truth table as well.

5 BY MR. CHANDLER:

11:09

6 Q. Please turn to page 12 of Exhibit 1029.
7 Let me know when you're there.

8 A. Okay.

9 Q. As shown toward the bottom right of
10 page 12 of Exhibit 1029, CAS latency could be set to
11 three clock cycles, four clock cycles, or five clock
12 cycles, according to this DDR2 standard, correct?

11:09

13 MR. TEZYAN: Objection. Form.

14 THE WITNESS: That this section is talking
15 about the mode register and it stores values for
16 operating modes of DDR2, SDRAM. And one thing that
17 can be, as it says, controlled here is CAS latency,
18 and this table on the bottom right shows the
19 various -- various settings for A6, A5, and A4 that
20 can be used to specify certain latencies. Some that
21 are shown are a latency of 3, 4, and 5.

11:10

22 BY MR. CHANDLER:

23 Q. So in the DDR2 standard, examples of
24 permissible CAS latency values are three clock
25 cycles, four clock cycles, and five clock cycles, as

11:11

11:11

1 well as this optional two clock cycle, correct?

2 MR. TEZYAN: Object to form. And
3 objection relevance.

4 THE WITNESS: Looks like this is just
5 showing that bits A4 to A6 are used -- or the CAS 11:12
6 latency is defined by those bits, and it seems to be
7 showing that the values of 3, 4, and 5 are some of
8 the options that are there and there's other --
9 others that are reserved. Where 2 seems to be
10 optional. 11:12

11 BY MR. CHANDLER:

12 Q. And 3, 4, and 5 refer to clock cycles,
13 correct?

14 MR. TEZYAN: Same objections.

15 THE WITNESS: Perhaps. I note that the 11:12
16 paragraph above, fourth line from the bottom states,
17 "The DDR2 doesn't support half clock cycle latency
18 mode." So perhaps those are clock cycles.

19 BY MR. CHANDLER:

20 Q. So 3, 4, and 5 are full clock cycles. 11:13
21 There's no specification here for CAS latencies that
22 include a half clock cycle, correct?

23 MR. TEZYAN: Object to form. And
24 objection relevance.

25 THE WITNESS: I don't -- I don't see it 11:13

1 saying what the reserve fields are. But I -- I see
2 that the language of the paragraph above says that
3 DDR2 doesn't support half clock latency mode. So
4 perhaps the values of 3, 4, and 5 are actual clock
5 cycles.

11:13

6 BY MR. CHANDLER:

7 Q. On the page 14 of Exhibit 1029, on the
8 right side, the DDR2 standard teaches that additive
9 latency can be set to zero, one, two, three, or four
10 clock signals, correct?

11:14

11 MR. TEZYAN: Object to form. And same
12 objections to relevance.

13 THE WITNESS: Looks like it's describing
14 the extended mode register set for DDR2 and -- I'm
15 just reading the prior paragraphs.

11:14

16 It contains -- or it says the extended
17 mode register stores the data for additive latency.

18 BY MR. CHANDLER:

19 Q. And the values for additive latency that
20 are shown on page 14 of Exhibit 1029 include zero
21 clock cycles, one clock cycle, two clock cycles,
22 three clock cycles, and four clock cycles, correct?

11:15

23 MR. TEZYAN: Same objections.

24 THE WITNESS: I would say the additive
25 latency table there on the right-hand side of

11:15

1 page 14 shows you've got eight different rows. The
2 last three it says are reserved. The first five
3 shown an additive latency of zero through 4.

4 I don't see that it says clock cycles
5 specifically here. But perhaps that's what it's
6 getting at.

11:15

7 BY MR. CHANDLER:

8 Q. On page 24 of Exhibit 1029, under the
9 heading Posted CAS, the last sentence of that
10 section explains that write latency, abbreviated WL,
11 is always defined as read latency, abbreviated RL,
12 minus one, correct?

11:15

13 MR. TEZYAN: Objection. Form.

14 THE WITNESS: Reading the paragraph.

15 Saying that the right latency, WL, is
16 always defined as RL minus one, or read latency
17 minus one. Where read latency is defined as the sum
18 of additive latency plus CAS latency.

11:16

19 BY MR. CHANDLER:

20 Q. And additive latency is abbreviated AL and
21 CAS latency is abbreviated CL, correct?

11:17

22 A. In this paragraph, that looks correct,
23 yes.

24 Q. So read latency, RL, is defined as the sum
25 of additive latency, AL, plus CAS latency, CL,

11:17

1 correct?

2 MR. TEZYAN: Objection. Form. And
3 objection relevance. This is well outside the scope
4 of his declaration.

5 THE WITNESS: It looks like in this 11:17
6 paragraph, in the sentence it's saying where read
7 latency is defined as the sum of additive latency
8 plus CAS latency, or RL equals AL plus CL.

9 BY MR. CHANDLER:

10 Q. On page 28 of Exhibit 1029, there is 11:17
11 Figure 27 which illustrates a seamless burst read
12 operation, according to the DDR2 standard, correct?

13 A. It looks like it's giving examples of --
14 of what it's referring to in Figure 27 is seamless
15 burst read operation for a certain configuration 11:18
16 of -- of parameters.

17 Q. In Figure 27 of the DDR2 standard marked
18 as Exhibit 1029 there are two read commands labeled
19 "Read A" at time zero and "Read B" at time T2,
20 correct? 11:18

21 A. That's right. One at T0 and one at T2.

22 Q. And in Figure 27, the burst length,
23 abbreviated BL, is four, correct?

24 A. That looks correct.

25 Q. In Figure 27 of the DDR2 standard the data 11:19

1 requested by the Read A command starts coming out at
2 time T5 and ends at time T7, and then the data
3 requested by the Read B command starts immediately
4 after that at time T7, correct?

5 MR. TEZYAN: Object to form.

11:19

6 THE WITNESS: So it looks like this
7 example is doing two read commands, Read A and
8 Read B, at T0 and T2, and it looks like the -- with
9 the burst length four.

10 And it's saying the operation is allowed
11 regardless of the same or different banks as long as
12 the banks are activated and the data out, A0 through
13 A3, as you mentioned, are between the T5 and T7.

11:20

14 And then the -- which seems to be with the -- the
15 Read A command at T0. And then the Read B command
16 at T2 has the "D Out B0" in that lower right
17 starting at T7.

11:20

18 BY MR. CHANDLER:

19 Q. In Figure 27 of the DDR2 standard marked
20 as Exhibit 1029, on the DQS line, there is a
21 preamble between time T4 and T5 before the data
22 starts coming out at time T5, correct?

11:20

23 MR. TEZYAN: Object to form.

24 THE WITNESS: I'm just going back to the
25 earlier language to see if that window of time on

11:21

1 DQS is referred to as "preamble."

2 So I see that there is, in Figure 27 on
3 the DQS line, a one full cycle period between T4 and
4 T5 that it seems the DQS is held in a -- in a
5 certain state. I just don't -- I went back a few 11:22
6 paragraphs and pages, I don't see that it's calling
7 that a preamble necessarily.

8 BY MR. CHANDLER:

9 Q. In Figure 27 of the DDR2 standard, on the
10 DQS line, the DQS signal is driven low for a full 11:22
11 clock cycle between times T4 and T5 before the data
12 starts to come out on the DQ line starting at T5,
13 correct?

14 MR. TEZYAN: Object to form.

15 THE WITNESS: I think that may be what 11:23
16 it's visualizing.

17 BY MR. CHANDLER:

18 Q. And if you search for the word "preamble"
19 on Exhibit 1029, you will see that the DDR2 standard
20 does use the term "preamble," which is a term a 11:23
21 person of ordinary skill in the art would be
22 familiar with as representing that one clock cycle
23 period where the DQS stroke signal goes low before
24 it starts transitioning up and down to clock out
25 data on the DQ lines, correct? 11:24

1 MR. TEZYAN: Object to form.

2 THE WITNESS: It looks like page 29 is
3 saying a data stroke signal, which is the signal we
4 were looking at on page 27, should be driven low,
5 one clock prior to the WL, I think that's the right 11:24
6 latency. And it's referred to as a preamble. So it
7 does look like potentially that -- that period in
8 time of Figure 27 when DQS is pulled low is a
9 preamble.

10 BY MR. CHANDLER: 11:24

11 Q. In Figure 27 of the DDR2 standard, the DQS
12 line does not show a preamble where the signal goes
13 low between time T6 and T7 before the data
14 associated with Read B starts to come out on the DQ
15 line at time T7, correct? 11:25

16 MR. TEZYAN: Object to form.

17 THE WITNESS: Well, I want to -- one
18 thing, the preamble that we were -- that I was just
19 discussing in burst right -- I'm sorry -- in
20 Section 2.2.4.4, on page 29, is -- seems to be 11:25
21 referring to a burst right operation. And it looks
22 like your -- the Figure 27 that we were discussing a
23 few moments ago is for burst read operations.

24 BY MR. CHANDLER:

25 Q. So for example, Figure 30 of Exhibit 1029 11:26

1 shows a one clock cycle preamble for the DQS similar
2 to the one clock cycle preamble for DQS shown in
3 Figure 27, right?

4 MR. TEZYAN: Object to form.

5 THE WITNESS: That it looks to be showing, 11:26
6 again, for a burst length of eight -- I'm sorry, a
7 burst length of four, in Figure 30, that the DQS
8 line is pulled low from T3 to T4.

9 BY MR. CHANDLER:

10 Q. And if you look at the top of page 68 of 11:27
11 Exhibit 1029, the read preamble is between 0.9 and
12 1.1 clock cycles, correct?

13 A. It looks like Table 36 is talking about
14 timing parameters related to speed grading, and the
15 read preamble for each of the DDR2 listed in this 11:27
16 table shows the same minimum and maximum of 0.9 and
17 1.1. And the units here are -- it looks like it's
18 clock ticks.

19 Q. So getting back to Figure 27 of
20 Exhibit 1029 shown on page 28, do you have that in 11:28
21 front of you?

22 A. I do.

23 Q. So in Figure 27, there's a one clock cycle
24 preamble for the DQS signal before read data starts
25 coming out at T5 associated with the command Read A. 11:28

1 But there's no preamble for the DQS signal between
2 times T6 and T7 before the read data associated with
3 the command Read B starts coming out on the DQ line,
4 correct?

5 MR. TEZYAN: Object to the form. 11:29

6 THE WITNESS: I would say for the scenario
7 that's described in this Figure 27, which seems to
8 be talking about the -- the various banks, that it
9 seems like there's only a preamble on the DQS
10 between T4 and T5. 11:29

11 BY MR. CHANDLER:

12 Q. And not between T6 and T7, correct?

13 MR. TEZYAN: Object to form.

14 THE WITNESS: That's for this particular
15 figure, that seems to be what it's visualizing. 11:29

16 BY MR. CHANDLER:

17 Q. Now, you're familiar with back-to-back
18 adjacent read commands, also known as BBARX,
19 correct?

20 A. Yes. And I believe it's something I 11:30
21 discuss in my declaration.

22 Q. And back-to-back adjacent read commands
23 can cross the boundary between two memory devices,
24 correct?

25 MR. TEZYAN: Object to form. 11:30

1 THE WITNESS: The -- that's -- that sounds
2 right. That's part of what I address starting in
3 paragraph 88 of my declaration.

4 BY MR. CHANDLER:

5 Q. In rank multiplication, two separate 11:30
6 memory devices can behave as a single virtual memory
7 device, correct?

8 A. In the scenario of rank multiplication,
9 yes, they can be trying to emulate a single device.

10 Q. In Figure 27 of Exhibit 1029, if you 11:30
11 perform a seamless burst read operation on a memory
12 module with rank multiplication where there are two
13 separate memory devices pretending to be a single
14 virtual memory device, it's possible for the Read A
15 commands to go to one memory device and for the 11:31
16 Read B command to go to the other memory device
17 resulting in a back-to-back adjacent read command
18 that crosses the boundary between those two physical
19 memory devices, correct?

20 MR. TEZYAN: Objection. Incomplete 11:31
21 hypothetical.

22 THE WITNESS: I'm just going back through
23 the section of my declaration.

24 So I think as a concept, if you're asking
25 is it possible for one read command to go to one 11:32

1 memory device of one rank and another read command
2 to go to a memory device within a separate rank in a
3 rank multiplication scenario, that's possible.

4 BY MR. CHANDLER:

5 Q. And it's possible for those two read 11:33
6 commands to be what are referred to as back-to-back
7 adjacent read commands where there is data that's
8 supposed to be coming out from one memory device
9 followed immediately by data coming out of a second
10 memory device, and in that scenario the '912 patent 11:33
11 teaches there's a possibility of some collisions,
12 correct?

13 MR. TEZYAN: Objection. Form.

14 THE WITNESS: The back-to-back read
15 scenario is -- so I talk about this, in part, on 11:33
16 paragraph 88 and how, at least in the context of the
17 '386 reference, there's a memory device A in Rank 0
18 and a memory device B in Rank 1 and issues
19 pertaining to the last data strobe of the memory
20 device A and a preamble time of a data stroke for 11:34
21 the memory device B.

22 BY MR. CHANDLER:

23 Q. And that can create collisions in the
24 back-to-back adjacent read command scenario,
25 correct? 11:34

1 A. In the collisions in the sense of these
2 data strobes for the two memory devices effectively
3 trying to do different things at the same point in
4 time.

5 Q. Could you turn to the '436 patent marked 11:34
6 as 1009 and let me know when you have it in front of
7 you.

8 A. Okay.

9 Q. As shown on the cover page of
10 Exhibit 1009, the '436 patent does not claim 11:35
11 priority to the '244 provisional application that we
12 were discussing earlier, correct?

13 A. If I'm understanding the Related U.S.
14 Application Data section, that looks right. I don't
15 see the '244 listed here directly. 11:35

16 Q. Please turn to Figure 11A of the '436
17 patent. Let me know when you're there.

18 A. Okay.

19 Q. Figure 11A of the '436 patent illustrates
20 a memory module according to an embodiment of the 11:36
21 invention disclosed in the '436 patent, correct?

22 A. It's the embodiment in the '436 that's a
23 four -- excuse me -- a four rank memory module.

24 Q. Figure 11A of the '436 patent shows a
25 memory module of 600 that includes four ranks of 11:36

1 memory labeled 620, 625, 630, and 635, correct?

2 A. The memory module 600. And it's
3 comprising the logic element 640 and it also has
4 memory components -- I'm sorry, the first rank, 620;
5 second rank, 625; third rank, 630; and fourth rank,
6 635. 11:37

7 And I was just referring back to column 16
8 around line 61.

9 Q. As shown in Figure 11A of the '436 patent,
10 each of those ranks has nine memory devices labeled 11:37
11 610, correct?

12 A. That looks correct, yes.

13 Q. And then column 17 of the '436 patent
14 starting at line 10 teaches that there doesn't have
15 to be nine memory devices, there could be a 11:38
16 different number of memory devices in each rank,
17 correct?

18 MR. TEZYAN: Object to form.

19 THE WITNESS: Looks like it's saying each
20 of the ranks of 11A has nine memory components. 11:38

21 Other numbers of memory components in each of the
22 ranks is also compatible with embodiments herein.

23 BY MR. CHANDLER:

24 Q. Figure 11A of the '436 patent shows that
25 all four ranks of memory devices receives the 11:38

1 signals BNK0, BNK1, A0 to A12, RAS, CAS, and WE,
2 correct?

3 MR. TEZYAN: Object to form.

4 THE WITNESS: That looks like how it's
5 visualized in Figure 11A. 11:39

6 MR. TEZYAN: Is now a good stopping point
7 for lunch? I think it's 1:40 Central time.

8 MR. CHANDLER: Let me just finish out the
9 question on this figure.

10 Q. Those signals in Figure 11A of the '436 11:39
11 patent labeled BNK0, BNK1, A0 to A12, RAS, CAS, and
12 WE come directly from the memory controller rather
13 than being generated by the logic element 640,
14 correct?

15 MR. TEZYAN: Object to form. 11:39

16 THE WITNESS: The -- it's saying the
17 memory module -- I mean, again, column 16 at the
18 last paragraph, "The memory module 600 further
19 comprises a logic element 640 which receives a first
20 set of address and control signals from a memory 11:40
21 controller (not shown)."

22 And so it looks like the signals coming in
23 that are going to the logic element are coming from
24 the memory controller.
25

1 BY MR. CHANDLER:

2 Q. And the signals going to the four ranks of
3 memory devices labeled BNK0, BNK1, A0 to A12, RAS,
4 CAS, and WE also come directly from the memory
5 controller in Figure 11A of the '436 patent,
6 correct? 11:41

7 MR. TEZYAN: Object to form.

8 THE WITNESS: It looks like -- give me one
9 second, please.

10 It looks like Figure 11A is showing arrows 11:41
11 going, for example, from the RAS, CAS, and WE also
12 to the -- the blocks that are illustrated as the
13 various ranks.

14 BY MR. CHANDLER:

15 Q. And that's true for RAS, CAS, and WE, as 11:42
16 well as A0 through A12, Bank 1 and Bank 0, correct?

17 A. That looks to be how it's visualizing,
18 that there was a path for those signals coming in
19 externally from block 600 going to, for example, 620
20 that it refers to as a first rank. 11:43

21 Q. And it also goes to the other three ranks,
22 625, 630, and 635, correct?

23 A. That looks to be how it's visualized, yes.

24 Q. Figure 11A of the '436 patent shows that
25 the chip select signal CS0 also comes directly from 11:43

1 the memory controller and then goes to all the
2 memory devices in ranks 620 and 625, correct?

3 MR. TEZYAN: Object to form.

4 THE WITNESS: Looks like -- at least in
5 column 18 it's talking about, at the very top, in 11:44
6 certain embodiments, the PLD instead uses sequential
7 combinational logic procedures to produce four gated
8 chip select signals, CS0a through CS1b, which are
9 each transmitted to a corresponding one of the four
10 ranks. 11:44

11 BY MR. CHANDLER:

12 Q. I'm talking about something different,
13 though. I'm talking about in Figure 11A of the '436
14 patent the signal CS0 and CS1.

15 Do you see those? 11:45

16 A. Yes, I do. I do.

17 Q. So in Figure 11A of the '436 patent the
18 chip select signal CS0 comes directly from the
19 memory controller and goes to all the memory devices
20 in ranks 620 and 625, correct? 11:45

21 MR. TEZYAN: Object to form.

22 THE WITNESS: Well, as I am talking about
23 it in my declaration, those CS0 and CS1 are used as
24 part of this translation process in '436.

25 If you're asking are they visualized as an 11:46

1 arrow coming in from external to block 600 that
2 appears to flow to either the rank 620 and 625 or
3 630 and 635, it appears that that's at least in part
4 how some of the arrows are arranged.

5 BY MR. CHANDLER:

11:46

6 Q. So in Figure 11A of the '436 patent,
7 the -- the arrows for the chip select signal CS0
8 teach that the signal comes directly from the memory
9 controller and then goes to all the memory devices
10 in ranks 620 and 625, correct?

11:46

11 MR. TEZYAN: Object to form.

12 THE WITNESS: I don't see that -- maybe
13 you can refresh me. I don't recall addressing that
14 in my declaration or seeing that description in --
15 in the '436 right now. I see that there's an arrow
16 visualized here but that the signals are used as
17 part of the generating of the -- the gated chip
18 select signals.

11:47

19 BY MR. CHANDLER:

20 Q. We'll get to the gated CAS signals in
21 Figure 11A in a moment. For now, I'm just talking
22 about the chip select signal CS0 and the chip select
23 signal CS1.

11:47

24 Understood?

25 A. Sure.

11:47

1 Q. So in Figure 11 of the '436 patent the
2 chip select signal CS0 is illustrated as coming
3 directly from the memory controller and going to all
4 the memory devices in ranks 620 and 625, correct?

5 MR. TEZYAN: Object to form.

11:48

6 THE WITNESS: I -- I see that CS0 is
7 visualized as coming externally from block 600. And
8 it looks like the arrow ends at the block 620 and
9 625. Just at the periphery of those blocks.

10 BY MR. CHANDLER:

11:48

11 Q. Are you having trouble understanding
12 Figure 11A of the '436 patent?

13 I mean, do you think a person of ordinary
14 skill in the art would understand it?

15 MR. TEZYAN: Object to form.

11:48

16 THE WITNESS: I'm answering your question
17 as to how the figure is visualized.

18 BY MR. CHANDLER:

19 Q. In Figure 11A of the '436 patent, do you
20 believe a person of ordinary skill in the art would
21 understand that chip select zero comes from the
22 memory controller and goes to all the memory devices
23 in ranks 620 and 625?

11:49

24 MR. TEZYAN: Object to form.

25 THE WITNESS: I would say that the way

11:49

1 Figure 11 is visualized it's showing CS0 coming in
2 to block 600 and going to the -- the block 620 and
3 625.

4 BY MR. CHANDLER:

5 Q. And block 620 and 625 are two ranks of 11:49
6 memory devices, correct?

7 A. That is -- that is how they're described,
8 yes.

9 Q. And so do you believe a person of ordinary
10 skill in the art looking at Figure 11A of the '436 11:49
11 patent would understand that the chip select signal
12 CS0 goes to all the memory devices in ranks 620 and
13 625?

14 MR. TEZYAN: Object to form.

15 THE WITNESS: I would say that's not how 11:50
16 the figure's illustrating it. I would say to the
17 extent that they are used as part of, for example, a
18 DDR2 command encoding or a RAS, CAS, WE, or CS0
19 indicates what the function is. That may be the
20 case. But strictly how the figure is visualized, I 11:50
21 just don't see it visualized that way to ask, if I
22 understood your question, as to how it's visualized.

23 BY MR. CHANDLER:

24 Q. Well, I'm trying to understand what it
25 teaches to a person of ordinary skill in the art. 11:51

1 And if you're not sure what it teaches to a person
2 of ordinary skill in the art, that's fine, just let
3 me know, but if -- if you believe that it binds a
4 teaching of a person of ordinary skill in the art to
5 understand what that is?

11:51

6 MR. TEZYAN: Objection.

7 THE WITNESS: Well, I would say if a
8 person of skill in the art is looking at this
9 reference and contemplating DRAM commands that are
10 encoded via a chip select, write enable, row address
11 strobe, column address strobe, et cetera, that the
12 DRAM, for example, if the DRAMs are performing a
13 read, they'd be getting a command over those signals
14 coming in.

11:51

15 BY MR. CHANDLER:

11:51

16 Q. Do you believe a person of ordinary skill
17 in the art looking at Figure 11A of the '436 patent
18 would understand that the chip select signal CS0
19 goes to all the memory devices in both rank 620 and
20 rank 625 or not?

11:52

21 MR. TEZYAN: Object to the form.

22 THE WITNESS: I would say that it -- the
23 various DRAMs comprising of rank are getting the
24 read command, for example, that they would be
25 receiving the various signals shown in Figure 11A to

11:52

1 indicate the command.

2 BY MR. CHANDLER:

3 Q. And my question's a little different.

4 So my question is, in Figure 11A of the
5 '436 patent, do you believe a person of ordinary 11:52
6 skill in the art would understand that the chip
7 select signal CS0 comes from the memory controller
8 and goes to all the memory devices in rank 620 and
9 625, or do you not know?

10 MR. TEZYAN: Object to form. 11:52

11 THE WITNESS: I'm not seeing that the
12 figure is showing that.

13 BY MR. CHANDLER:

14 Q. Okay. What do you see the figure is
15 showing where the chip select signal CS0 goes? What 11:53
16 memory devices get the chip select signal CS0 in
17 Figure 11A of the '436 patent?

18 MR. TEZYAN: Objection. Form.

19 THE WITNESS: So I don't see that the
20 Figure 11A is showing within the DRAM devices 11:53
21 comprising a rank the routing of the externally --
22 cutting in CS0 illustrated in this figure. I just
23 don't see that Figure 11A shows that one way or the
24 other.

25

1 BY MR. CHANDLER:

2 Q. In Figure 11A of the '436 patent the logic
3 element 640 does not receive any of the signals A0
4 through A12, correct?

5 A. I don't see in Figure 11A that the A0 to 11:54
6 A12 line is also fed into block 640.

7 Q. In Figure 11A of the '436 patent the logic
8 element 640 sends the signal CAS0a to all memory
9 devices in rank 620, correct?

10 A. Yeah, the gated chip select signals are 11:54
11 going out to one of each of those four ranks that's
12 shown in Figure 11A.

13 Q. And where are you seeing the term "gated
14 chip select signal"?

15 A. I was reading back from my -- my 11:55
16 declaration.

17 Q. Right. But where in the '436 patent
18 marked as Exhibit 1009?

19 MR. TEZYAN: Object to form.

20 BY MR. CHANDLER: 11:55

21 Q. You're getting a little -- I think you're
22 getting a little confused.

23 So for example, column 18, lines 9 through
24 10 of the '436 patent, Exhibit 1009, refer to gated
25 chip select signals CS0a, but that's not what I'm 11:56

1 talking about. I'm talking about a different
2 signal. It's a gated CAS signal, CAS0a in
3 Figure 11A of the '436 patent.

4 Do you understand?

5 A. Okay. Yes.

11:56

6 Q. In Figure 11A of the '436 patent, the
7 logic element 640 sends the signal CAS0a to all
8 memory devices in rank 620, correct?

9 MR. TEZYAN: Object to form.

10 THE WITNESS: It looks like the block 640
11 here, if you're asking about Figure 11A, is
12 outputting to CAS0a through 1B to each of those four
13 ranks, yes.

11:56

14 BY MR. CHANDLER:

15 Q. And in Figure 11A of the '436 patent the
16 logic element 640 sends the signal CAS0b to all
17 memory devices in rank 625, correct?

11:57

18 MR. TEZYAN: Object to form.

19 THE WITNESS: It looks like that CAS0b --
20 let me find it for you -- is going to the -- would
21 be going to the various memory devices in the
22 respective rank.

11:57

23 BY MR. CHANDLER:

24 Q. 625, correct?

25 A. That looks like how it's visualized in

11:57

1 Figure 11; that's right.

2 Q. And in Figure 11A of the '436 patent, the
3 logic element 640 sends the signal CAS1a to all the
4 memory devices in rank 630 and it sends the signal
5 CAS1b to all the memory devices in rank 635,
6 correct? 11:58

7 MR. TEZYAN: Object to form.

8 THE WITNESS: It looks like it's that,
9 CAS1a going to rank 630, yes. And CAS1b going to be
10 the rank 635. 11:58

11 BY MR. CHANDLER:

12 Q. Figure 11A of the '436 patent does not
13 show a phase lock loop, abbreviated PLL, correct?

14 A. I don't see a PLL explicitly shown in
15 Figure 11A. 11:58

16 Q. Figure 11A of the '436 patent does not
17 show any register separate from the logic element
18 640, correct?

19 MR. TEZYAN: Objection. Form.

20 THE WITNESS: I -- in -- it shows the
21 register in 640 in the context of the JEDEC
22 disclosure, but it doesn't -- I don't see it
23 visualize a block labeled "Register" in this figure
24 explicitly.

25

1 BY MR. CHANDLER:

2 Q. So to be clear, Figure 11A of the '436
3 patent does not explicitly show any register that's
4 separate from the logic element 640, correct?

5 MR. TEZYAN: Object to form.

11:59

6 THE WITNESS: I would say I don't see that
7 11A shows a visually separate block labeled as a
8 register.

9 MR. CHANDLER: Why don't we break for
10 lunch. Let's go off the record and we can talk
11 about how much time.

11:59

12 THE VIDEOGRAPHER: Off the record at
13 11:59 a.m. Pacific time.

14 (Whereupon, a brief recess was taken.)

15 THE VIDEOGRAPHER: On the record at
16 12:46 p.m. Pacific time.

12:46

17 BY MR. CHANDLER:

18 Q. Dr. Brogioli, do you have any
19 clarifications or corrections you'd like to make to
20 any of your testimony earlier today?

12:47

21 A. Not at this time, no.

22 Q. Please turn back to Exhibit 1029, the DDR2
23 standard, and go to page 7 and let me know when
24 you're there.

25 A. Okay.

12:47

1 Q. Pages 7 and 8 of the JEDEC DDR2 standard
2 marked as Exhibit 1029 show addressing for x8, x4,
3 and x16 DDR SDRAM memory devices of a few different
4 densities, correct?

5 MR. TEZYAN: Objection. Form.

12:47

6 THE WITNESS: They look like DDR2, the
7 DRAMs of different capacity or density and a number
8 of different parameters that go along with the
9 different configurations.

10 BY MR. CHANDLER:

12:48

11 Q. Including some of the memory devices are
12 x4, meaning they're 4 bits wide, some are x8,
13 meaning they're 8 bits wide, and some are x16,
14 meaning they're 16 bits wide, and when you write
15 that out you would write it as x4, x8, or x16,
16 correct?

12:48

17 A. That's typically correct; that's right.

18 Q. A person of ordinary skill in the art
19 would understand the information provided on pages 7
20 and 8 of the DDR2 standard marked as Exhibit 1029,
21 correct?

12:48

22 A. In the context of the reference I would
23 think so.

24 Q. A person of ordinary skill in the art
25 would understand how to use the information provided

12:49

1 on pages 7 and 8 of the DDR standard marked as
2 Exhibit 1029 to create a memory module with the
3 desired capacity, the desired number of memory
4 devices, and the desired bit width, correct?

5 A. I would say they would understand how to 12:49
6 use this information on pages 7 and 8 in the context
7 of this JEDEC reference.

8 Q. And in the context of this JEDEC reference
9 marked as Exhibit 1029, a person of ordinary skill
10 in the art would understand that the information 12:49
11 provided on pages 7 and 8 permit them to create a
12 memory module with the desired capacity, the desired
13 number of memory devices, and the desired bit width,
14 for example, 64 bits or 72 bits, correct?

15 MR. TEZYAN: Objection. Form. 12:50

16 THE WITNESS: I would say they would
17 understand how to use this information, but a
18 similar answer to before, you know, in the context
19 of what the JEDEC reference is explaining. I
20 don't -- I'm not of the opinion they would have sort 12:50
21 of limitless bounds on what they could use this
22 information for.

23 BY MR. CHANDLER:

24 Q. Well, I'm not asking about limitless
25 bounds. 12:50

1 I'm asking about a specific example, which
2 is, a person of ordinary skill in the art would know
3 how to use the information provided on pages 7 and 8
4 of the DDR standard marked as Exhibit 1029 to create
5 a memory module with the desired capacity, the
6 desired number of memory devices, and the desired
7 bit width.

12:50

8 A. Yeah, I would say in general within the
9 context of this reference that seems -- that seems
10 all right, yes.

12:51

11 Q. For example, in both Table 2 on page 7 of
12 Exhibit 1029 and Table 3, the bottom row shows that
13 the page size for the x16 memory devices in the
14 rightmost column is 2 kilobytes, which is twice as
15 big as the page size for the x8 memory devices in
16 the middle column of both Table 2 for 512 megabit
17 addressing as well as Table 3 for 1 gigabit
18 addressing, correct?

12:51

19 MR. TEZYAN: Object to form.

20 THE WITNESS: That looks to be what the
21 table's expressing.

12:52

22 BY MR. CHANDLER:

23 Q. Can the page size of a memory device
24 impact the performance characteristics of the memory
25 device?

12:52

1 MR. TEZYAN: Object to form.

2 THE WITNESS: You might need to be a bit
3 more specific there, but there -- there are ways
4 that it -- I think it could, yeah.

5 BY MR. CHANDLER:

12:52

6 Q. And what are some examples of ways that
7 the page size of a memory device could impact the
8 performance characteristics of the memory device?

9 A. Depending on how things are arranged, you
10 may have to -- you may not have to open and close
11 pages or things like that as frequently. Depending
12 on how you're using or what your system is trying to
13 do that may provide some performance benefits.

12:53

14 Q. And do you believe a person of ordinary
15 skill in the art would understand what you just
16 described?

12:53

17 A. I would say in general someone of skill in
18 the art would understand how page size might impact
19 other -- or how page size may impact performance
20 under certain use cases and things like that.

12:53

21 Q. Do you know if high performance server
22 computers typically use x4 memory devices, x8 memory
23 devices, or x16 memory devices?

24 A. I don't recall performing that analysis in
25 my declaration for specific types of servers or --

12:54

1 if that's what you're asking.

2 Q. Do you know if laptop computers typically
3 use x4 memory devices, x8 memory devices, or x16
4 memory devices?

5 A. Again, I haven't gone through an analysis 12:54
6 of typical laptop memory modules for a given period
7 of time in the market and what was common at that
8 time.

9 Q. What are some of the tradeoffs or benefits
10 of a x4 memory device versus a x8 memory device 12:54
11 versus a x16 memory devices?

12 MR. TEZYAN: Objection. Form.

13 THE WITNESS: In some -- one example might
14 be if you are trying to populate a given memory
15 module or rank with -- with memory devices and if, 12:55
16 for example, you use a smaller bit width like 4 with
17 a larger density on it, you've got more of the
18 memory devices per width of the rank and you can
19 have larger bit storage capacity, for example.
20 Things like that. 12:55

21 BY MR. CHANDLER:

22 Q. And what do you mean by larger bit storage
23 capacity in the answer you just gave?

24 A. The amount of -- the amount of data that
25 can be stored in a given memory device. 12:56

1 Q. And is that a good thing or a bad thing?
2 I'm trying to understand what you're getting at.

3 A. It probably depends on what you're trying
4 to do. There's a lot of, I would say, variability
5 there. Some of which I address in my declaration. 12:56

6 But you may want the ability to have
7 larger storage capacity on a memory module. That
8 may have other adverse impacts in terms of cost and
9 things like that. It's something that you would be
10 specific to, you know, a given designer or their 12:56
11 desired implementation.

12 (Whereupon, a brief discussion off the
13 record.)

14 BY MR. CHANDLER:

15 Q. For a given capacity of memory devices, 12:56
16 though, such as, to take an example, 512 megabits,
17 what are some tradeoffs between a x4 memory device
18 with 512 megabits capacity versus a x8 versus a x16
19 memory device, you know, all with the same capacity?

20 MR. TEZYAN: Object to form. 12:57

21 THE WITNESS: That means someone may
22 consider things like, well, for instance, the number
23 of the devices you can incorporate on a memory
24 module for, let's say, a given bit width or if
25 you're trying to support things like ECC, there may 12:57

1 be cost, varying cost points across them. There may
2 be varying power consumption points across them.
3 Things like that.

4 BY MR. CHANDLER:

5 Q. And do you believe a person of ordinary 12:58
6 skill in the art would understand the considerations
7 that you just mentioned to me when choosing between
8 a x4, x8, x16 memory device?

9 MR. TEZYAN: Objection. Form.

10 THE WITNESS: You probably have to ask a 12:58
11 more specific -- a specific question.

12 BY MR. CHANDLER:

13 Q. Well, I was just trying to understand what
14 you were getting at.

15 So was the answer that you were giving to 12:58
16 me something that you believe a person of ordinary
17 skill in the art would understand?

18 MR. TEZYAN: Objection. Form.

19 THE WITNESS: I would say in terms of
20 concepts like cost may be a design factor in a 12:58
21 system. Part availability at the time in the market
22 may be a factor to weigh in. The amount of storage
23 capacity that you want or need, things like that,
24 are just concepts I think someone might -- would
25 understand as a concept. That may be more or less 12:59

1 applicable to, you know, a given use case or design.

2 BY MR. CHANDLER:

3 Q. And I think you also mentioned power as a
4 potential tradeoff between x4, x8, and x16 memory
5 devices; is that correct? 12:59

6 A. In some situations, it can be, yes.

7 Q. In your opinion, does a single x16 memory
8 device generally consume more power, less power, or
9 about the same amount of power as two x8 memory
10 devices that together provide the same capacity as 12:59
11 the single x16 memory device?

12 MR. TEZYAN: Objection. Incomplete
13 hypothetical.

14 THE WITNESS: We'd need to go look at --
15 if I'm understanding your question -- the data 01:00
16 sheets for a given -- a given x16 memory device
17 versus a given x8 and that kind of thing. I
18 haven't -- I don't recall performing an analysis of
19 general power consumption requirements of varying
20 memory device configurations at the time of the 01:00
21 patent.

22 BY MR. CHANDLER:

23 Q. Could you take a look at Exhibit 2057
24 which I put in the chat. Let me know when you have
25 it open. 01:00

(Whereupon, Exhibit 2057, having been previously marked, was referenced.)

THE WITNESS: Okay.

BY MR. CHANDLER:

Q. Exhibit 2057 is a Micron data sheet for DDR2 RDIMM memory modules that are x72, or 72 bits, wide, correct?

01:01

A. That looks right, yes.

Q. And the memory modules described in Exhibit 2057 have a single rank of memory devices as shown on the bottom left of the cover page second bullet point from the bottom, correct?

01:01

A. That's correct, yes.

Q. And as shown on the cover page of Exhibit 2057, as well as on pages 7 and 8, the memory modules described in this data sheet have nine memory devices each 8 bits wide resulting in a total bit width of 72 bits, correct?

01:01

A. That looks to be correct, yes.

Q. Table 2 on page 2 of Exhibit 2057 also shows in the fourth row for device configuration that each memory device is x8, or 8 bits wide, correct?

01:02

A. That's correct.

Q. Exhibit 2057 does not describe any memory

01:02

1 modules using x4 memory devices, correct?

2 A. Looking at least based on the figures and
3 thumbing through it I don't see a x4 memory device
4 shown in here. The figures all seem to be -- excuse
5 me -- the nine memory device what looks like x8
6 configuration.

01:03

7 Q. Perhaps the cover of Exhibit 2057, as well
8 as the header on each page, refers to memory modules
9 with three different capacity, 256 megabytes,
10 512 megabytes, and 1 gigabyte, correct?

01:04

11 And that's also shown on page 2 in the
12 Table 2 headers, correct?

13 A. That looks correct, yes.

14 Q. There's no 2 gigabyte memory module
15 described in Exhibit 2057, correct?

01:04

16 A. Give me one second. I noticed that this
17 is, I believe, the same data sheet I discuss in
18 portions of my declaration.

19 Q. So there's no 2 gigabyte memory module
20 described in Exhibit 2057, correct?

01:05

21 MR. TEZYAN: Object to form.

22 THE WITNESS: On page 18 -- should be
23 orienting myself with the reference -- it looks like
24 it's referring to the 256-megabyte four component
25 data sheet. Which looks like what I'm referencing

01:06

1 on the table that spreads to page 123 of my
2 declaration.

3 BY MR. CHANDLER:

4 Q. The data sheet marked as Exhibit 2057 is
5 for three different memory module capacities,
6 256 megabyte, 512 megabyte, and 1 gigabyte, correct?

01:06

7 MR. TEZIAN: Object to form.

8 THE WITNESS: I would say those are three
9 configurations that are listed on the title page.

10 And I use this reference in an analysis in my
11 declaration.

01:06

12 BY MR. CHANDLER:

13 Q. Turn to page 2 of Exhibit 2057 and look at
14 Table 5 towards the bottom. And under the heading
15 Table 5, you see immediately below that it says,
16 "Base device"?

01:07

17 A. Yes, I do.

18 Q. In Exhibit 2057, the 1-gigabyte memory
19 module uses x8 memory devices with the part number
20 listed there under Table 5, which is MT47H128M8,
21 correct?

01:07

22 MR. TEZIAN: Object to form.

23 THE WITNESS: It looks like that is what
24 is being noted on -- as the base device referencing
25 to the -- excuse me -- referencing to the data sheet

01:08

1 for it as the base device, it looks like, in this
2 table.

3 BY MR. CHANDLER:

4 Q. And then on the top of page 18 of
5 Exhibit 2057, under the heading Table 13, it states
6 that the values shown in the table are computed from
7 the data sheet for MT47H256M4 DDR2 SDRAM, correct?

01:08

8 A. It says that. And computed from values
9 specified in the 1 gigabit, or 256 Meg x4, component
10 data sheet.

01:09

11 MR. CHANDLER: I have put in the chat a
12 new exhibit, 1109.

13 (Whereupon, Exhibit 1109 was marked for
14 identification.)

15 BY MR. CHANDLER:

01:09

16 Q. Let me know when you have it open.

17 A. Okay.

18 Q. Exhibit 1109 is a data sheet for Micron's
19 DDR2 SDRAM memory device with a capacity of
20 1 gigabyte, correct?

01:09

21 A. That looks correct based on the title on
22 the top right.

23 MR. TEZYAN: I'm sorry, it's still loading
24 on my end. One second.

25 Okay. I have it.

01:09

1 BY MR. CHANDLER:

2 Q. Exhibit 1109 provides information about
3 memory devices with the part number shown in the
4 upper left of the cover page, MT47H256M4, which are
5 x4 memory devices, correct?

01:10

6 MR. TEZYAN: Object to form.

7 THE WITNESS: That -- that may be what
8 it's saying, 32 Meg by x4 x8 banks.

9 BY MR. CHANDLER:

10 Q. Exhibit 1109 also provides information
11 about memory devices with the part number
12 MT47H128M8, which are x8 memory devices, correct?

01:10

13 MR. TEZYAN: Object to form.

14 THE WITNESS: That may -- perhaps is what
15 it's saying, yes.

01:11

16 BY MR. CHANDLER:

17 Q. Exhibit 1109 -- Exhibit 1109 also provides
18 information about memory devices with the part
19 number MT47H64M16, which are x16 memory devices,
20 correct?

01:11

21 MR. TEZYAN: Object to form.

22 THE WITNESS: That may be what it's
23 getting at for that part number.

24 MR. CHANDLER: All right. I'm putting in
25 the chat a new Exhibit 1110.

01:11

1 (Whereupon, Exhibit 1110 was marked for
2 identification.)

3 BY MR. CHANDLER:

4 Q. Let me know when you have it open.

5 A. Okay.

01:11

6 Q. Exhibit 1110 is a data sheet for Micron
7 DDR2 SDRAM memory devices with a capacity of
8 512 megabits, correct?

9 A. That looks like what it's saying in the
10 title.

01:12

11 Q. Exhibit 1110 provides information about
12 memory devices with the part number MT47H128M4,
13 which are x4 memory devices, correct?

14 MR. TEZYAN: Object to form.

15 THE WITNESS: That may be what it's
16 saying.

01:12

17 BY MR. CHANDLER:

18 Q. Exhibit 1110 also provides information
19 about memory devices with the part number MT47H64M8,
20 which are x8 memory devices, correct?

01:12

21 MR. TEZYAN: Object to form.

22 THE WITNESS: That may be what it's saying
23 here.

24 BY MR. CHANDLER:

25 Q. Exhibit --

01:13

1 A. In the description.

2 Q. Exhibit 1110 also provides information
3 about memory devices with the part number
4 MT47H32M16, which are x16 memory devices, correct?

5 MR. TEZYAN: Object to form.

01:13

6 THE WITNESS: I would say that it seems to
7 be -- it may be, again, referring to the x16
8 configuration for a memory device.

9 BY MR. CHANDLER:

10 Q. I'd like you to put two documents side by
11 side, so specifically look at page 28 of
12 Exhibit 1109, and next to it put page 29 of
13 Exhibit 1110, and let me know when you're ready.

01:13

14 A. One moment.

15 Can you give me the page numbers again?

01:14

16 Q. Page 28 of Exhibit 1109 and page 29 of
17 Exhibit 1110.

18 A. Okay. I think I've got it.

19 Q. So Table 10 of Exhibit 1109 and Table 11
20 of Exhibit 1110 provide the DDR2 IDD specifications
21 and conditions for Die Revision H of 1-gigabyte
22 memory devices in Exhibit 1109 and 512-megabit
23 memory devices in Exhibit 1110, correct?

01:14

24 MR. TEZYAN: Object to form.

25 THE WITNESS: It looks like the Table 10

01:15

1 for Exhibit 1109 is referring to 1 gigabit
2 configuration and the Table 11 in Exhibit 1110 is
3 referring to the 512 megabit configuration.

4 BY MR. CHANDLER:

5 Q. As shown in these tables, one x16 memory 01:15
6 device with 1 gigabit of capacity, as shown, for
7 example, in 11 -- Exhibit 1109, always uses less
8 power for a given operation, such as the operation
9 pre-charge standby current, than if you were to take
10 two x8 memory devices with 512 megabits of capacity, 01:15
11 as shown in Exhibit 1110, correct?

12 MR. TEZYAN: Object to form.

13 THE WITNESS: I -- I'm just trying to make
14 sure I'm remembering your question before I go
15 through the table. 01:16

16 You're asking about the x16 configuration;
17 is that right?

18 BY MR. CHANDLER:

19 Q. I'm comparing one x16 memory device with
20 1 gigabit of capacity to two x8 memory devices each 01:16
21 with 512 megabits of capacity together equaling
22 1 gigabit of capacity.

23 Understood?

24 A. I think so, yep. Okay. Just give me a --

25 Q. And -- and just to make the question 01:16

1 clearer, as shown in these tables in Exhibit 1109
2 and 1110, one x16 memory device with 1 gigabit of
3 capacity always uses less power for a given
4 operation than if you were to take two x8 memory
5 devices with 512 megabits of capacity, correct?

01:17

6 MR. TEZYAN: Object to form.

7 THE WITNESS: Just continuing on to the
8 next page.

9 So it looks like for each of the
10 individual rows in this table taken in isolation
11 for, A, what looks like singular x16 memory device
12 of 1 gigabit versus the two x8 512-megabit devices,
13 the -- for that individual comparison per line in
14 the table, the two x8 devices, if I'm pronouncing
15 this right or not, would be a higher number in the
16 milliamp units than the singular x16 device for that
17 corresponding row.

01:20

01:20

18 BY MR. CHANDLER:

19 Q. And as a consequence of that, the x16
20 memory device would use less power than two x8
21 memory devices, given that they have the same
22 voltage, correct, power being current by voltage?

01:21

23 MR. TEZYAN: Object to form.

24 THE WITNESS: So perhaps for a given
25 operation, comparing the one x16 device to a

01:21

1 corresponding two x8 devices, but as I talk about in
2 my declaration, for a given memory module that's not
3 necessarily the case, taking into account other
4 module level aspects.

5 BY MR. CHANDLER:

01:22

6 Q. As shown in Table 10 of Exhibit 1109, and
7 Table 11 of Exhibit 1110, one x8 memory device with
8 1 gigabit of capacity always uses less power for a
9 given operation, such as pre-charged standby
10 current, than if you were to take two x4 memory
11 devices each with a 512-megabit capacity, correct?

01:22

12 MR. TEZYAN: Object to form.

13 THE WITNESS: So your question is a
14 similar comparison between a singular x8 1-gigabit
15 memory device to two -- versus two x4 512 gigabit;
16 is that correct?

01:22

17 BY MR. CHANDLER:

18 Q. Yes.

19 A. Okay.

20 Q. And you may have said 512 gigabit, but to
21 be clear, it's 512 megabit.

01:23

22 A. Correct, yes.

23 Okay. So it looks like when comparing a
24 single x8 1-gigabit memory device current ratings in
25 Exhibit 1109 Table 10, two, numerical 2, two of the

01:25

1 x4 512-megabit memory devices of Exhibit 1110
2 Table 11, that at least for each of the
3 corresponding line items in the table the milliamp
4 number for the two x4 devices in Table 11 of
5 Exhibit 1110 would be higher.

01:25

6 Q. Could you turn to the '912 patent marked
7 as Exhibit 1001.

8 A. Okay.

9 Q. And go to column 9. Let me know when
10 you're there.

01:26

11 A. Okay.

12 Q. In column 9 of the '912 patent starting
13 around line 23, it describes a serial presence
14 detect device, abbreviated SPD, correct?

15 A. That's correct.

01:26

16 Q. A person of ordinary skill in the art
17 would have been familiar with SPD devices, correct?

18 A. That's correct.

19 Q. Memory modules typically include an SPD
20 device to tell the host computer about
21 characteristics of the memory module and
22 characteristics of the memory devices on the memory
23 module, correct?

01:26

24 A. In JEDEC-type memory modules, that's
25 generally correct. There's a device on -- or this

01:27

1 SPD on the module that can contain information like
2 is listed here in column 9 to inform the host of
3 various characteristics.

4 Q. Column 9 of the '912 patent, starting
5 around line 38, describes some of the information
6 contained in a typical SPD, correct?

01:27

7 MR. TEZYAN: Object to form.

8 THE WITNESS: It looks like that's what
9 it's attempting to describe for a commercially
10 available module of a certain configuration. It's
11 listing some of the bytes of data in the SPD and
12 what -- what they -- or the information that they
13 contain in this example.

01:28

14 BY MR. CHANDLER:

15 Q. For example, SPD byte number 3 describes
16 the number of row address bits, byte number 4
17 describes the number of column address bits, byte
18 number 13 describes the bit width of the primary
19 DRAM memory device, and the list goes on from there,
20 correct?

01:28

01:28

21 A. That's -- that's right, yes.

22 Q. Is there a JEDEC document that provides
23 more information about the SPD?

24 A. I don't recall from memory if there's a
25 standalone document that does or doesn't sort of

01:29

1 in -- in -- in totality explaining the different
2 optionality of the SPD. Perhaps there is. I just
3 don't remember from memory.

4 MR. CHANDLER: All right. I'm marking a
5 new exhibit, 1106, which I put in the chat. 01:29

6 (Whereupon, Exhibit 1106 was marked for
7 identification.)

8 BY MR. CHANDLER:

9 Q. Let me know when you have it open.

10 A. Okay. 01:29

11 Q. Exhibit 1106 is the JEDEC standard
12 number 21-C, Section 4.1.2.4 for the SPD used on DDR
13 SDRAM memory modules, correct?

14 A. It looks like this is the SPD on DDR, as
15 you said, or DDR modules, and it's kind of what I 01:30
16 was getting at a moment ago, it looks like an
17 appendix from a -- from a larger JEDEC reference,
18 and it's described as an application note. So it
19 looks like this is what it's describing.

20 Q. On the -- 01:30

21 A. That's not a standalone document, but a
22 section of another JEDEC document.

23 Q. On the first page of Exhibit 1106, there's
24 a list of SPD byte numbers and their corresponding
25 function, correct? 01:31

1 A. That looks correct. Going up from zero to
2 255.

3 Q. For example, on the first page of
4 Exhibit 1106, SPD byte number 3 describes the number
5 of row address bits, byte number 4 describes the
6 number of column address bits, byte number 13
7 describes the bit width of the primary DRAM memory
8 device, and so on, correct? 01:31

9 A. That's right. There's different functions
10 in this table that comprise different byte or
11 multiple byte locations with information in them, or
12 perhaps they're unspecified, or things like that. 01:31

13 Q. And those byte numbers on the first page
14 of Exhibit 1106 that I just read to you correspond
15 to the byte numbers and descriptions provided in the
16 '912 patent at column 9 starting around line 38 that
17 we discussed a moment ago, correct? 01:32

18 MR. TEZYAN: Objection. Form.

19 THE WITNESS: It looks like the '912 is
20 referring to the SPD for a commercial device, and
21 this looks like it's providing an example of fields
22 or -- or byte numbers and their functional
23 description or lack thereof and sort of reservation
24 for customer use in, according to this document, for
25 example, a double data rate SDRAM module. 01:32
01:33

1 BY MR. CHANDLER:

2 Q. Please turn to page 4 of Exhibit 1106.

3 Let me know when you are there.

4 A. Okay.

5 Q. As shown on page 4 of Exhibit 1106, byte
6 number 2 of the SPD specifies the fundamental memory
7 type, correct?

01:33

8 A. That's -- looks correct.

9 Q. For example, if byte number 2 is 7, the
10 memory type is double data rate DDR SDRAM, correct?

01:33

11 A. That looks correct, yes.

12 Q. If the byte number 2 is 4, the memory type
13 is single data rate SDR SDRAM, correct?

14 A. That looks correct. Correct. If the --
15 if this byte is set to binary 4, or the number 4,
16 then that's what it's informing the system of.

01:34

17 Q. And if byte number 2 is set to 6, that
18 indicates the memory type is DDR SGRAM, correct?

19 A. That's correct.

20 Q. A person of ordinary skill in the art
21 would have understood that a memory module can
22 include either SDR DRAM or DDR DRAM or DDR SGRAM,
23 correct?

01:34

24 MR. TEZYAN: Object to form.

25 THE WITNESS: In the context of this -- I

01:34

1 think it's referred to as an application note we're
2 looking at, in the context of this JEDEC standard,
3 that the SPD data here is intended to inform, at
4 least at a binary level, to specify different types
5 of memory on a memory module.

01:35

6 BY MR. CHANDLER:

7 Q. Please turn to page 7 of Exhibit 1106.
8 Let me know when you're there.

9 A. Okay.

10 Q. As shown on page 7 of Exhibit 1106, byte
11 number 5 of the SPD describes the number of physical
12 banks on the memory module which, as we discussed
13 earlier, is also known as ranks, correct?

01:35

14 MR. TEZYAN: Object to form.

15 THE WITNESS: In some cases, the term
16 "bank," some cases in the past, the term "bank" and
17 "rank" were used somewhat interchangeably at certain
18 points in time.

01:35

19 BY MR. CHANDLER:

20 Q. As shown on page 7 of Exhibit 1106, byte
21 number 5 in the SPD can be set to indicate that the
22 memory module has one rank or two ranks or three
23 ranks or four ranks or potentially even a higher
24 number of ranks, correct?

01:36

25 A. It looks like it's specifying what this

01:36

1 table described as the number of banks at least
2 defined between -- well, the number one on up -- it
3 looks like it's at least being able to -- in a
4 binary sense specify up to 255 here.

5 Q. Please turn to page 8 of Exhibit 1106. 01:37
6 Let me know when you're there.

7 A. Okay.

8 Q. As shown on page 8 of Exhibit 1106,
9 bytes 6 and 7 of the SPD describe the module's data
10 width, correct? 01:37

11 A. It looks like those two bytes are being
12 used to inform of the module data width and then
13 there is some description as to how that's
14 represented in these two bytes, or 16 bits, of data.

15 Q. For example, as shown on page 8 of 01:38
16 Exhibit 1106, the module's data width can be
17 32 bits, correct?

18 A. That looks -- it looks like, if I'm
19 following Table 2.6, the line number 32 is I think
20 specified data with 32 and showing bit positions in 01:38
21 byte 6 and it continues up through 255 in this
22 table -- well, for this byte, rather.

23 Q. Page 8 of Exhibit 1106 permits the module
24 data width to be less than 32 bits, such as 16 bits
25 or 8 bits, correct? Those are permissible SPD 01:39

1 values, correct?

2 A. I would answer that those appear to be
3 values you can put into these byte positions in the
4 SPD's data. Some of which can specify a module
5 width of zero. It seems to be indicating that at
6 least in terms of sticking ones and zeros in memory
7 you can stick more or less whatever you'd like in
8 these two bit -- I'm sorry, these two byte fields.

01:39

9 Q. Page 8 of Exhibit 1106 also permits the
10 module data width specified in the SPD to be more
11 than 32 bits, for example, it could be specified as
12 36 bits or 64 bits, among other things, correct?

01:40

13 MR. TEZYAN: Object to form.

14 THE WITNESS: It looks like at least the
15 bit encoding supported here for byte 6, I think your
16 question was around 36 as the data width. It looks
17 like there's a -- a binary value. You can stick in
18 byte 6 to at least indicate in terms of SPD memory a
19 width of 36.

01:40

20 BY MR. CHANDLER:

01:41

21 Q. Please turn to page 13 of Exhibit 1106.
22 Let me know when you're there.

23 A. Okay.

24 Q. As shown on page 13 of Exhibit 1106, byte
25 number 13 of the SPD describes the primary SDRAM

01:41



1 width, correct?

2 A. I'm just reading. Reading the paragraph
3 first.

4 So it looks like it is -- this byte 13 is
5 being used to specify aspects of the SDRAM, the
6 SDRAM bit width itself. 01:42

7 Q. For example, as shown on page 13 of
8 Exhibit 1106, the width of the SDRAM memory device
9 on the memory module can be 4 bits wide or 8 bits
10 wide or 16 bits wide or 32 bits wide, among other 01:42
11 possibilities, correct?

12 MR. TEZYAN: Object to form.

13 THE WITNESS: I would say that this
14 table -- or, I'm sorry, this Section 2.13 for
15 byte 13 is showing within the SPD's list of data -- 01:42
16 bytes of data, these are possible values you can
17 stick in there ranging from it looks like bit width
18 of 1 to 4 to 8, 9, 127 are just different encodings
19 of numbers that one can put in there.

20 BY MR. CHANDLER: 01:43

21 Q. And the paragraph at the top of page 13 of
22 Exhibit 1106, in the last two sentences, calls out
23 examples of primary SDRAM widths of x4, x8, x16,
24 x32, as well as x9, x18, and x36, correct?

25 A. I -- I see those sentences, yes. 01:43

1 Q. Please turn to page 15 of Exhibit 1106.

2 A. Okay.

3 Q. As shown on page 15 of Exhibit 1106, byte
4 number 17 defines the number of banks on the SDRAM
5 device, correct?

01:44

6 A. That looks like what this byte position 17
7 is used for.

8 Q. For example, the SDRAM device can be
9 specified by this SPD entry as having two banks or
10 four banks as possible examples, correct?

01:44

11 A. Those are possible values of bits you can
12 stick in there. It looks like it ranges from 1 to
13 255.

14 MR. CHANDLER: I'd like to introduce a new
15 exhibit, 1107, which I put in the chat.

01:45

16 (Whereupon, Exhibit 1107 was marked for
17 identification.)

18 BY MR. CHANDLER:

19 Q. And let me know when you have it open.

20 MR. TEZYAN: If you're going on to a new
21 exhibit, now might be a good time for a break since
22 we've been going for about an hour.

01:45

23 MR. CHANDLER: Sure. Let's take a quick
24 five-minute break.

25 MR. TEZYAN: Thanks.

01:45

1 THE VIDEOGRAPHER: Off the record at
2 1:45 p.m. Pacific time.

3 (Whereupon, a brief recess was taken.)

4 THE VIDEOGRAPHER: On the record at
5 1:51 p.m. Pacific time.

01:51

6 BY MR. CHANDLER:

7 Q. All right. Dr. Brogioli, do you have
8 Exhibit 1107 in front of you?

9 A. Okay.

10 Q. Exhibit 1107 is the JEDEC standard
11 number 21-C, Section 4.1.2.10 for the SPD used on
12 DDR2 SDRAM memory modules, correct?

01:51

13 A. That looks to be correct, yes.

14 Q. So Exhibit 1107 is the SPD for DDR2 memory
15 modules, while Exhibit 1106 that we looked at a
16 moment ago was the SPD for DDR1 memory modules,
17 correct?

01:52

18 A. That looks right, yes.

19 Q. On the first page of Exhibit 1107, there's
20 a list of SPD byte numbers and their corresponding
21 function similar to the description provided in the
22 '912 patent at column 9 starting around line 38 that
23 we discussed a few moments ago, correct?

01:52

24 MR. TEZYAN: Object to form.

25 THE WITNESS: This is yet again another

01:52

1 SPD address map and it's showing various bytes
2 positions and what the functions are that are
3 described that can be specified there. So things
4 from -- similar to what we talked about before, all
5 the way through serial numbers or regions open for 01:53
6 customer use and things like that.

7 BY MR. CHANDLER:

8 Q. On page 4 of Exhibit 1107, byte number 2
9 of the SPD specifies the fundamental memory type,
10 correct? 01:53

11 A. That looks correct. And there's a number
12 of different settings that one can put in here.

13 Q. For example, if -- if byte number 2 of the
14 SPD is set to 8, that indicates that the memory type
15 is DDR2 SDRAM, correct? 01:54

16 A. That is I believe what it's supposed to
17 intend, yes, for byte -- I'm sorry, byte 2, set 2,
18 number 8.

19 Q. On page 7 of Exhibit 1107, byte number 5
20 of the SPD describes the number of ranks on the 01:54
21 memory module, correct?

22 A. The -- it's describing the number of
23 rank -- the number of ranks and package on the SDRAM
24 module and module height. And it shows for this
25 byte 5 -- 5 -- number -- in the list, the fifth 01:55

1 byte, I guess, how the different bit fields in there
2 can be used to specify this information.

3 Q. On page 7 of Exhibit 1107, a rank is
4 defined as, quote, any DRAMs connected to the same
5 physical chip select, end quote, correct? 01:55

6 A. I see that for this -- this table, yes.

7 Q. As shown on the right-hand column of
8 page 7 of Exhibit 1107, byte 5 of the SPD can
9 specify that the memory module has one rank or two
10 ranks or three ranks or four ranks or potentially 01:56
11 even a higher number of ranks, correct?

12 MR. TEZYAN: Object to form.

13 THE WITNESS: It looks like for byte 5 the
14 bit positions, or the three bits, 2, 1, and 0, you
15 can set to values to specify what looks like ranging 01:56
16 from zero to perhaps what is eight ranks, at least
17 in terms of what you can stick in that bit field.

18 BY MR. CHANDLER:

19 Q. Let's be clear, the minimum value in that
20 bit field for byte 5 of the SPD would indicate one 01:56
21 rank, correct?

22 MR. TEZYAN: Object to form.

23 THE WITNESS: I see that the -- those
24 three bits set to 000 is to denote one rank. If
25 they're set to 1 that denotes two. And if they're 01:57

1 set to 111, which would be 7, that denotes eight
2 ranks.

3 BY MR. CHANDLER:

4 Q. On page 8 of Exhibit 1107, byte number 6
5 of the SPD specifies the module's data width,
6 correct? 01:57

7 A. That looks correct.

8 Q. For example, as shown on page 8 of
9 Exhibit 1107, the module's data width can be
10 specified as 32 bits wide, correct? 01:57

11 MR. TEZYAN: Object to form.

12 THE WITNESS: I would say that byte 6 of
13 this DDR2 SPD layout shows that it seems like any
14 value between zero and 255 can be -- well, values
15 ranging from zero to 255 can be written into this 01:58
16 byte specifying different settings, different
17 settings -- information related to the module data
18 width.

19 BY MR. CHANDLER:

20 Q. On page 13 of Exhibit 1107, byte number 13 01:58
21 of the SPD specifies the primary SDRAM width,
22 correct?

23 A. It looks like that is what is intended to
24 be shown here. It is the primary -- the primary
25 SDRAM width, which is the second sentence, that 01:59

1 which is used for data.

2 Q. For example, as shown on page 13 of
3 Exhibit 1107, the width of the SDRAM memory device
4 on the memory module can be specified in the SPD as
5 4 bits wide or 8 bits wide or 16 bits wide or
6 32 bits wide, correct?

01:59

7 MR. TEZYAN: Object to form.

8 THE WITNESS: It looks like the table, the
9 SDRAM -- I'm sorry.

10 The table shown here allows for different
11 bit settings in byte 13 to indicate, at least in
12 a -- in a number within the SPD, an SDRAM width
13 ranging from 1 up through 15, and it seems to
14 continue up to 255.

02:00

15 Q. And the paragraph at the top of page 13 of
16 Exhibit 1107 specifically provides examples of an
17 SDRAM width of x4, x8, x16, and x32, as well as x9,
18 x18, and x36, correct?

02:00

19 MR. TEZYAN: Object to form.

20 THE WITNESS: It seems to be in terms of
21 bit values that can be stuck in this byte 13
22 position. That seems to be what it's explaining.

02:00

23 BY MR. CHANDLER:

24 Q. At the time of the '912 patent, x32 DDR
25 memory devices were commercially available, correct?

02:01

1 MR. TEZYAN: Object to form.

2 THE WITNESS: I don't recall in the
3 context of JEDEC SDRAM memory devices. As I recall,
4 and I think other experts such as Dr. Wolfe said the
5 same thing, they were x4, x8, and x16.

02:01

6 MR. CHANDLER: I put in the chat a new
7 exhibit, 1111.

8 (Whereupon, Exhibit 1111 was marked for
9 identification.)

10 BY MR. CHANDLER:

02:01

11 Q. Please open it up and let me know when you
12 have it in front of you.

13 A. Okay.

14 Q. I will represent to you that Exhibit 1111
15 is a copy of Micron's web page in the year 2003 as
16 captured by the Wayback Machine.

02:02

17 Are you familiar with the Wayback Machine?

18 MR. TEZYAN: I'll object to form and note
19 for the record that the printout says 10/1/23,
20 10:49 a.m., at the top.

02:02

21 THE WITNESS: So I'm generally familiar
22 with the Wayback Machine. I -- I haven't used it in
23 some time.

24 BY MR. CHANDLER:

25 Q. Please go to page 2 of Exhibit 1111 and

02:02

1 let me know when you're there.

2 A. Okay.

3 Q. Under the heading DDR SDRAM Data Sheets,
4 Exhibit 1111 shows that Micron was selling a
5 64-megabit x32 DDR SDRAM memory device with the part
6 number MT46V2M32, correct?

02:03

7 MR. TEZYAN: Object to form.

8 THE WITNESS: It looks like just going on
9 the contents of this -- this entry in the document,
10 that it -- there's a data sheet with a revision. It
11 seems to be December 2001 for what this page calls
12 an "X" 32, a x32, perhaps, DDR SDRAM.

02:03

13 MR. CHANDLER: I'd like to introduce a new
14 exhibit, 1112, which I have put in the chat.

15 (Whereupon, Exhibit 1112 was marked for
16 identification.)

02:04

17 BY MR. CHANDLER:

18 Q. Let me know when you have it open.

19 A. Okay.

20 Q. Exhibit 1112 is the Micron data sheet for
21 x32 DDR SDRAM with the part number MT46V2M32,
22 correct?

02:04

23 A. That -- that's right based -- that looks
24 right based on the entries at the top of the page.
25 There's that and then like a V1 variant.

02:04

1 Q. Exhibit 1112 shows an example of a DDR
2 SDRAM memory device that is 32 bits wide, correct?

3 MR. TEZYAN: Object to form.

4 THE WITNESS: I'm just reviewing the
5 document, the first couple pages.

02:05

6 It looks like this Micron data sheet is
7 for something called a x32 64-megabit device.

8 BY MR. CHANDLER:

9 Q. And that device is 32 bits wide, correct?

10 MR. TEZYAN: Object to form.

02:06

11 THE WITNESS: It looks like whatever this
12 device is, I think it's -- it's saying, at least in
13 certain places, it's x32. And I really -- I don't
14 think I've analyzed this reference or seen it in
15 this proceeding, but we can see different data lines
16 visualized on the pin assignment that look like they
17 go from DQ0 to DQ31.

02:06

18 MR. CHANDLER: Okay. I'd like to
19 introduce a new exhibit, 1113.

20 (Whereupon, Exhibit 1113 was marked for
21 identification.)

02:07

22 BY MR. CHANDLER:

23 Q. I put it in the chat. Let me know when
24 you have it open.

25 A. Okay.

02:07

1 Q. Exhibit 1113 is the Micron data sheet for
2 x32 --

3 MR. TEZIAN: I'm sorry, one second. I
4 can't see the exhibit yet.

5 MR. CHANDLER: Apologies. Let me know
6 when you're ready. 02:07

7 MR. TEZIAN: Sorry to interrupt. Okay.
8 BY MR. CHANDLER:

9 Q. Exhibit 1113 is the Micron data sheet for
10 x32 GDDR3 DRAM with the part number MT44H8M32,
11 correct? 02:08

12 A. It looks like it is intending to say it's
13 a form of DDR3 -- or GDDR3 DRAM, graphics DRAM, and
14 it looks like it's saying a x32 configuration for
15 this part. 02:09

16 Q. The cover page of Exhibit 1113 in the
17 upper left on the fourth bullet point indicates that
18 this is a double data rate, DDR, architecture with
19 two data accesses per clock cycle, correct?

20 A. That seems to be what that bullet point is
21 getting at or suggesting. 02:09

22 Q. And Exhibit 1113 is an example of a DDR
23 memory device that's 32 bits wide, correct?

24 A. It -- I don't know that the reference -- I
25 don't see that it mentions anything JEDEC 02:10

1 necessarily, but it seems to be saying it is a -- a
2 DRAM, or double data rate, graphics DRAM that seems
3 to be described in a x32 configuration.

4 MR. CHANDLER: All right. Let me
5 introduce a new exhibit, 1114, which I'll put in the 02:10
6 chat.

7 (Whereupon, Exhibit 1114 was marked for
8 identification.)

9 BY MR. CHANDLER:

10 Q. And let me know when you have it open. 02:10

11 A. Okay.

12 Q. Exhibit 1114 is the Micron data sheet for
13 x36 DDR SRAM with the part number MT57V256H36P,
14 correct?

15 A. Looks like -- yes, I see that part number, 02:11
16 and it's being described as a -- a DDR SRAM, and the
17 capacity -- or the storage capacity is 9 megabits.

18 Q. The cover page of Exhibit 1114 in the
19 upper left, third bullet point, indicates that this
20 memory device has double data rate operation, 02:11
21 correct?

22 A. That seems to be what it's suggesting.

23 Q. Exhibit 1114 is an example of a DDR memory
24 device that's 36 bits wide, correct?

25 A. It seems to be indicating that it is a 02:12

1 36-bit-wide configuration.

2 Q. Please open Exhibit 2110, which has been
3 premarked, and I will put it in the chat for your
4 convenience.

5 (Whereupon, Exhibit 2110, having been
6 previously marked, was referenced.)

02:12

7 BY MR. CHANDLER:

8 Q. And let me know when you have it open.

9 A. Okay.

10 Q. Exhibit 2110 is a data sheet for a DDR4
11 SDRAM, correct?

02:13

12 A. That looks to be, at least based on the
13 title, what it's describing.

14 Q. This DDR4 data sheet is from the year
15 2015, correct?

02:13

16 A. I see on the bottom of the first page that
17 it's copyright 2015, Micron. And then on the lower
18 left it's the Revision T of this document. And it
19 says 09/2021, so it looks like it's the
20 September 2021 revision. And the "EN" probably
21 means the English language version.

02:14

22 Q. DDR4 SDRAMs had not been standardized by
23 JEDEC by the time of the '912 patent back around the
24 time frame of 2004 and 2005, correct?

25 A. That sounds right to me, that the -- the

02:14

1 standardization would not -- would not have been
2 completed at that time, if it was even in progress.

3 Q. Please turn back to Exhibit 1032 and let
4 me know when you're there. I gave it to you
5 previously in the chat. If you need it again, just 02:15
6 let me know.

7 A. Thanks. I've got it. Okay.

8 Q. Exhibit 1032 is Section 4.20.4 of the
9 JEDEC standard 21-C from 2002 for a certain DDR
10 SDRAM registered DIMMs, correct? 02:15

11 A. That looks correct. The 2002 -- or
12 January of '02 SDRAM registered DIMM.

13 Q. There are other sections of the JEDEC 21-C
14 standard for other types of memory modules, correct?

15 A. I -- I would say that sounds right, but 02:15
16 I -- I don't recall all the contents of this -- the
17 full version of this particular document.

18 Q. Please open Exhibit 2050 and let me know
19 when you're there. You may have had it previously.
20 But I also put it in the chat. 02:16

21 A. Okay.

22 Q. Exhibit 2050 is Section 4.20.2 of the
23 JEDEC standard 21-C from the year 2002 for certain
24 SDRAM registered DIMMs, correct?

25 A. That's right. This looks like for the 02:16

1 PC 133.

2 Q. Please open Exhibit 2049, which you may
3 have opened previously, but I also put it in the
4 chat. Let me know when you got it.

5 A. All right.

02:17

6 Q. Exhibit 2049 is Section 4.20.6 of JEDEC
7 standard 21-C from the year 2003 for certain DDR
8 SDRAM unbuffered SO-DIMMs, correct?

9 A. That looks correct.

10 Just as a -- as a note, I'm looking -- as
11 I'm looking at Exhibit 2049, I'm also looking at
12 Exhibit 1032. They both are from the 21-C JEDEC
13 standard, but it seems like we're looking at
14 different revisions over time, 1.3, for example, and
15 1.4.

02:17

16 But that's correct, Exhibit 2049 seems to
17 be related to the DDR SDRAM unbuffered SO-DIMM.

18 Q. And we're also looking at slightly
19 different sections of the JEDEC 21-C standard,
20 correct? For example, Exhibit 1032 is
21 Section 4.20.4, whereas Exhibit 2049 is
22 Section 4.20.6, correct?

02:18

23 A. That's right.

24 MR. CHANDLER: All right. I'd like to
25 introduce a new exhibit, 1108, which I put in the

02:18

02:18

1 chat.

2 (Whereupon, Exhibit 1108 was marked for
3 identification.)

4 BY MR. CHANDLER:

5 Q. Let me know when you have it open. 02:19

6 A. Okay.

7 Q. Exhibit 1108 is Section 4.5.9 of the
8 JEDEC 21-C standard for DDR SGRAM SO-DIMMs, correct?

9 A. That's the title of this section, yes,
10 that's right. 02:19

11 Q. Page 7 of Exhibit 1108 shows a x32 DDR
12 SGRAM memory device at the top, correct? In
13 particular, the device at the top is 512K by 32, and
14 then there's a little note off to the right that
15 indicates that in the alternative you can use a DDR 02:20
16 SGRAM that's 256K by 32, correct?

17 MR. TEZYAN: Object to form.

18 THE WITNESS: So it looks like this page
19 number 7 is showing the -- an instance of a 512K x32
20 SGRAM. And then the -- I guess there's an asterisk 02:20
21 here in the middle of the page that says the
22 configuration can use 8 megabit DDR SGRAM 256K x32
23 for a 1 megabyte total.

24 BY MR. CHANDLER:

25 Q. Page 7 of Exhibit 1108 shows that the 02:21

1 memory module on that page has a single x32 memory
2 device for the entire memory module, correct?

3 MR. TEZYAN: Object to form. And
4 incomplete hypothetical.

5 THE WITNESS: Going back to look at the 02:21
6 language around this -- this section.

7 I'm not -- not sure that that's what it's
8 showing. So the prior pages -- I guess I'll go
9 backwards.

10 So starting on page 7. And it's showing 02:23
11 what looks like a single SGRAM device here. If I go
12 back to the first page, page 1, the second bullet
13 point mentions a 64-bit data bus. And then there's
14 a couple other passages.

15 If we skip ahead to -- there's language 02:24
16 around -- under Electrical Characteristics on
17 page 5 -- of two SGRAMs on the module, multiple
18 SGRAMs on the module. And then language on page 5,
19 I guess, in the middle of the page saying, "For
20 designs in which a 32-bit interface is 02:25
21 sufficient" --

22 (Whereupon a brief discussion off the
23 record.)

24 THE WITNESS: "For designs in which a
25 32-bit interface is sufficient, this specification 02:25

1 defines an option to use half of the SO-DIMM data
2 bus." Other language like that.

3 BY MR. CHANDLER:

4 Q. So on the cover page of Exhibit 1108, sort
5 of in the middle, it shows four different options 02:25
6 for how to configure the SO-DIMM. There's the 512K
7 x1 bank x32. And it identifies Figure 4.5.9-D for
8 that option, correct, and then there's three other
9 options below that?

10 MR. TEZYAN: Object to form. 02:26

11 THE WITNESS: I see roughly in the
12 middle -- right above that table on page 1, it looks
13 like it's showing four -- or it's referring the
14 reader to four different figures, 4.5.9-D through G,
15 of what look like different configurations. 02:26

16 BY MR. CHANDLER:

17 Q. So page 7 of Exhibit 1108 is the option
18 where the SO-DIMM memory module has a single x32
19 memory device as the only memory device for the
20 entire memory module, and then page 8 of 02:27
21 Exhibit 1108 gives a different option where there
22 are two x32 memory devices on the SO-DIMM memory
23 module, correct?

24 MR. TEZYAN: Object to the form of the
25 question. 02:27

1 THE WITNESS: So it looks like the figure
2 on -- there's two figures, one on page 7 and one on
3 page 8, and we see that the Figure 7, the block D0
4 shows the DQ -- I'm sorry -- DQ lines, effectively
5 zero through 31. Whereas -- and that's a 512K x32 02:28
6 memory device.

7 And the figure on page 8 is showing a --
8 two of those 512K x32 SGRAM devices, DQ lines for
9 the first one ranging from zero through 31, and the
10 second labeled DQ32 to 64. 02:29

11 BY MR. CHANDLER:

12 Q. And that's consistent with the cover page
13 of Exhibit 1108, towards the top in the third entry
14 for data configuration, there's two different
15 configurations defined. There's a 32-bit wide 02:30
16 without parity or there's a 64-bit wide without
17 parity, correct?

18 And then it goes on to say "configurations
19 are defined using x32 SGRAM memories in 1 and 2 bank
20 configurations," correct? 02:30

21 MR. TEZYAN: Object to form.

22 THE WITNESS: Well, I see the -- the words
23 that you pointed to. But the 32-bit without parity
24 and 64-bit without parity are referring to two data
25 word configurations that are defined -- or -- yeah, 02:30

1 defined is what the reference says.

2 But I note that the second bullet point
3 down in the section shows a 64-bit data bus.

4 BY MR. CHANDLER:

5 Q. And Exhibit 1108 teaches on page 5, as you 02:31
6 were reading from before, that for designs where a
7 32-bit interface is sufficient you don't need to use
8 all 64 bits, instead you can use 32 bits, and in
9 that instance, the memory module can have a single
10 x32 memory device as the only memory device on the 02:31
11 SO-DIMM memory module, correct?

12 MR. TEZYAN: Object to form.

13 THE WITNESS: It sounds like this is
14 describing that either way you have a 64-bit module
15 but may just be not using half of the 64-bit 02:32
16 interface. That's still the width of the module, it
17 sounds like, but that only 32 bits are being
18 populated or used. And perhaps that aligns with the
19 configuration of just, you know, one -- to the
20 extent I'm reviewing page 7 correctly, there's one 02:32
21 memory device. You're not even populating the width
22 of the module.

23 BY MR. CHANDLER:

24 Q. And in the example on page 7 of
25 Exhibit 1108, there would be no data on the other 02:32

1 32 bits?

2 MR. TEZYAN: Object to form.

3 THE WITNESS: I would say that to the
4 extent the -- we're talking about a 64-bit data bus,
5 as the first page of the reference shows, and
6 perhaps as example some of the pin assignments shown
7 on page 2, you know, that show in the upper -- upper
8 left, up to DQ63, I don't see those being specified
9 in at least the signals that are shown on page 7.

02:33

10 The DQs would -- at least it's only explicitly
11 showing DQs from D0 to D32.

02:33

12 MR. CHANDLER: Okay. I'd like to mark a
13 new exhibit, 1115, which I've put in the chat.

14 (Whereupon, Exhibit 1115 was marked for
15 identification.)

02:34

16 BY MR. CHANDLER:

17 Q. Let me know when you have it open.

18 A. Okay.

19 Q. Exhibit 1115 is a Micron data sheet for a
20 memory module with the part number MT1LSDT132AGP,
21 correct?

02:34

22 A. That is the part number on this data
23 sheet, yes.

24 Q. The memory module described in
25 Exhibit 1115 is 32 bits wide and only contains a

02:34

1 single x32 memory device, as shown in the upper
2 right of the first page of Exhibit 1115, as well as
3 on the last page of Exhibit 1115, correct?

4 A. Are you asking about --

5 MR. TEZYAN: Object to form.

02:35

6 THE WITNESS: I'm sorry.

7 Were you asking about the pin assignments
8 shown on the first and last page?

9 BY MR. CHANDLER:

10 Q. I was asking about the width of the memory
11 module.

02:35

12 A. Okay.

13 Q. Shown on the first page of Exhibit 1115,
14 and also the last page of Exhibit 1115, is 32 bits
15 wide and contains only a single x32 memory device,
16 correct?

02:35

17 MR. TEZYAN: Objection. Form and
18 foundation.

19 THE WITNESS: So it looks like it's
20 denoting this as a -- in the title x32
21 configuration. And the last page is what you were
22 asking about seems to show physical dimensions of
23 the device. And -- I'm just going through the intro
24 of the description to see what it's actually
25 describing.

02:36

02:37

1 It looks like the General Description
2 states the part number "is a high speed CMOS,
3 dynamic random access, 4 megabit solid-state memory
4 organized in a x32 configuration. This module is
5 configured as a single bank with a synchronous
6 interface," et cetera.

02:38

7 BY MR. CHANDLER:

8 Q. And page 3 of 1115 shows 32 DQ data lines
9 in the functional block diagram for this memory
10 module, correct?

02:38

11 A. For this, it looks like for this
12 functional block diagram of the -- of the block
13 shown on this figure, there are DQ lines zero
14 through DQ31.

15 Q. Okay. Can you turn back to the '912
16 patent marked as Exhibit 1001 and go to Figure 1A.
17 Let me know when you're there.

02:38

18 A. Okay.

19 Q. Figure 1A of the '912 patent illustrates a
20 memory module that includes four ranks labeled 32,
21 34, 36, and 38, correct?

02:39

22 A. As I recall, it is illustrating the 32
23 through 38 as a multiple ranks in this illustration.

24 Q. And specifically four ranks, correct?

25 A. That looks right for this figure.

02:40

1 I'm going back to column 21, as an
2 example, where it talks about block 32 as a first
3 rank, and 34 as a second rank, 38 should be here,
4 and a fourth rank -- up through fourth rank 38.

5 Q. And 36 is the third rank, correct? 02:40

6 A. That looks like what it's saying in, yep,
7 column 22 at least.

8 Q. Figure 1A of the '912 patent illustrates
9 multiple memory devices, 30 in each rank, correct?
10 It's described, for example, in column 6, line 33. 02:41

11 A. That's right. It's referring to memory
12 devices 30.

13 Q. So Figure 1A shows multiple memory devices
14 labeled 30 in each of the four ranks, correct?

15 A. That looks to be what it's illustrating,
16 yes. 02:41

17 Q. Figure 1A of the '912 patent illustrates a
18 register 60 with signals going out to the right to
19 the memory devices 30, correct?

20 A. The register -- 02:42

21 MR. TEZYAN: Object to form.

22 THE WITNESS: The -- the block 60 is
23 referred to as "register." The register -- yeah,
24 it's referred to as a register. And at least in
25 Figure 1A, there are various signals coming in and 02:42

1 out of block 60.

2 BY MR. CHANDLER:

3 Q. And the signals coming out of register 60
4 in Figure 1A go to the memory devices 30, correct?

5 MR. TEZYAN: Object to form.

02:43

6 THE WITNESS: It -- yeah, I'm going back
7 to column 5 for us, roughly around line 33, and that
8 the register 60 receives and buffers plurality of
9 control signals, dot, dot, dot, and then at 34, "and
10 transmits corresponding signals to the appropriate
11 memory devices 30."

02:43

12 BY MR. CHANDLER:

13 Q. Figure 1A of the '912 patent illustrates a
14 logic element 40 receiving chip select signal CS0
15 and CS1, one address signal labeled AN+1, command
16 signals, and bank address signals labeled BA0
17 through BAM, correct?

02:43

18 A. That looks correct for logic element 40.

19 Q. As shown in Figure 1A of the '912 patent,
20 the logic element 40 does not receive the address
21 signals labeled A0 through AN, correct?

02:44

22 A. In Figure 1A, I don't see that
23 explicitly --

24 (Whereupon, a brief discussion off the
25 record.)

02:44

1 THE WITNESS: I don't see that visualized
2 in Figure 1A. The A0 to AN appear to be going to
3 the register 60.

4 BY MR. CHANDLER:

5 Q. And not to the logic element 40, correct? 02:44

6 A. That's not how it's at least illustrated.

7 Q. Figure 1A does not illustrate A0 through
8 AN going to logic element 40, correct?

9 MR. TEZYAN: Object to form.

10 THE WITNESS: Just going back to my 02:45
11 declaration for you.

12 That looks -- yeah, that looks to be how
13 figure -- Figure 1A is illustrated here.

14 BY MR. CHANDLER:

15 Q. As shown in Figure 1A of the '912 patent, 02:46
16 the logic element 40 generates four chip select
17 signals labeled CS0a, CS0b, CS1a, and CS1b
18 corresponding to the four ranks labeled 32, 34, 36,
19 38, correct?

20 A. Let me see how those are described for 02:47
21 you. Let me see.

22 In Figure 1A the CS0a through CS1b are
23 signals that are going to each of the -- these
24 respective rank box 32, 34, 36, and 38.

25 Q. In Figure 1A of the '912 patent, the chip 02:47

1 select signals CS08 selects all the memory devices
2 in rank 32, correct?

3 A. I think you said CS08 and maybe you meant
4 CS0a?

5 Q. Correct.

02:48

6 A. So the CS0a is going to the rank 32
7 device -- memory devices in rank -- in rank
8 block 32.

9 Q. And that chip select signal CS0a, when it
10 is activated will select all of the memory devices
11 in rank 32, correct?

02:48

12 MR. TEZYAN: Object to form.

13 THE WITNESS: That that signal will be
14 part of the -- part of the process of selecting that
15 specific rank.

02:49

16 BY MR. CHANDLER:

17 Q. In Figure 1A of the '912 patent, chip
18 select signal CS1a selects all the memory devices in
19 rank 36, correct?

20 A. That it is -- for instance, if rank 36 is
21 to be the selected rank, CS1a is part of that
22 process in going to rank 36 and the memory devices
23 within it.

02:49

24 Q. In Figure 1A of the '912 patent, chip
25 select signal CS0b selects all the memory devices in

02:49

1 rank 34, correct?

2 A. I would say that signal CS0b is used -- is
3 part of that rank selection process if it's the rank
4 that's in block 34 that's selected for that -- that
5 command or that action.

02:50

6 Q. In Figure 1A of the '912 patent, chip
7 select signal CS1b selects all the memory devices in
8 rank 38, correct?

9 A. As a similar answer. If rank 38 is the
10 rank to be selected, the signal CS1b is part of that
11 process.

02:50

12 Q. In Figure 1A of the '912 patent, the chip
13 select signal CS0a, goes to all the memory devices
14 in rank 32 so that it can be part of the process of
15 selecting those memory devices in rank 32 when
16 needed, correct?

02:51

17 MR. TEZYAN: Objection. Form.

18 THE WITNESS: That as -- at least in part
19 is described in Table 1, I think you were asking me
20 about CS1a, would be used as part of the process of
21 accessing that corresponding block 36 rank of memory
22 devices.

02:51

23 BY MR. CHANDLER:

24 Q. In Figure 1A of the '912 patent, the chip
25 select signal CS0a goes to all the memory devices in

02:52

1 rank 32 so that it can be part of the process of
2 selecting those memory devices in rank 32 when
3 needed, correct?

4 MR. TEZYAN: Objection. Form.

5 THE WITNESS: That CS1 -- I think you were 02:52
6 asking about 1A.

7 BY MR. CHANDLER:

8 Q. No, CS0a.

9 A. Okay. CS --

10 MR. TEZYAN: Same objection. 02:52

11 THE WITNESS: Similar to how the states
12 are described in Table 1, CS0a can be pulled low as
13 part of the process of selecting the Rank 0 in that
14 case, accessing memory in Rank 0.

15 BY MR. CHANDLER: 02:53

16 Q. Which in Figure 1A is labeled rank 32,
17 correct?

18 A. The block 32 in Figure 1A.

19 Q. Figure 1A of the '912 patent does not
20 expressly show any of the data lines or data strobe 02:53
21 lines, correct?

22 A. I don't see those explicitly shown in this
23 figure.

24 Q. As explained at column 5, starting at
25 line 28, Figure 1A of the '912 patent also 02:53

1 illustrates a phase lock loop device 50, sometimes
2 abbreviated PLL, that transmits clock signals to the
3 memory devices 30, logic element 40, and the
4 register 60, correct?

5 A. That's correct.

02:54

6 Q. Figure 1B of the '912 patent is similar to
7 Figure 1A, except Figure 1B illustrates the memory
8 module with only two ranks of memory devices labeled
9 rank 32 and 34, correct?

10 A. I'm in column 6 at line 34.

02:54

11 "In other embodiments, the memory devices
12 30 are arranged in two ranks, as schematically
13 illustrated by Figure 1B."

14 Q. Figure 1B of the '912 patent illustrates
15 multiple memory devices 30 in each rank, correct?

02:55

16 A. It looks like it is illustrating multiple
17 of the memory devices in those ranks in Figure 1B.

18 Q. Figure 1B of the '912 patent illustrates
19 phase lock loop device 50, sometimes abbreviated
20 PLL, transmitting clock signals to the memory
21 devices 30, the logic element 40, and the
22 register 60, similar to what we saw in Figure 1A,
23 correct?

02:55

24 A. That -- that looks correct, yes.

25 Q. Figure 1B of the '912 patent illustrates a

02:56

1 register 60 with signals going out to the right to
2 the memory devices 30, similar to what we saw in
3 Figure 1A, correct?

4 MR. TEZYAN: Object to form.

5 THE WITNESS: It looks like it is visually 02:56

6 similar, and I refer back to the description in
7 column 5 towards line 31 that, "The register 60
8 receives and buffers a plurality of control signals,
9 including address, and transmits corresponding

10 signals to the appropriate memory devices." 02:56

11 BY MR. CHANDLER:

12 Q. In Figure 1B of the '912 patent
13 register 60 receives the same signals that we
14 discussed for Figure 1A, specifically a clock signal
15 from PLL 50, command signals, bank addresses signals 02:57
16 BA0 to BAM, and address signals A0 to AN, correct?

17 MR. TEZYAN: Object to form.

18 THE WITNESS: It looks like, at least in
19 terms of how the figures are visualized and labeled,
20 they seem to be similar in that regard. 02:57

21 BY MR. CHANDLER:

22 Q. Figure 1B of the '912 patent illustrates
23 logic element 40 receiving one chip select signal
24 CS0, one address signal labeled AN+1, command
25 signals, and bank address signals labeled BA0 to 02:57

1 BAM, correct?

2 MR. TEZYAN: Object to form.

3 THE WITNESS: That is how in Figure 1B
4 block 40 is illustrated.

5 BY MR. CHANDLER:

02:58

6 Q. As shown --

7 A. The signals are labeled.

8 Go ahead.

9 Q. As shown in Figure 1B of the '912 patent,
10 logic element 40 does not receive the address
11 signals labeled A0 to AN, correct?

02:58

12 A. I see those signals visualized as going to
13 block 60 in this figure.

14 Q. And not to logic element 40, correct?

15 A. I don't see those labeled in the way
16 Figure 1B is visualized.

02:58

17 Q. In Figure 1B in the '912 patent, logic
18 element 40 receives only one chip select signal CS0
19 and it generates two chip select signals labeled
20 CS0a and CS0b, correct?

02:59

21 A. That for Figure 1B, one of the signals
22 coming in to block the logic element 40 is a CS0.
23 And it's being generated or transmitted from
24 block 40, or from this logic element, is a CS0a and
25 a CS0b.

02:59

1 Q. In Figure 1B of the '912 patent, the chip
2 select signal CS0a goes to the memory devices in
3 rank 32 and the chip select signal CS0b goes to the
4 memory devices in rank 34, correct?

5 MR. TEZYAN: Objection. Form.

02:59

6 THE WITNESS: That the -- the way it's
7 visualized, the CS0a coming out of logic element 40
8 is going to the -- the rank in block 32, including
9 memory devices 30, and similarly, the CS0b is going
10 to the, in Figure 1B, block 34 for that rank and
11 memory devices 30 within it.

03:00

12 BY MR. CHANDLER:

13 Q. Figure 1B of the '912 patent does not
14 expressly show any of the data lines or data strobe
15 lines, correct?

03:00

16 A. I don't see them explicitly visualized
17 here.

18 Q. Figure 1C of the '912 patent illustrates
19 another memory module N [sic], correct?

20 MR. TEZYAN: Object to form.

03:00

21 THE WITNESS: Give me one...

22 BY MR. CHANDLER:

23 Q. That discuss, for example, column 10
24 starting around line 57?

25 A. Yes --

03:01

1 Q. And to be clear, I said memory module 10,
2 the number 10, not the letter N like Nancy.

3 A. That was what threw me off.

4 I see that. Line 56 or so. It's
5 Figure 1C. Schematically illustrates an exemplary
6 memory -- memory module 10. 03:01

7 Q. Figure C of the '912 patent only shows two
8 memory devices, 31 and 33, on memory module 10,
9 correct?

10 A. A pair of substantially identical memory
11 devices 31 and 33. 03:01

12 Q. Figure 1C does not show a data buffer,
13 correct?

14 MR. TEZYAN: Object to form.

15 THE WITNESS: I'm just reading the
16 description here. 03:02

17 So it looks like it starts describing
18 Figure 1C at the very bottom of column 10. And
19 mentions the memory devices in the SPD 70.

20 I'm skipping ahead. 03:03

21 But I don't see that there's a block
22 within -- within block 10 of Figure 1C explicitly
23 showing other -- other components.

24 BY MR. CHANDLER:

25 Q. Column 10 of the '912 patent, starting 03:03

1 around line 60, teaches that each memory device 31
2 and 33 in Figure 1C has a bit width, a number of
3 banks, a number of rows, and a number of columns,
4 correct?

5 A. That's correct.

03:03

6 Q. The memory module in Figure 1C of the '912
7 patent also includes an SPD device 70, correct?

8 A. That's correct. An SPD that -- SPD device
9 comprising data characterizing the pair of memory
10 devices.

03:04

11 Q. The SPD 70 can be read by the system
12 memory controller to learn about the characteristics
13 of the memory module, correct?

14 MR. TEZIAN: Object to form.

15 THE WITNESS: That generally sounds true
16 from the description in -- in various JEDEC
17 references, that something would read information
18 from the -- or those bytes in the SPD to understand
19 aspects of what it's saying here at the bottom of
20 column 10 and top of column 11 are aspects of the
21 memory devices.

03:04

22 BY MR. CHANDLER:

23 Q. Column 11 of the '912 patent, starting
24 around line 5, teaches that the SPD 70 of Figure 1C
25 tells the host computer that there's one higher

03:05

03:05

1 density memory device when in reality there are
2 actually two lower density memory devices, 31 and
3 33, correct?

4 A. That it's this -- the SPD within the
5 memory module is talking -- or is programmed to 03:05
6 describe this combined pair of lower density devices
7 as one virtual or sort of pseudo higher density
8 device.

9 Q. Column 10 of the '912 patent, around
10 line 65, teaches that the SPD 70 of Figure 1C tells 03:06
11 the host computer that the higher density memory
12 device has twice the bit width of each of the two
13 lower density memory devices, 31 and 33, correct?

14 A. That's -- yeah, what it's saying in the
15 last sentence, that, "The data characterize the pair 03:06
16 of memory devices 31 and 33 as a virtual memory
17 device having a second bit width equal to twice the
18 first bit width."

19 MR. CHANDLER: Why don't we go off record
20 and take a quick break. 03:07

21 THE VIDEOGRAPHER: Off the record at
22 3:07 p.m. Pacific time.

23 (Whereupon, a brief recess was taken.)

24 THE VIDEOGRAPHER: Did you get a run time
25 in the chat? 03:17

1 (Whereupon, a brief discussion off the
2 record.)

3 THE VIDEOGRAPHER: On the record at
4 3:17 p.m. Pacific time.

5 BY MR. CHANDLER:

03:18

6 Q. Dr. Brogioli, do you have any corrections
7 or clarifications you would like to make to any of
8 your testimony?

9 A. Not at this time, no.

10 Q. I'm sorry, say again.

03:18

11 A. I'm saying not at this time, no.

12 Q. Please turn to page 133 of your expert
13 declaration marked as Exhibit 2062 and let me know
14 when you're there.

15 A. Okay.

03:18

16 Q. In the middle of page 133 of your expert
17 declaration marked as Exhibit 2062, you have
18 included two annotated versions of Figure 4B of the
19 Perego reference, correct?

20 A. That looks correct. This is 4B of Perego.

03:18

21 Q. The illustrations on page 133 of your
22 expert declaration marked as Exhibit 2062 were
23 created by you, not by Dr. Wolfe or by Samsung,
24 correct?

25 MR. TEZYAN: Object to form.

03:19

1 THE WITNESS: I believe the highlighting
2 may have been added by me or perhaps -- perhaps
3 Dr. Wolfe, but I think -- I think I did.

4 BY MR. CHANDLER:

5 Q. Neither you nor Netlist ever asked
6 Dr. Wolfe if the figure on page 133 of your
7 declaration marked as Exhibit 2062 accurately
8 represents Dr. Wolfe's opinions, correct?

03:19

9 MR. TEZYAN: Object to form.

10 THE WITNESS: My intention was to
11 visualize what Dr. Wolfe was saying in his
12 declaration, or deposition, as to whether -- I
13 didn't show these figures to Dr. Wolfe myself
14 personally. As to whether he had seen them through
15 some other avenue or -- I'm not sure.

03:20

16 BY MR. CHANDLER:

17 Q. To be clear, you're not aware of any
18 evidence that Dr. Wolfe has ever seen the
19 illustrations on page 133 of your expert declaration
20 marked as Exhibit 2062 or has ever agreed with those
21 illustrations, correct?

03:20

22 MR. TEZYAN: Object to form.

23 THE WITNESS: I would say I don't know if
24 someone other than me presented these figures to him
25 or not. I don't know one way or the other.

03:20

1 MR. CHANDLER: Please pull up
2 Exhibit 1006. And I'll put it in the chat in case
3 you don't have it handy.

4 (Whereupon, Exhibit 1006, having been
5 previously marked, was referenced.)

03:20

6 BY MR. CHANDLER:

7 Q. And let me know when you have it open.

8 A. Okay.

9 Q. Exhibit 1006 is the '668 provisional
10 application filed March 5th, 2004, correct?

03:21

11 A. That looks correct.

12 Q. On page 3 of Exhibit 1006, at the top, the
13 title of the '668 provisional application is
14 unbuffered memory module using shared DQS pins,
15 correct?

03:22

16 A. That's correct.

17 Q. Page 11 of Exhibit 1006 provides a
18 functional block diagram for the unbuffered memory
19 module disclosed in the '668 provisional
20 application, correct?

03:22

21 MR. TEZYAN: Object to form.

22 THE WITNESS: I see that the figure is
23 titled "Functional Block Diagram."

24 BY MR. CHANDLER:

25 Q. And page 11 of Exhibit 1006 shows that the

03:23

1 memory module in the '668 provisional is unbuffered,
2 as also indicated in the title, and you can see that
3 because the signals on the bottom left go from the
4 memory controller to the memory devices without
5 going through a register or a buffer, correct?

03:23

6 MR. TEZYAN: Object to form.

7 THE WITNESS: It looks like -- well, I
8 don't see in this figure -- I see it's illustrating
9 what look like various memory devices and the
10 connections from, for example, the DQ signal coming
11 in.

03:24

12 BY MR. CHANDLER:

13 Q. But you don't see any register or buffer
14 on page 11 of Exhibit 1006, correct?

15 A. I don't see a separate block that seems to
16 be indicating that there's a -- is a logical
17 register or something like that.

03:24

18 Q. On the upper left of page 11 of
19 Exhibit 1006, it shows SDRAMU0 connected to data
20 lines DQ0 through DQ3 and data strobe line RDQS0H,
21 and it also shows SDRAMU1 connected to data lines
22 DQ4 through DQ7 and data strobe line RDQS0L,
23 correct?

03:24

24 A. That seems to be what is shown, yes.

25 Q. Both SDRAMU0 and U1 receive the same chip

03:25

1 select signal CS0 asterisk, correct?

2 A. That seems to be what's visualized.

3 Q. Both SDRAM0 and SDRAM -- I apologize. I
4 misspoke.

5 Both SDRAMU0 and SDRAMU1 are in the same 03:26
6 rank and will perform the same commands at
7 substantially the same time, correct?

8 MR. TEZYAN: Object to form.

9 THE WITNESS: It looks like within that
10 figure, the -- I lost my place -- the U0 DRAM is 03:26
11 connected to the CS0 all the way through the
12 subsequent DRAMs. So they're all sharing this
13 common chip select signal, CS0 asterisk.

14 BY MR. CHANDLER:

15 Q. And as a result of sharing the common chip 03:27
16 select signal CS0 asterisk, those SDRAMs would
17 normally perform the same commands at substantially
18 the same time, correct?

19 MR. TEZYAN: Object to form of the
20 question. 03:27

21 THE WITNESS: I mean, if you're asking if
22 this CS signal is -- is turned on and then each of
23 the memory devices receive a -- a read command, in
24 this figure it looks like they would all perform
25 that read command, in addition to the other required 03:28

1 signaling.

2 BY MR. CHANDLER:

3 Q. Bottom left of page 11 of Exhibit 1006
4 shows that RDQS0H and RDQS0L are connected to the
5 same data strobe line through some resistors,
6 correct? 03:28

7 A. It looks like there are resistors present,
8 at least is what's indicated in the illustration in
9 the lower left.

10 Q. And the illustration on the lower left of 03:28
11 page 11 of Exhibit 1006 shows two data strobe
12 signals tied together through some resistors,
13 including, for example, the two data strobe signals
14 RDQS0H and RDQS0L, correct?

15 A. It looks like it's saying there's a DQS -- 03:29
16 DQS0 to DQS8, and it's showing two paths comprising
17 resistors for the RDQS0H to RDQSAH and an RDQS0L to
18 RDQSAL.

19 Q. Page 7 of Exhibit 1006 also shows in the
20 upper right TD -- two DQS strobe lines connected by 03:30
21 current limiting resistors, correct?

22 A. That is what Figure 3 seems to be showing,
23 yes.

24 Q. The bottom of page 7 of Exhibit 1006 is a
25 timing diagram showing that the difference in time 03:30

1 between DQS1 and DQS2 can be 0.8 nanoseconds,
2 correct?

3 A. It looks like it's showing that the time
4 between the two vertical bars at the transition of
5 DQS1 and then the transition of DQS2 is -- it looks
6 like it's indicating 0.8 nanoseconds.

03:31

7 Q. And 0.8 nanoseconds is calculated as twice
8 the value of tDQSQ, correct?

9 A. That seems to be what the -- this portion
10 of the figure is showing.

03:32

11 Q. DQS1 and DQS2 can be the strobe signals
12 for two memory devices in the same rank, correct?

13 MR. TEZYAN: Object to form.

14 THE WITNESS: I'm trying to refresh myself
15 as to which the DQ -- the DQs in this figure are
16 referring to. Just going back to the description.

03:33

17 Figure 3 is described in 10, paragraph 10,
18 as exemplary embodiment in which current limiting
19 resistors are used to reduce the current flow
20 between DQS pins. And I'm just continuing on.

03:34

21 BY MR. CHANDLER:

22 Q. As we just discussed with reference to
23 page 11 of Exhibit 1006 in the bottom left, two DQS
24 signals, such as RDQS0HL and RDQS0L, can be for two
25 memory devices in the same rank.

03:34

1 And for clarity, if I misspoke, it's
2 RDQS0H and RDQS0L can be two strobe signals tied
3 together going to two memory devices in the same
4 rank, correct?

5 MR. TEZYAN: Object to form.

03:35

6 THE WITNESS: So the RDQS0 -- I'm trying
7 to reorient myself with this figure. One moment.

8 So paragraph 16 is -- is explaining that
9 the two x4 DRAM devices have lower bit densities,
10 are behaving as one x8 of a higher density. And the
11 resistance values of those limiting resistors are to
12 reduce current flowing between two DQS pins.

03:36

13 BY MR. CHANDLER:

14 Q. So in that example where two x4 DRAM
15 memory devices are acting like one x8 memory device,
16 that's an example where the two DQS signals can be
17 for two memory devices in the same rank, correct?

03:37

18 MR. TEZYAN: Object to form.

19 THE WITNESS: If -- if I'm recalling the
20 figure correctly, it can be the case of the
21 resistors in this lower left of Figure 3 are for an
22 RDQS0H and a corresponding RDQS0L that look like,
23 for example, would be the U0 and U1 blocks in the
24 upper left of the figure.

03:37

25

1 BY MR. CHANDLER:

2 Q. On page 7 of Exhibit 1006, the current
3 limiting resistors shown in the upper right are
4 needed because the timing difference between DQS1
5 and DQS2 can create a collision of up to 0.8
6 nanoseconds when DQS1 is driven low and DQS2 is
7 driven high, correct?

03:38

8 MR. TEZYAN: Object to form.

9 THE WITNESS: So in -- it looks like in
10 part I'm addressing this in paragraph 99 of my
11 declaration talking about that the '668 is talking
12 about a -- this resisted network that's resolving
13 collisions during read operations between the two
14 DQS signal drivers. And it involves both the DQS
15 signal voltage as well as the short circuit currents
16 that are responding to I believe points that
17 Dr. Wolfe had made.

03:38

18 BY MR. CHANDLER:

19 Q. As explained at the top of page 5 of
20 Exhibit 1006, if there were not the current limiting
21 resistors shown on page 7, the result would be that
22 during the 0.8 nanoseconds, where there's a
23 potential collision, the current flowing between the
24 two DQS pins can be substantial resulting in heating
25 and eventual failure of devices on the memory

03:39

03:39

03:40



1 module, correct?

2 A. That it's -- I think you're referring to
3 paragraph 15, talking about the scenario when one
4 DQS is low and one is high in this window of time,
5 if the example being the 8 nanoseconds of Figure 3 03:40
6 we discussed earlier, in that scenario, you can have
7 current flowing between the two pins and -- the pins
8 12 and 22 and that can cause heat and potential
9 damage of -- degradation of reliability, things like
10 that. 03:41

11 Q. You may have said 8 nanoseconds, but the
12 potential collision window is 0.8 nanoseconds,
13 correct?

14 A. That's correct.

15 Q. And so the current limiting resistors 03:41
16 shown on the upper right of page 7 are needed to
17 prevent heating and potential failure of devices on
18 the memory module during that 0.8 nanosecond window
19 of time where the two DQS signals can collide,
20 correct? 03:41

21 MR. TEZYAN: Object to form.

22 THE WITNESS: That -- that's one thing
23 that's going on here, that during that .8 nanosecond
24 window, you can have averse conditions occurring
25 that create unwanted current flows and is part of 03:42

1 the system that can be damaging, thermal problems,
2 things like that.

3 BY MR. CHANDLER:

4 Q. On page 15 of Exhibit 1006, there is a
5 table that provides AC timing parameters and
6 specifications, correct?

03:42

7 A. That looks correct.

8 Q. And in the middle of the table on page 18
9 of Exhibit 1006 is the parameter tDQSQ with the max
10 value on the right of 0.4 nanoseconds for a DDR400A
11 memory device, correct?

03:43

12 A. It looks like the tDQSQ is a data strobe
13 edge to out -- I think it's supposed to say output
14 data edge, and the two numbers in this row are .45
15 and .40 nanoseconds, with a footnote that says
16 consists of data pin skew and output data patterns
17 and P channel to N channel variation with the output
18 drivers for -- for any given cycle.

03:43

19 Q. And tDQSQ of 0.4 nanoseconds, that's for
20 the column corresponding to the DDR400A memory
21 device, correct?

03:44

22 A. That's right, the .4 nanoseconds is for
23 the DDR400.

24 Q. And the .4 nanoseconds shown for the row
25 tDQSQ on page 15 of Exhibit 1006, that's consistent

03:44

1 with and corresponds with what's shown on page 7 of
2 Exhibit 1006 where the 0.8 nanoseconds is calculated
3 as two times tDQSQ, correct?

4 A. It looks like those -- assuming the value
5 of .4 for tDQSQ we were just discussing, the result 03:45
6 would be the .8 nanoseconds.

7 Q. Could you turn to Exhibit 1029 again, the
8 DDR2 standard and go to page 26.

9 A. Page 6, you said?

10 Q. 26. 03:45

11 A. Okay.

12 Q. At the bottom of page 26 of the DDR2
13 standard marked as Exhibit 1029, it has Figure 23,
14 and it shows at the bottom of that figure the
15 parameter tDQSQ max that we were just talking about 03:45
16 on pages 7 and 15 of Exhibit 1006, correct?

17 MR. TEZYAN: Object to form.

18 THE WITNESS: I see that in this figure
19 there is a tDQSQ with a qualifier max on it
20 illustrated here. 03:46

21 BY MR. CHANDLER:

22 Q. On page 27 of the DDR2 standard marked as
23 Exhibit 1029, Figure 24 shows the timing for a burst
24 read operation, correct?

25 A. That's right, with certain parameters 03:46

1 associated with it.

2 Q. At time T5 in Figure 24 of Exhibit 1029,
3 there is a slight difference between when the clock
4 transitions at time T5 and when the DQS strobe
5 signal transitions from low to high, and that slight
6 difference is identified as tDQSCK, correct?

03:47

7 MR. TEZYAN: Object to form.

8 THE WITNESS: It looks like that is -- the
9 figure's in trying to -- or intending to illustrate
10 that the tDQS -- I'm sorry, the DQS at T5, or
11 slightly thereafter, transitions or perhaps reaches
12 its midpoint slightly after the T5 -- well, vertical
13 time interval, and the -- the item tDQSCK is shown
14 as -- I'm sorry, it looks like portions of that time
15 window delta there is supposed to be less than or
16 equal to tDQSCK.

03:47

17 BY MR. CHANDLER:

18 Q. If you turn back to Exhibit 1006, which is
19 the '668 provisional, and you go to page 15.

20 A. Let me move this.

03:48

21 (Whereupon, a brief discussion off the
22 record.)

23 BY MR. CHANDLER:

24 Q. All right. Do you have Exhibit 1006,
25 page 15, in front of you?

03:48

1 A. I do.

2 Q. So the '668 provisional application marked
3 as Exhibit 1006 shows on page 15 towards the middle
4 that there is the parameter tDQSCK, which has a
5 value on the right of plus or minus 0.55 nanoseconds
6 for DDR400A memory devices, correct?

03:49

7 A. That's correct.

8 Q. Page 15 of the '668 provisional
9 application marked as Exhibit 1006 also shows
10 towards the middle of that table that the minimum
11 clock cycle is 5 nanoseconds, correct, in particular
12 when the CAS latency is 3.0 and the memory device is
13 a DDR400A?

03:49

14 MR. TEZIAN: Object to form.

15 THE WITNESS: It looks like -- yeah, it's
16 about eight rows down, the clock cycle time for at
17 least CA -- it looks like CL or CAS latency of 3, it
18 shows for the DDR400 a minimum value of
19 5 nanoseconds and a max of 10.

03:50

20 BY MR. CHANDLER:

03:50

21 Q. We discussed earlier the preamble for DQS
22 strobe signals being one clock cycle, so in this
23 table on page 15 of the provisional application
24 marked as Exhibit 1006, the preamble for a DQS
25 strobe signal would be a minimum of 5 nanoseconds,

03:51

1 correct?

2 MR. TEZYAN: Object to form.

3 THE WITNESS: I don't know. I do recall
4 earlier today a figure, that if I recall from memory
5 correctly, the preamble time was one full clock
6 cycle in that particular illustration.

03:51

7 BY MR. CHANDLER:

8 Q. And that's shown in the DDR2 standard
9 marked as Exhibit 1029, for example, in Figure 24 on
10 page 27, correct?

03:52

11 A. That looks to be --

12 MR. TEZYAN: Object to form.

13 THE WITNESS: -- a similar figure to what
14 we were discussing earlier with regard to what
15 looked like a DQS signal preamble period for a
16 specific -- a specific scenario or configuration.

03:52

17 BY MR. CHANDLER:

18 Q. And page 68 of Exhibit 1029 at the top
19 indicates the read preamble needs to be between 0.9
20 and 1.1 clock cycles, correct?

03:52

21 A. The -- at the very top of page 68 there's
22 a row for read preamble, and it looks like for a
23 DDR2 SS 800 the minimum is .9 T CK and the maximum
24 is 1.1 T CK.

25 Q. And turning back to page 15 of

03:53

1 Exhibit 1006, the read preamble needs to be the same
2 as shown in the middle of that table, correct, the
3 read preamble TR pre needs to be between 0.9 and 1.1
4 clock cycles, correct?

5 A. In this table on page 15 of Exhibit 1006, 03:54
6 at least in the right-hand column for a D32K
7 DDR400A, it's showing the read preamble is minimum
8 .9 T CK, maximum 1.1 T CK.

9 Q. So for a DQS strobe signal in Exhibit 1006
10 the length of the preamble is going to be at least 03:54
11 0.9 times 5 nanoseconds, which I believe is 4.5
12 nanoseconds; is that fair?

13 MR. TEZYAN: Object to form.

14 THE WITNESS: If you're talking about in
15 the context of the tens or a six reference, and we 03:54
16 are assuming the minimum clock time for the DDR400
17 of 5 nanoseconds, and the read preamble is supposed
18 to be -- and that's equivalent to the T CK or the
19 minimum T CK, .9 of that is -- I think is
20 4.5 nanoseconds. 03:55

21 BY MR. CHANDLER:

22 Q. Your expert declaration marked as
23 Exhibit 2062 does not discuss the parameter tDQSCK,
24 correct?

25 MR. TEZYAN: Object to form. 03:55

1 THE WITNESS: I don't see that -- that
2 symbol name or that value name used explicitly.

3 BY MR. CHANDLER:

4 Q. Your expert declaration marked as
5 Exhibit 2062 does not discuss the parameter TR pre,
6 correct? 03:56

7 MR. TEZYAN: Object to form.

8 THE WITNESS: So as I recall, at least in
9 a few places I talk about DQS preamble. I think one
10 example is in paragraph 89. But I don't use the 03:56
11 exact symbol name that is shown in the '668 table on
12 page 15, tDQS pre, I believe it is.

13 BY MR. CHANDLER:

14 Q. Could you turn to the '912 patent and go
15 to Figure 2A. Let me know when you're there. 03:57

16 A. Okay.

17 Q. Figure 2A of the '912 patent illustrates a
18 memory module 10, correct?

19 A. Let's see. 2A starts to be described --
20 yes, I'm on, I guess, column 19 at least. 03:58

21 Figure 2A schematically illustrates an
22 exemplary module 10.

23 Q. And the memory module in Figure 2A of the
24 '912 patent has two ranks labeled 32 and 34 each
25 containing multiple memory devices labeled 30, 03:58

1 correct?

2 A. It's a first rank, 32; a second rank, 34;
3 and a plurality of substantially identical memory
4 devices 30.

5 Q. The memory module in Figure 2A of the '912
6 patent includes a logic element 40, correct?

03:58

7 A. That's correct.

8 Q. The memory module in Figure 2A of the '912
9 patent receives two chip select signals, CS0 and
10 CS1, correct?

03:59

11 A. That's correct. Those are -- CS0 and CS1
12 we see coming into the box 10 of the memory module.

13 Q. In Figure 2A of the '912 patent, the chip
14 select signals CS0 goes to the logic element 40 and
15 to all the memory devices in rank 32, correct?

03:59

16 MR. TEZYAN: Object to form.

17 THE WITNESS: It shows that the signal CS0
18 flows into memory module 10 and the block 40, as
19 well -- the logic element 40, as well as flowing to
20 D rank 32 that is comprised of the memory devices
21 30.

04:00

22 BY MR. CHANDLER:

23 Q. In Figure 2A of the '912 patent, the chip
24 select signal CS1 goes to the logic element 40 and
25 also to all the memory devices in rank 34, correct?

04:00

1 MR. TEZYAN: Object to form.

2 THE WITNESS: The CS1 is flowing into the
3 memory module 10, to the logic element 40, and then
4 here we see it going to rank 34 that's comprised of
5 those memory devices 30.

04:00

6 BY MR. CHANDLER:

7 Q. In Figure 2A of the '912 patent, the
8 memory devices in both ranks 32 and 34 also receive
9 from the memory controller the following signals,
10 bank address signals BA0 and BA1, address signals A0
11 to A11, RAS, CAS, and WE, correct?

04:01

12 MR. TEZYAN: Object to form.

13 THE WITNESS: It looks like those signals
14 are coming into the module 10 and going to the
15 rank 32 and rank 34 here.

04:01

16 BY MR. CHANDLER:

17 Q. In Figure 2A of the '912 patent, it does
18 not expressly show any of the data lines or data
19 strobe lines, correct?

20 A. I do not see, for example, a DQ or DQS or
21 a -- a signal denoted as that visualized in
22 Figure 2A.

04:01

23 Q. Figure 3A of the '912 patent illustrates
24 another memory module 10, correct?

25 A. That's correct.

04:02

1 Q. Figure 3A of the '912 patent is similar to
2 Figure 11A of the '436 patent that we discussed
3 earlier, correct?

4 MR. TEZYAN: Object to form.

5 THE WITNESS: Just pulling up the '436.

04:02

6 So there are some similarities. There are
7 some what look like perhaps minor differences in
8 some of the naming, but -- but in terms of the flow
9 or architecture, they look to be similar.

10 BY MR. CHANDLER:

04:03

11 Q. Figure 3A of the '912 patent does not
12 expressly show any of the data lines or data strobe
13 lines, correct?

14 A. I don't see those explicitly visualized in
15 this figure.

04:03

16 Q. Figure 6A of the '912 patent is described
17 in column 24 starting around line 13, correct?

18 A. That is correct.

19 Q. Figure 6A of the '912 patent illustrates a
20 circuit diagram of a conventional memory module 100
21 showing the inner connections between the DQ data
22 signal lines 102 of memory devices A and B and their
23 DQS data strobe signal lines 104, correct?

04:04

24 A. That's what the sentence at line 13 says.

25 Q. And if you look at Figure 6A of the '912

04:04

1 patent, the memory devices A and B need to be in
2 different ranks because if they were in the same
3 rank they would output data to DQ line 112 at the
4 same time causing collisions, correct?

5 MR. TEZYAN: Objection. Form.

04:05

6 THE WITNESS: All it's saying about -- I
7 see it's saying about Figure A, sorry, 6A, is that
8 in certain embodiments the -- I'm sorry -- each of
9 the memory devices have their DQ data signal lines
10 electrically coupled to a common DQ line 112, and
11 the DQS data strobe signals coupled to a common DQS
12 line 114.

04:06

13 BY MR. CHANDLER:

14 Q. A person of ordinary skill in the art
15 would understand that if the memory device A and B
16 were in the same rank during a read operation that
17 would mean that both memory device A and B would try
18 to output data at the same time onto data line DQ
19 112 resulting in a potential collision, correct?

04:06

20 MR. TEZYAN: Objection to form.

04:06

21 THE WITNESS: I'm not sure that this
22 figure gets into that one way or the other. It
23 seems to just be showing a small portion of a
24 circuit in relation to a -- a memory module 100.

25

1 BY MR. CHANDLER:

2 Q. Take a look at Figure 6B of the '912
3 patent, which is described at column 24 including
4 from lines 23 through 58, correct?

5 A. That looks roughly right, yes. 04:07

6 Q. Figure 6B of the '912 patent tries to
7 solve the problem of collisions from back-to-back
8 adjacent read commands, abbreviated BBARX, correct?

9 A. It looks like it's -- at least in the
10 first paragraph are talking about the -- the BBARX 04:08
11 and trying to avoid -- trying to avoid those
12 collisions with this mechanism to electrically
13 isolate the DQS data strobe signal lines 104 of the
14 memory devices from one another during this
15 transition period. 04:08

16 Q. As explained at column 24, starting around
17 line 39, the solution proposed by Figure 6B of the
18 '912 patent is to include FET switches at 122 and
19 124 to prevent the DQS strobe signals from colliding
20 with each other, correct? 04:09

21 A. So it's saying here, starting at 39, that
22 there's the isolation device 120 and it has -- we
23 can see the squares within it, 122 and 124, and
24 those are switches to switch 122 electrically
25 coupled to the first data strobe and the second 04:09

1 switch, 124, to the second.

2 And it mentions -- it makes mention of
3 field effect transistor switches with some
4 references to Texas Instruments parts with what
5 looks like a model number.

04:10

6 Q. And field effects transistor switches are
7 referred to as FET switches, F-E-T switches,
8 correct?

9 A. That's right. That's what it says here.

10 Q. And the passage you just referred to
11 teaches that the FET switches can be used to prevent
12 the DQS strobe signals from colliding with each
13 other, correct?

04:10

14 A. That there's a first switch for a first
15 data strobe line and a second switch for a second
16 data strobe signal line and the -- this reference
17 talking about the embodiment within this reference
18 is saying a field effect transistor is something
19 that can be used here.

04:10

20 Q. And specifically in column 24, lines 35
21 through 38, the purpose of those field effect
22 transistors in isolation device 120 is to prevent
23 the DQS strobe signal lines from causing a
24 collision, correct?

04:11

25 MR. TEZYAN: Object to form.

04:11

1 THE WITNESS: That 35, line 35 is saying
2 that the isolation device 120 of certain embodiments
3 multiplexes the DQS data strobe signal lines 104 of
4 this Figure 6B of the two ranks of memory devices 30
5 from one another to avoid this BBARX collision in
6 this scenario.

04:11

7 BY MR. CHANDLER:

8 Q. Figure 6D of the '912 patent is described
9 at column 25 starting around line 6, correct?

10 A. That looks right.

04:12

11 Q. Figure 6D of the '912 patent also
12 discloses using FET switches similar to 122 and 124
13 that we discussed before, but in Figure 6D the FET
14 switches are on the DQ data lines, correct?

15 MR. TEZYAN: Object to form.

04:12

16 THE WITNESS: One second to review the
17 passage.

18 So it's saying the isolation device 120
19 comprises a pair of switches on the DQ data signal
20 lines, and it refers similar to the switches 122,
21 124 on the DQS data strobe lines 104 from 6B. And
22 then in other embodiments the isolation device 120
23 comprises a logic element as schematically
24 illustrated in 6D.

04:13

25 MR. CHANDLER: I want to introduce a new

04:13

1 exhibit, 1105, which I'm putting in the chat.

2 (Whereupon, Exhibit 1105 was marked for
3 identification.)

4 BY MR. CHANDLER:

5 Q. Let me know when you have it open. 04:14

6 A. Okay.

7 Q. Exhibit 1105 is an annotated version of
8 Figure 5 of the '912 patent.

9 For ease of reference we added some
10 vertical red dash lines to distinguish between the 04:14
11 different time periods and at the bottom we added
12 some green boxes to label the different time
13 periods.

14 Do you understand?

15 MR. TEZYAN: Objection. Foundation. And 04:14
16 objection form.

17 THE WITNESS: Okay.

18 BY MR. CHANDLER:

19 Q. Figure 5 of the '912 patent is described
20 at column 24 starting around line 9, correct? 04:14

21 A. At least in part, yes, about line 9 or so.

22 Q. And can you put Exhibit 1105 side by side
23 with Figure 6D of the '912 patent and let me know
24 when you're ready.

25 A. Okay. 04:15

1 Q. In Figure 5 of the '912 patent, strobe A
2 corresponds to DQSa in Figure 6D, and strobe B
3 corresponds to DQsb in Figure 6D, and the combined
4 strobe in Figure 5 corresponds to line 114 in
5 Figure 6D, correct?

04:16

6 MR. TEZYAN: Objection. Form.

7 THE WITNESS: I see those labels in the
8 figure, and I see the strobe A and strobe B aspects
9 of which we talked about before. I don't -- it
10 looks like at least the combined strobe is some
11 aspect of the various strobes above it being put
12 into a composite waveform.

04:17

13 BY MR. CHANDLER:

14 Q. And you understand that Figure 5 of the
15 '912 patent is illustrating the collision window
16 that can occur when there's back-to-back adjacent
17 read commands and that Figure 6D of the '912 patent
18 provides a solution to that collision window such
19 that back-to-back adjacent read commands can be
20 performed without a collision, right?

04:17

21 MR. TEZYAN: Object to form.

22 THE WITNESS: I would say one of the
23 things Figure 5 is -- is addressing is the collision
24 window that I believe is made or illustrated in
25 Figure 5. And Figure 6D is talking about ways of

04:17

04:18

1 handling the various DQS lines via the block 120 in
2 Figure 6D.

3 BY MR. CHANDLER:

4 Q. So in Figure 6D, there's a switch 140 in
5 block 120 that can switch between the strobe line
6 DQSa and the strobe line DQsb thus preventing a
7 collision, correct?

04:18

8 MR. TEZYAN: Object to form.

9 THE WITNESS: That in -- it looks like the
10 way Figure 6D is described, roughly column 25, is
11 that the dotted square 120 is the isolation device
12 and that within their block 150 is -- in this case
13 is a logic element in 150. And it's being used for
14 the DQS data strobe lines in this case.

04:18

15 BY MR. CHANDLER:

04:19

16 Q. Well, to be clear, 150 is not for the DQS
17 strobe lines, it's for the DQS data lines, correct?

18 A. That's -- that's correct, for Figure 6D.
19 It's the DQa and DQb that are flowing into 150.

20 Q. In Figure 5 of the '912 patent, data A
21 corresponds to DQa in Figure 6D, data B in Figure 5
22 corresponds to DQb in Figure 6D, and combined data
23 in Figure 5 corresponds to line 112 in Figure 6D,
24 correct?

04:19

25 MR. TEZYAN: Object to form.

04:20

1 THE WITNESS: What I recall Figure 5
2 talking about here is -- I seem to have lost my
3 place in the patent. That there is a set of data on
4 the line data A and some data on the line for
5 data B. And it looks like, at a high level, the
6 combined data is to show a combined -- those
7 different transactions, what they look like.

04:21

8 BY MR. CHANDLER:

9 Q. In Figure 5 of the '912 patent there's a
10 first read command labeled "Read A." Then there's a
11 preamble on strobe A. And then there's two clock
12 cycles of strobe signals on strobe A, correct?

04:21

13 MR. TEZYAN: Object to form.

14 THE WITNESS: It looks like Figure A is
15 showing a read command happening around that first
16 dotted red line. And then for the strobe A it looks
17 like it's showing that they pulled low -- or
18 slightly before the second red line and then begins
19 cycling up and down starting at the third red line
20 and stops at the fifth red line here.

04:22

21 BY MR. CHANDLER:

22 Q. And in Figure 5 of '912 patent in response
23 to the Read A command, the data A is output over two
24 clock cycles beginning at the third dashed red line
25 and ending before the fifth dashed red line,

04:22

04:23

1 correct?

2 A. It looks like that's how it's visualized,
3 that there's four transactions of data here, Qa0 to
4 Qa3.

5 Q. And then in Figure 5 in the '912 patent 04:23
6 there's a Read B command at the third dashed line
7 which results in data B being output starting at the
8 fifth dashed line that's red and ending before the
9 last dashed line that's red, correct?

10 A. It looks like it's showing that there's a 04:24
11 command Read B at that second dashed line. And
12 subsequent to that we see the data B line showing
13 four transactions, or pulses, of Qb0 through Qb3.

14 Q. So the net result of Figure 6D in the '912
15 patent, as shown in Figure 5 of the '912 patent, is 04:25
16 that there can be two read commands, A and B,
17 resulting in a strobe signal on line 114 of
18 Figure 6D that starts in what's labeled in
19 Exhibit 1105 as the T1-Pre-a and runs through T5-b.
20 And then you've got data output on the DQ data 04:25
21 line 112 in Figure 6D in time periods T2-a, T3-a,
22 T4-b, and T5-b, as annotated in Figure 5 of
23 Exhibit 1105, correct?

24 MR. TEZYAN: Object to form.

25 THE WITNESS: So Figure 5 is just showing, 04:26

1 as it says, back in I guess column 3 of the '912,
2 that it's illustrating a last data -- data strobe of
3 memory device A colliding with a preamble time
4 interval of the data strobe of memory device B.

5 And so there's the read command -- or the 04:26
6 Read A at the first dotted red line resulting in
7 data A, Qa0 to Qa3. And there's a Read B that's
8 visualized here on the third red dotted line
9 resulting in data B, Qb0 to Qb3.

10 And it's illustrating a collision window 04:27
11 between -- as it's described in column 3, the data
12 strobe of the memory device A and the data strobe of
13 the memory device B and the preamble time.

14 BY MR. CHANDLER:

15 Q. Dr. Brogioli, Netlist did not invent SDRAM 04:27
16 memory devices, correct?

17 MR. TEZYAN: Object to form.

18 THE WITNESS: I don't recall, at least in
19 this IPR, claiming that Netlist invented the SDRAM
20 memory device itself. 04:27

21 BY MR. CHANDLER:

22 Q. Netlist did not invent DDR1 or DDR2 or
23 DDR3 memory devices, correct?

24 A. I don't believe Netlist, to my knowledge,
25 has claimed to invent those memory devices. 04:28

1 Q. Netlist did not invent the memory module,
2 correct?

3 MR. TEZYAN: Object to form.

4 THE WITNESS: I would say that there
5 are -- well, at least in the context of my
6 declaration today, there are other references that
7 may have used the phrase "memory module" in them,
8 but I don't think as a whole they've claimed to
9 necessarily have invented that.

04:28

10 BY MR. CHANDLER:

04:28

11 Q. Netlist did not invent the DIMM memory
12 module, correct?

13 A. I don't believe Netlist has claimed to
14 invent the DIMM as a whole.

15 Q. Netlist did not invent the RDIMM memory
16 module, correct?

04:28

17 MR. TEZYAN: Object to form.

18 THE WITNESS: I don't recall, at least in
19 this proceeding, citing to documents saying Netlist
20 invented the RDIMM itself.

04:28

21 BY MR. CHANDLER:

22 Q. And Netlist did not invent the buffered
23 DIMM memory module, correct?

24 MR. TEZYAN: Object to form.

25 THE WITNESS: I don't recall Netlist or --

04:29

1 today pulling up a Netlist referencing Netlist
2 invented the idea of a buffer, if that's what you're
3 asking, generically.

4 BY MR. CHANDLER:

5 Q. Do you have any corrections or 04:29
6 clarifications you would like to make to any of your
7 testimony today?

8 MR. TEZYAN: Objection. Form.

9 THE WITNESS: Not that I have sitting here
10 right now, no. 04:29

11 MR. CHANDLER: All right. I pass the
12 witness.

13 MR. TEZYAN: Let's take a ten-minute
14 break.

15 THE VIDEOGRAPHER: Off the record at 04:29
16 4:29 p.m. Pacific time.

17 (Whereupon, a brief recess was taken.)

18 THE VIDEOGRAPHER: On the record at
19 4:40 p.m. Pacific time.

20 EXAMINATION 04:40

21 BY MR. TEZYAN:

22 Q. Good evening, Dr. Brogioli.

23 Do you recall questions from counsel
24 regarding certain x32 data issues?

25 A. Yes, I do. 04:41

1 Q. Could you please pull up Ex. 1030. Let me
2 know when you have it.

3 A. Okay.

4 Q. Can you please go to page 1.

5 And for clarity, this is the stamped
6 page 1 that at the top reads "Double Data Rate (DDR)
7 SDRAM Specification."

04:41

8 Let me know when you're there.

9 A. Okay.

10 Q. Do you see on the bottom there's a note in
11 a black box?

04:41

12 A. Yes.

13 Q. Could you please read the first sentence
14 of that note.

15 A. "This specification defines the minimum
16 set of requirements for JEDEC 64M x4/x8/x16 DDR
17 SDRAMs."

04:41

18 Q. Could you please turn to Exhibit 1029,
19 JESD79-2. Let me know when you have that, please.

20 A. Okay.

04:42

21 Q. Could you please go to page 7 of
22 Exhibit 1029.

23 A. Okay.

24 Q. What bit widths are specified on page 7 of
25 Exhibit 1029?

04:42

1 A. X4, x8, and x16.

2 Q. And what bit widths are specified on
3 page 8 of Exhibit 1029?

4 A. X4, x8, and x16.

5 Q. Are any other bit widths specified in 04:42
6 Exhibit 1029, JESD79-2?

7 A. No.

8 Q. Other than the x4, x8, and x16 bit widths
9 specified in JESD79 that's Exhibit 1030, and
10 JESD79-2, Exhibit 1029, are there any other bit 04:43
11 widths specified in Exhibit 1029 or Exhibit 1023 --
12 I'm sorry, Exhibit 1030?

13 A. Not that I'm aware of, no.

14 Q. Are you aware of any examples of JEDEC
15 standardized DDR DRAM memory modules with a single 04:43
16 device per rank?

17 MR. CHANDLER: Object to form.

18 THE WITNESS: No. No, I'm not.

19 BY MR. TEZYAN:

20 Q. I'm going to drop an exhibit in the chat 04:43
21 and let me know when you get it.

22 A. Okay.

23 Q. Do you see what I've marked as
24 Exhibit 2117, the deposition transcript of Herald
25 Stone, Ph.D., dated Friday August 18, 2023? 04:44

1 (Whereupon, Exhibit 2117, having been
2 previously marked, was referred to.)

3 MR. CHANDLER: And just to be clear, this
4 is -- was previously marked; is that correct?

5 MR. TEZYAN: I believe this was served but
6 not filed. So I may have misspoke.

04:44

7 MR. CHANDLER: Okay. Well, if it's been
8 served but not filed, we object to it, and you're
9 not going to have an opportunity to file it because
10 you already had your opportunity to file it.

04:45

11 And we would object to it as hearsay
12 because it's a deposition of Micron's expert outside
13 of this IPR proceeding. And it was taken in a
14 district court action, not in any of these IPR
15 proceedings, and we were not given notice of that
16 deposition. We weren't given the opportunity to
17 attend that deposition. So it's hearsay and
18 inadmissible, as well as being irrelevant.

04:45

19 MR. TEZYAN: Understood. We disagree.

20 Q. Dr. Brogioli, can you please go to page 43
21 of this transcript.

04:45

22 MR. CHANDLER: Objection. Leading.

23 THE WITNESS: Okay.

24 BY MR. TEZYAN:

25 Q. Can you please read lines 6 through 11.

04:46

1 MR. CHANDLER: Objection. Hearsay.

2 Having the witness read hearsay still makes it
3 hearsay.

4 BY MR. TEZYAN:

5 Q. Dr. Brogioli, could you please read
6 lines 6 through 11.

04:46

7 MR. CHANDLER: Same objection.

8 THE WITNESS: Out loud or to myself?

9 BY MR. TEZYAN:

10 Q. Out loud, please.

04:46

11 A. So line 6 is, "Question, Why isn't it
12 consistent?"

13 And the answer is, "Ranks are -- I'm
14 reading now to 2058. Ranks are specific to memory
15 modules and refer to a subarray made of multiple
16 DRAM components."

04:46

17 Q. Okay. Could you please go to page 44 of
18 this exhibit.

19 A. Okay.

20 Q. And could you please read from lines 15
21 through 20.

04:46

22 MR. CHANDLER: Objection. Leading. As
23 well as objection hearsay. Having the witness read
24 hearsay testimony is still hearsay. And also
25 objection, lack of relevance, from a different

04:47

1 proceeding.

2 THE WITNESS: So, "Question, And so in the
3 present and past, rank has always been more than one
4 chip?"

5 "The Witness, In the present and past for 04:47
6 this definition of rank, for this definition, it has
7 been more than one chip."

8 (Whereupon a brief discussion off the
9 record.)

10 BY MR. TEZYAN: 04:47

11 Q. Okay. And could you please go to PDF
12 page 46.

13 A. Okay.

14 Q. And could you please read lines 22 through
15 25 all the way through line 8 on the next page, 04:48
16 skipping the objection.

17 MR. CHANDLER: Objection. Leading.
18 Objection. Outside the scope of cross. And
19 objection hearsay. You're having the witness read
20 hearsay which is still hearsay. 04:48

21 And it also doesn't provide admissible
22 evidence to simply have one expert repeat what the
23 other expert says. Completely improper. Objection.

24 THE WITNESS: You want me to begin on
25 line 20; is that correct? 04:48

1 BY MR. TEZYAN:

2 Q. Line 22 of page 46, please.

3 MR. CHANDLER: Same objection.

4 THE WITNESS: Okay.

5 And question from I guess Mr. Sheasby.

04:48

6 "Let me ask it this way, once JEDEC was
7 created and they began to specify memory, DDR memory
8 devices, the width was either 64 or 72, correct?

9 "Answer, In the DDR and the DDR2 standards
10 the widths are 64 and 72. That is correct.

04:49

11 "Question, Okay. And for widths of 64 and
12 72, in the context of JEDEC DDR, a rank is always
13 more than one chip?

14 "The Witness, Again, in the past, it has
15 been more than one chip."

04:49

16 BY MR. TEZYAN:

17 Q. And the witness is Micron's expert,
18 Dr. Stone, correct?

19 A. That's correct.

20 Q. Do you agree with Dr. Stone that in the
21 past and present a rank of DDR DRAM devices is
22 always more than one chip?

04:49

23 MR. CHANDLER: Objection. Leading.

24 Objection. Outside the scope of cross. And

25 objection hearsay. Asking the witness to repeat

04:50

1 hearsay is still hearsay.

2 THE WITNESS: So I do agree with that
3 statement, yes.

4 MR. TEZYAN: And, Ted, your phone was
5 breaking up. There was some weird feedback. 04:50

6 MR. CHANDLER: Objection. Leading.

7 MR. TEZYAN: No, I heard the objection.
8 I'm just letting you know. It just sounds kind of
9 strange when you're talking.

10 MR. CHANDLER: Okay. 04:50

11 BY MR. TEZYAN:

12 Q. Okay. Dr. Brogioli, do you recall
13 questions from counsel this morning about whether
14 you analyzed validity using your construction or
15 Dr. Wolfe's construction? 04:50

16 A. Yes, I do.

17 Q. For clarity, Dr. Wolfe's construction of
18 rank is that a rank can comprise one or more memory
19 devices, right?

20 A. That's correct. 04:51

21 Q. Did you analyze the invalidity arguments
22 made by petitioner under your own construction of
23 rank?

24 A. I used, well, both constructions of rank
25 in my analysis. 04:51

1 Q. So to be clear, you also analyzed the
2 validity arguments made by petitioner under
3 Dr. Wolfe's construction of rank as well, correct?

4 A. That's correct.

5 Q. Do you recall questions from counsel about
6 paragraph 1 of the '244 provisional?

04:51

7 And that's Exhibit 1005 if you want to
8 pull it up.

9 A. I -- yes, I think I recall questions
10 around this paragraph and as part of the -- this
11 part of the document.

04:52

12 Q. Okay. And do you recall discussions with
13 counsel regarding whether the '244 provisional
14 discloses DDR DRAMs?

15 A. Yes.

04:52

16 Q. At the time of the invention when a person
17 of ordinary skill in the art reads the '244
18 provisional would they understand that the DRAMs
19 would include JEDEC standardized DDR devices?

20 A. Yes, that there were JEDEC
21 standardizations for those devices widely used in
22 industry. That's what I was getting at earlier
23 today in the discussion. That's what someone
24 reading this document would -- would have in mind.

04:52

25 Q. Would they understand that the invention

04:52

1 described in the '244 provisional was to work with
2 the JEDEC standard memory modules and DDR devices?

3 A. Yes, they would.

4 Q. Why is that?

5 A. Well, the JEDEC, as the reference mentions 04:53
6 DRAM, and JEDEC had put out standardization of these
7 DRAM components, as well as these were widely used
8 components in industry, there's nothing in the
9 reference saying that this is some other type of
10 memory system outside of -- outside of that. 04:53

11 Q. So a person of skill in the art reading
12 the '244 provisional would understand that the
13 inventors were in possession of a memory module of
14 DDR memory devices operating as described in
15 Claim 16? 04:53

16 A. Yes, that's right, that they would be in
17 possession of it.

18 MR. TEZYAN: Pass the witness.

19 MR. CHANDLER: Can we go off the record
20 and take a short break? 04:53

21 MR. TEZYAN: Sure. How short?

22 THE VIDEOGRAPHER: Off the record at
23 4:53 p.m. Pacific time.

24 (Whereupon, a brief recess was taken.)

25 THE VIDEOGRAPHER: Just a moment, 04:57

1 everyone.

2 On the record at 4:57 p.m. Pacific time.

3 EXAMINATION

4 BY MR. CHANDLER:

5 Q. Dr. Brogioli, could you pull up Claim 16
6 of the '912 patent and let me know when you have it.

04:58

7 A. Okay.

8 Q. You were asked by counsel for Netlist
9 about the JESD79 specification and JES79-2
10 specification, correct?

04:58

11 A. That's correct.

12 Q. Claim 16 of the '912 patent is not limited
13 to the JESD79 or the JESD79-2 specification,
14 correct?

15 MR. TEZYAN: Object to form.

04:58

16 THE WITNESS: I would say I don't see that
17 mentioned explicitly in Claim 16, but it -- the
18 reference contemplates the JEDEC standards.

19 BY MR. CHANDLER:

20 Q. Let's be clear about that.

04:59

21 Are you -- is it your testimony that
22 Claim 16 of the '912 patent is limited to the
23 requirements of JESD79 and JESD79-2?

24 MR. TEZYAN: Objection. Form. And
25 outside the scope.

04:59

1 THE WITNESS: I -- so as I said earlier,
2 the '912 patent contemplates JEDEC. I haven't
3 formed an opinion that -- in my declaration that
4 Claim 16 itself is limited to a specific JEDEC --
5 specific specification or version of that 04:59
6 specification.

7 BY MR. CHANDLER:

8 Q. So to be clear, you are not offering the
9 opinion that Claim 16 of the '912 patent is limited
10 to any particular JEDEC specification, including, 04:59
11 but not limited to, JESD79 and JESD79-2, correct?

12 MR. TEZYAN: Objection. Misstates
13 testimony.

14 THE WITNESS: I -- I haven't offered an
15 opinion either way that Claim 16 itself is limited 05:00
16 to a specific JEDEC specification or -- or a version
17 thereof.

18 BY MR. CHANDLER:

19 Q. Claim 16 of the '912 patent requires
20 double data rate memory devices, correct? 05:00

21 A. DDR, double data rate memory devices, yes.

22 Q. And as we discussed earlier, there are
23 SRAM double D, double data rate memory devices,
24 correct?

25 MR. TEZYAN: Objection. Form. 05:00

1 THE WITNESS: I believe we looked at a
2 reference this afternoon that was contemplating
3 double data rate SRAM type devices.

4 BY MR. CHANDLER:

5 Q. Claim 16 of the '912 patent does not
6 explicitly require DRAM memory devices, correct?

05:01

7 MR. TEZIAN: Objection to form.

8 THE WITNESS: Well, the reference itself
9 talks about DRAM devices in the specification.

10 BY MR. CHANDLER:

05:01

11 Q. My question's a little different. I'm
12 talking about the requirements of Claim 16 of the
13 '912 patent.

14 A. I don't see the Claim 16 language saying
15 DRAM explicitly.

05:01

16 Q. And if you look directly below the
17 Claim 16 in the '912 patent, the next claim in the
18 re-exam certificate is Claim 28, which does
19 specifically require DDR DRAM memory, correct?

20 A. I'm skipping ahead to 28 for you.

05:02

21 I see that claim -- Claim 28 on page 44
22 mentions double data rate dynamic random access
23 memory.

24 Q. Claim 16 of the '912 patent does not
25 require DDR DRAM memory, it just requires DDR

05:02

1 memory, which can be a problem in DDR DRAM memory,
2 correct?

3 MR. TEZYAN: Object to the form of the
4 question.

5 THE WITNESS: Well, as I certainly talked 05:02
6 about earlier today, there's DDR DRAM and DRAM and
7 JEDEC contemplated by the '912, but I don't see --
8 if you're asking do I see DRAM explicitly mentioned
9 in Claim 16, I don't see DRAM explicitly said right
10 there. 05:03

11 BY MR. CHANDLER:

12 Q. But you were asked by counsel for Netlist
13 about x14 [sic], x16, x32 memory devices, and maybe
14 x8 as well, right?

15 MR. TEZYAN: Object to form. 05:03

16 THE WITNESS: I think I was asked about
17 x4, x8, and x16 only.

18 BY MR. CHANDLER:

19 Q. Nothing in Claim 16 of the '912 patent
20 limits the claim to either x4 or x8 or x16 memory 05:03
21 devices, correct?

22 MR. TEZYAN: Object to form.

23 THE WITNESS: I don't recall seeing x4,
24 x8, or x16 mentioned explicitly in the language of
25 that claim. 05:03

1 BY MR. CHANDLER:

2 Q. The '912 patent at column 6, line 17,
3 explicitly contemplates memory devices having a bit
4 width of 32 bits, correct?

5 MR. TEZYAN: Objection. Form. And asked
6 and answered.

05:04

7 THE WITNESS: So the -- or this section of
8 column 6 mentions the embodiments herein include,
9 but are not limited to, RAM, DRAM, SDRAM, double
10 data rate, DRAM, of DDR1, DDR2, DDR3.

05:04

11 And then states, "In addition, memory
12 devices 30 having bit widths of three" -- I'm
13 sorry -- "4, 8, 16, 32, as well as other bit widths,
14 are compatible with embodiments described herein."

15 So it's saying something in addition in
16 that language.

05:05

17 BY MR. CHANDLER:

18 Q. You are not offering the opinion that
19 Claim 16 of the '912 patent excludes memory devices
20 that are 32 bits wide, correct?

05:05

21 MR. TEZYAN: Object to form.

22 THE WITNESS: I would say largely my
23 discussion of x32 memory devices was in response to
24 certain arguments with Dr. Wolfe. I don't recall
25 offering an opinion as to whether Claim 16 was

05:05

1 limited to a certain x8 or otherwise in my
2 declaration.

3 BY MR. CHANDLER:

4 Q. Column 5 of the '912 patent around line 61
5 discloses that memory modules compatible with the
6 embodiments of the '912 patent can be 32 bits wide,
7 correct?

05:05

8 MR. TEZYAN: Objection. Asked and
9 answered.

10 THE WITNESS: I see that it says that here
11 in this paragraph starting at column 5, line 56,
12 32 bytes, 64 bits, et cetera.

05:06

13 BY MR. CHANDLER:

14 Q. You are not offering the opinion that
15 Claim 16 of the '912 patent excludes memory modules
16 that are 32 bits wide, correct?

05:06

17 A. I don't recall offering an opinion on
18 Claim 16 as to whether the claim itself specified a
19 bit width or precluded another bit width. I don't
20 recall addressing that in my declaration.

05:07

21 Q. You were asked questions about the '244
22 provisional application marked as Exhibit 1005,
23 correct?

24 A. That's correct.

25 Q. At the time of the '244 provisional

05:07

1 application marked as Exhibit 1005, there were a
2 number of different types of memory devices that
3 were known, including SRAM, SGRAM, single data rate,
4 SDRAM, double data rate, SDRAM, and more beyond that
5 list, correct?

05:08

6 MR. TEZYAN: Objection. Form.

7 THE WITNESS: Speaking generally as types
8 of memory that were out there, that's true.

9 BY MR. CHANDLER:

10 Q. DDR is a type of synchronous DRAM,
11 correct?

05:08

12 A. That's correct.

13 Q. The '244 provisional application marked as
14 Exhibit 1005 does not refer to synchronous DRAM, or
15 SDRAM, correct?

05:09

16 MR. TEZYAN: Objection. Form.

17 THE WITNESS: I would say it mentions
18 DRAM. And someone reading the reference would be
19 aware of the various JEDEC standards around DRAM or
20 synchronous DRAM.

05:09

21 BY MR. CHANDLER:

22 Q. But they would also be aware of the DRAM
23 that's not synchronous, correct?

24 MR. TEZYAN: Object to form.

25 THE WITNESS: I would think they might be

05:09

1 aware that there would be such a thing out there, or
2 had been, you know, present in the -- in the field.

3 BY MR. CHANDLER:

4 Q. And you say that a person of ordinary
5 skill in the art would be aware of DDR memory
6 devices, but they would also be aware of memory
7 devices that are not DDR, correct?

05:09

8 MR. TEZYAN: Object to form.

9 THE WITNESS: That there were types of
10 memory out in the industry that were not DDR like
11 JEDEC contemplates.

05:09

12 BY MR. CHANDLER:

13 Q. And we looked, for example, at the SPD
14 standard that indicates that memory modules can use
15 several different types of memory, correct?

05:10

16 MR. TEZYAN: Object to form.

17 THE WITNESS: I would say that that SPD
18 specification says you can set up bit values for a
19 number of different things. I haven't seen that
20 necessarily all of those were used or not used at
21 any given time. But you could set different byte
22 fields to different things.

05:10

23 BY MR. CHANDLER:

24 Q. We also looked at the Jacob's paper marked
25 as Exhibit 1034 which talks about a number of

05:10

1 different types of memory devices, including Rambus
2 DRAM, correct?

3 MR. TEZYAN: Object to form.

4 THE WITNESS: I would say the Jacob's
5 paper contemplates -- mentioned things like certain
6 variants of Rambus.

05:11

7 BY MR. CHANDLER:

8 Q. You indicated in response to questions
9 from counsel for Netlist that you analyzed
10 Dr. Wolfe's claim construction?

05:11

11 A. That's correct.

12 MR. TEZYAN: Object to form.

13 THE WITNESS: I addressed his claim
14 construction in my declaration, I should say.

15 BY MR. CHANDLER:

05:11

16 Q. And I understand that you address
17 Dr. Wolfe's claim construction for rank and you
18 disagree with it.

19 But where do you contend in your
20 declaration did you apply Dr. Wolfe's claim
21 construction as part of your validity analysis or
22 the grounds asserted against Claim 16 in the '912
23 patent?

05:11

24 MR. TEZYAN: Object to form.

25 THE WITNESS: It sounds like that would be

05:12

1 addressed in the -- the analysis I did of the
2 various references that he had offered and stated he
3 had made about them.

4 BY MR. CHANDLER:

5 Q. I'm a little unclear. Are there
6 particular page or paragraph numbers?

05:12

7 MR. TEZYAN: Object to form.

8 THE WITNESS: Yeah, I would say in my
9 discussion of the various grounds that he had
10 offered, as I recall there were three of them, that
11 his own construction wasn't met by those grounds
12 either.

05:12

13 BY MR. CHANDLER:

14 Q. Where do you say that in your declaration
15 marked as Exhibit 2062?

05:13

16 A. I guess I would say that it's -- it's
17 covered throughout the discussion in the
18 declaration.

19 Q. Is there any particular paragraphs you can
20 identify?

05:13

21 MR. TEZYAN: Object to form.

22 THE WITNESS: I guess I don't have a
23 specific sentence to cite in mind or a specific
24 paragraph necessarily. It would be my overall
25 discussion of the grounds in combinations that

05:13

1 Dr. Wolfe had provided.

2 BY MR. CHANDLER:

3 Q. Do you have any corrections or
4 clarifications that you would like to make to your
5 testimony?

05:14

6 A. Not at this time, no.

7 MR. CHANDLER: All right. That will
8 conclude the deposition. Thanks very much.

9 THE VIDEOGRAPHER: Counsel, would you like
10 us to conclude the video deposition at this time?

05:14

11 MR. CHANDLER: Yes, please.

12 THE VIDEOGRAPHER: Before I do, I just
13 need to ask if anyone needs a copy of the video.

14 MR. CHANDLER: Yes, we will -- petitioner
15 will take a copy.

05:14

16 THE VIDEOGRAPHER: Thank you.

17 MR. TEZYAN: I guess we'll take one as
18 well, on whatever timeline they get it.

19 THE VIDEOGRAPHER: Thank you very much.

20 This concludes today's deposition of
21 Michael C. Brogioli. We're off the video record at
22 5:14 p.m. Pacific time on October 3rd, 2023.

05:14

23 (Whereupon, the deposition was concluded
24 at 5:14 p.m.)

25

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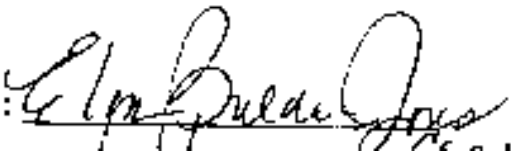
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4 Reporter of the State of California, duly authorized
5 to administer oaths pursuant to Section 2025 of the
6 California Code of Civil Procedure, do hereby
7 certify that

8 MICHAEL CHARLES BROGIOLI,
9 the witness in the foregoing deposition, was by me
10 duly sworn to testify the truth, the whole truth and
11 nothing but the truth in the within-entitled cause;
12 that said testimony of said witness was reported by
13 me, a disinterested person, and was thereafter
14 transcribed under my direction into typewriting and
15 is a true and correct transcription of said
16 proceedings.

17 I further certify that I am not of counsel or
18 attorney for either or any of the parties in the
19 foregoing deposition and caption named, nor in any
20 way interested in the outcome of the cause named in
21 said deposition dated the 10th day of
22 October, 2023.

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