UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.,
Petitioner,

v.

NETLIST, INC.,
Patent Owner.

Case No. IPR2022-00615
U.S. Patent No. 7,619,912

DECLARATION OF MICHAEL C. BROGIOLI, PH.D. IN SUPPORT OF PATENT OWNER'S RESPONSE

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EX2001	Complaint for Patent Infringement and Summons in *Netlist, Inc., v. Google, Inc.*, Case No. 4:09-cv-05718 ("Google Action"), filed December 4, 2009.
EX2002	Complaint for Patent Infringement and Summons in *Netlist Inc. v. Inphi Corp.*, Case No. 2:09-cv-06900, filed September 22, 2009.
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EX2020	Inphi Corporation, 2010 Form 10-K (March 4, 2011).
EX2021	*Inphi to Partner With Samsung Semiconductor to Showcase LRDIMM Technology at VMworld 2012*, GlobeNewswire (August 21, 2012).
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EX2023	ORDER Re: Motions for Summary Judgement and Related Applications, in *Netlist Inc. v. Samsung Electronics Co., Ltd.*, Case No. 8:20-cv-00993, filed October 14, 2021.
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EX2025	Redline Comparison of EX1035 (U.S. Patent No. 7,363,422 to Perego) With Related U.S. Patent No. 7,356,639.

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EX2027	*Why Samsung Needs To Move Beyond Android – And Google*, ComputerWorld (July 11, 2014).
EX2028	Smart Global Holdings, Inc. 2020 Form 10-K (October 22, 2020).
EX2029	Inphi's Feb. 13, 2012 Comments in Reexamination, Reexamination Control No. 95/001,339.
EX2030	Samsung Electronics Co., Ltd. 2021 Half-year Business Report.
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EX2036	Emails Between Netlist's Counsel and Samsung's IPR Counsel (Aug. 26 – 29, 2022).
EX2037	Emails Between Netlist's Counsel and Samsung's Litigation Counsel (Aug. 24 – 29, 2022).
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EX2048	Declaration of H. Annita Zhong ISO of Netlist's Exhibit 2047
EX2049	PC3200/PC2700/PC2100/PC1600 DDR SDRAM Unbuffered SO-DIMM, Reference Design Specification, Revision 1.4 (Jan. 10, 2003)
EX2050	PC133 SDRAM Registered DIMM, Revision 1.4 (Feb. 2002)
EX2051	Smart Modular Technologies SG5127FBD225652-SA FBDIMM datasheet (March 20, 2007)

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EX2052	Crisp, R., "Direct Rambus Technology: The New Main Memory Standard," *IEEE Micro*, pp. 18-28 (1997)
EX2053	"XDR Architecture " by Rambus (last modified December 2005), downloaded from https://web.archive.org/web/20110724044154/http://www.rambus.com/assets/documents/products/dl_0161_v0_8.pdf
EX2054	Samsung datasheet on Rambus Direct RDRAM (Dec. 2001)
EX2055	*Samsung Electronics Co., Ltd. v. Netlist, Inc.*, IPR2022-00063, Paper 1
EX2056	Deposition Transcript of Dr. Andrew Wolfe from IPR2022-01427/IPR2022-001428 (June 27, 2023)
EX2057	Micron, *256MB, 512MB, 1GB (x72, ECC, SR) 240-Pin DDR2 SDRAM RDIMM Features* (2003), downloaded from https://mediawww.micron.com/-/media/client/global/documents/products/datasheet/modules/rdimm/htf9c32_64_128x72.pdf?rev=ca2587e210f14889ad6fe88e3511e938
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EX2060	JEDEC Standard, FBDIMM Specification: DDR2 SDRAM Fully Buffered DIMM (FBDIMM) Design Specification, JESD205 (March 2007) ("JESD205")
EX2061	*Samsung Electronics Co., Ltd. v. Netlist, Inc.*, IPR2022-00063, Paper 13 (P.T.A.B. May 5, 2022).
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EX2100	Datasheet for Samsung's RIMM MR16R1624
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EX2104	Deposition Transcript of Dr. Vivek Subramanian in IPR2022-00639
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EX2107	*Frequently Asked Questions*, What is the difference between a "bank" and a "rank?", Micron, https://www.micron.com/support/faqs (last accessed Mar. 7, 2023).
EX2108	*Frequently Asked Questions*, What is a "rank"?, Micron, https://www.micron.com/support/faqs (last accessed Mar. 7, 2023).
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EX2111	August 22, 2017 Notice of Allowance in '215 Patent File History
EX2112	*What is a Memory Rank*, Crucial: Micron, https://www.crucial.com/support/articles-faq-memory/what-is-a-memory-rank (last accessed Mar. 7, 2023)
EX2113	*Lecture 15: DRAM Main Memory Systems*, University of Utah, https://my.eng.utah.edu/~cs6810/pres/11-6810-15.pdf
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EX2116	Datasheet for Micron DDR2 SDRAM FBDIMM MT36HTF51272FD

I, Michael C. Brogioli, declare as follows:

I. INTRODUCTION

1. Netlist, Inc. has retained me to provide testimony regarding the technology involved in U.S. Patent No. 7,619,912 ("the '912 patent") and how it compares with the asserted art.

2. I am being compensated for my work in this matter at my standard hourly rate for consulting services. My compensation is not dependent on the outcome of the case and does not affect the substance of my statements in this Declaration. I have no financial interest in the matter or the patents at issue.

3. I have reviewed the specification and the claims of the '912 patent. I am familiar with the technology involved therein, having worked in the field for the past 23+ years.

4. To prepare this Declaration, I have considered the petition, Dr. Wolfe's declaration, the exhibits already submitted, my own experience and knowledge, and the documents cited herein. I provide my testimony from the perspective of a person of ordinary skill in the art at the time of the invention. I was at least a person of ordinary skill in the art at the time of the invention. I am familiar with the knowledge and skill level of these people at the time of the invention because I was intimately involved in the industry at the time and had

frequent interactions with such people at the relevant time. I have also been asked to apply the plain and ordinary meaning of the terms from the perspective of a person of ordinary skill in the art in light of the specification and other intrinsic evidence.

II. EXPERT QUALIFICATIONS AND COMPENSATION

5. Below is a summary of my education and experience. My *curriculum vitae*, included as **Appendix A** hereto, records my education, experience, and publications in greater detail.

6. I am currently an Adjunct Professor of Electrical and Computer engineering at Rice University in Houston, Texas, and Managing Director of Polymathic Consulting in Austin, Texas. I received my Bachelor of Electrical Engineering from Rensselaer Polytechnic Institute in 1999, my Master of Science in Electrical and Computer Engineering from Rice University in 2003, and my Doctorate of Electrical and Computer Engineering from Rice University in 2007.

7. While at Rice University, I developed various computer architecture designs for embedded and high-performance systems, including

memory systems. For example, from 1999 to 2003, I worked in the area of low-power computing, specifically focusing on dynamic power management and performance of configurable memory systems, including SRAM based caches. From 2002 to 2004, I developed Spinach, a computer architecture design and modeling toolset, which models system components common to all programmable computing environments, including memory systems, microprocessors, interconnects, etc. From 2004 to 2009, I developed Spinach DSP-FPGA, a modular and composable simulator design infrastructure for programmable and reconfigurable embedded SOC architectures specifically targeting mobile, low-power, and embedded and portable computing devices. From 2005 to 2009, I developed and published a retargetable compiler infrastructure and hardware design exploration toolkit for systems related to embedded computing technologies, which is also used in the design space exploration of memory systems and related technologies. Many of these tools have been used at United States universities in the area of electrical and computer engineering research.

8. In the late 1990s, I was a hardware and software developer at Vicarious Visions in New York, developing third-party titles for Nintendo's handheld consoles, in addition to various hardware interfaces and software optimizations related to the limited memory I/O and size. During my career, I have served as Chief Technology Officer, advisory board, and board of directors member, often in co-founding roles.

9. From June 2006 to August 2007, I worked as the Technical Co-Founder of Method Seven LLC in Boston, MA, working with high-performance software and hardware systems architecture. I am currently a co-founder, co-inventor, and Chief Technology Officer of Network Native, an Internet of Things technology company as well as others that are detailed on my CV (Appendix A).

10. I have held the position of Adjunct Professor at Rice University since 2009 and the position of Managing Director at Polymathic Consulting since 2011. At Rice University, I instruct graduate-level curriculum in the areas of computer architecture, hardware and software systems. I also advise on university research and various design initiatives. At Polymathic Consulting, I

work with a range of technologists from early-stage start-ups to Fortune 500 companies on similar technologies.

11. From 2008 to 2009, I was Senior Engineer working in high-performance compiler designs and next-generation microprocessors and architectures at Freescale Semiconductor in Austin, TX. From November 2009 to October 2011, I was Chief Architect, Senior Member Technical Staff, at Freescale Semiconductor in Austin, TX (formerly Motorola), responsible for management of technology, engineering roadmaps, design lead on software infrastructure, and next-generation microprocessor architectures for embedded computing. During my tenure at Freescale Semiconductor, I was in charge of system developer tools for processor design, both in the hardware and software spaces. These included tools used for the programming of processors, simulation and design of processors, and related technologies.

12. I have previously worked for Texas Instruments' Advanced Architecture and Chip Technology division in Houston, Texas, in the areas of high-performance mobile and embedded systems design at the hardware and systems software level, specifically around heterogeneous computing, high-

speed bus, and interconnect technologies. I also have worked at Intel Corporation's Microprocessor Research Labs in the areas of computer architecture and compiler technologies.

13. I am recognized as an expert in the field of computer architecture, computer hardware and computer software systems as they relate to the subject matter at hand. I am a member of the Institute of Electrical and Electronics Engineers (IEEE) and have been a Program Committee member for the IEEE and ACM Design Automation Conference since 2011, and have held the role of Program Chair of Design Automation Conference in the area of Embedded Computing.

14. Over the past 15 plus years, I have authored numerous peer-reviewed publications, as well as engineering books in the area of computer hardware and software design. Many of these incorporate technologies specific to the subject matter at hand, including memory system design, optimization for memory systems, and interconnect technology. These publications are disclosed in my *curriculum vitae*, attached as Appendix A. I have previously served as an engineering consultant and testifying witness on matters related to, and

including, microprocessors, chip technology, memory systems, memory modules and related aspects of JEDEC standards, as well as various memory and interconnect technologies. My *curriculum vitae* contains more information on my background and experience, as well as the cases in which I have served as an expert witness over at least the past four years.

15. I am also a named inventor on the following United States patent applications: U.S. Pat. Appl. 17/578,408; U.S. Pat. Appl. 17/306,839; U.S. Pat. Appl. 17/060,625; U.S. Pat. Appl. 16/721,913; and U.S. Pat. Appl. 15/110,643.

16. More information regarding the patent applications for which I am a named inventor can be found in my *curriculum vitae*, attached as Appendix A.

17. I have extensive firsthand experience with the technology underlying the ’912 patent. I have worked with various SRAM and DRAM technologies, including software and systems optimization related to size and performance of such memories, since the late 1990s. My development of various embedded systems work in the late 1990s include SRAM technologies and high speed access of said systems. Further work in the late 1990s included optimization of memory intensive applications for efficient high performance

usage of SRAM and DRAM memory systems, and optimizations for memory system I/O. My work in the early 2000s was around the use of configurable memory systems and caches comprised of SRAM technologies, and the optimization of memory accesses to maximize CPU compute throughput. I have designed memory system architectures, and system simulation and design technologies both in my doctoral research and publications, as well as within my various roles in industry going back to the early and mid-2000s.

III. A PERSON OF ORDINARY SKILL IN THE ART

18. I have been asked to apply Samsung's definition of a person of ordinary skill in the art for this declaration, in particular the supposed knowledge that such persons would have had at the time of the invention. I understand that Samsung asserts that such people would be familiar with the "various standards of the day including the JEDEC industry standards, and knowledgeable about the design and operation of standardized DRAM and SDRAM memory devices and memory modules and how they interacted with the memory controller of a computer system." Pet. 5-6. I understand that Samsung also asserts that a person of ordinary skill in the art would have been "familiar with the structure and

operation of circuitry used to access and control computer memories, including sophisticated circuitries such as ASICs and CPLDs, and more low-level circuits such as tri-state buffers, flip flops and registers." Pet. 6. I apply Samsung's proposed level of knowledge in my analysis.

19. I note that in the 2004-2005 timeframe, the vast majority of the DRAM devices and modules would have followed the JEDEC specifications, such that a general reference to DRAM, especially in the context of usage with computer and server systems, would suggest JEDEC-style DRAM devices or modules to a person of ordinary skill in the art. For instance, a person of ordinary skill in the art would recognize the "64Mb×8," "128Mb×8," "128Mb×4" DRAM devices mentioned in the '912 patent, 1:35-2:15, as referring to JEDEC-style DDR2 devices. EX1029, p.7. Similarly, they would recognize the x64 and x72-wide memory modules mentioned in the '912 patent, 2:16-22, as referencing JEDEC-style memory modules. EX1032, p.4.20.4-10 (x64 and x72 memory module organizations). Additionally, because "rank" is a JEDEC-developed concept for DRAM devices, they would recognize that the memory modules discussed in the '912 patent as JEDEC-style DRAM modules.

20. In the 2004-2005 timeframe, there were also known non-JEDEC-style memories and modules. One was Rambus's proprietary DRAM devices and modules. The first generation of Rambus DRAM is called RDRAM, using a fully multiplexed bus in which address, control, and data all travel over the same set of electrical wires, at different times. EX1034, p.7. RDRAMs used packet transactions where "first an address/control packet is driven, then the data." *Id.* Because RDRAM devices each have only a single bus and no "separate segments dedicated to separate functions," they are limited to one transaction per cycle, thus limiting the bus's potential concurrency. *Id.* RDRAM was therefore "not considered well suited to the PC main memory market." *Id.*

21. RDRAM then evolved to Concurrent RDRAM, which had a byte-wide data segment plus one-bit address segment and one-bit control segment. *Id.* This expanded the number of potential actions that could be performed simultaneously to three. *Id.*

22. Concurrent RDRAM further evolved into Direct RDRAM, "which increases the width of the data segments to two bytes, the width of the address segments to five bits, and the width of the control segments to three bits." *Id.*;

see also EX2052. "Like its predecessors, [Direct RDRAM] has a wide internal bus connected via a high-speed interface to a narrow external bus." EX2052, p.21. "The narrow on-chip bus is serialized and deserialized to provide a 144-/128-bit data path into the core, which provides 16 bytes every 10 ns internally. The Rambus interface transforms the 10-ns internal bus into an external 1.25-ns bus that is 2 bytes wide to yield the 1,600-Mbyte/s bandwidth." *Id.*

23. "The Direct Rambus channel includes an 18-bit wide bidirectional data field and an 8-bit-wide field carrying commands and row and column addresses. Like its predecessors, random column addresses can be supplied to the Direct RDRAMs while data is being transferred." *Id.*, p.22. Direct Rambus supports fully concurrent RAS and CAS operation in a pipelined microarchitecture that includes write buffering and each device can service up to four outstanding requests. *Id.*

24. In JEDEC-style DIMMs, several DRAMs are "ganged together in parallel to provide the necessary aggregate bandwidth," thus increasing the size of independent banks but not their number. *See* EX2052, p. 23 (Fig. 8(a), reproduced below). In contrast, "a Direct RDRAM spans the entire channel"

and "the CPU accesses each RDRAM independently." *Id.*, p. 23. "So each DRAM directly adds to the number of memory banks accessible to the memory controller." *Id.*; *see* Fig. 8(b) below.

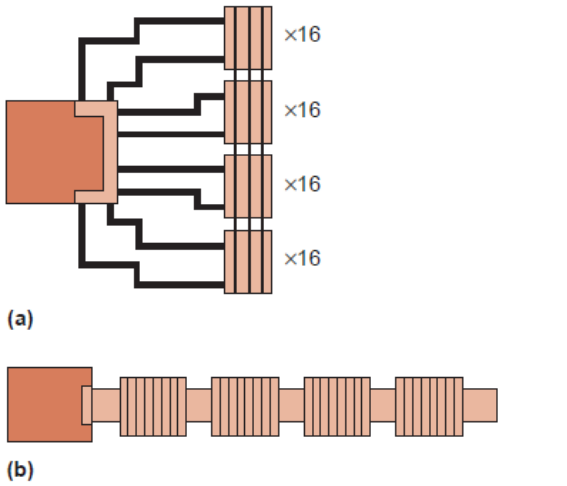


Figure 8. Bank counts: a 32-Mbyte, 64M SDRAM system with four large banks (a) versus a 32-Mbyte, 64M Direct RDRAM system with 32 small banks (b).

25. DRAM modules comprised of Direct RDRAMs are abbreviated as RIMMs. *Id.*, p.26. Although similar in form, "RIMMs are fundamentally different" from the JEDEC-style DRAMs in that "[i]nstead of being connected in parallel, RIMMs are connected in series when installed in a system." *Id.* The serial connections in RIMMs result in significantly different electrical characteristics of RIMMs compared to JEDEC-style DIMMs. RDRAMs mounted on a RIMM behave as if they were soldered directly to the

motherboard, thus "virtually eliminat[ing] signal integrity concerns associated with DIMMs because there are no long stubs on a RIMM." *Id.*, p.26-27.

26. After Direct Rambus, Rambus also developed XDR architecture featuring a differential clock input (clock from master), request/command bus RQ11…0 and bidirectional differential data bus DQ15…0/DQN15…0. The data busses are connected point-to-point, but the request bus may be connected to several memory chips in parallel (multi-drop). *See*, *e.g.*, EX2053, p.8-10.

27. A person of ordinary skill in the art would be aware of the basic architecture and operation of Rambus's DRAMs and modules and understand that they differ greatly from JEDEC-style devices and modules. Although a persons of ordinary skill in the art as defined by Samsung were supposedly familiar with "various standards," they are not alleged to be familiar with proprietary technology such as Rambus's various generations of RDRAMs and RIMMs. Modifying Rambus technology to fit the JEDEC-mode and vice versa at the time of the invention would be beyond the skill level of a person of ordinary skill in the art given their significant differences in architecture and signaling protocols.

28. For example, RIMMs don't have the concept of organizing memory devices in "ranks" as in JEDEC. RIMM I/O signals do not include those for chip-select signals, though it does have a 5-bit bus containing control and address information for column accesses and a 3-bit bus containing control and address information for row accesses. *See* EX2100, pp. 3-4.

Signal	Pins	I/O	Type	Description
RCOL4.. RCOL0	A73, B73, A71, B71, A69	I	RSL	Column bus. 5-bit bus containing control and address information for column accesses.
RCTM	A79	I	RSL	Clock to master. Interface clock used for transmitting RSL signals to the Channel. Positive polarity.
RCTMN	A81	I	RSL	Clock to master. Interface clock used for transmitting RSL signals to the Channel. Negative polarity.
RDQA8.. RDQA0	A91, B91, A89, B89, A87, B87, A85, B85, A83	I/O	RSL	Data bus A. A 9-bit bus carrying a byte of read or write data between the Channel and the RDRAM device. RDQA8 is non-functional on modules x16 RDRAM devices.
RDQB8.. RDQB0	B61, A61, B63, A63, B65, A65, B67, A67, B69	I/O	RSL	Data bus B. A 9-bit bus carrying a byte of read or write data between the Channel and the RDRAM device. RDQB8 is non-functional on modules x16 RDRAM devices.
RROW2.. RROW0	B77, A75, B75	I	RSL	Row bus. 3-bit bus containing control and address information for row accesses.

29. The Direct RDRAMs have corresponding I/O signals. EX2054 (Samsung RDRAM datasheet, preliminary), p.3.

Signal	I/O	Type	# Pins center	Description
CTMN	I	RSL[b]	1	Clock to master. Interface clock used for transmitting RSL signals to the Channel. Negative polarity.
CTM	I	RSL[b]	1	Clock to master. Interface clock used for transmitting RSL signals to the Channel. Positive polarity.
RQ7..RQ5 or ROW2..ROW0	I	RSL[b]	3	Row access control. Three pins containing control and address information for row accesses.
RQ4..RQ0 or COL4..COL0	I	RSL[b]	5	Column access control. Five pins containing control and address information for column accesses.
DQB7.. DQB0	I/O	RSL[b]	8	Data byte B.Eight pins which carry a byte of read or write data between the Channel and the RDRAM.

30. This layout is consistent with that shown in Perego-422's Figures 4A-4B.

IV. THE '912 PATENT

A. General Overview

31. The '912 patent relates to memory module technology, and more specifically, to a concept called rank multiplication. A memory module is a device that contains individual memory devices (e.g. DRAM chips) arranged in "ranks" on a printed circuit board. *Id.* at 1:26-31; *see infra*, V. A memory module communicates with a computer system (e.g. a computer server) via the computer system's memory controller. *Id.* at 11:43-48. At the time of the invention, most computer systems supported accessing only one or two ranks,

limiting the number of ranks that can be added per memory module. *Id.*, 1:20-2:42.

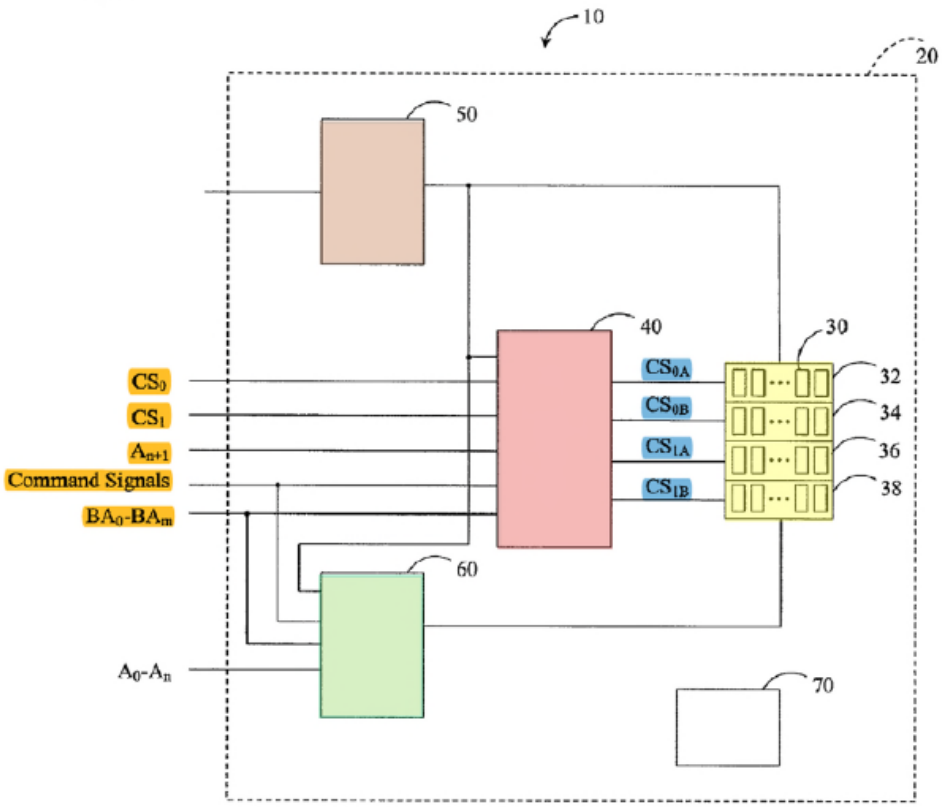
32. The '912 patent teaches that one way to upgrade the memory capacity of a memory module is to use on-module logic to present a memory module with, *e.g.*, 2n physical ranks of memory devices, as a module with n (virtual) ranks to the computer system. *Id.*, 6:64-7:19. In this way, "even though the memory module 10 actually has the first number of [physical] ranks of memory devices 30, the memory module 10 simulates a virtual memory module by operating as having the second number of [logical or virtual] ranks of memory devices 30." *Id.*, 7:9-13. This technique is commonly referred to as "rank multiplication."

33. Rank multiplication allows a designer to expand the number of ranks and hence the total memory capacity on a memory module. It also enables them to construct a memory module of a given capacity using lower density memory devices that often cost less. *Id.*, 4:42-58, 22:5-14. For example, for the same 1 GB memory capacity, it could be more cost-effective to use thirty-six

256-Mb DRAMs arranged in 4 ranks than eighteen 512-Mb DRAMs arranged in two ranks. *Id.*, 4:42-58, 4:59-5:5.

34. Figure 1A from the '912 patent, with Petitioner's annotations below, illustrates an example of a memory module with rank multiplication capability. The memory module has a register 60 (green), a logic element 40 (red), and a phase-lock loop ("PLL") device 50 (brown).

Figure 1A:



35. The logic element receives a set of input control signals from the computer system that include chip-select signals CS_0-CS_1, address signal A_{n+1}, and bank address signals BA_0-BA_m. *Id.*, 7:35-53; Fig. 1A. From the computer system's perspective, it is connected to only two ranks of memory devices, to be selected by CS_0 or CS_1, even though the memory devices are arranged in four physical ranks. *Id.*, 6:55-7:19. In response to the received input control signals, the logic element then generates a set of output control signals, corresponding to the four physical ranks of the memory devices. *Id.*, 6:61-63. The logic element 40 also receives command signals (such as read/write) from the computer system. *Id.*, 6:55-61, 7:46-53. In response to the command signal and the input signals, the logic element transmits the command signal to the memory devices on the selected rank of the memory module. *Id.*, 7:50-53. In some embodiments, command signals are transmitted to only a single memory device on a multi-device rank at a time. *Id.*, p. 44, 3:9-43.[1]

[1] For shorthand, I refer to individual elements of claim 16 in the same manner as Petitioner. *See* Pet. x-xi.

36. The ’912 patent discloses, among other teachings, two examples including sections of Verilog code to perform logic translations. EX1001, 14:8-10 (“Examples 1 and 2 provide exemplary sections of Verilog code compatible with certain embodiments described herein”).

37. Example 2 provides code that corresponds to “a logic element 40 which receives one gated CAS signal from the computer system and which generates two gated CAS signals.” EX1001, 17:30-32, 18:28-30; 17:28-31 (Example 2 discloses “memory density multiplication from 256 Mb to 512 Mb using DDR2 memory devices and gated CAS signals with the row A_{13} density transition bit”). The memory devices on the memory module of Example 2 are organized in two physical ranks, denoted as “rnk0” and “rnk1” in the code in Example 2.

```
assign    pcas_0_N = ~cas0_o;
assign    pcas_1_N = ~cas1_o;
assign    rd0_o_R1 = rasN_R & cas0_o & weN_R & ~rs0N_R; // rnk0 rd cmd cyc
assign    rd1_o_R1 = rasN_R & cas1_o & weN_R & ~rs0N_R; // rnk1 rd cmd cyc
assign    wr0_o_R1 = rasN_R & cas0_o & ~weN_R & ~rs0N_R; // rnk0 wr cmd cyc
assign    wr1_o_R1 = rasN_R & cas1_o & ~weN_R & ~rs0N_R ; // rnk1 wr cmd cyc
```

EX1001, p. 31.

38. As shown below, in Example 2, the logic element receives a set of input signals including bank address signals (denoted as "bnk0" and "bnk1"), row address (A13), and a single chip-select signal (denoted in the code as "rs0") from the host memory controller.

```
// latched a13 flags cs0, banks 0-3
 always @(posedge clk_in)
  if (actv_cmd_R & ~rs0N_R & ~bnk1_R & ~bnk0_R ) // activate
  begin
          1_a13_00 <= a13_r ;
  end
 always @(posedge clk_in)
  if (actv_cmd_R & ~rs0N_R & ~bnk1_R & bnk0_R)   // activate
  begin
          1_a13_01 <= a13_r ;
  end
 always @(posedge clk_in)
  if (actv_cmd_R & ~rs0N_R & bnk1_R & ~bnk0_R)   // activate
  begin
          1_a13_10 <= a13_r ;
  end
 always @(posedge clk_in)
  if (actv_cmd_R & ~rs0N_R & bnk1_R & bnk0_R)    // activate
  begin
          1_a13_11 <= a13_r ;
  end
```

EX1001, p. 30 (set of input signals).

39. In response to the set of input signals received, for example for a read command, the Verilog code in Example 2 provides that the logic element receives an input CAS signal and generates two output CAS signals (cas0_o and cas1_o), corresponding to the two physical ranks of memory devices (rnk0 and rnk1). *See* below and EX1001, 17:30-32, 18:28-30. Signals cas0_o and cas1_o are then used to generate two module read commands that are transmitted to each of the two physical ranks of memory devices (rnk0 and rnk1).

```
// gated cas
assign cas_i = ~(casN_R);
assign cas0_o = ( ~rasN_R & cas_i)
        | ( rasN_R & ~1_a13_00 & ~bnk1_R & ~bnk0_R & cas_i)
        | ( rasN_R & ~1_a13_01 & ~bnk1_R & bnk0_R & cas_i)
        | ( rasN_R & ~1_a13_10 & bnk1_R & ~bnk0_R & cas_i)
        | ( rasN_R & ~1_a13_11 & bnk1_R & bnk0_R & cas_i)
        ;
assign cas1_o = ( ~rasN_R & cas_i)
        | ( rasN_R & 1_a13_00 & ~bnk1_R & ~bnk0_R & cas_i)
        | ( rasN_R & 1_a13_01 & ~bnk1_R & bnk0_R & cas_i)
        | ( rasN_R & 1_a13_10 & bnk1_R & ~bnk0_R & cas_i)
        | ( rasN_R & 1_a13_11 & bnk1_R & bnk0_R & cas_i)
        ;
```

EX1001, p. 30-31 (generating cas0_o and Cas1_o corresponding to the two physical ranks rnk0 and rank1, respectively)

```
assign    rd0_o_R1 = rasN_R & cas0_o & weN_R & ~rs0N_R; // rnk0 rd cmd cyc
assign    rd1_o_R1 = rasN_R & cas1_o & weN_R & ~rs0N_R; // rnk1 rd cmd cyc
```

EX1001, p. 31 (read commands for the two physical ranks rnk0 and rnk1)

40. While a command is transmitted to both rnk0 and rank 1 in this embodiment, the Verilog code in Example 2 further provides for two control signals specifically for controlling two separate FET switches: "**en_fet_a**," corresponding to one of the memory devices, e.g., memory device "a," in physical rank 0 (rnk0) and "**en_fet_b**" corresponding to one of the memory devices, e.g. memory device "b," in physical rank 1 (rnk1). Signal "en_fet_a" is used to enable or disable the FET switch for memory device "a" in physical rank 0 (rnk0), and "en_fet_b" is used to enable or disable FET switch for

memory device "b" from physical rank 1 (rnk1). By providing for the selective enabling or disabling of the FET switch associated with memory device "a" or memory device "b," Example 2 teaches how to transmit a command to a single memory device on a physical rank of multiple memory devices.

```
always @(posedge clk_in)
 begin
 if (
   (rd0_o_R2 & ~rd1_o_R4)                                   // pre-am rd if no ped on rnk 1
  | rd0_o_R3                                                // 1st cyc of rd brst
  | rd0_o_R4                                                // 2nd cyc of rd brst
  | (rd0_o_R5 & ~rd1_o_R2 & ~rd1_o_R3)                      // post-rd cyc if no ped on rnk 1
  | (wr0_o_R1)                                              // pre-am wr
  | wr0_o_R2 | wr0_o_R3                                     // wr brst 1st & 2nd cyc
  | (wr0_o_R4)                                              // post-wr cyc (chgef9)
  | wr1_o_R1 | wr1_o_R2 | wr1_o_R3 | wr1_o_R4 // rank 1 (chgef9)
  )
                 en_fet_a <= 1'b1;                          // enable fet
 else
                 en_fet_a <= 1'b0;                          // disable fet
 end
always @(posedge clk_in)
        begin
        if (
              (rd1_o_R2 & ~rd0_o_R4)
             | rd1_o_R3
             | rd1_o_R4
             | (rd1_o_R5 & ~rd0_o_R2 & ~rd0_o_R3)
           | (wr1_o_R1)                                     // (chgef8)
           | wr1_o_R2 | wr1_o_R3
      | (wr1_o_R4)                                          // post-wr cyc (chgef9)
      | wr0_o_R1 | wr0_o_R2 | wr0_o_R3 | wr0_o_R4           // rank 0 (chgef9)
            )
                 en_fet_b <= 1'b1;                          //
        else
                 en_fet_b <= 1'b0;
        end
```

EX1001, p. 31 ("R#" denotes the cycle number of the read burst, *e.g.*, R1, R2, R3, R4 corresponds to the first, second, third, and fourth cycle respectively).

41. A comparison to the Verilog code described in Example 1 further illustrates this point. Example 1 provides exemplary code for a logic element

that receives as input one chip-select signal from the computer system, and which generates two chip-select signals for two physical ranks on the module. EX1001, 14:20-24; 14:17-20 ("An exemplary section of Verilog code compatible with memory density multiplication from 512 Mb to 1 Gb using DDR2 memory devices with the BA_2 density transition bit is listed below in Example 1.").

```
// Gated Chip Selects
assign      pcs0a_1 = (~rs0_in_N & ~ras_in_N & ~cas_in_N)                    // ref,md reg set
            | (~rs0_in_N & ras_in_N & cas_in_N)                              // ref exit, pwr dn
            | (~rs0_in_N & ~ras_in_N & cas_in_N & ~we_in_N & a10_in)         // pchg all
            | (~rs0_in_N & ~ras_in_N & cas_in_N & ~we_in_N & ~a10_in & ~ba2_in)// pchg single bnk
            | (~rs0_in_N & ~ras_in_N & cas_in_N & we_in_N      & ~ba2_in)    // activate
            | (~rs0_in_N & ras_in_N & ~cas_in_N            & ~ba2_in)        // xfr
            ;
assign      pcs0b_1 = (~rs0_in_N & ~ras_in_N & ~cas_in_N)                    // ref,md reg set
            | (~rs0_in_N & ras_in_N & cas_in_N)                              // ref exit, pwr dn
            | (~rs0_in_N & ~ras_in_N & cas_in_N & ~we_in_N & a10_in)         // pchg all
            | (~rs0_in_N & ~ras_in_N & cas_in_N & ~we_in_N & ~a10_in & ba2_in)// pchg single bnk
            | (~rs0_in_N & ~ras_in_N & cas_in_N & we_in_N      & ba2_in)     // activate
            | (~rs0_in_N & ras_in_N & ~cas_in_N            & ba2_in) // xfr
            ;


always @(posedge clk_in)
  begin
        acs_cyc2 <= acs_cyc1 ;      // cs active
        ba2_cyc2 <= ba2_r ;
        ba2_cyc3 <= ba2_cyc2 ;
        ba2_cyc4 <= ba2_cyc3 ;
        ba2_cyc5 <= ba2_cyc4 ;
        rd_cmd_cyc2 <= rd_cmd_cyc1 & acs_cyc1;
        rd_cmd_cyc3 <= rd_cmd_cyc2 ;
        rd_cmd_cyc4 <= rd_cmd_cyc3 ;
        rd_cmd_cyc5 <= rd_cmd_cyc4 ;
        rd_cmd_cyc6 <= rd_cmd_cyc5 ;
        rd_cmd_cyc7 <= rd_cmd_cyc6 ;
        wr_cmd_cyc2 <= wr_cmd_cyc1 & acs_cyc1;
        wr_cmd_cyc3 <= wr_cmd_cyc2 ;
        wr_cmd_cyc4 <= wr_cmd_cyc3 ;
        wr_cmd_cyc5 <= wr_cmd_cyc4 ;
```

EX1001, p. 28-29 (Example 1 denoting similar set of input signals received as in Example 2, e.g., address signal "a10," bank address signal "ba2," and chip-select signal "rs0").

42. However, in contrast to Example 2, the Verilog code in Example 1 provides for the generation of ***multiple*** control signals to control ***multiple*** DQS signals from ***multiple*** memory devices in each rank. This is achieved by using multiple FET switches: fet1a, fet2a, and fet3a to control DQS signals from three different memory devices belonging to the same physical rank (rnk0); and fet1b,

fet2b, and fet3b to control DQS signals from 3 different memory devices belonging to the same physical rank (rnk1).[2]

```
// DQ FET enables
assign        enq_fet1 = dq_cyc | dq_ncyc
assign        enq_fet2 = dq_cyc | dq_ncyc ;
assign        enq_fet3 = dq_cyc | dq_ncyc
assign          enq_fet4 = dq_cyc | dq_ncyc ;
assign          enq_fet5 = dq_cyc | dq_ncyc ;
// DQS FET enables
assign        ens_fet1a = dqs_cyc_a | dqs_ncyc_a ;
assign        ens_fet2a = dqs_cyc_a | dqs_ncyc_a ;
assign        ens_fet3a = dqs_cyc_a | dqs_ncyc_a ;
assign        ens_fet1b = dqs_cyc_b | dqs_ncyc_b ;
assign        ens_fet2b = dqs_cyc_b | dqs_ncyc_b ;
assign        ens_fet3b = dqs_cyc_b | dqs_ncyc_b ;
```

Memory devices in rnk0

Memory devices in rnk1

EX1001, p. 30.

43. In other words, Example 1 teaches enabling or disabling the DQ and DQS lines for a plurality of memory devices in each corresponding rank, not a single memory device. But as explained above, Example 2, teaches selectively enabling or disabling of the FET switch associated with memory device "a" or memory device "b" in each corresponding rank. *Supra*, ¶40.

[2] At the time of the invention, each memory device had only one DQS pin. *See* EX1001, 21:13-16 ("For two 'x4' memory devices 30 to work in tandem to mimic a 'x8' memory device, ***the*** relative DQS pins of the two memory devices 30 in certain embodiments are advantageously tied together, as described more fully below.").

B. Relevant Prosecution History

44. The application that issued as the ’912 patent was filed on September 27, 2007. EX1002. There were no official rejections during the prosecution of the ’912 patent. *Id.* The ’912 patent issued on November 17, 2009. EX1001.

45. On April 20, 2010, a first request for *inter partes* reexamination of claims 1-51 of the ’912 patent was filed by third party requester Inphi Corp. (“Inphi”), which was assigned control No. 95/001,339. EX1010, 1366. In its request for reexamination, Inphi asserted that claim 16 of the ’912 patent was invalid because “[o]ne of ordinary skill in the art would have understood from [Amidi] that the command signal may be transmitted to the DDR memory devices serially in a sequential fashion.” EX2016, 141.

46. On October 20, 2010, a second request for *inter partes* reexamination of claims 1, 3-4, 6- 11, 15, 18-22, 24-25, 27-29, 31-34, 36-39, 41-45, and 50 of the ’912 patent was filed by third party requester SMART Modular Technologies (WWH), Inc. (“SM”), which was assigned control No. 95/000,578. EX1010, 1366. On October 21, 2010, a third request for *inter*

partes reexamination of claims 1, 3-4, 6-11, 15, 18-22, 24-25, 27-29, 31-34, 36-39, 41-45, and 50 of the ’912 patent was filed by third party requester Google, Inc. (“Google”) which was assigned control No. 95/000,579. *Id.* On February 25, 2011, the PTO merged the ’578, ’579, and ’339 proceedings into a single proceeding. *Id.*, 1367. The PTO authorized all Requesters to file comments. EX1010, 1367 n.1 (Decision Merging Proceedings: “Each time that the patent owner files a response to an action on the merits from the Patent and Trademark Office, the third-party requester shall have one opportunity to file written comments addressing issues raised by the action of the Office or the patent owner's response thereto.”).

47. On April 4, 2011, the Examiner issued a non-final Office Action in the merged proceedings, wherein the Examiner rejected certain claims of the ’912 patent, but affirmed the validity of claim 16. EX1010, 1402-03, 1405. Specifically, the Examiner concluded that, “[w]ith respect to claims 16, 17, Requester 1 asserts that ‘[o]ne of ordinary skill in the art would have understood from [Amidi] that the command signal may be transmitted to the DDR memory devices serially in a sequential fashion’ without any reasoned explanation to

support the assertion. Conclusion of obviousness requires more than a mere conclusory statement." *Id.*, 1402-03; *see also id.*, 1405 (same for Ground 5: Amidi in view of a reference called "Dell2").

48. On October 14, 2011, the Examiner issued another Office Action which again confirmed claim 16 as patentable. *Id.*, 2899-900. On January 14, 2012, Patent Owner filed a response to the October 14, 2011 Office Action, in which Patent Owner rewrote claim 16 in independent form. *Id.*, 3106-07. No other changes were made to claim 16 throughout reexamination. *See* EX1001, p. 44, 3:9-43.

49. On February 13, 2012, Inphi filed its comments in the merged proceedings. EX2029, 26-28. In these comments, Inphi argued that the examiner should reconsider the confirmation of claim 16:

> The Examiner should reconsider the confirmation and allowance of claim 16 over Amidi because the limitation, "wherein the command signal is transmitted to only one DDR memory device at a time" is disclosed by Amidi. As in all DDR memory devices, Amidi provides RAS and CAS signals to isolate a particular memory device in an array of memory cells at the intersection of the particular row and column given by those signals…. The

> intersection of row and column accesses given by RAS and CAS signals, and associated address signals, is for the purpose of accessing a single memory cell. Id. For instance, as shown in Murdocca at p. 248, each intersection of row and column is a unique memory device. Thus, this limitation is inherent in Amidi.

Id., 26-27.

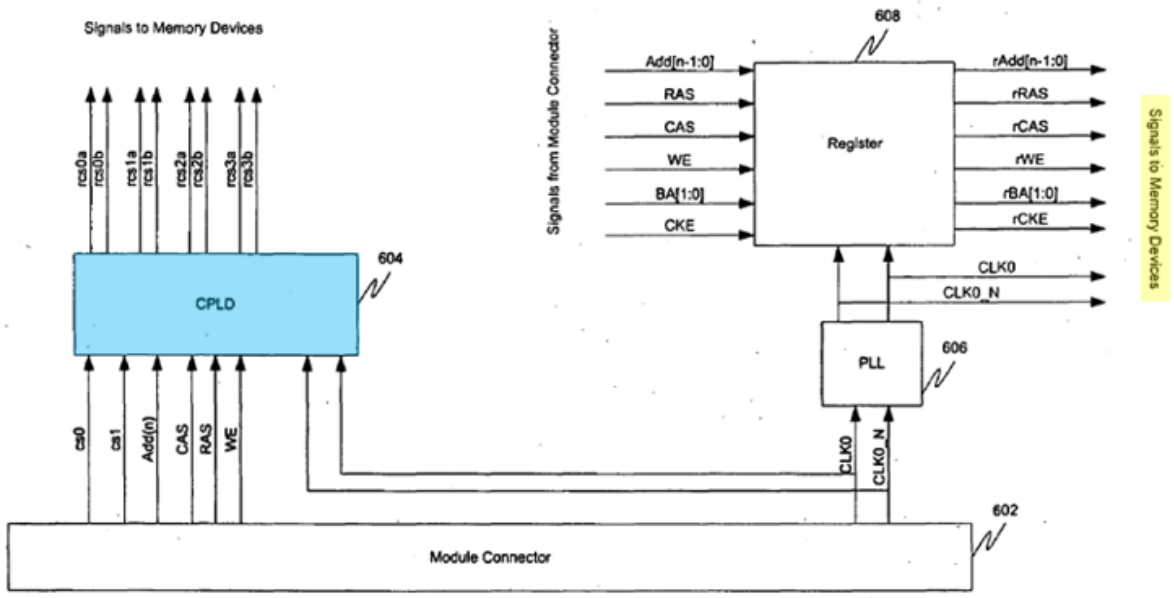
50. On November 13, 2012, the Examiner issued another non-final Office Action in the merged proceedings, wherein the Examiner again confirmed the patentability of claim 16:

> With respect to claims 16 and 17, Requester 1 asserts that "[o]ne of ordinary skill in the art would have understood from the '152 publication that the command signal may be transmitted to the DDR memory devices serially in a sequential fashion" without any reasoned explanation to support the assertion. Conclusion of obviousness requires more than a mere conclusory statement. The claims require transmission of a command signal to only one DDR memory device at a time. Requester has not provided a reasonable explanation as to why one skilled in the art would transmit a command signal to only one DDR memory device at a time ***when there is a plurality of memory devices in a rank***.

Id., 3865-67. Additionally, the Examiner responded to Inphi's February 13, 2012 comments, rejecting the argument that Amidi disclosed Element [16.e]:

> With respect to claims 16 and 17, Requester 1 argues that the limitation "wherein the command signal is transmitted to only one DDR memory device at a time" is disclosed by Amidi allegedly because Amidi provides RAS and CAS signals to isolate a particular memory device in an array of memory cells at the intersection of the particular row and column given by those signals for the purpose of accessing a single memory cell (Comments, pp. 19-20). This is not a persuasive argument because Amidi does not disclose that RAS or CAS signals are transmitted to only one DDR memory device that is being accessed at a time. ***In fact, Figure 6 shows that RAS and CAS signals are transmitted to all devices***. See also JEDEC standard 21-C, p. 4.20-3- 12. RAS, CAS, and WE signals are transmitted to all 18 devices D0-D17 in the DIMM module.

Id., 3904.



Row Address Decoding
FIG.6A

51. On August 14, 2013, SM filed comments in response to the November 13, 2012 Office action, in which, SM argued that Amidi disclosed [16.e] to the extent this limitation was construed to cover single-device ranks:

> **Scope and Content of Amidi**[.] In addition to the limitations of Claim 15, Claim 16 requires "the command signal is transmitted to only one DDR memory device at a time." To the extent the Examiner construes the limitation "the command signal is transmitted to only one DDR memory device at a time" as requiring only that the command signals are sent to a single rank

> because ***"one memory device" encompasses a rank of memory, Amidi discloses this limitation***.

Id., 4442.

52. On March 21, 2014, the Examiner issued an Action Closing Prosecution, in which the Examiner entered SM's comments into the record, but nonetheless maintained its construction of claim 16. *Id.*, 4828, 4830, 4702-4, 4723-25. Thereafter, the parties filed their respective notices of appeal to the Patent Trial and Appeal Board ("Board").

53. On May 31, 2016, the Board issued a Decision on appeal, affirming the Examiner's decision to confirm as valid claim 16. EX1011, 78-80. The Board explained:

> We agree that Amidi teaches using a command signal to read or write to a cell within a DDR memory device. *See* Amidi ¶ 61. Presumably, because Amidi discusses a particular cell within a bank, Requester 1 contends that the command signals are being transmitted to one DDR memory device at a time as recited. R1 App. Br. 18; R1 Reb. Br. 9. Yet, as the Examiner indicates:
>
> > Requester 1 asserts that "[o]ne of ordinary skill in the art would have understood from the '152 publication [of

> Amidi] that the command signal may be transmitted to the DDR memory devices serially in a sequential fashion" without any reasoned explanation to support the assertion…. The claims require transmission of a command signal *to only one DDR memory device at a time*. Requester has not provided a reasonable explanation as to why one skilled in the art would transmit a command *signal to only one DDR memory device at a time when there is a plurality of memory devices in a rank*.

RAN 29 (emphasis added).

That is, Figures 6A and 6B of Amidi show various command signals (e.g., CS0, CS1, CKE, CAS, RAS, and WE) being transmitted to more than one memory device. Amidi ¶ 62, Fig. 6A-6B (stating "Signals to Memory Devices" at the far right) Moreover, Amidi's Figures 6A and 6B undermines Requester l's assertion that delivering command signals to two or more memory cells at a time would create data bus contention. See R1 Reb. Br. 9. That is, Amidi's Figures 6A and 6B further teach or suggest that the command signal is transmitted to a cell within multiple memory devices at a time. Thus, although Dr. Wang's testimony states that the RAS and CAS signals are used to isolate a particular memory cell in an array of a memory device (2d Wang

> Decl. ¶ 13), there is countering evidence in Amidi to demonstrate that isolating a cell relates to isolating a cell within multiple memory devices at the same time.

EX1011, 79-80.

54. The Board's May 31, 2016 Order also included new grounds of rejection for claims other than 16. *Id.*, 105. Following remand to the Examiner, Patent Owner amended certain claims, but did not amend claim 16. EX1010, 7279-80. The parties thereafter filed their respective appeals to the Board, and the Board again affirmed claim 16. EX1011, 152.

55. The parties filed their respective appeals to the U.S. Court of Appeals for the Federal Circuit, which affirmed the Board. *Google LLC v. Netlist, Inc.*, 810 F. App'x 902 (Fed. Cir. 2020).

56. I understand Petitioner asserts three grounds to challenge claim 16 of the '912 patent.

Ground	**Claim challenged**	**35 U.S.C. §**	**References**
1	16	103(a)	Perego
2	16	103(a)	Perego, Amidi
3	16	103(a)	Ellsberry

57. I provide my analysis below.

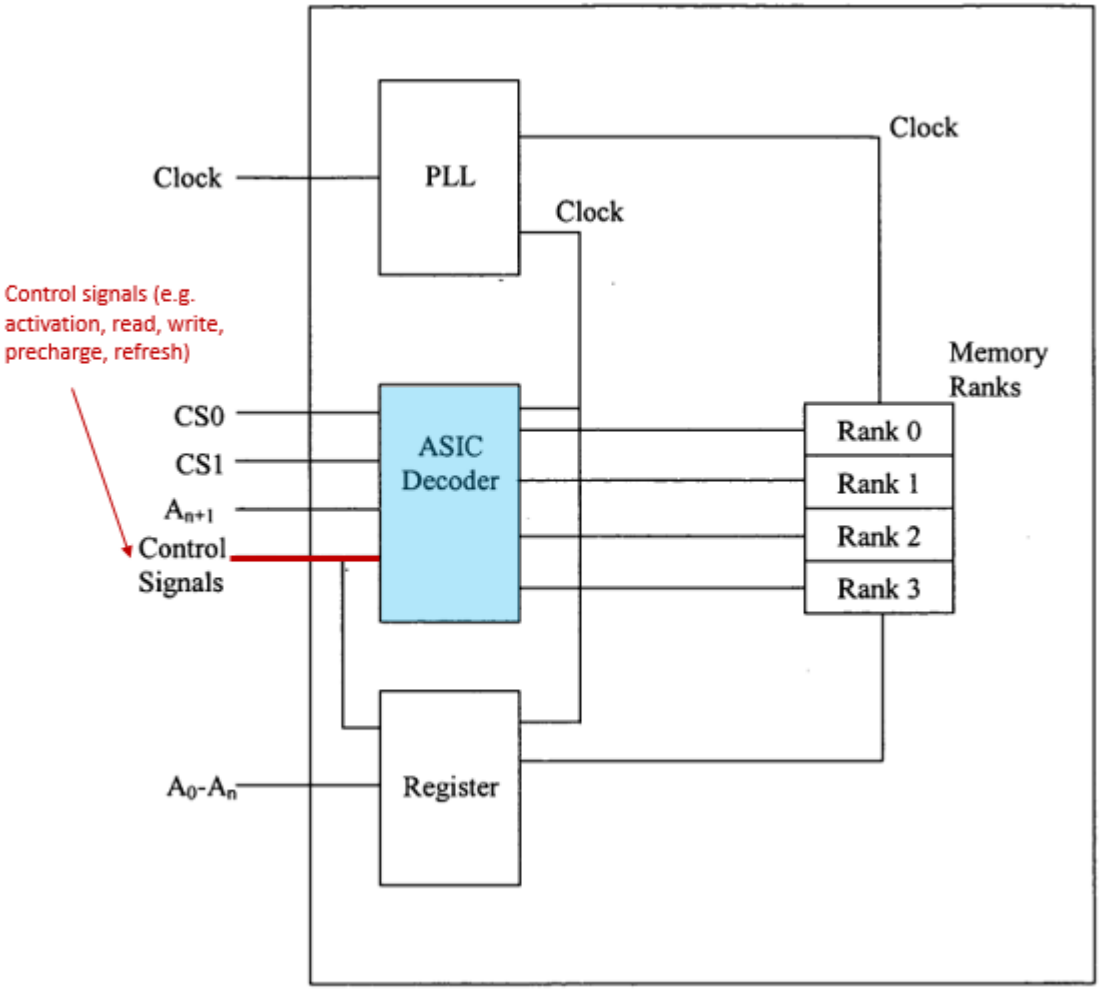
C. Priority Date of the ’912 Patent

58. The ’912 patent claims priority to three provisional applications: Nos. 60/588,244 (EX1005, the “’244 provisional”) filed on July 15, 2004, 60/550,668 (EX1006, the “’668 provisional”) filed on March 5, 2004, and 60/575,595 (EX1007, the “’595 provisional”) filed on May 28, 2004. EX1001. The ’912 patent also claims priority to application No. 11/173,175, filed July 1, 2005, now U.S. Patent No. 7,289,386 (the “’386 patent”) (EX1008), which is a continuation-in-part of application No. 11/075,395, filed March 7, 2005, now U.S. Patent No. 7,286,436 (the “’436 patent”) (EX1009). EX1001. I understand that in connection with Ground 3, Petitioner argues that Ellsberry (filed on June 1, 2005) is prior art to the ’912 patent because none of the three provisional applications and the ’436 patent provide sufficient disclosure to support certain claim elements. For the reasons that follow, I disagree.[3]

[3] For purposes of this declaration, I have been asked to only render an opinion on Petitioner’s arguments regarding the ’244 provisional and ’436 patent.

1. The ’244 Provisional (EX1005)

59. The ’244 provisional discloses a memory module comprising DRAM devices arranged in ranks and a memory module decoder that is configured to simulate a memory module with a smaller number of ranks (e.g., two logical ranks) than the module actually has (e.g., four physical ranks). EX1005, [0001]-[0002], [0005]-[0008], [0024]-[0025]. The decoder comprises an ASIC (blue) that “decodes two chip-select signals and one control signal (such as an address signal) and converts them into four chip-select signals.” *Id.*, [0005]. The decoder also receives certain control signals, e.g. command signals that “include, but are not limited to, activation read, write, precharge, and refresh.” *Id.*, [0019].



60. With respect to certain four-rank memory module embodiments, "the ASIC uses one additional address signal (A_{n+1}) and at least one control signal. Exemplary control signals compatible with embodiments described herein control functions including, but are not limited to, refresh, precharge, and other operations used for the proper functioning of the memory module." *Id.*

[0010]; *see also id.*, [0025] ("The decoder is configured to receive input signals comprising a first number of chip-select signals and at least one control signal and to convert the input signals into output signals, the output signals comprising a second number of chip-select signals and to pass the output signals to the first number of ranks, the second number of chip-select signals being greater than or equal to the first number of chip-select signals."); Figure 1 (reproduced above). Figure 1 also uses specific terminology indicating that the '244 memory module is a JEDEC-style memory module. For instance, Figure 1 depicts two chip-select signals CS0, and CS1. According to Petitioner's evidence, a "chip-select bus, is essential in a JEDEC-style memory system[.]" EX1034, p.2. Likewise, the figure use the term "rank." As Micron acknowledges, "[t]he term rank was created by JEDEC," EX2112, 1.

61. I agree with Petitioner that the "ASIC Decoder" of the '244 provisional corresponds to a "logic element." Pet. 63; EX1003, ¶189. However, I disagree with the Petitioner's characterization of the '244 provisional as containing "no disclosure [the ASIC Decoder] receives any 'bank address' signals." Pet. 63.

62. Specifically, a person of ordinary skill would understand, per the JEDEC DRAM standards of the day, that the "control signals" for certain memory operations—such as READ/WRITE—received by the decoder ASIC (blue) would necessarily include bank address signals. Under Petitioner's proposed level of skill in the art, a person of ordinary skill in the art at the time of the '912 patent "would have been knowledgeable about the JEDEC DDR (EX1030, EX1031) and DDR2 (EX1029, EX1039) SDRAM standards." Pet. 6.

63. According to the JEDEC standards, performing certain commands such as Bank Activation, Write, and Read necessarily requires bank address signals as part of the command code. For example, JESD79-2 provides that bank address inputs "BA0-BA2 define to which bank an Active, Read, Write or Precharge command is being applied." EX1029, 6 (reproduced below). The Command Truth Table of JESD79-2 also indicates that "Bank addresses BA0, BA1, BA2 (BA) determine which bank is to be operated on." *Id.*, 49 n.2 (reproduced below, both as-truncated in the Petition and in full). Likewise, JESD79 provides that "Bank Address Inputs: BA0 and BA1 define to which

bank an ACTIVE, Read, Write or PRECHARGE command is being applied."

EX1030, 7.

1.2 Input/Output Functional Description

Symbol	Type	Function
CK, $\overline{CK}$	Input	**Clock:** CK and $\overline{CK}$ are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of CK. Output (read) data is referenced to the crossings of CK and $\overline{CK}$ (both directions of crossing).
CKE	Input	**Clock Enable:** CKE HIGH activates, and CKE Low deactivates, internal clock signals and device input buffers and output drivers. Taking CKE Low provides Precharge Power-Down and Self Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is synchronous for power down entry and exit, and for self refresh entry. CKE is asynchronous for self refresh exit. CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK, $\overline{CK}$, ODT and CKE are disabled during power-down. Input buffers, excluding CKE, are disabled during self refresh.
$\overline{CS}$	Input	**Chip Select:** All commands are masked when $\overline{CS}$ is registered HIGH. $\overline{CS}$ provides for external Rank selection on systems with multiple Ranks. $\overline{CS}$ is considered part of the command code.
ODT	Input	On Die Termination: ODT (registered HIGH) enables termination resistance internal to the DDR2 SDRAM. When enabled, ODT is only applied to each DQ, DQS, $\overline{DQS}$, RDQS, $\overline{RDQS}$, and $\overline{DM}$ signal for x4x8 configurations. For x16 configuration ODT is applied to each DQ, UDQS/$\overline{UDQS}$, LDQS/$\overline{LDQS}$, $\overline{UDM}$, and $\overline{LDM}$ signal. The ODT pin will be ignored if the Extended Mode Register (EMRS) is programmed to disable ODT.
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	Input	**Command Inputs:** $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ (along with $\overline{CS}$) define the command being entered.
DM (UDM), (LDM)	Input	**Input Data Mask:** DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH coincident with that input data during a Write access. DM is sampled on both edges of DQS. Although DM pins are input only, the DM loading matches the DQ and DQS loading. For x8 device, the function of DM or RDQS/$\overline{RDQS}$ is enabled by EMRS command.
BA0 - BA2	Input	**Bank Address Inputs:** BA0 and BA1 for 256 and 512Mb, BA0 - BA2 define to which bank an Active, Read, Write or Precharge command is being applied. Bank address also determines if the mode register or extended mode register is to be accessed during a MRS or EMRS cycle.
A0 - A15	Input	**Address Inputs:** Provided the row address for Active commands and the column address and Auto Precharge bit for Read/Write commands to select one location out of the memory array in the respective bank. A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by BA0, BA1. The address inputs also provide the op-code during Mode Register Set commands.

(EX1029, 6)

Table 10 — Command truth table.

Function	CKE		$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA0 BA1 BA2	A15-A11	A10	A9 - A0	Notes
	Previous Cycle	Current Cycle									
Bank Activate	H	H	L	L	H	H	BA	Row Address			1,2
Write	H	H	L	H	L	L	BA	Column	L	Column	1,2,3,
Write with Auto Precharge	H	H	L	H	L	L	BA	Column	H	Column	1,2,3,
Read	H	H	L	H	L	H	BA	Column	L	Column	1,2,3
Read with Auto-Precharge	H	H	L	H	L	H	BA	Column	H	Column	1,2,3

NOTE 1 All DDR2 SDRAM commands are defined by states of $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and CKE at the rising edge of the clock.
NOTE 2 Bank addresses BA0, BA1, BA2 (BA) determine which bank is to be operated upon. For (E)MRS BA selects an (Extended) Mode Register.

Pet. 45-46 (truncated truth table of JESD 79-2, EX1029, 49)

Table 10 — Command truth table.

Function	CKE Previous Cycle	CKE Current Cycle	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA0 BA1 BA2	A15-A11	A10	A9 - A0	Notes
(Extended) Mode Register Set	H	H	L	L	L	L	BA	OP Code			1,2
Refresh (REF)	H	H	L	L	L	H	X	X	X	X	1
Self Refresh Entry	H	L	L	L	L	H	X	X	X	X	1
Self Refresh Exit	L	H	H	X	X	X	X	X	X	X	1,7
			L	H	H	H					
Single Bank Precharge	H	H	L	L	H	L	BA	X	L	X	1,2
Precharge all Banks	H	H	L	L	H	L	X	X	H	X	1
Bank Activate	H	H	L	L	H	H	BA	Row Address			1,2
Write	H	H	L	H	L	L	BA	Column	L	Column	1,2,3
Write with Auto Precharge	H	H	L	H	L	L	BA	Column	H	Column	1,2,3
Read	H	H	L	H	L	H	BA	Column	L	Column	1,2,3
Read with Auto-Precharge	H	H	L	H	L	H	BA	Column	H	Column	1,2,3
No Operation	H	X	L	H	H	H	X	X	X	X	1
Device Deselect	H	X	H	X	X	X	X	X	X	X	1
Power Down Entry	H	L	H	X	X	X	X	X	X	X	1,4
			L	H	H	H					
Power Down Exit	L	H	H	X	X	X	X	X	X	X	1,4
			L	H	H	H					

NOTE 1 All DDR2 SDRAM commands are defined by states of $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and CKE at the rising edge of the clock.

NOTE 2 Bank addresses BA0, BA1, BA2 (BA) determine which bank is to be operated upon. For (E)MRS BA selects an (Extended) Mode Register.

NOTE 3 Burst reads or writes at BL=4 cannot be terminated or interrupted. See sections "Reads interrupted by a Read" and "Writes interrupted by a Write" in section 2.2.4 for details.

NOTE 4 The Power Down Mode does not perform any refresh operations. The duration of Power Down is therefore limited by the refresh requirements outlined in section 2.2.7.

NOTE 5 The state of ODT does not affect the states described in this table. The ODT function is not available during Self Refresh. See section 2.2.2.4.

NOTE 6 "X" means "H or L (but a defined logic level)".

NOTE 7 Self refresh exit is asynchronous.

EX1029, 49 (complete truth table)

64. I note that this evidence is cited by the Petition itself. Pet. 44-49. In fact, citing to the command truth table of JESD79-2, Petitioner states that "to perform a read or write operation, the JEDEC standard … first requires ***a Bank Activate command with*** the row and ***bank address signals***, followed by ***a read or write command with the corresponding bank address signals***." Pet. 45-46 (citing EX1029, 49 n.2). The Petition also relies on the JEDEC standard to argue that Perego-422 discloses receiving "bank address signals" by a logic element. Pet. 36-37 ("A POSITA would have understood that, for DDR memory devices, the 'address lines' (and 'address information') labeled RQ in Perego … convey both row/column, and bank, addresses, per the JEDEC standard.") (citing EX1029 and EX1032).

65. Moreover, a POSITA would understand that the control signal would include bank address signals because the '244 provisional states that "two chip-select signal and one control signal (such as ***an address signal***)" can be used to generate four chip-select signals. EX1009, [0005]. As shown in EX1029, address bits suitable for differentiating between two 512Mb devices emulating a 1Gb device would be BA2. *See* EX1029, p.7. Thus, a POSITA

would recognize that the "address signal" mentioned in the '244 provisional, [0005] would include BA2 and that the inventors were in possession of the memory module of claim 16.

> **[0005]** In certain embodiments described herein, a memory module having a first number of ranks comprises a memory module decoder. The decoder of certain embodiments comprises an Application Specific Integrated Circuit ("ASIC") that decodes two chip-select signals and one control signal (such as an address signal) and converts them into four chip-select signals. The decoder of certain embodiments also decodes certain commands (such as refresh or precharge) that require all the ranks of memory to be active.

EX1009, [0005]

Table 2 — 512Mb Addressing

Configuration	128Mb x4	64Mb x 8	32Mb x16
# of Bank	4	4	4
Bank Address	BA0,BA1	BA0,BA1	BA0,BA1
Auto precharge	A10/AP	A10/AP	A10/AP
Row Address	A0 ~ A13	A0 ~ A13	A0 ~ A12
Column Address	A0 ~ A9,A11	A0 ~ A9	A0 ~ A9
Page size *1	1 KB	1 KB	2 KB

Table 3 — 1Gb Addressing

Configuration	256Mb x4	128Mb x 8	64Mb x16
# of Bank	8	8	8
Bank Address	BA0 ~ BA2	BA0 ~ BA2	BA0 ~ BA2
Auto precharge	A10/AP	A10/AP	A10/AP
Row Address	A0 ~ A13	A0 ~ A13	A0 ~ A12
Column Address	A0 ~ A9,A11	A0 ~ A9	A0 ~ A9
Page size *1	1 KB	1 KB	2 KB

EX1029, p. 7

66. Accordingly, a person of ordinary skill in the art would have understood that the '244 provisional disclosed a "logic element" receiving "bank

address signals" as such signals were part of the control signals received for read, write, and precharge. Thus, based on the '244 provisional's disclosure and the purported knowledge of a person of ordinary skill in the art (specifically, the above JEDEC standards), a person of ordinary skill in the art would have understood that the inventors were in possession of the concept that bank address signals were received by the logic element. *See supra*, ¶¶59-64.

67. I provide below a claim chart showing where the written description support for each element appears.

'912, claim 16	**Support in the '244 Provisional**
[16.pre] A memory module connectable to a computer system, the memory module comprising:	*See, e.g.*, • EX1005, [0001] ("Certain types of memory modules comprise a plurality of dynamic random-access memory (DRAM) devices mounted on a printed circuit board (PCB). ***These memory modules are typically mounted in a memory slot or socket of a computer system*** (e.g., a server system or a personal computer) ***and are accessed by the processor of the computer system***."). • *Id.*, [0004] ("During operation, the ranks of a memory module are selected or activated by rank-select signals, also called chip-select signals, ***that are received from the processor***."); *see also id.*, [0005]-[0010].

	• *Id.*, p. 10: Figure 1 also depicts a memory module connectable to a computer system that receives certain signals from the processor of a computer system. *See id.*, [0009].
[16.a] a printed circuit board;	*See, e.g.*, • *Id.*, [0001] ("Certain types of memory modules comprise a plurality of dynamic random-access memory (DRAM) devices mounted on ***a printed circuit board (PCB).***"). • *Id.*, [0023] ("In certain embodiments, a memory module comprises a printed circuit board (PCB) and a plurality of dynamic random-access memory (DRAM) devices mounted on the PCB."); *id.*, [0025]-[0026] (embodiments also describing a memory module comprising a PCB). • *Id.*, p. 10: A person of ordinary skill in the art would understand that the memory module illustrated in Figure 1 comprises a printed circuit board ("PCB").
[16.b] a plurality of double-data-rate (DDR) memory devices coupled to the printed circuit board,	*See, e.g.*, EX1005, [0023] ("In certain embodiments, a memory module comprises a printed circuit board (PCB) and a plurality of dynamic random-access memory (DRAM) devices mounted on the PCB."); *id.*, [0025]-[0026]. A person of ordinary skill in the art would understand that disclosure of "DRAM" around the

	time of the ’244 provisional application’s disclosure would have included double-data rate (“DDR”) DRAM. *See supra*, ¶19; EX2103 (Wolfe Tr.), at 72:7-14 (“Q. So in 2004 and 2005, when a person with ordinary skill in the art mentions a DRAM device, would others understand that the DRAM device they refer to would include DDR2 or DDR device? A. I think they would understand that it could include a DDR or DDR2 device, especially if they were in the context of a general purpose computer.”).
[16.b.i] the plurality of DDR memory devices having a first number of DDR memory devices arranged in a first number of ranks;	*See* evidence for [16.b]; *See also, e.g.*, • [0023] (“In certain embodiments, a memory module comprises a printed circuit board (PCB) and a plurality of dynamic random-access memory (DRAM) devices mounted on the PCB. ***The plurality of DRAM devices are arranged in a first number of ranks***.”); [0025]-[0026] (embodiments also describing a memory module with a plurality of DRAM device arranged in a “first number of ranks”). • *Id.*, p. 10: Figure 1 depicts “Memory Ranks” including “Rank 0,” “Rank 1,” “Rank 2,” and “Rank 3.”
[16.c] a circuit coupled to the printed circuit board, the circuit	*See generally* disclosure related to “decoder” and “register”, *e.g.*, • EX1005, [0005] (“In certain embodiments described herein, a memory module having

comprising a logic element and a register,	a first number of ranks comprises a memory module decoder. The decoder of certain embodiments comprises an Application Specific Integrated Circuit ('ASIC') . . . ."); [0006]-[0008]. • *Id.*, [0023] ("In certain embodiments, a memory module comprises a printed circuit board (PCB) and a plurality of dynamic random-access memory (DRAM) devices mounted on the PCB. . . . The memory module further comprises ***a decoder mounted on the PCB***."). • *Id.*, p. 10: Figure 1 illustrates a memory module including a "circuit" comprising a logic element ("ASIC decoder") and a register; [0009] ("Figure 1 schematically illustrates a memory module comprising one embodiment of the decoder as described herein. The phase-locked loop ('PLL') provides the clock signals to the ranks of memory, ***the register, and the ASIC decoder.***" … "The ***register*** buffers address signals (Ao-An) from **a processor (not shown)**").
[16.c.i] the logic element receiving a set of input signals from the computer system, the set of input signals comprising at least one row/column	The '244 Provisional provides support for a logic element (e.g., "ASIC Decoder") receiving, from the computer system, the claimed set of input signals. *See, e.g.*, EX1005, p. 10: Figure 1 illustrates a memory module including an ASIC Decoder which receives, from the computer system, at least one row/column address signal (A_{n+1}), bank address

address signal, bank address signals, and at least one chip-select signal,	signals ("Control Signals"), and at least one chip-select signal (CS0 or CS1). <u>"at least one row/column address signal"</u> • *Id.*, [0010] ("In certain embodiments in which the computer system supports four-rank memory modules, the ASIC uses one additional address signal (A_{n+1}) and at least one control signal."). • *Id.*, [0023] ("The decoder is configured to receive input signals comprising a first number of chip-select signals and at least one control signal."); *id.*, [0025] ("The decoder is configured to receive input signals comprising a first number of chip-select signals and at least one control signal"); *id.*, [0026] ("The decoder is configured either (i) to pass input signals comprising a first number of chip-select signals and at least one control signal to the first number of ranks."). • A person of ordinary skill in the art would understand that DDR2 devices, which would be understood as encompassed by the reference to "DRAM," would require column addresses for read/write operations and row addresses for bank activation, for example. *E.g.*, EX1042, p.29; EX2103 at 72:7-14 ("Q. So in 2004 and 2005, when a person with ordinary skill in the art mentions a DRAM device, would others understand that the DRAM device they refer to would include DDR2 or DDR device? A. I think they would understand

	that it could include a DDR or DDR2 device, especially if they were in the context of a general purpose computer.”). Thus, a person of ordinary skill in the art would understand that the inventors were in possession of the invention that includes “a set of input signals” that comprises “at least one row/column address signal.” <u>“at least one chip-select signal”</u> • *Id.*, [0005] (“In certain embodiments described herein, a memory module having a first number of ranks comprises a memory module decoder. The decoder of certain embodiments comprises an Application Specific Integrated Circuit (‘ASIC’) that decodes two chip-select signals and one control signal (such as an address signal) and converts them into four chip-select signals.”). • *Id.*, [0009] (“The ASIC uses the two chip-select signals (CS_0, CS_1) provided by the processor.”). • [0023], [0025]-[0026] (embodiments where decoder receives input signals comprising chip-select signals). <u>“bank address signals”</u> • [0001] (disclosing DRAM memory modules “mounted in a memory slot or socket of a computer system (e.g., a server system or a personal computer) and are accessed by the processor of the computer system.”). A POSITA would have

	understood that a DRAM device used in connection with personal computers would receive bank address signals for a read or write operation. *See* EX2103 (Wolfe Tr.), 73:9-15; 74:19-75:5; 78:1-8; 78:16-79:9 . Q. And you said that if the DRAM device was used in connection with a personal computer, then a person of ordinary skill in the art would understand that a DRAM device could be a DDR2 or DDR device, correct? A. That would be true in the 2000 to 2006 time frame. (EX2103, 73:9-73:15) Q. You are saying that it would be ordinary for a personal computer to send CAS bar, RAS bar, WE bar, chip select signals and bank address signals to the memory module for a read and write operation at the time of the invention; is that correct? A. Yes, I think that's fair. And then one would have to look at how those are then connected on the memory module to figure out whether or not that's at all relevant to these claims. Q. Is that something a person of ordinary skill in the art would understand? A. Yes. (EX2103, 74:19-75:5)

	Q. So in the 2005 and 2005 {sic} time period, a conventional PC system would send chip select signals, CAS bar, RAS bar, write enable bar, bank address signals to a DIMM for a read and write operation; is that correct? A. That would be typical. And, again, then it would depend on the implementation as to what the DIMM did with those signals. (*Id.*, 78:1-8) Q. Okay. And for bank activation, would those -- would those same signals be sent from a conventional PC system to a memory module in the 2004 and 2005 time period? A. Again, I don't know what you mean by signals being sent. They would be physically connected, but they could be -- some of those signals could be dormant in a bank -- in a bank activation. Q. What do you mean by some of the signals

	would be dormant? A. They may not be doing anything. There may not be any information being provided on some of those signals during a bank activate. Q. Okay. But those signals would be sent and received, just that they would not be used. Is that what you mean? A. From the perspective of the DIMM, I think that is -- that's -- that would be common. (*Id.*, 78:16-79:9) • Fig. 1 (depicting ASIC Decoder receiving "Control Signals"). • [0005] ("***The [ASIC] decoder*** of certain embodiments also ***decodes certain commands*** (such as refresh or precharge) ***that require all the ranks of memory to be active***."). A person of ordinary skill in the art would understand that the "Control Signals" referenced in Figure 1 would include bank address signals for commands like precharge, refresh, activate, read and write that are used to operate the memory modules. *See* Pet. at 45-46 (citing EX1029, 49 n.2 ("Bank addresses BA0, BA1, BA2 (BA) determine which bank is to be operated on.").); *see also* EX1030, 7 ("Bank Address Inputs: BA0 and BA1 define to which bank an ACTIVE, Read, Write or PRECHARGE command is being applied.").

	• [0009] (the memory module of Fig. 1 is described as having an ASIC Decoder receiving "two chip-select signals (CS0, CS1) provided by the processor" and a register receiving "address signals (A_0-A_n) provided by the processor"). • [0010] ("In certain embodiments in which the computer system supports four-rank memory modules, the ASIC uses one additional address signal (A_{n+1}) and at least one control signal. ***Exemplary control signals compatible with embodiments described herein control functions including, but are not limited to, refresh, precharge, and other operations used for the proper functioning of the memory module***.") • [0011] ("Table 1 provides a logic table for the selection of ranks of memory", and Table 1 illustrates input and output signals of the ASIC decoder, including "**Control Signals,**" which "involves a number of control signals that define operations such as refresh, precharge, and other operations.");

Table 1:

Input signals to ASIC Decoder

Four Output Signals From ASIC Decoder, one for each of the 4-Ranks

State	CS0	CS1	A_{n+1}	Control	RS0	RS1	RS2	RS3
1	0	1	0	Active	0	1	1	1
2	0	1	1	Active	1	0	1	1
3	0	1	x	Active	0	0	1	1
4	1	0	0	Active	1	1	0	1
5	1	0	1	Active	1	1	1	0
6	1	0	x	Active	1	1	0	0
7	1	1	x	x	1	1	1	1

Note:

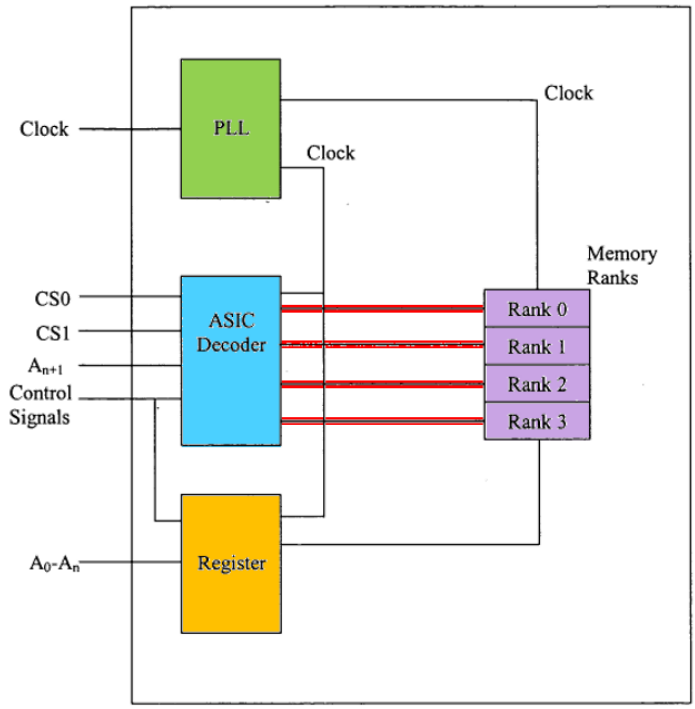
1. CS0, CS1, RS0, RS1, RS2, and RS3 are active low signals.
2. A_{n+1} is an active high signal.
3. 'x' is a Don't Care condition.
4. Control involves a number of control signals that define operations such as refresh, precharge, and other operations.

- [0019] ("The ***'Control'*** column of Table 1 ***represents the various commands that a DRAM device can execute***, examples of which include, but are not limited to, activation, read, write, precharge, and refresh."). A person of ordinary skill in the art would understand that, per the JEDEC DDR specification, certain commands include bank address signals that are part of the command code. *See* Pet. at 45-46 (citing EX1029, 49 n.2 ("Bank addresses BA0, BA1, BA2 (BA) determine which bank is to be operated on.").); *see also* EX1030, 7 ("Bank Address Inputs: BA0 and BA1 define to which bank an ACTIVE, Read, Write or PRECHARGE command is being applied.").

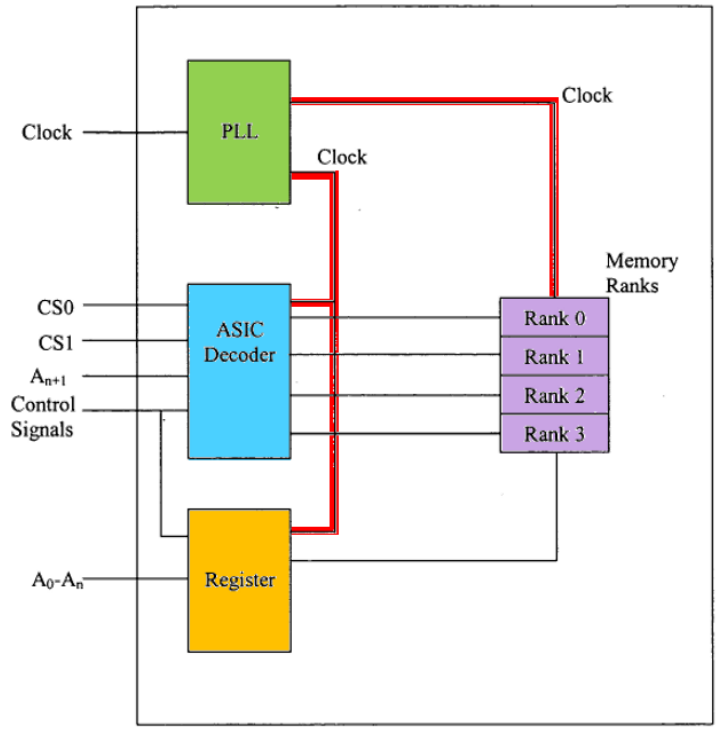
  Note [0019] discloses, for example, that in State (4), a Read command is listed for "Control" and only one of the 4 ranks is selected. In contrast, in State (6), where A_{n+1} is "don't care" (which means its value does not affect the logic function performed by the ASIC decoder), the

	inventor defines, for example, a refresh command for "Control" in State 6 where two ranks of the 4 ranks are selected. As is clear from Table 1, gated CS (RS#) depends on not just A_{n+1}, but also other command signals.
[16.c.ii] the set of input signals configured to control a second number of DDR memory devices arranged in a second number of ranks, the second number of DDR memory devices smaller than the first number of DDR memory devices and the second number of ranks less than the first number of ranks,	*See* evidence cited for [16.c.i]. *See also, e.g.*, • EX1005, [0023] ("In certain embodiments, a memory module comprises a printed circuit board (PCB) and a plurality of dynamic random-access memory (DRAM) devices mounted on the PCB. The plurality of DRAM devices are arranged in a first number of ranks. The memory module further comprises a decoder mounted on the PCB. The decoder is configured to receive input signals comprising a first number of chip-select signals and at least one control signal. ***The decoder is further configured to convert the input signals to output signals comprising a second number of chip-select signals***."); [0024]. • *Id.*, [0025] ("The decoder is configured to receive input signals comprising a first number of chip-select signals and at least one control signal and to convert the input signals into output signals, the output signals comprising a second number of chip-select signals and to pass the output

	signals to the first number of ranks, the second number of chip-select signals being greater than or equal to the first number of chip-select signals. In certain such embodiments, the memory module is configured to operate as (i) a memory module having the first number of ranks or (ii) ***a memory, module having a second number of ranks which is less than the first number of ranks***."); [0026].
[16.c.iii] the circuit generating a set of output signals in response to the set of input signals, the set of output signals configured to control the first number of DDR memory devices arranged in the first number of ranks,	*See* evidence cited for [16.c.i] – [16.c.ii]. *See also, e.g.*, EX1005, p. 10: Figure 1 depicts the circuit (ASIC Decoder + Register) receiving, as input, a set of input signals, and outputting signals to "Memory Ranks" Rank 0 – Rank 3.

	Figure 1: 
[16.c.iv] wherein the circuit further responds to a command signal and the set of input signals from the computer system by selecting one or two ranks of the first number of ranks and transmitting the command signal to at least one DDR	*See* evidence cited for [16.b], [16.c.ii]-[16.c.iii]. *See also, e.g.*, • EX1005, [0011] ("Table 1 provides a logic table for the selection of the ranks of memory compatible with embodiments described herein."); *see also id.* at [0012]-[0017] (description of various logical states in Table 1); and specifically, two ranks are selected in State# (6) where an example refresh command is transmitted to the two ranks that are selected by RS2 and RS3, while in State# (4) an example read command is sent only to the one rank that

<table>
<tr><td>memory device of the selected one or two ranks of the first number of ranks; and</td><td>is selected by RS2, [0019].
Table 1:
<table><tr><th>State</th><th>CS0</th><th>CS1</th><th>A_{n+1}</th><th>Control</th><th>RS0</th><th>RS1</th><th>RS2</th><th>RS3</th></tr><tr><td>1</td><td>0</td><td>1</td><td>0</td><td>Active</td><td>0</td><td>1</td><td>1</td><td>1</td></tr><tr><td>2</td><td>0</td><td>1</td><td>1</td><td>Active</td><td>1</td><td>0</td><td>1</td><td>1</td></tr><tr><td>3</td><td>0</td><td>1</td><td>x</td><td>Active</td><td>0</td><td>0</td><td>1</td><td>1</td></tr><tr><td>4</td><td>1</td><td>0</td><td>0</td><td>Active</td><td>1</td><td>1</td><td>0</td><td>1</td></tr><tr><td>5</td><td>1</td><td>0</td><td>1</td><td>Active</td><td>1</td><td>1</td><td>1</td><td>0</td></tr><tr><td>6</td><td>1</td><td>0</td><td>x</td><td>Active</td><td>1</td><td>1</td><td>0</td><td>0</td></tr><tr><td>7</td><td>1</td><td>1</td><td>x</td><td>x</td><td>1</td><td>1</td><td>1</td><td>1</td></tr></table></td></tr>
<tr><td>[16.d] a phase-lock loop device coupled to the printed circuit board,</td><td>See infra, evidence cited for [16.d.i].</td></tr>
<tr><td>[16.d.i] the phase-lock loop device operatively coupled to the plurality of DDR memory devices, the logic element, and the register,</td><td>Figure 1 depicts the PLL transmits a clock signal a plurality of memory devices (“Memory Ranks”), a logic element (“ASIC Decoder), and the register (“Register”).</td></tr>
</table>

	Figure 1:  A person of ordinary skill in the art would understand that the PLL is "operatively coupled" to each of these components because the PLL is coupled to each of these components, and each of these components requires a clock signal to operate. *See* EX1005, [0009] ("The phase-locked loop ("PLL") ***provides <u>the</u> clock signals to the ranks of memory, the register, and the ASIC decoder.***").
[16.e] wherein the command signal is transmitted to only one DDR memory device at a time.	*See, e.g.*, [0019]: The "Control" column of Table 1 represents the various commands that a DRAM device can execute, examples of which include, but are not limited to,

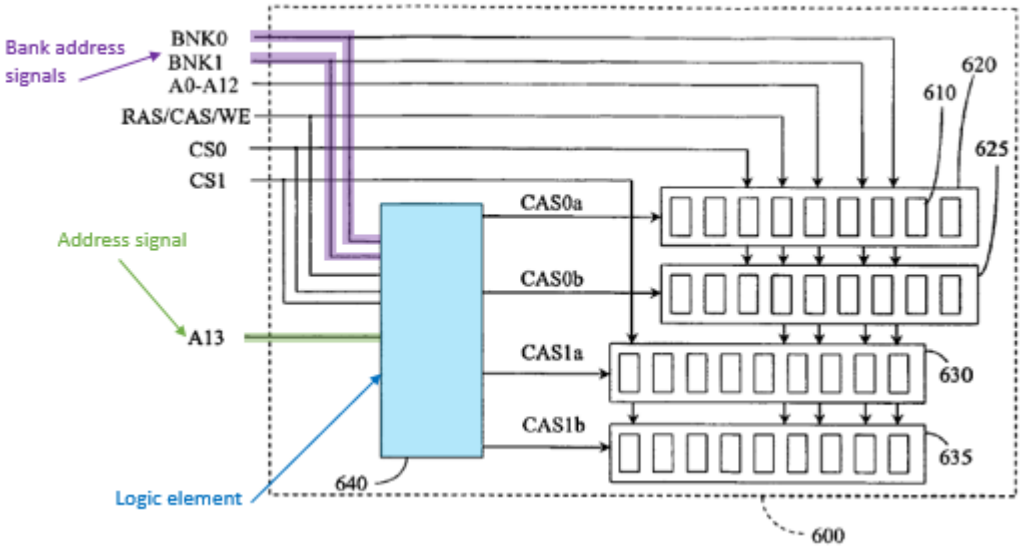
	activation, read, write, precharge, and refresh. In certain embodiments, the control command is passed through to the selected rank only (e.g., state 4 of Table 1). ***In such embodiments, the control command (e.g., read) is sent to only one DRAM device or the other DRAM device so that data is supplied from one device at a time.*** In other embodiments, the control command is passed through to both associated ranks (e.g., state 6 of Table 1). In such embodiments, the control command (e.g., refresh) is sent to both DRAM devices to ensure that the memory content of the devices remains valid over time. Certain embodiments utilize a logic table such as that of Table 1 to simulate a single DRAM device from two DRAM devices by selecting two ranks concurrently.

2. The ’436 Patent (EX1009)

68. The ’436 patent discloses increasing the memory capacity or memory density of a memory module by implementing a logic element that performs operations on certain input signals. EX1009, 3:5-38; 17:30-18:11. Figure 11A illustrates an embodiment featuring a four-rank memory module with a logic element 640 (blue) which receives a first set of address and control

signals, including at least bank address signals BNK0 and BNK1, address signal A13, and command signals such as RAS/CAS/WE, CS0 and CS1 (chip select 0 and 1). The '436 patent explains that "[t]o access the additional memory density of the high-density memory module 600, the two chip-select signals (CS0, CS1) are used with other address and control signals to gate a set of four gated CAS signals." *Id.*, 17:31-34; *see also id.*, 17:34-39 ("For example, to access the additional ranks of four-rank 1-GB 128M 8-byte DDR1 DRAM memory module, the CS0 and CS1 signals along with the other address and control signals are used to gate the CAS signal appropriately, as schematically illustrated by FIG. 11A.").

FIGURE 11A



69. As depicted in Figure 11A above, the logic element (blue) "receives a first set of address and control signals," including bank address signals (BNK0-1, purple), address signal A13, and chip-select signals CS0-CS1, and "translates the first set of address and control signals into a second set of address and control signals which is compatible with the first plurality of memory locations of the memory module 600 and which is transmitted to the first rank 620, the second rank 625, the third rank 630, and the fourth rank 635." *Id.*, 16:57-17:10. The '436 patent further explains that, in certain embodiments, the logic element comprises a programmable logic device "PLD," where "the PLD uses sequential and combinatorial logic procedures to produce the gated CAS signals," each transmitted to one of the corresponding four ranks, or in other embodiments, "the PLD 642 instead uses sequential and combinatorial logic procedures to produce four gated chip-select signals (e.g., CS0a, CS0b, CS1a, and CS1b)," each transmitted to one of the corresponding four ranks. *Id.*, 17:41-43, 18:3-11. The '436 patent expressly provides that the PLD can "comprise[] an ASIC, an FPGA, a custom-designed semiconductor device, or a CPLD." *Id.*, 17:46-48; *see also id.*, 16:6-15 (similar disclosure for embodiment depicted in Figures 10A-10B).

Specific examples of PLDs include those made by Altera or Xilinx. *Id.*, 17:48-52. In addition to the embodiment in Figures 11A-11B, the '436 patent also illustrates a similar embodiment in Figures 10A-10B. *Id.*, 14:66-16:56.

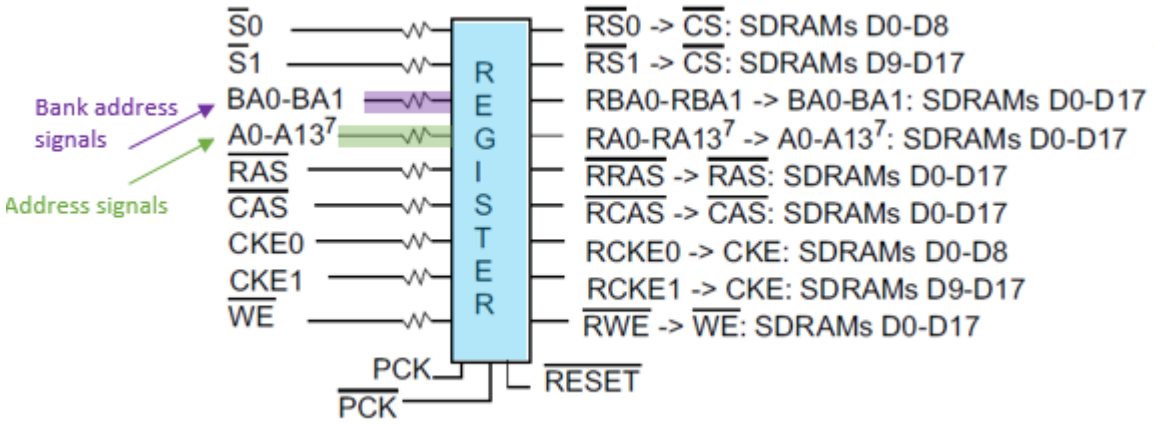
70. I understand Petitioner makes three arguments regarding the adequacy of the '436 patent's disclosure. I address each in turn.

a) Alleged Absence of the "Circuit"

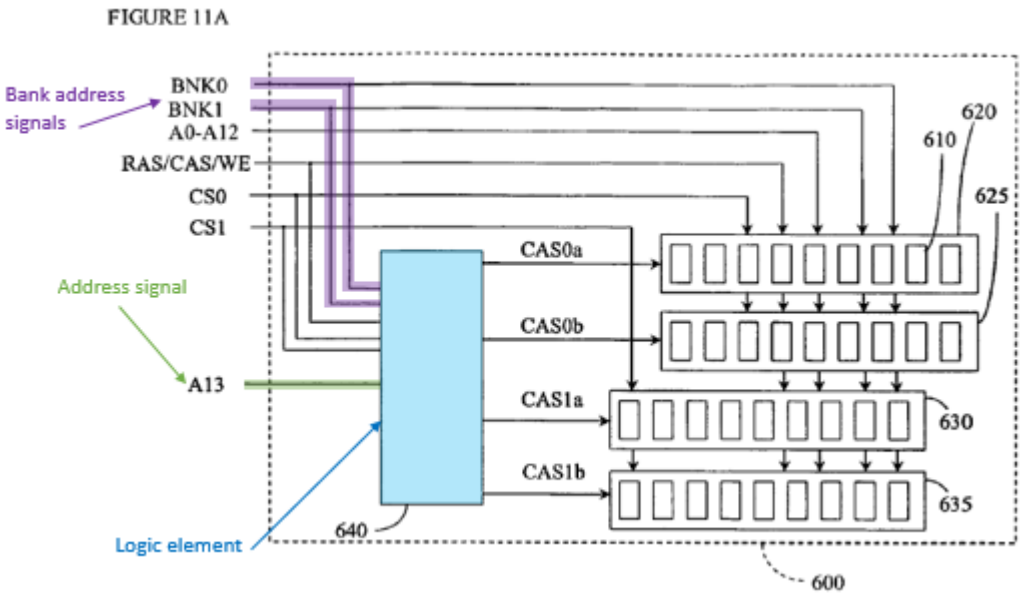
71. Petitioner's first argument is that the '436 patent "lack[s] any embodiment including 'a circuit' comprising 'a logic element' and 'a register' as ... shown in Figure 1A of the 912 Patent." Pet. 64. I disagree for the reasons that follow.

72. The '436 patent expressly discloses embodiments featuring registered DIMMs, which are necessarily understood to be memory modules with a register between a computer system's memory controller and the DRAM devices on the module. EX1009, 7:22-28 ("[M]emory modules 100 compatible with embodiments described herein include, but are not limited to, ... registered DIMMs (RDIMMs)."). The JEDEC design specification for DDR RDIMMs, JEDEC No. 21C, which Samsung alleges to be part of the knowledge possessed

by a person of ordinary skill in the art, schematically depicts a register, for example, for a x72 RDIMM. *See, e.g.*, EX1032, 4.20.4-10 to 4.20.4-16 (example below).



(EX1032, 4.20.4-12)



(EX1009, Fig. 11A)

73. I note that several of the signals entering the "REGISTER" function block above are also depicted as entering logic element 640 in Figure 11A of the '436 patent, including two bank address signals (BA0, BA1 in the figure from JEDEC No. 21C, BNK0, BNK1 in Figure 11A from the '436 patent), address signal A13, and two chip-select signals (S0/S1 in the figure from JEDEC No. 21C, CS0 and CS1 in Figure 11A from the '436 patent), indicating that the "register" and "logic element" are part of the same component illustrated in the "REGISTER" function block in JEDEC No. 21C.

74. Moreover, a person of ordinary skill in the art would understand the "REGISTER" function block in an RDIMM would include both logic elements for data processing and a register for storing data bits because (1) translating the input bits to output registered bits would involve the use of logic elements to process the input bits; and (2) the description of the functional block as a "register" would indicate to a person of ordinary skill in the art that the block included register functionality. I also understand that during reexamination, the Board also found that "registers [for an RDIMM] perform some type of logic function or comprise a logic circuit." EX1011, 19.

75. The exemplary logic elements disclosed by the '436 patent include various PLDs such as ASICs, FPGAs, and CPLDs. EX1009, 16:12-20, 17:46-52. A person of ordinary skill in the art would have understood that integrated devices such as ASICs, FPGAs, and CPLDs include both logic elements (*e.g.*, for performing logical operations) and registers (*e.g.*, for storing, buffering, and/or transmitting signals). This is consistent with the Board's findings in the '912 reexamination, in which, in referring to identical disclosure in the '912 patent during reexamination, the Board observed that "the expansive examples

in the ’912 patent of a logic element cover custom devices or a device of various discrete electrical components, which includes at least some types of registers.” EX1011, 19; *see also id.*, 17 (“The ’912 patent states that logic element 40 in certain embodiments can be a PLD, an ... (ASIC), ... (FPGA), or a ... (CPLD).”). Moreover, the ’436 patent specifically mentions Xilinx PLDs as an example of the claimed logic element. EX1009, 16:16-20, 17:48-50. One example of a Xilinx PLD suitable for memory applications is the Xilinx FPGA depicted below, which features a logic elements and a register:

XILINX SOLUTIONS

FIGURE 2-4: SPARTAN-3 FEATURES

The Spartan-3 FPGA memory architecture provides the optimal granularity and efficient area utilization.

Shift register SRL16 blocks

- Each CLB LUT works as a 16-bit fast, compact shift register
- Cascade LUTs to build longer shift registers
- Implement pipeline registers and buffers for video or wireless

EX2031, 27.

76. Likewise, with respect to certain embodiments shown in Figures 10A-10B, the ’436 patent expressly discloses a “logic element 540” that includes a programmable-logic device PLD 542. The PLD 542 would “save[] or latch[] the A13 address” during a row access for use as “an extra column address” in the subsequent column access. EX1009, 16:27-45. A person of ordinary skill in the art would have necessarily understood that the PLD includes registers to latch the received address signal A13, and thus that the logic element 540 includes both the logic element and the “register” element for storing extra address bits.

77. Furthermore, the ’436 patent teaches that “the logic element [circuit] 640 comprises a programmable-logic device (PLD) 642” among other elements. EX1001, 17:41-45. The ’436 patent teaches that the PLD 642 in the circuit 640 “uses ***sequential and combinatorial logic*** procedures” to produce gated CAS signals or gated chip-select signals for each of the four ranks. *Id.*, 18:3-11.

78. A person of ordinary skill in the art would understand that sequential logic would include both a logic element to perform the logic function

and a storage or register component to store parameters related to state machines. I understand that Dr. Wolfe agrees with me on this point. For example, Dr. Wolfe testified that ***sequential logic "describes a combination of logic functions and registers"*** because "sequential logic implements what we call state machines, which are time-variant logic functions that can perform different logic equations at different points in time based on the storage of what we call state register values." EX2103, 117:16-118:6. He further testified that, to implement sequential logic, one "would need both state storage in the form of a register or an equivalent, plus some what we call combinational logic functions." *Id.*, 118:7-24. Dr. Wolfe testified that both the register and the logic functions "would somehow be present" for sequential logic. *Id.*; *see also* 118:2-13 (combinatorial logic is logic that does not store results). And that is something a POSITA would have understood in 2004-2005. *Id.*, 119:14-18.

79. Thus, as I have stated earlier, a person of ordinary skill in the art would understand that, although the '912 patent describes 640 as a "logic element," element 640 is also an example of a recited "circuit," which has a PLD 642 that includes both a logic element to perform the logic functions (sequential

and combinatorial logic) and a register to store the "state register values" for the sequential logic. EX2103, 117:16-119:18; EX1009, 17:41-45, 18:3-11.

80. That is, a person of ordinary skill in the art would have understood that the '436 discloses a circuit comprising a logic element and a register.

b) Alleged Absence of Using "Row" and/or "Bank Address" Signals

81. Petitioner's second argument is that the '436 "lack[s] any Verilog code showing the use of 'row' and/or 'bank address signals'" such as Examples 1 and 2 of the '912 patent. Pet. 64; EX1003, ¶190 (Dr. Wolfe asserting that the '436 patent lacks "any Verilog code showing the use of the row address and/or bank address signals for rank multiplication"). I disagree for the reasons that follow.

82. I note that claim 16 only requires "the circuit generating a set of output signals ***in response*** to the set of input signals" that include row and bank address signals. This is disclosed, for example, in Figures 11A-11B of the '436 patent, which shows four gated CAS signals generated in response to the set of input signals that include both row address signal A13 and bank address signals BNK0/1. *See also* EX1009, Fig. 10B (logic element 540 outputting rank

selection signals in response to input signals that include bank address signals and row address signal A13).

83. The'436 patent explains that "[t]o access the additional memory density of the high-density memory module 600, the two chip-select signals (CS0, CS1) ***are used with other address and control signals*** to gate a set of four CAS signals." EX1009, 17:30-34. "For example, to access the additional ranks of four-rank 1-GB 128M 8-byte DDR1 DRAM memory module, the CS0 and CS1 signals along with the other address and control signals are used to gate the CAS signal appropriately, as schematically illustrated by FIG. 11A." *Id.*, 17:34-39. Additionally, instead of gated CAS signals, "[i]n certain other embodiments, the PLD 642 … uses sequential and combinatorial logic procedures to produce four gated chip-select signals (e.g., CS0a, CS0b, CS1a, and CS1b) which are each transmitted to a corresponding one of the four ranks 620, 625, 630, 635." EX1009, 18:6-11.

FIGURE 11A

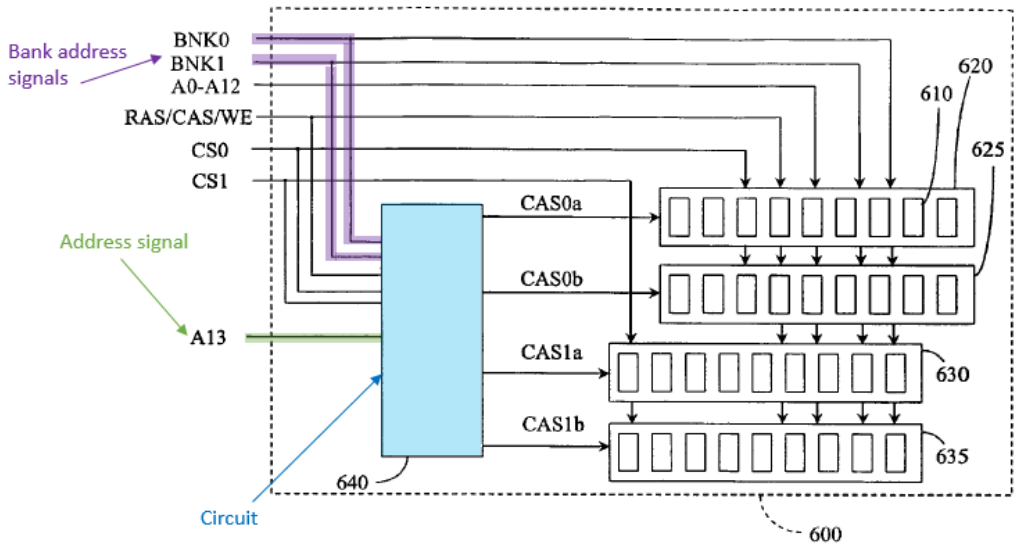
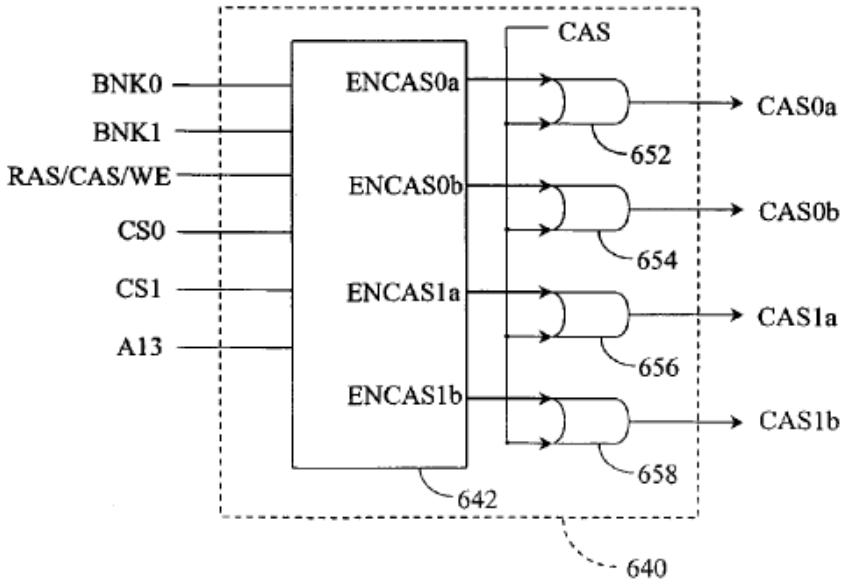


FIGURE 11B



84. As seen in the annotated figure above, the logic element (blue) receives both address signal (A13) and bank address signals (BNK0-1), and in response to A13, BNK0-1, as well as signals CS0, CS1, RAS/CAS/WE, the logic element outputs four gated CAS signals. *Id.*, 17:31-34 ("To access the additional memory density of the high-density memory module 600, the two chi-select signals … are ***used with other address and control signals*** to gate a set of four gated CAS signals"), 18:6-11 (instead of gated CAS signals, "[i]n certain other embodiments, the PLD 642 … uses sequential and combinatorial logic procedures to produce four gated chip-select signals (e.g., CS0a, CS0b, CS1a, and CS1b) which are each transmitted to a corresponding one of the four ranks 620, 625, 630, 635."); Fig. 11A; EX1029, 49 ("All DDR2 SDRAM commands are defined by states of CS, RAS, CAS, WE and CKE at the rising edge of the clock."). Thus, a person of ordinary skill in the art would necessarily understand from Figure 11A that the "other address … signals" used by the '436 patent to "gate a set of four CAS signals" or generate four chip-select signals include the row address A13 and the bank addresses BNK0 and BNK1. EX1009, 17:31-34, 18:6-9.

85. Additionally, as previously discussed, a person of ordinary skill in the art would know that a bank address signal (e.g. BNK0 or BNK1) would be used, for example, to select the targeted memory bank for a command, per the DDR standards. EX1009, 12:48-52 ("'JEDEC standard JESD79D, [DDR] SDRAM Specification," … [is] incorporated in its entirety by reference herein"); EX1029, 6 ("BA0 - BA2 define to which bank an Active, Read, Write or Precharge command is being applied."), 49 (Command truth table, and Note 2: "Bank addresses BA0, BA1, BA2 (BA) determine which bank is to be operated upon"); *supra*, ¶¶59-64.

86. As the Board previously found, a POSITA "would have reasonably concluded that the signals that enter logic element [] have some purpose and affect the output signals." EX1011, 88. Thus, based on the disclosures and associated figures, a person of ordinary skill in the art would understand that the inventors were in possession of the invention that includes the element of a circuit "generating a set of output signals in response to the set of inputs signals" that include "at least one row/column address signal, bank address signals and at least one chip-select signals").

87. I also note that Petitioner asserts in the Petition that Perego-422 inherently discloses a logic element that receives a row address and bank address signals per the JEDEC standard. Pet. 36-37; Pet. 45-46 ("[T]o perform a read or write operation, the JEDEC standard (shown below) first requires a Bank Activate command with the row and bank address signals, followed by a read or write command with the corresponding bank address signals…. Thus, a person of ordinary skill in the art would have understood that the target memory device and its target memory bank ***is selected in accordance with the bank address signals*** of the read or write command and ***the previously received row address and bank address signals*** of the activate command."). Under the same logic that Petitioner has applied, a person of ordinary skill in the art would have understood that the '436 discloses a circuit using a row and bank address signal.

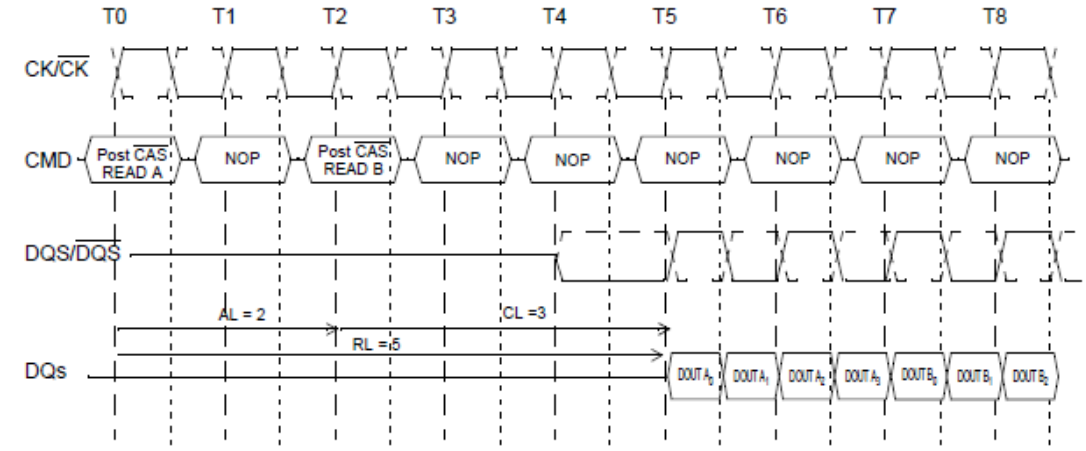
c) Alleged Non-Enablement of the '436 Invention

88. Petitioner's third argument is that the '436 patent fails to disclose any solution to the problem of executing a "standard" back-to-back read command which cross memory device boundaries ("BBARX"), and thus the disclosure of the '436 patent does not adequately support claim 16. Pet. 65-68.

Petitioner contends that material added in the July 1, 2005 application that issued as the ’386 patent is necessary to support claim 16. *Id.*, 66. As the ’386 patent explains, a BBARX (*i.e.*, across memory device “a” in Rank0 and memory device “b” in Rank1) may result in collisions when “the last data strobe of memory device ‘a’ collides with the pre-amble time interval of the data strobe of memory device ‘b.’” EX1008, 24:16-30. One solution to this problem is to “insert wait time intervals or clock cycles to avoid collisions or interference between [BBARX],” but in the context of rank multiplication, the memory controller is unaware of the physical boundaries of the memory devices on a rank. *Id.*, 24:15-30.

89. As an initial matter, Petitioner cites to various commands that were a part of the JEDEC standards of the day to argue that BBARX were “part of the normal operation of memory modules at the time.” Pet. 66. Petitioner cites to the “seamless burst read operation” for DDR2 memories (EX1029, Fig. 27), as one such example. *Id.* JESD 79-2 explains that a “[b]urst mode operation is used to provide a constant flow of data to memory locations (write cycle), or from memory locations (read cycle).” EX1029, 25. As illustrated below, in a

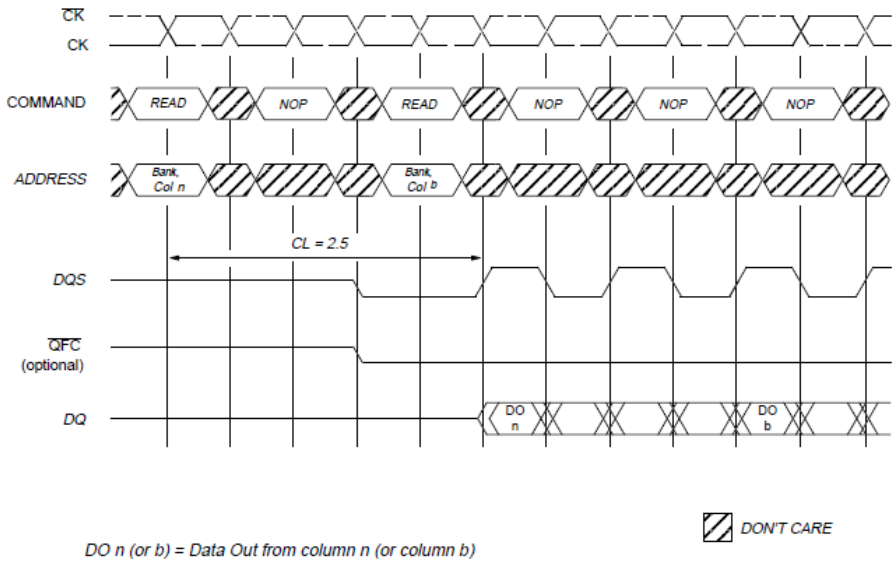
seamless burst operation, the memory controller issues two read commands (Read A, Read B) at T0 and T2, separated by a NOP, which is followed by four-bit bursts of data starting at T5. *Id.*, 28. However, the timing issues that arise in the context of successive read bursts are different from a BBARX because there is only a single DQS preamble for the same read operation by the same memory device and there is no DQS collision window. This is because the seamless burst command is bursting data to/from a single memory device via separate burst commands, via a single set of DQ and DQS lines whose signaling does not overlap simultaneously in time. In other words, the resultant DQ and DQS signaling for each of the READ A and READ B commands, as illustrated in the figure below, do not occur at the same point in time which could result in a collision.



The seamless burst read operation is supported by enabling a read command at every other clock for BL = 4 operation, and every 4 clock for BL = 8 operation. This operation is allowed regardless of same or different banks as long as the banks are activated.

Figure 27 — Seamless Burst Read Operation: RL = 5, AL = 2, and CL = 3, BL = 4

90. Nor do the DDR standards Petitioner cite feature BBARX. Petitioner's Figure 8 shows successive read commands to different columns *within* the same memory device, as confirmed by the description "Read commands shown must be to ***the same device***." EX1030, 19 (Figure 8, reproduced below).



DO n (or b) = Data Out from column n (or column b)
Burst Length = 4 or 8 (if 4, the bursts are concatenated; if 8, the second burst interrupts the first)
3 subsequent elements of Data Out appear in the programmed order following DO n
3 (or 7) subsequent elements of Data Out appear in the programmed order following DO b
Shown with nominal tDQSCK, and tDQSQ
Read commands shown must be to the same device

Figure 8
CONSECUTIVE READ BURSTS – REQUIRED CAS LATENCIES

91. Even if it was necessary for a memory system designer to find a solution to the BBARX issue, based on the ’436 patent disclosure and knowledge of the art, such a designer could overcome the supposed challenge of executing BBARX on a rank-multiplied module without undue experimentation. For example, a person of ordinary skill in the art could readily configure the memory controller in a memory system featuring the ’436 module to use appropriate timing sequences to avoid such collisions by inserting a delay between successive read commands, without the need to know the physical boundaries of

the memory devices. The memory designer could also use a serial presence detect (SPD) device to inform the memory controller of the physical boundaries of each memory device. A SPD device "store[s] the configuration information of the memory module on a read-only memory device whose content can be retrieved by the memory controller as part of the system initialization process," which allows the memory controller to "obtain the configuration and timing parameters required to optimally access data from DRAM devices on the memory module." EX1033, 421. By configuring a SPD device to inform the memory controller of the physical boundaries of the memory module, a person of ordinary skill in the art could insert delays where appropriate to avoid BBARX collisions.

92. Samsung's non-enablement argument also fails to take into consideration the priority document incorporated in the '436 patent. For example, the '436 patent claims priority to and incorporates by reference, among others, U.S. Provisional Application 60/550,668. EX1009, 1:7-12. The '668 Application (EX1006) addresses the DQS bus conflict issue caused by tying

DQS pins of two devices together. EX2103, 127:5-128:16, 129:18-130:5; EX1006, [0008]-[0009], [0014]-[0015].

93. This results in the same bus conflict problem referenced on page 65 of the Petition and pages 89-90 of EX1043, that is, when one pin is driven high and the other connected pin is driven low at the same time. The '668 Application teaches that this problem could be solved via current-limiting resistors using schemes shown in Figures 3-4. EX1006, [0016]-[0017]. Dr. Wolfe agrees that the solution would address the issues related to damage to the drivers (i.e., "potentially destroy[ing] the drivers in the memory devices" mentioned on Pet. 65). EX2103, 128:17-129:17, 130:22-24 ("1006 mitigates the physical damage issues"); *see also* EX1006, Figs 3-4 (in even the worst case scenarios, the current through DRAM drivers is 34mA, less than the 50mA short-circuit current specified on p.12).

94. I understand that Dr. Wolfe disputes that the solution would address the signal error problem, *i.e.*, "whether the proper voltage level is provided at the right time in order for you to have the right alignment between the DQS and DQ." EX2103, 129:11-17, 130:6-131:8. Dr. Wolfe appears to be concerned

that the voltage level might not correctly reflect the voltage needed for logic 1 and logic 0 at the right time. *Id.*

95. But the specific solution of the ’668 Application addresses this signal error issue as well. For instance, as shown in ’668 Figure 4, a resistor divider network is used such that the combined DQS signal voltage level is at the mid-point of VDD (2.7V) and ground (0V), matching the voltage level of VTT (*see* table below). EX1005, p.13.

DC OPERATING CONDITIONS AND CHARACTERISTICS

Parameter	Symbol	Min		Max		Unit	Note
		D27J	D32K	D27J	D32K		
Supply Voltage	VDD	2.3	2.5	2.7	2.7	V	
I/O Supply Voltage	VDDQ	2.3	2.5	2.7	2.7	V	
I/O Reference Voltage	VREF	0.49*VDD		0.51*VDD		V	1
I/O Termination voltage(system)	VTT	VREF-0.04		VREF+0.04		V	2

96. This means the combined DQS signal voltage level would transition in the same way as would normally be driven by a DRAM DQS driver to overcome the termination voltage V_{TT}, as shown in EX1006, Fig. 3 and annotated Fig. 4 below.

Figure 3:

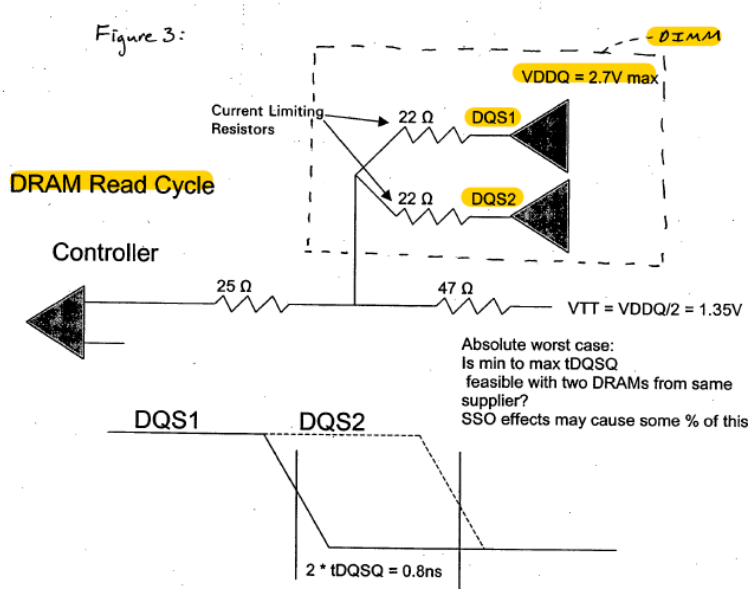
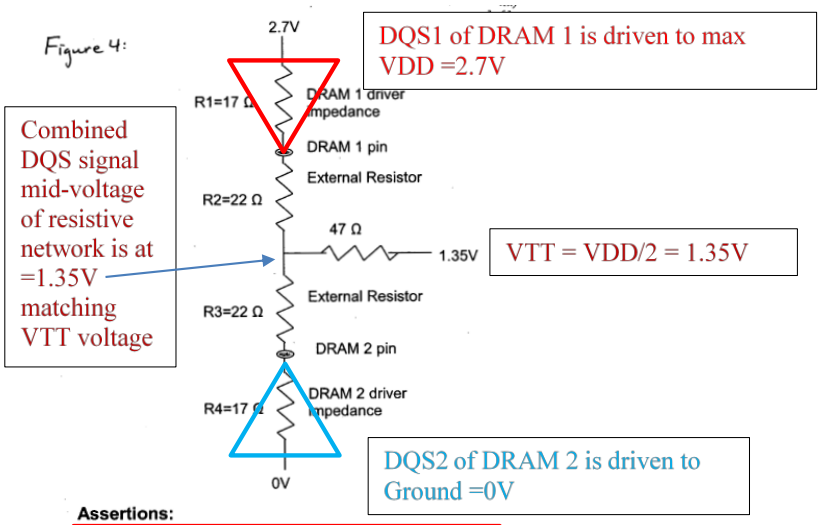


Figure 4:



Assertions:

Data Read operation so controller is in hi-Z
DRAM 1 driving high, DRAM 2 driving low
Upper network = lower network so mid-voltage = VTT voltage
therefore RTT is not considered
Concern is power burn in the drivers

Voltage at DRAM 2 pin = R4/(R1+R2+R3+R4) * 2.7V = 0.59V
Current in DRAM2 driver = 0.59V/ R4 = 34 mA
Power dissipation in DRAM 2 driver = 34mA * 0.59V = 20 mW
22Ω resistors, R1 and R2 are current limiters

Duration of overdrive = 0.8ns max
Total surge = 0.59V * 1.2ns = 0.3 V-ns
JEDEC spec for overshoot/undershoot = 2.4 V-ns

97. In the ’668 Application, the illustrated solution and computation example consider worst case conditions for the combined DQS signal level voltage, i.e., choosing maximum operating voltage of 2.7V and choosing twice the worst case scenario for potential skew between DQS and DQ signals to account for “**variation of the output drivers for any given cycle.**” *See* EX1006, p. 16, note 12. The disclosed solution further specifies that due to the collision of DQS1 (=2.7V) and DQS2 (=0V) and in the extreme case when one DRAM1 DQS driver skew is at +0.4ns while the skew of DRAM2 DQS driver is at -0.4ns, the circuit of the specific solution of the ’668 Application would results in a maximum voltage at DRAM2 driver pin of 0.59V. This yields a total surge of 0.3V-ns for the duration of 0.8ns. *Id.*

98. This surge level is far below the tolerance under JEDEC specification for overshoot and undershoot of 2.4V-ns. *See* EX1006, Figs. 3-4. This means that the resulting surge is within the JEDEC specification tolerance and will not adversely affect the signal detection of logic levels 1 and 0.

99. Thus, the ’668 Application provides a solution via a resistive network that resolves collisions, during read operations, between two DQS

signal drivers that are combined. The solution solves both the combined DQS signal voltage level issue as well as the short circuit currents causing the driver damage issue. *Id.*

V. CLAIM CONSTRUCTION

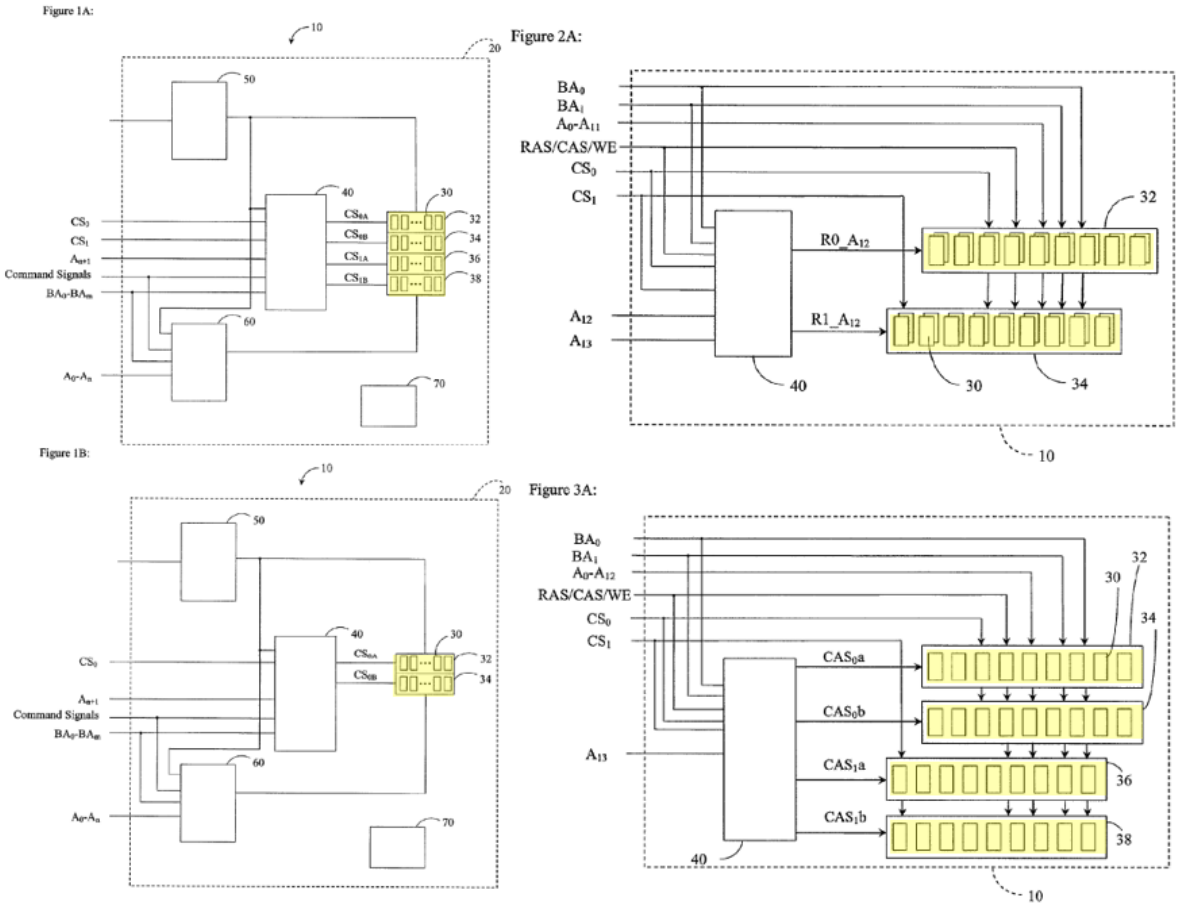
A. "Rank"

100. I am asked to comment on whether, in the context of the '912 patent, a person of ordinary skill in the art would understand that a rank of memory devices on a DRAM module can include a single memory device per rank. My opinion, as informed by the patent itself and the state of knowledge at the time of the invention, is no.

101. I understand that during reexamination, the Examiner allowed claim 16 by concluding that Amidi did not teach a person of ordinary skill in the art how to "transmit a command signal to only one DDR memory device at a time ***when there is a plurality of memory devices in a rank***." EX1010, 3865-67; *supra*, ¶50. I understand that SmartModule submitted comments challenging this claim construction, specifically arguing that Amidi rendered claim 16 obvious to the extent that claim 16 "requir[ed] only that the command signals are sent to a single rank ***because "one memory device" encompasses a rank of***

[one] memory." EX1010, 4442; *see supra*, ¶51. In the subsequent Office action, the Examiner maintained the construction of claim 16. EX1010, 4828, 4830, 4702-4, 4723-25; *see supra*, ¶52. The Board affirmed the Examiner's decision upholding the patentability of claim 16 because the claims require a plurality of memory devices in a rank and Amidi does not disclose addressing a single device within the plurality of devices that constitutes a rank. EX1011, 79-80; *see supra*, ¶53. I agree with the Examiner's and Board's construction because, as explained below, that construction comports with the intrinsic evidence, which consistently shows that a "rank" of memory devices includes more than one memory device.

102. The figures in the '912 patent consistently show memory modules featuring multiple memory devices in each rank. *See id.*, Fig. 1A-B, 6:31-38, 2A, 3A (reproduced below, with multi-device ranks highlighted).



103. The written description makes repeated and consistent references to ranks composed of multiple memory devices:

- "[I]n certain embodiments, two ranks of memory devices having a memory density are used to simulate ***a single rank of memory devices*** having twice the memory density…." *Id.*, 12:13-25.

- "Thus, in certain embodiments, even though the memory module 10 actually has the first number of ***ranks of memory devices*** 30, the memory module 10 simulates a virtual memory module by operating as having the second number of ***ranks of memory devices*** 30." *Id.*, 7:9-13.
- "[I]n certain embodiments, the ***memory devices*** 30 are arranged in four ranks, as schematically illustrated by FIG. 1A. In other embodiments, the ***memory devices*** 30 are arranged in two ranks, as schematically illustrated by FIG. 1B. Other numbers of ***ranks of the memory devices*** 30 are also compatible with embodiments described herein." *Id.*, 6:31-38.

See also id., 7:55-8:43, 8:64-9:18 (Tables 1 and 2 providing logic tables "for the selection among ***ranks of memory devices*** 30"); *id.*, 10:31-35 ("In certain embodiments, the SPD device 70 comprises data which characterize the memory module 10 as having fewer ***ranks of memory devices*** than the memory module 10 actually has, ….").

104. The specification also distinguishes embodiments that "multipl[y] memory devices per rank" as depicted in Figures 1C and 2A from embodiments directed to "multipl[ying] the number of ranks per memory module" (*e.g.*, Figs. 1A-1B, 3A). *Compare* EX1001, 12:12-15 (discussing emulating a single, high density memory device where "[i]n certain embodiments, ***two memory devices*** having a memory density are used to simulate a ***single memory device*** having twice the memory density") & 12:36-37 (implementation that "multiplies memory devices per rank") *with id.*, 12:15-21 ("[I]n certain embodiments, two ***ranks of memory devices*** having a memory density are used to simulate ***a single rank of memory devices*** having twice the memory density") & 12:37-38 (implementation that "multiplies the number of ranks per memory module").

105. I understand that Petitioner relies upon the following passage from the '912 patent to support its interpretation that a "rank" of memory devices encompasses a single memory device:

> In certain embodiments, the command signal is passed through to the selected rank only (**e.g., state 4 of Table 1**). In such embodiments, the command signal (e.g., read) is sent to only one memory device or the other memory device so that data is supplied from one memory device at a time. In other embodiments, the command signal is passed through to both

> associated ranks (e**.g., state 6 of Table 1**). In such embodiments, the command signal (e.g., refresh) is sent to both memory devices to ensure that the memory content of the memory devices remains valid over time.

EX1001, 8:50-58 (quoted at Pet. 13-14).

106. Table 1 is a logic diagram "for the selection among ***ranks of memory devices*** using chip-select signals," indicating that the description that follows refers to ranks of multiple memory devices. *Id.*, 7:56-8:10.

> Table 1 provides a logic table compatible with certain embodiments described herein for the selection among ranks of memory devices **30** using chip-select signals.

TABLE 1

State	CS_0	CS_1	A_{n+1}	Command	CS_{0A}	CS_{0B}	CS_{1A}	CS_{1B}
1	0	1	0	Active	0	1	1	1
2	0	1	1	Active	1	0	1	1
3	0	1	x	Active	0	0	1	1
4	1	0	0	Active	1	1	0	1

State	CS_0	CS_1	A_{n+1}	Command	CS_{0A}	CS_{0B}	CS_{1A}	CS_{1B}
5	1	0	1	Active	1	1	1	0
6	1	0	x	Active	1	1	0	0
7	1	1	x	x	1	1	1	1

Note:

1. CS_0, CS_1, CS_{0A}, CS_{0B}, CS_{1A}, and CS_{1B} are active low signals.
2. A_{n+1} is an active high signal.
3. 'x' is a Don't Care condition.
4. Command involves a number of command signals that define operations such as refresh, precharge, and other operations.

107. In state 4 above, the rank corresponding to CS_{1A} is chosen. *Id.*, 8:29-32 ("In Logic State 4: CS_1 is active low, A_{n+1}, is non-active, and Command

is active. CS_{1A} is pulled low, thereby selecting Rank 2."). Based on the description of Table 1 above, state 4 is referring to transmitting a command signal to a rank with ***multiple memory devices***, in this example, a rank of two memory devices, such that "the command signal (e.g., read) is sent to only one memory device or the other memory device" in the same rank "so that data is supplied from one memory device at a time." *Id.*, 8:50-54. This is confirmed by the reference to "memory devices 30," which are consistently referred to throughout the specification as part of multi-device ranks. *See, e.g.*, *id.*, 6:31-38, 20:64-65, 22:34-35; Figs. 1A, 1B, 2A, 3A. Read in context, the embodiments described with reference to Table 1 refer to transmitting a command signal to one of multiple memory devices in the selected rank (*i.e.*, one of at least two memory devices in the rank corresponding to CS_{1A}). To the extent Petitioner contends that this is the only disclosure in the '912 patent regarding [16.e], I disagree for reasons explained above. *See supra*, ¶¶36-43.

108. I also understand that Petitioner argues that disclosures in the related '215 patent suggests "that a 'rank' just requires 'at least one … memory integrated circuit.'" Paper 14 at 5 (citing '215 patent, 3:33-35, 37:35-38). As

an initial matter, I note that this disclosure does not appear in the specification of the ’912 patent. *See generally* EX1001.

109. The disclosure that Petitioner points to, reproduced below, when read in context, would not be understood as defining the term “rank.” Rather, the disclosures provide context that a claimed “buffer” can be, but need not be, coupled to multiple memory devices in the rank. In other words, the buffer can be coupled to just “one” memory IC in the rank. *See* EX2109, 204 (37:35-38, 37:46-50) (“a buffer coupled between the at least one first memory integrated circuit and the memory bus, and between the at least one second memory integrated circuit and the memory bus”) (highlighted below). The ’215 claim also specifies that the buffer, in response to a memory command, “enable[s] communication of the first[/second] data burst between <u>the at least one first[/second] memory integrated circuit</u>” and the memory controller. *Id.*, p. 204 (37:54-56, 37:59-61, highlighted in green). This is consistent with the ’215 specification, where the language that Petitioner relies upon (yellow) is immediately followed by reference to the first and second data burst (green).

Id., 3:25-53. The disclosures simply provide context for the later-recited first/second memory ICs and their structures and functions.

1. A memory module operable in a computer system to communicate data with a memory controller of the computer system via a memory bus in response to memory commands received from the memory controller, the memory commands including a first memory command and a subsequent second memory command, the first memory command to cause the memory module to receive or output a first data burst and the second memory command to cause the memory module to receive or output a second data burst, the memory module comprising:

a printed circuit board having a plurality of edge connections configured to be electrically coupled to a corresponding plurality of contacts of a module slot of the computer system;

a register coupled to the printed circuit board and configured to receive and buffer first command and address signals representing the first memory command, and to receive and buffer second command and address signals representing the second memory command;

a plurality of memory integrated circuits mounted on the printed circuit board and arranged in a plurality of ranks including a first rank and a second rank, the plurality of memory integrated circuits including at least one first memory integrated circuit in the first rank and at least one second memory integrated circuit in the second rank, wherein the first rank is selected to receive or output the first data burst in response to the first memory command and is not selected to communicate data with the memory controller in response to the second memory command, and wherein the second rank is selected to receive or output the second data burst in response to the second memory command and is not selected to communicate data with the memory controller in response to the first memory command;

a buffer coupled between the at least one first memory integrated circuit and the memory bus, and between the at least one second memory integrated circuit and the memory bus; and

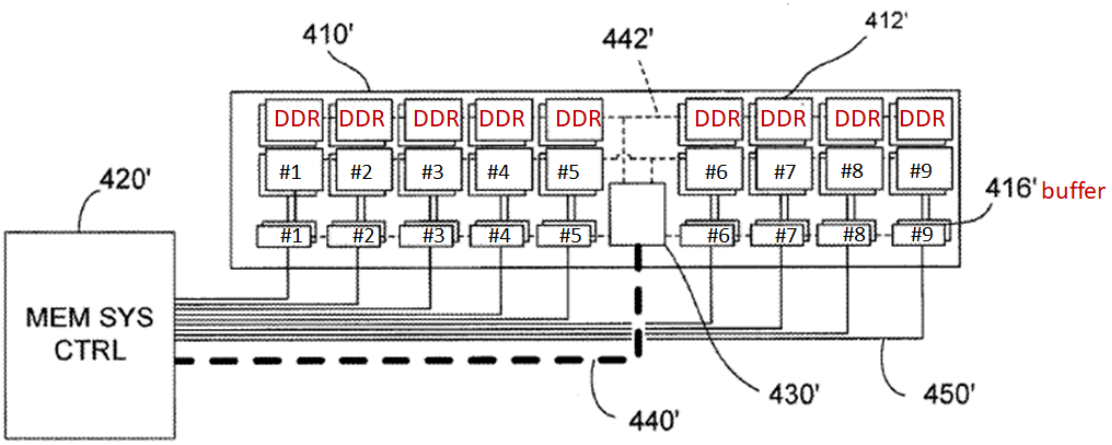
logic coupled to the buffer and configured to respond to the first memory command by providing first control signals to the buffer to enable communication of the first data burst between the at least one first memory integrated circuit and the memory controller through the buffer, wherein the logic is further configured to respond to the second memory command by providing second control signals to the buffer to enable communication of the second data burst between the at least one second memory integrated circuit and the memory controller through the buffer, the second control signals being different from the first control signals.

(EX2038 cl. 1, 37:13-62)

In certain embodiments, the printed circuit board has a plurality of edge connections configured to be electrically coupled to a corresponding plurality of contacts of a module slot of the computer system. The register is configured to receive and buffer first command and address signals representing the first memory command, and to receive and buffer second command and address signals representing the second memory command. The plurality of memory integrated circuits are arranged in a plurality of ranks including a first rank and a second rank, and including at least one first memory integrated circuit in the first rank and at least one second memory integrated circuit in the second rank. The first rank is selected to receive or output the first data burst in response to the first memory command and is not selected to communicate data with the memory controller in response to the second memory command. The second rank is selected to receive or output the second data burst in response to the second memory command and is not selected to communicate data with the memory controller in response to the first memory command.

(EX2038, 3:25-43)

110. An illustration of what the ’215 claim is referring to is provided below. As can be seen, in the configuration below, there are multiple buffers for data signal line, each buffer coupled to only one of the memory devices in each of the ranks. But each rank has multiple devices. In the ’215 patent, Figures 5A-5B illustrate similar constructs (albeit showing only one of the buffers/switches 120). *See* EX2038, 8:66-9:3 (“The one or more switches 120 [data buffers] are operatively coupled to the logic element 122 to receive control signals from the logic element 122 and to selectively electrically couple one or more data signal lines to a common data signal line.”).



111. Additionally, if as Petitioner alleges, a single memory device could be understood to be a “rank,” there would have been no need for the applicant to

draft claims reciting "at least one first memory integrated circuit in the first rank" and "at least one second memory integrated circuit in the second rank." EX2038, 37:34-38.

112. A construction of "rank" that requires more than one memory device is also consistent with Samsung and Micron's evidence and the positions taken outside this proceeding. For instance, in IPR2022-00063 (in which I served as an expert witness), Samsung asserted that "[t]he term 'rank' should be construed to mean an independent set of memory device***s*** [plural] that act together in response to a memory command … to read or write the full bit-width of the memory module." EX2055, 13. This definition does not provide for a single-device-per-rank construct.

113. The proposed construction in IPR2022-00063 by Samsung is consistent with the agreed-to construction for "rank" in *Netlist Inc. v. Google LLC*, Case No. 3:09-cv-4718 (N.D. Cal.), where the parties have agreed that the term "rank" as used in the '912 patent should be construed to mean "a group of memory device***s*** [plural] enabled to receive and transmit data by a common chip-

select signal." EX2026, 7.[4] Again, this construction contemplates multiple devices per rank.

114. I also understand that Dr. Wolfe agreed in IPR2022-01427/28 that "a rank is a collection of DRAMs that respond a common memory command simultaneously." EX2056, 36:2-10.

> Q. Okay. I thought a rank is a collection of DRAMs that respond to a common memory command simultaneously. That's not your understanding of what rank is?
>
> MR. CHANDLER: Objection. Form.
>
> THE WITNESS: That is my understanding. But I think in common usage, one would still call something a rank if it had that capability but also had the capability to do a partial read.

[4] This definition is not precise, and a better construction for "rank" would be "a predetermined set of DRAMs on a memory module that act together to send or receive a fixed number of data bits via a fixed width data bus, in response to a read or write command and independently from other DRAMs on the memory module."

115. While Dr. Wolfe also asserts that a rank of memory devices can "do a partial read," the testimony nevertheless confirmed the understanding that a rank includes multiple devices. Instead, what Dr. Wolfe is saying is that not all devices in a rank need to participate in a read or write. That, however, is inconsistent with the Petition's proposal that the devices in a rank are to "act together" in response to command signals. Pet. 12.

116. I also note that in one JEDEC proposal by Samsung, Samsung stated that "[a] rank of memory is defined as the collection of SDRAMs driven by a given rank select signal, S0 through S3." EX1091, p.147.

Serial Presence Detect:

Byte 5 of the standard serial presence detect (SPD) describes the number of ranks of memory installed on the RDIMM. A rank of memory is defined as the collection of SDRAMs driven by a given rank select signal, $\overline{S0}$ through $\overline{S3}$. SPD byte 5 of a 4 rank RDIMM will contain the value 0x04.

117. I understand that when discussing this passage, Samsung's corporate representative on the topic of JEDEC standardization of memory modules, Dr. Sungjoo Park, denied that a rank of memory could include just a single DRAM:

> Q: It says, quote, "a rank of memory is defined as the collection of SDRAMs," plural, "driven by a given rank select signal."
>
> Do you see that?

A: Yes, I see that.

Q: Sir, this statement is incorrect; the accepted definition of rank in 2007 or 2008 in the concept of DRAM memory modules includes a single DRAM; correct?

A: ***No, that's not right***.

EX1090, 87:1-17. This understanding is consistent with the Jacob textbook (2008) cited in the Petition.

118. For example, the Jacob textbook (EX1033) consistently depicts and describes ranks on a memory module as having more than one memory device per rank. For example, Figure 10.5 mentioned immediately before the first statement shows four devices per rank. *See* EX1033, 413.

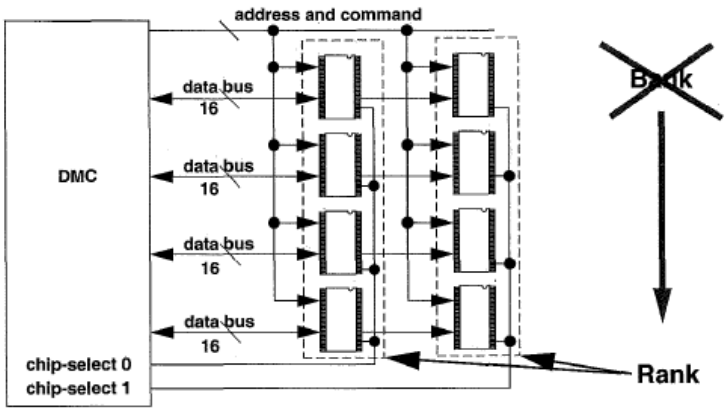


FIGURE 10.5: Memory system with 2 ranks of DRAM devices.

See also, EX1033, 318 ("Each rank is ***a set of DRAM devices*** that operate in unison"), 319 Fig. 7.5 ("Each rank is a set of ganged DRAM devices"), 421 ("a DRAM memory module can be organized as multiple ranks of DRAM devices on the same memory module, ***with each rank consisting of multiple DRAM devices***").

119. I understand that the Jacob textbook states that "a *rank* of memory is a '*bank*' of one or more DRAM devices that operate in lockstep in response to a given command." EX1033, 413. I agree that historically, "rank" and "bank" were sometimes used interchangeably. For instance, the "banks" shown in Figure 2 of Ellsberry would be understood as "ranks." But I disagree that this history or the Jacob textbook suggests that a person of ordinary skill in the art would understand a rank of DRAM devices on a memory module could include just one DRAM device.

120. For instance, Jacob continues from the statement quoted above and cited in the Petition that, because "the word *bank* has already been used to describe the number of independent arrays within a DRAM device," the term "rank" is used "[t]o lessen the confusion." EX1033, 413. The Jacob textbook

then states "the word *rank* is ***now used*** to denote a set of DRAM devices that operate in lockstep to respond to a given command." *Id.* A person of ordinary skill in the art would understand from the context that it is this statement that conveys the understanding of the term "rank" at the time of invention. That definition of "rank" ***excludes*** the reference to "one or more DRAM devices," i.e., excludes a single-device "rank."

121. In fact, the reference to "operat[ing] in lockstep" in EX1033 would not make any sense for a single-device rank, because in such a rank, there would be no other DRAM devices that operate "in lockstep" in response to a command. Similarly, the Petition's proposed construction—"an independent set of ***one or more memory devices*** on a memory module that ***act together*** in response to command signals … to read or write the full bit-width of the memory module"—connotes multiple devices per rank because "act[ing] together" again connotes multiple devices. Pet. 12.

122. Micron's definition of "rank" outside this proceeding also indicates that the industry understands a rank in the context of a DRAM module as including more than one device. For example, Micron's website notes that the

term "ranks" "are specific to memory modules and refer to ***a sub-array of multiple*** DRAM components":

What is the difference between a "bank" and a "rank?"

Banks are specific to individual DRAM components and refer to sub-arrays within the DRAM component. Ranks are specific to memory modules and refer to a sub-array made of multiple DRAM components.

EX2058, EX2107 (Micron FAQs), 2.

123. In another FAQ, Micron states that "[a] rank typically refers to the data bus width of a system," and "[t]his width is generally 64 or 72 bits." EX2108, p.2.

What is a "rank"?

A rank typically refers to the data bus width of a system. This width is generally 64 or 72 bits. For example, if 8 components with a width of 8 bits each are mounted to a PCB, this creates a module that is 64 bits wide, enabling a 64-bit word to be read out of the module. We refer to this as a "single-rank" module. Sixteen components with a width of 8 bits each can be mounted to a PCB to form two, 64-bit-wide ranks, creating a "dual-rank" module.

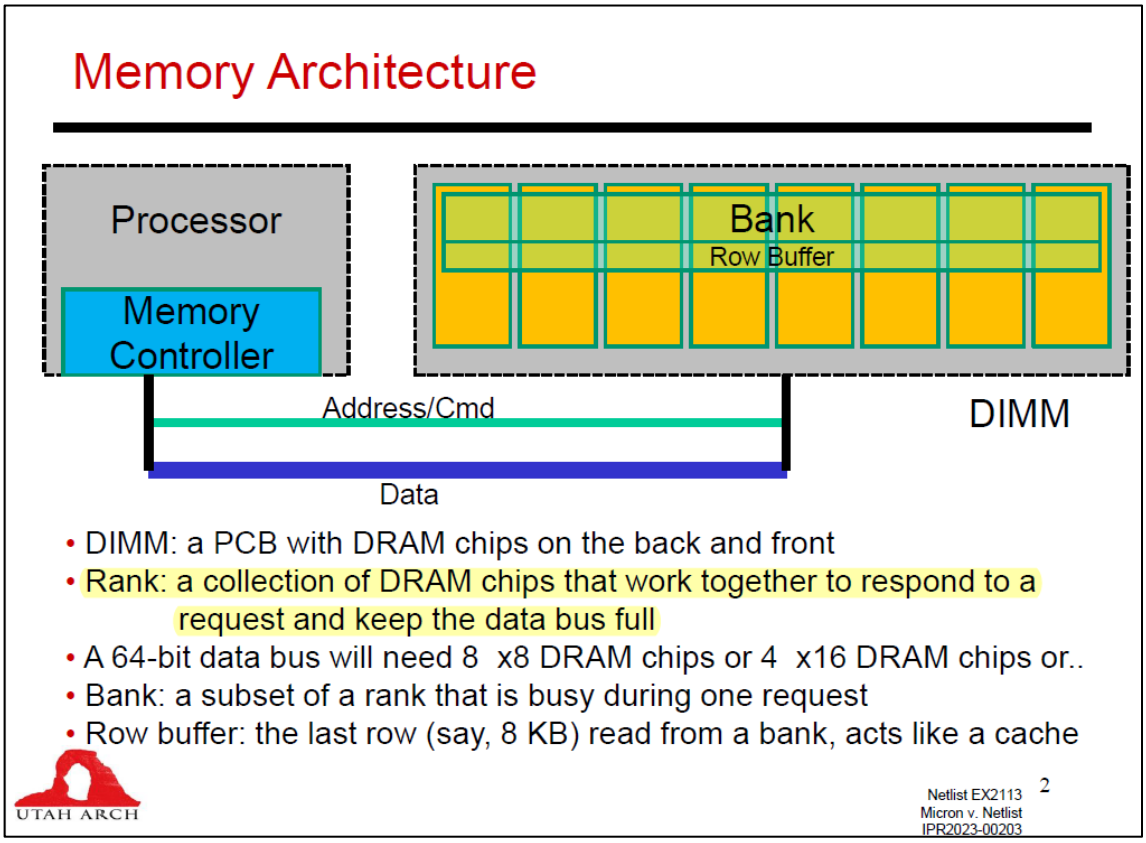
124. On another web site, Micron explains that "[a] rank is a data block that is 64 bits wide" without ECC or "72 bits wide" with ECC. EX2112, 1.

What is a Memory Rank?

The term rank was created by JEDEC, the memory industry's standards group, to distinguish between the number of memory banks on a module as opposed to the number of memory banks on a component, or memory chip. The concept of memory rank applies to all memory module form factors, though in general it tends to matter primarily on server platforms, due to the larger amounts of memory they manage.

A memory rank is a block or area of data that is created using some, or all, of the memory chips on a module. A rank is a data block that is 64 bits wide. On systems that support Error Correction Code (ECC) an additional 8 bits are added, which makes the data block 72 bits wide. Depending on how a memory module is engineered, it may have one, two, or four blocks of 64-bit wide data areas (or 72-bit wide in the case of ECC modules.) This is referred to as single-rank, dual-rank, and quad-rank. Crucial denotes this on the module label as 1Rx4, or 2Rx4, 2Rx8, or similar.

125. Samsung's and Micron's statements on the definition of "rank" outside this proceeding is consistent with how the concept of "rank" is taught in college. *See* EX2113, p.2 ("rank" is described as "a collection of ***DRAM chips*** that work together with respect to request and keep the data bus full").



126. Thus, in the context of the ’912 patent, a rank of DDR devices on a memory module would not be understood as including a rank of a single DDR device.

VI. OVERVIEW OF THE REFERENCES

127. I provide the following brief overview of each reference cited in the Petition.

A. Perego-422

128. U.S. Patent No. 7,363,422 to Perego ("Perego-422") was filed January 28, 2004, and issued as a patent on April 22, 2008. EX1035. While Perego-422 was not considered during the prosecution of the '912 patent, I note that a related patent, U.S. Patent No. 7,356,639 to Perego ("Perego-639") was disclosed by Patent Owner in an Information Disclosure Statement dated June 19, 2009, and considered by the Examiner. *See* EX1002, 125, 523.

129. Perego-422 discloses a memory system architecture with point-to-point topology which includes buffered modules having a configurable width buffer device. EX1035, Abstract; 5:35-55, 8:10-17, 8:20-26. In Perego-422's memory system 305, depicted below, buffered modules 330a-330n include a configurable-width data buffer (red) that receives signals from the memory controller via point-to-point links 320a-n. *Id.*, 5:64-6:3, 6:12-18. The buffer device communicates to the plurality of memory devices on the buffered module via channels 370. *Id.*, 5:4-6, 6:18-24. Perego-422 provides that these channels "may be subdivided into several addressable subsets," and discloses an embodiment wherein "the target subset of secondary channel signal lines may

be selected via address bits provided as part of the primary channel request" from the memory controller. *Id.*, 14:62-65, 15:31-40. Perego-422 explains that one purported benefit of accessing a subset of secondary channel signal lines per transaction is that this allows "grouping memory devices into multiple independent target subsets (i.e. more independent banks)." *Id.*, 15:40-45.

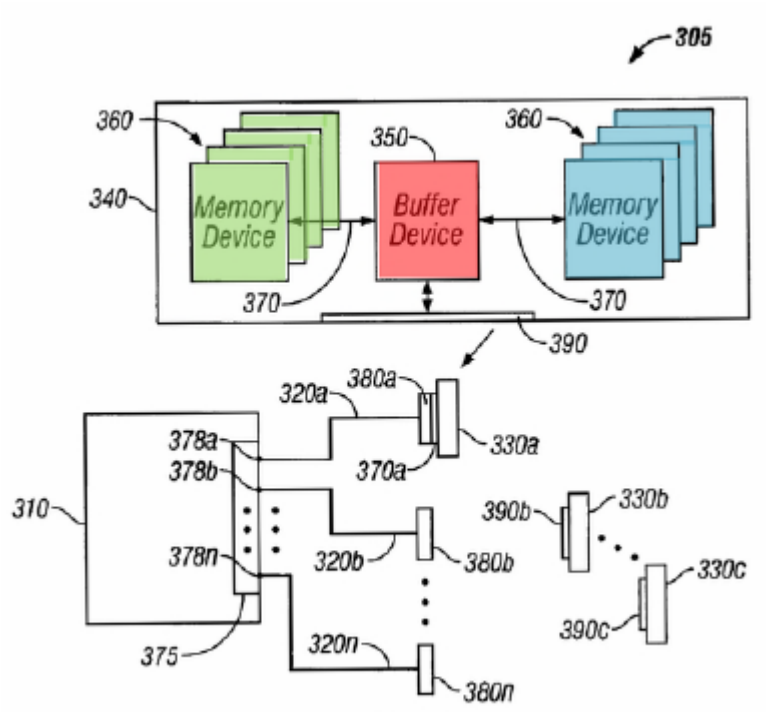


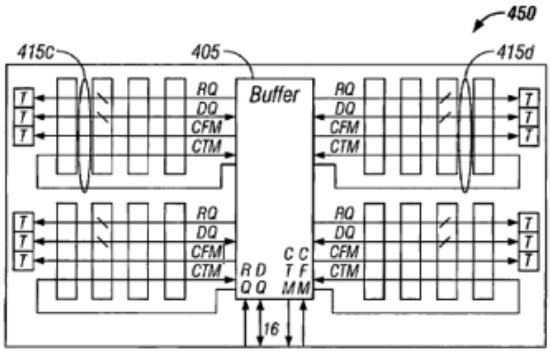
FIG. 3B

130. Figures 4A-4C depict buffered memory modules according to embodiments of Perego-422's invention. *Id.*, 9:26-33. I understand that Petitioner relies on a modified version of Perego-422's Figure 4B, *see, e.g.*, Pet.

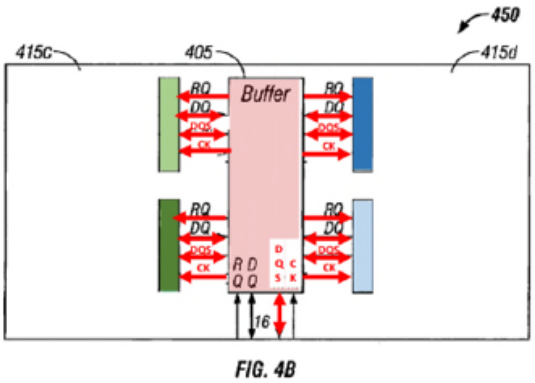
61-62. In Petitioner's modified version of Figure 4B, the buffered module of Perego-422 features four single-device ranks with one x16 memory device in each rank. Pet. 30-31. I understand that Petitioner contends that each of the memory devices has its own "dedicated" channel, and thus the four channels correspond to the claimed "first number of ranks." Pet. 30; EX1003, ¶124 (Dr. Wolfe modifying Fig. 4B such that "each of channels 415a-d is coupled to a single respective DDR memory device").

131. For context, the original Figure 4B of Perego-422 shows a memory module with multiple memory devices (*e.g.*, 32) that communicate with the data buffer via four channels (415a-415d). *Id.*, 9:26-33, 10:22-36, Fig. 4B (reproduced below side-by-side with Petitioner's modified version of Figure 4B). Perego-422 explains that these channels may operate in pairs or simultaneously. *Id.*, 10:22-36. In the paired arrangement, "channels 415c and 415d are ***routed in parallel*** with channels 415a and 415b." *Id.*, 10:24-25. In the simultaneous arrangement, "channels 415a and 415b may operate ***simultaneously*** with channels 415c and 415d." *Id.*, 10:32-33. For the paired arrangement, a person of ordinary skill in the art would regard the memory

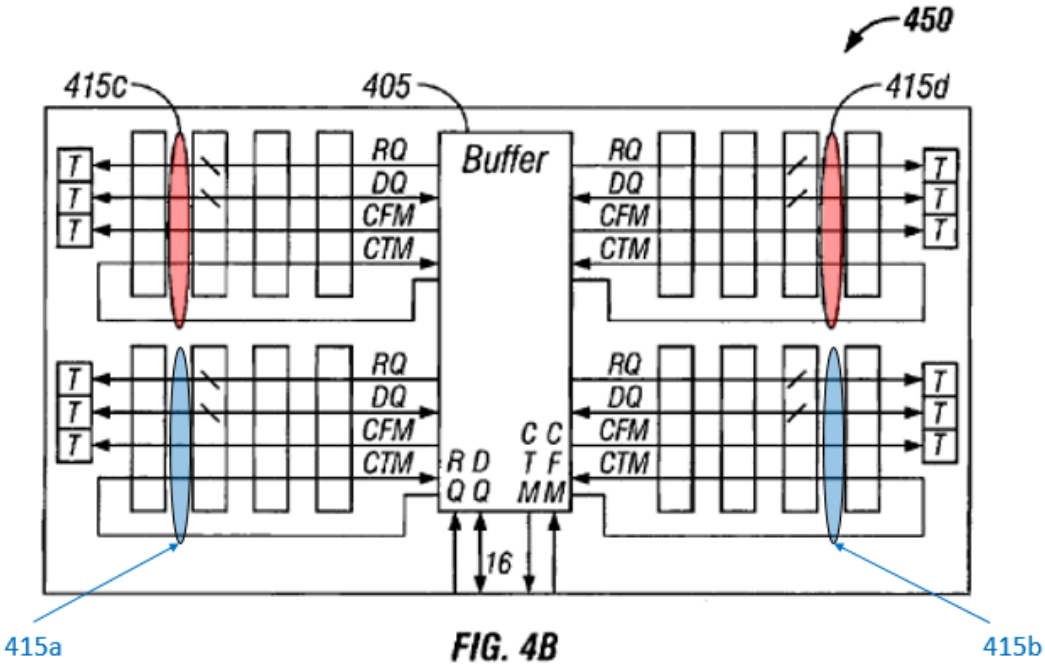
devices in channels 415a and 415b as belonging to a single rank because they operate together in response to a command, and similarly the memory devices in channels 415c and 415d as belonging to a single rank because they operate together in response to a command. Similarly, when all four channels operate simultaneously, a person of ordinary skill in the art would regard all memory devices in the four channels as belonging to a single rank because of their "togetherness." In other words, neither arrangement is compatible with Petitioner's single-device rank construct based on Figure 4B. *See infra*, VII.C.2.



EX1035, Fig. 4B



Pet. 62 (modified Figure 4B)



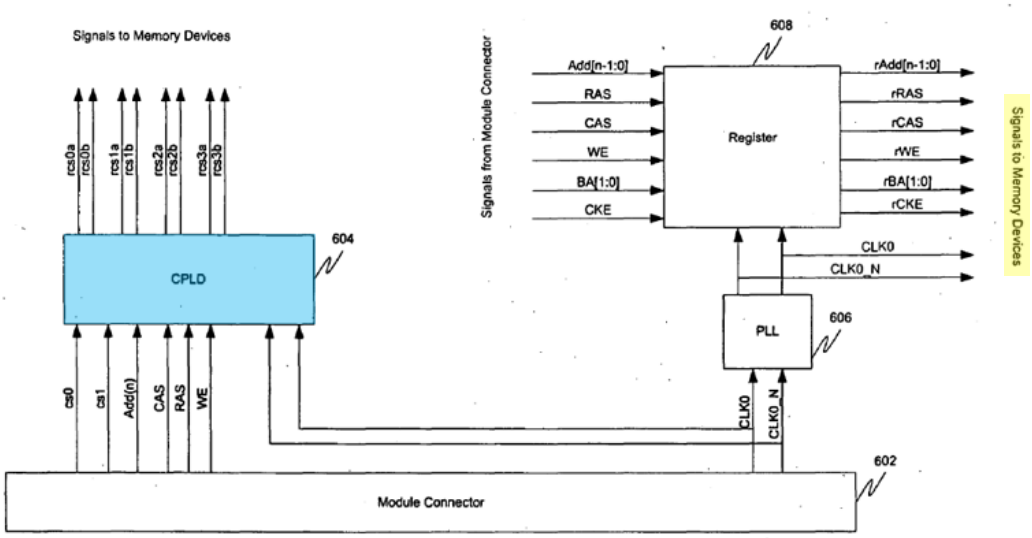
EX1035, Fig. 4B (annotated to show four channels 415a-d).

B. Amidi

132. U.S. Patent Application Publication No. 2006/0117152 to Amidi et al. ("Amidi") was filed on January 5, 2004 and published on June 1, 2006. EX1036.

133. Amidi discloses a four-rank "transparent" memory module which emulates a memory module with two ranks in order to "fit[] into a memory socket having two chip select signals routed." EX1036, Abstract [0011]. Figure 6A illustrates Amidi's four-rank memory module, which features a CPLD that

receives as input two chip-select signals (cs0/cs1), Add(n), and commands (*e.g.*, RAS/CAS/WE) and "generates rcs2 and rcs3, besides rcs0 and rcs1 off of CS0, CS1 and Add(n) from the memory controller side." *Id.*, [0050]-[0051].



Row Address Decoding
FIG.6A

134. As summarized above, Amidi was considered extensively throughout the '912 reexamination. *See supra*, IV.B. The Examiner concluded that Amidi's RAS and CAS signals ("command signals") were not transmitted to only one DDR memory device on the selected rank, as required by the claims. EX1010, 3865-67, 3904. The Board later affirmed this finding, emphasizing the Examiner's conclusion that "Requester has not provided a reasonable

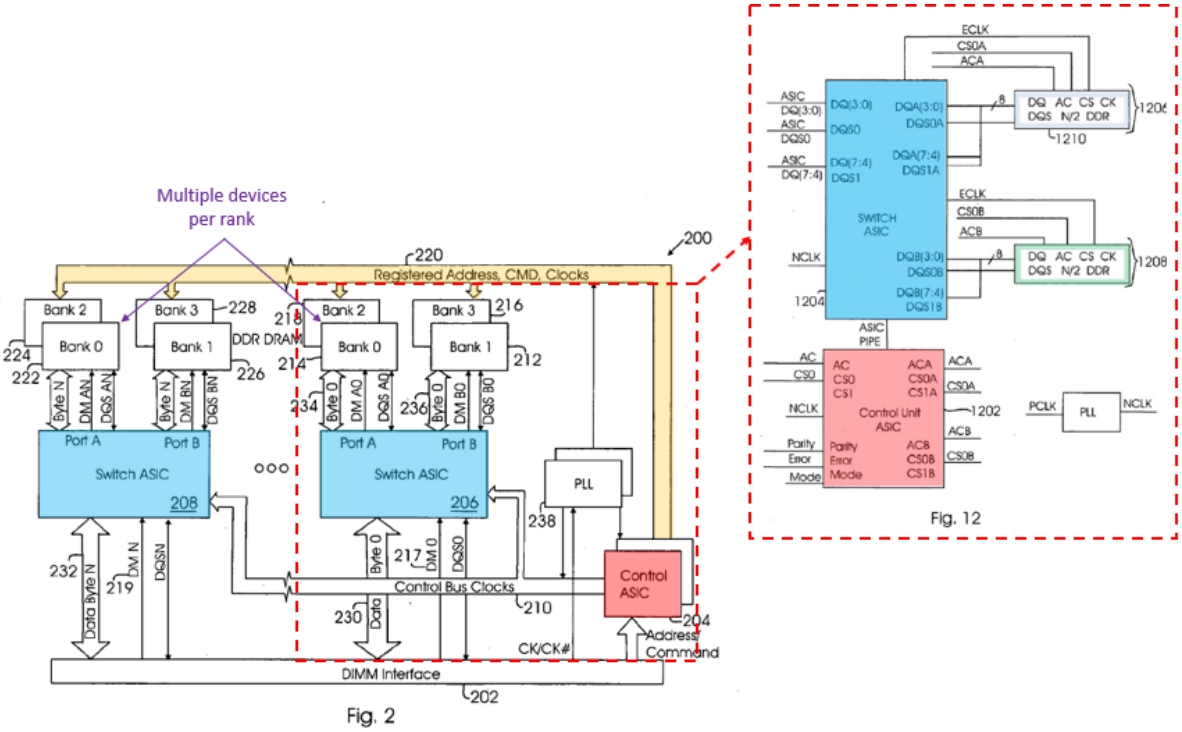
explanation as to why one skilled in the art would transmit a command signal to ***only one DDR memory device at a time when there is a plurality of memory devices in a rank***." EX1011, 79. The Board explained that Figures 6A and 6B of Amidi "show[ed] various command signals [] being transmitted to more than one memory device," as evidenced by the label "Signals to Memory ***Devices***" on those figures. *Id.*

C. Ellsberry

135. U.S. Patent Application Publication No. 2006/0277355 (EX1037) ("Ellsberry") was filed on June 1, 2005. Ellsberry was cited by the Examiner during prosecution of the '912 patent, but was not considered as prior art because "the Examiner … assumed Ellsberry was not prior art." Pet. 112; EX1002, 510. As discussed above, I agree with the Examiner that Ellsberry is not prior art to the '912 patent, which claims priority to, *inter alia*, the '244 provisional and the '436 patent. *See supra*, IV.C.

136. Ellsberry discloses a memory module architecture, depicted in Figure 2, that "permits transparent bank switching of memory devices." EX1037, [0001]. Control ASIC 204 (red) "receives memory addresses and

commands over the DIMM interface 202" from the system memory controller, and switch ASICs 206 and 208 (blue) "receive data information from the DIMM interface 202 via data buses 230 & 232, respectively." *Id.*, [0028]-[0029]. Each switch ASIC is connected to a number of memory banks (e.g., Bank 0-3 below), each with one or more memory devices. *Id.* Switch ASICs 206 and 208 receive respectively data byte group N and data byte group 0, provided "simultaneously" by the DIMM interface 202. *Id.*, [0030], Fig. 2 (depicting at least two data groups); Fig. 5 (depicting nine data groups). As explained in greater detail below in Section IX, Figures 10-13 illustrate parts of Ellsberry's overall memory module architecture depicted in Figure 2. *See id.*, Figs. 2 and 12 (reproduced below, annotated); EX1038, 50 (Board noting that "Figure 13 shows ***part of a memory module***"), 51, 57, 77, 81; EX2032, 40 n.11.



137. Control ASIC 204 sends command signals to memory devices in different memory banks via bus 220. *Id.*, [0030]. Each switch ASIC includes two data ports, Port A and Port B, coupled respectively to data busses 234 and 236. One method Ellsberry discloses for sending commands to selected banks is the use of a row/bank addressing scheme to send commands to an intended bank, while sending NOP commands to the other bank. *Id.*, [0042] ("Row/Bank addressing is used, then a READAP command is sent to the intended bank while a NOP command is sent to the other bank."). I note that Petitioner's analysis

only relies on Ellsberry's row/bank addressing mode. *See* Pet. 100-102, 109-110.

VII. PEREGO-422 DOES NOT RENDER OBVIOUS CLAIM 16

A. Perego-422 Does Not Disclose or Suggest Rank Multiplication

1. Perego-422 has no need for rank multiplication

138. I understand that the Petition's unpatentability theory for the Perego-422 grounds are based on a mapping that each channel constitutes a rank. *See* Pet. 30-31 (modified Perego, Figure 4B showing four devices in four channels, allegedly one for each rank); EX2103, 198:3-14 (Dr. Wolfe confirming that he is only "relying on an embodiment where each channel is one rank"). Under that theory and given Perego-422's express disclosures, there is no reason for Perego-422 to adopt rank multiplication because Perego-422 can use address bits to select any number of channels (the alleged rank) on the memory module.

139. As would be understood by a person of ordinary skill in the art, rank multiplication is used where the number of (chip-select) signals that memory controllers can use to select a set of memory devices (a rank) is less than the number of sets of memory devices (number of physical ranks) on a memory

module. ’912 patent (EX1001), 2:38-41 (“Most computer and server systems support one-rank and two-rank memory modules. By only supporting one-rank and two-rank memory modules, the memory density that can be incorporated into each memory slot is limited.”); EX1036, [0010] (“As explained earlier, all standard memory modules have only two chip select signals per memory socket routed. Therefore, such [four-rank] memory module would not be viable.”), [0011] (“A need therefore exists for a transparent four rank memory module fitting into a memory socket having two chip select signals routed. A primary purpose of the present invention is to solve these needs and provide further, related advantages.”). But that limitation does not exist in Perego-422 because Perego-422 uses “address of the transaction [to] determine which target subset of channels 370 will be utilized for the data transfer portion of the transaction.” EX1035, 14:62-65. That is, Perego-422 already has a way to select the desired number of channels and associated devices (and that method does not at all rely on chip-select signals). *Id.*; *see also* 15:37-40 (“the target subset of secondary channel signal lines may be selected via address bits provided as part of the primary channel request”), 10:20-22 (“The width of the channel refers to the

number of parallel signal paths included in each channel"); 10:22-36 (Perego-422 already capable of having two out of four channels or all four channels run simultaneously).

140. Thus, if each channel is a rank as asserted, there would be no need for Perego-422 to utilize rank multiplication to "fool" the memory controller into believing that there are fewer channels on a module than there actually are. Perego-422's memory controller apparently can just utilize address bits to signal which channel or channels to target.

2. There is no substantial evidence for rank multiplication in the manner suggested by Petitioner

141. For Ground 1, Petitioner argues that a POSITA would have used "four ranks of low density (inexpensive) x16 memory devices in place of one rank of high-capacity (expensive) x8 memory devices." Pet. 39. Specifically, Petitioner argues that a person of ordinary skill in the art would have used four 16-bit wide 32Mbx16 DDR2 devices instead of two 128Mbx8 DDR2 devices to form a 2Gb memory module. Pet. 40-41.

142. I note that no references of record have proposed this type of "rank multiplication" where four lower-density devices of 2*n*-bit width in four ranks

are used to simulate two higher-density devices with *n*-bit width in a single logic rank. Instead, even according to the Petition, Amidi and Ellsberry each use two lower-density *n*-bit width device to simulate one higher-density *n*-bit width device. Pet. 43 (in Amidi, "a (virtual) 128Mbx16 memory device" is emulated as "two 64Mbx16 memory devices"), Pet. 84-85 (in Ellsberry, "two 256Mb(x8) memory devices emulate one 512Mb(x8) memory device"). The '436 patent disclosed that two 128Mbx4 devices could be used to emulate one 128Mbx8 device. *See* EX1009, 15:59-64 ("In certain embodiments, a memory controller of a computer system utilizing a 1-GB 128M 8 memory module 500 comprising pairs of the 512-Mb 128M 4 memory components 510 supplies the address and control signals including the extra row address (A13) to the memory module 500."); *see also id.*, 17:25-29 (doubling memory density by doubling the number of ranks).

143. There are good reasons that the art has not gone the way Samsung suggested. First, the use of x16 devices is incompatible with memory modules having the ECC functionality where an additional byte is added to the memory module width. But the resulting x72-bit width is not divisible by 16-bits.

Second, Samsung's modification contemplates multiplying one rank into four ranks, making it incompatible with implementations having two virtual ranks. Emulating two virtual ranks with eight physical ranks would result in either insufficient space on the memory module or requiring fairly costly stacked chip technology. Third, quadrupling the number of ranks would make both the on-module logic more complicated and the routing to actual ranks more challenging than doubling the number of ranks, potentially eviscerating any device-level cost and power savings and making the whole system more costly and power hungry. Additionally, instead of just a single load from 1R or two loads from 2R, the bus has to deal with 4 loads from 4 ranks, which can significantly lower the actual data speed. For all these reasons, it is not surprising that the skilled artisans have never taken the path suggested by Samsung.

144. I understand that Dr. Wolfe admitted at deposition that the cost difference between x8 and x16 devices for a given density "depends on the market at the time." EX2103, 91:13-15. But I have not seen any data that substantiates the assertion that four 32Mbx16 DDR2 would have been cheaper than two 128Mbx8 DDR2 devices at the time of the inventions.

145. Additionally, if cost was a major motivation, Petitioner has not shown why a POSITA would have chosen four 32Mbx16 memory over four 64Mbx8 DDR2: Dr. Wolfe testified that ordinarily, 64MBx8 would be ***cheaper*** than the 32MBx16. EX2103, 91:25-92:2 ("Q. So initially 64Mbx8 is actually cheaper than the 32Mbx16? A. It's ordinarily what happens.").

146. Petitioner also argues that it was a trend at the time to increase DRAM data width. Pet. 39. Petitioner cites to EX1034, a paper by Jacob to support this assertion. But in that article, immediately following the section on "Increase DRAM Data Width" is a section on "Increase Module Data Width." EX1034, 20. The article further states "the DIMM bandwidth is more important than the bandwidth of an individual DRAM." *Id.* This statement makes sense because for improved throughput, module bit-width, not device bit-width, controls. Thus, if increasing device data width is for achieving higher bandwidth and throughput, then a person of ordinary skill in the art would not have reduced the module width from the then standard 64 bits to 16 bits, because the module bit width, not the device data bit width, determines what the bandwidth and throughput would be.

147. Petitioner also argues that using four 32MBx16 DDR2 would improve power consumption. Pet. 41. I reviewed the cited evidence and do not believe it supports Petitioner's contention. EX1035, 15:40-45, for example, discloses saving power by "addressing a subset of secondary channel signal lines per transaction," not using x8 versus x16 devices. The cited portion of EX1036 and EX1029 do not mention power usage. Additionally, EX1036 discusses devices of the same bit width. EX1036, [0046]-[0048]. Dr. Wolfe's testimony is also insufficient because it just considers the number of devices used per access cycles, but does not consider (1) power consumption per x16 device versus per x8 device and (2) the power consumption by devices not participating in the access cycle. For example, a 512MB module made from 64Mbx8-667 and a 2GB module made from 256Mbx4-667 devices have the following active current values according to a Micron datasheet. EX2057, pp.14, 18:

	Precharge standby current (mA)	active burst write current (mA)	active burst read current (mA)
512MB made from 64Mbx8-667	450	1530	1620

2GB made from 256Mbx4-667	360	1215	1215

148. Of note, each of the modules above is a single-rank module: 64Mb/(8 bits per byte) ×8×(64bit ÷ 8bit per device) = 512MB per rank; 256Mb/(8 bits per byte) ×4×(64bit ÷ 4 bit per device)=2GB per rank.

149. Assuming that each rank in a 2GB module made from 64Mbx8 devices would have the same active standby and write/read current as in the single-rank 512MB module, then for a 2GB module the total current in a write cycle would be 1530mA*n + 450mA*3n=2745n (n is the number of devices per rank, and when one rank is writing, the other three ranks are in standby).

150. In contrast, for the single-rank 2GB module made of x4 devices, the total current in a write cycle would be 1215mA*2n, less than 2745n. Hence, it is not the case that using twice the devices in a read/write cycle would necessarily result in higher power consumption.

B. Under the Correct Construction of "rank," Petitioner's Single-Device Constructs Are Not "ranks" [16.b.i]/[16.c.ii]

151. Claim 16 requires a "plurality of DDR memory devices having a first number of DDR memory devices arranged in a first number of ***ranks***," and

"a second number of DDR memory devices arranged in a second number of ***ranks***." EX1001, p. 44, 3:9-43; [16.b.i], [16.c.ii].

152. As discussed above, in the context of the '912 patent, a "rank" would be understood as comprising more than one memory device. *See supra*, V. By contrast, both Grounds 1 and 2 of the Petition rest on hypothetical constructs featuring single-device ranks, with one memory device corresponding to each of the four channels in Perego-422's Figure 4B. Pet. 28-43, 52, 54, 57, 62; *supra*, ¶¶130-131.

153. As a preliminary matter, I note that Petitioner has not shown that each channel constitutes a rank even under Petitioner's own definition of "rank," because it has not shown that any of Perego-422's memory devices "***act together*** in response to command signals." *E.g.*, Pet. 28-32. *See infra*, ¶¶220-222.

154. Even if Perego-422 discloses the concept of organizing memory devices in "ranks," the Petition is admittedly limited to single-device ranks only. Petitioner's first example (Ground 1) features four x16 memory devices arranged in what it defines as four ranks ("first number of ranks"). Pet. 30 ("With respect to the 'number' of memory devices and ranks, Perego teaches an embodiment in

which its module includes four memory devices arranged in four ranks, each rank having a single memory device with a 'dedicated channel,' as shown in Figure 4B below ….”); *id.*, 39-41 (contending that “[a] POSITA would have understood that Perego’s module could use x16 memory devices to upgrade a memory system configured for memory modules having [two] x8 memory devices” arranged in one rank (second number of ranks)). That is, Petitioner’s first example is limited to a first number of single-device “ranks,” not the claimed ranks, which comprise multiple devices. *See supra*, V.

155. Petitioner’s second example (Ground 2) features four x16 memory devices arranged in what it defines as four ranks (“first number of ranks”) that Petitioner contends can simulate a module with two x16 memory devices arranged in what it defines as two ranks (“second number of ranks”) based on the combination of Perego-422 and Amidi. Pet. 42-43 (“In this second example, a POSITA would have been motivated to build Perego’s 16-bit wide module with four x16 memory devices for a system where the memory controller can control only two ranks per module, as in Amidi.”). As with Example 1, Petitioner’s relied-upon construct is a module “where each rank has one x16

memory device." Pet. 42; *id*., 43 (modified Fig. 4B). As above, Petitioner's second example is concededly limited to a first number of single-device "ranks," not the claimed ranks, which comprise multiple devices. *See supra*, V.

156. Accordingly, the Petition's Ground 1 (Perego-422) and Ground 2 (Perego-422 in view of Amidi) fail to disclose Elements [16.b.i]/[16.c.ii].

157. The Petition would also fail under Petitioner's own construction. Perego-422's implementation would involve numerous instances in which there are multiple devices per rank. *See*, *e.g.*, IPR2022-00454 ID at 25 (64-bit wide rank). But like the requesters in the '912 re-examination, Petitioner has not shown "why one skilled in the art would transmit a command signal to ***only one DDR memory device at a time when there is a plurality of memory devices in a rank***." EX1011, 79.

158. There is also no evidence that Perego-422 can target a single device in a "rank," which Petitioner asserts corresponds to a channel. For example, Perego-422 discloses subdividing channels into "several addressable subsets" and that the "address of the transaction will determine which target ***subset of channels*** 370 will be utilized for the data transfer portion of the transaction."

EX1035, 14:62-65. That is, Perego-422 discloses how to select a particular channel, but not a particular device connected to the channels. Similarly 15:37-40 relates to selecting a "target subset of secondary channel signal lines," and not specific devices. I agree with Dr. Wolfe that this passage does not teach selecting a particular group of devices to respond to a read or write operation:

> Q. But by selecting a subset of secondary channel signals, are you selecting a particular group of devices to respond to a single read or write request?
>
> A: I don't think so. Not in that situation. I think that that's specific to channel signal lines.
>
> ***
>
> Q. So you don't think this paragraph [15:37-45] has anything to do with grouping devices into different ranks?
>
> A: ***I do not think that this paragraph specifies how ranks are selected or enabled***.

EX2103, 202:8-204:10 (objections omitted).

159. I am informed that when a proposed modification would impair the primary reference's operation or stated goal during the majority of operation, then the modification is not obvious. In contrast to Petitioner's proposal to

decrease data bit width, Perego-422 emphasizes the need to increase bandwidth and capacity:

- 1:27-30: "In addition to upgradeability, many of these contemporary memory systems also require high ***throughput for bandwidth intensive applications***, such as graphics."
- 2:26-29: "There is a need for memory system architectures or interconnect topologies that provide flexible and cost effective upgrade capabilities ***while providing high bandwidth*** to keep pace with microprocessor operating frequencies."
- 3:31-36: "A buffer device having configurable width functionality may be employed to allow ***memory subsystem bandwidth to scale*** as the system is upgraded or to allow ***theoretical maximum memory subsystem bandwidth*** to be achieved among possible memory module configurations."
- 10:31-36: "In alternate embodiments, channels 415 a and 415 b may operate simultaneously with channels 415 c and 415 d ***to realize greater bandwidth***. By operating a plurality of channels in parallel, the bandwidth of the module may be increased independently of the memory capacity. The advantages of greater bandwidth may be realized in conjunction with larger capacity as more modules incorporated by the memory system 305 (see FIG. 3B) increase the system memory capacity."

160. Modifying the module data bit width to 16-bits is antithetical to the stated goal of increased bandwidth because as stated above, the module bit width is more important in determining the bandwidth/throughput than the individual devices' data bus width. Moreover, for increased capacity, it would also be more

desirable to use devices of narrower data bus width. This is because if the module width is n, then using ×8 devices would result in twice as many devices per rank as when using ×16 devices. Thus, if the ×8 devices have the same density as the ×16 devices, then a module made with ×8 devices would have twice the number of devices per module as a module made with ×16 devices, thus doubling the capacity. Hence, the proposed modification is inconsistent with the stated objective of Perego-422 and a person of ordinary skill in the art would not have made the proposed modification.

C. Perego-422's "channels" Do Not Constitute a "rank" Under Petitioner's Construction [16.b.i]/[16.c.ii]

161. Perego-422 does not use the term "rank." *See* EX2103, 204:16-21 (Dr. Wolfe acknowledging that Perego-422 does not use the word "rank").[5]

162. Grounds 1 and 2 rest on modified Figure 4B featuring four channels with one DDR each, with Petitioner interpreting each channel as one rank. Pet.

[5] Dr. Wolfe also testified that the term "bank" in Perego, 15:42-45 does not refer to "rank," but rather "page registers which can be activated corresponding to different addresses." EX2103, 203:11-25. In other words, the "bank" here refers to the internal array organization of a DRAM chip and not the module-level organization.

28-60; EX2103, 198:3-14 (Dr. Wolfe confirming that he is only "relying on an embodiment where ***each channel is one rank***"). Petitioner has not shown that each channel would qualify as a "rank" under its own construction for multiple reasons.

1. A DDR memory module of 16 bits and less was not known at the time of the invention

163. The Petition relies exclusively on 16-bit wide DDR memory modules having one 16-bit DDR per rank. *See, e.g.*, Pet. 39, 41 (relying on x8 and x16 memory devices for 16-bit-wide memory modules). But there is no evidence that a memory module of such a width and with DDR devices was known at the time of the invention. *See* cl. 16 (reciting memory modules having DDR devices); *cf.* EX1001, 5:60-64 (disclosing 32-bit wide modules as the lowest bit-width compatible with embodiments of the invention). Dr. Wolfe could not recall having ever "used a memory module with DDR or newer generations of DRAMs that's 16 bit wide or below" despite his 40 years of experience in the industry. EX2103, 146:2-12; *see also* 155:13-25 (not aware of any x8 memory modules using JEDEC compliant DDR or DDR2 devices or any articles describing such modules).

164. I am not aware of DDRx modules with a data bus width of 16 bits and below. This is likely because, at the time of the invention, the memory bus width on the CPU was generally 32 bits or higher, making 16-bit memory modules incompatible with the vast majority of the memory controllers. Petitioner does not suggest modifying memory controllers.

165. Another drawback of Petitioner's modification is that x16 memory devices would be incompatible with 72-bit memory modules (ones having ECC), because 72 is not divisible by 16.

166. Because Petitioner's proposal is incompatible with the vast majority of operations, the modification is not obvious.

2. Each channel reads or writes less than full bit-width of Perego-422's memory module

167. Petitioner relies on a modified Fig. 4B that supposedly involves four ranks, "each rank having a single memory device with a 'dedicated channel.'" Pet. 30-31. Perego-422 describes two alternative embodiments for the "quad-channel module 450" shown in Figure 4B. EX1035, 10:22-46. In one embodiment, "channels 415c and 415d are ***routed in parallel*** with channels 415a and 415b" (EX1035, 10:23-26), and in "alternate embodiments," "channels 415a

and 415b may operate ***simultaneously*** with channels 415c and 415d" (*id.*, 10:32-34). If Petitioner agrees with Dr. Wolfe that the two channels operating concurrently should be regarded as a single rank, (*see* EX2103, 198:3-8),[6] there are multiple (two or four) devices per rank in the modified Figure 4B.

168. But if Petitioner still considers that each channel is a rank, then the bit width per rank, *i.e.*, 16 bits, is less than the full bit width of the memory module, characterized by the device access width W_A. EX1035, 14:23-27 & 14:38 (memory device access width, W_A, is the "number of bits that can be accessed in a single memory device transfer operation to or from configurable width buffer device 391"); EX2103, 60:21-61:5 ("memory module bit-width" is a term "used to describe the number of bits that are communicated in a single read or write operation between the memory module and the host computer"); I agree that a person of ordinary skill in the art would have regarded W_A, corresponding to the number of bits per read/write operation, as the width of a rank.

[6] I understand that the parties agree that memory devices in a "rank" must "act together in response to command signals …." Pet. 12.

169. For example, under Petitioner's mapping involving ×16 memory devices, in the embodiment where channels 415 c/d are "routed in parallel" with channels 415 a/b, each transfer is 32 bits. In the embodiment where all four channels operate simultaneously, each transfer is 64 bits.

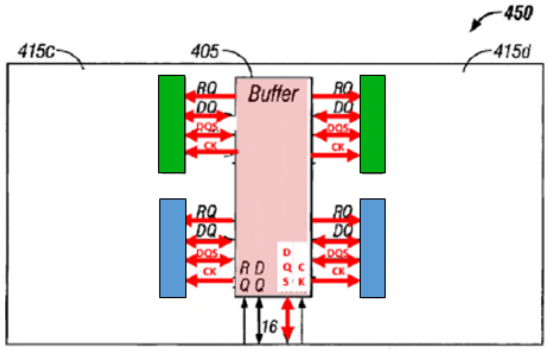


FIG. 4B

First arrangement (415c-d operate in parallel with 415a-b), 2x the device bit-width is transferred per operation

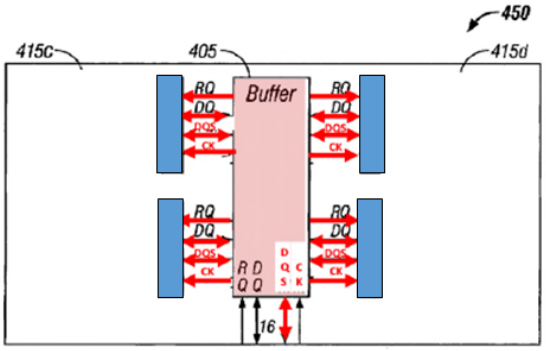


FIG. 4B

Second arrangement (all four channels operate simultaneously), 4x the device bit-width is transferred per operation

170. That is, the memory device access width, W_A, for Figure 4B would be either twice the per-channel bit width (first arrangement) or four times the per-channel bit widths. Hence, in response to a read/write operation, the memory device in each channel (the identified rank) does not "read or write the full bit-width of the memory module," as required by Petitioner's own definition.

171. Petitioner may argue that the memory module width is W_{DP} and not W_A. *See* Pet. 31 (contending that memory device access width $W_A = 16$, and "width of the memory module" is $W_{DP} = 16$). But even Dr. Wolfe testified that most engineers would describe the embodiment having a W_A of 128 bits and a W_{DP} of 16 bits "as a 128-bit wide memory module because that's the size of the transfers." EX2103, 61:6-14. Dr. Wolfe also testified that W_{DP} corresponds to the number of pins on the buffer device. EX2103, 56:13-21. That is, Dr. Wolfe does not regard W_{DP} as the module width; and I agree.

172. Petitioner may also argue that it is relying on implementations where read and write operations each involved just one 16-bit channel, resulting in a W_A-to-W_{DP} ratio of 1. But as noted above in Section VII.C.1, there is no evidence that at the time of the invention, 16-bit memory controllers operable with DDR/DDR2 SDRAMs memory modules existed. As a result, a POSITA would not have modified Perego-422 to generate 16-bit wide memory modules.

173. In the Institution Decision, the Board noted that "a single channel is feasible" in Perego-422. ID at 47; EX1035, 10:14-17. However, I agree with Dr. Wolfe that Perego-422's single-channel arrangement would have only one

physical rank and is "not practicing rank multiplication" as required by claim 16. EX2103, 53:7-54:7. Perego-422's single-channel embodiment therefore does not render obvious claim 16.

3. Channels selected for read/write are based solely on address information

174. The read/write operation of the set of devices in a rank is required to be "in response to command signals, including chip select signals." *See* Pet. 12.

175. Dr. Wolfe admits that Perego-422 does not use the words "chip select signal" or "rank select signal." *See* EX2103, 84:14-19 ("Q. And where does the word 'chip select signal' appear in Perego? A. In one place their individual device. Let me see. I don't think there's an explicit description of a chip select line...."). Rather, in the cited portion, Perego-422 discloses selecting a "target subset of secondary channel signal lines … ***via address bits*** provided as part of the primary channel request." EX1035, 15:37-40; *see also* EX1035, 14:60-65 (using addresses to "determine which target subset of channels 370 will be utilized for the data transfer portion of the transaction").

176. Dr. Wolfe states that "[a] chip select signal determines whether or not to pay attention to the command in a DDR environment." EX2103, 141:2-4. But nothing in Perego-422 suggests that the address bits used to select targeted channels are used to determine whether to pay attention to the command in a DDR environment.

177. Dr. Wolfe disagrees that selecting a subset of secondary channel signal lines is selecting a particular group of devices to respond to a single read/write request. EX2103, 202:8-10, 203:2-9. Dr. Wolfe further disagrees that the passage in 15:37-45 "specifies how ranks are selected or enabled." *Id.*, 202:8-204:10 (objections omitted):

> Q. But by selecting a subset of secondary channel signals, are you selecting a particular group of devices to respond to a single read or write request?
>
> A: I don't think so. Not in that situation. I think that that's specific to channel signal lines.
>
> ***
>
> Q. So you don't think this paragraph [15:37-45] has anything to do with grouping devices into different ranks?
>
> A: ***I do not think that this paragraph specifies how ranks are selected or enabled***.

178. Dr. Wolfe also clarified that the phrase "independent banks" in the passage and relied on by Petitioner (Pet. 28-29, 63) does not refer to different ranks, but "page registers which can be activated corresponding to different addresses." EX2103, 203:11-25 (objections omitted).

179. He confirmed that this disclosure in the preferred embodiment "simply has to do with the number of independent banks that are open at a time," not selecting or enabling a group of memory devices constituting a "rank." *Id.*, 203:15-20. (Here, "banks" means memory arrays in a DDR device and each bank has a corresponding page register. *See* EX2103, 47:16-48:15; EX1033, p.414).

180. The Petition also argues that EX1035, 6:15-19 discloses "selecting 'one' memory device and transmitting … corresponding signals to the selected memory device." Pet. 37, 53. But the disclosure in 6:15-19 simply reads "[i]n a normal memory read operation, buffer device 350 receives control, and address information from controller 310 via point-to-point link 320a and in response, transmits corresponding signals to one or more, or all of memory devices 360 via channels 370." To the extent that Petitioner argues that a single ×16 memory

device can form one rank, as explained in Section VII.C.1, at the time of the invention, there were no known DDRx memory modules that were 16-bit wide or below and Petitioner has not provided any reason why a POSITA would have been interested in such a module.

181. A person of ordinary skill in the art would understand that even in JEDEC-style memory systems, address bits are distinct in function and organization from a "chip select signal." *See* EX1033, p.318 ("The busses in a JEDEC-style system are classified by their function and organization into *data, address, control,* and *chip-select* busses."); *compare* EX1029, 6 ("Chip Select: ... CS provides for external Rank Selection on systems with multiple Ranks.") *with id.*, 6 ("A0 – A15 ... Address Inputs: Provided the row address for Active commands and the column address and Auto Precharge bit for Read/Write commands to select one location out of the memory array in the respective bank."); EX1032, 4.20.4-6 to 4.20.4-7 (distinguishing between "SDRAM address bus" A0-A15 and "SDRAM chip select lines" S0-S3).

182. While address bits can be used in conjunction with chip-select signals (if they are used) to generate gated chip select signals (*e.g.*, EX1001, Fig.

10A), they are still different signals from chip-select signals. The claims also differentiate "address signals" and "chip-select signals" by separately reciting "row/column address signal, bank address signals" on the one hand and "chip-select signal" on the other hand. *See* Pet. ix, [16.c.i]. Perego-422's reference to address bits does not disclose or suggest reading or writing in response to a chip-select signal.

D. Perego-422's "logic element" Does Not Receive the Claimed "set of input signals" [16.c.i]/[16.c.ii]

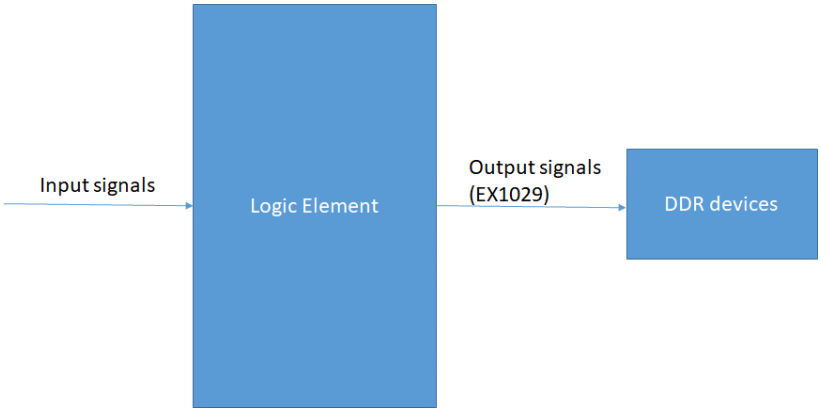
183. Claim 16 requires that a DDR DRAM module including a "logic element receiving a set of input signals from the computer system, the set of input signals comprising at least one row/column address signal, bank address signals, and at least one chip-select signal." EX1001, p. 44, 3:18-22. Perego-422 does not disclose or suggest this limitation.

1. The relied-on JEDEC standards do not fill the gaps in Perego-422's disclosures

184. Petitioner asserts that this limitation is inherently taught in Perego-422 based on the JEDEC DDR DRAM standards (EX1029) and JEDEC DDR registered DIMM ("RDIMM") standard (EX1032). I disagree.

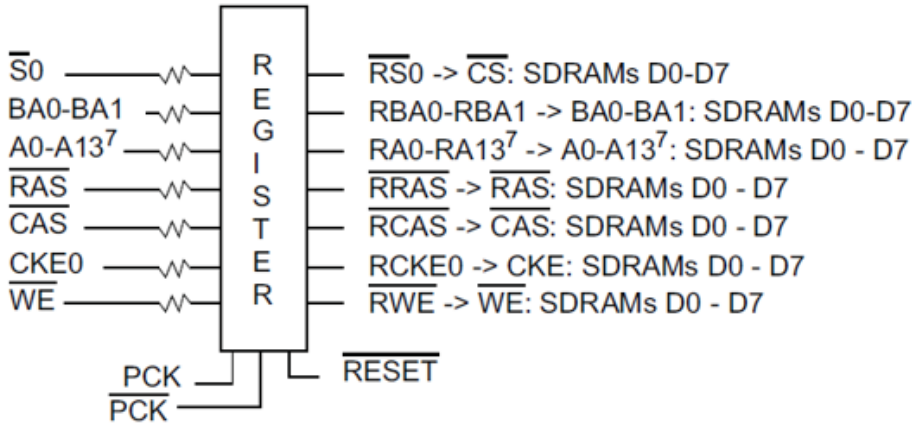
185. First, Petitioner relies on EX1029 to assert that the logic element receives "signals associated with a read or write command per the JEDEC standard." Pet. 35-36 (citing EX1029, 6, 49). EX1029 is a JEDEC specification for DDR2 SDRAM memory devices. Where there is a buffer that can "translate protocols employed by controller … to the protocol utilized in a particular device implementation," (Perego-422 10:63-67), EX1029 provides information on the C/A signals that are output from the buffer and transmitted to DDR2 devices, but not information on signals received by the buffer. EX2103, 35:12-23 (Dr. Wolfe stating "Exhibit 1029 describes the address and control protocols ***for DDR2 DRAM devices*** at the time."). I also understand and agree with Dr. Wolfe that not every utilization of a DDR2 device requires that a logic element or a buffer receive the signals specified in EX1029. EX2103, 113:12-113:23 (Dr. Wolfe explaining that bank address signal must be received by the DRAM "[i]n order to use a DRAM chip such as the kind that's described in Exhibit 1029," but "[n]ot in every utilization of a DDR2 device" is it required for a logic element to receive the bank address signal). As I have noted earlier, Perego-422 utilizes addresses to select channels. *See* Perego, 14:63-67, 15:37-40, 10:20-36.

186. The Petition acknowledges that it relied on signals "for DDR memory devices," instead of those received by the alleged logic element 540. Pet. 37 (referencing address lines RQ "for DDR memory devices"). That is, Petitioner's citation to EX1029 at most shows that if Perego-422's memory module used JEDEC-compliant DDR2 devices, those devices may receive certain signals, not that the separate "logic element"—in particular the "Request & Address Logic 540" of Perego-422 would receive the recited input signals from the computer system. *See* Pet. 33 (mapping 540 to "logic element") and illustration below.



187. Second, for this element, the only module-level specification Petitioner cites is the JEDEC 21C standard for DDR RDIMMs, EX1032. Pet. 37; EX1032, 4.20.4-1. But Petitioner provides no evidence that Perego-422 is

compatible with this cited specification. The RDIMM specification requires a register that registers C/A signals including RAS, CAS, WE, chip-select and address signals, as depicted below. EX1032, 4.20.4-11.



188. Perego-422 expressly distinguishes its buffers containing the logic element 540 from those "disposed on the conventional DIMM module" that were "used to buffer or register control signals such as RAS and CAS, etc. and address signals." EX1035, 6:27-30. A person of ordinary skill in the art would understand that "conventional DIMM module" refers to JEDEC-style modules. *See*, *e.g.*, EX2052, Figs. 1, 8 (a person of ordinary skill in the art would recognize the referenced "conventional" DRAM system is a JEDEC-style system); *id generally* (distinguishing Rambus-style DIMMs with JEDEC-style conventional DIMMs). Because the RDIMM specification (the cited portion of JEDEC 21C

specification) specifies structures and operation of conventional DIMM modules and because Perego-422 does not use such conventional registered DIMMs (RDIMM), EX1032 is not on point.

189. I understand that Petitioner asserts that in order "to translate protocols," the signaling received from the computer system would inherently include the "at least one row/column address signal, bank address signals, and at least one chip-select signal." *See* Pet. 38. I disagree. In fact, by disclosing use of translation protocols to generate the output signals sent to the memory devices (EX1035, 10:63-67), Perego-422 contemplates that the input signals would be different from the output—otherwise there would be no need for translation.

190. Perego-422's packetized protocol relied on by the Petition differs from that described in EX1029 and EX1032 in important ways. Perego-422 states that "[i]n a normal memory read operation, buffer device 350 receives ***control, and address information*** from controller 310 via point-to-point link 320a" (EX1035, 6:15-19, cited on Pet. 51-52); and such "control ***information*** and address ***information*** may be decoded" by circuit 540 before being supplied via interface 520 to the memory devices (EX1035, 13:54-59, Pet. 36). Notably,

Perego-422 does not describe the signals it receives as control and address "signals," but only as "information." *See* EX1035, 6:15-19, 9:50-57, 13:49-59.

191. Claim 16 requires input "signals," and not input "information." EX1012, 3:18-22 ("the logic element receiving a set of input signals from the computer system, the set of input signals comprising at least one row/column address signal, bank address signals, and at least one chip-select signal."). The patent specification consistently shows different lines, each dedicated to a particular type of signal, for connecting the memory controller to the logic element. *See* EX1001, Fig. 1A (lines CS_0, CS_1, A_{n+1}, Command Signals, BA_0-Ba_m), Fig. 1B (lines CS_0, A_{n+1}, Command Signals, BA_0-Ba_m), and descriptions at 6:54-63, 7:39-49; Figs. 2A, 2B, and 20:53-21:58; Figs. 3A, 3B, and 22:15-26.

192. These examples in the '912 patent do not reference packetized signaling or "bundling" the individually recited input signals. *Cf.* EX2103, 37:5-37:10 (Dr. Wolfe testifying that a common general definition of "packets" is "bundles of information that are sent at different times on the same wire"). I agree with Dr. Wolfe that there is a distinction between a "signal" and "information" that could be contained in a signal. EX2103, 61:15-23 (Dr. Wolfe

explaining that "[t]ypically, [a] signal would be something physical," while "information would be the knowledge contained in that signal."). While claim 16 does not recite specific I/O pins or wires, the presence or absence of those wires and pins provides insight into whether a particular signal is provided to or generated by a component.

193. Dr. Wolfe confirmed that JEDEC-compliant RDIMMs at issue in EX1032 do not feature the packetized protocol cited on Petition 36 (citing EX1035, 13:54-59, Figs. 4B, 5B). EX2103, 40:20-41:11; 28:8-16 ("Q. And in the – in the traditional DIMM, is the multiplex control and address information demuxed from the data? .... No, not in a traditional DIMM that it would be compliant with JEDEC Standard 21-C [EX1032]. It would not have that characteristic."); 39:12-16 (confirming that DRAMs compliant with EX1029 "do have distinct pins for A0 through A15"); *see also* EX2103, 29:20-30:23 (discussing Perego-422, 13:49-54 on Perego-422's ability "to extract the address and control information from the data" and Dr. Wolfe is unable to recall any JEDEC standard that extracts C/A information from data and "do[es]n't recall any JEDEC standard that [he] relied on as an exhibit for [his] declaration that

extracts the address and control information from the data"), 30:25-31:7 ("Q: And do you recall of any JEDEC standards you relied on in which control information and address information is decoded and separated from multiplex data? A: I don't recall that being in any of the JEDEC specifications that I relied on as exhibits to my declaration.") (objections omitted), 42:19-24 ("Q: For the JEDEC standards you relied upon, are you aware of any modules that actually used packetized signaling scheme that a [sic] Rambus used? A. For the JEDEC standards that I relied on as exhibits to my declaration, I'm not aware of any of them using a Rambus compliant signaling protocol."). That is, Perego-422 does not disclose or suggest that its element 540 receives from the computer system signals described in EX1029 or EX1032. *See also*, EX2100, 3-4 (RIMMs developed by Rambus do not have specific signals for bank address or chip-select signals, only column bus and row bus signals); EX2053, p.2 (EX2060, p.29 (no chip-select or enumerated address signals listed for "FBDIMM Channel Signals" received by the buffer); EX2051, pp.4-5 (no enumerated C/A signals received at the FBDIMM connectors; instead, the information is carried on the pins for the southbound lanes), EX2116, pp.3-4 (same).

194. Perego-422's point-to-point architecture follows the same signaling protocol as the point-to-point fully-buffered DIMM ("FBDIMM") architecture. EX1035, 9:50-57, 13:49-59. In the point-to-point FBDIMM architecture, the memory controller provides PCI-express like serial signaling over 10 differential signaling pairs. EX2114, pp.9-10 (showing serial signaling similar to PCI-Express from memory controller); EX2115, 1 (FBDIMM "replaces the shared parallel interface between the memory controller and DRAM chips with a point-to-point serial interface between the memory controller and an intermediate buffer"). Like Perego, FBDIMM receives serialized and packetized control and address information. *See* EX2116, pp.3-4 (no input pins assigned specifically for address signals, CAS_bar, WE_bar, RAS_bar, bank addresses or chip select signals; instead only "Primary southbound data" pins PS[9:0] and PS#[9:0]), p.6 (inputs to buffer AMB do not include row/column address signals, bank address signals or chip-selects even though the output to DRAMs does). Put another way, the signals transmitted from the buffer to the DRAMs can be generated by logic on the buffer based on information received from the computer system, instead of being received from the computer system. For instance, Dr. Wolfe

testified that in a packetized protocol such as Rambus's, "control and address data would be broken up into chunks ... 8 bits at a time, and sent as a sequence over a limited number of wires and then ***reconstituted on the module itself into individual signals***." EX2103, 18:5-18. He acknowledged that signals reconstituted by the logic element and transmitted to the memory devices are "not in the same packetized form that is transmitted over the logic channel." *Id.*, 22:9-23.

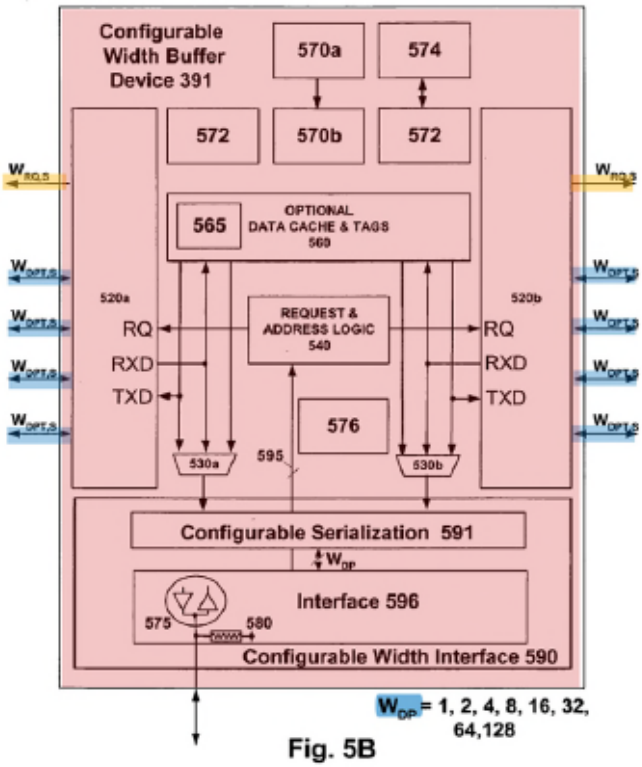


Fig. 5B

195. The "reconstituted" signals transmitted from the request & address logic 540 to the DRAMs are not the same as the "set of input signals" "from the computer system." Instead, those reconstituted signals cited by Petitioner are generated internally by the circuit, and not received by the logic element from the computer system, as required by [16.c.i.].

2. Perego-422 does not disclose a "chip select signal"

196. For reasons stated in Section VII.C.3, the Petition has also not identified any disclosure in Perego-422 of a "chip select signal" received by the buffer or the request & address logic 540. Instead, as noted above, the Petition cites the JEDEC standard for DDR2 SDRAM devices, EX1029, as disclosing the "at least one chip-select signal." Pet. 35-36. As explained above, that signal is what is output by the request and address logic 540 (if Perego-422 uses DDR2 memory devices), not what is received by the logic 540.

197. I also disagree that chip-select signals are inherently present because it is "associated with a read or write command per the JEDEC standard." Pet. 35-36; EX1003, ¶132 (citing EX1029, at 6, 49 n.2). The Petition relies on Perego-422's non-JEDEC compliant point-to-point configurations with

configurable widths. *See*, *e.g.*, Pet. 49 (for 16.c.iii, citing to 6:15-19 that specifically mentions "point-to-point link"); Pet. 31, 34, 56 (configurable width embodiment Fig. 5b); EX2103, 43:12-20 (a JEDEC compliant memory module does not ordinarily have a configurable buffer width); *see also* EX2100, 2-5 (no chip-select pins or signals for RIMMs). Perego-422 specifically contrasts the relied-on configuration with "conventional DIMM module," which a person of ordinary skill in the art would understand refers to JEDEC-style RDIMMs. EX1035, 6:27-33. Moreover, even in JEDEC-specified FBDIMMs, the buffer (AMB) does not receive the enumerated set of input signals—instead, it receives commands and write data on 10 pins on southbound lanes. *See*, *e.g.*, EX2060, p.29; EX2051, p.5; EX2116, pp.3-4. That is, there is no evidence that the identified buffer receives chip-select signals.

198. I understand that Micron's expert, Dr. Stone, has testified that chip-select signals can be produced locally. EX2059, 74:19-76:6 (discussing Fig. 4.5 of the Stone book (EX1043),[7] pointing to a 4-by-16 decoder in which "4 bits from the address go to the decoder, and they're used in this case, in this example,

[7] EX2059, 71:25-72:2, 72:13-16.

to create chip selects. 4 bits give you 16 possibilities, and that's how we select them. In that case, I would say this chip select is produced on the board [module]. It's produced locally.").

199. In other words, co-Petitioner's expert in the district court action has agreed that providing chip-select to a memory device does not mean that chip-select signals are received from the computer system (memory controller). Instead, they can be generated locally, *e.g.*, via a buffer like Perego-422's that can translate the protocols used by memory controllers to protocols used by memory devices.

E. Perego-422 Does Not Disclose [16.c.iv]

200. Element 16.c.iv recites "wherein the circuit further responds to a command signal and the set of input signals from the computer system by selecting one or two ranks of the first number of ranks and transmitting the command signal to at least one DDR memory device of the selected one or two ranks of the first number of ranks." Perego-422 does not disclose this limitation for two independent reasons: (1) it does not disclose "selecting one or two ranks …." and (2) it does not disclose a circuit that "responds to a command signal"

and "transmit[s] ***the*** command signal to at least one DDR memory device of the selected … ranks."

1. Perego-422 does not disclose selecting ranks in the claimed manner

201. The Petition cites 15:37-40 and 6:15-19 for alleged disclosure of rank selection. Pet. 53-55. For reasons stated in Section VII.C.3, those passages do not disclose selecting ranks in the claimed manner.

202. Dr. Wolfe, for example, testified that the passage in 15:37-40 does not specify rank selection or enablement. *See* EX2103, 202:8-204:10 (objections omitted):

> Q. But by selecting a subset of secondary channel signals, are you selecting a particular group of devices to respond to a single read or write request?
>
> A: I don't think so. Not in that situation. I think that that's specific to channel signal lines.
>
> ***
>
> Q. So you don't think this paragraph [15:37-45] has anything to do with grouping devices into different ranks?
>
> A: ***I do not think that this paragraph specifies how ranks are selected or enabled***.

203. And I agree with Dr. Wolfe that the phrase "independent banks" in 15:40-45 does not refer to different ranks, but "page registers which can be activated corresponding to different addresses." EX2103, 203:11-25. This is consistent with Rambus's designs, which was to maximize the number of independent banks that can be accessed in parallel at a given time. *See* EX2052, p.23 (contrasting Rambus Direct RDRAM memory systems with traditional JEDEC-style systems and noting that one difference is the number of independent banks each system could have).

204. As to EX1035, 6:15-19, it provides "[i]n a normal memory read operation, buffer device 350 receives control, and address information from controller 310 via point-to-point link 320a and in response, transmits corresponding signals to one or more, or all of memory devices 360 via channels 370." This passage does not say anything about selecting a rank.

205. The Petition does not cite other disclosures of "ranks" or selecting ranks in Perego-422, and provides no explanation as to how "grouping memory devices into multiple independent target subsets" discloses "rank." The Petition

therefore has not established that Perego-422 discloses "ranks" or selecting ranks.

2. Perego-422 does not disclose a "circuit" that "responds to a command signal and the set of input signals" by, *inter alia*, "transmitting *the* command signal to at least one DDR memory device" of the selected rank(s)

206. Claim 16 requires a "circuit comprising a logic element and a register" in which the logic element receives specific input signals from the computer system and "wherein the circuit further ***responds to a command signal*** and the set of input signals from the computer system by selecting one or two ranks of the first number of ranks and ***transmitting the command signal*** to at least one DDR memory device of the selected one or two ranks of the first number of ranks." Pet. ix-x. Because Pergo uses a buffer to translate the received serialized packets into signals used by DDR2 devices, whatever signals received are not the signals sent to the DDR2 devices. This is different from the '912 specification's way of generating additional chips-select signals that does not involve decoding and extracting C/A information from multiplexed packets.

207. Petitioner maps the claimed circuit to the combination of Perego-422's request & address logic 540 ("logic element") and registers 597f-m

("register"). Pet. 33-35 (citing EX1035, 6:12-27, 13:54-59). Petitioner contends that [16.c.iii] is met because "[i]n a normal memory read operation, buffer device 350 receives control, and address information from controller 310 via point-to-point link 320a and in response, transmits corresponding signals to one or more, or all of memory devices 360 via channels 370." Pet. 51-52 (citing EX1035, 6:15-19).

208. Petitioner incorrectly assumes that Perego-422's circuit registers control/address signals are "similar to the standard registered modules of the time." Pet. 34-35 (citing EX1032). The standard RDIMMs do not receive or translate packetized input protocol to signaling protocol used by DDRx devices, as in Perego-422. EX1032, 4.20.4-10 (depicting register of a JEDEC-standardized RDIMM, which shows the register block (i.e., the "circuit") receiving control signals such as RAS, CAS, WE, and outputting registered control signals in response); *see* Section VII.D.1; EX2103, 29:20-30:23, 30:25-31:7, 42:19-24 (Dr. Wolfe unable to identify any JEDEC standards that he relied on that used the kind of packetized signaling protocol relied on in the Petition).

209. Indeed, Perego-422 distinguishes its buffer from the registers of a conventional RDIMM. *See, e.g.*, EX1035, 6:27-30 (distinguishing its normal memory operation and what happens in standard RDIMMs "by way of comparison").

> With further reference to FIGS. **3**A and **3**B, buffer device **350** transceives and provides isolation between signals interfacing to controller **310** and signals interfacing to the plurality of memory devices **360**. In a normal memory read operation, buffer device **350** receives control, and address information from controller **310** via point-to-point link **320***a* and in response, transmits corresponding signals to one or more, or all of memory devices **360** via channels **370**. One or more of memory devices **360** may respond by transmitting data to Buffer device **350** which receives the data via one or more of channels **370** and in response, transmits corresponding signals to controller **310** via point-to-point link **320***a*. Controller **310** receives the signals corresponding to the data at corresponding ports **378***a*–**378***n*. In this embodiment, memory subsystems **330***a*–**330***n* are buffered modules. By way of comparison, buffers disposed on the conventional DIMM module in U.S. Pat. No. 5,513,135 are employed to buffer or register control signals such as RAS, and CAS, etc., and address signals. Data I/Os of the memory devices disposed on the DIMM are connected directly to the DIMM connector (and ultimately to data lines on an external bus when the DIMM is employed in memory system **100**).

(EX1035 at 6:12-30)

210. In Perego-422's packetized protocol, the control/address information transmitted from the computer system is "reconstituted" on the buffer device before being transmitted from the DRAMs. EX2103, 18:5-18;

EX1035, 10:59-67 (buffer "to translate protocol employed by controller … to the protocol utilized in a particular memory device implementation"), 13:49-59 (buffer extracting C/A information from data by *e.g.*, decoding and separating C/A information from multiplexed data).

211. Because this translation transforms serialized signals to ones suitable for use by DDR2 devices, a person of ordinary skill in the art would understand that the command signal received by the buffer device for, *e.g.*, a read/write operation, is not the same command signal outputted to the DDR memory devices. *Id.* Hence, Perego-422 does not disclose any "circuit" designed to "respond[] to a command signal" and "transmit[] ***the*** command signal to at least one DDR memory device" in the selected rank(s) because the command signal that was received by the buffer is not the same as the command signal that was sent by the buffer.

F. Perego-422 Does Not Disclose [16.d.i]

212. There is no substantial evidence that circuit 570a-b is operatively coupled to the register (16.d.i). The Petition argues that Perego-422, 12:65-13:5, teaches that the clock circuit 570a-b provides internal clock and synchronizing

signals to the circuits within the buffer device. Pet. 59-60. But the cited disclosure merely discloses "generat[ing] internal synchronization clock signals having a predetermined temporal relationship" without disclosing to which circuits in the buffer device the signal is provided. EX1035, 12:65-13:5.

213. Petitioner assumes that because CTM and CFM signals are exchanged with the host at the interface 590 and interface 590 includes a register, the clock circuit would be operatively coupled to the register. Pet. 59-60. But I have not seen any evidence that those CTM/CFM signals are sent or received by the register.

214. Instead, the Petition merely asserts that the register "'transceives and provides isolation' of address, command, and data signals between the memory controller and the memory devices on the module…," without any reference to clock signals. Pet. 34. As is clear from Fig. 4B shown on Pet. 60, the clock signals are transmitted on different lines than control/address lines RQ or data lines DQ. EX1035, 9:43-45 ("Signal lines of channels 415a and 415b include control lines (RQ), data lines (DQ) and clock lines (CFM, CTM).");

9:50-53 (noting RQ lines are for transporting control information and address information).

215. Thus, the fact that the register is coupled to RQ and DQ lines does not shed light on whether the register is also coupled with clock lines or the clock circuit 570a-b. In other words, there is no substantial evidence that Perego-422 discloses a PLL that is operatively coupled to the register. Pet. 59-60 (cited expert declaration merely parrots the same conclusory statement).

216. Petitioner may argue that the limitation would be obvious by "us[ing] the functionality of Amidi's register in Perego-422 to synchronize the incoming address and control signals with the local clock signal …." Pet. 35. But that does not explain why the register should be operatively coupled with the clock signals of Perego-422: for instance, the logic element 540 which receives, translates and outputs the address and control information to the DDR devices is already allegedly coupled to the clock signals to synchronize the address/control signals with the clock signals. Pet. 35-36, 58-59. Petitioner does not explain why the clock circuit should also be coupled to the register for that

synchronization. Thus, Petitioner has not shown that 16.d.i is disclosed or rendered obvious by Perego-422 alone or in combination with another reference.

VIII. PEREGO-422 AND AMIDI DO NOT RENDER OBVIOUS CLAIM 16

217. I understand that Ground 2 adds Amidi to provide a second way of rank multiplication. But the addition does not cure the deficiencies that I noted above for Ground 1. For instance, the combination would still have no need for rank multiplication (or rank in general) given how Perego-422 selects channels for memory operations. As another example, the combination would still have no recited set of input signals because it uses addresses to select channels and not chip-selects. As yet another example, because Perego-422 still operates a buffer that translates serialized incoming request packets to signaling protocols used by DDR2 devices, the combination still does not send "the" command signals. Below I provide some examples of the deficiencies.

A. Petitioner's Combination Still Relies on 16-bit Wide Single-Device Implementations

218. Claim 16 requires that "the command signal [be] transmitted to only one DDR memory device at a time." EX1001, p. 44, 3:42-43. Petitioner only asserts that the limitation is met if each rank has a single device. *See, e.g.*, Pet.

61-62 ("Perego discloses 'wherein the command signal [e.g., for a read or write command per the JEDEC standard, EX1029,6,49] is transmitted to only one DDR memory device at a time,' … in an implementation like the one illustrated below, where each memory device has a 'dedicated channel.'") and Fig. 4B (reproduced below as modified by Petitioner); *id.*, 62-63 ("Consequently, when the width of one memory device is equivalent to that of the module, the command received at a specific time is transmitted to only one DDR memory device at a time."). But as explained in Section V above, each "rank" is understood to have two or more memory devices; and claim 16 requires sending a command to a single device at a time even though there are multiple devices in each rank. For this reason, Ground 2 (Perego-422 in view of Amidi) fails to disclose Elements [16.e].

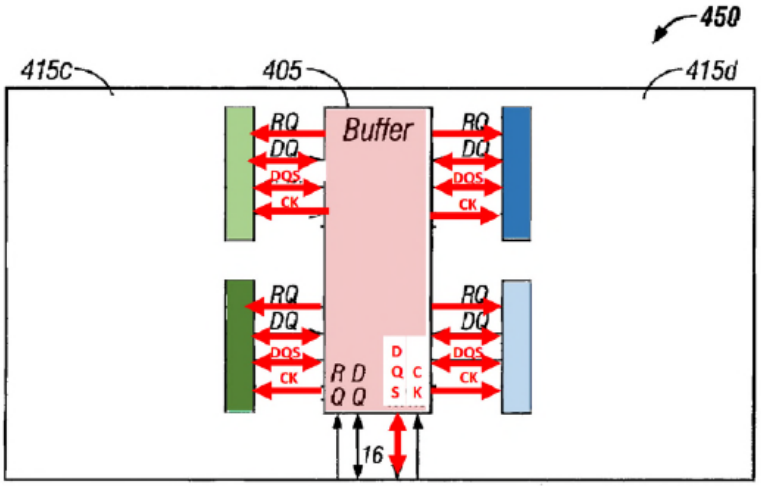


FIG. 4B

219. Even accepting for the sake of argument Petitioner's construction that a "rank" could theoretically be composed of a single memory device, I note that Perego-422 does not disclose a memory module with only a single device in each "rank." As noted above, Petitioner assumes that each channel in modified Figure 4B corresponds to a rank. *See* Pet. 61-62; EX1003, ¶124; *supra*, ¶130; *supra* VII.B. That is not supported by Perego-422's specification. The buffer circuit in Figure 4B communicates with the memory devices via four channels 415a-415d, either in a paired arrangement (one pair, 415c/415d, another pair 415a/415b), or in a simultaneous arrangement (all four channels simultaneously). EX1035, 9:26-33, 10:22-36. In the paired arrangement,

"channels 415c and 415d are ***routed in parallel*** with channels 415a and 415b." *Id.*, 10:23-36. In the simultaneous arrangement, "channels 415a and 415b may operate ***simultaneously*** with channels 415c and 415d." *Id.*, 10:32-33.

220. Even under Petitioner's construction, neither of these arrangements allows for the possibility of single-device ranks. Petitioner contends that a person of ordinary skill in the art would understand the term "rank" to mean "an independent set of one or more memory devices on a memory module ***that act together in response to command signals***, including chip-select signals, to read or write the full bit-width of the memory module." Pet. 12. Perego-422 would inform a person of ordinary skill in the art that, in the paired arrangement, the devices connected to channels 415c/d correspond to one "rank" because they are "routed in parallel," that is, the memory devices would be understood to "act together in response to command signals." For similar reasons, a person of ordinary skill in the art would understand that the devices connected to channels 415a/b correspond to another "rank." Thus, in the paired arrangement, Perego-422's Figure 4B illustrates two ranks: one corresponding to memory devices connected to channels 415c/d, the other corresponding to memory devices

connected to channels 415a/b. Likewise, a person of ordinary skill in the art would understand that the simultaneous arrangement corresponds to a one-rank module, because all the memory devices connected to channels 415a-d "act together in response to command signals."

221. Applying these principles from Perego-422's express teachings to Petitioner's single-device construct, a person of ordinary skill in the art would understand Petitioner's modified Figure 4B to correspond to either a two-rank module, with ***two devices in each rank*** (paired-channel arrangement) or a one-rank module, with ***four devices in the rank*** (simultaneous-channel arrangement).

222. Additionally, as noted for Ground 1, Perego-422 does not teach sending commands to only one device associated with a particular channel. Thus, Petitioner are relying on implementations where for the majority of the operation, the system was not even enabled for operating as claimed.

223. I also incorporate discussions in Sections VII.B and VII.C.

B. Petitioner's Combination Does Not Disclose a "logic element" that Receives the Claimed "set of input signals" [16.c.i]

224. Ground 2 still relies on Perego-422 for the limitation that requires the "logic element" to receive the enumerated "set of input signals." *See* Pet. 35-38 (analysis of Element [16.c.i]); *id.*, 47-48 (arguing that "[t]o the extent one might argue Amidi does not disclose that the 'logic 48 element' receives the claimed 'bank address signals' as part of the 'set of input signals,' Perego, alone or in combination with Amidi, teaches this"); *see also id.*, 102 (conceding "Amidi is used here only as a secondary reference with respect to a few specific limitations"). As explained above, Perego-422 does not disclose those elements; as such addition of Amidi would not cure the deficiencies, and Ground 2 fails.

C. Petitioner Has Not Shown Why A POSITA Would Have Modified Perego-422 To Include Amidi's Ranks

225. Petitioner's motivation-to-combine arguments do not support the proposed combination. Petitioner does not propose changing Perego-422's fundamental operation. Nor does assert that there would be benefits by deviating from Perego-422's use of an address bit—not a chip-select signal—to select the target memory devices for operation. EX1035, 10:23-33. Finally, Petitioner's motivation-to-combine arguments based on supposed cost-effectiveness of using

lower-density DRAM are conclusory, unsupported and contradicted by the testimony of its own declarant.

226. As explained in Section VII.A, Perego-422 does not need rank multiplication because it can use address bits to select any channel of choice. *See* EX1035, 14:63-65, 15:37-40, 10:20-36. Amidi does not change that conclusion because, according to Amidi, the reason to utilize rank multiplication is to address the problem of the limited number of chip-select signals that memory controllers could provide to a standard memory module. EX1036, [0010]-[0011] (describing as the "primary purpose of the present invention" resolving the need for "a transparent four rank memory module fitting into a memory socket having two chip select signals routed); [0036] (Amidi "allows the four rank memory modules to communicate with a memory socket having only two chip select signals routed."); [0041] ("CPLD 410 allows a system having a memory socket with only two chip select signals routed to interface with a four rank memory module where typically a two rank memory module couples with the memory socket.").

227. Perego-422, on the other hand, increases memory capacity "[b]y incorporating more channels and additional memory devices." EX1035, 10:26-31. Its point-to-point architecture allows further increase in capacity by adding more modules. *Id.*, 10:36-39, 3:31-47, 5:39-44, 6:62-64; *see also* EX2114, pp.13, 17 (noting that FBDIMM's point-to-point configuration allows more DIMMs to be used per memory controller and hence solves the capacity issue).

228. In contrast, Perego-422 uses addresses to select the desired channels. EX1035, 14:63-65, 15:37-40, 10:20-36. And the number of modules is limited by the number of ports the system 300 has, not the number of chip-select signals that can be provided by the computer system. *See* EX1035, 5:8-15. In other words, Perego-422 just does not have the same problem as prior art that utilized rank multiplication—it does not rely on chip-select for channel selection and therefore its operation is not limited by the number of chip-select signals that the memory controller can send. It has no need for rank multiplication.

229. Petitioner asserts that both Perego-422 and Amidi teach that the module can "hide" the type of memory devices actually used from the memory

controller, i.e., that "a memory module can be configured to present the system memory controller with memory device configurations that are different from the actual memory devices used." Pet. 23 (citing EX1035, 10:56-67, EX1036, [0011]). But the transparency referenced in Perego-422 relates to the type of memory device (*e.g.*, Rambus DRAM versus DDR2, DDR or SDRAM), (EX1035, 10:54-63), whereas the transparency in Amidi relates to the bit-width and density of the memory device (*e.g.*, x8 versus x16, 512Mb versus 1Gb) (EX1036, [0012]). That is, unlike Amidi, Perego-422 does not attempt to hide its number of channels from the controller. Instead, Perego-422 teaches expressly that its channels can be divided into addressable subsets and be selected using address bits. EX1036, 14:63-65, 15:37-40. The transparency in Perego-422 is the signaling protocol, not the number of channels (or ranks). EX1036, 10:59-67 (using buffer to translate signaling protocols). Thus, a POSITA would not look to Amidi for modification because Perego-422 just does not have the same issue as Amidi and a desire to hide the DRAM technology type would not lead one to multiply ranks.

230. Amidi therefore does not change the fact that Perego-422 has no need for rank multiplication.

231. The Petition also does not explain how Perego-422's system is to provide the required chip-select signal to Amidi's CPLD (*see* EX1036, [0043] (CPLD utilizes two chip-select signals for rank activation)) in the combined system. Nor does Petitioner explain how a system that does not conform to the concept of "rank," such as Perego-422's, would inherently provide such a chip-select signal. *See* EX1035 *generally* (describing secondary channels, but not ranks); *see also* EX2103, 202:8-204:10 (discussing 15:37-45, "independent banks" mentioned there relates to page registers on a memory device, not ranks); 95:20 (one page register per bank).

232. Petitioner also fails to address that Perego-422 and Amidi employ different topology and signaling protocol. Perego-422 (a Rambus invention) emphasizes its ability to "translate protocols employed by controller 310 to the protocol utilized in a particular memory device implementation," *e.g.*, to translate between a Rambus controller protocol and a DDR DRAM protocol. EX1035, 10:54-67. For example, as Dr. Wolfe explained, "[t]he Rambus

DRAM memory modules used a packetized communication scheme that used a narrower communication channel than the most common other DIMMs at the time." EX2103, 13:7-12. According to Dr. Wolfe, in the Rambus protocol, the computer system "provide[s] bundles of information that could include control, address or data sharing the same channel at that time." *Id.*, 40:20-41:4. This information is then "reconstituted" by a logic element on the memory module. EX2103, 22:9-23, 18:5-18, 18:19-19:9, 21:8-17. For example, Dr. Wolfe testified that in this protocol, "control and address information would be sent along a relatively narrow channel as a sequence of packets and then reconstituted into individual signals by the logic functions on the -- within the Rambus chips." *Id.*, 19:3-9. He further explained that, in the Rambus modules, "the individual selection signals to select columns, rows, banks, and die would be reconstituted within some logic somewhere on the memory module." *Id.*, 19:15-22. In other words, the output signals from the logic element "is not in the same packetized form that it is transmitted over the Rambus channel." *Id.*, 22:18-21.

233. Consistent with the Rambus approach, Perego-422 repeatedly emphasizes that its invention follows a similar packetized protocol. Petitioner

admits that Perego-422's "buffer device 350 receives control[] and address information from controller 310" via point-to-point link 320a. Pet. 49, 59 (citing EX1035, 6:15-19); EX1035, 5:6-15. To transmit this information over Perego-422's point-to-point links, Perego-422 teaches that "any multiplexed combination of control, address information and data intended for memory devices coupled to configurable width buffer device 391 is received via configurable width interface 590." EX1035, 13:49-54. Perego-422 further explains that such "control information and address information may be decoded and separated from multiplexed data and provided on lines 595 to request & address logic 540 from interface 596," and [t]he data may then be provided to configurable serialization circuit 591." Figs.5B, 4B. Such a protocol differs from the JEDEC-style signaling used by Amidi. EX2103, 29:20-30:23, 30:25-31:7, 42:19-24 (Dr. Wolfe was unable to identify any JEDEC standards that he relied on that used the kind of packetized signaling protocol relied on in the Petition). That is, Perego-422 and Amidi are also incompatible in their signaling and architecture.

D. Petitioner's Reasons to Combine Are Deficient

234. Petitioner also argues a POSITA would have combined Amidi and Perego-422 to "lower the cost and increase upgrade flexibility of the memory modules." Pet. 23. Petitioner contends this is supported by Perego-422's disclosure of a "backwards-compatible" buffer device, which allegedly provides the flexibility to upgrade a memory system by employing new-generation memory devices on a system with a conventional memory controller, or vice versa. *Id.*, EX1035, 6:34-43. That, however, is a different problem than the one rank multiplication tries to solve (which is to have more numbers of physical ranks than supported).

235. Petitioner also presents no evidence to justify its economic rationale for implementing rank multiplication on Perego-422's system. For example, Petitioner argues that a POSITA would have been motivated to increase the capacity of a memory module "by using four ranks of low density (inexpensive) x16 memory devices in place of one rank of high capacity (expensive) x8 memory devices" given the "then-current trend to increase the data width of the memory devices." Pet. 39. But Petitioner provides no historical data at the time

of Perego-422's invention to substantiate this trend. Dr. Wolfe admitted at deposition, the cost difference between x8 and x16 devices for a given density "depends on the market at the time." EX2103, 91:13-15.

236. Dr. Wolfe's testimony further contradicted Petitioner's argument following the supposed "trend at the time of Perego's disclosure," a POSITA would have known that "another option to double the capacity of the one-rank module to 2Gb would be to use wider lower-density memory devices, such as four 16-bit wide 32Mbx16 memory devices" instead of four 8-bit wide (64MB) memory devices. Pet. 41. For example, Dr. Wolfe testified that ordinarily, 64MBx8 is ***cheaper*** than the 32MBx16, contrary to Petitioner's conclusory assertions that x8 devices are "expensive" and x16 devices are "inexpensive." Pet. 37. There is thus no substantial evidence that using four 32Mbx16 DDR2 would have saved cost over two 64Mbx16 DDR2, or that it would not have been more cost effective to use two 128Mbx8 device. *Cf.*, EX2103, 91:25-92:2 ("Q. So initially 64Mbx8 is actually cheaper than the 32Mbx16? A. It's ordinarily what happens.")

237. Petitioner thus has not explained how Amidi would confer the "flexibility" Perego-422 seeks to achieve, let alone square the two incompatible approaches to increasing memory capacity and/or bandwidth.

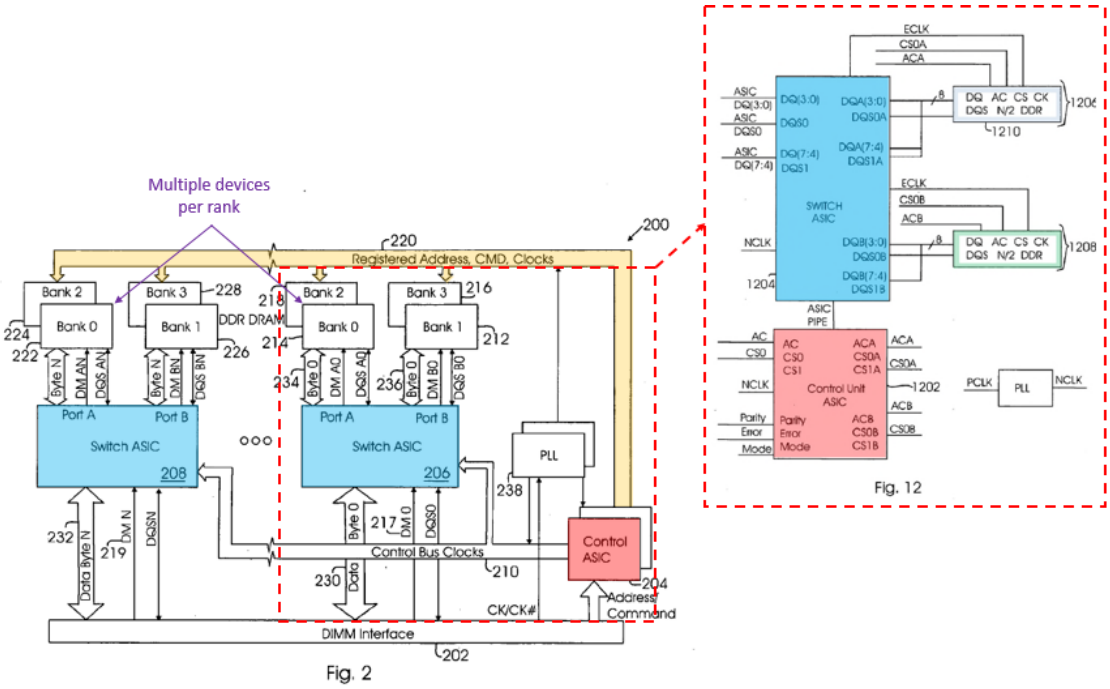
IX. ELLSBERRY DOES NOT RENDER OBVIOUS CLAIM 16

238. The Petition alleges that the Board previously "found that each of Ellsberry's multiple (M) data groups simultaneously output or receive one byte (n=8 bits), thus acting on the full bit width (N=Mxn) of the module." Pet. 74. That is, the Board has found that in Ellsberry, multiple devices act together to output the full bit width of the memory module, and under Petitioner's own definition, those multiple devices would constitute a single rank. *See* Pet. 12 (Petitioner's proposed definition for "rank").

239. The Petition then points to Ellsberry's Figure 12 to argue that Ellsberry could be implemented as single-device ranks. *See*, *e.g.*, Pet. 75 (arguing that "Ellsberry discloses a memory module which is eight bits wide and has two 8-bit wide ranks…."). Pointing to [0021] and [0030], Petitioner argues that Ellsberry allegedly "teaches a POSITA that a memory module can include

only a single data group having a data buffer and corresponding memory devices." Pet. 76. That is incorrect.

240. Although Ellsberry describe Figures 10-13 as illustrating "different configurations of memory modules (e.g., DIMMs) that can be built" using its disclosures, (EX1037, [0021]), a POSITA would not understand this to mean that Figures 10-13 each illustrate a memory module, but that they instead each depict a different configuration for one data group of the memory module.



(EX1037, Fig. 2 as compared to Fig. 12)

241. Figure 2 of Ellsberry illustrates "Data Group 0 through Data Group N" being provided "simultaneously." EX1037, [0030]; *see* annotation above. Each data group is associated with a memory device. That is, each "rank" of Ellsberry would include multiple data groups and hence multiple switch ASICs and the associated memory devices in each rank. *Id.*, Fig. 2 (showing two each of "Bank 0" through "Bank 3" with the rest (N=2 through N-1) omitted for simplicity); *see also* [0035] (referencing memory banks coupled to switches 206 and 208, implicating multiple data groups and hence multiple devices per full-bit-width of the memory module). Figure 2, however, does not provide details on how each switch ASIC is connected to the different memory banks, and that is where Figures 10-13 come in to provide that detail. Hence, a person of ordinary skill in the art would view Figures 10-13 as depicting the connection in each data group, not that it depicts a memory module of a single data group.

242. This conclusion is consistent with other parts of Ellsberry. For instance, Figure 6 of Ellsberry illustrates "four banks of five hundred and twelve

(512) megabits (Mbit) memory device 606, in a dual stacked configuration" that "appear to the system processor as 2 Gbit DRAM devices." EX1037, [0051].[8]

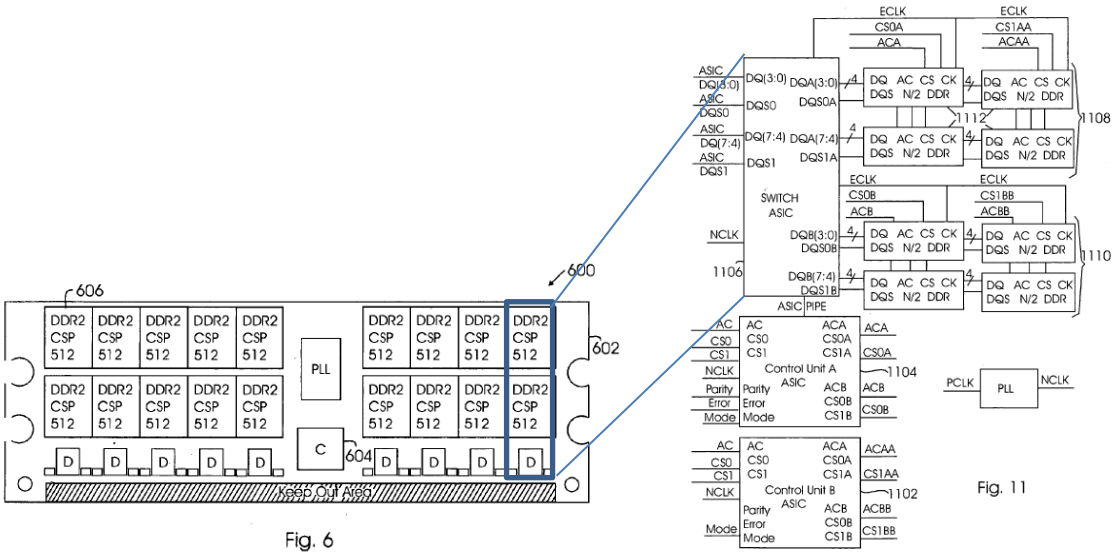


Fig. 6

Fig. 11

243. Figure 6 shows multiple data groups per rank. Ellsberry notes, however, the module illustrated in Figure 6 uses a configuration "similar to that illustrated in Fig. 11," *id.*, even though Figure 11, like Figure 12, shows only a single bank switch and one data group. Thus, a POSITA would understand that Figures 10-13 are used to illustrate how each data group and each data switch on the memory module can be implemented, and not how many data groups the

[8] In Figure 6, each side of the memory module has a control unit. EX1037, [0051].

memory modules are to have. *See, e.g.*, EX1038, 50 (noting "Figure 13 shows ***part of a memory module***"), 51, 57, 81; EX2061, 40 n.11 (agreeing with Samsung that "FIGS. 2, 5, and 13 of Ellsberry correspond to a 'First Embodiment' utilizing four ranks, each composed of nine 8-bit memory devices for a total bit width of 72").

244. As the Board previously noted, "in reference to Figures 10, 11, 12, and 13, Ellsberry states '[t]hese configurations employ the control unit and bank switch previously described,' ***thus relating these figures to the earlier-described control units and switches*** (including Figures 2, 5, and 6).'" EX1038, 77 (citing EX1037, [0052]). But each of these earlier-mentioned memory modules has multiple data groups and hence multiple devices per rank. *See* EX1037, Figs. 2, 5-6.

245. This understanding would also be consistent with the state of the art. Dr. Wolfe testified that he did not recall having ever "used a memory module with DDR or newer generations of DRAMs that's 16 bit wide or below" despite his 40 years of experience in the industry. EX2103, 146:2-12; *see also* 155:13-25 (not aware of any x8 memory modules using JEDEC compliant DDR or

DDR2 devices or any articles describing such modules). Another expert of Samsung, Dr. Subramanian, also testified that he could not recall any memory module—regardless of JEDEC compliance—that was/is 8-bit or 16-bit wide. EX2104, 258:3-259:7.

246. I understand that a reference is to be interpreted from the perspective of a person of ordinary skill in the art and their knowledge. The evidence is that at the time of the invention, there were no known eight-bit-wide memory modules with the claimed DDRx devices on them as Petitioner now contends. EX2103, 146:2-12, 155:13-25; EX2104, 258:3-259:7. Indeed, going from the industry-standard 64-bit module to 8-bit would be going against the alleged industry trend of increasing module data width (*i.e.*, "Go Wider, Not Faster"). EX1034, p.20-21.

247. It would also be going against Ellsberry's stated goal is to "reliably comply with industry standards." EX1037, [0009]; *see also*, *e.g.*, *id.*, [0050] (in connection with Figure 5: "[a]s a result of this architecture, the memory module presents a single electrical load to the system and is compatible with existing standards (e.g., JEDEC compatible, etc.)" and generally incorporating by

reference JEDEC standards). There is no substantial evidence that a JEDEC standard-compliant DDR module would have a single device per rank.[9] EX1029, for example, illustrates that the per-device bit width is x4, x8 or x16. *See* EX1029, pp.1-3; *see also* Pet. 69-111 (citing EX1029 DDR2 SDRAM specification repeatedly), Pet. 73 (citing EX1032 DDR SDRAM RDIMM Specification). EX1032, a module-level specification, requires 64- or 72-bit wide memory modules. EX1032, p.4.20-4.5 ("DIMM organization" "x72 ECC, x64"). This means that there are eight or nine x8 devices per rank. EX2103, 46:3-15 (a 64-bit wide memory module would have, respectively, sixteen x4 DRAM devices, eight x8 DRAM devices, and four x16 DRAM devices, per rank); EX2112, 1 (Micron stating "[a] rank is a data block that is 64 bits wide"); EX1090, 86:19-87:17 (Samsung corporate witness denies that a rank could include a single DRAM).

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[9] Co-Petitioner, Micron, acknowledges that the term "rank" "was created by JEDEC … to distinguish between the number of memory banks on a module as opposed to the number of memory banks on a component." EX2112, 1. Hence, claim 16 implies a JEDEC-style memory module with DDR devices whose full bit-width is x64 or x72 (ECC). *See* EX1032, p.4.20.4-5; EX2049, p. 6; EX2050, p.4.20.2-5.

248. Ellsberry also aims to "expand[] the memory capacity of a memory module." *Id.*, [0010], title. Reducing the number of devices per rank (to one device per rank) would reduce rather than expand the capacity of the memory module. Petitioner argues, however, that [0035] suggests "that the configuration can, but is not required to, be expanded to several data groups." EX1003, ¶217 (quoting EX1037, [0035]). But [0035] actually references ***two*** switch ASICs corresponding to ***two*** data groups:

> The control unit 204 then handles mapping the logical memory addresses it receives via the DIMM interface 202 to a corresponding bank for a particular memory bank coupled to the ***switches 206 and 208***. This same principal is expanded when implementing a wider memory bus formed by several data groups composed of a plurality of memory bank switches and the associated memories.

EX1037, [0035]; *see also id.*, [0030] (noting that "***a first data group*** … is received by ***bank switch 206*** while a ***second data group*** … is received by ***bank switch 208***"). Thus, Ellsberry teaches starting with at least two bank switches, consistent with Figure 2's illustration of Ellsberry's overall architecture. EX1037, Fig. 2.

249. Petitioner also points to Perego-422's configurable bit-width with a W_{DP} of 8 bits to suggest that a POSITA would design an 8-bit wide DDR DRAM module. Dr. Wolfe testified, however, that the memory device access width, W_A, not W_{DP}, corresponds to the number of bits "for a single read or write operation." EX2103, 55:4-57:4, 61:6-14. Given Petitioner's own definition of "rank," which references the set of memory devices that, in response to command signals, reads or writes "the full bit-width of the memory module," the 8-bit-wide W_{DP} disclosed by Perego-422 does not at all demonstrate that a POSITA would have constructed an 8-bit wide memory modules because W_{DP} is not the full bit-width of the memory module, as Dr. Wolfe confirmed. *Id.*; *see also* EX1035, 14:63-67 (selecting channels by using address bits).

250. Petitioner also argues that it would have been obvious to a POSITA to make a module with only a single data group, because allegedly a POSITA would have understood that such a module "would have been simpler to make and required fewer parts, leaving fewer error sources." Pet. 76. I disagree because nothing in Ellsberry suggests that it is concerned with such simplicity:

otherwise it would not be teaching ways to comply with JEDEC standards that have multiple devices per rank.

251. A POSITA would not have thought of constructing an 8-bit wide DDR memory module as Petitioner argues because it was simply not known or suitable for use with a computer system at the time, which was generally 32-bit or 64-bit wide. EX2103, 146:2-12, 155:13-25 (Dr. Wolfe unaware of any x8 memory modules with DDRx devices or any articles describing such modules); EX2104, 258:3-259:13 (Dr. Subramanian not aware of any x8 memory modules with DDR's on them).

252. Nor does it make technical or economic sense. If a single one-byte (8-bit) data group was indeed desired for simplicity and reduction of error, Ellsberry would/should just couple a 512Mbx8 or 1Gb/x8 device directly to the CPU and memory controller, without using a memory module at all. By coupling a memory device, instead of an 8-bit wide memory module, directly to the CPU, there would be no need for switch ASIC, control ASIC, multi-layer PCB and its complicated routing. The cost savings associated with eliminating these components (costly switch ASIC, control ASIC and PCB) and the resulting

simplification in design would more than offset the cost difference between a single 512Mbx8 and two 256Mbx8 devices or cost differences between a single 1Gbx8 and two 512Mbx8 devices. For instance, it was known that ASICs would require application-specific custom designs and PCB designs require balancing of mechanical and electrical properties as well as involving complicated signal routing. Thus, there would be no technical or economic reasons for a person of ordinary skill in the art to use a memory module having only two 256Mbx8 memory devices arranged in two ranks to mimic a 512Mbx8 device or a memory module having only two 512Mbx8 memory devices arranged in two ranks to mimic a 1Gbx8 device.

253. There is no substantial evidence that Ellsberry, aiming to be JEDEC compliant, discloses or suggests the use of single-device-per-rank memory modules. Nor is there any substantial evidence that a POSITA would have modified Ellsberry to arrive at such single-device-per-rank memory modules given Ellsberry's desire to expand capacity rather than shrink memory module capacity (reducing the number of devices per rank would reduce the memory capacity accordingly).

254. But Ground 3 relies on single-device-per-rank constructs. Without them, Petitioner does not show how element [16.e] could be met. Petitioner therefore has not shown that "the command signal is transmitted to only one DDR memory device at a time" when there are multiple devices per rank, as in Ellsberry.

X. NO SIMULTANEOUS INVENTION

255. I understand that Petitioner argues that alleged similarities between Ellsberry and/or Amidi/Perego-422 and the '912 patent is evidence of "simultaneous invention" supporting obviousness. Pet. 111. I disagree. The Board has considered and rejected the argument that Amidi renders obvious claim 16, which I understand that the Federal Circuit upheld. *See supra*, ¶¶45-55. Perego-422 does not solve the same problem as the '912 patent because it does not even need rank multiplication, as explained above. *See supra*, ¶¶138-150. As to Ellsberry, the Petition cites repeatedly to the JEDEC standard; but JEDEC-style DDR2 memory modules are 64-bit or 72-bit wide, resulting in eight or nine x8 DDR2 devices. *See* EX1032 (x64 or x72 module widths); *supra*,

¶¶245-247. Petitioner does not contend that Ellsberry could send command to just one DDR device in a multi-device rank.

* * *

I declare that all statements made herein of my knowledge are true, and that all statements made on information and belief are believed to be true, and that all these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Executed this 10th Day of August, 2023, in Austin, Texas.

Michael C. Brogioli, Ph.D.

APPENDIX A

Michael C. Brogioli, Ph.D.

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Rice University, Houston, Texas USA

Ph.D., Electrical and Computer Engineering, 2007

- Dissertation Topic: "Reconfigurable Heterogeneous DSP/FPGA Based Embedded Architectures for Numerically Intensive Embedded Computing Workloads."
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- Dissertation Topic: "Dynamically Reconfigurable Data Caches in Low Power Computing."
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Rensselaer Polytechnic Institute, Troy, New York USA

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Certificates

Harvard Business School, Boston, Massachusetts, USA

Certificate in Investment Portfolios with Alternate Investments, 2022

- Venture Capital, Growth Equity, Distress Investing, Private Debt, Hedge Funds, Portfolio Construction.

Professional Experience

Polymathic Consulting, TX USA
Managing Director **2011 - Present**
Founder and managing director of Polymathic Consulting, servicing clients ranging from early stage technology start-up endeavors to Fortune 100 and beyond. Clients turn to Polymathic for expansive, proven engineering, research and development, intellectual property and technical leadership to effectively advance their real world business needs.

IEEE and ACM Design Automation Conference, USA
Steering Committee
Conference Chair, Embedded Systems and Software Track **2016 - Present**
Design Automation Conference is the premiere technical conference and trade show specializing in Hardware, Software, Internet of Things, Embedded Systems and related Design Methodologies. Conference chair, responsible for the review, critique, and acceptance of academia and industry based publications in the areas of embedded systems, embedded software, and embedded system design.

Rice University, TX USA
Adjunct Professor, Electrical and Computer Engineering **2009 - Present**

Samsung Ex. 1102, p. 189
Samsung Electronics Co., Ltd. v. Netlist, Inc., IPR2023-00454

Professor of Ph.D. candidate level courses in wireless telecommunications, embedded computing software, embedded computing hardware, and software/hardware optimization in modern computing systems utilizing modern high level programming languages. Advisor of senior and graduate student based projects revolving around multi-core heterogeneous systems as they pertain to wireless telecommunications, medical and video.

University of Texas, Austin, TX USA
Guest Lecturer, School of Engineering **2021 - Present**
Guest lecturer in "Legal Issues and Technology Management", on subjects relating to technology, management, financial and fund raising matters, technology transfer, and certain legal issues. Students are primarily comprised of those with existing degrees, and a number of years of industry experience.

RISC-V Foundation, Berkeley, CA USA
Technical Committee **2018 - Present**
RISC-V is an open CPU instruction set architecture (ISA) based on established reduced instruction set computing (RISC) principles. The RISC-V Foundation is a non-profit consortium chartered to standardize, protect, and promote the free and open RISC-V instruction set architecture together with its hardware and software ecosystem for use in all computing devices.

Freescale Semiconductor, TX USA
Chief Architect, Senior Member Technical Staff **2009 - 2011**
Technical architect of Freescale's DSP compilers and related technology. Responsible for management of technology, engineering roadmaps, design lead on compiler infrastructure and optimizations (high level and low level), next generation ABI definitions and next generation architecture solutions. Technical lead on multi-year engagement with processor architects in design of next generation DSP cores. Developed software infrastructure for migrating OEM competitor software stacks to Freescale solutions, tools generation, software packages, migration strategies and white papers. Technical lead on Tier-1 OEM customer relationships, evaluations of 3rd party technologies for potential partnerships and acquisitions, led various university research collaborations on behalf of Freescale. Development and deployment of internal software engineering policies and practices.

Freescale Semiconductor, TX USA
Senior Compiler Engineer V
High Performance Compiler Design, Processor Architecture **2007 - 2009**
Team leader on compiler engineering effort to provide intuitive, interactive end user experience for DSP compiler tool suite. Designed a framework to guide users in achieving highly optimized compiled VLIW code. Assembly listing reports for optimization failure advice, porting advice when migrating from competitor architectures, advice on code modifications for optimization enablement. Lead designer, engineering effort director, project planning and scoping, release schedule, and drafting of specification. Development of various compiler optimizations for VLIW processing as well as software emulation layers for running competitor software solutions on Freescale silicon.

Advising of next-gen DSP core architecture team in creating a highly orthogonal, compiler targetable multi-clustered VLIW based digital signal processor architecture. Work with future basestation architecture teams on designing next-gen basestation architecture for 4G LTE incorporating control and data plane processing with appropriate programming models.

Method Seven, MA USA
Technical Co-Founder
High Performance Software and Hardware Systems Architecture **2006 - 2007**
Founded Method Seven, a financial engineering company applying biologically inspired machine learning to financial market analysis. Principal software systems architect and hardware systems architect for both research and deployment platforms. Led research and development of platform

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for scans and overlays covering the NASDAQ, NYSE, and AMEX markets using proprietary technologies.

Texas Instruments, TX USA
Advanced Architecture and Chip Technologies
Microprocessor and Systems Architecture **2005**
System modelling and architectural exploration of Davinci^{TM}system-on-chip (SOC) architecture designed for embedded video processing. SystemC based simulation models of on–chip crossbars, bus arbitration and bridge technology, as well as on–chip and off–chip memory controllers within application specific heterogeneous SOC architectures.

Fulbright and Jaworski LLP, TX USA
Scientific Advisor, Intellectual Property
Electrical, Computer Engineering and Computer Science **2005 - 2007**
Intellectual property consultant and technology advisor on litigation and prosecution work including, but not limited to: CDMA2000 3G wireless standards, wireless communications systems, embedded computing, and large scale modular software systems. Reverse engineering of source code varying from VHDL to high level object oriented applications, as well at patent prosecution and litigation work.

Intel Corporation, CA USA
Microprocessor Research Labs
Compiler Engineering **2000**
Implemented speculative multi–threading support in Intel's IA–64 compiler. Developed new program analysis and back end code generation phases to support speculatively launching threads at runtime. Analyzed the performance potentials of SPEC95 benchmarks with respect to speculatively multi–threaded execution.

Rice University, TX USA
Computer Architecture and Circuit Design (Instructor) **2000 - 2003**
Graduate instructor of graduate and undergraduate curriculum in the areas of Electrical and Computer Engineering, specifically relating to Computer Architecture and Circuit Design. Advised student projects, instructed classes and led laboratory work.

Vicarious Visions, NY USA
Lead Software Engineer **1999**
Principal engineer on Activision's "AMF Extreme Bowling" for Nintendo's Color Gameboy gaming console. Developed PC based audio and graphics development tools suite for use with Color Gameboy game production. Coded innovative, highly optimized assembly routines for real time speech and full motion video on the console's limited Zilog Z80 processor resources.

Stratus Computer, MA USA
Hardware Engineering **1997 - 1998**
Debugged locked step CPU operation and memory management issues in Stratus' fault tolerant UNIX release 3.4. Qualified Hewlett Packard PA–8000 series CPU modules under Stratus' proprietary OS release, VOS 14.0, during alpha and beta test phases. Wrote C code and UNIX shell scripts for recreating documented system failures, and to automate remote kernel updates and OS installs as well as data logging.

Rensselaer Polytechnic Institute, NY USA
Digital Microelectronics Design (Instructor) **1997 - 1998**
Undergraduate instructor of undergraduate courses in digital microelectronics and circuit design. Instructed weekly lessons, computer design labs, graded exams and problem sets.

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Rensselaer Electric Motor Sports, NY USA
Hardware and Software Engineering **1995 - 1997**
This project was funded by, and led by, General Motors Corporation and Honda of America. Hardware and software co-design of embedded operating system and hardware platform for electrical vehicle prototypes, running on 16-bit Motorola 68K dual processor platform. Designed power engineering test platform for dynamometers, including hardware and user interface software.

Appointed Conference Committees and Organizations

IEEE International Conference on Communications, USA
Technical Review Committee, Machine Learning for Communications Track **2021 - Present**
Technical committee member responsible for the review, critique, and acceptance of academia and industry based publications and research in the areas of machine learning for communications systems.

IEEE International Symposium on Circuits and Systems, USA
Technical Review Committee **2021 - Present**
Technical committee member responsible for the review, critique, and acceptance of academia and industry based publications and research in the areas of computing, including energy aware systems, multicore processing, and adaptive computing.

IEEE and ACM Design Automation Conference, USA
Technical Steering Committee, Embedded Computing Track **2019 - Present**
Technical Steering Committee member responsible for the review, critique, and acceptance of academia and industry based publications and research in the area of embedded computing and related systems, including embedded hardware, embedded software, firmware and tools.

IEEE and ACM Design Automation Conference, USA
Co-chair, Program Committee, Embedded Systems and Software Track **2014 - 2019**
Co-chair and Program Committee member responsible for the review, critique, and acceptance of academia and industry based publications in the areas of embedded systems, embedded software, and embedded system design. Design Automation Conference is an annual technical conference and trade show specializing in electronic systems.

IEEE and ACM Design Automation Conference, USA
Program Committee, Designer and User Track **2011 - Present**
Program Committee member responsible for the review, critique, and acceptance of academia and industry based publications in the areas of automated system design, both of hardware, software, and system analysis. Design Automation Conference is an annual technical conference and trade show specializing in electronic systems.

ACM Great Lakes Symposium on VLSI, Stresa-Lago Maggiore, Italy
Program Committee **2007**
Reviewer and committee member in the area of system-on-chip architectures, VLSI design, and compiler driven architecture design space exploration.

IEEE International Symposium on Personal Indoor and Mobile Radio Communications, Helsinki, Finland
Program Committee **2006**
Reviewer and committee member in the area of personal and mobile area radio communications and related systems.

ACM International Conference on Parallel Architectures and Compilation Techniques, Charlottesville, VA, USA
Program Committee **2002**
Reviewer and committee member in the area of parallel computer architectures, programming lan-

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guages and related compiler technologies.

Books and Contributed Chapters

Brogioli, Michael C., and Kraeling, Mark B., *Internet of Things - A Synopsis of the Internet of Things, its History, Application, Technology, Architecture, and Challenges Moving Forward*, Software Engineering for Embedded Systems - Methods, Practical Techniques and Applications, 2nd Edition, Elsevier Publishing, 2019.

Brogioli, Michael C., *Software and Compiler Optimization for Microcontrollers, Embedded Processors and DSPs*, Software Engineering for Embedded Systems - Methods, Practical Techniques and Applications, 2nd Edition, Elsevier Publishing, 2019.

Brogioli, Michael C., *Embedded and Multicore System Architecture - Design and Optimization*, Software Engineering for Embedded Systems - Methods, Practical Techniques and Applications, 2nd Edition, Elsevier Publishing, 2019.

Leotescu, Florin, and Cristian, Marius and Brogioli, Michael C., *Performance Analysis using NXP's i.MX RT1050 Crossover Processor and the Zephyr Real-Time Operating System*, Software Engineering for Embedded Systems - Methods, Practical Techniques and Applications, 2nd Edition, Elsevier Publishing, 2019.

Wu, Michael and Sun, Yang and Wang, Guohui and Brogioli, Michael C. and Cavallaro, J. R., *Implementation of a High Throughput 3GPP Turbo Decoder on GPU Architectures*, Software Development for Networking Applications – Expert Guides Series, Elsevier Publishing, Atlanta, GA, 2018.

Brogioli, M. C., *On The C++ Programming Language for Embedded Software, Systems, and Platforms*, Software Engineering for Embedded Systems – Expert Guides Series, Elsevier Publishing, Atlanta, GA, 2013.

Brogioli, M. C., *Software Optimizations for Memory Performance in Embedded Systems*, Software Engineering for Embedded Systems – Expert Guides Series, Elsevier Publishing, Atlanta, GA, 2013.

Invited Co-Author, *Signal Processing Systems Handbook, Second Edition*, Springer Publishing Company, 11 West 42nd Street, New York, NY, 2012.

Brogioli, M. C., *Software Programmable DSP Architectures*, Expert Guide DSP for Embedded and Real-Time Systems, pp. 63-75, Elsevier Publishing, Atlanta, GA, 2012.

Brogioli, M. C., *The DSP Hardware / Software Continuum*, Expert Guide DSP for Embedded and Real-Time Systems, pp. 103-113, Elsevier Publishing, Atlanta, GA, 2012.

Brogioli, M. C., *DSP Optimization - Memory Optimization*, Expert Guide DSP for Embedded and Real-Time Systems, pp. 217-241, Elsevier Publishing, Atlanta, GA, 2012.

Brogioli, M. C. and Dew, Stephen, *Optimizing DSP Software - High level Languages and Programming Models*, Expert Guide DSP for Embedded and Real-Time Systems, pp. 167-179, Elsevier Publishing, Atlanta, GA, 2012.

Sun, Yang, Amiri, Kiarash, Brogioli, Michael, Wang, Guohui, and Cavallaro, Joseph R., *DSP Hardware Accelerator Architectures for Communication Applications*, Springer Publishing, New York, NY, Spring 2012.

Sun, Yang, and Amiri, Kiarash, and Brogioli, Michael C., and Cavallaro, Joseph, *Application-Specific Accelerators for Communications*, Springer Publishing Company, 11 West 42nd Street, New York,

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NY, 2010.

Invited Co-Author, *Signal Processing Systems Handbook, First Edition*, Springer Publishing Company, 11 West 42nd Street, New York, NY, 2010.

Publications and Invited Papers

Brogioli, Michael, C., and Games, William, and Moats, Richard, *Current and Future Challenges in Internet of Things (IoT) Development Silos (Part I)*, Embedded Computing Design Magazine, USA, 2020.

Brogioli, Michael, C., and Games, William, and Moats, Richard, *On Solving the IoT Development Silo Problem* IEEE Real-Time and Embedded Technology and Applications Symposium, Tools and Demos Session, Montreal, Canada, 2019.

Moats, Richard, and Games, Bill, and Brogioli, M. C., *Arch - A New Language For The Next Wave of Network-Connected Embedded Development*, Design Automation Conference, Austin, Texas, 2017.

Moats, Richard, and Games, Bill, and Brogioli, M. C., *Network Native - The Next Wave of Connected Embedded Development*, Network Native Inc., Austin, Texas, 2017.

Invited Paper, Arokia I, Brogioli, Michael, Jain, Nitjin and Garg, Umang, *LTE Layer 1 Software Design on Heterogeneous Multicore DSP Platforms*, IEEE 45th Asilomar Conference on Signals, Systems and Computers, Pacific Grove, CA, 2011.

Kyriakopoulous, Konstantinos, Brogioli, Michael C., and Zhang, Ruihao, *Improving Software Systems Quality through Well Defined Development Methodologies*, 2011 Test Methodology and Efficiency Symposium, Freescale Semiconductor, Austin, TX, USA, 2011.

Brogioli, Michael C., and Cavallaro, J.R., *Compiler Driven Architecture Design Space Exploration for Embedded DSP Workloads: A Study in Software Programmability Versus Hardware Acceleration*, IEEE 43rd Asilomar Conference on Signals, Systems and Computers, Pacific Grove, CA, 2009.

Brogioli, Michael C., and Zhang, Ruihao, *Compiler Feedback: Guiding Performance of Compiled C Code*, Freescale Semiconductor White Paper, Austin, TX, 2009.

Brogioli, M.C., and Cavallaro, J., *RISD: A Retargetable Compiler Infrastructure for Scalable Multi-Clustered VLIW DSP Architectures*, IEEE 5th Dallas Circuits and Systems Workshop, Dallas, TX, 2007.

Brogioli, Michael C., Radosavljevic, P., and Cavallaro, J., *A General Hardware/Software Codesign Methodology for Embedded Signal Processing and Multimedia Workloads*, IEEE 40th Asilomar Conference on Signals, Systems, and Computers, Pacific Grove, CA, 2006.

Brogioli, Michael C., Radosavljevic, P., and Cavallaro, J., *Hardware/Software Co-design Methodology for DSP/FPGA Partitioning: A Case Study for Meeting Real-Time Processing Deadlines in 3.5G Mobile Receivers*, 49th IEEE International Midwest Symposium on Circuits and Systems, San Juan, Puerto Rico, 2006.

Brogioli, Michael C., Willmann, P.D., and Rixner, S., *Parallelization Strategies for Network Interface Firmware*, IEEE/ACM 4th Annual Workshop on Optimizations for DSP and Embedded Systems (In Conjunction with IEEE/ACM International Symposium on Code Generation and Optimization), Manhattan, NY, 2006.

Brogioli, Michael C., Gadhiok, M., and Cavallaro, J., *Design and Analysis of Heterogeneous DSP/FPGA Based Architectures for 3GPP Wireless Systems*, IEEE Real-Time and Embedded Technology and

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Applications Symposium Work-in-Progress Sessions, San Jose, CA, 2006.

Brogioli, Michael C., and Cavallaro, J., *Modelling Heterogeneous DSP-FPGA Based System Partitioning with Extensions to the Spinach Simulation Environment*, IEEE 39th Asilomar Conference on Signals, Systems, and Computers, Pacific Grove, CA, 2005.

Joseph R. Cavallaro, Michael C. Brogioli, Alexandre de Baynast, and Predrag, Radosavljevic, *Reconfigurable Architectures for Wireless Systems: Design Exploration and Integration Challenges*, Wireless World Research Forum, Toronto, CA, 2004.

Brogioli, Michael C., Pai, V.S., Willmann, P.D., *Spinach: A Liberty–Based Simulator For Programmable Network Interface Architectures*, ACM SIGPLAN/SIGBED Conference on Languages Compilers and Tools for Embedded Systems, San Diego, CA, 2004.

Brogioli, Michael C., *Dynamically Reconfigurable Data Caches in Low Power Computing*, Masters Thesis, Rice University, Houston Texas, 2002.

Brogioli, Michael C., and Jones, Bryan, *Dynamically Configurable Caches in Low Power Computing*, Internal White Paper, Rice University, Houston Texas, 2001.

Patents

Gregory D. Chiocco and Michael C. Brogioli, *Systems and Methods for Obtaining Location Data*, U.S. Patent Application 18/080,411, filed December 2022. Patent Pending.

Donald W. Games, Michael C. Brogioli Ph.D., Richard Moats, *System And Method for Holistic Application Development and Deployment in a Distributed Heterogeneous Computing Environment*, U.S. Patent Application 17/745,792, filed May 2022. Patent Pending.

Gregory D. Chiocco and Michael C. Brogioli, *Systems and Methods for Traversing A Three Dimensional Space*, U.S. Patent No. 11,526,180.

Gregory D. Chiocco and Michael C. Brogioli, *Systems and Methods for Aggregating Harvest Yield Data*, U.S. Patent No. 11,354,757.

Gregory D. Chiocco and Michael C. Brogioli, *Systems And Methods For Communication in GNSS Based Autonomous Vehicle Deployment*, U.S. Patent Application 17/060,625, filed March 2021. Patent Pending.

Michael C. Brogioli and Gregory D. Chiocco, *Systems and Methods for Connected Computation in Network Constrained Systems*, U.S. Patent No. 11,354,757.

Donald W. Games, Michael C. Brogioli Ph.D., Richard Moats, *System And Method for Holistic Application Development and Deployment in a Distributed Heterogeneous Computing Environment*, U.S. Patent No. 11,340,887.

Michael C. Brogioli, Ph.D., Cesar Taylor M.D., and Howard Roberts, *Location Agnostic Platform for Medical Condition Monitoring and Prediction and Method of Use Thereof*, Patent No: 147145.010100/US, 2014.

Cesar Taylor M.D., and Michael C. Brogioli Ph.D., and Howard Roberts, *System for Holistic Pain Monitoring and Prediction and Method of User Thereof*, Patent No: 147145.010200/US, 2014.

Cesar Taylor M.D., and Michael C. Brogioli Ph.D., and Howard Roberts, *System for Prevention of Narcotic Diversion and Method of Use Thereof*, Patent No: 147145.010300/US, 2014.

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Howard Roberts, Cesar Taylor M.D., and Michael C. Brogioli Ph.D., *Magnetometer Breathing Sensor and Method of User Thereof*, Patent No: 147145.010400/US, 2014.

Leadership and Board Membership

Tandem Motion Company FL, USA
Advisory Board **2021 - Present**
Advisory board member on intellectual property strategy, fundraising, finance and select technologies. Tandem is building hybrid solutions for heavy duty internal combustion engine vehicles.

AgCompute CA USA
Advisory Board, Co-Inventor **2019 - Present**
Advisory board and co-inventor of patent pending technology for the advancement of Agriculture Technology in areas of low network connectivity and adverse conditions. Innovative sensor, edge and cloud computing solutions for in-field real time asset management.

MIT MassChallenge USA
Mentor, Speaker **2017 - Present**
MassChallenge is a global startup accelerator with a focus on high-impact, early-stage entrepreneurs. Through its global network of accelerators in Boston, London, Mexico City, Geneva, Jerusalem and Texas, coupled with unrivaled access to our corporate partners, MassChallenge has driven growth and created value the world over. To date, MassChallenge has raised over $2B in funding, generated over $900M in revenue, and created over 65,000 jobs.

ScribeSense, TX USA
Board of Directors **2017**
ScribeSense is a *patented* cloud-based grading platform for schools and the only solution for grading free-form paper tests. ScribeSense automatically grades handwritten tests with 99% accuracy. Teachers scan and upload their own tests using a standard school scanner. ScribeSense's visual analytics enables data-driven decision making so schools can improve student learning and retain top teacher talent.

Southwest Angel Network for Social Impact, TX USA
Board of Directors **2015 - 2019**
The Southwest Angel Network for Social Impact (SWAN Impact) is a community of like-minded investors who enjoy working together to *Make the world a better place, one company at a time.* We believe that we can have the most significant impact by funding for-profit start-up companies who are building sustainable businesses.

Network Native, TX USA
Board of Directors, Co-Founder, Interim CTO **2015 - Present**
Board member and co-inventor, advising in the areas of Internet of Things technologies, specifically related to product developer solutions, programming languages and platforms, security and infrastrucure. Business development, marketing, and fund raising. Have held various roles, including but not limited to interim CTO.

NewCrew, TX USA
Advisory Board **2015 - 2016**
Board member advising in the areas of mobile computing, social computing, and geofencing technologies. Business development, marketing, and fund raising.

AngelSpan, TX USA
Advisory Board **2015 - 2016**
Board member advising in the areas of professional investor relations to start-ups, resource allocation, and a platform for increased efficiency and valuation of early stage companies and venture capital portfolios.

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Student Loan Genius (now Vault), TX USA
Advisory Board, Interim CTO **2013 - 2014**
Advisory board member and interim CTO advising in the areas of financial transactions systems and enterprise software, as they pertain to solving the student loan debt crisis for early stage science, technology, engineering and medicine (STEM) employees. Technology, recruiting, fund raising.

HealthBits, TX USA
Board Member, Co-Inventor **2013 - 2014**
Board member advising in the areas of large scale enterprise software systems, real-time computing and medical sensing devices across complex event processing systems.

Osmek, TX USA
Interim CTO, Advisory Board **2012 - 2014**
Interim CTO and board member advising in the areas of large scale cloud based content management software systems. Providing innovative media content management for heterogeneous web enabled devices with geolocational services, primarily using PHP and Python programming languages.

Academia

Rice University, Houston, Texas USA
DSP Compiler Design **2005 - 2009**
Developed *RISD*, a retargetable compiler infrastructure for clustered VLIW DSP architectures. By taking pre-existing code schedules and binaries for existing DSP applications, RISD takes a flexible machine definition for which the code should be recompiled. Users can specify the number of VLIW clusters, functional units per VLIW cluster, functional unit mix per VLIW cluster, register file sizes, cluster interconnect topology (point-to-point versus 2d mesh network), multi-cluster scheduling algorithms, and inter-cluster cross-register file bandwidth and latencies.

Compiler framework was used to perform compiler driven design space exploration of massively multi-clustered VLIW based architectures versus FPGA and ASIP implementations of software kernels. RISD was used in studies comparing tradeoffs in computational throughput versus gates required to implement programmable DSP cores containing many register files and VLIW compute clusters, versus FPGA efficiency when including routing overhead for large scale problems.

Rice University, Houston, Texas USA
DSP/FPGA Based System-On-Chip Architectural Simulator Design **2004 - 2009**
Developed *Spinach DSP-FPGA*, a modular and composable simulator design infrastructure for programmable and reconfigurable embedded SOC architectures. Designed and developed modular and composable software modules to bit-true, cycle accurately simulate Texas Instruments C62x and C64x DSPs and MIPS style processors. Additionally, designed and developed support for SRAM and DRAM style memories, heterogeneous memory systems, heterogeneous clock domains, as well as runtime reconfigurable Xilinx Virtex II based FPGA computing elements, cache and memory controllers, bus arbiters, and on-chip interconnect fabric.

System was validated against compiled code DSP firmware from Texas Instruments' Code Composer Studio running on the simulator versus actual hardware benchmarks. Simulation platform was used to investigate highly heterogeneous multi-processor DSP based SOC architectures containing one or more Xilinx style FPGA based hardware coprocessors. Studies in 3.5G wireless telecommunications as well as H.26x video processing were performed to gain insight into overall system bottlenecks, hardware and software partitioning strategies, and tradeoffs of overall system design.

Rice University, Houston, Texas USA
Programmable Network Interface Architecture Simulator Design **2002 - 2004**
National Science Foundation Grant Nos. CCF-0532448 and CNS-0532452
Developed *Spinach*, a simulator design toolset for modelling programmable network interface architectures. Spinach models system components common to all programmable environments (ALUs,

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control and data paths, register files, instruction processing), as well as components specific to embedded computing (software controlled SRAM scratchpad memory, hardware assists for DMA and medium access control). Spinach is a simulator design infrastructure, rather than a simulator per se. As such, the same underlying C code framework is used to model a uniprocessor Gigabit network interface, a multi-processor Gigabit network interface, or a 10 Gigabit multi-processor network interface with highly heterogeneous memory systems. Only a small number of lines of high level scripting language code is required to describe each of the various systems.

Spinach was validated by modeling the Tigon-2 programmable Ethernet controller by Alteon Websystems, running actual compiled code Ethernet processing firmware and by comparing the reported results to actual hardware benchmarks. Spinach was also used to obtain new insights into the performance of Gigabit and 10 Gigabit network interfaces both in terms of hardware architecture and firmware parallelization strategies. *Public Website: https://sourceforge.net/projects/spinach/*

Rice University, Houston, Texas USA
Software Engineering and Consulting **2000**
Implemented instruction selection and register allocation optimizations in UHFFT, an adaptive and portable software library for the Fast Fourier Transform. Performed in depth analysis of register pressure, compiler generated spill code, memory hierarchy utilization, and instruction selection for non–trivially sized FFT matrices running on commercially available hardware platforms. Utilized reverse Cuthill–McKee technique to achieve near optimal computation orderings and minimize live data set sizes, as well as optimize register allocation and instruction selection phases of compilation.

Select Expert Witness, Consultant Engagements

Daedalus Prime LLC* v. Samsung Electronics Co., Ltd. et. al
Bluepeak Law Group LLP, NY, USA
Expert Witness in Dynamic Power Management **2023 - Present**
Case Subject Matter - Dynamic power management of multicore processors, memory systems and related domains.
Work Performed - Expert consulting.

Certain Semiconductors and Devices and Products Containing the Same, Including Printed Circuit Boards, Automotive Parts, and Automobiles, Inv. No. 337-TA-1332
Daedalus Prime LLC*
Reichman Jorgensen LLP, CA, USA
Expert Witness in Dynamic Power Management **2022**
Case Subject Matter - Dynamic power management of multicore processors, memory systems and related domains.
Work Performed - Expert consulting.

Definitive Holdings LLC v. Powerteq LLC*
Proskauer Rose LLP, NY, USA
Expert Witness in Embedded Software and Hardware **2022 - Present**
Case Subject Matter - Automotive engine control software and hardware systems.
Work Performed - Expert consulting, declarations (to date).

Aire Technology Ltd.* v. Apple Inc.
Aire Technology Ltd.* v. Google LLC
Aire Technology Ltd.* v. Samsung Electronics Co., Ltd. et. al
Russ, August, and Kabat LLP, Los Angeles, CA, USA
Expert Witness in Computer Hardware Design **2022**
Case Subject Matter - Computer hardware design as it relates to Near Field Communication.
Work Performed - Expert consulting, declarations, deposition testimony.

WSOU Investments, LLC* v. ZTE Corporation et. al

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Kasowitz Benson Torres LLP, NY, USA
Expert Witness in Video and Telecommunications Computing **2022 - 2023**
Case Subject Matter - Expert Witness in hardware and software design as it relates to video and telecommunications processing.
Work Performed - Expert consulting and expert declaration.

Robert Zeidman* v. Lindell Management LLC
Bailey Glasser LLP, Washington DC, USA
Expert Witness in Computer Software and Networking **2022 - 2023**
Case Subject Matter - Expert Witness in computer software and networking as it pertains to voting information related to the United States 2020 Presidential Election.
Work Performed - Expert consulting, expert reports, testimony at hearing.

Netlist, Inc.* v. Samsung Electronics Co., Ltd. et. al
Irell & Manella LLP, CA, USA
Expert Witness in Computer Memory Architecture **2022 - Present**
Case Subject Matter - Expert Witness in computer memory architecture, including performance and power related issues.
Work Performed - Expert consulting, expert reports, trial testimony (to date).

Samsung Electronics Co., Ltd v. Netlist, Inc*
Irell & Manella LLP, CA, USA
Expert Witness in Computer Memory **2022 - Present**
Case Subject Matter - Expert Witness in computer memory module architecture, including DRAM and related technologies.
Work Performed - Expert consulting, IPR declarations, depositions (to date).

Maxell Ltd* v. Lenovo Group Ltd., et. al
Mayer Brown LLP, Washington D.C., USA
Expert Witness in Power Management **2022 - Present**
Case Subject Matter - Expert Witness in the area of mobile processing and power management.
Work Performed - Expert consulting (to date).

Q Technologies, Inc.* v. Walmart, Inc.
Q Technologies, Inc.* v. Neutron Holdings, Inc. d/b/a/ LIME
Kane Russell Coleman & Logan PC, TX, USA
Expert Witness in Mobile Payments Systems **2021 - Present**
Case Subject Matter - Expert Witness in the area of mobile payments processing systems.
Work Performed - Expert consulting, expert reports (to date).

Samsung Electronics Co., Ltd v. Netlist, Inc*
Gibson Dunn & Crutcher LLP, CA, USA
Expert Witness in Computer Memory **2021 - 2022**
Case Subject Matter - Expert Witness in computer memory module architecture, including DRAM and related technologies.
Work Performed - Expert consulting, IPR declarations, deposition.

Sonrai Memory Limited* v. Oracle Corporation
Russ, August, and Kabat LLP, Los Angeles, CA, USA
Expert Witness in Memory and Compression Technology **2021 - 2022**
Case Subject Matter - Memory controllers, memory technology and data compression technology.
Work Performed - Expert consulting, claim construction, declarations, depositions.

Certain Laptops, Desktops, Servers, Mobile Phones, Tablets, and Components Thereof,

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Inv. No. 337-TA-1280
Sonrai Memory Limited*
Russ, August, and Kabat LLP, Los Angeles, CA, USA
Expert Witness in Low Power Systems **2021 - 2022**
Case Subject Matter - System on chips, operating systems and system components related power consumption in computing devices.
Work Performed - Expert consulting, claim construction declarations, expert reports, depositions.

Future Link Systems LLC* v. Advanced Microdevices, Inc.
Future Link Systems LLC* v. Apple, Inc
Future Link Systems LLC* v. Broadcom, Inc; Broadcom Corp.
Future Link Systems LLC* v. Qualcomm, Inc.; Qualcomm Technologies
Future Link Systems LLC* v. Realtek Semiconductor Corp.
Russ, August, and Kabat LLP, Los Angeles, CA, USA
Expert Witness in Circuit Design, Interconnects and Test **2021 - 2022**
Case Subject Matter - Semiconductor circuit design and reuse, memory design and test, PCI Express and related interconnect technologies.
Work Performed - Expert consulting, claim construction, declarations, depositions.

Certain UMTS and LTE Cellular Communications Modules and Products and Products Containing the Same, Inv. No. 337-TA-1240
Philips RS North America LLC and Koninklijke Philips N.V.*
Foley & Lardner LLP, MA, USA
Expert Witness in Wireless Computing Technology **2020 - 2021**
Case Subject Matter - Embedded computing technology related to wireless mobile devices, including 3GPP standards based functionality.
Work Performed - Expert consulting, expert reports, deposition, trial testimony.

Acqis* v. Samsung Electronics Co., LTD
Robins Kaplan LLP, USA
Expert Witness in Mobile Devices and Interconnects **2021**
Case Subject Matter - Chip and chipset interconnect technology relating to mobile and non-mobile devices.
Work Performed - Expert consulting, expert reports, depositions.

Neodron Limited* v. Texas Instruments, Inc
Neodron Limited* v. Cypress Semiconductor Corp
Neodron Limited* v. Renesas Electronics Corp
Neodron Limited* v. ST Microelectronics N.V.
Russ, August, and Kabat LLP, Los Angeles, CA, USA
Expert Witness in Touch Screen Technology and Related Systems **2020 - 2021**
Case Subject Matter - Expert witness in hardware/software systems for touch screen technology, including analog and digital signaling and processing.
Work Performed - Expert consulting, declarations.

Qualcomm Inc. v. Monterey Research LLC*
Desmarais LLP, NY, USA
Expert Witness in Memory Systems Technology **2021**
Case Subject Matter - SRAM and DRAM technology, burst functionality and related matters.
Work Performed - Expert consulting, IPR declarations, depositions.

Advanced Micro Devices Inc. v. Monterey Research LLC*
Desmarais LLP, NY, USA
Expert Witness in Memory Systems, Interconnects **2021**

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Case Subject Matter - SRAM and DRAM technology, multi-ported memory systems, boot technology and related technologies.
Work Performed - Expert consulting, IPR declarations, depositions.

Analog Devices Inc. v. Xilinx Inc.*
Morrison & Foerster LLP, CA, USA
Expert Witness in FPGAs and Configurable Computing **2020 - 2021**
Case Subject Matter - FPGAs and solutions related to crossbar interconnects, high speed transceivers, and configurable computing.
Work Performed - Expert consulting, IPR declarations, depositions.

TriOptima AB v. Quantile Technologies Limited*
Caldwalader Wickersham & Taft, New York, USA
Expert Witness in Source Code for FinTech Systems **2020**
Case Subject Matter - Technology implementations of financial services related to compression and derivatives markets.
Work Performed - Expert consulting, source code review.

Unified Patents LLC v. JustService.net LLC*
Sheridan Ross P.C., Colorado, USA
Expert Witness in Virtual Data Storage Systems **2020 - 2021**
Case Subject Matter - Web enabled virtual data storage systems for backup, storing and transferring of data.
Work Performed - Expert consulting, declarations, depositions.

Karya Property Management, LLC* v. ResMan, LLC
Baker Botts LLP, Houston, Texas, USA
Expert Witness in Distributed Software Systems **2020 - 2021**
Case Subject Matter - Expert witness in the areas of distributed software systems, including data base technologies, as they relate to property management software and related systems.
Work Performed - Expert consulting, claim construction, IPR declarations, CBM declarations, depositions, expert reports.

Certain Touch-Controlled Mobile Devices, Computers, and Components Thereof, Inv. No. 337-TA-1193
Neodron Limited*
Russ, August, and Kabat LLP, Los Angeles, CA, USA
Expert Witness in Touch Screen Technology and Related Systems **2020**
Case Subject Matter - Expert witness in hardware/software systems for touch screen technology in mobile devices.
Work Performed - Expert consulting.

VLSI Technology LLC* v. Intel Corporation
Irell & Manella LLP, Los Angeles, CA USA
Expert Witness in Computer Architecture **2020 - 2021**
Case Subject Matter - Expert witness in the area of computer architecture, microprocessors and power management.
Work Performed - Expert consulting and source code review, expert reports, depositions, trial testimony.

Optimum Imaging Technologies LLC* v. Canon Inc.
Ruyak Cherian LLP, Washington D.C., USA
Expert Witness in FPGA Based Image Processing Systems **2019 - 2021**
Case Subject Matter - Expert witness and consultant in the area of heterogeneous FPGA/DSP/CPU

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based systems as applied to image and video processing technology.
Work Performed - Expert consulting, claim construction declarations, expert reports, depositions, IPR declarations.

Dish Network, LLC v. Contemporary Display LLC*
Toler Law Group, P.C., Texas., USA
Expert Witness in Real Time Video Processing **2020**
Case Subject Matter - Expert Witness in real-time video processing technology over the Internet, including related user interfaces and quality of service.
Work Performed - Consulting, IPR declarations, deposition.

Dish Network, LLC v. Contemporary Display LLC*
Toler Law Group, P.C., Texas., USA
Expert Witness in Real Time Video Processing **2020**
Case Subject Matter - Expert Witness in real-time video processing technology over Internet, including related user interfaces and quality of service.
Work Performed - Consulting, IPR declarations, deposition.

Multimedia Content Management LLC* v. Dish Network LLC
Sheridan Ross P.C., Colorado, USA
Expert Witness in Real Time Video Processing **2019 - 2020**
Case Subject Matter - Expert Witness in Internet based real-time video processing set top boxes, and related content processing and distribution.
Work Performed - Expert consulting.

Exegy Inc. et al v. ACTIV Financial Systems, Inc.*
Wolf Greenfield & Sachs P.C., USA
Expert Witness High Speed Computing for Financial Services **2019 - 2021**
Case Subject Matter - Expert Witness in microprocessor and FPGA based system design for high speed financial services, high speed RDMA systems, etc.
Work Performed - Expert consulting, IPR declarations, depositions.

Certain Touch-Controlled Mobile Devices, Computers, and Components Thereof, Inv. No. 337-TA-1162
Neodron Limited*
Russ, August, and Kabat LLP, Los Angeles, CA, USA
Expert Witness in Touch Screen Technology and Related Systems **2019 - 2020**
Case Subject Matter - Expert witness in hardware/software systems for touch screen technology in mobile devices.
Work Performed - Expert consulting, claim construction declaration, expert reports, depositions.

Maxell, Ltd., et al.,* v. Apple Inc.
Mayer Brown LLP, Washington D.C., USA
Expert Witness in Embedded Computer Architecture **2019 - 2021**
Case Subject Matter - Expert witness and consulting engineer in low power computing and power management.
Work Performed - Expert consulting, claim construction declaration, claim construction deposition, expert reports, infringement and validity depositions.

Nuvoton Technology Corporation* v. Microchip Technology Inc.
Finnegan, Henderson, Farabow, Garrett & Dunner, Washington D.C., USA
Expert Witness in Embedded Computer Architecture **2019 - 2020**
Case Subject Matter - Expert witness in embedded memory system hardware, direct memory access engines, memory controllers, and analog/digital and digital/analog ASICs.

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Work Performed - Expert consulting, declarations, claim construction deposition, IPR declarations, deposition.

Shuttlewagon Inc.*, v. Innovative Quality Solutions, LLC
Stroz Friedberg, Massachusetts, USA
Expert Witness in Embedded Computing **2019**
Case Subject Matter - Expert witness in Programmable Logic Controllers (PLCs), IEC 61131 IE / CodeSys and real-time computing as it pertains to industrial equipment, as well as misappropriation of proprietary technology.
Work Performed - Expert consulting.

RDM, Inc. v. Citoc Inc.*
Citoc Incorporated, Texas, USA
Expert Witness in Cloud / Web Based Computing **2019**
Case Subject Matter - Expert witness cloud deployed, web based, infrastructure management software and best practices in deploying solutions to consumers. Work Performed - Expert consulting.

ResMan, LLC v. Karya Property Management, LLC et al.*
Beck Redden LLP, Texas, USA
Expert Witness in Software Design **2019 - 2021**
Case Subject Matter - Expert witness in trade secret matters related to design and architecture of consumer facing software products.
Work Performed - Expert consulting, expert reports, depositions, trial testimony.

Qualcomm* v. Apple Inc.
Case No. 3:17-cv-02398-DMS-MDD
Quinn Emanuel Urquhart & Sullivan, CA, USA
Expert Witness in Mobile Devices and Computer Architecture **2019**
Case Subject Matter - Expert witness in mobile devices, computer architecture, and software system design for wireless communications.
Work Performed - Expert consulting.

Vasu Networks Corporation*
Skiermont Derby, Texas, USA
Consulting Expert in Cellular Network Technologies **2019**
Case Subject Matter - Consulting expert in matters related to Single Radio Voice Call Continuity, Dual Radio Voice Call Continuity, and various heterogeneous wireless technologies and standards committees related to seamless connectivity.
Work Performed - Consulting expert.

Qualcomm* v. Apple Inc.
Case No. 37-2017-00041389-CU-BC-NC
Quinn Emanuel Urquhart & Sullivan, CA, USA
Expert Witness in Mobile Devices and Computer Architecture **2018 - 2019**
Case Subject Matter - Expert witness in mobile devices, computer architecture, and software system design for wireless communications.
Work Performed - Expert consulting.

Qualcomm* v. Apple Inc.
Inv No. 337-TA-1093
Quinn Emanuel Urquhart & Sullivan, CA, USA
Expert Witness in Mobile Devices and Computer Architecture **2017 - 2018**
Case Subject Matter - Expert witness in mobile devices, computer architecture, and software system

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design for wireless communications.
Work Performed - Expert consulting, expert reports, depositions, trial testimony.

Qualcomm* v. Apple Inc.
Quinn Emanuel Urquhart & Sullivan, CA, USA
Case No. 3:17-CV-1375-DMS-MDD
Expert Witness in Mobile Devices and Computer Architecture **2018 - 2019**
Case Subject Matter - Expert witness in wireless mobile devices, computer architecture, and software system design.
Work Performed - Expert consulting, expert reports, depositions, trial testimony.

Redzone Wireless LLC v. Netgear Inc.*
Bird Marella, CA, USA
Expert Witness in Wireless Hardware/Software Systems **2018 - 2019**
Case Subject Matter - Manufacturing of software and hardware used in wireless routers and base stations, including chipsets and software solutions.
Work Performed - Expert consulting, expert reports, depositions.

Nvidia* v. ZiiLabs Corporation
Quinn Emanuel Urquhart & Sullivan, NY, USA
Expert Witness in GPU Architecture, Computer Architecture **2018**
Case Subject Matter - Expert witness in the areas of Graphics Processor (GPU) architectures, memory systems architectures, and microprocessor design.
Work Performed - Expert consulting.

Acqis* v. EMC Corporation
Cooley LLP, CA, USA
Expert Witness in Computer Architecture **2017 - 2018**
Case Subject Matter - Expert witness in the areas of PCI, PCI-Express, system-on-chip technology, and computer memory technologies.
Work Performed - Expert consulting.

Qualcomm* v. Apple Inc.
Certain Mobile Electronic Devices and Radio Frequency and Processing Components Thereof, Inv No. 337-TA-1065
Quinn Emanuel Urquhart & Sullivan, CA, USA
Expert Witness in Mobile Devices and Computer Architecture **2017 - 2018**
Case Subject Matter - Expert witness in mobile devices, computer architecture, and software system design.
Work Performed - Expert consulting, expert reports, depositions.

Network Management Solutions* v. AT&T Mobility et. al
IP Law Leaders, Washington DC, USA
Expert Witness in Cellular Network Management **2017**
Case Subject Matter - Expert witness in mobile devices, wireless technology, 3GPP standards, and alarm management.
Work Performed - Expert consulting.

Certain Memory Modules and Components Thereof, and Products Containing Same, Investigation No. 337-TA-1023
Netlist* v. S.K. Hynix
Mintz Levin Cohn Ferris Glovsky and Popeo PC, Boston, MA, USA
Expert Witness in Computer Architecture and Memory Systems **2016 - 2017**
Case Subject Matter - Expert witness in the area of JEDEC standards essential DRAM memory

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module technology, relating to DIMM, R-DIMM and LR-DIMM as it applies to server based computing.
Work Performed - Expert consulting, source code review, declarations, expert reports, depositions, ITC trial testimony.

Certain Audio Processing Hardware, Software, and Products Containing Same, Inv. No. 337-TA-1026
Andrea Electronics Corporation*
Pepper Hamilton, LLP, Washington, DC, USA
Expert Witness in Audio Processing Hardware and Software **2017**
Case Subject Matter - Expert witness in hardware/software based digital signal processing systems audio processing and noise cancellation technology.
Work Performed - Expert consulting.

Specialized Monitoring Solutions, LLC v. Lutron Electronics Co., Inc.*
Vinson & Elkins LLP, Texas USA
Expert Witness in Embedded and Distributed Software Systems **2017**
Case Subject Matter - Expert witness in embedded software and hardware systems, as well as distributed data storage and sensing.
Work Performed - Expert consulting, claim construction analysis.

Huawei Technologies Co., Ltd.*, v. Samsung Electronics America, Inc. et al
Sidley Austin LLP, California USA
Expert Witness in 4G and Legacy Cellular Technologies **2016 - 2017**
Case Subject Matter - Expert witness in 4G and legacy cellular technologies.
Work Performed - Expert consulting, affidavits, claim construction.

Godo Kaisha IP Bridge 1* v. Broadcom Limited et. al
Ropes & Gray LLP, New York USA
Expert Witness in Computer Architecture **2016 - 2017**
Case Subject Matter - Consultant in the area of ARM based embedded computing architecture and system on-chip technology. Reverse engineering of VHDL, Verilog and RTL based technologies, as it pertains to multicore system architectures.
Work Performed - Expert consulting, source code review, claim construction.

Huawei Technologies Co. Ltd.* v. T-Mobile US, Inc. and T-Mobile USA, Inc.
Fish & Richardson P.C., Texas USA
Expert Witness in 4G and Legacy Cellular Technologies **2016 - 2017**
Case Subject Matter - Expert witness in 4G and legacy cellular technologies.
Work Performed - Expert consulting, claim construction, affidavits.

ACI Worldwide Corp. v. Mastercard International Incorporated*
Armstrong Teasdale LLP, Missouri, USA
Expert witness regarding financial transaction systems **2016 - 2017**
Case Subject Matter - Expert witness in trade secret misappropriation as it pertains to middleware message passing systems and financial transaction networks.
Work Performed - Expert consulting, source code review, declarations, expert reports, depositions.

Sony Computer Entertainment America v. Rothschild Digital Media Innovations*
Carey Rodriguez Milian Gonya, LLP, Florida, USA
Expert witness regarding distributed multimedia systems **2016**
Case Subject Matter - Expert witness in the area of distributed computing systems and multimedia technologies.
Work Performed - Expert consulting, declarations, expert reports, deposition.

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DTS, Inc., et al. v. Nero AG, et al.*
Glaser Weil Fink Jacobs Howard Avchen & Shapiro, Los Angeles CA, USA
Expert witness regarding distributed multimedia systems **2016**
Case Subject Matter - Expert witness in the area of software solutions for audio and video codecs.
Work Performed - Expert consulting, source code review, experimental analysis, expert reports, depositions.

Advanced Silicon Technologies*
Mintz Levin Cohn Ferris Glovsky and Popeo PC, Boston, MA, USA
Expert Consultant in Microprocessor Architecture, Intellectual Property **2015 - 2016**
Case Subject Matter - Consultant in the area of computer architecture and microprocessor technologies, specifically related to memory systems.
Work Performed - Expert consulting.

Certain Audio Processing Hardware and Software and Products Containing the Same, ITC Inv. No. 337-TA-949
Lenovo (United States), Inc.*
Toshiba Corp
Akin Gump Strauss Hauer & Feld LLP, Philadelphia, PA, USA
Expert Witness in Digital Signal Processing, Intellectual Property **2015 - 2016**
Case Subject Matter - Expert witness in hardware/software based digital signal processing systems tailored for noise cancellation technology.
Work Performed - Expert consulting, source code review, claim construction, expert reports, deposition.

Intel Corporation v. Future Link Systems*
Irell & Manella LLP, Los Angeles, CA USA
Expert Witness in Computer Architecture **2015 - 2018**
Case Subject Matter - Expert witness in the areas of PCI, PCI-Express, system-on-chip technology, and computer memory technologies.
Work Performed - Expert consulting, source code review, declarations, expert reports, deposition.

Advanced Touchscreen and Gesture Technologies, LLC* v. Samsung Electronics, America, Inc., et al.
Robins Kaplan LLP, Intellectual Property, Minnesota, USA
Expert Witness in Mobile Devices and User Interfaces **2015 - 2017**
Case Subject Matter - Expert witness in the analysis and reverse engineering of software systems pertaining to mobile devices, and human computer interfaces.
Work Performed - Expert consulting, declarations, expert reports.

Intellectual Ventures* v. Ericsson et al.
Dechert LLP, Los Angeles, CA, USA
Expert Witness in 3GPP standards and LTE Technologies, Intellectual Property 2014 - 2016
Case Subject Matter - Expert witness in 3GPP standards as they pertain to LTE cellular communications networks, in addition to system hardware and software design.
Work Performed - Expert consulting, source code review, declarations, claim construction, tutorials.

Papst Licensing GMBH & Co. KG.*
DiNovo & Price Ellwanger Hardy, Austin, TX USA
Expert Witness in FPGA Technologies, Intellectual Property **2014 - 2016**
Case Subject Matter - Consultant in FPGA computing platforms and design flow processes, prior art, and infringement analysis.
Work Performed - Expert consulting, claim construction.

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Locata LBS* v. Paypal Inc., et al.
Glaser Weil Fink Jacobs Howard Avchen & Shapiro, Los Angeles, CA, USA
Expert Witness in Geofencing Systems, Intellectual Property 2014 - 2015
Case Subject Matter - Expert witness in geofencing technology, geolocational technology, and systems architecture as it pertains to mobile cellular telecommunications and enterprise software systems.
Work Performed - Expert consulting, claim construction, expert reports, deposition testimony.

Cell and Network Selection LLC v. ZTE*
Pillsbury, Winthrop Shaw & Pittman, San Diego, CA, USA
Expert Witness in 3G/4G Cellular Technology, Intellectual Property 2014 - 2015
Case Subject Matter - Expert witness in technology pertaining to 3G, 3.5G, 3.75G and 4G wireless handset technology.
Work Performed - Expert consulting, claim construction, expert reports, deposition testimony.

CA Inc. D/B/A CA Technologies* v. AppDynamics, Inc.
Bracewell & Giuliani, Houston, TX, USA
Holland & Knight, Boston MA USA
Expert Witness in Enterprise Software Monitoring, Intellectual Property 2014 - 2015
Case Subject Matter - Expert witness in technology pertaining to dynamic runtime profiling of distributed software applications, specifically around Java and .NET technologies.
Work Performed - Expert consulting, source code review, declarations, expert reports, deposition testimony.

M Seven System Limited v. Leap Wireless International, Inc.* et al.
Glaser Weil Fink Jacobs Howard Avchen & Shapiro, Los Angeles, CA, USA
Expert Witness in 3G/4G Feature Phone Software Systems, Intellectual Property 2014
Case Subject Matter - Expert witness in the area of mobile telecommunications technology, particularly cellular handset hardware and software design.
Work Performed - Expert consulting, source code review.

Lunareye v. Passtime*.
Conley Rose, P.C., Austin, TX, USA
Expert Witness in GPS Tracking Solutions 2014
Case Subject Matter - Expert witness in the area of mobile GPS tracking solutions software and hardware systems.
Work Performed - Expert consulting.

Certain Wireless Devices With 3G and/or 4G Capabilities and Components Thereof, ITC Inv. No. 337-TA-868
Interdigital, Inc.*
Wilson, Sonsini, Goodrich & Rosati LLP, Austin, TX, USA
Expert Witness in 3G/4G Cellular Technology, Intellecutal Property 2013 - 2015
Case Subject Matter - Expert witness in software systems and hardware systems, as they pertain to 3G/4G cellular communications and standards.
Work Performed - Expert consulting, source code review, claim construction, declarations, expert report, depositions, ITC trial testimony.

Investment Technology Group* v. United States Internal Revenue Services
Expert Witness in Financial Services Technology 2013
Case Subject Matter - Expert witness in the area of high performance software systems targeting financial market services.
Work Performed - Expert consulting, source code review, declarations, depositions, testimony at hearing.

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Carrier Corporation v. Goodman Manufacturing*, et al.
Baker Botts LLP, Houston, TX USA
Expert Witness in Software and Hardware Systems, Intellectual Property 2013 - 2014
Case Subject Matter - Expert witness in the area of microprocessor based, serial distributed communications systems.
Work Performed - Expert consulting, source code review.

Gametek LLC* v. Facebook Inc. et al.
Collins, Edmonds, Porgorzelski, Schlather & Tower PLLC, Houston, TX USA
Expert Witness in Mobile Gaming Technologies, Intellectual Property **2013**
Case Subject Matter - Expert witness in internet based client-server software systems for mobile and web browser based gaming technology.
Work Performed - Expert consulting, source code review.

Ultimate Pointer LLC* v. Nintendo Co. LTD et al.
Conley Rose P.C., Houston, TX USA
Expert Witness in Console Based Video Game Technology, Intellectual Property 2013 - 2015
Case Subject Matter - Expert witness in hardware and software systems for console based video game technology.
Work Performed - Expert consulting, source code review, declarations, expert reports, deposition testimony.

Alliantgroup, L.P. v. Tax Point Advisors*
Jeffrey Feingold and Tax Point Advisors, Houston, TX USA
Expert Witness in Internet Technology **2013**
Case Subject Matter - Expert witness in IP based internet technology, packet spoofing and information systems.
Work Performed - Expert consulting, declarations.

Kerry T. Thibodeaux, M.D. v. American Lifecare Inc.*
Cox, Cox Filo, Camel & Wilson, Lake Charles, LA USA
Expert Witness in Medical Software Systems **2013**
Case Subject Matter - Expert witness in medical billing and expense recording enterprise software systems.
Work Performed - Expert consulting.

Opelousas General Hospital Authority et al v. Fairpay Solutions Inc*
Cox, Cox Filo, Camel & Wilson, Lake Charles, LA USA
Expert Witness in Medical Software Systems **2013**
Case Subject Matter - Expert witness in medical billing and expense recording enterprise software systems.
Work Performed - Expert consulting.

Wi-LAN USA, Inc. and Wi-LAN, Inc.* v. Alcatel-Lucent USA Inc.
Vinson Elkins LLP, Dallas, TX USA
Expert Witness in 3GPP LTE Technology, Intellectual Property **2012 - 2013**
Case Subject Matter - Reverse engineering, analysis and education of counsel in the 3GPP LTE specification, and related software and hardware systems.
Work Performed - Expert consulting, source code review, claim construction, expert declarations.

Wi-LAN USA, Inc. and Wi-LAN, Inc.* v. Ericsson Inc., and Telefonaktiebolaget LM Ericsson
Vinson Elkins LLP, Dallas, TX USA

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Expert Witness in 3GPP LTE Technology, Intellectual Property **2012 - 2013**
Case Subject Matter - Reverse engineering, analysis and education of counsel in the 3GPP LTE specification, and related software and hardware systems.
Work Performed - Expert consulting, source code review, claim construction, expert declarations.

E-Contact Technologies, LLC v. Dell Inc.*, et al.
Baker Botts LLP, Houston, TX USA
Expert Witness in Mobile Operating Systems, Intellectual Property **2012**
Case Subject Matter - Reverse engineering and analysis of the Android operating system as it pertained to mobile and tablet computing devices. Source code reverse engineering, system architecture and related analysis.
Work Performed - Expert consulting, source code review.

CheckFree Corporation* and CashEdge, Inc.* v. Metavante Corporation and Fidelity National Information Services, Inc.
Paul, Weiss, Rifkind, Wharton & Garrison LLP, New York, NY USA
Expert Witness in Banking and Billing Software Systems, Intellectual Property **2012**
Case Subject Matter - Software systems analysis and reverse engineering of large scale software based financial billing systems. Source code reverse engineering, claim chart generation, expert report generation and testimony.
Work Performed - Expert consulting, source code review.

Realtime Data, LLC v. NASDAQ*, Chase Bank*, Goldman Sachs* et al.
Proskauer Rose LLP, New York, NY USA
Expert Witness High Performance Software Systems, Intellectual Property **2012**
Case Subject Matter - Expert witness for joint defense counsel in the matter of large scale high frequency financial data aggregation platforms.
Work Performed - Expert consulting, claim construction, technical tutorials, declaration, expert reports, deposition testimony.

Realtime Data, LLC v. Thomson Reuters* et al.
Vinson & Elkins LLP, Austin, TX USA
Consultant in High Performance Software Systems, Intellectual Property **2011 - 2012**
Case Subject Matter - Expert witness for joint defense counsel in the matter of large scale high frequency financial data aggregation platforms.
Work Performed - Expert consulting, claim construction, technical tutorials, declaration, expert reports, deposition testimony.

General Electric Co.* v. Mitsubishi Heavy Industries Ltd.
Weil, Gotshal & Manges LLP, Dallas, TX USA
Expert Witness in Hardware/Software Analysis, Intellectual Property **2010 - 2011**
Case Subject Matter - Reverse engineering of real-time embedded system software source code and hardware system architecture pertaining to variable speed wind turbines and FPGA based subsystems.
Work Performed - Expert consulting, declarations, source code review.

Atlantic Specialty Insurance et al v. AE Outfitters Retail Company*, et al
Smith Mazure Director Wilkins Young & Yagerman, P.C., NY USA
Expert Witness in Embedded Hardware/Software Systems **2011**
Case Subject Matter - Hardware and software system analysis of real-time networked embedded computing systems as it pertains to fire alarm infrastructure and fault handling.
Work Performed - Expert consulting, technical tutorial, expert declarations.

Gamestop*, Inc v. Bexar Appraisal

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Brusniak and Blackwell PC, Dallas, TX USA
Expert Witness in Software Analysis, Intellectual Property Litigation **2011**
Case Subject Matter - Expert witness on the tangibility of software as it pertains to embedded computing, networking, and gaming platforms.
Work Performed - Expert consulting, expert declarations.

Quality Analytic Systems, Inc. v. Zebec Data Systems*
Rymer, Moore, Jackson & Echols, P.C., Houston, TX USA
Expert Witness in Software Systems **2011**
Case Subject Matter - Reverse engineering and software analysis of enterprise level internet based medical billing software systems.
Work Performed - Expert consulting, source code review, declarations, arbitration.

Passlogix, Inc. v. 2FA Inc.*
Expert Witness in Smart Card Middleware Solutions, Trade Secret Exposure **2010**
Case Subject Matter - Trade secret analysis of software and systems architecture as it pertains to optimal selection of smart card middleware solutions on a given computer system.
Work Performed - Expert consulting, expert declarations.

Terra Nova Sciences*. v. JOA Oil and Gas, B. V. et al.
Abraham & Watkins et al. LLP, Houston, TX USA
Expert Witness in Software Systems, Intellectual Property Litigation **2010**
Case Subject Matter - Expert software analyst of algorithms and geomechanics modeling systems as they pertain to oil well reservoirs.
Work Performed - Expert consulting, source code review.

Paltalk Holdings, Inc.* v. Sony Computer Entertainment America Inc. et al.
Heim Payne & Chorush LLP, Houston, TX USA
Software Analysis Expert, Intellectual Property Litigation **2010**
Case Subject Matter - Reverse engineering of internet based client-server video game console and server software architecture.
Work Performed - Expert consulting, source code review, infringement analysis.

Technomedia International, Inc.* v. International Training Services, Inc., et al.
Bracewell & Giuliani, LLP, Houston, TX USA
Expert Witness in Software Analysis, Contract Dispute **2010**
Case Subject Matter - Web enabled teaching materials as it pertains to oil well drilling. Analysis of internet based audio and video content delivery mechanisms and related website architecture.
Work Performed - Expert consulting, expert reports.

Gamestop, Inc* v. Bexar Appraisal
Brusniak and Blackwell PC, Dallas, TX USA
Expert Witness in Software Analysis, Tax Dispute **2009 - 2010**
Case Subject Matter - On the tangibility of software as it pertains to embedded computing, networking, and gaming platforms.
Work Performed - Expert consulting, expert reports.

Whetstone Electronics, LLC* v. Epson America, et al.
DiNovo & Price Ellwanger Hardy, Austin, TX USA
Expert Witness in System Analysis, Intellectual Property Litigation **2009 - 2011**
Case Subject Matter - Embedded computing systems pertaining to printer technology and computer hardware acceleration (microprocessors, DSP, FPGA and CPLD).
Work Performed - Expert consulting.

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Whetstone Electronics, LLC* v. Xerox Corporation, et al
DiNovo & Price Ellwanger Hardy, Austin, TX USA
Expert Witness in System Analysis, Intellectual Property Litigation 2009 - 2011
Case Subject Matter - Embedded computing systems pertaining to printer technology and computer hardware acceleration (microprocessors, DSP, FPGA and CPLD).
Work Performed - Expert consulting.

General Electric, Inc.* v. Mitsubishi Heavy Industries, Inc.
Vinson & Elkins LLP, Austin, TX USA
Expert Witness in Hardware and Software Analysis, Intellectual Property 2008 - 2009
Case Subject Matter - Real time embedded computing and hardware/software designs for variable speed wind turbines, including digital signal processing DSP and FPGA based subsystems.
Work Performed - Expert consulting, source code review, technical tutorials, declarations, expert reports, depositions, ITC trial preparation.

ecording enterprise software systems.
Work Performed - Expert consulting.

Wi-LAN USA, Inc. and Wi-LAN, Inc.* v. Alcatel-Lucent USA Inc.
Vinson Elkins LLP, Dallas, TX USA
Expert Witness in 3GPP LTE Technology, Intellectual Property 2012 - 2013
Case Subject Matter - Reverse engineering, analysis and education of counsel in the 3GPP LTE specification, and related software and hardware systems.
Work Performed - Expert consulting, source code review, claim construction, expert declarations.

Wi-LAN USA, Inc. and Wi-LAN, Inc.* v. Ericsson Inc., and Telefonaktiebolaget LM Ericsson
Vinson Elkins LLP, Dallas, TX USA
Expert Witness in 3GPP LTE Technology, Intellectual Property 2012 - 2013
Case Subject Matter - Reverse engineering, analysis and education of counsel in the 3GPP LTE specification, and related software and hardware systems.
Work Performed - Expert consulting, source code review, claim construction, expert declarations.

E-Contact Technologies, LLC v. Dell Inc.*, et al.
Baker Botts LLP, Houston, TX USA
Expert Witness in Mobile Operating Systems, Intellectual Property 2012
Case Subject Matter - Reverse engineering and analysis of the Android operating system as it pertained to mobile and tablet computing devices. Source code reverse engineering, system architecture and related analysis.
Work Performed - Expert consulting, source code review.

CheckFree Corporation* and CashEdge, Inc.* v. Metavante Corporation and Fidelity National Information Services, Inc.
Paul, Weiss, Rifkind, Wharton & Garrison LLP, New York, NY USA
Expert Witness in Banking and Billing Software Systems, Intellectual Property 2012
Case Subject Matter - Software systems analysis and reverse engineering of large scale software based financial billing systems. Source code reverse engineering, claim chart generation, expert report generation and testimony.
Work Performed - Expert consulting, source code review.

Realtime Data, LLC v. NASDAQ*, Chase Bank*, Goldman Sachs* et al.
Proskauer Rose LLP, New York, NY USA
Expert Witness High Performance Software Systems, Intellectual Property 2012
Case Subject Matter - Expert witness for joint defense counsel in the matter of large scale high

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frequency financial data aggregation platforms.
Work Performed - Expert consulting, claim construction, technical tutorials, declaration, expert reports, deposition testimony.

Realtime Data, LLC v. Thomson Reuters* et al.
Vinson & Elkins LLP, Austin, TX USA
Consultant in High Performance Software Systems, Intellectual Property 2011 - 2012
Case Subject Matter - Expert witness for joint defense counsel in the matter of large scale high frequency financial data aggregation platforms.
Work Performed - Expert consulting, claim construction, technical tutorials, declaration, expert reports, deposition testimony.

General Electric Co.* v. Mitsubishi Heavy Industries Ltd.
Weil, Gotshal & Manges LLP, Dallas, TX USA
Expert Witness in Hardware/Software Analysis, Intellectual Property 2010 - 2011
Case Subject Matter - Reverse engineering of real-time embedded system software source code and hardware system architecture pertaining to variable speed wind turbines and FPGA based subsystems.
Work Performed - Expert consulting, declarations, source code review.

Atlantic Specialty Insurance et al v. AE Outfitters Retail Company*, et al
Smith Mazure Director Wilkins Young & Yagerman, P.C., NY USA
Expert Witness in Embedded Hardware/Software Systems 2011
Case Subject Matter - Hardware and software system analysis of real-time networked embedded computing systems as it pertains to fire alarm infrastructure and fault handling.
Work Performed - Expert consulting, technical tutorial, expert declarations.

Gamestop*, Inc v. Bexar Appraisal
Brusniak and Blackwell PC, Dallas, TX USA
Expert Witness in Software Analysis, Intellectual Property Litigation 2011
Case Subject Matter - Expert witness on the tangibility of software as it pertains to embedded computing, networking, and gaming platforms.
Work Performed - Expert consulting, expert declarations.

Quality Analytic Systems, Inc. v. Zebec Data Systems*
Rymer, Moore, Jackson & Echols, P.C., Houston, TX USA
Expert Witness in Software Systems 2011
Case Subject Matter - Reverse engineering and software analysis of enterprise level internet based medical billing software systems.
Work Performed - Expert consulting, source code review, declarations, arbitration.

Passlogix, Inc. v. 2FA Inc.*
Expert Witness in Smart Card Middleware Solutions, Trade Secret Exposure 2010
Case Subject Matter - Trade secret analysis of software and systems architecture as it pertains to optimal selection of smart card middleware solutions on a given computer system.
Work Performed - Expert consulting, expert declarations.

Terra Nova Sciences*. v. JOA Oil and Gas, B. V. et al.
Abraham & Watkins et al. LLP, Houston, TX USA
Expert Witness in Software Systems, Intellectual Property Litigation 2010
Case Subject Matter - Expert software analyst of algorithms and geomechanics modeling systems as they pertain to oil well reservoirs.
Work Performed - Expert consulting, source code review.

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Paltalk Holdings, Inc.* v. Sony Computer Entertainment America Inc. et al.
Heim Payne & Chorush LLP, Houston, TX USA
Software Analysis Expert, Intellectual Property Litigation **2010**
Case Subject Matter - Reverse engineering of internet based client-server video game console and server software architecture.
Work Performed - Expert consulting, source code review, infringement analysis.

Technomedia International, Inc.* v. International Training Services, Inc., et al.
Bracewell & Giuliani, LLP, Houston, TX USA
Expert Witness in Software Analysis, Contract Dispute **2010**
Case Subject Matter - Web enabled teaching materials as it pertains to oil well drilling. Analysis of internet based audio and video content delivery mechanisms and related website architecture.
Work Performed - Expert consulting, expert reports.

Gamestop, Inc* v. Bexar Appraisal
Brusniak and Blackwell PC, Dallas, TX USA
Expert Witness in Software Analysis, Tax Dispute **2009 - 2010**
Case Subject Matter - On the tangibility of software as it pertains to embedded computing, networking, and gaming platforms.
Work Performed - Expert consulting, expert reports.

Whetstone Electronics, LLC* v. Epson America, et al.
DiNovo & Price Ellwanger Hardy, Austin, TX USA
Expert Witness in System Analysis, Intellectual Property Litigation **2009 - 2011**
Case Subject Matter - Embedded computing systems pertaining to printer technology and computer hardware acceleration (microprocessors, DSP, FPGA and CPLD).
Work Performed - Expert consulting.

Whetstone Electronics, LLC* v. Xerox Corporation, et al
DiNovo & Price Ellwanger Hardy, Austin, TX USA
Expert Witness in System Analysis, Intellectual Property Litigation **2009 - 2011**
Case Subject Matter - Embedded computing systems pertaining to printer technology and computer hardware acceleration (microprocessors, DSP, FPGA and CPLD).
Work Performed - Expert consulting.

General Electric, Inc.* v. Mitsubishi Heavy Industries, Inc.
Vinson & Elkins LLP, Austin, TX USA
Expert Witness in Hardware and Software Analysis, Intellectual Property 2008 - 2009
Case Subject Matter - Real time embedded computing and hardware/software designs for variable speed wind turbines, including digital signal processing DSP and FPGA based subsystems.
Work Performed - Expert consulting, source code review, technical tutorials, declarations, expert reports, depositions, ITC trial preparation.

Paltalk Holdings, Inc.* v. Microsoft Corporation
Heim Payne & Chorush LLP, Houston, TX USA
Technical Expert, Intellectual Property Litigation **2007 - 2008**
Case Subject Matter - Internet based client server console gaming architecture for real time experience.
Work Performed - Expert consulting, source code review, technical tutorials.

Paltalk Holdings, Inc.* v. Microsoft Corporation
Heim Payne & Chorush LLP, Houston, TX USA
Technical Expert, Intellectual Property Litigation **2007 - 2008**
Case Subject Matter - Internet based client server console gaming architecture for real time experi-

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ence.
Work Performed - Expert consulting, source code review, technical tutorials.

SuperSpeed Software, LLC* v. IBM Corporation
Heim Payne & Chorush LLP, Houston, TX USA
Technical Expert in Software Analysis, Intellectual Property Litigation **2007 - 2008**
Case Subject Matter - Computer database technology, parallel file systems and clustered computing.
Work Performed - Expert consulting, technical tutorial, source code review.

QPSX Developments 5 Pty Ltd.* v. Juniper Networks, Inc.
Fulbright and Jaworski LLP, Houston, TX USA
Technical Consultant, Intellectual Property Litigation **2006 - 2007**
Case Subject Matter - Data transmission algorithms for computer networks.
Work Performed - Consulting, claim construction, claim chart preparation, technical tutorials.

Commonwealth Scientific and Indus. Research Org.* v. Buffalo Tech. Inc.
Fulbright and Jaworski LLP, Houston, TX USA
Technical Consultant, Intellectual Property Litigation **2006 - 2007**
Case Subject Matter - High speed data rate network for wireless local area networks.
Work Performed - Consulting, claim construction, claim chart preparation, technical tutorials.

Microsoft Corporation v. Commonweatlh Scientific and Indus. Research Org.*
Fulbright and Jaworski LLP, Houston, TX USA
Technical Consultant, Intellectual Property Litigation **2006 - 2007**
Case Subject Matter - High speed data rate communications for wireless local area networks.
Work Performed - Consulting, claim construction, claim chart preparation, technical tutorials.

Tantivy Communications, Inc.* v. Lucent Technologies, Inc.
Fulbright and Jaworski LLP, Houston, TX USA
Technical Consultant, Intellectual Property Litigation **2004 - 2005**
Case Subject Matter - CDMA2000 based cellular networks, including data retransmission algorithms at multiple layers.
Work Performed - Consulting, claim construction, claim chart preparation, technical tutorials.

Volunteer Organizations

Rice Alliance for Technology and Entrepreneurship Austin, Texas, USA
Executive Committee **2009 - Present**
The Rice Alliance for Technology and Entrepreneurship strives to improve the entrepreneurial ecosystem of Central Texas by: helping entrepreneurs successfully found, fund, grow and exit new companies, helping investors successfully identify and engage with promising new ventures, and showcasing emerging technologies and business models to further educate and engage the community.

Capital Factory, TX USA
Mentor **2014 - Present**
Mentor, advisor and investor in one of the most successful start-up accelerators in the United States.

OwlSpark - Rice University, Houston, Texas, USA
Mentor **2014**
Mentor and advisor to university based early stage technology companies within Rice University's accelerator program.

Incubation Station, TX USA
Mentor **2013**
Incubation Station is an accelerator that brings together a consortium of Austins notable entrepreneurs, investors and advisors for the purpose of mentoring high-potential, market-validated

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consumer product companies to more effectively manufacture, distribute, market and grow their products and services.

Honors and Awards

Texas Instruments Fellowship Recipient
Nokia Grant Recipient
National Science Foundation Grant Recipient
Rice University Fellowship Recipient
Rensselaer Alumni Scholarship Recipient
Linear Tech / Mueller Scholarship Recipient
Rensselaer Polytechnic Institute: Graduated Cum Laude, Deans List All Semesters
Eta Kappa Nu - National Electrical and Computer Engineering Honors Society
IEEE Member - Institute of Electrical and Electronics Engineers
ACM Member - Association For Computing Machinery

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