

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD., MICRON TECHNOLOGY, INC.,
MICRON SEMICONDUCTOR PRODUCTS, INC., and
MICRON TECHNOLOGY TEXAS LLC,¹
Petitioners,

v.

NETLIST, INC.,
Patent Owner.

Case No. IPR2023-00454
Patent No. 11,093,417

PATENT OWNER SUR-REPLY

¹ Micron Technology, Inc., Micron Semiconductor Products, Inc., and Micron Technology Texas LLC filed a motion for joinder and a petition in IPR2023-01141 and have been joined as petitioners in this proceeding.

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EXHIBIT LIST

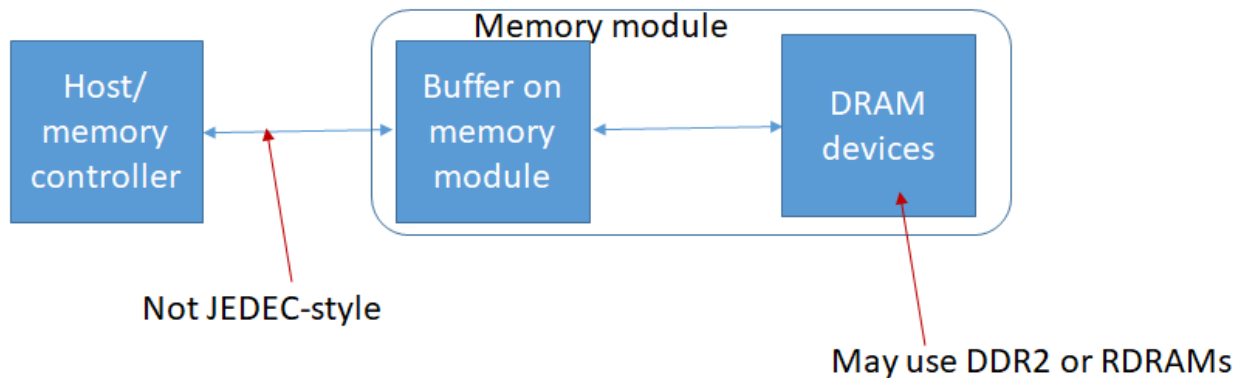
Exhibit No.	Document
EX2001	Crisp, R., “Direct Rambus Technology: The New Main Memory Standard,” <i>IEEE Micro</i> , pp. 18-28 (1997)
EX2002	Datasheet for Samsung’s RIMM MR16R1624 (Wolfe Deposition Exhibit 2100)
EX2003	Deposition Transcript of Dr. Andrew Wolfe from IPR2022-00615
EX2004	Samsung Datasheet on Rambus Direct RDRAM (Dec. 2001)
EX2005	Deposition Transcript of SungJoo Park in <i>Netlist, Inc. v. Samsung Electronics Co., Ltd.</i> , 2:21-cv-00463-JRG (E.D. Tex. November 23, 2022) (excerpt)
EX2006	Ex. 7 to Park Depo
EX2007	<i>Frequently Asked Questions</i> , What is the difference between a "bank" and a "rank?", Micron, https://web.archive.org/web/20141231144416/https://www.micron.com/support/faqs (last accessed Mar. 7, 2023).
EX2008	Reserved
EX2009	“XDR Architecture “ by Rambus (last modified December 2005), downloaded from https://web.archive.org/web/20110724044154/http://www.rambus.com/assets/documents/products/dl_0161_v0_8.pdf
EX2010	IDT, “DDR4 LRDIMMs Unprecedented Memory Bandwidth on Samsung DDR4 LRDIMM Enabled by IDT’s Register and Data Buffer,” downloaded from https://www.renesas.com/us/en/document/whp/ddr4-lrdimms-both-memory-capacity-and-speed

EX2011	“HyperCloud HCDIMM: Scaling the High Density Memory Cliff,” July 14, 2012, downloaded from https://web.archive.org/web/20120915083048/http://www.netlist.com/media/blog/hypercloud-memory-scaling-the-high-density-memory-cliff/
EX2012	<i>What is a Memory Rank</i> , Crucial: Micron, https://www.crucial.com/support/articles-faq-memory/what-is-a-memory-rank (last accessed Mar. 7, 2023)
EX2013	<i>Lecture 15: DRAM Main Memory Systems</i> , University of Utah, https://my.eng.utah.edu/~cs6810/pres/11-6810-15.pdf
EX2114	“Configuring and using DDR3 memory with HP ProLiant Gen8 Servers: Best Practice Guidelines for ProLiant Servers with Intel Xeon Processors” by HP, downloaded from https://web.archive.org/web/20121023195754/http://h20000.www2.hp.com/bc/docs/support/SupportManual/c03293145/c03293145.pdf
EX2015	Ganesh, B. et al., <i>Fully-Buffered DIMM Memory Architectures: Understanding Mechanisms, Overheads and Scaling</i> , HPCA (2007)
EX2116	Datasheet for Micron DDR2 SDRAM FBDIMM MT36HTF51272FD
EX2017	U.S. Patent No. 7,356,639 (“Perego-639”)
EX2018	Redline Comparison of EX1035 (U.S. Patent No. 7,363,422 to Perego) With Related U.S. Patent No. 7,356,639
EX2019	US District Court – Judicial Caseload Profile (as of December 31, 2022)
EX2020	JESD79-2B
EX2021	Amended Docket Control Order in <i>Netlist, Inc. v. Samsung Electronics Co. Ltd.</i> , 2:22-cv-00293-JRG (E.D. Tex. Feb. 1, 2023)

EX2022	Cover pleading of Samsung's invalidity contentions in <i>Netlist, Inc. v. Samsung Electronics Co. Ltd.</i> , 2:22-cv-00293-JRG (E.D. Tex. April 13, 2023)
EX2023	IPR2023-00203, Paper 8
EX2024	Declaration of Steven Przybylski, Ph.D.
EX2025	Rambus®, Advance Information, 64/72-Mbit (256Kx16/18x16d) Direct RDRAMDirect™ Data Sheet, Modified Mar 12, 1998
EX2026	Direct Rambus™ 1.6GB/sec memory Technology Disclosure, Oct. 15, 1997
EX2027	Direct Rambus™ RIMM™ Module Specification, Version 1.0
EX2028	Samsung Electronics, 256 Mbit XDR DRAM (F-die), 2M x 16(/8/4) bit x 8s Banks, Version 1.0, Jan. 2005
EX2029	Przybylski, Steven A., "NEW DRAM TECHNOLOGIES, A Comprehensive Analysis of the New Architectures," Second Edition, ©1996
EX2030	Claim Construction Memorandum Opinion and Order, Doc. 228, Case 2:22-cv-00293, filed Nov. 21, 2023
EX2031	JEDEC Standard No. 21-C (Rev. 1.0) SPD for DDR2 memory modules, http://web.archive.org/web/20050515195114/http://www.jedec.org:80/download/search/4_01_02_10R13.pdf
EX2032	Brent Keeth, <i>et. al.</i> , DRAM Circuit Design, Fundamental and High-Speed Topics, IEEE Press Series on Microelectronic Systems, ©2008
EX2033	Deposition Transcript of Dr. Andrew Wolfe, Nov. 4, 2023
EX2034	U.S. Patent No. 7,610,447 issued to Pergo <i>et al.</i> , Oct. 27, 2009
EX2035	Texas Instruments, Direct Rambus™ Clock Generator, CDCR83A, Aug. 2005

I. INTRODUCTION

Petitioner attempts to extend Perego's reference to JEDEC-compliant memory *devices* to the interface between the memory *module* and the host controller. But despite two rounds of briefing, Petitioner fails to identify in Perego any disclosure of a memory module with input chip-select signals or multiple ranks.



This is unsurprising because a JEDEC-compliant memory bus interface that depends on chip-select signals for selecting devices for operation would destroy Perego's "principles of operation" and render it "inoperable for its intended purpose." *Adidas AG v. Nike, Inc.*, 963 F.3d 1355, 1358-59 (Fed. Cir. 2020). Perego contemplates high-bandwidth, flexible, and upgradeable modules that permit direct addressing of any Rambus-style memory device, while also supporting DDR2 SDRAM memory devices and maintaining compatibility with future generations of memory devices. POR 23-24; EX2024, ¶129; EX1071, 2:15-30, 5:56-6:43, 10:63-67.

Petitioner attempts several unjustified leaps in reasoning that start with Perego's intended purpose of flexibility and end with a hypothetical memory module lacking that very flexibility, thereby destroying Perego's principles of operation. First, Petitioner relies on Perego's disclosure of DDR2 memory-device compatibility to suggest module and system changes unrelated to memory devices. For example, Petitioner contends that a POSITA would modify Perego's *module* and *primary channel* to comply with JESD21-C—which is not a part of any ground—despite Perego already accommodating JESD79-2 memory *devices* through protocol translation functionality in the buffer. Reply 11. Petitioner then incorrectly calls this hypothetical combination a “disclosed embodiment” to avoid justifying the necessary modifications. Reply 14-15. Petitioner then leverages this mischaracterization to suggest that Perego discloses many additional features, such as rank multiplication, which Perego does not even suggest. Reply 10. The net result is an inflexible system lacking the flexibility that Perego intended to provide. EX2024, ¶134. In other words, Petitioner's proposed combination would destroy the very flexibility it relies upon to argue that a POSITA would combine any JEDEC concepts with Perego in the first place. That is hindsight at its extreme.

A POSITA would not have been motivated to make these modifications, particularly because modifying Perego's primary channel to conform with JESD21-C and add a *chip-select bus*, which Petitioner now admits is *essential* to a JEDEC

memory system (Reply 5), would destroy the very flexibility that permits Perego to accommodate DDR2 SDRAMs as well as different types of memory devices on different modules, as well as the ability to address any device on a memory module and provide the same bandwidth regardless of how many memory modules are used per channel. *E.g.*, EX1071, 5:39-44, 7:20-29, 10:63-67, 14:62-15:2, 15:37-40, EX2024, ¶¶129, 134, 154 (“Any attempt to do this by a POSITA would change the operating principles of Perego regarding how to provide a high performance memory module that provides backward and forward compatibility”). For example, implementing a JEDEC-compliant bus between the memory controller and Perego’s memory modules would destroy the system’s ability to address memory devices independently, which enables broad re-configurability and upgrade flexibility. *E.g.*, EX2024, ¶129 (testifying that “compliance with [JESD21-C] would make the module non-functional for Direct RDRAMs and XDR DRAMs”); *id.*, ¶¶155, 159. In other words, implementing a JEDEC-compliant primary channel including input chip-select lines to Perego’s modules would not add functionality; it would defeat Perego’s purpose.

The Petition and Reply nonetheless contend that a POSITA would have such a motivation, based primarily on allegations that various aspects of the ’417 Patent’s claimed invention were “known.” But a POSITA’s alleged familiarity with certain aspects of both JEDEC-compliant modules and the very different modules of Perego

does not provide a motivation to combine those teachings, much less combine them in the hindsight-driven manner suggested in the Petition. *See Virtek Vision Int’l ULC v. Assembly Guidance Sys., Inc.*, 2024 WL 1292734, at *3 (Fed. Cir. Mar. 27, 2024) (“It does not suffice to meet the motivation to combine requirement to recognize that two alternative arrangements ... were both known in the art.”). After all, “obviousness concerns whether a skilled artisan not only ***could have*** made but ***would have*** been motivated to make the combinations or modifications of prior art to arrive at the claimed invention.” *Belden Inc. v. Berk-Tek LLC*, 805 F.3d 1064, 1073 (Fed. Cir. 2015). Petitioner fails to meet its burden because a POSITA ***would not*** have made the fundamental and undisclosed modifications to Perego’s module that would destroy its principles of operation.

II. LEVEL OF SKILL

Petitioner mischaracterizes Dr. Przybylski’s testimony. He did not admit error in his opinion regarding a POSITA’s familiarity with the internal design of memory devices, but rather his characterization of the number of pages dedicated to the topic in one book that post-dates the invention. EX1095, 149:9-16; EX2024, ¶69. The Reply omits Dr. Przybylski’s “principal point”—consistent with his declaration—“that the design of DRAMs and the design of memory system using DRAMs are two separate bodies of art,” and “the POSITA ... with relatively little ... experience being principally related to the design of memory systems would not be necessarily

familiar with all of the material” in those textbooks. EX1095, 150:17-25. Regardless, Petitioner identifies no aspect of this IPR that turns on this dispute.

III. CLAIM CONSTRUCTION OF “RANK”

Netlist’s POR and its expert’s declaration and deposition testimony clearly indicate that Netlist applied *Petitioner’s proposed construction* of “rank” without making any concessions. *E.g.*, POR 9 (“Solely for purposes of responding to this Petition, however, Netlist applies Petitioner’s proposed construction.”); EX2024, ¶165; EX1095, 447:23-448:11. Dr. Przybylski also correctly noted inconsistencies between this construction and the one adopted in co-pending district court litigation unrelated to the “one or more” aspect argued by Petitioner. *See* EX2024, ¶164.

IV. ATTACKS ON DR. PRZYBYLSKI DESIGNED TO DISTRACT FROM THE SERIOUS DEFECTS IN THE PETITION

Petitioner levels inappropriate and unsubstantiated attacks on the credibility of Netlist’s expert. As noted above, the question of whether a rank requires more than one memory device is not relevant because it did not form the basis of any opinions offered in this IPR. Petitioner also attacks Dr. Przybylski’s testimony regarding the JEDEC SPD standard (Reply 2 n.2), but fails to explain the relevance of that testimony. Further, the alleged inconsistencies do not withstand scrutiny. First, the “testimony of another Netlist expert” does not specifically address whether 8-bit wide memory modules were permitted. EX1101, 152:8-18 (testifying that

“values ranging from zero to 255 can be written,” which does not mean all values within that range were permitted). Second, the document itself does not support a contrary interpretation. *See* EX1095, 500:20-501:17, 502:6-503:12. And third, Petitioner has not established that Ellsberry’s Figure 10 complies with the SPD standard in EX2031, and Dr. Przybylski explained that Figure 10 does not appear to depict the full width of the module. EX1095, 503:13-504:17.

V. GROUND 1

A. Perego’s Teachings Are Incompatible with JEDEC Memory Module Standards

Petitioner continues to obfuscate the lines between memory *devices* (such as DDR2 SDRAMs) and memory *modules* (such as DDR2 RDIMMs). Despite Netlist explaining this distinction in detail (POR 20-21), as well as the lack of motivation to modify Perego’s teachings to achieve JEDEC compatible modules (POR 29-30), Petitioner simply asserts that Perego itself teaches such modules (*e.g.*, Reply 14 (asserting that “Perego itself expressly discloses using ... a JEDEC-style bus”); *id.* at 11 (asserting that “Perego does disclose using ... JEDEC-style memory busses”)), which is demonstrably false. Indeed, Petitioner elsewhere concedes that using a JEDEC bus allegedly would have been an obvious modification, rather than an express disclosure in Perego. *See* Reply 11.

Petitioner argues that JESD21-C need not be included in the Grounds because it is *only* cited for purposes of supporting a *motivation to combine* Perego and JESD79-2. *See* Reply 3-4, 13-14. As such, Petitioner may not rely on JESD21-C for missing limitations of the '417 Patent's challenged claims. Yet Petitioner continues to do so. *E.g.*, Reply 3 (relying on JESD21-C for "receiving chip select signals at the memory module"). Indeed, Petitioner must rely on JESD21-C for the input chip-select signals to the memory module, as Perego does not even mention the term "chip select," much less disclose or suggest such signals on the *primary channel*. The devices described in JESD79-2 receive chip-select signals from the module over the *secondary channel*, which are distinct from the chip-select signals received by the module from the memory controller over the primary channel as described in JESD21-C. This failure of proof alone provides reasons to reject this ground, as each claim requires input chip-select signals, which Petitioner now admits are "essential in a JEDEC-style memory system." Reply 5.

Perego nowhere discloses chip-select signals on the primary channel. That is because—even in embodiments supporting DDR2 memory devices—the protocol translation functionality in Perego's on-module buffer generates any chip-select signals expected by the SDRAMs and controls them via the secondary channels. POR 25-27; EX2024, ¶¶111, 132-33; EX1071, 9:54-57, 10:54-67. Petitioner argues that Perego merely teaches "translating protocols in general," which Petitioner

contends can also be used to implement rank multiplication. Reply 10. But Perego does not even hint at rank multiplication and does not organize memory devices into multiple ranks. EX2024, ¶¶160, 196. Indeed, Perego’s architecture is incompatible with the concept of ranks or rank multiplication because it directly accesses individual memory devices, and thus does not need to have multiple devices appear as a single, larger one to the memory controller. POR 33-34; EX2001, 23; EX2024, ¶¶155, 167-70. Furthermore, Perego does *not* disclose *generic* “translation” logic, very specific translation functionality that does not suggest rank multiplication (EX2024, ¶160): “Different types of memory devices may be included on different modules within a memory system, by employing buffer device 405 to translate protocols employed by controller 310 to the protocol utilized in a particular memory device implementation.” EX1071, 10:63-67. That functionality in turn relies on Perego’s disclosed channel architecture. EX2024, ¶137 (“Changing the primary channel of Perego ... would deprive Perego of the basis of its advantages, as well as compatibility with heterogeneous memory systems.”). JEDEC signaling, for example, would lack additional bank address bits, rendering the module non-functional for certain Rambus memory devices, and forward compatibility would be lost by downgrading the primary channel. EX2024, ¶¶129, 134.

The only backward compatibility disclosed by Perego relates to this protocol translation function to support both old and new types of memory devices within a

single memory system. EX1071, 6:37-43, 10:63-67. Petitioner contends, however, that Netlist ignores Perego's reference to existing and future *memory controllers*. Reply 12-13. Even if that characterization of Perego's disclosure is correct, Petitioner's theory would require modifying the *primary channel* and its interface to the *memory module*.² Perego discloses/suggests that memory device compatibility is achieved by modifying the buffer to implement protocol translation functionality, not altering the module to interface with different controllers. EX2024, ¶111. Those are two different approaches; disclosure of one does not suggest the other.

Petitioner also relies heavily on Perego's disclosure that alternate embodiments may replace control lines RQ in Fig. 4A with "individual control lines, for example, [RAS], [CAS], etc., and address lines." EX1071, 9:58-60. This disclosure does not suggest the use of a JEDEC-compliant primary channel. *Contra* Reply 6-8. First, this relates to secondary channel signal lines. EX1071, 9:43-60. Second, even earlier non-DDR "asynchronous DRAMs use the RAS and CAS signals as strobes." EX1069, 9. Notably, the enumerated control signals do not

² The Board appears to have misapprehended the distinction between memory devices and modules, mischaracterizing a DIMM (memory *module*) as a type of *device* with which Perego sought to preserve backward compatibility. ID 20.

mention WE, CKE, or especially chip select (CS) used by standard DDR2 SDRAMs. *See* EX1064, 49. Petitioner relies on the disclosure of chip-select signals in a patent cited by Perego (EX1081, Fig. 3) but ignores the context. That patent provides a prior art “comparison” to Perego’s inventions. EX1071, 6:27-30. Indeed, the appearance of CTM and CFM signal lines in Figure 4A would suggest a non-JEDEC memory (and corresponding non-JEDEC primary channel). EX2024, ¶150 (“A POSITA would understand ... that these signals are those of a Direct RDRAM channel.”).

Petitioner also wrongly contends that Perego teaches replacing the control lines in both the primary and secondary channels in Fig. 4A. The relevant disclosure contains no indication that modifications to the secondary channel (i.e., the lines between the memory devices 410a-h and the buffer 405) require changes to the primary channel (i.e., the lines between the memory module and the external memory controller). Petitioner appears to assume without explanation that it would be obvious to modify both RQ lines, but that ignores Perego’s buffer (the integral part of Perego) and the importance of backward and forward memory-device compatibility through the buffer’s protocol translation functionality. That translation functionality may require different control lines on the secondary channel for different signaling protocols needed by different memory device types (EX1071, 10:63-67), but that does not suggest modifying the primary channel, which would

destroy Perego's memory-device flexibility, backward-compatibility, and upgradeability as described above. EX2024, ¶137. Likewise, Perego's reference to multi-drop busses does not imply a JEDEC-compliant bus; Rambus systems can use a multi-drop bus. EX2024, ¶52.

Additionally, Perego contemplates an architecture where system bandwidth is maintained even when using only a single memory module. EX1071, 5:39-44. A chip-select bus in the primary channel would make this impossible because each standard memory slot is designed to receive a set number of chip-select signals (EX1079, ¶10), and when a memory module is removed from the slot, the chip-select signals intended for that slot cannot be redirected to another slot to maintain the bandwidth. Thus, a JEDEC-compliant module would also defeat Perego's intended purpose of providing a high-bandwidth memory architecture. EX1071, 2:15-30.

The mere fact that JEDEC-standardized modules dominated the market at the time of the invention also does not provide motivation to modify Perego. *See Virtek*, 2024 WL 1292734, at *3. There are fundamental differences between Perego's architecture and that of a JEDEC-style module (EX2024, ¶¶188-90; EX1069, 11-16), such that a POSITA would not have even started with Perego if they desired JEDEC compliance. Petitioner also contends that JEDEC DDR modules have equally high performance to the Rambus-style primary channel disclosed in Perego (Reply 13), but again ignores Dr. Przybylski's testimony, which undermines the

reasonableness of Petitioner's reliance on the Jacob book (EX1070, 23). *See* EX1095, 280:22-283:7 (identifying errors in the comparison and testifying that, under a proper analysis, "the peak bandwidth of direct Rambus would be substantially greater than that of a direct SDRAM memory subsystem"), 227:18-228:10 (noting that tradeoffs between DDR and Rambus memory systems described in the Jacobs book "are a very high level and not necessarily accurate in most or even many circumstances").

More importantly, a POSITA would not have converted Perego's modules and primary channel to comply with JEDEC standards because doing so would destroy Perego's "principles of operation" and render it "inoperable for its intended purpose." *Adidas*, 963 F.3d at 1358-59; *see* EX2024, ¶¶134, 139. Indeed, converting Perego to a JEDEC-compliant module to add a chip-select bus would destroy the very flexibility that permits Perego to accommodate either DDR2 SDRAMs or Rambus Direct RDRAMs, even within the same system. EX2024, ¶¶129, 154. For example, the lack of additional bank address bits permitting the controller to access memory devices individually would make Perego incompatible with the Rambus memory devices disclosed in the majority of its embodiments and limit the bandwidth of the memory system. EX2024, ¶¶129, 130, 134, 155, 159; POR 24, 28-30. As explained above in the Introduction, Petitioner would sacrifice the very flexibility upon which Petitioner built its case. Thus, implementing a JEDEC-

compliant primary channel would not be a “suitable option” in the context of Perego’s disclosed memory system. *Contra* Reply 13. The Reply ignores the destruction of this principle of Perego’s operation and intended purpose, which would dissuade a POSITA from making the proposed modifications. This deficiency provides another independent reason to reject this Ground.

Implementing a JESD21-C-compliant primary channel having chip-select networks in Perego would also preclude the buffer device that is the hallmark of Perego’s memory system. *E.g.*, EX2024, ¶135 (explaining that “an addressing scheme based on chip selects is incompatible with such variable width interfaces because the address of storage locations would change”); EX1071, Title (“Configurable Width Buffered Module”), Abstract. No prior art contemplates centralized buffers for JESD21-C-compliant modules. *See* EX1071, 6:27-33.

B. A POSITA Would Not Have Combined Perego and JESD79-2 to Implement a JEDEC-Compliant Memory Module

Petitioner’s Reply arguments in favor of combining Perego and JESD79-2 are misguided for many of the same reasons already articulated above. As previously established, neither Perego nor JESD79-2 relate to JEDEC-compliant memory modules. POR 20-24. And because Perego discloses using JESD79-2-compliant DDR2 SDRAMs in embodiments in which a protocol-translating buffer device is controlling them, JESD79-2 would not motivate a POSITA to modify Perego’s

primary channels, as the DDR2 SDRAM memory devices already receive the signals specified in JESD79-2 from the buffer. EX2024, ¶113.

Further, despite Petitioner’s statement that a POSITA would not need to modify the teachings of Perego to implement a JEDEC-compliant primary channel because that is “a disclosed embodiment” (Reply 14-15), Petitioner has admitted that this is a proposed obviousness modification (and thus is not “disclosed”). Reply 11. Nor, as explained above, would a POSITA be motivated to modify Perego’s teachings to do so, as Perego already teaches how to use DDR2 SDRAMs without such modifications, particularly when those modification would destroy Perego’s principles of operation and render it inoperable for its intended purpose. Section V.A, *supra*.

C. Ground 1 Does Not Teach or Suggest Claim Limitations Related to Input Chip-Select Signals, Corresponding Registered Chip-Select Signals, or a Plurality of Ranks Receiving Chip-Select Signals with Different Values

The Reply does not overcome Netlist’s explanation that Perego’s module does not receive chip-select input signals and a POSITA would not be motivated to add a chip-select bus to Perego’s primary channel. It simply references arguments already refuted above. The Reply also suggests that Perego’s reference to DDR2 SDRAM devices requires multiple ranks receiving chip-select signals with different values, but that presupposes the existence of multiple ranks. It is undisputed that Perego

does not even mention the terms “rank” or “chip select.” Nor would a POSITA understand Perego to disclose multiple ranks.

First, modules with non-JEDEC (e.g., Rambus) memory devices are incompatible with the JEDEC-created concept of ranks because they are accessed individually. POR 33-34; EX2001, 23; EX2024, ¶¶167-70; EX2012.

Petitioner’s theory regarding “target subsets” does not support the presence of ranks (POR 35-36; EX2024, ¶165), and Petitioner does not defend this theory in Reply other than attempting to claim that Netlist mischaracterized Dr. Wolfe’s testimony. But the additional testimony cited by Petitioner does not undermine Dr. Wolfe’s admission cited by Netlist. POR 35; EX2003, 202:8-204:10 (“I do not think that this paragraph [EX1070, 7:40-45] specifies how ranks are selected or enabled.”). Furthermore, Perego discloses that “target subsets” are selected with address bits, not chip-select signals. EX1071, 15:37-40.

Nor does Petitioner attempt to refute Netlist’s clarification that Jacob’s statements regarding “chip-select information” allegedly used in Rambus systems, which the Board relied on preliminarily in its Institution Decision (ID at 14-15; EX1069, 11-12), is “not accurate,” and that “chip-select information” as used by Jacobs in EX1069 “is not germane to the chip-select signals or lines required by JEDEC standards and the ’417 Patent.” POR 31-32; EX2024, ¶47.

Second, for the Fig. 3C embodiment that can use DDR2 SDRAMs, Dr. Przybylski explained that it comprises a single rank (and thus require a single registered chip-select signal), and Petitioner has not rebutted this testimony. POR 34; EX2024, ¶¶171-72. Likewise, Petitioner has not rebutted Dr. Przybylski's testimony that even if DDR2 SDRAMS could be used in Figs. 4A-4C, the alleged ranks of that embodiment, as well as the alleged rank of Fig. 3C, would not match the width of the module as required by Petitioner's construction. EX2024, ¶¶173-75.³ Furthermore, even if the memory devices received multiple chip-select signals with different values, these would be generated by the protocol translation functionality within the buffer on the module, and Perego does not disclose receiving corresponding input chip-select signals from the primary channel. EX2024, ¶¶111-13; Ex. 1071, 10:59-67, Fig. 2A. Dr. Brogioli, an expert for Netlist in a different IPR, did not admit otherwise. He merely observed that under Petitioner's theory in that case, there would be multiple devices per rank because devices in multiple channels were operating together. *See* EX1020, ¶¶93-94. And as discussed above,

³ In fact, for the 64-bit module the Petition relies on (Pet. 38), the module has to use x16 DDR2 devices and all four channels in order to obtain the 64 data bits per transaction. Thus, devices in all four channels operate together and are a single rank.

even if one modified Perego to implement multiple ranks on the module, there would be no chip-select signals on the primary channel.

D. Ground 1 Does Not Teach or Suggest the Claimed Data Delay Limitations

Limitation [1.f] requires data transfers to be registered through the claimed circuitry between the memory devices and the module bus.⁴ The claimed time delay must include delay in the data path; delay on the address/control path alone cannot satisfy this element. POR 36; EX2024, ¶179. The Petition provided little argument for this limitation, contending only that JESD21-C discloses adding “an additional clock cycle” based on registering the address and command signals and implying that this could be accomplished through JESD79-2’s disclosure of “Additive Latency.” Pet. 95 (citing EX1062, 68 n.1; EX1064, 12, 14). Petitioner suggested that it would have been obvious to add a clock cycle to Perego to comply with JEDEC standards and permit the circuitry “enough time to perform its functions,” including registering data signals with latches 597m-f using internal clock circuit 570a-b. Pet. 95-96. Netlist rebutted Petitioner’s argument based on the irrelevance of

⁴ Contrary to the Reply, the examiner considered substantially the same references. Paper 6, 60-61 (Ellsberry; Halbert; a family member of Perego sharing the same specification; and JESD79-2B, a slight update to JESD79-2); EX1002, 229-30.

control/address path delay and the fact that Additive Latency (AL) relates only to the latency of memory devices. POR 36-36; EX2024, ¶¶178-87.

Petitioner no longer argues that AL or registering address and control signals can satisfy this limitation. For example, Petitioner now claims that it cited EX1062's disclosure of delays on the address/control path only to suggest that any signal could be delayed by a full clock cycle (Reply 18), and that it cited EX1064's disclosure of AL only to show that latency is measured in full clock cycles (Reply 19-20). Petitioner now instead contends that a data buffer itself necessarily adds additional delay, and that it would have been obvious to add a full clock cycle of delay, as required by claim 9.

This is an entirely new rationale, relying on new and different evidence, which is not permitted in Reply. *See, e.g., Intelligent Bio-Systems, Inc. v. Illumina Cambridge Ltd.*, 821 F.3d 1359, 1369 (Fed. Cir. 2016) (Petitioners must “adhere to the requirement that the initial petition identify ‘with particularity’ the ‘evidence that supports the grounds for the challenge to each claim.’” (quoting 35 U.S.C. § 312(a)(3))); accord 37 C.F.R. § 42.104. “[P]etitioner may not submit new evidence or argument in reply that it could have presented earlier” TPG 73. And Petitioner may not introduce an “entirely new rationale,” *Intelligent Bio-Systems*, 821 F.3d at 1370, or rely “on previously unidentified portions of a prior-art reference

to make a meaningfully distinct contention,” *Ariosa Diagnostics v. Verinata Health, Inc.*, 805 F.3d 1359, 1367 (Fed. Cir. 2015).

The Reply is problematic in other respects as well. For example, Petitioner’s new argument that it would have been obvious to insert delay in the data path to permit time to buffer the data reflects the inventors’ insights, not a POSITA’s knowledge. EX1001, 22:46-49 (“This extra cycle of time in certain embodiments advantageously provides sufficient time budget to add a buffer which electrically isolates the ranks of memory devices 30 from the memory controller 20.”). Petitioner also distorts the testimony of Dr. Przybylski, who did not admit that there would be a motivation to add a buffer on the data path. The quoted testimony relates to the inventors’ insight, not a recognition existing prior to the ’417 Patent. *See* EX1095, 136:3-137:11. And his testimony regarding “examples of a register or buffer that includes a cycle of delay” made no reference to data buffers. *Id.* at 135:2-17.

Petitioner focuses extensively on AL and CAS Latency (CL) disclosed in JESD79-2 and their programmability, but these value relate to memory device latency, not the overall latency of the module. EX2024, ¶180. And Netlist did rebut Petitioner’s preclusion argument based on a prior Board decision, not because it “was unrelated to data transfers” (Reply 20), but rather because it included different limitations. POR 38-39.

Petitioner also asserts that Netlist conceded that Perego's clock circuits 570a-b are needed for proper data capture by Perego's data buffer, but Petitioner ignores the true function and purpose of the clock circuits 570a-b and Netlist's arguments regarding them, including Dr. Przybylski's un rebutted testimony that they are "irrelevant to the question of whether there is an extra clock cycle of latency added to the path through the buffer circuit." EX2024, ¶¶184-86; POR 39. In sum, Petitioner failed to carry its burden of demonstrating that Perego and JESD79-2 teach or suggest limitation [1.f].

VI. GROUND 2

A. Ellsberry Is Not a "Printed Publication" Under § 311(b)

Petitioner cites no binding authority permitting the Board to consider Ellsberry a "printed publication" under § 311(b). The Board decisions cited by Petitioner are not precedential, and the MPEP "does not have the force of law or the force of the rules in Title 37." MPEP, Foreword. The cited Federal Circuit case does not address this issue and merely states that Congress presumably drafted § 311(b) with reference to § 301(a), but that re-examination provision—properly interpreted—likewise excludes references such as Ellsberry, which were not published until after the priority date and never issued as patents.

B. The '417 Patent Is Entitled to the '087 Provisional's Priority Date

As previously explained (POR 46), Netlist is only required to address arguments raised in the Petition and need not address points not in dispute, such as elements that Petitioner does not contend are missing from the '087 Provisional. Regardless, Netlist presented evidence indicating where disclosure in the '087 Provisional may be found for each claim element, and the Reply *fails to identify even a single additional limitation* allegedly lacking support in the exemplary citations provided in the POR.

The chart provided by Netlist also does not rely on obviousness. Notably, the chart specifically identifies supportive citations *in the '087 Provisional [EX1005] for each limitation*. POR 46-49; EX2024, ¶92. Again, the only limitations in dispute relate to the “data buffer control signals,” which Netlist addressed in great detail. That is all that was required, as supported by Petitioner’s own cited case. *See Continental Auto. Sys., Inc. v. Intellectual Ventures II LLC*, IPR2022-00972, Paper 49, at 24-25 (PTAB Dec. 5, 2023) (requiring patent owner to identify written description support in only the single disputed claim element).

Petitioner fails to rebut Dr. Przybylski’s explanation of a POSITA’s understanding that the '087 Provisional provides written description support for the “data buffer control signals.” POR 43-44; EX2024, ¶¶82-83. Petitioner’s four arguments lack merit. First, Petitioner repeats its contention that write commands

could instead rely on chip-select signals to select the appropriate rank. But Petitioner fails to acknowledge, much less rebut, Dr. Przybylski's explanation that "the RBDL must understand *when* to forward data from the memory bus to the rank data buses," which the data buffer control signals would provide. EX2024, ¶84; POR 44. Second, Petitioner improperly faults the '087 Provisional for not *expressly* disclosing the claimed signals for determining the appropriate rank for a read command instead of considering how a POSITA would understand the application's disclosures. POR 42-44. But as Petitioner acknowledges, a "patent need not teach, and preferably omits, what is *well known* in the art." Reply 9 (citing MPEP § 2164.01).

Third, Petitioner presents an improper new argument, speculating that data buffer control signals could be received directly from the memory controller. Petitioner again ignores Dr. Przybylski's testimony that a POSITA would understand that the MUX/DEMUX "necessarily would receive control signals (i.e., the claimed 'data buffer control signals') from the command decode circuitry," which a POSITA would understand "necessarily ... would receive commands from an external memory controller and would include command decode circuitry to interpret those commands." EX2024, ¶¶81-82; POR 43-44; EX1005, ¶7 (disclosing that the RBDL "comprises a logic translation element"). Fourth, Petitioner again suggests that the DQS preamble could control data transfers through the buffer. Petitioner contends that an Intel patent refutes the notion that it would be impossible

to detect such preambles in any instance. But that is not Netlist’s position. As explained by Dr. Przybylski, “at least some of the time, there is no discernable transition in the voltage on the DQS signal at the start of the preamble,” which results in the “lack of a *reliably discernable* preamble,” and thus a POSITA would understand that such preambles cannot be *relied upon* to control data transfers through the buffer. EX2024, ¶¶86-88; POR 45; EX1095, 303:5-308:6.

C. No Motivation to Combine Ellsberry with Ground 1

Petitioner does not dispute Netlist’s argument that the alleged relevance of JEDEC standards would not motivate a POSITA to combine the teachings of Ellsberry, JESD79-2, and Perego. POR 50. Petitioner instead relies on Perego’s purported ability to perform rank multiplication. But “[t]here is no suggestion within the disclosure of Perego that the memory controller is presented with a view of the memory system in which it appears to the memory controller that two or more memory devices are actually one larger device.” EX2024, ¶160; *see also id.*, ¶196 (“the concept of rank multiplication is completely foreign to Perego”). A POSITA would not modify the teachings of Perego to implement a JEDEC-compliant module or rank multiplication due to, among other things, the loss of flexibility to support “different types of memory devices on different modules,” which provides “cost savings and tradeoffs ... available to a system architect at all times.” EX2024, ¶203 (citing Ex. 1071, Figure 5A, Figure 5B, 9:50-57, 10:54-67, 11:1-25, 11:56-12:3);

POR 29-30; EX2024, ¶¶134, 140. Petitioner argues that Perego’s buffer may “render the *type of memory device* transparent to the system” (Reply 26), but that is not the same as the organizational transparency of rank multiplication.

Petitioner does not dispute that “Ellsberry’s distributed data buffers are different from Perego’s centralized buffer.” Reply 27. Petitioner argues that both approaches were “known alternatives,” but that is not sufficient. *See, e.g., Virtek*, 2024 WL 1292734, at *3; *Belden*, 805 F.3d at 1073 (“[O]bviousness concerns whether a skilled artisan not only *could have* made but *would have* been motivated to make the combinations or modifications”). Petitioner also takes issue with the date of EX2010, but does not refute EX2010’s discussion of the significant differences between centralized and distributed buffer architectures. Petitioner likewise fails to address the differences between Ellsberry’s buffering of DQ signals and Perego’s “much more comprehensive change to the memory system architecture” as disclosed in Petitioner’s own references. EX2024, ¶202; POR 51-52; EX1073, ¶¶12, 47, Figs. 5, 6; EX1071, Abstract. A POSITA would not have combined the teachings of these references.

VII. GROUND 3: HALBERT DOES NOT SUPPORT OBVIOUSNESS

Halbert discloses neither multiple “ranks” according to Petitioner’s proposed construction nor chip-select signals with different values. Petitioner’s arguments to the contrary rest entirely on Halbert’s use of the word “generally” as purportedly

implying that Halbert’s alleged “ranks” may not operate in lockstep. But Halbert contains no such disclosure, and operating “ranks” 140 and 142 independently would alter Halbert’s “principles of operation” and render it “inoperable for its intended purpose,” including causing it to lose half of the data. *Adidas*, 963 F.3d at 1358-59; *see* POR 52-54; EX2024, ¶¶208-16. Indeed, the Board has rejected the same theory in another IPR involving Halbert and a Netlist patent reciting similar language. *See* IPR2022-00745, Paper 34, at 15 (PTAB Oct. 30, 2023) (Even if Halbert could “be configured to operate with active and non-active signals such that ranks 140 and 142 do not operate concurrently,” “operating only one of the ranks at a time” would defeat the purpose of increasing memory throughput); EX1078, 3:43-48 (disclosing “allowing a faster system memory data bus to operate at full speed with slower memory devices”).

Petitioner also fails to rebut Netlist’s arguments that Halbert lacks disclosure of registering data transfers for an amount of time delay. Contrary to the Reply, the Petition’s discussion of these limitations (Pet. 124-26) does not specifically identify delay in the data path as distinct from delay attributable to the address/control path. EX2024, ¶217; POR 54. Further, even Petitioner’s new Reply argument interpreting an alleged delay through the data interface circuit in Halbert is only 0.5 clock cycles. Reply 29.

VIII. NO SIMULTANEOUS INVENTION

Petitioner's simultaneous invention theory rests entirely on the premise that multiple references allegedly disclose "rank multiplication." But rank multiplication is only one concept implicated by the claimed inventions, and not even a required one at that. Simultaneous invention requires invention of all of the claimed elements, which Petitioner falls far short of demonstrating. *See, e.g., Endo Pharms. Inc. v. Actavis LLC*, 922 F.3d 1365, 1378 n.14 (Fed. Cir. 2019).

IX. CONCLUSION

For at least these reasons and those articulated in the POR, the Board should decline to find the challenged claims of the '417 Patent unpatentable.

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Respectfully submitted,

/Philip Warrick/

H. Annita Zhong (Reg. No. 66,530)
Jason Sheasby (*pro hac vice* to be requested)
IRELL & MANELLA LLP
1800 Avenue of the Stars, Suite 900
Los Angeles, CA 90067
Tel: (310) 277-1010
Fax: (310) 203-7199

Jonathan M. Lindsay (Reg. No. 45,810)
IRELL & MANELLA LLP
840 Newport Center Dr., Ste. 400
Newport Beach, California 92660
Telephone: (949) 760-0991
Facsimile: (949) 760-5200

Philip Warrick (Reg. No. 54,707)
IRELL & MANELLA LLP
750 17th Street NW, Ste. 850
Washington, DC 20006
Telephone: (202) 777-6500

Email: NetlistIPR@irell.com

Counsel for Patent Owner Netlist, Inc.

CERTIFICATE OF WORD COUNT

I hereby certify, pursuant to 37 C.F.R. section 42.24, that the foregoing Patent Owner Sur-Reply contains 5,566 words, excluding the words in the table of contents, table of authorities, mandatory notices under section 42.8, this certificate of word count, certificate of service, and exhibit list. The word count is based on the word count of the Microsoft Word program used to prepare the Patent Owner Sur-Reply.

/Philip Warrick/
Philip Warrick (Reg. No. 54,707)

CERTIFICATE OF SERVICE

I hereby certify, pursuant to 37 C.F.R. section 42.6, that on April 3, 2024, a complete copy of the **PATENT OWNER'S SUR-REPLY** was served upon the following, by ELECTRONIC MAIL:

BAKER BOTTS L.L.P.

Eliot D. Williams, Reg. No. 50,822
Theodore W. Chandler, Reg. No. 50,319
Ferenc Pazmandi, Reg. No. 66,216
John F. Gaustad, Reg. No. 69,522
Brianna L. Potter, Reg. No. 76,748
DLSamsungNetlistIPRs@BakerBotts.com

WINSTON & STRAWN LLP

Juan C. Yaquian, Reg. 70,755
Michael Rueckheim
James C. Lin
Winston-IPR-NetList@winston.com

/Susan M. Langworthy/
Susan M. Langworthy