

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD., MICRON TECHNOLOGY, INC.,
MICRON SEMICONDUCTOR PRODUCTS, INC., and
MICRON TECHNOLOGY TEXAS LLC,[†]

Petitioner,

v.

NETLIST, INC.,

Patent Owner

IPR2023-00454
Patent 11,093,417 B2

EXHIBIT 1115:

Petitioner's Demonstratives for Oral Argument on May 3, 2024

[†] Micron Technology, Inc., Micron Semiconductor Products, Inc., and Micron Technology Texas LLC filed a motion for joinder and a petition in IPR2023-01141 and have been joined as petitioners to this proceeding.

Petitioner Samsung Electronics Co., Ltd.'s Oral Argument for PTAB Hearing

Samsung Electronics Co., Ltd. v. Netlist, Inc.,

IPR2023-00454 and IPR2023-00455 (U.S. Patent Nos. 11,093,417 and 9,858,215)

May 3, 2024

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OVERVIEW

1

OVERVIEW OF '417 AND '215 PATENTS, AND INSTITUTED GROUNDS

'417 AND '215 PATENTS

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

'215 Patent

(12) United States Patent Solomon et al.	(10) Patent No.: US 9,858,215 B1 (45) Date of Patent: Jan. 2, 2018
(54) MEMORY MODULE WITH DATA BUFFERING (71) Applicant: Netlist, Inc. , Irvine, CA (US) (72) Inventors: Jeffrey C. Solomon , Irvine, CA (US); Jayesh R. Bhakta , Cerritos, CA (US) (73) Assignee: Netlist, Inc. , Irvine, CA (US)	continuation of application No. 11/335,875, filed on Jan. 19, 2006, now Pat. No. 7,532,537, which is a continuation-in-part of application No. 11/173,175, filed on Jul. 1, 2005, now Pat. No. 7,289,386, which is a continuation-in-part of application No. 11/075,395, filed on Mar. 7, 2005, now Pat. No. 7,286,436. Provisional application No. 60/645,087, filed on Jan. 19, 2005, provisional application No. 60/588,244, filed on Jul. 15, 2004, provisional application No. 60/550,668, filed on Mar. 5, 2004, provisional application No. 60/575,595, filed on May 28, 2004, provisional application No. 60/590,038, filed on Jul. 21, 2004.

**No support for claims
before July 1, 2005**

'417 Patent (continuation of the '215 Patent)

(12) United States Patent Solomon et al.	(10) Patent No.: US 11,093,417 B2 (45) Date of Patent: Aug. 17, 2021
(54) MEMORY MODULE WITH DATA BUFFERING	continuation of application No. 11/335,875, filed on Jan. 19, 2006, now Pat. No. 7,532,537, which is a continuation-in-part of application No. 11/173,175, filed on Jul. 1, 2005, now Pat. No. 7,289,386, which is a continuation-in-part of application No. 11/075,395, filed on Mar. 7, 2005, now Pat. No. 7,286,436. Provisional application No. 60/645,087, filed on Jan. 19, 2005, provisional application No. 60/588,244, filed on Jul. 15, 2004, provisional application No. 60/550,668, filed on Mar. 5, 2004, provisional application No. 60/575,595, filed on May 28, 2004, provisional application No. 60/590,038, filed on Jul. 21, 2004.
(71) Applicant: Netlist, Inc. , Irvine, CA (US)	
(72) Inventors: Jefferey C. Solomon , Irvine, CA (US); Jayesh R. Bhakta , Cerritos, CA (US)	
(73) Assignee: Netlist, Inc. , Irvine, CA (US)	
Related U.S. Application Data continuation of application No. 14/715,486, filed on May 18, 2015, now Pat. No. 9,858,215, which is a	

**No support for claims
before July 1, 2005**

'417/'215 Patent problem: Cost of high-density memory

1Gb:



512Mb:



512Mb:



Most high-density memory modules are currently built with 512-Megabit ("512-Mb") memory devices wherein each memory device has a 64 M×8-bit configuration. For example, a 1-Gigabyte ("1-GB") memory module with error checking capabilities can be fabricated using eighteen such 512-Mb memory devices. Alternatively, it can be economically advantageous to fabricate a 1-GB memory module using lower-density memory devices and doubling the number of memory devices used to produce the desired word width. For example, by fabricating a 1-GB memory module using thirty-six 256-Mb memory devices with 64 M×4-bit configuration, the cost of the resulting 1-GB memory module can be reduced since the unit cost of each 256-Mb memory device is typically lower than one-half the unit cost of each 512-Mb memory device. The cost savings can be significant, even though twice as many 256-Mb memory devices are used in place of the 512-Mb memory devices. For example, by using pairs of 512-Mb memory devices rather than single 1-Gb memory devices, certain embodiments described herein reduce the cost of the memory module by a factor of up to approximately five.

'215: EX1001 at 13:51-14:4

'417: EX1001 at 15:63-16:16

'417/'215 Patent solution: Rank multiplication (with "fork in the road") so two ranks of low-density memory appear as one rank of high-density memory

Two chip selects on the memory module (10) for **two** (lower-density) physical ranks

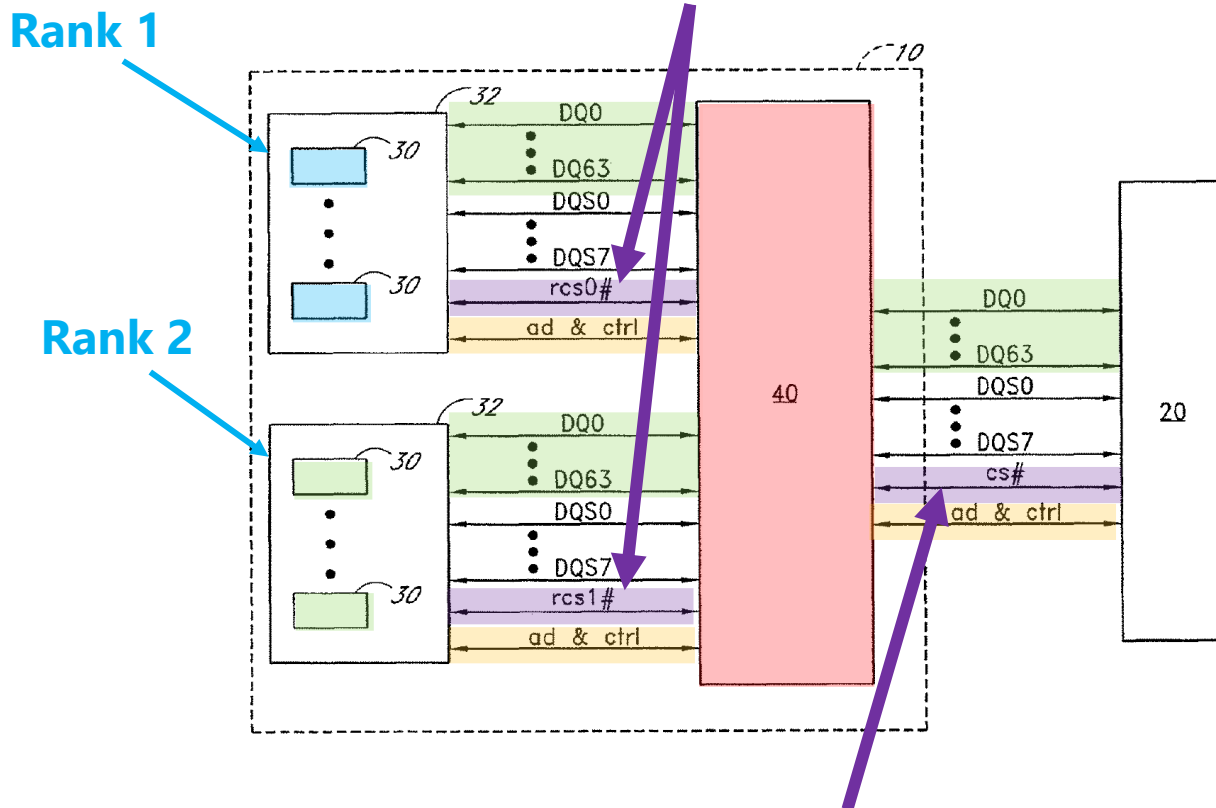


FIG. 1 One chip select from the host's memory controller (20) for **one** (higher density) virtual rank

In certain embodiments described herein in which the number of ranks 32 of the memory module 10 is doubled or quadrupled, the circuit 40 generates a set of output address and command signals so that the selection decoding is transparent to the computer system. However, in certain

The DRAM devices of a memory module are generally arranged as ranks or rows of memory, each rank of memory generally having a bit width. For example, a memory module in which each rank of the memory module is 64 bits wide is described as having an "x64" organization. Simi-

During operation, the ranks of a memory module are selected or activated by address and command signals that are received from the processor. Examples of such address and command signals include, but are not limited to, rank-select signals, also called chip-select signals. Most computer

'417: EX1001 at 14:25-:29, 2:47-:51, 2:65-3:2
'215: EX1001 at 12:13-:17, 2:41-:55, 2:59-:63

'417/'215 solution: Rank multiplication with "fork in the road" in buffer circuit (40) to avoid collisions

transparent to the computer system. However, in certain such embodiments, there are memory device boundaries of which the computer system is unaware, so there are occasions in which BBARX occurs without the cognizance of the memory controller 20 of the computer system. As shown in FIG. 7, the last data strobe of memory device "a" collides with the pre-amble time interval of the data strobe of memory device "b," resulting in a "collision window."

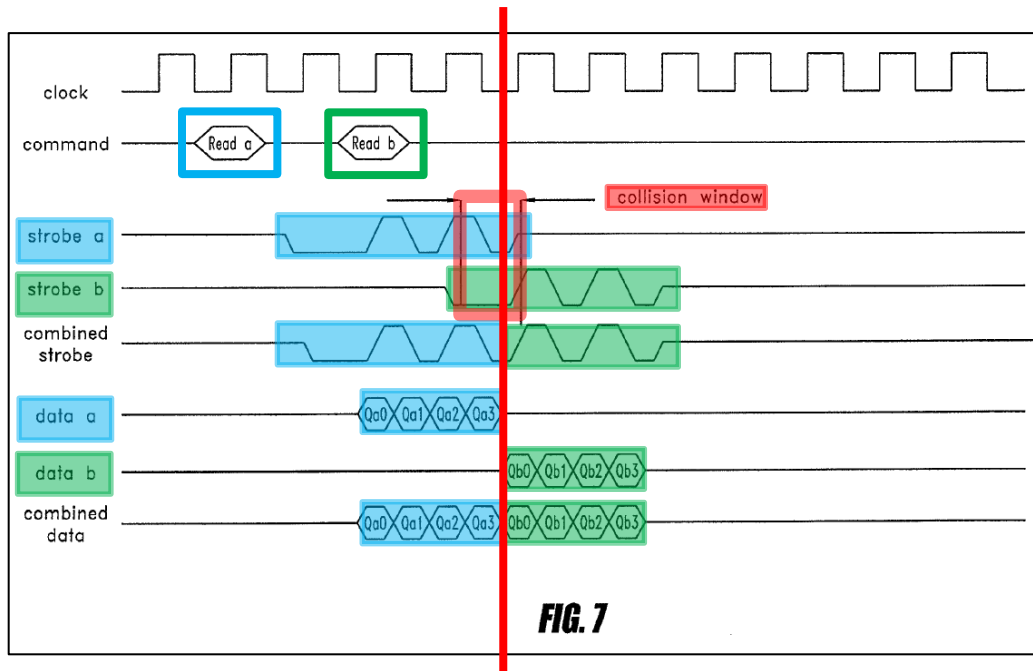


FIG. 7

'417: EX1001 at 14:29-:36 & Fig. 7
'215: EX1001 at 12:17-:24 & Fig. 7

Rank a

Rank b

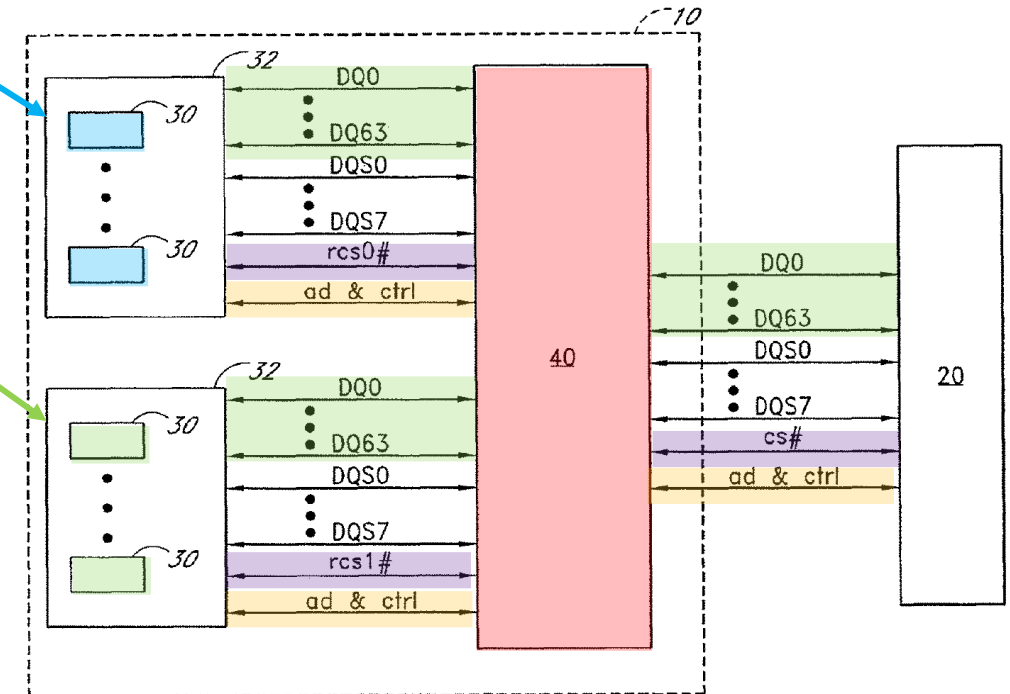


FIG. 1

'417: Paper 1 (Pet.) at 10-15, 79-83
'215: Paper 1 (Pet.) at 10-14, 67-71

'417/'215: Buffer circuit (40) requires one extra clock cycle for address/control and data

In certain embodiments, the circuit 40 comprises the SPD device 240 which reports the CAS latency (CL) to the memory controller of the computer system. The SPD device 240 of certain embodiments reports a CL which has one more cycle than does the actual operational CL of the memory array. In certain embodiments, data transfers between the memory controller and the memory module are registered for one additional clock cycle by the circuit 40. The additional clock cycle of certain embodiments is added to the transfer time budget with an incremental overall CAS latency. This extra cycle of time in certain embodiments advantageously provides sufficient time budget to add a buffer which electrically isolates the ranks of memory devices 30 from the memory controller 20. The buffer of certain embodiments comprises combinatorial logic, registers, and logic pipelines. In certain embodiments, the buffer adds a one-clock cycle time delay, which is equivalent to a registered DIMM, to accomplish the address decoding. The one-cycle time delay of certain such embodiments provides sufficient time for read and write data transfers to provide the functions of the data path multiplexer/demultiplexer. Thus, for example, a DDR2 400-MHz memory system in accordance with embodiments described herein has an overall CAS latency of four, and uses memory devices with a CAS latency of three. In still other embodiments, the SPD device

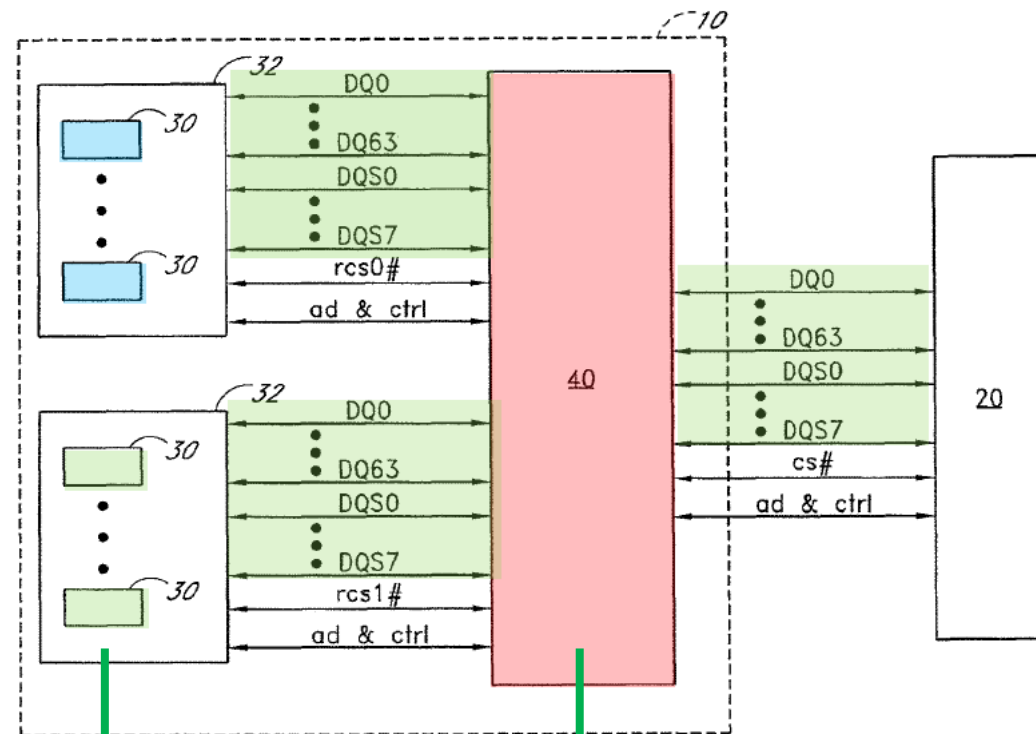


FIG. 1

3 clock cycles + 1 clock cycle = 4 clock cycles

'417: EX1001 at 22:36:-60

'215: EX1001 at 20:22:-46

'417: Paper 1 (Pet.) at 12-15

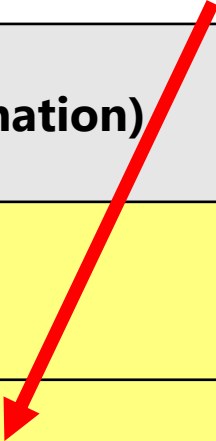
'215: Paper 1 (Pet.) at 12-14

INSTITUTED GROUNDS & PRIOR ART

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Instituted Grounds

Dispute whether Ellsberry (filed June 1, 2005) is prior art



Grounds	'417 Patent	'215 Patent	Prior art (§103(a) combination)
1	Claims 1-15	Claims 1-29	<u>Perego</u> + <u>JESD79-2</u>
2	Claims 1-15	Claims 1-29	Ground 1 + <u>Ellsberry</u>
3	Claims 1-15	Claims 1-29	Ground 1 + <u>Halbert</u>
4		Claims 1-29	Ground 1 + <u>Matsui2</u>

'417: Paper 1 (Pet.) at 5; Paper 11 (ID) at 5, 42
'215: Paper 1 (Pet.) at 5; Paper 11 (ID) at 4, 34

Prior Art: Perego (U.S. Patent No. 7,363,422) [EX1071]

(12) **United States Patent**
Perego et al.

(10) **Patent No.:** **US 7,363,422 B2**
(45) **Date of Patent:** ***Apr. 22, 2008**

(54) **CONFIGURABLE WIDTH BUFFERED
MODULE**

(75) **Inventors:** **Richard Perego**, San Jose, CA (US);
Fred Ware, Los Altos Hills, CA (US);
Ely Tsern, Los Altos, CA (US)

(73) **Assignee:** **Rambus Inc.**, Los Altos, CA (US)

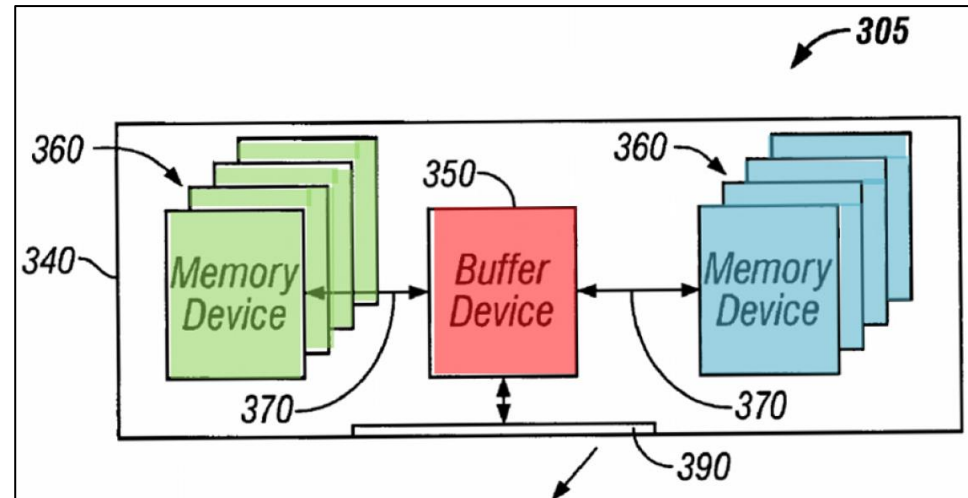
Buffer device 350 provides a high degree of system flexibility. New generations of memory devices may be phased in with controller 310 or into memory system 300 by modifying buffer device 350. Backward compatibility with existing generations of memory devices (i.e., memory devices 360) may also be preserved. Similarly, new generations of controllers may be phased in which exploit features of new generations of memory devices while retaining backward compatibility with existing generations of memory devices.

EX1071 at 6:34-43

(21) **Appl. No.:** **10/766,131**

(22) **Filed:** **Jan. 28, 2004**

(65) **Prior Publication Data**
US 2004/0186956 A1 Sep. 23, 2004



EX1071 at Fig. 3B

Prior Art: JESD79-2 standard for DDR2 memory [EX1064]

JEDEC **DDR2 SDRAM SPECIFICATION** **SEPTEMBER 2003**

1.2 Input/Output Functional Description

Symbol	Type	Function
CS	Input	Chip Select: All commands are masked when CS is registered HIGH. CS provides for external Rank selection on systems with multiple Ranks. CS is considered part of the command code.
RAS, CAS, WE	Input	Command Inputs: RAS, CAS and WE (along with CS) define the command being entered.
BA0 - BA2	Input	Bank Address Inputs: BA0 and BA1 for 256 and 512Mb, BA0 - BA2 define to which bank an Active, Read, Write or Precharge command is being applied. Bank address also determines if the mode register or extended mode register is to be accessed during a MRS or EMRS cycle.
A0 - A15	Input	Address Inputs: Provided the row address for Active commands and the column address and Auto Precharge bit for Read/Write commands to select one location out of the memory array in the respective bank. A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by BA0, BA1 . The address inputs also provide the op-code during Mode Register Set commands.
DQ	Input/Output	Data Input/ Output: Bi-directional data bus.
DQS , (DQS) (UDQS), (UDQS) (LDQS), (LDQS) (RDQS), (RDQS)	Input/Output	Data Strobe: output with read data, input with write data. Edge-aligned with read data, centered in write data. For the x16, LDQS corresponds to the data on DQ0-DQ7 ; UDQS corresponds to the data on DQ8-DQ15 . For the x8, an RDQS option using DM pin can be enabled via the EMRS(1) to simplify read timing. The data strobes DQS, LDQS, UDQS, and RDQS may be used in single ended mode or paired with optional complementary signals DQS, LDQS, UDQS, and RDQS to provide differential pair signaling to the system during both reads and writes. An EMRS(1) control bit enables or disables all complementary data strobe signals.

Table 10 — Command truth table.

Function	CKE		CS	RAS	CAS	WE	BA0 BA1 BA2	A15-A11	A10	A9 - A0	Notes
	Previous Cycle	Current Cycle									
Bank Activate	H	H	L	L	H	H	BA	Row Address			1,2
Write	H	H	L	H	L	L	BA	Column	L	Column	1,2,3
Write with Auto Precharge	H	H	L	H	L	L	BA	Column	H	Column	1,2,3
Read	H	H	L	H	L	H	BA	Column	L	Column	1,2,3
Device Deselect	H	X	H	X	X	X	X	X	X	X	1

NOTE 1 All DDR2 SDRAM commands are defined by states of **CS, RAS, CAS, WE** and CKE at the rising edge of the clock.

CAS Latency

A6	A5	A4	Latency
0	0	0	Reserved
0	0	1	Reserved
0	1	0	2(Optional)
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	Reserved
1	1	1	Reserved

A5	A4	A3	Additive Latency
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

EMRS(1). The **Write Latency (WL)** is always defined as **RL - 1** (read latency - 1) where read latency is defined as the sum of additive latency plus CAS latency (**RL=AL+CL**). Read or Write operations using **AL**

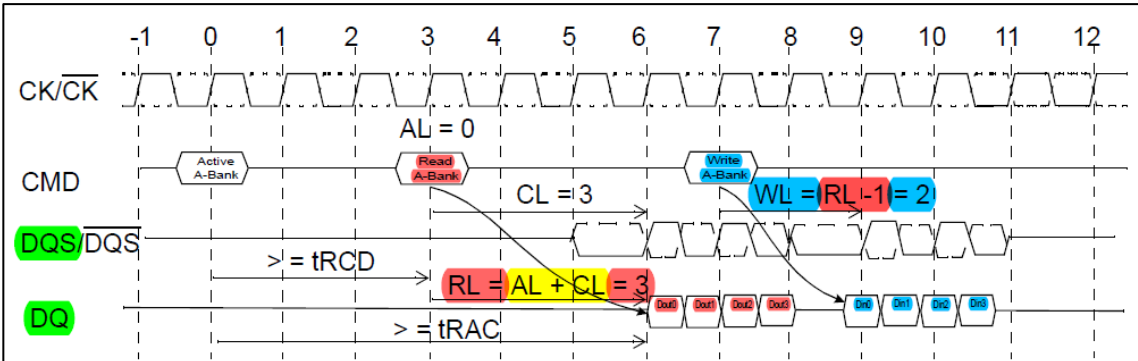


Figure 22 — Example 2: Read Followed by a Write to the Same Bank [AL = 0 and CL = 3, RL = (AL + CL) = 3, WL = (RL - 1) = 2, BL = 4]

EX1064 (JESD79-2) at 12, 14, 24-25

Prior Art: Ellsberry (U.S. Patent Pub. No. 2006/0277355) [EX1073]

(19) **United States**

(12) **Patent Application Publication**
Ellsberry et al.

(10) **Pub. No.: US 2006/0277355 A1**

(43) **Pub. Date: Dec. 7, 2006**

(54) **CAPACITY-EXPANDING MEMORY DEVICE**

(22) Filed:

Jun. 1, 2005

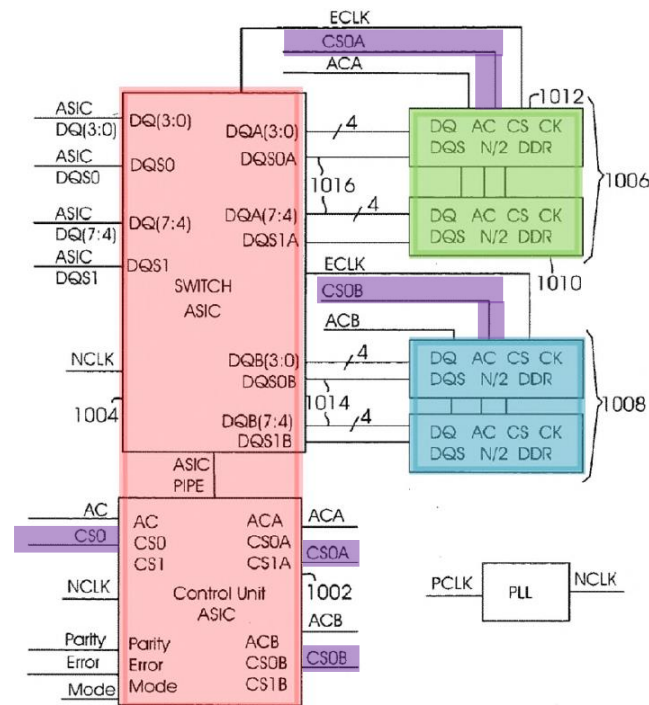


Fig. 10

(57)

ABSTRACT

The invention relates to a device, system, and method for expanding the memory capacity of a memory module. A **control unit and memory bank switch** are mounted on a memory module to selectively control write and/or read operations to/from memory devices communicatively coupled to the memory bank switch. **By selectively routing data to and from the memory devices, a plurality of memory devices may appear as a single memory device** to the operating system. That is, the invention expands the addressable memory banks on a module by making **two smaller-capacity memory devices emulate a single higher-capacity memory device**.

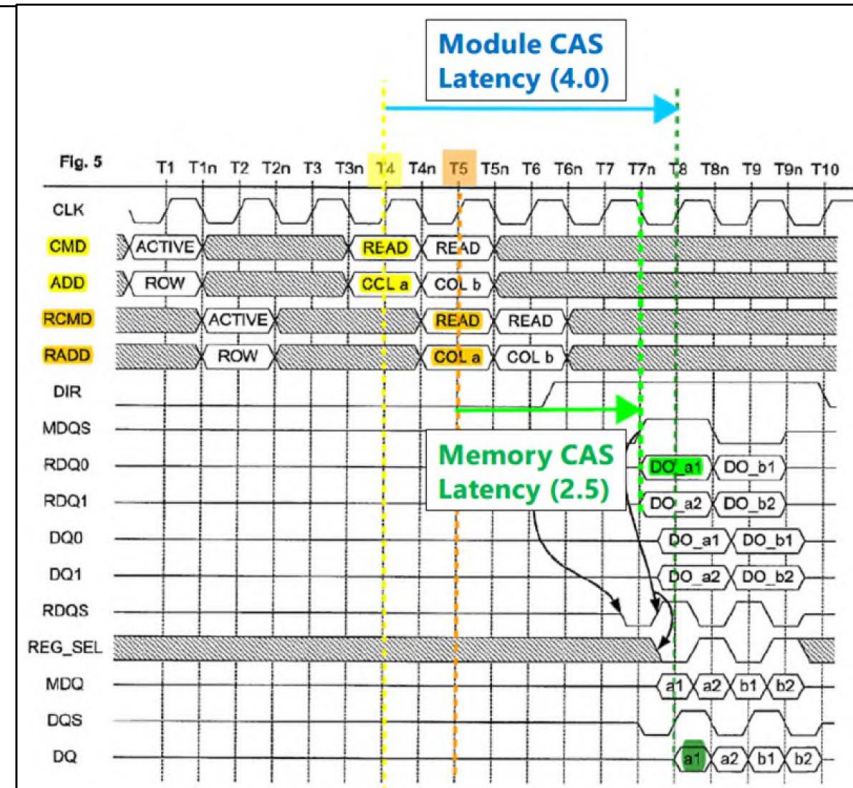
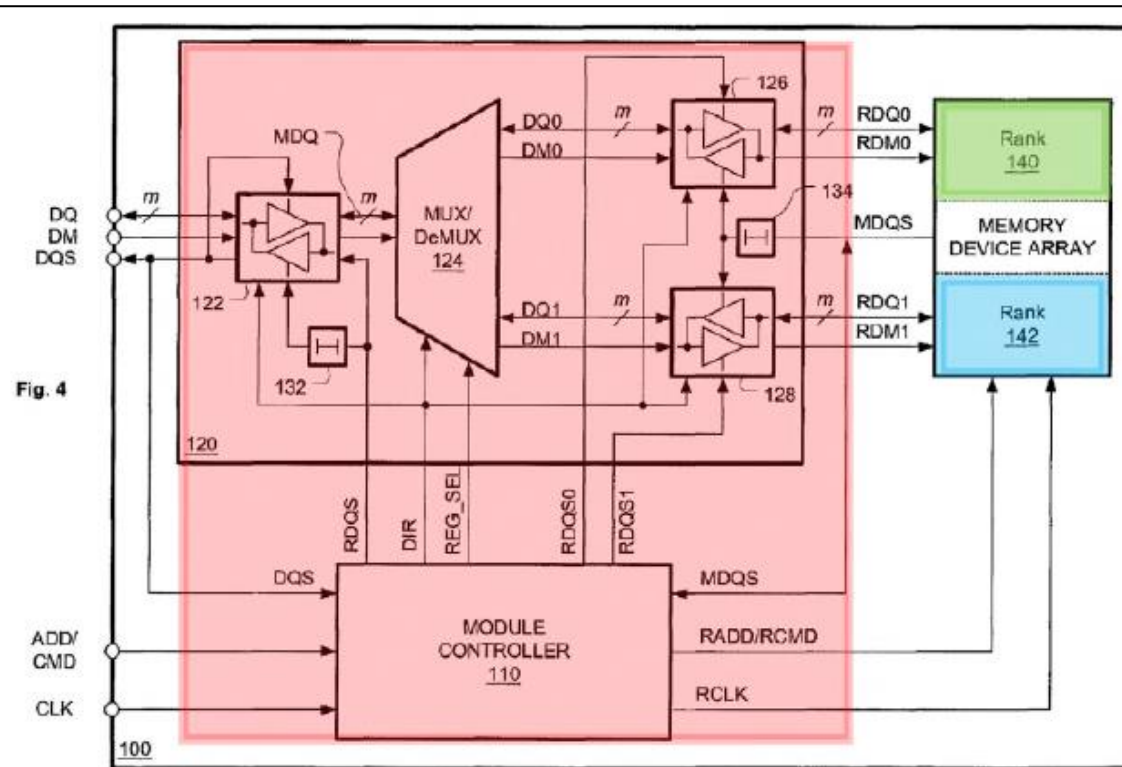
Prior Art: Halbert (U.S. Patent No. 7,024,518) [EX1078]

(12) **United States Patent**
Halbert et al.

(10) **Patent No.:** **US 7,024,518 B2**
(45) **Date of Patent:** **Apr. 4, 2006**

(54) **DUAL-PORT BUFFER-TO-MEMORY
INTERFACE**

(22) Filed: **Mar. 13, 2002**



Prior Art: Matsui2 (U.S. Patent Pub. No. 2003/0039151) [EX1082]

(19) **United States**

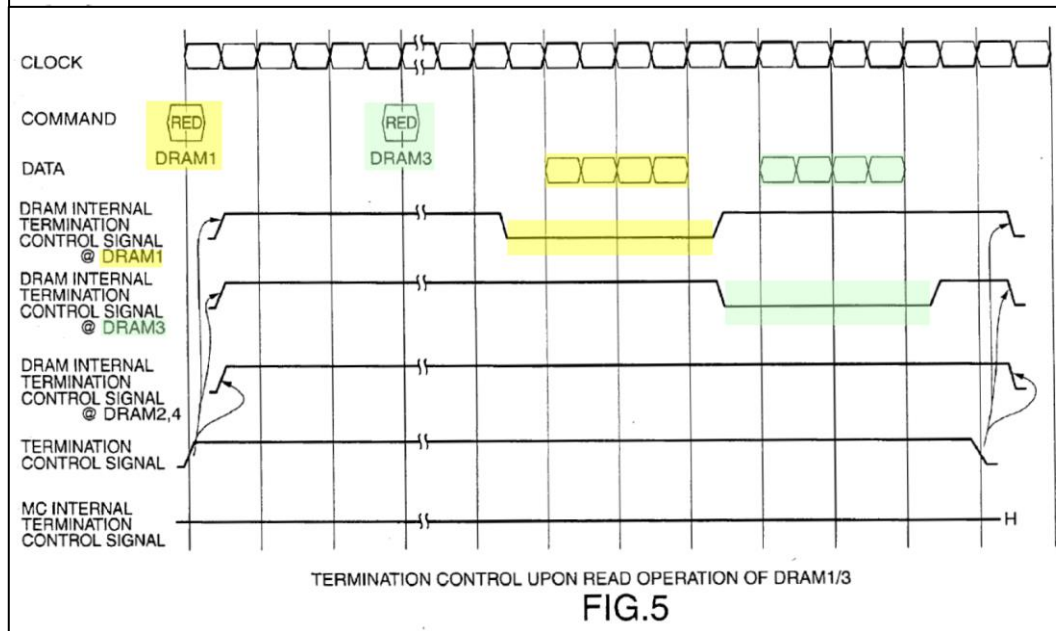
(12) **Patent Application Publication**
Matsui

(10) Pub. No.: **US 2003/0039151 A1**

(43) Pub. Date: **Feb. 27, 2003**

(54) **MEMORY DEVICE AND MEMORY SYSTEM**

(22) Filed: **Aug. 23, 2002**



[0037] The memory controller 21 comprises a control unit 211 for delivering a termination control signal to the control signal line 25, a driver 212 for delivering data to the data bus 22 upon carrying out a data write operation, a receiver 220 for receiving data from the data bus 22 upon carrying out a data read operation, and a termination circuit 213 to be put into an operating state in case where the data are read from the DRAM1, the DRAM2, the DRAM3, and the DRAM4. The driver 212 and the receiver 220 are selectively connected to the termination circuit 213 under control of the control unit 211 as will later be described.

LEVEL OF SKILL 2

Netlist only disputes whether a POSITA knew about the internal “design” of memory devices and modules

B. Person of Ordinary Skill in the Art (“POSITA”)

A POSITA in the field of the 417 Patent in 2004 or 2005 would have had an advanced degree in electrical or computer engineering and at least two years working in the field, or a bachelor’s degree in such engineering disciplines and at least three years working in the field. EX1003, ¶48. Additional training can substitute for educational or research experience, and vice versa. *Id.* A POSITA would have been familiar with various standards of the day including the JEDEC industry standards, and knowledgeable about the design and operation of standardized DRAM and SDRAM memory devices and memory modules and how they interacted with the memory controller of a computer system. *Id.* Specifically, he or she would have been knowledgeable about the JEDEC DDR and DDR2 SDRAM standards used to standardize the functioning of memory devices, and the JEDEC 21-C standard used to standardize different possibilities for the physical layout of memory devices on a module as well as different possibilities for density and organization of the memory devices to achieve a given memory capacity. *Id.*;

see also id. ¶¶49-50 (citing EX1001, 6:43-58, 23:23-24:22, 39:21-28 (referring to JEDEC standards); EX1060, EX1062, EX1064, EX1066). He or she would also have been familiar with the structure and operation of circuitry used to access and control computer memories, including sophisticated circuits such as ASICs (Application-Specific Integrated Circuits) and CPLDs (Complex Programmable Logic Devices) and more low-level circuits such as tri-state buffers, flip flops and registers. *Id.* ¶48.

‘417 Paper 1 (Pet.) at 9-10; *see also* ‘215 Paper 1 (Pet.) at 9-10 (similar)

Netlist's expert admitted that books in the field (including his own) taught about the internal design of memory devices and modules



Q. Chapter 8 of the Jacob textbook marked as Exhibit 1070, starting on page 353 and ending on page 376, describes the internal operation and structure of DRAM memory devices; correct?

A. Generally speaking, that's true.
So I was clearly in error when I said the two pages in one figure.

Chapter 8	DRAM Device Organization: Basic Circuits and Architecture	353
8.1	DRAM Device Organization	353
8.2	DRAM Storage Cells	355
8.3	RAM Array Structures	358
8.4	Differential Sense Amplifier	360
8.5	Decoders and Redundancy	366
8.6	DRAM Device Control Logic	368
8.7	DRAM Device Configuration	370
8.8	Data I/O	372
8.9	DRAM Device Packaging	373
8.10	DRAM Process Technology and Process Scaling Considerations	374

EX1070 at xiv

Q. And did you write this book marked as Exhibit 1097 yourself?

A. Yes.

Q. Please turn to page 41 of Exhibit 1097, which is Chapter 3 of your book, and let me know when you're there.

A. I'm at Chapter 3.

3 DRAM Basics

The discussion of DRAM basics in this chapter begins with a general description of how a DRAM stores information, how information is presented to a **generic DRAM**, and how it is retrieved again. Section 3.4 then describes the semiconductor technology used to make DRAMs and discusses the evolution of that technology over the past two decades. Section 3.5 contains greater detail about the finer points of DRAM design and their implications for present and future memory systems.

EX1095 at 149:9:16, 168:10-:16; see also id. at 151:2-154:19, 163:15-:22

EX1097 at 41

CLAIM CONSTRUCTION

3

“RANK”: ONE OR MORE MEMORY DEVICES

The Board has repeatedly construed “*rank*” to include one or more memory devices, rejecting Netlist’s arguments

Trials@uspto.gov
571-272-7822

Paper 11
Date: August 1, 2023

 UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.,
Petitioner,

v.

NETLIST, INC.,
Patent Owner.

IPR2023-00455
Patent 9,858,215 B1

Before PATRICK M. BOUCHER, JON M. JURGOVAN, and
DANIEL J. GALLIGAN, *Administrative Patent Judges*.

GALLIGAN, *Administrative Patent Judge*.

DECISION
Granting Institution of *Inter Partes* Review
35 U.S.C. § 314

For the reasons discussed above, we preliminarily determine that a
rank may have only one memory device. We do not construe the term
further at this time. See *Realtime Data*, 912 F.3d at 1375.

‘215: Paper 11 (ID) at 9-13

Trials@uspto.gov
571-272-7822

Paper 96
Entered: April 17, 2024

 UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD., MICRON TECHNOLOGY, INC.,
MICRON SEMICONDUCTOR PRODUCTS, INC., and MICRON
TECHNOLOGY TEXAS LLC,¹
Petitioner,

v.

NETLIST, INC.,
Patent Owner.

IPR2022-00615
Patent 7,619,912 C1

Before JON M. JURGOVAN, DANIEL J. GALLIGAN, and
KARA L. SZPONDOWSKI, *Administrative Patent Judges*.

JURGOVAN, *Administrative Patent Judge*.

JUDGMENT
Final Written Decision
Determining Challenged Claim Unpatentable
Dismissing Patent Owner’s Motion to Submit Supplemental Information
Dismissing Petitioner’s Motion to Exclude
35 U.S.C. § 318(a)

Based on the foregoing, we conclude that **“rank” as used in the ‘912
patent can include only “one memory device.”** Because the intrinsic record
is clear, we need not resort to extrinsic evidence to determine the scope of

EX1114 at 13-24; see also EX1023 at 29-33; EX2023 at 4-6

The District Court also construed “*rank*” to include one or more memory devices, rejecting Netlist’s arguments



The Disputed Terms	The Court’s Construction
The “Rank” Terms (’912 Patent, ’417 Patent, ’215 Patent)	A “rank” of memory is “a ‘bank’ of one or more devices on a memory module that operate in response to a given signal”

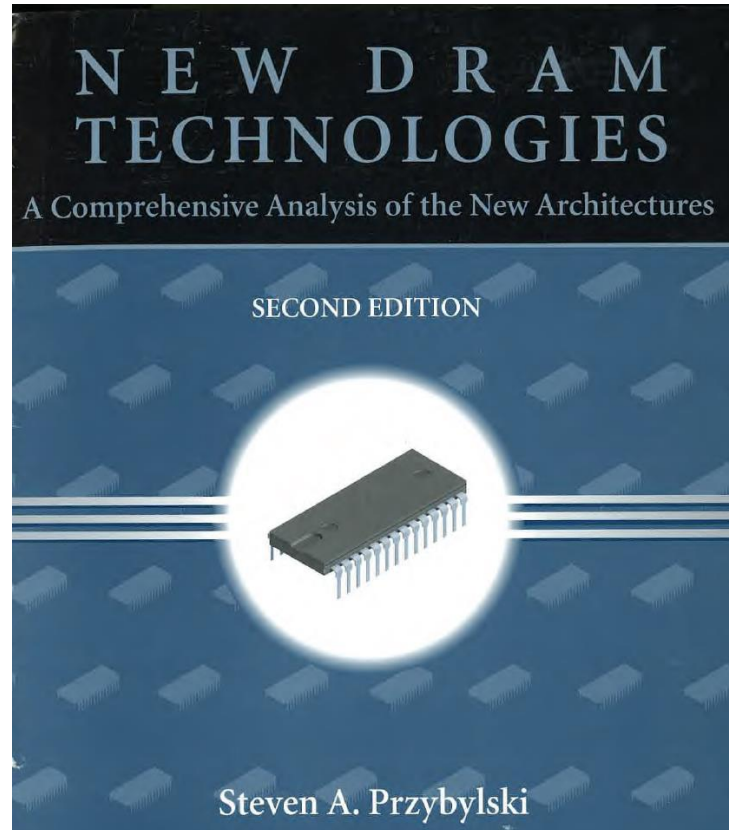
EX2030 at 35; *see also id.* at 11-14

The textbook definition of “*rank*” (including by Netlist’s expert on the left) includes just one memory device

Rank

A rank of DRAMs, SIMMs, or DIMMs is the physical collection of devices that have to be present or not present as a group for the memory system to operate properly. A rank of memory typically consists of one or more DRAMs that are ganged in parallel and accessed together as a wider organizational unit. A rank may

EX1097 (Przybylski textbook) at 497



10.2.2 Rank

Figure 10.5 shows a memory system populated with 2 ranks of DRAM devices. Essentially, a rank of memory is a “bank” of one or more DRAM devices that operate in lockstep in response to a given command. However, the word *bank* has already been used to describe the number of independent DRAM arrays within a DRAM device. To lessen the confusion associated with overloading the nomenclature, the word *rank* is now used to denote a set of DRAM devices that operate in lockstep to respond to a given command in a memory system.

In modern memory systems, multiple DRAM devices are commonly grouped together to provide the data bus width and capacity required by a given memory system. For example, 18 DRAM devices, each with a 4-bit-wide data bus, are needed in a given rank of memory to form a 72-bit-wide data bus. In contrast, embedded systems that do not require as much capacity or data bus width typically use fewer devices in each rank of memory—sometimes as few as one device per rank.

EX1070 (Jacob textbook) at 413-14

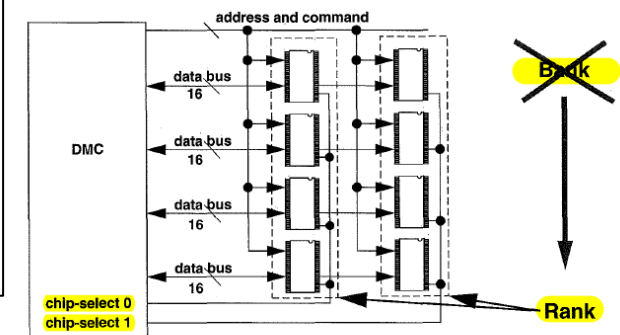
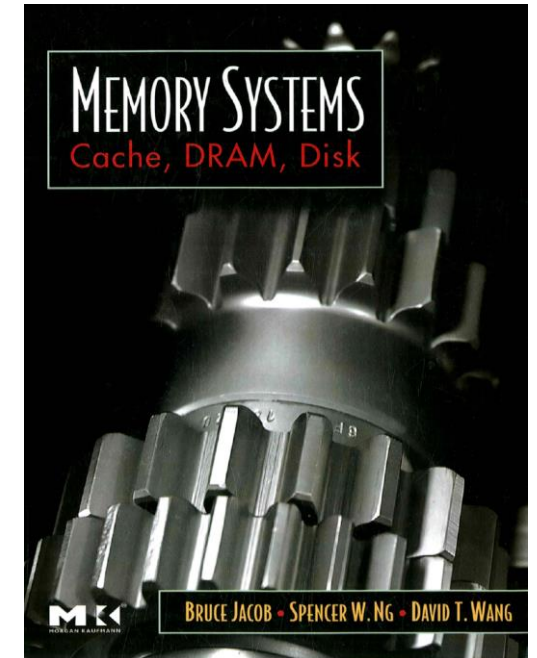


FIGURE 10.5: Memory system with 2 ranks of DRAM devices.

The '215 Patent expressly claims one memory device in each rank

(12) **United States Patent**
Solomon et al.

(10) **Patent No.:** **US 9,858,215 B1**
(45) **Date of Patent:** **Jan. 2, 2018**

(54) **MEMORY MODULE WITH DATA
BUFFERING**

(71) Applicant: **Netlist, Inc.**, Irvine, CA (US)

(72) Inventors: **Jeffrey C. Solomon**, Irvine, CA (US);
Jayesh R. Bhakta, Cerritos, CA (US)

a plurality of memory integrated circuits mounted on the printed circuit board and arranged in a plurality of ranks including a first rank and a second rank, the plurality of memory integrated circuits including at least one first memory integrated circuit in the first rank and at least one second memory integrated circuit in the second rank, wherein the first rank is selected to receive

'215: EX1001 at 37:32-:38



Petitioner contends that U.S. Patent 9,858,215 B1 ("the '215 patent") is related to the '912 patent, and that it refers to "rank" as "at least one memory integrated circuit." Ex. 1058, 152, 187 (3:33-35), 204 (37:35-38). Although Patent Owner characterizes Petitioner's observation as a "trick" because Patent Owner added disclosure to the '215 patent that is not present in the '912 patent (Prelim. Sur-Reply 6-7), Patent Owner does not deny that the '215 patent defines "rank" in this way. Claim terms must be interpreted consistently across related patents. *See SightSound Techs., LLC v. Apple*

EX1023 at 32;
see also '215: Paper 11 (ID) at 10-11

The '417/'215 Patents disclose an embodiment where each “rank” has just “one” memory device, as found by the Board



Patent Owner counters that, “[r]ead in context, the embodiments described with reference to Table 1 refer to transmitting a command signal to one of the multiple memory devices in the selected rank.” Prelim. Resp. 11. On this record, we disagree with Patent Owner’s interpretation of this passage. The ’215 patent states that Table 1 is a logic table “for the selection among ranks of memory devices 30 using chip-select signals.” Ex. 1001, 16:22–24. We see nothing in Table 1 that indicates a further selection of memory devices within each rank. Rather, the passage quoted above indicates an embodiment in which each rank has one memory device because it describes sending the command signal “to only one memory device or the other memory device” by reference to logic showing the selection of one rank or another rank. See Ex. 1001, 16:66–17:12.

On this preliminary record, we determine that the intrinsic evidence supports Petitioner’s position that a rank may have only one memory device.

’215: Paper 11 (ID) at 12; see also EX1114 at 15-18 (quoting EX1015 (912 Patent) at 7:55-9:21); EX2023 at 5-6 (same)

Table 1 provides a logic table compatible with certain embodiments described herein for the selection among ranks of memory devices 30 using chip-select signals.

TABLE 1

State	CS ₀	CS ₁	A _{n+1}	Command	CS _{0A}	CS _{0B}	CS _{1A}	CS _{1B}
1	0	1	0	Active	0	1	1	1
2	0	1	1	Active	1	0	1	1
3	0	1	x	Active	0	0	1	1
4	1	0	0	Active	1	1	0	1
5	1	0	1	Active	1	1	1	0
6	1	0	x	Active	1	1	0	0
7	1	1	x	x	1	1	1	1

The “Command” column of Table 1 represents the various commands that a memory device (e.g., a DRAM device) can execute, examples of which include, but are not limited to, activation, read, write, precharge, and refresh. In certain embodiments, the command signal is passed through to the selected rank only (e.g., state 4 of Table 1). In such embodiments, the command signal (e.g., read) is sent to only one memory device or the other memory device so that data is supplied from one memory device at a time. In other embodiments, the command signal is passed through to both associated ranks (e.g., state 6 of Table 1). In such embodiments, the command signal (e.g., refresh) is sent to both memory devices to ensure that the memory content of the memory devices remains valid over time. Certain embodiments utilize a logic table such as that of Table 1 to simulate a single memory device from two memory devices by selecting two ranks concurrently.

’417: EX1001 at 18:37-19:27
 ’215: EX1001 at 16:22-17:13

The '417/'215 Patents use the term "*rank*" consistent with the textbook definition that includes just one memory device per rank (e.g., one x16 or one x32 device per rank)

The DRAM devices of a memory module are generally arranged as ranks or rows of memory, each rank of memory generally having a bit width. For example, a memory module in which each rank of the memory module is 64 bits wide is described as having an "x64" organization. Similarly, a memory module having 72-bit-wide ranks is described as having an "x72" organization.

During operation, the ranks of a memory module are selected or activated by address and command signals that are received from the processor. Examples of such address and command signals include, but are not limited to, rank-select signals, also called chip-select signals. Most computer and server systems support one-rank and two-rank memory modules. By only supporting one-rank and two-rank memory modules, the memory density that can be incorporated in each memory slot is limited.

'417: EX1001 at 2:47-:53, 2:65-3:6

'215: EX1001 at 2:41-:47, 2:59-:67

Various types of memory modules 10 are compatible with embodiments described herein. For example, memory modules 10 having memory capacities of 512-MB, 1-GB, 2-GB, 4-GB, 8-GB, as well as other capacities, are compatible with embodiments described herein. Certain embodiments described herein are applicable to various frequencies including, but not limited to 100 MHz, 200 MHz, 400 MHz, 800 MHz, and above. In addition, memory modules 10 having widths of 4 bytes, 8 bytes, 16 bytes, 32 bytes, or 32 bits, 64 bits, 128 bits, 256 bits, as well as other widths (in bytes or in bits), are compatible with embodiments described herein. In certain embodiments, the memory module 10 comprises a printed circuit board on which the memory devices 30 are mounted, a plurality of edge connectors configured to be electrically coupled to a corresponding plurality of contacts of a module slot of the computer system, and a plurality of electrical conduits which electrically couple the memory devices 30 to the circuit 40 and which electrically couple the circuit 40 to the edge connectors. Furthermore, memory modules 10 compatible with embodiments described herein include, but are not limited to, single in-line memory modules (SIMMs), dual in-line memory modules (DIMMs), small-outline DIMMs (SO-DIMMs), unbuffered DIMMs (UDIMMs), registered DIMMs (RDIMMs), fully-buffered DIMM (FB-DIMM), rank-buffered DIMMs (RBDIMMs), mini-DIMMs, and micro-DIMMs.

Memory devices 30 compatible with embodiments described herein include, but are not limited to, random-access memory (RAM), dynamic random-access memory (DRAM), synchronous DRAM (SDRAM), and double-data-rate DRAM (e.g., SDR, DDR-1, DDR-2, DDR-3). In addition, memory devices 30 having bit widths of 4, 8, 16, 32, as well as other bit widths, are compatible with embodiments described herein. Memory devices 30 compatible

'417: EX1001 at 6:24-:58

'215: EX1001 at 5:44-6:11

JEDEC allowed module widths equal to the DRAM width (e.g., 8, 16, or 32 bits)

Byte 6: Module Data Width

Byte 6 is used to designate the module's data width. For example:

If the module's Data Width is:	and Byte 6 is:
64	0100 0000
72	0100 1000

Line #	Data Width	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
0	0	0	0	0	0	0	0	0	0	00
-	-	-	-	-	-	-	-	-	-	-
32	32	0	0	1	0	0	0	0	0	20

Byte 13: Primary SDRAM Width

Bits 0-7 of this byte indicate the width of the primary data SDRAM. The primary SDRAM is that which is used for data; examples of primary (data) SDRAM widths are x4, x8, x16, and x32. Note that if the module is made with SDRAMs which provide for data and error checking, e.g. x6, x18, and x36, then it is also designated in this field.

Line #	SDRAM Data Width	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
15	15	0	0	0	0	1	1	1	1	0F
-	-	-	-	-	-	-	-	-	-	-
254	254	1	1	1	1	1	1	1	0	FE

Q. For example, as shown on page 8 of Exhibit 1107, the module's data width can be specified as 32 bits wide, correct?

MR. TEZYAN: Object to form.

THE WITNESS: I would say that byte 6 of this DDR2 SPD layout shows that it seems like any value between zero and 255 can be -- well, values ranging from zero to 255 can be written into this byte specifying different settings, different settings -- information related to the module data width.

EX1101 at 152:4-:19; see also EX1114 at 51

EX2031 at 8, 13

Netlist has dropped its proposed construction for “rank” in these IPRs

Netlist disagrees with Petitioner’s proposed construction for “rank,” in particular, that a rank could include a single memory device. Contra Pet. 26. However, the Board need not resolve that dispute to address the parties’ arguments

Solely for purposes of responding to this Petition, however, Netlist applies Petitioner’s proposed construction: “an independent set of one or more memory devices on a memory module that act together in response to command signals, including chip-select signals, to read or write the full bit-width of the memory module.” Pet. 26

‘417: Paper 22 (POR) at 8-9; *see also* ‘215: Paper 22 (POR) at 8-9

GROUND 1 ('215 AND '417)

4

GROUND 1: PEREGO + JESD79-2

SUMMARY OF GROUND 1

PEREGO + JESD79-2

Ground 1: Perego's buffer (red), like that of the '417/'215 Patents, isolates the memory devices (blue/green) from the memory controller

Perego

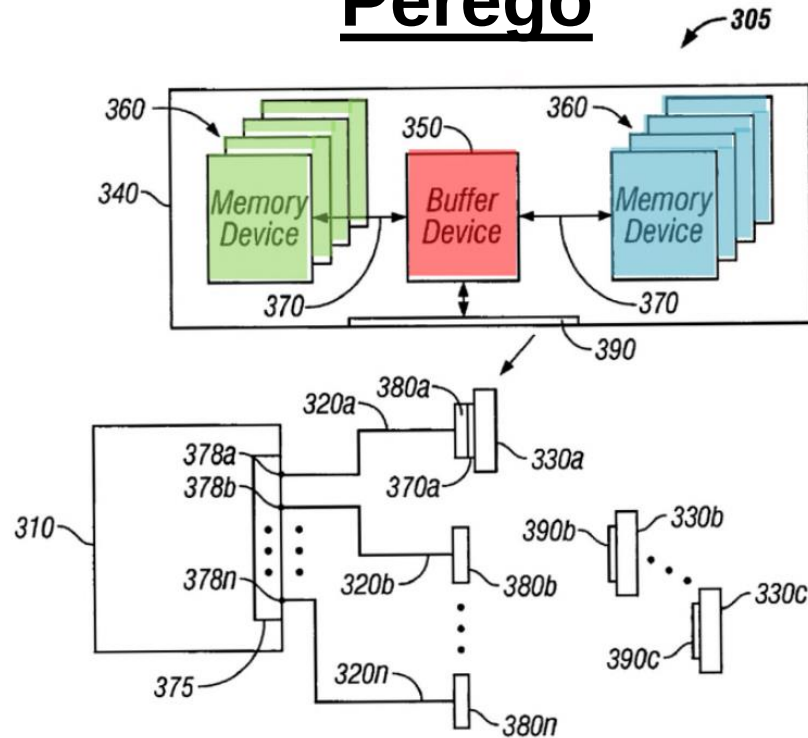
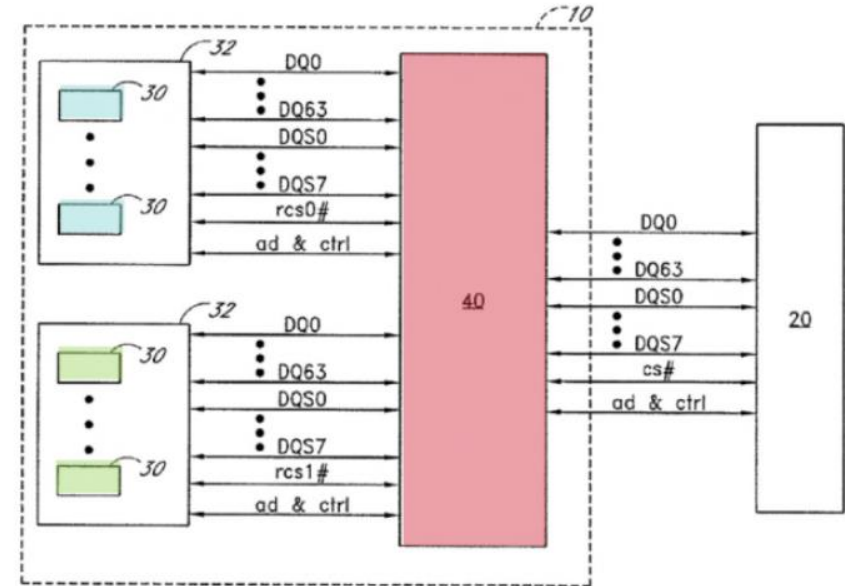


FIG. 3B

With further reference to FIGS. 3A and 3B, **buffer device 350** transceives and provides isolation between signals interfacing to controller 310 and signals interfacing to the plurality of memory devices 360. In a normal memory read

EX1071 (Perego) at 6:12-15, Fig. 3B

'417/215 Patents



In certain embodiments, the circuit 40 selectively isolates the loads of at least some of the memory devices 30 from the computer system. The circuit 40 of certain embodiments is configured to present a significantly reduced load to the computer system. In certain embodiments in which the

'417: EX1001 at 7:61-8:4, Fig. 1

'215: EX1001 at 7:14-:18, Fig. 1

'417: Paper 1 (Pet.) at 28-30

'215: Paper 1 (Pet.) at 30-32

32

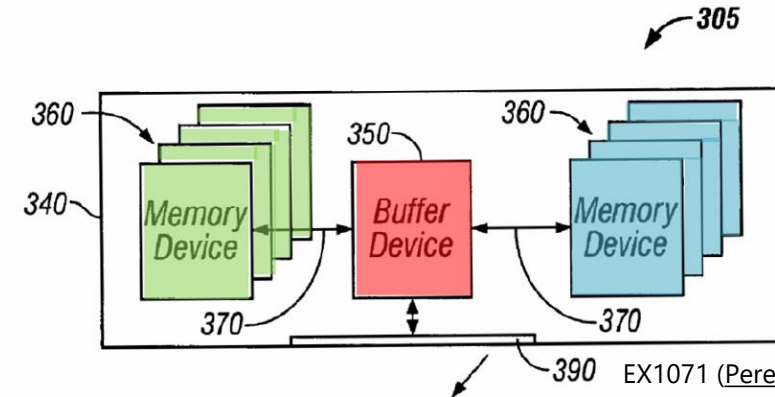
Ground 1: Perego's buffer (red) also allows flexible, cost-effective, and transparent upgrades so DDR2 SDRAMs can be used with existing and new generations of controllers

There is a need for memory system architectures or interconnect topologies that provide flexible and cost effective upgrade capabilities while providing high bandwidth to keep pace with microprocessor operating frequencies.

EX1071 (Perego) at 2:26-:29

In one embodiment, memory devices **410a–410h** are Rambus® Dynamic Random access Memory (RDRAM) devices operating at a data rate of 1066 Mbits/sec. Other memory devices may be implemented on module **400**, for example, Double Data Rate 2 (DDR2) DRAM devices and Synchronous DRAM (SDRAM) devices. Utilizing buffer device **405** between the memory devices and controller in accordance with the present invention (e.g., see FIG. 3) may feasibly render the type of memory device transparent to the system. Different types of memory devices may be included on different modules within a memory system, by employing buffer device 405 to translate protocols employed by controller 310 to the protocol utilized in a particular memory device implementation.

EX1071 (Perego) at 10:54-:67



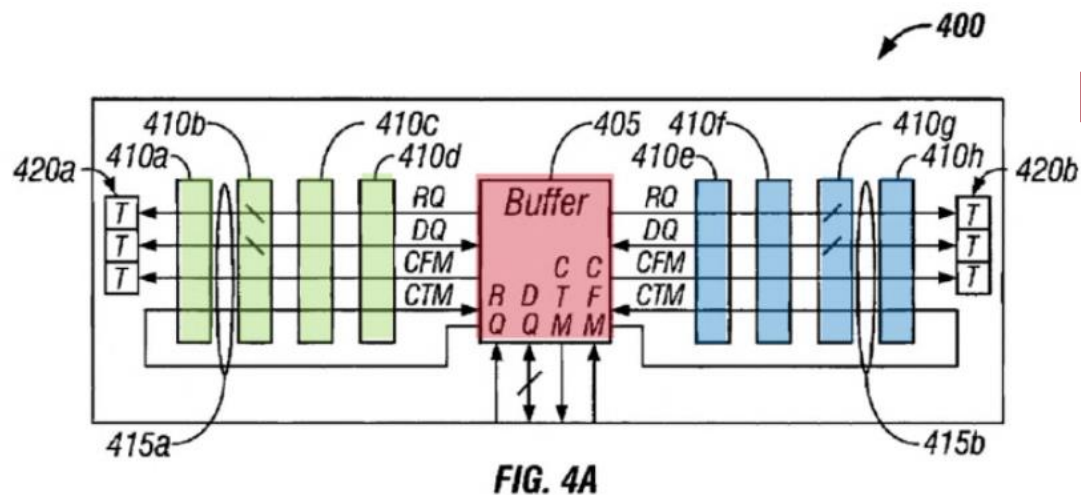
EX1071 (Perego) at Fig. 3B

Buffer device **350** provides a high degree of system flexibility. New generations of memory devices may be phased in with controller 310 or into memory system **300** by modifying buffer device 350. Backward compatibility with existing generations of memory devices (i.e., memory devices **360**) may also be preserved. Similarly, new generations of controllers may be phased in which exploit features of new generations of memory devices while retaining backward compatibility with existing generations of memory devices.

EX1071 (Perego) at 6:34-:43

Ground 1: Perego + JESD79-2 (DDR2 SDRAM standard)

Perego: Buffered module, using DDR2 SDRAM memories, compatible with existing controllers



In one embodiment, memory devices 410a-410h are Rambus® Dynamic Random access Memory (RDRAM) devices operating at a data rate of 1066 Mbits/sec. Other memory devices may be implemented on module 400, for example, **Double Data Rate 2 (DDR2) DRAM devices and Synchronous DRAM (SDRAM) devices.** Utilizing buffer

EX1071 (Perego) at 10:54:-67, Fig. 4A

JESD79-2: Details of DDR2 SDRAM systems including their signaling and timing

CS	Input	Chip Select: All commands are masked when $\overline{\text{CS}}$ is registered HIGH. $\overline{\text{CS}}$ provides for external Rank selection on systems with multiple Ranks. CS is considered part of the command code.
RAS, CAS, WE	Input	Command Inputs: RAS, CAS and WE (along with $\overline{\text{CS}}$) define the command being entered.
BA0 - BA2	Input	Bank Address Inputs: BA0 and BA1 for 256 and 512Mb, BA0 - BA2 define to which bank an Active, Read, Write or Precharge command is being applied. Bank address also determines if the mode register or extended mode register is to be accessed during a MRS or EMRS cycle.
A0 - A15	Input	Address Inputs: Provided the row address for Active commands and the column address and Auto Precharge bit for Read/Write commands to select one location out of the memory array in the respective bank. A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by BA0, BA1. The address inputs also provide the op-code during Mode Register Set commands.
DQ	Input/Output	Data Input/ Output: Bi-directional data bus.
DQS (DQS), (UDQS), (UDQS), (LDQS), (LDQS), (RDQS), (RDQS)	Input/Output	Data Strobe: output with read data, input with write data. Edge-aligned with read data, centered in write data. For the x16, LDQS corresponds to the data on DQ0-DQ7; UDQS corresponds to the data on DQ8-DQ15. For the x8, an RDQS option using DM pin can be enabled via the EMRS(1) to simplify read timing. The data strobes DQS, LDQS, UDQS, and RDQS may be used in single ended mode or paired with optional complementary signals $\overline{\text{DQS}}$, $\overline{\text{LDQS}}$, $\overline{\text{UDQS}}$, and $\overline{\text{RDQS}}$ to provide differential pair signaling to the system during both reads and writes. An EMRS(1) control bit enables or disables all complementary data strobe signals.

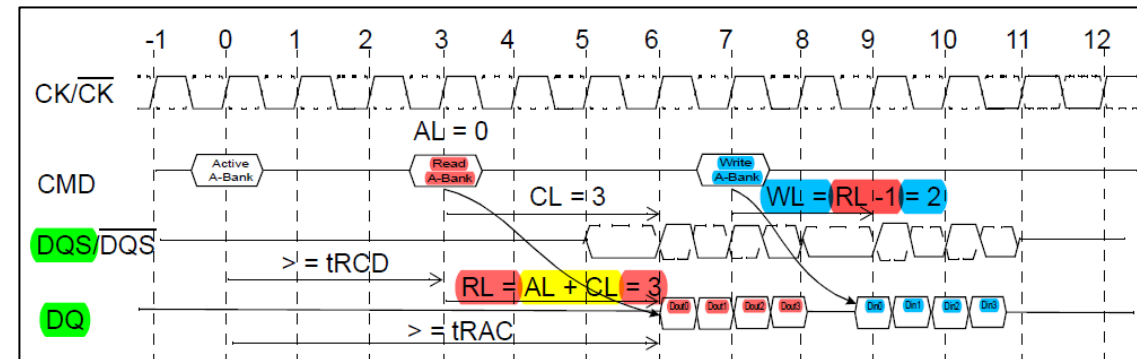


Figure 22 — Example 2: **Read** Followed by a **Write** to the Same Bank
[AL = 0 and CL = 3, RL = (AL + CL) = 3, WL = (RL - 1) = 2, BL = 4]

EX1064 (JESD79-2) at 6, 25

PEREGO TEACHES JEDEC-STYLE IMPLEMENTATIONS WITH CHIP SELECTS

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Netlist contends Ground 1 does not render obvious chip-select signals

Neither Perego nor JESD79-2 disclose such input chip select signals or lines. Perego discloses Rambus-style modules that employ a point-to-point architecture and configurable bit-width interfaces that are fundamentally different than the conventional memory bus required by JEDEC module standards and do not include chip-select lines or otherwise convey chip-select signals. JESD79-2 is the standard

'417: Paper 22 (POR) at 1; see also '215: Paper 22 (POR) at 1

'417 Patent

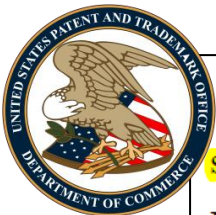
1. A memory module operable in a computer system to communicate data with a memory controller of the computer system via a N-bit wide memory bus in response to read or write memory commands received from the memory controller, the memory bus including address and control signal lines and data signal lines, the memory module comprising:
a printed circuit board having a plurality of edge connections configured to be electrically coupled to a corresponding plurality of contacts of a module slot of the computer system;
logic coupled to the printed circuit board and configurable to receive a set of input address and control signals associated with a read or write memory command via the address and control signal lines and to output a set of registered address and control signals in response to the set of input address and control signals, the set of input address and control signals including a plurality of input chip select signals and other input address and control signals, ...

'215 Patent

1. A memory module operable in a computer system to communicate data with a memory controller of the computer system via a memory bus in response to memory commands received from the memory controller, the memory commands including a first memory command and a subsequent second memory command, the first memory command to cause the memory module to receive or output a first data burst and the second memory command to cause the memory module to receive or output a second data burst, the memory module comprising:

9. The memory module of claim 1, wherein the first memory command includes at least one first chip select signal and the second memory command includes at least one second chip select signal.

The Institution Decision correctly found that it was obvious for Perego's memory module to receive JEDEC-style signals, including “chip select” signals

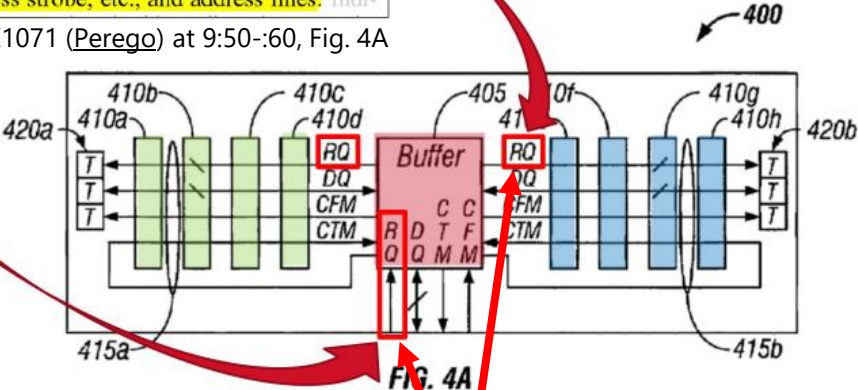


As to Patent Owner’s suggestion that “providing input chip-select signals to Perego’s buffer device” would “go beyond” JESD79-2 (Prelim. Resp. 17), we are sufficiently persuaded by Petitioner’s contentions that this would have been obvious based on JESD79-2 and the knowledge of other JEDEC standards. In particular, Petitioner argues that it “would have been obvious to a [person of ordinary skill in the art] in light of JESD79-2 and knowledge of the JEDEC standards that the memory controller would provide multiple chip-select signals to the memory module,” citing in support JEDEC DIMM standards that show pins for receiving chip select signals at the memory module. Pet. 57–58 (citing Ex. 1003 ¶¶ 251–252, Ex. 1064, 6; Ex. 1062, 6; Ex. 1066, 6–7). Thus, Patent Owner’s argument that JESD79-2 “describes the input/output to SDRAM devices, and not the input/output to a logic device coupled between a memory controller and memory devices” (Prelim. Resp. 14 (citing Ex. 1064)) does not fully address Petitioner’s contentions for this subject matter.

‘417: Paper 11 (ID) at 19-20; see also ‘215: Paper 11 (ID) at 14-15, 27

In alternate embodiments, control lines (RQ) may comprise individual control lines, for example, row address strobe, column address strobe, etc., and address lines. Indi-

EX1071 (Perego) at 9:50:60, Fig. 4A



RAS, CAS, WE	Input	Command Inputs: RAS, CAS and WE along with CS define the command being entered.
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EX1064 (JESD79-2) at 6

Jedec Standard No. 21-C

DDR SDRAM Registered DIMM Design Specification

Pin Name	Description
RAS	SDRAM row address strobe
CAS	SDRAM column address strobe
WE	SDRAM write strobe
S0 - S3	SDRAM chip select lines (Physical banks 0, 1, 2, and 3)

EX1062 at 6

JEDEC Standard No. 21C

DDR2 SDRAM Registered DIMM Design Specification

Pin Name	Description
RAS	Row Address Strobe
CAS	Column Address Strobe
WE	Write Enable
S[3:0]	Chip Selects

EX1066 at 6-7

Perego's "individual control lines" (RQ) correspond to JEDEC-style control lines, including RAS, CAS, WE, and CS (chip select)

In one embodiment, memory devices 410a–410h are Rambus® Dynamic Random access Memory (RDRAM) devices operating at a data rate of 1066 Mbits/sec. Other memory devices may be implemented on module 400, for example, Double Data Rate 2 (DDR2) DRAM devices and Synchronous DRAM (SDRAM) devices. Utilizing buffer

In accordance with an embodiment of the present invention, control lines (RQ) transport control (e.g., read, write, precharge . . .) information and address (e.g., row and column) information contained in packets. By bundling control and address information in packets, protocols required to communicate to memory devices 410a–410h are independent of the physical control/address interface implementation.

In alternate embodiments, control lines (RQ) may comprise individual control lines, for example, row address strobe, column address strobe, etc., and address lines. Indi-

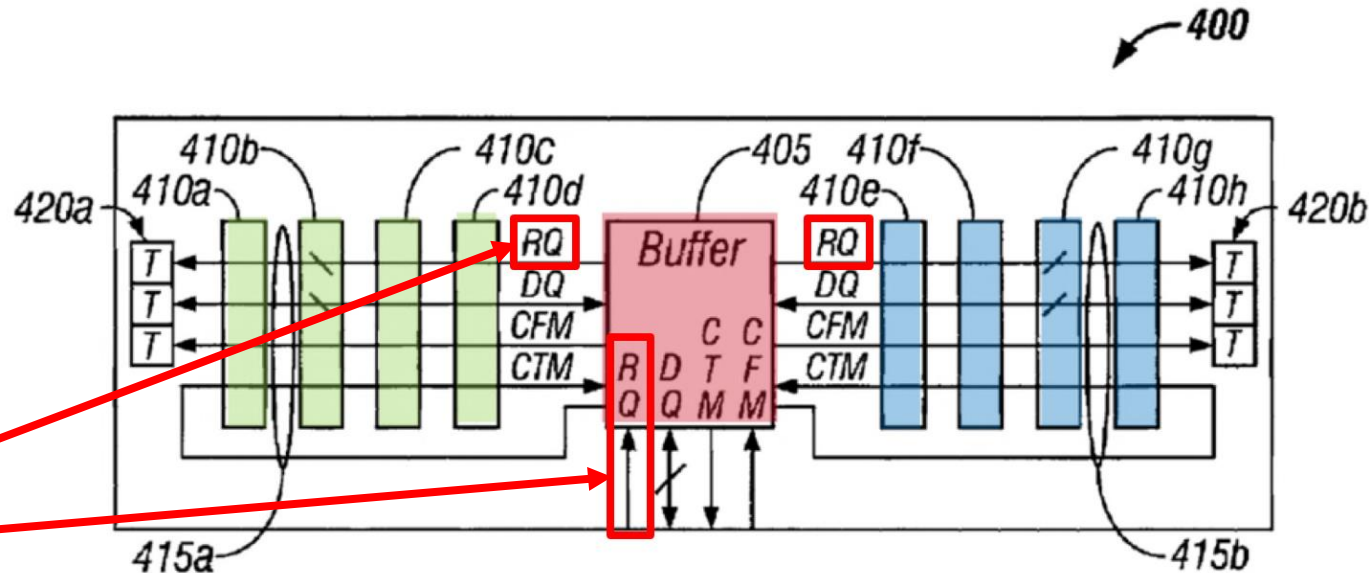


FIG. 4A

EX1071 (Perego) at 9:50-60, 10:54-:59 & Fig. 4A

JEDEC DDR2 SDRAM SPECIFICATION

CS	Input	Chip Select: All commands are masked when CS is registered HIGH. CS provides for external Rank selection on systems with multiple Ranks. CS is considered part of the command code.
ODT	Input	On Die Termination: ODT (registered HIGH) enables termination resistance internal to the DDR2 SDRAM. When enabled, ODT is only applied to each DQ, DQS, DQS, RDQS, RDQS, and DM signal for x4/x8 configurations. For x16 configuration ODT is applied to each DQ, UDQS/UDQS, LDQS/LDQS, UDM, and LDM signal. The ODT pin will be ignored if the Extended Mode Register (EMRS) is programmed to disable ODT.
RAS, CAS, WE	Input	Command Inputs: RAS, CAS and WE (along with CS) define the command being entered.



A patent need not teach, and preferably omits, what is well known in the art.

EX1064 (JESD79-2) at 6

MPEP 2164.01

Perego (like JEDEC) teaches that memory modules (DIMMs) receive “chip select” signals along with RAS, CAS, and address signals

modules. By way of comparison, buffers disposed on the conventional DIMM module in U.S. Pat. No. 5,513,135 are employed to buffer or register control signals such as RAS, and CAS, etc., and address signals. Data I/Os of the memory

EX1071 (Perego) at 6:27-:30

Jedec Standard No. 21-C

DDR SDRAM Registered DIMM Design Specification

Pin Name	Description
$\overline{\text{RAS}}$	SDRAM row address strobe
$\overline{\text{CAS}}$	SDRAM column address strobe
$\overline{\text{WE}}$	SDRAM write strobe
$\overline{\text{S0}} - \overline{\text{S3}}$	SDRAM chip select lines (Physical banks 0, 1, 2, and 3)

EX1062 at 6

JEDEC Standard No. 21C

DDR2 SDRAM Registered DIMM Design Specification

Pin Name	Description
$\overline{\text{RAS}}$	Row Address Strobe
$\overline{\text{CAS}}$	Column Address Strobe
$\overline{\text{WE}}$	Write Enable
$\overline{\text{S}}[3:0]$	Chip Selects

EX1066 at 6-7

168 PIN SDRAM DIMM

PIN NAME	#PINS	PIN FUNCTION
A0-A13	14	ADDRESS INPUT
DQ0-DQ79	80	DATA IN/DATA OUT
CS0-CS4	4	CHIP SELECT
WE0	1	WRITE ENABLE
CLK0, CLK1	2	CLOCK
CKE	1	CLOCK ENABLE
Vref	2	POWER SUPPLY FOR REFERENCE
Vcc	17	POWER SUPPLY
Vss	18	GROUND
PD	9	PRESENCE DETECT
ID	4	DIMM ID BIT
SCAS	1	SYNCHRONOUS COLUMN ADDRESS STROBE
SRAS	1	SYNCHRONOUS ROW ADDRESS STROBE
PDE	1	PRESENCE DETECT ENABLE
DQM	4	DATA INPUT/OUTPUT MASK
(DQMB)	(8)	(DATA INPUT/OUTPUT MASK BYTE)
RFU	1	RESERVED FOR FUTURE USE
DU	4	DON'T USE

fig. 3

EX1081 at Fig.3

Perego's "individual control lines" (RQ) do not correspond to Rambus

In one embodiment, memory devices 410a-410h are Rambus® Dynamic Random access Memory (RDRAM) devices operating at a data rate of 1066 Mbits/sec. Other memory devices may be implemented on module 400, for example, Double Data Rate 2 (DDR2) DRAM devices and Synchronous DRAM (SDRAM) devices. Utilizing buffer

In accordance with an embodiment of the present invention, control lines (RQ) transport control (e.g., read, write, precharge . . .) information and address (e.g., row and column) information contained in packets. By bundling control and address information in packets, protocols required to communicate to memory devices 410a-410h are independent of the physical control/address interface implementation.

In alternate embodiments, control lines (RQ) may comprise individual control lines, for example, row address strobe, column address strobe, etc., and address lines. Indi-

JEDEC DDR2 SDRAM SPECIFICATION

CS	Input	Chip Select: All commands are masked when CS is registered HIGH. CS provides for external Rank selection on systems with multiple Ranks. CS is considered part of the command code.
ODT	Input	On Die Termination: ODT (registered HIGH) enables termination resistance internal to the DDR2 SDRAM. When enabled, ODT is only applied to each DQ, DQS, DQS, RDQS, RDQS, and DM signal for x4/x8 configurations. For x16 configuration ODT is applied to each DQ, UDQS/UDQS, LDQS/LDQS, UDM, and LDM signal. The ODT pin will be ignored if the Extended Mode Register (EMRS) is programmed to disable ODT.
RAS, CAS, WE	Input	Command Inputs: RAS, CAS and WE (along with CS) define the command being entered.



ADVANCE INFORMATION

Direct RDRAM™ 64/72-Mbit (256Kx16/18x16d)

RQ7..RQ5 or ROW2..ROW0	I	RSL	Row access control. Three pins containing control and address information for row accesses.
RQ4..RQ0 or COL4..COL0	I	RSL	Column access control. Five pins containing control and address information for column accesses.
DQB8..DQB0	I/O	RSL	Data byte B. Nine pins which carry a byte of read or write data between the channel and the RDRAM.

EX2025 at 3

No individual "row address strobe [RAS], column address strobe [CAS] [...] and address lines"

Q. All right. So to be clear, a DDR memory device has a pin dedicated to a RAS signal and has a pin dedicated to a CAS signal; whereas, a Rambus direct DRAM does not; is that fair?

A. That is fair.

EX1095 at 235:1-236:25



EX1064 (JESD79-2) at 6

Rambus uses multiplexed “chip select” information, while JEDEC uses individual “chip select” lines

Synchronous DRAM Architectures, Organizations, and Alternative Technologies

Prof. Bruce L. Jacob

application: in the Rambus bus organization, all addresses, commands, data, and chip-select information are sent on the same bus lines. This is why the organization is called “multiplexed.” At different points in time, the same physical lines carry dissimilar classes of information.

EX1069 at 1, 11

Q. Do you consider Professor Bruce

Jacob to be an expert in the field of the '417 and '215 patents, the author of the textbook marked as Exhibit 1070?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: Yes. He's certainly quite knowledgeable in this field.

EX1095 at 163:15-:22



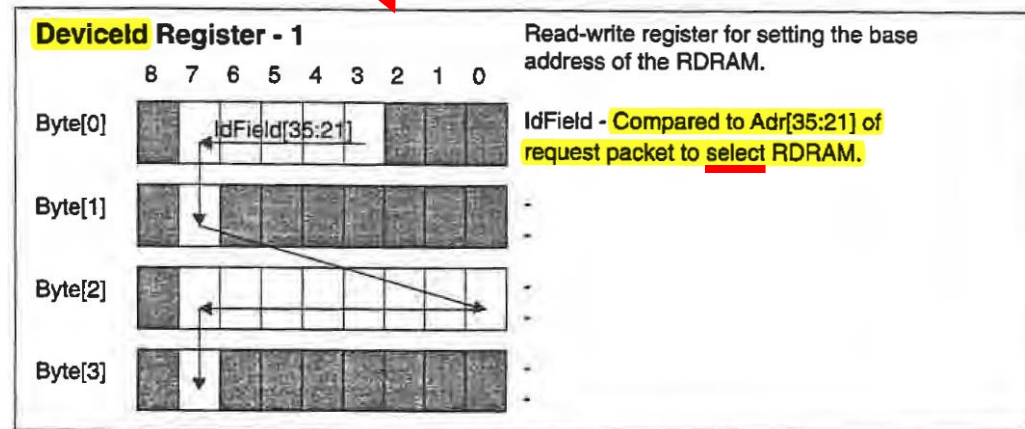
Q. And in that embodiment, the buffer of Perego would not receive chip select signals, for example, from the memory controller; correct?

MR. CHANDLER: Object to form.

THE WITNESS: I disagree. The Rambus protocol, for example, does include chip select signals. They are simply multiplexed

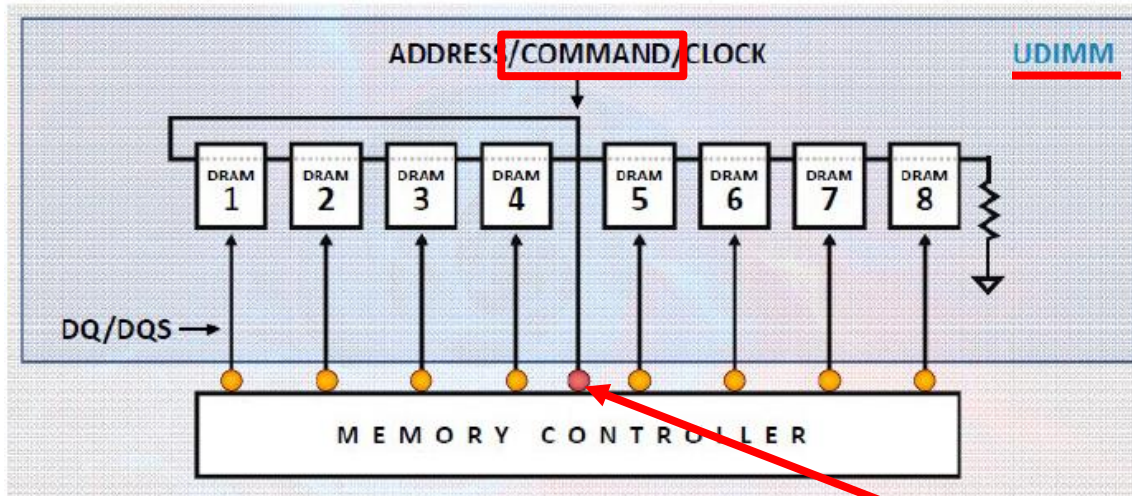
on to the same wires as other signals, in a packetized form.

EX2033 at 148:8-:16; see also id. at 149:24-150:17

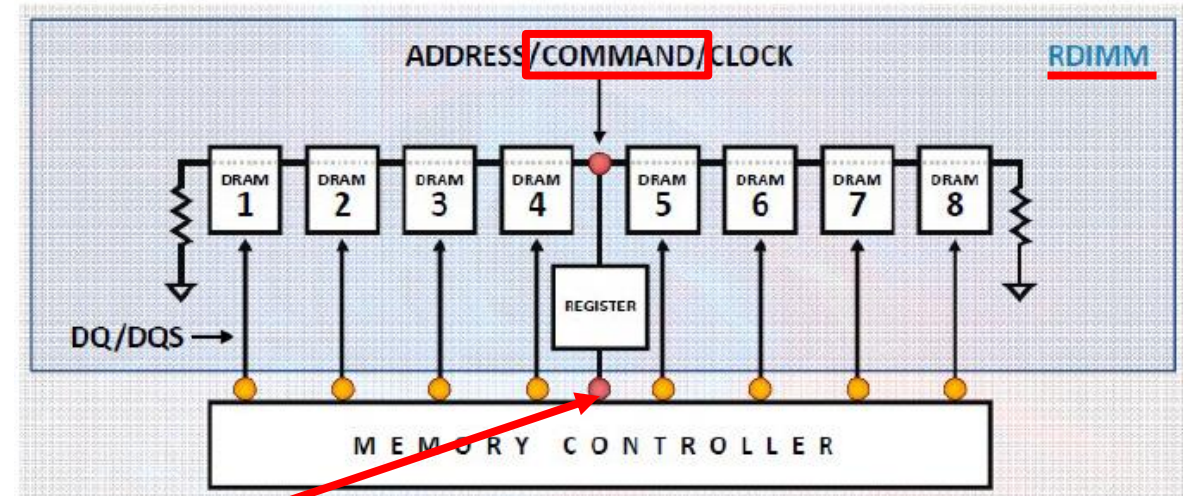


EX1097 at 821-22; see also EX1095 at 191:19-193:24

JESD79-2 is relevant to memory modules because it requires the command (e.g., read/write) to include “chip select” signals



EX1103 at 7; see also EX1095 at 57:2-9; EX2024, ¶132



EX1103 at 8; see also EX1095 at 57:2-9; EX2024, ¶132

$\overline{CS}$	Input	Chip Select: All commands are masked when $\overline{CS}$ is registered HIGH. $\overline{CS}$ provides for external Rank selection on systems with multiple Ranks. $\overline{CS}$ is considered part of the command code.
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EX1064 (JESD79-2) at 6

Jedec Standard No. 21-C

DDR SDRAM Registered **DIMM Design Specification**

Pin Name	Description
$\overline{RAS}$	SDRAM row address strobe
$\overline{CAS}$	SDRAM column address strobe
$\overline{WE}$	SDRAM write strobe
$\overline{S0} - \overline{S3}$	SDRAM chip select lines (Physical banks 0, 1, 2, and 3)

EX1062 at 6

JEDEC Standard No. 21C

DDR2 SDRAM Registered **DIMM Design Specification**

Pin Name	Description
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
$\overline{S}[3:0]$	Chip Selects

EX1066 at 6-7

JESD79-2 governs DDR2 signaling on all modules using DDR2 SDRAMs

Q. I just want to be clear at a high level. It's not like JEDEC has one standard for DDR memory devices that are intended for a UDIMM and a different standard for DDR memory devices intended for an RDIMM; instead, JEDEC has one standard for the memory device; and that same memory device may be used on different types of memory modules. Maybe it's a UDIMM. Maybe it's an RDIMM. Maybe it's something else.
Is that fair?

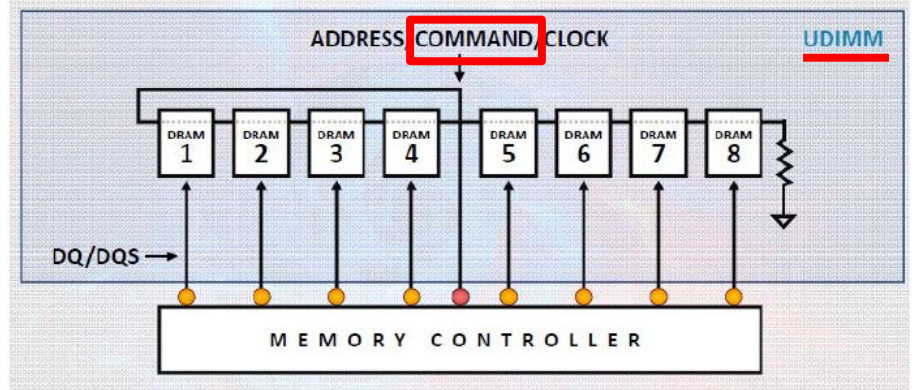
....
THE WITNESS: JEDEC has standardized SDRAMs of different flavors. It's also standardized modules that use those DRAMs that are standardized....
But, in general, your assertion is accurate, that the generations of modules and the generations of SDRAMs, both as standardized by JEDEC, go hand in hand.



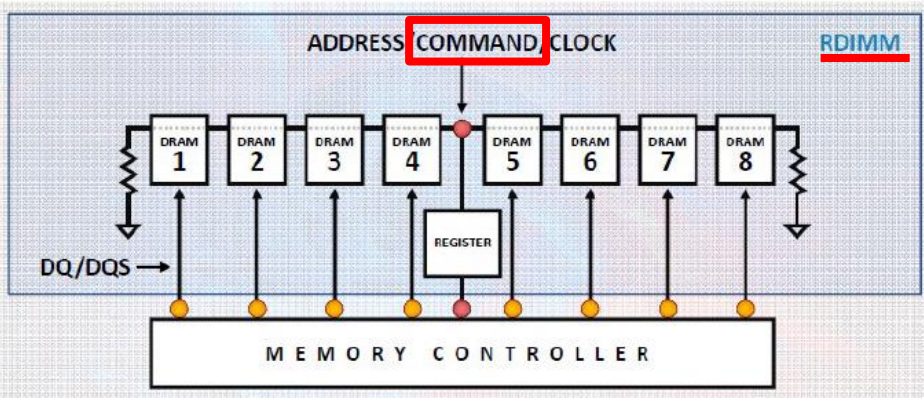
JEDEC DDR2 SDRAM SPECIFICATION

$\overline{CS}$	Input	Chip Select: All commands are masked when $\overline{CS}$ is registered HIGH. $\overline{CS}$ provides for external Rank selection on systems with multiple Ranks. $\overline{CS}$ is considered part of the command code.
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EX1064 (JESD79-2) at 6



EX1103 at 7 ; see also EX1095 at 57:2-:9; EX2024, ¶132



EX1103 at 8 ; see also EX1095 at 57:2-:9; EX2024, ¶132

No dispute a POSITA knew about the JEDEC standards for memory devices and modules, providing a motivation to use a JEDEC interface with “chip select” signals



master. Thus I believe a POSITA here would be knowledgeable about the operation of standardized DRAM and SDRAM memory devices and memory modules including these commercially available devices and how these devices and modules interacted with memory controllers of a computer system.

EX2024 ¶168; see also EX2024, ¶¶19-36 (admitting POSITA knew about chip select signals, UDIMM, and RDIMM); EX1095, 53:4-:23, 139:22-141:22



The motivation need **not** be found in the references sought to be combined, but may be found in any number of sources, including **common knowledge, the prior art as a whole**, or the nature of the problem itself."

DyStar Textilfarben GmbH v. C.H. Patrick Co., 464 F.3d 1356, 1361 (Fed. Cir. 2006)

Jedec Standard No. 21-C
DDR SDRAM Registered DIMM Design Specification

Pin Name	Description
$\overline{\text{RAS}}$	SDRAM row address strobe
$\overline{\text{CAS}}$	SDRAM column address strobe
$\overline{\text{WE}}$	SDRAM write strobe
$\overline{\text{S}}_0 - \overline{\text{S}}_3$	SDRAM chip select lines (Physical banks 0, 1, 2, and 3)

EX1062 at 6

JEDEC Standard No. 21C
DDR2 SDRAM Registered DIMM Design Specification

Pin Name	Description
$\overline{\text{RAS}}$	Row Address Strobe
$\overline{\text{CAS}}$	Column Address Strobe
$\overline{\text{WE}}$	Write Enable
$\overline{\text{S}}[3:0]$	Chip Selects

EX1066 at 6-7

A POSITA knew that chip-select signals are essential for JEDEC-style memory systems, and create “ranks” of one or more memory devices



DDR2 SDRAM SPECIFICATION

CS	Input	Chip Select: All commands are masked when CS is registered HIGH. CS provides for external Rank selection on systems with multiple Ranks. CS is considered part of the command code.
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EX1064 (JESD79-2) at 6

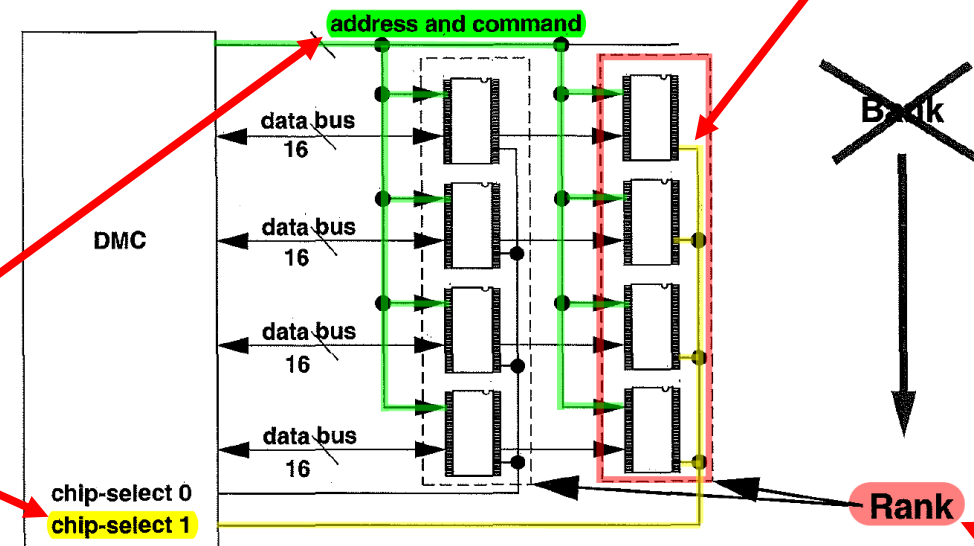


FIGURE 10.5: Memory system with 2 ranks of DRAM devices.

EX1070 (Jacob textbook) at 413-14

This last bus, the chip-select bus, is essential in a JEDEC-style memory system, as it enables the intended recipient of a memory request. A value is asserted on the chip-select bus at the time of a request (e.g., read or write). The chip-select bus contains a separate wire for every rank of DRAM in the system. The chip-select signal thus passes over a wire unique to each small set of DRAMs and enables or disables the DRAMs in that rank so that they, respectively, either handle the request currently on the bus or ignore the request currently on the bus. Thus, only the DRAMs to which the request is directed handle the request. Even though all DRAMs in the system are connected to the same address and control busses and could, in theory, all respond to the same request at the same time, the chip-select bus prevents this from happening.

EX1069 (Jacob Paper) at 2-3

Q. And do you believe it's consistent with the understanding of a person of ordinary skill in the art that the chip-select bus is essential in a JEDEC-style memory system?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: Yes. Because JEDEC-style -- JEDEC-defined and standardized SDRAMs have chip-select inputs, you need to have a mechanism for feeding those signals, so it is essential. If you don't have some mechanism for triggering the chip-select inputs of the SDRAMs, they will not operate as you expect.

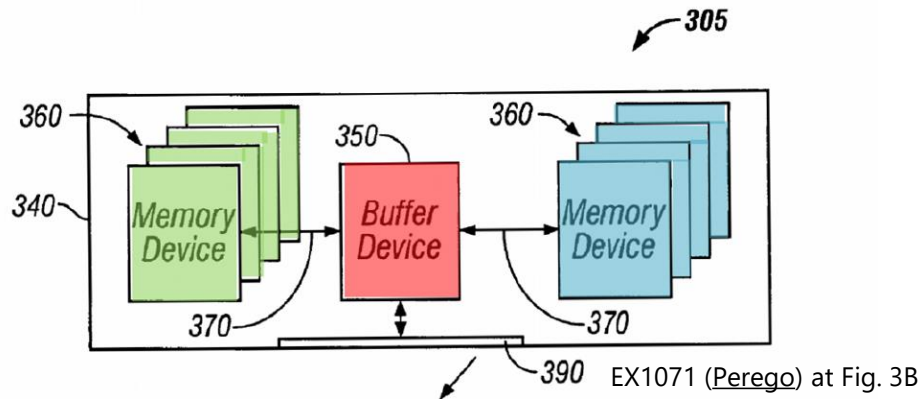
EX1095 at196:7-19

Rank

A rank of DRAMs, SIMMs, or DIMMs is the physical collection of devices that have to be present or not present as a group for the memory system to operate properly. A rank of memory typically consists of one or more DRAMs that are ganged in parallel and accessed together as a wider organizational unit. A rank may

EX1097 (Przybylski textbook) at 497

Perego's buffer was intended to be compatible with both existing and new memory devices and controllers, which by 2004-2005 were overwhelmingly JEDEC, not Rambus



Buffer device 350 provides a high degree of system flexibility. New generations of memory devices may be phased in with controller 310 or into memory system 300 by modifying buffer device 350. Backward compatibility with existing generations of memory devices (i.e., memory devices 360) may also be preserved. Similarly, new generations of controllers may be phased in which exploit features of new generations of memory devices while retaining backward compatibility with existing generations of memory devices.

EX1071 (Perego) at 6:34-:43

72. I note that in the 2004-2005 timeframe, the vast majority of the DRAM devices and modules sold would have been compliant with one of the JEDEC standards, such that a general reference to DRAM, especially in the context of usage main memory of general purpose computer and server systems, would suggest to a POSITA the use of JEDEC-standard compliant SDRAM devices or modules. For instance, a person of ordinary skill in the art would

EX2024, 1172



But you're absolutely correct that the industry did select the JEDEC approach and reject the Rambus approach.

BY ATTORNEY CHANDLER:

Q. And that was known by the 2004-2005 time frame?

A. Yeah. It was clear earlier than that even that it was not going to become the mainstream memory type for PCs and servers, at least.

EX1095 at 286:6-:15

JEDEC provided "high bandwidth" — even better than Rambus

TABLE Ov.3 Cross-comparison of SDRAM, DDR SDRAM, and DRDRAM memory systems

DRAM Technology	Operating Frequency (Data Bus)	Pin Count per Channel	Peak Bandwidth	Sustained BW on StreamAdd	Bits per Pin per Cycle (Peak)	Bits per Pin per Cycle (Sustained)
SDRAM	133	152	1064 MB/s	540 MB/s	0.4211	0.2139
DDR SDRAM	2 * 200	171	3200 MB/s	1496 MB/s	0.3743	0.1750
DRDRAM	2 * 600	117	2400 MB/s	1499 MB/s	0.1368	0.0854

JEDEC:
Rambus:

EX1070 at 23

Q. And in this comparison on page 23 of Exhibit 1070, the DDR memory system in the second row had a better peak bandwidth than the direct Rambus DRAM memory system; correct?

A. That's what he shows here, yes.

EX1095 at 230:23-231:2

Q. Do you consider Professor Bruce Jacob to be an expert in the field of the '417 and '215 patents, the author of the textbook marked as Exhibit 1070?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: Yes. He's certainly quite knowledgeable in this field.

EX1095 at 163:15-22

Q. So would it be fair to say both at the time of your book marked as Exhibit 1097, which is around 1996, as well as the time of the '417 and '215 patents in the 2004-2005 time frame, that a person of ordinary skill in the art knew that strengths of DDR SDRAMs and DDR2 SDRAMs included that they were standardized by JEDEC; they were commodity parts; they were interchangeable parts; and that high bandwidth was possible?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: Yes. However, what constitutes high bandwidth in 2000 -- I'm sorry -- 1996 is different than what passes for high bandwidth in 2004 and '5. But, generally speaking, that's true.

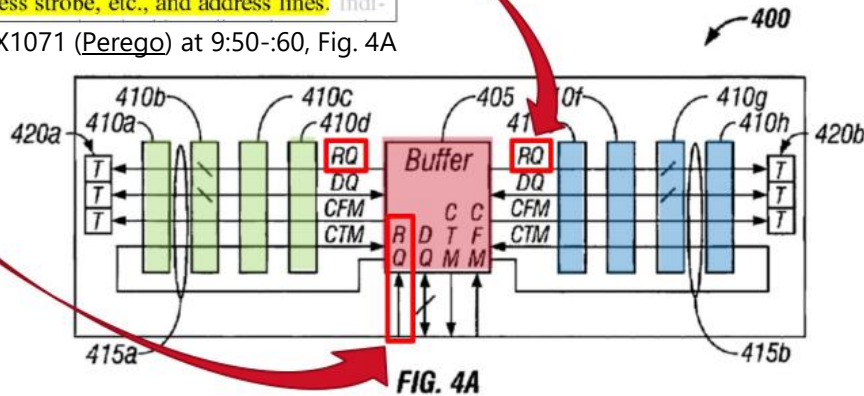
EX1095 at 181:23-182:14



Perego discloses a “bus” with individual lines consistent with JEDEC, not just “point-to-point” connections like Rambus

In alternate embodiments, control lines (RQ) may comprise individual control lines, for example, row address strobe, column address strobe, etc., and address lines. Indi-

EX1071 (Perego) at 9:50-:60, Fig. 4A



Here and in the detailed description to follow, “bus” denotes a plurality of signal lines, each having one or more connection points for “transceiving” (i.e., transmitting or receiving). Each connection point connects or couples to a

EX1071 (Perego) at 1:50-:53

In several embodiments, one or more busses or a plurality of point-to-point links may be used to couple one or more buffer devices to a master (e.g., a controller or microprocessor device). A dynamic point-to-point link topology or

EX1071 (Perego) at 3:41-:44

subsystem port via one point-to-point link. The memory subsystem port is disposed on the memory controller interface, which includes a plurality of memory subsystem ports, each having a connection to a point-to-point link. In other embodiments, memory subsystems are connected to a memory subsystem port via a bus (i.e., a plurality of signal lines). A combination of bus and point-to-point connections

EX1071 (Perego) at 5:18-:24

Signaling over point-to-point links 320a-320n or alternatively, over bussed topologies, may incorporate different modulation methods such as non-return to zero (NRZ),

EX1071 (Perego) at 8:42-:44



Q. Well, in general, Perego describes, for example, a point-to-point topology; correct?

A. Perego describes a point-to-point topology for Rambus embodiments. He doesn't limit his invention in any way to a point-to-point topology. And, in fact, by explaining that his invention can be built with DDR2, he specifically informs a reader that a point-to-point topology is not necessary.

EX2033 at 29:3-:11

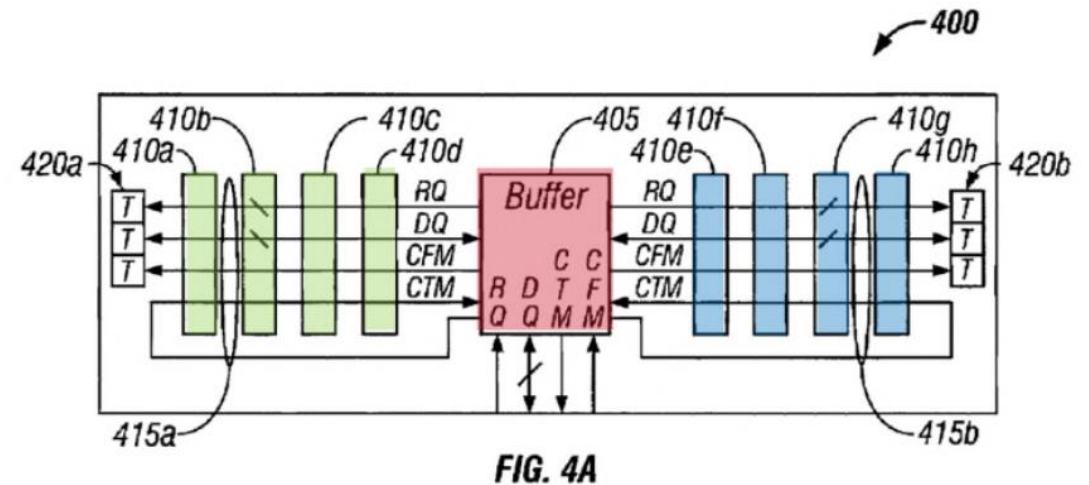
Perego does not require a Rambus interface when (optionally) “translat[ing] protocols” from the controller to the memory devices



A. No. Because, again, Perego tells us that his embodiments are compatible with DDR. A person of ordinary skill would know how to build a memory interface for a variety of different known memory types by following the specifications.

And there's no reason, in view of Perego, why they would necessarily need to use a Rambus-compatible memory interface. Perego teaches that the interface need not be a Rambus-compliant interface, either.

EX2033 at 132:13-:22

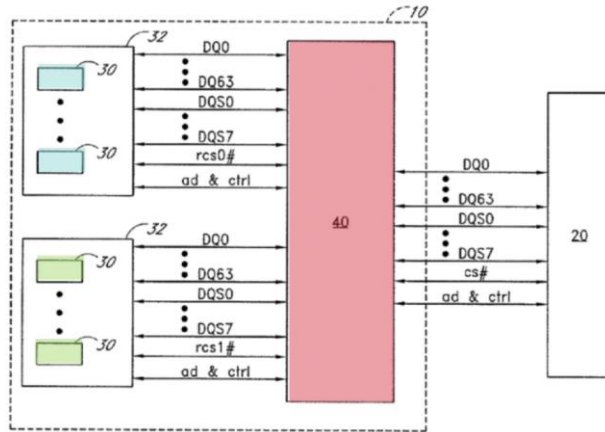


system. Different types of memory devices may be included on different modules within a memory system, by employing buffer device 405 to translate protocols employed by controller 310 to the protocol utilized in a particular memory device implementation.

EX1071 (Perego) at 10:63-:67 & Fig. 4A

"Translat[ion]" does not require a Rambus interface; it includes rank multiplication using the "address bit" of a JEDEC interface

'417/215 Patents

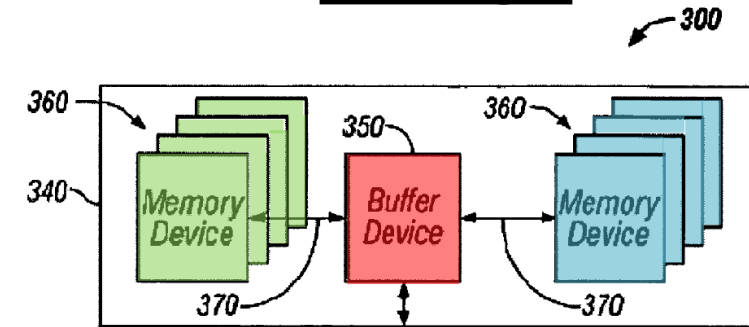


In certain embodiments utilizing memory density multiplication embodiments, the memory module 10 can have various types of memory devices 30 (e.g., DDR1, DDR2, DDR3, and beyond). The circuit 40 of certain such embodiments utilizes implied translation logic equations having variations depending on whether the density transition bit is a row, column, or internal bank address bit. In addition, the translation logic equations of certain embodiments vary depending on the type of memory module 10 (e.g., UDIMM, RDIMM, FBDIMM, etc.). Furthermore, in certain embodi-

'417: EX1001 at 23:23-35 & Fig.1

'215: EX1001 at 21:8-20 & Fig. 1

Perego



EX1071 (Perego) at Fig. 3A (in part)

system. Different types of memory devices may be included on different modules within a memory system, by employing buffer device 405 to translate protocols employed by controller 310 to the protocol utilized in a particular memory device implementation.

EX1071 (Perego) at 10:63-:67

ondary channel signal lines for each transaction. According to a preferred embodiment, the target subset of secondary channel signal lines may be selected via address bits provided as part of the primary channel request. By accessing

EX1071 (Perego) at 15:37-40; see also EX2033 at 176:22-178:6

Rank multiplication was a known technique to save costs

(19) **United States**

(12) **Patent Application Publication**
Amidi et al.

(22) Filed: **Jan. 5, 2004**

(10) Pub. No.: **US 2006/0117152 A1**
(43) Pub. Date: **Jun. 1, 2006**

(54) **TRANSPARENT FOUR RANK MEMORY
MODULE FOR STANDARD TWO RANK
SUB-SYSTEMS**

[0041] The CPLD 410 emulates a two rank memory module on the four rank memory module 400. CPLD 410 allows a system having a memory socket with only two chip select signals routed to interface with a four rank memory module where typically a two rank memory module couples with the memory socket. The CPLD 410 determines which rank from the four ranks to activate based upon the address and command signals from a memory controller coupled to the memory module 410. The algorithm of CPLD 410 is further described in FIGS. 5 and 7.

[0043] FIG. 5 illustrates a truth table used in the process of the CPLD 410 to determine which rank is active (rank 0, rank 1, rank 2, or rank 3). CPLD 410 utilized three variables to determine the active rank: the highest address number Add(n), a first chip select signal (CS0), and a second chip select signal (CS1). As previously mentioned, each memory socket includes two active chip select signals (CS0 and CS1). CPLD 410 combines these two variables (CS0 and CS1) with the address number signal 210 from the address bus 202 to determine the active rank. Add(n) includes the highest binary digit from the address number signal 210. For example, the highest address number Add(n) when the address signal 210 is 10010 would be the first digit to the left: "1".

[0008] Because memory devices with lower densities are cheaper and more readily available, it may be advantageous to build the above same density memory module using lower densities devices. However, in order to achieve a density of,

Add(n)	CS1	CS0	Active Bank
0	1	0	0
0	0	1	1
1	1	0	2
1	0	1	3

Truth Table
FIG.5

1Gb: \$\$\$\$\$\$
\$\$\$\$\$\$

512Mb: \$
512Mb: \$

EX1079 (Amidi) at [0008], [0041, 43] & Fig.5

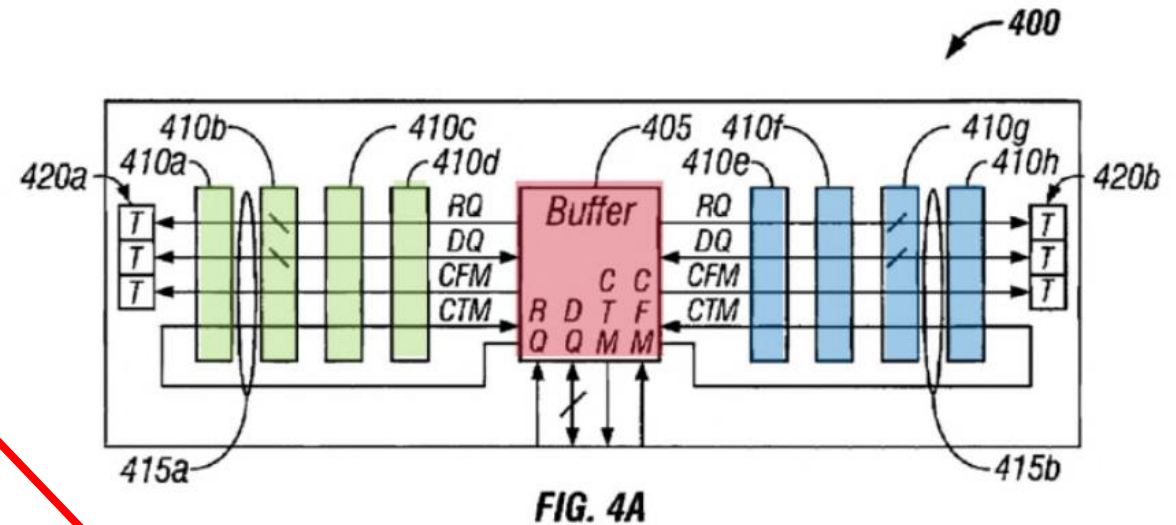
IT WAS OBVIOUS TO COMBINE
PEREGO WITH JESD79-2

The Institution Decision correctly found a motivation to combine Perego and JESD79-2



On this record, we are sufficiently persuaded by Petitioner's argument that a person of ordinary skill in the art **would have combined the teachings of Perego and JESD79-2**. As Petitioner correctly points out (Pet. 30), **Perego discloses using DDR2 memory devices**. Ex. 1071, 10:56–59 (“Other memory devices may be implemented on module 400, for example, Double Data Rate 2 (DDR2) DRAM devices and Synchronous DRAM (SDRAM) devices.”). On this record, **we find this teaching to use DDR2 sufficiently supports Petitioner's rationale to combine Perego with JESD79-2**, which is the JEDEC DDR2 SDRAM Specification. Ex. 1064, 1 (cover page). As to Patent Owner's argument that Rambus memories lack a chip select network (Prelim. Resp. 37), the reference on which Patent Owner relies discloses that chip select information is still used in the particular Rambus devices described. See Ex. 1069, 11 (“[I]n the Rambus bus organization, all addresses, commands, data, and chip-select information are sent on the same bus lines.”), 12 (“[T]he example system uses a total of nine (9) lines to carry all necessary information, including addresses, commands, chip-select information, and data.”). Thus, on this record, Patent Owner's focus on the lack of a chip select network, which is not recited in the claims of the '417 patent, appears misplaced. We address Patent Owner's more specific arguments below in the discussion of individual claim recitations.

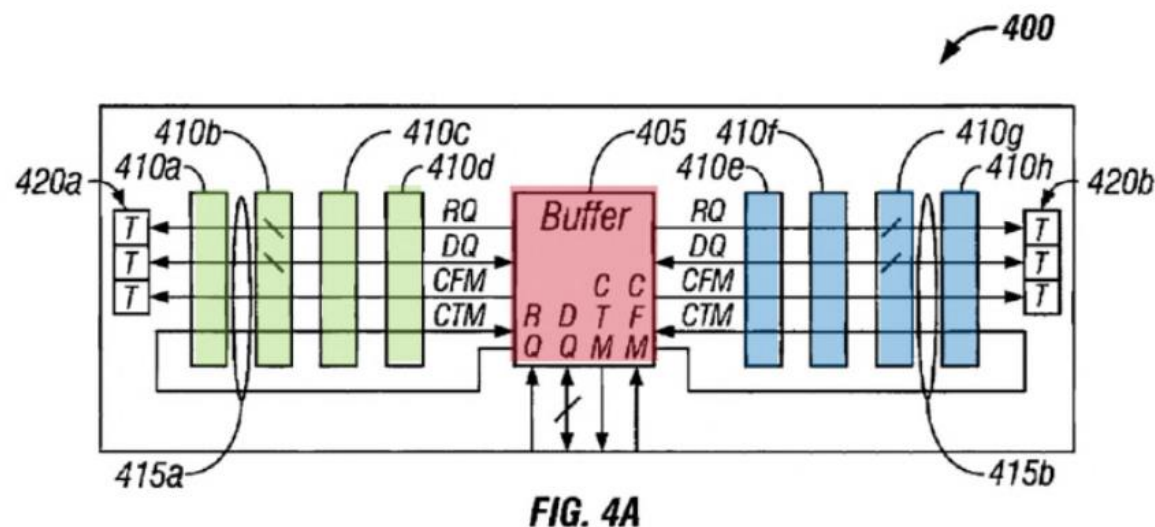
'417: Paper 11 (ID) at 14; see also '215: Paper 11 (ID) at 14-15



In one embodiment, memory devices **410a–410h** are Rambus® Dynamic Random access Memory (RDRAM) devices operating at a data rate of 1066 Mbts/sec. Other memory devices may be implemented on module 400, for example, **Double Data Rate 2 (DDR2) DRAM devices and Synchronous DRAM (SDRAM) devices**. Utilizing buffer

EX1071 (Perego) at 10:54–:59 & Fig. 4A

Perego teaches using DDR2, which Netlist admits use “chip-select signals” to select “ranks”

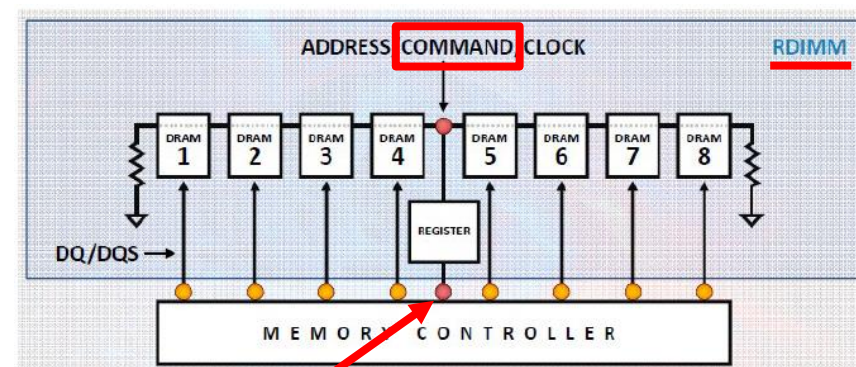


In one embodiment, memory devices 410a–410h are Rambus® Dynamic Random access Memory (RDRAM) devices operating at a data rate of 1066 Mbits/sec. Other memory devices may be implemented on module 400, for example, Double Data Rate 2 (DDR2) DRAM devices and Synchronous DRAM (SDRAM) devices. Utilizing buffer

EX1071 (Perego) at 10:54--:59 & Fig. 4A

differences between JEDEC-style memory and Rambus memory). This is particularly true for chip-select signals, which are a hallmark of JEDEC-compliant bus architecture and relate to several claim elements of the '215 Patent. E.g., EX2024, ¶ 132; EX1069, 2 (characterizing “the chip-select bus” as “essential in a JEDEC-style memory system”). Chip-select signals are used to select ranks, e.g., EX2031, 7 (“Rank: any DRAMs connected to the same CS”), and the concept of

'215: Paper 22 (POR) at 22; see also '417: Paper 22 (POR) at 21



EX1103 at 8; see also EX2024, ¶132

CS	Input	Chip Select: All commands are masked when CS is registered HIGH. CS provides for external Rank selection on systems with multiple Ranks. CS is considered part of the command code.
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EX1064 (JESD79-2) at 6

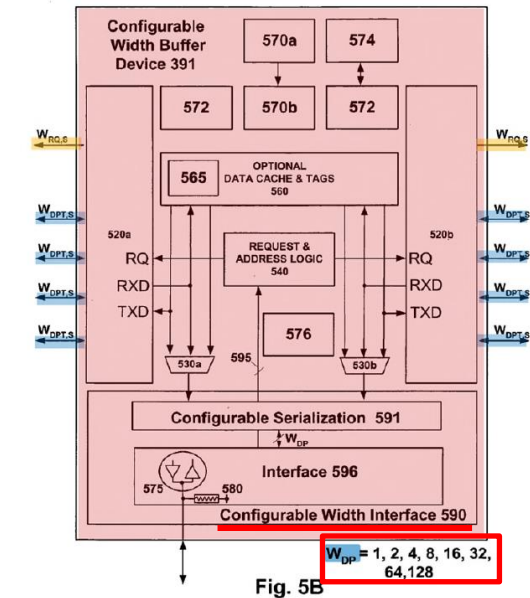
Perego's "configurable width interface" is compatible with JEDEC

Q. Can you have a configurable bit width module that is compliant with JEDEC specifications?

A. I would think so, because if you read Perego, he indicates that one of the ways of configuring it is to have a resistor or a jumper that's installed at manufacture time that configures it to a fixed bit width. In that case, I think it can certainly be JEDEC compliant.



EX2033 at 127:10-128:13; see also *id.* at 135:18-138:8



Various types of state storage are possible. In the described embodiment, the state storage takes the form of a width selection register or latch. This type of state can be easily changed via software during system operation, allowing a high degree of flexibility, and making configuration operations that are transparent to the end user. However, other types of state storage are possible, including but not limited to manual jumper or switch settings and module presence detection or type detection mechanisms. The latter class of mechanisms may employ pull-up or pull-down resistor networks tied to a particular logic level (high or low), which may change state when a module is added or removed from the system.

EX1071 (Perego) at 16:53-:65 & Fig. 5B

Perego discloses a serialization ratio of 1:1 for the “configurable width interface,” e.g., 64-bit interface and 64-bit ranks, which is compatible with DDR2



Furthermore, Perego discloses a serialization ratio of 1:1, meaning that the memory device access width (W_A) and the configured buffer device interface width (W_{DP}) are the same. Ex. 1071, 14:32–40, 17:22–28. In such a configuration, each rank would match the full bit-width of the memory module as in Petitioner’s proposed construction. See Pet. 26.

‘417: Paper 11 (ID) at 26; see also ‘215: Paper 11 (ID) at 20

FIG. 5C illustrates another embodiment of configurable width interface 590 shown in FIG. 5B. FIG. 5C illustrates a multiplexer/demultiplexer circuit 597, for example that may be disposed in configurable serialization circuit 591 (FIG. 5B) to perform multiplexing/demultiplexing functions. For the embodiment illustrated by FIG. 5C, the serialization ratio is 1:1. Serialization ratios greater than 1:1 are possible

EX1071 (Perego) at 17:22-:28

$$R_S = W_A : W_{DP}$$

Where:

R_S =Serialization Ratio

W_A =Memory Device Access Width

W_{DP} =Configured Buffer Device Interface Width

EX1071 (Perego) at 14:35-:40

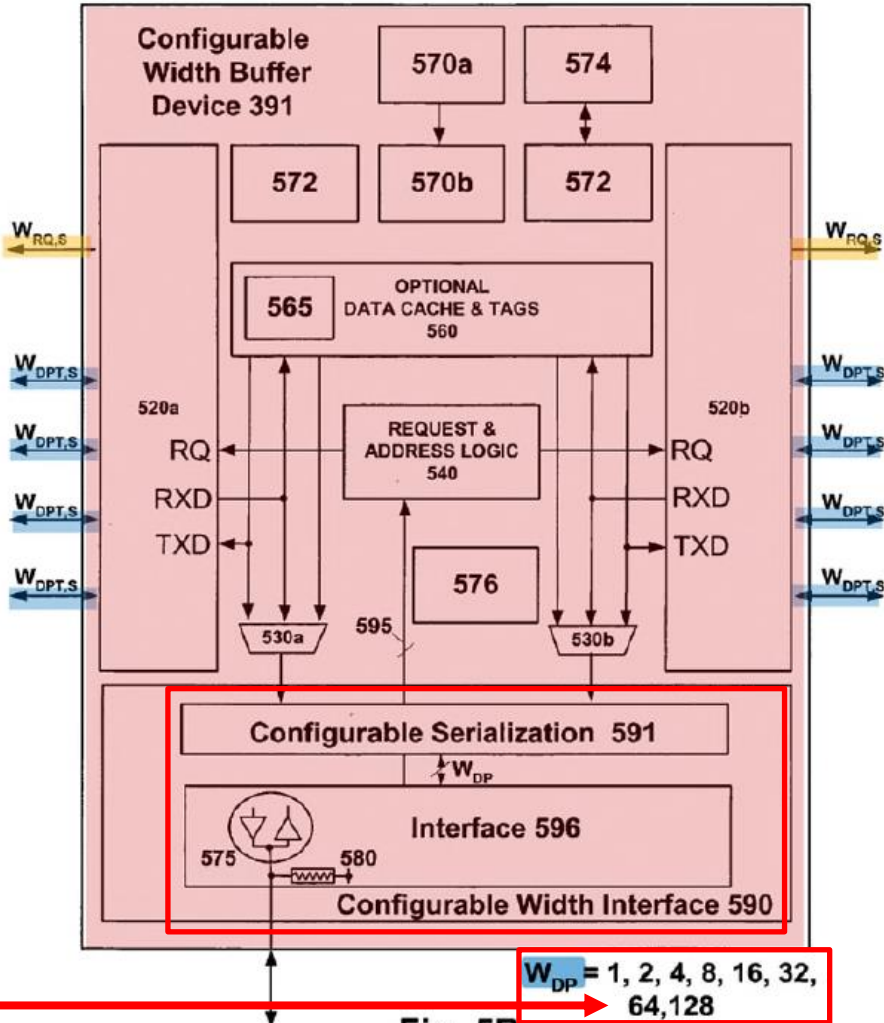
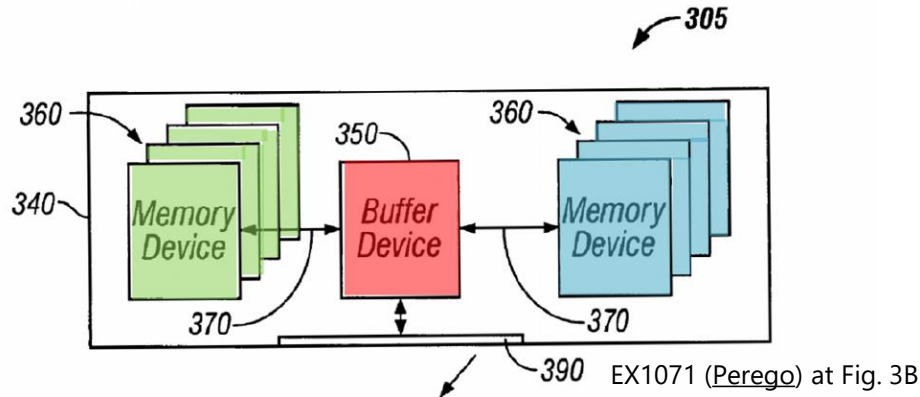


Fig. 5B

EX1071 (Perego) at Fig. 5B

‘417: Paper 27 (Reply) at 12; Paper 1 (Pet.) at 37-38, 64-69
‘215: Paper 27 (Reply) at 11-12; Paper 1 (Pet.) at 39, 57-59

Perego's flexibility and compatibility targeted existing and future memory controllers, the "vast majority" of which complied with JEDEC



Buffer device 350 provides a high degree of system flexibility. New generations of memory devices may be phased in with controller 310 or into memory system 300 by modifying buffer device 350. Backward compatibility with existing generations of memory devices (i.e., memory devices 360) may also be preserved. Similarly, new generations of controllers may be phased in which exploit features of new generations of memory devices while retaining backward compatibility with existing generations of memory devices.

EX1071 (Perego) at 6:34-:43

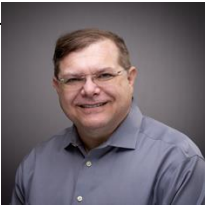
72. I note that in the 2004-2005 timeframe, the vast majority of the DRAM devices and modules sold would have been compliant with one of the JEDEC standards, such that a general reference to DRAM, especially in the context of usage main memory of general purpose computer and server systems, would suggest to a POSITA the use of JEDEC-standard compliant SDRAM devices or modules. For instance, a person of ordinary skill in the art would



EX2024, ¶72

Q. Would you agree that system layout resource requirements would be a factor when one is deciding how to implement a memory module?

A. It could be a factor. But we know both at that time and prior and subsequently, the vast majority of -- the majority of the market chose to use parallel signal connection paths and not a narrow packet protocol approach.



EX2033 at 149:7-:23

JEDEC was known as a suitable option — even better than Rambus

JEDEC:
Rambus:

TABLE Ov.3 Cross-comparison of SDRAM, DDR SDRAM, and DRDRAM memory systems

DRAM Technology	Operating Frequency (Data Bus)	Pin Count per Channel	Peak Bandwidth	Sustained BW on StreamAdd	Bits per Pin per Cycle (Peak)	Bits per Pin per Cycle (Sustained)
SDRAM	133	152	1064 MB/s	540 MB/s	0.4211	0.2139
DDR SDRAM	2 * 200	171	3200 MB/s	1496 MB/s	0.3743	0.1750
DRDRAM	2 * 600	117	2400 MB/s	1499 MB/s	0.1368	0.0854

Q. And in this comparison on page 23 of Exhibit 1070, the DDR memory system in the second row had a better peak bandwidth than the direct Rambus DRAM memory system; correct?

A. That's what he shows here, yes.

EX1095 at 230:23-231:2

Q. Do you consider Professor Bruce Jacob to be an expert in the field of the '417 and '215 patents, the author of the textbook marked as Exhibit 1070?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: Yes. He's certainly quite knowledgeable in this field.

EX1095 at 163:15-:22



"[I]t's not necessary to show that a combination is the *best* option, only that it be a ***suitable*** option."

Intel Corp. v. PACT XPP Schweiz AG,
61 F.4th 1373, 1380-81 (Fed. Cir. 2023)

The motivation to combine can be found outside the references being combined, such as JESD21-C discussed in the Petition and Institution Decision



The motivation need **not** be found in the references sought to be combined, but may be found in any number of sources, including **common knowledge, the prior art as a whole, or the nature of the problem itself.**

DyStar Textilfarben GmbH v. C.H. Patrick Co., 464 F.3d 1356, 1361 (Fed. Cir. 2006)

EX1062, pp.1, 5-9; EX1066, pp.1, 4-8. Indeed, Perego discloses an upgradeable memory system that includes interfaces for DIMM and other removable memory modules, EX1071, 1:58-2:6 (discussing DIMM format disclosed by U.S. Patent No. 5,513,135, EX1081), along with a need for “flexible and cost effective upgrade capabilities,” EX1071, 2:26-29, 6:34-43. *See* EX1003, ¶180. A POSITA would have therefore been motivated to implement Perego’s memory modules in a registered DIMM format with DDR memory devices that fits into DIMM connectors and uses DIMM module input signals, according to JEDEC standards, including JESD21-C and JESD79-2. EX1003, ¶¶180-183. Perego also discloses

‘417: Paper 1 (Pet.) at 32; *see also* ‘215: Paper 1 (Pet.) at 34

Jedec Standard No. 21-C

DDR SDRAM Registered **DIMM Design Specification**

Pin Name	Description
$\overline{\text{RAS}}$	SDRAM row address strobe
$\overline{\text{CAS}}$	SDRAM column address strobe
$\overline{\text{WE}}$	SDRAM write strobe
$\overline{\text{S}}_0 - \overline{\text{S}}_3$	SDRAM chip select lines (Physical banks 0, 1, 2, and 3)

EX1062 at 6

JEDEC Standard No. 21C

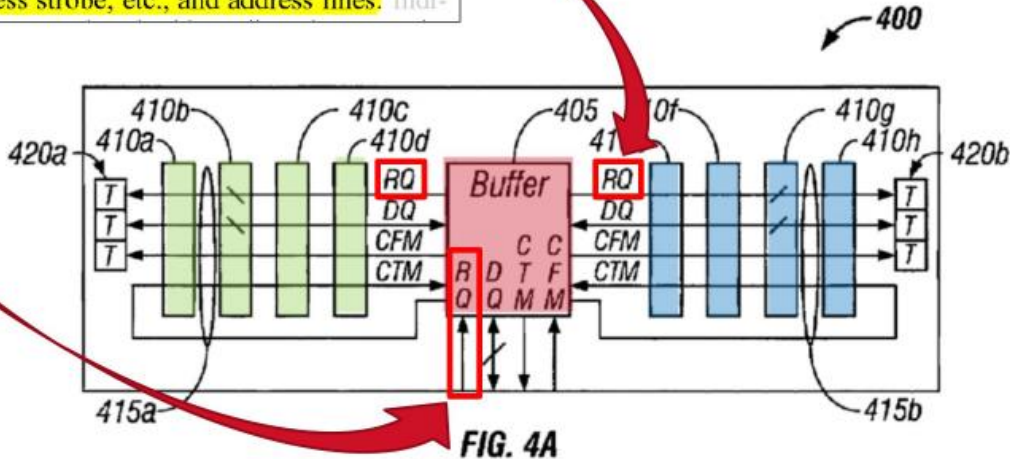
DDR2 SDRAM Registered **DIMM Design Specification**

Pin Name	Description
$\overline{\text{RAS}}$	Row Address Strobe
$\overline{\text{CAS}}$	Column Address Strobe
$\overline{\text{WE}}$	Write Enable
$\overline{\text{S}}[3:0]$	Chip Selects

EX1066 at 6-7

“Translat[ing] protocols” in Perego includes from one JEDEC protocol to another (both with address/control lines), and does not require a Rambus interface

In alternate embodiments, control lines (RQ) may comprise individual control lines, for example, row address strobe, column address strobe, etc., and address lines. Indi-

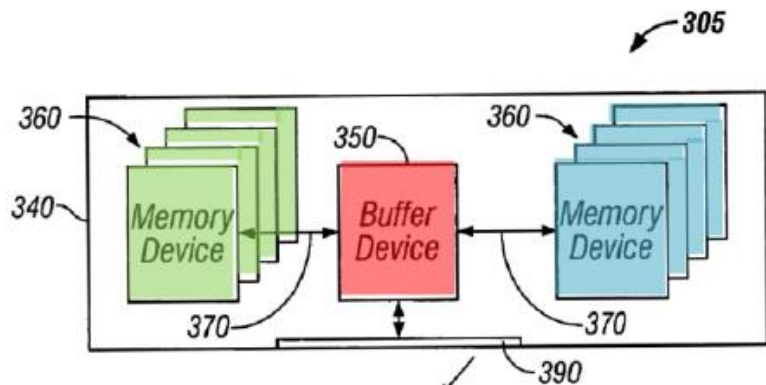


EX1071 (Perego) at 9:50-60, Fig. 4A

In one embodiment, memory devices 410a-410h are Rambus® Dynamic Random access Memory (RDRAM) devices operating at a data rate of 1066 Mbits/sec. Other memory devices may be implemented on module 400, for example, Double Data Rate 2 (DDR2) DRAM devices and Synchronous DRAM (SDRAM) devices. Utilizing buffer device 405 between the memory devices and controller in accordance with the present invention (e.g., see FIG. 3) may feasibly render the type of memory device transparent to the system. Different types of memory devices may be included on different modules within a memory system, by employing buffer device 405 to translate protocols employed by controller 310 to the protocol utilized in a particular memory device implementation.

EX1071 (Perego), 10:54-67 & Fig. 4A

A JEDEC-style implementation of Perego would not sacrifice its benefits or basic principles, including electrical “isolation” by the buffer for high performance



With further reference to FIGS. 3A and 3B, buffer device 350 transceives and provides isolation between signals interfacing to controller 310 and signals interfacing to the plurality of memory devices 360. In a normal memory read

EX1071 (Perego) at 6:12-:15 & Fig.3B

Q. What impact does a higher electrical load have on data signals that are being transmitted to and from a memory controller?

THE WITNESS: Again, that's a question that requires a substantial amount of electronics and math to answer properly. Just say that higher loads are more challenging and have negative impacts.

Q. And what impact does a buffer on the data lines have with respect to loads on the data signals?

THE WITNESS: Again, within the context of 2004-2005 and the knowledge and experience of a POSITA, the general idea that reducing or otherwise managing loads to minimize their impact on data communications is a good thing.

EX1095 at 130:6-:16, 130:23-131:8 (objections omitted);
see also *id.* at 124:23-126:21, 136:8-137:11



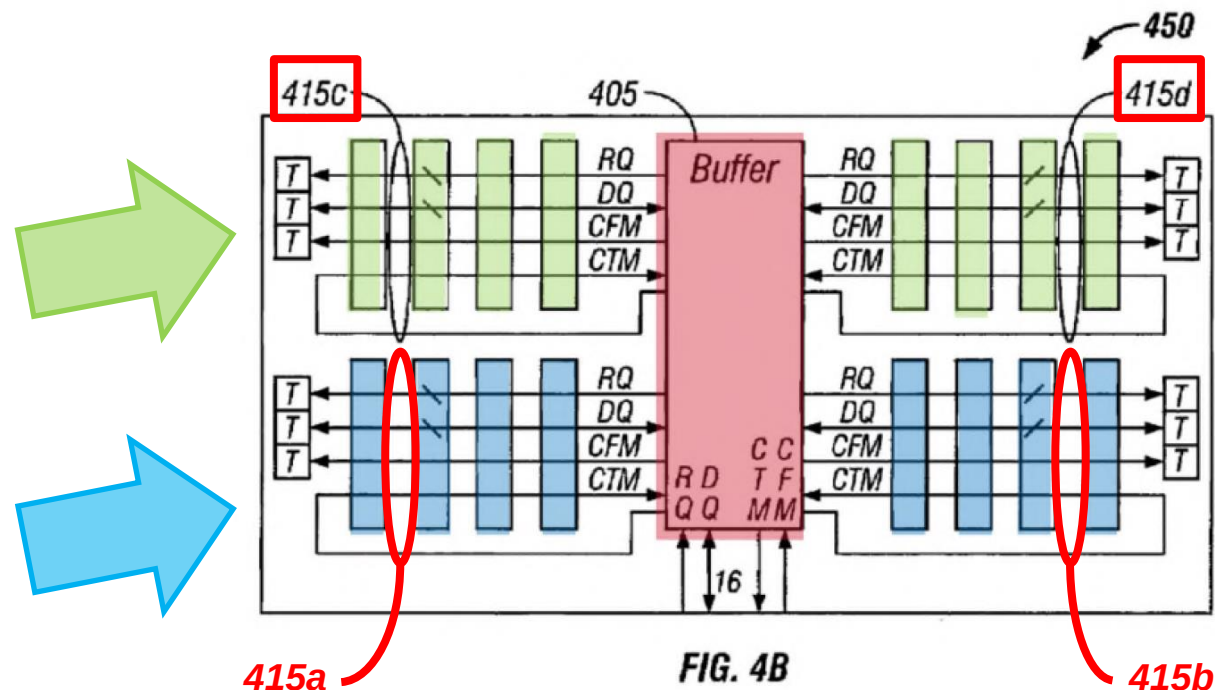
PEREGO AND JESD79-2 TEACH JEDEC-STYLE "RANKS" USING CHIP SELECTS

Netlist has admitted Perego discloses “ranks”



or write the full bit-width of the memory module.” Pet., 12. Perego-422 would inform a person of ordinary skill in the art that, in the paired arrangement, **the devices connected to channels 415c/d correspond to one “rank”** because they are “routed in parallel,” that is, the memory devices would be understood to “act together in response to command signals.” For similar reasons, a person of ordinary skill in the art would understand that **the devices connected to channels 415a/b correspond to another “rank.”** Thus, in the paired arrangement, Perego-422’s **Figure 4B illustrates two ranks: one corresponding to memory devices connected to channels 415c/d, the other corresponding to memory devices connected to channels 415a/b.** Likewise, a person of ordinary skill in the art

EX1020, ¶194; see also EX1019, p.43; EX1102, ¶131



included in each channel. FIG. 4B illustrates a quad-channel module 450 having **channels 415a–415d**. In this embodi-

EX1071 (Perego) at 10:22–:24 & Fig.4B

Perego discloses a serialization ratio of 1:1 for the “configurable width interface,” e.g., 64-bit interface and 64-bit ranks, which is compatible with DDR2



Furthermore, Perego discloses a serialization ratio of 1:1, meaning that the memory device access width (W_A) and the configured buffer device interface width (W_{DP}) are the same. Ex. 1071, 14:32–40, 17:22–28. In such a configuration, each rank would match the full bit-width of the memory module as in Petitioner’s proposed construction. See Pet. 26.

‘417: Paper 11 (ID) at 26; see also ‘215: Paper 11 (ID) at 20

FIG. 5C illustrates another embodiment of configurable width interface 590 shown in FIG. 5B. FIG. 5C illustrates a multiplexer/demultiplexer circuit 597, for example that may be disposed in configurable serialization circuit 591 (FIG. 5B) to perform multiplexing/demultiplexing functions. For the embodiment illustrated by FIG. 5C, the serialization ratio is 1:1. Serialization ratios greater than 1:1 are possible

EX1071 (Perego) at 17:22-:28

$$R_S = W_A : W_{DP}$$

Where:

R_S =Serialization Ratio

W_A =Memory Device Access Width

W_{DP} =Configured Buffer Device Interface Width

EX1071 (Perego) at 14:35-:40

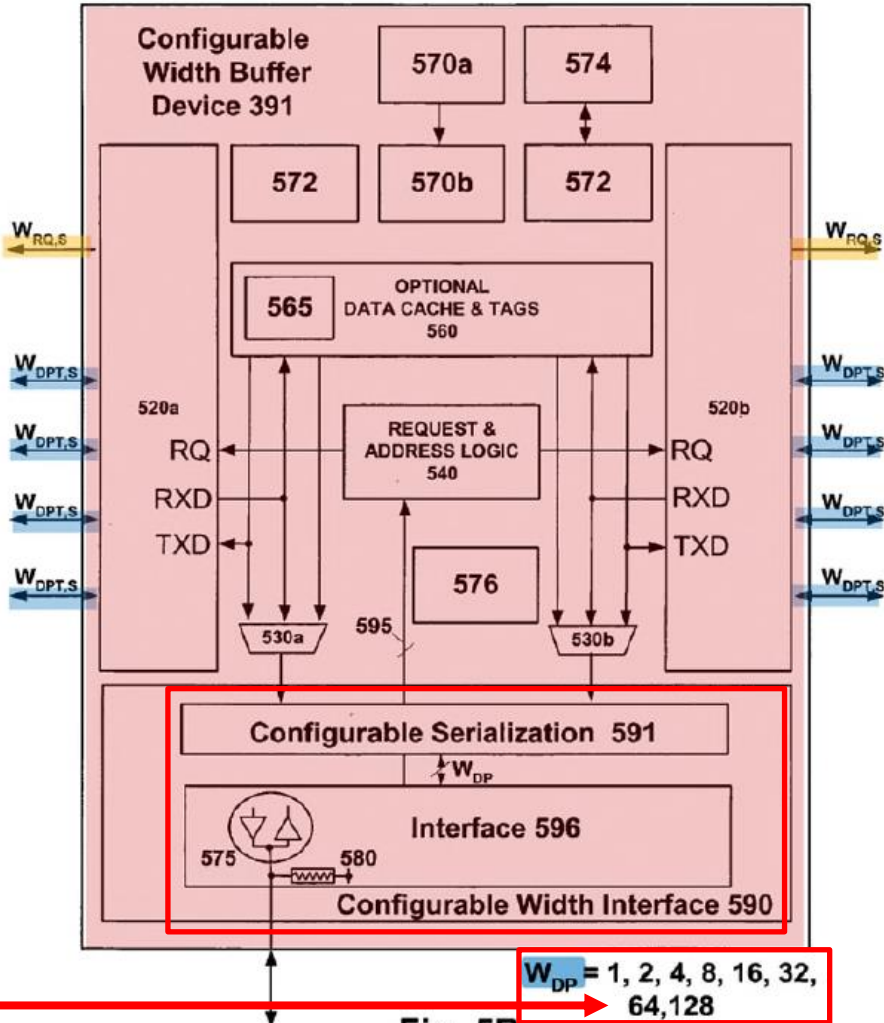


Fig. 5B

EX1071 (Perego) at Fig. 5B

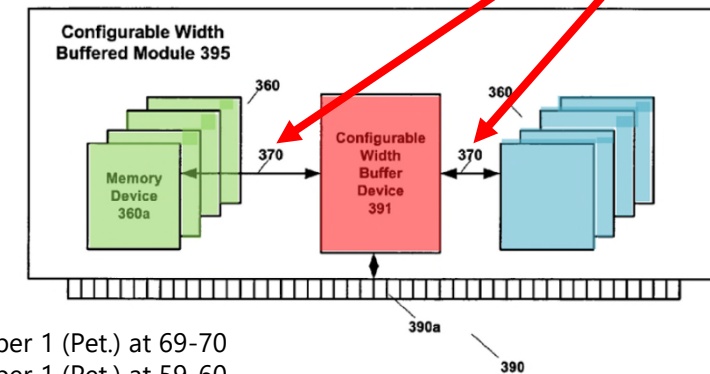
‘417: Paper 27 (Reply) at 12; Paper 1 (Pet.) at 37-38, 64-69
‘215: Paper 27 (Reply) at 11-12; Paper 1 (Pet.) at 39, 57-59

Perego discloses multiple channels for data, corresponding to multiple ranks of memory devices

7:65-8:5, 13:6-17 In that configuration, Dr. Przybylski further explains that a POSITA would understand, particularly in view of the '099 Application incorporated by reference in Perego, that interfaces 520a and 520b of the configurable buffer device 391 in Figure 3C work in tandem and that all of the memory devices would need to be activated together as one DDR SDRAM rank.

Paper 22 (POR) at 34

Perego teaches that the data width accessed in a memory transaction (W_A), and the data width of the buffer interfacing with the memory controller (W_{DP}), can both be the same (e.g., both 64 bits), such that the ratio $W_A/W_{DP} = 1:1$. EX1071, 14:16-40, 17:22-28 ("1:1"), Fig.5C; EX1003, ¶281. A POSITA would understand that W_A refers to the bit-width of each "rank" of memory devices (e.g., 64 bits can be read or written at a time) when only "one" of the "one or more channels 370" (shown below) is used for a read or write operation. EX1071, 6:12-24, 14:23-27, Fig.3C; EX1003, ¶¶282-283. Accordingly, when Perego's buffer device has two channels, and each channel is connected to one rank, Perego's module includes two ranks of memory devices (green and blue below). EX1003, ¶283.



'417: Paper 1 (Pet.) at 69-70
'215: Paper 1 (Pet.) at 59-60

Fig. 3C

Netlist’s argument that Figures 4A-C show Rambus DRAM (RDRAM) ignores Perego’s express disclosure of DDR2, which requires chip-selects and “ranks”

Petitioner nonetheless presents colored versions of Perego’s Figures 3C, 4A, 4B, and 4C to suggest ranks. Pet. 64-65. A POSITA, however, would understand that the memories depicted in Figures 4A-4C are Direct RDRAM embodiments, which do not receive chip-select signals, EX2024, ¶¶ 167, 170; EX1071, 10:54-56;

Paper 22 (POR) at 33

In one embodiment, memory devices 410a–410h are Rambus® Dynamic Random access Memory (RDRAM) devices operating at a data rate of 1066 Mbits/sec. Other memory devices may be implemented on module 400, for example, Double Data Rate 2 (DDR2) DRAM devices and Synchronous DRAM (SDRAM) devices. Utilizing buffer

EX1071 (Perego) at 10:54-:59

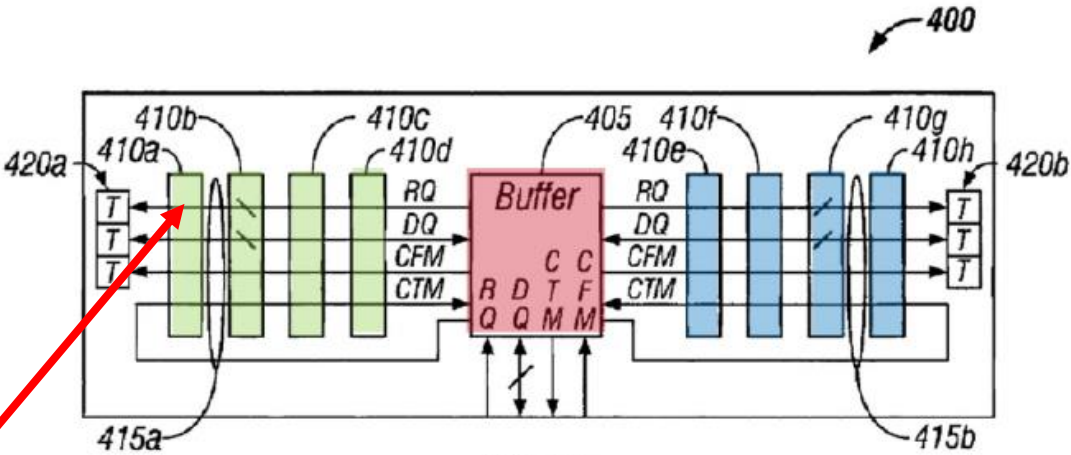


FIG. 4A

EX1071 (Perego) at Fig.4A

JEDEC DDR2 SDRAM SPECIFICATION		
CS	Input	Chip Select: All commands are masked when CS is registered HIGH. CS provides for external Rank selection on systems with multiple Ranks. CS is considered part of the command code.

EX1064 (JESD79-2) at 6

Rambus also uses "chip select" information

Synchronous DRAM Architectures, Organizations, and Alternative Technologies

Prof. Bruce L. Jacob

application: in the Rambus bus organization, all addresses, commands, data, and chip-select information are sent on the same bus lines. This is why the organization is called "multiplexed." At different points in time, the same physical lines carry dissimilar classes of information.

EX1069 at 1, 11

Q. Do you consider Professor Bruce

Jacob to be an expert in the field of the '417 and '215 patents, the author of the textbook marked as Exhibit 1070?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: Yes. He's certainly quite knowledgeable in this field.

EX1095 at 163:15-:22



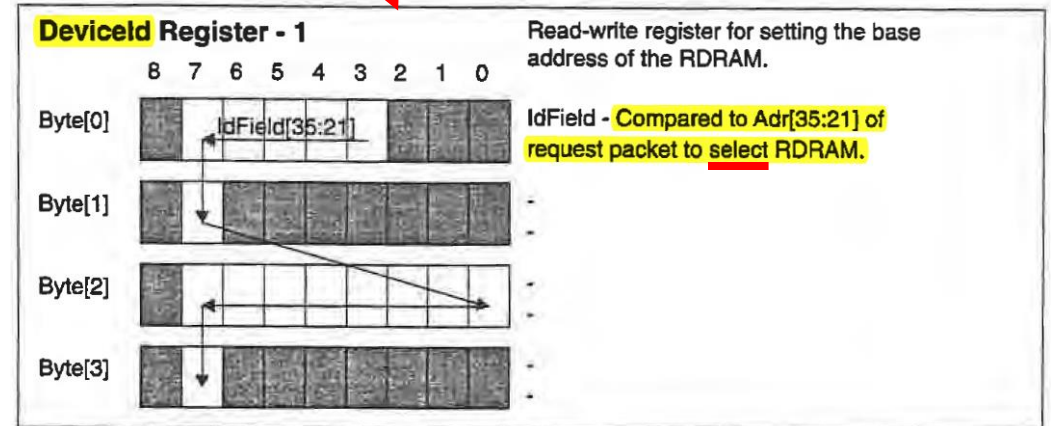
Q. And in that embodiment, the buffer of Perego would not receive chip select signals, for example, from the memory controller; correct?

MR. CHANDLER: Object to form.

THE WITNESS: I disagree. The Rambus protocol, for example, does include chip select signals. They are simply multiplexed

on to the same wires as other signals, in a packetized form.

EX2033 at 148:8-:16; see also id. at 149:24-150:17



EX1097 at 821-22; see also EX1095 at 191:19-193:24

Netlist mischaracterizes Dr. Wolfe's testimony from a different IPR regarding "ranks" in Perego

construction. EX2024, ¶ 165. Indeed, Petitioner's own expert, Dr. Wolfe, testified to the opposite conclusion while testifying in IPR2022-00615 regarding a related Netlist patent. EX2003, 202:8-204:10 ("I do not think that this paragraph [Perego 15:37-45] specifies how ranks are selected or enabled," and "independent banks" refers to "the number of page registers which can be activated corresponding to different addresses" "throughout the system"). Furthermore, this paragraph of

'417: Paper 22 (POR) at 35
'215: Paper 22 (POR) at 34-35

Q. I did a search for the word "rank" in Perego and I came up empty handed. Do you recall --

A. I think that's right. I think we already talked about this. I believe Perego does not use the specific word even though he clearly discloses the concept.

EX2003 at 204:12-21; see also *id.* at 79:17-82:3, 82:14-84:13

ondary channel signal lines for each transaction. According to a preferred embodiment, the target subset of secondary channel signal lines may be selected via address bits provided as part of the primary channel request. By accessing a subset of secondary channel signal lines per transaction, a number of benefits may be derived. One of these benefits is reduced power consumption. Another benefit is higher performance by grouping memory devices into multiple independent target subsets (i.e. more independent banks).

EX1071 (Perego) at 15:37-45

Q. Is Perego referencing a rank, in your view, when it says "independent banks"?

A. I think broadly he is -- is talking about the same general concept.

Q. So my follow-up question is, when performing rank multiplication with Perego, would that be performed only with address bits and with nothing else?

THE WITNESS: No. You still need to send the proper commands, and you still need to select the proper chips with the proper chip select values.

EX2033 at 71:5-73:7, 176:6-178:6 (objection omitted);
see also *id.* at 160:16-161:14

EX1069 (Jacob Paper) at 2-3



2.2.12 No Operation Command

2.2.13 Deselect Command

EX1064 (JESD79-2) at 48-49

Function	~~CSE~~	~~CS~~	~~RAS~~	~~CAS~~	~~WE~~	~~BA0 BA1 BA2~~	A15-A11	A10	A9 - A0	Notes	
	Previous Cycle	Current Cycle									
Write	H	H	L	H	L	L	BA	Column	L	Column	1,2,3
Device Deselect	H	X	H	X	X	X	X	X	X	X	1

EX1095 at 203:9-204:6 (objection omitted)

PEREGO AND JESD79-2 DISCLOSE REGISTERING DATA FOR AN ADDITIONAL CLOCK CYCLE

'417/'215: Buffer circuit (40) requires one extra clock cycle for address/control and data

In certain embodiments, the circuit 40 comprises the SPD device 240 which reports the CAS latency (CL) to the memory controller of the computer system. The SPD device 240 of certain embodiments reports a CL which has one more cycle than does the actual operational CL of the memory array. In certain embodiments, data transfers between the memory controller and the memory module are registered for one additional clock cycle by the circuit 40. The additional clock cycle of certain embodiments is added to the transfer time budget with an incremental overall CAS latency. This extra cycle of time in certain embodiments advantageously provides sufficient time budget to add a buffer which electrically isolates the ranks of memory devices 30 from the memory controller 20. The buffer of certain embodiments comprises combinatorial logic, registers, and logic pipelines. In certain embodiments, the buffer adds a one-clock cycle time delay, which is equivalent to a registered DIMM, to accomplish the address decoding. The one-cycle time delay of certain such embodiments provides sufficient time for read and write data transfers to provide the functions of the data path multiplexer/demultiplexer. Thus, for example, a DDR2 400-MHz memory system in accordance with embodiments described herein has an overall CAS latency of four, and uses memory devices with a CAS latency of three. In still other embodiments, the SPD device

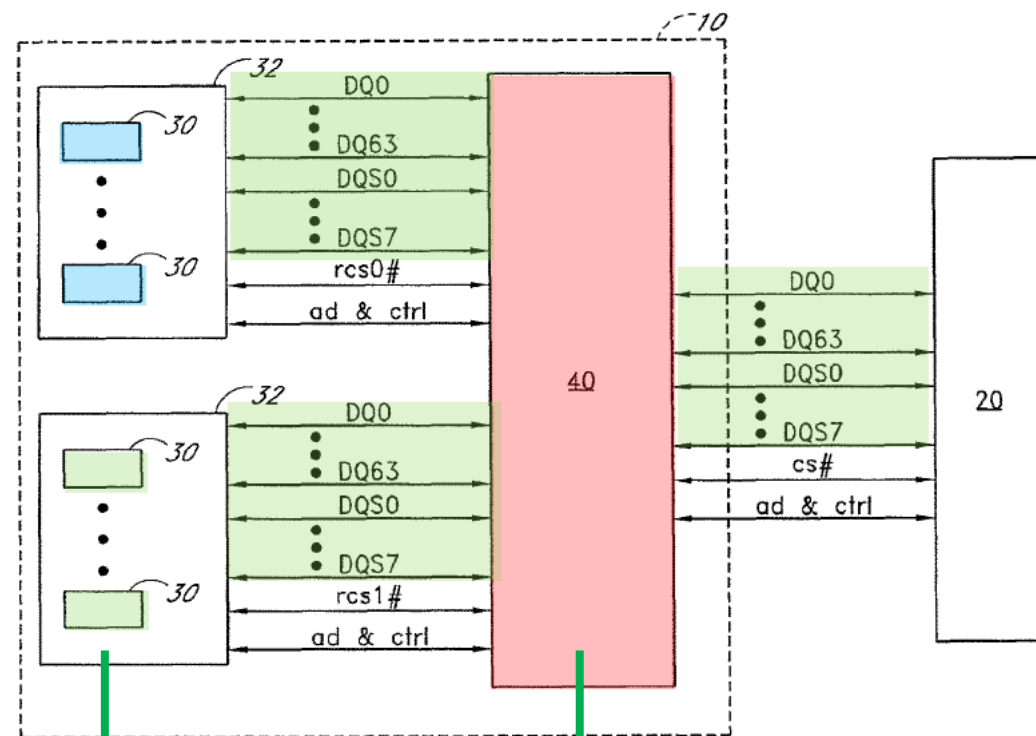


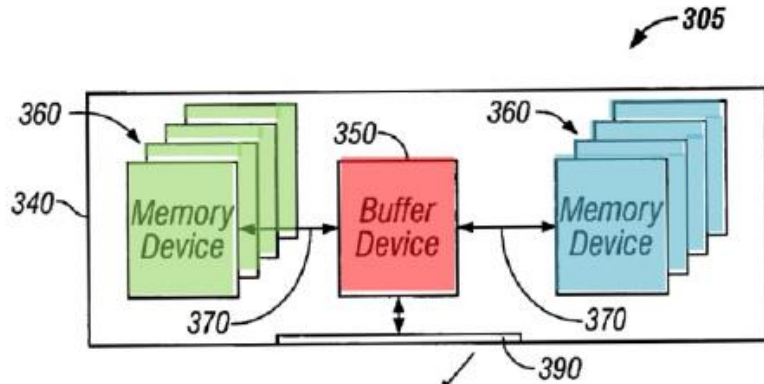
FIG. 1

3 clock cycles + 1 clock cycle = 4 clock cycles

'417: EX1001 at 22:36:-60
'215: EX1001 at 20:22:-46

'417: Paper 1 (Pet.) at 12-15
'215: Paper 1 (Pet.) at 12-14

Perego teaches using a data buffer to provide electrical “isolation” for high performance



With further reference to FIGS. 3A and 3B, buffer device 350 transceives and provides isolation between signals interfacing to controller 310 and signals interfacing to the plurality of memory devices 360. In a normal memory read

EX1071 (Perego) at 6:12-:15 & Fig.3B

Q. What impact does a higher electrical load have on data signals that are being transmitted to and from a memory controller?

THE WITNESS: Again, that's a question that requires a substantial amount of electronics and math to answer properly. Just say that higher loads are more challenging and have negative impacts.

Q. And what impact does a buffer on the data lines have with respect to loads on the data signals?

THE WITNESS: Again, within the context of 2004-2005 and the knowledge and experience of a POSITA, the general idea that reducing or otherwise managing loads to minimize their impact on data communications is a good thing.

EX1095 at 130:6-:16, 130:23-131:8 (objections omitted);
see also *id.* at 124:23-126:21, 136:8-137:11



Netlist's expert admitted it was known that buffering the data lines causes latency, similar to buffering other signal lines

Q. For example, is it possible that if you put a buffer on a data line, that the buffer could add a latency of one clock cycle?

....

THE WITNESS: We're specifically talking about data lines at this point?

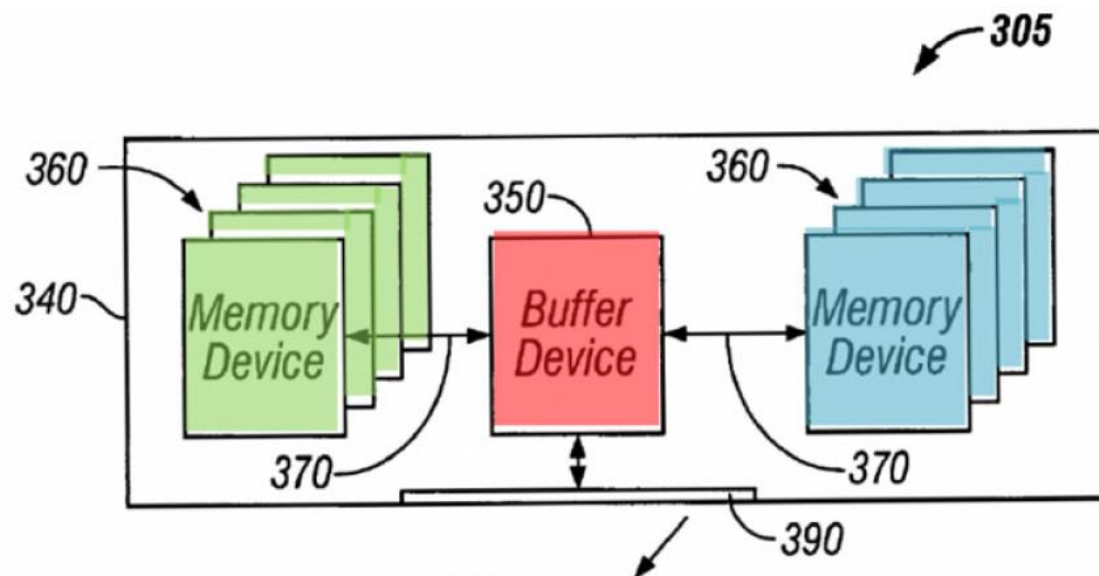
BY ATTORNEY CHANDLER:

Q. Yes.

A. Okay. So in the context of 2004-2005 and the knowledge of a POSITA, I think a POSITA would understand that a -- a buffer generally could add a small amount or a larger amount of latency, and depending on what's inside of it.

So -- and that would apply to data as well as anything else that the POSITA is dealing with.

EX1095 at 133:8-134:7



EX1071 (Perego) Fig. 3B

Netlist's expert admitted there was a motivation to put a buffer on the data path even though it adds a delay of one clock cycle

Q. As a layperson, to me it's a little bit counterintuitive as to why you would want to put a data buffer on a memory module if that data buffer is going to delay the signal by one clock cycle. And yet if I understand your earlier testimony, there's situations in which the data buffer can improve performance.

So how would you explain to me why adding a data buffer, which delays the data signal by one clock cycle, actually improves the performance of the memory module?

EX1095 at 136:8-18

THE WITNESS: Well, let's say you have two cars, a Ferrari and a Volkswagen Beetle.

The Ferrari takes ten minutes to warm up before you get to drive it; but once you're driving, you're going faster. So depending on how far you're going, either the Volkswagen Beetle or the Ferrari will get there faster.

It's the same sort of trade-offs that exist in the digital world, where the trade-off between operating frequency and latency is very poignant, and different solutions make sense in different domains for different types of memory systems, for different types of modules and different system types.



EX1095 at 136:21-137:11

The Institution Decision correctly found a motivation for Perego's data buffer to add a delay of one clock cycle, increasing the overall CAS latency of the memory module by one clock cycle



Patent Owner also argues that “Petitioner has also not provided competent evidence” to show that “the overall CAS latency of the memory module is greater than an actual operational CAS latency of each of the memory devices,” as recited in claim 1. Prelim. Resp. 44. **We disagree.**

Petitioner presents detailed testimony from Dr. Wolfe explaining how Perego's registered data transfers would have introduced delay. In particular, Dr. Wolfe, citing Perego's disclosures of data latches and an internal clock to generate synchronizing clock signals (Ex. 1071, 12:65–13:5, 17:61–63, Fig. C), provides the following testimony:

A Skilled Artisan would have understood from these disclosures that Perego's latching of the data signals and the use of internal synchronizing clock signals adds a predetermined amount of time delay for each data transfer through the buffer because the output of the latch needs to be in synchronization with an internal clock. A Skilled Artisan would have understood that such **registering of the data signals would require the addition of a fixed time delay, such as one clock cycle,** for each registered data transfer through the circuitry with respect to the actual operational CAS latency of each of the plurality of memory integrated circuits.

Ex. 1003 ¶ 360. Dr. Wolfe further explains how Perego's “latching delays in the buffer device of Perego increase the overall CAS latency of the memory module compared to the CAS latency of the memory devices.”

Ex. 1003 ¶ 362 (citing Ex. 1071, 12:65–13:5, 18:65–19:3, Figs. 5B, 5C). On this record, **we find Petitioner's evidence sufficiently persuasive to show that Perego teaches that “data transfers through the circuitry are registered for an amount of time delay such that the overall CAS latency of the memory module is greater than an actual operational CAS latency of each of the memory devices,” as recited in claim 1.**

'417: Paper 11 (ID) at 33-34

According to an embodiment of the present invention, **clock circuit 570a-b** includes one or more clock alignment circuits for phase or **delay adjusting internal clock signals** with respect to an external clock (not shown). Clock alignment circuit may utilize an external clock from an existing clock generator, or an internal clock generator to provide an internal clock, to generate internal synchronizing clock signals having a predetermined temporal relationship.

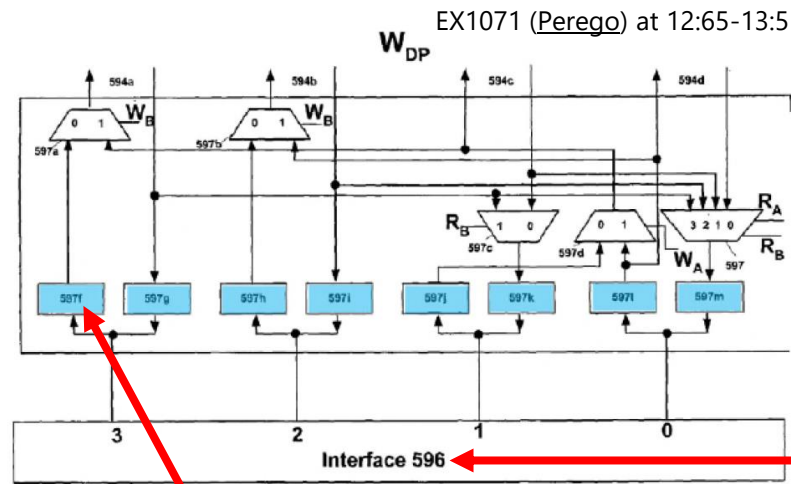


Fig. 5C

Multiplexer/demultiplexer **circuit 597** includes input and output latches **597f-m**, two for each configurable width buffer device data connection in interface **596**. Multiplexer/

EX1071 (Perego) at 17:61-:63

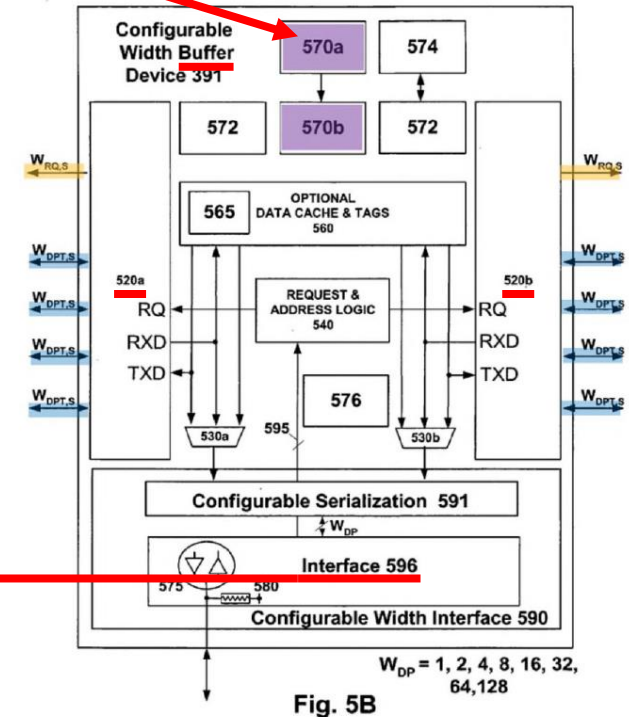


Fig. 5B

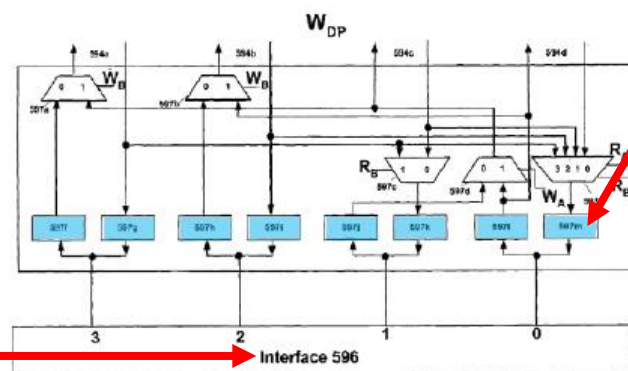
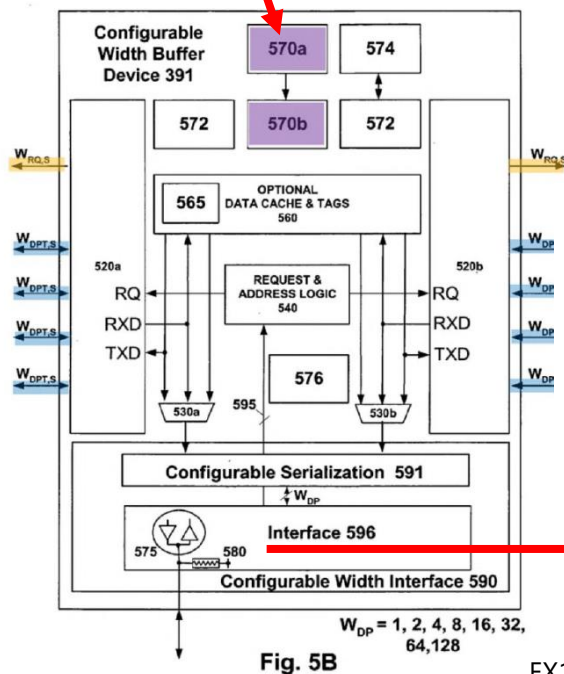
In embodiments of the present invention, **interfaces 520a and 520b** include multiplexer/demultiplexer circuit **597**, also known as a type of partial crossbar circuit, for transferring signals between configurable width buffer device **391** and memory devices on configurable width buffered module **395**. In an alternate embodiment of the present invention, a full crossbar circuit is used.

EX1071 (Perego) at 18:65-19:3

Netlist admits that clock signals from clock circuit 570a-b (purple) synchronize data capture, which Dr. Wolfe explains is done by Perego's latches (blue), causing delays

EX2024, ¶ 186. Finally, Petitioner cites EX1071, 12:65-13:5, which relates to “clock circuit 570a-b” and “adjusting internal clock signals with respect to an external clock.” As explained by Dr. Przybylski, this disclosure is not relevant to whether or not delay is added to the data path through the buffer circuit, but rather to controlling phase alignment between clock signals to ensure incoming data capture. EX2024, ¶

'417: Paper 22 (POR) at 39
'215: Paper 22 (POR) at 37



EX1071 (Perego) Figs. 5B & 5C

width buffer device data connection in interface 596.”). Perego's buffer circuit includes “clock circuit 570a-b ... to generate internal synchronizing clock signals having a predetermined temporal relationship.” *Id.* at 12:65-13:5. A Skilled Artisan would have understood from these disclosures that Perego's latching of the data signals and the use of internal synchronizing clock signals adds a predetermined amount of time delay for each data transfer through the buffer because the output of the latch needs to be in synchronization with an internal clock. A Skilled Artisan would have understood that such registering of the data signals would require the addition of a fixed time delay, such as one clock cycle, for each registered data transfer through the circuitry with respect to the actual operational CAS latency of each of the plurality of memory integrated circuits.



'417: EX1003, ¶1360
'215: EX1003, ¶1335

JESD79-2 teaches programmable CAS latency with integer values (e.g., 3 or 4 clock cycles) for the amount of time needed to perform a read or write

3.2.1 Programmable CAS Latency

JEDEC's *programmable CAS latency* is used to allow each system vendor to optimize the performance of its systems. It is programmed at system initialization and, according to industry designers, it is never set again while the machine is running [Lee 2002, Baker 2002,

EX1069 (Jacob paper) at 15; see also EX1095 at 250:4-:10, 252:2-:7

4.1 Programmable CAS Latency

The primary benefit of programmable CAS latency is flexibility: its presence in a DRAM allows a fast part to emulate the behavior of a slow part, which would enable an OEM or end consumer to intermingle parts from different generations (with different speeds) in the same system or intermingle same-generation parts from different manufacturers (which might have slightly different performance capabilities due to slight variations in process technologies) in the same DIMM [Lee 2002, Baker 2002, Kellogg 2002, Macri 2002, Ryan 2002, Rhoden 2002, Sussman 2002]. To illustrate, if a DRAM manufacturer has a part with a minimum 20ns CAS readout, the part could conceivably work as a CAS-2, 100MHz part (20ns requires 2 cycles at 100MHz), a CAS-3, 150MHz part (20ns requires 3 cycles at 150MHz), or a CAS-4, 200MHz part (20ns requires 4 cycles at 200MHz). Note that the part would never be able to make CAS-2 latencies at the higher bus speeds or CAS-3 at the highest bus speed (CAS-2 requires 13.33ns at 150MHz and 10ns at 200MHz; CAS-3 requires 15ns at 200MHz).

EX1069 (Jacob paper) at 16

JEDEC DDR2 SDRAM SPECIFICATION

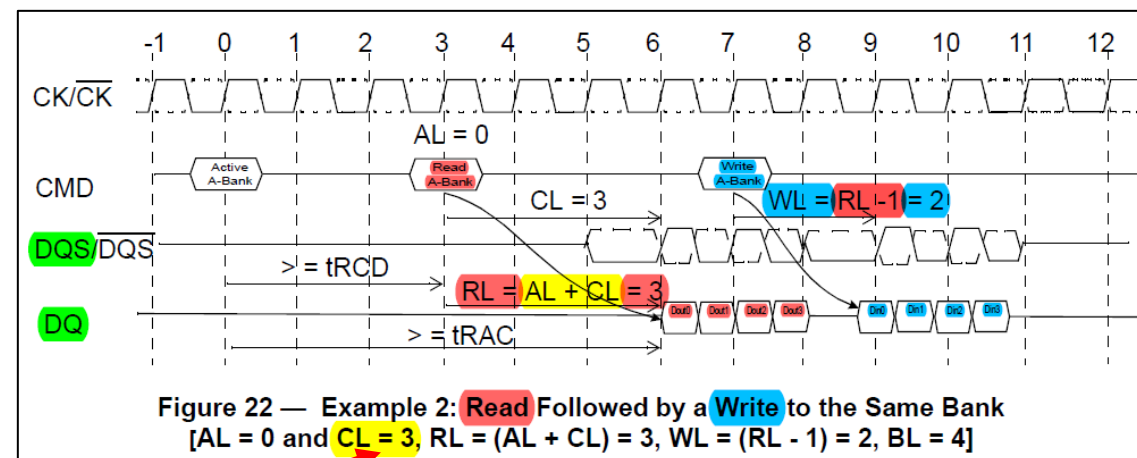
CAS Latency

A6	A5	A4	Latency
0	0	0	Reserved
0	0	1	Reserved
0	1	0	2(Optional)
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	Reserved
1	1	1	Reserved

A5	A4	A3	Additive Latency
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

SDRAM. Burst address sequence type is defined by A3, CAS latency is defined by A4 ~ A6. The DDR2 doesn't support half clock latency mode. A7 is used for test mode. A8 is used for DLL reset. A7 must be set

EMRS(1). The Write Latency (WL) is always defined as $RL - 1$ (read latency - 1) where read latency is defined as the sum of additive latency plus CAS latency ($RL = AL + CL$). Read or Write operations using AL



EX1064 (JESD79-2) at 12, 14, 24-25; see also EX2031 at 16 (Byte 18)

JEDEC taught delaying data by one additional clock cycle, and Netlist's expert admitted such delay was common for a data buffer

DDR SDRAM Registered DIMM

In a registered DIMM, data is delayed an additional clock cycle due to the on-DIMM pipeline register (that is, Device CL [clock cycles] + 1 = DIMM CAS latency).

EX1062 at 68

DDR2 SDRAM RDIMM

CL = CAS (READ) latency; registered mode will add one clock cycle to CL.

EX1109 at 1

Q. If you include a buffer on the data line of a memory module, would that buffer normally add a latency to the data signal as it passes through the buffer?

THE WITNESS: Inevitably, there's some delay, depending on the type of buffer and its characteristics internally. It can be very small or it can be substantial. It all depends, again, on the unique characteristics of the circumstance we're talking about.

EX1095 at 132:20-133:6 (objection omitted)

Q. Was it common for a register for a buffer to delay a signal by one clock cycle?

THE WITNESS: There are many examples of a register or buffer that includes a cycle of delay. There are many examples that include many cycles of delay; and there are examples that have fractions of a cycle of delay.

EX1095 at 135:2-:14 (objection omitted)

"Where a prior art patent discloses a **range of values**, showing a claimed value falls within that range meets a party's burden of establishing the narrower claim would have been obvious where there is no reason to think the result would be unpredictable."

Gen. Hosp. Corp. v. Sienna Biopharms., Inc.,
888 F.3d 1368, 1373 (Fed. Cir. 2018)



Perego combined with JESD79-2 teaches registering data for one additional clock cycle, consistent with standard integer latencies



width buffer device data connection in interface 596.”). Perego’s buffer circuit includes “clock circuit 570a-b ... to generate internal synchronizing clock signals having a predetermined temporal relationship.” *Id.* at 12:65-13:5. A Skilled Artisan would have understood from these disclosures that Perego’s latching of the data signals and the use of internal synchronizing clock signals adds a predetermined amount of time delay for each data transfer through the buffer because the output of the latch needs to be in synchronization with an internal clock. A Skilled Artisan would have understood that such registering of the data signals would require the addition of a fixed time delay, such as one clock cycle, for each registered data transfer through the circuitry with respect to the actual operational CAS latency of each of the plurality of memory integrated circuits.

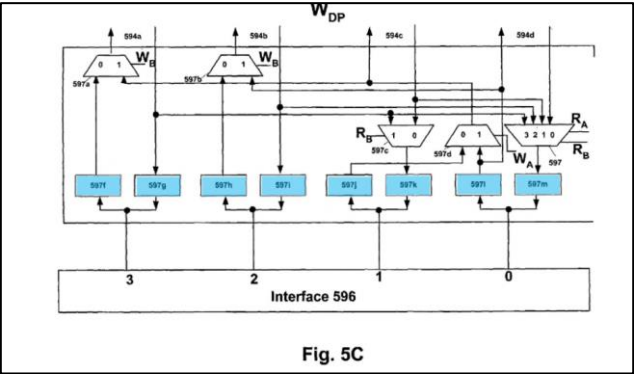


Fig. 5C

EX1071 (Perego) FIG. 5C

’417: EX1003, ¶1360
’215: EX1003, ¶1335

Perego discloses providing “access latency values” to the memory controller during initialization, EX1071, 12:20-34, Fig.5B, and a POSITA would have known from the JEDEC standards (including JESD79-2, shown below) that the data transfers in Perego’s memory module are enabled in accordance with these “access latency values,” including CAS latency (expressed in terms of an integer number of clock cycles), which are programmed during initialization by the memory controller and used to properly time burst operations to comply with the JEDEC standards, *see* EX1064, pp.12 (first below, showing “CAS Latency” of 2, 3, 4, or 5

’417: Pet. at 92-94
’215: Pet. at 84-86

JEDEC DDR2 SDRAM SPECIFICATION

CAS Latency

A6	A5	A4	Latency
0	0	0	Reserved
0	0	1	Reserved
0	1	0	2(Optional)
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	Reserved
1	1	1	Reserved

A5	A4	A3	Additive Latency
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

SDRAM. Burst address sequence type is defined by A3, CAS latency is defined by A4 ~ A6. The DDR2 doesn’t support half clock latency mode. A7 is used for test mode. A8 is used for DLL reset. A7 must be set

EX1064 (JESD79-2) at 12, 14

Netlist mischaracterizes the Petition, which used Additive Latency (which can be 0 clock cycles) to show that DDR2 systems measure latency in integer values

Second, Petitioner cites pages of EX1064 (JESD79-2) that relate to Additive Latency (AL). But there is a reason this concept is found in the DDR2 SDRAM standard. AL relates to the latency of the SDRAMs—i.e., a portion of the “actual operational CAS latency of each of the memory devices” and not any additional latency at the module level. EX2024; EX1064, 14 (Additive Latency programmed

'417: Paper 22 (POR) at 37
'215: Paper 22 (POR) at 36

JEDEC DDR2 SDRAM SPECIFICATION

cycle. If a R/W command is issued to a bank that has not satisfied the t_{RCDmin} specification, then additive latency must be programmed into the device to delay when the R/W command is internally issued to the device. The additive latency value must be chosen to assure t_{RCDmin} is satisfied. Additive latencies of 0, 1, 2, 3 and 4 are supported. Once a bank has been activated it must be precharged before another Bank

SDRAM Burst address sequence type is defined by A3, CAS latency is defined by A4 ~ A6. The DDR2 doesn't support half clock latency mode. A7 is used for test mode. A8 is used for DLL reset. A7 must be set

EMRS(1). The Write Latency (WL) is always defined as $RL - 1$ (read latency - 1) where read latency is defined as the sum of additive latency plus CAS latency ($RL = AL + CL$). Read or Write operations using AL

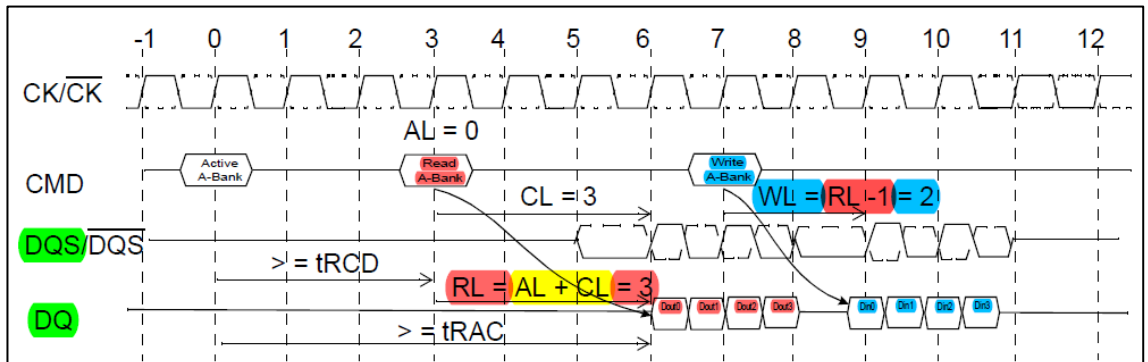


Figure 22 — Example 2: Read Followed by a Write to the Same Bank
[AL = 0 and CL = 3, RL = (AL + CL) = 3, WL = (RL - 1) = 2, BL = 4]

EX1064 (JESD79-2) at 23-25; see also EX2031 at 16 (Byte 18)

'215 PATENT, CLAIMS 4 AND 25

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

'215 Patent, Claims 4 and 25

5. Claims 4 and 25 (POR 38)

Netlist's arguments about claims 4 and 25 of the 215 Patent (requiring "one more clock cycle") are incorrect for the same reasons discussed directly above (pp.17-21).

'215: Paper 27 (Reply) at 21

'215 PATENT, CLAIMS 14–15 AND 26

'215 Patent, Claims 14–15 and 26

6. Claims 14-15 and 26 (POR 38-39)

Netlist's arguments about claims 14-15 and 26 of the 215 Patent are incorrect because they assume Perego is limited to a *single* rank, which is incorrect as discussed above (pp.15-17). Perego renders obvious a “fork in the road” with *multiple* ranks. Pet. 63-72, 107-10, 112.

'215: Paper 27 (Reply) at 21

GROUND 2 ('215 AND '417)

5

GROUND 2: GROUND 1 + ELLSBERRY

ELLSBERRY IS A “PRINTED PUBLICATION” UNDER § 311(B)

GROUND 2: GROUND 1 + ELLSBERRY

Ellsberry [EX1073] is a printed publication and prior art under §102(e) as of its filing date of June 1, 2005

(19) United States	
(12) Patent Application Publication	(10) Pub. No.: US 2006/0277355 A1
Ellsberry et al.	(43) Pub. Date: Dec. 7, 2006
(54) CAPACITY-EXPANDING MEMORY DEVICE	G06F 12/06 (2006.01)
(76) Inventors: Mark Ellsberry , Santa Clara, CA (US); Paul Sweere , Irvine, CA (US); Michael Sansur , Costa Mesa, CA (US); Grant Stockton , Fountain Valley, CA (US)	(52) U.S. Cl. 711/5; 711/154
Correspondence Address: LOZA & LOZA 6285 EAST SPRING STREET, # 327N LONG BEACH, CA 90808 (US)	(57) ABSTRACT The invention relates to a device, system, and method for expanding the memory capacity of a memory module. A control unit and memory bank switch are mounted on a memory module to selectively control write and/or read operations to/from memory devices communicatively coupled to the memory bank switch. By selectively routing data to and from the memory devices, a plurality of memory devices may appear as a single memory device to the operating system. That is, the invention expands the addressable memory banks on a module by making two smaller-capacity memory devices emulate a single higher-capacity memory device.
(21) Appl. No.: 11/142,989	
(22) Filed: Jun. 1, 2005	
Publication Classification	
(51) Int. Cl. G06F 13/00 (2006.01)	

EX1073

The Board has repeatedly held that patent applications are “printed publications” and entitled to their §102(e) filing date under 35 U.S.C. § 311(b)

Trials@uspto.gov
571-272-7822

Paper 96
Entered: April 17, 2024

UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD., MICRON TECHNOLOGY, INC.,
MICRON SEMICONDUCTOR PRODUCTS, INC., and MICRON
TECHNOLOGY TEXAS LLC,¹
Petitioner,

v.

NETLIST, INC.,
Patent Owner.

IPR2022-00615
Patent 7,619,912 C1

Before JON M. JURGOVAN, DANIEL J. GALLIGAN, and
KARA L. SZPONDOWSKI, *Administrative Patent Judges*.

JURGOVAN, *Administrative Patent Judge*.

JUDGMENT
Final Written Decision
Determining Challenged Claim Unpatentable
Dismissing Patent Owner's Motion to Submit Supplemental Information
Dismissing Petitioner's Motion to Exclude
35 U.S.C. § 318(a)

December 2006). Ellsberry is prior art at least under 35 U.S.C. § 102(e)(1), being “an application for patent, **published** under section 122(b), by another filed in the United States before the invention by the applicant for patent.” See Ex. 1037, code (22) (filing date of June 1, 2005). Thus, Petitioner asserts a permissible ground of unpatentability under 35 U.S.C. § 311(b)

EX1114 at 34-35; see also EX2023 at 7-10

Trials@uspto.gov
571-272-7822

Paper 33
Date: June 26, 2023

UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.,
Petitioner,

v.

LYNK LABS, INC.,
Patent Owner.

IPR2022-00149
Patent 10,687,400 B2

Before JON B. TORNQUIST, ARTHUR M. PESLAK, and
STEPHEN E. BELISLE, *Administrative Patent Judges*.

PESLAK, *Administrative Patent Judge*.

JUDGMENT
Final Written Decision
Determining All Challenged Claims Unpatentable
35 U.S.C. § 314(a)

Petitioner counters that “Martin qualifies as a ‘patent[] and **printed publication[]** under § 311(b) at least because it is ‘an application for patent, published under section 122(b), by another **filed** in the United States before the invention by the applicant for patent’ according to § 102(e)(1).” Pet.

We agree with Petitioner

EX1098 at 10-12; see also EX1099 at 27-29

Trials@uspto.gov
571-272-7822

Paper 11
Date: August 1, 2023

UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.,
Petitioner,

v.

NETLIST, INC.,
Patent Owner.

IPR2023-00455
Patent 9,858,215 B1

Before PATRICK M. BOUCHER, JON M. JURGOVAN, and
DANIEL J. GALLIGAN, *Administrative Patent Judges*.

GALLIGAN, *Administrative Patent Judge*.

DECISION
Granting Institution of *Inter Partes* Review
35 U.S.C. § 314

record, we are persuaded by Petitioner’s contentions that Ellsberry is prior art under 35 U.S.C. § 102(e), having been filed “by another . . . in the United States before the invention by the applicant for patent.” See Pet. 5–8

‘215: Paper 11 (ID) at 29
‘417: Paper 11 (ID) at 38-39

The language of 35 U.S.C. § 311(b) mirrors the language in pre-AIA § 301, which was understood to include published patent applications under §102(e)

§ 311. Inter partes review

(a) IN GENERAL.—Subject to the provisions of this chapter, a person who is not the owner of a patent may file with the Office a petition to institute an inter partes review of the patent. The Director shall establish, by regulation, fees to be paid by the person requesting the review, in such amounts as the Director determines to be reasonable, considering the aggregate costs of the review.

(b) SCOPE.—A petitioner in an inter partes review may request to cancel as unpatentable 1 or more claims of a patent only on a ground that could be raised under section 102 or 103 and only on the basis of prior art consisting of patents or printed publications.



"[W]hen Congress enacted the 'prior art consisting of patents or printed publications' provision for IPRs in section 311(b) [in 2011], it is presumed to have done so with reference to the same specialized provision in the reexamination statute [§301]."

Qualcomm Inc. v. Apple Inc.,
24 F.4th 1367, 1375 (Fed. Cir. 2022) (cleaned up)

§ 301. Citation of prior art

Any person at any time may cite to the Office in writing prior art consisting of patents or printed publications which that person believes to have a bearing on the patentability of any claim of a particular patent. If the person explains in writing the pertinency and manner of applying such prior art to at least one claim of the patent, the citation of such prior art and the explanation thereof will become a part of the official file of the patent. At the written request of the person citing the prior art, his or her identity will be excluded from the patent file and kept confidential.

(Added Pub. L. 96-517, §1, Dec. 12, 1980, 94 Stat. 3015.)

§ 302. Request for reexamination

Any person at any time may file a request for reexamination by the Office of any claim of a patent on the basis of any prior art cited under the provisions of section 301 of this title. The request must be in writing and must be accompanied by payment of a reexamination fee established by the Director pursuant to the provisions of section 41 of this title. The request must set forth the pertinency and manner of applying cited prior art to every claim for which reexamination is requested. Unless the requesting person is the owner of the patent, the Director promptly will send a copy of the request to the owner of record of the patent.

MPEP (8th ed. 2001)

2217 Statement in the Request Applying Prior Art

The third sentence of 35 U.S.C. 302 indicates that the "request must set forth the pertinency and manner of applying cited prior art to every claim for which reexamination is requested." 37 CFR 1.510(b)(2) requires that the request include "[a]n identification of every claim for which reexamination is requested, and a detailed explanation of the pertinency and manner of applying the cited prior art to every claim for which reexamination is requested." If the request is filed by the patent owner, the request for reexamination may also point out how claims distinguish over cited prior art.

The prior art applied may only consist of prior art patents or printed publications. Substantial new questions of patentability may be based upon the following portions of 35 U.S.C. 102:

"(a)...patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for patent, or"

"(b) the invention was patented or described in a printed publication in this or a foreign country... more than one year prior to the date of the application for patent in the United States, or"

"(e) the invention was described in—

(1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or

ELLSBERRY IS PRIOR ART BECAUSE EX1005 DOES NOT
PROVIDE §112 SUPPORT FOR THE '417/'215 CLAIMS

GROUND 2: GROUND 1 + ELLSBERRY

Netlist had the burden of production to show that Ellsberry (filed June 1, 2005) is not prior art to the '417 and '215 Patents



"[W]e find that Petitioner carried its initial burden to show that Ellsberry is prior art. The burden of production thus shifts to Patent Owner to show that the subject matter of [the] claim[s]...is supported by its priority applications such that Ellsberry is not prior art."

EX1023 at 26 (citing *Dynamic Drinkware, LLC v. National Graphics, Inc.*, 800 F.3d 1375, 1379 (Fed. Cir. 2021))

'417 Patent



"Petitioner was not required to rebut in advance Patent Owner's argument and evidence alleging priority to the [earlier] application."

Continental Auto. Sys., Inc. v. Intellectual Ventures II LLC,
IPR2022-00972, Paper 49, at 28 (PTAB Dec. 5, 2023)

'215 Patent

(12) United States Patent Solomon et al.		(10) Patent No.: US 11,093,417 B2 (45) Date of Patent: Aug. 17, 2021
(54) MEMORY MODULE WITH DATA BUFFERING	continuation of application No. 11/335,875, filed on Jan. 19, 2006, now Pat. No. 7,532,537, which is a continuation-in-part of application No. 11/173,175, filed on Jul. 1, 2005, now Pat. No. 7,289,386, which is a continuation-in-part of application No. 11/075,395, filed on Mar. 7, 2005, now Pat. No. 7,286,436.	
(71) Applicant: Netlist, Inc. , Irvine, CA (US)		
(72) Inventors: Jefferey C. Solomon , Irvine, CA (US); Jayesh R. Bhakta , Cerritos, CA (US)		
(73) Assignee: Netlist, Inc. , Irvine, CA (US)	Provisional application No. 60/645,087, filed on Jan. 19, 2005, provisional application No. 60/588,244, filed on Jul. 15, 2004, provisional application No. 60/550,668, filed on Mar. 5, 2004, provisional application No. 60/575,595, filed on May 28, 2004, provisional application No. 60/590,038, filed on Jul. 21, 2004.	

(12) United States Patent Solomon et al.		(10) Patent No.: US 9,858,215 B1 (45) Date of Patent: Jan. 2, 2018
(54) MEMORY MODULE WITH DATA BUFFERING	continuation of application No. 11/335,875, filed on Jan. 19, 2006, now Pat. No. 7,532,537, which is a continuation-in-part of application No. 11/173,175, filed on Jul. 1, 2005, now Pat. No. 7,289,386, which is a continuation-in-part of application No. 11/075,395, filed on Mar. 7, 2005, now Pat. No. 7,286,436.	
(71) Applicant: Netlist, Inc. , Irvine, CA (US)		
(72) Inventors: Jeffrey C. Solomon , Irvine, CA (US); Jayesh R. Bhakta , Cerritos, CA (US)		
(73) Assignee: Netlist, Inc. , Irvine, CA (US)	Provisional application No. 60/645,087, filed on Jan. 19, 2005, provisional application No. 60/588,244, filed on Jul. 15, 2004, provisional application No. 60/550,668, filed on Mar. 5, 2004, provisional application No. 60/575,595, filed on May 28, 2004, provisional application No. 60/590,038, filed on Jul. 21, 2004.	

Netlist's chart (below) mixes and matches provisionals, which is insufficient to show § 112 support for the claims in the '417 and '215 Patents

Claim/Element	Exemplary Citations of Support
1.a.1	EX1005, Fig. 1, [0001]-[0004], [0007]-[0008], [0010]-[0011], [0014]-[0015], [0016]
1.a.2	EX1005, Fig. 1, [0001], [0004]-[0005], [0007], [0009]-[0018], [0021]; EX1006, [0019]; EX1007, [0015], 9-11, 14-16; EX1008, [0015], 16-18, 21-23; EX1009, [0006]; EX1011, 4:65-66; 5:31-34, 8:58-62
1.a.3	[1.a.2] EX1005, Fig. 1, [0017]; EX1007, [0015], 9-12 14-17; EX1008, [0015], 16-19, 21-24
1.a.4	[1.a.1]
1.b	EX1005, Fig. 1, [0001], [0003]; EX1006, [0001], [0023], [0025]-[0026]; EX1007, [0006], 9, 20, 22-23, 25-38; EX1008, [0001], [0007], [0019], APPX 1, [0006], 16, 27-44; EX1011, 1:22-25, 3:56-60, 7:50-54, 11:22-30, Fig. 5A-5B
1.c	[1.a.2], [1.a.3], [1.b] EX1005, Fig. 1, [0004]-[0011], [0014], [0016]-[0017]; EX1007, 10; EX1008, 17; EX1006, [0009]-[0010], Fig. 1
1.d.1	[1.b] EX1005, [0004]-[0010], [0015]; EX1007, 9, 11, 20, 22-23, 25-38; EX1008, 16, 18, 27-44

'417: Paper 22 (POR) at 46-49
'215: Paper 22 (POR) at 46-50

"[A] description that merely renders the invention obvious does not satisfy the [written description] requirement[.]"

Ariad Pharms., Inc. v. Eli Lilly & Co., 598 F.3d 1336, 1352 (Fed. Cir. 2010) (en banc);
see also *Rivera v. ITC*, 857 F.3d 1315, 1322 (Fed. Cir. 2017).



"A **provisional application shall not be entitled to the right of priority of any other application** under section 119 or 365(a) of this title **or to the benefit of an earlier filing date** in the United States under section 120, 121, or 365(c) of this title."

35 U.S.C. § 111(b)(7) (pre-AIA)



"An application for patent for an invention disclosed in the manner provided by the first paragraph of section 112 of this title in an application previously filed in the United States . . . which is **filed by an inventor or inventors named in the previously filed application** shall have the same effect, as to such invention, as though filed on the date of the prior application, **if . . . it contains** or is amended to contain **a specific reference to the earlier filed application. . . .**"

35 U.S.C. § 120 (pre-AIA)



"37 C.F.R. § 42.24(a) sets word limits for petitions, motions, and replies, and § 42.6(a)(3) **prohibits incorporating arguments by reference** from one document into another."



Trial Practice Guide at 35

'417: Paper 27 (Reply) at 22-23
'215: Paper 27 (Reply) at 22-23

Netlist's chart (below) mixes and matches provisionals, which is insufficient to show \$112 support for the claims in the '417 and '215 Patents (naming Solomon and Bhakta)

Claim/Element	Exemplary Citations of Support
1.a.1	EX1005, Fig. 1, [0001]-[0004], [0007]-[0008], [0010]-[0011], [0014]-[0015], [0016]
1.a.2	EX1005, Fig. 1, [0001], [0004]-[0005], [0007], [0009]-[0018], [0021]; EX1006, [0019]; EX1007, [0015], 9-11, 14-16; EX1008, [0015], 16-18, 21-23; EX1009, [0006]; EX1011, 4:65-66; 5:31-34, 8:58-62
1.a.3	[1.a.2] EX1005, Fig. 1, [0017]; EX1007, [0015], 9-12 14-17; EX1008, [0015], 16-19, 21-24
1.a.4	[1.a.1]
1.b	EX1005, Fig. 1, [0001], [0003]; EX1006, [0001], [0023], [0025]-[0026]; EX 1007, [0006], 9, 20, 22-23, 25-38; EX1008, [0001], [0007], [0019], APPX 1, [0006], 16, 27-44; EX1011, 1:22-25, 3:56-60, 7:50-54, 11:22-30, Fig. 5A-5B
1.c	[1.a.2], [1.a.3], [1.b] EX1005, Fig. 1, [0004]-[0011], [0014], [0016]-[0017]; EX1007, 10; EX1008, 17; EX1006, [0009]-[0010], Fig. 1
1.d.1	[1.b] EX1005, [0004]-[0010], [0015]; EX1007, 9, 11, 20, 22-23, 25-38; EX1008, 16, 18, 27-44

'417: Paper 22 (POR) at 46-49
'215: Paper 22 (POR) at 46-50

(12) United States Patent Bhakta et al. (54) HIGH-DENSITY MEMORY MODULE UTILIZING LOW-DENSITY MEMORY COMPONENTS (75) Inventors: Jayesh R. Bhakta, Cerritos, CA (US); Jeffrey Solomon, Irvine, CA (US); William M. Gervasi, Ladera Ranch, CA (US)	(10) Patent No.: US 7,286,436 B2 (45) Date of Patent: Oct. 23, 2007 (21) Appl. No.: 11/075,395 (22) Filed: Mar. 7, 2005 (65) Prior Publication Data US 2005/0281096 A1 Dec. 22, 2005 Related U.S. Application Data (60) Provisional application No. 60/590,038, filed on Jul. 21, 2004, provisional application No. 60/575,595, filed on May 28, 2004, provisional application No. 60/550,668, filed on Mar. 5, 2004.
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EX1011

This is a request for filing a **PROVISIONAL** APPLICATION FOR PATENT under 37 CFR § 1.53(c).

For: **MEMORY MODULE WITH TIED DQS PINS**

Name of **First Inventor:** **William M. Gervasi**
Residence Address: 147 Belridge Drive, Los Gatos, California 91789

Name of **Second Inventor:** **Jeffrey Solomon**
Residence Address: 16 Silver Fir, Irvine, California 92604

Name of **Third Inventor:** **Jayesh R. Bhakta**
Residence Address: 12220 Rose Street, Cerritos, California 90703 ..

EX1009 (provisional July 21, 2004)

ATTENTION: **PROVISIONAL** PATENT APPLICATION

Sir:

This is a request for filing a PROVISIONAL APPLICATION FOR PATENT under 37 CFR § 1.53(c).

For: **UNBUFFERED MEMORY MODULE USING SHARED DQS PINS**

Inventors: Not yet named

EX1007 (provisional Mar. 5, 2004)

This is a request for filing a **PROVISIONAL** APPLICATION FOR PATENT under 37 CFR § 1.53(c).

For: **METHOD OF FORMING A MEMORY MODULE HAVING x8 ORGANIZATION USING DRAM DEVICES HAVING x4 ORGANIZATION**

Name of **First Inventor:** **William M. Gervasi**
Residence Address: 147 Belridge Drive, Los Gatos, California 95032

Name of **Second Inventor:** **Jeff Solomon**
Residence Address: 16 Silver Fir, Irvine, California 92604

EX1008 (provisional May 28, 2004)

This is a request for filing a **PROVISIONAL** APPLICATION FOR PATENT under 37 CFR § 1.53(c).

For: **MEMORY MODULE DECODER FOR SIMULATING A MEMORY MODULE HAVING FEWER RANKS**

Name of **First Inventor:** **Robert S. Pauley**
Residence Address: 26322 Eastview Court, San Juan Capistrano, California 92675
Citizenship: United States

Name of **Second Inventor:** **Jayesh R. Bhakta**
Residence Address: 12220 Rose Street, Cerritos, California 90703
Citizenship: United States

Name of **Third Inventor:** **William M. Gervasi**
Residence Address: 147 Belridge Drive, Los Gatos, California 95032
Citizenship: United States

Name of **Fourth Inventor:** **Chi She Chen**
Residence Address: 944 Crystal Water Lane, Walnut, California 91789
Citizenship: Taiwan

Name of **Fifth Inventor:** **Jeffrey C. Solomon**
Residence Address: 16 Silver Fir, Irvine, California 92604
Citizenship: United States

Name of **Sixth Inventor:** **Yu Hui Zhang**
Residence Address: 1518 S. Jellick Avenue, Rowland Heights, California 91748
Citizenship: United States

EX1006 (provisional July 15, 2004)

EX1005 (provisional Jan. 19, 2005)

Provisional Application COVER SHEET

Attorney Docket No.: **NETL030PR**
Inventor: **Jeffrey Solomon**
Title: **RANK BUFFERED DUAL INLINE MEMORY MODULE**
Express Mail Label No.: **EV 318992171 US**

Direct all correspondence to Customer No.: 20995 **Date: January 19, 2005**

Page 1 of 1

EX1010 (provisional Jan. 19, 2005)

EX1011 (provisional Jan. 19, 2005)

Netlist's sur-reply relies only on EX1005 (provisional filed Jan. 19, 2005) to try to show §112 support for the claims in the '417 and '215 Patents — without explanations for each limitation

Claim/Element	Exemplary Citations of Support
1.a.1	EX1005, Fig. 1, [0001]-[0004], [0007]-[0008], [0010]-[0011], [0014]-[0015], [0016]
1.a.2	EX1005, Fig. 1, [0001], [0004]-[0005], [0007], [0009]-[0018], [0021]
1.a.3	[1.a.2] EX1005, Fig. 1, [0017]
1.a.4	[1.a.1]
1.b	EX1005, Fig. 1, [0001], [0003]
1.c	[1.a.2], [1.a.3], [1.b] EX1005, Fig. 1, [0004]-[0011], [0014], [0016]-[0017]
1.d.1	[1.b] EX1005, [0004]-[0010], [0015]

'417: Paper 22 (POR) at 46-49
'215: Paper 22 (POR) at 46-50

"[A] description that merely renders the invention obvious does not satisfy the [written description] requirement[.]"

Ariad Pharms., Inc. v. Eli Lilly & Co., 598 F.3d 1336, 1352 (Fed. Cir. 2010) (en banc);
see also *Rivera v. ITC*, 857 F.3d 1315, 1322 (Fed. Cir. 2017).



"37 C.F.R. § 42.24(a) sets word limits for petitions, motions, and replies, and § 42.6(a)(3) **prohibits incorporating arguments by reference** from one document into another."

Trial Practice Guide at 35



"Petitioner was not required to rebut in advance Patent Owner's argument and evidence alleging priority to the [earlier] application."

Continental Auto. Sys., Inc. v. Intellectual Ventures II LLC,
IPR2022-00972, Paper 49, at 28 (PTAB Dec. 5, 2023)



The '087 provisional [EX1005] does not disclose the claimed "[data buffer] control signals"

'417 Patent

1. A memory module operable in a computer system to communicate data with a memory controller of the computer system via a N-bit wide memory bus in response to read or write memory commands received from the memory controller, the memory bus including address and control signal lines and data signal lines, the memory module comprising: a printed circuit board having a plurality of edge connections configured to be electrically coupled to a corresponding plurality of contacts of a module slot of the computer system;

logic coupled to the printed circuit board and configurable

...

active signal value, wherein the logic is further configurable to output data buffer control signals in response to the read or write memory command;

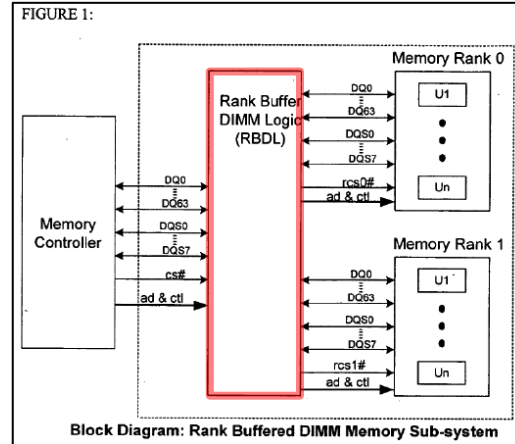
...

response to the read or write command; and

circuitry coupled between the data signal lines in the N-bit wide memory bus and corresponding data pins of memory devices in each of the plurality of N-bit wide ranks, the circuitry being configurable to transfer the burst of N-bit wide data signals between the N-bit wide memory bus and the memory devices in the one of the plurality of N-bit wide ranks in response to the data buffer control signals and in accordance with an overall CAS latency of the memory module;

...

'417: EX1001



[0007] Figure 1 schematically illustrates a block diagram of a dual inline memory module (DIMM) memory subsystem in accordance with embodiments described herein. The DIMM of Figure 1 comprises a logic translation element, labeled as "Rank Buffer DIMM Logic (RBDL)." In certain embodiments, the logic translation element is electrically connected to the memory controller of the computer system and is electrically connected to the ranks of memory devices (or chips) of the DIMM. In certain embodiments, the logic translation element comprises address decoding logic which transparently translates from a system memory density domain of the computer system to a physical memory density domain of the DIMM.

[0005] In certain embodiments, the memory devices of the DIMM are configured in two or more ranks of memory devices. A pair of memory devices, one from each of two ranks, are configured to simulate a memory device having twice the memory capacity of an individual memory device. The DIMM of certain embodiments utilizes a transition bit to select which rank of memory devices is enabled for a read or write transfer operation. In certain embodiments, the logic translation element further comprises a data path multiplexer/demultiplexer which logically isolates the ranks of memory devices from one another. In certain embodiments, the logic translation element further comprises a serial-presence-detect (SPD) element which reports the CAS latency (CL) to the memory controller. The SPD element of certain embodiments reports a CL which has one more cycle than does the actual operational CL of the memory array.

'215 Patent

1. A memory module operable in a computer system to communicate data with a memory controller of the computer system via a memory bus in response to memory commands received from the memory controller, the memory commands including a first memory command and a subsequent second memory command, the first memory command to cause the memory module to receive or output a first data burst and the second memory command to cause the memory module to receive or output a second data burst, the memory module comprising:

...

a plurality of memory integrated circuits mounted on the printed circuit board and arranged in a plurality of ranks including a first rank and a second rank, the plurality of memory integrated circuits including at least one first memory integrated circuit in the first rank and at least one second memory integrated circuit in the second rank, wherein the first rank is selected to receive or output the first data burst in response to the first memory command and is not selected to communicate data with the memory controller in response to the second memory command, and wherein the second rank is selected to receive or output the second data burst in response to the second memory command and is not selected to communicate data with the memory controller in response to the first memory command;

...

logic coupled to the buffer and configured to respond to the first memory command by providing first control signals to the buffer to enable communication of the first data burst between the at least one first memory integrated circuit and the memory controller through the buffer, wherein the logic is further configured to respond to the second memory command by providing second control signals to the buffer to enable communication of the second data burst between the at least one second memory integrated circuit and the memory controller through the buffer, the second control signals being different from the first control signals.

The '087 provisional [EX1005] does not disclose the claimed "[data buffer] control signals"

'417 Patent

1. A memory module operable in a computer system to communicate data with a memory controller of the computer system via a N-bit wide memory bus in response to read or write memory commands received from the memory controller, the memory bus including address and control signal lines and data signal lines, the memory module comprising: a printed circuit board having a plurality of edge connections configured to be electrically coupled to a corresponding plurality of contacts of a module slot of the computer system;

logic coupled to the printed circuit board and configurable

...

active signal value, wherein the logic is further configurable to output data buffer control signals in response to the read or write memory command;

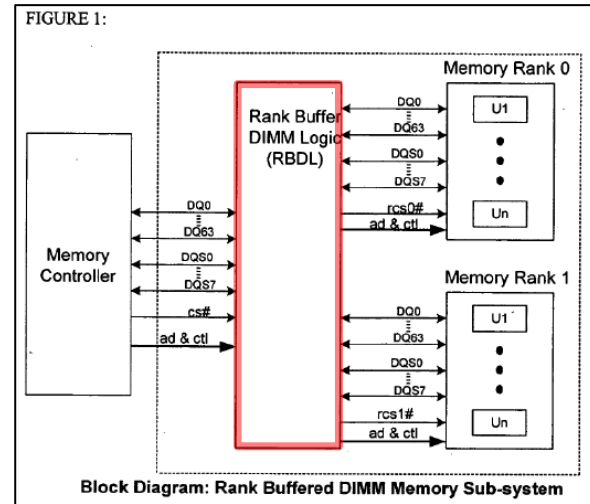
...

response to the read or write command; and

circuitry coupled between the data signal lines in the N-bit wide memory bus and corresponding data pins of memory devices in each of the plurality of N-bit wide ranks, the circuitry being configurable to transfer the burst of N-bit wide data signals between the N-bit wide memory bus and the memory devices in the one of the plurality of N-bit wide ranks in response to the data buffer control signals and in accordance with an overall CAS latency of the memory module;

....

'417: EX1001



EX1005 at 10



Q. Paragraph 5 of the '087

provisional marked as Exhibit 1005 refers to a multiplexer/demultiplexer; correct?

A. Yes, it does.

Q. But that paragraph does not

mention any control signals for that multiplexer/demultiplexer; correct?

A. It doesn't mention control

signals for the multiplexer/demultiplexer, but that doesn't mean those signals are not inherent in -- in that any multiplexer/demultiplexer needs to have control signals to determine its behavior.

EX1095 at 263:12-24; see also id. at 263:6-267:5

'215 Patent

1. A memory module operable in a computer system to communicate data with a memory controller of the computer system via a memory bus in response to memory commands received from the memory controller, the memory commands including a first memory command and a subsequent second memory command, the first memory command to cause the memory module to receive or output a first data burst and the second memory command to cause the memory module to receive or output a second data burst, the memory module comprising:

... a plurality of memory integrated circuits mounted on the printed circuit board and arranged in a plurality of ranks including a first rank and a second rank, the plurality of memory integrated circuits including at least one first memory integrated circuit in the first rank and at least one second memory integrated circuit in the second rank, wherein the first rank is selected to receive or output the first data burst in response to the first memory command and is not selected to communicate data with the memory controller in response to the second memory command, and wherein the second rank is selected to receive or output the second data burst in response to the second memory command and is not selected to communicate data with the memory controller in response to the first memory command;

... logic coupled to the buffer and configured to respond to the first memory command by providing first control signals to the buffer to enable communication of the first data burst between the at least one first memory integrated circuit and the memory controller through the buffer, wherein the logic is further configured to respond to the second memory command by providing second control signals to the buffer to enable communication of the second data burst between the at least one second memory integrated circuit and the memory controller through the buffer, the second control signals being different from the first control signals.

'215: EX1001

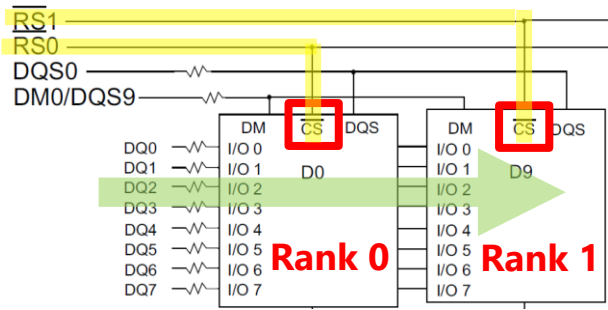
The '087 provisional [EX1005] does not disclose the claimed "[data buffer] control signals" to transfer data to one of the ranks — data could be sent to both ranks as taught by JEDEC

'417 Patent

1. A memory module operable in a computer system to communicate data with a memory controller of the computer system via a N-bit wide memory bus in response to read or write memory commands received from the memory controller, the memory bus including address and control signal lines and data signal lines, the memory module comprising: a printed circuit board having a plurality of edge connections configured to be electrically coupled to a corresponding plurality of contacts of a module slot of the computer system; logic coupled to the printed circuit board and configurable to output data buffer control signals in response to the read or write memory command; response to the read or write command; and circuitry coupled between the data signal lines in the N-bit wide memory bus and corresponding data pins of memory devices in each of the plurality of N-bit wide ranks, the circuitry being configurable to transfer the burst of N-bit wide data signals between the N-bit wide memory bus and the memory devices in the one of the plurality of N-bit wide ranks in response to the data buffer control signals and in accordance with an overall CAS latency of the memory module;

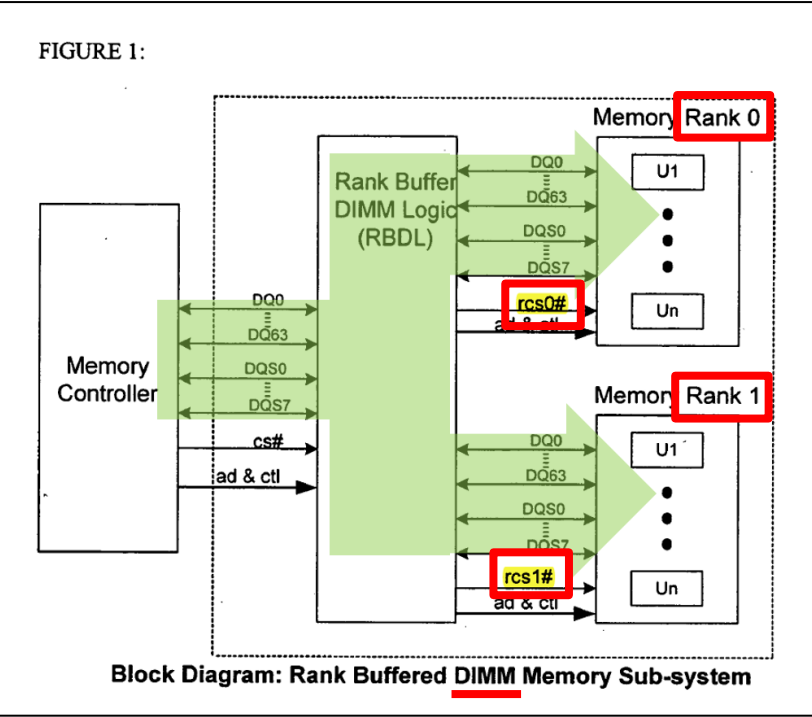
'417: EX1001

Jedec Standard No. 21-C
DDR SDRAM Registered DIMM Design Specification



EX1062 at 12

FIGURE 1:



Block Diagram: Rank Buffered DIMM Memory Sub-system

EX1005 at 10

'215 Patent

1. A memory module operable in a computer system to communicate data with a memory controller of the computer system via a memory bus in response to memory commands received from the memory controller, the memory commands including a first memory command and a subsequent second memory command, the first memory command to cause the memory module to receive or output a first data burst and the second memory command to cause the memory module to receive or output a second data burst, the memory module comprising: a plurality of memory integrated circuits mounted on the printed circuit board and arranged in a plurality of ranks including a first rank and a second rank, the plurality of memory integrated circuits including at least one first memory integrated circuit in the first rank and at least one second memory integrated circuit in the second rank, wherein the first rank is selected to receive or output the first data burst in response to the first memory command and is not selected to communicate data with the memory controller in response to the second memory command, and wherein the second rank is selected to receive or output the second data burst in response to the second memory command and is not selected to communicate data with the memory controller in response to the first memory command; logic coupled to the buffer and configured to respond to the first memory command by providing first control signals to the buffer to enable communication of the first data burst between the at least one first memory integrated circuit and the memory controller through the buffer, wherein the logic is further configured to respond to the second memory command by providing second control signals to the buffer to enable communication of the second data burst between the at least one second memory integrated circuit and the memory controller through the buffer, the second control signals being different from the first control signals.

'215: EX1001

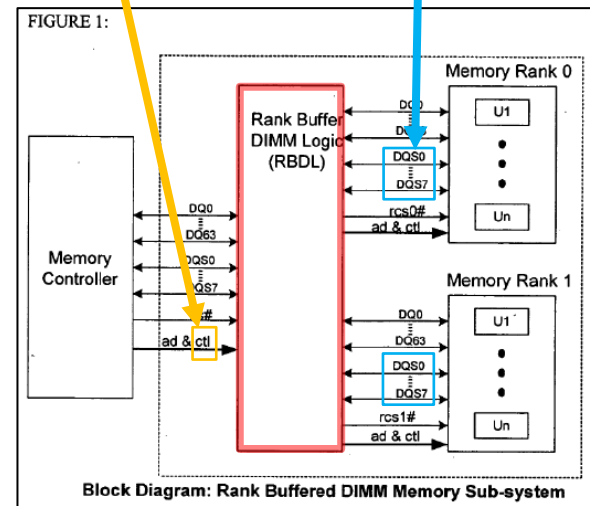
The '087 provisional [EX1005] does not disclose the claimed "[data buffer] control signals" generated by logic on the module — the control signals could come from outside the logic

'417 Patent

1. A memory module operable in a computer system to communicate data with a memory controller of the computer system via a N-bit wide memory bus in response to read or write memory commands received from the memory controller, the memory bus including address and control signal lines and data signal lines, the memory module comprising: a printed circuit board having a plurality of edge connections configured to be electrically coupled to a corresponding plurality of contacts of a module slot of the computer system; logic coupled to the printed circuit board and configurable to output data buffer control signals in response to the read or write memory command; response to the read or write command; and circuitry coupled between the data signal lines in the N-bit wide memory bus and corresponding data pins of memory devices in each of the plurality of N-bit wide ranks, the circuitry being configurable to transfer the burst of N-bit wide data signals between the N-bit wide memory bus and the memory devices in the one of the plurality of N-bit wide ranks in response to the data buffer control signals and in accordance with an overall CAS latency of the memory module;

'417: EX1001

EX1095, 406:5-408:6. More significantly, there is no disclosure that the MUX/DEMUX makes such a selection in response to "[first/second] control signals" that were output from the "logic" on the "memory module" in "respon[se] to the [first/second] memory command," as required by the claims. Instead, any selection by the MUX/DEMUX could be made in response to other signals from outside the logic on the memory module, such as control signals directly from the memory controller, or the DQS preamble from the memory devices, see EX1064, 26 (t_{RPRE}); EX1095, 245:1-247:14. It is not sufficient for Netlist to explain away the DQS preamble, POR 44-45, because that still leaves open other possibilities, such as control signals from the memory controller. And



EX1005 at 10

'215 Patent

1. A memory module operable in a computer system to communicate data with a memory controller of the computer system via a memory bus in response to memory commands received from the memory controller, the memory commands including a first memory command and a subsequent second memory command, the first memory command to cause the memory module to receive or output a first data burst and the second memory command to cause the memory module to receive or output a second data burst, the memory module comprising: a plurality of memory integrated circuits mounted on the printed circuit board and arranged in a plurality of ranks including a first rank and a second rank, the plurality of memory integrated circuits including at least one first memory integrated circuit in the first rank and at least one second memory integrated circuit in the second rank, wherein the first rank is selected to receive or output the first data burst in response to the first memory command and is not selected to communicate data with the memory controller in response to the second memory command, and wherein the second rank is selected to receive or output the second data burst in response to the second memory command and is not selected to communicate data with the memory controller in response to the first memory command; logic coupled to the buffer and configured to respond to the first memory command by providing first control signals to the buffer to enable communication of the first data burst between the at least one first memory integrated circuit and the memory controller through the buffer, wherein the logic is further configured to respond to the second memory command by providing second control signals to the buffer to enable communication of the second data burst between the at least one second memory integrated circuit and the memory controller through the buffer, the second control signals being different from the first control signals.

Netlist's expert's opinion that a DQS preamble cannot be detected is contrary to the record

Netlist's expert's opinion...

Q. So in your opinion, a person of ordinary skill in the art would not be trying to detect the preamble itself? Is that sort of the basis for your opinion in your declaration, starting on paragraph 88 of the '417 IPR and paragraph 91 of the '215 IPR?

A. Much stronger than that. It's not that he wouldn't try to; it's that he can't. There's nothing to grab onto to say "I'm in the preamble now." ...



EX1095 at 291:8-:19 (objection omitted)

... is contrary to the record

(12) **United States Patent**
Srikanth et al.

(10) Patent No.: **US 7,002,378 B2**

(45) Date of Patent: **Feb. 21, 2006**

(22) Filed: **Dec. 29, 2000**

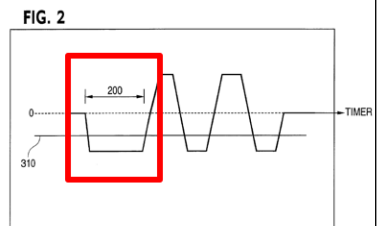
(54) **VALID DATA STROBE DETECTION
TECHNIQUE**

(73) Assignee: **Intel Corporation**, Santa Clara, CA (US)

to latch incorrect data. Accordingly, there is a need for a technique which can identify a valid READ PREAMBLE and subsequently use the validated PREAMBLE to latch the correct data at the receiver.

PREAMBLE period would be equal to 9 ns. The minimum READ PREAMBLE period may be used in accordance with the DDR SDRAM manufacturers and JEDEC specifications for validating the READ PREAMBLE.

by the DDR SDRAM device, if the signal at the receiver is below a predetermined value 310, as illustrated in FIG. 2, for at least a minimum number of samples (e.g. 6 or 7 samples) as sampled by both edges of the 400 MHz clock, then a valid READ PREAMBLE is presumed to have been detected.



EX1113 at 1:49-2:11, 3:48-67 & Fig.2

Netlist's expert's opinion contrary to the record must be disregarded



"[W]e must disregard the testimony of an expert that is plainly inconsistent with the record"

Homeland Housewares, LLC v. Whirlpool Corp.,
865 F.3d 1372, 1378 (Fed. Cir. 2017)



"Courts and tribunals properly discount expert testimony that is at odds with a patent's disclosure, as we did here."

CareFusion Corp. v. Baxter Int'l Inc.,
IPR2016-01463, Paper 40, at 4 (PTAB June 13, 2018)

A POSITA WOULD HAVE COMBINED GROUND 1 WITH ELLSBERRY

Ground 2: Ground 1 + Ellsberry

Perego: Buffered module, using DDR2 SDRAM memories, compatible with existing controller

+

JESD79-2: Details of DDR2 SDRAM systems including their signaling and timing

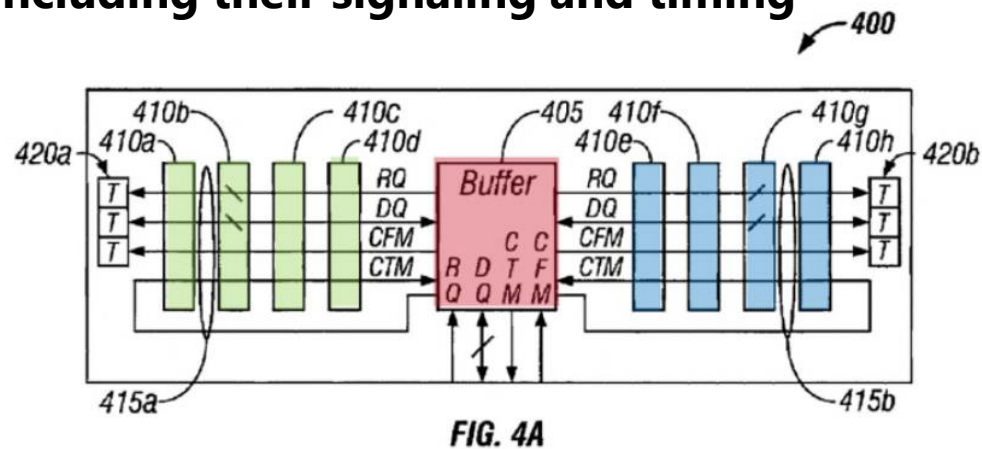


FIG. 4A

In one embodiment, memory devices 410a–410h are Rambus® Dynamic Random access Memory (RDRAM) devices operating at a data rate of 1066 Mbits/sec. Other memory devices may be implemented on module 400, for example, Double Data Rate 2 (DDR2) DRAM devices and Synchronous DRAM (SDRAM) devices. Utilizing buffer

EX1071 (Perego) at 10:54:67, Fig. 4A

Ellsberry: Details of data buffering and rank multiplication with DDR2 signals and timing

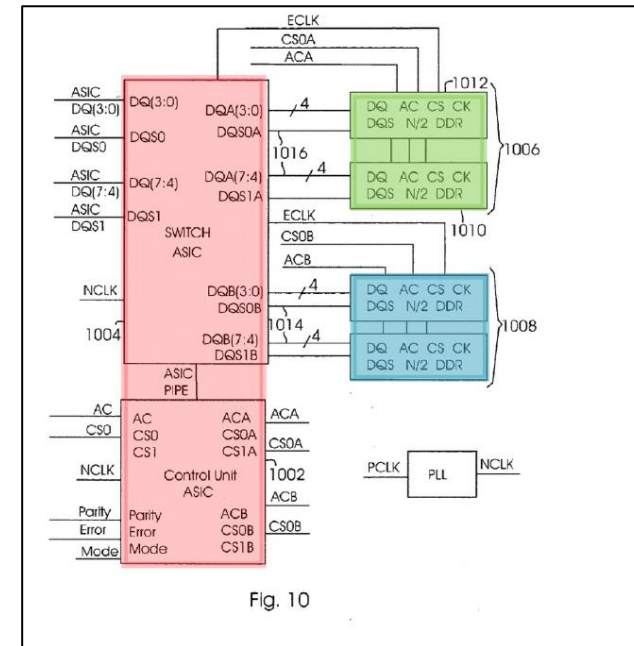


Fig. 10

memory bus. For example, the invention expands the addressable memory banks on a module by making two smaller-capacity memory devices emulate a single higher-capacity memory device. In one implementation, the invention permits two separate SDRAM DDR devices to appear as a single higher-capacity SDRAM DDR device to a source device (e.g., microprocessor, memory controller, etc.).

EX1073 (Ellsberry) at [0026]

The Institution Decision correctly found a motivation to combine Ellsberry with Ground 1 (Perego and JESD79-2)



Perego discloses ranks of memory. Patent Owner further argues that, if Perego discloses ranks, there is no need to look to Ellsberry for teachings on how to target certain devices because Perego discloses its own way of targeting a channel. Prelim. Resp. 37. For the reasons discussed in § II.E.2, we are sufficiently persuaded that the combination of Perego and JESD79-2 teaches the subject matter of claim 1, but **we also are sufficiently persuaded that a person of ordinary skill in the art would have considered additional relevant teachings, such as those in Ellsberry related to active and non-active chip select signals. See Pet. 118–19.**

Patent Owner argues that Petitioner “ignores the significant structural differences in Perego and Ellsberry.” Prelim. Resp. 38; *see* Prelim. Resp. 38–41 (additional arguments regarding structural differences in the references). **On this record, we do not view any alleged structural differences as an impediment to relying on particular teachings of Ellsberry.** Indeed, the Federal Circuit has

consistently held . . . that “[t]he test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference; nor is it that the claimed invention must be expressly suggested in any one or all of the references. Rather, the test is what the combined teachings of the references would have suggested to those of ordinary skill in the art.”

MCM Portfolio LLC v. Hewlett-Packard Co., 812 F.3d 1284, 1294 (Fed. Cir. 2015) (quoting *In re Keller*, 642 F.2d 413, 425 (CCPA 1981)).

‘215: Paper 11 (ID) at 30-32; *see also* ‘417: Paper 11 (ID) at 9-10, 39

Table 10 — Command truth table.

Function	CKE		CS	RAS	CAS	WE
	Previous Cycle	Current Cycle				
Write	H	H	L	H	L	L
Device Deselect	H	X	H	X	X	X

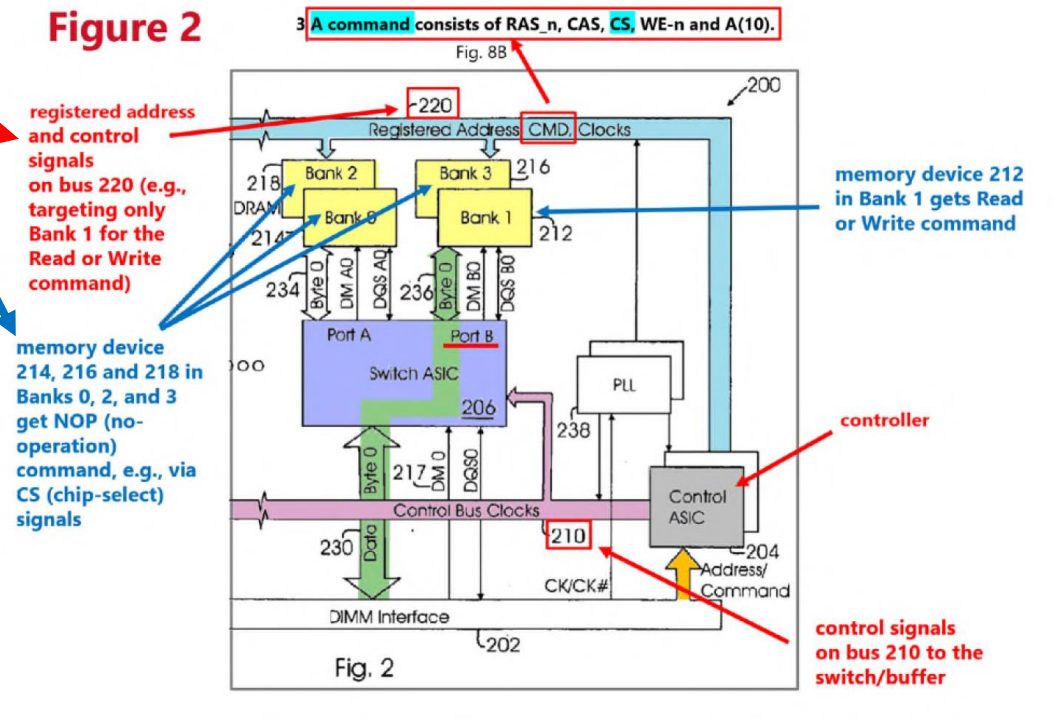
EX1064 (JESD79-2) at 48-49

coupled to the control unit and the bus. The control unit maps a received logical address to a physical address corresponding to the particular memory bank configuration employed. It also directs commands to the memory banks to indicate which memory bank should be operational and which one should be passive (do nothing). The memory bank switch is designed to receive data information from the bus and direct the data information to a plurality of physical memory banks according to control signals from the control unit that maps one logical memory bank to a plurality of physical memory banks. The memory module further includes a plurality of memory devices coupled to the

ks, the plurality of memory memory device to the system single memory device has plurality of memory devices.

EX1073 (Ellsberry) at [0011] & Figs. 2, 8; *see also* EX1074 at 31-37

Figure 2



‘417: Paper 1 (Pet.) at 117

‘215: Paper 1 (Pet.) at 118

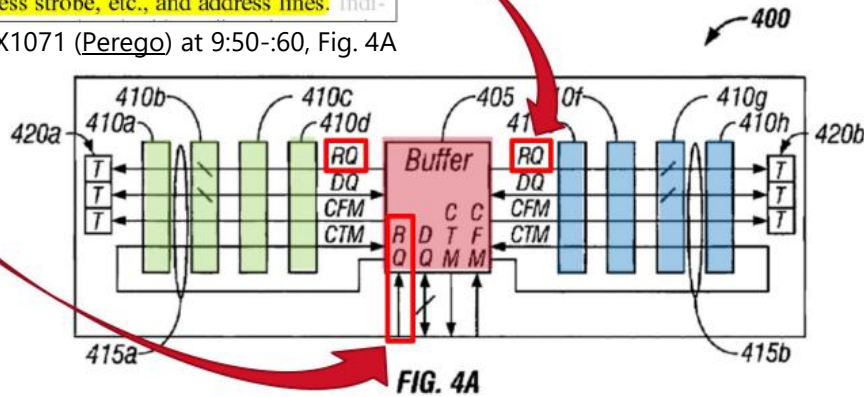
‘417: Paper 27 (Reply) at 26-27; Paper 1 (Pet.) at 20-22, 111-20

‘215: Paper 27 (Reply) at 26-27; Paper 1 (Pet.) at 20-22, 112-26

Perego discloses a “bus” with individual lines consistent with Ellsberry and JEDEC, not just “point-to-point” connections like Rambus

In alternate embodiments, control lines (RQ) may comprise individual control lines, for example, row address strobe, column address strobe, etc., and address lines. Indi-

EX1071 (Perego) at 9:50-:60, Fig. 4A



Here and in the detailed description to follow, “bus” denotes a plurality of signal lines, each having one or more connection points for “transceiving” (i.e., transmitting or receiving). Each connection point connects or couples to a

EX1071 (Perego) at 1:50-:53

In several embodiments, one or more busses or a plurality of point-to-point links may be used to couple one or more buffer devices to a master (e.g., a controller or microprocessor device). A dynamic point-to-point link topology or

EX1071 (Perego) at 3:41-:44



Q. Well, in general, Perego describes, for example, a point-to-point topology; correct?

A. Perego describes a point-to-point topology for Rambus embodiments. He doesn't limit his invention in any way to a point-to-point topology. And, in fact, by explaining that his invention can be built with DDR2, he specifically informs a reader that a point-to-point topology is not necessary.

EX2033 at 29:3-:11

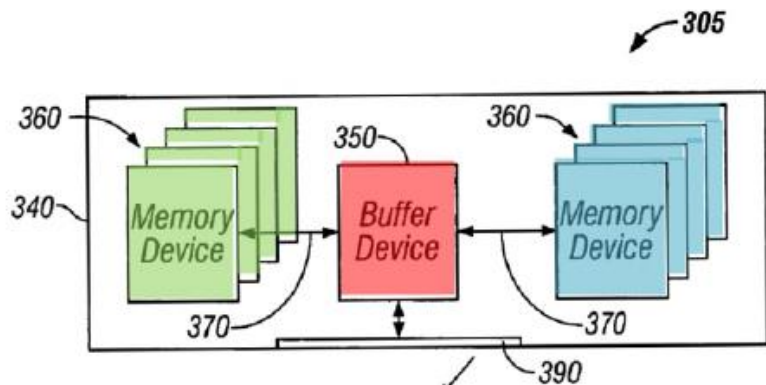
subsystem port via one point-to-point link. The memory subsystem port is disposed on the memory controller interface, which includes a plurality of memory subsystem ports, each having a connection to a point-to-point link. In other embodiments, memory subsystems are connected to a memory subsystem port via a bus (i.e., a plurality of signal lines). A combination of bus and point-to-point connections

EX1071 (Perego) at 5:18-:24

Signaling over point-to-point links 320a-320n or alternatively, over bussed topologies, may incorporate different modulation methods such as non-return to zero (NRZ),

EX1071 (Perego) at 8:42-:44

Both Perego and Ellsberry teach that a data buffer provides electrical isolation for high performance



With further reference to FIGS. 3A and 3B, buffer device 350 transceives and provides isolation between signals interfacing to controller 310 and signals interfacing to the plurality of memory devices 360. In a normal memory read,

EX1071 (Perego) at 6:12-:15 & Fig.3B

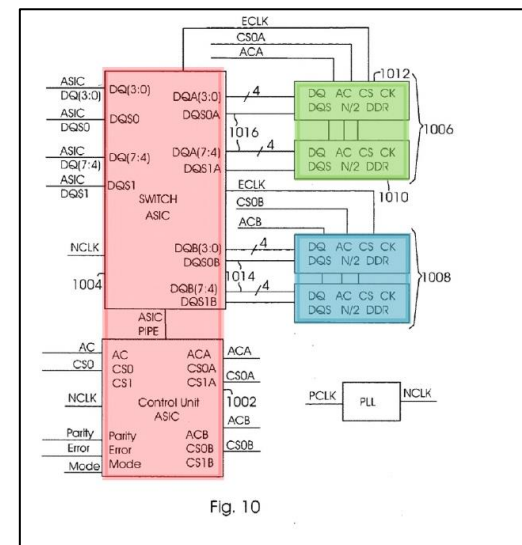


Fig. 10

[0012] The invention expands the memory capacity of a memory module by using a plurality of smaller-capacity memory devices that function as a single higher-capacity memory device. This is accomplished without the need to add more lines to the bus or any additional external signal. Moreover, the load on the bus is not increased because the memory bank switches present a single load to the bus, not the load of the individual memory devices coupled thereto.

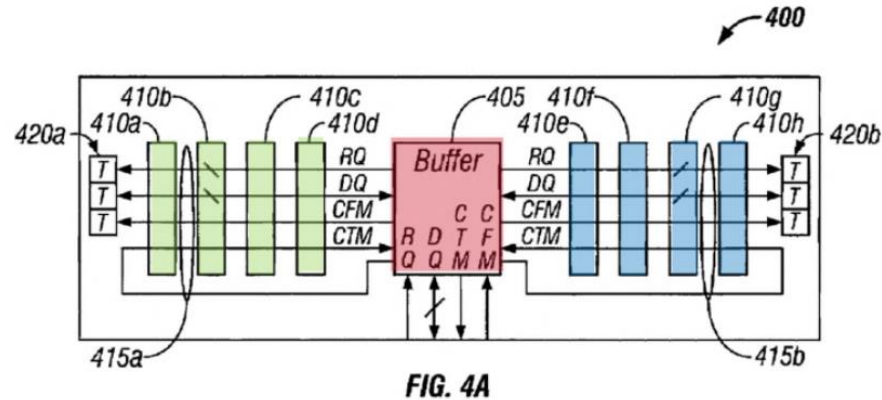
As a result of this architecture, the memory module presents a single electrical load to the system and is compatible with existing standards (e.g., JEDEC compatible, etc.). The Joint Electron Device Engineering Council (JEDEC) standards, used in many memory applications, are incorporated herein by reference.

EX1073 (Ellsberry) at [0012], [0050] & Fig.10; EX1074 at 52-56

'417: Paper 27 (Reply) at 14-15, 26-27; Paper 1 (Pet.) at 20-22, 28-33, 50-51, 111-120

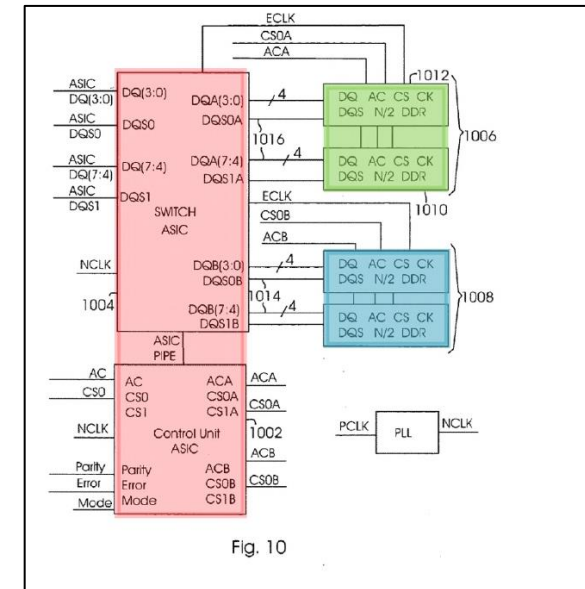
'215: Paper 27 (Reply) at 14-15, 26-27; Paper 1 (Pet.) at 20-22, 30-35, 80, 112-26

Perego's buffer, like Ellsberry, enables rank multiplication by making the type of memory device "transparent" to the system



In one embodiment, memory devices 410a-410h are Rambus® Dynamic Random access Memory (RDRAM) devices operating at a data rate of 1066 Mbits/sec. Other memory devices may be implemented on module 400, for example, Double Data Rate 2 (DDR2) DRAM devices and Synchronous DRAM (SDRAM) devices. Utilizing buffer device 405 between the memory devices and controller in accordance with the present invention (e.g., see FIG. 3) may feasibly render the type of memory device transparent to the system. Different types of memory devices may be included on different modules within a memory system, by employing buffer device 405 to translate protocols employed by controller 310 to the protocol utilized in a particular memory device implementation.

EX1071 (Perego), 10:54-:67 & Fig. 4A



[0026] One embodiment of the invention relates to a system that expands the memory capacity of a memory module without increasing the bus size. A controller and memory bank switch allow the use of separate smaller-capacity memory devices to emulate a single higher-capacity memory device to a host system. This effectively expands the number of addressable banks per memory module without the need for additional chip select lines on the main memory bus. For example, the invention expands the

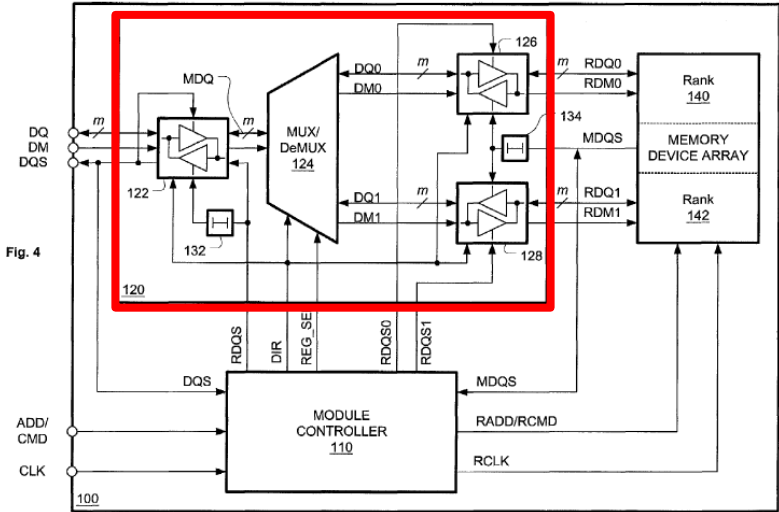
EX1073 (Ellsberry) at [0026] & Fig.10

Both centralized data buffers (like Perego) and distributed data buffers (like Ellsberry) were known alternatives, as confirmed by Halbert

cation in many other advantageous ways. For instance, although the illustrated embodiments use one or two interface circuits and a separate module controller, all of these devices could be integrated in a single device, or in some other number of packages with some other division of the tasks to be performed by the module. The ranks need not be arranged on opposite sides of a card. Such minor modifications are encompassed within the invention, and are intended to fall within the scope of the claims. Although the

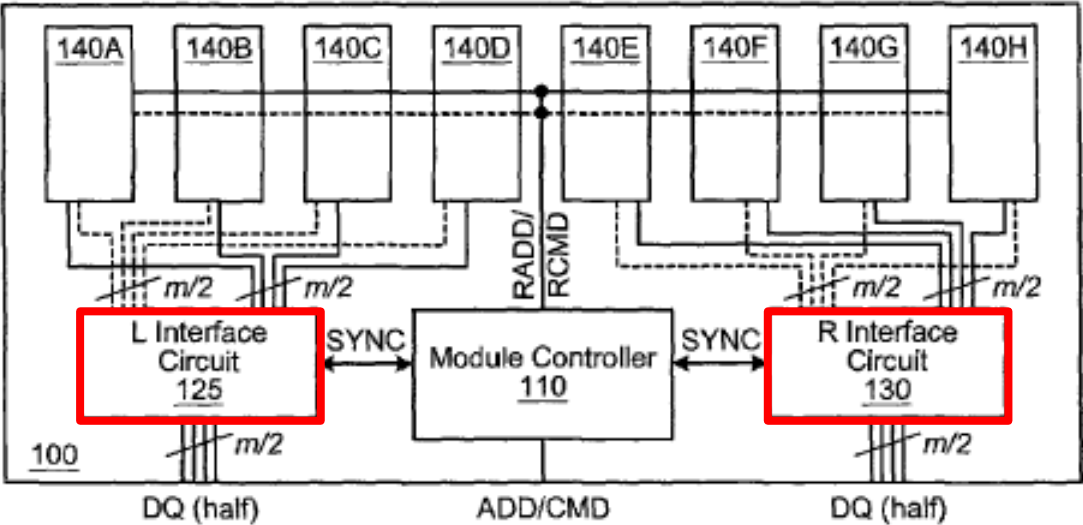
EX1078 (Halbert) at 10:1-:8

Central Data Buffer (m bits wide)



EX1078 (Halbert) at Fig. 4

Distributed Data Buffers



EX1078 (Halbert) at 7:31-:53 & Fig. 7

EX2010 (subject to motion to exclude) is about DDR4 speeds from 10 years after the '417/'215 Patents and is not relevant to the motivation to combine Ellsberry with Perego at DDR2 speeds

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Integrated Device Technology

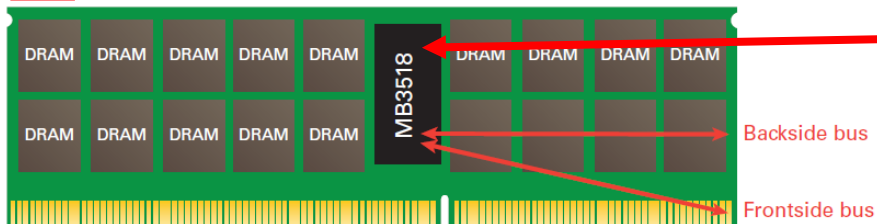


WHITE PAPER

DDR4 LRDIMMs

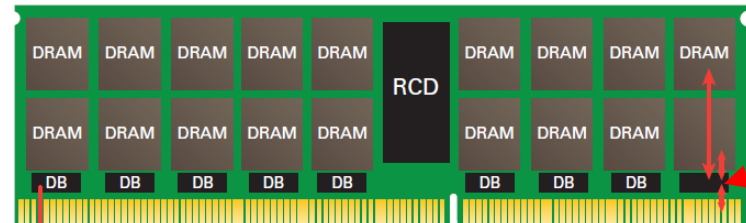
Unprecedented Memory Bandwidth on Samsung DDR4 LRDIMM Enabled by IDT's Register and Data Buffer

DDR3 LRDIMM



Longer traces, both frontside and backside

DDR4 LRDIMM



Data Buffer

Very short frontside trace
Backside same as RDIMM trace length

To understand how DDR4 achieves this breakthrough in LRDIMM technology, stark contrasts can be shown with DDR3. DDR4 and DDR3 LRDIMMs both reduce the number of data loads to improve signal integrity on the memory module's data bus from a maximum of 4 data loads down to 1 data load; however, DDR4 introduces some additional features to reduce overall latency and improve signal integrity, leading to speeds comparable to DDR4 RDIMM. The following tables summarize the key points in this article:

DDR3 LRDIMM Design	Characteristic	Downside
Centralized memory buffer	Longer I/O trace lengths	Longer stubs connected to memory channel cause worse signal reflections, resulting in poorer signal integrity
		Longer traces cause increased latency
		Longer traces cause longer I/O bus turnaround time
Component latency	Delay is approximately 2.5ns	Longer propagation delay adds to latency

DDR4 LRDIMM Design	Characteristic	Upside
Distributed buffers	Shorter I/O trace lengths	Shorter stubs connected to memory channel cause less pronounced signal reflections, resulting in improved signal integrity
		Shorter traces reduce latency
		Shorter traces reduce I/O bus turnaround time
Component latency	Delay is approximately 1.2ns	50% less latency than DDR3 memory buffer,

EX2010 at 1, 2-3, 7

GROUND 3 ('215 AND '417)

6

GROUND 3: GROUND 1 + HALBERT

SUMMARY OF GROUND 3

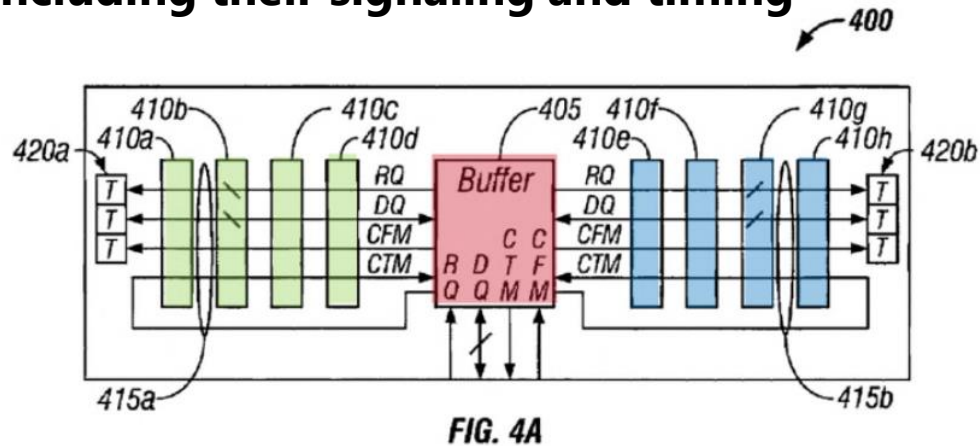
GROUND 1 + HALBERT

Ground 3: Ground 1 + Halbert

Perego: Buffered module, using DDR2 SDRAM memories, compatible with existing controller

+

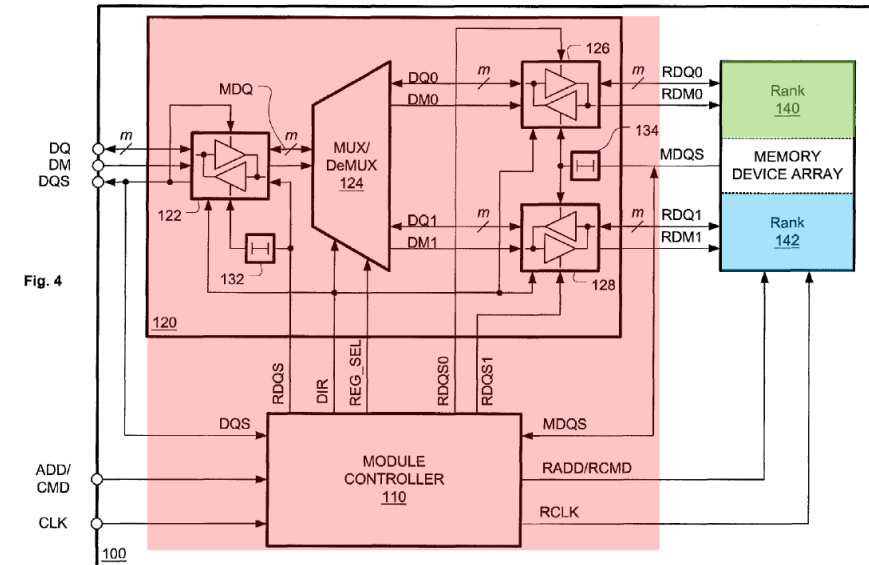
JESD79-2: Details of DDR2 SDRAM systems including their signaling and timing



In one embodiment, memory devices 410a–410h are Rambus® Dynamic Random access Memory (RDRAM) devices operating at a data rate of 1066 Mbits/sec. Other memory devices may be implemented on module 400, for example, Double Data Rate 2 (DDR2) DRAM devices and Synchronous DRAM (SDRAM) devices. Utilizing buffer

EX1071 (Perego) at 10:54-:67, Fig. 4A

Halbert: Details of data buffering with JEDEC signals and timing



attached to. The exemplary embodiments also allow the memory devices to be isolated from the full capacitive loading effects of the system memory data bus. Further, the memory devices of the embodiments avoid arrangements of competing memory banks that load each other, as is the case with a dual-bank DIMM. Finally, with the disclosed embodi-

EX1078 (Halbert) at 3:67-4:5, Fig. 4

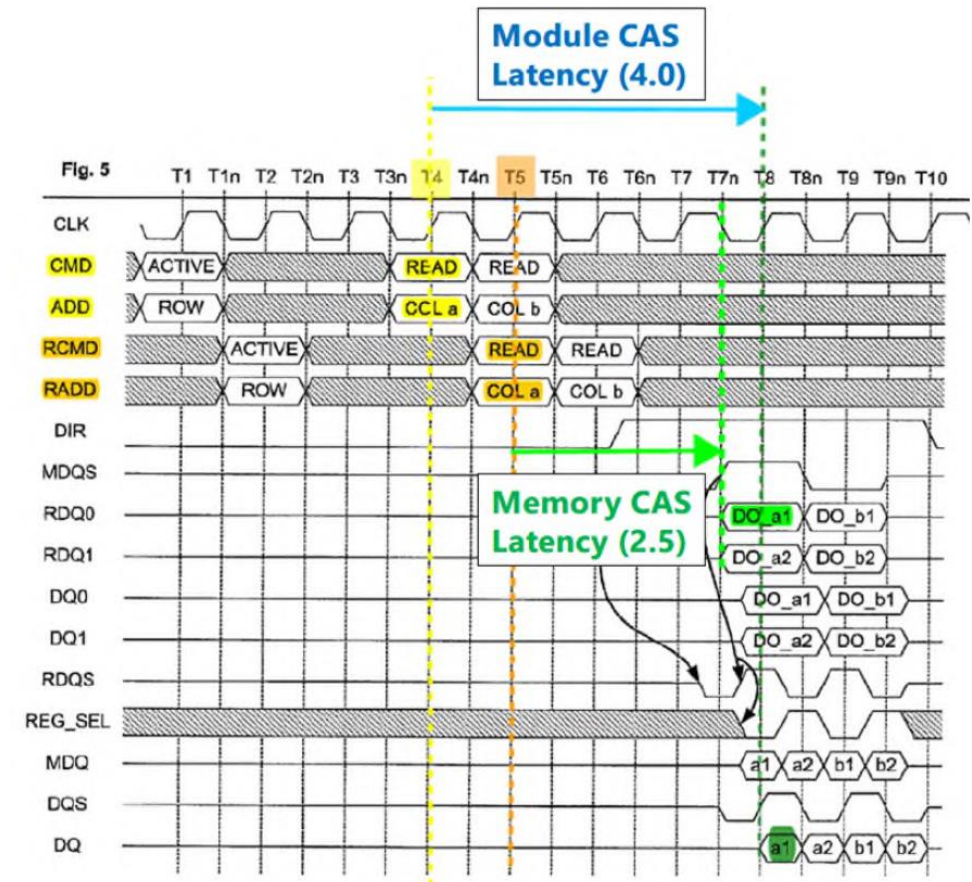
A POSITA WOULD HAVE COMBINED GROUND 1 WITH HALBERT

The Institution Decision correctly found a motivation to combine Halbert with Ground 1 (Perego and JESD79-2)



59. For claim 1, we understand Petitioner to be relying on “Halbert’s disclosure of m-bit wide ranks . . . where ‘m’ can be 64 bits” to bolster its contention that having multiple ranks would have been obvious. Pet. 123–24. We also understand Petitioner to be relying on Halbert’s disclosure of a memory module CAS latency that exceeds the CAS latency of a memory device on the module. Pet. 124–26. This latter teaching appears particularly relevant given the Examiner’s reasons for allowance, which we discuss above in § II.A.2. *See* Ex. 1002, 229–30 (Examiner’s reasons for allowance stating that the “closest prior art of record” does not teach the “circuitry” limitation, including the CAS latency recitations). On this record, we are sufficiently persuaded by Petitioner’s reasoning that a person of ordinary skill in the art “would have recognized that the combination would have resulted in a predictable variation, which would improve similar devices like Perego in the same way and not yield unexpected results or challenges.” *See* Pet. 122 (citing Ex. 1003 ¶ 198).

‘417: Paper 11 (ID) at 41; *see also* ‘215: Paper 11 (ID) at 32-33; EX1030 at 9-11



‘417: Paper 1 (Pet.) at 126
‘215: Paper 1 (Pet.) at 131

Halbert is not limited to memory ranks that perform operations concurrently



As we noted in our Institution Decision, Halbert teaches that “[g]enerally, multiple ranks will receive the same address and commands, and will perform memory operations with the interface circuit concurrently.” Inst. Dec. 28–29 (citing Ex. 1006, 4:57–59). Halbert’s use of the word “generally” means that it is not always the case that memory ranks perform memory operations concurrently. Inst. Dec. 28–29. Thus, as shown in

EX1107 at 27

Q. And do you see on page 149 of Exhibit 1003 in the '417 IPR and also page 152 of Exhibit 1003 of the '215 IPR you have an annotated version of Figure 4 of Halbert that shows Rank 140 in green and Rank 142 in blue?

A. Yes.

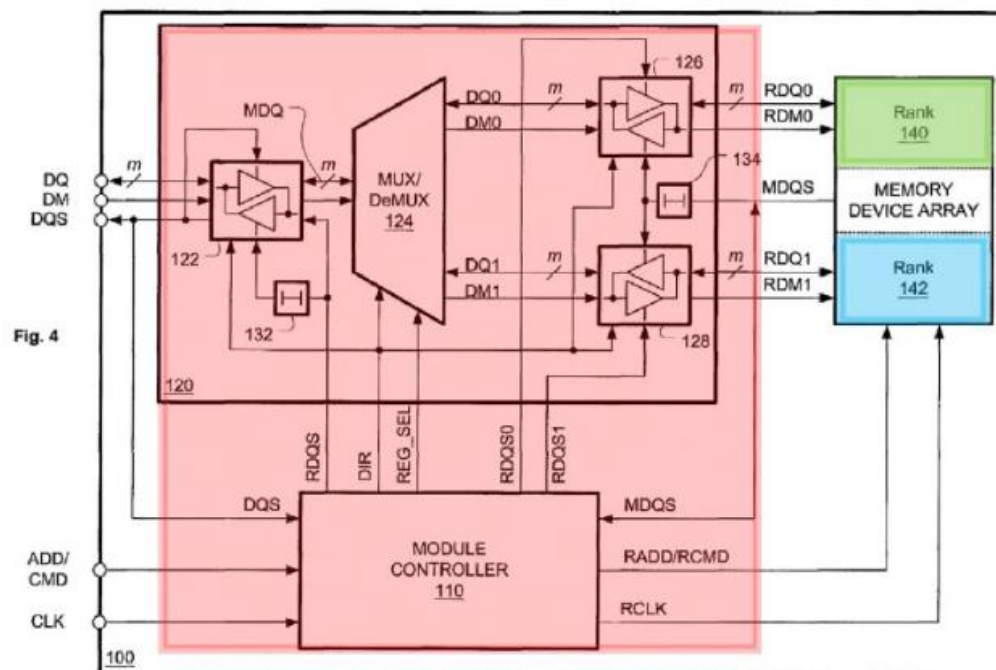
Q. For clarity, can Rank 140 in Halbert and Rank 142 in Halbert, in at least some embodiments, be two separate ranks?

MR. WARRICK: Objection. Form. Leading.

THE WITNESS: Yes. That's what I was indicating in these sections of the report.

EX2033 at 181:3–14

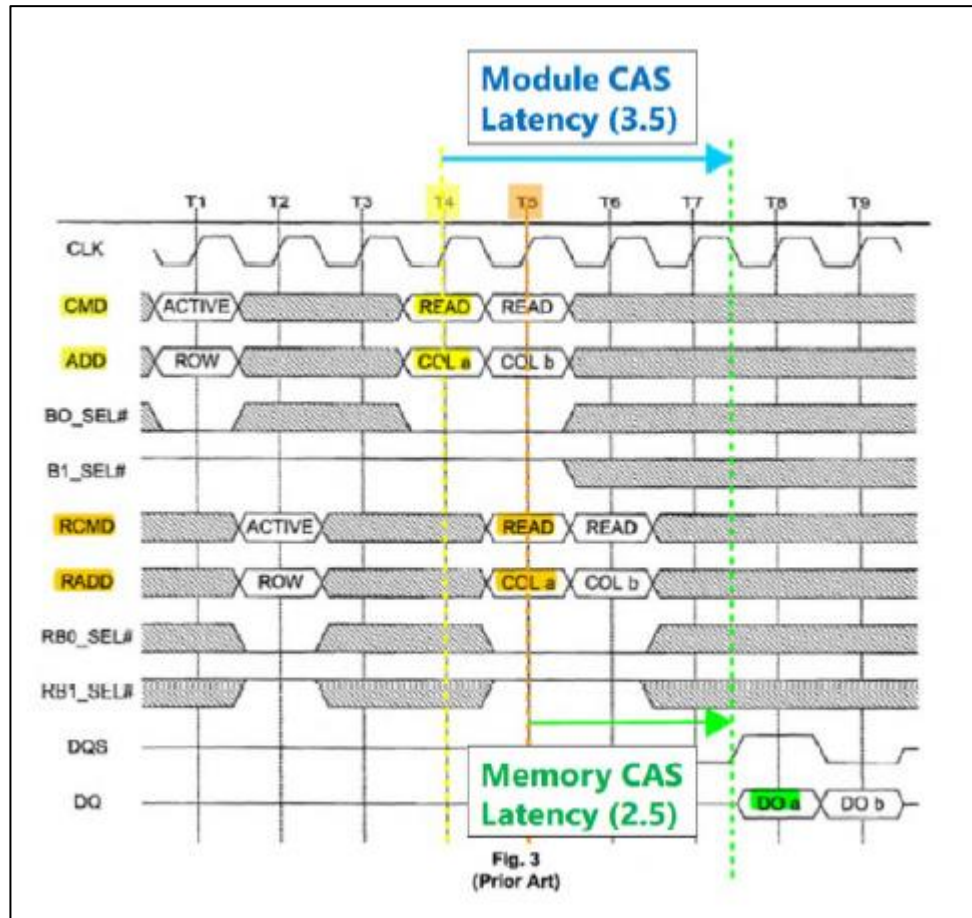
Generally, multiple ranks will receive the same address and commands, and will perform memory operations with the interface circuit concurrently.



EX1078 (Halbert) at 4:57–:59 & Fig. 4

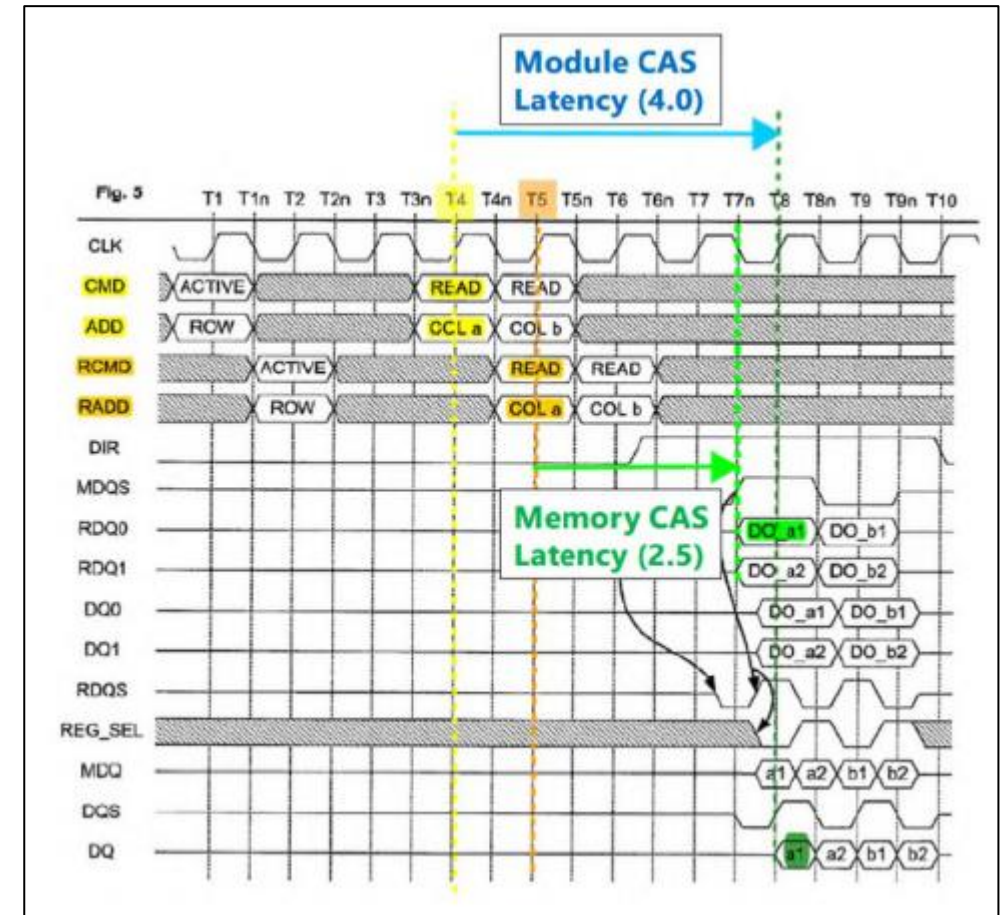
Halbert teaches that adding a data buffer increases the module CAS latency (e.g., by 0.5 clock cycles)

Without data buffer: 3.5 clock cycles



EX1078 (Halbert) at Fig. 3

With data buffer: 4.0 clock cycles



EX1078 (Halbert) at Fig. 5

DDR2 measured latencies in full clock cycles, providing a motivation to delay Halbert's data signal by one full clock cycle



336. A Skilled Artisan would have understood that latencies like the CAS latency of the memory devices are set to a selected value from among a set of predetermined values according to respective standards. For example, the first generation of DDR memory devices could be programmed to have a CAS latency of 1.5, 2, 2.5, or 3 clock cycles. EX1060 (JESD79) at 9-10. Perego expressly discloses using DDR2 SDRAM devices, EX1071 at 10:54-59, and a Skilled Artisan would have understood that **DDR2 memory devices had latency parameters like CAS latency and Additive Latency that could take values of integer clock cycles only.** EX1064 (JESD79-2) at 12 (“The **DDR2 doesn't support half clock latency mode.**”), Fig. 8 (showing CAS Latency of 2, 3, 4, 5), 14 (Fig. 9 showing Additive Latency of 0, 1, 2, 3, 4). **Therefore, a Skilled Artisan would have been motivated to implement a whole-clock-cycle latency for registering the data signals in order to be compatible with the corresponding JEDEC standard. A Skilled Artisan would have also understood that a full clock cycle would have provided more time budget for the data registration thereby avoiding synchronization issues and resulting in more stable, reliable operation.**

JEDEC DDR2 SDRAM SPECIFICATION

CAS Latency

A6	A5	A4	Latency
0	0	0	Reserved
0	0	1	Reserved
0	1	0	2(Optional)
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	Reserved
1	1	1	Reserved

A5	A4	A3	Additive Latency
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

SDRAM. Burst address sequence type is defined by A3, CAS latency is defined by A4 ~ A6. The **DDR2 doesn't support half clock latency mode.** A7 is used for test mode. A8 is used for DLL reset. A7 must be set

EX1064 (JESD79-2) at 12, 14

'215: EX1003 at ¶336

'417: EX1003 at ¶361

'417: Paper 27 (Reply) at 29-30; Paper 1 (Pet.) at 122-25

'215: Paper 27 (Reply) at 29-30; Paper 1 (Pet.) at 129-31

GROUND 4 ('215)

7

GROUND 4: GROUND 1 + MATSUI2

Ground 4 invalidates the '215 Patent

F. Ground 4 adding Matsui2 to Ground 1 (POR 55)

Netlist's arguments against Ground 4 depend entirely on its arguments against Ground 1, *see* POR 55, and thus they are incorrect for all the reasons above (pp.3-21) and as explained in the Petition, Pet. 131-34.

'215: Paper 27 (Reply) at 30

SIMULTANEOUS INVENTION

8

Netlist is incorrect, as a legal matter, that “anticipatory references” are needed to show “simultaneous invention”



“Independently made, **simultaneous inventions**, made ‘within a comparatively short space of time,’ are persuasive evidence that the claimed apparatus ‘was the product only of ordinary mechanical or engineering skill.’...The existence of the Pallmac and Visy machines, however, shows that the Tecasa machine was invented within a ‘comparatively short space of time.’...The district court was therefore correct to conclude that the invention of the Tecasa machine, occurring only a year later than the earliest possible reduction-to-practice date of the claimed invention, qualified as a **simultaneous invention**. As such, ‘though not determinative of statutory **obviousness**, [it is] strong evidence of what constitutes the level of ordinary skill in the art.’”

Geo. M. Martin Co. v. Alliance Machine Sys. Int’l LLC,
618 F.3d 1294, 1305-06 (Fed. Cir. 2010)

“The fact of **near-simultaneous invention**, though not determinative of statutory **obviousness**, is strong evidence of what constitutes the level of ordinary skill in the art.’ *The Int’l Glass Co. v. United States*, 187 Ct.Cl. 376, 408 F.2d 395, 405 (1969).”...

....
The issue of simultaneous invention is directly tied to the level of knowledge attributable to one of ordinary skill in the art. The district court weighed the testimony discussed above, and determined that there was evidence of **simultaneous invention**....

Ecolechem, Inc. v. S. Cal. Edison Co.,
227 F.3d 1361, 1379 (Fed. Cir. 2000)

The '417/'215 Patents disclose and claim "rank multiplication"



Q. Are you familiar with the concept of rank multiplication?

A. Generally yes; and as it's described within this patent specification, yes.

EX1095 at 341:8-11

469. The 417 Patent discloses and claims "rank multiplication" as the solution to expensive, high-density memory devices where "the price per bit ratio of the higher-density DRAM devices is greater than that of the lower-density DRAM devices." See, e.g., EX1001 at 15:62-19:27. But in my opinion, Skilled

'417: EX1003 at ¶469

603. The 215 Patent discloses and claims "rank multiplication" as the solution to expensive, high-density memory devices where "the price per bit ratio of the higher-density DRAM devices is greater than that of the lower-density DRAM devices." See, e.g., EX1001 at 13:51-17:12. But in my opinion, Skilled

'215: EX1003 at ¶603

Most high-density memory modules are currently built with 512-Megabit ("512-Mb") memory devices wherein each memory device has a 64 M×8-bit configuration. For example, a 1-Gigabyte ("1-GB") memory module with error checking capabilities can be fabricated using eighteen such 512-Mb memory devices. Alternatively, it can be economically advantageous to fabricate a 1-GB memory module using lower-density memory devices and doubling the number of memory devices used to produce the desired word width. For example, by fabricating a 1-GB memory module using thirty-six 256-Mb memory devices with 64 M×4-bit configuration, the cost of the resulting 1-GB memory module can be reduced since the unit cost of each 256-Mb memory device is typically lower than one-half the unit cost of each 512-Mb memory device. The cost savings can be significant, even though twice as many 256-Mb memory devices are used in place of the 512-Mb memory devices. For example, by using pairs of 512-Mb memory devices rather than single 1-Gb memory devices, certain embodiments described herein reduce the cost of the memory module by a factor of up to approximately five.

'215: EX1001 at 13:51-14:4

'417: EX1001 at 15:63-16:16

Netlist's expert admitted that Ellsberry implements rank multiplication in a manner "similar" to the '417/'215 Patents



Q. Well, Ellsberry marked as Exhibit 1073 implements rank multiplication; right? For example, in the abstract, last sentence, Ellsberry marked as Exhibit 1073 teaches "making two smaller-capacity memory devices emulating a single higher-capacity memory device"; correct?

A. Yes, the last sentence of the abstract is:

"That is, the invention expands the addressable memory banks on a module by making two smaller-capacity memory devices emulate a single higher-capacity memory device."

And in the context of the JEDEC -- SDRAM memory systems generally, that is what we call rank multiplication.

Q. And, for example, [i]n Figure 7A, 7B, 7C, 7D, E and F, Ellsberry teaches the use of what the '417 and '215 patents refer to as a density transition bit, but which Ellsberry labels a physical bank select, in the column second from the right. . . . And that's similar to the density transition bit in the '417 and '215 patents that we looked at a little bit earlier; correct?

....

THE WITNESS: Similar, yes. I don't know if it's precisely identical in all cases. We'd have to look at the different configurations that are being talked about in the two references. But the general idea appears to be similar.

EX1095 at 414:8-416:7

MOTION TO EXCLUDE 9

EX2003 is impermissible hearsay and inadmissible under FRE 403

1 UNITED STATES PATENT AND TRADEMARK OFFICE
2 BEFORE THE PATENT TRIAL AND APPEAL BOARD
3
4 SAMSUNG ELECTRONICS CO., LTD.,
5 Petitioner,
6 v.
7 NETLIST, INC.,
8 Patent Owner,
9
10 Case No. IPR2022-00615
11 Patent No. 7,619,912
12
13
14
15
16 REMOTE VIDEOTAPED DEPOSITION BY VIRTUAL ZOOM OF
17 ANDREW WOLFE, PH.D.
18 WEDNESDAY, JANUARY 4, 2023
19
20
21 Reported by:
22 Ashala Tylor, CSR #2436, CLR, CRR, RPR
23 JOB NO. 5621734
24
25 PAGES 1 - 233

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Veritext Legal Solutions
866 299-5127

Netlist EX2003
Samsung v Netlist

EX2003 is impermissible hearsay:

- **From a different IPR proceeding**
- **FRE 106 does not apply**
 - Netlist is the party trying to introduce EX2003, so only Samsung could rely on FRE 106, not Netlist
- **FRE 804(b) does not apply**
 - Netlist deposed the expert in this IPR. See EX2033.
- **FRE 801(d)(1) does not apply**
 - Netlist did not cross-examine the witness about his prior testimony
- **FRE 801(d)(2) does not apply**
 - "Since an expert witness is not subject to the control of the party opponent [i.e., Samsung] with respect to consultation and testimony he or she is hired to give, the expert witness cannot be deemed an agent [i.e., of Samsung]." *HTC Corp. v. Telefonaktiebolaget LM Ericsson*, 12 F.4th 476, 489–90 (5th Cir. 2021)

EX2003 is inadmissible under FRE 403:

- **Different patent was at issue**
- **Netlist deposed the same witness regarding the patents at issues in these IPRs. See EX2033.**

EX2003 is inadmissible under 37 C.F.R. § 42.53(f)(5)-(6)

C E R T I F I C A T E

I, the undersigned, a Certified Shorthand Reporter for the State of California, do hereby certify:

That the foregoing proceedings were taken before me at the time and place herein set forth; that a verbatim record of the proceedings was made by me using machine shorthand, which was thereafter transcribed under my direction; further, that the foregoing is an accurate transcription thereof.

I further certify that I am neither financially interested in the action nor a relative or employee of any attorney of any of the parties.

IN WITNESS THEREOF, I have this date subscribed my name this 6th day of January, 2023.



ASHALA TYLOR, CLR, RPR, CRR, CSR #2436

Page 233

D E C L A R A T I O N

I hereby declare I am the deponent in the within matter; that I have read the foregoing transcript and know the contents thereof; and I declare that the same is true of my knowledge except as to the matters which are therein stated upon my information or belief, and as to those matters, I believe them to be true.

I declare under the penalties of perjury under the laws of the United States that the foregoing is true and correct.

This declaration is executed this _____ day of _____, 20____, at _____

CITY STATE

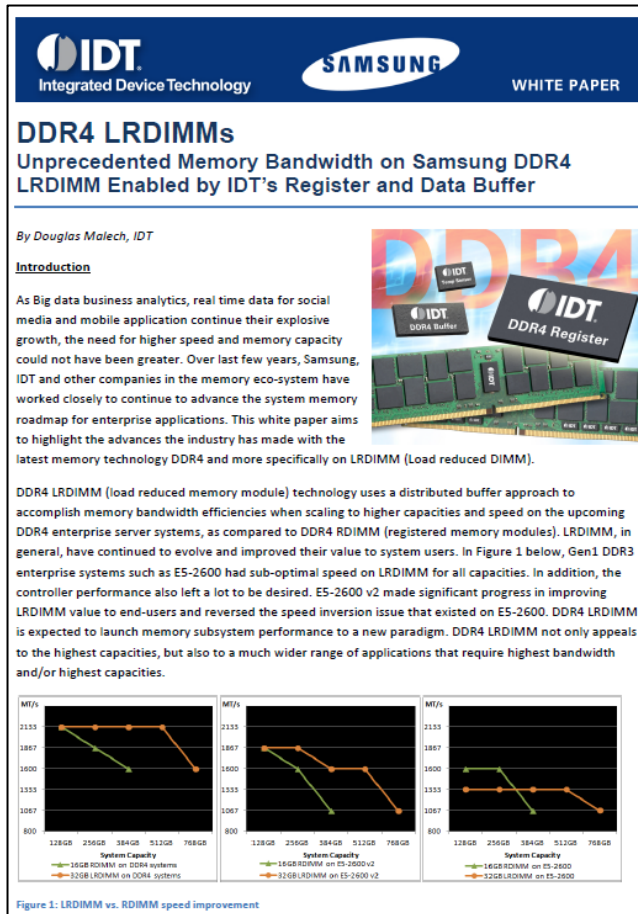
ANDREW WOLFE, PH.D.

Page 232

EX2003 is inadmissible under 37 C.F.R. § 42.53(f)(5)-(6):

- The witness requested a copy of the transcript to review and make corrections. EX2003 at 231:9–10.
- The witness provided a corrected and signed copy of the transcript to Netlist on August 9, 2023
- EX2003 lacks the witness's signature and corrections
- The certificate shows the witness did not refuse to read or sign the transcript

EX2010 is improper hearsay, is irrelevant, and lacks probative value



Integrated Device Technology, IDT and t
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EX2010 is improper hearsay:

- EX2010 is from a third party ("Douglas Malech"), from the company "IDT"
- Offered for the truth of the matter asserted

EX2010 is irrelevant and lacks probative value:

- Almost 10 years after the priority date of the '417 and '215 patents
- Obviousness must be determined as of "the time the invention was made." See 35 U.S.C. § 103(a) (pre-AIA).

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