

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD., MICRON TECHNOLOGY, INC.,
MICRON SEMICONDUCTOR PRODUCTS, INC., and
MICRON TECHNOLOGY TEXAS LLC,¹
Petitioners,

v.

NETLIST, INC.,
Patent Owner.

Case No. IPR2023-00454
Patent No. 11,093,417

EXHIBIT 2036

¹ Micron Technology, Inc., Micron Semiconductor Products, Inc., and Micron Technology Texas LLC filed a motion for joinder and a petition in IPR2023-01141 and have been joined as petitioners in this proceeding.

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SAMSUNG ELECTRONICS CO., LTD.

Petitioner,

v.

NETLIST, INC.

Patent Owner.

**IPR2023-00454 & IPR2023-00455
(U.S. Patent Nos. 11,093,417 & 9,858,215)**

May 3, 2024



IPR2023-00454: Paper 1 (Petition); 11 (Institution Decision); 22 (POR); 27 (Petitioner Reply); 32 (Sur-Reply)

IPR2023-00455: Paper 1 (Petition); 11 (Institution Decision); 22 (POR); 27 (Petitioner Reply); 32 (Sur-Reply)

**Unless otherwise noted, all citations
to papers filed in IPR2023-00454**

Patent Owner Netlist Outline

1. The '417 and '215 Patents

2. All of Petitioner's Grounds are Deficient
3. The Netlist Claims are Directed to Memory Modules
4. Perego vs. JEDEC-Compliant Memory Architectures
5. Ground 1: Perego and JESD79-2
6. Ground 2: Ground 1 + Ellsberry
7. Ground 3: Ground 1 + Halbert

Each Change to a Memory System Leads to a Cascade of Changes

- **Increasing Memory Capacity and Number of Ranks¹ introduces problems**
 - Host System Limitations²
 - Increased Electrical Load³ → lower speed
 - Potential Collisions⁴
 - Timing⁵

¹ EX2024 (Dr. Przybylski Declaration), ¶¶ 74-78

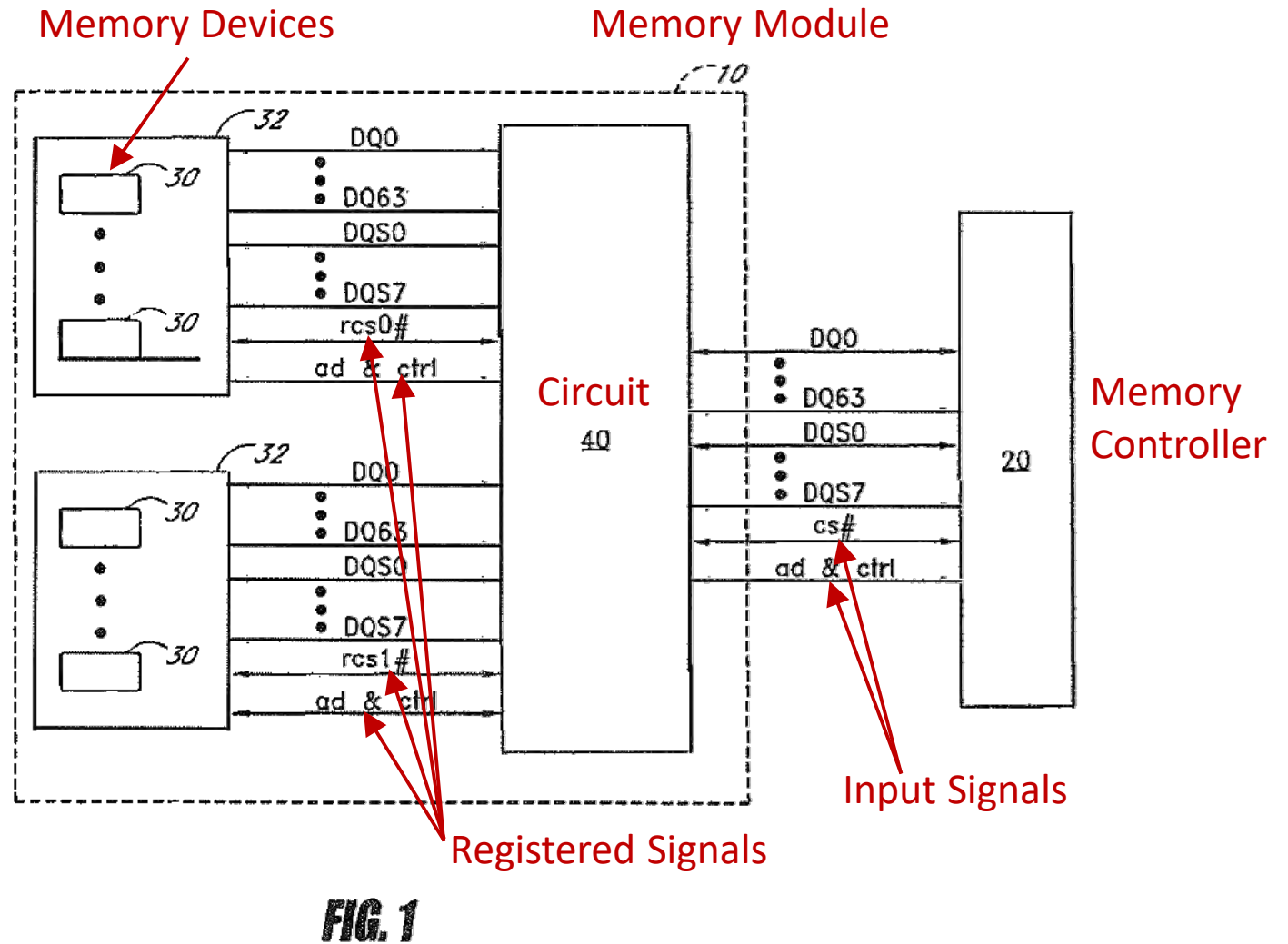
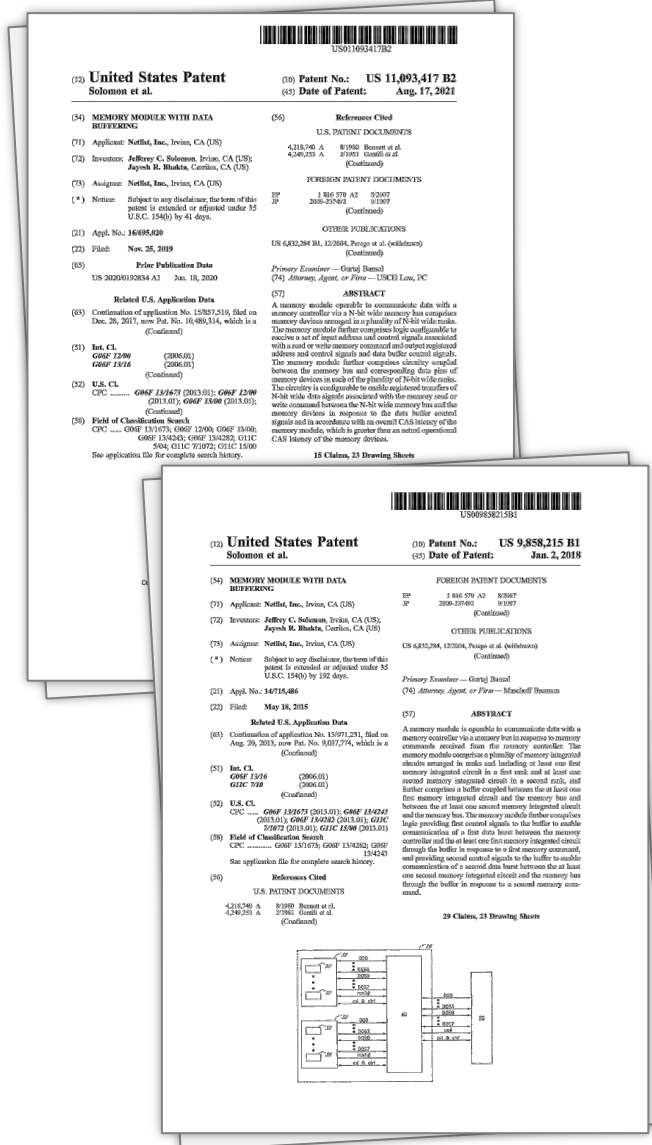
² EX1001 ('417 Patent), 3:2-6, 21:2-9, 22:63-26:6, 41:52-64

³ EX1001, 5:64-10:57

⁴ EX1001, 13:24-15:61, Fig. 7

⁵ EX1001, 22:36-62

'417 and '215 Patents: Figure 1



'417 and '215 Patents: Figure 8D

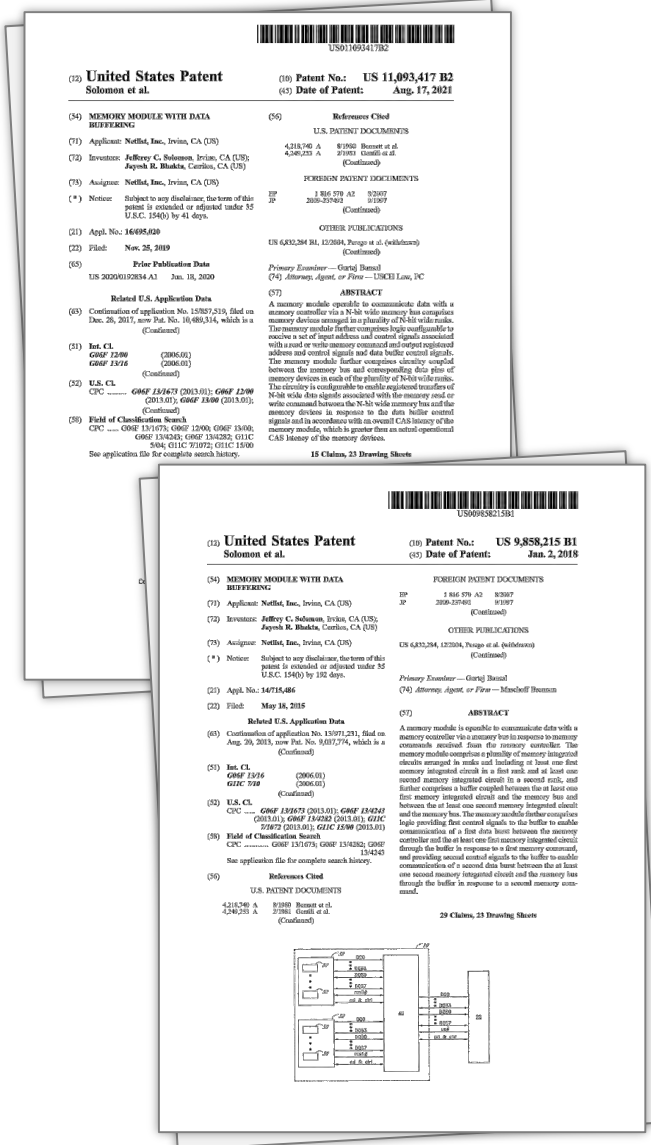
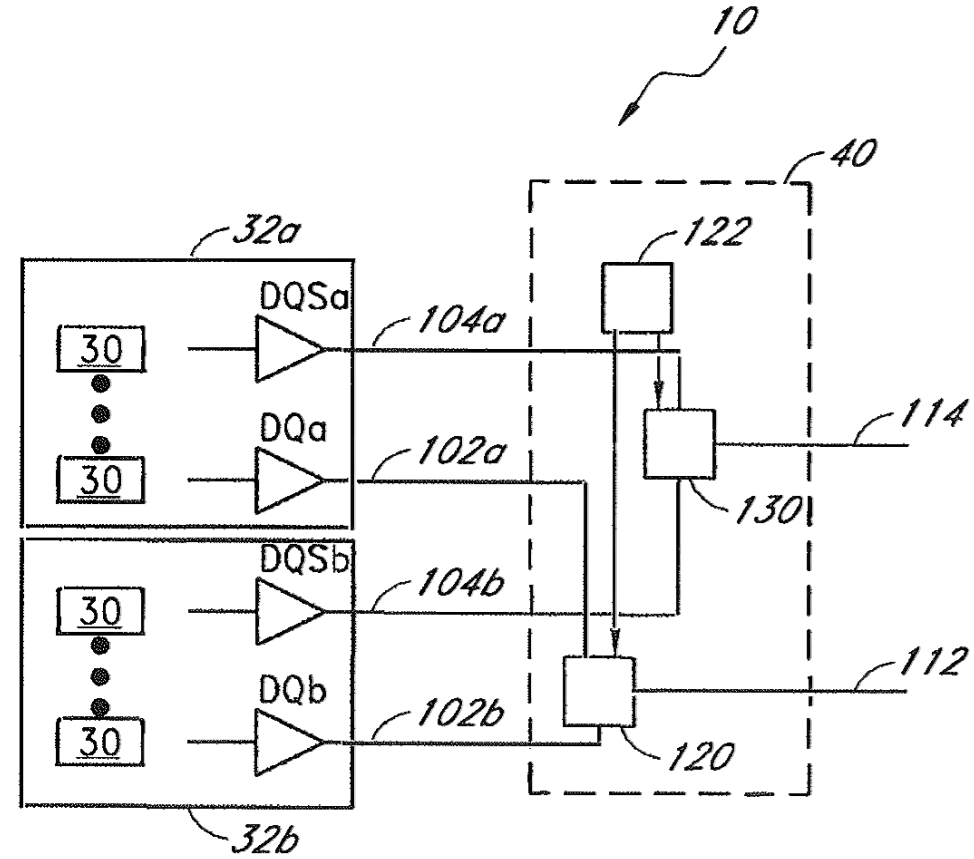
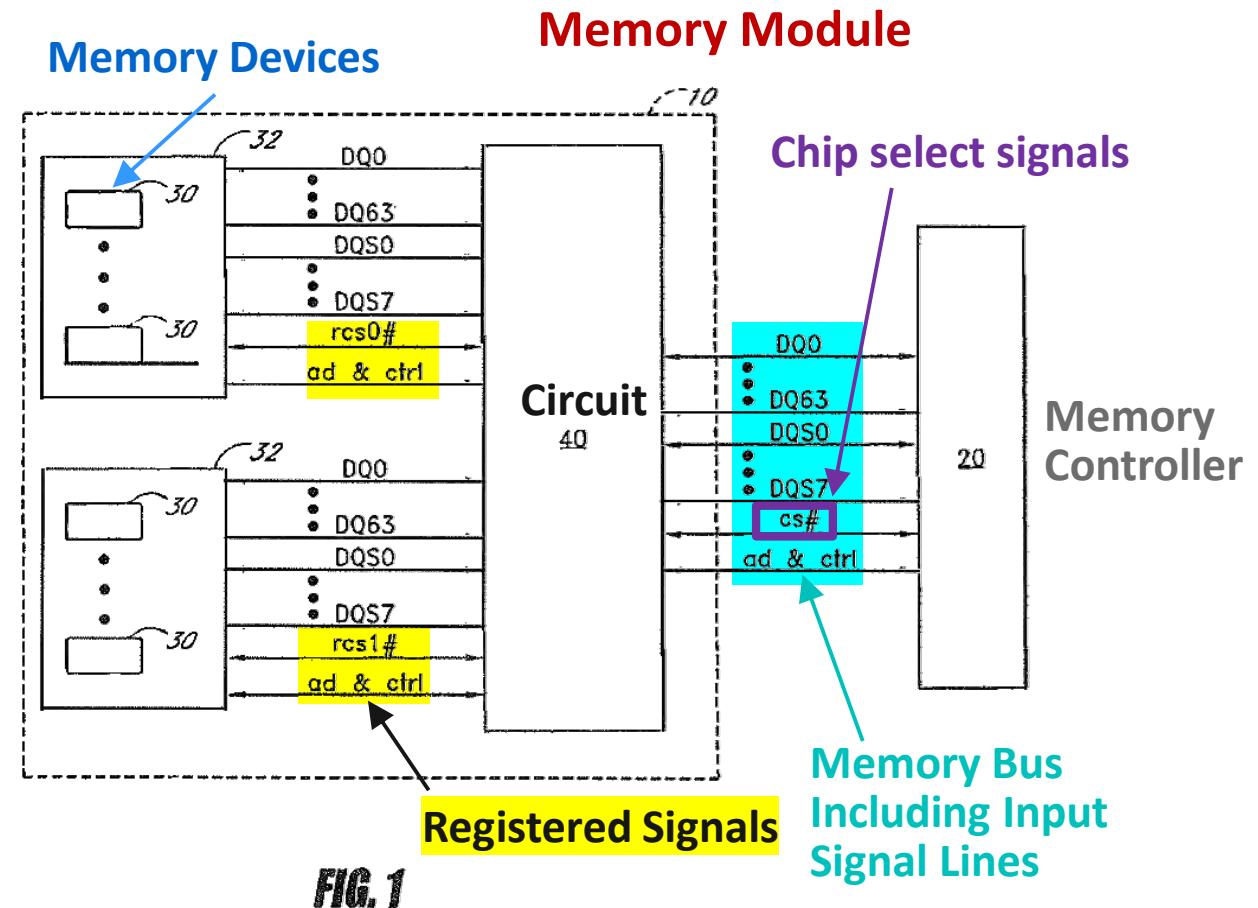


FIG. 8D



'417 Claim 1

1. A **memory module** operable in a computer system to communicate data with a **memory controller** of the computer system via a **N-bit wide memory bus** in response to read or write memory commands received from the memory controller, the **memory bus including address and control signal lines and data signal lines**, the memory module comprising: a printed circuit board having a plurality of edge connections configured to be electrically coupled to a corresponding plurality of contacts of a module slot of the computer system; logic coupled to the printed circuit board and configurable to receive a set of **input address and control signals associated with a read or write memory command via the address and control signal lines** and to **output a set of registered address and control signals** in response to the set of input address and control signals, **the set of input address and control signals including a plurality of input chip select signals and other input address and control signals**, the plurality of **input chip select signals including one chip select signal having an active signal value and one or more other input chip select signals each having a non-active signal value**, the set of **registered address and control signals including a plurality of registered chip select signals** corresponding to respective ones of the plurality of input chip select signals and other registered address and control signals corresponding to respective ones of the other input address and control signals, the **plurality of registered chip select signals including one registered chip select signal having an active signal value and one or more other registered chip select signals each having a non-active signal value**,



'417 Claim 1

(continued)

wherein the logic is further configurable to output data buffer control signals in response to the read or write memory command;

memory devices mounted on the printed circuit board and arranged in a plurality of N-bit wide ranks, wherein the plurality of N-bit wide ranks correspond to respective ones of the plurality of registered chip select signals such that each of the plurality of registered chip select signals is received by memory devices one respective N-bit wide rank of the plurality of N-bit-wide ranks, wherein one of the plurality of N-bit wide ranks including memory devices receiving the registered chip select signal having the active signal value and the other registered address and control signals is configured to receive or output a burst of N-bit wide data signals in response to the read or write command; and

circuitry coupled between the data signal lines in the N-bit wide memory bus and corresponding data pins of memory devices in each of the plurality of N-bit wide ranks, the circuitry being configurable to transfer the burst of N-bit wide data signals between the N-bit wide memory bus and the memory devices in the one of the plurality of N-bit wide ranks in response to the data buffer control signals and in accordance with an overall CAS latency of the memory module;

wherein data transfers through the circuitry are registered for an amount of time delay such that the overall CAS latency of the memory module is greater than an actual operational CAS latency of each of the memory devices.

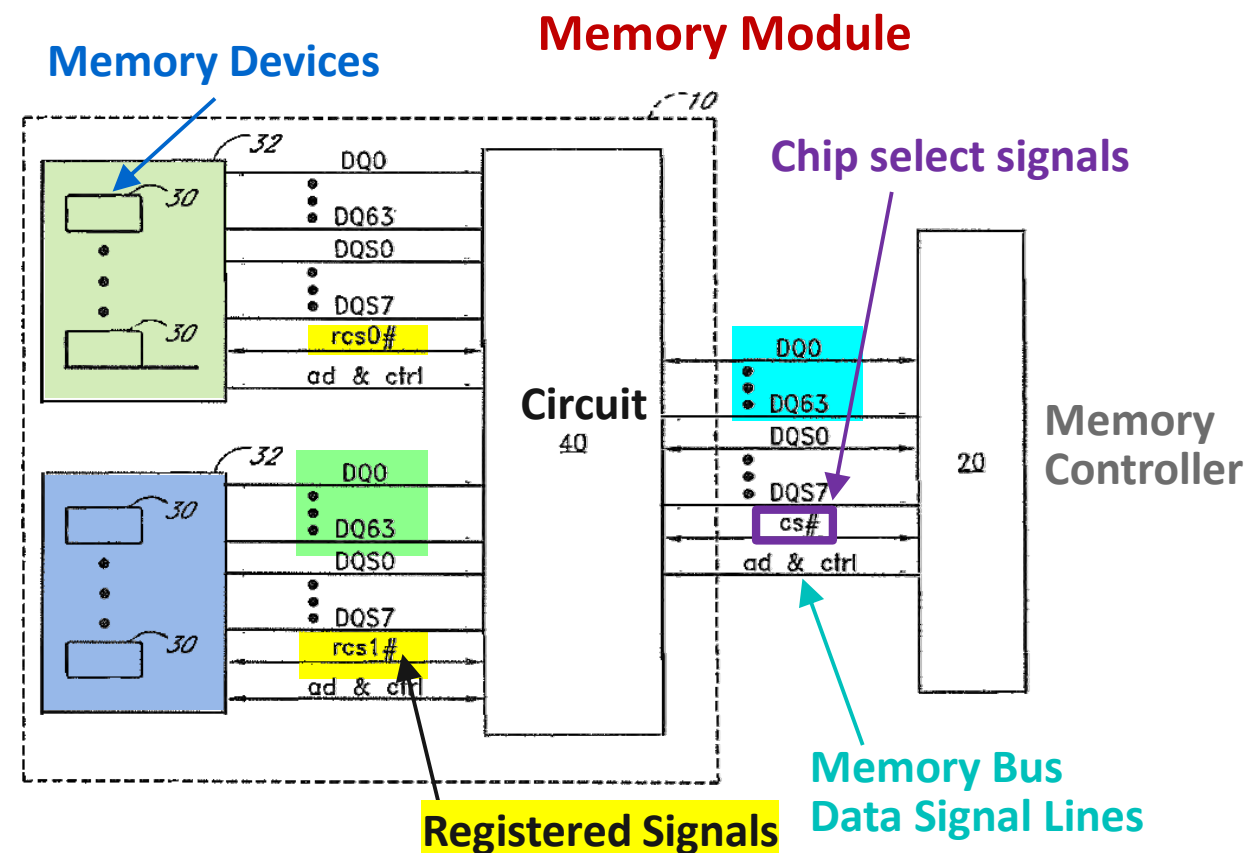


FIG. 1

'417 Claim 1

(continued)

wherein the logic is further configurable to output data buffer control signals in response to the read or write memory command; memory devices mounted on the printed circuit board and arranged in a plurality of N-bit wide ranks, wherein the plurality of N-bit wide ranks correspond to respective ones of the plurality of registered chip select signals such that each of the plurality of registered chip select signals is received by memory devices one respective N-bit wide rank of the plurality of N-bit-wide ranks, wherein one of the plurality of N-bit wide ranks including memory devices receiving the registered chip select signal having the active signal value and the other registered address and control signals is configured to receive or output a burst of N-bit wide data signals in response to the read or write command; and

circuitry coupled between the data signal lines in the N-bit wide memory bus and corresponding data pins of memory devices in each of the plurality of N-bit wide ranks, the circuitry being configurable to transfer the burst of N-bit wide data signals between the N-bit wide memory bus and the memory devices in the one of the plurality of N-bit wide ranks in response to the data buffer control signals and in accordance with an overall CAS latency of the memory module;

wherein data transfers through the circuitry are registered for an amount of time delay such that the overall CAS latency of the memory module is greater than an actual operational CAS latency of each of the memory devices.

In the example embodiments schematically illustrated by FIGS. 3A, 3B, 4A, and 4B, the circuit 40 comprises a logic element which is integral with and comprises the switches 120 which are coupled to the DQ data signal lines and the DQS data strobe signal lines. In certain such embodiments, each switch 120 comprises a data path multiplexer/demultiplexer. In certain other embodiments, the circuit 40 comprises a logic element 122 which is a separate component operatively coupled to the switches 120, as schematically illustrated by FIGS. 5A-5D. The one or more switches 120 are operatively coupled to the logic element 122 to receive control signals from the logic element 122 and to selectively electrically couple one or more data signal lines to a common data signal line. Example switches compatible with

9:37-50

In certain embodiments, the circuit 40 also provides the load isolation described above in reference to FIGS. 1-5. For example, as schematically illustrated by FIG. 8C, the circuit 40 comprises both the switch 120 for the DQ data signal lines 102a, 102b and the switch 130 for the DQS data strobe signal lines 104a, 104b. While in certain embodiments, the switches 130 are integral with a logic element of the circuit 40, in certain other embodiments, the switches 130 are separate components which are operatively coupled to a logic element 122 of the circuit 40, as schematically illustrated by FIG. 8D. In certain such embodiments, the control and timing of the switch 130 is performed by the circuit 40 which is resident on the memory module 10. Example

15:28-40

'417 Claim 1

(continued)

wherein the logic is further configurable to output data buffer control signals in response to the read or write memory command;
memory devices mounted on the printed circuit board and arranged in a plurality of N-bit wide ranks, wherein the plurality of N-bit wide ranks correspond to respective ones of the plurality of registered chip select signals such that each of the plurality of registered chip select signals is received by memory devices one respective N-bit wide rank of the plurality of N-bit-wide ranks, wherein one of the plurality of N-bit wide ranks including memory devices receiving the registered chip select signal having the active signal value and the other registered address and control signals is configured to receive or output a burst of N-bit wide data signals in response to the read or write command; and

circuitry coupled between the data signal lines in the N-bit wide memory bus and corresponding data pins of memory devices in each of the plurality of N-bit wide ranks, the circuitry being configurable to transfer the burst of N-bit wide data signals between the N-bit wide memory bus and the memory devices in the one of the plurality of N-bit wide ranks in response to the data buffer control signals and in accordance with an overall CAS latency of the memory module;

wherein data transfers through the circuitry are registered for an amount of time delay such that the overall CAS latency of the memory module is greater than an actual operational CAS latency of each of the memory devices.

In certain embodiments, the circuit 40 comprises the SPD device 240 which reports the CAS latency (CL) to the memory controller of the computer system. The SPD device 240 of certain embodiments reports a CL which has one more cycle than does the actual operational CL of the memory array. In certain embodiments, data transfers between the memory controller and the memory module are registered for one additional clock cycle by the circuit 40. The additional clock cycle of certain embodiments is added to the transfer time budget with an incremental overall CAS latency. This extra cycle of time in certain embodiments advantageously provides sufficient time budget to add a buffer which electrically isolates the ranks of memory devices 30 from the memory controller 20. The buffer of certain embodiments comprises combinatorial logic, registers, and logic pipelines. In certain embodiments, the buffer

22:36-52

'417 Claim 1

(continued)

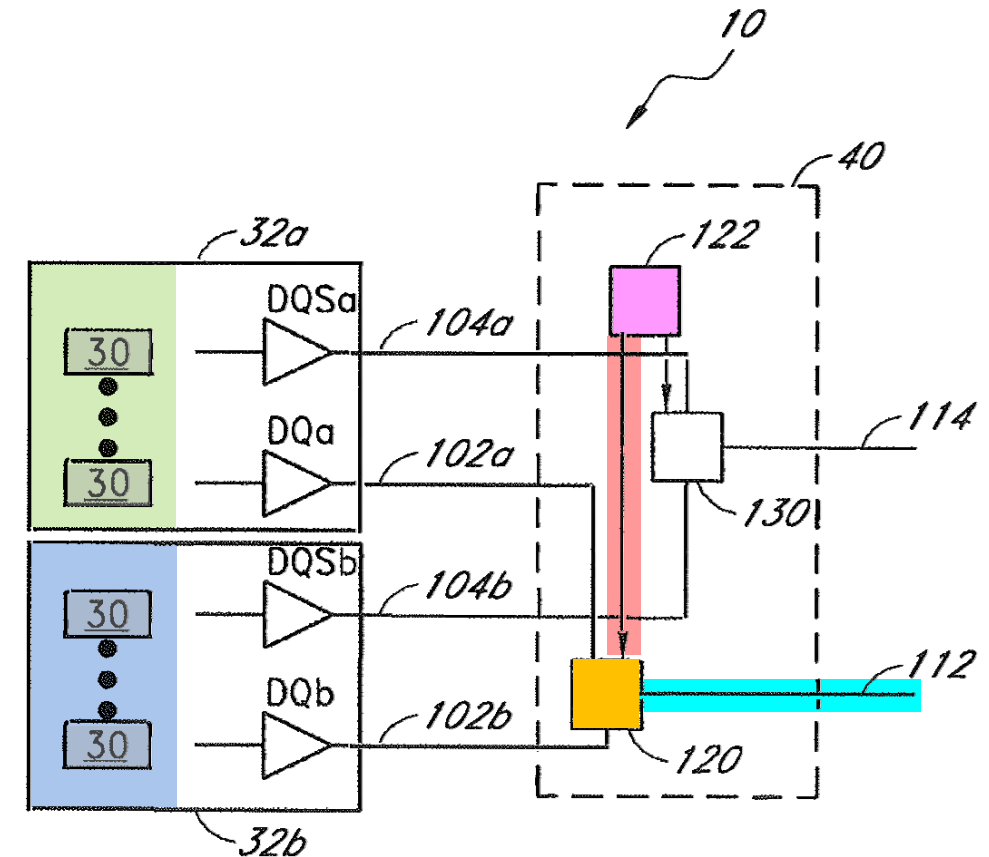
wherein the logic is further configurable to output data buffer control signals in response to the read or write memory command;

memory devices mounted on the printed circuit board and arranged in a plurality of N-bit wide ranks, wherein the plurality of N-bit wide ranks correspond to respective ones of the plurality of registered chip select signals such that each of the plurality of registered chip select signals is received by memory devices one respective N-bit wide rank of the plurality of N-bit-wide ranks, wherein one of the plurality of N-bit wide ranks including memory devices receiving the registered chip select signal having the active signal value and the other registered address and control signals is configured to receive or output a burst of N-bit wide data signals in response to the read or write command; and

circuitry coupled between the data signal lines in the N-bit wide memory bus and corresponding data pins of memory devices in each of the plurality of N-bit wide ranks, the circuitry being configurable to transfer the burst of N-bit wide data signals between the N-bit wide memory bus and the memory devices in the one of the plurality of N-bit wide ranks in response to the data buffer control signals and in accordance with an overall CAS latency of the memory module;

wherein data transfers through the circuitry are registered for an amount of time delay such that the overall CAS latency of the memory module is greater than an actual operational CAS latency of each of the memory devices.

FIG. 8D



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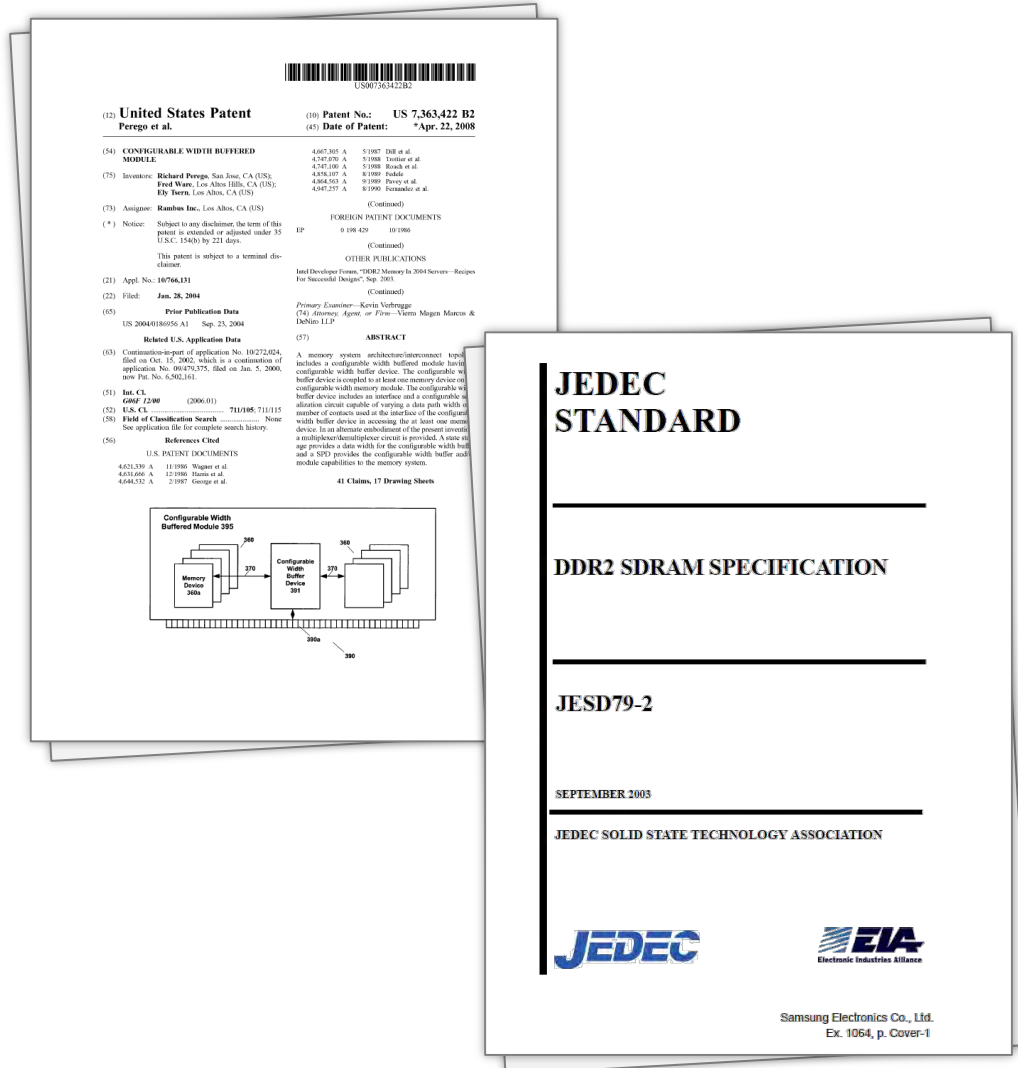
7. Ground 3: Ground 1 + Halbert

All of Petitioner's Grounds Are Deficient

GROUND 1

- **Missing Elements:**
 - **No** input chip-select signals
 - **No** plurality of ranks
 - **No** CAS-latency claim elements

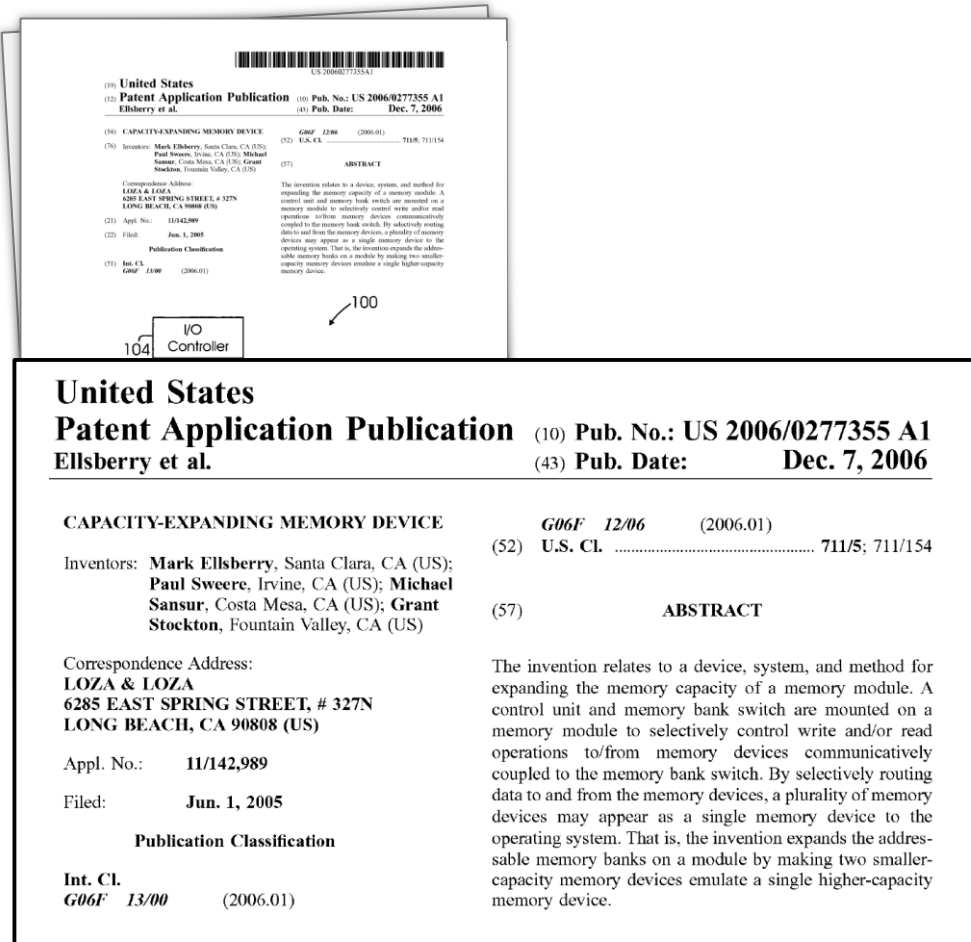
- **No Motivation to Combine *Perego* and *JESD79-2*:**
 - Perego architecture and JEDEC architecture are two divergent approaches
 - Adding chip-selects to Perego would destroy the principle of operation of Perego
 - Perego already provides support for DDR2 memory devices through a translation feature



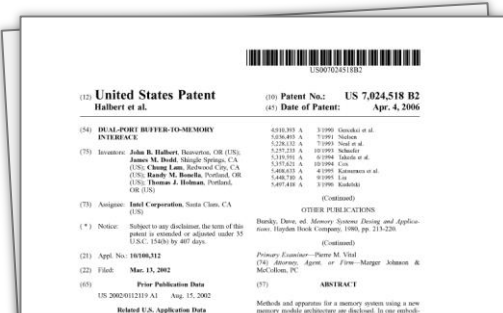
All of Petitioner's Grounds Are Deficient

GROUND 2

- Ellsberry is **not** a printed publication (similar issue now before the Federal Circuit)
- Ellsberry is **not** Prior Art: Ellsberry was filed Jun. 1, 2005. The '087 provisional application supports the challenged claims and was filed on January 19, 2005, prior to Ellsberry.
 - The '537 Patent starts the continuation chain and claims priority to the '087 provisional application
- **No** motivation to combine JEDEC-style teachings with Perego's primary link architecture



All of Petitioner's Grounds Are Deficient



In an operating environment, the data buffer connects to a memory bus. When a data access is performed, both ranks exchange data signaling with their corresponding data registers during a single data access. At the buffer, the memory bus data transfer occurs in two consecutive clock cycles, one cycle for each rank. This allows the memory bus transfer rate to double for the same memory bus width and memory device speed.

GROUND 3

- *Halbert* characterizes two parts of a memory array as “ranks”
- But they operate together to double the transfer rate, **NOT** as independent ranks according to Petitioner’s construction
 - **No** registered chip-selects of an inactive value
- **No** disclosure of CAS latency related limitation

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'417 and '215 Patents: “Memory Module with Data Buffering”



(12) United States Patent
Solomon et al.

(10) Patent No.: US 11,093,417 B2
(45) Date of Patent: Aug. 17, 2021

(54) MEMORY MODULE WITH DATA
BUFFERING

(56) References Cited
U.S. PATENT DOCUMENTS

(71) Applicant: Netlist, Inc., Irvine, CA (US)

4,218,740 A 8/1980 Bennett et al.

(12) United States Patent
Solomon et al.

(10) Patent No.: US 11,093,417 B2
(45) Date of Patent: Aug. 17, 2021

(54) MEMORY MODULE WITH DATA
BUFFERING

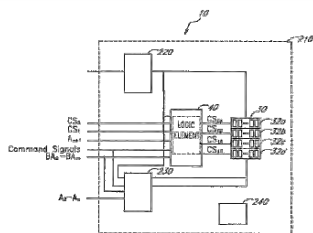
(56) References Cited
U.S. PATENT DOCUMENTS

(71) Applicant: Netlist, Inc., Irvine, CA (US)

4,218,740 A 8/1980 Bennett et al.

See application file for complete search history.

15 Claims, 23 Drawing Sheets



IPR2023-00454: EX1001



(12) United States Patent
Solomon et al.

(10) Patent No.: US 9,858,215 B1
(45) Date of Patent: Jan. 2, 2018

(54) MEMORY MODULE WITH DATA
BUFFERING

FOREIGN PATENT DOCUMENTS

(71) Applicant: Netlist, Inc., Irvine, CA (US)

JP 1 816 570 A2 8/2007
JP 2009-237491 9/1997
(Continued)

(72) Inventor: Jeffrey C. Solomon, Irvine, CA (US);
Jayesh R. Bhakta, Carlsbad, CA (US)

OTHER PUBLICATIONS

(73) Assignee: Netlist, Inc., Irvine, CA (US)

US 6,832,284, 12/2004, Pease et al. (withdrawn)
(Continued)

(*) Notice: Subject to any disclaimer, the term of this
patent is extended or adjusted under 35
U.S.C. 154(b) by 192 days.

Primary Examiner—Guraj Bhatta

(21) Appl. No.: 14/715,486

(74) Attorney, Agent, or Firm—Maschhoff Brennan

(22) Filed: May 18, 2015

(57) ABSTRACT

Related U.S. Application Data

(63) Continuation of application No. 13/971,231, filed on
Aug. 20, 2013, now Pat. No. 9,037,774, which is a
(Continued)

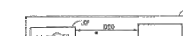
(51) Int. Cl.
G06F 15/26 (2006.01)
G1C 7/18 (2006.01)
(Continued)

A memory module is operable to communicate data with a
memory controller via a memory bus in response to memory
commands received from the memory controller. The
memory module comprises a plurality of memory integrated
circuits arranged in banks and including at least one first
memory integrated circuit in a first bank and at least one
second memory integrated circuit in a second bank, and
further comprises a buffer coupled between the at least one
first memory integrated circuit and the memory bus and
between the at least one second memory integrated circuit
and the memory bus. The memory module further comprises
logic providing first control signals to the buffer to enable
communication of a first data burst between the memory
controller and the at least one first memory integrated circuit
through the buffer in response to a first memory command,
and providing second control signals to the buffer to enable
communication of a second data burst between the at least
one second memory integrated circuit and the memory bus
through the buffer in response to a second memory com-
mand.

(56) References Cited

U.S. PATENT DOCUMENTS
4,218,740 A 8/1980 Bennett et al.
4,240,233 A 7/1989 Gossin et al.
(Continued)

29 Claims, 23 Drawing Sheets



(12) United States Patent
Solomon et al.

(10) Patent No.: US 9,858,215 B1
(45) Date of Patent: Jan. 2, 2018

(54) MEMORY MODULE WITH DATA
BUFFERING

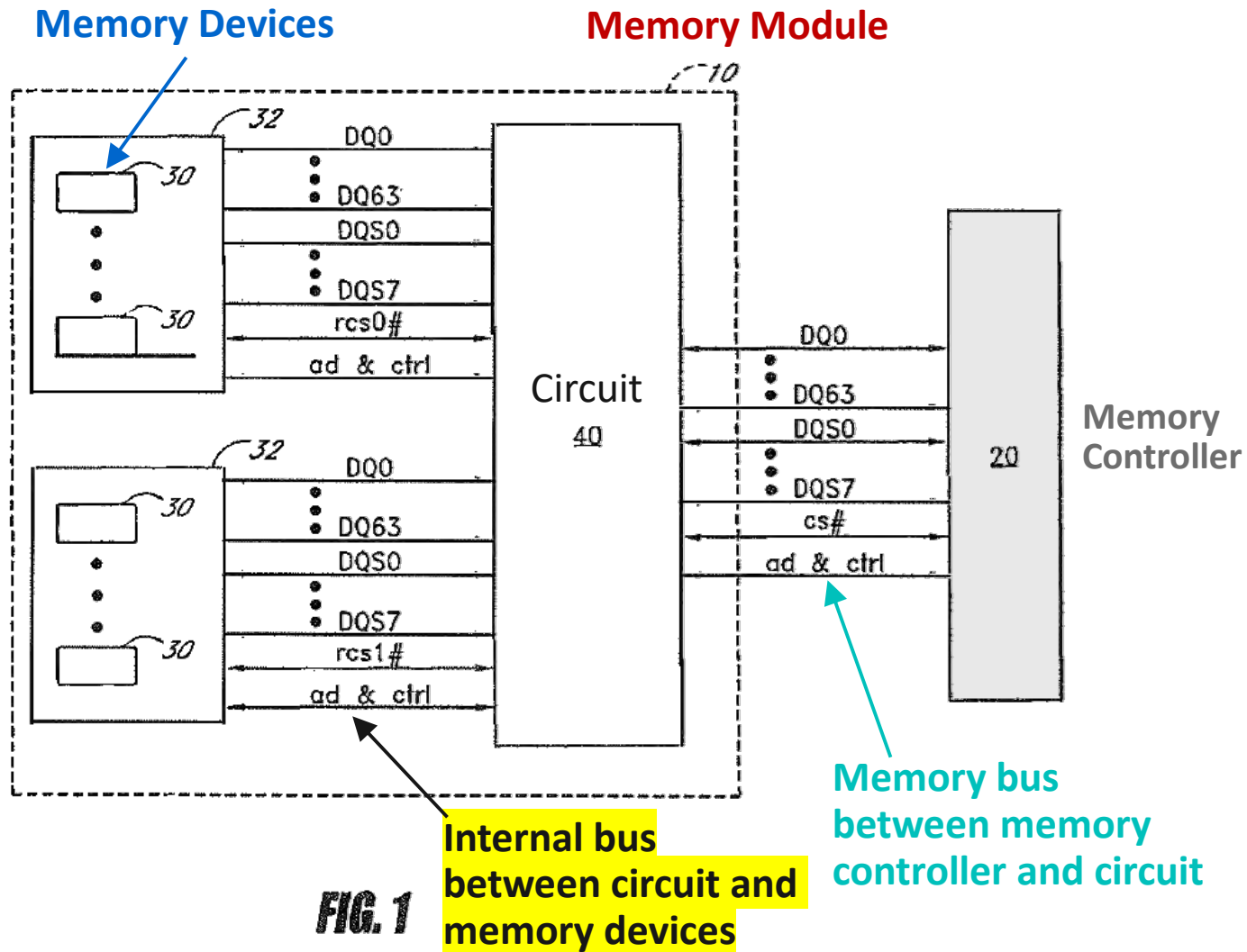
FOREIGN PATENT DOCUMENTS

(71) Applicant: Netlist, Inc., Irvine, CA (US)

EP 1 816 570 A2 8/2007
JP 2009-237492 9/1997

IPR2023-00455: EX1001

Memory Devices = Memory Chips on a Module



'417 Patent Figure 1

Memory module includes

- memory devices
- bus between memory controller and circuit 40
- bus between circuit 40 and memory devices

The Claimed Memory Module

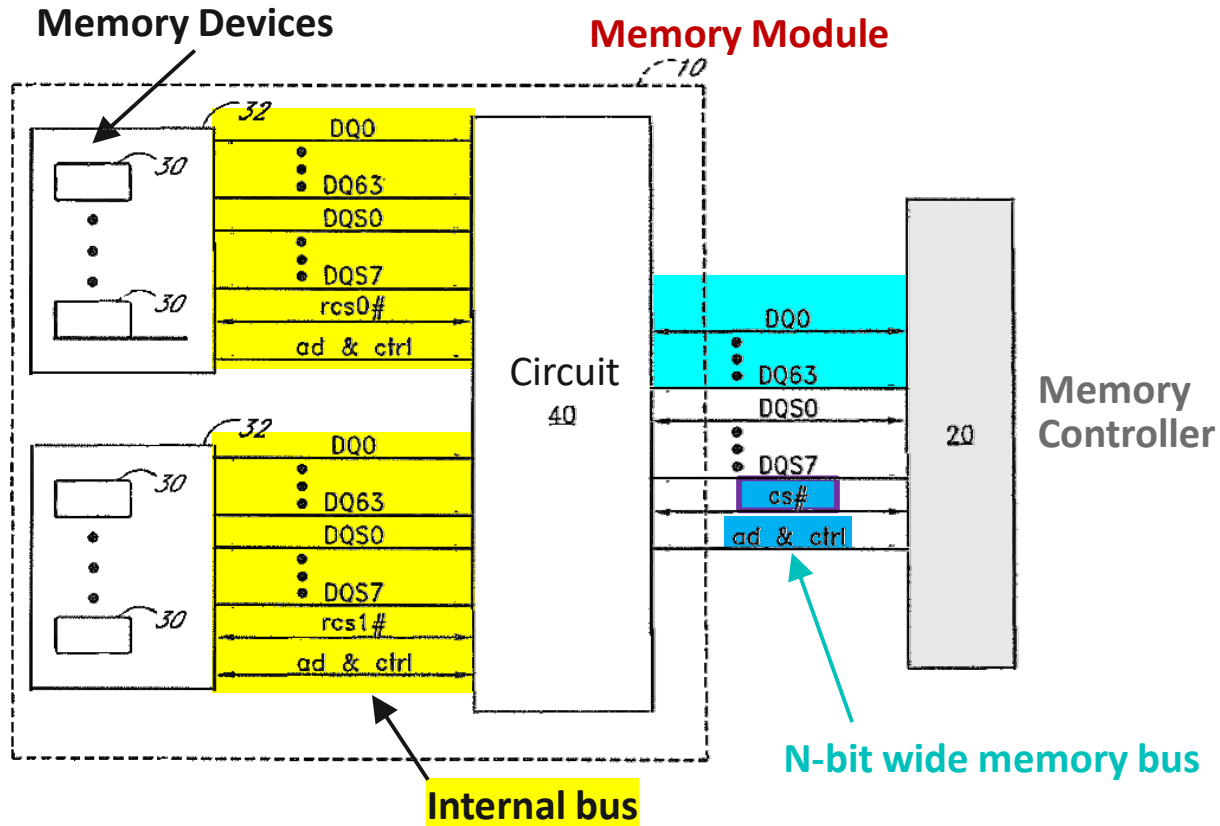


FIG. 1

1. A **memory module** operable in a computer system to communicate data with a **memory controller** of the computer system via a N-bit wide memory bus in response to read or write memory commands received from the **memory controller**, the memory bus including **address and control signal lines** and **data signal lines**, the memory module comprising:

“Input Signals” Come from Memory Controller in the Host

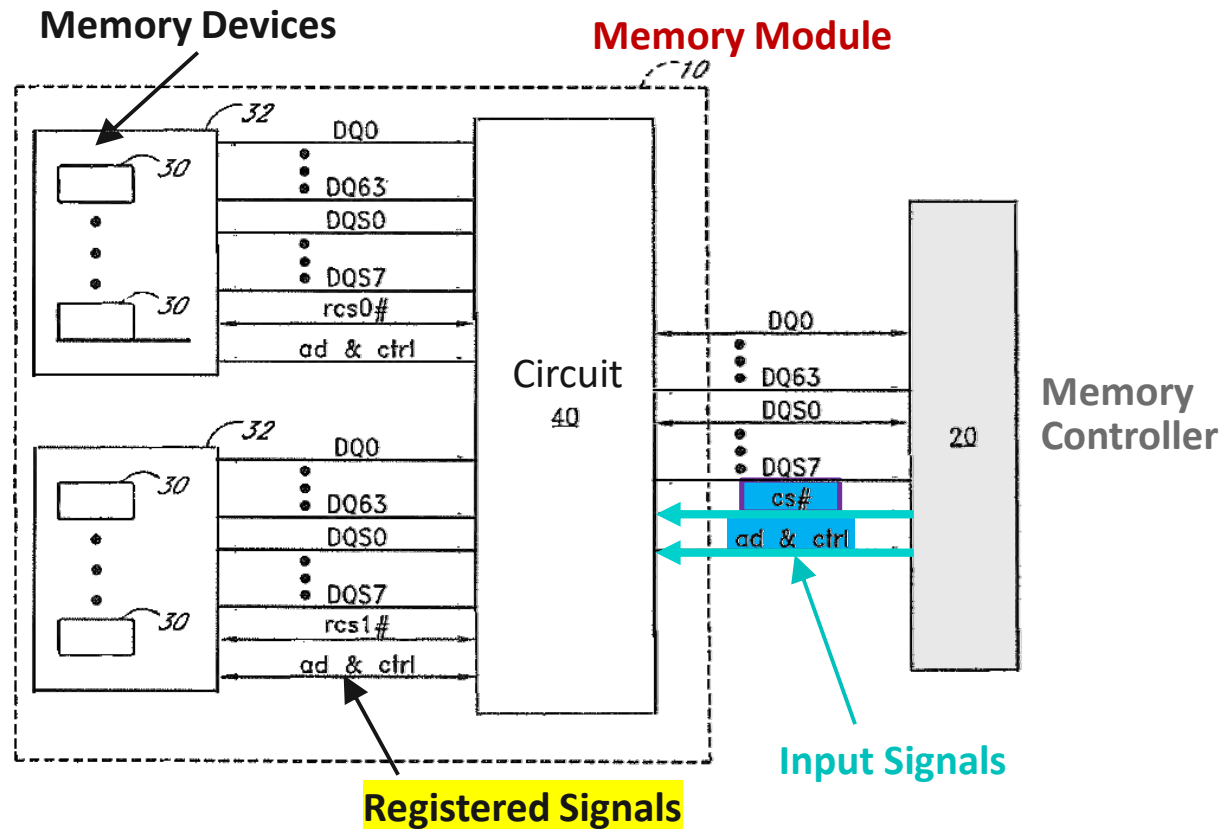


FIG. 1

logic coupled to the printed circuit board and configurable to receive a set of **input address and control signals** associated with a read or write memory command **via the address and control signal lines** and to output a set of registered address and control signals in response to the set of input address and control signals, the set of **input address and control signals including a plurality of input chip select signals and other input address and control signals**, the plurality of input chip select signals including one chip select signal having an active signal value and one or more other input chip select signals each having a non-active signal value, the set of registered address and control signals including a plurality of registered chip select signals corresponding to respective ones of the plurality of input chip select signals and other registered address and control signals corresponding to respective ones of the other input address and control signals, the plurality of registered chip select signals including one registered chip select signal having an active signal value and one or more other registered chip select signals each having a non-active signal value,

“Registered” Signals Provided by Logic to the Memory Devices

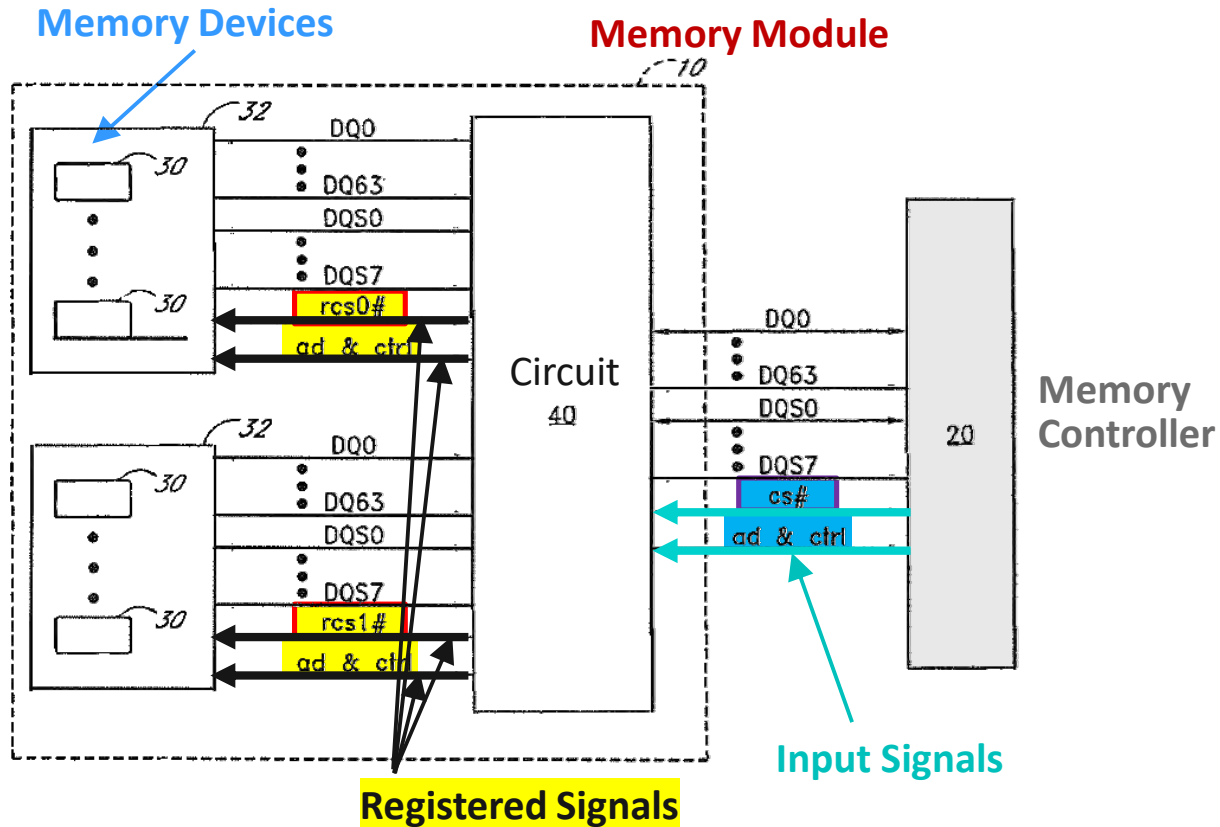


FIG. 1

logic coupled to the printed circuit board and configurable to receive a set of input address and control signals associated with a read or write memory command via the address and control signal lines and **to output a set of registered address and control signals in response to the set of input address and control signals**, the set of input address and control signals including a plurality of input chip select signals and other input address and control signals, the plurality of input chip select signals including one chip select signal having an active signal value and one or more other input chip select signals each having a non-active signal value, **the set of registered address and control signals including a plurality of registered chip select signals** corresponding to respective ones of the plurality of **input chip select signals** and **other registered address and control signals** corresponding to respective ones of the **other input address and control signals**, **the plurality of registered chip select signals including one registered chip select signal having an active signal value and one or more other registered chip select signals each having a non-active signal value**,

Memory Devices = Memory Chips on a Module

Perego Figures 3C, 4A

Memory module includes:

- memory devices
- primary link/channel
- secondary channel

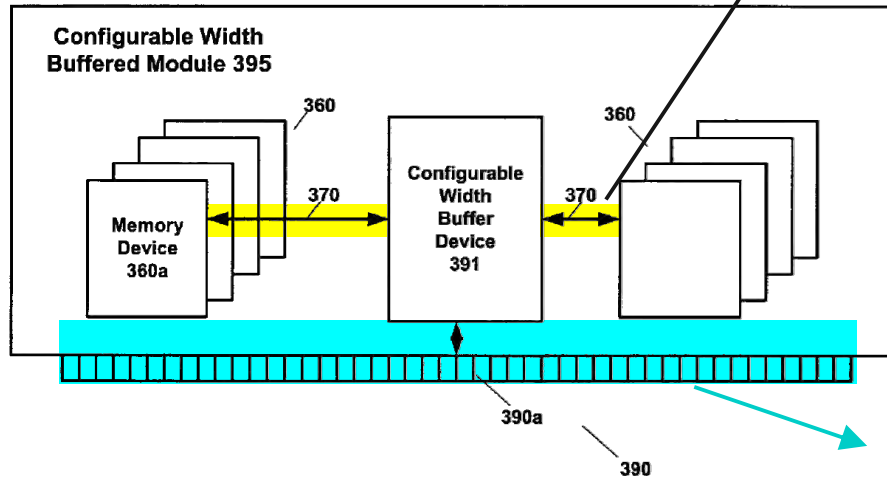


Fig. 3C

Secondary Channels
Between Buffer and
Memory Devices
Communicating
"Registered Signals"

Primary Links/Channels
Between Host
and Buffer
Communicating
"Input Signals"

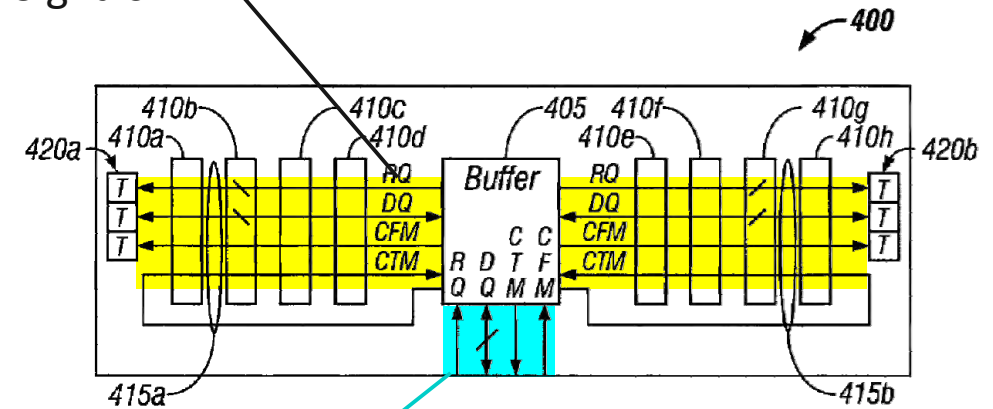
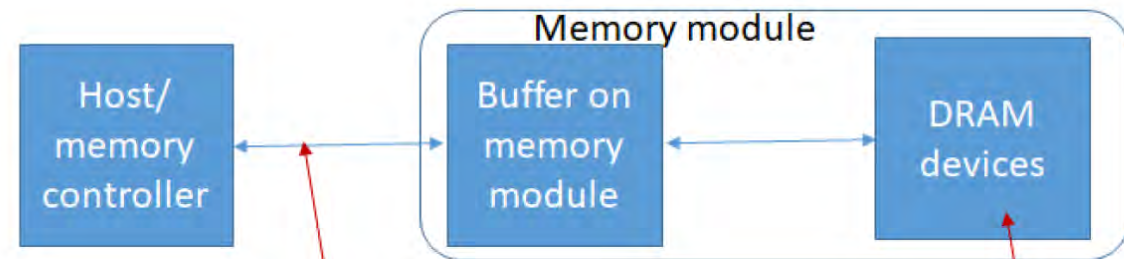


FIG. 4A

Using JEDEC-Style Memory Devices Affects Only the Secondary Channel

Perego

- Describes forward- and backward-compatibility with different types of memory devices
- Does **NOT** describe different types of primary links

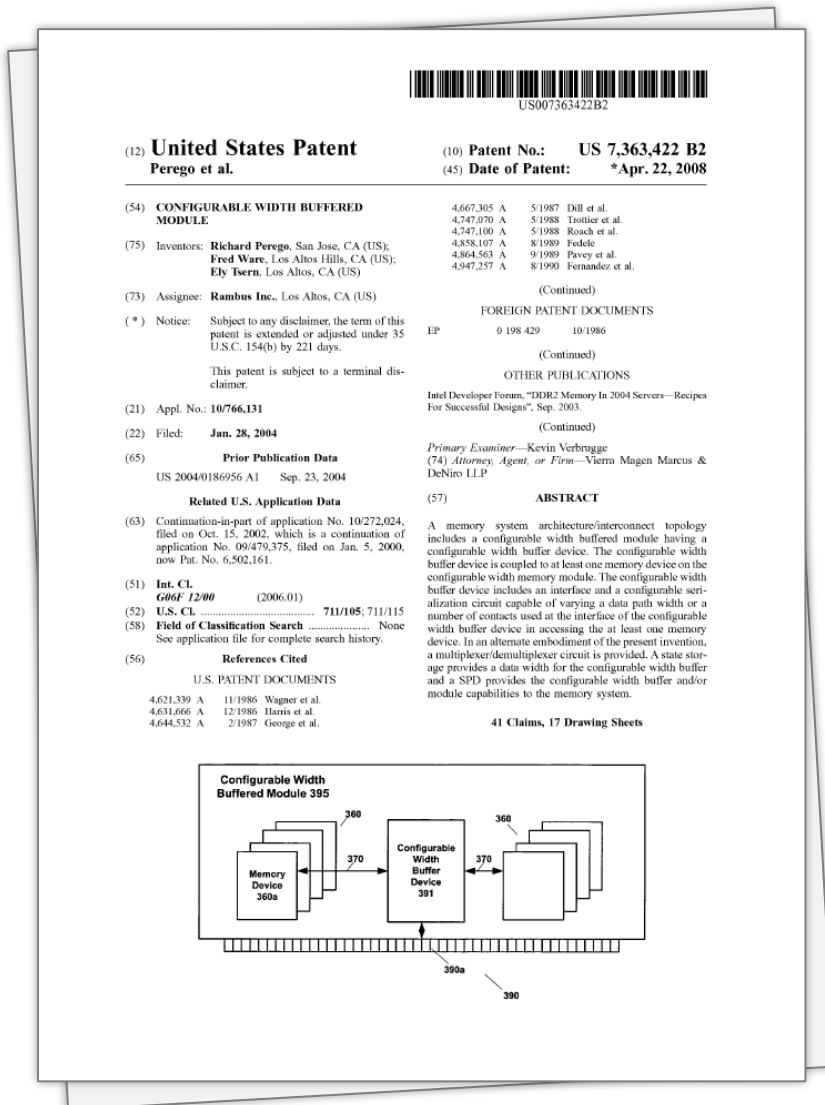


Not JEDEC-style

- Input signals not JEDEC

May use DDR2 or RDRAMs

- “Registered” signal may be JEDEC



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Prior Art Memory System # 1

(12) United States Patent
Solomon et al.

(10) Patent No.: US 11,093,417 B2
(45) Date of Patent: Aug. 17, 2021

With reference to FIG. 1, a representational block diagram of a conventional memory system employing memory modules is illustrated. Memory system 100 includes memory controller 110 and modules 120a–120c. Memory controller 110 is coupled to modules 120a–120c via control/address bus 130, data bus 140, and corresponding module control lines 150a–150c. Control/address bus 130 typically comprises a plurality of address lines and control signals (e.g., RAS, CAS and WE).

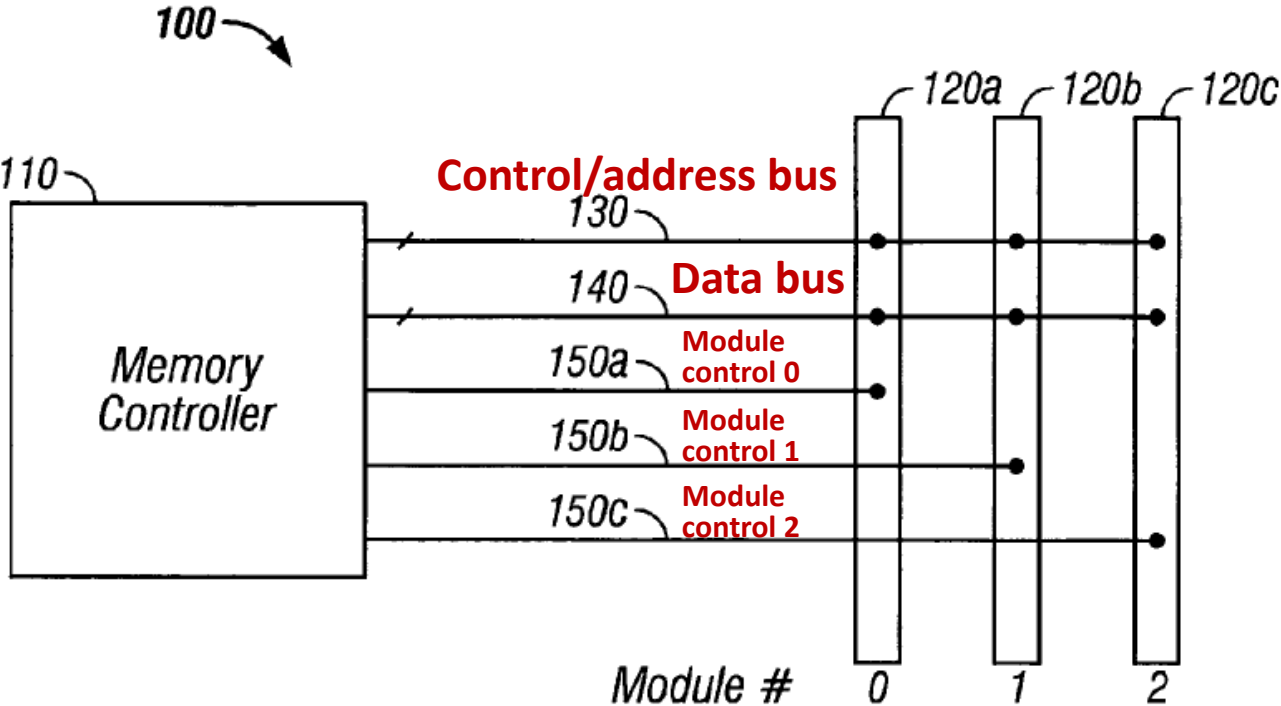
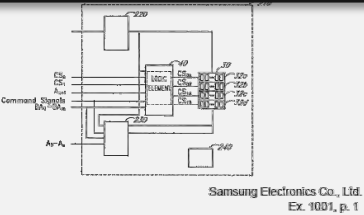


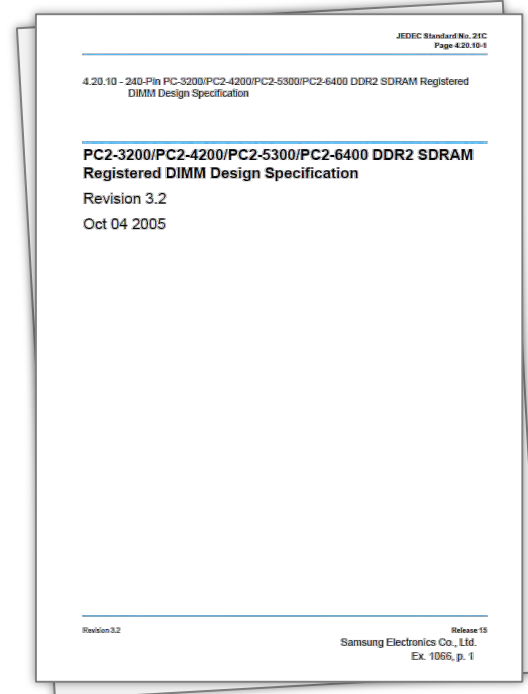
FIG. 1
(Prior Art)

JEDEC-Compliant Memory Modules

JESD21-C

- **Not** Packetized
- **Must Include** Chip Select Input Lines, Among Others

Pin Name	Description	Number	Pin Name	Description	Number
CK0	Clock Input, positive line	1	ODT[1:0]	On Die Termination Inputs	2
$\overline{\text{CK0}}$	Clock input, negative line	1	DQ[63:0]	Data Input/Output	64
CKE[1:0]	Clock Enables	2	CB[7:0]	Data check bits Input/Output	8
$\overline{\text{RAS}}$	Row Address Strobe	1	DQS[8:0]	Data strobes	9
$\overline{\text{CAS}}$	Column Address Strobe	1	$\overline{\text{DQS}}$ [8:0]	Data strobes, negative line	9
$\overline{\text{WE}}$	Write Enable	1	DM[8:0]/DQS[17:9]	Data Masks / Data strobes	9
$\overline{\text{S}}$ [3:0]	Chip Selects	4	$\overline{\text{DQS}}$ [17:9]	Data strobes, negative line	9
A[9:0],A[15:11]	Address Inputs	15	RFU	Reserved for Future Use	2
A10/AP	Address Input/Autoprecharge	1	NC	No Connect	1
BA[2:0]	SDRAM Bank Addresses	3	TEST	Memory bus test tool (Not Connected and Not Useable on DIMMs)	1
SCL	Serial Presence Detect (SPD) Clock Input	1	V_{DD}	Core Power	11
SDA	SPD Data Input/Output	1	V_{DDQ}	I/O Power	11
SA[2:0]	SPD Address Inputs	3	V_{SS}	Ground	64
Par_In	Parity bit for the Address and Control bus	1	V_{REF}	Input/Output Reference	1
$\overline{\text{Err_Out}}$	Parity error found on the Address and Control bus	1	V_{DDSPD}	SPD Power	1
$\overline{\text{RESET}}$	Register and PLL control pin	1	total		240



Need for High Bandwidth Memory System

(12) **United States Patent**
Perego et al.

(10) **Patent No.:** US 7,363,422 B2
(45) **Date of Patent:** *Apr. 22, 2008

(54) **CONFIGURABLE WIDTH BUFFERED MODULE**

(75) **Inventors:** Richard Perego, San Jose, CA (US); Fred Ware, Los Altos Hills, CA (US); Ely Ysern, Los Altos, CA (US)

(73) **Assignee:** Rambus Inc., Los Altos, CA (US)

(*) **Notice:** Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(o) by 221 days.

This patent is subject to a terminal disclaimer.

(21) **Appl. No.:** 10/766,131

(22) **Filed:** Jan. 28, 2004

(65) **Prior Publication Data**
US 2004/0186956 A1 Sep. 23, 2004

Related U.S. Application Data

(63) **Continuation-in-part of application No. 10/272,024, filed on Oct. 15, 2002, which is a continuation of application No. 09/470,375, filed on Jan. 9, 2000, now Pat. No. 6,502,161.**

(51) **Int. Cl.**
G06F 12/00 (2006.01)

(52) **U.S. Cl.**
711/105, 711/115

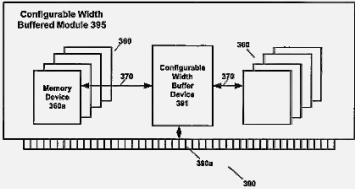
(58) **Field of Classification Search**
None

(56) **References Cited**

U.S. PATENT DOCUMENTS

4,631,239 A 11/1986 Wagner et al.
4,631,666 A 12/1986 Harris et al.
4,644,532 A 2/1987 George et al.

41 Claims, 17 Drawing Sheets



Samsung Electronics Co., Ltd.
Ex. 1071, p. 1

There is a need for memory system architectures or interconnect topologies that provide flexible and cost effective upgrade capabilities while providing high bandwidth to keep pace with microprocessor operating frequencies.

Perego's Solution for a High Bandwidth Memory System

A dynamic point-to-point topology may also be employed to connect the memory subsystem port to each of the memory subsystems. A dynamic point-to-point topology includes a first plurality of point-to-point connections between the memory controller and a first memory module and a second plurality of point-to-point connections between the memory controller and the second memory module in a first configuration. For example, when the second memory module is removed from the system and a second configuration is desired, the plurality of point-to-point connections are routed to the first memory module to retain system bandwidth between memory modules and the controller or increase the bandwidth to the first memory module. The routing may be performed in a number of ways including using a continuity module or switches. In an embodiment, a configurable width buffer device disposed on the first memory module provides the flexibility to configure the width of the first memory module to accept switch between the first and second configurations. That is the configurable width buffer device may provide the flexibility to configure the module to connect to the first plurality of point-to-point connections in the first configuration and to connect to the second plurality of point-to-point links in the second configuration.

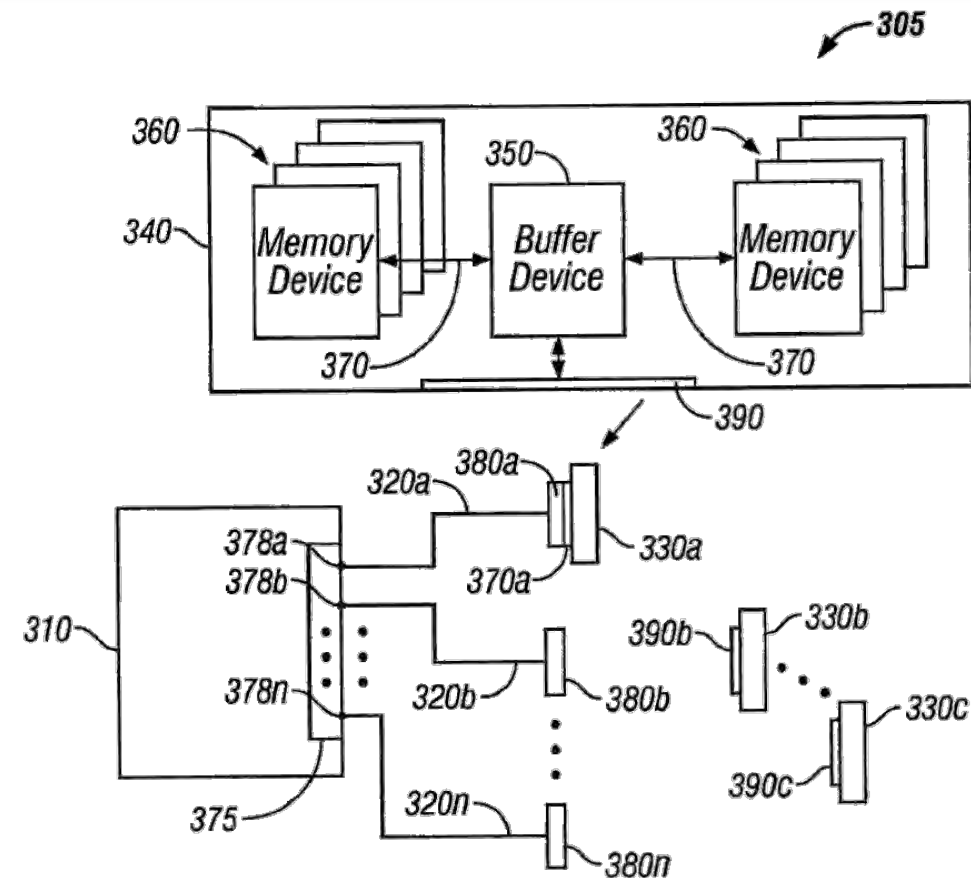
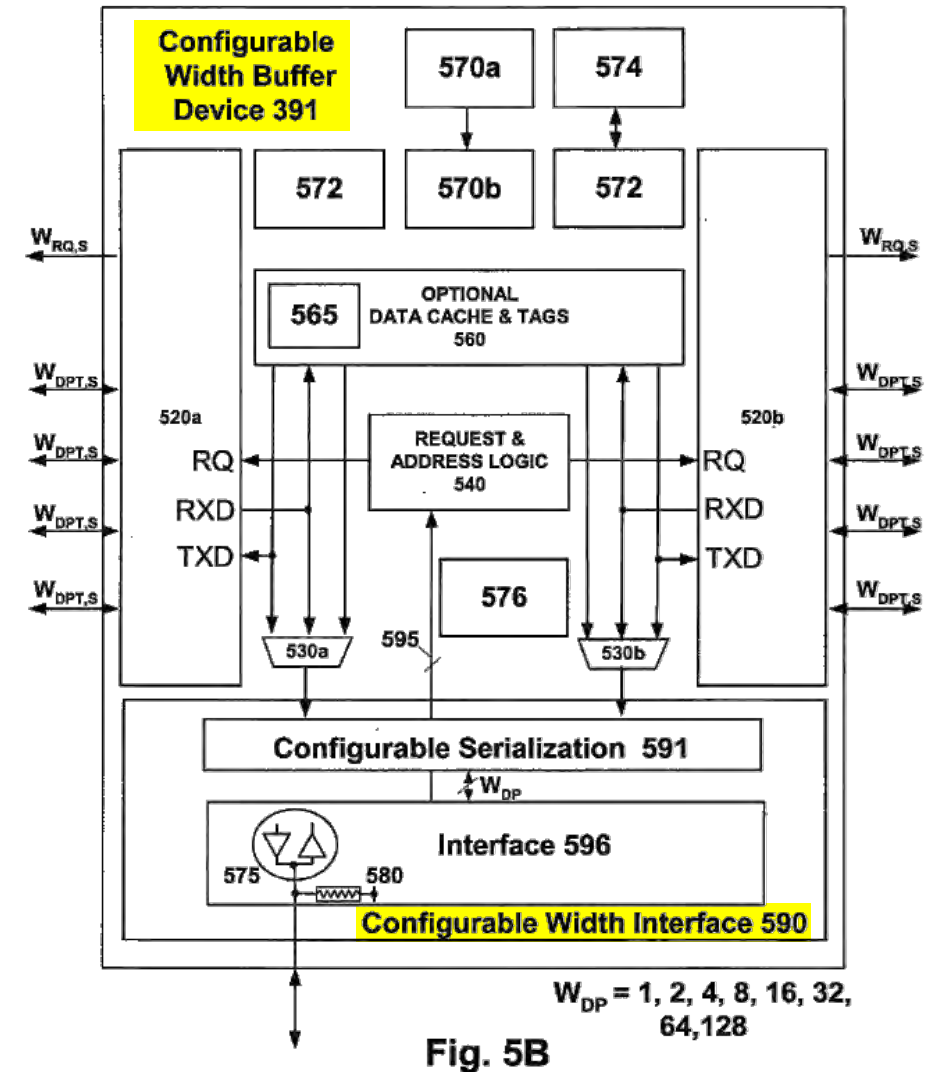


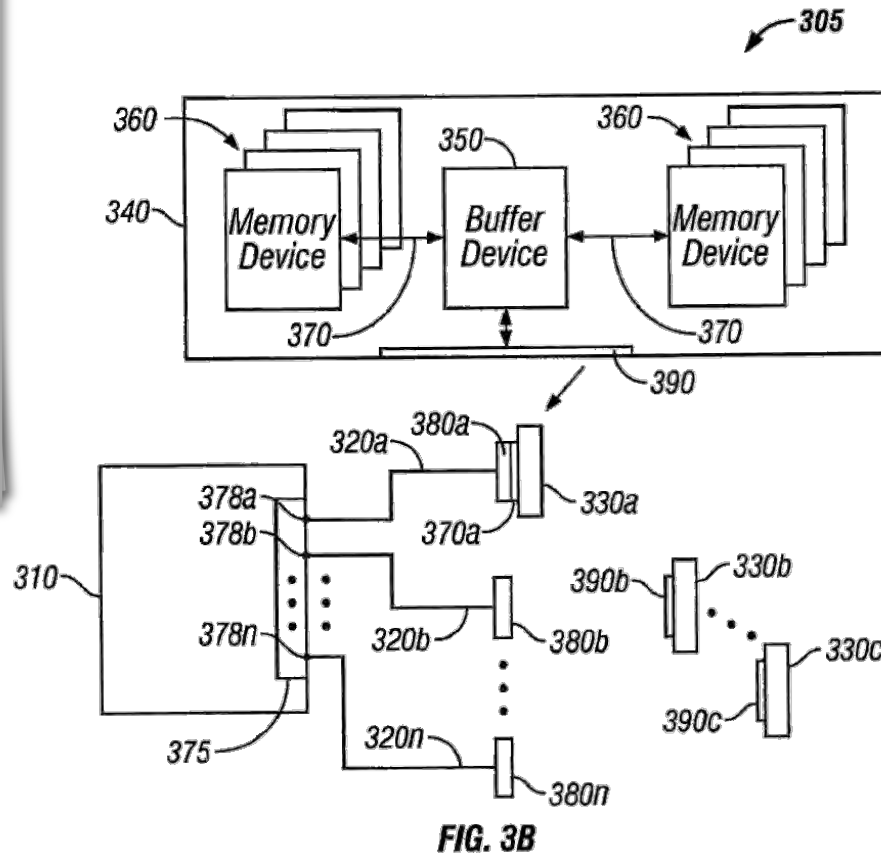
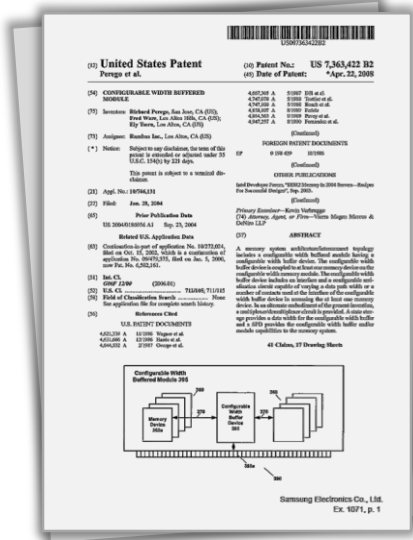
FIG. 3B

Dynamic Point-to-Point Topology Enabled by Configurable Width Buffer Device

A **dynamic point-to-point topology** may also be employed to connect the memory subsystem port to each of the memory subsystems. A dynamic point-to-point topology includes a first plurality of point-to-point connections between the memory controller and a first memory module and a second plurality of point-to-point connections between the memory controller and the second memory module in a first configuration. For example, when the second memory module is removed from the system and a second configuration is desired, the plurality of point-to-point connections are routed to the first memory module to retain system bandwidth between memory modules and the controller or increase the bandwidth to the first memory module. The routing may be performed in a number of ways including using a continuity module or switches. In an embodiment, a **configurable width buffer device** disposed on the first memory module provides the flexibility to configure the width of the first memory module to accept switch between the first and second configurations. That is the **configurable width buffer device** may provide the flexibility to configure the module to connect to the first plurality of point-to-point connections in the first configuration and to connect to the second plurality of point-to-point links in the second configuration.



Perego's High Bandwidth Memory System



- Fig. 3B shows “an exemplary system that uses configurable width modules coupled in a dynamic point-to-point configuration”
- Memory subsystems 330a-c are each a buffered memory module with a configurable width interface
- Point-to-point links 320b-320n coupled to unpopulated mating connectors 380b-n are “routed to access the single buffered memory module located in mating connector 380a”
- Module in connector 380a “programmed to include an interface width that may accommodate the routed point-to-point links 320b-320n”
- U.S. App. No. 09/797,099 (incorporated by reference) provides more implementation details (issued as U.S. Patent No. 7,610,447 (EX2034))

Perego Uses Addresses to Select Target Channels

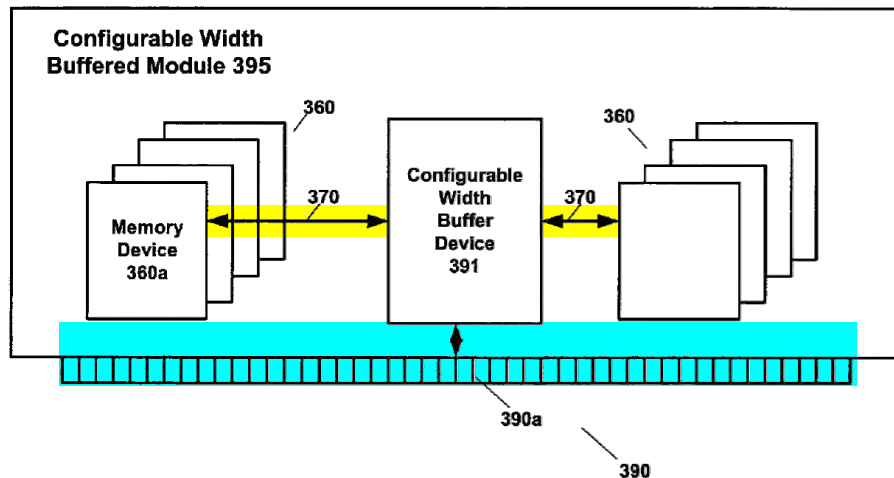


Fig. 3C

Configurable serialization circuit **591** performs serialization and deserialization functions depending upon the desired serialization ratio as defined above. As the memory device access width is reduced from its maximum value, memory device access granularity (measured in quanta of data) is commensurately reduced, and an access interleaving or multiplexing scheme may be employed to ensure that all storage locations within memory devices **360** can be accessed. The number of signal lines of channels **370** may be increased or decreased as the memory device access width changes. Channels **370** (FIG. 3C) may be subdivided into several addressable subsets. The address of the transaction will determine which target subset of channels **370** will be utilized for the data transfer portion of the transaction. In addition, the number of transceiver circuits included in interface **520a** and **520b** that are employed to communicate with one or more memory devices may be configured based on the desired serialization ratio. Typically, configuration of the transceivers may be effectuated by enabling or disabling how many transceivers are active in a given transfer between one or more memory devices and configurable width buffer device **391**.

Perego Can Select Any Target Channel Sets with Address Signals

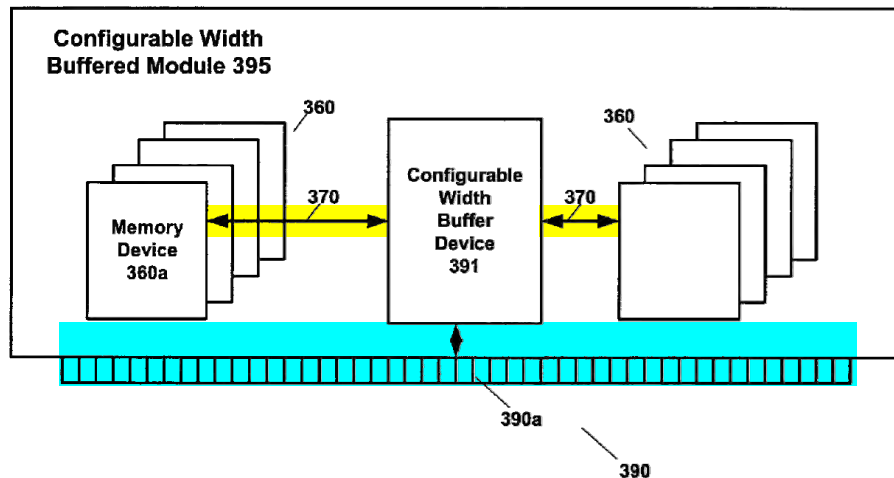


Fig. 3C

If the total number of secondary channel signal lines per configurable width buffer device **391**, $W_{DP,S}$ is greater than the minimum number required per transaction, $W_{DPT,S}$, then configurable width buffer device **391** may employ a configurable datapath router within interface **591** to route requests between the primary channel and the target subset of secondary channel signal lines for each transaction. According to a preferred embodiment, the target subset of secondary channel signal lines may be selected via address bits provided as part of the primary channel request. By accessing a subset of secondary channel signal lines per transaction, a number of benefits may be derived. One of these benefits is reduced power consumption. Another benefit is higher performance by grouping memory devices into multiple independent target subsets (i.e. more independent banks).

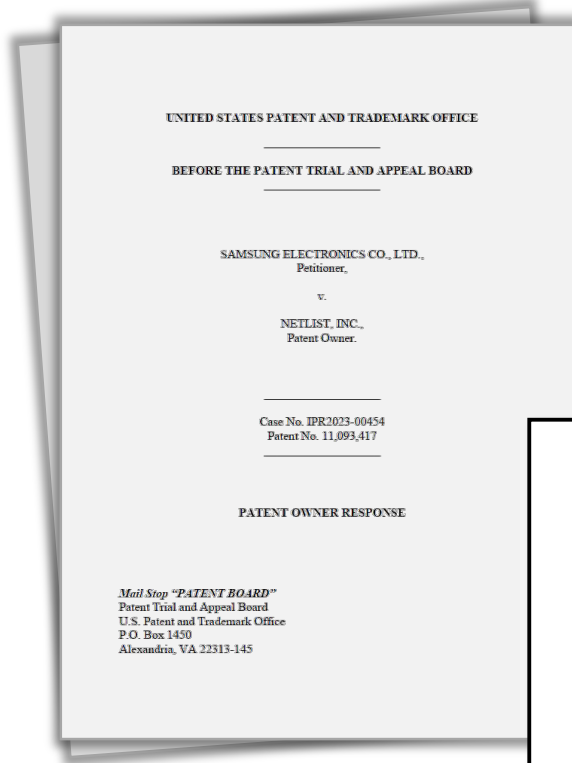
Patent Owner Netlist Outline

1. The '417 and '215 Patents
2. All of Petitioner's Grounds are Deficient
3. The Netlist Claims are Directed to Memory Modules
4. Perego vs. JEDEC-Compliant Memory Architectures
- 5. Ground 1: Perego and JESD79-2**
6. Ground 2: Ground 1 + Ellsberry
7. Ground 3: Ground 1 + Halbert

No Claim Construction Disputes

Netlist Applied Petitioner's Proposed Construction of "Rank"

- Solely for purposes of these IPRs

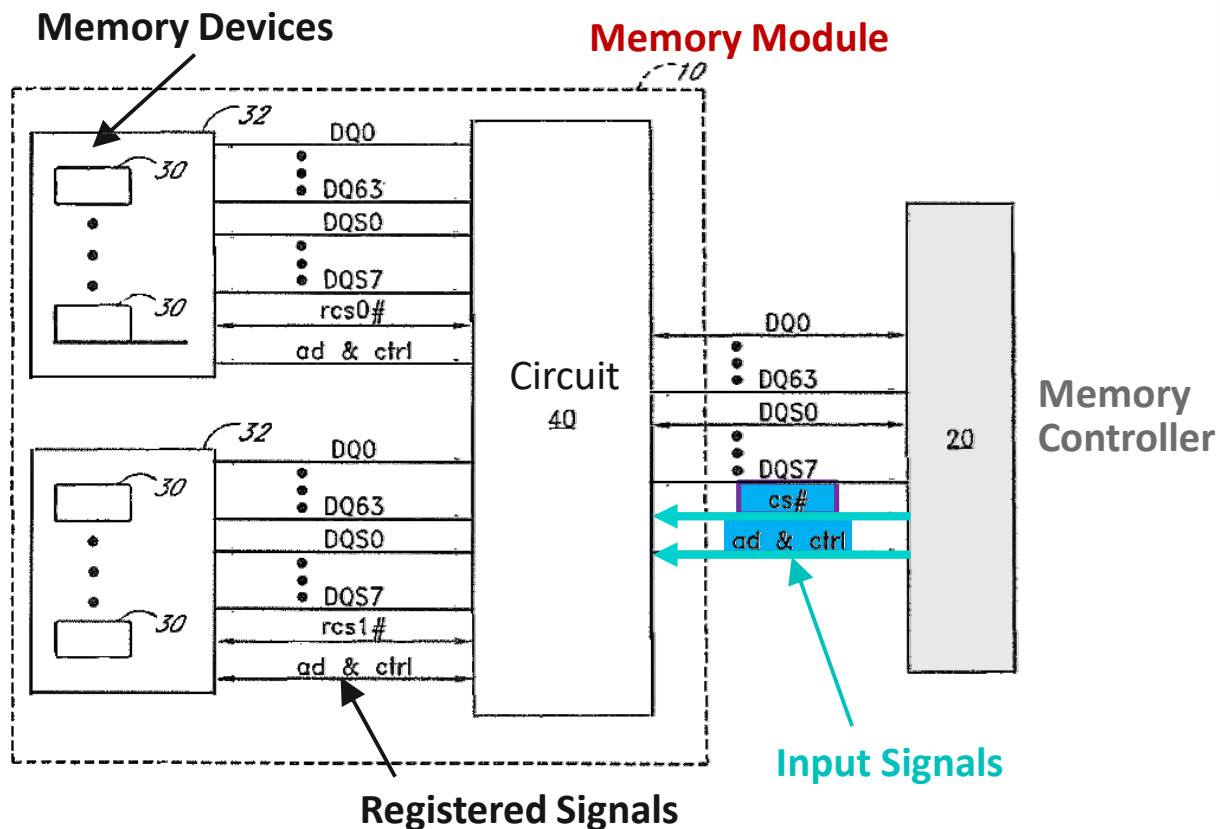


Solely for purposes of responding to this Petition, however, Netlist applies Petitioner's proposed construction: "an independent set of one or more memory devices on a memory module that act together in response to command signals, including chip-select signals, to read or write the full bit-width of the memory module." Pet. 26; *cf. SAS Inst., Inc. v. Iancu*, 138 S. Ct. 1348, 1355 (2018) ("[I]n an inter partes review the petitioner is master of its complaint....").

Ground 1: Perego and JESD79-2

1. Perego and JESD79-2 **do not disclose or suggest** input “chip select signals”
2. No motivation to modify Perego to add input chip selects as Petitioner proposed
3. Perego and JESD79-2 do not disclose or suggest the CAS-latency claim elements
4. Perego and JESD79-2 do not disclose or suggest a plurality of “ranks”

Missing Limitation #1 in '417 Patent: Input Chip Select Signals



1. A memory module operable in a computer system to communicate data with a memory controller of the computer system via a N-bit wide memory bus in response to read or write memory commands received from the memory controller, the memory bus including address and control signal lines and data signal lines, the memory module comprising:

logic coupled to the printed circuit board and configurable to receive a set of input address and control signals associated with a read or write memory command via the address and control signal lines and to output a set of registered address and control signals in response to the set of input address and control signals, the set of input address and control signals including a plurality of input chip select signals and other input address and control signals, the plurality of input chip select signals including one chip select signal having an active signal value and one or more other input chip select signals each having a non-active signal value, the set of registered address and control signals including a plurality of registered chip select signals corresponding to respective ones of the plurality of input chip select

Input
to the
Claimed
Memory
Module

Missing Limitation #1 in '215 Patent: Input Chip Select Signals

1. A **memory module** operable in a computer system to communicate data with a memory controller of the computer system via a memory bus in response to memory commands received from the memory controller, the memory commands including a first memory command and a subsequent second memory command, the first memory command to cause the memory module to receive or output a first data burst and the second memory command to cause the memory module to receive or output a second data burst, the memory module comprising:

- a printed circuit board having a plurality of edge connections configured to be electrically coupled to a corresponding plurality of contacts of a module slot of the computer system;
- a register coupled to the printed circuit board and configured to receive and buffer **first command and address signals** representing the **first memory command**, and to receive and buffer **second command and address signals** representing the **second memory command**;

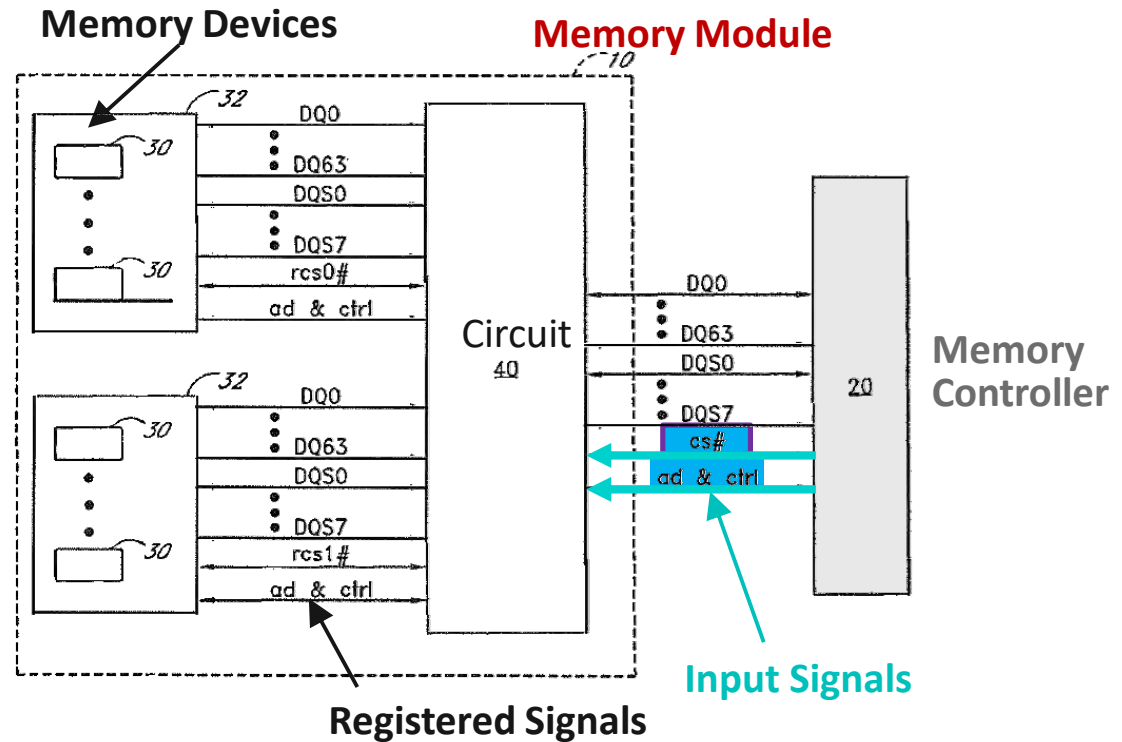


FIG. 1

9. The memory module of claim 1, wherein the first **memory command** includes at least one **first chip select signal** and the **second memory command** includes at least one **second chip select signal**.

Input to the Claimed Memory Module

No Assertion That Perego Discloses Receiving Chip Select Signals from Host

Petition

Ground 1 teaches “the set of input address and control signals [from [1.c.1] (pp.43-51)] including a plurality of input chip select signals [e.g., “CS” signals as part of the input read or write command from the memory controller, as required by JESD79-2, EX1064, pp.6 (first below), 24-33, 49 (second below)] *and other input address and control signals* [e.g., bank and row/column address signals (e.g., BA0-BA2, A0-A15), and RAS, CAS and WE control signals, as part of the input read or write command from the memory controller, as required by JESD79-2, EX1064, pp.6 (first below), 24-33, 49 (second below)], *the plurality of input chip*

Pet. 51-52

DDR2 SDRAM SPECIFICATION

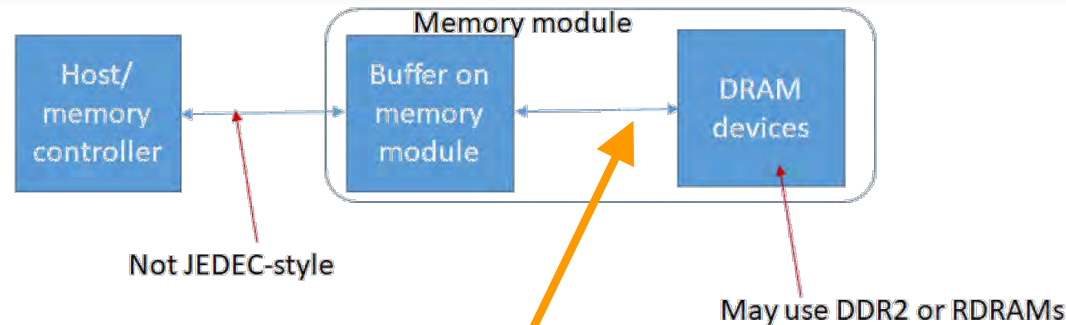
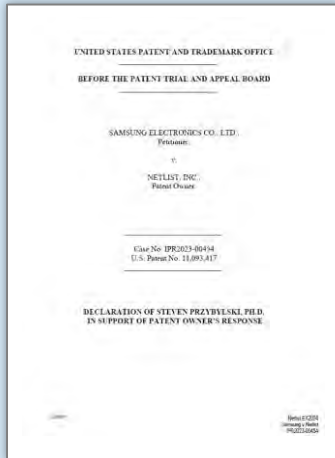
JESD79-2 Describes JEDEC-Compliant Memory *Devices*, **NOT** Claimed “Memory Module[s]”



JESD79-2

- JEDEC DDR2 Standard for Synchronous Dynamic Random Access Memory (SDRAM)
- Describes individual memory devices
- Does **NOT** describe memory modules

JESD79-2 Does NOT Define JEDEC Primary Bus or Modules



115. JESD79-2 is a DRAM (i.e., memory device) standard. It is not a module standard. As such, it does not define any memory bus (or signals therein) between a module and a memory controller or any characteristics or features of any buffer or register devices on a module. Other documents ratified by the JEDEC council relate to modules of different types and capabilities, some of which rely on the use of JEDEC-compliant memory devices.

Steven Przybylski, Ph.D.
Expert Witness



Perego Uses Address Bits to Select Target Devices

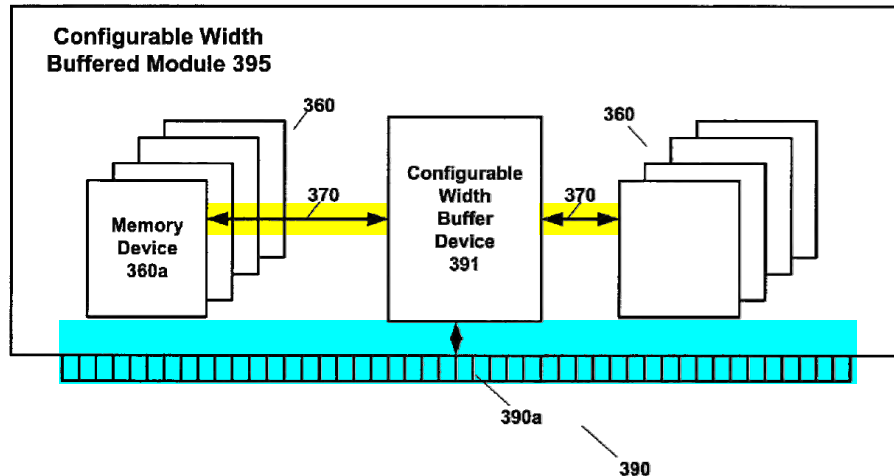


Fig. 3C

If the total number of secondary channel signal lines per configurable width buffer device **391**, $W_{DP,S}$ is greater than the minimum number required per transaction, $W_{DPT,S}$, then configurable width buffer device **391** may employ a configurable datapath router within interface **591** to route requests between the primary channel and the target subset of secondary channel signal lines for each transaction. According to a preferred embodiment, the target subset of secondary channel signal lines may be selected via address bits provided as part of the primary channel request. By accessing a subset of secondary channel signal lines per transaction, a number of benefits may be derived. One of these benefits is reduced power consumption. Another benefit is higher performance by grouping memory devices into multiple independent target subsets (i.e. more independent banks).

Perego Uses Addresses to Select Target Subsets of Channels/Devices

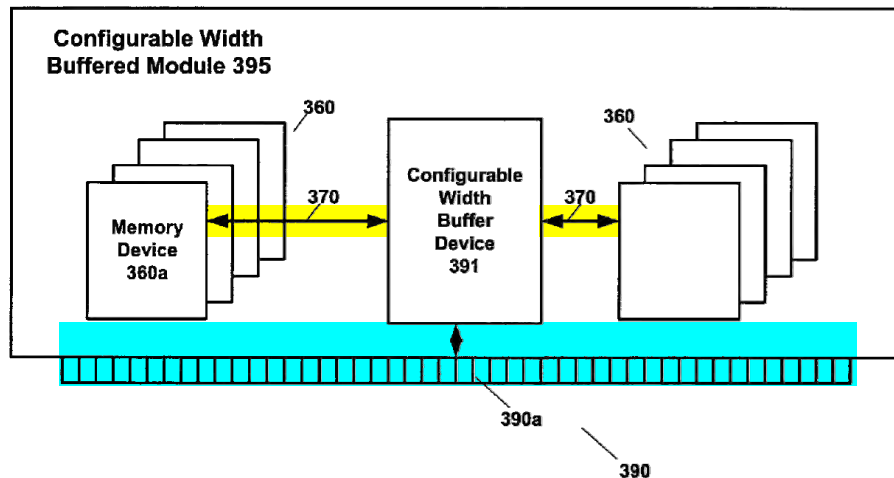
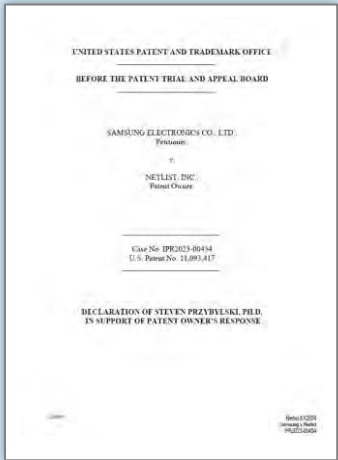


Fig. 3C

Configurable serialization circuit **591** performs serialization and deserialization functions depending upon the desired serialization ratio as defined above. As the memory device access width is reduced from its maximum value, memory device access granularity (measured in quanta of data) is commensurately reduced, and an access interleaving or multiplexing scheme may be employed to ensure that all storage locations within memory devices **360** can be accessed. The number of signal lines of channels **370** may be increased or decreased as the memory device access width changes. Channels **370** (FIG. 3C) may be subdivided into several addressable subsets. The address of the transaction will determine which target subset of channels **370** will be utilized for the data transfer portion of the transaction. In addition, the number of transceiver circuits included in interface **520a** and **520b** that are employed to communicate with one or more memory devices may be configured based on the desired serialization ratio. Typically, configuration of the transceivers may be effectuated by enabling or disabling how many transceivers are active in a given transfer between one or more memory devices and configurable width buffer device **391**.

No Chip Select Signals in Rambus Systems



Steven Przybylski, Ph.D.
Expert Witness



47. Finally, the addressing paradigm is different for Direct RDRAMs than for any of the JEDEC-Standardized SDRAMs. For JEDEC-Standardized SDRAM devices, the chip select signal, CS, which is part of the command bus, is used to identify which devices are going to respond to a command. Direct RDRAMs do not have a chip select signal. Instead, each device on the channel is given a unique identifier during initialization. All command packets include a 5 bit device identifier to identify which singular DRAM on the channel is to respond to the command. As Jacob puts it, the information that determines which devices will respond to a command—what he dubs the chip-select information— "travel(s) over the same set of electrical wires but at different times." Direct Rambus channels do not use dedicated address, control, data and chip-select signals. Ex. 1069, p. 7. Therefore, there are no chip-select signals as the term would be understood by a POSITA in either the Direct RDRAM or the XDR

RDRAM architectures. The passages quoted by the Board from Ex. 1069 (Paper 11, at 14) say that the original RDRAM includes chip-select information. This is not accurate. The original RDRAM being described in these paragraphs included only an address field in the command packets and did not have any dedicated fields that a POSITA would consider as chip-select information or chip-select signals as shown below.

Bus Data									
Bus Cntl	8	7	6	5	4	3	2	1	0
Start	Op0	Addr9..2							
Op1	Op3	Addr17..10							
OpX1	Addr26..18								
Op2	Addr35..27								
OpX2	Rsrv		Count6,4,2			Rsrv			
Close/Rsrv	Rsrv		Count7,5,3			Count1,0		Addr1,0	

Figure 8-8 A Rambus Request Packet takes 12 ns on the bus.

No “Chip Select Information” in Rambus Systems

Institution Decision

the JEDEC DDR2 SDRAM Specification. Ex. 1064, 1 (cover page). As to Patent Owner’s argument that Rambus memories lack a chip select network (Prelim. Resp. 37), the reference on which Patent Owner relies discloses that chip select information is still used in the particular Rambus devices described. See Ex. 1069, 11 (“[I]n the Rambus bus organization, all addresses, commands, data, and chip-select information are sent on the same bus lines.”), 12 (“[T]he example system uses a total of nine (9) lines to carry all necessary information, including addresses, commands, chip-select information, and data.”). Thus, on this record, Patent Owner’s focus on the lack of a chip select network, which is not recited in the claims of the ’417 patent, appears misplaced. We address Patent Owner’s more specific arguments below in the discussion of individual claim recitations.

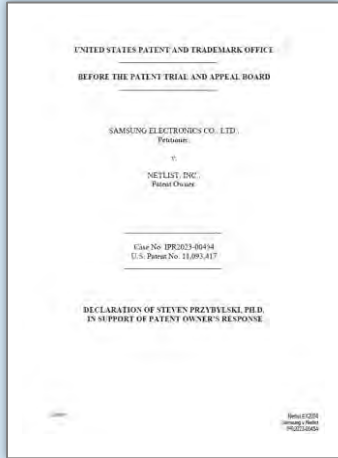
Institution Decision 14

Dr. Przybylski

- Description in EX1069, section 1.3.2 on chip select information is not accurate
- “I think the person of ordinary skill that did happen to know about the original RDRAMs would recognize that ***there's no chip-select information in that architecture, that everything is address-based.***”

EX1095 (Dep. Tr.), 206:12-207:13

All Device Selection Done Through Address Bits

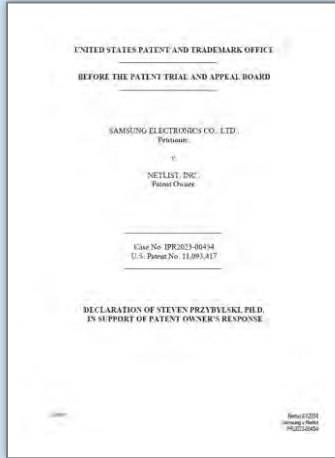


Steven Przybylski, Ph.D.
Expert Witness



- Q. When you say everything address-based, there are certain address signals that select the chip?
- A. As we saw it when we looked at the RDRAM data sheet that was attached to my book, we saw that the register defined the base address of -- that a particular RDRAM would respond to.
Do you remember that?
- Q. Yes.
- A. Okay. So the -- *there is no chip-select-select signal* as it exists in any of the JEDEC standardized memory devices; instead, there is *only* the -- *the memory controller throws the address out there. And whichever RDRAM matches the address or the -- that the accessed address is within the range of that RDRAM, that RDRAM says, oh, it's for me*; I'm going to do something. So *there's no chip-select signal*, and there's no chip-select information per se in the command packet for that generation of RDRAM.

Address and Chip Selects Are Different



Steven Przybylski, Ph.D.
Expert Witness

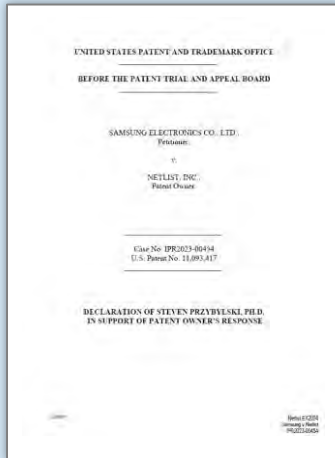


“But they're [memory devices are] also autonomous in that the memory devices determine when to respond to the request. *And there is a profound conceptual difference between an address and the chip-select.* And you see that pervasively throughout the JEDEC standardization -- standards for SDRAMs and for all other devices that have chip-select inputs. They were conceptually and temporally -- not -- they are conceptually different from addresses.

“In this case, for the RDRAMs being described in this paragraph, there are no chip-select signals; there's no chip-select signal lines. *The memory controller, when it's sending out an address as part of a packet, a command packet, it's not even cognizant of which memory is going to respond, because that's handled a priori in the programming of the registers.*

“So the whole concept of chip-select is dramatically different in this generation of RDRAMs.”

No Input Chip Select Signals in Perego



Steven Przybylski, Ph.D.
Expert Witness



113. There is one important consequence of this independence of the memory device type that is especially relevant to the present proceeding: there are no ranks as the term is generally understood by a POSITA and no chip select signals on the primary channel. Because the memory system can include modules that include either Direct RDRAMs, which are not organized into ranks as, for example, DDR2 SDRAMs are, or include chip-select signals, as DDR2 SDRAMs it does not make sense to include this concept or these signal into the primary channel. Indeed, since the end of each point-to-point channel 320 is a single module, and the memory locations in each module are identified purely by address bits, chip select signals are entirely superfluous. Indeed, all of the descriptions of the embodiments of the primary channel do not mention chip selects. And, for example, the modules shown in Figure 2A use SDRAM, which receive chip select signals even though the Direct Rambus Channel on which the modules sit does not include any chip select signals. Therefore, a POSITA would understand that those CS signals to the SDRAMs were generated locally by the Memory Translator Hub (MTH) from the addressing information.

Perego Figures 4A & 4B Depict Rambus Direct RDRAM System with No Input Chip Select Signals from the Host

Perego

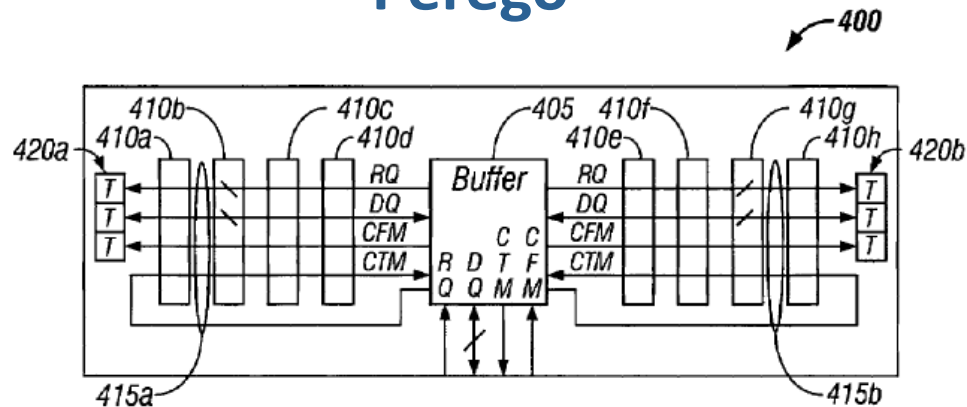


FIG. 4A

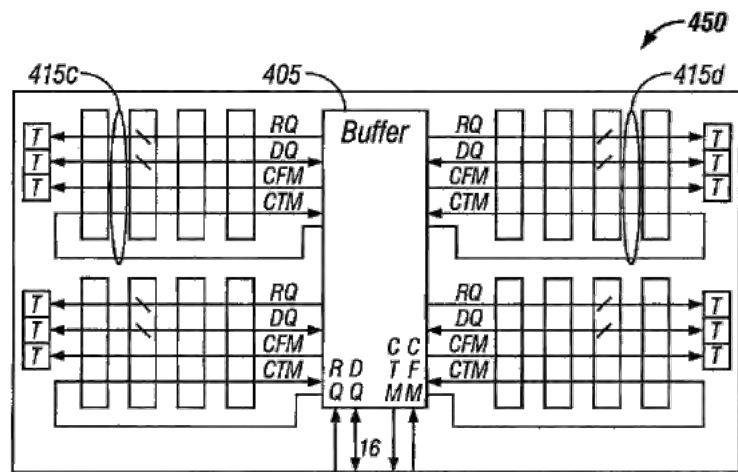


FIG. 4B

EX1071 (Perego), Figs. 4A, 4B

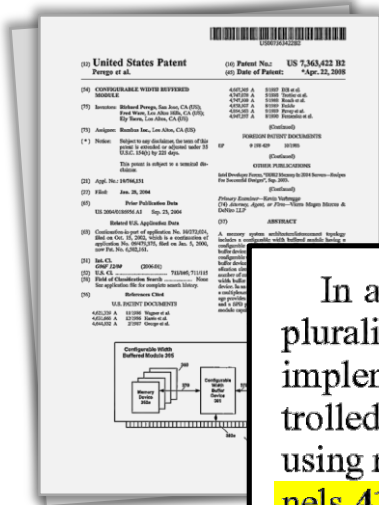
Rambus RIMMs

Steven Przybylski, Ph.D.
Netlist Expert Witness

device levels. Ex. 1071, 9:34-64, 10:63-67. Petitioner also notes that Figures 4A and 4B show RQ and QD lines connecting to the memory bus, but fails to note that in these embodiments, the primary channel includes not only RQ and DQ but clock signals CTM and CFM. Petition, p. 41 (citing Ex. 1071, 9:58-60, Figs. 4A, 4B). A POSITA would understand, as described above, that these signals are those of a Direct RDRAM channel. This is what is shown in the prior-art embodiment of Figure 2A where a single bus-structure Rambus Channel is used to connect high-bandwidth channels as described in the Direct RDRAM architecture. Ex. 2001, pp. 26-27. These bus embodiments for the primary

EX2024, ¶ 150

Alternative Embodiments Directed Solely to Secondary Channel



In an embodiment, channels 415a and 415b consist of a plurality of signal lines in a relatively short multi-drop bus implementation. The plurality of signal lines may be controlled impedance transmission lines that are terminated using respective termination elements 420a and 420b. Channels 415a and 415b are relatively short (i.e., are coupled to relatively few memory devices relative to a conventional memory system, for example see FIGS. 2A and 2B) and connect to an I/O interface (not shown) of each memory device via a short stub. Signal lines of channels 415a and 415b include control lines (RQ), data lines (DQ) and clock lines (CFM, CTM). The varieties of interconnect topologies, interconnect types, clocking methods, signaling references, signaling methods, and signaling apparatus described above in reference to point-to-point links 320a–320n may equally apply to channels 415a and 415b.

In accordance with an embodiment of the present invention, control lines (RQ) transport control (e.g., read, write, precharge . . .) information and address (e.g., row and column) information contained in packets. By bundling control and address information in packets, protocols required to communicate to memory devices 410a–410h are independent of the physical control/address interface implementation.

In alternate embodiments, control lines (RQ) may comprise individual control lines, for example, row address strobe, column address strobe, etc., and address lines. Individual point-to-point control and address lines increase the number of parallel signal connection paths, thereby increasing system layout resource requirements with respect to a narrow “packet protocol” approach. In one alternate embodiment illustrated in FIG. 6A, individual device select lines 633a and 633b are employed to perform device selection. Individual device select lines 633a and 633b decrease some latency consumed by decoding device identification that normally is utilized when multiple devices share the same channel and incorporate individual device identification values.

The Figure 6A Embodiment of Perego Confirms Alternate Embodiments Relate to Options on Secondary Channel

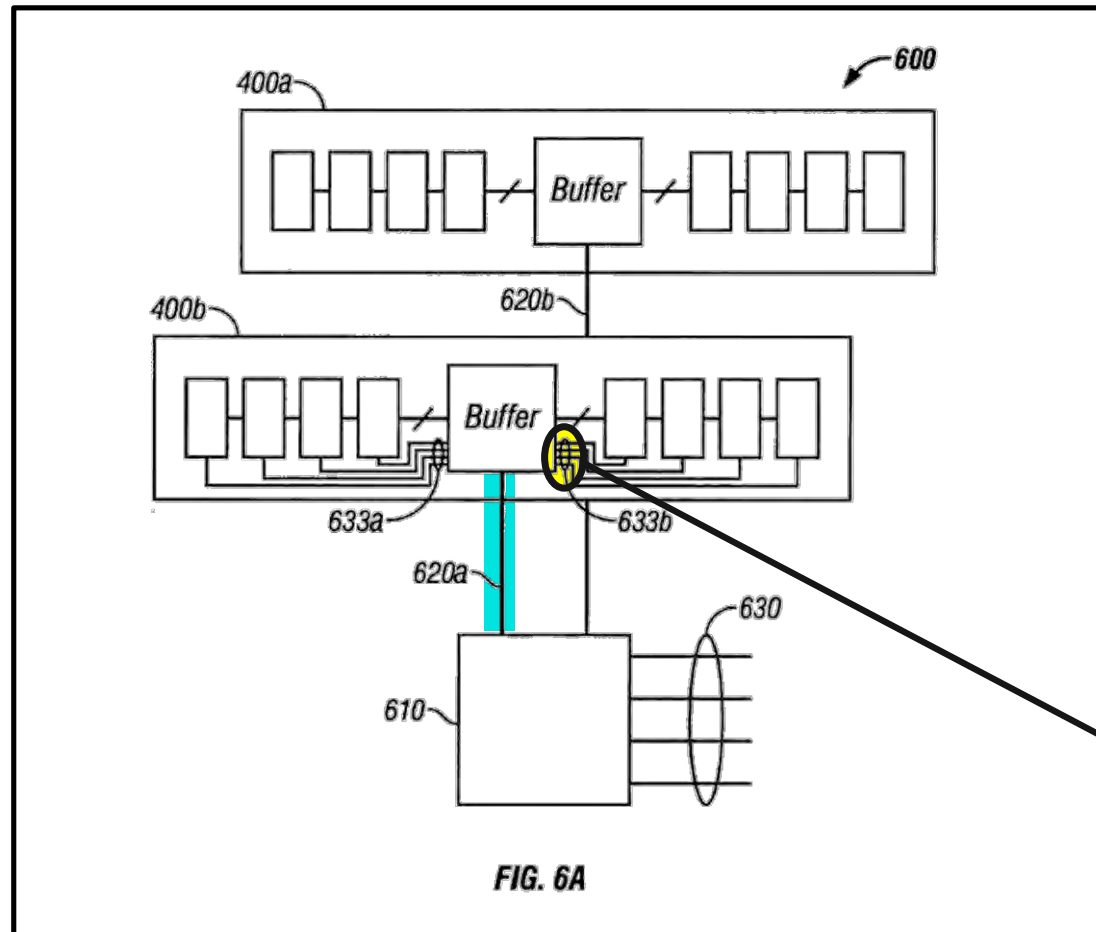


FIG. 6A

EX1071 (Perego), Fig. 6A

In alternate embodiments, control lines (RQ) may comprise individual control lines, for example, row address strobe, column address strobe, etc., and address lines. Individual point-to-point control and address lines increase the number of parallel signal connection paths, thereby increasing system layout resource requirements with respect to a narrow “packet protocol” approach. In one alternate embodiment illustrated in FIG. 6A, individual device select lines 633a and 633b are employed to perform device selection. Individual device select lines 633a and 633b decrease some latency consumed by decoding device identification that normally is utilized when multiple devices share the same channel and incorporate individual device identification values.

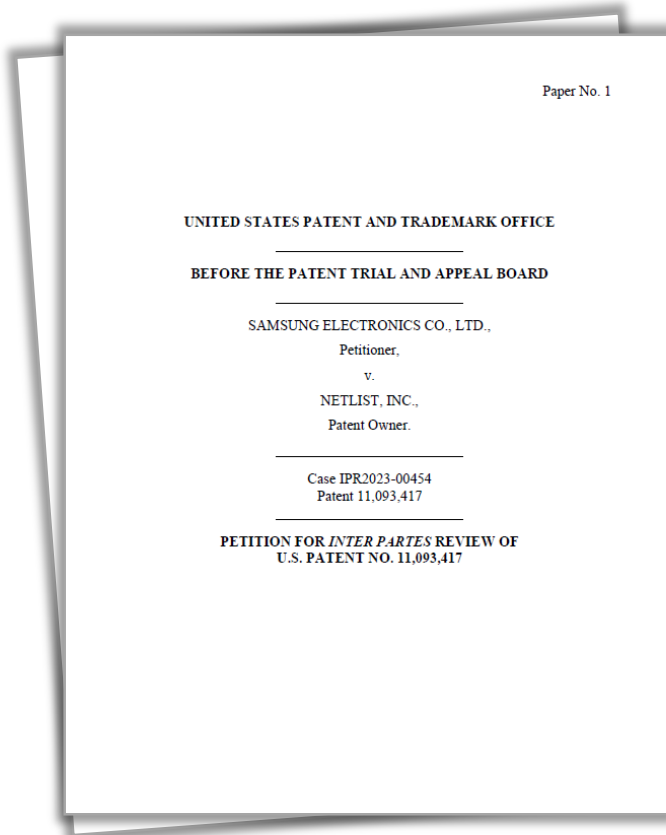
EX1071 (Perego), 9:58-10:4

- 1) individual device select lines on **secondary channel**
- 2) no modification on **primary channel**
- 3) buffer for translation as needed

Ground 1: Perego and JESD79-2

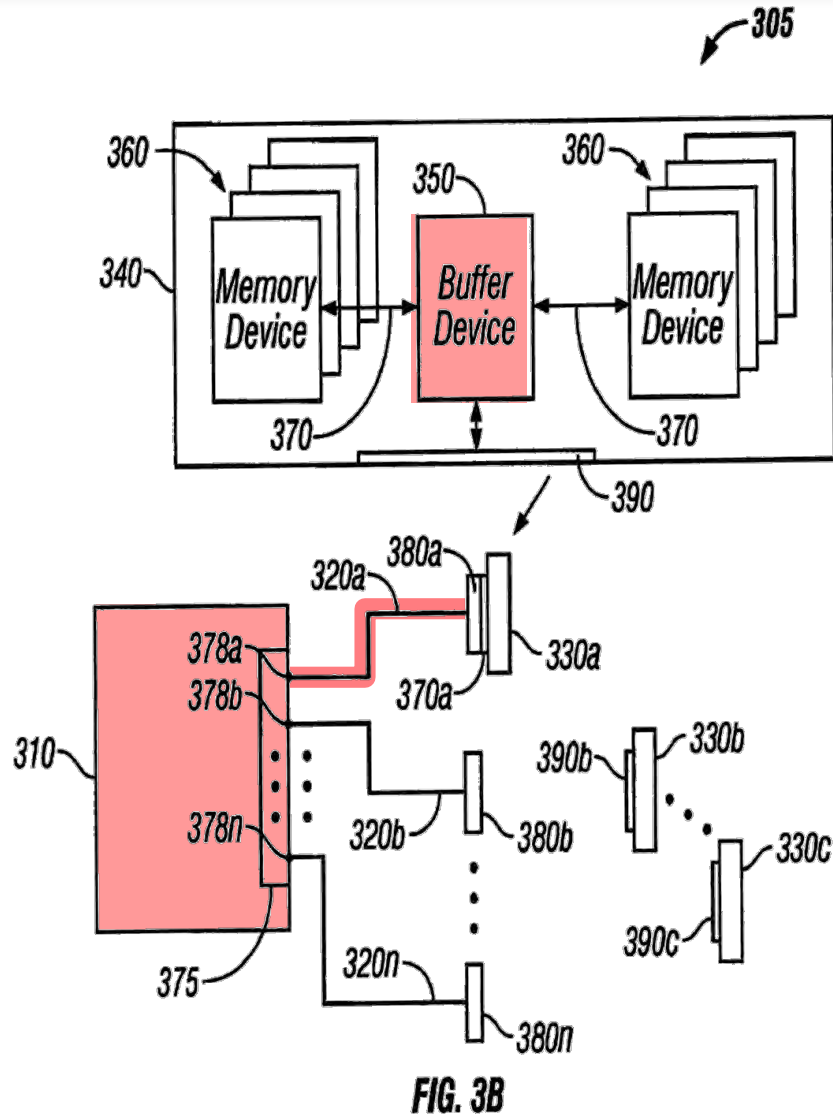
1. Perego and JESD79-2 do not disclose or suggest input “chip select signals”
- 2. No motivation to modify** Perego to add input chip selects as Petitioner proposed
3. Perego and JESD79-2 do not disclose or suggest the CAS-latency claim elements
4. Perego and JESD79-2 do not disclose or suggest a plurality of “ranks”

'417 Petition Suggests Modifying Perego to Provide Input Chip Selects



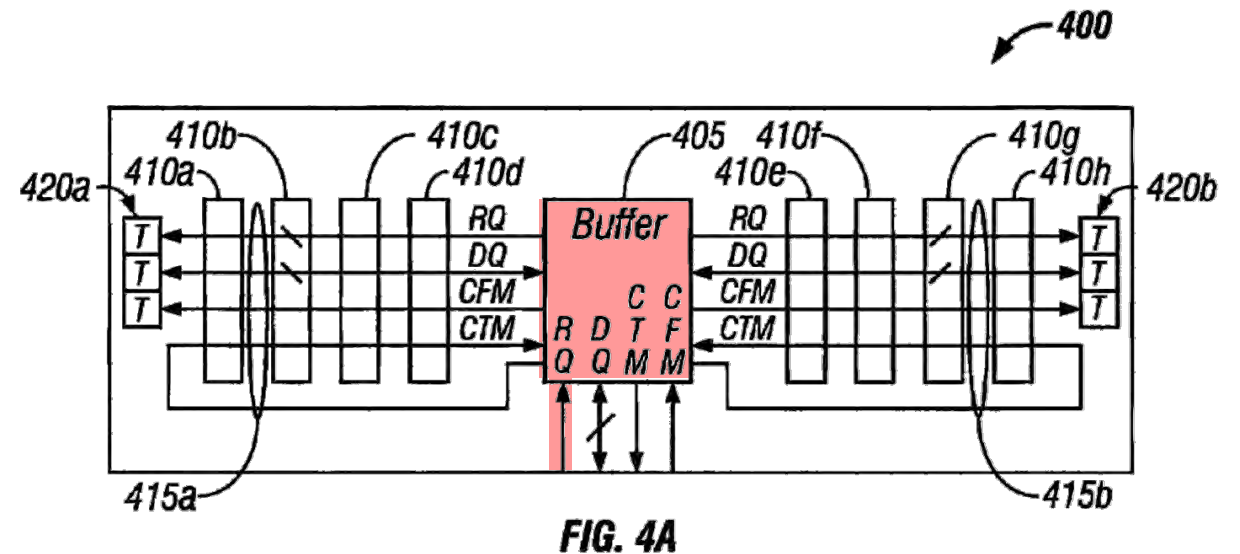
It also would have been obvious to a POSITA in light of JESD79-2 and knowledge of the JEDEC standards that the memory controller would provide multiple chip-select signals to the memory module (e.g., “S0-S3” below), corresponding to multiple “*ranks*” of memory devices (called “physical banks” below, *see* pp.26-28), where one of those chip-select signals is active to select the target rank of memory devices for the read or write operation, and the other chip-select signal(s) are inactive so that the other rank(s) of memory devices do not participate in the read or write operation. EX1003, ¶¶251-252; EX1064, p.6 (“CS provides for external Rank selection on systems with multiple Ranks.”); EX1062, p.6 (below); EX1066, pp.6-7 (similar).

Petition Proposal: Perego + JESD79-2 + JEDEC 21-C



Proposed Combination:

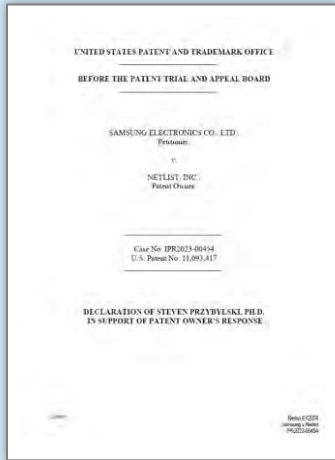
- 1) Modify/Replace Perego Memory Controller 310 to Generate S0-S3;
- 2) Modify Point-to-Point Link 320 to Transmit S0-S3
- 3) Modify Buffer 350/405 to Receive S0-S3



No Motivation to Modify Perego

- 1. Perego's Rambus system and JEDEC are fundamentally different architectures**
2. Modifying Perego would destroy its principles of operation
3. Perego provides a solution to accommodate DDR2 SDRAMs

Perego's Rambus Addressing Is Not Compatible with JEDEC-style DIMMs, Such as Those Described in the '417 and '215 Patents



Steven Przybylski, Ph.D.
Expert Witness

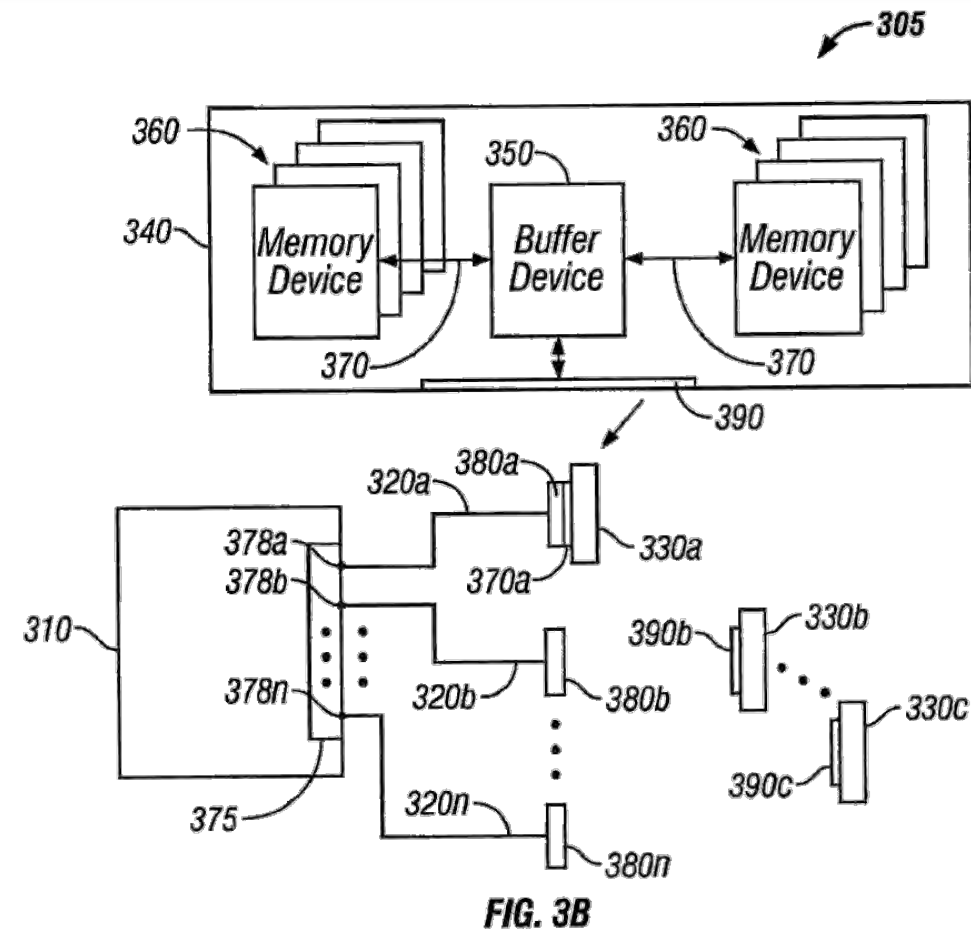


189. Specifically, the '417 Patent discloses and claims modules that use JEDEC-compliant DRAMs and that have a memory bus interface that is similar to JEDEC-standardized RDIMMs. Improvements are made to improve the signal loading and improve bandwidth performance within the context of a multi-drop memory bus with conventional signal trace topologies.

translation embodiments of the buffer device. But the essential and radically different approach of Perego is the focus on a dynamic point-to-point memory system topology and configurable data path widths allowing for changes to the capacity of the memory system, changing the number of used DQ signal traces on the primary channel without losing access to any of the storage locations.

Perego's Solution for a High Bandwidth Memory System

A dynamic point-to-point topology may also be employed to connect the memory subsystem port to each of the memory subsystems. A dynamic point-to-point topology includes a first plurality of point-to-point connections between the memory controller and a first memory module and a second plurality of point-to-point connections between the memory controller and the second memory module in a first configuration. For example, when the second memory module is removed from the system and a second configuration is desired, the plurality of point-to-point connections are routed to the first memory module to retain system bandwidth between memory modules and the controller or increase the bandwidth to the first memory module. The routing may be performed in a number of ways including using a continuity module or switches. In an embodiment, a configurable width buffer device disposed on the first memory module provides the flexibility to configure the width of the first memory module to accept switch between the first and second configurations. That is the configurable width buffer device may provide the flexibility to configure the module to connect to the first plurality of point-to-point connections in the first configuration and to connect to the second plurality of point-to-point links in the second configuration.



Dynamic Point-to-Point Topology Enabled by Configurable Width Buffer Device

A dynamic point-to-point topology may also be employed to connect the memory subsystem port to each of the memory subsystems. A dynamic point-to-point topology includes a first plurality of point-to-point connections between the memory controller and a first memory module and a second plurality of point-to-point connections between the memory controller and the second memory module in a first configuration. For example, when the second memory module is removed from the system and a second configuration is desired, the plurality of point-to-point connections are routed to the first memory module to retain system bandwidth between memory modules and the controller or increase the bandwidth to the first memory module. The routing may be performed in a number of ways including using a continuity module or switches. In an embodiment, a configurable width buffer device disposed on the first memory module provides the flexibility to configure the width of the first memory module to accept switch between the first and second configurations. That is the configurable width buffer device may provide the flexibility to configure the module to connect to the first plurality of point-to-point connections in the first configuration and to connect to the second plurality of point-to-point links in the second configuration.

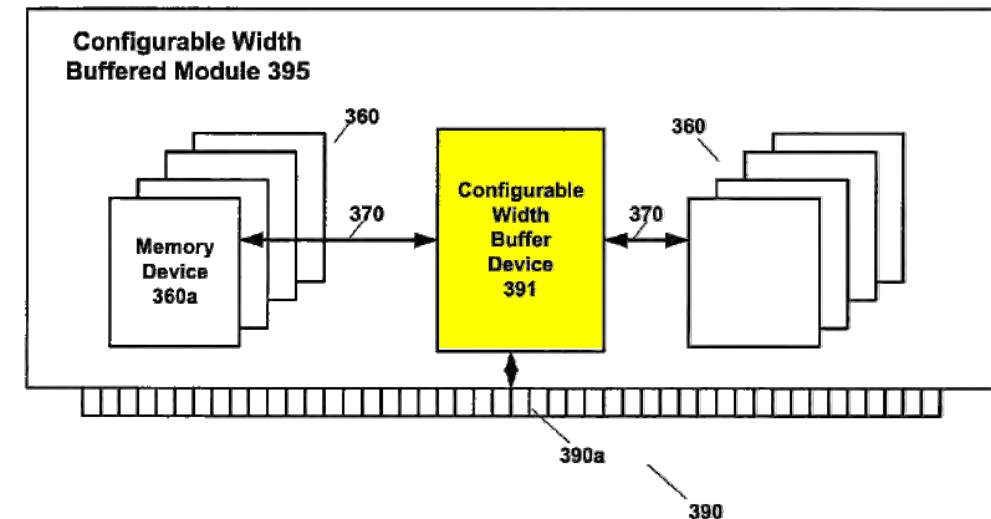
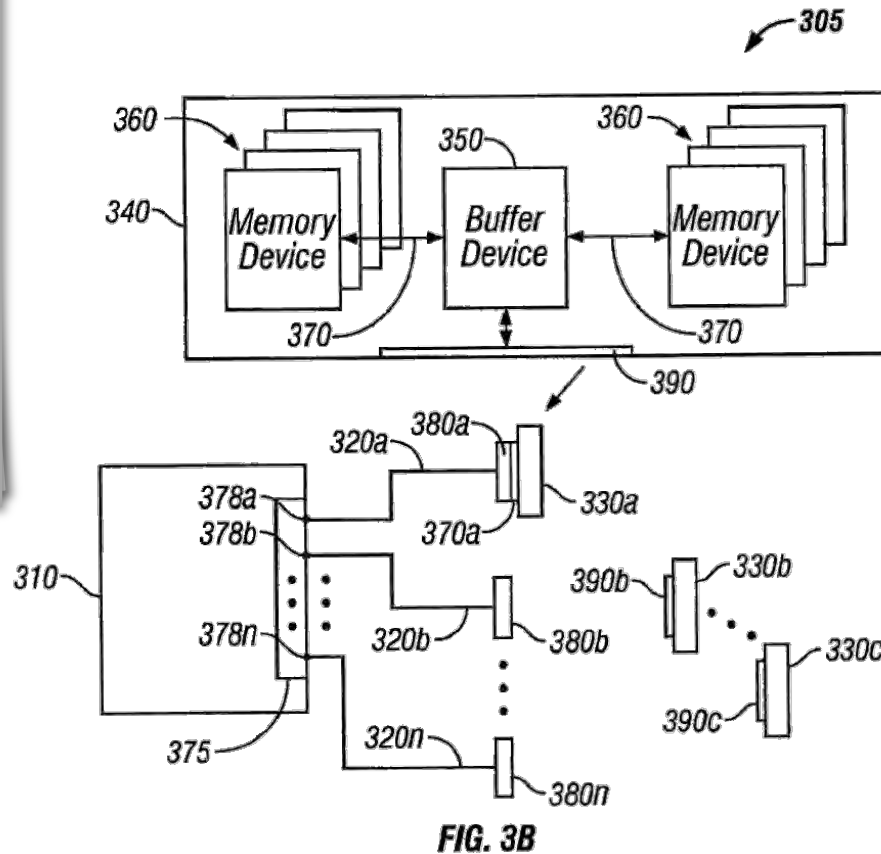
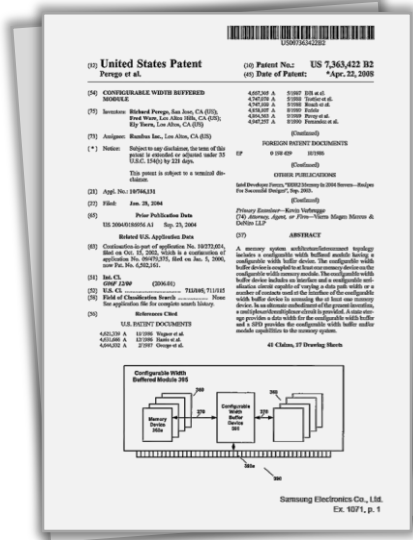


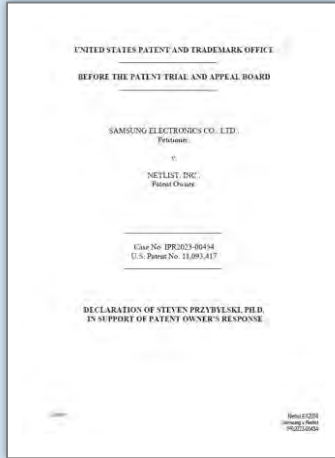
Fig. 3C

Perego's High Bandwidth Memory System



- Fig. 3B shows “an exemplary system that uses configurable width modules coupled in a dynamic point-to-point configuration”
- Memory subsystems 330a-c are each a buffered memory module with a configurable width interface
- Point-to-point links 320b-320n coupled to unpopulated mating connectors 380b-n are “routed to access the single buffered memory module located in mating connector 380a”
- Module in connector 380a “programmed to include an interface width that may accommodate the routed point-to-point links 320b-320n”
- U.S. App. No. 09/797,099 (incorporated by reference) provides more implementation details (issued as U.S. Patent No. 7,610,447 (EX2034))

Perego System Architected Differently from JEDEC System



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Expert Witness

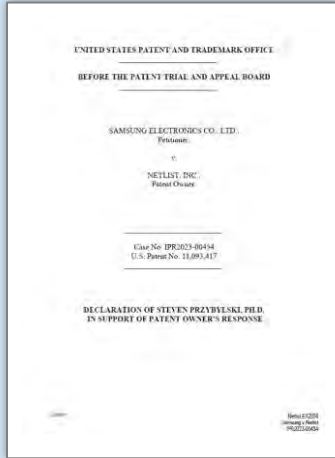


139. Thus, a POSITA would not be motivated, as Petitioner suggests, to implement Perego's memory modules in a registered DIMM format ... and uses DIMM module input signals according to section 4.10.20 of JESD21-C because, among other things:

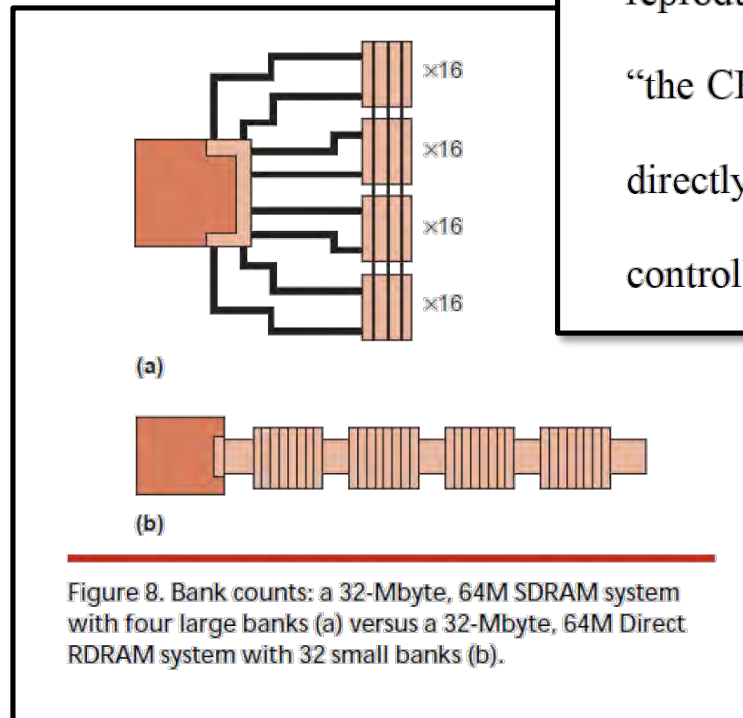
- 1) Such a module would have lower performance than the module contemplated by Perego.
- 2) Such a primary channel would provide signal traces to convey signals that are not transmitted nor received.
- 3) Such a module would provide inadequate addressing for the memory types that are central to the inventive advantages disclosed by Perego. In particular, the module interfaces defined by section 4.10.20 of JESD21-C allow for 4 chip select signals, 3 bank address bits, and up to 16 row and column address bits per bank. A POSITA would recognize that if the modules described by Perego were modified as described by the Petition, there would be, at a minimum, inadequate bank address bits and no interface support for sub-column addressing Ex. 2009, p. 7, 8, 11.

- 4) Perego already discloses the use of DDR2 SDRAMs within its modules through the use of protocol translation with certain embodiments of its buffer device. Ex. 1071, 10:63-67. Thus a POSITA would not have a reason to modify the Perego architecture away from the dynamic point-to-point interconnect system and the advantages presented by this system. Ex. 1071, 3:55-61.
- 5) Perego discloses that the memory interfaces 520 on buffer circuit can drive an unspecified number of subsets. Ex. 1071, 7:48-64. Perego indicates that the address of a read or write in conjunction with the current configured width of the interface, not a chip-select signal, specifies which target subset or subsets will be accessed in response to the command. Ex. 1071, 14:62-15:6. Thus an interface in which chip-select signals are an integral part of the subset selection mechanism is not consistent with the teaching of Perego.

Perego's Individual Device Addressing Is Not Compatible with JEDEC-Style DIMMs



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Expert Witness



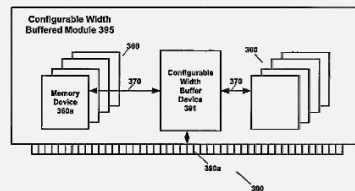
51. In JEDEC-style DIMMs, several DRAMs are “ganged together in parallel to provide the necessary aggregate bandwidth,” thus increasing the size of independent banks but not their number. *See* Ex. 2001, p. 23 (Fig. 8(a), reproduced below). In contrast, “a Direct RDRAM spans the entire channel” and “the CPU accesses each RDRAM independently.” *Id.*, p. 23. “So each DRAM directly adds to the number of memory banks accessible to the memory controller.” *Id.*; *see* Fig. 8(b) below.

No Motivation to Modify Perego

1. Perego's Rambus system and JEDEC are fundamentally different architectures
- 2. Modifying Perego would destroy its principles of operation**
3. Perego provides a solution to accommodate DDR2 SDRAMs

Perego's Design Objectives

 US007363422B2	
(12) United States Patent Perego et al.	(10) Patent No.: US 7,363,422 B2 (45) Date of Patent: *Apr. 22, 2008
(54) CONFIGURABLE WIDTH BUFFERED MODULE	4,657,305 A 5/1987 Dill et al. 4,747,070 A 5/1988 Taitel et al. 4,747,460 A 5/1988 Rouch et al. 4,853,187 A 8/1989 Taitel 4,864,583 A 9/1989 Parvy et al. 4,947,137 A 9/1989 Terasaki et al.
(75) Inventors: Richard Perego, San Jose, CA (US); Fred Ware, Los Altos Hills, CA (US); Ely Ysern, Los Altos, CA (US)	(Continued)
(73) Assignee: Rambus Inc., Los Altos, CA (US)	FOREIGN PATENT DOCUMENTS
(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(o) by 221 days.	EP 0 198 429 10/1986 (Continued)
This patent is subject to a terminal disclaimer.	OTHER PUBLICATIONS
(21) Appl. No.: 10/766,131	Intel Developer Forum, "DDR2 Memory In 2004 Servers—Recipes For Successful Design", Sep. 2003. (Continued)
(22) Filed: Jan. 28, 2004	Priority Examiner—Kevin Vorhiesse (74) Attorney, Agent, or Firm—Viera Magen Marcus & DeNiro LLP
(65) US 2004/0186956 A1 Sep. 23, 2004	(57) ABSTRACT
Related U.S. Application Data	(57) A memory system architecture/interconnect topology includes a configurable width buffered module having a configurable width buffer device. The configurable width buffer device is coupled to at least one memory device on the configurable width memory module. The configurable width buffer device includes an interface and a configurable self-activation circuit capable of varying a data path width or a number of contacts used at the interface of the configurable width buffer device in accessing the at least one memory device. In an alternate embodiment of the present invention, a multiplexed/demultiplex circuit is provided. A state storage provides a data width for the configurable width buffer and a SPD provides the configurable width buffer and/or module capabilities to the memory system.
(63) Continuation-in-part of application No. 10/272,024, filed on Oct. 15, 2002, which is a continuation of application No. 09/470,375, filed on Jan. 9, 2000, now Pat. No. 6,502,161.	
(51) Int. Cl. G06F 12/00 (2006.01)	
(52) U.S. Cl. 711/105, 711/115	
(58) Field of Classification Search None See application file for complete search history.	
(56) References Cited	
U.S. PATENT DOCUMENTS	
4,631,239 A 11/1986 Wagner et al. 4,631,666 A 12/1986 Harris et al. 4,644,532 A 2/1987 George et al.	41 Claims, 17 Drawing Sheets



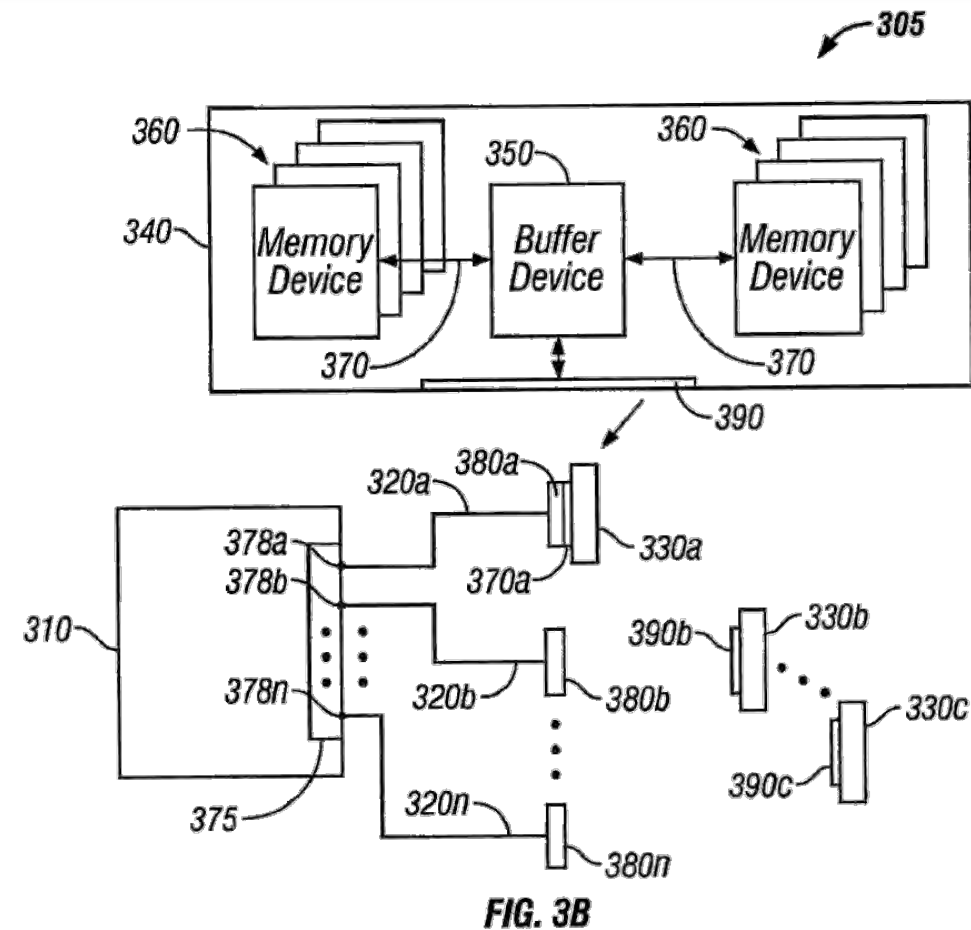
Samsung Electronics Co., Ltd.
Ex. 1071, p. 1

There is a need for memory system architectures or interconnect topologies that provide flexible and cost effective upgrade capabilities while providing high bandwidth to keep pace with microprocessor operating frequencies.

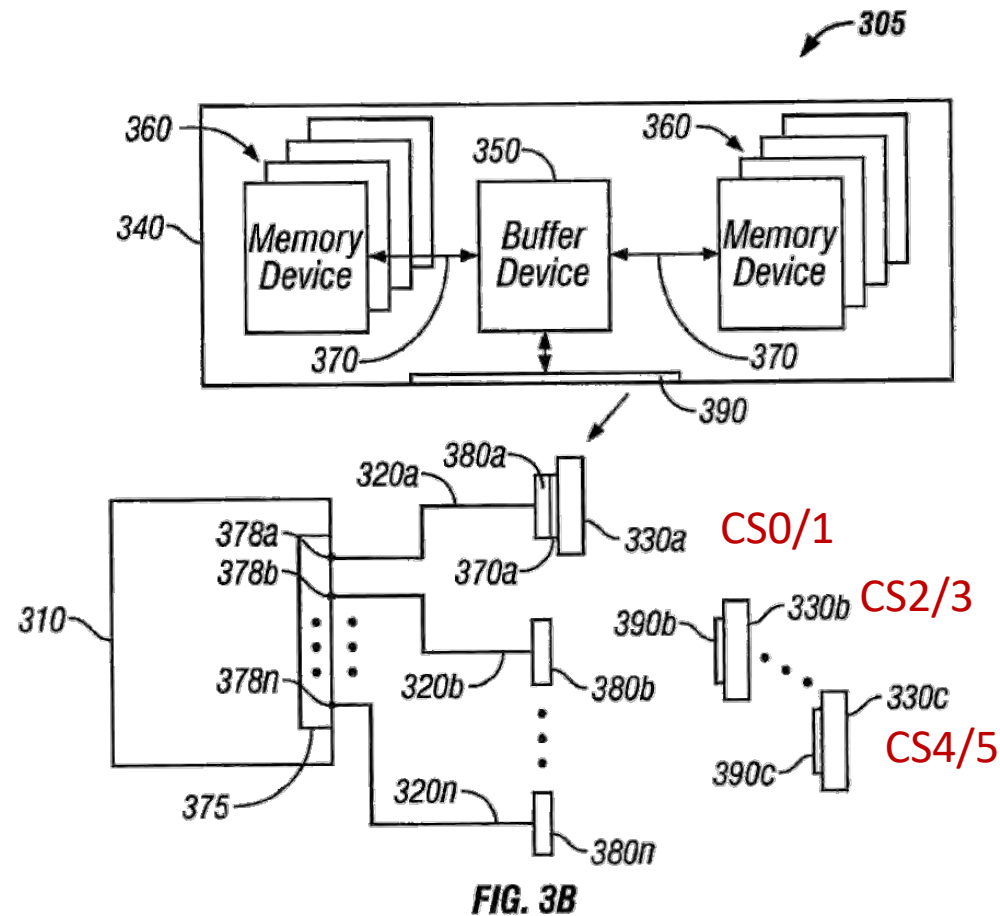
EX1071 (Perego), 2:26-29

Perego Achieves Its Stated Objective with a Dynamic Point-to-Point Topology

A dynamic point-to-point topology may also be employed to connect the memory subsystem port to each of the memory subsystems. A dynamic point-to-point topology includes a first plurality of point-to-point connections between the memory controller and a first memory module and a second plurality of point-to-point connections between the memory controller and the second memory module in a first configuration. For example, when the second memory module is removed from the system and a second configuration is desired, the plurality of point-to-point connections are routed to the first memory module to retain system bandwidth between memory modules and the controller or increase the bandwidth to the first memory module. The routing may be performed in a number of ways including using a continuity module or switches. In an embodiment, a configurable width buffer device disposed on the first memory module provides the flexibility to configure the width of the first memory module to accept switch between the first and second configurations. That is the configurable width buffer device may provide the flexibility to configure the module to connect to the first plurality of point-to-point connections in the first configuration and to connect to the second plurality of point-to-point links in the second configuration.



JEDEC-Style Signaling Destroys Dynamic Rerouting and System Bandwidth Preservation

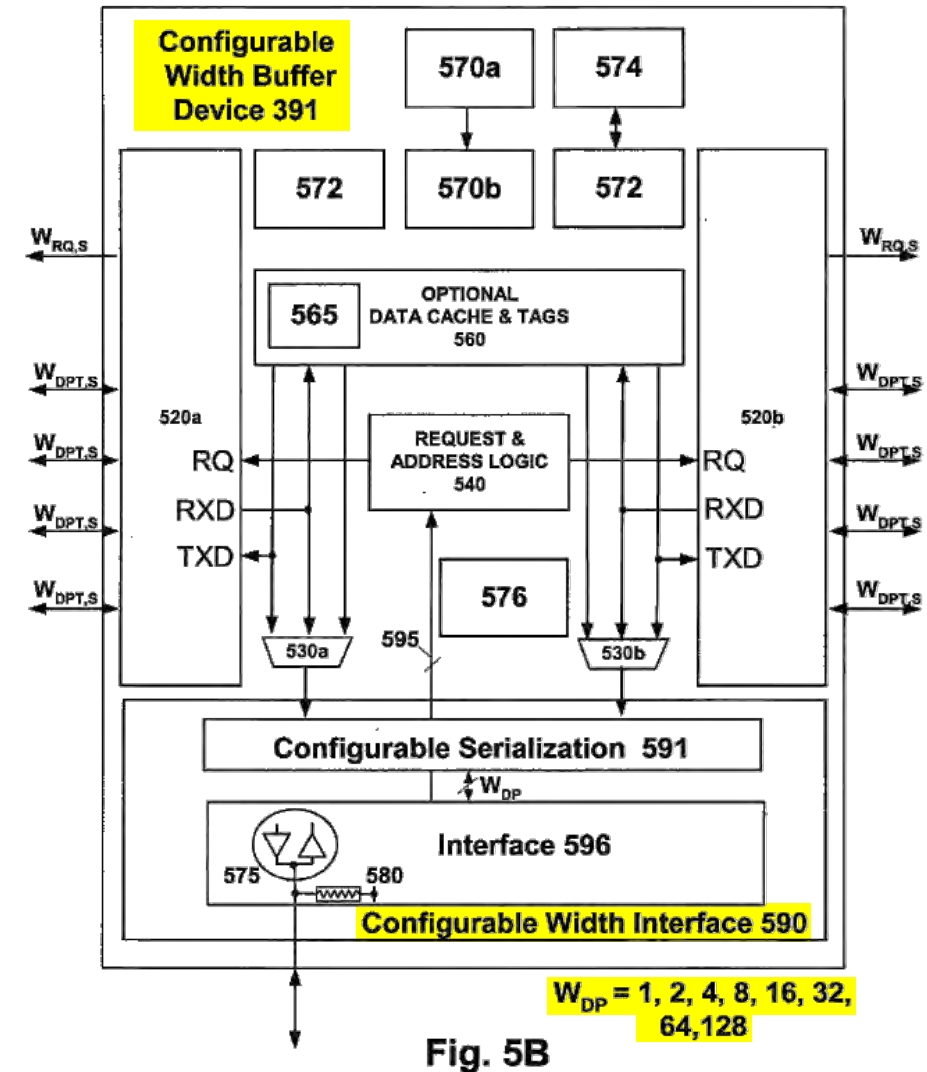


- In JEDEC, each memory slot can accept up to two chip-select signals. EX1079, [0010]
- Cannot redirect traffic associated with CS2/3 and CS4/5 to slot 380a associated with CS0/1 only

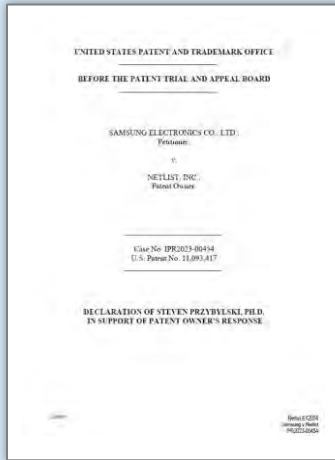
If modified as proposed

Perego Achieves Dynamic Point-to-Point Topology with Configurable Width Buffer Device

A dynamic point-to-point topology may also be employed to connect the memory subsystem port to each of the memory subsystems. A dynamic point-to-point topology includes a first plurality of point-to-point connections between the memory controller and a first memory module and a second plurality of point-to-point connections between the memory controller and the second memory module in a first configuration. For example, when the second memory module is removed from the system and a second configuration is desired, the plurality of point-to-point connections are routed to the first memory module to retain system bandwidth between memory modules and the controller or increase the bandwidth to the first memory module. The routing may be performed in a number of ways including using a continuity module or switches. In an embodiment, a configurable width buffer device disposed on the first memory module provides the flexibility to configure the width of the first memory module to accept switch between the first and second configurations. That is the configurable width buffer device may provide the flexibility to configure the module to connect to the first plurality of point-to-point connections in the first configuration and to connect to the second plurality of point-to-point links in the second configuration.



Adjusting Primary Link Would Change the Operating Principles of Perego



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Expert Witness



EX2024, ¶ 154;
see also ¶ 199;
Sur-Reply 3, 12

154. As described above, this assumption is invalid. On careful consideration of the teaching of Perego, a POSITA would not adjust the primary link (the memory bus interface) to mimic that of a DDR2 SDRAM or that of a DDR2 RDIMM. Any attempt to do this by a POSITA would change the operating principles of Perego regarding how to provide a high performance memory module that provides backward and forward compatibility and consistent addressing of storage location in the face of variable and dynamically configurable data path width and the memory device independence articulated by Perego. Ex. 1071, 10:59-63 (“Utilizing buffer device 405 between the memory devices and controller in accordance with the present invention (e.g., see Fig. 3) may feasibly render the type of memory device transparent to the system.”).

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Netlist slide, p. 66

JEDEC-Style Signaling Would Also Destroy Perego's Flexible Forward and Backward Memory Device Compatibility

Perego accommodates different types of memory devices, and this principle of operation would be destroyed by replacing its primary channel with a JEDEC-compliant bus.

There is a need for memory system architectures or interconnect topologies that provide flexible and cost effective upgrade capabilities while providing high bandwidth to keep pace with microprocessor operating frequencies.

EX1071 (Perego), 2:26-29

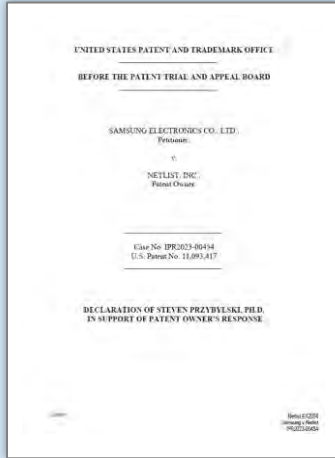
Buffer device 350 provides a high degree of system flexibility. New generations of memory devices may be phased in with controller 310 or into memory system 300 by modifying buffer device 350. Backward compatibility with existing generations of memory devices (i.e., memory devices 360) may also be preserved. Similarly, new generations of controllers may be phased in which exploit features of new generations of memory devices while retaining backward compatibility with existing generations of memory devices.

EX1071 (Perego), 6:34-43

- It “would change the operating principles of Perego regarding how to provide a high performance memory module that provides backward and forward compatibility.”
- It “would deprive Perego of the basis of its advantages, as well as compatibility with heterogeneous memory systems.”
- “[F]orward compatibility would be lost because the primary link interface would be stuck at DDR2-levels....”
- It “would make the module non-functional for Direct RDRAMs and XDR DRAMs,” because it would lack “additional Bank Address bits.”

EX2024, ¶¶ 129, 134, 137, 154

Changing Memory Bus Interface Would Make the Perego Memory Module Non-Functional for Rambus Memory Devices



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Expert Witness



JEDEC standards, including JESD21-C and JESD79-2.” Petition, p. 32. In this regard, Section 4.20.10 of JESD21-C requires Clock Enables, Chip Selects, exactly 3 Bank Address signals, ODT (on-die termination), bidirectional differential data strobe signals, data mask signals and a voltage reference signal.

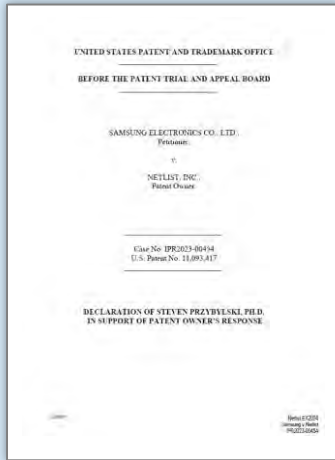
Ex. 1066, p. 6. These are all unnecessary, unusable or detrimental in the context of Perego’s memory system and module architecture. For example, Perego’s

Direct RDRAM and XDR DRAM embodiments require additional Bank Address bits to properly address the banks internal to those memory device types, so compliance with the standard in Ex. 1066 would make the module non-functional for Direct RDRAMs and XDR DRAMs, which would defeat Perego’s

ability to support “[d]ifferent types of memory devices ... on different modules within a memory system,” Ex. 1071, 10:63-67, as well as Perego’s support of not only “backward compatibility with existing generations of memory devices,” but also “new generations of memory devices,” Ex. 1071, 6:39-43.

**JESD21-C,
DDR2
RDIMM**

Adjusting Primary Link Would Deprive Perego of Its Advantages

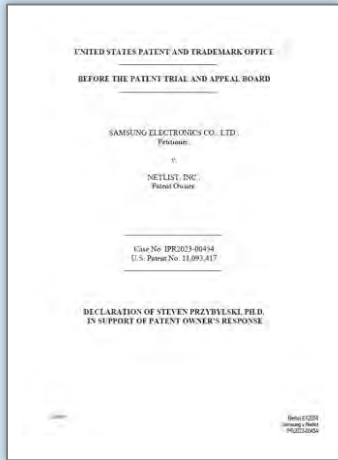


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137. As noted above, the higher bandwidth performance of memory systems constructed of Rambus Direct RDRAMs or XDR DRAMs stems from the channel architecture, including the topology and signaling standards. Changing the primary channel of Perego to resemble that of a DDR2 SDRAM as suggested in the Petition would deprive Perego of the basis of its advantages, as well as compatibility with heterogeneous memory systems.

No Motivation to Combine/Modify Perego's Primary Channel



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Expert Witness



190. In contrast, the principal and illustrated embodiments use unconventional DRAMs developed by Rambus Inc. and are not JEDEC-standardized. Conventional SDRAMs can also be used because of the protocol translation embodiments of the buffer device. But the essential and radically different approach of Perego is the focus on a dynamic point-to-point memory system topology and configurable data path widths allowing for changes to the capacity of the memory system, changing the number of used DQ signal traces on the primary channel without losing access to any of the storage locations.

Not Obvious When Modification Requires Changing Primary Reference's Principle of Operation



“We hold, further, that the combination of Jepson with Chinnery et al. is ***not a proper ground for rejection*** of the claims here on appeal. This suggested combination of references would require ***a substantial reconstruction and redesign of the elements*** shown in Chinnery et al. as well as ***a change in the basic principles under which the*** Chinnery et al. ***construction was designed to operate.***”

In re Ratti, 270 F.2d 810, 813 (CCPA 1959)

No Motivation to Modify Perego

1. Perego's Rambus system and JEDEC are fundamentally different architectures
2. Modifying Perego would destroy its principles of operation
3. **Perego provides a solution to accommodate DDR2 SDRAMs**

No Motivation to Modify Perego's Primary Channel Because Perego's Buffer Already Facilitates Use of SDRAM Memory Devices

(12) United States Patent
Perego et al.

(10) Patent No.
(45) Date of Pat.

(54) CONFIGURABLE WIDTH BUFFERED
MODULE

(75) Inventors: Richard Perego, San Jose, CA (US);
Erik Ware, Los Altos Hills, CA (US);
Ely Beem, Los Altos, CA (US)

(73) Assignee: Rambus Inc., Los Altos, CA (US)

(*) Notice: Subject to any disclaimer, the term of this
patent is extended or adjusted under 35
U.S.C. 154(b) by 221 days.
This patent is subject to a terminal dis-
claimer.

(21) Appl. No.: 10/766,131

(22) Filed: Jan. 25, 2004

(65) Prior Publication Data
US 2004/0186956 A1 Sep. 23, 2004

Related U.S. Application Data

(63) Continuation-in-part of application No. 10/272,024,
filed on Oct. 15, 2002, which is a continuation of
application No. 09/479,375, filed on Jan. 3, 2000,
now Pat. No. 6,502,161.

(51) Int. Cl. G06F 12/00 (2006.01)

(52) U.S. Cl. 719/105; 711/115

(56) Field of Classification Search: None
See application file for complete search history.

(56) References Cited

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4,621,339 A 11/1986 Wagner et al.

4,621,686 A 12/1986 Thoma et al.

4,644,532 A 2/1997 George et al.

FOREIGN

EP 9 198 478

CITE

Intel Developer Forum '99

For Successful Design

Primary Examiner—S.

(74) Attorney, Agent,

DeBiro LLP

(57)

A memory system

includes a configurable

width buffer device

coupled to a configurable

width memory device

and a configurable width

memory device. In an alternate

embodiment, the configurable

width memory device

provides a data width

and a SPD provides the

module capabilities to

41 Claims

In one embodiment, memory devices **410a–410h** are Rambus® Dynamic Random access Memory (RDRAM) devices operating at a data rate of 1066 Mbits/sec. Other memory devices may be implemented on module **400**, for example, Double Data Rate 2 (DDR2) DRAM devices and Synchronous DRAM (SDRAM) devices. Utilizing buffer device **405** between the memory devices and controller in accordance with the present invention (e.g., see FIG. 3) may feasibly render the type of memory device transparent to the system. Different types of memory devices may be included on different modules within a memory system, by employing buffer device **405** to translate protocols employed by controller **310** to the protocol utilized in a particular memory device implementation.

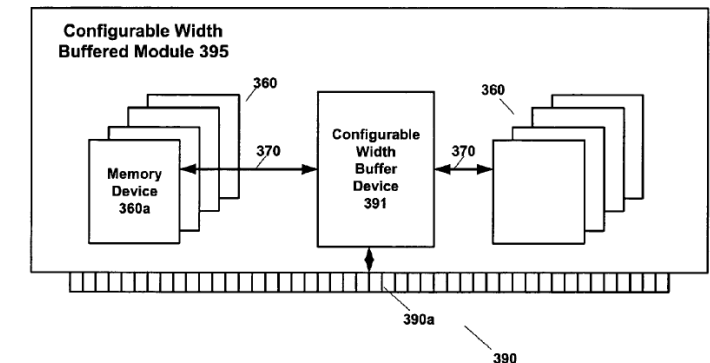
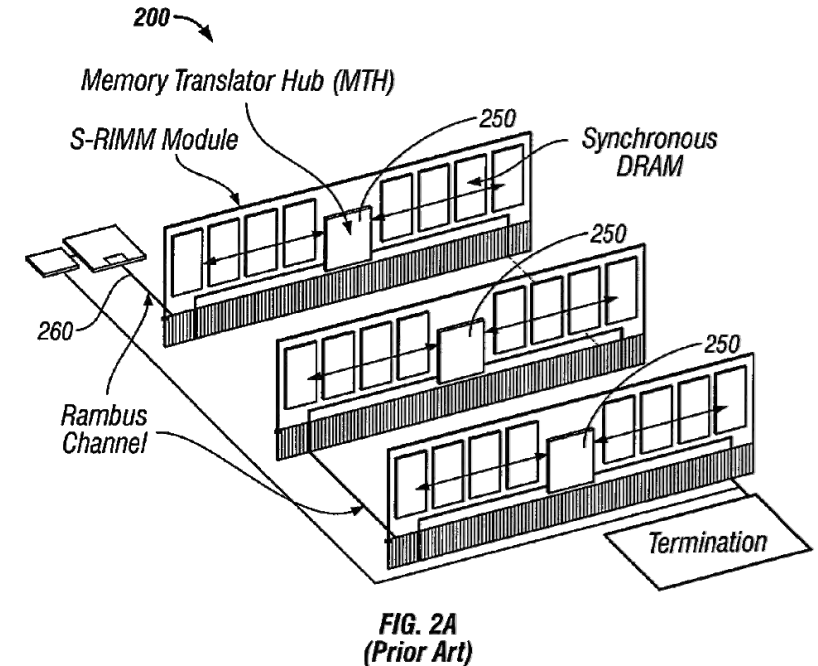


Fig. 3C

Perego Does Not Suggest Compatibility with JEDEC Controllers or Modules

Buffer device **350** provides a high degree of system flexibility. New generations of memory devices may be phased in with controller **310** or into memory system **300** by modifying buffer device **350**. Backward compatibility with existing generations of memory devices (i.e., memory devices **360**) may also be preserved. Similarly, new generations of controllers may be phased in which exploit features of new generations of memory devices while retaining backward compatibility with existing generations of memory devices.

EX1071 (Perego),
6:34-43

Netlist admits that Perego discloses “retaining backward compatibility with existing generations of memory devices” and compatibility for “new generations of memory devices,” POR 23-24, but ignores that Perego explains that this compatibility and flexibility also applies to existing and future *memory* “*controllers*,” EX1071, 6:34-43, which were overwhelmingly JEDEC-compliant at the time, as Netlist’s expert admitted above (pp.5-6), providing further motivation to implement Perego in a JEDEC-style memory system, as recognized by the Board above (p.9, n.4).

Reply 12-13

Petitioner contends that Perego supports other types of controllers, but the cited text in Perego addresses “*new generations of controllers*” and says nothing about other *types of controllers or modules* (as it does for memory devices).

Sur-Reply 8-9

In one embodiment, memory devices **410a–410h** are Rambus® Dynamic Random access Memory (RDRAM) devices operating at a data rate of 1066 Mbits/sec. Other memory devices may be implemented on module **400**, for example, Double Data Rate 2 (DDR2) DRAM devices and Synchronous DRAM (SDRAM) devices. Utilizing buffer

EX1071 (Perego), 10:54-59

Perego Does Not Suggest Replacing RQ Control Lines in Primary Link with Chip Select Lines

Perego

In alternate embodiments, control lines (RQ) may comprise individual control lines, for example, row address strobe, column address strobe, etc., and address lines. Individual point-to-point control and address lines increase the number of parallel signal connection paths, thereby increasing system layout resource requirements with respect to a narrow “packet protocol” approach. In one alternate embodiment illustrated in FIG. 6A, individual device select lines 633a and 633b are employed to perform device selection. Individual device select lines 633a and 633b decrease

EX1071 (Perego), 9:58-67

Petitioner’s reliance on an alternate embodiment in Perego disclosing individual control lines such as “row address strobe” (RAS) and “column access strobe” (CAS) is misplaced. RAS and CAS lines are not specific to SDRAMs.

The primary difference between SDRAMs and earlier asynchronous DRAMs is the presence in the system of a clock signal against which all actions (command and data transmissions) are timed. Whereas asynchronous DRAMs use the RAS and CAS signals as strobes—that is, the strobes directly cause the DRAM to sample addresses and/or data off the bus—SDRAMs instead use the clock as a strobe, and the RAS and CAS signals are simply commands that are themselves sampled off the bus in time with the clock strobe.

EX1069 (Jacob), p.9

Perego Does Not Suggest Including Chip Select Lines in RQ Lines



NOTE 1 All DDR2 SDRAM commands are defined by states of $\overline{\text{CS}}$, $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$ and CKE at the rising edge of the clock.

EX1064 (JESD79-2), p.49

Perego does not mention WE, CKE, or chip select (CS) signals used by DDR2 SDRAMs; and reference to RAS/CAS does not imply a DRAM system using CS lines

Perego Does Not Suggest Using Chip Select Lines

(12) **United States Patent**
Perego et al.

(10) **Patent No.:** US 7,363,422 B2
(45) **Date of Patent:** Apr. 22, 2008

(54) **CONFIGURABLE WIDTH BUFFERED MODULE**

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(73) **Assignee:** Rambus Inc., Los Altos, CA (US)

(*) **Notice:** Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 221 days.
This patent is subject to a terminal disclaimer.

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Related U.S. Application Data

(63) Continuation-in-part of application No. 10/272,024, filed on Oct. 15, 2002, which is a continuation of application No. 09/479,375, filed on Jan. 3, 2000, now Pat. No. 6,502,161.

(51) **Int. Cl.**
G06F 12/00 (2006.01)

(52) **U.S. Cl.** 719/105; 711/115

(56) **Field of Classification Search** None
See application file for complete search history.

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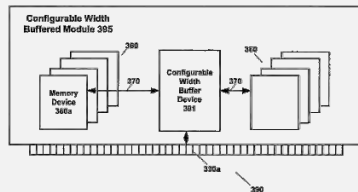
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(Continued)

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(74) **Attorney, Agent, or Firm—Vernon Mague Moreno & DeNiro LLP**

(57) **ABSTRACT**

A memory system architecture/interconnect topology includes a configurable width buffered module having a configurable width buffer device. The configurable width buffer device is coupled to at least one memory device on the configurable width memory module. The configurable width buffer device includes an interface and a configurable utilization circuit capable of varying a data path width or a number of contents used at the interface of the configurable width buffer device in accordance with at least one memory device. In an alternate embodiment of the present invention, a multiplexor/demultiplexer circuit is provided. A state storage provides a data width for the configurable width buffer and a SPD provides the configurable width buffer and/or module capabilities to the memory system.

41 Claims, 17 Drawing Sheets



modules. By way of comparison, buffers disposed on the conventional DIMM module in U.S. Pat. No. 5,513,135 are employed to buffer or register control signals such as RAS, and CAS, etc., and address signals. Data I/Os of the memory

EX1071 (Perego), 6:27-30

And the patent cited in Perego that Petitioner relies upon was cited as a prior-art “comparison” to Perego’s alleged inventions.

The Figure 6A Embodiment of Perego Provides Individual Device Select Lines

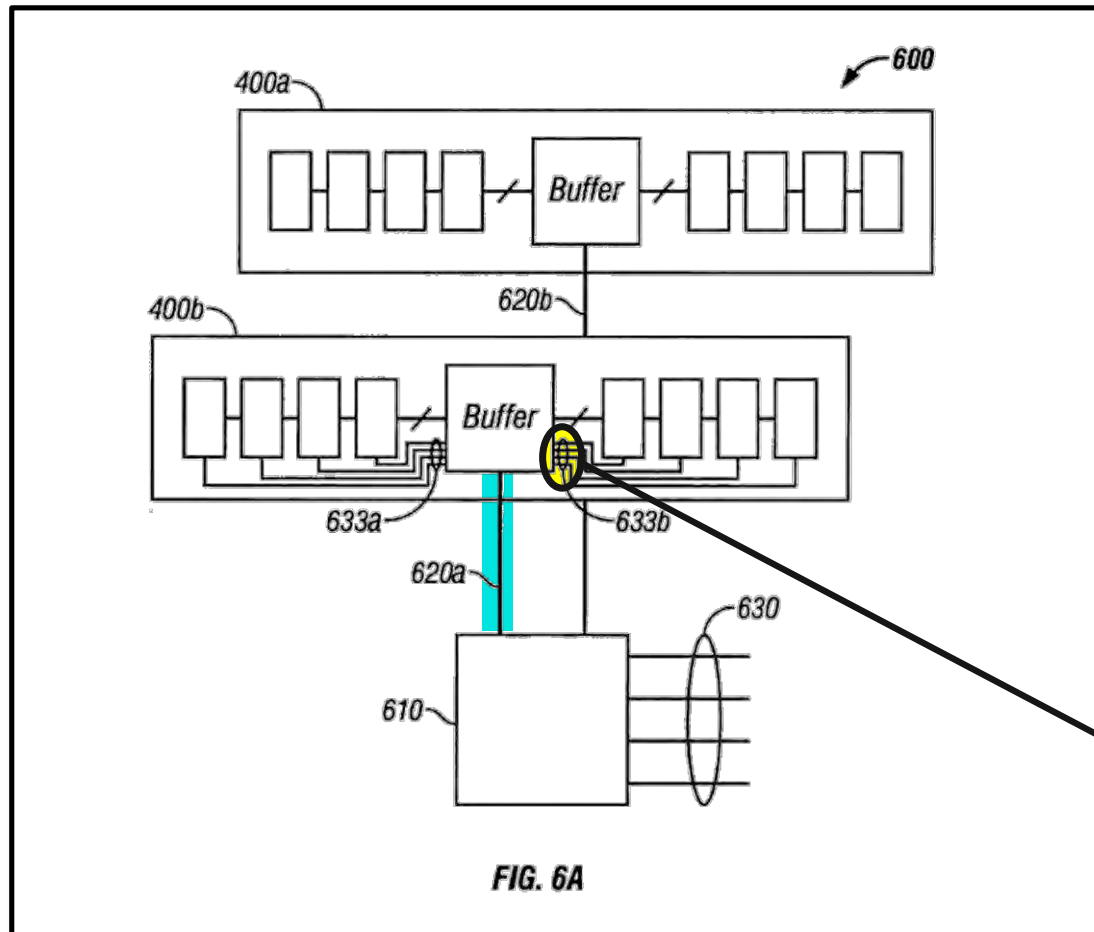


FIG. 6A

EX1071 (Perego), Fig. 6A

In alternate embodiments, control lines (RQ) may comprise individual control lines, for example, row address strobe, column address strobe, etc., and address lines. Individual point-to-point control and address lines increase the number of parallel signal connection paths, thereby increasing system layout resource requirements with respect to a narrow “packet protocol” approach. In one alternate embodiment illustrated in FIG. 6A, individual device select lines 633a and 633b are employed to perform device selection. Individual device select lines 633a and 633b decrease some latency consumed by decoding device identification that normally is utilized when multiple devices share the same channel and incorporate individual device identification values.

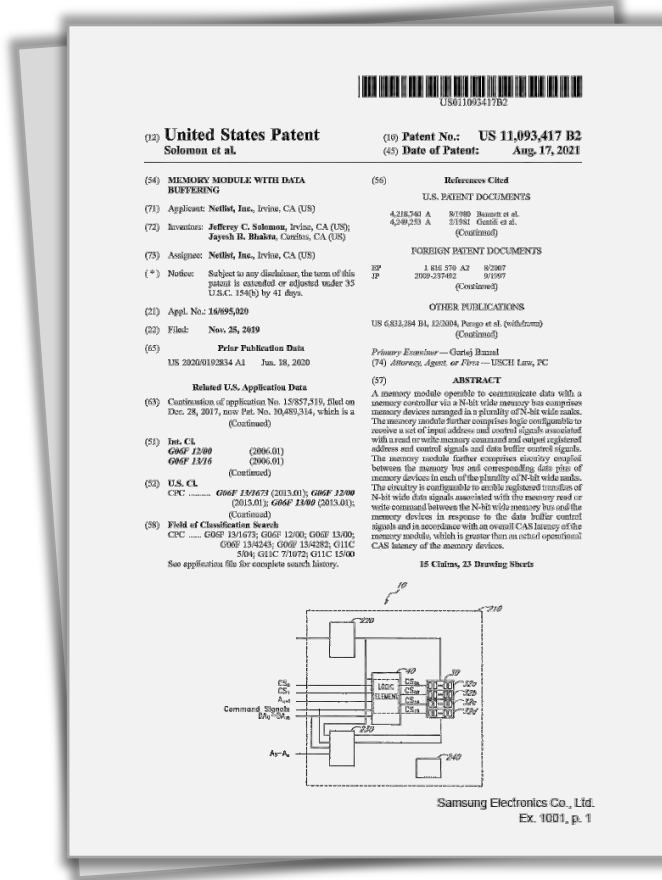
EX1071 (Perego), 9:58-10:4

- 1) individual device select lines on **secondary channel**
- 2) no modification on **primary channel**
- 3) buffer for translation as needed

Ground 1: Perego and JESD79-2

1. Perego and JESD79-2 do not disclose or suggest input “chip select signals”
2. No motivation to modify Perego to add input chip selects as Petitioner proposed
3. Perego and JESD79-2 **do not disclose or suggest** the CAS-latency claim elements
4. Perego and JESD79-2 do not disclose or suggest a plurality of “ranks”

Missing Limitation #2 in '417 Patent: CAS-Latency Claim Elements



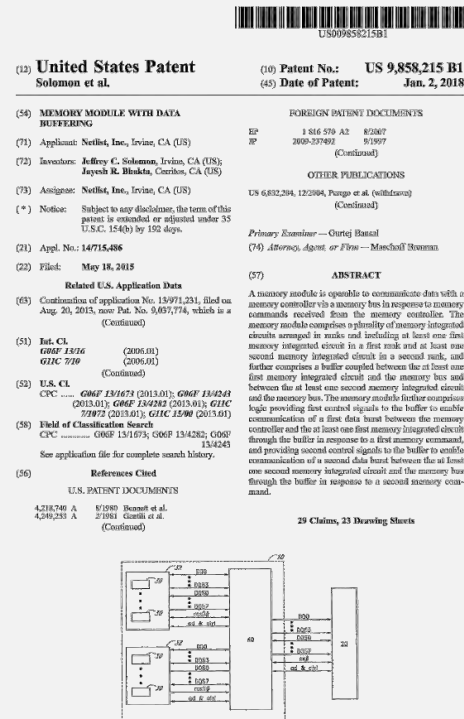
1. A memory module operable in a computer system to communicate data with a memory controller of the computer system via a N-bit wide memory bus in response to read or write memory commands received from the memory controller, the memory bus including address and control signal lines and data signal lines, the memory module comprising:

circuitry coupled between the data signal lines in the N-bit wide memory bus and corresponding data pins of memory devices in each of the plurality of N-bit wide ranks, the circuitry being configurable to transfer the burst of N-bit wide data signals between the N-bit wide memory bus and the memory devices in the one of the plurality of N-bit wide ranks in response to the data buffer control signals and in accordance with an overall CAS latency of the memory module; wherein data transfers through the circuitry are registered for an amount of time delay such that the overall CAS latency of the memory module is greater than an actual operational CAS latency of each of the memory devices.

Additional CAS latency must be due at least in part to delay through the circuitry (data buffer), and not to registering the control or address signals, or delay associated with memory devices.

POR 36-39, 54;
Sur-Reply 17-18, 25

Missing Limitation #2 in '215 Patent: CAS-Latency Claim Elements



1. A memory module operable in a computer system to communicate data with a memory controller of the computer system via a memory bus in response to memory commands received from the memory controller, the memory commands including a first memory command and a subsequent second memory command, the first memory command to cause the memory module to receive or output a first data burst and the second memory command to cause the memory module to receive or output a second data burst, the memory module comprising:

8. The memory module of claim 1, wherein the buffer comprises combinatorial logic, registers, and logic pipelines, and is configured to register an additional clock cycle for transferring the first data burst or the second data burst through the buffer.

Additional CAS latency must be due at least in part to delay through the (data) buffer, and not to registering the control or address signals, or delay associated with memory devices.

POR 35-38;
Sur-Reply 16-19

Petition Conflates Delay Through Data Path and Delay Through C/A Path

Petition

Under the JEDEC standards, “an additional clock cycle” is added to the “CAS latency” of the memory devices to leave enough time for the register on the memory module to perform its functions. See EX1062, p.68 n.1; EX1064, pp.12 (“CAS Latency” of 2, 3, 4, or 5 clock cycles), 14 (permitting additional “Additive Latency” of 1 clock cycle); EX1003, ¶¶359-362. It would have been obvious to add one additional clock cycle to Perego for the same reason, i.e., so that the memory module complies with the timing of the JEDEC standards, and so the “circuitry” has enough time to perform its functions (including “register[ing]” the data signals for interfaces 520a/b with latches 597f-m, blue, below) using “internal” clock circuit 570a-b (purple, below). EX1003, ¶¶359-362; EX1071, 18:65-19:3, 17:61-63, 12:65-13:5, Figs.5B-5C.

Petition 95

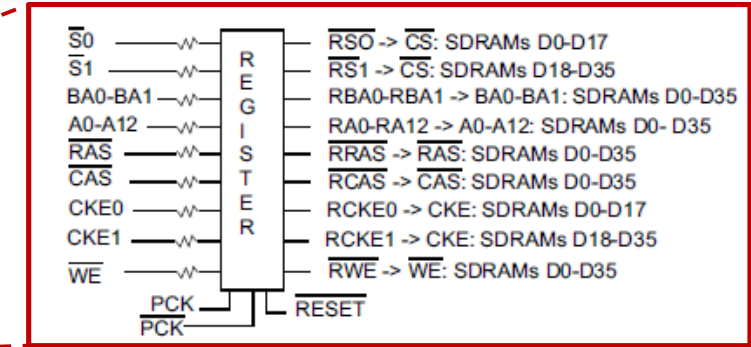
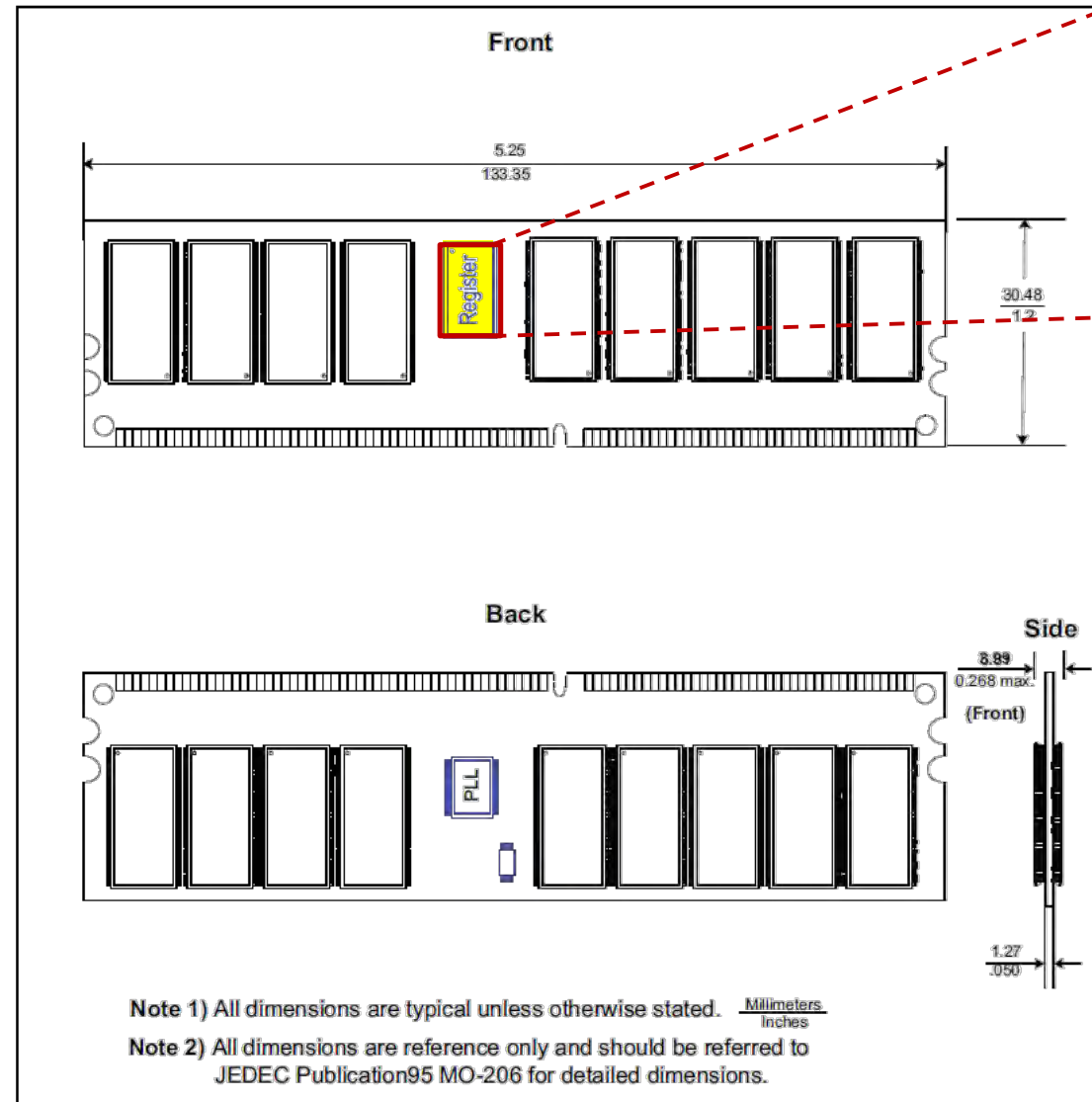
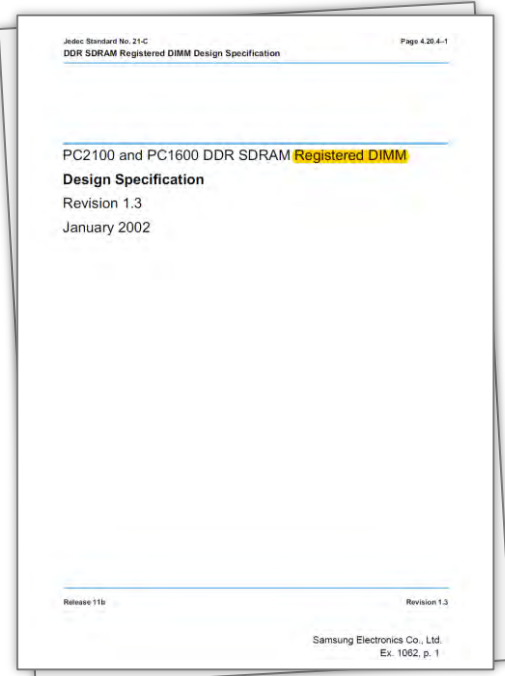
Corresponding to claimed “logic” in element 1b, **not “circuitry” in 1e-1f.**

POR 36-39, 54; Sur-Reply 17, 25

DDR RDIMM Standard, which has only “logic” that registers the command/address signals and no “circuitry” that registers relevant data signals

See EX1062 (JESD21-C), pp. 10-16, 29-35

EX1062 Does Not Disclose Delay Through Data Path Because It Has No Buffers on the Data Path



**RDIMM “register” only registers
command and address signals**

Petition Conflates Delay Through Data Buffer with Delay Parameters in Memory Devices

Petition

Under the JEDEC standards, “an additional clock cycle” is added to the “CAS latency” of the memory devices to leave enough time for the register on the memory module to perform its functions. See EX1062, p.68 n.1; EX1064, pp.12 (“CAS Latency” of 2, 3, 4, or 5 clock cycles), 14 (permitting additional “Additive Latency” of 1 clock cycle); EX1003, ¶¶359-362. It would have been obvious to add one additional clock cycle to Perego for the same reason, i.e., so that the memory module complies with the timing of the JEDEC standards, and so the “circuitry” has enough time to perform its functions (including “register[ing]” the data signals for interfaces 520a/b with latches 597f-m, blue, below) using “internal” clock circuit 570a-b (purple, below). EX1003, ¶¶359-362; EX1071, 18:65-19:3, 17:61-63, 12:65-13:5, Figs.5B-5C.

Petition 95

DDR2 SDRAM Specification, which is a device-level, not module-level specification

See EX1064 (JESD79-2), cover; POR 20-21

DDR device specific parameter, not a module parameter.

See EX1062 (JESD21-C), cover, p. 24; POR 37-38

EX1064 Does Not Disclose Delay Through Data Path Because It Is a Device-Level Specification and Does Not Specify Module-Level Delays



2.2.3 Bank Activate Command

The Bank Activate command is issued by holding $\overline{\text{CAS}}$ and $\overline{\text{WE}}$ high with $\overline{\text{CS}}$ and $\overline{\text{RAS}}$ low at the rising edge of the clock. The bank addresses BA0 ~ BA2 are used to select the desired bank. The row address A0 through A15 is used to determine which row to activate in the selected bank. The Bank Activate command must be applied before any Read or Write operation can be executed. Immediately after the bank active command, the DDR2 SDRAM can accept a read or write command on the following clock cycle. If a R/W command is issued to a bank that has not satisfied the t_{RCDmin} specification, then additive latency must be programmed into the device to delay when the R/W command is internally issued to the device. The additive latency value must be chosen to assure t_{RCDmin} is satisfied. Additive latencies of 0, 1, 2, 3 and 4 are supported. Once a bank has been activated it must be precharged before another Bank Activate command can be applied to the same bank. The bank active and precharge times are defined as t_{RAS} and t_{RP} , respectively. The minimum time interval between successive Bank Activate commands to the same bank is determined by the RAS cycle time of the device (t_{RC}). The minimum time interval between Bank Activate commands is t_{RRD} .

2.2.4.1 Posted $\overline{\text{CAS}}$

Posted $\overline{\text{CAS}}$ operation is supported to make command and data bus efficient for sustainable bandwidths in DDR2 SDRAM. In this operation, the DDR2 SDRAM allows a $\overline{\text{CAS}}$ read or write command to be issued immediately after the $\overline{\text{RAS}}$ bank activate command (or any time during the $\overline{\text{RAS}}$ - $\overline{\text{CAS}}$ -delay time, t_{RCD} , period). The command is held for the time of the Additive Latency (AL) before it is issued inside the device. The Read Latency (RL) is controlled by the sum of AL and the $\overline{\text{CAS}}$ latency (CL). Therefore if a user chooses to issue a R/W command before the t_{RCDmin} , then AL (greater than 0) must be written into the EMRS(1). The Write Latency (WL) is always defined as $\text{RL} - 1$ (read latency - 1) where read latency is defined as the sum of additive latency plus $\overline{\text{CAS}}$ latency ($\text{RL} = \text{AL} + \text{CL}$). Read or Write operations using AL allow seamless bursts (refer to seamless operation timing diagram examples in Read burst and Write burst section).

Classical Hindsight: Insight for Adding Delay in Data Path Came from Netlist's Patents

Petition

Under the JEDEC standards, “an additional clock cycle” is added to the “CAS latency” of the memory devices to leave enough time for the register on the memory module to perform its functions. *See* EX1062, p.68 n.1; EX1064, pp.12 (“CAS Latency” of 2, 3, 4, or 5 clock cycles), 14 (permitting additional “Additive Latency” of 1 clock cycle); EX1003, ¶¶359-362. It would have been obvious to add one additional clock cycle to Perego for the same reason, i.e., so that the memory module complies with the timing of the JEDEC standards, and so the “circuitry” has enough time to perform its functions (including “register[ing]” the data signals for interfaces 520a/b with latches 597f-m, blue, below) using “internal” clock circuit 570a-b (purple, below). EX1003, ¶¶359-362; EX1071, 18:65-19:3, 17:61-63, 12:65-13:5, Figs.5B-5C.

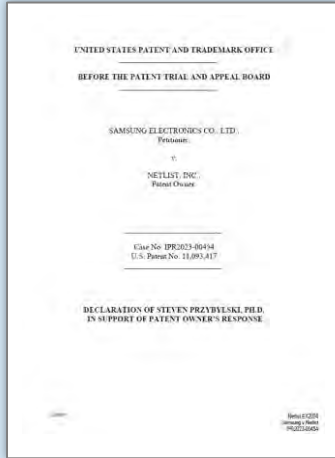
Petition 95

'417 Disclosure

memory array. In certain embodiments, data transfers between the memory controller and the memory module are registered for one additional clock cycle by the circuit 40. The additional clock cycle of certain embodiments is added to the transfer time budget with an incremental overall CAS latency. This extra cycle of time in certain embodiments advantageously provides sufficient time budget to add a buffer which electrically isolates the ranks of memory devices 30 from the memory controller 20. The buffer of certain embodiments comprises combinatorial logic, registers, and logic pipelines. In certain embodiments, the buffer adds a one-clock cycle time delay, which is equivalent to a registered DIMM, to accomplish the address decoding. The one-cycle time delay of certain such embodiments provides sufficient time for read and write data transfers to provide the functions of the data path multiplexer/demultiplexer. Thus,

EX1001 ('417 patent), 22:41-56

Cited Portions of Perego Not Related to Delay Through Data Buffers



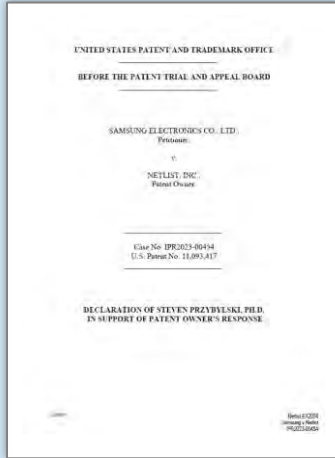
Steven Przybylski, Ph.D.
Expert Witness



184. The Petition concludes this section by saying that a cycle would be added “so the “*circuitry*” has enough time to perform its functions (including “*register[ing]*” the data signals for interfaces 520a/b with latches 597f-m, blue, below) using “internal” clock circuit 570a-b (purple, below).”

185. The Petition recites 3 passages for Perego in support of these assertions: 18:65-19:3, 17:61-63, 12:65-13:5. None of these actually speaks to the question at hand. The passage at 12:65-13:5 is about the global clock source

Perego 12:65-13:5 Relates to Clock Signal Adjustment



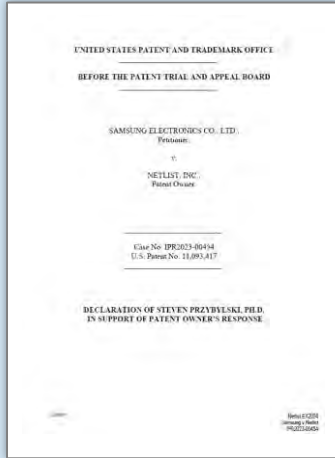
Steven Przybylski, Ph.D.
Expert Witness



the question at hand. The passage at 12:65-13:5 is about the global clock source for the buffer device and not about the timing of data through the buffer device.

The units 570a and 570b are clock circuits for generating and adjusting clock signals so they meet phase requirements for proper operation of the buffer device. Ex. 1071, 12:12:52-13:5. They may include a “Direct Rambus Clock Generator” which was a device that Rambus specified and a variety of semiconductor vendors produced. Perego discloses that this functionality can be within the buffer device 405 instead of being a discrete separate integrated circuit. Regardless of its location, its functionality is the same. Ex. 2035 (Direct Rambus Clock Generator). Specifically it “includes signals to synchronize the Direct Rambus channel clock to an external system or processor clock.” Ex. 2035

Perego 12:65-13:5 Relates to Aligning Phases of CLK and CLKB



Steven Przybylski, Ph.D.
Expert Witness



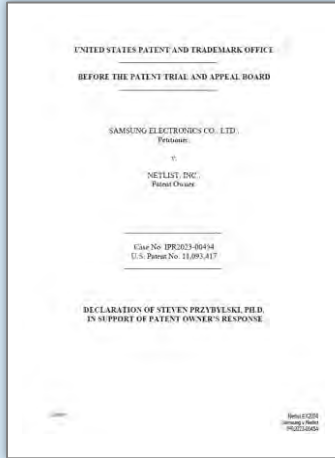
EX2024, ¶¶ 184-185,
POR 38; EX1071
(Perego), 12:65-13:5

(Direct Rambus Clock Generator), p. 1. The nature of the Direct Rambus Channel is such that the phase of the ClockToMaster must be adjusted so that the clock signal arrives at the buffer device in phase alignment with the buffer-devices internal clock so that the incoming data can be properly captured. This is what the clock generator does. Ex. 2035 (Direct Rambus Clock Generator), p. 1 (“Synchronizes the Clock Domains of the Rambus Channel With An External System or Processor Clock.”). The signal ClockToMaster and the buffer device internal clock are provided to the PCLKM and SyncClkN input puts to the clock generator and it adjusts the phase of CLK and CLKB so that those two inputs are phase aligned. This is all it does and it is only relevant to the Direct RDRAM-based embodiments. It is irrelevant to the question of whether there is an extra clock cycle of latency added to the path through the buffer circuit.

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Netlist slide, p. 89

Other Cited Portions of Perego Not Related to MUX/DeMUX Timing



Steven Przybylski, Ph.D.
Expert Witness



186. The passage at 17:61-63 is about the structure of the multiplexer/demultiplexer, not its timing. And finally, the passage at 18:65-19:3 is about whether the multiplexer/demultiplexer 597 implements a full or partial crossbar. None of the support offered actually supports the statements made about the delay experienced by data as it traverses the buffer device.

Reasoning in Reply Still Fails

Reply

36-37 (citing EX1062, 68 n.1),⁵ but the Petition pointed to that disclosure to show that if *any* signal is registered on a memory module — including data signals as in *Perego* — it was obvious to delay the signal for one full clock cycle to allow enough time for the functions of the register. Pet. 94-96, 118-19; *see also Intel*, 61

Reply 18-20

Essentially an improper “common sense” reasoning

- If registering C/A results in one clock cycle delay, then obvious for the DQ signals
- *But:*
 - No prior disclosure of increasing overall CAS latency for delay on data path
 - *Perego* does not disclose it
 - Increase in column access time due to C/A processing

Sur-Reply 17-20

Questions Raised by the Board at Institution: Petitioner Abandons Reliance on AL

latency. Prelim. Resp. 45 (citing Ex. 1064, 24; Ex. 1075, 15:52–57). Thus, according to Patent Owner, the CAS latency of the memory module would equal the actual operational CAS latency of the memory device, rather than being greater than the actual operational CAS latency, as recited in claim 1. Prelim. Resp. 45. We encourage the parties to address this argument further during trial because, to the extent the JESD79-2’s disclosure of AL is specific to the memory devices themselves, it would appear that this AL would impact the actual operational CAS latency of the memory device. In

Institution Decision 35

Petitioner has abandoned this theory, arguing for the first time in reply that it does not rely on AL to teach this claim element.

Because Additive Latency (AL) is specific to the memory devices, it cannot satisfy the claim requirement that “the overall CAS latency of the memory module is *greater than* an actual CAS latency of each of the memory devices” (‘417 claim 1).

Netlist argues that “Additive Latency (AL)” is only relevant to the memory devices, not “latency at the module level.” POR 37-38 (citing ID 35). But the Petition merely cited “Additive Latency” to show that latency is measured in *full* clock cycles for DDR2 memory devices, Pet. 92-95, which Netlist does not dispute

Reply 19-20

Questions Raised by the Board at Institution: Still No Evidence that DDR2 RDIMM Standard Specifies a One-Clock-Cycle Delay

Patent Owner also argues that Petitioner's reliance on the DDR RDIMM specification's disclosure of adding an extra clock cycle on the memory module is misplaced because (1) "Perego expressly distinguishes its data buffer to that on a traditional RDIMM" and (2) "no similar language is found in JEDEC's DDR2 RDIMM specification." Prelim. Resp. 43 (citing Ex. 1071, 6:27–33; Ex. 1066, 94–96; Ex. 1062, 68). As to Patent Owner's first argument, we disagree for the reasons given above in § II.E.2.d based on Perego's disclosure of wanting to maintain backward compatibility. Ex. 1071, 2:4–6, 6:27–33, 6:37–39. As to Patent Owner's second argument, some additional development of the record would be helpful during trial.

Institution Decision 35-36

Petitioner identifies **no such disclosure** in the JEDEC Standard, citing instead a Micron product datasheet.

As Netlist correctly noted, the language relied upon by Petitioner in the DDR version of the JESD21-C Standard (EX1062) is **not found in the DDR2 version (EX1066)**.

⁵ Netlist also suggests "no similar language" exists for DDR2 RDIMM memory modules, POR 37; ID 35-36, which is incorrect. EX1109, 1 ("registered mode will add one clock cycle to CL [CAS latency]" for DDR2 RDIMM).

Reply 18 n.5

There Is No Estoppel

Limitation in IPR2017-00547	Why No Estoppel
wherein the first logic element is configured to determine a latency value based on a previous memory command received by the memory module from the memory controller, and wherein the first logic element controls the second logic element to selectively enable the data communication according to the latency value EX1030 (FWD in IPR2017-00549), p.3 (claim 1 of U.S. Patent No. 8,765,364)	• No requirement that the delay be associated with “data transfers through the circuitry [data buffer]” — Delay could be due to time needed to decode and process command/address signals through an RCD register, for example • No requirement that the “overall CAS latency of the memory module” be “greater than an actual operational CAS latency of each of the memory devices”

Ground 1: Perego and JESD79-2

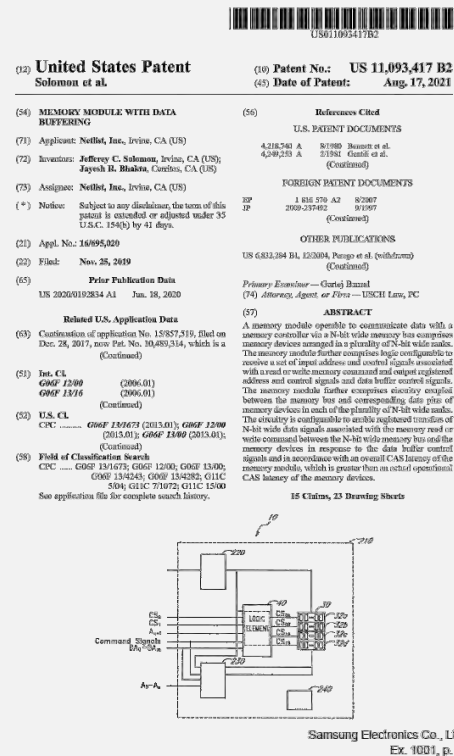
1. Perego and JESD79-2 do not disclose or suggest input “chip select signals”
2. No motivation to modify Perego to add input chip selects as Petitioner proposed
3. Perego and JESD79-2 do not disclose or suggest the CAS-latency claim elements
4. Perego and JESD79-2 **do not disclose or suggest** a plurality of “ranks”

Missing Limitation #3 in '417 Patent: Plurality of Ranks

1. A memory module operable in a computer system to communicate data with a memory controller of the computer system via a N-bit wide memory bus in response to read or write memory commands received from the memory controller, the memory bus including address and control signal lines and data signal lines, the memory module comprising:

memory devices mounted on the printed circuit board and arranged in a plurality of N-bit wide ranks, wherein the plurality of N-bit wide ranks correspond to respective ones of the plurality of registered chip select signals such that each of the plurality of registered chip select signals is received by memory devices one respective N-bit wide rank of the plurality of N-bit-wide ranks, wherein one of the plurality of N-bit wide ranks including memory devices receiving the registered chip select signal having the active signal value and the other registered address and control signals is configured to receive or output a burst of N-bit wide data signals in response to the read or write command; and

Must have multiple ranks corresponding to registered chip select signals



Missing Limitation #3 in '215 Patent: Plurality of Ranks



1. A memory module operable in a computer system to communicate data with a memory controller of the computer system via a memory bus in response to memory commands

received
mands in
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cause the
burst an
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memory

a plurality of memory integrated circuits mounted on the printed circuit board and arranged in a plurality of ranks including a first rank and a second rank, the plurality of memory integrated circuits including at least one first memory integrated circuit in the first rank and at least one second memory integrated circuit in the second rank, wherein the first rank is selected to receive or output the first data burst in response to the first memory command and is not selected to communicate data with the memory controller in response to the second memory command, and wherein the second rank is selected to receive or output the second data burst in response to the second memory command and is not selected to communicate data with the memory controller in response to the first memory command;

Purported “Ranks”

Ground 1 teaches “*memory devices [e.g., 360, 410, below] mounted on the printed circuit board [from [1.b] (pp.42-43)] and arranged in a plurality of N-bit wide [e.g., 64-bit wide] ranks [e.g., green, blue].*” EX1003, ¶¶274-296.

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.,

Petitioner,

v.

NETLIST, INC.,

Patent Owner.

Case IPR2023-00454
Patent 11,093,417

PETITION FOR INTER PARTES REVIEW OF
U.S. PATENT NO. 11,093,417

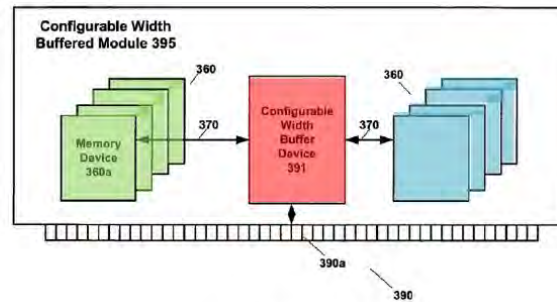


Fig. 3C

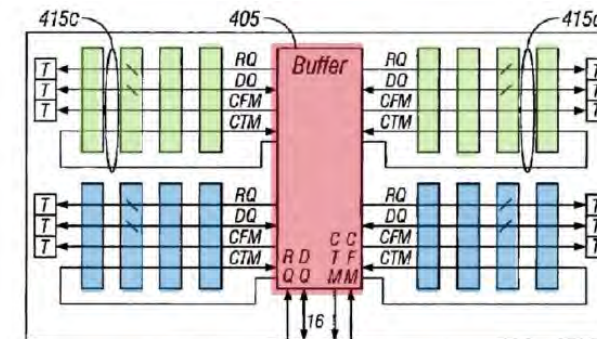


FIG. 4B

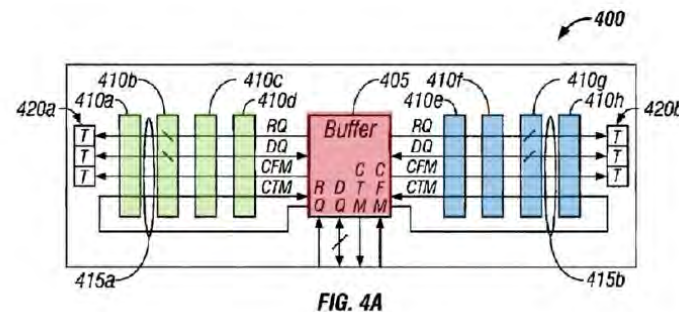


FIG. 4A

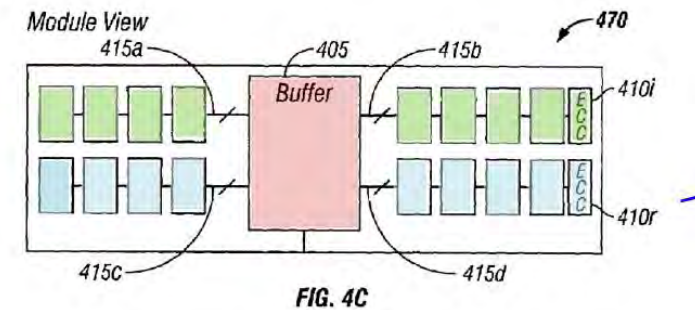
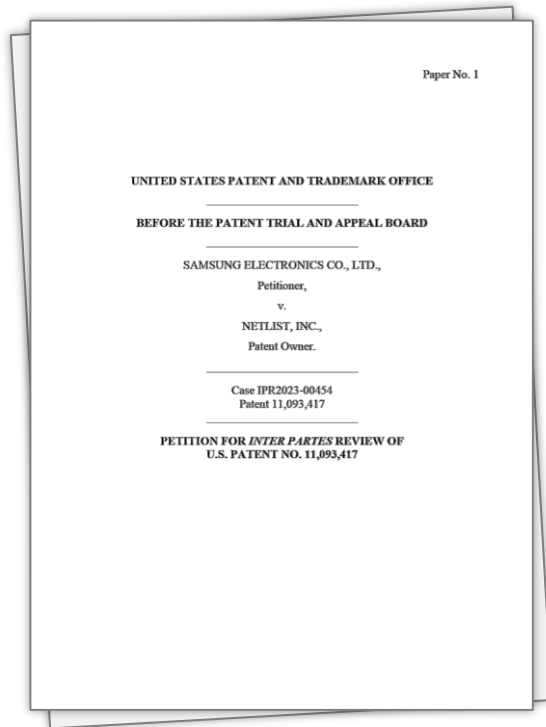


FIG. 4C

Purported Ranks Identified in Petition



Perego discloses “grouping memory devices into multiple independent target subsets (i.e. more *independent banks*),” EX1071, 15:37-45, which renders obvious the claim limitation “*ranks*” as properly construed (pp.26-28). EX1003, ¶276.

Perego also teaches that the “*ranks*” are each “*N-bit wide*” (e.g., 64-bits wide): For example, Perego teaches that “interfaces 520a and 520b [below] may be programmed to connect to 16‘x4’ width memory devices, 8‘x8’ width memory devices or 4‘x16’ width memory devices,” EX1071, 14:10-15, Figs.5A-5B, resulting in a “*rank*” with a bit-width of 64 bits, consistent with the standard DIMM layout shown above, *see, e.g.*, EX1062, p.13 (describing a “x64 DIMM, populated as two physical banks [i.e., “*ranks*,” *see* pp.26-28] of [eight] x8 DDR SDRAMs [i.e., D0-D7, and D8-D15]”). The terms ‘x4’, ‘x8’ and ‘x16’—pronounced “by four,” “by eight,” and “by sixteen”—refer to the data width of a single memory device, EX1069, p.1, so eight ‘x8’ memory devices results in a total bit-width of 64 bits. EX1003, ¶¶279-280.

Only One Device in a Purported Rank Responds at a Time

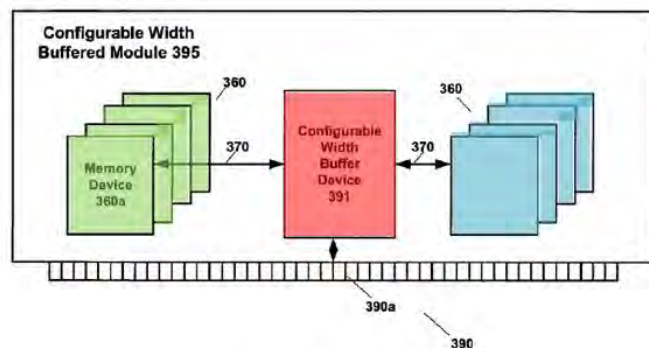


Fig. 3C

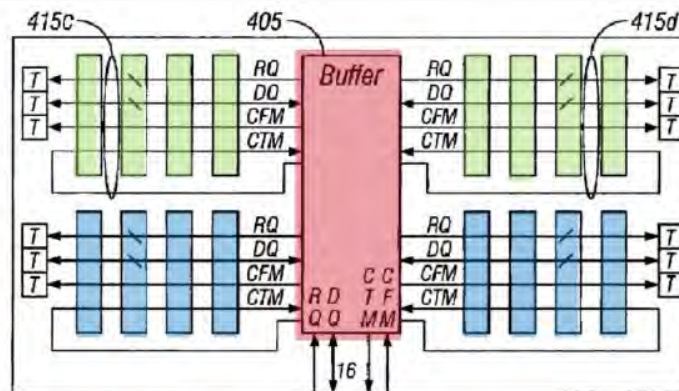


FIG. 4B

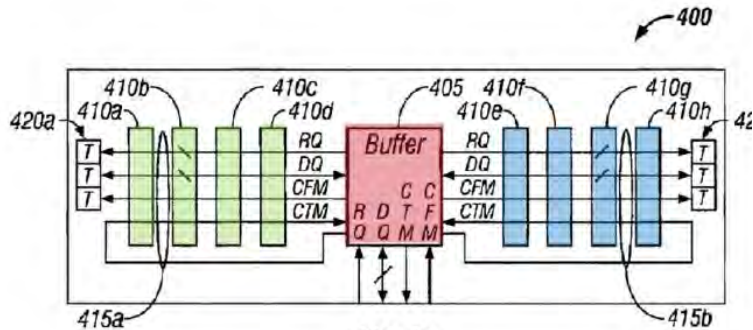


FIG. 4A

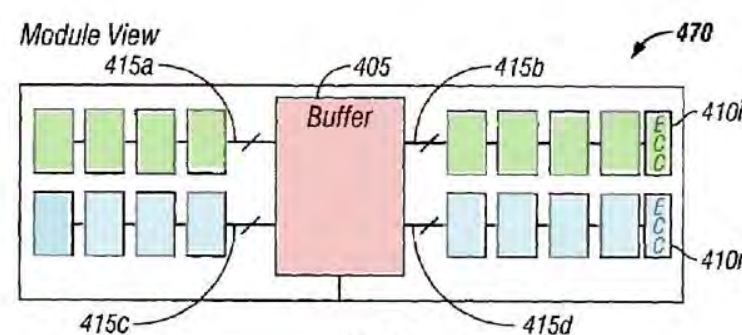
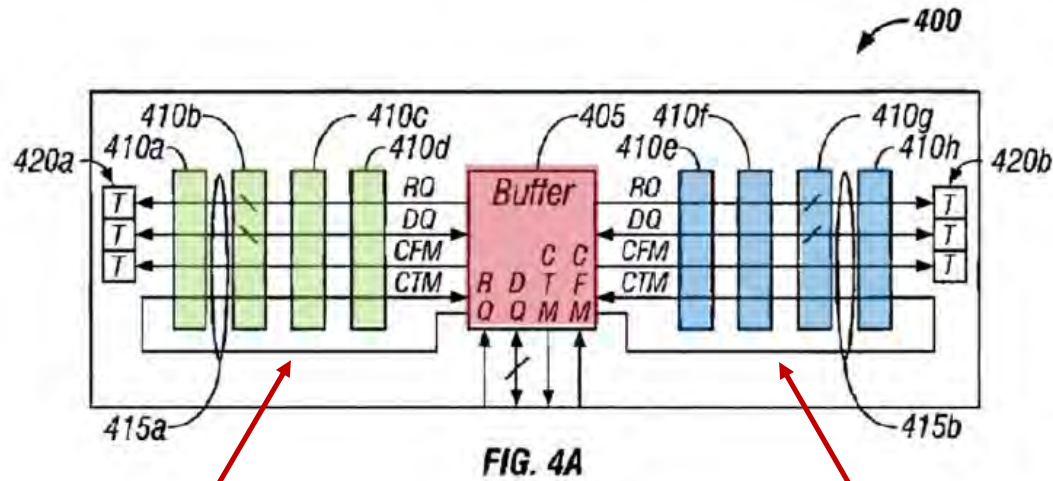


FIG. 4C

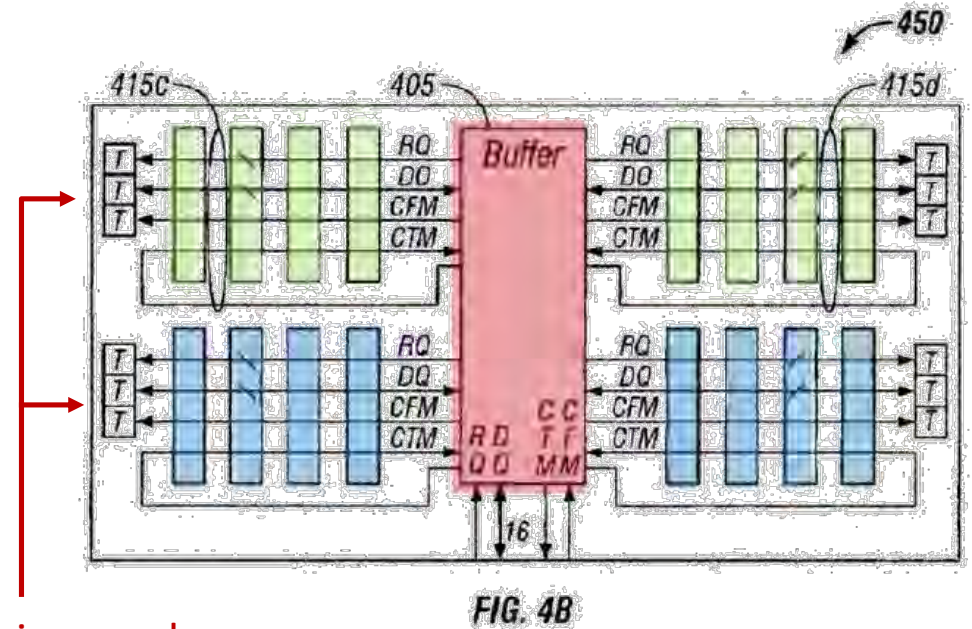
**Each memory device is accessed individually;
the memory devices do not “act together”.**

Purported Ranks Identified in Petition Do Not Read/Write Full 64-bit Width Specified by JEDEC



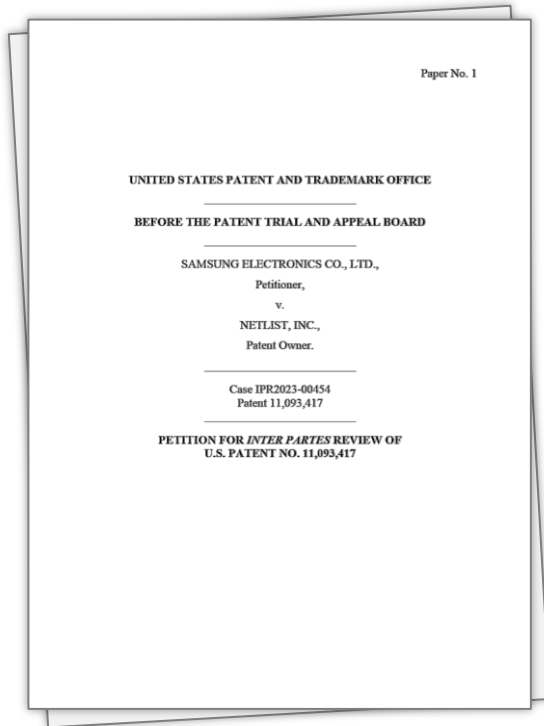
4 x16 devices
on channel 415a

4 x16 devices
on channel 415b



8 x8 devices each
on channels 415c/d and 415a/b

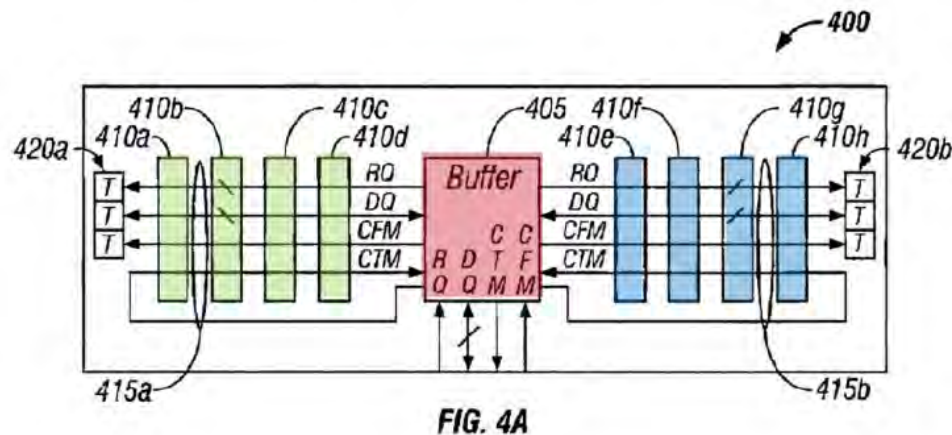
Purported Disclosure or Suggestion of “Ranks”



Perego discloses “grouping memory devices into multiple independent target subsets (i.e. more *independent banks*),” EX1071, 15:37-45, which renders obvious the claim limitation “*ranks*” as properly construed (pp.26-28). EX1003, ¶276.

Perego also teaches that the “*ranks*” are each “*N-bit wide*” (e.g., 64-bits wide): For example, Perego teaches that “interfaces 520a and 520b [below] may be programmed to connect to 16‘x4’ width memory devices, 8‘x8’ width memory devices or 4‘x16’ width memory devices,” EX1071, 14:10-15, Figs.5A-5B, resulting in a “*rank*” with a bit-width of 64 bits, consistent with the standard DIMM layout shown above, *see, e.g.*, EX1062, p.13 (describing a “x64 DIMM, populated as two physical banks [i.e., “*ranks*,” *see* pp.26-28] of [eight] x8 DDR SDRAMs [i.e., D0-D7, and D8-D15]”). The terms ‘x4’, ‘x8’ and ‘x16’—pronounced “by four,” “by eight,” and “by sixteen”—refer to the data width of a single memory device, EX1069, p.1, so eight ‘x8’ memory devices results in a total bit-width of 64 bits. EX1003, ¶¶279-280.

Passage Relied on by Petitioner



If the total number of secondary channel signal lines per configurable width buffer device **391**, $W_{DP,S}$ is greater than the minimum number required per transaction, $W_{DPT,S}$, then configurable width buffer device **391** may employ a configurable datapath router within interface **591** to route requests between the primary channel and the target subset of secondary channel signal lines for each transaction. According to a preferred embodiment, the target subset of secondary channel signal lines may be selected via address bits provided as part of the primary channel request. By accessing a subset of secondary channel signal lines per transaction, a number of benefits may be derived. One of these benefits is reduced power consumption. Another benefit is higher performance by grouping memory devices into multiple independent target subsets (i.e. more independent banks).

“Independent Banks” Unrelated to “Ranks”

Petition

Perego discloses “grouping memory devices into multiple independent target subsets (i.e. more *independent banks*),” EX1071, 15:37-45, which renders obvious the claim limitation “*ranks*” as properly construed (pp.26-28). EX1003, ¶276.

Petition 67

Dr. Wolfe
Samsung Expert Witness

Q. So why don't you read a few lines down, column 15, lines 40 to 45.

A. Again, I don't think it has to do with enabling or disabling devices. I think it simply has to do with being able to impact the number of independent banks that are open at a time.

Q. When you say “independent banks,” which -- what do you mean?

A. It would mean the number of page registers which can be activated corresponding to different addresses.

Not
“rank”

EX2003 (Wolfe Depo Tr. in IPR2022-00615), 203:15-25

Petition Identifies “Target Subsets” That Are Not Ranks

Petition

Perego discloses “grouping memory devices into multiple independent target subsets (i.e. more *independent banks*),” EX1071, 15:37-45, which renders obvious the claim limitation “*ranks*” as properly construed (pp.26-28). EX1003, ¶276.

Petition 67

Steven Przybylski, Ph.D.
Netlist Expert Witness

ranks. Ex. 2033 (Wolfe Deposition Transcript), 71:5-72:4. But this passage has nothing to do with ranks, much less ranks according to Petitioner’s proposed construction. Indeed, in a prior deposition regarding a related Netlist patent, Dr. Wolfe testified: “I do not think that this paragraph [the same paragraph in Perego] specifies how ranks are selected or enabled,” and he further testified that “independent banks” refers to “the number of page registers which can be activated corresponding to different addresses” “throughout the system.” Ex. 2003, 202:8-204:10. Indeed, this paragraph of Perego states that “the target subset of secondary channel lines may be selected via address bits,” which are distinct from the chip-select signals required by Petitioner’s own proposed construction. See also Ex. 1069, p. 2 (stating that “the chip-select bus, is essential in a JEDEC-style memory system”).

EX2024, ¶ 165

Perego Can Address/Select Any Number of Channels

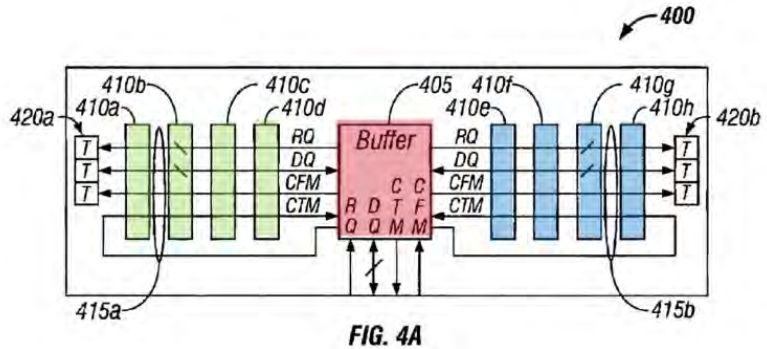


FIG. 4A

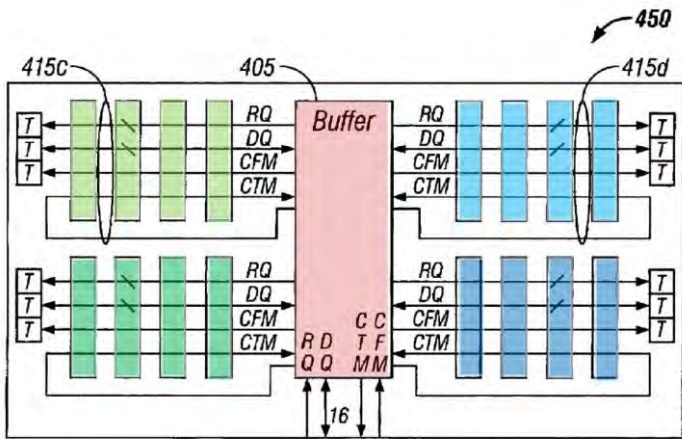


FIG. 4B

(Petition 47; each color block of 4 devices a channel)

may be implemented on the module. The width of the channel refers to the number of parallel signal paths included in each channel. FIG. 4B illustrates a quad-channel module 450 having channels 415a–415d. In this embodiment, channels 415c and 415d are routed in parallel with channels 415a and 415b to support more memory devices (e.g., 32 memory devices). By incorporating more channels and additional memory devices, module 450 (FIG. 4B) may be implemented in memory systems that require large memory capacity, for example, in server or workstation class systems.

In alternate embodiments, channels 415a and 415b may operate simultaneously with channels 415c and 415d to realize greater bandwidth. By operating a plurality of channels in parallel, the bandwidth of the module may be increased independently of the memory capacity. The advantages of greater bandwidth may be realized in conjunction with larger capacity as more modules incorporated by the memory system 305 (see FIG. 3B) increase the system

Patent Owner Netlist Outline

1. The '417 and '215 Patents
2. All of Petitioner's Grounds are Deficient
3. The Netlist Claims are Directed to Memory Modules
4. Perego vs. JEDEC-Compliant Memory Architectures
5. Ground 1: Perego and JESD79-2
- 6. Ground 2: Ground 1 + Ellsberry**
7. Ground 3: Ground 1 + Halbert

Ground 2: Ground 1 + Ellsberry

1. Ellsberry is not a “printed publication” pursuant to Section 311(b)
2. Ellsberry is **not** prior art because the '087 Provisional predates Ellsberry
3. Petitioner’s mapping of Ellsberry’s disclosure
4. No motivation to combine Ellsberry and Perego

011905

113009 U.S. PTO
60/645087

US011093417B2

Provisional application No. 60/645,087, filed on Jan. 19, 2005, provisional application No. 60/588,244, filed on Jul. 15, 2004, provisional application No. 60/550,668, filed on Mar. 5, 2004, provisional application No. 60/575,595, filed on May 28, 2004, provisional application No. 60/590,038, filed on Jul. 21, 2004.

The '417 and '215 Patents Properly Claim Priority to the '087 Provisional Application Through the '537 Patent

58110
013905

13905 U.S. PTO
60/645087
013905

Provisional Application COVER SHEET

Attorney Docket No.: NETL-030PR
Inventor: Jeffrey Solomon
Title: RANK BUFFERED DUAL IN-LINE MEMORY MODULE
Express Mail Label No.: EV 318992171 US

Direct all correspondence to Customer No.: 20995 Date: January 19, 2005 Page 1 of 1

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

The following enclosures are transmitted herewith to be filed in the Provisional Patent Application of:

Inventor : Jeffrey Solomon
Residence Address : 16 Silver Fir, Irvine, California 92604

APPLICATION ELEMENTS:

(X) Specification in seven (7) pages.
(X) Drawings in one (1) sheet.
(X) Return prepaid postcard.

FILING FEES:

(X) A check in the amount of \$200.00 is enclosed to cover the filing fee.

This invention WAS NOT made by an agency of the United States Government or under a contract with an agency of the United States Government.

The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Account No. 11-1410.

Bruce S. Kohnkowitz
Registration No. 47,677
Attorney of Record
Customer No. 20,995
(949) 760-0464

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013905

Samsung Electronics Co., Ltd.
Ex. 1005, p. 1

US007537B2

United States Patent
Solomon et al.

(19) Patent No.: US 7,532,537 B2
(45) Date of Patent: May 12, 2009

(54) MEMORY MODULE WITH A CIRCUIT PROVIDING LOAD ISOLATION AND MEMORY DOMAIN TRANSLATION

(75) Inventors: Jeffrey C. Solomon, Irvine, CA (US); Jayesh R. Bhakta, Carlsbad, CA (US)

(73) Assignee: Netlist, Inc., Irvine, CA (US)

(* *) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 170 days.

(21) Appl. No.: 11/038,875
(22) Filed: Jan. 19, 2006

(65) Prior Publication Data
US 2006/02586 A1 Nov. 23, 2006

Related U.S. Application Data
(63) Continuation-in-part of application No. 11/173,175, filed on Jul. 1, 2005, now Pat. No. 7,289,386, which is a continuation-in-part of application No. 11/075,395, filed on Mar. 7, 2005, now Pat. No. 7,286,436.
(60) Provisional application No. 60/645,087, filed on Jan. 19, 2005, provisional application No. 60/588,244, filed on Jul. 15, 2004, provisional application No. 60/550,668, filed on Mar. 5, 2004, provisional application No. 60/575,595, filed on May 28, 2004, provisional application No. 60/590,038, filed on Jul. 21, 2004.

(51) Int. Cl.
G11C 8/00 (2006.01)

(52) U.S. Cl.
365/230.06, 365/51, 365/233.13

(58) Field of Classification Search
365/52, 191, 230.03, 230.06, 230.08, 233.1, 365/233.13
See application file for complete search history.

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OTHER PUBLICATIONS
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(74) Attorney, Agent, or Firm: Kohnke, Martens, Olson & Bear LLP

Primary Examiner: Van Thi Nguyen
Assistant Examiner: Alexander Sokolov

(57) **ABSTRACT**
A memory module includes a plurality of memory devices and a circuit. Each memory device has a corresponding load. The circuit is electrically coupled to the plurality of memory devices and is configured to be electrically coupled to a memory controller of a computer system. The circuit selectively isolates one or more of the loads of the memory devices from the computer system. The circuit comprises logic which translates between a system memory domain of the computer system and a physical memory domain of the memory module.

44 Claims, 23 Drawing Sheets

Samsung Electronics Co., Ltd.
Ex. 1032, p. 1

The present application is a continuation-in-part of U.S. patent application Ser. No. 11/173,175, filed Jul. 1, 2005 now U.S. Pat No. 7,289,386, which claims the benefit of U.S. Provisional Application No. 60/588,244, filed Jul. 15, 2004 and which is a continuation-in-part of U.S. patent application Ser. No. 11/075,395, filed Mar. 7, 2005 now U.S. Pat No. 7,283,436, which claims the benefit of U.S. Provisional Application No. 60/550,668, filed Mar. 5, 2004, U.S. Provisional Application No. 60/575,595, filed May 28, 2004, and U.S. Provisional Application No. 60/590,038, filed Jul. 21, 2004. U.S. patent application Ser. Nos. 11/173,175 and 11/075,395, and U.S. Provisional Application Nos. 60/588,244, 60/550,668, 60/575,595, and 60/590,038 are each incorporated in its entirety by reference herein. The present application also claims the benefit of U.S. Provisional Application No. 60/645,087, filed Jan. 19, 2005, which is incorporated in its entirety by reference herein.

Allegedly Missing Disclosure from the '087 Provisional

(12) United States Patent
Solomon et al.

(10) Patent No.: US 11,093,417 B2
(45) Date of Patent: Aug. 17, 2021

active signal value, wherein the logic is further configurable to output data buffer control signals in response to the read or write memory command;

(21) Appl. No. 16/095,020

Original Patent Application
US 6,832,284 B1, 12/2004, Pango et al. (withdrawn)

circuitry coupled between the data signal lines in the N-bit wide memory bus and corresponding data pins of memory devices in each of the plurality of N-bit wide ranks, the circuitry being configurable to transfer the burst of N-bit wide data signals between the N-bit wide memory bus and the memory devices in the one of the plurality of N-bit wide ranks in response to the data buffer control signals and in accordance with an overall CAS latency of the memory module;



IPR2023-00454: EX1001 ('417 patent), claim 1

(12) United States Patent
Solomon et al.

(10) Patent No.: US 9,858,215 B1
(45) Date of Patent: Jan. 2, 2018

(54) MEMORY MODULE WITH DATA

FOREIGN PATENT DOCUMENTS

JP 1 816 579 A2 8/2007

JP 2009-237491 9/2007

(71) Applicant: Netlist, Inc., Irvine, CA (US)

(Continued)

(72) Inventor: Jeffrey C. Solomon, Irvine, CA (US);
James J. Whitaker, San Jose, CA (US)

logic coupled to the buffer and configured to respond to the first memory command by providing first control signals to the buffer to enable communication of the first data burst between the at least one first memory integrated circuit and the memory controller through the buffer, wherein the logic is further configured to respond to the second memory command by providing second control signals to the buffer to enable communication of the second data burst between the at least one second memory integrated circuit and the memory controller through the buffer, the second control signals being different from the first control signals.



IPR2023-00455: EX1001 ('215 patent), claim 1

Petitioner Alleges Only One Missing Disclosure from the '087 Provisional

Petitions

EX1005, Fig.1; EX1003, ¶¶58-60. But the '087 Provisional fails to disclose data buffer control signals for enabling the transfer of data bursts through the buffer in response to read or write memory commands. EX1003, ¶61. The '087 Provisional

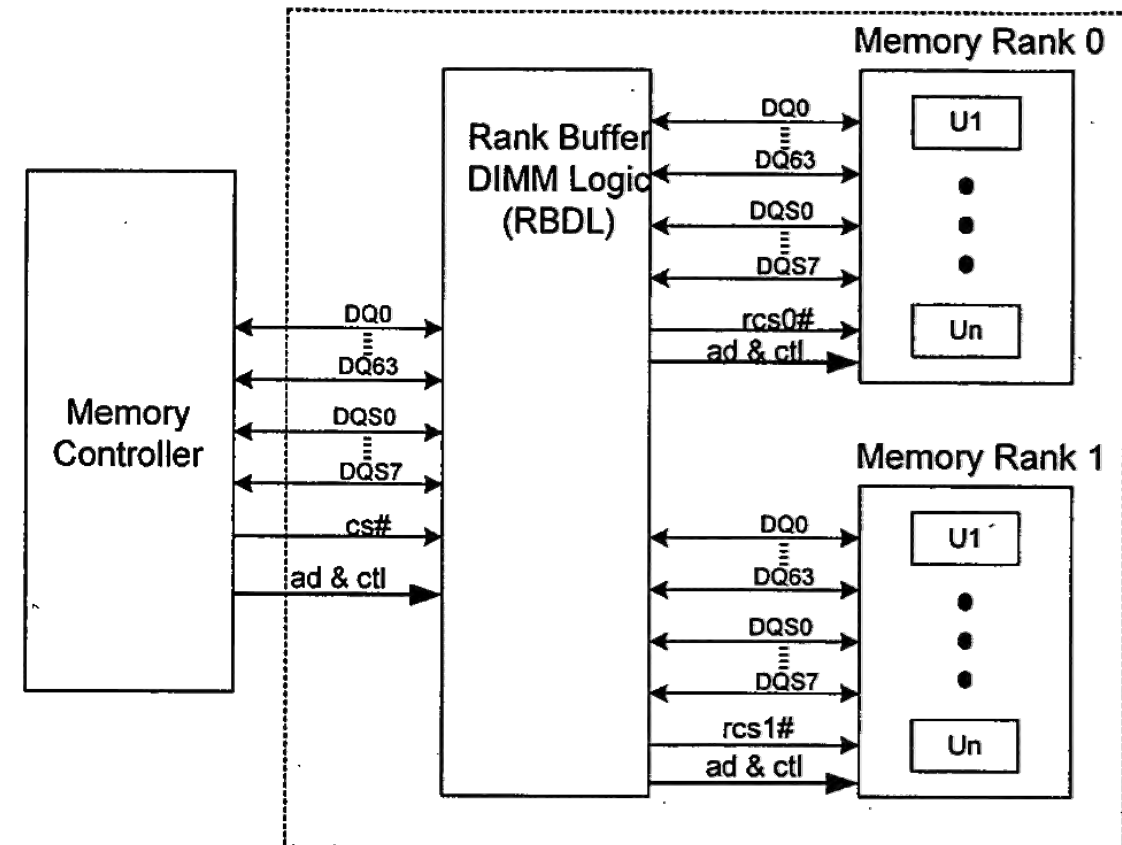
IPR2023-00454: Petition 7

EX1005, Fig.1; EX1003, ¶¶58-60. But the '087 Provisional fails to disclose different first/second control signals to the buffer for enabling the communication of data bursts through the buffer in response to memory commands. EX1003, ¶61.

IPR2023-00455: Petition 7

Would a POSITA understand that the inventors possessed the claimed control signals?

FIGURE 1:



Block Diagram: Rank Buffered DIMM Memory Sub-system

EX1005 ('087 provisional), Fig. 1

'087 Provisional Application

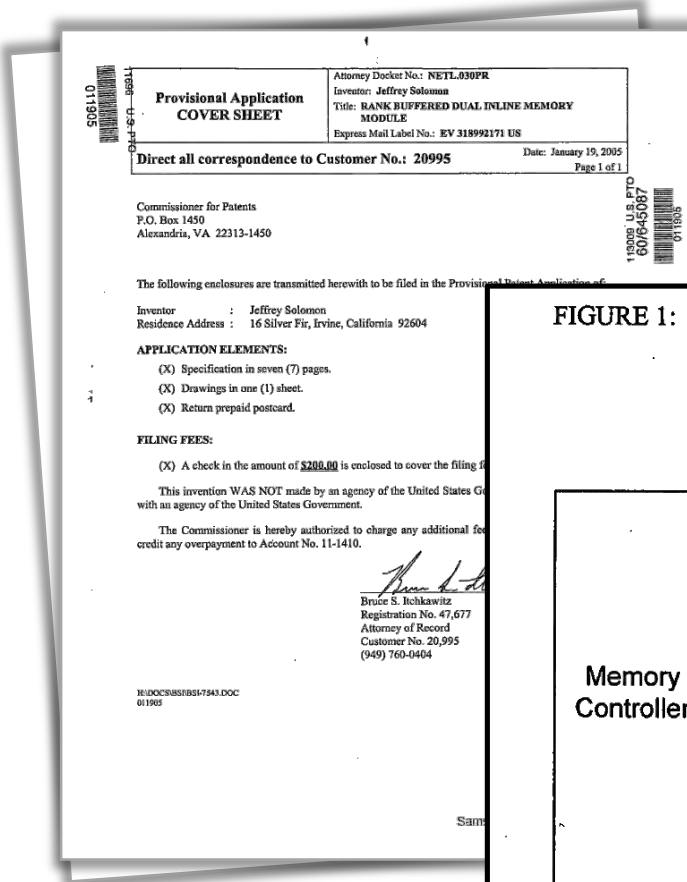
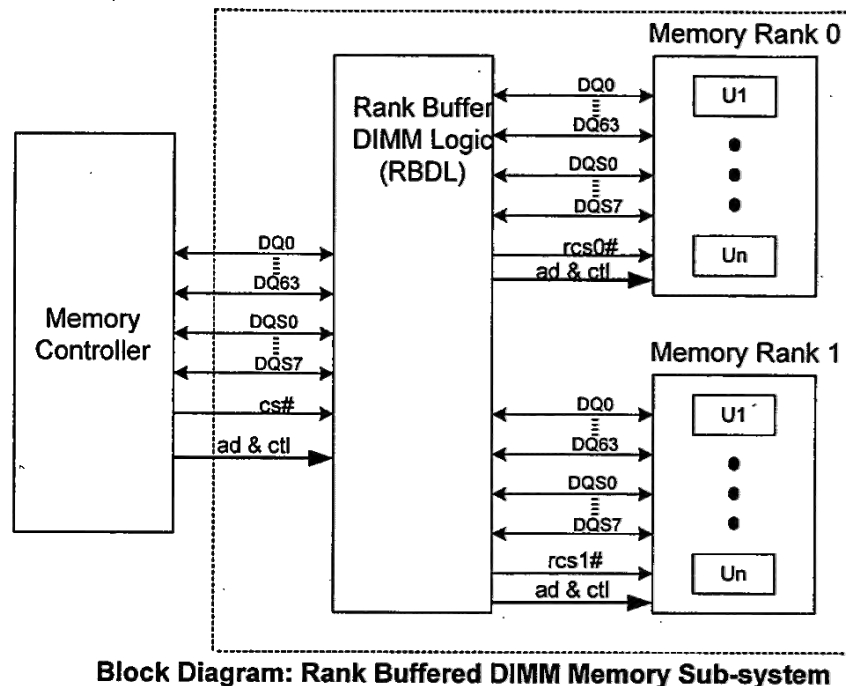


FIGURE 1:



[0007] Figure 1 schematically illustrates a block diagram of a dual inline memory module (DIMM) memory subsystem in accordance with embodiments described herein. The DIMM of Figure 1 comprises a logic translation element, labeled as “Rank Buffer DIMM Logic (RBDL).” In certain embodiments, the logic translation element is electrically connected to the memory controller of the computer system and is electrically connected to the ranks of memory devices (or chips) of the DIMM. In certain embodiments, the logic translation element comprises address decoding logic which transparently translates from a system memory density domain of the computer system to a physical memory density domain of the DIMM.

[0008] In certain embodiments, the logic translation element comprises a data path multiplexer/demultiplexer which logically isolates the ranks of memory devices from one another. The data path multiplexer/demultiplexer of certain embodiments advantageously diminishes the effects of jitter and other sources of noise, and simplifies various other aspects of operation of the memory module, including, but not limited to, setup-and-hold time, clock skew, package skew, and process, temperature, voltage, and transmission line variations.

'087 Provisional Application

Provisional Application
COVER SHEET

Attorney Docket No.: NETL-030PR
Inventor: Jeffrey Solomon
Title: RANK BUFFERED DUAL INLINE MEMORY
MODULE
Express Mail Label No.: EV 318992171 US

Direct all correspondence to Customer No.: 20995 Date: January 19, 2005
Page 1 of 1

Commissioner for Patents
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Residence Address : 16 Silver Fir, Irvine, California 92604

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(X) Specification in seven (7) pages.
(X) Drawings in one (1) sheet.
(X) Return prepaid postcard.

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(X) A check in the amount of \$200.00 is enclosed to cover the filing fee.

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Registration No. 47,677
Attorney of Record
Customer No. 20,995
(949) 760-0464

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01/19/05

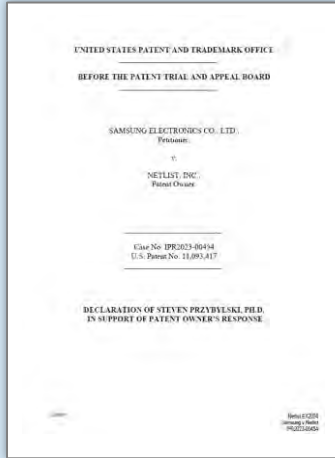
Samsung Electronics Co., Ltd.
Ex. 1005, p. 1

[0017] In certain embodiments, the multiplexer/demultiplexer advantageously provides DQ/DQS paths for each rank of memory devices which are separate from one another, and which are separate from the memory controller of the computer system. In certain such embodiments, data transfers between the memory controller and the DIMM are registered for one additional clock cycle by the logic translation element. The additional clock cycle of certain embodiments is added to the transfer time budget with an incremental overall CAS latency. Thus, for example, a DDR2 400-MHz memory system in accordance with embodiments described herein has an overall CAS latency of four, and uses memory devices with a CAS latency of three.

Dr. Przybylski Confirms That a POSITA Would Understand That the Inventors Were in Possession of the Inventions

Detailed explanation of why a POSITA reading the '087 Provisional would understand that, among other things:

1. The “Rank Buffer DIMM Logic transfers ... bursts of data between the DRAMs in the memory ranks and the memory bus connecting the module to the memory controller.”
2. The “data path multiplexer/demultiplexer in the RBDL would have to transfer read data bursts from one of the ranks of DRAMs to the memory bus towards the memory controller, depending on the specific read command being executed by the module (and vice versa for write commands).”
3. The “claimed ‘circuitry’ is at least in part said ***multiplexer/demultiplexer***, which a POSITA would understand ***necessarily would receive control signals*** (i.e., the claimed ‘data buffer control signals’) ***from the command decode circuitry*** (a POSITA would understand necessarily that the module described in the '087 Provisional would receive commands from an external memory controller and would include ***command decode circuitry to interpret those commands***).”



Steven Przybylski, Ph.D.
Expert Witness

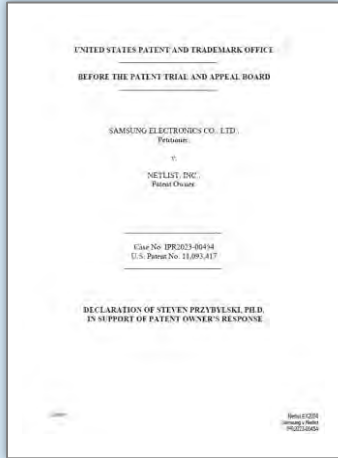


Dr. Przybylski Confirms That Petitioner's Alternatives Were Not Viable

Contrary to Petitioner's argument that one could just use chip select signals:

1. "This argument does not apply at all to reads, during which the RBDL must select the data coming from the one addressed Rank and transfer it to the memory bus."
2. "[F]or write commands, the **RBDL must understand when to forward data from the memory bus to the rank data buses. That 'when' information must be provided by data buffer control signals.**"

Petitioner has NOT rebutted this testimony



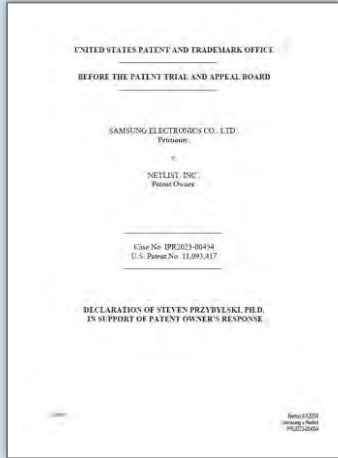
Steven Przybylski, Ph.D.
Expert Witness



Dr. Przybylski Confirms That Petitioner's Alternatives Were Not Viable

Contrary to Petitioner's argument that one could use DQS preambles:

- “[A]t least some of the time, there is no discernable transition in the voltage on the DQS signal at the start of the preamble,” which results in the “lack of a **reliably discernable** preamble,” and thus a POSITA would understand that such preambles cannot be relied upon to control data transfers through the buffer.
- **Dr. Wolfe Agreed that the preamble is not being driven to a particular voltage. EX2033, 171:12-172:20**



Steven Przybylski, Ph.D.
Expert Witness



Samsung's Expert Agrees That DQS Preamble Not Driven to a Particular Voltage

Dr. Wolfe

Expert Witness

SAMSUNG

Q. So just to make sure I have this correct, in Figure 23, when we see DQS on the right side of the figure in what appears to be a flat line, it's not showing a voltage that's, for example, halfway between the VSS and VDD; it's not showing the voltages at half VDD; but only that the DQS output driver of the SDRAM is in a high impedant state.

Do I have that right?

A. Yes, I believe that's correct.

Petitioner Uses the Same Approach as Netlist When Evaluating Prior Art's Disclosure

Petition

A POSITA would have understood from Perego's descriptions of "control information and address information [being] decoded and separated from multiplexed data and provided on lines 595 to request & address logic 540 from interface 596," and from Perego's description of data signals being selectively routed to and from a subset of memory devices and the memory controller through the buffer device, that Perego's buffer device includes logic configured to output data buffer control signals to activate only the channel that transfers the data between the memory controller and the targeted rank, keeping the other channels in a "ready or standby state" thus providing "reduced power consumption." EX1071, 13:54-59, 12:9-12, 11:56-61, 6:15-25, 21:16-20, 15:40-45; EX1003, ¶¶267-269.

Petition 63

Steven Przybylski, Ph.D.
Netlist Expert Witness

However, a POSITA looking at Figure 1 and paragraphs [0007] and [0008] of the '087 provisional filed in January 2005 would understand that: 1) the disclosed DIMM module has a 64-bit data bus, just as all the JEDEC-

executed by the module (and vice versa for write commands); and 5) the claimed "circuitry" is at least in part said multiplexer/demultiplexer, which a POSITA would understand necessarily would receive control signals (i.e., the claimed "data buffer control signals") from the command decode circuitry (a POSITA would understand necessarily that the module described in the '087 Provisional would receive commands from an external memory controller and would include command decode circuitry to interpret those commands), and those control

EX2024, ¶ 82

Netlist slide, p. 119

Petitioner Applied the Wrong Standard to the Written Description Analysis of the '087 Provisional

With respect to the limitation “*data buffer control signals*,” Netlist admits that this is **not expressly disclosed** by the '087 Provisional. POR 42-43; EX1095, 453:23-454:21. Instead, Netlist argues that this limitation is implied by the combination of the box in Figure 1 (shown below) labeled “Rank Buffer DIMM Logic (RBDL),” the JEDEC standards, and the passing references to a “data path multiplexer/demultiplexer.” POR 43-44; EX1095, 263:6-267:5 (arguing a MUX/DEMUX “*necessarily* has to have control signals”).

Reply 23-24

As Petitioner itself admits:

incorrect as explained above, and ignores the maxim that “[a] patent need not **teach, and preferably omits, what is well known in the art,**” MPEP §2164.01.

Reply 9

- *Ariad Pharms., Inc. v. Eli Lilly & Co.*, 598 F.3d 1336, 1352 (Fed. Cir. 2010) (specification need not recite claimed invention in *haec verba*).
- *LizardTech, Inc. v. Earth Res. Mapping, Inc.*, 424 F.3d 1336, 1345 (Fed. Cir. 2005) (“[T]he patent specification is written for a [POSITA], and such a person comes to the patent with the knowledge of what has come before.”)
- *Capon v. Eshhar*, 418 F.3d 1349, 1357-58 (Fed. Cir. 2005) (“The ‘written description’ requirement must be applied in the context of the particular invention and the state of the knowledge [in the art].”).

Ground 2: Ground 1 + Ellsberry

1. Ellsberry is not a “printed publication” pursuant to Section 311(b)
2. Ellsberry is not prior art because the '087 Provisional predates Ellsberry
- 3. Petitioner’s mapping of Ellsberry’s disclosure**
4. No motivation to combine Ellsberry and Perego

Petitioner's Mapping of Ellsberry's Disclosure to Element 1e-1f and 9

Ground 2 also further renders obvious [1.e.3]-[1.f] (pp.92-96) and [9] (pp.106-107), concerning “*overall CAS latency of the memory module*” that is “*greater than an actual operational CAS latency of each of the memory devices*” by “*at least one clock cycle.*” EX1003, ¶¶374-378, 434-436. Ellsberry teaches that the command from the memory controller setting the CAS latency for the DDR memory devices should be modified so that it is one clock cycle less than specified by the memory controller:

Command	Mode	Addr	P Bank	DDR A		DDR B	
				Command	Addr	Command	Addr
MRS	X	X	X	MRS	1	MRS	1
EMRS	X	X	X	EMRS	2	EMRS	2

NOTES: 1. if cl_mode = subtract; cl = cl - 1 to DDRs
2. ods squelch-based on ODS setting, rtt squelch-based on REFF setting, ocd squelch-default, dqs_n enable, rdqs disable, out squelch - enable

EX1073, [0044], Figs.8A-8B; EX1003, ¶¶376-377. The result is that the “*overall CAS latency of the memory module*” is “*one clock cycle*” more than the “*actual operational CAS latency of each of the memory devices.*” *Id.*

Ground 2: Ground 1 + Ellsberry

1. Ellsberry is not a “printed publication” pursuant to Section 311(b)
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3. Petitioner’s mapping of Ellsberry’s disclosure
- 4. No motivation to combine Ellsberry and Perego**

No Motivation to Combine

- Unclear what Petitioner is adding from Ellsberry to Ground 1
- No motivation for rank multiplication
 - Perego uses addresses to select any individual devices
 - Not suffering the insufficient # of CS per slot problem
- No reason to look to Ellsberry's data buffer
 - Configurable width data buffer central to Perego, material details already disclosed
 - Ellsberry does not provide any detail on a configurable width data buffer

Perego Does Not Teach Rank Multiplication



Steven Przybylski, Ph.D.
Expert Witness

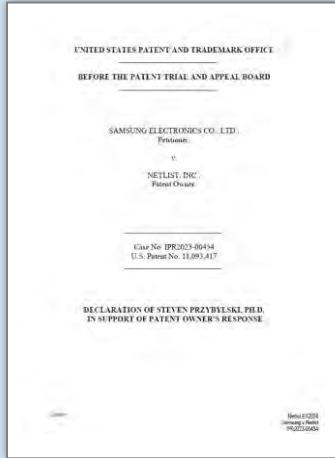


160. Petitioner argues that Perego teaches rank multiplication and that the language about target subsets being selected by addresses teaches the pervasive use of rank multiplication and the increase in presumed chip select signals at the memory device side of the buffer circuit relative to the primary link side. Petition, pp. 50-51. This not correct. Perego does not implement rank multiplication. There is no suggestion within the disclosure of Perego that the memory controller is presented with a view of the memory system in which it appears to the memory controller that two or more memory devices are actually one larger device. The idea that addresses can be used to identify and route transactions to specific target subsets of channels 370 is completely different from the rank multiplication that can occur in memory modules of the style standardized by JEDEC such as those found in JESD21-C. Ex. 1071, 11:56-12:3, 15:31-42; Ex. 1066.

Patent Owner Netlist Outline

1. The '417 and '215 Patents
2. All of Petitioner's Grounds are Deficient
3. The Netlist Claims are Directed to Memory Modules
4. Perego vs. JEDEC-Compliant Memory Architectures
5. Ground 1: Perego and JESD79-2
6. Ground 2: Ground 1 + Ellsberry
- 7. Ground 3: Ground 1 + Halbert**

Halbert's "Ranks" Respond to the Same Commands in Parallel

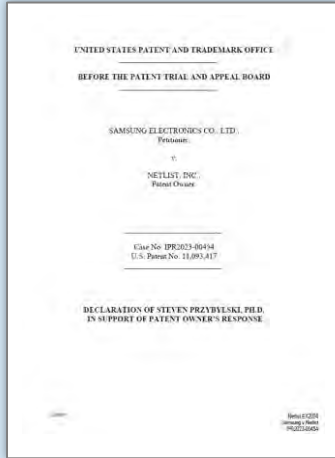


Steven Przybylski, Ph.D.
Expert Witness



125. Halbert teaches using the data interface circuit 120 to aggregate data transfers between “slower memory devices” (e.g., memory devices in ranks 140 and 142) and a “faster system memory bus,” by accessing the multiple ranks of memory devices 140 and 142 simultaneously and in parallel. The data interface circuit 120 interfaces with “slower memory devices” via a wider (2m-bit) module data bus at half the data rate of the narrower (m-bit) and “faster system memory bus.” *Id.*, 4:36-5:22. In this manner, “multiple ranks will receive the same address and commands, and will perform memory operations with the interface circuit concurrently.” *Id.*, 4:57-59 (emphasis added). According to Halbert, its unique design “widens the data bus on the memory module as compared to the width of the system memory data bus,” which “allow[s] a faster system memory data bus to operate at full speed with slower memory devices.”

Registered Chip Select Signals in Halbert Have Same Value



Steven Przybylski, Ph.D.
Expert Witness



213. There is no support for the idea that memory devices in 140 and those in 142 receive separate or different registered chip select signals. They are in fact the two halves of a single 2m-wide memory structure. The two halves of this single structure are interleaved within data interface circuit 120. The function

216. The embodiments of Halbert referred to in the Petition do not support the teaching of a plurality of N-bit ranks and or a plurality of input chip select signals or registered chip select signals. Thus, Halbert cannot cure these and other deficiencies in Perego identified with respect to Ground 1. Therefore Ground 3 also fails to render the claims of the '417 Patent obvious.

Halbert's Registered Chip Select Signals Are of the Same Value for Concurrent Operations

chip select signals, [15.6] *the first plurality of registered chip select signals including a first registered chip select signal having an active signal value and one or more other registered chip select signals each having a non-active signal value*

2015). Halbert's Figure 5 shows operating ranks 140 and 142 concurrently to increase memory throughput. If active and non-active signals are applied to ranks 140 and 142 in Halbert's Figure 5, the increased memory throughput would be eliminated by operating only one of the ranks at a time. In other words, Halbert's Figure 4 memory module would operate at the rate of each of ranks 140 and 142, rather than "twice the data rate" of the ranks. See Ex. 1005 ¶ 24. Petitioner's analysis for limitation 15.6 does not sufficiently address Halbert's Figure 4, much less "explain why a person of ordinary skill in the art would have combined elements from specific references *in the way the claimed invention does*," accounting for the performance impact of not operating ranks 140 and 142 concurrently. See *ActiveVideo Networks, Inc. v. Verizon Comm'ns, Inc.*, 694 F.3d 1312, 1328 (Fed. Cir. 2012).



Petitioner's Expert Agreed

Dr. Wolfe

Expert Witness

SAMSUNG

Q. **Would you call the memory device array of Halbert a single rank?**

* * *

A. No. I think they receive separate control signals.

Q. And what's your basis for saying that?

A. They are selected based on -- well, let me check here. No, actually, that happens elsewhere. I do think in the way that I've defined "rank," those would be separate -- **those would be a single rank.** This particular patent has its own definition of "rank."

The Board Has Rejected Petitioner's Reliance on the "Generally" Language in Related '314 Patent's IPR

Reply

Halbert explains that "multiple ranks will receive the same address and commands" only "[g]enerally," not always. EX1078, 4:57-:59. "Halbert's use of the word 'generally' means that it is not always the case that memory ranks perform memory operations concurrently." EX1107, 27. Contrary to Netlist's mischaracterization, the testimony of Dr. Wolfe is consistent with this understanding of Halbert. EX2033, 179:20-181:14; *see also* EX1095, 421:20-424:1.

Reply 28

IPR2022-00745, FWD

Indeed, Halbert discloses that "[g]enerally, multiple ranks will receive the same address and commands, and will perform memory operations with the interface circuit concurrently" (Ex. 1005 ¶ 30 (emphasis added)), which suggests that the memory need not be limited to concurrently-operating ranks. But as the Federal Circuit has stated, "obviousness concerns whether a skilled artisan not only *could have made* but *would have been motivated to make* the combinations or modifications of prior art to arrive at the claimed invention." *Belden Inc. v. Berk-Tek LLC*, 805 F.3d 1064, 1074 (Fed. Cir. 2015). Halbert's Figure 5 shows operating ranks 140 and 142 concurrently to increase memory throughput. If active and non-active signals are applied to ranks 140 and 142 in Halbert's Figure 5, the increased memory throughput would be eliminated by operating only one of the ranks at a time.

IPR2022-00745, Paper 34 (FWD), 15

No Teaching of “Data Transfers ... Are Registered for an Amount of Time Delay”

- **No disclosure** of “an amount of time delay” for registered “data transfers through the circuitry [data buffer]”
(’417 patent, element [1.f])
- Halbert relies on “registering the **address and command** signals,” not data signals (see EX1003, ¶ 366)

CERTIFICATE OF SERVICE

I hereby certify, pursuant to 37 C.F.R. section 42.6, that on April 30, 2024, a complete copy of the **PATENT OWNER'S EXHIBIT 2036** was served upon the following, by ELECTRONIC MAIL:

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