13146 U.S.PTO
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PROVISIONAL APPLICATION FOR PATENT COVER SHEET

17510 U.S.PTO
60/588244
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For: **MEMORY MODULE DECODER FOR SIMULATING A MEMORY MODULE HAVING FEWER RANKS**

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Enclosed are:

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Attorney Docket No.	:	NETL.027PR
Applicants	:	Robert S. Pauley et al.
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Attorney	:	Bruce S. Itchkawitz
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Ex. 1006, p. 3

MEMORY MODULE DECODER FOR SIMULATING A MEMORY MODULE HAVING FEWER RANKS

Detailed Description

[0001] Certain types of memory modules comprise a plurality of dynamic random-access memory (DRAM) devices mounted on a printed circuit board (PCB). These memory modules are typically mounted in a memory slot or socket of a computer system (e.g., a server system or a personal computer) and are accessed by the processor of the computer system.

[0002] The DRAM devices of a memory module are generally arranged as ranks or rows of memory, each rank of memory generally having a bit width. For example, a memory module in which each rank of the memory module is 64 bits wide is described as having an "x 64" organization. Similarly, a memory module having 72-bit-wide ranks is described as having an "x 72" organization.

[0003] The memory density of a memory module increases with the number of ranks. For example, a memory module with four ranks has double the density of a memory module with two ranks and four times the density of a memory module with one rank.

[0004] During operation, the ranks of a memory module are selected or activated by rank-select signals, also called chip-select signals, that are received from the processor. Most computer and server systems support one-rank and two-rank memory modules. By only supporting one-rank and two-rank memory modules, the memory density that can be incorporated in each memory slot is limited.

[0005] In certain embodiments described herein, a memory module having a first number of ranks comprises a memory module decoder. The decoder of certain embodiments comprises an Application Specific Integrated Circuit ("ASIC") that decodes two chip-select signals and one control signal (such as an address signal) and converts them into four chip-select signals. The decoder of certain embodiments also decodes certain commands (such as refresh or precharge) that require all the ranks of memory to be active.

[0006] In certain embodiments, a four-rank memory module with a decoder simulates and appears to be a two-rank memory module to the computer system. In certain

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Ex. 1006, p. 4

embodiments, the decoder can be alternatively configured to make the same four-rank memory module appear as a four-rank memory module when used in a computer system compatible with such four-rank memory modules. Therefore, in certain such embodiments, the same memory module can be used with computer systems having different configuration requirements.

[0007] In certain embodiments, a two-rank memory module with a decoder simulates and appears to be a one-rank memory module to the computer system. In certain embodiments, the decoder can be alternatively configured to make the same two-rank memory module appear as a two-rank memory module when used in a computer system compatible with such two-rank memory modules. Therefore, in certain such embodiments, the same memory module can be used with computer systems having different configuration requirements.

[0008] In certain embodiments, the decoder effectively increases the memory density available to the computer system. In certain embodiments, the decoder provides flexibility since the memory module can be used with computer systems designed for different numbers of ranks (e.g., either with computer systems designed for two-rank memory modules or with computer systems designed for four-rank memory modules).

[0009] Figure 1 schematically illustrates a memory module comprising one embodiment of the decoder as described herein. The phase-locked loop ("PLL") provides the clock signals to the ranks of memory, the register, and the ASIC decoder. The register buffers address signals (A_0-A_n) from a processor (not shown) and sends the address signals to the appropriate ranks of memory. The ASIC uses the two chip-select signals (CS0, CS1) provided by the processor. In certain embodiments, the memory module comprises commercially-available components, except for the ASIC which is a custom device.

[0010] In certain embodiments in which the computer system supports four-rank memory modules, the ASIC uses one additional address signal (A_{n+1}) and at least one control signal. Exemplary control signals compatible with embodiments described herein control functions including, but are not limited to, refresh, precharge, and other operations used for the proper functioning of the memory module.

Samsung Electronics Co., Ltd.
Ex. 1006, p. 5

[0011] Table 1 provides a logic table for the selection of the ranks of memory compatible with embodiments described herein.

Table 1:

State	CS0	CS1	A_{n+1}	Control	RS0	RS1	RS2	RS3
1	0	1	0	Active	0	1	1	1
2	0	1	1	Active	1	0	1	1
3	0	1	x	Active	0	0	1	1
4	1	0	0	Active	1	1	0	1
5	1	0	1	Active	1	1	1	0
6	1	0	x	Active	1	1	0	0
7	1	1	x	x	1	1	1	1

Note:

1. CS0, CS1, RS0, RS1, RS2, and RS3 are active low signals.
2. A_{n+1} is an active high signal.
3. 'x' is a Don't Care condition.
4. Control involves a number of control signals that define operations such as refresh, precharge, and other operations.

[0012] In Logic State 1: CS0 is active low, A_{n+1} is non-active, and Control is active. RS0 is pulled low, thereby selecting Rank 0.

[0013] In Logic State 2: CS0 is active low, A_{n+1} is active, and Control is active. RS1 is pulled low, thereby selecting Rank 1.

[0014] In Logic State 3: CS0 is active low, A_{n+1} is Don't Care, and Control is active high. RS0 and RS1 are pulled low, thereby selecting Ranks 0 and 1.

[0015] In Logic State 4: CS1 is active low, A_{n+1} is non-active, and Control is active. RS2 is pulled low, thereby selecting Rank 2.

[0016] In Logic State 5: CS1 is active low, A_{n+1} is active, and Control is active. RS3 is pulled low, thereby selecting Rank 3.

[0017] In Logic State 6: CS1 is active low, A_{n+1} is Don't Care, and Control is active. RS2 and RS3 are pulled low, thereby selecting Ranks 2 and 3.

[0018] In Logic State 7: CS0 and CS1 are pulled non-active high, which deselects all ranks, i.e., RS0 through RS3 are pulled high.

[0019] The "Control" column of Table 1 represents the various commands that a DRAM device can execute, examples of which include, but are not limited to, activation,

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Ex. 1006, p. 6

read, write, precharge, and refresh. In certain embodiments, the control command is passed through to the selected rank only (e.g., state 4 of Table 1). In such embodiments, the control command (e.g., read) is sent to only one DRAM device or the other DRAM device so that data is supplied from one device at a time. In other embodiments, the control command is passed through to both associated ranks (e.g., state 6 of Table 1). In such embodiments, the control command (e.g., refresh) is sent to both DRAM devices to ensure that the memory content of the devices remains valid over time. Certain embodiments utilize a logic table such as that of Table 1 to simulate a single DRAM device from two DRAM devices by selecting two ranks concurrently.

[0020] For certain computer systems compatible with four-rank memory modules, by routing four chip-select signals (CS0 through CS3) to each module slot, rather than only two chip-select signals, the computer system can address twice as much memory as a computer system which routes only two chip-select signals to each module slot. By placing a memory module compatible with certain embodiments described herein in a module slot that is four-rank-ready, the memory module is operated in a pass-through mode, i.e., sending the four chip-select signals directly to the four ranks of the memory module.

[0021] Certain embodiments advantageously increase the memory capacity per memory slot or socket on the system board of the computer system. Certain embodiments advantageously allow for higher memory capacity in systems with limited memory slots. Certain embodiments advantageously allow for flexibility in system board design. Certain embodiments advantageously provide lower costs of board designs.

[0022] Various embodiments of the present invention have been described above. Although this invention has been described with reference to these specific embodiments, the descriptions are intended to be illustrative of the invention and are not intended to be limiting. Various modifications and applications may occur to those skilled in the art without departing from the true spirit and scope of the invention.

Summary of the Invention

[0023] In certain embodiments, a memory module comprises a printed circuit board (PCB) and a plurality of dynamic random-access memory (DRAM) devices mounted on the PCB. The plurality of DRAM devices are arranged in a first number of ranks. The

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Ex. 1006, p. 7

memory module further comprises a decoder mounted on the PCB. The decoder is configured to receive input signals comprising a first number of chip-select signals and at least one control signal. The decoder is further configured to convert the input signals to output signals comprising a second number of chip-select signals.

[0024] In certain embodiments, the first number of chip-select signals is smaller than the second number of chip-select signals. In certain such embodiments, the memory module is configured to simulate a memory module having a second number of ranks which is less than the first number of ranks.

[0025] In certain embodiments, a memory module comprises a printed circuit board (PCB) and a plurality of dynamic random-access memory (DRAM) devices mounted on the PCB. The plurality of DRAM devices are arranged in a first number of ranks. The memory module further comprises a decoder mounted on the PCB. The decoder is configured to receive input signals comprising a first number of chip-select signals and at least one control signal and to convert the input signals into output signals, the output signals comprising a second number of chip-select signals and to pass the output signals to the first number of ranks, the second number of chip-select signals being greater than or equal to the first number of chip-select signals. In certain such embodiments, the memory module is configured to operate as (i) a memory module having the first number of ranks or (ii) a memory module having a second number of ranks which is less than the first number of ranks.

[0026] In certain embodiments, a memory module comprises a printed circuit board (PCB) and a plurality of dynamic random-access memory (DRAM) devices mounted on the PCB. The plurality of DRAM devices are arranged in a first number of ranks. The memory module further comprises a decoder mounted on the PCB. The decoder is configured either (i) to pass input signals comprising a first number of chip-select signals and at least one control signal to the first number of ranks, or (ii) to convert the input signals into output signals comprising a second number of chip-select signals and to pass the output signals to the first number of ranks. In certain such embodiments, the memory module is configured to operate as (i) a memory module having the first number of ranks or (ii) a

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Ex. 1006, p. 8

memory module having a second number of ranks which is less than the first number of ranks.

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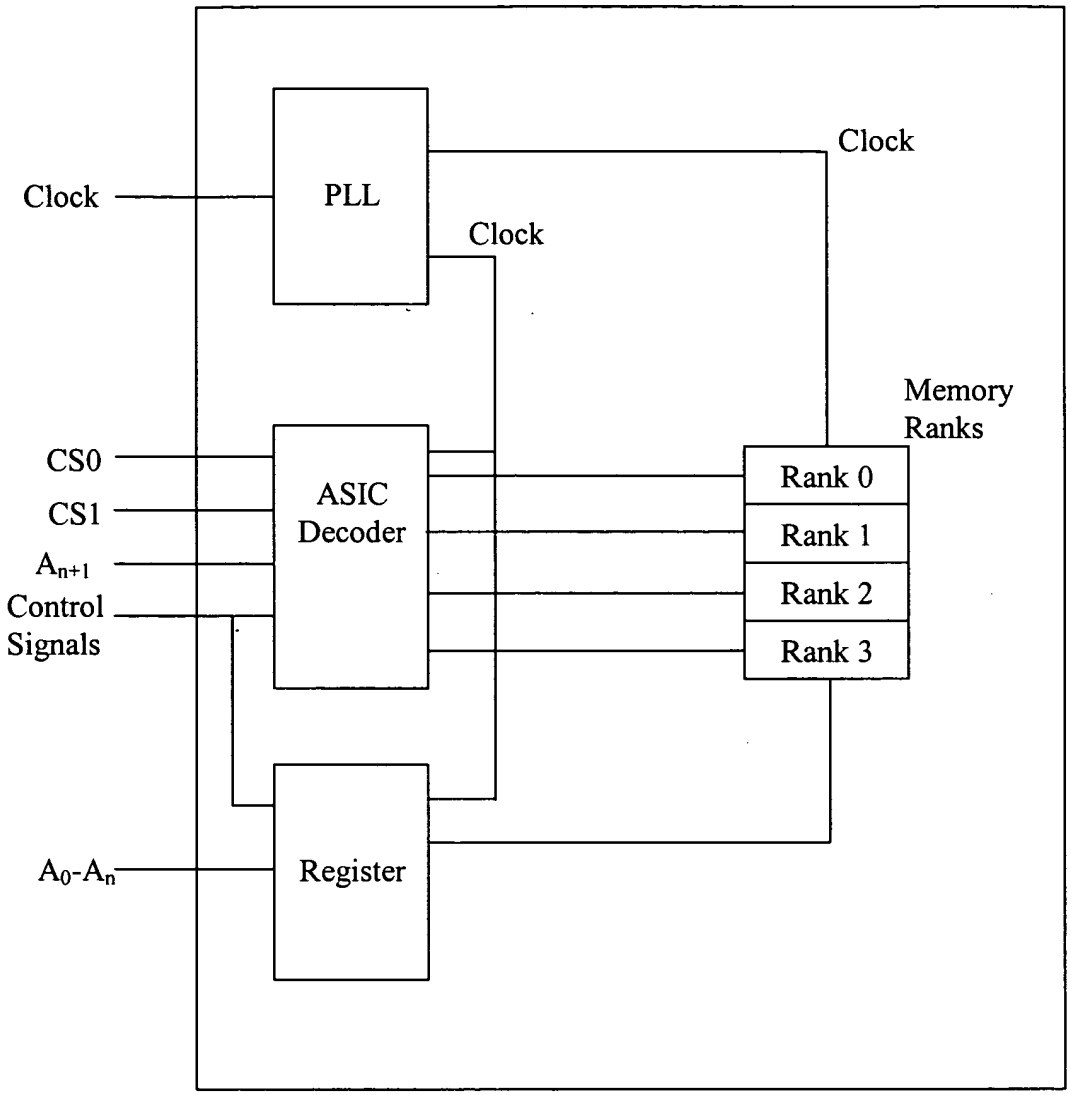
Samsung Electronics Co., Ltd.
Ex. 1006, p. 9

Figure 1:



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Ex. 1006, p. 10

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PTO-1556
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