

DECLARATION - USA PATENT APPLICATION

As a below named inventor, I hereby declare that:

My residence, mailing address and citizenship are as stated below next to my name;

I believe I am an original, first and joint inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled MEMORY MODULE WITH A CIRCUIT PROVIDING LOAD ISOLATION AND MEMORY DOMAIN TRANSLATION; the specification of which was filed on January 19, 2006 as Application Serial No. 11/335,875.

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims;

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, § 1.56;

I hereby claim the benefit under Title 35, United States Code, § 120 of any United States applications listed below, and insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code § 112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, § 1.56, which became available between the filing date of the prior application and the national or PCT international filing date of this application:

Prior U.S.A. Applications

Application No.: 11/173,175	Filing Date: 07/01/05	Status: Pending
Application No.: 60/588,244	Filing Date: 07/15/04	Status: N/A
Application No. 11/075,395	Filing Date: 03/07/05	Status: Pending
Application No. 60/550,668	Filing Date: 03/05/04	Status: N/A
Application No. 60/575,595	Filing Date: 05/28/04	Status: N/A
Application No. 60/590,038	Filing Date: 07/21/04	Status: N/A
Application No. 60/645,087	Filing Date: 01/19/05	Status: N/A

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful, false statements may jeopardize the validity of the application or any patent issued thereon.

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**CIRCUIT PROVIDING LOAD ISOLATION AND MEMORY DOMAIN
TRANSLATION FOR MEMORY MODULE**

Cross-Reference to Related Applications

[0001] The present application is a continuation of U.S. Pat. Appl. No. 12/629,827, filed December 2, 2009, which is a continuation of U.S. Pat. Appl. No. 12/408,652, filed March 20, 2009, which is a continuation of U.S. Pat. Appl. No. 11/335,875, filed January 19, 2006, which claims the benefit of U.S. Provisional Appl. No. 60/645,087, filed January 19, 2005 and which is a continuation-in-part of U.S. Pat. Appl. No. 11/173,175, filed July 1, 2005, which claims the benefit of U.S. Provisional Appl. No. 60/588,244, filed July 15, 2004 and which is a continuation-in-part of U.S. Pat. Appl. No. 11/075,395, filed March 7, 2005, which claims the benefit of U.S. Provisional Appl. No. 60/550,668, filed March 5, 2004, U.S. Provisional Appl. No. 60/575,595, filed May 28, 2004, and U.S. Provisional Appl. No. 60/590,038, filed July 21, 2004. U.S. Pat. Appl. Nos. 12/629,827, 12/408,652, 11/335,875, 11/173,175, and 11/075,395 and U.S. Provisional Appl. Nos. 60/550,668, 60/575,595, 60/590,038, 60/588,244, and 60/645,087 are each incorporated in their entirety by reference herein.

Background of the Invention

Field of the Invention

[0002] The present invention relates generally to memory modules of a computer system, and more specifically to devices and methods for improving the performance, the memory capacity, or both, of memory modules.

Description of the Related Art

[0003] Certain types of memory modules comprise a plurality of dynamic random-access memory (DRAM) devices mounted on a printed circuit board (PCB). These memory modules are typically mounted in a memory slot or socket of a computer system (e.g., a server system or a personal computer) and are accessed by the processor of the computer system. Memory modules typically have a memory configuration with a unique combination of rows, columns, and banks which result in a total memory capacity for the memory module.

[0004] For example, a 512-Megabyte memory module (termed a "512-MB" memory module, which actually has 2^{29} or 536,870,912 bytes of capacity) will typically utilize eight 512-Megabit DRAM devices (each identified as a "512-Mb" DRAM device, each actually having 2^{29} or 536,870,912 bits of capacity). The memory cells (or memory locations) of each 512-Mb DRAM device can be arranged in four banks, with each bank having an array of 2^{24} (or 16,777,216) memory locations arranged as 2^{13} rows and 2^{11} columns, and with each memory location having a width of 8 bits. Such DRAM devices with 64M 8-bit-wide memory locations (actually with four banks of 2^{27} or 134,217,728 one-bit memory cells arranged to provide a total of 2^{26} or 67,108,864 memory locations with 8 bits each) are identified as having a "64Mb x 8" or "64M x 8-bit" configuration, or as having a depth of 64M and a bit width of 8. Furthermore, certain commercially-available 512-MB memory modules are termed to have a "64M x 8-byte" configuration or a "64M x 64-bit" configuration with a depth of 64M and a width of 8 bytes or 64 bits.

[0005] Similarly, a 1-Gigabyte memory module (termed a "1-GB" memory module, which actually has 2^{30} or 1,073,741,824 bytes of capacity) can utilize eight 1-Gigabit DRAM devices (each identified as a "1-Gb" DRAM device, each actually having 2^{30} or 1,073,741,824 bits of capacity). The memory locations of each 1-Gb DRAM device can be arranged in four banks, with each bank having an array of memory locations with 2^{14} rows and 2^{11} columns, and with each memory location having a width of 8 bits. Such DRAM devices with 128M 8-bit-wide memory locations (actually with a total of 2^{27} or 134,217,728 memory locations with 8 bits each) are identified as having a "128Mb x 8" or "128M x 8-bit" configuration, or as having a depth of 128M and a bit width of 8. Furthermore, certain commercially-available 1-GB memory modules are identified as having a "128M x 8-byte" configuration or a "128M x 64-bit" configuration with a depth of 128M and a width of 8 bytes or 64 bits.

[0006] The commercially-available 512-MB (64M x 8-byte) memory modules and the 1-GB (128M x 8-byte) memory modules described above are typically used in computer systems (e.g., personal computers) which perform graphics applications since such "x 8" configurations are compatible with data mask capabilities often used in such graphics applications. Conversely, memory modules with "x 4" configurations are typically used in

computer systems such as servers which are not as graphics-intensive. Examples of such commercially available “x 4” memory modules include, but are not limited to, 512-MB (128M x 4-byte) memory modules comprising eight 512-Mb (128Mb x 4) memory devices.

[0007] The DRAM devices of a memory module are generally arranged as ranks or rows of memory, each rank of memory generally having a bit width. For example, a memory module in which each rank of the memory module is 64 bits wide is described as having an “x 64” organization. Similarly, a memory module having 72-bit-wide ranks is described as having an “x 72” organization.

[0008] The memory capacity of a memory module increases with the number of memory devices. The number of memory devices of a memory module can be increased by increasing the number of memory devices per rank or by increasing the number of ranks. For example, a memory module with four ranks has double the memory capacity of a memory module with two ranks and four times the memory capacity of a memory module with one rank. Rather than referring to the memory capacity of the memory module, in certain circumstances, the memory density of the memory module is referred to instead.

[0009] During operation, the ranks of a memory module are selected or activated by address and command signals that are received from the processor. Examples of such address and command signals include, but are not limited to, rank-select signals, also called chip-select signals. Most computer and server systems support one-rank and two-rank memory modules. By only supporting one-rank and two-rank memory modules, the memory density that can be incorporated in each memory slot is limited.

[0010] Various aspects of the design of a memory module impose limitations on the size of the memory arrays of the memory module. Certain such aspects are particularly important for memory modules designed to operate at higher frequencies. Examples of such aspects include, but are not limited to, memory device (e.g., chip) densities, load fan-out, signal integrity, available rank selects, power dissipation, and thermal profiles.

Summary of the Invention

[0011] In certain embodiments, a memory module comprises a plurality of memory devices and a circuit. Each memory device has a corresponding load. The circuit is electrically coupled to the plurality of memory devices and is configured to be electrically

coupled to a memory controller of a computer system. The circuit selectively isolates one or more of the loads of the memory devices from the computer system. The circuit comprises logic which translates between a system memory domain of the computer system and a physical memory domain of the memory module.

[0012] In certain embodiments, a method of using a memory module with a computer system is provided. The method comprises providing a memory module having a plurality of memory devices and a circuit. The circuit is electrically coupled to the plurality of memory devices. The circuit is configured to be electrically coupled to a computer system. Each memory device has a corresponding load. The method further comprises electrically coupling the memory module to the computer system. The method further comprises activating the circuit to selectively isolate at least one of the loads of the memory devices from the computer system and to translate between a system memory domain of the computer system and a physical memory domain of the memory module.

[0013] In certain embodiments, a memory module is connectable to a computer system. The memory module comprises a first memory device having a first data signal line and a first data strobe signal line. The memory module further comprises a second memory device having a second data signal line and a second data strobe signal line. The memory module further comprises a common data signal line connectable to the computer system. The memory module further comprises a device electrically coupled to the first data signal line, to the second data signal line, and to the common data signal line. The device selectively electrically couples the first data signal line to the common data signal line and selectively electrically couples the second data signal line to the common data signal line. The device comprises logic which translates between a system memory domain of the computer system and a physical memory domain of the memory module.

Brief Description of the Drawings

[0014] Figure 1 schematically illustrates an example memory module in accordance with certain embodiments described herein.

[0015] Figure 2 schematically illustrates a circuit diagram of two memory devices of a conventional memory module.

[0016] Figures 3A and 3B schematically illustrate example memory modules having a circuit which selectively isolates one or both of the DQ data signal lines of the two memory devices from the computer system in accordance with certain embodiments described herein.

[0017] Figures 4A and 4B schematically illustrate example memory modules having a circuit which selectively isolates one or both of the DQ data signal lines of the two ranks of memory devices from the computer system in accordance with certain embodiments described herein.

[0018] Figures 5A-5D schematically illustrate example memory modules having a circuit comprising a logic element and one or more switches operatively coupled to the logic element in accordance with certain embodiments described herein.

[0019] Figure 6A shows an exemplary timing diagram of a gapless read burst for a back-to-back adjacent read condition from one memory device.

[0020] Figure 6B shows an exemplary timing diagram with an extra clock cycle between successive read commands issued to different memory devices for successive read accesses from different memory devices.

[0021] Figure 7 shows an exemplary timing diagram in which the last data strobe of memory device “a” collides with the pre-ambule time interval of the data strobe of memory device “b.”

[0022] Figures 8A-8D schematically illustrate circuit diagrams of example memory modules comprising a circuit which multiplexes the DQS data strobe signal lines from one another in accordance with certain embodiments described herein.

[0023] Figure 9A schematically illustrates an example memory module with four ranks of memory devices compatible with certain embodiments described herein.

[0024] Figure 9B schematically illustrates an example memory module with two ranks of memory devices compatible with certain embodiments described herein.

[0025] Figure 9C schematically illustrates another example memory module in accordance with certain embodiments described herein.

[0026] Figure 10A schematically illustrates an exemplary memory module which doubles the rank density in accordance with certain embodiments described herein.

[0027] Figure 10B schematically illustrates an exemplary circuit compatible with embodiments described herein.

[0028] Figure 11A schematically illustrates an exemplary memory module which doubles number of ranks in accordance with certain embodiments described herein.

[0029] Figure 11B schematically illustrates an exemplary circuit compatible with embodiments described herein.

[0030] Figure 12 schematically illustrates an exemplary memory module in which a data strobe (DQS) pin of a first memory device is electrically connected to a DQS pin of a second memory device while both DQS pins are active.

[0031] Figure 13 is an exemplary timing diagram of the voltages applied to the two DQS pins due to non-simultaneous switching.

[0032] Figure 14 schematically illustrates another exemplary memory module in which a DQS pin of a first memory device is connected to a DQS pin of a second memory device.

[0033] Figure 15 schematically illustrates an exemplary memory module in accordance with certain embodiments described herein.

[0034] Figures 16A and 16B schematically illustrate a first side and a second side, respectively, of a memory module with eighteen 64M x 4 bit, DDR-1 SDRAM FBGA memory devices on each side of a 184-pin glass-epoxy printed circuit board.

[0035] Figures 17A and 17B schematically illustrate an exemplary embodiment of a memory module in which a first resistor and a second resistor are used to reduce the current flow between the first DQS pin and the second DQS pin.

[0036] Figure 18 schematically illustrates another exemplary memory module compatible with certain embodiments described herein.

[0037] Figure 19 schematically illustrates a particular embodiment of the memory module schematically illustrated by Figure 18.

Detailed Description of Example Embodiments

Load Isolation

[0038] Figure 1 schematically illustrates an example memory module 10 compatible with certain embodiments described herein. The memory module 10 is

connectable to a memory controller 20 of a computer system (not shown). The memory module 10 comprises a plurality of memory devices 30, each memory device 30 having a corresponding load. The memory module 10 further comprises a circuit 40 electrically coupled to the plurality of memory devices 30 and configured to be electrically coupled to the memory controller 20 of the computer system. The circuit 40 selectively isolates one or more of the loads of the memory devices from the computer system. The circuit 40 comprises logic which translates between a system memory domain of the computer system and a physical memory domain of the memory module 10.

[0039] As used herein, the term “load” is a broad term which includes, without limitation, electrical load, such as capacitive load, inductive load, or impedance load. As used herein, the term “isolation” is a broad term which includes, without limitation, electrical separation of one or more components from another component or from one another. As used herein, the term “circuit” is a broad term which includes, without limitation, an electrical component or device, or a configuration of electrical components or devices which are electrically or electromagnetically coupled together (e.g., integrated circuits), to perform specific functions.

[0040] Various types of memory modules 10 are compatible with embodiments described herein. For example, memory modules 10 having memory capacities of 512-MB, 1-GB, 2-GB, 4-GB, 8-GB, as well as other capacities, are compatible with embodiments described herein. Certain embodiments described herein are applicable to various frequencies including, but not limited to 100 MHz, 200 MHz, 400 MHz, 800 MHz, and above. In addition, memory modules 10 having widths of 4 bytes, 8 bytes, 16 bytes, 32 bytes, or 32 bits, 64 bits, 128 bits, 256 bits, as well as other widths (in bytes or in bits), are compatible with embodiments described herein. In certain embodiments, the memory module 10 comprises a printed circuit board on which the memory devices 30 are mounted, a plurality of edge connectors configured to be electrically coupled to a corresponding plurality of contacts of a module slot of the computer system, and a plurality of electrical conduits which electrically couple the memory devices 30 to the circuit 40 and which electrically couple the circuit 40 to the edge connectors. Furthermore, memory modules 10 compatible with embodiments described herein include, but are not limited to, single in-line memory

modules (SIMMs), dual in-line memory modules (DIMMs), small-outline DIMMs (SO-DIMMs), unbuffered DIMMs (UDIMMs), registered DIMMs (RDIMMs), fully-buffered DIMM (FBDIMM), rank-buffered DIMMs (RBDIMMs), mini-DIMMs, and micro-DIMMs.

[0041] Memory devices 30 compatible with embodiments described herein include, but are not limited to, random-access memory (RAM), dynamic random-access memory (DRAM), synchronous DRAM (SDRAM), and double-data-rate DRAM (e.g., SDR, DDR-1, DDR-2, DDR-3). In addition, memory devices 30 having bit widths of 4, 8, 16, 32, as well as other bit widths, are compatible with embodiments described herein. Memory devices 30 compatible with embodiments described herein have packaging which include, but are not limited to, thin small-outline package (TSOP), ball-grid-array (BGA), fine-pitch BGA (FBGA), micro-BGA (μ BGA), mini-BGA (mBGA), and chip-scale packaging (CSP). Memory devices 30 compatible with embodiments described herein are available from a number of sources, including but not limited to, Samsung Semiconductor, Inc. of San Jose, California, Infineon Technologies AG of San Jose, California, and Micron Technology, Inc. of Boise, Idaho. Persons skilled in the art can select appropriate memory devices 30 in accordance with certain embodiments described herein.

[0042] In certain embodiments, the plurality of memory devices 30 comprises a first number of memory devices 30. In certain such embodiments, the circuit 40 selectively isolates a second number of the memory devices 30 from the computer system, with the second number less than the first number.

[0043] In certain embodiments, the plurality of memory devices 30 are arranged in a first number of ranks. For example, in certain embodiments, the memory devices 30 are arranged in two ranks, as schematically illustrated by Figure 1. In other embodiments, the memory devices 30 are arranged in four ranks. Other numbers of ranks of the memory devices 30 are also compatible with embodiments described herein.

[0044] In certain embodiments, the circuit comprises a logic element selected from a group consisting of: a programmable-logic device (PLD), an application-specific integrated circuit (ASIC), a field-programmable gate array (FPGA), a custom-designed semiconductor device, and a complex programmable-logic device (CPLD). In certain embodiments, the logic element of the circuit 40 is a custom device. Sources of logic

elements compatible with embodiments described herein include, but are not limited to, Lattice Semiconductor Corporation of Hillsboro, Oregon, Altera Corporation of San Jose, California, and Xilinx Incorporated of San Jose, California. In certain embodiments, the logic element comprises various discrete electrical elements, while in certain other embodiments, the logic element comprises one or more integrated circuits.

[0045] In certain embodiments, the circuit 40 further comprises one or more switches which are operatively coupled to the logic element to receive control signals from the logic element. Examples of switches compatible with certain embodiments described herein include, but are not limited to, field-effect transistor (FET) switches, such as the SN74AUC1G66 single bilateral analog switch available from Texas Instruments, Inc. of Dallas, Texas.

[0046] Figure 2 schematically illustrates a circuit diagram of two memory devices 30a, 30b of a conventional memory module showing the interconnections between the DQ data signal lines 102a, 102b of the memory devices 30a, 30b and the DQS data strobe signal lines 104a, 104b of the memory devices 30a, 30b. Each of the memory devices 30a, 30b has a plurality of DQ data signal lines and a plurality of DQS data strobe signal lines, however, for simplicity, Figure 2 only illustrates a single DQ data signal line and a single DQS data strobe signal line for each memory device 30a, 30b. The DQ data signal lines 102a, 102b and the DQS data strobe signal lines 104a, 104b are typically conductive traces etched on the printed circuit board of the memory module. As shown in Figure 2, each of the memory devices 30a, 30b has their DQ data signal lines 102a, 102b electrically coupled to a common DQ line 112 and their DQS data strobe signal lines 104a, 104b electrically coupled to a common DQS line 114. The common DQ line 112 and the common DQS line 114 are electrically coupled to the memory controller 20 of the computer system. Thus, the computer system is exposed to the loads of both memory devices 30a, 30b concurrently.

[0047] In certain embodiments, the circuit 40 selectively isolates the loads of at least some of the memory devices 30 from the computer system. The circuit 40 of certain embodiments is configured to present a significantly reduced load to the computer system. In certain embodiments in which the memory devices 30 are arranged in a plurality of ranks, the circuit 40 selectively isolates the loads of some (e.g., one or more) of the ranks of the

memory module 10 from the computer system. In certain other embodiments, the circuit 40 selectively isolates the loads of all of the ranks of the memory module 10 from the computer system. For example, when a memory module 10 is not being accessed by the computer system, the capacitive load on the memory controller 20 of the computer system by the memory module 10 can be substantially reduced to the capacitive load of the circuit 40 of the memory module 10.

[0048] As schematically illustrated by Figures 3A and 3B, an example memory module 10 compatible with certain embodiments described herein comprises a circuit 40 which selectively isolates one or both of the DQ data signal lines 102a, 102b of the two memory devices 30a, 30b from the common DQ data signal line 112 coupled to the computer system. Thus, the circuit 40 selectively allows a DQ data signal to be transmitted from the memory controller 20 of the computer system to one or both of the DQ data signal lines 102a, 102b. In addition, the circuit 40 selectively allows one of a first DQ data signal from the DQ data signal line 102a of the first memory device 30a or a second DQ data signal from the DQ data signal line 102b of the second memory device 30b to be transmitted to the memory controller 20 via the common DQ data signal line 112 (see, e.g., triangles on the DQ and DQS lines of Figures 3A and 3B which point towards the memory controller). While various figures of the present application denote read operations by use of DQ and DQS lines which have triangles pointing towards the memory controller, certain embodiments described herein are also compatible with write operations (e.g., as would be denoted by triangles on the DQ or DQS lines pointing away from the memory controller).

[0049] For example, in certain embodiments, the circuit 40 comprises a pair of switches 120a, 120b on the DQ data signal lines 102a, 102b as schematically illustrated by Figure 3A. Each switch 120a, 120b is selectively actuated to selectively electrically couple the DQ data signal line 102a to the common DQ signal line 112, the DQ data signal line 102b to the common DQ signal line 112, or both DQ data signal lines 102a, 102b to the common DQ signal line 112. In certain other embodiments, the circuit 40 comprises a switch 120 electrically coupled to both of the DQ data signal lines 102a, 102b, as schematically illustrated by Figure 3B. The switch 120 is selectively actuated to selectively electrically couple the DQ data signal line 102a to the common DQ signal line 112, the DQ data signal

line 102b to the common DQ signal line 112, or both DQ signal lines 102a, 102b to the common DQ signal line 112. Circuits 40 having other configurations of switches are also compatible with embodiments described herein. While each of the memory devices 30a, 30b has a plurality of DQ data signal lines and a plurality of DQS data strobe signal lines, Figures 3A and 3B only illustrate a single DQ data signal line and a single DQS data strobe signal line for each memory device 30a, 30b for simplicity. The configurations schematically illustrated by Figures 3A and 3B can be applied to all of the DQ data signal lines and DQS data strobe signal lines of the memory module 10.

[0050] In certain embodiments, the circuit 40 selectively isolates the loads of ranks of memory devices 30 from the computer system. As schematically illustrated in Figures 4A and 4B, example memory modules 10 compatible with certain embodiments described herein comprise a first number of memory devices 30 arranged in a first number of ranks 32. The memory modules 10 of Figures 4A and 4B comprises two ranks 32a, 32b, with each rank 32a, 32b having a corresponding set of DQ data signal lines and a corresponding set of DQS data strobe lines. Other numbers of ranks (e.g., four ranks) of memory devices 30 of the memory module 10 are also compatible with certain embodiments described herein. For simplicity, Figures 4A and 4B illustrate only a single DQ data signal line and a single DQS data strobe signal line from each rank 32.

[0051] The circuit 40 of Figure 4A selectively isolates one or more of the DQ data signal lines 102a, 102b of the two ranks 32a, 32b from the computer system. Thus, the circuit 40 selectively allows a DQ data signal to be transmitted from the memory controller 20 of the computer system to the memory devices 30 of one or both of the ranks 32a, 32b via the DQ data signal lines 102a, 102b. In addition, the circuit 40 selectively allows one of a first DQ data signal from the DQ data signal line 102a of the first rank 32a and a second DQ data signal from the DQ data signal line 102b of the second rank 32b to be transmitted to the memory controller 20 via the common DQ data signal line 112. For example, in certain embodiments, the circuit 40 comprises a pair of switches 120a, 120b on the DQ data signal lines 102a, 102b as schematically illustrated by Figure 4A. Each switch 120a, 120b is selectively actuated to selectively electrically couple the DQ data signal line 102a to the common DQ data signal line 112, the DQ data signal line 102b to the common DQ data

signal line 112, or both DQ data signal lines 102a, 102b to the common DQ data signal line 112. In certain other embodiments, the circuit 40 comprises a switch 120 electrically coupled to both of the DQ data signal lines 102a, 102b, as schematically illustrated by Figure 4B. The switch 120 is selectively actuated to selectively electrically couple the DQ data signal line 102a to the common DQ data signal line 112, the DQ data signal line 102b to the common DQ data signal line 112, or both DQ data signal lines 102a, 102b to the common DQ data signal line 112. Circuits 40 having other configurations of switches are also compatible with embodiments described herein.

[0052] In the example embodiments schematically illustrated by Figures 3A, 3B, 4A, and 4B, the circuit 40 comprises a logic element which is integral with and comprises the switches 120 which are coupled to the DQ data signal lines and the DQS data strobe signal lines. In certain such embodiments, each switch 120 comprises a data path multiplexer/demultiplexer. In certain other embodiments, the circuit 40 comprises a logic element 122 which is a separate component operatively coupled to the switches 120, as schematically illustrated by Figures 5A-5D. The one or more switches 120 are operatively coupled to the logic element 122 to receive control signals from the logic element 122 and to selectively electrically couple one or more data signal lines to a common data signal line. Example switches compatible with embodiments described herein include, but are not limited to field-effect transistor (FET) switches, such as the SN74AUC1G66 single bilateral analog switch available from Texas Instruments, Inc. of Dallas, Texas. Example logic elements 122 compatible with certain embodiments described herein include, but are not limited to, programmable-logic devices (PLD), application-specific integrated circuits (ASIC), field-programmable gate arrays (FPGA), custom-designed semiconductor devices, and complex programmable-logic devices (CPLD). Example logic elements 122 are available from Lattice Semiconductor Corporation of Hillsboro, Oregon, Altera Corporation of San Jose, California, and Xilinx Incorporated of San Jose, California.

[0053] In certain embodiments, the load isolation provided by the circuit 40 advantageously allows the memory module 10 to present a reduced load (e.g., electrical load, such as capacitive load, inductive load, or impedance load) to the computer system by selectively switching between the two ranks of memory devices 30 to which it is coupled.

This feature is used in certain embodiments in which the load of the memory module 10 may otherwise limit the number of ranks or the number of memory devices per memory module. In certain embodiments, the memory module 10 operates as having a data path rank buffer which advantageously isolates the ranks of memory devices 30 of the memory module 10 from one another, from the ranks on other memory modules, and from the computer system. This data path rank buffer of certain embodiments advantageously provides DQ-DQS paths for each rank or sets of ranks of memory devices which are separate from one another, or which are separate from the memory controller of the computer system. In certain embodiments, the load isolation advantageously diminishes the effects of capacitive loading, jitter and other sources of noise. In certain embodiments, the load isolation advantageously simplifies various other aspects of operation of the memory module 10, including but not limited to, setup-and-hold time, clock skew, package skew, and process, temperature, voltage, and transmission line variations.

[0054] For certain memory module applications that utilize multiple ranks of memory, increased load on the memory bus can degrade speed performance. In certain embodiments described herein, selectively isolating the loads of the ranks of memory devices 30 advantageously decreases the load on the computer system, thereby allowing the computer system (e.g., server) to run faster with improved signal integrity. In certain embodiments, load isolation advantageously provides system memory with reduced electrical loading, thereby improving the electrical topology to the memory controller 20. In certain such embodiments, the speed and the memory density of the computer system are advantageously increased without sacrificing one for the other.

[0055] In certain embodiments, load isolation advantageously increases the size of the memory array supported by the memory controller 20 of the computer system. The larger memory array has an increased number of memory devices 30 and ranks of memory devices 30 of the memory module 10, with a corresponding increased number of chip selects. Certain embodiments described herein advantageously provide more system memory using fewer chip selects, thereby avoiding the chip select limitation of the memory controller.

[0056] An exemplary section of Verilog code corresponding to logic compatible with a circuit 40 which provides load isolation is listed below in Example 1. The exemplary

code of Example 1 corresponds to a circuit 40 comprising six FET switches for providing load isolation to DQ and DQS lines.

[0057] Example 1:

```
//===== declarations
reg          rasN_R, casN_R, weN_R;
wire         actv_cmd_R, pch_cmd_R, pch_all_cmd_R, ap_xfr_cmd_R_R;
wire         xfr_cmd_R, mrs_cmd, rd_cmd_R;
//----- DDR 2 FET
reg          brs0N_R;           // registered chip sel
reg          brs1N_R;           // registered chip sel
reg          brs2N_R;           // registered chip sel
reg          brs3N_R;           // registered chip sel
wire         sel;
wire         sel_01;
wire         sel_23;
wire         rd_R1;
wire         wr_cmd_R, wr_R1;
reg          rd_R2, rd_R3, rd_R4, rd_R5;
reg          wr_R2, wr_R3, wr_R4, wr_R5;
reg          enfet1, enfet2, enfet3, enfet4, enfet5, enfet6;
wire         wr_01_R1, wr_23_R1;
reg          wr_01_R2, wr_01_R3, wr_01_R4;
reg          wr_23_R2, wr_23_R3, wr_23_R4;
wire         rodt0_a, rodt0_b;
//===== logic
always @(posedge clk_in)
begin
    brs0N_R <= brs0_in_N;    // cs0
    brs1N_R <= brs1_in_N;    // cs1
    brs2N_R <= brs2_in_N;    // cs2
    brs3N_R <= brs3_in_N;    // cs3
    rasN_R  <= brras_in_N;
    casN_R  <= brcas_in_N;
    weN_R   <= bwe_in_N;

end
assign sel = ~brs0N_R | ~brs1N_R | ~brs2N_R | ~brs3N_R;
assign sel_01 = ~brs0N_R | ~brs1N_R;
assign sel_23 = ~brs2N_R | ~brs3N_R;
assign actv_cmd_R = !rasN_R & casN_R & weN_R; // activate cmd
assign pch_cmd_R = !rasN_R & casN_R & !weN_R; // pchg cmd
assign xfr_cmd_R = rasN_R & !casN_R;          // xfr cmd
assign mrs_cmd = !rasN_R & !casN_R & !weN_R; // md reg set cmd
assign rd_cmd_R = rasN_R & !casN_R & weN_R;   // read cmd
assign wr_cmd_R = rasN_R & !casN_R & !weN_R;  // write cmd
//-----
assign rd_R1 = sel & rd_cmd_R; // rd cmd cyc 1
assign wr_R1 = sel & wr_cmd_R; // wr cmd cyc 1
//-----
always @(posedge clk_in)
begin
    rd_R2 <= rd_R1;
    rd_R3 <= rd_R2;
```

```

        rd_R4 <= rd_R3;
        rd_R5 <= rd_R4;
//      rd0_o_R6 <= rd0_o_R5;
        wr_R2 <= wr_R1;
        wr_R3 <= wr_R2;
        wr_R4 <= wr_R3;
        wr_R5 <= wr_R4;
    end
//-----
assign wr_01_R1 = sel_01 & wr_cmd_R; // wr cmd cyc 1 for cs 2 & cs3
assign wr_23_R1 = sel_23 & wr_cmd_R; // wr cmd cyc 1 for cs 2 & cs3
    always @(posedge clk_in)
        begin
            wr_01_R2 <= wr_01_R1;
            wr_01_R3 <= wr_01_R2;
            wr_01_R4 <= wr_01_R3;
            wr_23_R2 <= wr_23_R1;
            wr_23_R3 <= wr_23_R2;
            wr_23_R4 <= wr_23_R3;
        end
assign rodt0_ab = (rodt0) // odt cmd from sys
    | (wr_23_R1) // wr 1st cyc to other rnks (assume single dimm per channel)
    | (wr_23_R2) // wr 2nd cyc to other rnks (assume single dimm per channel)
    | (wr_23_R3) // wr 3rd cyc to other rnks (assume single dimm per channel)
    ;
assign rodt1_ab = (rodt1) // odt cmd from sys
    | (wr_01_R1) // wr 1st cyc to other rnks (assume single dimm per channel)
    | (wr_01_R2) // wr 2nd cyc to other rnks (assume single dimm per channel)
    | (wr_01_R3) // wr 3rd cyc to other rnks (assume single dimm per channel)
    ;
//-----
    always @(posedge clk_in)
        begin
            if (
                | (rd_R2) // pre-am rd
                | (rd_R3) // 1st cyc of rd brst (cl3)
                | (rd_R4) // 2nd cyc of rd brst (cl3)
                | (wr_R1) // pre-am wr
                | (wr_R2) // wr brst 1st cyc
                | (wr_R3) // wr brst 2nd cyc
            ) begin
                enfet1 <= 1'b1; // enable fet
                enfet2 <= 1'b1; // enable fet
                enfet3 <= 1'b1; // enable fet
                enfet4 <= 1'b1; // enable fet
                enfet5 <= 1'b1; // enable fet
                enfet6 <= 1'b1; // enable fet
            end
            else
                begin
                    enfet1 <= 1'b0; // disable fet
                    enfet2 <= 1'b0; // disable fet
                    enfet3 <= 1'b0; // disable fet
                    enfet4 <= 1'b0; // disable fet
                    enfet5 <= 1'b0; // disable fet
                end
        end

```

```

end
    enfet6 <= 1'b0;          // disable fet
end

```

Back-to-Back Adjacent Read Commands

[0058] Due to their source synchronous nature, DDR SDRAM (e.g., DDR1, DDR2, DDR3) memory devices operate with a data transfer protocol which surrounds each burst of data strobes with a pre-ambler time interval and a post-ambler time interval. The pre-ambler time interval provides a timing window for the receiving memory device to enable its data capture circuitry when a known valid level is present on the strobe signal to avoid false triggers of the memory device's capture circuit. The post-ambler time interval provides extra time after the last strobe for this data capture to facilitate good signal integrity. In certain embodiments, when the computer system accesses two consecutive bursts of data from the same memory device, termed herein as a "back-to-back adjacent read," the post-ambler time interval of the first read command and the pre-ambler time interval of the second read command are skipped by design protocol to increase read efficiency. Figure 6A shows an exemplary timing diagram of this "gapless" read burst for a back-to-back adjacent read condition from one memory device.

[0059] In certain embodiments, when the second read command accesses data from a different memory device than does the first read command, there is at least one time interval (e.g., clock cycle) inserted between the data strobes of the two memory devices. This inserted time interval allows both read data bursts to occur without the post-ambler time interval of the first read data burst colliding or otherwise interfering with the pre-ambler time interval of the second read data burst. In certain embodiments, the memory controller of the computer system inserts an extra clock cycle between successive read commands issued to different memory devices, as shown in the exemplary timing diagram of Figure 6B for successive read accesses from different memory devices.

[0060] In typical computer systems, the memory controller is informed of the memory boundaries between the ranks of memory of the memory module prior to issuing read commands to the memory module. Such memory controllers can insert wait time intervals or clock cycles to avoid collisions or interference between back-to-back adjacent

read commands which cross memory device boundaries, which are referred to herein as “BBARX.”

[0061] In certain embodiments described herein in which the number of ranks 32 of the memory module 10 is doubled or quadrupled, the circuit 40 generates a set of output address and command signals so that the selection decoding is transparent to the computer system. However, in certain such embodiments, there are memory device boundaries of which the computer system is unaware, so there are occasions in which BBARX occurs without the cognizance of the memory controller 20 of the computer system. As shown in Figure 7, the last data strobe of memory device “a” collides with the pre-amble time interval of the data strobe of memory device “b,” resulting in a “collision window.”

[0062] Figures 8A-8D schematically illustrate circuit diagrams of example memory modules 10 comprising a circuit 40 which multiplexes the DQS data strobe signal lines 104a, 104b of two ranks 32a, 32b from one another in accordance with certain embodiments described herein. While the DQS data strobe signal lines 104a, 104b of Figures 8A-8D correspond to two ranks 32a, 32b of memory devices 30, in certain other embodiments, the circuit 40 multiplexes the DQS data strobe signal lines 104a, 104b corresponding to two individual memory devices 30a, 30b.

[0063] Figure 8A schematically illustrates a circuit diagram of an exemplary memory module 10 comprising a circuit 40 in accordance with certain embodiments described herein. In certain embodiments, BBARX collisions are avoided by a mechanism which electrically isolates the DQS data strobe signal lines 104a, 104b from one another during the transition from the first read data burst of one rank 32a of memory devices 30 to the second read data burst of another rank 32b of memory devices 30.

[0064] In certain embodiments, as schematically illustrated by Figure 8A, the circuit 40 comprises a first switch 130a electrically coupled to a first DQS data strobe signal line 104a of a first rank 32a of memory devices 30 and a second switch 130b electrically coupled to a second DQS data strobe signal line 104b of a second rank 32b of memory devices 30. In certain embodiments, the time for switching the first switch 130a and the second switch 130b is between the two read data bursts (e.g., after the last DQS data strobe of the read data burst of the first rank 32a and before the first DQS data strobe of the read data

burst of the second rank 32b). During the read data burst for the first rank 32a, the first switch 130a is enabled. After the last DQS data strobe of the first rank 32a and before the first DQS data strobe of the second rank 32b, the first switch 130a is disabled and the second switch 130b is enabled.

[0065] As shown in Figure 8A, each of the ranks 32a, 32b otherwise involved in a BBARX collision have their DQS data strobe signal lines 104a, 104b selectively electrically coupled to the common DQS line 114 through the circuit 40. The circuit 40 of certain embodiments multiplexes the DQS data strobe signal lines 104a, 104b of the two ranks 32a, 32b of memory devices 30 from one another to avoid a BBARX collision.

[0066] In certain embodiments, as schematically illustrated by Figure 8B, the circuit 40 comprises a switch 130 which multiplexes the DQS data strobe signal lines 104a, 104b from one another. For example, the circuit 40 receives a DQS data strobe signal from the common DQS data strobe signal line 114 and selectively transmits the DQS data strobe signal to the first DQS data strobe signal line 104a, to the second DQS data strobe signal line 104b, or to both DQS data strobe signal lines 104a, 104b. As another example, the circuit 40 receives a first DQS data strobe signal from the first rank 32a of memory devices 30 and a second DQS data strobe signal from a second rank 32b of memory devices 30 and selectively switches one of the first and second DQS data strobe signals to the common DQS data strobe signal line 114.

[0067] In certain embodiments, the circuit 40 also provides the load isolation described above in reference to Figures 1-5. For example, as schematically illustrated by Figure 8C, the circuit 40 comprises both the switch 120 for the DQ data signal lines 102a, 102b and the switch 130 for the DQS data strobe signal lines 104a, 104b. While in certain embodiments, the switches 130 are integral with a logic element of the circuit 40, in certain other embodiments, the switches 130 are separate components which are operatively coupled to a logic element 122 of the circuit 40, as schematically illustrated by Figure 8D. In certain such embodiments, the control and timing of the switch 130 is performed by the circuit 40 which is resident on the memory module 10. Example switches 130 compatible with embodiments described herein include, but are not limited to field-effect transistor (FET) switches, such as the SN74AUC1G66 single bilateral analog switch available from Texas

Instruments, Inc. of Dallas, Texas, and multiplexers, such as the SN74AUC2G53 2:1 analog multiplexer/demultiplexer available from Texas Instruments, Inc. of Dallas, Texas.

[0068] The circuit 40 of certain embodiments controls the isolation of the DQS data strobe signal lines 104a, 104b by monitoring commands received by the memory module 10 from the computer system and producing “windows” of operation whereby the appropriate switches 130 are activated or deactivated to enable and disable the DQS data strobe signal lines 104a, 104b to mitigate BBARX collisions. In certain other embodiments, the circuit 40 monitors the commands received by the memory module 10 from the computer system and selectively activates or deactivates the switches 120 to enable and disable the DQ data signal lines 102a, 102b to reduce the load of the memory module 10 on the computer system. In still other embodiments, the circuit 40 performs both of these functions together.

Command Signal Translation

[0069] Most high-density memory modules are currently built with 512-Megabit (“512-Mb”) memory devices wherein each memory device has a 64M x 8-bit configuration. For example, a 1-Gigabyte (“1-GB”) memory module with error checking capabilities can be fabricated using eighteen such 512-Mb memory devices. Alternatively, it can be economically advantageous to fabricate a 1-GB memory module using lower-density memory devices and doubling the number of memory devices used to produce the desired word width. For example, by fabricating a 1-GB memory module using thirty-six 256-Mb memory devices with 64M x 4-bit configuration, the cost of the resulting 1-GB memory module can be reduced since the unit cost of each 256-Mb memory device is typically lower than one-half the unit cost of each 512-Mb memory device. The cost savings can be significant, even though twice as many 256-Mb memory devices are used in place of the 512-Mb memory devices. For example, by using pairs of 512-Mb memory devices rather than single 1-Gb memory devices, certain embodiments described herein reduce the cost of the memory module by a factor of up to approximately five.

[0070] Market pricing factors for DRAM devices are such that higher-density DRAM devices (e.g., 1-Gb DRAM devices) are much more than twice the price of lower-density DRAM devices (e.g., 512-Mb DRAM devices). In other words, the price per bit ratio of the higher-density DRAM devices is greater than that of the lower-density DRAM devices.

This pricing difference often lasts for months or even years after the introduction of the higher-density DRAM devices, until volume production factors reduce the costs of the newer higher-density DRAM devices. Thus, when the cost of a higher-density DRAM device is more than the cost of two lower-density DRAM devices, there is an economic incentive for utilizing pairs of the lower-density DRAM devices to replace individual higher-density DRAM devices.

[0071] Figure 9A schematically illustrates an exemplary memory module 10 compatible with certain embodiments described herein. The memory module 10 is connectable to a memory controller 20 of a computer system (not shown). The memory module 10 comprises a printed circuit board 210 and a plurality of memory devices 30 coupled to the printed circuit board 210. The plurality of memory devices 30 has a first number of memory devices 30. The memory module 10 further comprises a circuit 40 coupled to the printed circuit board 210. The circuit 40 receives a set of input address and command signals from the computer system. The set of input address and command signals correspond to a second number of memory devices 30 smaller than the first number of memory devices 30. The circuit 40 generates a set of output address and command signals in response to the set of input address and command signals. The set of output address and command signals corresponds to the first number of memory devices 30.

[0072] In certain embodiments, as schematically illustrated in Figure 9A, the memory module 10 further comprises a phase-lock loop device 220 coupled to the printed circuit board 210 and a register 230 coupled to the printed circuit board 210. In certain embodiments, the phase-lock loop device 220 and the register 230 are each mounted on the printed circuit board 210. In response to signals received from the computer system, the phase-lock loop device 220 transmits clock signals to the plurality of memory devices 30, the circuit 40, and the register 230. The register 230 receives and buffers a plurality of command signals and address signals (e.g., bank address signals, row address signals, column address signals, gated column address strobe signals, chip-select signals), and transmits corresponding signals to the appropriate memory devices 30. In certain embodiments, the register 230 comprises a plurality of register devices. While the phase-lock loop device 220, the register 230, and the circuit 40 are described herein in certain embodiments as being

separate components, in certain other embodiments, two or more of the phase-lock loop device 220, the register 230, and the circuit 40 are portions of a single component. Persons skilled in the art are able to select a phase-lock loop device 220 and a register 230 compatible with embodiments described herein.

[0073] In certain embodiments, the memory module 10 further comprises electrical components which are electrically coupled to one another and are surface-mounted or embedded on the printed circuit board 210. These electrical components can include, but are not limited to, electrical conduits, resistors, capacitors, inductors, and transistors. In certain embodiments, at least some of these electrical components are discrete, while in other certain embodiments, at least some of these electrical components are constituents of one or more integrated circuits.

[0074] In certain embodiments, the printed circuit board 210 is mountable in a module slot of the computer system. The printed circuit board 210 of certain such embodiments has a plurality of edge connections electrically coupled to corresponding contacts of the module slot and to the various components of the memory module 10, thereby providing electrical connections between the computer system and the components of the memory module 10.

[0075] In certain embodiments, the plurality of memory devices 30 are arranged in a first number of ranks 32. For example, in certain embodiments, the memory devices 30 are arranged in four ranks 32a, 32b, 32c, 32d, as schematically illustrated by Figure 9A. In certain other embodiments, the memory devices 30 are arranged in two ranks 32a, 32b, as schematically illustrated by Figure 9B. Other numbers of ranks 32 of the memory devices 30 are also compatible with embodiments described herein.

[0076] As schematically illustrated by Figures 9A and 9B, in certain embodiments, the circuit 40 receives a set of input command signals (e.g., refresh, precharge) and address signals (e.g., bank address signals, row address signals, column address signals, gated column address strobe signals, chip-select signals) from the memory controller 20 of the computer system. In response to the set of input address and command signals, the circuit 40 generates a set of output address and command signals.

[0077] In certain embodiments, the set of output address and command signals corresponds to a first number of ranks in which the plurality of memory devices 30 of the memory module 10 are arranged, and the set of input address and command signals corresponds to a second number of ranks per memory module for which the computer system is configured. The second number of ranks in certain embodiments is smaller than the first number of ranks. For example, in the exemplary embodiment as schematically illustrated by Figure 9A, the first number of ranks is four while the second number of ranks is two. In the exemplary embodiment of Figure 9B, the first number of ranks is two while the second number of ranks is one. Thus, in certain embodiments, even though the memory module 10 actually has the first number of ranks of memory devices 30, the memory module 10 simulates a virtual memory module by operating as having the second number of ranks of memory devices 30. In certain embodiments, the memory module 10 simulates a virtual memory module when the number of memory devices 30 of the memory module 10 is larger than the number of memory devices 30 per memory module for which the computer system is configured to utilize. In certain embodiments, the circuit 40 comprises logic (e.g., address decoding logic, command decoding logic) which translates between a system memory domain of the computer system and a physical memory domain of the memory module 10.

[0078] In certain embodiments, the computer system is configured for a number of ranks per memory module which is smaller than the number of ranks in which the memory devices 30 of the memory module 10 are arranged. In certain such embodiments, the computer system is configured for two ranks of memory per memory module (providing two chip-select signals CS_0 , CS_1) and the plurality of memory modules 30 of the memory module 10 are arranged in four ranks, as schematically illustrated by Figure 9A. In certain other such embodiments, the computer system is configured for one rank of memory per memory module (providing one chip-select signal CS_0) and the plurality of memory modules 30 of the memory module 10 are arranged in two ranks, as schematically illustrated by Figure 9B.

[0079] In the exemplary embodiment schematically illustrated by Figure 9A, the memory module 10 has four ranks of memory devices 30 and the computer system is configured for two ranks of memory devices per memory module. The memory module 10 receives row/column address signals or signal bits (A_0 - A_{n+1}), bank address signals (BA_0 -

BA_m), chip-select signals (CS₀ and CS₁), and command signals (e.g., refresh, precharge, etc.) from the computer system. The A₀-A_n row/column address signals are received by the register 230, which buffers these address signals and sends these address signals to the appropriate ranks of memory devices 30. The circuit 40 receives the two chip-select signals (CS₀, CS₁) and one row/column address signal (A_{n+1}) from the computer system. Both the circuit 40 and the register 230 receive the bank address signals (BA₀-BA_m) and at least one command signal (e.g., refresh, precharge, etc.) from the computer system.

Logic Tables

[0080] Table 1 provides a logic table compatible with certain embodiments described herein for the selection among ranks of memory devices 30 using chip-select signals.

Table 1:

State	CS ₀	CS ₁	A _{n+1}	Command	CS _{0A}	CS _{0B}	CS _{1A}	CS _{1B}
1	0	1	0	Active	0	1	1	1
2	0	1	1	Active	1	0	1	1
3	0	1	x	Active	0	0	1	1
4	1	0	0	Active	1	1	0	1
5	1	0	1	Active	1	1	1	0
6	1	0	x	Active	1	1	0	0
7	1	1	x	x	1	1	1	1

Note:

1. CS₀, CS₁, CS_{0A}, CS_{0B}, CS_{1A}, and CS_{1B} are active low signals.
2. A_{n+1} is an active high signal.
3. 'x' is a Don't Care condition.
4. Command involves a number of command signals that define operations such as refresh, precharge, and other operations.

[0081] In Logic State 1: CS₀ is active low, A_{n+1} is non-active, and Command is active. CS_{0A} is pulled low, thereby selecting Rank 0.

[0082] In Logic State 2: CS₀ is active low, A_{n+1} is active, and Command is active. CS_{0B} is pulled low, thereby selecting Rank 1.

[0083] In Logic State 3: CS₀ is active low, A_{n+1} is Don't Care, and Command is active high. CS_{0A} and CS_{0B} are pulled low, thereby selecting Ranks 0 and 1.

[0084] In Logic State 4: CS₁ is active low, A_{n+1} is non-active, and Command is active. CS_{1A} is pulled low, thereby selecting Rank 2.

[0085] In Logic State 5: CS₁ is active low, A_{n+1} is active, and Command is active. CS_{1B} is pulled low, thereby selecting Rank 3.

[0086] In Logic State 6: CS₁ is active low, A_{n+1} is Don't Care, and Command is active. CS_{1A} and CS_{1B} are pulled low, thereby selecting Ranks 2 and 3.

[0087] In Logic State 7: CS₀ and CS₁ are pulled non-active high, which deselects all ranks, i.e., CS_{0A}, CS_{0B}, CS_{1A}, and CS_{1B} are pulled high.

[0088] The "Command" column of Table 1 represents the various commands that a memory device (e.g., a DRAM device) can execute, examples of which include, but are not limited to, activation, read, write, precharge, and refresh. In certain embodiments, the command signal is passed through to the selected rank only (e.g., state 4 of Table 1). In such embodiments, the command signal (e.g., read) is sent to only one memory device or the other memory device so that data is supplied from one memory device at a time. In other embodiments, the command signal is passed through to both associated ranks (e.g., state 6 of Table 1). In such embodiments, the command signal (e.g., refresh) is sent to both memory devices to ensure that the memory content of the memory devices remains valid over time. Certain embodiments utilize a logic table such as that of Table 1 to simulate a single memory device from two memory devices by selecting two ranks concurrently.

[0089] Table 2 provides a logic table compatible with certain embodiments described herein for the selection among ranks of memory devices 30 using gated CAS signals.

Table 2:

CS*	RAS*	CAS*	WE*	Density Bit	A ₁₀	Command	CAS0*	CAS1*
1	x	x	x	x	x	NOP	x	x
0	1	1	1	x	x	NOP	1	1
0	0	1	1	0	x	ACTIVATE	1	1
0	0	1	1	1	x	ACTIVATE	1	1
0	1	0	1	0	x	READ	0	1
0	1	0	1	1	x	READ	1	0
0	1	0	0	0	x	WRITE	0	1

0	1	0	0	1	x	WRITE	1	0
0	0	1	0	0	0	PRECHARGE	1	1
0	0	1	0	1	0	PRECHARGE	1	1
0	0	1	0	x	1	PRECHARGE	1	1
0	0	0	0	x	x	MODE REG SET	0	0
0	0	0	1	x	x	REFRESH	0	0

[0090] In certain embodiments in which the density bit is a row address bit, for read/write commands, the density bit is the value latched during the activate command for the selected bank.

Serial-Presence-Detect Device

[0091] Memory modules typically include a serial-presence detect (SPD) device 240 (e.g., an electrically-erasable-programmable read-only memory or EEPROM device) comprising data which characterize various attributes of the memory module, including but not limited to, the number of row addresses the number of column addresses, the data width of the memory devices, the number of ranks, the memory density per rank, the number of memory devices, and the memory density per memory device. The SPD device 240 communicates this data to the basic input/output system (BIOS) of the computer system so that the computer system is informed of the memory capacity and the memory configuration available for use and can configure the memory controller properly for maximum reliability and performance.

[0092] For example, for a commercially-available 512-MB (64M x 8-byte) memory module utilizing eight 512-Mb memory devices each with a 64M x 8-bit configuration, the SPD device contains the following SPD data (in appropriate bit fields of these bytes):

- Byte 3: Defines the number of row address bits in the DRAM device in the memory module [13 for the 512-Mb memory device].
- Byte 4: Defines the number of column address bits in the DRAM device in the memory module [11 for the 512-Mb memory device].
- Byte 13: Defines the bit width of the primary DRAM device used in the memory module [8 bits for the 512-Mb (64M x 8-bit) memory device].
- Byte 14: Defines the bit width of the error checking DRAM device used in the memory module [8 bits for the 512-Mb (64M x 8-bit) memory device].

Byte 17: Defines the number of banks internal to the DRAM device used in the memory module [4 for the 512-Mb memory device].

[0093] In a further example, for a commercially-available 1-GB (128M x 8-byte) memory module utilizing eight 1-Gb memory devices each with a 128M x 8-bit configuration, as described above, the SPD device contains the following SPD data (in appropriate bit fields of these bytes):

Byte 3: Defines the number of row address bits in the DRAM device in the memory module [14 for the 1-Gb memory device].

Byte 4: Defines the number of column address bits in the DRAM device in the memory module [11 for the 1-Gb memory device].

Byte 13: Defines the bit width of the primary DRAM device used in the memory module [8 bits for the 1-Gb (128M x 8-bit) memory device].

Byte 14: Defines the bit width of the error checking DRAM device used in the memory module [8 bits for the 1-Gb (128M x 8-bit) memory device].

Byte 17: Defines the number of banks internal to the DRAM device used in the memory module [4 for the 1-Gb memory device].

[0094] In certain embodiments, the SPD device 240 comprises data which characterize the memory module 10 as having fewer ranks of memory devices than the memory module 10 actually has, with each of these ranks having more memory density. For example, for a memory module 10 compatible with certain embodiments described herein having two ranks of memory devices 30, the SPD device 240 comprises data which characterizes the memory module 10 as having one rank of memory devices with twice the memory density per rank. Similarly, for a memory module 10 compatible with certain embodiments described herein having four ranks of memory devices 30, the SPD device 240 comprises data which characterizes the memory module 10 as having two ranks of memory devices with twice the memory density per rank. In addition, in certain embodiments, the SPD device 240 comprises data which characterize the memory module 10 as having fewer memory devices than the memory module 10 actually has, with each of these memory devices having more memory density per memory device. For example, for a memory module 10 compatible with certain embodiments described herein, the SPD device 240 comprises data which characterizes the memory module 10 as having one-half the number of memory devices that the memory module 10 actually has, with each of these memory devices

having twice the memory density per memory device. Thus, in certain embodiments, the SPD device 240 informs the computer system of the larger memory array by reporting a memory device density that is a multiple of the memory devices 30 resident on the memory module 10. Certain embodiments described herein advantageously do not require system level changes to hardware (e.g., the motherboard of the computer system) or to software (e.g., the BIOS of the computer system).

[0095] Figure 9C schematically illustrates an exemplary memory module 10 in accordance with certain embodiments described herein. The memory module 10 comprises a pair of substantially identical memory devices 31, 33. Each memory device 31, 33 has a first bit width, a first number of banks of memory locations, a first number of rows of memory locations, and a first number of columns of memory locations. The memory module 10 further comprises an SPD device 240 comprising data that characterizes the pair of memory devices 31, 33. The data characterize the pair of memory devices 31, 33 as a virtual memory device having a second bit width equal to twice the first bit width, a second number of banks of memory locations equal to the first number of banks, a second number of rows of memory locations equal to the first number of rows, and a second number of columns of memory locations equal to the first number of columns.

[0096] In certain such embodiments, the SPD device 240 of the memory module 10 is programmed to describe the combined pair of lower-density memory devices 31, 33 as one virtual or pseudo-higher-density memory device. In an exemplary embodiment, two 512-Mb memory devices, each with a 128M x 4-bit configuration, are used to simulate one 1-Gb memory device having a 128M x 8-bit configuration. The SPD device 240 of the memory module 10 is programmed to describe the pair of 512-Mb memory devices as one virtual or pseudo-1-Gb memory device.

[0097] For example, to fabricate a 1-GB (128M x 8-byte) memory module, sixteen 512-Mb (128M x 4-bit) memory devices can be used. The sixteen 512-Mb (128M x 4-bit) memory devices are combined in eight pairs, with each pair serving as a virtual or pseudo-1-Gb (128M x 8-bit) memory device. In certain such embodiments, the SPD device 240 contains the following SPD data (in appropriate bit fields of these bytes):

Byte 3: 13 row address bits.
Byte 4: 12 column address bits.

Byte 13: 8 bits wide for the primary virtual 1-Gb (128M x 8-bit) memory device.

Byte 14: 8 bits wide for the error checking virtual 1-Gb (128M x 8-bit) memory device.

Byte 17: 4 banks.

[0098] In this exemplary embodiment, bytes 3, 4, and 17 are programmed to have the same values as they would have for a 512-MB (128M x 4-byte) memory module utilizing 512-Mb (128M x 4-bit) memory devices. However, bytes 13 and 14 of the SPD data are programmed to be equal to 8, corresponding to the bit width of the virtual or pseudo-higher-density 1-Gb (128M x 8-bit) memory device, for a total capacity of 1-GB. Thus, the SPD data does not describe the actual-lower-density memory devices, but instead describes the virtual or pseudo-higher-density memory devices. The BIOS accesses the SPD data and recognizes the memory module as having 4 banks of memory locations arranged in 2^{13} rows and 2^{12} columns, with each memory location having a width of 8 bits rather than 4 bits.

[0099] In certain embodiments, when such a memory module 10 is inserted in a computer system, the computer system's memory controller then provides to the memory module 10 a set of input address and command signals which correspond to the number of ranks or the number of memory devices reported by the SPD device 240. For example, placing a two-rank memory module 10 compatible with certain embodiments described herein in a computer system compatible with one-rank memory modules, the SPD device 240 reports to the computer system that the memory module 10 only has one rank. The circuit 40 then receives a set of input address and command signals corresponding to a single rank from the computer system's memory controller, and generates and transmits a set of output address and command signals corresponding to two ranks to the appropriate memory devices 30 of the memory module 10.

[0100] Similarly, when a two-rank memory module 10 compatible with certain embodiments described herein is placed in a computer system compatible with either one- or two-rank memory modules, the SPD device 240 reports to the computer system that the memory module 10 only has one rank. The circuit 40 then receives a set of input address and command signals corresponding to a single rank from the computer system's memory controller, and generates and transmits a set of output address and command signals corresponding to two ranks to the appropriate memory devices 30 of the memory module 10.

[0101] Furthermore, a four-rank memory module 10 compatible with certain embodiments described herein simulates a two-rank memory module whether the memory module 10 is inserted in a computer system compatible with two-rank memory modules or with two- or four-rank memory modules. Thus, by placing a four-rank memory module 10 compatible with certain embodiments described herein in a module slot that is four-rank-ready, the computer system provides four chip-select signals, but the memory module 10 only uses two of the chip-select signals.

[0102] In certain embodiments, the circuit 40 comprises the SPD device 240 which reports the CAS latency (CL) to the memory controller of the computer system. The SPD device 240 of certain embodiments reports a CL which has one more cycle than does the actual operational CL of the memory array. In certain embodiments, data transfers between the memory controller and the memory module are registered for one additional clock cycle by the circuit 40. The additional clock cycle of certain embodiments is added to the transfer time budget with an incremental overall CAS latency. This extra cycle of time in certain embodiments advantageously provides sufficient time budget to add a buffer which electrically isolates the ranks of memory devices 30 from the memory controller 20. The buffer of certain embodiments comprises combinatorial logic, registers, and logic pipelines. In certain embodiments, the buffer adds a one-clock cycle time delay, which is equivalent to a registered DIMM, to accomplish the address decoding. The one-cycle time delay of certain such embodiments provides sufficient time for read and write data transfers to provide the functions of the data path multiplexer/demultiplexer. Thus, for example, a DDR2 400-MHz memory system in accordance with embodiments described herein has an overall CAS latency of four, and uses memory devices with a CAS latency of three. In still other embodiments, the SPD device 240 does not utilize this extra cycle of time.

Memory Density Multiplication

[0103] In certain embodiments, two memory devices having a memory density are used to simulate a single memory device having twice the memory density, and an additional address signal bit is used to access the additional memory. Similarly, in certain embodiments, two ranks of memory devices having a memory density are used to simulate a single rank of memory devices having twice the memory density, and an additional address

signal bit is used to access the additional memory. As used herein, such simulations of memory devices or ranks of memory devices are termed as “memory density multiplication,” and the term “density transition bit” is used to refer to the additional address signal bit which is used to access the additional memory by selecting which rank of memory devices is enabled for a read or write transfer operation.

[0104] For example, for computer systems which are normally limited to using memory modules which have a single rank of 128M x 4-bit memory devices, certain embodiments described herein enable the computer system to utilize memory modules which have double the memory (e.g., two ranks of 128M x 4-bit memory devices). The circuit 40 of certain such embodiments provides the logic (e.g., command and address decoding logic) to double the number of chip selects, and the SPD device 240 reports a memory device density of 256M x 4-bit to the computer system.

[0105] In certain embodiments utilizing memory density multiplication embodiments, the memory module 10 can have various types of memory devices 30 (e.g., DDR1, DDR2, DDR3, and beyond). The circuit 40 of certain such embodiments utilizes implied translation logic equations having variations depending on whether the density transition bit is a row, column, or internal bank address bit. In addition, the translation logic equations of certain embodiments vary depending on the type of memory module 10 (e.g., UDIMM, RDIMM, FBDIMM, etc.). Furthermore, in certain embodiments, the translation logic equations vary depending on whether the implementation multiplies memory devices per rank or multiplies the number of ranks per memory module.

[0106] Table 3A provides the numbers of rows and columns for DDR-1 memory devices, as specified by JEDEC standard JESD79D, “Double Data Rate (DDR) SDRAM Specification,” published February 2004, and incorporated in its entirety by reference herein.

Table 3A:

	128-Mb	256-Mb	512-Mb	1-Gb
Number of banks	4	4	4	4
Number of row address bits	12	13	13	14
Number of column address bits for “x 4” configuration	11	11	12	12
Number of column address bits for “x 8” configuration	10	10	11	11

Number of column address bits for "x 16" configuration	9	9	10	10
--	---	---	----	----

[0107] As described by Table 3A, 512-Mb (128M x 4-bit) DRAM devices have 2^{13} rows and 2^{12} columns of memory locations, while 1-Gb (128M x 8-bit) DRAM devices have 2^{14} rows and 2^{11} columns of memory locations. Because of the differences in the number of rows and the number of columns for the two types of memory devices, complex address translation procedures and structures would typically be needed to fabricate a 1-GB (128M x 8-byte) memory module using sixteen 512-Mb (128M x 4-bit) DRAM devices.

[0108] Table 3B shows the device configurations as a function of memory density for DDR2 memory devices.

Table 3B:

	Number of Rows	Number of Columns	Number of Internal Banks	Page Size (x4s or x8s)
256 Mb	13	11	4	1 KB
512 Mb	14	11	4	1 KB
1 Gb	14	11	8	1 KB
2 Gb	15	11	8	1 KB
4 Gb	16	11	8	1 KB

Table 4 lists the corresponding density transition bit for the density transitions between the DDR2 memory densities of Table 3B.

Table 4:

Density Transition	Density Transition Bit
256 Mb to 512 Mb	A ₁₃
512 Mb to 1 Gb	BA ₂
1 Gb to 2 Gb	A ₁₄
2 Gb to 4 Gb	A ₁₅

Other certain embodiments described herein utilize a transition bit to provide a transition from pairs of physical 4-Gb memory devices to simulated 8-Gb memory devices.

[0109] In an example embodiment, the memory module comprises one or more pairs of 256-Mb memory devices, with each pair simulating a single 512-Mb memory device. The simulated 512-Mb memory device has four internal banks while each of the two 256-Mb memory devices has four internal banks, for a total of eight internal banks for the pair of 256-Mb memory devices. In certain embodiments, the additional row address bit is translated by

the circuit 40 to the rank selection between each of the two 256-Mb memory devices of the pair. Although there are eight total internal banks in the rank-converted memory array, the computer system is only aware of four internal banks. When the memory controller activates a row for a selected bank, the circuit 40 activates the same row for the same bank, but it does so for the selected rank according to the logic state of the additional row address bit A₁₃.

[0110] In another example embodiment, the memory module comprises one or more pairs of 512-Mb memory devices, with each pair simulating a single 1-Gb memory device. The simulated 1-Gb memory device has eight internal banks while each of the two 512-Mb memory devices has four internal banks, for a total of eight internal banks for the pair of 512-Mb memory devices. In certain embodiments, the mapped BA₂ (bank 2) bit is used to select between the two ranks of 512-Mb memory devices to preserve the internal bank geometry expected by the memory controller of the computer system. The state of the BA₂ bit selects the upper or lower set of four banks, as well as the upper and lower 512-Mb rank.

[0111] In another example embodiment, the memory module comprises one or more pairs of 1-Gb memory devices, with each pair simulating a single 2-Gb memory device. Each of the two 1-Gb memory devices has eight internal banks for a total of sixteen internal banks, while the simulated 2-Gb memory device has eight internal banks. In certain embodiments, the additional row address bit translates to the rank selection between the two 1-Gb memory devices. Although there are sixteen total internal banks per pair of 1-Gb memory devices in the rank-converted memory array, the memory controller of the computer system is only aware of eight internal banks. When the memory controller activates a row of a selected bank, the circuit 40 activates the same row for the same bank, but it does so for the selected rank according to the logic state of the additional row address bit A₁₄.

[0112] The circuit 40 of certain embodiments provides substantially all of the translation logic used for the decoding (e.g., command and address decoding). In certain such embodiments, there is a fully transparent operational conversion from the "system memory" density domain of the computer system to the "physical memory" density domain of the memory module 10. In certain embodiments, the logic translation equations are programmed in the circuit 40 by hardware, while in certain other embodiments, the logic

translation equations are programmed in the circuit 40 by software. Examples 1 and 2 provide exemplary sections of Verilog code compatible with certain embodiments described herein. As described more fully below, the code of Examples 1 and 2 includes logic to reduce potential problems due to “back-to-back adjacent read commands which cross memory device boundaries or “BBARX.” Persons skilled in the art are able to provide additional logic translation equations compatible with embodiments described herein.

[0113] An exemplary section of Verilog code compatible with memory density multiplication from 512 Mb to 1 Gb using DDR2 memory devices with the BA₂ density transition bit is listed below in Example 2. The exemplary code of Example 2 corresponds to a circuit 40 which receives one chip-select signal from the computer system and which generates two chip-select signals.

[0114] Example 2:

```
always @(posedge clk_in)
begin
    rs0N_R <= rs0_in_N;    // cs0
    rasN_R <= ras_in_N;
    casN_R <= cas_in_N;
    weN_R <= we_in_N;

end

// Gated Chip Selects
assign pcs0a_1 = (~rs0_in_N & ~ras_in_N & ~cas_in_N)           // ref,md reg set
                | (~rs0_in_N & ras_in_N & cas_in_N)           // ref exit, pwr dn
                | (~rs0_in_N & ~ras_in_N & cas_in_N & ~we_in_N & a10_in) // pchg all
                | (~rs0_in_N & ~ras_in_N & cas_in_N & ~we_in_N & ~a10_in & ~ba2_in) // pchg single bnk
                | (~rs0_in_N & ~ras_in_N & cas_in_N & we_in_N & ~ba2_in) // activate
                | (~rs0_in_N & ras_in_N & ~cas_in_N & ~ba2_in) // xfr
                ;
assign pcs0b_1 = (~rs0_in_N & ~ras_in_N & ~cas_in_N)           // ref,md reg set
                | (~rs0_in_N & ras_in_N & cas_in_N)           // ref exit, pwr dn
                | (~rs0_in_N & ~ras_in_N & cas_in_N & ~we_in_N & a10_in) // pchg all
                | (~rs0_in_N & ~ras_in_N & cas_in_N & ~we_in_N & ~a10_in & ba2_in) // pchg single bnk
                | (~rs0_in_N & ~ras_in_N & cas_in_N & we_in_N & ba2_in) // activate
                | (~rs0_in_N & ras_in_N & ~cas_in_N & ba2_in) // xfr
                ;

//-----
always @(posedge clk_in)
begin
    a4_r <= a4_in ;
    a5_r <= a5_in ;
    a6_r <= a6_in ;
    a10_r <= a10_in ;
    ba0_r <= ba0_in ;
    ba1_r <= ba1_in ;
    ba2_r <= ba2_in ;
    q_mrs_cmd_cycl <= q_mrs_cmd ;

end
////////////////////////////////////
// determine the cas latency
////////////////////////////////////
assign q_mrs_cmd_r = (!rasN_R & !casN_R & !weN_R)
                    & !rs0N_R
                    & (!ba0_r & !ba1_r)
```

```

; // md reg set cmd

always @(posedge clk_in)
if (~reset_N) // lmr
    cl3 <= 1'b1 ;
else if (q_mrs_cmd_cyc1) // load mode reg cmd
begin
    cl3 <= (~a6_r & a5_r & a4_r);
end

always @(posedge clk_in)
if (~reset_N) // reset
    cl2 <= 1'b0 ;
else if (q_mrs_cmd_cyc1) // load mode reg cmd
begin
    cl2 <= (~a6_r & a5_r & ~a4_r);
end

always @(posedge clk_in)
if (~reset_N) // reset
    cl4 <= 1'b0 ;
else if (q_mrs_cmd_cyc1) // load mode reg cmd
begin
    cl4 <= (a6_r & ~a5_r & ~a4_r);
end

always @(posedge clk_in)
if (~reset_N) cl5 <= 1'b0 ;
else if (q_mrs_cmd_cyc1) // load mode reg cmd
begin
    cl5 <= (a6_r & ~a5_r & a4_r);
end

assign pre_cyc2_enfet = (wr_cmd_cyc1 & acs_cyc1 & cl3) // wr brst cl3 preamble
;
assign pre_cyc3_enfet = (rd_cmd_cyc2 & cl3) // rd brst cl3 preamble
| (wr_cmd_cyc2 & cl3) // wr brst cl3 1st pair
| (wr_cmd_cyc2 & cl4) // wr brst cl4 preamble
;

assign pre_cyc4_enfet = (wr_cmd_cyc3 & cl3) // wr brst cl3 2nd pair
| (wr_cmd_cyc3 & cl4) // wr brst cl4 1st pair
| (rd_cmd_cyc3 & cl3) // rd brst cl3 1st pair
| (rd_cmd_cyc3 & cl4) // rd brst cl4 preamble
;

assign pre_cyc5_enfet = (rd_cmd_cyc4 & cl3) // rd brst cl3 2nd pair
| (wr_cmd_cyc4 & cl4) // wr brst cl4 2nd pair
| (rd_cmd_cyc4 & cl4) // rd brst cl4 1st pair
;

// dq
assign pre_dq_cyc = pre_cyc2_enfet
| pre_cyc3_enfet
| pre_cyc4_enfet
| pre_cyc5_enfet
;

assign pre_dq_ncyc = enfet_cyc2
| enfet_cyc3
| enfet_cyc4
| enfet_cyc5
;

// dqs

```

```

assign      pre_dqsa_cyc = (pre_cyc2_enfet & ~ba2_r)
              |(pre_cyc3_enfet & ~ba2_cyc2)
              |(pre_cyc4_enfet & ~ba2_cyc3)
              |(pre_cyc5_enfet & ~ba2_cyc4)
              ;
assign      pre_dqsb_cyc = (pre_cyc2_enfet & ba2_r)
              |(pre_cyc3_enfet & ba2_cyc2)
              |(pre_cyc4_enfet & ba2_cyc3)
              |(pre_cyc5_enfet & ba2_cyc4)
              ;
assign      pre_dqsa_ncyc = (enfet_cyc2 & ~ba2_cyc2)
              |(enfet_cyc3 & ~ba2_cyc3)
              |(enfet_cyc4 & ~ba2_cyc4)
              |(enfet_cyc5 & ~ba2_cyc5)
              ;
assign      pre_dqsb_ncyc = (enfet_cyc2 & ba2_cyc2)
              |(enfet_cyc3 & ba2_cyc3)
              |(enfet_cyc4 & ba2_cyc4)
              |(enfet_cyc5 & ba2_cyc5)
              ;

always @(posedge clk_in)
begin
    acs_cyc2 <= acs_cyc1 ;           // cs active
    ba2_cyc2 <= ba2_r ;
    ba2_cyc3 <= ba2_cyc2 ;
    ba2_cyc4 <= ba2_cyc3 ;
    ba2_cyc5 <= ba2_cyc4 ;

    rd_cmd_cyc2 <= rd_cmd_cyc1 & acs_cyc1;
    rd_cmd_cyc3 <= rd_cmd_cyc2 ;
    rd_cmd_cyc4 <= rd_cmd_cyc3 ;
    rd_cmd_cyc5 <= rd_cmd_cyc4 ;
    rd_cmd_cyc6 <= rd_cmd_cyc5 ;
    rd_cmd_cyc7 <= rd_cmd_cyc6 ;

    wr_cmd_cyc2 <= wr_cmd_cyc1 & acs_cyc1;
    wr_cmd_cyc3 <= wr_cmd_cyc2 ;
    wr_cmd_cyc4 <= wr_cmd_cyc3 ;
    wr_cmd_cyc5 <= wr_cmd_cyc4 ;

end

always @(negedge clk_in)
begin
    dq_ncyc <= dq_cyc;
    dqs_ncyc_a <= dqs_cyc_a;
    dqs_ncyc_b <= dqs_cyc_b;

end

// DQ FET enables
assign      enq_fet1 = dq_cyc | dq_ncyc ;
assign      enq_fet2 = dq_cyc | dq_ncyc ;
assign      enq_fet3 = dq_cyc | dq_ncyc ;
assign      enq_fet4 = dq_cyc | dq_ncyc ;
assign      enq_fet5 = dq_cyc | dq_ncyc ;

// DQS FET enables
assign      ens_fet1a = dqs_cyc_a | dqs_ncyc_a ;
assign      ens_fet2a = dqs_cyc_a | dqs_ncyc_a ;
assign      ens_fet3a = dqs_cyc_a | dqs_ncyc_a ;
assign      ens_fet1b = dqs_cyc_b | dqs_ncyc_b ;
assign      ens_fet2b = dqs_cyc_b | dqs_ncyc_b ;
assign      ens_fet3b = dqs_cyc_b | dqs_ncyc_b ;

```

[0115] Another exemplary section of Verilog code compatible with memory density multiplication from 256 Mb to 512 Mb using DDR2 memory devices and gated CAS

signals with the row A₁₃ density transition bit is listed below in Example 3. The exemplary code of Example 3 corresponds to a circuit 40 which receives one gated CAS signal from the computer system and which generates two gated CAS signals.

[0116] Example 3:

```
// latched a13 flags cs0, banks 0-3
always @(posedge clk_in)
  if (actv_cmd_R & ~rs0N_R & ~bnk1_R & ~bnk0_R) // activate
    begin
      l_a13_00 <= a13_r;
    end
  always @(posedge clk_in)
    if (actv_cmd_R & ~rs0N_R & ~bnk1_R & bnk0_R) // activate
      begin
        l_a13_01 <= a13_r;
      end
    always @(posedge clk_in)
      if (actv_cmd_R & ~rs0N_R & bnk1_R & ~bnk0_R) // activate
        begin
          l_a13_10 <= a13_r;
        end
      always @(posedge clk_in)
        if (actv_cmd_R & ~rs0N_R & bnk1_R & bnk0_R) // activate
          begin
            l_a13_11 <= a13_r;
          end
        end
// gated cas
assign cas_i = ~(casN_R);
assign cas0_o = (~rasN_R & cas_i)
  | (rasN_R & ~l_a13_00 & ~bnk1_R & ~bnk0_R & cas_i)
  | (rasN_R & ~l_a13_01 & ~bnk1_R & bnk0_R & cas_i)
  | (rasN_R & ~l_a13_10 & bnk1_R & ~bnk0_R & cas_i)
  | (rasN_R & ~l_a13_11 & bnk1_R & bnk0_R & cas_i);
assign cas1_o = (~rasN_R & cas_i)
  | (rasN_R & l_a13_00 & ~bnk1_R & ~bnk0_R & cas_i)
  | (rasN_R & l_a13_01 & ~bnk1_R & bnk0_R & cas_i)
  | (rasN_R & l_a13_10 & bnk1_R & ~bnk0_R & cas_i)
  | (rasN_R & l_a13_11 & bnk1_R & bnk0_R & cas_i);
assign pcas_0_N = ~cas0_o;
assign pcas_1_N = ~cas1_o;

assign rd0_o_R1 = rasN_R & cas0_o & weN_R & ~rs0N_R; // mk0 rd cmd cyc
assign rd1_o_R1 = rasN_R & cas1_o & weN_R & ~rs0N_R; // mk1 rd cmd cyc
assign wr0_o_R1 = rasN_R & cas0_o & ~weN_R & ~rs0N_R; // mk0 wr cmd cyc
assign wr1_o_R1 = rasN_R & cas1_o & ~weN_R & ~rs0N_R; // mk1 wr cmd cyc

always @(posedge clk_in)
  begin
    rd0_o_R2 <= rd0_o_R1;
    rd0_o_R3 <= rd0_o_R2;
    rd0_o_R4 <= rd0_o_R3;
    rd0_o_R5 <= rd0_o_R4;

    rd1_o_R2 <= rd1_o_R1;
    rd1_o_R3 <= rd1_o_R2;
    rd1_o_R4 <= rd1_o_R3;
    rd1_o_R5 <= rd1_o_R4;

    wr0_o_R2 <= wr0_o_R1;
  end
```

```

        wr0_o_R3 <= wr0_o_R2;
        wr0_o_R4 <= wr0_o_R3;

        wr1_o_R2 <= wr1_o_R1;
        wr1_o_R3 <= wr1_o_R2;
        wr1_o_R4 <= wr1_o_R3;
    end

    always @(posedge clk_in)
    begin
        if (
            (rd0_o_R2 & ~rd1_o_R4)                // pre-am rd if no ped on mnk 1
            | rd0_o_R3                               // 1st cyc of rd brst
            | rd0_o_R4                               // 2nd cyc of rd brst
            | (rd0_o_R5 & ~rd1_o_R2 & ~rd1_o_R3)    // post-rd cyc if no ped on mnk 1
            | (wr0_o_R1)                             // pre-am wr
            | wr0_o_R2 | wr0_o_R3                   // wr brst 1st & 2nd cyc
            | (wr0_o_R4)                             // post-wr cyc (chgef9)
            | wr1_o_R1 | wr1_o_R2 | wr1_o_R3 | wr1_o_R4 // rank 1 (chgef9)
        )
            en_fet_a <= 1'b1;                      // enable fet
        else
            en_fet_a <= 1'b0;                      // disable fet
        end

    always @(posedge clk_in)
    begin
        if (
            (rd1_o_R2 & ~rd0_o_R4)
            | rd1_o_R3
            | rd1_o_R4
            | (rd1_o_R5 & ~rd0_o_R2 & ~rd0_o_R3)
            | (wr1_o_R1)                             // (chgef8)
            | wr1_o_R2 | wr1_o_R3
            | (wr1_o_R4)                             // post-wr cyc (chgef9)
            | wr0_o_R1 | wr0_o_R2 | wr0_o_R3 | wr0_o_R4 // rank 0 (chgef9)
        )
            en_fet_b <= 1'b1;                      //
        else
            en_fet_b <= 1'b0;
        end
    end

```

[0117] In certain embodiments, the chipset memory controller of the computer system uses the inherent behavioral characteristics of the memory devices (e.g., DDR2 memory devices) to optimize throughput of the memory system. For example, for each internal bank in the memory array, a row (e.g., 1KB page) is advantageously held activated for an extended period of time. The memory controller, by anticipating a high number of memory accesses or hits to a particular region of memory, can exercise this feature to advantageously eliminate time-consuming pre-charge cycles. In certain such embodiments in which two half-density memory devices are transparently substituted for a single full-density memory device (as reported by the SPD device 240 to the memory controller), the memory devices advantageously support the “open row” feature.

[0118] Figure 10A schematically illustrates an exemplary memory module 10 which doubles the rank density in accordance with certain embodiments described herein.

The memory module 10 has a first memory capacity. The memory module 10 comprises a plurality of substantially identical memory devices 30 configured as a first rank 32a and a second rank 32b. In certain embodiments, the memory devices 30 of the first rank 32a are configured in pairs, and the memory devices 30 of the second rank 32b are also configured in pairs. In certain embodiments, the memory devices 30 of the first rank 32a are configured with their respective DQS pins tied together and the memory devices 30 of the second rank 32b are configured with their respective DQS pins tied together, as described more fully below. The memory module 10 further comprises a circuit 40 which receives a first set of address and command signals from a memory controller (not shown) of the computer system. The first set of address and command signals is compatible with a second memory capacity substantially equal to one-half of the first memory capacity. The circuit 40 translates the first set of address and command signals into a second set of address and command signals which is compatible with the first memory capacity of the memory module 10 and which is transmitted to the first rank 32a and the second rank 32b.

[0119] The first rank 32a of Figure 10A has 18 memory devices 30 and the second rank 32b of Figure 10A has 18 memory devices 30. Other numbers of memory devices 30 in each of the ranks 32a, 32b are also compatible with embodiments described herein.

[0120] In the embodiment schematically illustrated by Figure 10A, the memory module 10 has a width of 8 bytes (or 64 bits) and each of the memory devices 30 of Figure 10A has a bit width of 4 bits. The 4-bit-wide (“x 4”) memory devices 30 of Figure 10A have one-half the width, but twice the depth of 8-bit-wide (“x 8”) memory devices. Thus, each pair of “x 4” memory devices 30 has the same density as a single “x 8” memory device, and pairs of “x 4” memory devices 30 can be used instead of individual “x 8” memory devices to provide the memory density of the memory module 10. For example, a pair of 512-Mb 128M x 4-bit memory devices has the same memory density as a 1-Gb 128M x 8-bit memory device.

[0121] For two “x 4” memory devices 30 to work in tandem to mimic a “x 8” memory device, the relative DQS pins of the two memory devices 30 in certain embodiments are advantageously tied together, as described more fully below. In addition, to access the

memory density of a high-density memory module 10 comprising pairs of “x 4” memory devices 30, an additional address line is used. While a high-density memory module comprising individual “x 8” memory devices with the next-higher density would also utilize an additional address line, the additional address lines are different in the two memory module configurations.

[0122] For example, a 1-Gb 128M x 8-bit DDR-1 DRAM memory device uses row addresses A_{13} - A_0 and column addresses A_{11} and A_9 - A_0 . A pair of 512-Mb 128M x 4-bit DDR-1 DRAM memory devices uses row addresses A_{12} - A_0 and column addresses A_{12} , A_{11} , and A_9 - A_0 . In certain embodiments, a memory controller of a computer system utilizing a 1-GB 128M x 8 memory module 10 comprising pairs of the 512-Mb 128M x 4 memory devices 30 supplies the address and command signals including the extra row address (A_{13}) to the memory module 10. The circuit 40 receives the address and command signals from the memory controller and converts the extra row address (A_{13}) into an extra column address (A_{12}).

[0123] Figure 10B schematically illustrates an exemplary circuit 40 compatible with embodiments described herein. The circuit 40 is used for a memory module 10 comprising pairs of “x 4” memory devices 30 which mimic individual “x 8” memory devices. In certain embodiments, each pair has the respective DQS pins of the memory devices 30 tied together. In certain embodiments, as schematically illustrated by Figure 10B, the circuit 40 comprises a programmable-logic device (PLD) 42, a first multiplexer 44 electrically coupled to the first rank 32a of memory devices 30, and a second multiplexer 46 electrically coupled to the second rank 32b of memory devices 30. In certain embodiments, the PLD 42 and the first and second multiplexers 44, 46 are discrete elements, while in other certain embodiments, they are integrated within a single integrated circuit. Persons skilled in the art can select an appropriate PLD 42, first multiplexer 44, and second multiplexer 46 in accordance with embodiments described herein.

[0124] In the exemplary circuit 40 of Figure 10B, during a row access procedure (CAS is high), the first multiplexer 44 passes the A_{12} address through to the first rank 32, the second multiplexer 46 passes the A_{12} address through to the second rank 34, and the PLD 42 saves or latches the A_{13} address from the memory controller. In certain embodiments, a copy

of the A_{13} address is saved by the PLD 42 for each of the internal banks (e.g., 4 internal banks) per memory device 30. During a subsequent column access procedure (CAS is low), the first multiplexer 44 passes the previously-saved A_{13} address through to the first rank 32a as the A_{12} address and the second multiplexer 46 passes the previously-saved A_{13} address through to the second rank 32b as the A_{12} address. The first rank 32a and the second rank 32b thus interpret the previously-saved A_{13} row address as the current A_{12} column address. In this way, in certain embodiments, the circuit 40 translates the extra row address into an extra column address in accordance with certain embodiments described herein.

[0125] Thus, by allowing two lower-density memory devices to be used rather than one higher-density memory device, certain embodiments described herein provide the advantage of using lower-cost, lower-density memory devices to build “next-generation” higher-density memory modules. Certain embodiments advantageously allow the use of lower-cost readily-available 512-Mb DDR-2 SDRAM devices to replace more expensive 1-Gb DDR-2 SDRAM devices. Certain embodiments advantageously reduce the total cost of the resultant memory module.

[0126] Figure 11A schematically illustrates an exemplary memory module 10 which doubles number of ranks in accordance with certain embodiments described herein. The memory module 10 has a first plurality of memory locations with a first memory density. The memory module 10 comprises a plurality of substantially identical memory devices 30 configured as a first rank 32a, a second rank 32b, a third rank 32c, and a fourth rank 32d. The memory module 10 further comprises a circuit 40 which receives a first set of address and command signals from a memory controller (not shown). The first set of address and command signals is compatible with a second plurality of memory locations having a second memory density. The second memory density is substantially equal to one-half of the first memory density. The circuit 40 translates the first set of address and command signals into a second set of address and command signals which is compatible with the first plurality of memory locations of the memory module 10 and which is transmitted to the first rank 32a, the second rank 32b, the third rank 32c, and the fourth rank 32d.

[0127] Each rank 32a, 32b, 32c, 32d of Figure 11A has 9 memory devices 30. Other numbers of memory devices 30 in each of the ranks 32a, 32b, 32c, 32d are also compatible with embodiments described herein.

[0128] In the embodiment schematically illustrated by Figure 11A, the memory module 10 has a width of 8 bytes (or 64 bits) and each of the memory devices 30 of Figure 11A has a bit width of 8 bits. Because the memory module 10 has twice the number of 8-bit-wide (“x 8”) memory devices 30 as does a standard 8-byte-wide memory module, the memory module 10 has twice the density as does a standard 8-byte-wide memory module. For example, a 1-GB 128M x 8-byte memory module with 36 512-Mb 128M x 8-bit memory devices (arranged in four ranks) has twice the memory density as a 512-Mb 128M x 8-byte memory module with 18 512-Mb 128M x 8-bit memory devices (arranged in two ranks).

[0129] To access the additional memory density of the high-density memory module 10, the two chip-select signals (CS₀, CS₁) are used with other address and command signals to gate a set of four gated CAS signals. For example, to access the additional ranks of four-rank 1-GB 128M x 8-byte DDR-1 DRAM memory module, the CS₀ and CS₁ signals along with the other address and command signals are used to gate the CAS signal appropriately, as schematically illustrated by Figure 11A. Figure 11B schematically illustrates an exemplary circuit 40 compatible with embodiments described herein. In certain embodiments, the circuit 40 comprises a programmable-logic device (PLD) 42 and four “OR” logic elements 52, 54, 56, 58 electrically coupled to corresponding ranks 32a, 32b, 32c, 32d of memory devices 30.

[0130] In certain embodiments, the PLD 42 comprises an ASIC, an FPGA, a custom-designed semiconductor device, or a CPLD. In certain embodiments, the PLD 42 and the four “OR” logic elements 52, 54, 56, 58 are discrete elements, while in other certain embodiments, they are integrated within a single integrated circuit. Persons skilled in the art can select an appropriate PLD 42 and appropriate “OR” logic elements 52, 54, 56, 58 in accordance with embodiments described herein.

[0131] In the embodiment schematically illustrated by Figure 11B, the PLD 42 transmits each of the four “enabled CAS” (ENCAS_{0a}, ENCAS_{0b}, ENCAS_{1a}, ENCAS_{1b}) signals to a corresponding one of the “OR” logic elements 52, 54, 56, 58. The CAS signal is

also transmitted to each of the four “OR” logic elements 52, 54, 56, 58. The CAS signal and the “enabled CAS” signals are “low” true signals. By selectively activating each of the four “enabled CAS” signals which are inputted into the four “OR” logic elements 52, 54, 56, 58, the PLD 42 is able to select which of the four ranks 32a, 32b, 32c, 32d is active.

[0132] In certain embodiments, the PLD 42 uses sequential and combinatorial logic procedures to produce the gated CAS signals which are each transmitted to a corresponding one of the four ranks 32a, 32b, 32c, 32d. In certain other embodiments, the PLD 42 instead uses sequential and combinatorial logic procedures to produce four gated chip-select signals (e.g., CS_{0a}, CS_{0b}, CS_{1a}, and CS_{1b}) which are each transmitted to a corresponding one of the four ranks 32a, 32b, 32c, 32d.

Tied Data Strobe Signal Pins

[0133] For proper operation, the computer system advantageously recognizes a 1-GB memory module comprising 256-Mb memory devices with 64M x 4-bit configuration as a 1-GB memory module having 512-Mb memory devices with 64M x 8-bit configuration (e.g., as a 1-GB memory module with 128M x 8-byte configuration). This advantageous result is desirably achieved in certain embodiments by electrically connecting together two output signal pins (e.g., DQS or data strobe pins) of the two 256-Mb memory devices such that both output signal pins are concurrently active when the two memory devices are concurrently enabled. The DQS or data strobe is a bi-directional signal that is used during both read cycles and write cycles to validate or latch data. As used herein, the terms “tying together” or “tied together” refer to a configuration in which corresponding pins (e.g., DQS pins) of two memory devices are electrically connected together and are concurrently active when the two memory devices are concurrently enabled (e.g., by a common chip-select or CS signal). Such a configuration is different from standard memory module configurations in which the output signal pins (e.g., DQS pins) of two memory devices are electrically coupled to the same source, but these pins are not concurrently active since the memory devices are not concurrently enabled. However, a general guideline of memory module design warns against tying together two output signal pins in this way.

[0134] Figures 12 and 13 schematically illustrate a problem which may arise from tying together two output signal pins. Figure 12 schematically illustrates an exemplary

memory module 305 in which a first DQS pin 312 of a first memory device 310 is electrically connected to a second DQS pin 322 of a second memory device 320. The two DQS pins 312, 322 are both electrically connected to a memory controller 330.

[0135] Figure 13 is an exemplary timing diagram of the voltages applied to the two DQS pins 312, 322 due to non-simultaneous switching. As illustrated by Figure 13, at time t_1 , both the first DQS pin 312 and the second DQS pin 322 are high, so no current flows between them. Similarly, at time t_4 , both the first DQS pin 312 and the second DQS pin 322 are low, so no current flows between them. However, for times between approximately t_2 and approximately t_3 , the first DQS pin 312 is low while the second DQS pin 322 is high. Under such conditions, a current will flow between the two DQS pins 312, 322. This condition in which one DQS pin is low while the other DQS pin is high can occur for fractions of a second (e.g., 0.8 nanoseconds) during the dynamic random-access memory (DRAM) read cycle. During such conditions, the current flowing between the two DQS pins 312, 322 can be substantial, resulting in heating of the memory devices 310, 320, and contributing to the degradation of reliability and eventual failure of these memory devices.

[0136] A second problem may also arise from tying together two output signal pins. Figure 14 schematically illustrates another exemplary memory module 305 in which a first DQS pin 312 of a first memory device 310 is electrically connected to a second DQS pin 322 of a second memory device 320. The two DQS pins 312, 322 of Figure 14 are both electrically connected to a memory controller (not shown). The DQ (data input/output) pin 314 of the first memory device 310 and the corresponding DQ pin 324 of the second memory device 320 are each electrically connected to the memory controller by the DQ bus (not shown). Typically, each memory device 310, 320 will have a plurality of DQ pins (e.g., eight DQ pins per memory device), but for simplicity, Figure 14 only shows one DQ pin for each memory device 310, 320.

[0137] Each of the memory devices 310, 320 of Figure 14 utilizes a respective on-die termination or "ODT" circuit 332, 334 which has termination resistors (e.g., 75 ohms) internal to the memory devices 310, 320 to provide signal termination. Each memory device 310, 320 has a corresponding ODT signal pin 362, 364 which is electrically connected to the memory controller via an ODT bus 340. The ODT signal pin 362 of the first memory device

310 receives a signal from the ODT bus 340 and provides the signal to the ODT circuit 332 of the first memory device 310. The ODT circuit 332 responds to the signal by selectively enabling or disabling the internal termination resistors 352, 356 of the first memory device 310. This behavior is shown schematically in Figure 14 by the switches 342, 344 which are either closed (dash-dot line) or opened (solid line). The ODT signal pin 364 of the second memory device 320 receives a signal from the ODT bus 340 and provides the signal to the ODT circuit 334 of the second memory device 320. The ODT circuit 334 responds to the signal by selectively enabling or disabling the internal termination resistors 354, 358 of the second memory device 320. This behavior is shown schematically in Figure 14 by the switches 346, 348 which are either closed (dash-dot line) or opened (solid line). The switches 342, 344, 346, 348 of Figure 14 are schematic representations of the operation of the ODT circuits 332, 334, and do not signify that the ODT circuits 332, 334 necessarily include mechanical switches.

[0138] Examples of memory devices 310, 320 which include such ODT circuits 332, 334 include, but are not limited to, DDR2 memory devices. Such memory devices are configured to selectively enable or disable the termination of the memory device in this way in response to signals applied to the ODT signal pin of the memory device. For example, when the ODT signal pin 362 of the first memory device 310 is pulled high, the termination resistors 352, 356 of the first memory device 310 are enabled. When the ODT signal pin 362 of the first memory device 310 is pulled low (e.g., grounded), the termination resistors 352, 356 of the first memory device 310 are disabled. By selectively disabling the termination resistors of an active memory device, while leaving the termination resistors of inactive memory devices enabled, such configurations advantageously preserve signal strength on the active memory device while continuing to eliminate signal reflections at the bus-die interface of the inactive memory devices.

[0139] In certain configurations, as schematically illustrated by Figure 14, the DQS pins 312, 322 of each memory device 310, 320 are selectively connected to a voltage VTT through a corresponding termination resistor 352, 354 internal to the corresponding memory device 310, 320. Similarly, in certain configurations, as schematically illustrated by Figure 14, the DQ pins 314, 324 are selectively connected to a voltage VTT through a

corresponding termination resistor 356, 358 internal to the corresponding memory device 310, 320. In certain configurations, rather than being connected to a voltage VTT, the DQ pins 314, 324 and/or the DQS pins 312, 322 are selectively connected to ground through the corresponding termination resistors 352, 354, 356, 358. The resistances of the internal termination resistors 352, 354, 356, 358 are selected to clamp the voltages so as to reduce the signal reflections from the corresponding pins. In the configuration schematically illustrated by Figure 14, each internal termination resistor 352, 354, 356, 358 has a resistance of approximately 75 ohms.

[0140] When connecting the first memory device 310 and the second memory device 320 together to form a double word width, both the first memory device 310 and the second memory device 320 are enabled at the same time (e.g., by a common CS signal). Connecting the first memory device 310 and the second memory device 320 by tying the DQS pins 312, 322 together, as shown in Figure 14, results in a reduced effective termination resistance for the DQS pins 312, 322. For example, for the exemplary configuration of Figure 14, the effective termination resistance for the DQS pins 312, 322 is approximately 37.5 ohms, which is one-half the desired ODT resistance (for 75-ohm internal termination resistors) to reduce signal reflections since the internal termination resistors 352, 354 of the two memory devices 310, 320 are connected in parallel. This reduction in the termination resistance can result in signal reflections causing the memory device to malfunction.

[0141] Figure 15 schematically illustrates an exemplary memory module 400 in accordance with certain embodiments described herein. The memory module 400 comprises a first memory device 410 having a first data strobe (DQS) pin 412 and a second memory device 420 having a second data strobe (DQS) pin 422. The memory module 400 further comprises a first resistor 430 electrically coupled to the first DQS pin 412. The memory module 400 further comprises a second resistor 440 electrically coupled to the second DQS pin 422 and to the first resistor 430. The first DQS pin 412 is electrically coupled to the second DQS pin 422 through the first resistor 430 and through the second resistor 440.

[0142] In certain embodiments, the memory module 400 is a 1-GB unbuffered Double Data Rate (DDR) Synchronous Dynamic RAM (SDRAM) high-density dual in-line memory module (DIMM). Figures 16A and 16B schematically illustrate a first side 462 and

a second side 464, respectively, of such a memory module 400 with eighteen 64M x 4-bit, DDR-1 SDRAM FBGA memory devices on each side of a 184-pin glass-epoxy printed circuit board (PCB) 460. In certain embodiments, the memory module 400 further comprises a phase-lock-loop (PLL) clock driver 470, an EEPROM for serial-presence detect (SPD) data 480, and decoupling capacitors (not shown) mounted on the PCB in parallel to suppress switching noise on VDD and VDDQ power supply for DDR-1 SDRAM. By using synchronous design, such memory modules 400 allow precise control of data transfer between the memory module 400 and the system controller. Data transfer can take place on both edges of the DQS signal at various operating frequencies and programming latencies. Therefore, certain such memory modules 400 are suitable for a variety of high-performance system applications.

[0143] In certain embodiments, the memory module 400 comprises a plurality of memory devices configured in pairs, each pair having a first memory device 410 and a second memory device 420. For example, in certain embodiments, a 128M x 72-bit DDR SDRAM high-density memory module 400 comprises thirty-six 64M x 4-bit DDR-1 SDRAM integrated circuits in FBGA packages configured in eighteen pairs. The first memory device 410 of each pair has the first DQS pin 412 electrically coupled to the second DQS pin 422 of the second memory device 420 of the pair. In addition, the first DQS pin 412 and the second DQS pin 422 are concurrently active when the first memory device 410 and the second memory device 420 are concurrently enabled.

[0144] In certain embodiments, the first resistor 430 and the second resistor 440 each has a resistance advantageously selected to reduce the current flow between the first DQS pin 412 and the second DQS pin 422 while allowing signals to propagate between the memory controller and the DQS pins 412, 422. In certain embodiments, each of the first resistor 430 and the second resistor 440 has a resistance in a range between approximately 5 ohms and approximately 50 ohms. For example, in certain embodiments, each of the first resistor 430 and the second resistor 440 has a resistance of approximately 22 ohms. Other resistance values for the first resistor 430 and the second resistor 440 are also compatible with embodiments described herein. In certain embodiments, the first resistor 430 comprises a single resistor, while in other embodiments, the first resistor 430 comprises a plurality of

resistors electrically coupled together in series and/or in parallel. Similarly, in certain embodiments, the second resistor 440 comprises a single resistor, while in other embodiments, the second resistor 440 comprises a plurality of resistors electrically coupled together in series and/or in parallel.

[0145] Figures 17A and 17B schematically illustrate an exemplary embodiment of a memory module 400 in which the first resistor 430 and the second resistor 440 are used to reduce the current flow between the first DQS pin 412 and the second DQS pin 422. As schematically illustrated by Figure 17A, the memory module 400 is part of a computer system 500 having a memory controller 510. The first resistor 430 has a resistance of approximately 22 ohms and the second resistor 440 has a resistance of approximately 22 ohms. The first resistor 430 and the second resistor 440 are electrically coupled in parallel to the memory controller 510 through a signal line 520 having a resistance of approximately 25 ohms. The first resistor 430 and the second resistor 440 are also electrically coupled in parallel to a source of a fixed termination voltage (identified by VTT in Figures 17A and 17B) by a signal line 540 having a resistance of approximately 47 ohms. Such an embodiment can advantageously be used to allow two memory devices having lower bit widths (e.g., 4-bit) to behave as a single virtual memory device having a higher bit width (e.g., 8-bit).

[0146] Figure 17B schematically illustrates exemplary current-limiting resistors 430, 440 in conjunction with the impedances of the memory devices 410, 420. During an exemplary portion of a data read operation, the memory controller 510 is in a high-impedance condition, the first memory device 410 drives the first DQS pin 412 high (e.g., 2.7 volts), and the second memory device 420 drives the second DQS pin 422 low (e.g., 0 volts). The amount of time for which this condition occurs is approximated by the time between t_2 and t_3 of Figure 13, which in certain embodiments is approximately twice the tDQSQ (data strobe edge to output data edge skew time, e.g., approximately 0.8 nanoseconds). At least a portion of this time in certain embodiments is caused by simultaneous switching output (SSO) effects.

[0147] In certain embodiments, as schematically illustrated by Figure 17B, the DQS driver of the first memory device 410 has a driver impedance R_1 of approximately

17 ohms, and the DQS driver of the second memory device 420 has a driver impedance R_4 of approximately 17 ohms. Because the upper network of the first memory device 410 and the first resistor 430 (with a resistance R_2 of approximately 22 ohms) is approximately equal to the lower network of the second memory device 420 and the second resistor 440 (with a resistance R_3 of approximately 22 ohms), the voltage at the midpoint is approximately $0.5 * (2.7 - 0) = 1.35$ volts, which equals V_{TT} , such that the current flow across the 47-ohm resistor of Figure 17B is approximately zero.

[0148] The voltage at the second DQS pin 422 in Figure 17B is given by $V_{DQS2} = 2.7 * R_4 / (R_1 + R_2 + R_3 + R_4) = 0.59$ volts and the current flowing through the second DQS pin 422 is given by $I_{DQS2} = 0.59 / R_4 = 34$ milliamps. The power dissipation in the DQS driver of the second memory device 420 is thus $P_{DQS2} = 34 \text{ mA} * 0.59 \text{ V} = 20$ milliwatts. In contrast, without the first resistor 430 and the second resistor 440, only the 17-ohm impedances of the two memory devices 410, 420 would limit the current flow between the two DQS pins 412, 422, and the power dissipation in the DQS driver of the second memory device 420 would be approximately 107 milliwatts. Therefore, the first resistor 430 and the second resistor 440 of Figures 17A and 17B advantageously limit the current flowing between the two memory devices during the time that the DQS pin of one memory device is driven high and the DQS pin of the other memory device is driven low.

[0149] In certain embodiments in which there is overshoot or undershoot of the voltages, the amount of current flow can be higher than those expected for nominal voltage values. Therefore, in certain embodiments, the resistances of the first resistor 430 and the second resistor 440 are advantageously selected to account for such overshoot/undershoot of voltages.

[0150] For certain such embodiments in which the voltage at the second DQS pin 422 is $V_{DQS2} = 0.59$ volts and the duration of the overdrive condition is approximately 0.8 nanoseconds at maximum, the total surge is approximately $0.59 \text{ V} * 1.2 \text{ ns} = 0.3 \text{ V-ns}$. For comparison, the JEDEC standard for overshoot/undershoot is 2.4 V-ns, so certain embodiments described herein advantageously keep the total surge within predetermined standards (e.g., JEDEC standards).

[0151] Figure 18 schematically illustrates another exemplary memory module 600 compatible with certain embodiments described herein. The memory module 600 comprises a termination bus 605. The memory module 600 further comprises a first memory device 610 having a first data strobe pin 612, a first termination signal pin 614 electrically coupled to the termination bus 605, a first termination circuit 616, and at least one data pin 618. The first termination circuit 616 selectively electrically terminating the first data strobe pin 612 and the first data pin 618 in response to a first signal received by the first termination signal pin 614 from the termination bus 605. The memory module 600 further comprises a second memory device 620 having a second data strobe pin 622 electrically coupled to the first data strobe pin 612, a second termination signal pin 624, a second termination circuit 626, and at least one data pin 628. The second termination signal pin 624 is electrically coupled to a voltage, wherein the second termination circuit 626 is responsive to the voltage by not terminating the second data strobe pin 622 or the second data pin 628. The memory module 600 further comprises at least one termination assembly 630 having a third termination signal pin 634, a third termination circuit 636, and at least one termination pin 638 electrically coupled to the data pin 628 of the second memory device 620. The third termination signal pin 634 is electrically coupled to the termination bus 605. The third termination circuit 636 selectively electrically terminates the data pin 628 of the second memory device 620 through the termination pin 638 in response to a second signal received by the third termination signal pin 634 from the termination bus 605.

[0152] Figure 19 schematically illustrates a particular embodiment of the memory module 600 schematically illustrated by Figure 18. The memory module 600 comprises an on-die termination (ODT) bus 605. The memory module 600 comprises a first memory device 610 having a first data strobe (DQS) pin 612, a first ODT signal pin 614 electrically coupled to the ODT bus 605, a first ODT circuit 616, and at least one data (DQ) pin 618. The first ODT circuit 616 selectively electrically terminates the first DQS pin 612 and the DQ pin 618 of the first memory device 610 in response to an ODT signal received by the first ODT signal pin 614 from the ODT bus 605. This behavior of the first ODT circuit 616 is schematically illustrated in Figure 14 by the switches 672, 676 which are selectively closed (dash-dot line) or opened (solid line).

[0153] The memory module 600 further comprises a second memory device 620 having a second DQS pin 622 electrically coupled to the first DQS pin 612, a second ODT signal pin 624, a second ODT circuit 626, and at least one DQ pin 628. The first DQS pin 612 and the second DQS pin 622 are concurrently active when the first memory device 610 and the second memory device 620 are concurrently enabled. The second ODT signal pin 624 is electrically coupled to a voltage (e.g., ground), wherein the second ODT circuit 626 is responsive to the voltage by not terminating the second DQS pin 622 or the second DQ pin 624. This behavior of the second ODT circuit 626 is schematically illustrated in Figure 14 by the switches 674, 678 which are opened.

[0154] The memory module 600 further comprises at least one termination assembly 630 having a third ODT signal pin 634 electrically coupled to the ODT bus 605, a third ODT circuit 636, and at least one termination pin 638 electrically coupled to the DQ pin 628 of the second memory device 620. The third ODT circuit 636 selectively electrically terminates the DQ pin 628 of the second memory device 620 through the termination pin 638 in response to an ODT signal received by the third ODT signal pin 634 from the ODT bus 605. This behavior of the third ODT circuit 636 is schematically illustrated in Figure 19 by the switch 680 which is either closed (dash-dot line) or opened (solid line).

[0155] In certain embodiments, the termination assembly 630 comprises discrete electrical components which are surface-mounted or embedded on the printed-circuit board of the memory module 600. In certain other embodiments, the termination assembly 630 comprises an integrated circuit mounted on the printed-circuit board of the memory module 600. Persons skilled in the art can provide a termination assembly 630 in accordance with embodiments described herein.

[0156] Certain embodiments of the memory module 600 schematically illustrated by Figure 19 advantageously avoid the problem schematically illustrated by Figure 12 of electrically connecting the internal termination resistances of the DQS pins of the two memory devices in parallel. As described above in relation to Figure 14, Figures 18 and 19 only show one DQ pin for each memory device for simplicity. Other embodiments have a plurality of DQ pins for each memory device. In certain embodiments, each of the first ODT circuit 616, the second ODT circuit 626, and the third ODT circuit 636 are responsive to a

high voltage or signal level by enabling the corresponding termination resistors and are responsive to a low voltage or signal level (e.g., ground) by disabling the corresponding termination resistors. In other embodiments, each of the first ODT circuit 616, the second ODT circuit 626, and the third ODT circuit 636 are responsive to a high voltage or signal level by disabling the corresponding termination resistors and are responsive to a low voltage or signal level (e.g., ground) by enabling the corresponding termination resistors. Furthermore, the switches 672, 674, 676, 678, 680 of Figure 18 are schematic representations of the enabling and disabling operation of the ODT circuits 616, 626, 636 and do not signify that the ODT circuits 616, 626, 636 necessarily include mechanical switches.

[0157] The first ODT signal pin 614 of the first memory device 610 receives an ODT signal from the ODT bus 605. In response to this ODT signal, the first ODT circuit 616 selectively enables or disables the termination resistance for both the first DQS pin 612 and the DQ pin 618 of the first memory device 610. The second ODT signal pin 624 of the second memory device 620 is tied (e.g., directly hard-wired) to the voltage (e.g., ground), thereby disabling the internal termination resistors 654, 658 on the second DQS pin 622 and the second DQ pin 628, respectively, of the second memory device 620 (schematically shown by open switches 674, 678 in Figure 19). The second DQS pin 622 is electrically coupled to the first DQS pin 612, so the termination resistance for both the first DQS pin 612 and the second DQS pin 622 is provided by the termination resistor 652 internal to the first memory device 610.

[0158] The termination resistor 656 of the DQ pin 618 of the first memory device 610 is enabled or disabled by the ODT signal received by the first ODT signal pin 614 of the first memory device 610 from the ODT bus 605. The termination resistance of the DQ pin 628 of the second memory device 620 is enabled or disabled by the ODT signal received by the third ODT signal pin 634 of the termination assembly 630 which is external to the second memory device 620. Thus, in certain embodiments, the first ODT signal pin 614 and the third ODT signal pin 634 receive the same ODT signal from the ODT bus 605, and the termination resistances for both the first memory device 610 and the second memory device 620 are selectively enabled or disabled in response thereto when these memory devices are concurrently enabled. In this way, certain embodiments of the memory module 600

schematically illustrated by Figure 19 provides external or off-chip termination of the second memory device 620.

[0159] Certain embodiments of the memory module 600 schematically illustrated by Figure 19 advantageously allow the use of two lower-cost readily-available 512-Mb DDR-2 SDRAM devices to provide the capabilities of a more expensive 1-GB DDR-2 SDRAM device. Certain such embodiments advantageously reduce the total cost of the resultant memory module 600.

[0160] Certain embodiments described herein advantageously increase the memory capacity or memory density per memory slot or socket on the system board of the computer system. Certain embodiments advantageously allow for higher memory capacity in systems with limited memory slots. Certain embodiments advantageously allow for flexibility in system board design by allowing the memory module 10 to be used with computer systems designed for different numbers of ranks (e.g., either with computer systems designed for two-rank memory modules or with computer systems designed for four-rank memory modules). Certain embodiments advantageously provide lower costs of board designs.

[0161] In certain embodiments, the memory density of a memory module is advantageously doubled by providing twice as many memory devices as would otherwise be provided. For example, pairs of lower-density memory devices can be substituted for individual higher-density memory devices to reduce costs or to increase performance. As another example, twice the number of memory devices can be used to produce a higher-density memory configuration of the memory module. Each of these examples can be limited by the number of chip select signals which are available from the memory controller or by the size of the memory devices. Certain embodiments described herein advantageously provide a logic mechanism to overcome such limitations.

[0162] Various embodiments of the present invention have been described above. Although this invention has been described with reference to these specific embodiments, the descriptions are intended to be illustrative of the invention and are not intended to be limiting. Various modifications and applications may occur to those skilled in the art without departing from the true spirit and scope of the invention.

WHAT IS CLAIMED IS:

1. A circuit configured to be mounted on a memory module having a physical memory domain with a first number of ranks, each rank of the first number of ranks comprising a plurality of double-data-rate (DDR) memory devices that are configured to be activated concurrently with one another and separately from the DDR memory devices of the other ranks by a first number of chip-select signals for receiving and transmitting data having a bit width of the rank, the first number of ranks comprising a first number of DDR memory devices, the memory module configured to be operationally coupled to a computer system, the circuit configurable to:

receive a set of signals comprising bank address signals, row/column address signals, and a second number of chip-select signals, wherein the received set of signals are capable of controlling a memory module having a system memory domain with a second number of ranks of DDR memory devices that are configured to be activated concurrently with one another and separately from the DDR memory devices of the other ranks for receiving and transmitting data having a bit width of the rank, the second number of ranks comprising a second number of DDR memory devices, the second number of ranks smaller than the first number of ranks, the second number of chip-select signals smaller than the first number of chip-select signals, and the second number of DDR memory devices smaller than the first number of DDR memory devices;

generate phase-locked clock signals in response to clock signals of the computer system, wherein the circuit is configurable to transmit the generated phase-locked clock signals to the first number of ranks;

selectively isolate a load of at least one rank of the first number of ranks from the computer system in response to the received set of signals; and

translate between the system memory domain and the physical memory domain, wherein the translating comprises generating the first number of chip-select signals to the first number of ranks in response to the phase-locked clock signals and the received bank address signals, the received second number of chip-select signals, and at least one of the received row/column address signals.

2. The circuit of Claim 1, wherein the circuit is further configurable to store an address signal of the received set of signals during a row access procedure and to pass the stored address signal as an address signal to the first number of ranks during a subsequent column address procedure.

3. The circuit of Claim 1, wherein the circuit is further configurable to buffer a plurality of the received row/column address signals during a row access procedure and to transmit the plurality of the received row/column address signals to the first number of ranks during a subsequent column access procedure.

4. The circuit of Claim 3, wherein the plurality of the received row/column address signals are buffered and transmitted by the circuit at least partially in response to the phase-locked clock signals.

5. The circuit of Claim 4, wherein the circuit is configurable so that a single component of the circuit performs two or more of (i) the generating of the phase-locked clock signals, (ii) the buffering of the plurality of the received row/column address signals, and (iii) the translating between the system memory domain and the physical memory domain.

6. The circuit of Claim 1, wherein the circuit is further configurable to receive an input command signal from the computer system and to generate and transmit an output command signal to the first number of ranks.

7. The circuit of Claim 6, wherein the circuit is further configurable to respond to the received bank address signals, the received second number of chip-select signals, and the received row/column address signals by selecting at least one rank of the first number of ranks and transmitting the output command signal to the at least one selected at least one rank of the first number of ranks.

8. The circuit of Claim 1, wherein the system memory domain has a first memory density per rank and the physical memory domain has a second memory density per rank less than the first memory density per rank.

9. The circuit of Claim 1, wherein the circuit has a load and selectively isolating a load of the at least one rank from the computer system comprises presenting the load of the circuit to the computer system.

10. The circuit of Claim 1, wherein the circuit is further configurable to selectively electrically couple the first number of ranks to the computer system and to selectively isolate the first number of ranks from one another and from the computer system.

11. The circuit of Claim 10, wherein the circuit is further configurable to provide data paths for each rank of the first number of ranks, wherein the data paths are separate from one another.

12. The circuit of Claim 10, wherein the circuit is further configurable to provide data paths for each rank of the first number of ranks, wherein the data paths are separate from the computer system.

13. The circuit of Claim 1, wherein the circuit is further configurable to translate between the system memory domain and the physical memory domain by generating control signals corresponding to the physical memory domain in response to one or more control signals of the received set of signals.

14. The circuit of Claim 13, wherein the one or more control signals comprises a row address bit and the circuit is further configurable to latch the row address bit.

15. The circuit of Claim 1, wherein the circuit is further configurable to transmit a set of output signals to the first number of ranks, the set of output signals compatible with the physical memory domain.

16. The circuit of Claim 15, wherein the circuit is further configurable to receive a command signal from the computer system, to select at least one rank of the first number of ranks, and to transmit the command signal to the selected at least one rank.

17. The circuit of Claim 1, wherein the circuit is further configurable to selectively isolate a data signal line of the first number of ranks from the computer system.

18. The circuit of Claim 1, wherein the memory module has attributes and the circuit is further configurable to store data accessible to the computer system, wherein the data characterizes the memory module as having attributes that are different from the attributes of the memory module.

19. The circuit of Claim 18, wherein the attributes are selected from a group consisting of: a number of row addresses, a number of column addresses, a number of DDR

memory devices, a data width of the DDR memory devices, a memory density per DDR memory device, a number of ranks, and a memory density per rank.

20. The circuit of Claim 1, wherein the circuit is further configurable to store data accessible to the computer system, wherein the data characterizes the memory module as having the second number of ranks.

21. The circuit of Claim 20, wherein the data further characterizes the memory module as having a memory density per rank that is greater than a memory density per rank of the first number of ranks.

22. The circuit of Claim 20, wherein the data further characterizes the memory module as having the second number of DDR memory devices.

23. The circuit of Claim 22, wherein the data further characterizes the memory module as having a memory density per DDR memory device that is greater than a memory density per DDR memory device of the first number of DDR memory devices.

24. A circuit configured to be mounted on a memory module having a physical memory domain with a first number of ranks, each rank of the first number of ranks comprising a plurality of double-data-rate (DDR) memory devices that are configured to be activated concurrently with one another and separately from the DDR memory devices of the other ranks by a first number of chip-select signals for receiving and transmitting data having a bit width of the rank, the first number of ranks comprising a first number of DDR memory devices, the memory module configured to be operationally coupled to a computer system, the circuit comprising:

means for receiving a set of signals comprising bank address signals, row/column address signals, and a second number of chip-select signals, wherein the received set of signals are capable of controlling a memory module having a system memory domain with a second number of ranks of DDR memory devices that are configured to be activated concurrently with one another and separately from the DDR memory devices of the other ranks for receiving and transmitting data having a bit width of the rank, the second number of ranks comprising a second number of DDR memory devices, the second number of ranks smaller than the first number of ranks, the second number of chip-select signals smaller than the first number of chip-

select signals, and the second number of DDR memory devices smaller than the first number of DDR memory devices;

means for generating phase-locked clock signals in response to clock signals of the computer system, wherein the generated phase-locked clock signals are transmitted to the first number of ranks;

means for selectively isolating a load of at least one rank of the first number of ranks from the computer system in response to the set of received signals; and

means for translating between the system memory domain and the physical memory domain, wherein the translating comprises generating the first number of chip-select signals in response to the phase-locked clock signals and the received bank address signals, the received second number of chip-select signals, and at least one of the received row/column address signals.

25. The circuit of Claim 24, wherein the circuit further comprises means for buffering a plurality of the received row/column address signals during a row access procedure to be transmitted to the first number of ranks during a subsequent column access procedure.

26. The circuit of Claim 25, wherein the means for buffering the plurality of the received row/column address signals is at least partially responsive to the phase-locked clock signals.

27. The circuit of Claim 26, wherein two or more of the means for generating the phase-locked clock signals, the means for buffering the plurality of the received row/column address signals, and the means for translating between the system memory domain and the physical memory domain are portions of a single component.

28. The circuit of Claim 24, wherein the circuit further comprises means for generating an output command signal to be transmitted to a selected at least one rank of the first number of ranks, the means for generating the output command signal responsive to the received bank address signals, the received second number of chip-select signals, and the received row/column address signals.

29. The circuit of Claim 24, wherein the memory module has attributes and the circuit further comprises means to store data accessible to the computer system, wherein the

data characterizes the memory module as having attributes that are different from the attributes of the memory module.

30. The circuit of Claim 29, wherein the attributes are selected from a group consisting of: a number of row addresses, a number of column addresses, a number of DDR memory devices, a data width of the DDR memory devices, a memory density per DDR memory device, a number of ranks, and a memory density per rank.

31. A method of using a memory module having a physical memory domain with a first number of ranks, each rank of the first number of ranks comprising a plurality of double-data-rate (DDR) memory devices that are configured to be activated concurrently with one another and separately from the DDR memory devices of the other ranks by a first number of chip-select signals for receiving and transmitting data having a bit width of the rank, the first number of ranks comprising a first number of DDR memory devices, the memory module configured to be operationally coupled to a computer system, the method comprising:

providing a circuit configured to be mounted on the memory module;

using the circuit to receive a set of signals comprising bank address signals, row/column address signals, and a second number of chip-select signals, wherein the received set of signals are capable of controlling a memory module having a system memory domain with a second number of ranks of DDR memory devices that are configured to be activated concurrently with one another and separately from the DDR memory devices of the other ranks for receiving and transmitting data having a bit width of the rank, the second number of ranks comprising a second number of DDR memory devices, the second number of ranks smaller than the first number of ranks, the second number of chip-select signals smaller than the first number of chip-select signals, and the second number of DDR memory devices smaller than the first number of DDR memory devices;

using the circuit to generate phase-locked clock signals in response to received clock signals of the computer system, and transmitting the generated phase-locked clock signals to the DDR memory devices of the first number of ranks;

using the circuit to selectively isolate a load of at least one rank of the first number of ranks from the computer system in response to the set of received signals; and

using the circuit to translate between the system memory domain and the physical memory domain, wherein the translation comprises providing the first number of chip-select signals to the first number of ranks in response to the phase-locked clock signals and the received bank address signals, the received second number of chip-select signals, and at least one of the received row/column address signals.

32. The method of Claim 31, further comprising using the circuit to buffer a plurality of the received row/column address signals during a row access procedure and to transmit the plurality of the received row/column address signals to the first number of ranks during a subsequent column access procedure.

33. The method of Claim 32, wherein the plurality of the received row/column address signals are buffered and transmitted by the circuit at least partially in response to the phase-locked clock signals.

34. The method of Claim 33 wherein a single component of the circuit performs two or more of (i) the generating of the phase-locked clock signals, (ii) the buffering of the plurality of the received row/column address signals, and (iii) the translating between the system memory domain and the physical memory domain.

35. The method of Claim 31, further comprising using the circuit to receive an input command signal from the computer system and to generate and transmit an output command signal to the first number of ranks.

36. The method of Claim 35, further comprising using the circuit to respond to the received bank address signals, the received second number of chip-select signals, and the received row/column address signals by selecting at least one rank of the first number of ranks and transmitting the output command signal to the at least one selected at least one rank of the first number of ranks.

37. The method of Claim 31, wherein using the circuit to selectively isolate a load of the at least one rank from the computer system comprises presenting a load of the circuit to the computer system.

38. The method of Claim 31, further comprising using the circuit to selectively isolate a data signal line of the first number of ranks from the computer system.

39. The method of Claim 31, wherein the memory module has attributes and the method further comprises using the circuit to store data accessible to the computer system, wherein the data characterizes the memory module as having attributes that are different from the attributes of the memory module.

40. The method of Claim 39, wherein the attributes are selected from a group consisting of: a number of row addresses, a number of column addresses, a number of DDR memory devices, a data width of the DDR memory devices, a memory density per DDR memory device, a number of ranks, and a memory density per rank.

CIRCUIT PROVIDING LOAD ISOLATION AND MEMORY DOMAIN TRANSLATION FOR MEMORY MODULE

Abstract

A circuit is configured to be mounted on a memory module connectable to a computer system so as to be electrically coupled to a plurality of memory devices on the memory module. The memory module has a first number of ranks of double-data-rate (DDR) memory devices activated by a first number of chip-select signals. The circuit is configurable to receive bank address signals, a second number of chip-select signals, and row/column address signals from the computer system. The circuit is further configurable to generate phase-locked clock signals in response to clock signals received from the computer system, to selectively isolate one or more loads of the first number of ranks from the computer system, and to translate between a system memory domain and a physical memory domain of the memory module.

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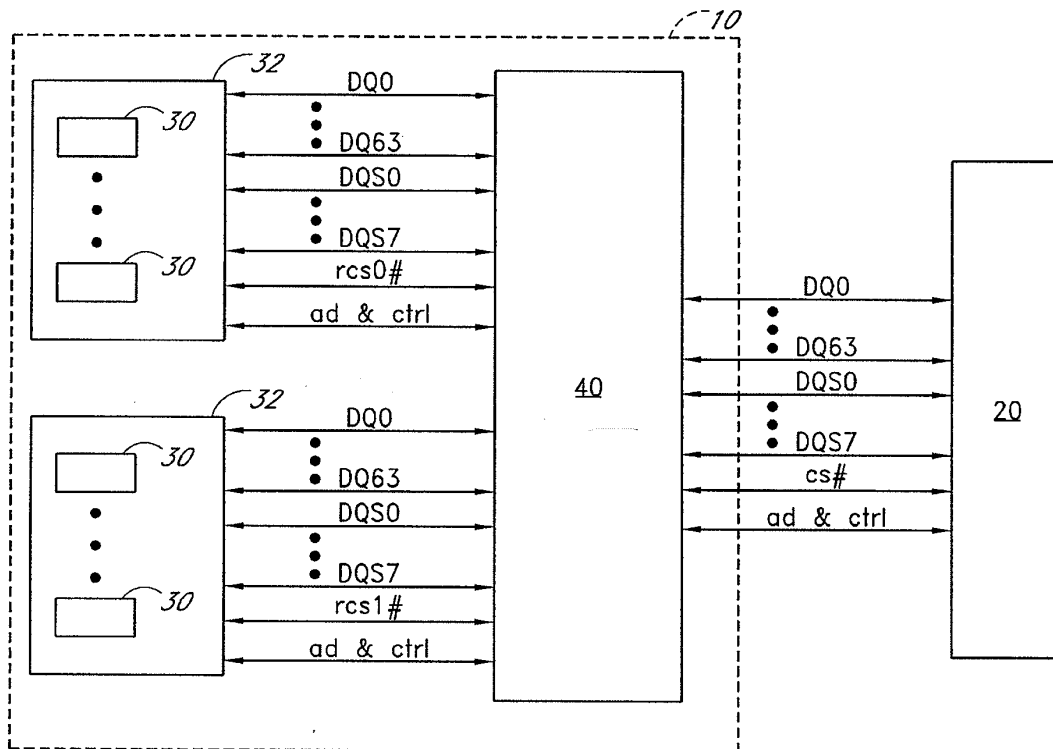
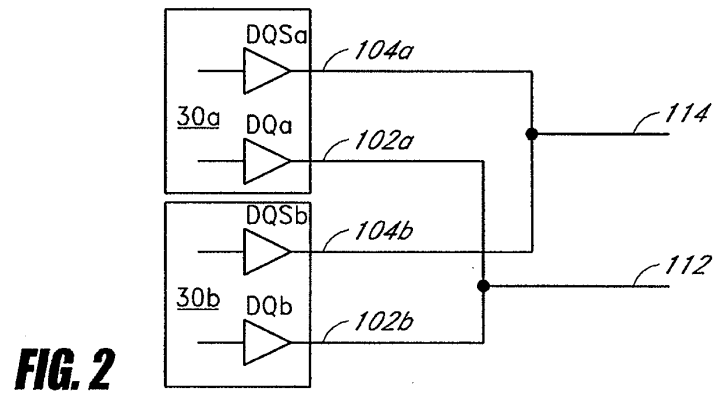
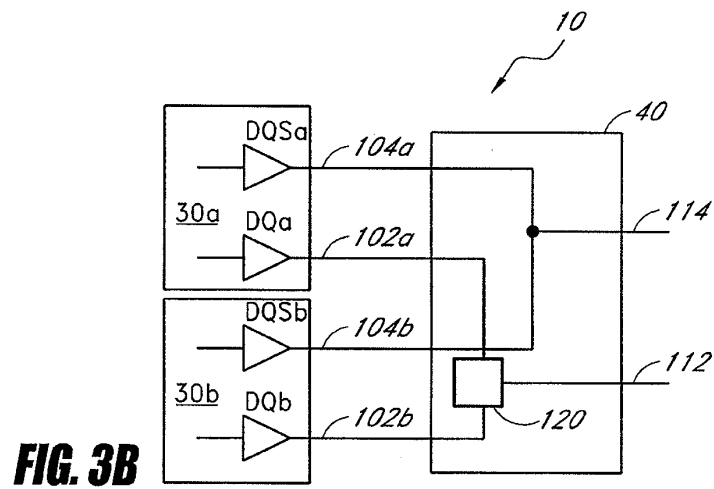
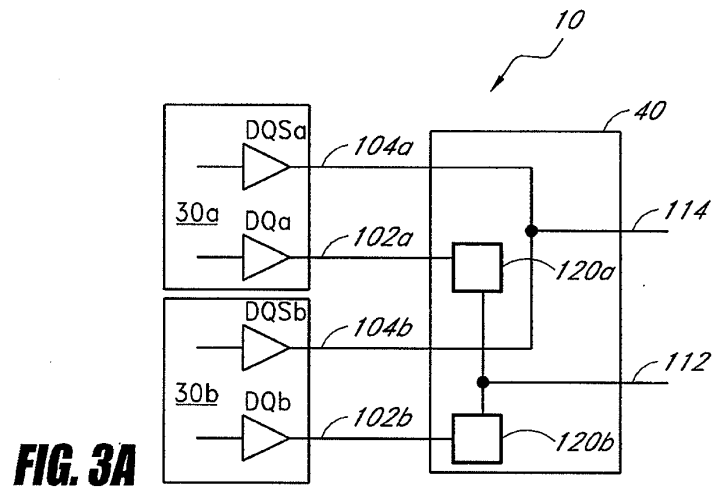
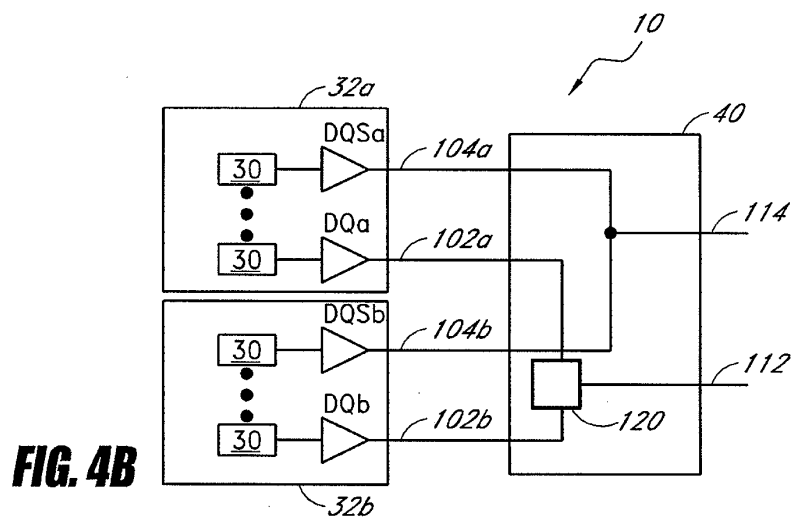
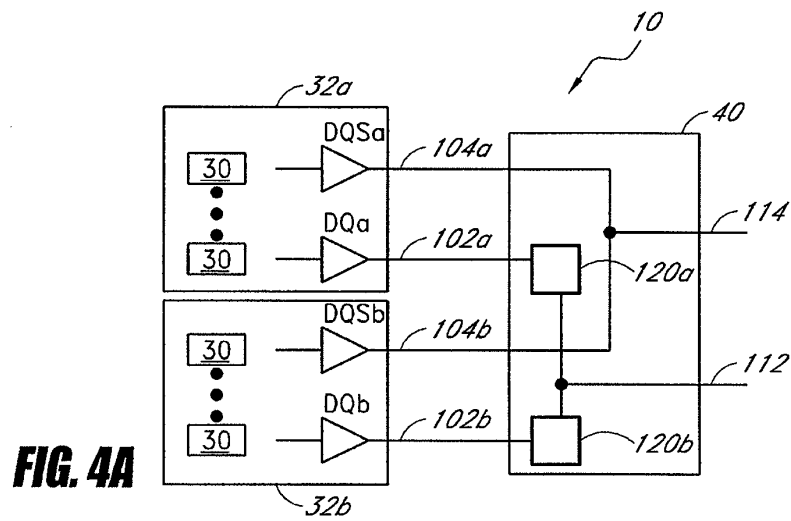
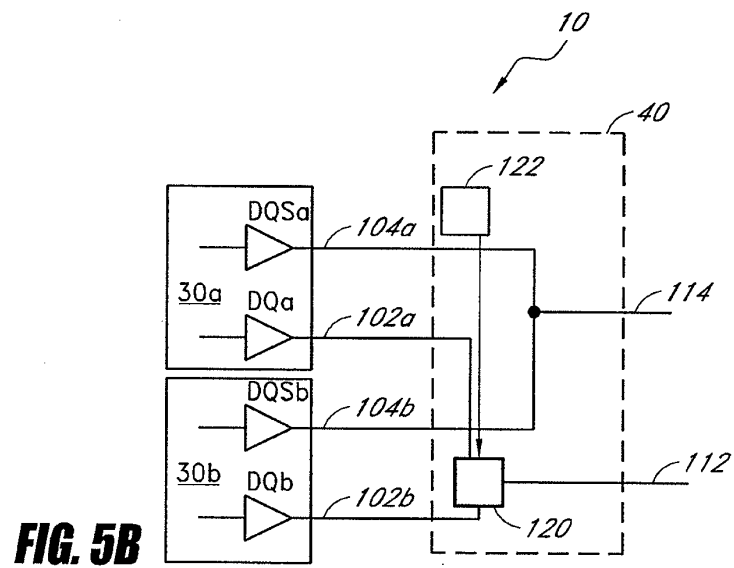
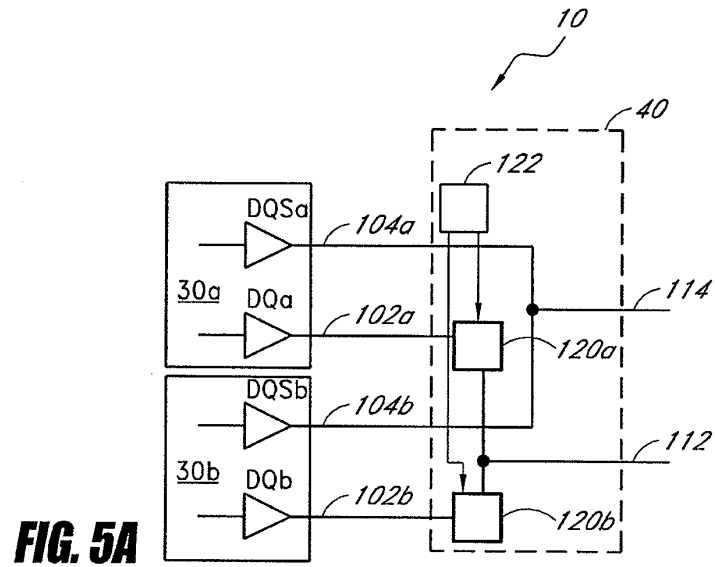


FIG. 1











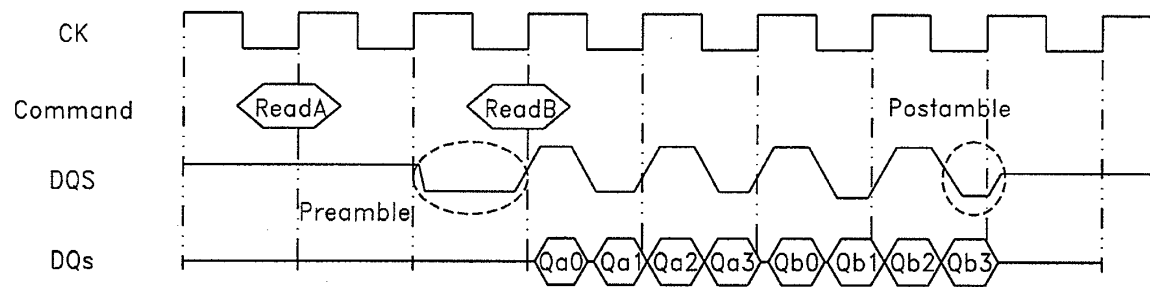


FIG. 6A

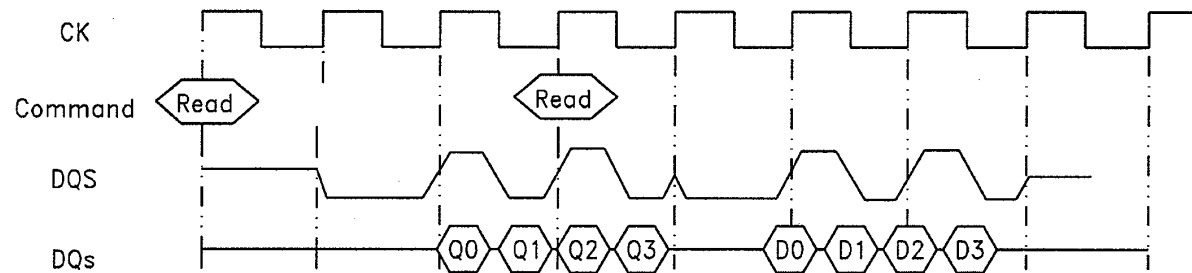
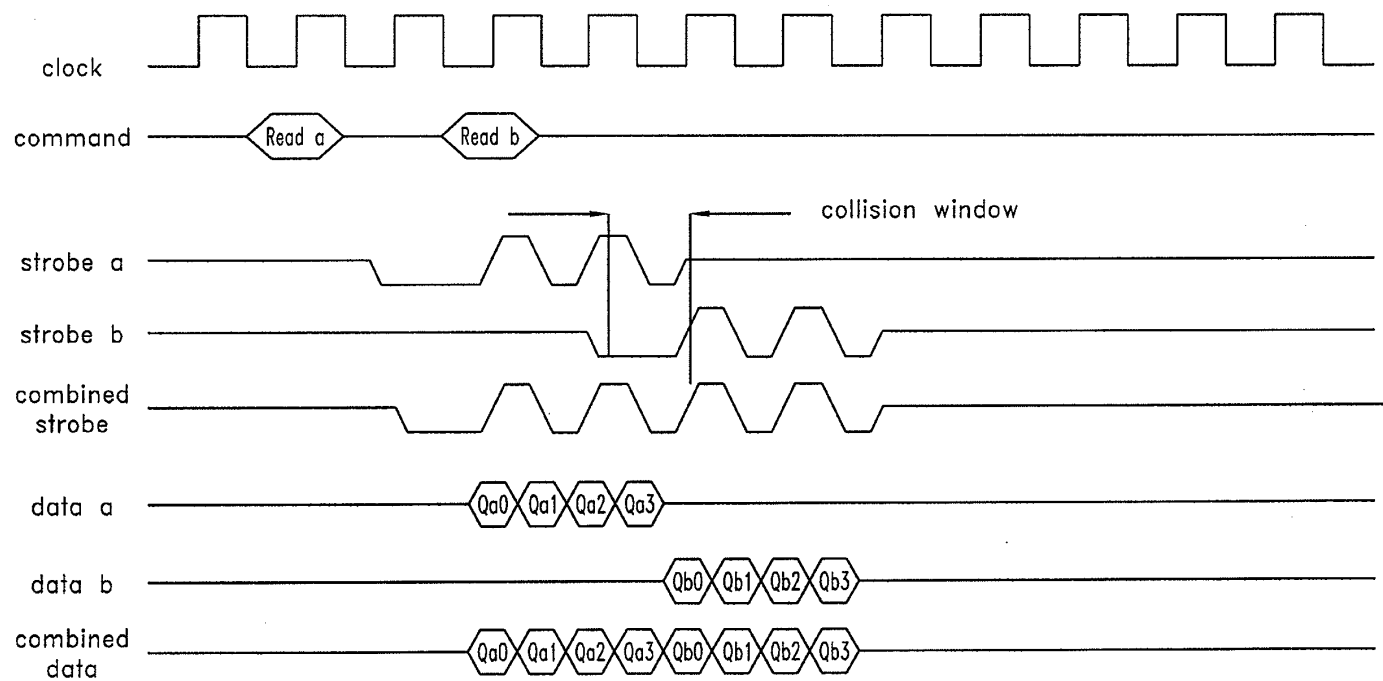


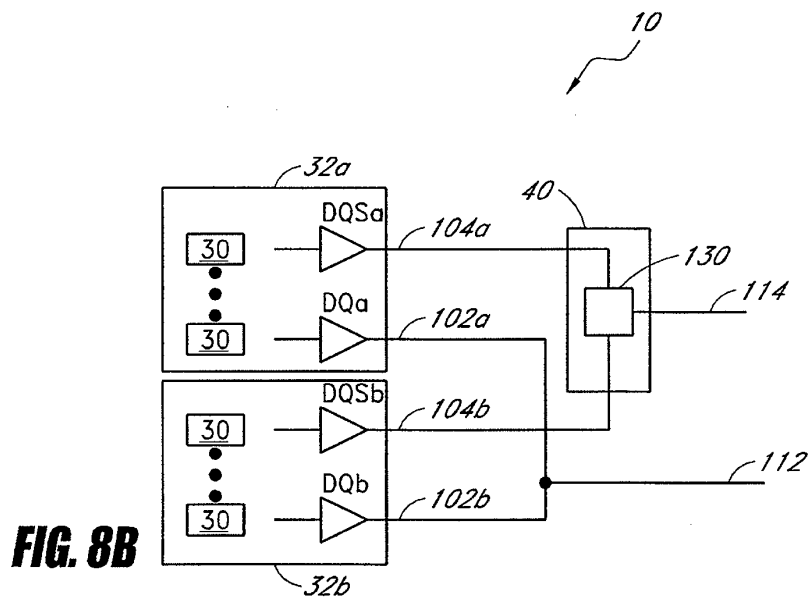
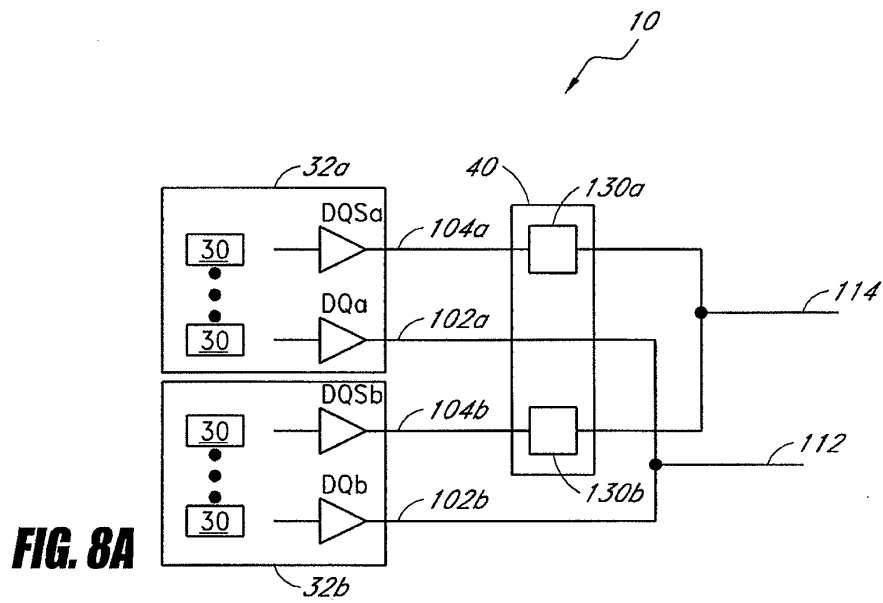
FIG. 6B

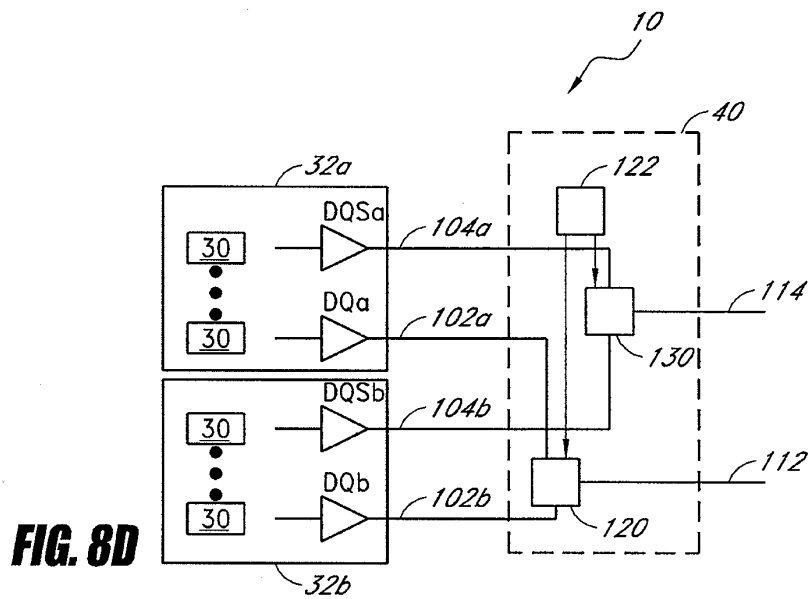
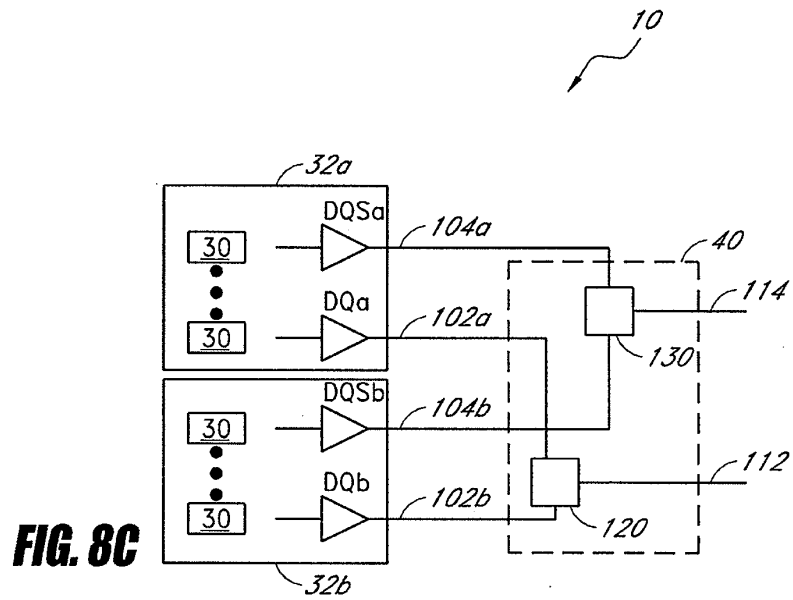
7/23



8/23

FIG. 7





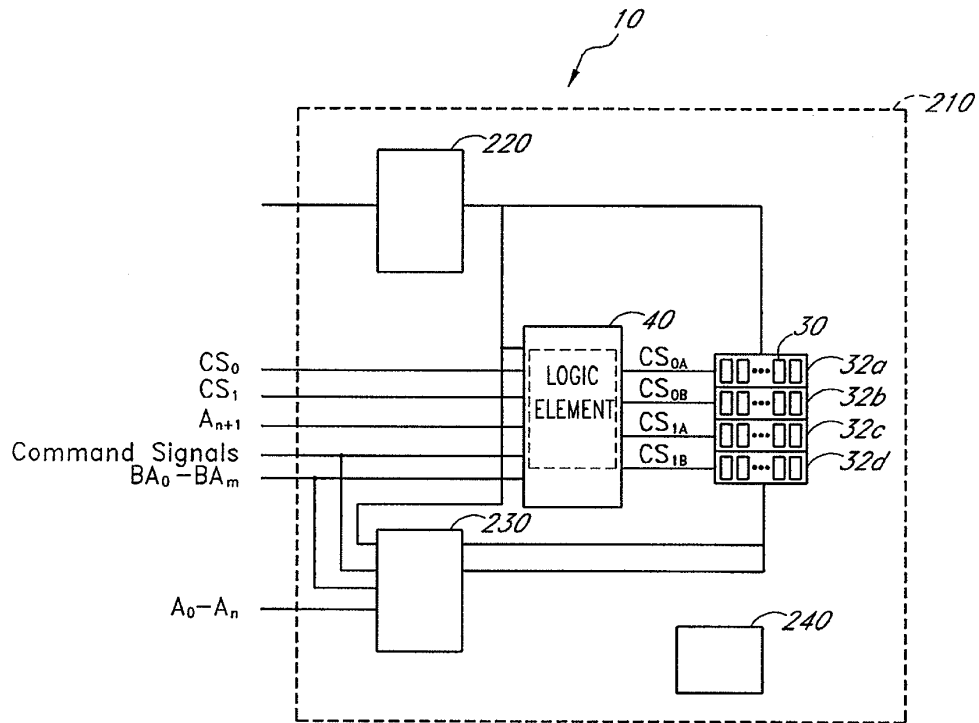


FIG. 9A

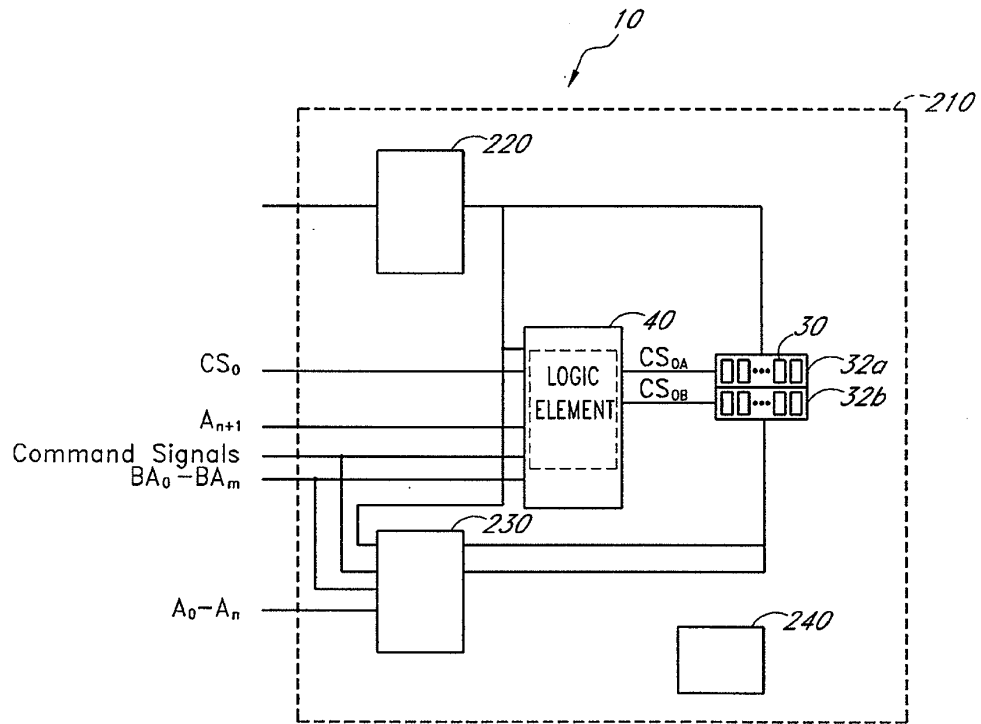
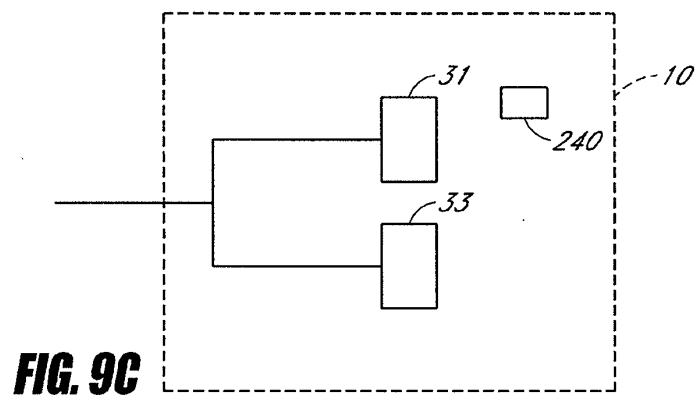


FIG. 9B



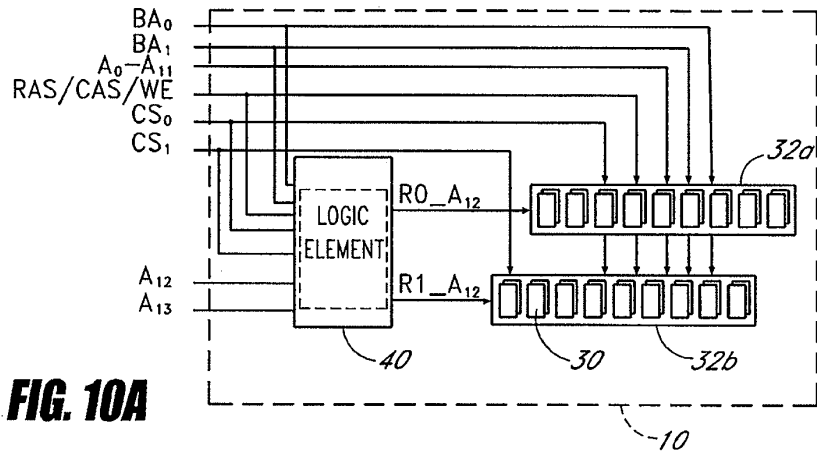


FIG. 10A

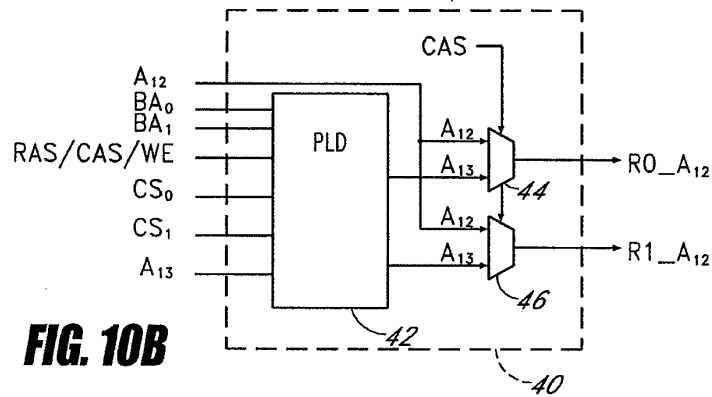


FIG. 10B

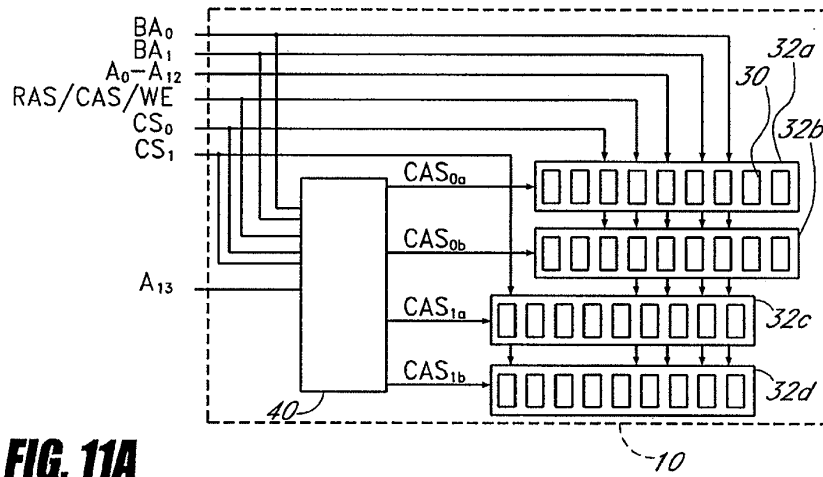


FIG. 11A

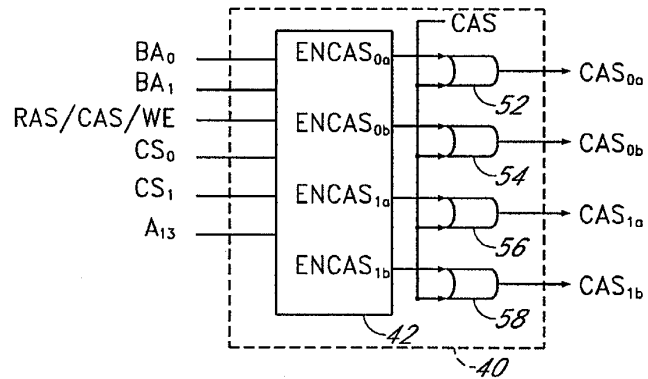
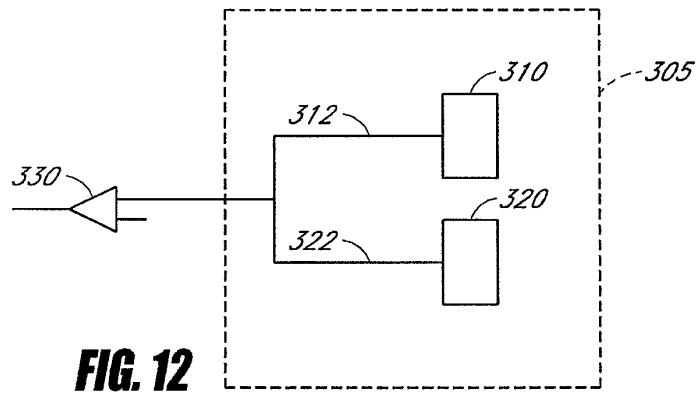


FIG. 11B



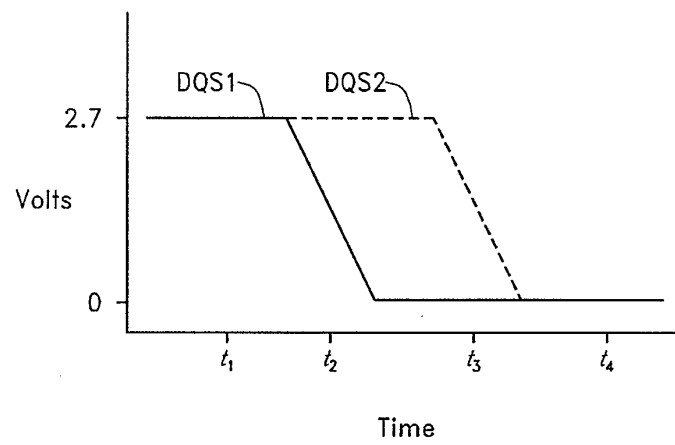
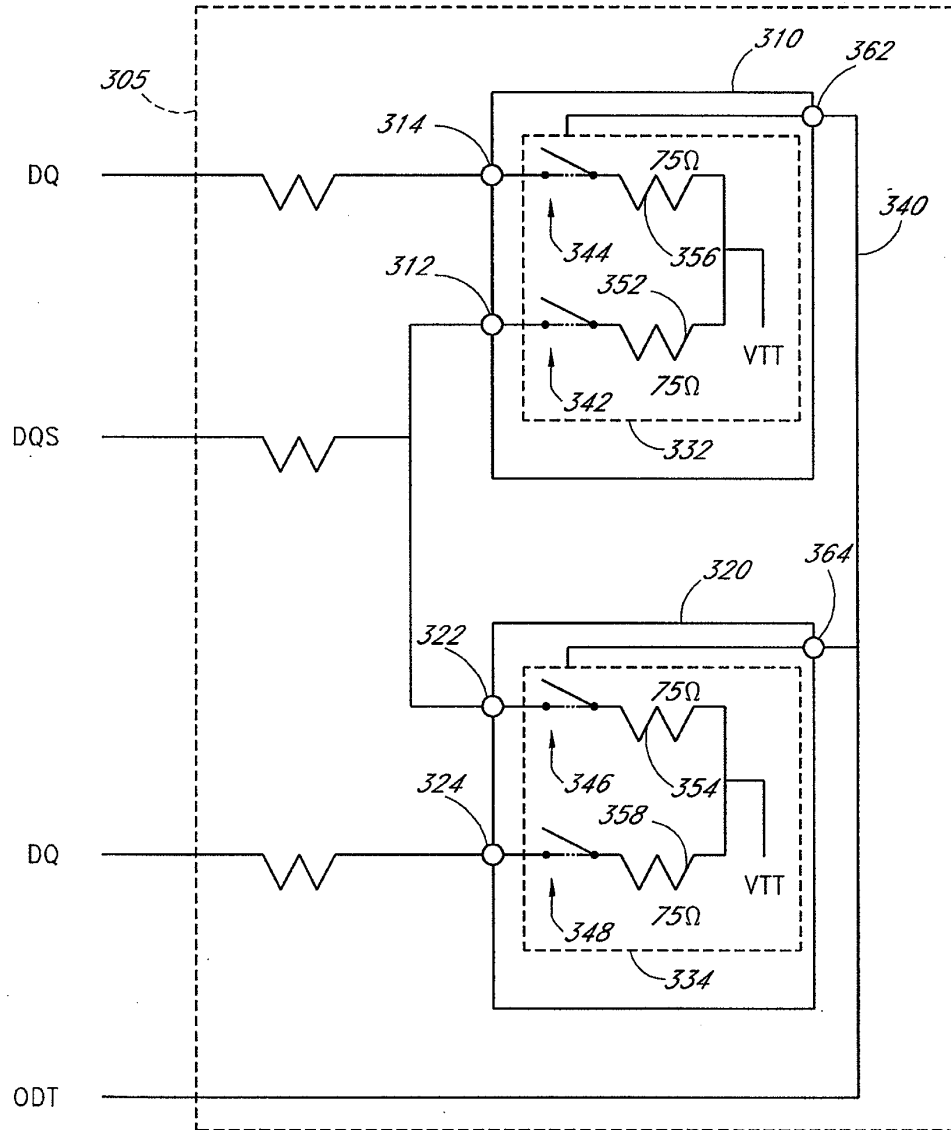


FIG. 13

**FIG. 14**

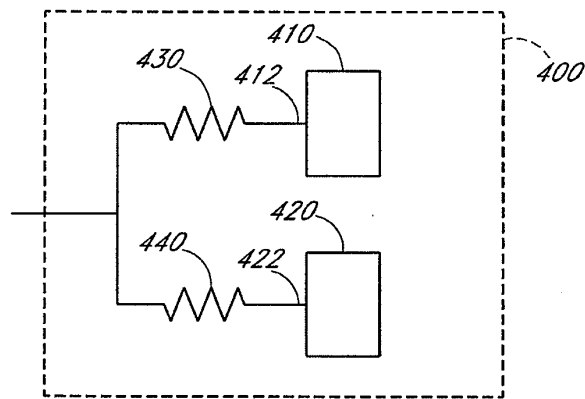


FIG. 15A

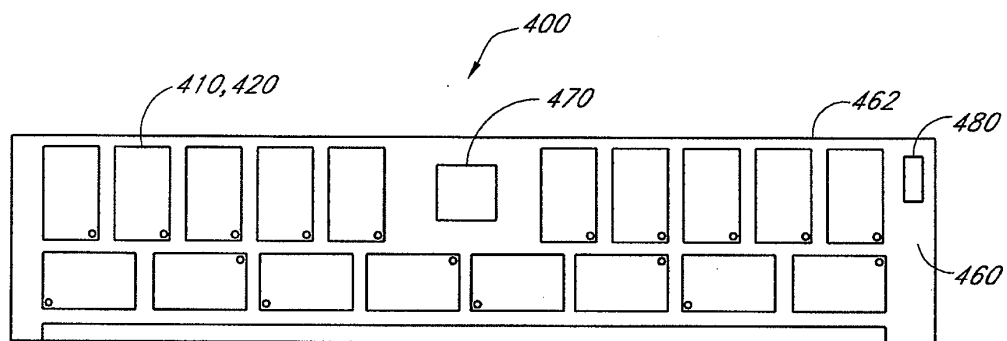


FIG. 16A

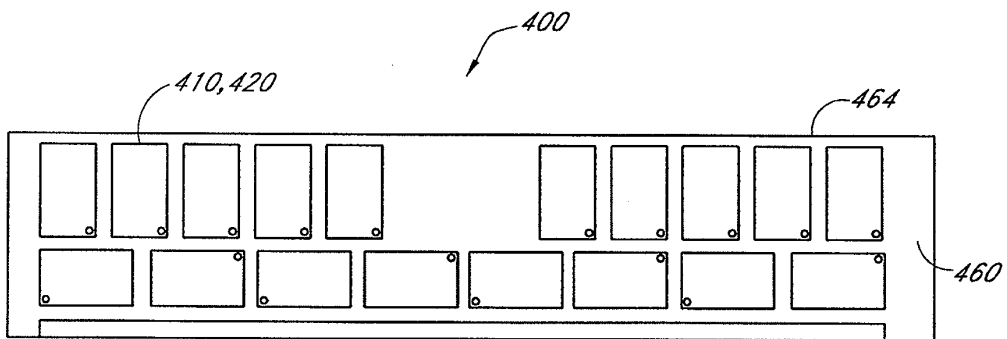


FIG. 16B

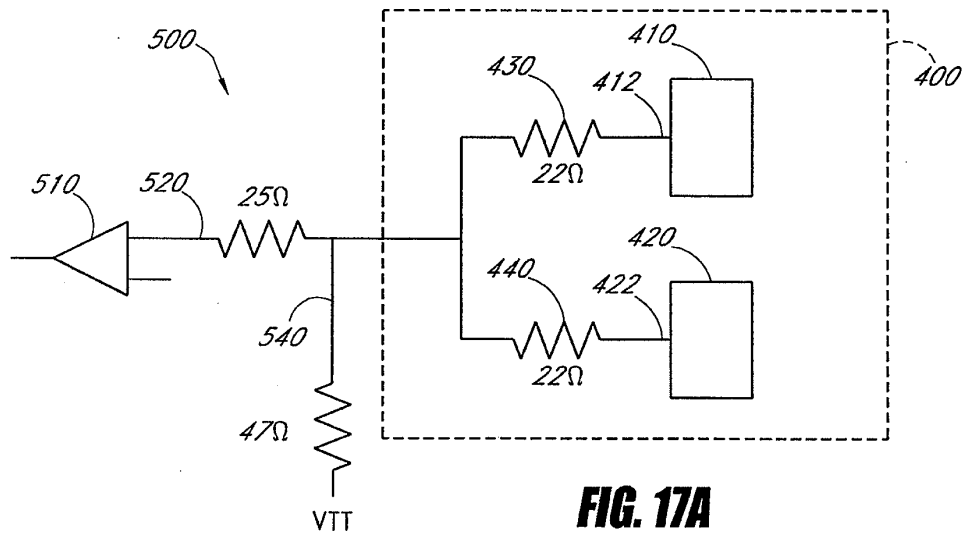


FIG. 17A

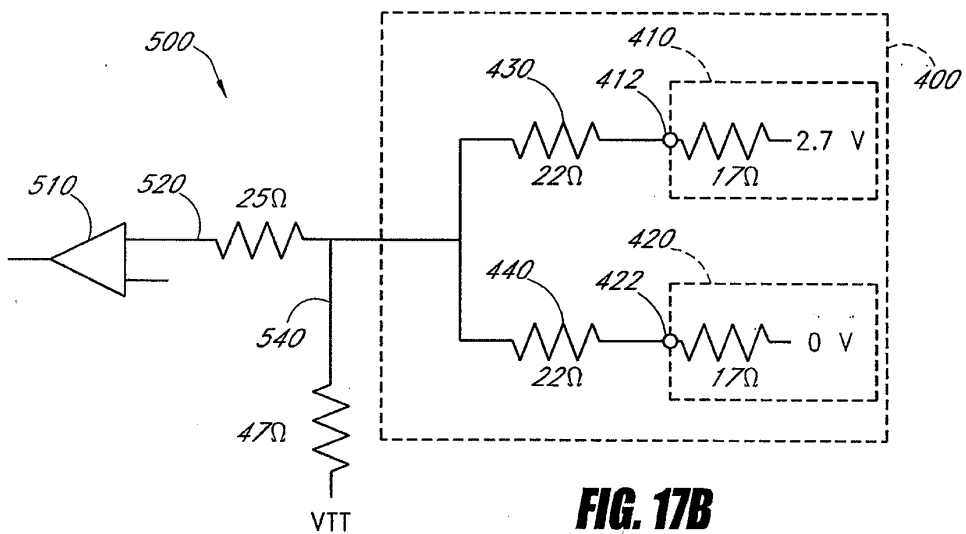


FIG. 17B

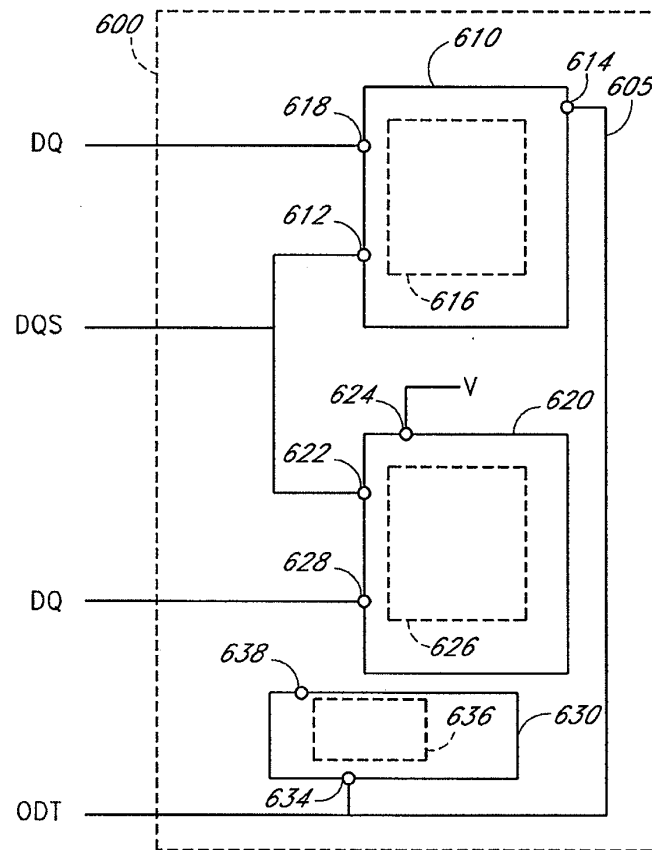
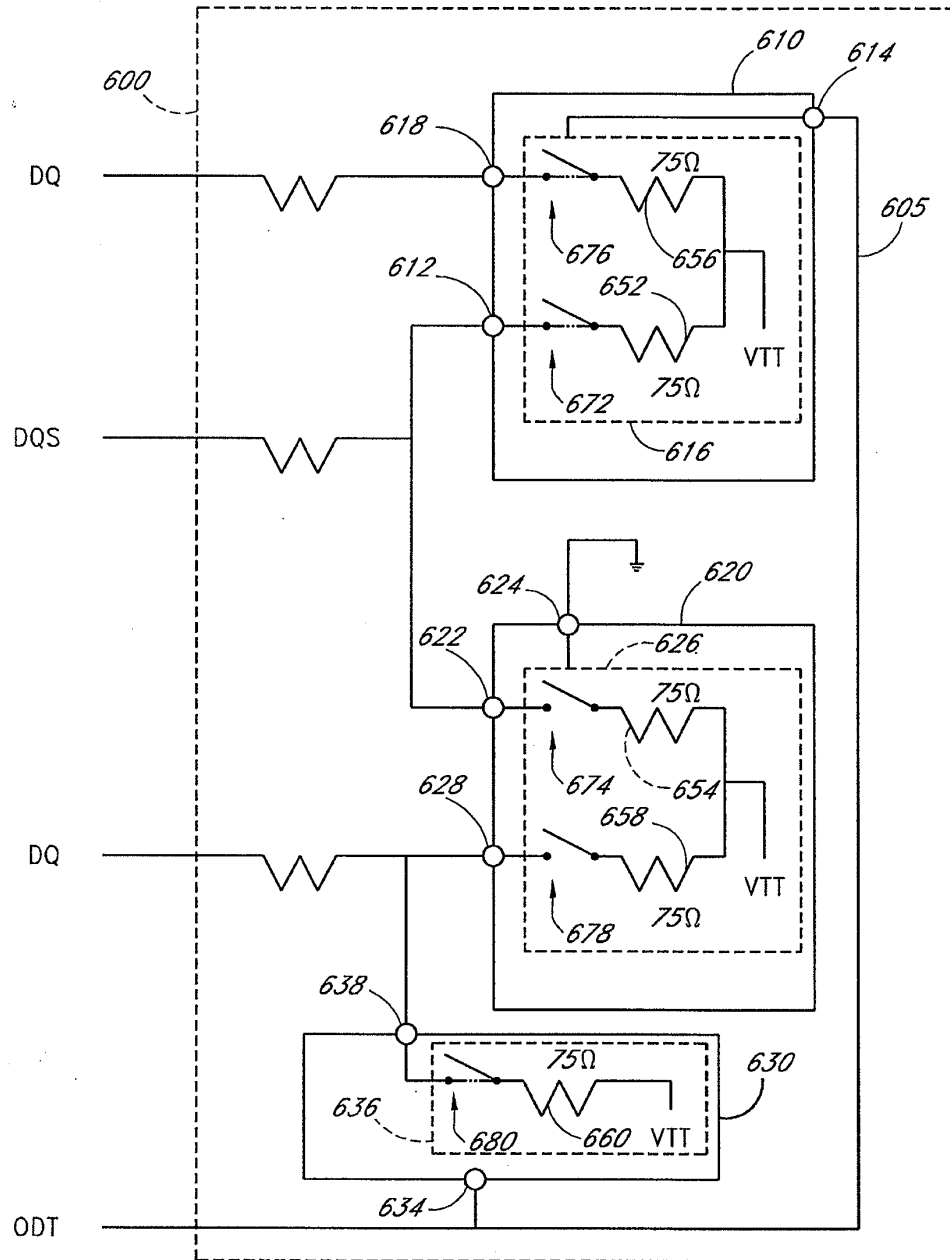


FIG. 18

**FIG. 19**

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Application Data Sheet 37 CFR 1.76		Attorney Docket Number	NETL.18CPCPCCC
		Application Number	
Title of Invention	CIRCUIT PROVIDING LOAD ISOLATION AND MEMORY DOMAIN TRANSLATION FOR MEMORY MODULE		
The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76. This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.			

Secrecy Order 37 CFR 5.2

☐	Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)
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Applicant Information:

Applicant 1					
Applicant Authority		☒ Inventor		☐ Legal Representative under 35 U.S.C. 117	
				☐ Party of Interest under 35 U.S.C. 118	
Prefix	Given Name	Middle Name	Family Name	Suffix	
	Jeffrey	C.	Solomon		
Residence Information (Select One) ☒ US Residency ☐ Non US Residency ☐ Active US Military Service					
City	Irvine	State/Province	CA	Country of Residence	US
Citizenship under 37 CFR 1.41(b)		US			
Mailing Address of Applicant:					
Address 1		16 Silver Fir			
Address 2					
City	Irvine	State/Province	CA		
Postal Code	92604	Country	US		
Applicant 2					
Applicant Authority		☒ Inventor		☐ Legal Representative under 35 U.S.C. 117	
				☐ Party of Interest under 35 U.S.C. 118	
Prefix	Given Name	Middle Name	Family Name	Suffix	
	Jayesh	R.	Bhakta		
Residence Information (Select One) ☒ US Residency ☐ Non US Residency ☐ Active US Military Service					
City	Cerritos	State/Province	CA	Country of Residence	US
Citizenship under 37 CFR 1.41(b)		US			
Mailing Address of Applicant:					
Address 1		12220 Rose Street			
Address 2					
City	Cerritos	State/Province	CA		
Postal Code	90703	Country	US		
All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the Add button.					
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Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below. For further information see 37 CFR 1.33(a).	
☐	An Address is being provided for the correspondence information of this application.

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Application Data Sheet 37 CFR 1.76		Attorney Docket Number	NETL.18CPCPCCC	
		Application Number		
Title of Invention	CIRCUIT PROVIDING LOAD ISOLATION AND MEMORY DOMAIN TRANSLATION FOR MEMORY MODULE			
Customer Number	20995			
Email Address	efiling@kmob.com		Add Email	Remove Email

Application Information:

Title of the Invention	CIRCUIT PROVIDING LOAD ISOLATION AND MEMORY DOMAIN TRANSLATION FOR MEMORY MODULE			
Attorney Docket Number	NETL.18CPCPCCC	Small Entity Status Claimed ☐		
Application Type	Nonprovisional			
Subject Matter	Utility			
Suggested Class (if any)		Sub Class (if any)		
Suggested Technology Center (if any)				
Total Number of Drawing Sheets (if any)	23	Suggested Figure for Publication (if any)		

Publication Information:

☐	Request Early Publication (Fee required at time of Request 37 CFR 1.219)
☐	Request Not to Publish. I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application has not and will not be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32). Enter either Customer Number or complete the Representative Name section below. If both sections are completed the Customer Number will be used for the Representative Information during processing.			
Please Select One:	☒ Customer Number	☐ US Patent Practitioner	☐ Limited Recognition (37 CFR 11.9)
Customer Number	20995		

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, or 365(c) or indicate National Stage entry from a PCT application. Providing this information in the application data sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78(a)(2) or CFR 1.78(a)(4), and need not otherwise be made part of the specification.			
Prior Application Status	Pending	Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
	Continuation of	12/629827	2009-12-02
Prior Application Status	Patented	Remove	

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	NETL.18CPCPCCC
		Application Number	
Title of Invention	CIRCUIT PROVIDING LOAD ISOLATION AND MEMORY DOMAIN TRANSLATION FOR MEMORY MODULE		

Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
12/629827	Continuation of	12/408652	2009-03-20	7636274	2009-12-22
Prior Application Status		Patented		Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
12/408652	Continuation of	11/335875	2006-01-19	7532537	2009-05-12
Prior Application Status		Expired		Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)		
11/335875	non provisional of	60/645087	2005-01-19		
Prior Application Status		Patented		Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
11/335875	Continuation in part of	11/173175	2005-07-01	7289386	2007-10-30
Prior Application Status		Expired		Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)		
11/173175	non provisional of	60/588244	2004-07-15		
Prior Application Status		Patented		Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
11/173175	Continuation in part of	11/075395	2005-03-07	7286436	2007-10-23
Prior Application Status		Expired		Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)		
11/075395	non provisional of	60/550668	2004-03-05		
Prior Application Status		Expired		Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)		
11/075395	non provisional of	60/575595	2004-05-28		
Prior Application Status		Expired		Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)		
11/075395	non provisional of	60/590038	2004-07-21		
Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the Add button.					

Foreign Priority Information:

This section allows for the applicant to claim benefit of foreign priority and to identify any prior foreign application for which priority is not claimed. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55(a).			
Remove			
Application Number	Country ¹	Parent Filing Date (YYYY-MM-DD)	Priority Claimed
			☐ Yes ☐ No

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	NETL.18CPCPCCC
		Application Number	
Title of Invention	CIRCUIT PROVIDING LOAD ISOLATION AND MEMORY DOMAIN TRANSLATION FOR MEMORY MODULE		

Additional Foreign Priority Data may be generated within this form by selecting the **Add** button.

Assignee Information:

Providing this information in the application data sheet does not substitute for compliance with any requirement of part 3 of Title 37 of the CFR to have an assignment recorded in the Office.

Assignee 1

If the Assignee is an Organization check here. ☒

Organization Name Netlist, Inc.

Mailing Address Information:

Address 1 51 Discovery #150

Address 2

City Irvine State/Province CA

Country US Postal Code 92618

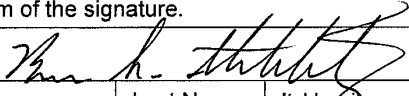
Phone Number Fax Number

Email Address

Additional Assignee Data may be generated within this form by selecting the **Add** button.

Signature:

A signature of the applicant or representative is required in accordance with 37 CFR 1.33 and 10.18. Please see 37 CFR 1.4(d) for the form of the signature.

Signature			Date (YYYY-MM-DD)	2010-11-29	
First Name	Bruce	Last Name	Itchkawitz	Registration Number	47677

This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Acknowledgement Receipt	
EFS ID:	8924349
Application Number:	12955711
International Application Number:	
Confirmation Number:	8026
Title of Invention:	CIRCUIT PROVIDING LOAD ISOLATION AND MEMORY DOMAIN TRANSLATION FOR MEMORY MODULE
First Named Inventor/Applicant Name:	Jeffrey C. Solomon
Customer Number:	20995
Filer:	Bruce S. Itchkawitz/Valerie Jones
Filer Authorized By:	Bruce S. Itchkawitz
Attorney Docket Number:	NETL.18CPCPCCC
Receipt Date:	29-NOV-2010
Filing Date:	
Time Stamp:	18:35:54
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Oath or Declaration filed	declaration.pdf	121328 b4676c2f230c5c54ee0491c2ce2ddf06245195e	no	2

Warnings:

Information:

2		specification.pdf	3393406 12649ebd37e24ad5c2625e0062f3899cf259523e	yes	61
	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Specification		1	52	
	Claims		53	60	
	Abstract		61	61	
Warnings:					
Information:					
3	Drawings-only black and white line drawings	drawings.pdf	675007 51f62eb2fd552b1637d21b4368cd301b25fb2510	no	23
Warnings:					
Information:					
4	Application Data Sheet	ads.pdf	317171 ef6ac95377de00dd9d09ec81a3731936e4a5368b0	no	5
Warnings:					
Information:					
This is not an USPTO supplied ADS fillable form					
Total Files Size (in bytes):			4506912		
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					



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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY. DOCKET NO.	TOT CLAIMS	IND CLAIMS
12/955,711	11/29/2010	2827	0.00	NETL.18CPCPCCC	40	3

CONFIRMATION NO. 8026

20995
KNOBBE MARTENS OLSON & BEAR LLP
2040 MAIN STREET
FOURTEENTH FLOOR
IRVINE, CA 92614

FILING RECEIPT



OC000000044902175

Date Mailed: 12/14/2010

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Applicant(s)

Jeffrey C. Solomon, Irvine, CA;
Jayesh R. Bhakta, Cerritos, CA;

Assignment For Published Patent Application

Netlist, Inc., Irvine, CA

Power of Attorney: None

Domestic Priority data as claimed by applicant

This application is a CON of 12/629,827 12/02/2009
which is a CON of 12/408,652 03/20/2009 PAT 7,636,274
which is a CON of 11/335,875 01/19/2006 PAT 7,532,537
which claims benefit of 60/645,087 01/19/2005
and is a CIP of 11/173,175 07/01/2005 PAT 7,289,386
which claims benefit of 60/588,244 07/15/2004
and is a CIP of 11/075,395 03/07/2005 PAT 7,286,436
which claims benefit of 60/550,668 03/05/2004
and claims benefit of 60/575,595 05/28/2004
and claims benefit of 60/590,038 07/21/2004

Foreign Applications

If Required, Foreign Filing License Granted: 12/10/2010

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 12/955,711**

Projected Publication Date: To Be Determined - pending completion of Missing Parts

page 1 of 3

Samsung Electronics Co., Ltd.

Ex. 1044, p. 94

Non-Publication Request: No

Early Publication Request: No

Title

CIRCUIT PROVIDING LOAD ISOLATION AND MEMORY DOMAIN TRANSLATION FOR MEMORY MODULE

Preliminary Class

365

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at <http://www.uspto.gov/web/offices/pac/doc/general/index.html>.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, <http://www.stopfakes.gov>. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4158).

LICENSE FOR FOREIGN FILING UNDER
Title 35, United States Code, Section 184
Title 37, Code of Federal Regulations, 5.11 & 5.15

GRANTED

The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where the conditions for issuance of a license have been met, regardless of whether or not a license may be required as set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign AssetsControl, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).



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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
12/955,711	11/29/2010	Jeffrey C. Solomon	NETL.18CPCPCCC

CONFIRMATION NO. 8026

FORMALITIES LETTER

20995
KNOBBE MARTENS OLSON & BEAR LLP
2040 MAIN STREET
FOURTEENTH FLOOR
IRVINE, CA 92614



OC000000044902176

Date Mailed: 12/14/2010

NOTICE TO FILE MISSING PARTS OF NONPROVISIONAL APPLICATION

FILED UNDER 37 CFR 1.53(b)

Filing Date Granted

Items Required To Avoid Abandonment:

An application number and filing date have been accorded to this application. The item(s) indicated below, however, are missing. Applicant is given **TWO MONTHS** from the date of this Notice within which to file all required items below to avoid abandonment. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a).

- The statutory basic filing fee is missing.
Applicant must submit \$330 to complete the basic filing fee for a non-small entity. If appropriate, applicant may make a written assertion of entitlement to small entity status and pay the small entity filing fee (37 CFR 1.27).

The applicant needs to satisfy supplemental fees problems indicated below.

The required item(s) identified below must be timely submitted to avoid abandonment:

- Additional claim fees of \$1040 as a non-small entity, including any required multiple dependent claim fee, are required. Applicant must submit the additional claim fees or cancel the additional claims for which fees are due.
- A surcharge (for late submission of filing fee, search fee, examination fee or oath or declaration) as set forth in 37 CFR 1.16(f) of \$130 for a non-small entity, must be submitted.

SUMMARY OF FEES DUE:

Total fee(s) required within **TWO MONTHS** from the date of this Notice is \$2260 for a non-small entity

- \$330 Statutory basic filing fee.
- \$130 Surcharge.
- The application search fee has not been paid. Applicant must submit \$540 to complete the search fee.
- The application examination fee has not been paid. Applicant must submit \$220 to complete the examination fee for a non-small entity.
- Total additional claim fee(s) for this application is \$1040
 - \$1040 for 20 total claims over 20.

Replies should be mailed to:

Mail Stop Missing Parts
Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

Registered users of EFS-Web may alternatively submit their reply to this notice via EFS-Web.

<https://sportal.uspto.gov/authenticate/AuthenticateUserLocalEPF.html>

For more information about EFS-Web please call the USPTO Electronic Business Center at **1-866-217-9197** or visit our website at <http://www.uspto.gov/ebc>.

If you are not using EFS-Web to submit your reply, you must include a copy of this notice.

/mkanno/

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875					Application or Docket Number 12/955,711	
APPLICATION AS FILED - PART I						
(Column 1)		(Column 2)		SMALL ENTITY		OR
FOR	NUMBER FILED	NUMBER EXTRA	RATE(\$)	FEE(\$)	OTHER THAN SMALL ENTITY	
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A		N/A	330
SEARCH FEE (37 CFR 1.16(k), (j), or (m))	N/A	N/A	N/A		N/A	540
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A		N/A	220
TOTAL CLAIMS (37 CFR 1.16(i))	40	minus 20 = *	20		x 52 =	1040
INDEPENDENT CLAIMS (37 CFR 1.16(h))	3	minus 3 = *			x 220 =	0.00
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$270 (\$135 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).					0.00
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))						0.00
* If the difference in column 1 is less than zero, enter "0" in column 2.				TOTAL		TOTAL 2130
APPLICATION AS AMENDED - PART II						
(Column 1)		(Column 2)		(Column 3)		SMALL ENTITY
AMENDMENT A	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE(\$)	ADDITIONAL FEE(\$)	OTHER THAN SMALL ENTITY
	Total (37 CFR 1.16(i))	*	Minus	**	=	RATE(\$)
	Independent (37 CFR 1.16(h))	*	Minus	***	=	ADDITIONAL FEE(\$)
	Application Size Fee (37 CFR 1.16(s))					x
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))					=
				TOTAL		TOTAL
				ADD'L FEE		ADD'L FEE
AMENDMENT B						
(Column 1)		(Column 2)		(Column 3)		SMALL ENTITY
AMENDMENT B	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE(\$)	ADDITIONAL FEE(\$)	OTHER THAN SMALL ENTITY
	Total (37 CFR 1.16(i))	*	Minus	**	=	RATE(\$)
	Independent (37 CFR 1.16(h))	*	Minus	***	=	ADDITIONAL FEE(\$)
	Application Size Fee (37 CFR 1.16(s))					x
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))					=
				TOTAL		TOTAL
				ADD'L FEE		ADD'L FEE
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3. ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20". *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3". The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.						

Please Direct All Correspondence to Customer Number 20995

RESPONSE TO FORMALITIES NOTICE

Applicant : Solomon et al.
App. No : 12/955,711
Filed : November 29, 2010
For : CIRCUIT PROVIDING LOAD
ISOLATION AND MEMORY
DOMAIN TRANSLATION FOR
MEMORY MODULE
Art Unit : 2827

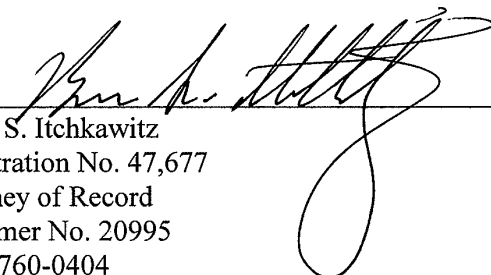
**Mail Stop Missing Parts
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450**

Dear Sir:

The above-captioned application was filed without filing fees.

- (X) Total fees of \$2,260 will be paid via EFS Web. Extension of time is requested by payment of any extension fee.

The Commissioner is hereby authorized to charge any additional fees which may be required, now or in the future, or credit any overpayment, to Account No. 11-1410.


Bruce S. Itchkawitz
Registration No. 47,677
Attorney of Record
Customer No. 20995
(949) 760-0404

10239742
010311

Electronic Patent Application Fee Transmittal				
Application Number:		12955711		
Filing Date:		29-Nov-2010		
Title of Invention:		CIRCUIT PROVIDING LOAD ISOLATION AND MEMORY DOMAIN TRANSLATION FOR MEMORY MODULE		
First Named Inventor/Applicant Name:		Jeffrey C. Solomon		
Filer:		Bruce S. Itchkawitz/Jessica Noda		
Attorney Docket Number:		NETL.18CPCPCCC		
Filed as Large Entity				
Utility under 35 USC 111(a) Filing Fees				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Utility application filing	1011	1	330	330
Utility Search Fee	1111	1	540	540
Utility Examination Fee	1311	1	220	220
Pages:				
Claims:				
Claims in excess of 20	1202	20	52	1040
Miscellaneous-Filing:				
Late filing fee for oath or declaration	1051	1	130	130

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				2260

Electronic Acknowledgement Receipt	
EFS ID:	9153736
Application Number:	12955711
International Application Number:	
Confirmation Number:	8026
Title of Invention:	CIRCUIT PROVIDING LOAD ISOLATION AND MEMORY DOMAIN TRANSLATION FOR MEMORY MODULE
First Named Inventor/Applicant Name:	Jeffrey C. Solomon
Customer Number:	20995
Filer:	Bruce S. Itchkawitz/Shirley Martinez
Filer Authorized By:	Bruce S. Itchkawitz
Attorney Docket Number:	NETL.18CPCPCCC
Receipt Date:	03-JAN-2011
Filing Date:	29-NOV-2010
Time Stamp:	17:54:32
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	\$2260
RAM confirmation Number	3921
Deposit Account	111410
Authorized User	KNOBBE MARTENS OLSON AND BEAR
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees) Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)	

File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Applicant Response to Pre-Exam Formalities Notice	mparts.pdf	31179	no	1
			0152597c90a4d2880d530fbdee5e4a00d502d337		
Warnings:					
Information:					
2	Fee Worksheet (PTO-875)	fee-info.pdf	38660	no	2
			cca92290a01fad8231255dc0aac943fe29c90ea9		
Warnings:					
Information:					
Total Files Size (in bytes):			69839		
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					



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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY. DOCKET NO.	TOT CLAIMS	IND CLAIMS
12/955,711	11/29/2010	2827	2260	NETL.18CPCPCCC	40	3

CONFIRMATION NO. 8026

UPDATED FILING RECEIPT



OC000000045272554

20995
KNOBBE MARTENS OLSON & BEAR LLP
2040 MAIN STREET
FOURTEENTH FLOOR
IRVINE, CA 92614

Date Mailed: 01/05/2011

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Applicant(s)

Jeffrey C. Solomon, Irvine, CA;
Jayesh R. Bhakta, Cerritos, CA;

Assignment For Published Patent Application

Netlist, Inc., Irvine, CA

Power of Attorney: None

Domestic Priority data as claimed by applicant

This application is a CON of 12/629,827 12/02/2009
which is a CON of 12/408,652 03/20/2009 PAT 7,636,274
which is a CON of 11/335,875 01/19/2006 PAT 7,532,537
which claims benefit of 60/645,087 01/19/2005
and is a CIP of 11/173,175 07/01/2005 PAT 7,289,386
which claims benefit of 60/588,244 07/15/2004
and is a CIP of 11/075,395 03/07/2005 PAT 7,286,436
which claims benefit of 60/550,668 03/05/2004
and claims benefit of 60/575,595 05/28/2004
and claims benefit of 60/590,038 07/21/2004

Foreign Applications

If Required, Foreign Filing License Granted: 12/10/2010

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 12/955,711**

Projected Publication Date: 04/14/2011

Non-Publication Request: No

Early Publication Request: No

Title

CIRCUIT PROVIDING LOAD ISOLATION AND MEMORY DOMAIN TRANSLATION FOR MEMORY MODULE

Preliminary Class

365

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Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at <http://www.uspto.gov/web/offices/pac/doc/general/index.html>.

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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875						Application or Docket Number 12/955,711				
APPLICATION AS FILED - PART I										
(Column 1)		(Column 2)		SMALL ENTITY		OTHER THAN SMALL ENTITY				
FOR	NUMBER FILED	NUMBER EXTRA	RATE(\$)	FEE(\$)		RATE(\$)	FEE(\$)			
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	330			
SEARCH FEE (37 CFR 1.16(k), (j), or (m))	N/A	N/A	N/A			N/A	540			
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	220			
TOTAL CLAIMS (37 CFR 1.16(i))	40	minus 20 = 20				x 52 =	1040			
INDEPENDENT CLAIMS (37 CFR 1.16(h))	3	minus 3 = *				x 220 =	0.00			
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$270 (\$135 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00			
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00			
* If the difference in column 1 is less than zero, enter "0" in column 2.				TOTAL		TOTAL	2130			
APPLICATION AS AMENDED - PART II										
(Column 1)		(Column 2)		(Column 3)		SMALL ENTITY		OTHER THAN SMALL ENTITY		
AMENDMENT A		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE(\$)	ADDITIONAL FEE(\$)		RATE(\$)	ADDITIONAL FEE(\$)
	Total (37 CFR 1.16(i))	*	Minus	**	=	x	=		x	=
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x	=		x	=
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))									
TOTAL ADD'L FEE									TOTAL ADD'L FEE	
AMENDMENT B		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE(\$)	ADDITIONAL FEE(\$)		RATE(\$)	ADDITIONAL FEE(\$)
	Total (37 CFR 1.16(i))	*	Minus	**	=	x	=		x	=
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x	=		x	=
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))									
TOTAL ADD'L FEE									TOTAL ADD'L FEE	
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3. ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20". *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3". The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.										

INFORMATION DISCLOSURE STATEMENT BY APPLICANT	Application No.	12/955,711
	Filing Date	November 29, 2010
	First Named Inventor	Solomon et al.
	Art Unit	2824
(Multiple sheets used when necessary)	Examiner	Sofocleous, Alexander
SHEET 1 OF 14	Attorney Docket No.	NETL.18CPCPCCC

U.S. PATENT DOCUMENTS					
Examiner Initials	Cite No.	Document Number Number - Kind Code (if known) Example: 1,234,567 B1	Publication Date MM-DD-YYYY	Name of Patentee or Applicant	Pages, Columns, Lines Where Relevant Passages or Relevant Figures Appear
	1	4,368,515	1/11/1983	Nielsen	
	2	4,392,212	7/5/1983	Miyasaka et al.	
	3	4,633,429	12/30/1986	Lewandowski et al.	
	4	4,670,748	6/2/1987	Williams	
	5	4,866,603	9/1989	Chiba	
	6	4,958,322	9/18/1990	Kosugi et al.	
	7	4,961,172	10/2/1990	Shubat et al.	
	8	4,980,850	12/25/1990	Morgan	
	9	5,247,643	9/21/1993	Shottan	
	10	5,345,412	9/6/1994	Shiratsuchi	
	11	5,426,753	6/20/1995	Moon	
	12	5,483,497	1/9/1996	Mochizuki et al.	
	13	5,495,435	2/1/1996	Sugahara	
	14	5,581,498	12/3/1996	Ludwig et al.	
	15	5,590,071	12/31/1996	Kolor et al.	
	16	5,699,542	12/16/1997	Mehta et al.	
	17	5,702,984	12/30/1997	Bertin et al.	
	18	5,703,826	12/30/1997	Hush et al.	
	19	5,745,914	4/28/1998	Connolly et al.	
	20	5,802,395	9/1/1998	Connolly et al.	
	21	5,805,520	9/8/1998	Anglada et al.	
	22	5,822,251	10/13/1998	Bruce et al.	
	23	5,926,827	7/20/1999	Dell et al.	
	24	5,959,930	9/28/1999	Sakurai	
	25	5,963,464	10/5/1999	Dell et al.	
	26	5,966,736	10/12/1999	Gittinger et al.	
	27	6,018,787	1/25/2000	Ip	
	28	6,044,032	3/28/2000	Li	
	29	6,070,217	5/30/2000	Connolly et al.	

Examiner Signature	Date Considered
*Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.	

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	First Named Inventor	Solomon et al.
	Art Unit	2824
(Multiple sheets used when necessary)	Examiner	Sofocleous, Alexander
SHEET 2 OF 14	Attorney Docket No.	NETL.18CPCPCCC

U.S. PATENT DOCUMENTS					
Examiner Initials	Cite No.	Document Number Number - Kind Code (if known) Example: 1,234,567 B1	Publication Date MM-DD-YYYY	Name of Patentee or Applicant	Pages, Columns, Lines Where Relevant Passages or Relevant Figures Appear
	30	6,070,227	5/30/2000	Rokicki	
	31	6,097,652	8/1/2000	Roh	
	32	6,108,745	8/22/2000	Gupta et al.	
	33	6,134,638	10/17/2000	Olarig, et al.	
	34	6,151,271	11/17/2000	Lee	
	35	6,154,418	11/28/2000	Li	
	36	6,154,419	11/28/2000	Shakkarwar	
	37	6,185,654	2/6/2001	Van Doren	
	38	6,209,074	3/27/2001	Dell et al.	
	39	6,226,709	5/1/2001	Goodwin et al.	
	40	6,233,650	5/1/2001	Johnson et al.	
	41	6,226,736	5/1/2001	Niot	
	42	6,247,088	6/12/2001	Seo et al.	
	43	6,317,352	11/13/2001	Halbert et al.	
	44	6,400,637	6/4/2002	Akamatsu et al.	
	45	6,408,356	6/18/2002	Dell	
	46	6,414,868	7/2/2002	Wong et al.	
	47	6,415,374	7/2/2002	Faue et al.	
	48	6,438,062	8/2002	Curtis et al.	
	49	6,446,184	9/2002	Dell et al.	
	50	6,446,158	9/2002	Karabatsos	
	51	6,453,381	9/17/2002	Yuan et al.	
	52	6,470,417	10/22/2002	Kolor et al.	
	53	6,502,161	12/31/2002	Perego et al.	
	54	6,518,794	2/11/2003	Coteus et al.	
	55	6,526,473	2/25/2003	Kim	
	56	6,530,007	3/4/2003	Olarig et al.	
	57	6,530,033	3/2003	Raynham et al.	
	58	6,553,450	4/22/2003	Dodd et al.	

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	First Named Inventor	Solomon et al.
	Art Unit	2824
	Examiner	Sofocleous, Alexander
SHEET 3 OF 14	Attorney Docket No.	NETL.18CPCPCCC

U.S. PATENT DOCUMENTS					
Examiner Initials	Cite No.	Document Number Number - Kind Code (if known) Example: 1,234,567 B1	Publication Date MM-DD-YYYY	Name of Patentee or Applicant	Pages, Columns, Lines Where Relevant Passages or Relevant Figures Appear
	59	6,618,320	9/9/2003	Hasegawa et al.	
	60	6,621,496	9/16/2003	Ryan	
	61	6,625,081	9/23/2003	Roohparvar et al.	
	62	6,625,687	9/23/2003	Halbert et al.	
	63	6,636,935	10/21/2003	Ware et al.	
	64	6,646,949	11/11/2003	Ellis et al.	
	65	6,658,509	12/2/2003	Bonella et al.	
	66	6,674,684	1/6/2004	Shen	
	67	6,681,301	1/20/2004	Mehta et al.	
	68	6,683,372	1/27/2004	Wong et al.	
	69	6,705,877	3/1/2004	Li et al.	
	70	6,697,888	2/24/2004	Halbert et al.	
	71	6,717,855	4/6/2004	Lai	
	72	6,738,880	5/18/2004	Lai et al.	
	73	6,742,098	5/25/2004	Halbert et al.	
	74	6,754,797	6/22/2004	Wu et al.	
	75	6,785,189	8/31/2004	Jacobs et al.	
	76	6,788,592	9/7/2004	Nakata et al.	
	77	6,807,125	10/19/2004	Coteus et al.	
	78	6,813,196	11/2/2004	Park et al.	
	79	6,834,014	12/21/2004	Yoo et al.	
	80	6,854,042	2/8/2005	Karabatsos	
	81	6,880,094	4/12/2005	LaBerge	
	82	6,889,304	5/3/2005	Perego et al.	
	83	6,912,615	6/28/2005	Nicolai	
	84	6,912,628	6/28/2005	Wicki et al.	
	85	6,925,028	8/2/2005	Hosokawa et al.	
	86	6,944,694	9/13/2005	Pax	
	87	6,950,366	9/27/2005	Lapidus et al.	

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	First Named Inventor	Solomon et al.
	Art Unit	2824
	Examiner	Sofocleous, Alexander
SHEET 4 OF 14	Attorney Docket No.	NETL.18CPCPCCC

U.S. PATENT DOCUMENTS					
Examiner Initials	Cite No.	Document Number Number - Kind Code (if known) Example: 1,234,567 B1	Publication Date MM-DD-YYYY	Name of Patentee or Applicant	Pages, Columns, Lines Where Relevant Passages or Relevant Figures Appear
	88	6,961,281	11/1/2005	Wong et al.	
	89	6,981,089	12/27/2005	Dodd et al.	
	90	6,982,892	1/3/2006	Lee et al.	
	91	6,982,893	1/3/2006	Jakobs	
	92	6,990,043	1/24/2006	Kuroda et al.	
	93	6,996,686	2/7/2006	Doblar et al.	
	94	7,007,130	2/28/2006	Holman	
	95	7,046,538	5/1/2006	Kinsley et al.	
	96	7,007,175	2/28/2006	Chang et al.	
	97	7,054,179	5/30/2006	Cogdill et al.	
	98	7,065,626	6/20/2006	Schumacher et al.	
	99	7,073,041	7/4/2006	Dwyer et al.	
	100	7,120,727	10/10/2006	Lee et al.	
	101	7,124,260	10/17/2006	LaBerge et al.	
	102	7,127,584	10/24/2006	Thompson et al.	
	103	7,130,952	10/31/2006	Nanki et al.	
	104	7,133,960	11/7/2006	Thompson et al.	
	105	7,133,972	11/7/2006	Jeddeloh	
	106	7,142,461	11/28/2006	Janzen	
	107	7,167,967	1/1/2007	Bungo et al.	
	108	7,149,841	12/12/2006	LaBerge	
	109	7,181,591	2/20/2007	Tsai	
	110	7,200,021	4/3/2007	Raghuram	
	111	7,227,910	6/5/2007	Lipka	
	112	7,266,639	9/4/2007	Raghuram	
	113	7,272,709	9/18/2007	Zitlaw et al.	
	114	7,281,079	10/9/2007	Bains et al.	
	115	7,286,436	10/23/2007	Bhakta et al.	
	116	7,289,386	10/30/2007	Bhakta et al.	

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U.S. PATENT DOCUMENTS					
Examiner Initials	Cite No.	Document Number Number - Kind Code (if known) Example: 1,234,567 B1	Publication Date MM-DD-YYYY	Name of Patentee or Applicant	Pages, Columns, Lines Where Relevant Passages or Relevant Figures Appear
	117	7,346,750	3/18/2008	Ishikawa	
	118	7,356,639	12/23/2004	Perego et al.	
	119	7,370,238	5/6/2008	Billick et al.	
	120	7,437,591	10/14/2008	Wong	
	121	7,471,538	12/1/2008	Hofstra	
	122	7,461,182	12/2/2008	Fukushima et al.	
	123	7,532,537	5/12/2009	Solomon et al.	
	124	7,619,912	11/17/2009	Bhakta et al.	
	125	7,636,274	12/22/2009	Solomon et al.	
	126	7,864,627	1/4/2011	Bhakta et al.	
	127	7,881,150	2/1/2011	Solomon et al.	
	128	RE 36229	6/15/1999	Cady	
	129	US 2001/0003198 A1	6/7/2001	Wu	
	130	US 2001/0052057	12/13/2001	Lai	
	131	US 2002/0088633	7/11/2002	Kong et al.	
	132	US 2003/0063514	4/3/2003	Faue	
	133	US 2003/0090359	5/2003	Ok, Seung Han	
	134	US 2003/0090879	5/15/2003	Doblar et al.	
	135	US 2003/0191995	10/9/2003	Abrosimov et al.	
	136	US 2003/0210575	11/13/2003	Seo et al.	
	137	US 2004/0000708	1/1/2004	Rapport et al.	
	138	US 2004/0037158	2/26/2004	Coteus et al.	
	139	US 2004/0201968	10/14/2004	Tafolla	
	140	US 2005/0036378	2/17/2005	Kawaguchi et al.	
	141	US 2005/0281096	12/22/2005	Bhakta et al.	
	142	US 2006/0044860	3/2/2006	Kinsley et al.	
	143	US 2006/0117152 A1	6/1/2006	Amidi	
	144	US 2006/0126369	6/15/2006	Raghuram	
	145	US 2006/0129755	6/15/2006	Raghuram	

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*Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.	

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	First Named Inventor	Solomon et al.
	Art Unit	2824
(Multiple sheets used when necessary)	Examiner	Sofocleous, Alexander
SHEET 6 OF 14	Attorney Docket No.	NETL.18CPCPCCC

U.S. PATENT DOCUMENTS					
Examiner Initials	Cite No.	Document Number Number - Kind Code (if known) Example: 1,234,567 B1	Publication Date MM-DD-YYYY	Name of Patentee or Applicant	Pages, Columns, Lines Where Relevant Passages or Relevant Figures Appear
	146	US 2006/0179206	8/10/2006	Brittain et al.	
	147	US 2006/0259711	11/2006	Oh, Jong-Hoon	
	148	US 2006/0267172	11/30/2006	Nguyen et al.	
	149	US 2006/0277355	12/1/2006	Ellsbury et al.	
	150	US 2010/0128507	5/1/2010	Solomon et al.	
	151	Application Number 12/504,131; filed 07/16/2009; Owned by Netlist, Inc.			
	152	Application Number 12/761,179; filed 04/15/2010; Owned by Netlist, Inc.			
	153	Application Number 12/815,339; filed 06/14/2010; Owned by Netlist, Inc.			
	154	Application Number 12/774,632; filed 05/05/2010; Owned by Netlist, Inc.			
	155	Application Number 12/422,925; filed 04/13/2009; Owned by Netlist, Inc.			
	156	Application Number 12/422,853; filed 04/13/2009; Owned by Netlist, Inc.			
	157	Application Number 12/954,492; filed 11/24/10; Owned by Netlist, Inc.			
	158	Application Number 12/981,380; filed 11/29/10; Owned by Netlist, Inc.			
	159	Application Number 12/912,623; filed 10/26/10; Owned by Netlist, Inc.			
	160	Application Number 95/001,339; filed 06/08/2010; Owned by Netlist, Inc.			
	161	Application Number 95/001,337; filed 06/04/2010; Owned by Netlist, Inc.			
	162	Application Number 95/000,546; filed 05/11/2010; Owned by Netlist, Inc.			
	163	Application Number 95/001,381; filed 06/09/2010; Owned by Netlist, Inc.			

Examiner Signature	Date Considered
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(Multiple sheets used when necessary)</i>	Application No.	12/955,711
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	First Named Inventor	Solomon et al.
	Art Unit	2824
	Examiner	Sofocleous, Alexander
SHEET 7 OF 14	Attorney Docket No.	NETL.18CPCPCCC

U.S. PATENT DOCUMENTS					
Examiner Initials	Cite No.	Document Number Number - Kind Code (if known) Example: 1,234,567 B1	Publication Date MM-DD-YYYY	Name of Patentee or Applicant	Pages, Columns, Lines Where Relevant Passages or Relevant Figures Appear
	164	Request for <i>Inter Partes</i> Reexamination; Reexam App. No. 95/000,577 for U.S. Pat. No. 7,289,386 filed 10/20/2010			
	165	Request for <i>Inter Partes</i> Reexamination; Reexam App. No. 95/000,578 for U.S. Pat. No. 7,619,912 filed 10/20/2010			
	166	Request for <i>Inter Partes</i> Reexamination; Reexam App. No. 95/000,579 for U.S. Pat. No. 7,619,912 filed 10/21/2010			

FOREIGN PATENT DOCUMENTS						
Examiner Initials	Cite No.	Foreign Patent Document Country Code-Number-Kind Code Example: JP 1234567 A1	Publication Date MM-DD-YYYY	Name of Patentee or Applicant	Pages, Columns, Lines Where Relevant Passages or Relevant Figures Appear	T ¹
	167	WO 1992/002879	2/20/1992	Du Pont Pixel Systems Limited		
	168	WO 1994/007242	3/31/1994	Atmel Corporation		
	169	WO 1995/034030	12/14/1995	Intel Corporation		
	170	WO 2002/058069	7/25/2002	Honeywell International Inc.		
	171	WO 2003/017283	2/27/2003	Micron Technology, Inc.		
	172	WO 2003/069484	8/21/2003	Micron Technology, Inc.		
	173	WO 2006/055497	5/26/2006	Intel Corporation		

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	174	"64 & 72 Pin Zip/Simm Sram Module", JEDEC, Standard No. 21-C, www.jedec.com/download/search/4_04_01.pdf, June 1997 pages 4.4.1-1.	
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	266	U.S. District Court Northern District of California, Case No. CV08 04144, GOOGLE INC. v. NETLIST, INC., Appendix 1 To Google's Responsive Claim Construction Brief, filed August 25, 2009 in 4 pages.	
	267	U.S. District Court Northern District of California, Case No. CV08 04144, GOOGLE INC. v. NETLIST, INC., Attachment 1 To Exhibit B To Joint Claim Construction And Prehearing Statement, filed June 12, 2009 in 7 pages.	
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Electronic Acknowledgement Receipt	
EFS ID:	9253994
Application Number:	12955711
International Application Number:	
Confirmation Number:	8026
Title of Invention:	CIRCUIT PROVIDING LOAD ISOLATION AND MEMORY DOMAIN TRANSLATION FOR MEMORY MODULE
First Named Inventor/Applicant Name:	Jeffrey C. Solomon
Customer Number:	20995
Filer:	Bruce S. Itchkawitz/Lori Larson
Filer Authorized By:	Bruce S. Itchkawitz
Attorney Docket Number:	NETL.18CPCPCCC
Receipt Date:	18-JAN-2011
Filing Date:	29-NOV-2010
Time Stamp:	17:39:05
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Applicant summary of interview with examiner	interview_summary.pdf	78908 fa45b39567dc89a0d819bb43debae2c2c6e46d82	no	2

Warnings:

Information:

2		ids.pdf	995110	yes	15
	7960281484bc6296269ace81026fe3e3515f14b1				
	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Transmittal Letter		1	1	
	Information Disclosure Statement (IDS) Filed (SB/08)		2	15	
Warnings:					
Information:					
Total Files Size (in bytes):			1074018		
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants	:	Solomon et al.	Group Art Unit 2824
Appl. No.	:	12/955,711	
Filed	:	November 29, 2010	
For	:	CIRCUIT PROVIDING LOAD ISOLATION AND MEMORY DOMAIN TRANSLATION FOR MEMORY MODULE	
Examiner	:	Alexander Sofocleous	
Conf. No.	:	8026	

STATEMENT OF SUBSTANCE OF JANUARY 11, 2011 INTERVIEW**Mail Stop Amendment**

Commissioner for Patents

P.O. Box 1450

Alexandria, VA 22313-1450

Dear Sir:

Applicants submit this summary of the substance of the personal interview conducted on January 11, 2011.

Attendees, Date and Type of Interview

The interview was conducted in person on January 11, 2011 and was attended by Examiner Alexander Sofocleous and Applicants' representative, Bruce S. Itchkawitz (Reg. No. 47,677). No exhibits were shown and no demonstrations were conducted.

Identification of Claims Discussed

Claims 1, 24, and 31

Identification of Prior Art Discussed

Amidi et al. (U.S. Pat. Appl. Publ. No. 2006/0117152)

Substance of Interview

As summarized in the form PTOL-413 prepared at the time of the interview, agreement was reached that the claims are patentable over Amidi et al. and the other references of record,

Appl. No. : 12/955,711
Filed : November 29, 2010

alone or in combination with one another. The phrase "other references of record," as used in the form PTOL-413, refers to all the references of record in the parent patents and patent applications to which the present application claims priority.

As referred to in the form PTOL-413, initially it was agreed that these references were to be cited on a form PTO-892 prepared by the examiner after the interview. However, it was later agreed that these references would instead be cited on an Information Disclosure Statement prepared and submitted by Applicants. The Information Disclosure Statement being submitted herewith cites these references.

In addition, agreement was reached that the recitation of rank in the preambles of Claims 1, 24, and 31 (i.e., "each rank of the first number of ranks comprising a plurality of double-data-rate (DDR) memory devices that are configured to be activated concurrently with one another and separately from the DDR memory devices of the other ranks by a first number of chip-select signals for receiving and transmitting data having a bit width of the rank") is supported by the disclosure.

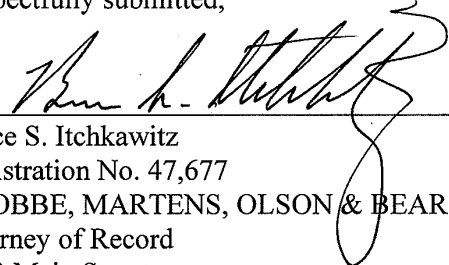
It was also agreed to cosmetically amend Claims 7 and 36 by Examiner's Amendment.

Please charge any additional fees, including any fees for additional extension of time, or credit overpayment to Deposit Account No. 11-1410.

Respectfully submitted,

Dated: 1/18/11

By:


Bruce S. Itchkawitz
Registration No. 47,677
KNOBBE, MARTENS, OLSON & BEAR, LLP
Attorney of Record
2040 Main Street
Fourteenth Floor
Irvine, CA 92614
(949) 760-0404

10314945
011811

INFORMATION DISCLOSURE STATEMENT

Applicant : Solomon et al.
App. No : 12/955711
Filed : November 29, 2010
For : CIRCUIT PROVIDING LOAD
ISOLATION AND MEMORY
DOMAIN TRANSLATION FOR
MEMORY MODULE
Examiner : Sofocleous, Alexander
Art Unit : 2824
Conf No. : 8026

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

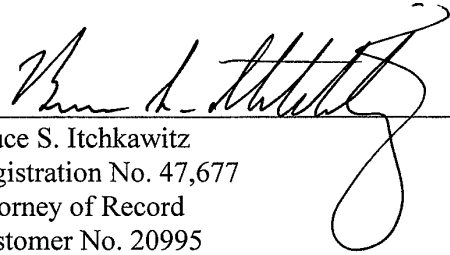
Enclosed is a PTO/SB/08 Equivalent listing 289 references that are of record in U.S. patent application No. 12/629,827, filed December 2, 2009, which is the parent of this continuation application, and is relied upon for an earlier filing date under 35 U.S.C. § 120. Copies of the references are not submitted pursuant to 37 C.F.R. § 1.98(d).

This Information Disclosure Statement is being filed before the receipt of a first Office Action on the merits, and presumably no fee is required. If a first Office Action on the merits was mailed before the mailing date of this Statement, the Commissioner is authorized to charge the fee set forth in 37 C.F.R. § 1.17(p) to Deposit Account No. 11-1410.

Respectfully submitted,

KNOBBE, MARTENS, OLSON & BEAR, LLP

Dated: 1/18/11

By: 

Bruce S. Itchkawitz
Registration No. 47,677
Attorney of Record
Customer No. 20995
(949) 760-0404

10316221//011811



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

20995 7590 02/02/2011

KNOBBE MARTENS OLSON & BEAR LLP
2040 MAIN STREET
FOURTEENTH FLOOR
IRVINE, CA 92614

EXAMINER

SOFOCLEOUS, ALEXANDER

ART UNIT

PAPER NUMBER

2824

DATE MAILED: 02/02/2011

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/955,711	11/29/2010	Jeffrey C. Solomon	NETL18CPCPCCC	8026

TITLE OF INVENTION: CIRCUIT PROVIDING LOAD ISOLATION AND MEMORY DOMAIN TRANSLATION FOR MEMORY MODULE

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	\$1510	\$300	\$0	\$1810	05/02/2011

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: **Mail** **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax **(571)-273-2885**

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

20995 7590 02/02/2011

KNOBBE MARTENS OLSON & BEAR LLP
2040 MAIN STREET
FOURTEENTH FLOOR
IRVINE, CA 92614

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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12/955,711 11/29/2010 Jeffrey C. Solomon NETL.18CPCPCCC 8026

TITLE OF INVENTION: CIRCUIT PROVIDING LOAD ISOLATION AND MEMORY DOMAIN TRANSLATION FOR MEMORY MODULE

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	\$1510	\$300	\$0	\$1810	05/02/2011

EXAMINER	ART UNIT	CLASS-SUBCLASS
SOFOCLEOUS, ALEXANDER	2824	365-230060

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

- (1) the names of up to 3 registered patent attorneys or agents OR, alternatively, 1 _____
(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed. 2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

- ☐ Issue Fee
☐ Publication Fee (No small entity discount permitted)
☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)

- ☐ A check is enclosed.
☐ Payment by credit card. Form PTO-2038 is attached.
☐ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)

- ☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27. ☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____

Date _____

Typed or printed name _____

Registration No. _____

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/955,711	11/29/2010	Jeffrey C. Solomon	NETL18CPCPCCC	8026
20995	7590	02/02/2011	EXAMINER	
KNOBBE MARTENS OLSON & BEAR LLP 2040 MAIN STREET FOURTEENTH FLOOR IRVINE, CA 92614			SOFOCLEOUS, ALEXANDER	
			ART UNIT	PAPER NUMBER
			2824	
DATE MAILED: 02/02/2011				

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 0 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 0 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

Notice of Allowability	Application No.	Applicant(s)	
	12/955,711	SOLOMON ET AL.	
	Examiner	Art Unit	
	ALEXANDER SOFOCLEOUS	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to the Application filed November 29, 2010.

2. ☒ The allowed claim(s) is/are 1-40.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) ☐ All b) ☐ Some* c) ☐ None of the:
 1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

* Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
 (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
 1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
 (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892) 2. ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 3. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date <u>1/18/2011</u> 4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material	5. ☐ Notice of Informal Patent Application 6. ☒ Interview Summary (PTO-413), Paper No./Mail Date <u>20110111</u> . 7. ☒ Examiner's Amendment/Comment 8. ☒ Examiner's Statement of Reasons for Allowance 9. ☐ Other _____.
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/ALEXANDER SOFOCLEOUS/ Examiner, Art Unit 2824	
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Summary of Record of Interview Requirements

Manual of Patent Examining Procedure (MPEP), Section 713.04, Substance of Interview Must be Made of Record

A complete written statement as to the substance of any face-to-face, video conference, or telephone interview with regard to an application must be made of record in the application whether or not an agreement with the examiner was reached at the interview.

Title 37 Code of Federal Regulations (CFR) § 1.133 Interviews

Paragraph (b)

In every instance where reconsideration is requested in view of an interview with an examiner, a complete written statement of the reasons presented at the interview as warranting favorable action must be filed by the applicant. An interview does not remove the necessity for reply to Office action as specified in §§ 1.111, 1.135. (35 U.S.C. 132)

37 CFR §1.2 Business to be transacted in writing.

All business with the Patent or Trademark Office should be transacted in writing. The personal attendance of applicants or their attorneys or agents at the Patent and Trademark Office is unnecessary. The action of the Patent and Trademark Office will be based exclusively on the written record in the Office. No attention will be paid to any alleged oral promise, stipulation, or understanding in relation to which there is disagreement or doubt.

The action of the Patent and Trademark Office cannot be based exclusively on the written record in the Office if that record is itself incomplete through the failure to record the substance of interviews.

It is the responsibility of the applicant or the attorney or agent to make the substance of an interview of record in the application file, unless the examiner indicates he or she will do so. It is the examiner's responsibility to see that such a record is made and to correct material inaccuracies which bear directly on the question of patentability.

Examiners must complete an Interview Summary Form for each interview held where a matter of substance has been discussed during the interview by checking the appropriate boxes and filling in the blanks. Discussions regarding only procedural matters, directed solely to restriction requirements for which interview recordation is otherwise provided for in Section 812.01 of the Manual of Patent Examining Procedure, or pointing out typographical errors or unreadable script in Office actions or the like, are excluded from the interview recordation procedures below. Where the substance of an interview is completely recorded in an Examiners Amendment, no separate Interview Summary Record is required.

The Interview Summary Form shall be given an appropriate Paper No., placed in the right hand portion of the file, and listed on the "Contents" section of the file wrapper. In a personal interview, a duplicate of the Form is given to the applicant (or attorney or agent) at the conclusion of the interview. In the case of a telephone or video-conference interview, the copy is mailed to the applicant's correspondence address either with or prior to the next official communication. If additional correspondence from the examiner is not likely before an allowance or if other circumstances dictate, the Form should be mailed promptly after the interview rather than with the next official communication.

The Form provides for recordation of the following information:

- Application Number (Series Code and Serial Number)
- Name of applicant
- Name of examiner
- Date of interview
- Type of interview (telephonic, video-conference, or personal)
- Name of participant(s) (applicant, attorney or agent, examiner, other PTO personnel, etc.)
- An indication whether or not an exhibit was shown or a demonstration conducted
- An identification of the specific prior art discussed
- An indication whether an agreement was reached and if so, a description of the general nature of the agreement (may be by attachment of a copy of amendments or claims agreed as being allowable). Note: Agreement as to allowability is tentative and does not restrict further action by the examiner to the contrary.
- The signature of the examiner who conducted the interview (if Form is not an attachment to a signed Office action)

It is desirable that the examiner orally remind the applicant of his or her obligation to record the substance of the interview of each case. It should be noted, however, that the Interview Summary Form will not normally be considered a complete and proper recordation of the interview unless it includes, or is supplemented by the applicant or the examiner to include, all of the applicable items required below concerning the substance of the interview.

A complete and proper recordation of the substance of any interview should include at least the following applicable items:

- 1) A brief description of the nature of any exhibit shown or any demonstration conducted,
- 2) an identification of the claims discussed,
- 3) an identification of the specific prior art discussed,
- 4) an identification of the principal proposed amendments of a substantive nature discussed, unless these are already described on the Interview Summary Form completed by the Examiner,
- 5) a brief identification of the general thrust of the principal arguments presented to the examiner,
(The identification of arguments need not be lengthy or elaborate. A verbatim or highly detailed description of the arguments is not required. The identification of the arguments is sufficient if the general nature or thrust of the principal arguments made to the examiner can be understood in the context of the application file. Of course, the applicant may desire to emphasize and fully describe those arguments which he or she feels were or might be persuasive to the examiner.)
- 6) a general indication of any other pertinent matters discussed, and
- 7) if appropriate, the general results or outcome of the interview unless already described in the Interview Summary Form completed by the examiner.

Examiners are expected to carefully review the applicant's record of the substance of an interview. If the record is not complete and accurate, the examiner will give the applicant an extendable one month time period to correct the record.

Examiner to Check for Accuracy

If the claims are allowable for other reasons of record, the examiner should send a letter setting forth the examiner's version of the statement attributed to him or her. If the record is complete and accurate, the examiner should place the indication, "Interview Record OK" on the paper recording the substance of the interview along with the date and the examiner's initials.

Continuation of Substance of Interview including description of the general nature of what was agreed to if an agreement was reached, or any other comments: On January 11, 2011, discussed the recitation of rank in the preamble and agreed it is supported by the disclosure. It was also agreed that the claims distinguish over Amidi et al. and the other references of record, alone or in combination (see form PTO-892). It was also agreed to cosmetically amend claims 7 and 36 by Examiner's Amendment.

***A subsequent telephone interview was held to discuss filing an IDS (instead of citing the references on the PTO-892). Applicant's interview summary submitted 1/18/2011 completely and accurately reflects the substance of both of these interviews. AGS 1/24/2011

DETAILED ACTION

1. This action is responsive to the following communication: Application filed on November 29, 2010 and the Information Disclosure Statement filed January 18, 2011.
2. Claims 1-40 are pending. Claims 7 and 36 are cosmetically amended by Examiner's Amendment. Claims 1, 24, and 31 are independent.

EXAMINER'S AMENDMENT

3. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a personal interview with Bruce Itchkawitz (Reg. No. 47,677) on January 11, 2011.

In the Claims, Claim 7, line 4, change "the at least one selected" to --the selected--.

In the Claims, Claim 36, line 4, change "the at least one selected" to --the selected--.

Subsequent Interview and Applicant's Interview Summary

4. A subsequent telephone interview was held to discuss the filing of the IDS, which was agreed to be more practical instead of the Examiner citing all of the

references from the related applications on the PTO-892. Applicant's summary of the interviews submitted January 18, 2011 completely and accurately reflects the substance of the interviews.

Information Disclosure Statement

5. Acknowledgment is made of applicant's Information Disclosure Statement (IDS) filed on January 18, 2011. This IDS has been considered.

6. Citation 127 (U.S. Patent 7,881,150) has not yet actually published; although it is scheduled and due for publishing on February 1, 2011 (likely after the mailing of this Action but prior to Patent maturity). This citation corresponds to application 12/629,827 for which its prosecution history has been reviewed and considered; and thus, it has been considered.

7. Citations 151 and 152 (corresponding to applications 12/504,131 and 12/761,179, respectively) have since published as patent application publications (2011/0016269 and 2001/0016250, respectively). These two citations have been struck-through in favor of their corresponding patent application publications. The patent application publications have been cited on form PTO-892 to reflect consideration.

8. It is noted that the prosecution histories for the following related applications have been reviewed and considered: 11/075,395; 11/173,175; 11/335,875; 12/408,652; 12/629,827; 12/981,380; 11/862,931; 12/577,682; and 12/954,492.

9. It is further noted that the following re-examination prosecution histories

have been reviewed and considered: 95/000,546; 95/000,577; 95/001,338;
95/001,381; 95/001,337; 95/000,578; 95/000,579; and 95/001,339.

10. Additionally, it is noted that the following prosecution history has been reviewed and considered: 11/142,989.

Allowable Subject Matter

11. **Claims 1-40 are allowed.**

12. The following is an examiner's statement of reasons for allowance:

With respect to independent claim 1, there is no teaching, suggestion, or motivation for combination in the prior art to a circuit configured to be mounted on a memory module (configured to be operationally coupled to a computer system) having a physical memory domain with a first number of ranks (having a first number of DDR memory devices), wherein each rank includes a plurality of DDR memory devices configured to be activated concurrently with one another and separately from the DDR memory devices of other ranks by a first number of chip-select signals for receiving and transmitting data having a bit width of the rank, wherein the circuit is configured to receive a set of signals including bank address signals, row/column address signals, and a second number of chip-select signals (smaller than the first chip-select signals), wherein the set of signals are capable of controlling a memory module having a system memory domain with a second number of ranks (smaller than the first number of ranks) having a second number of DDR memory devices (smaller than the first number

of DDR memory devices), wherein the circuit is configurable to generate phase-locked clock signals (for which the circuit is further configurable to transmit these phase-locked clock signals to the first number of ranks), wherein the circuit is configurable to selectively isolate a load of at least one rank of the first number of ranks from the computer system in response to the received set of signals, and wherein the circuit is configurable to translate between the system memory domain and the physical memory domain which includes generating the first number of chip-select signals in response to the phase-locked clock signals and the received banks address signals, in combination with the other limitations.

With respect to independent claim 24, there is no teaching, suggestion, or motivation for combination in the prior art to a circuit configured to be mounted on a memory module (configured to be operationally coupled to a computer system) having a physical memory domain with a first number of ranks (having a first number of DDR memory devices), wherein each rank includes a plurality of DDR memory devices configured to be activated concurrently with one another and separately from the DDR memory devices of other ranks by a first number of chip-select signals for receiving and transmitting data having a bit width of the rank, wherein the circuit includes: means for receiving a set of signals including bank address signals, row/column address signals, and a second number of chip-select signals (smaller than the first chip-select signals), wherein the set of signals are capable of controlling a memory module having a system memory domain with a second number of ranks (smaller than the first number of ranks) having a second number of DDR memory devices (smaller than the first number

of DDR memory devices), means for generating phase-locked clock signals (which are further transmitted to the first number of ranks), means for selectively isolating a load of at least one rank of the first number of ranks from the computer system in response to the received set of signals, and means for translating between the system memory domain and the physical memory domain which includes generating the first number of chip-select signals in response to the phase-locked clock signals and the received banks address signals, in combination with the other limitations.

With respect to independent claim 31, there is no teaching, suggestion, or motivation for combination in the prior art to a method of using a memory module (configured to be operationally coupled to a computer system) having a physical memory domain with a first number of ranks (having a first number of DDR memory devices), wherein each rank includes a plurality of DDR memory devices configured to be activated concurrently with one another and separately from the DDR memory devices of other ranks by a first number of chip-select signals for receiving and transmitting data having a bit width of the rank, including: providing a circuit (configured to be mounted on the memory module), using the circuit to receive a set of signals including bank address signals, row/column address signals, and a second number of chip-select signals (smaller than the first chip-select signals), wherein the set of signals are capable of controlling a memory module having a system memory domain with a second number of ranks (smaller than the first number of ranks) having a second number of DDR memory devices (smaller than the first number of DDR memory devices),

using the circuit to generate phase-locked clock signals (for which the circuit is further configurable to transmit these phase-locked clock signals to the first number of ranks), wherein the circuit is configurable to selectively isolate a load of at least one rank of the first number of ranks from the computer system in response to the received set of signals, and using the circuit to translate between the system memory domain and the physical memory domain which includes generating the first number of chip-select signals in response to the phase-locked clock signals and the received banks address signals, in combination with the other limitations.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

CONCLUSION

The following prior art made of record and not relied upon is considered pertinent to applicant's disclosure: Amidi et al. (U.S. Patent Application Publication 2006/0117152 citation 143 on IDS), Ellsberry et al. (U.S. Patent Application 2006/0277355 citation 149 on IDS), Dell et al. '074 (U.S. Patent 6,209,074 citation 38 on IDS), Johnson et al. (U.S. Patent 6,233,650 citation 40 on IDS), Karabatsos (U.S. Patent 6,446,158 citation 50 on IDS), Dell et al. '184 (U.S. Patent 6,446,184 citation 49 on IDS), Kinsley et al. (U.S. Patent 7,046,538

citation 95 on IDS), Lamb et al. (U.S. Patent 6,807,650), Ruckerbauer et al. (U.S. Patent 7,078,793), and LaBerge et al. (U.S. Patent 7,124,260).

Amidi et al. shows a four rank memory module with a CPLD, register, and PLL.

Ellsberry et al., filed after the instant application's earliest effective filing date, show a memory module with controller and PLL.

Dell et al. '074 teach an SDRAM memory module with an ASIC so a memory module utilizing memory chips having 4-banks may be used in a memory system that would be expecting each memory chip to have 2-banks.

Johnson et al. teach a memory system employing a switch to selectively couple the data bus of two of the four DIMMs (either DIMMs 1 and 2, or DIMMs 3 and 4).

Karabatsos a first memory device which is selectively connected to the data bus by a first switch and a second memory device which is selectively connected to the data bus by a second switch, such that e.g., the first memory device and second memory device may be single data rate memory which, by employing the first and second switches, may operate as a double data rate memory.

Dell et al. '184 teach an SDRAM memory module with an ASIC so a memory module utilizing memory chips having 4-banks may be used in a memory system that would be expecting each memory chip to have 2-banks.

Kinsley et al., filed after the instant application's earliest effective filing date, teach a four-rank memory module with the memory chips of a fourth rank stacked on the memory chips of a third rank which are stacked on the memory chips of a second rank which are stacked on the memory chips of the first rank.

Lamb et al. provide a glossary of terms including the definition of rank.

Ruckerbauer et al. provide a discussion of memory modules and ranks. The teachings also include stacking memory chips in particular configurations.

LaBerge et al. also provide a discussion of memory modules and ranks.

None of the references, alone or in combination, meet all of the following limitations: a circuit configured to be mounted on a memory module (configured to be operationally coupled to a computer system) having a physical memory domain with a first number of ranks (having a first number of DDR memory devices), wherein each rank includes a plurality of DDR memory devices configured to be activated concurrently with one another and separately from the DDR memory devices of other ranks by a first number of chip-select signals for receiving and transmitting data having a bit width of the rank, wherein the circuit is configured to receive a set of signals including bank address signals, row/column address signals, and a second number of chip-select signals (smaller than the first chip-select signals), wherein the set of signals are capable of controlling a memory module having a system memory domain with a second number of ranks (smaller than the first number of ranks) having a second number of DDR memory devices (smaller than the first number of DDR memory devices),

wherein the circuit is configurable to generate phase-locked clock signals (for which the circuit is further configurable to transmit these phase-locked clock signals to the first number of ranks), wherein the circuit is configurable to selectively isolate a load of at least one rank of the first number of ranks from the computer system in response to the received set of signals, and wherein the circuit is configurable to translate between the system memory domain and the physical memory domain which includes generating the first number of chip-select signals in response to the phase-locked clock signals and the received banks address signals, **as recited in claim 1**; a circuit configured to be mounted on a memory module (configured to be operationally coupled to a computer system) having a physical memory domain with a first number of ranks (having a first number of DDR memory devices), wherein each rank includes a plurality of DDR memory devices configured to be activated concurrently with one another and separately from the DDR memory devices of other ranks by a first number of chip-select signals for receiving and transmitting data having a bit width of the rank, wherein the circuit includes: means for receiving a set of signals including bank address signals, row/column address signals, and a second number of chip-select signals (smaller than the first chip-select signals), wherein the set of signals are capable of controlling a memory module having a system memory domain with a second number of ranks (smaller than the first number of ranks) having a second number of DDR memory devices (smaller than the first number of DDR memory devices), means for generating phase-locked clock signals (which are further transmitted to the first number of ranks), means for selectively

isolating a load of at least one rank of the first number of ranks from the computer system in response to the received set of signals, and means for translating between the system memory domain and the physical memory domain which includes generating the first number of chip-select signals in response to the phase-locked clock signals and the received banks address signals, **as recited in claim 24**; and a method of using a memory module (configured to be operationally coupled to a computer system) having a physical memory domain with a first number of ranks (having a first number of DDR memory devices), wherein each rank includes a plurality of DDR memory devices configured to be activated concurrently with one another and separately from the DDR memory devices of other ranks by a first number of chip-select signals for receiving and transmitting data having a bit width of the rank, including: providing a circuit (configured to be mounted on the memory module), using the circuit to receive a set of signals including bank address signals, row/column address signals, and a second number of chip-select signals (smaller than the first chip-select signals), wherein the set of signals are capable of controlling a memory module having a system memory domain with a second number of ranks (smaller than the first number of ranks) having a second number of DDR memory devices (smaller than the first number of DDR memory devices), using the circuit to generate phase-locked clock signals (for which the circuit is further configurable to transmit these phase-locked clock signals to the first number of ranks), wherein the circuit is configurable to selectively isolate a load of at least one rank of the first number of ranks from the computer system in response to the

received set of signals, and using the circuit to translate between the system memory domain and the physical memory domain which includes generating the first number of chip-select signals in response to the phase-locked clock signals and the received banks address signals, **as recited in claim 31**.

When responding to this office action, applicants are advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist the examiner in locating appropriate paragraphs.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander Sofocleous whose telephone number is 571-272-0635. The examiner can normally be reached on 7:00am - 4pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on 571-272-1869. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-

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Art Unit: 2824

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free).

/ALEXANDER SOFOCLEOUS/
Examiner, Art Unit 2824

Notice of References Cited	Application/Control No. 12/955,711		Applicant(s)/Patent Under Reexamination SOLOMON ET AL.	
	Examiner ALEXANDER SOFOCLEOUS		Art Unit 2824	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-2011/0016269	01-2011	Lee et al.	711/105
*	B	US-2011/0016250	01-2011	Lee et al.	710/308
*	C	US-6,807,650	10-2004	Lamb et al.	716/101
*	D	US-7,078,793	07-2006	Ruckerbauer et al.	257/686
*	E	US-7,124,260	10-2006	LaBerge et al.	711/155
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

<i>Index of Claims</i> 	Application/Control No. 12955711	Applicant(s)/Patent Under Reexamination SOLOMON ET AL.
	Examiner ALEXANDER SOFOCLEOUS	Art Unit 2824

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☒ Claims renumbered in the same order as presented by applicant	☐ CPA	☐ T.D.	☐ R.1.47
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CLAIM		DATE									
Final	Original	01/14/2011									
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<i>Index of Claims</i> 	Application/Control No. 12955711	Applicant(s)/Patent Under Reexamination SOLOMON ET AL.
	Examiner ALEXANDER SOFOCLEOUS	Art Unit 2824

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☒ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47										
CLAIM		DATE								
Final	Original	01/14/2011								
	37	=								
	38	=								
	39	=								
	40	=								

Issue Classification 	Application/Control No. 12955711	Applicant(s)/Patent Under Reexamination SOLOMON ET AL.
	Examiner ALEXANDER SOFOCLEOUS	Art Unit 2824

ORIGINAL						INTERNATIONAL CLASSIFICATION												
CLASS		SUBCLASS				CLAIMED					NON-CLAIMED							
365		230.06				G	1	1	C	8 / 00 (2006.01.01)								
CROSS REFERENCE(S)																		
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)																	
365	51	149	230.03	233.13														

☒ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47															
Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original

(Assistant Examiner) _____ (Date) _____ /ALEXANDER SOFOCLEOUS/ Examiner, Art Unit 2824 (Primary Examiner) _____ (Date) _____		Total Claims Allowed: 40 O.G. Print Claim(s) 1 O.G. Print Figure 1, 9a	
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Search Notes 	Application/Control No. 12955711	Applicant(s)/Patent Under Reexamination SOLOMON ET AL.
	Examiner ALEXANDER SOFOCLEOUS	Art Unit 2824

SEARCHED			
Class	Subclass	Date	Examiner
365	51, 149, 230.03, 230.06, 233.13	01/27/2011	AGS

SEARCH NOTES		
Search Notes	Date	Examiner
reviewed reexamination histories: 95/000,546; 95/000,577; 95/000,578; 95/000,579; 95/001,337; 95/001,338; 95/001,339; and 95/001,381	01/25/2011	AGS
reviewed parent case histories: 11/075,395; 11/173,175; 11/335,875; 12/408,652; and 12/629,827	01/26/2011	AGS
reviewed related case histories: 11/862,931; 12/577,682; 12/954,492; and 12/981,380	01/26/2011	AGS
reviewed application history: 11/142,989	01/26/2011	AGS
see EAST search history	01/27/2011	AGS

INTERFERENCE SEARCH			
Class	Subclass	Date	Examiner
365	51, 149, 230.03, 230.06, 233.13	01/27/2011	AGS

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Receipt date: 01/18/2011

12955711 - GAU: 2824

PTO/SB/08 Equivalent

INFORMATION DISCLOSURE STATEMENT BY APPLICANT	Application No.	12/955,711
	Filing Date	November 29, 2010
	First Named Inventor	Solomon et al.
	Art Unit	2824
(Multiple sheets used when necessary)	Examiner	Sofocleous, Alexander
SHEET 1 OF 14	Attorney Docket No.	NETL.18CPCPCCC

U.S. PATENT DOCUMENTS					
Examiner Initials	Cite No.	Document Number Number - Kind Code (if known) Example: 1,234,567 B1	Publication Date MM-DD-YYYY	Name of Patentee or Applicant	Pages, Columns, Lines Where Relevant Passages or Relevant Figures Appear
	1	4,368,515	1/11/1983	Nielsen	
	2	4,392,212	7/5/1983	Miyasaka et al.	
	3	4,633,429	12/30/1986	Lewandowski et al.	
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	23	5,926,827	7/20/1999	Dell et al.	
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	28	6,044,032	3/28/2000	Li	
	29	6,070,217	5/30/2000	Connolly et al.	

Examiner Signature	/Alexander Sofocleous/	Date Considered	01/24/2011
*Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.			

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Samsung Electronics Co., Ltd.

Ex. 1044, p. 152

Receipt date: 01/18/2011

12955711 - GAU: 2824

PTO/SB/08 Equivalent

INFORMATION DISCLOSURE STATEMENT BY APPLICANT	Application No.	12/955,711
	Filing Date	November 29, 2010
	First Named Inventor	Solomon et al.
	Art Unit	2824
(Multiple sheets used when necessary)	Examiner	Sofocleous, Alexander
SHEET 2 OF 14	Attorney Docket No.	NETL.18CPCPCCC

U.S. PATENT DOCUMENTS					
Examiner Initials	Cite No.	Document Number Number - Kind Code (if known) Example: 1,234,567 B1	Publication Date MM-DD-YYYY	Name of Patentee or Applicant	Pages, Columns, Lines Where Relevant Passages or Relevant Figures Appear
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	31	6,097,652	8/1/2000	Roh	
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Examiner Signature	/Alexander Sofocleous/	Date Considered	01/24/2011
*Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.			

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Ex. 1044, p. 153

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12955711 - GAU: 2824

PTO/SB/08 Equivalent

INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(Multiple sheets used when necessary)</i>	Application No.	12/955,711
	Filing Date	November 29, 2010
	First Named Inventor	Solomon et al.
	Art Unit	2824
	Examiner	Sofocleous, Alexander
SHEET 3 OF 14	Attorney Docket No.	NETL.18CPCPCCC

U.S. PATENT DOCUMENTS					
Examiner Initials	Cite No.	Document Number Number - Kind Code (if known) Example: 1,234,567 B1	Publication Date MM-DD-YYYY	Name of Patentee or Applicant	Pages, Columns, Lines Where Relevant Passages or Relevant Figures Appear
	59	6,618,320	9/9/2003	Hasegawa et al.	
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	61	6,625,081	9/23/2003	Roohparvar et al.	
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	87	6,950,366	9/27/2005	Lapidus et al.	

Examiner Signature	/Alexander Sofocleous/	Date Considered	01/24/2011
*Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.			

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(Multiple sheets used when necessary)</i>	Application No.	12/955,711
	Filing Date	November 29, 2010
	First Named Inventor	Solomon et al.
	Art Unit	2824
	Examiner	Sofocleous, Alexander
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U.S. PATENT DOCUMENTS					
Examiner Initials	Cite No.	Document Number Number - Kind Code (if known) Example: 1,234,567 B1	Publication Date MM-DD-YYYY	Name of Patentee or Applicant	Pages, Columns, Lines Where Relevant Passages or Relevant Figures Appear
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	Filing Date	November 29, 2010
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	152	Application Number 12/781,179; filed 04/13/2010; Owned by Netlist, Inc.			
	153	Application Number 12/815,339; filed 06/14/2010; Owned by Netlist, Inc.			
	154	Application Number 12/774,632; filed 05/05/2010; Owned by Netlist, Inc.			
	155	Application Number 12/422,925; filed 04/13/2009; Owned by Netlist, Inc.			
	156	Application Number 12/422,853; filed 04/13/2009; Owned by Netlist, Inc.			
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	158	Application Number 12/981,380; filed 11/29/10; Owned by Netlist, Inc.			
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	160	Application Number 95/001,339; filed 06/08/2010; Owned by Netlist, Inc.			
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	162	Application Number 95/000,546; filed 05/11/2010; Owned by Netlist, Inc.			
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	169	WO 1995/034030	12/14/1995	Intel Corporation		
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(Multiple sheets used when necessary)</i>	Application No.	12/955,711
	Filing Date	November 29, 2010
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	Art Unit	2824
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NON PATENT LITERATURE DOCUMENTS			
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Examiner Signature	/Alexander Sofocleous/	Date Considered	01/24/2011
*Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.			

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Ex. 1044, p. 162

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PTO/SB/08 Equivalent

INFORMATION DISCLOSURE STATEMENT BY APPLICANT	Application No.	12/955,711
	Filing Date	November 29, 2010
	First Named Inventor	Solomon et al.
	Art Unit	2824
(Multiple sheets used when necessary)	Examiner	Sofocleous, Alexander
SHEET 12 OF 14	Attorney Docket No.	NETL.18CPCPCCC

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ¹
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	260	U.S. District Court Central District of California, Case No. CV09 06900, NETLIST, INC. vs. INPHI CORPORATION, Defendant Inphi Corporation's Answer To Plaintiff's First Amended Complaint For Patent Infringement, filed February 11, 2010 in 9 pages.	
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT	Application No.	12/955,711
	Filing Date	November 29, 2010
	First Named Inventor	Solomon et al.
	Art Unit	2824
(Multiple sheets used when necessary)	Examiner	Sofocleous, Alexander
SHEET 13 OF 14	Attorney Docket No.	NETL.18CPCPCCC

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ¹
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT	Application No.	12/955,711
	Filing Date	November 29, 2010
	First Named Inventor	Solomon et al.
	Art Unit	2824
(Multiple sheets used when necessary)	Examiner	Sofocleous, Alexander
SHEET 14 OF 14	Attorney Docket No.	NETL.18CPCPCCC

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ¹
	288	U.S. District Court Northern District of California, Case No. CV09 05718, NETLIST, INC. vs. GOOGLE, INC., Plaintiff Netlist, Inc's Opening Claim Construction Brief, filed July 16, 2010 in 29 pages.	
	289	Yao, YL. "High Density Memory Selection Circuit,: IP.com, IPCOM000078218D, 1972.	

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BIB DATA SHEET

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SERIAL NUMBER	FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.		
12/955,711	11/29/2010 RULE	365	2824	NETL.18CPCPCCC		
APPLICANTS Jeffrey C. Solomon, Irvine, CA; Jayesh R. Bhakta, Cerritos, CA;						
** CONTINUING DATA ***** This application is a CON of 12/629,827 12/02/2009 PAT 7,881,150 which is a CON of 12/408,652 03/20/2009 PAT 7,636,274 which is a CON of 11/335,875 01/19/2006 PAT 7,532,537 which claims benefit of 60/645,087 01/19/2005 and is a CIP of 11/173,175 07/01/2005 PAT 7,289,386 which claims benefit of 60/588,244 07/15/2004 and is a CIP of 11/075,395 03/07/2005 PAT 7,286,436 which claims benefit of 60/550,668 03/05/2004 and claims benefit of 60/575,595 05/28/2004 and claims benefit of 60/590,038 07/21/2004						
** FOREIGN APPLICATIONS *****						
** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ** 12/10/2010						
Foreign Priority claimed 35 USC 119(a-d) conditions met Verified and Acknowledged	☐ Yes ☒ No ☐ Yes ☒ No /ALEXANDER SOFOCLEOUS/ Examiner's Signature	☐ Met after Allowance Initials	STATE OR COUNTRY CA	SHEETS DRAWINGS 23	TOTAL CLAIMS 40	INDEPENDENT CLAIMS 3
ADDRESS KNOBBE MARTENS OLSON & BEAR LLP 2040 MAIN STREET FOURTEENTH FLOOR IRVINE, CA 92614 UNITED STATES						
TITLE CIRCUIT PROVIDING LOAD ISOLATION AND MEMORY DOMAIN TRANSLATION FOR MEMORY MODULE						
FILING FEE RECEIVED 2260	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:			☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit		

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
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S7	11	11/173175	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/01/12 17:29
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S2	0	12/955711	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/01/12 17:29
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S20	49	rank with defin\$5 same memory adj module	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/01/12 17:47
S22	1	(10/228781).APP.	USPAT; USOCR	AND	ON	2011/01/12 17:57

S23	125	("20010003198" "20010052057" "20020088633" "20030063514" "20030090359" "20030090879" "20030191995" "20030210575" "20040000708" "20040037158" "20040201968" "20050036378" "20050281096" "20060044860" "20060117152" "20060126369" "20060129755" "20060179206" "20060259711" "20060267172" "20060277355" "20100128507" "4368515" "4392212" "4633429" "4670748" "4866603" "4958322" "4961172" "4980850" "5247643" "5345412" "5426753" "5483497" "5495435" "5581498" "5590071" "5699542" "5702984" "5703826" "5745914" "5802395" "5805520" "5822251" "5926827" "5959930" "5963464" "5966736" "6018787" "6044032" "6070217" "6070227" "6097652" "6108745" "6134638" "6151271" "6154418" "6154419" "6185654" "6209074" "6226709" "6226736" "6233650" "6247088" "6317352" "6400637" "6408356" "6414868" "6415374" "6446158" "6446184" "6453381" "6470417" "6502161" "6518794" "6526473" "6530007" "6530033" "6553450" "6618320" "6621496" "6625081" "6625687" "6636935" "6646949" "6658509" "6674684" "6681301" "6683372" "6697888" "6705877" "6717855" "6738880" "6742098" "6754797" "6785189" "6788592" "6807125" "6813196" "6834014" "6854042" "6880094" "6889304" "6912615" "6912628" "6925028" "6944694" "6950366" "6961281" "6981089" "6982892" "6982893" "6990043" "6996686" "7007130" "7007175" "7046538").PN. OR ("7054179" "7065626" "7073041" "7120727" "7124260" "7127584" "7130952" "7133960" "7133972" "7142461" "7149841" "7167967" "7181591" "7200021" "7227910" "7266639" "7272709" "7281079" "7286436" "7289386" "7346750" "7356639" "7370238" "7437591" "7461182" "7471538" "7532537" "7619912"	USPAT; USOCR	AND	ON	2011/01/12 18:15
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S24	22	("20010003198" "20010052057" "20020088633" "20030063514" "20030090359" "20030090879" "20030191995" "20030210575" "20040000708" "20040037158" "20040201968" "20050036378" "20050281096" "20060044860" "20060117152" "20060126369" "20060129755" "20060179206" "20060259711" "20060267172" "20060277355" "20100128507" "4368515" "4392212" "4633429" "4670748" "4866603" "4958322" "4961172" "4980850" "5247643" "5345412" "5426753" "5483497" "5495435" "5581498" "5590071" "5699542" "5702984" "5703826" "5745914" "5802395" "5805520" "5822251" "5926827" "5959930" "5963464" "5966736" "6018787" "6044032" "6070217" "6070227" "6097652" "6108745" "6134638" "6151271" "6154418" "6154419" "6185654" "6209074" "6226709" "6226736" "6233650" "6247088" "6317352" "6400637" "6408356" "6414868" "6415374" "6446158" "6446184" "6453381" "6470417" "6502161" "6518794" "6526473" "6530007" "6530033" "6553450" "6618320" "6621496" "6625081" "6625687" "6636935" "6646949" "6658509" "6674684" "6681301" "6683372" "6697888" "6705877" "6717855" "6738880" "6742098" "6754797" "6785189" "6788592" "6807125" "6813196" "6834014" "6854042" "6880094" "6889304" "6912615" "6912628" "6925028" "6944694" "6950366" "6961281" "6981089" "6982892" "6982893" "6990043" "6996686" "7007130" "7007175" "7046538").PN. OR ("7054179" "7065626" "7073041" "7120727" "7124260" "7127584" "7130952" "7133960" "7133972" "7142461" "7149841" "7167967" "7181591" "7200021" "7227910" "7266639" "7272709" "7281079" "7286436" "7289386" "7346750" "7356639" "7370238" "7437591"	US-PGPUB	AND	ON	2011/01/12 18:16

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S28	6463	(365/51,52,149,233.13).CCLS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2011/01/13 10:12
S29	125	(("4368515" or ("4392212" or ("4633429" or ("4670748" or ("4866603" or ("4958322" or ("4961172" or ("4980850" or ("5247643" or ("5345412" or ("5426753" or ("5483497" or ("5495435" or ("5581498" or ("5590071" or ("5699542" or ("5702984" or ("5703826" or ("5745914" or ("5802395" or ("5805520" or ("5822251" or ("5926827" or ("5959930" or ("5963464" or ("5966736" or ("6018787" or ("6044032" or ("6070217" or ("6070227" or ("6097652" or ("6108745" or ("6134638" or ("6151271" or ("6154418" or ("6154419" or ("6185654" or ("6209074" or ("6226709" or ("6226736" or ("6233650" or ("6247088" or ("6317352" or ("6400637" or ("6408356" or ("6414868" or ("6415374" or ("6446158" or ("6446184" or ("6453381" or ("6470417" or ("6502161" or ("6518794" or ("6526473" or ("6530007" or ("6530033" or ("6553450" or ("6618320" or ("6621496" or ("6625081" or ("6625687" or ("6636935" or ("6646949" or ("6658509" or ("6674684" or ("6681301" or ("6683372" or ("6697888" or ("6705877" or ("6717855" or ("6738880" or ("6742098" or ("6754797" or ("6785189" or ("6788592" or ("6807125" or ("6813196" or ("6834014" or ("6854042" or ("6880094" or ("6889304" or ("6912615" or ("6912628" or ("6925028" or ("6944694" or ("6950366" or ("6961281" or ("6981089" or ("6982892" or ("6982893" or ("6990043" or ("6996686" or ("7007130" or ("7007175" or ("7046538" or ("7054179" or	USPAT	OR	OFF	2011/01/13 10:32

		("7065626" or ("7073041" or ("7120727" or ("7124260" or ("7127584" or ("7130952" or ("7133960" or ("7133972" or ("7142461" or ("7149841" or ("7167967" or ("7181591" or ("7200021" or ("7227910" or ("7266639" or ("7272709" or ("7281079" or ("7286436" or ("7289386" or ("7346750" or ("7356639" or ("7370238" or ("7437591" or ("7461182" or ("7471538" or ("7532537" or ("7619912" or ("7636274" or ("RE36229"))).PN.				
S30	273	rank with bank ((memory adj module) or dimm or ddr)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/01/13 10:46
S33	0	12/851339	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/01/13 11:26
S32	1	12/761179	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/01/13 11:26
S31	1	12/504131	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/01/13 11:26

S34	1	11/142989	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/01/24 15:37
S35	189	rank bank ((memory adj module) or dimm or ddr) (pll or dll)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/01/25 13:50
S36	41	("20020002662" "20030090879" "5535169" "5959930" "6108745" "6115314" "6134168" "6414868" "6636957").PN. OR ("6961281").URPN.	US-PGPUB; USPAT; USOCR	AND	ON	2011/01/25 14:10
S37	3	12/504131	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/01/26 10:40
S38	2	12/761179	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/01/26 10:41
S43	0	12/954492	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/01/26 10:42

S42	1	12/422853	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/01/26 10:42
S41	1	12/422925	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/01/26 10:42
S40	1	12/774632	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/01/26 10:42
S39	1	12/815339	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/01/26 10:42
S45	0	12/912623	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/01/26 10:43
S44	0	12/981380	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/01/26 10:43

S47	5	(rank bank ((memory adj module) or dimm or ddr\$1) (dll or pll or ((phase or delay) adj lock\$3))).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/01/26 10:49
S46	214	(rank bank ((memory adj module) or dimm or ddr\$1) (dll or pll or ((phase or delay) adj lock\$3)))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/01/26 10:49
S48	13	((("4368515") or ("5581498") or ("5745914") or ("5926827") or ("6209074") or ("6233650") or ("6414868") or ("6446158") or ("6446184") or ("6961281") or ("7046538") or ("20060117152") or ("20060277355")).PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2011/01/26 11:11
S50	62	rank S49	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/01/26 11:12
S49	6149	(365/230.06).CCLS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2011/01/26 11:12
S51	1	(10/161377).APP.	USPAT; USOCR	AND	ON	2011/01/26 11:15

S53	18	rank S52	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/01/26 12:07
S52	433	(365/233.13).CCLS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2011/01/26 12:07
S56	105	S55 rank bank	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/01/27 12:14
S55	16251	(365/51,52,149,230.03,230.06,233.13).CCLS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2011/01/27 12:14
S57	31	S55 rank bank (pll or dll)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/01/27 12:15
S58	196	(rank with clock) bank	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/01/27 13:50

S59	132	(rank with clock) bank ((memory adj module) or dimm or simm or ddr\$1)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/01/27 13:51
L1	40	(rank with clock) bank ((memory adj module) or dimm or simm or ddr\$1) (pll or dll or ((phase or delay) adj lock\$3))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/01/27 13:53
L3	555	((memory adj module) or dimm or simm or ddr\$1) 2	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/01/27 13:54
L2	8865	(rank with (translat\$3 or conver\$4 or doubl\$3 or increas\$3))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/01/27 13:54
L6	37	((memory adj module) or dimm or simm or ddr\$1) same 4	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/01/27 13:55
L5	195	((memory adj module) or dimm or simm or ddr\$1) 4	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/01/27 13:55

L4	3340	(rank with (translat\$3 or conver\$4))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2011/01/27 13:55
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EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S25	0	12/954492	US-PGPUB; USPAT; UPAD	AND	ON	2011/01/12 17:28
S26	0	12/955711	US-PGPUB; USPAT; UPAD	AND	ON	2011/01/12 17:29
S54	5	(rank bank ((memory adj module) or dimm or ddr\$1) (dll or pll or ((phase or delay) adj lock\$3))).clm.	US-PGPUB; USPAT; UPAD	AND	ON	2011/01/26 11:11
L7	0	((rank with clock) bank ((memory adj module) or dimm or simm or ddr\$1) (pll or dll or ((phase or delay) adj lock\$3))).clm.	US-PGPUB; USPAT; UPAD	AND	ON	2011/01/27 13:58
L11	341	(rank with (translat\$3 or conver\$4)).clm.	US-PGPUB; USPAT; UPAD	AND	ON	2011/01/27 13:59
L10	216	(rank bank).clm.	US-PGPUB; USPAT; UPAD	AND	ON	2011/01/27 13:59
L9	15032	(365/51,52,149,230.03,230.06,233.13).CCLS.	US-PGPUB; USPAT; UPAD	OR	OFF	2011/01/27 13:59

L8	12051	((memory adj module) or dimm or simm or ddr\$1)).clm.	US-PGPUB; USPAT; UPAD	AND	ON	2011/01/27 13:59
L14	5	10 13	US-PGPUB; USPAT; UPAD	AND	ON	2011/01/27 14:00
L13	389	8 12	US-PGPUB; USPAT; UPAD	AND	ON	2011/01/27 14:00
L12	25528	(pll or dll or ((phase or delay) adj lock\$3)).clm.	US-PGPUB; USPAT; UPAD	AND	ON	2011/01/27 14:00

1/27/2011 2:00:56 PM

C:\Documents and Settings\asofocleous\My Documents\EAST\Workspaces\12954492-12955711-5.wsp

**REVOCATION
AND
GENERAL POWER OF ATTORNEY**

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

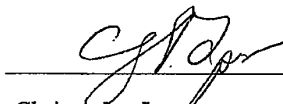
The undersigned is an empowered representative of the Assignee and hereby appoints the registrants of Knobbe, Martens, Olson & Bear, LLP, **Customer No. 20,995**, as attorneys and agents to represent the Assignee before the United States Patent and Trademark Office (USPTO) in connection with any and all patent applications assigned to the Assignee according to the USPTO assignment records or assignment documents supplied with an accompanying Statement Under 37 CFR § 3.73(b). This appointment is to be to the exclusion of the inventor(s) and his attorney(s) in accordance with the provisions of 37 CFR § 3.71.

Submission of this paper in connection with any matter of the below named assignee, together with a statement under 37 CFR 3.73(b), shall serve to revoke any previous powers of attorney in that matter.

A Statement Under 37 CFR § 3.73(b), signed by a registrant of Knobbe, Martens, Olson & Bear, LLP, is attached setting forth a full chain of title for the subject application owned by the Assignee named below.

Please recognize or change the correspondence address for the application identified in the attached Statement to **Customer No. 20,995**.

By:



Date:

6/7/07

Name:

Christopher Lopes

Title: Vice President

Assignee: NETLIST, INC.

475 Goddard, Suite 100

Address: Irvine, CA 92618

3429813/ap
021507

Electronic Acknowledgement Receipt	
EFS ID:	9364209
Application Number:	12955711
International Application Number:	
Confirmation Number:	8026
Title of Invention:	CIRCUIT PROVIDING LOAD ISOLATION AND MEMORY DOMAIN TRANSLATION FOR MEMORY MODULE
First Named Inventor/Applicant Name:	Jeffrey C. Solomon
Customer Number:	20995
Filer:	Bruce S. Itchkawitz/Valerie Jones
Filer Authorized By:	Bruce S. Itchkawitz
Attorney Docket Number:	NETL.18CPCPCCC
Receipt Date:	02-FEB-2011
Filing Date:	29-NOV-2010
Time Stamp:	19:21:26
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment		no			
File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		poa.pdf	74976	yes	2
			baf51e77d5516203624aea14f7c26b92b9af2920		

	Multipart Description/PDF files in .zip description		
	Document Description	Start	End
	Assignee showing of ownership per 37 CFR 3.73(b).	1	1
	Power of Attorney	2	2
Warnings:			
Information:			
Total Files Size (in bytes):		74976	
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.			

STATEMENT UNDER 37 CFR § 3.73(b)
ESTABLISHMENT OF ASSIGNEE

Applicant	:	Solomon et al.
App. No.	:	12/955711
Filed	:	November 29, 2010
For	:	CIRCUIT PROVIDING LOAD ISOLATION AND MEMORY DOMAIN TRANSLATION FOR MEMORY MODULE
Examiner	:	Sofocleous, Alexander
Group Art Unit	:	2824

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

This document is being filed with a copy of a Power of Attorney signed by the Assignee. This Statement sets forth the chain of title of the above-identified application.

Netlist, Inc., a corporation, is the Assignee of the entire right, title, and interest of the above-referenced application by virtue of:

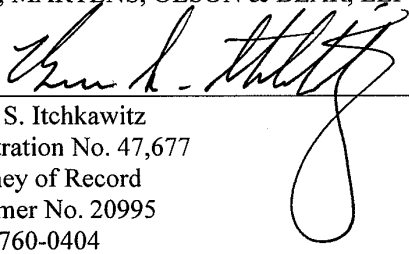
The Assignment from the inventors to the Assignee recorded in the United States
Patent and Trademark Office on July 17, 2006, at Reel 018104, and Frame 0964.

The undersigned is an agent of Customer Number 20995 and is authorized to act on behalf of the Assignee. Please recognize or change the correspondence address for the above-identified application to **Customer No. 20995**.

Respectfully submitted,

KNOBBE, MARTENS, OLSON & BEAR, LLP

Dated: 2/2/11

By: 
Bruce S. Itchkawitz
Registration No. 47,677
Attorney of Record
Customer No. 20995
(949) 760-0404

10500314
013111

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: **Mail** **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax **(571)-273-2885**

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

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20995 7590 02/02/2011

KNOBBE MARTENS OLSON & BEAR LLP
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Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/955,711	11/29/2010	Jeffrey C. Solomon	NETL18CPCPCCC	8026

TITLE OF INVENTION: CIRCUIT PROVIDING LOAD ISOLATION AND MEMORY DOMAIN TRANSLATION FOR MEMORY MODULE

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	\$1510	\$300	\$0	\$1810	05/02/2011

EXAMINER	ART UNIT	CLASS-SUBCLASS
SOFOCLEOUS, ALEXANDER	2824	365-230060

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. Use of a Customer Number is required.

2. For printing on the patent front page, list

- (1) the names of up to 3 registered patent attorneys or agents OR, alternatively,
- (2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1. Knobbe, Martens,

2. Olson & Bear, LLP

3. _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

Netlist, Inc.

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Irvine, CA

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

- ☒ Issue Fee
- ☒ Publication Fee (No small entity discount permitted)
- ☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)

- ☐ A check is enclosed.
- ☐ Payment by credit card. Form PTO-2038 is attached.
- ☒ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number 11-1410 (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)

- ☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.
- ☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____

Date February 9, 2011

Typed or printed name Bruce S. Itchkawitz

Registration No. 47,677

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants : Solomon et al.
Appl. No. : 12/955,711
Filed : November 29, 2010
For : CIRCUIT PROVIDING LOAD
ISOLATION AND MEMORY
DOMAIN TRANSLATION FOR
MEMORY MODULE
Examiner : Alexander Sofocleous
Conf. No. : 8026

Group Art Unit 2824

COMMENTS ON EXAMINER'S STATEMENT OF REASONS FOR ALLOWANCE

Mail Stop- ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Arlington, VA 22313-1450

Dear Sir:

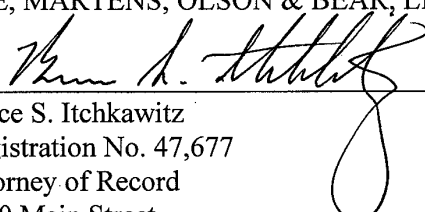
Applicants respectfully disagree with the Examiner's Statement of Reasons for Allowance to the extent that the features listed in the Examiner's Statement paraphrase or deviate from the claim language or are not present in all of the claims. For example, while page 4 of the Notice of Allowance refers to Claim 1 as reciting that "the circuit is configured to receive a set of signals," Claim 1 actually recites that "the circuit [is] configurable to receive a set of signals."

To the extent that there is any implication that the patentability of the claims rests on the recitation of a single feature, Applicants respectfully disagree with the Examiner's Statement because it is the combination of features that makes the claims patentable. Accordingly, Applicants submit that the claims of the present application are allowable because each of the claims recites a combination of features that are not anticipated or rendered obvious by the prior art.

Respectfully submitted,

KNOBBE, MARTENS, OLSON & BEAR, LLP

Dated: 2/11

By: 
Bruce S. Itchkawitz
Registration No. 47,677
Attorney of Record
2040 Main Street

Appl. No. : 12/955,711
Filed : November 29, 2010

Fourteenth Floor
Irvine, CA 92614
(949) 760-0404

10670641
020911

Electronic Patent Application Fee Transmittal				
Application Number:		12955711		
Filing Date:		29-Nov-2010		
Title of Invention:		CIRCUIT PROVIDING LOAD ISOLATION AND MEMORY DOMAIN TRANSLATION FOR MEMORY MODULE		
First Named Inventor/Applicant Name:		Jeffrey C. Solomon		
Filer:		Bruce S. Itchkawitz/Jessica Noda		
Attorney Docket Number:		NETL.18CPCPCCC		
Filed as Large Entity				
Utility under 35 USC 111(a) Filing Fees				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Utility Appl issue fee	1501	1	1510	1510
Publ. Fee- early, voluntary, or normal	1504	1	300	300

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				1810

Electronic Acknowledgement Receipt	
EFS ID:	9411814
Application Number:	12955711
International Application Number:	
Confirmation Number:	8026
Title of Invention:	CIRCUIT PROVIDING LOAD ISOLATION AND MEMORY DOMAIN TRANSLATION FOR MEMORY MODULE
First Named Inventor/Applicant Name:	Jeffrey C. Solomon
Customer Number:	20995
Filer:	Bruce S. Itchkawitz/Lori Larson
Filer Authorized By:	Bruce S. Itchkawitz
Attorney Docket Number:	NETL.18CPCPCCC
Receipt Date:	09-FEB-2011
Filing Date:	29-NOV-2010
Time Stamp:	18:18:24
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	\$1810
RAM confirmation Number	4971
Deposit Account	111410
Authorized User	KNOBBE MARTENS OLSON AND BEAR
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees) Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Issue Fee Payment (PTO-85B)	issue_fee.pdf	100548	no	1
			b8b07269664d3adc97a5b24f7c18f5f624fc a547		
Warnings:					
Information:					
2	Post Allowance Communication - Incoming	comments.pdf	51263	no	2
			ae37a9377746fd2a1a5e3848d4cdc926588 b18c6		
Warnings:					
Information:					
3	Fee Worksheet (PTO-875)	fee-info.pdf	32313	no	2
			dd9e962058509f04ce6b44c07e6ab892532 61b39		
Warnings:					
Information:					
Total Files Size (in bytes):			184124		
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					

Receipt date: 01/18/2011

12955711 - GAU: 2824

PTO/SB/08 Equivalent

INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(Multiple sheets used when necessary)</i> SHEET 3 OF 14	Application No.	12/955,711
	Filing Date	November 29, 2010
	First Named Inventor	Solomon et al.
	Art Unit	2824
	Examiner	Sofocleous, Alexander
	Attorney Docket No.	NETL.18CPCPCCC

U.S. PATENT DOCUMENTS					
Examiner Initials	Cite No.	Document Number Number - Kind Code (if known) Example: 1,234,567 B1	Publication Date MM-DD-YYYY	Name of Patentee or Applicant	Pages, Columns, Lines Where Relevant Passages or Relevant Figures Appear
	59	6,618,320	9/9/2003	Hasegawa et al.	
	60	6,621,496	9/16/2003	Ryan	
	61	6,625,081	9/23/2003	Roohparvar et al.	
	62	6,625,687	9/23/2003	Halbert et al.	
	63	6,636,935	10/21/2003	Ware et al.	
	64	6,646,949	11/11/2003	Ellis et al.	
	65	6,658,509	12/2/2003	Bonella et al.	
	66	6,674,684	1/6/2004	Shen	
	67	6,681,301	1/20/2004	Mehta et al.	
	68	6,683,372	1/27/2004	Wong et al.	
	69	6,705,877	3/1/2004	Li et al.	
	70	6,697,888	2/24/2004	Halbert et al.	
	71	~~6,717,855~~	4/6/2004	Lai <i>6,717,885</i>	
	72	6,738,880	5/18/2004	Lai et al.	
	73	6,742,098	5/25/2004	Halbert et al.	
	74	6,754,797	6/22/2004	Wu et al.	
	75	6,785,189	8/31/2004	Jacobs et al.	
	76	6,788,592	9/7/2004	Nakata et al.	
	77	6,807,125	10/19/2004	Coteus et al.	
	78	6,813,196	11/2/2004	Park et al.	
	79	6,834,014	12/21/2004	Yoo et al.	
	80	6,854,042	2/8/2005	Karabatsos	
	81	6,880,094	4/12/2005	LaBerge	
	82	6,889,304	5/3/2005	Perego et al.	
	83	6,912,615	6/28/2005	Nicolai	
	84	6,912,628	6/28/2005	Wicki et al.	
	85	6,925,028	8/2/2005	Hosokawa et al.	
	86	6,944,694	9/13/2005	Pax	
	87	6,950,366	9/27/2005	Lapidus et al.	

OP
2/23

Examiner Signature	/Alexander Sofocleous/	Date Considered	01/24/2011
*Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.			

T¹ - Place a check mark in this area when an English language Translation is attached.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /AGS/

Samsung Electronics Co., Ltd.

Ex. 1044, p. 196

Receipt date: 01/18/2011

12955711 - GAU: 2824

PTO/SB/08 Equivalent

INFORMATION DISCLOSURE STATEMENT BY APPLICANT	Application No.	12/955,711
	Filing Date	November 29, 2010
	First Named Inventor	Solomon et al.
	Art Unit	2824
(Multiple sheets used when necessary)		Examiner
SHEET 7 OF 14		Attorney Docket No.
		Sofocleous, Alexander
		NETL18CPCPCCC

U.S. PATENT DOCUMENTS					
Examiner Initials	Cite No.	Document Number Number - Kind Code (if known) Example: 1,234,567 B1	Publication Date MM-DD-YYYY	Name of Patentee or Applicant	Pages, Columns, Lines Where Relevant Passages or Relevant Figures Appear
	164	Request for <i>Inter Partes</i> Reexamination; Reexam App. No. 95/000,577 for U.S. Pat. No. 7,289,386 filed 10/20/2010	10/20/07	Bhakta et al.	
	165	Request for <i>Inter Partes</i> Reexamination; Reexam App. No. 95/000,578 for U.S. Pat. No. 7,619,912 filed 10/20/2010	11/20/09	Bhakta et al.	
	166	Request for <i>Inter Partes</i> Reexamination; Reexam App. No. 95/000,579 for U.S. Pat. No. 7,619,912 filed 10/21/2010	11/20/09	Bhakta et al.	

FOREIGN PATENT DOCUMENTS						
Examiner Initials	Cite No.	Foreign Patent Document Country Code-Number-Kind Code Example: JP 1234567 A1	Publication Date MM-DD-YYYY	Name of Patentee or Applicant	Pages, Columns, Lines Where Relevant Passages or Relevant Figures Appear	T ¹
	167	WO 1992/002879	2/20/1992	Du Pont Pixel Systems Limited		
	168	WO 1994/007242	3/31/1994	Atmel Corporation		
	169	WO 1995/034030	12/14/1995	Intel Corporation		
	170	WO 2002/058069	7/25/2002	Honeywell International Inc.		
	171	WO 2003/017283	2/27/2003	Micron Technology, Inc.		
	172	WO 2003/069484	8/21/2003	Micron Technology, Inc.		
	173	WO 2006/055497	5/26/2006	Intel Corporation		

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ¹
	174	"64 & 72 Pin Zip/Simm Sram Module", JEDEC, Standard No. 21-C, www.jedec.com/download/search/4_04_01.pdf , June 1997 pages 4.4.1-1.	
	175	"Bank Striping of Data Across Internal SDRAM Banks," IP.com, IPCOM000013697D, 2000.	
	176	"Distributed Memory Mapping," IP.com, IPCOM000014788D, 2000.	
	177	"Information Huawei or FPGA-Take Five," Electronic News, 2002, p. 24.	
	178	"Method for a high-performance DRAM address mapping mechanism," IP.com, IPCOM000008164D, 2002.	

Examiner Signature	/Alexander Sofocleous/	Date Considered	01/24/2011
*Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.			

T¹ - Place a check mark in this area when an English language Translation is attached.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /AGS/

Receipt date: 01/18/2011

12955711 - GAU: 2824

PTO/SB/08 Equivalent

INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(Multiple sheets used when necessary)</i> SHEET 5 OF 14	Application No.	12/955,711
	Filing Date	November 29, 2010
	First Named Inventor	Solomon et al.
	Art Unit	2824
	Examiner	Sofocleous, Alexander
	Attorney Docket No.	NETL.18CPCPCCC

U.S. PATENT DOCUMENTS

Examiner Initials	Cite No.	Document Number Number - Kind Code (if known) Example: 1,234,567 B1	Publication Date MM-DD-YYYY	Name of Patentee or Applicant	Pages, Columns, Lines Where Relevant Passages or Relevant Figures Appear
	117	7,346,750	3/18/2008	Ishikawa	
	118	7,356,639	~~12/23/2004~~	Perego et al. 04/2008	
	119	7,370,238	5/6/2008	Billick et al.	
	120	7,437,591	10/14/2008	Wong	
	121	7,471,538	12/1/2008	Hofstra	
	122	7,461,182	12/2/2008	Fukushima et al.	
	123	7,532,537	5/12/2009	Solomon et al.	
	124	7,619,912	11/17/2009	Bhakta et al.	
	125	7,636,274	12/22/2009	Solomon et al.	
	126	7,864,627	1/4/2011	Bhakta et al.	
	127	7,881,150	2/1/2011	Solomon et al.	
	128	RE 36229	6/15/1999	Cady	
	129	US 2001/0003198 A1	6/7/2001	Wu	
	130	US 2001/0052057	12/13/2001	Lai	
	131	US 2002/0088633	7/11/2002	Kong et al.	
	132	US 2003/0063514	4/3/2003	Faue	
	133	US 2003/0090359	5/2003	Ok, Seung Han	
	134	US 2003/0090879	5/15/2003	Doblar et al.	
	135	US 2003/0191995	10/9/2003	Abrosimov et al.	
	136	US 2003/0210575	11/13/2003	Seo et al.	
	137	US 2004/0000708	1/1/2004	Rapport et al.	
	138	US 2004/0037158	2/26/2004	Coteus et al.	
	139	US 2004/0201968	10/14/2004	Tafolla	
	140	US 2005/0036378	2/17/2005	Kawaguchi et al.	
	141	US 2005/0281096	12/22/2005	Bhakta et al.	
	142	US 2006/0044860	3/2/2006	Kinsley et al.	
	143	US 2006/0117152 A1	6/1/2006	Amidi	
	144	US 2006/0126369	6/15/2006	Raghuram	
	145	US 2006/0129755	6/15/2006	Raghuram	

Change(s) applied
to document,
/AJP/
2/24/2011

Examiner Signature	/Alexander Sofocleous/	Date Considered	01/24/2011
*Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.			

T¹ - Place a check mark in this area when an English language Translation is attached.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /AGS/

Samsung Electronics Co., Ltd.

Ex. 1044, p. 198



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/955,711	03/29/2011	7916574	NETL.18CPCPCCC	8026

20995 7590 03/09/2011
KNOBBE MARTENS OLSON & BEAR LLP
2040 MAIN STREET
FOURTEENTH FLOOR
IRVINE, CA 92614

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment is 0 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site <http://pair.uspto.gov> for additional applicants):

Jeffrey C. Solomon, Irvine, CA;
Jayesh R. Bhakta, Cerritos, CA;

Please Direct All Correspondence to Customer Number 20995

RESCISSION OF ANY PRIOR DISCLAIMERS AND REQUEST TO REVISIT ART

Applicant	: Solomon et al.
App. No	: 12/955,711
Filed	: November 29, 2010
For	: CIRCUIT PROVIDING LOAD ISOLATION AND MEMORY DOMAIN TRANSLATION FOR MEMORY MODULE
Examiner	: Sofocleous, Alexander
Art Unit	: 2824
Conf #	: 8026

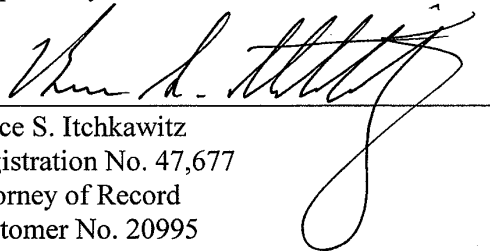
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

The claims of the present application are different and possibly broader in scope than the claims pursued in the parent application(s). To the extent any prior amendments or characterizations of the scope of any claim or referenced art could be construed as a disclaimer of any subject matter supported by the present disclosure, Applicant hereby rescinds and retracts such disclaimer. Accordingly, the references previously considered in the parent application(s) may need to be re-visited.

Please charge any additional fees, including any fees for additional extension of time, or credit overpayment to Deposit Account No. 11-1410.

Respectfully submitted,



Bruce S. Itchkawitz
Registration No. 47,677
Attorney of Record
Customer No. 20995
(949) 760-0404

Dated: March 15, 2011

10885948//031511

Electronic Acknowledgement Receipt	
EFS ID:	9665422
Application Number:	12955711
International Application Number:	
Confirmation Number:	8026
Title of Invention:	CIRCUIT PROVIDING LOAD ISOLATION AND MEMORY DOMAIN TRANSLATION FOR MEMORY MODULE
First Named Inventor/Applicant Name:	Jeffrey C. Solomon
Customer Number:	20995
Filer:	Bruce S. Itchkawitz/Sabrina Jacob
Filer Authorized By:	Bruce S. Itchkawitz
Attorney Docket Number:	NETL.18CPCPCCC
Receipt Date:	15-MAR-2011
Filing Date:	29-NOV-2010
Time Stamp:	17:48:01
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
------------------------	----

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Post Allowance Communication - Incoming	rescission.pdf	41127 a8c83e669247d7df69ca5133e2ccdd5e4e9b4978	no	1

Warnings:

Information:

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
12/955,711	11/29/2010	Jeffrey C. Solomon	NETL.18CPCPCCC

CONFIRMATION NO. 8026

20995
KNOBBE MARTENS OLSON & BEAR LLP
2040 MAIN STREET
FOURTEENTH FLOOR
IRVINE, CA 92614

PUBLICATION NOTICE



OC000000047145642

Title:CIRCUIT PROVIDING LOAD ISOLATION AND MEMORY DOMAIN TRANSLATION FOR MEMORY MODULE

Publication No.US-2011-0085406-A1

Publication Date:04/14/2011

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

The publication may be accessed through the USPTO's publically available Searchable Databases via the Internet at www.uspto.gov. The direct link to access the publication is currently <http://www.uspto.gov/patft/>.

The publication process established by the Office does not provide for mailing a copy of the publication to applicant. A copy of the publication may be obtained from the Office upon payment of the appropriate fee set forth in 37 CFR 1.19(a)(1). Orders for copies of patent application publications are handled by the USPTO's Office of Public Records. The Office of Public Records can be reached by telephone at (703) 308-9726 or (800) 972-6382, by facsimile at (703) 305-8759, by mail addressed to the United States Patent and Trademark Office, Office of Public Records, Alexandria, VA 22313-1450 or via the Internet.

In addition, information on the status of the application, including the mailing date of Office actions and the dates of receipt of correspondence filed in the Office, may also be accessed via the Internet through the Patent Electronic Business Center at www.uspto.gov using the public side of the Patent Application Information and Retrieval (PAIR) system. The direct link to access this status information is currently <http://pair.uspto.gov/>. Prior to publication, such status information is confidential and may only be obtained by applicant using the private side of PAIR.

Further assistance in electronically accessing the publication, or about PAIR, is available by calling the Patent Electronic Business Center at 1-866-217-9197.

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101



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 United States Patent and Trademark Office
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 P.O. Box 1450
 Alexandria, Virginia 22313-1450
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Bib Data Sheet

CONFIRMATION NO. 8026

SERIAL NUMBER 12/955,711	FILING OR 371(c) DATE 11/29/2010 RULE	CLASS 365	GROUP ART UNIT 2824	ATTORNEY DOCKET NO. NETL.18CPCPCCC
APPLICANTS Jeffrey C. Solomon, Irvine, CA; Jayesh R. Bhakta, Cerritos, CA;				
** CONTINUING DATA ***** This application is a CON of 12/629,827 12/02/2009 PAT 7881150 which is a CON of 12/408,652 03/20/2009 PAT 7636274 which is a CON of 11/335,875 01/19/2006 PAT 7532537 which is a CIP of 11/173,175 07/01/2005 PAT 7289386 which is a CIP of 11/075,395 03/07/2005 PAT 7286436 which claims benefit of 60/550,668 03/05/2004 and claims benefit of 60/575,595 05/28/2004 and claims benefit of 60/590,038 07/21/2004				
** FOREIGN APPLICATIONS *****				
IF REQUIRED, FOREIGN FILING LICENSE GRANTED ** 12/10/2010				
Foreign Priority claimed ☐ yes ☐ no 35 USC 119 (a-d) conditions ☐ yes ☐ no ☐ Met after met Allowance Verified and Acknowledged _____ Examiner's Signature Initials		STATE OR COUNTRY CA	SHEETS DRAWING 23	TOTAL CLAIMS 40
				INDEPENDENT CLAIMS 3
ADDRESS 20995				
TITLE CIRCUIT PROVIDING LOAD ISOLATION AND MEMORY DOMAIN TRANSLATION FOR MEMORY MODULE				
FILING FEE RECEIVED 2560	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:		☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit	



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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY. DOCKET NO.	TOT CLAIMS	IND CLAIMS
12/955,711	11/29/2010	2824	2560	NETL.18CPCPCCC	40	3

CONFIRMATION NO. 8026

CORRECTED FILING RECEIPT



OC000000054040452

20995
KNOBBE MARTENS OLSON & BEAR LLP
2040 MAIN STREET
FOURTEENTH FLOOR
IRVINE, CA 92614

Date Mailed: 05/03/2012

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Applicant(s)

Jeffrey C. Solomon, Irvine, CA;
Jayesh R. Bhakta, Cerritos, CA;

Assignment For Published Patent Application

Netlist, Inc., Irvine, CA

Power of Attorney: The patent practitioners associated with Customer Number 20995

Domestic Priority data as claimed by applicant

This application is a CON of 12/629,827 12/02/2009 PAT 7881150
which is a CON of 12/408,652 03/20/2009 PAT 7636274
which is a CON of 11/335,875 01/19/2006 PAT 7532537
which is a CIP of 11/173,175 07/01/2005 PAT 7289386
which is a CIP of 11/075,395 03/07/2005 PAT 7286436
which claims benefit of 60/550,668 03/05/2004
and claims benefit of 60/575,595 05/28/2004
and claims benefit of 60/590,038 07/21/2004

Foreign Applications (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see <http://www.uspto.gov> for more information.)

If Required, Foreign Filing License Granted: 12/10/2010

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 12/955,711**

Projected Publication Date: Not Applicable

Non-Publication Request: No

Early Publication Request: No
Title

CIRCUIT PROVIDING LOAD ISOLATION AND MEMORY DOMAIN TRANSLATION FOR MEMORY MODULE

Preliminary Class

365

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at <http://www.uspto.gov/web/offices/pac/doc/general/index.html>.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, <http://www.stopfakes.gov>. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4158).

LICENSE FOR FOREIGN FILING UNDER
Title 35, United States Code, Section 184
Title 37, Code of Federal Regulations, 5.11 & 5.15

GRANTED

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The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign Assets Control, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

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Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
12/955,711	11/29/2010	Jeffrey C. Solomon	NETL.000GEN

CONFIRMATION NO. 8026

POA ACCEPTANCE LETTER

20995
KNOBBE MARTENS OLSON & BEAR LLP
2040 MAIN STREET
FOURTEENTH FLOOR
IRVINE, CA 92614



Date Mailed: 05/10/2012

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 02/02/2011.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

/tkim/

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

REQUEST FOR CORRECTED FILING RECEIPT

Applicant	:	Solomon, et al.
Appl. No.	:	12/955,711
Filed	:	November 29, 2010
For	:	CIRCUIT PROVIDING LOAD ISOLATION AND MEMORY DOMAIN TRANSLATION FOR MEMORY MODULE
Art Unit	:	2824

Commissioner for Patents
P.O. Box 1450
Office of Initial Patent Examination
Customer Service Center
Alexandria, VA 22313-1450

Dear Sir:

Applicants hereby request that the Official Filing Receipt, a copy of which is enclosed, be corrected to reflect the accurate continuing data as claimed by the above-identified application. The Application Data Sheet as filed with the above-identified application on November 29, 2010 correctly listed the domestic priority data for the above-identified application. The Filing Receipt mailed by the USPTO on December 14, 2010 correctly listed the domestic priority data for the above-identified application. The issuance of the above-identified application as U.S. Pat. No. 7,916,574 on March 29, 2011 correctly listed the domestic priority data for the above-identified application. However, the "Corrected Filing Receipt" mailed by the USPTO on May 3, 2012 (more than one year after the patent issued) incorrectly excludes two U.S. provisional applications from the domestic priority data.

Appl. No. : 12/955,711
Filed : November 29, 2010

Applicants respectfully request that the continuing data be corrected to read:

The present application is a continuation of U.S. Pat. Appl. No. 12/629,827, filed December 2, 2009, which is a continuation of U.S. Pat. Appl. No. 12/408,652, filed March 20, 2009, which is a continuation of U.S. Pat. Appl. No. 11/335,875, filed January 19, 2006, **which claims the benefit of U.S. Provisional Appl. No. 60/645,087, filed January 19, 2005 and** which is a continuation-in-part of U.S. Pat. Appl. No. 11/173,175, filed July 1, 2005, **which claims the benefit of U.S. Provisional Appl. No. 60/588,244, filed July 15, 2004 and** which is a continuation-in-part of U.S. Pat. Appl. No. 11/075,395, filed March 7, 2005, which claims the benefit of U.S. Provisional Appl. No. 60/550,668, filed March 5, 2004, U.S. Provisional Appl. No. 60/575,595, filed May 28, 2004, and U.S. Provisional Appl. No. 60/590,038, filed July 21, 2004.

The following is enclosed as evidence of the proper priority:

- (X) A copy of the first page of the Specification listing the priority as filed.
- (X) A copy of the Application Data Sheet as filed.
- (X) A copy of the Official Filing Receipt dated December 14, 2010 showing the correct information.
- (X) A marked-up copy of the "Corrected Filing Receipt" showing the corrected information.

Respectfully submitted,

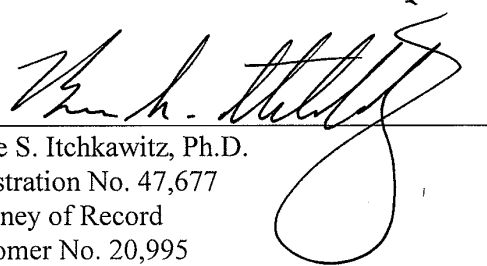
KNOBBE, MARTENS, OLSON & BEAR, LLP

Dated: _____

8/27/12

By: _____

Bruce S. Itchkawitz, Ph.D.
Registration No. 47,677
Attorney of Record
Customer No. 20,995
(949) 760-0404



13712827

**CIRCUIT PROVIDING LOAD ISOLATION AND MEMORY DOMAIN
TRANSLATION FOR MEMORY MODULE**

Cross-Reference to Related Applications

[0001] The present application is a continuation of U.S. Pat. Appl. No. 12/629,827, filed December 2, 2009, which is a continuation of U.S. Pat. Appl. No. 12/408,652, filed March 20, 2009, which is a continuation of U.S. Pat. Appl. No. 11/335,875, filed January 19, 2006, which claims the benefit of U.S. Provisional Appl. No. 60/645,087, filed January 19, 2005 and which is a continuation-in-part of U.S. Pat. Appl. No. 11/173,175, filed July 1, 2005, which claims the benefit of U.S. Provisional Appl. No. 60/588,244, filed July 15, 2004 and which is a continuation-in-part of U.S. Pat. Appl. No. 11/075,395, filed March 7, 2005, which claims the benefit of U.S. Provisional Appl. No. 60/550,668, filed March 5, 2004, U.S. Provisional Appl. No. 60/575,595, filed May 28, 2004, and U.S. Provisional Appl. No. 60/590,038, filed July 21, 2004. U.S. Pat. Appl. Nos. 12/629,827, 12/408,652, 11/335,875, 11/173,175, and 11/075,395 and U.S. Provisional Appl. Nos. 60/550,668, 60/575,595, 60/590,038, 60/588,244, and 60/645,087 are each incorporated in their entirety by reference herein.

Background of the Invention

Field of the Invention

[0002] The present invention relates generally to memory modules of a computer system, and more specifically to devices and methods for improving the performance, the memory capacity, or both, of memory modules.

Description of the Related Art

[0003] Certain types of memory modules comprise a plurality of dynamic random-access memory (DRAM) devices mounted on a printed circuit board (PCB). These memory modules are typically mounted in a memory slot or socket of a computer system (e.g., a server system or a personal computer) and are accessed by the processor of the computer system. Memory modules typically have a memory configuration with a unique combination of rows, columns, and banks which result in a total memory capacity for the memory module.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	NETL.18CPCPCCC
		Application Number	
Title of Invention	CIRCUIT PROVIDING LOAD ISOLATION AND MEMORY DOMAIN TRANSLATION FOR MEMORY MODULE		
The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76. This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.			

Secrecy Order 37 CFR 5.2

- ☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

Applicant Information:

Applicant 1				
Applicant Authority ☒ Inventor		☐ Legal Representative under 35 U.S.C. 117		☐ Party of Interest under 35 U.S.C. 118
Prefix	Given Name	Middle Name	Family Name	Suffix
	Jeffrey	C.	Solomon	
Residence Information (Select One) ☒ US Residency ☐ Non US Residency ☐ Active US Military Service				
City	Irvine	State/Province	CA	Country of Residence
				US
Citizenship under 37 CFR 1.41(b)		US		
Mailing Address of Applicant:				
Address 1		16 Silver Fir		
Address 2				
City	Irvine	State/Province	CA	
Postal Code	92604	Country	US	
Applicant 2				
Applicant Authority ☒ Inventor		☐ Legal Representative under 35 U.S.C. 117		☐ Party of Interest under 35 U.S.C. 118
Prefix	Given Name	Middle Name	Family Name	Suffix
	Jayesh	R.	Bhakta	
Residence Information (Select One) ☒ US Residency ☐ Non US Residency ☐ Active US Military Service				
City	Cerritos	State/Province	CA	Country of Residence
				US
Citizenship under 37 CFR 1.41(b)		US		
Mailing Address of Applicant:				
Address 1		12220 Rose Street		
Address 2				
City	Cerritos	State/Province	CA	
Postal Code	90703	Country	US	
All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the Add button.				
Add				

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below. For further information see 37 CFR 1.33(a). ☐ An Address is being provided for the correspondence Information of this application.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	NETL.18CPCPCCC	
		Application Number		
Title of Invention	CIRCUIT PROVIDING LOAD ISOLATION AND MEMORY DOMAIN TRANSLATION FOR MEMORY MODULE			
Customer Number	20995			
Email Address	efiling@kmob.com		Add Email	Remove Email

Application Information:

Title of the Invention	CIRCUIT PROVIDING LOAD ISOLATION AND MEMORY DOMAIN TRANSLATION FOR MEMORY MODULE		
Attorney Docket Number	NETL.18CPCPCCC	Small Entity Status Claimed ☐	
Application Type	Nonprovisional		
Subject Matter	Utility		
Suggested Class (if any)		Sub Class (if any)	
Suggested Technology Center (if any)			
Total Number of Drawing Sheets (if any)	23	Suggested Figure for Publication (if any)	

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)	
☐	Request Not to Publish. I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application has not and will not be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32). Enter either Customer Number or complete the Representative Name section below. If both sections are completed the Customer Number will be used for the Representative Information during processing.			
Please Select One:	☒ Customer Number	☐ US Patent Practitioner	☐ Limited Recognition (37 CFR 11.9)
Customer Number	20995		

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, or 365(c) or indicate National Stage entry from a PCT application. Providing this information in the application data sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78(a)(2) or CFR 1.78(a)(4), and need not otherwise be made part of the specification.			
Prior Application Status	Pending	Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
	Continuation of	12/629827	2009-12-02
Prior Application Status	Patented	Remove	

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	NETL.18CPCPCCC
		Application Number	
Title of Invention	CIRCUIT PROVIDING LOAD ISOLATION AND MEMORY DOMAIN TRANSLATION FOR MEMORY MODULE		

Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
12/629827	Continuation of	12/408652	2009-03-20	7636274	2009-12-22
Prior Application Status		Patented Remove			
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
12/408652	Continuation of	11/335875	2006-01-19	7532537	2009-05-12
Prior Application Status		Expired Remove			
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)		
11/335875	non provisional of	60/645087	2005-01-19		
Prior Application Status		Patented Remove			
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
11/335875	Continuation in part of	11/173175	2005-07-01	7289386	2007-10-30
Prior Application Status		Expired Remove			
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)		
11/173175	non provisional of	60/588244	2004-07-15		
Prior Application Status		Patented Remove			
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
11/173175	Continuation in part of	11/075395	2005-03-07	7286436	2007-10-23
Prior Application Status		Expired Remove			
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)		
11/075395	non provisional of	60/550668	2004-03-05		
Prior Application Status		Expired Remove			
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)		
11/075395	non provisional of	60/575595	2004-05-28		
Prior Application Status		Expired Remove			
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)		
11/075395	non provisional of	60/590038	2004-07-21		
Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the Add button.					

Foreign Priority Information:

This section allows for the applicant to claim benefit of foreign priority and to identify any prior foreign application for which priority is not claimed. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55(a).			
Remove			
Application Number	Country ¹	Parent Filing Date (YYYY-MM-DD)	Priority Claimed
			☐ Yes ☐ No

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	NETL.18CPCPCCC
		Application Number	
Title of Invention	CIRCUIT PROVIDING LOAD ISOLATION AND MEMORY DOMAIN TRANSLATION FOR MEMORY MODULE		

Additional Foreign Priority Data may be generated within this form by selecting the **Add** button.

Assignee Information:

Providing this information in the application data sheet does not substitute for compliance with any requirement of part 3 of Title 37 of the CFR to have an assignment recorded in the Office.

Assignee 1

If the Assignee is an Organization check here. ☒

Organization Name Netlist, Inc.

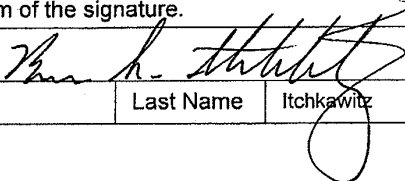
Mailing Address Information:

Address 1		51 Discovery #150	
Address 2			
City	Irvine	State/Province	CA
Country	US	Postal Code	92618
Phone Number		Fax Number	
Email Address			

Additional Assignee Data may be generated within this form by selecting the **Add** button.

Signature:

A signature of the applicant or representative is required in accordance with 37 CFR 1.33 and 10.18. Please see 37 CFR 1.4(d) for the form of the signature.

Signature			Date (YYYY-MM-DD)	2010-11-29	
First Name	Bruce	Last Name	Itchkawitz	Registration Number	47677

This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
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7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY. DOCKET NO	TOT CLAIMS	IND CLAIMS
12/955,711	11/29/2010	2827	0.00	NETL18CPCPCCC	40	3

CONFIRMATION NO. 8026

FILING RECEIPT



OC000000044902175

20995

KNOBBE MARTENS OLSON & BEAR LLP
2040 MAIN STREET
FOURTEENTH FLOOR
IRVINE, CA 92614

Date Mailed: 12/14/2010

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Applicant(s)

Jeffrey C. Solomon, Irvine, CA;
Jayesh R. Bhakta, Cerritos, CA;

Assignment For Published Patent Application

Netlist, Inc., Irvine, CA

Power of Attorney: None

Domestic Priority data as claimed by applicant

This application is a CON of 12/629,827 12/02/2009
which is a CON of 12/408,652 03/20/2009 PAT 7,636,274
which is a CON of 11/335,875 01/19/2006 PAT 7,532,537
which claims benefit of 60/645,087 01/19/2005
and is a CIP of 11/173,175 07/01/2005 PAT 7,289,386
which claims benefit of 60/588,244 07/15/2004
and is a CIP of 11/075,395 03/07/2005 PAT 7,286,436
which claims benefit of 60/550,668 03/05/2004
and claims benefit of 60/575,595 05/28/2004
and claims benefit of 60/590,038 07/21/2004

Foreign Applications

If Required, Foreign Filing License Granted: 12/10/2010

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 12/955,711**

Projected Publication Date: To Be Determined - pending completion of Missing Parts

page 1 of 3

Samsung Electronics Co., Ltd.

Ex. 1044, p. 217

Non-Publication Request: No

Early Publication Request: No
Title

CIRCUIT PROVIDING LOAD ISOLATION AND MEMORY DOMAIN TRANSLATION FOR MEMORY
MODULE

Preliminary Class

365

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

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NOT GRANTED

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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY. DOCKET NO.	TOT CLAIMS	IND CLAIMS
12/955,711	11/29/2010	2824	2560	NETL18CPCPCCC	40	3

CONFIRMATION NO. 8026

CORRECTED FILING RECEIPT



0000000054040452

20995
KNOBBE MARTENS OLSON & BEAR LLP
2040 MAIN STREET
FOURTEENTH FLOOR
IRVINE, CA 92614

Date Mailed: 05/03/2012

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Applicant(s)

Jeffrey C. Solomon, Irvine, CA;
Jayesh R. Bhakta, Cerritos, CA;

Assignment For Published Patent Application

Netlist, Inc., Irvine, CA

Power of Attorney: The patent practitioners associated with Customer Number 20995

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which is a CON of 12/408,652 03/20/2009 PAT 7636274 *which claims benefit of 60/645,087 01/19/2005*
which is a CON of 11/335,875 01/19/2006 PAT 7532537
which is a CIP of 11/173,175 07/01/2005 PAT 7289386
which is a CIP of 11/075,395 03/07/2005 PAT 7286436 *which claims benefit of 60/588,244 07/15/2004*
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If Required, Foreign Filing License Granted: 12/10/2010

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 12/955,711**

Projected Publication Date: Not Applicable

Non-Publication Request: No

page 1 of 3

Samsung Electronics Co., Ltd.

Ex. 1044, p. 220

Early Publication Request: No

Title

CIRCUIT PROVIDING LOAD ISOLATION AND MEMORY DOMAIN TRANSLATION FOR MEMORY
MODULE

Preliminary Class

365

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NOT GRANTED

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Electronic Acknowledgement Receipt	
EFS ID:	13591718
Application Number:	12955711
International Application Number:	
Confirmation Number:	8026
Title of Invention:	CIRCUIT PROVIDING LOAD ISOLATION AND MEMORY DOMAIN TRANSLATION FOR MEMORY MODULE
First Named Inventor/Applicant Name:	Jeffrey C. Solomon
Customer Number:	20995
Filer:	Bruce S. Itchkawitz/ThuyQuyen Nguyen
Filer Authorized By:	Bruce S. Itchkawitz
Attorney Docket Number:	NETL.18CPCPCCC
Receipt Date:	27-AUG-2012
Filing Date:	29-NOV-2010
Time Stamp:	12:41:36
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Request for Corrected Filing Receipt	Corrected_FR.pdf	850792 c21e95dd279d375f8a2e6b03fab22091910 ddcce	no	14

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If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.



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12/955,711	11/29/2010	2824	2560	NETL.18CPCPCCC	40	3

CONFIRMATION NO. 8026

CORRECTED FILING RECEIPT



OC000000056266450

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KNOBBE MARTENS OLSON & BEAR LLP
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FOURTEENTH FLOOR
IRVINE, CA 92614

Date Mailed: 09/05/2012

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Applicant(s)

Jeffrey C. Solomon, Irvine, CA;
Jayesh R. Bhakta, Cerritos, CA;

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Netlist, Inc., Irvine, CA

Power of Attorney: The patent practitioners associated with Customer Number 20995

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Projected Publication Date: Not Applicable

Non-Publication Request: No

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**REVOCATION
AND
GENERAL POWER OF ATTORNEY**

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

The undersigned is an empowered representative of the Assignee and hereby appoints the registrant, Jamie J. Zheng, Customer No. 79141, as attorney to represent the Assignee before the United States Patent and Trademark Office (USPTO) in connection with the patent assigned to the Assignee according to the USPTO assignment records or assignment documents supplied with the accompanying Statement Under 37 CFR § 3.73(b). This appointment is to be to the exclusion of the inventor(s) and his attorney(s) in accordance with the provisions of 37 CFR § 3.71.

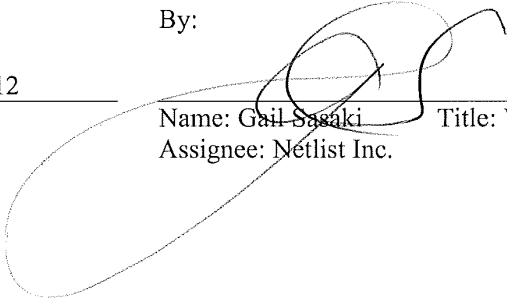
Submission of this paper in connection with any matter of the below named assignee, together with a statement under 37 CFR 3.73(b), shall serve to revoke any previous powers of attorneys in that matter.

A Statement under 37 CFR § 3.73(b) is attached setting forth a full chain of title for the subject patent owned by the Assignee named below.

Please recognize or change the correspondence address for the patent identified in the attached Statement to Customer No. 79141.

By:

Date: October 1, 2012


Name: Gail Sasaki Title: Vice President and CFO
Assignee: Netlist Inc.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

STATEMENT UNDER 37 CFR 3.73(b)Applicant/Patent Owner: Netlist, Inc.Application No./Patent No.: 7,916,574Filed/Issue Date: 29-Mar-2011

Titled:

CIRCUIT PROVIDING LOAD ISOLATION AND MEMORY DOMAIN TRANSLATION FOR MEMORY MODULE

Netlist, Inc., a Corporation

(Name of Assignee)

(Type of Assignee, e.g., corporation, partnership, university, government agency, etc.)

states that it is:

1. ☒ the assignee of the entire right, title, and interest in;
2. ☐ an assignee of less than the entire right, title, and interest in
(The extent (by percentage) of its ownership interest is _____ %); or
3. ☐ the assignee of an undivided interest in the entirety of (a complete assignment from one of the joint inventors was made)

the patent application/patent identified above, by virtue of either:

- A. ☒ An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel 018104, Frame 0964, or for which a copy therefore is attached.

OR

- B. ☐ A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as follows:

1. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

2. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

3. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

☐ Additional documents in the chain of title are listed on a supplemental sheet(s).

- ☒ As required by 37 CFR 3.73(b)(1)(i), the documentary evidence of the chain of title from the original owner to the assignee was, or concurrently is being, submitted for recordation pursuant to 37 CFR 3.11.

[NOTE: A separate copy (*i.e.*, a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, to record the assignment in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

Signature

Gail Sasaki

Printed or Typed Name

October 1, 2012

Date

VP and CFO

Title

This collection of information is required by 37 CFR 3.73(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Electronic Acknowledgement Receipt	
EFS ID:	13925349
Application Number:	12955711
International Application Number:	
Confirmation Number:	8026
Title of Invention:	CIRCUIT PROVIDING LOAD ISOLATION AND MEMORY DOMAIN TRANSLATION FOR MEMORY MODULE
First Named Inventor/Applicant Name:	Jeffrey C. Solomon
Customer Number:	20995
Filer:	Jamie Jie Zheng
Filer Authorized By:	
Attorney Docket Number:	NETL.18CPCPCCC
Receipt Date:	05-OCT-2012
Filing Date:	29-NOV-2010
Time Stamp:	18:32:05
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Power of Attorney	poa7916574.pdf	233711	no	2
			4aa886c52678401d93a4d27d27ba412d5a390dd2		

Warnings:

The page size in the PDF is too large. The pages should be 8.5 x 11 or A4. If this PDF is submitted, the pages will be resized upon entry into the Image File Wrapper and may affect subsequent processing

Information:

Total Files Size (in bytes):

233711

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
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Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
12/955,711	11/29/2010	Jeffrey C. Solomon	

79141
The Law Office of Jamie Zheng, Ph.D Esq.
P.O. Box 60573
Palo Alto, CA 94306

CONFIRMATION NO. 8026
POA ACCEPTANCE LETTER



Date Mailed: 10/23/2012

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 10/05/2012.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

/jtfitzhugh sr/

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101



UNITED STATES PATENT AND TRADEMARK OFFICE

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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
12/955,711	11/29/2010	Jeffrey C. Solomon	NETL.18CPCPCCC

CONFIRMATION NO. 8026

POWER OF ATTORNEY NOTICE

20995
KNOBBE MARTENS OLSON & BEAR LLP
2040 MAIN STREET
FOURTEENTH FLOOR
IRVINE, CA 92614



Date Mailed: 10/23/2012

NOTICE REGARDING CHANGE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 10/05/2012.

- The Power of Attorney to you in this application has been revoked by the assignee who has intervened as provided by 37 CFR 3.71. Future correspondence will be mailed to the new address of record(37 CFR 1.33).

/jtfitzhugh sr/

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

Docket No.: NETL018CPCPCCC

Customer No. 79141

ASSERTION OF ENTITLEMENT TO SMALL ENTITY STATUS UNDER 37 CFR 1.27

Applicant : Sonomon et al
App. No. : 12/955,711
Filed : November 29, 2010
For : CIRCUIT PROVIDING LOAD
ISOLATION AND MEMORY DOMAIN
TRANSLATION FOR MEMORY
MODULE
Examiner : SOFOCLEOUS, ALEXANDER
Art Unit : 2827
Conf. No. : 8026
Docket No. : NETL018CPCPCCC

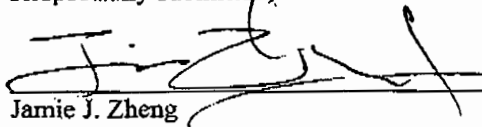
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

The Assignee, Netlist, Inc., of all rights and title to the above-identified patent is a small entity concern as defined in 37 C.F.R. 1.27(a). Assertion of entitlement to small entity status under 37 C.F.R. 1.27(c) is hereby made in this patent.

Applicants acknowledge the duty to file notification of a loss of entitlement to small entity status in the patent prior to paying, or at the time of paying, any maintenance fee due after the date on which status as a small entity is no longer appropriate.

Respectfully submitted,

Date: September 25, 2014
Jamie J. Zheng
Customer No. 7914151167
(Reg. No.)



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY.DOCKET NO./TITLE	REQUEST ID
12/955,711	11/29/2010	Jeffrey C. Solomon	129980-5013US	67129

Acknowledgement of Loss of Entitlement to Entity Status Discount

The entity status change request below filed through Private PAIR on 07/06/2018 has been accepted.

CERTIFICATIONS:

Change of Entity Status:

☒ Applicant changing to regular undiscounted fee status.

NOTE: Checking this box will be taken to be notification of loss of entitlement to small or micro entity status, as applicable.

This portion must be completed by the signatory or signatories making the entity status change in accordance with 37 CFR 1.4(d)(4).

Signature:	/Jamie J. Zheng/
Name:	Jamie J. Zheng
Registration Number:	51167