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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	NETL.018P2C7
	Application Number	
Title of Invention	LOAD-REDUCING CIRCUIT FOR MEMORY MODULE	

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Title of Invention	LOAD-REDUCING CIRCUIT FOR MEMORY MODULE	

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Title of the Invention	LOAD-REDUCING CIRCUIT FOR MEMORY MODULE		
Attorney Docket Number	NETL.018P2C7	**Small Entity Status Claimed**	☒
Application Type	Nonprovisional		
Subject Matter	Utility		
Suggested Class (if any)		**Sub Class (if any)**	
Suggested Technology Center (if any)			
Total Number of Drawing Sheets (if any)	23	**Suggested Figure for Publication (if any)**	8D

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☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)
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Prior Application Status	Pending		Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
	Continuation of	13287081	2011-11-01

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	NETL.018P2C7
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Prior Application Status	Patented				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
13287081	Continuation of	13032470	2011-02-22	8081536	2011-12-20
Prior Application Status	Patented				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
13032470	Continuation of	12955711	2010-11-29	7916574	2011-03-29
Prior Application Status	Patented				Remove
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12955711	Continuation of	12629827	2009-12-02	7881150	2011-02-01
Prior Application Status	Patented				Remove
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12629827	Continuation of	12408652	2009-03-20	7636274	2009-12-22
Prior Application Status	Patented				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
12408652	Continuation of	11335875	2006-01-19	7532537	2009-05-12
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11335875	non provisional of	60645087	2005-01-19		
Prior Application Status	Patented				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
11335875	Continuation in part of	11173175	2005-07-01	7289386	2007-10-30
Prior Application Status	Expired				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)		
11173175	non provisional of	60588244	2004-07-15		
Prior Application Status	Patented				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
11173175	Continuation in part of	11075395	2005-03-07	7286436	2007-10-23
Prior Application Status	Expired				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)		
11075395	non provisional of	60550668	2004-03-05		
Prior Application Status	Expired				Remove
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11075395	non provisional of	60575595	2004-05-28		

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Title of Invention	LOAD-REDUCING CIRCUIT FOR MEMORY MODULE	

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11075395	non provisional of	60590038	2004-07-21

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Clear

(•) Assignee	( ) Legal Representative under 35 U.S.C. 117	( ) Joint Inventor
( ) Person to whom the inventor is obligated to assign.	( ) Person who shows sufficient proprietary interest	

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Name of the Deceased or Legally Incapacitated Inventor :

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First Name	Jamie	Last Name	Zheng	Registration Number	51167

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LOAD-REDUCING CIRCUIT FOR MEMORY MODULE

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] The present application is a continuation of U.S. Pat. Appl. No. 13/287,081, filed November 1, 2011, which is a continuation of U.S. Pat. Appl. No. 13/032,470, filed February 22, 2011 and issued as U.S. Pat. No. 8,081,536, which is a continuation of U.S. Pat. Appl. No. 12/955,711, filed November 29, 2010 and issued as U.S. Pat. No. 7,916,574, which is a continuation of U.S. Pat. Appl. No. 12/629,827, filed December 2, 2009 and issued as U.S. Pat. No. 7,881,150, which is a continuation of U.S. Pat. Appl. No. 12/408,652, filed March 20, 2009 and issued as U.S. Pat. No. 7,636,274, which is a continuation of U.S. Pat. Appl. No. 11/335,875, filed January 19, 2006 and issued as U.S. Pat. No. 7,532,537, which claims the benefit of U.S. Provisional Appl. No. 60/645,087, filed January 19,2005 and which is a continuation-in-part of U.S. Pat. Appl. No. 11/173,175, filed July 1,2005 and issued as U.S. Pat. No. 7,289,386, which claims the benefit of U.S. Provisional Appl. No. 60/588,244, filed July 15, 2004 and which is a continuation-in-part of U.S. Pat. Appl. No. 11/075,395, filed March 7, 2005 and issued as U.S. Pat. No. 7,286,436, which claims the benefit of U.S. Provisional Appl. No. 60/550,668, filed March 5, 2004, U.S. Provisional Appl. No. 60/575,595, filed May 28, 2004, and U.S. Provisional Appl. No. 60/590,038, filed July 21, 2004. U.S. Pat. Appl. Nos. 13/287,081, 13/032,470, 12/955,711, 12/629,827, 12/408,652, 11/335,875, 11/173,175, and 11/075,395, and U.S. Provisional Appl. Nos. 60/550,668, 60/575,595, 60/590,038, 60/588,244, and 60/645,087 are each incorporated in its entirety by reference herein.

BACKGROUND OF THE INVENTION FIELD OF THE INVENTION

[0002] The present invention relates generally to memory modules of a computer system, and more specifically to devices and methods for improving the performance, the memory capacity, or both, of memory modules. Description of the Related Art

[0003] Certain types of memory modules comprise a plurality of dynamic random-access memory (DRAM) devices mounted on a printed circuit board (PCB). These memory modules are typically mounted in a memory slot or socket of a computer system (e.g., a server system or a personal computer) and are accessed by the processor of the

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computer system. Memory modules typically have a memory configuration with a unique combination of rows, columns, and banks which result in a total memory capacity for the memory module.

[0004] For example, a 512-Megabyte memory module (termed a "512-MB" memory module, which actually has 2^{29} or 536,870,912 bytes of capacity) will typically utilize eight 512-Megabit DRAM devices (each identified as a "512-Mb" DRAM device, each actually having 2^{29} or 536,870,912 bits of capacity). The memory cells (or memory locations) of each 512-Mb DRAM device can be arranged in four banks, with each bank having an array of 2^{24} (or 16,777,216) memory locations arranged as 2^{13} rows and 2^{11} columns, and with each memory location having a width of 8 bits. Such DRAM devices with 64M 8-bit-wide memory locations (actually with four banks of 2^{27} or 134,217,728 one-bit memory cells arranged to provide a total of 2^{26} or 67,108,864 memory locations with 8 bits each) are identified as having a "64Mb x 8" or "64M x 8-bit" configuration, or as having a depth of 64M and a bit width of 8. Furthermore, certain commercially-available 512-MB memory modules are termed to have a "64M x 8-byte" configuration or a "64M x 64-bit" configuration with a depth of 64M and a width of 8 bytes or 64 bits.

[0005] Similarly, a 1-Gigabyte memory module (termed a "1-GB" memory module, which actually has 2^{30} or 1,073,741,824 bytes of capacity) can utilize eight 1-Gigabit DRAM devices (each identified as a "1-Gb" DRAM device, each actually having 2^{30} or 1,073,741,824 bits of capacity). The memory locations of each 1-Gb DRAM device can be arranged in four banks, with each bank having an array of memory locations with 2^{14} rows and 2^{11} columns, and with each memory location having a width of 8 bits. Such DRAM devices with 128M 8-bit-wide memory locations (actually with a total of 2^{27} or 134,217,728 memory locations with 8 bits each) are identified as having a "128Mb x 8" or "128M x 8-bit" configuration, or as having a depth of 128M and a bit width of 8. Furthermore, certain commercially-available 1-GB memory modules are identified as having a "128M x 8-byte" configuration or a "128M x 64-bit" configuration with a depth of 128M and a width of 8 bytes or 64 bits.

[0006] The commercially-available 512-MB (64M x 8-byte) memory modules and the 1-GB (128M x 8-byte) memory modules described above are typically used in

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computer systems (e.g., personal computers) which perform graphics applications since such "x 8" configurations are compatible with data mask capabilities often used in such graphics applications. Conversely, memory modules with "x 4" configurations are typically used in computer systems such as servers which are not as graphics-intensive. Examples of such commercially available "x 4" memory modules include, but are not limited to, 512-MB (128M x 4-byte) memory modules comprising eight 512-Mb (128Mb x 4) memory devices.

[0007] The DRAM devices of a memory module are generally arranged as ranks or rows of memory, each rank of memory generally having a bit width. For example, a memory module in which each rank of the memory module is 64 bits wide is described as having an "x 64" organization. Similarly, a memory module having 72-bit-wide ranks is described as having an "x 72" organization.

[0008] The memory capacity of a memory module increases with the number of memory devices. The number of memory devices of a memory module can be increased by increasing the number of memory devices per rank or by increasing the number of ranks. For example, a memory module with four ranks has double the memory capacity of a memory module with two ranks and four times the memory capacity of a memory module with one rank. Rather than referring to the memory capacity of the memory module, in certain circumstances, the memory density of the memory module is referred to instead.

[0009] During operation, the ranks of a memory module are selected or activated by address and command signals that are received from the processor. Examples of such address and command signals include, but are not limited to, rank-select signals, also called chip-select signals. Most computer and server systems support one-rank and two-rank memory modules. By only supporting one-rank and two-rank memory modules, the memory density that can be incorporated in each memory slot is limited.

[0010] Various aspects of the design of a memory module impose limitations on the size of the memory arrays of the memory module. Certain such aspects are particularly important for memory modules designed to operate at higher frequencies. Examples of such aspects include, but are not limited to, memory device (e.g., chip) densities, load fan-out, signal integrity, available rank selects, power dissipation, and thermal profiles.

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SUMMARY OF THE INVENTION

[0011] In certain embodiments, a circuit is mountable on a memory module that includes a plurality of memory devices and operable in a computer system to perform memory operations in response to memory commands from a memory controller. The circuit comprises a register device configured to receive a set of input control/address signals associated with a respective memory command (e.g., a read command or a write command) from the memory controller and to generate a set of output control/address signals in response to the set of input control/address signals. The set of output control/address signals are provided to the plurality of memory devices. The circuit further comprises logic to monitor the memory commands from the memory controller and to selectively isolate one or more first memory devices among the plurality of memory devices from the memory controller in response to the respective memory command so as to reduce a load of the memory module to the computer system while one or more second memory devices among the plurality of memory devices are communicating with the memory controller in response to the set of output control/address signals.

[0012] In certain embodiments, the circuit further comprises DQ-DQS paths, and the logic selectively isolates one or more first memory devices by disabling at least one first group of DQ-DQS paths so as to isolate the one or more first memory devices. In certain embodiments, the logic is further configured to enable at least one second group of DQ-DQS paths in response to the respective memory command so as to allow the one or more second memory devices to communicate data with the memory controller in response to the output control/address signals. In certain embodiments, the logic element includes a buffer circuit to electrically and selectively isolate the one or more first memory devices from the memory controller and to selectively allow one or more second memory devices to communicate data with the memory controller, the buffer circuit adding a time delay (e.g., one clock cycle) to a data signal from the one or more second memory devices to the memory controller. In certain embodiments, the logic provides functions of a data path multiplexer/demultiplexer using the time delay. In certain embodiments, the logic is further configured to translate between a system memory domain and a physical memory device domain by generating a greater number of output control/address signals than the number of input control/address signals in response to the respective memory command. In certain embodiments, the logic

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receives one or more input chip select signals associated with the respective memory command, the one or more input chip select signals being less in number than chip-select signals in the output control/address signals.

[0013] In certain embodiments, a method of operating a circuit in a memory module comprises receiving a set of input control/address signals associated with a respective memory command from the memory controller, generating a set of output control/address signals in response to the set of input control/address signals, and providing the set of output control/address signals to a plurality of memory devices operable to perform memory operations in response to memory commands from a memory controller. The method further comprises monitoring the memory commands from the memory controller, and selectively isolating one or more first memory devices among the plurality of memory devices from the memory controller in response to the respective memory command so as to reduce a load of the memory module to the memory controller while one or more second memory devices among the plurality of memory devices are communicating with the memory controller in response to the set of output control/address signals. In certain embodiments, the method further comprises disabling at least one first group of DQ-DQS paths to isolate the one or more first memory devices and selectively enabling at least one second group of DQ-DQS paths to allow the one or more second memory devices to communicate data with the memory controller in response to the output control/address signals. In certain embodiments, the set of input control/address signals include at least one chip-select signal and the set of output control/address signals include a greater number of chip-select signals.

BRIEF DESCRIPTION OF THE DRAWINGS

[0014] Figure 1 schematically illustrates an example memory module in accordance with certain embodiments described herein.

[0015] Figure 2 schematically illustrates a circuit diagram of two memory devices of a conventional memory module.

[0016] Figure 3A and 3B schematically illustrate example memory modules having a circuit which selectively isolates one or both of the DQ data signal lines of the two

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memory devices from the computer system in accordance with certain embodiments described herein.

[0017] Figures 4A and 4B schematically illustrate example memory modules having a circuit which selectively isolates one or both of the DQ data signal lines of the two ranks of memory devices from the computer system in accordance with certain embodiments described herein.

[0018] Figures 5A-5D schematically illustrate example memory modules having a circuit comprising a logic element and one or more switches operatively coupled to the logic element in accordance with certain embodiments described herein.

[0019] Figure 6A shows an exemplary timing diagram of a gapless read burst for a back-to-back adjacent read condition from one memory device.

[0020] Figure 6B shows an exemplary timing diagram with an extra clock cycle between successive read commands issued to different memory devices for successive read accesses from different memory devices.

[0021] Figure 7 shows an exemplary timing diagram in which the last data strobe of memory device "a" collides with the pre-amble time interval of the data strobe of memory device "b."

[0022] Figures 8A-8D schematically illustrate circuit diagrams of example memory modules comprising a circuit which multiplexes the DQS data strobe signal lines from one another in accordance with certain embodiments described herein.

[0023] Figure 9A schematically illustrates an example memory module with four ranks of memory devices compatible with certain embodiments described herein.

[0024] Figure 9B schematically illustrates an example memory module with two ranks of memory devices compatible with certain embodiments described herein.

[0025] Figure 9C schematically illustrates another example memory module in accordance with certain embodiments described herein.

[0026] Figure 10A schematically illustrates an exemplary memory module which doubles the rank density in accordance with certain embodiments described herein.

[0027] Figure 10B schematically illustrates an exemplary circuit compatible with embodiments described herein.

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[0028] Figure 11A schematically illustrates an exemplary memory module which doubles number of ranks in accordance with certain embodiments described herein.

[0029] Figure 11B schematically illustrates an exemplary circuit compatible with embodiments described herein.

[0030] Figure 12 schematically illustrates an exemplary memory module in which a data strobe (DQS) pin of a first memory device is electrically connected to a DQS pin of a second memory device while both DQS pins are active.

[0031] Figure 13 is an exemplary timing diagram of the voltages applied to the two DQS pins due to non-simultaneous switching.

[0032] Figure 14 schematically illustrates another exemplary memory module in which a DQS pin of a first memory device is connected to a DQS pin of a second memory device.

[0033] Figure 15 schematically illustrates an exemplary memory module in accordance with certain embodiments described herein.

[0034] Figures 16A and 16B schematically illustrate a first side and a second side, respectively, of a memory module with eighteen 64M x 4 bit, DDR-1 SDRAM FBGA memory devices on each side of a 184-pin glass-epoxy printed circuit board.

[0035] Figures 17A and 17B schematically illustrate an exemplary embodiment of a memory module in which a first resistor and a second resistor are used to reduce the current flow between the first DQS pin and the second DQS pin.

[0036] Figure 18 schematically illustrates another exemplary memory module compatible with certain embodiments described herein.

[0037] Figure 19 schematically illustrates a particular embodiment of the memory module schematically illustrated by Figure 18.

Detailed Description of Example Embodiments

Load Isolation

[0038] Figure 1 schematically illustrates an example memory module 10 compatible with certain embodiments described herein. The memory module 10 is connectable to a memory controller 20 of a computer system (not shown). The memory module 10 comprises a plurality of memory devices 30, each memory device 30 having a

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corresponding load. The memory module 10 further comprises a circuit 40 electrically coupled to the plurality of memory devices 30 and configured to be electrically coupled to the memory controller 20 of the computer system. The circuit 40 selectively isolates one or more of the loads of the memory devices from the computer system. The circuit 40 comprises logic which translates between a system memory domain of the computer system and a physical memory domain of the memory module 10.

[0039] As used herein, the term "load" is a broad term which includes, without limitation, electrical load, such as capacitive load, inductive load, or impedance load. As used herein, the term "isolation" is a broad term which includes, without limitation, electrical separation of one or more components from another component or from one another. As used herein, the term "circuit" is a broad term which includes, without limitation, an electrical component or device, or a configuration of electrical components or devices which are electrically or electromagnetically coupled together (e.g., integrated circuits), to perform specific functions.

[0040] Various types of memory modules 10 are compatible with embodiments described herein. For example, memory modules 10 having memory capacities of 512-MB, 1-GB, 2-GB, 4-GB, 8-GB, as well as other capacities, are compatible with embodiments described herein. Certain embodiments described herein are applicable to various frequencies including, but not limited to 100 MHz, 200 MHz, 400 MHz, 800 MHz, and above. In addition, memory modules 10 having widths of 4 bytes, 8 bytes, 16 bytes, 32 bytes, or 32 bits, 64 bits, 128 bits, 256 bits, as well as other widths (in bytes or in bits), are compatible with embodiments described herein. In certain embodiments, the memory module 10 comprises a printed circuit board on which the memory devices 30 are mounted, a plurality of edge connectors configured to be electrically coupled to a corresponding plurality of contacts of a module slot of the computer system, and a plurality of electrical conduits which electrically couple the memory devices 30 to the circuit 40 and which electrically couple the circuit 40 to the edge connectors. Furthermore, memory modules 10 compatible with embodiments described herein include, but are not limited to, single in-line memory modules (SIMMs), dual in-line memory modules (DIMMs), small-outline DIMMs (SO-

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DIMMs), unbuffered DIMMs (UDIMMs), registered DIMMs (RDIMMs), fully-buffered DIMM (FBDIMM), rank-buffered DIMMs (RBDIMMs), mini-DIMMs, and micro-DIMMs.

[0041] Memory devices 30 compatible with embodiments described herein include, but are not limited to, random-access memory (RAM), dynamic random-access memory (DRAM), synchronous DRAM (SDRAM), and double-data-rate DRAM (e.g., SDR, DDR-1, DDR-2, DDR-3). In addition, memory devices 30 having bit widths of 4, 8, 16, 32, as well as other bit widths, are compatible with embodiments described herein. Memory devices 30 compatible with embodiments described herein have packaging which include, but are not limited to, thin small-outline package (TSOP), ball-grid-array (BGA), fine-pitch BGA (FBGA), micro-BGA (μBGA), mini-BGA (mBGA), and chip-scale packaging (CSP). Memory devices 30 compatible with embodiments described herein are available from a number of sources, including but not limited to, Samsung Semiconductor, Inc. of San Jose, California, Infineon Technologies AG of San Jose, California, and Micron Technology, Inc. of Boise, Idaho. Persons skilled in the art can select appropriate memory devices 30 in accordance with certain embodiments described herein.

[0042] In certain embodiments, the plurality of memory devices 30 comprises a first number of memory devices 30. In certain such embodiments, the circuit 40 selectively isolates a second number of the memory devices 30 from the computer system, with the second number less than the first number.

[0043] In certain embodiments, the plurality of memory devices 30 are arranged in a first number of ranks. For example, in certain embodiments, the memory devices 30 are arranged in two ranks, as schematically illustrated by Figure 1. In other embodiments, the memory devices 30 are arranged in four ranks. Other numbers of ranks of the memory devices 30 are also compatible with embodiments described herein.

[0044] In certain embodiments, the circuit comprises a logic element selected from a group consisting of: a programmable-logic device (PLD), an application-specific integrated circuit (ASIC), a field-programmable gate array (FPGA), a custom-designed semiconductor device, and a complex programmable-logic device (CPLD). In certain embodiments, the logic element of the circuit 40 is a custom device. Sources of logic elements compatible with embodiments described herein include, but are not limited to,

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Lattice Semiconductor Corporation of Hillsboro, Oregon, Altera Corporation of San Jose, California, and Xilinx Incorporated of San Jose, California. In certain embodiments, the logic element comprises various discrete electrical elements, while in certain other embodiments, the logic element comprises one or more integrated circuits.

[0045] In certain embodiments, the circuit 40 further comprises one or more switches which are operatively coupled to the logic element to receive control signals from the logic element. Examples of switches compatible with certain embodiments described herein include, but are not limited to, field-effect transistor (FET) switches, such as the SN74AUC1G66 single bilateral analog switch available from Texas Instruments, Inc. of Dallas, Texas.

[0046] Figure 2 schematically illustrates a circuit diagram of two memory devices 30a, 30b of a conventional memory module showing the interconnections between the DQ data signal lines 102a, 102b of the memory devices 30a, 30b and the DQS data strobe signal lines 104a, 104b of the memory devices 30a, 30b. Each of the memory devices 30a, 30b has a plurality of DQ data signal lines and a plurality of DQS data strobe signal lines, however, for simplicity, Figure 2 only illustrates a single DQ data signal line and a single DQS data strobe signal line for each memory device 30a, 30b. The DQ data signal lines 102a, 102b and the DQS data strobe signal lines 104a, 104b are typically conductive traces etched on the printed circuit board of the memory module. As shown in Figure 2, each of the memory devices 30a, 30b has their DQ data signal lines 102a, 102b electrically coupled to a common DQ line 112 and their DQS data strobe signal lines 104a, 104b electrically coupled to a common DQS line 114. The common DQ line 112 and the common DQS line 114 are electrically coupled to the memory controller 20 of the computer system. Thus, the computer system is exposed to the loads of both memory devices 30a, 30b concurrently.

[0047] In certain embodiments, the circuit 40 selectively isolates the loads of at least some of the memory devices 30 from the computer system. The circuit 40 of certain embodiments is configured to present a significantly reduced load to the computer system. In certain embodiments in which the memory devices 30 are arranged in a plurality of ranks, the circuit 40 selectively isolates the loads of some (e.g., one or more) of the ranks of the memory module 10 from the computer system. In certain other embodiments, the circuit 40

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selectively isolates the loads of all of the ranks of the memory module 10 from the computer system. For example, when a memory module 10 is not being accessed by the computer system, the capacitive load on the memory controller 20 of the computer system by the memory module 10 can be substantially reduced to the capacitive load of the circuit 40 of the memory module 10.

[0048] As schematically illustrated by Figures 3A and 3B, an example memory module 10 compatible with certain embodiments described herein comprises a circuit 40 which selectively isolates one or both of the DQ data signal lines 102a, 102b of the two memory devices 30a, 30b from the common DQ data signal line 112 coupled to the computer system. Thus, the circuit 40 selectively allows a DQ data signal to be transmitted from the memory controller 20 of the computer system to one or both of the DQ data signal lines 102a, 102b. In addition, the circuit 40 selectively allows one of a first DQ data signal from the DQ data signal line 102a of the first memory device 30a or a second DQ data signal from the DQ data signal line 102b of the second memory device 30b to be transmitted to the memory controller 20 via the common DQ data signal line 112 (see, e.g., triangles on the DQ and DQS lines of Figures 3A and 3B which point towards the memory controller). While various figures of the present application denote read operations by use of DQ and DQS lines which have triangles pointing towards the memory controller, certain embodiments described herein are also compatible with write operations (e.g., as would be denoted by triangles on the DQ or DQS lines pointing away from the memory controller).

[0049] For example, in certain embodiments, the circuit 40 comprises a pair of switches 120a, 120b on the DQ data signal lines 102a, 102b as schematically illustrated by Figure 3A. Each switch 120a, 120b is selectively actuated to selectively electrically couple the DQ data signal line 102a to the common DQ signal line 112, the DQ data signal line 102b to the common DQ signal line 112, or both DQ data signal lines 102a, 102b to the common DQ signal line 112. In certain other embodiments, the circuit 40 comprises a switch 120 electrically coupled to both of the DQ data signal lines 102a, 102b, as schematically illustrated by Figure 3B. The switch 120 is selectively actuated to selectively electrically couple the DQ data signal line 102a to the common DQ signal line 112, the DQ data signal line 102b to the common DQ signal line 112, or both DQ signal lines 102a, 102b to the

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common DQ signal line 112. Circuits 40 having other configurations of switches are also compatible with embodiments described herein. While each of the memory devices 30a, 30b has a plurality of DQ data signal lines and a plurality of DQS data strobe signal lines, Figures 3A and 3B only illustrate a single DQ data signal line and a single DQS data strobe signal line for each memory device 30a, 30b for simplicity. The configurations schematically illustrated by Figures 3A and 3B can be applied to all of the DQ data signal lines and DQS data strobe signal lines of the memory module 10.

[0050] In certain embodiments, the circuit 40 selectively isolates the loads of ranks of memory devices 30 from the computer system. As schematically illustrated in Figures 4A and 4B, example memory modules 10 compatible with certain embodiments described herein comprise a first number of memory devices 30 arranged in a first number of ranks 32. The memory modules 10 of Figures 4A and 4B comprises two ranks 32a, 32b, with each rank 32a, 32b having a corresponding set of DQ data signal lines and a corresponding set of DQS data strobe lines. Other numbers of ranks (e.g., four ranks) of memory devices 30 of the memory module 10 are also compatible with certain embodiments described herein. For simplicity, Figures 4A and 4B illustrate only a single DQ data signal line and a single DQS data strobe signal line from each rank 32.

[0051] The circuit 40 of Figure 4A selectively isolates one or more of the DQ data signal lines 102a, 102b of the two ranks 32a, 32b from the computer system. Thus, the circuit 40 selectively allows a DQ data signal to be transmitted from the memory controller 20 of the computer system to the memory devices 30 of one or both of the ranks 32a, 32b via the DQ data signal lines 102a, 102b. In addition, the circuit 40 selectively allows one of a first DQ data signal from the DQ data signal line 102a of the first rank 32a and a second DQ data signal from the DQ data signal line 102b of the second rank 32b to be transmitted to the memory controller 20 via the common DQ data signal line 112. For example, in certain embodiments, the circuit 40 comprises a pair of switches 120a, 120b on the DQ data signal lines 102a, 102b as schematically illustrated by Figure 4A. Each switch 120a, 120b is selectively actuated to selectively electrically couple the DQ data signal line 102a to the common DQ data signal line 112, the DQ data signal line 102b to the common DQ data signal line 112, or both DQ data signal lines 102a, 102b to the common DQ data signal line

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112. In certain other embodiments, the circuit 40 comprises a switch 120 electrically coupled to both of the DQ data signal lines 102a, 102b, as schematically illustrated by Figure 4B. The switch 120 is selectively actuated to selectively electrically couple the DQ data signal line 102a to the common DQ data signal line 112, the DQ data signal line 102b to the common DQ data signal line 112, or both DQ data signal lines 102a, 102b to the common DQ data signal line 112. Circuits 40 having other configurations of switches are also compatible with embodiments described herein.

[0052] In the example embodiments schematically illustrated by Figures 3A, 3B, 4A, and 4B, the circuit 40 comprises a logic element which is integral with and comprises the switches 120 which are coupled to the DQ data signal lines and the DQS data strobe signal lines. In certain such embodiments, each switch 120 comprises a data path multiplexer/demultiplexer. In certain other embodiments, the circuit 40 comprises a logic element 122 which is a separate component operatively coupled to the switches 120, as schematically illustrated by Figures 5A-5D. The one or more switches 120 are operatively coupled to the logic element 122 to receive control signals from the logic element 122 and to selectively electrically couple one or more data signal lines to a common data signal line. Example switches compatible with embodiments described herein include, but are not limited to field-effect transistor (FET) switches, such as the SN74AUC1G66 single bilateral analog switch available from Texas Instruments, Inc. of Dallas, Texas. Example logic elements 122 compatible with certain embodiments described herein include, but are not limited to, programmable-logic devices (PLD), application-specific integrated circuits (ASIC), field-programmable gate arrays (FPGA), custom-designed semiconductor devices, and complex programmable-logic devices (CPLD). Example logic elements 122 are available from Lattice Semiconductor Corporation of Hillsboro, Oregon, Altera Corporation of San Jose, California, and Xilinx Incorporated of San Jose, California.

[0053] In certain embodiments, the load isolation provided by the circuit 40 advantageously allows the memory module 10 to present a reduced load (e.g., electrical load, such as capacitive load, inductive load, or impedance load) to the computer system by selectively switching between the two ranks of memory devices 30 to which it is coupled. This feature is used in certain embodiments in which the load of the memory module 10 may

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otherwise limit the number of ranks or the number of memory devices per memory module. In certain embodiments, the memory module 10 operates as having a data path rank buffer which advantageously isolates the ranks of memory devices 30 of the memory module 10 from one another, from the ranks on other memory modules, and from the computer system. This data path rank buffer of certain embodiments advantageously provides DQ-DQS paths for each rank or sets of ranks of memory devices which are separate from one another, or which are separate from the memory controller of the computer system. In certain embodiments, the load isolation advantageously diminishes the effects of capacitive loading, jitter and other sources of noise. In certain embodiments, the load isolation advantageously simplifies various other aspects of operation of the memory module 10, including but not limited to, setup-and-hold time, clock skew, package skew, and process, temperature, voltage, and transmission line variations.

[0054] For certain memory module applications that utilize multiple ranks of memory, increased load on the memory bus can degrade speed performance. In certain embodiments described herein, selectively isolating the loads of the ranks of memory devices 30 advantageously decreases the load on the computer system, thereby allowing the computer system (e.g., server) to run faster with improved signal integrity. In certain embodiments, load isolation advantageously provides system memory with reduced electrical loading, thereby improving the electrical topology to the memory controller 20. In certain such embodiments, the speed and the memory density of the computer system are advantageously increased without sacrificing one for the other.

[0055] In certain embodiments, load isolation advantageously increases the size of the memory array supported by the memory controller 20 of the computer system. The larger memory array has an increased number of memory devices 30 and ranks of memory devices 30 of the memory module 10, with a corresponding increased number of chip selects. Certain embodiments described herein advantageously provide more system memory using fewer chip selects, thereby avoiding the chip select limitation of the memory controller.

[0056] An exemplary section of Verilog code corresponding to logic compatible with a circuit 40 which provides load isolation is listed below in Example 1. The exemplary

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code of Example 1 corresponds to a circuit 40 comprising six FET switches for providing load isolation to DQ and DQS lines.

[0057] Example 1:

```
//============================== declarations
  reg                   rasN_R, casN_R, weN_R;
  wire                  actv_cmd_R, pch_cmd_R, pch_all_cmd_R, ap_xfr_cmd_R_R;
  wire                  xfr_cmd_R,mrs_cmd,rd_cmd_R;
//------------------------- DDR 2 FET
  reg                   brs0N_R;                    // registered chip sel
  reg                   brs1N_R;                    // registered chip sel
  reg                   brs2N_R;                    // registered chip sel
  reg                   brs3N_R;                    // registered chip sel
  wire                  sel;
  wire                  sel_01;
  wire                  sel_23;
  wire                  rd_R1;
  wire                  wr_cmd_R,wr_R1;
  reg                   rd_R2,rd_R3,rd_R4,rd_R5;
  reg                   wr_R2,wr_R3,wr_R4,wr_R5;
  reg                   enfet1,enfet2,enfet3,enfet4,enfet5,enfet6;
  wire                  wr_01_R1,wr_23_R1;
  reg                   wr_01_R2,wr_01_R3,wr_01_R4;
  reg                   wr_23_R2,wr_23_R3,wr_23_R4;
  wire                  rodt0_a,rodt0_b;
//============================== logic
 always @(posedge clk_in)
        begin
                brs0N_R <= brs0_in_N;    // cs0
                brs1N_R <= brs1_in_N;    // cs1
                brs2N_R <= brs2_in_N;    // cs2
                brs3N_R <= brs3_in_N;    // cs3
                rasN_R  <= brras_in_N ;
                casN_R  <= brcas_in_N ;
                weN_R   <= bwe_in_N ;
        end
assign sel = ~brs0N_R | ~brs1N_R | ~brs2N_R | ~brs3N_R ;
assign sel_01 = ~brs0N_R | ~brs1N_R ;
assign sel_23 = ~brs2N_R | ~brs3N_R ;
assign actv_cmd_R = !rasN_R & casN_R & weN_R; // activate cmd
assign pch_cmd_R = !rasN_R & casN_R & !weN_R ;// pchg cmd
assign xfr_cmd_R = rasN_R & !casN_R;                  // xfr cmd
assign mrs_cmd = !rasN_R & !casN_R & !weN_R ;   // md reg set cmd
assign rd_cmd_R = rasN_R & !casN_R & weN_R ;   // read cmd
assign wr_cmd_R = rasN_R & !casN_R & !weN_R ; // write cmd
//---------------------------------------
assign    rd_R1 = sel & rd_cmd_R;  // rd cmd cyc 1
assign    wr_R1 = sel & wr_cmd_R;  // wr cmd cyc 1
//---------------------------------------
  always @(posedge clk_in)
        begin
                rd_R2 <= rd_R1 ;
                rd_R3 <= rd_R2;
```


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```
                rd_R4 <= rd_R3;
                rd_R5 <= rd_R4;
//              rd0_o_R6 <= rd0_o_R5;
                wr_R2 <= wr_R1 ;
                wr_R3 <= wr_R2;
                wr_R4 <= wr_R3;
                wr_R5 <= wr_R4;
        end
//---------------------------------------
assign  wr_01_R1 = sel_01 & wr_cmd_R;  // wr cmd cyc 1 for cs 2 & cs3
assign  wr_23_R1 = sel_23 & wr_cmd_R;  // wr cmd cyc 1 for cs 2 & cs3
 always @(posedge clk_in)
        begin
                wr_01_R2 <= wr_01_R1 ;
                wr_01_R3 <= wr_01_R2;
                wr_01_R4 <= wr_01_R3;
                wr_23_R2 <= wr_23_R1 ;
                wr_23_R3 <= wr_23_R2;
                wr_23_R4 <= wr_23_R3;
        end
assign  rodt0_ab = (rodt0)          // odt cmd from sys
                | (wr_23_R1)        // wr 1st cyc to other rnks (assume single dimm per channel)
                | (wr_23_R2)        // wr 2nd cyc to other rnks (assume single dimm per channel)
                | (wr_23_R3)        // wr 3rd cyc to other rnks (assume single dimm per channel)
                ;
assign  rodt1_ab = (rodt1)          // odt cmd from sys
                | (wr_01_R1)        // wr 1st cyc to other rnks (assume single dimm per channel)
                | (wr_01_R2)        // wr 2nd cyc to other rnks (assume single dimm per channel)
                | (wr_01_R3)        // wr 3rd cyc to other rnks (assume single dimm per channel)
                ;
//---------------------------------------
 always @(posedge clk_in)
        begin
  if (
    | (rd_R2)                       // pre-am rd
    | (rd_R3)                       // 1st cyc of rd brst (cl3)
    | (rd_R4)                       // 2nd cyc of rd brst (cl3)
    | (wr_R1)                       // pre-am wr
    | (wr_R2)                       // wr brst 1st cyc
    | (wr_R3)                       // wr brst 2nd cyc
     ) begin
                enfet1 <= 1'b1;     // enable fet
                enfet2 <= 1'b1;     // enable fet
                enfet3 <= 1'b1;     // enable fet
                enfet4 <= 1'b1;     // enable fet
                enfet5 <= 1'b1;     // enable fet
                enfet6 <= 1'b1;     // enable fet
      end
  else
      begin
                enfet1 <= 1'b0;     // disable fet
                enfet2 <= 1'b0;     // disable fet
                enfet3 <= 1'b0;     // disable fet
                enfet4 <= 1'b0;     // disable fet
                enfet5 <= 1'b0;     // disable fet
```


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```
                enfet6 <= 1'b0;          // disable fet
        end
    end
```

Back-to-Back Adjacent Read Commands

[0058] Due to their source synchronous nature, DDR SDRAM (e.g., DDR1, DDR2, DDR3) memory devices operate with a data transfer protocol which surrounds each burst of data strobes with a pre-amble time interval and a post-amble time interval. The pre-amble time interval provides a timing window for the receiving memory device to enable its data capture circuitry when a known valid level is present on the strobe signal to avoid false triggers of the memory device's capture circuit. The post-amble time interval provides extra time after the last strobe for this data capture to facilitate good signal integrity. In certain embodiments, when the computer system accesses two consecutive bursts of data from the same memory device, termed herein as a "back-to-back adjacent read," the post-amble time interval of the first read command and the pre-amble time interval of the second read command are skipped by design protocol to increase read efficiency. Figure 6A shows an exemplary timing diagram of this "gapless" read burst for a back-to-back adjacent read condition from one memory device.

[0059] In certain embodiments, when the second read command accesses data from a different memory device than does the first read command, there is at least one time interval (e.g., clock cycle) inserted between the data strobes of the two memory devices. This inserted time interval allows both read data bursts to occur without the post-amble time interval of the first read data burst colliding or otherwise interfering with the pre-amble time interval of the second read data burst. In certain embodiments, the memory controller of the computer system inserts an extra clock cycle between successive read commands issued to different memory devices, as shown in the exemplary timing diagram of Figure 6B for successive read accesses from different memory devices.

[0060] In typical computer systems, the memory controller is informed of the memory boundaries between the ranks of memory of the memory module prior to issuing read commands to the memory module. Such memory controllers can insert wait time intervals or clock cycles to avoid collisions or interference between back-to-back adjacent

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read commands which cross memory device boundaries, which are referred to herein as "BBARX."

[0061] In certain embodiments described herein in which the number of ranks 32 of the memory module 10 is doubled or quadrupled, the circuit 40 generates a set of output address and command signals so that the selection decoding is transparent to the computer system. However, in certain such embodiments, there are memory device boundaries of which the computer system is unaware, so there are occasions in which BBARX occurs without the cognizance of the memory controller 20 of the computer system. As shown in Figure 7, the last data strobe of memory device "a" collides with the pre-amble time interval of the data strobe of memory device "b," resulting in a "collision window."

[0062] Figures 8A-8D schematically illustrate circuit diagrams of example memory modules 10 comprising a circuit 40 which multiplexes the DQS data strobe signal lines 104a, 104b of two ranks 32a, 32b from one another in accordance with certain embodiments described herein. While the DQS data strobe signal lines 104a, 104b of Figures 8A-8D correspond to two ranks 32a, 32b of memory devices 30, in certain other embodiments, the circuit 40 multiplexes the DQS data strobe signal lines 104a, 104b corresponding to two individual memory devices 30a, 30b.

[0063] Figure 8A schematically illustrates a circuit diagram of an exemplary memory module 10 comprising a circuit 40 in accordance with certain embodiments described herein. In certain embodiments, BBARX collisions are avoided by a mechanism which electrically isolates the DQS data strobe signal lines 104a, 104b from one another during the transition from the first read data burst of one rank 32a of memory devices 30 to the second read data burst of another rank 32b of memory devices 30.

[0064] In certain embodiments, as schematically illustrated by Figure 8A, the circuit 40 comprises a first switch 130a electrically coupled to a first DQS data strobe signal line 104a of a first rank 32a of memory devices 30 and a second switch 130b electrically coupled to a second DQS data strobe signal line 104b of a second rank 32b of memory devices 30. In certain embodiments, the time for switching the first switch 130a and the second switch 130b is between the two read data bursts (e.g., after the last DQS data strobe of the read data burst of the first rank 32a and before the first DQS data strobe of the read data

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burst of the second rank 32b). During the read data burst for the first rank 32a, the first switch 130a is enabled. After the last DQS data strobe of the first rank 32a and before the first DQS data strobe of the second rank 32b, the first switch 130a is disabled and the second switch 130b is enabled.

[0065] As shown in Figure 8A, each of the ranks 32a, 32b otherwise involved in a BBARX collision have their DQS data strobe signal lines 104a, 104b selectively electrically coupled to the common DQS line 114 through the circuit 40. The circuit 40 of certain embodiments multiplexes the DQS data strobe signal lines 104a, 104b of the two ranks 32a, 32b of memory devices 30 from one another to avoid a BBARX collision.

[0066] In certain embodiments, as schematically illustrated by Figure 8B, the circuit 40 comprises a switch 130 which multiplexes the DQS data strobe signal lines 104a, 104b from one another. For example, the circuit 40 receives a DQS data strobe signal from the common DQS data strobe signal line 114 and selectively transmits the DQS data strobe signal to the first DQS data strobe signal line 104a, to the second DQS data strobe signal line 104b, or to both DQS data strobe signal lines 104a, 104b. As another example, the circuit 40 receives a first DQS data strobe signal from the first rank 32a of memory devices 30 and a second DQS data strobe signal from a second rank 32b of memory devices 30 and selectively switches one of the first and second DQS data strobe signals to the common DQS data strobe signal line 114.

[0067] In certain embodiments, the circuit 40 also provides the load isolation described above in reference to Figures 1-5. For example, as schematically illustrated by Figure 8C, the circuit 40 comprises both the switch 120 for the DQ data signal lines 102a, 102b and the switch 130 for the DQS data strobe signal lines 104a, 104b. While in certain embodiments, the switches 130 are integral with a logic element of the circuit 40, in certain other embodiments, the switches 130 are separate components which are operatively coupled to a logic element 122 of the circuit 40, as schematically illustrated by Figure 8D. In certain such embodiments, the control and timing of the switch 130 is performed by the circuit 40 which is resident on the memory module 10. Example switches 130 compatible with embodiments described herein include, but are not limited to field-effect transistor (FET) switches, such as the SN74AUC1G66 single bilateral analog switch available from Texas

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Instruments, Inc. of Dallas, Texas, and multiplexers, such as the SN74AUC2G53 2:1 analog multiplexer/demultiplexer available from Texas Instruments, Inc. of Dallas, Texas.

[0068] The circuit 40 of certain embodiments controls the isolation of the DQS data strobe signal lines 104a, 104b by monitoring commands received by the memory module 10 from the computer system and producing "windows" of operation whereby the appropriate switches 130 are activated or deactivated to enable and disable the DQS data strobe signal lines 104a, 104b to mitigate BBARX collisions. In certain other embodiments, the circuit 40 monitors the commands received by the memory module 10 from the computer system and selectively activates or deactivates the switches 120 to enable and disable the DQ data signal lines 102a, 102b to reduce the load of the memory module 10 on the computer system. In still other embodiments, the circuit 40 performs both of these functions together.

Command Signal Translation

[0069] Most high-density memory modules are currently built with 512-Megabit ("512-Mb") memory devices wherein each memory device has a 64M x 8-bit configuration. For example, a 1-Gigabyte ("1-GB") memory module with error checking capabilities can be fabricated using eighteen such 512-Mb memory devices. Alternatively, it can be economically advantageous to fabricate a 1-GB memory module using lower-density memory devices and doubling the number of memory devices used to produce the desired word width. For example, by fabricating a 1-GB memory module using thirty-six 256-Mb memory devices with 64M x 4-bit configuration, the cost of the resulting 1-GB memory module can be reduced since the unit cost of each 256-Mb memory device is typically lower than one-half the unit cost of each 512-Mb memory device. The cost savings can be significant, even though twice as many 256-Mb memory devices are used in place of the 512-Mb memory devices. For example, by using pairs of 512-Mb memory devices rather than single 1-Gb memory devices, certain embodiments described herein reduce the cost of the memory module by a factor of up to approximately five.

[0070] Market pricing factors for DRAM devices are such that higher-density DRAM devices (e.g., 1-Gb DRAM devices) are much more than twice the price of lower-density DRAM devices (e.g., 512-Mb DRAM devices). In other words, the price per bit ratio of the higher-density DRAM devices is greater than that of the lower-density DRAM devices.

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This pricing difference often lasts for months or even years after the introduction of the higher-density DRAM devices, until volume production factors reduce the costs of the newer higher-density DRAM devices. Thus, when the cost of a higher-density DRAM device is more than the cost of two lower-density DRAM devices, there is an economic incentive for utilizing pairs of the lower-density DRAM devices to replace individual higher-density DRAM devices.

[0071] Figure 9A schematically illustrates an exemplary memory module 10 compatible with certain embodiments described herein. The memory module 10 is connectable to a memory controller 20 of a computer system (not shown). The memory module 10 comprises a printed circuit board 210 and a plurality of memory devices 30 coupled to the printed circuit board 210. The plurality of memory devices 30 has a first number of memory devices 30. The memory module 10 further comprises a circuit 40 coupled to the printed circuit board 210. The circuit 40 receives a set of input address and command signals from the computer system. The set of input address and command signals correspond to a second number of memory devices 30 smaller than the first number of memory devices 30. The circuit 40 generates a set of output address and command signals in response to the set of input address and command signals. The set of output address and command signals corresponds to the first number of memory devices 30.

[0072] In certain embodiments, as schematically illustrated in Figure 9A, the memory module 10 further comprises a phase-lock loop device 220 coupled to the printed circuit board 210 and a register 230 coupled to the printed circuit board 210. In certain embodiments, the phase-lock loop device 220 and the register 230 are each mounted on the printed circuit board 210. In response to signals received from the computer system, the phase-lock loop device 220 transmits clock signals to the plurality of memory devices 30, the circuit 40, and the register 230. The register 230 receives and buffers a plurality of command signals and address signals (e.g., bank address signals, row address signals, column address signals, gated column address strobe signals, chip-select signals), and transmits corresponding signals to the appropriate memory devices 30. In certain embodiments, the register 230 comprises a plurality of register devices. While the phase-lock loop device 220, the register 230, and the circuit 40 are described herein in certain embodiments as being

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separate components, in certain other embodiments, two or more of the phase-lock loop device 220, the register 230, and the circuit 40 are portions of a single component. Persons skilled in the art are able to select a phase-lock loop device 220 and a register 230 compatible with embodiments described herein.

[0073] In certain embodiments, the memory module 10 further comprises electrical components which are electrically coupled to one another and are surface-mounted or embedded on the printed circuit board 210. These electrical components can include, but are not limited to, electrical conduits, resistors, capacitors, inductors, and transistors. In certain embodiments, at least some of these electrical components are discrete, while in other certain embodiments, at least some of these electrical components are constituents of one or more integrated circuits.

[0074] In certain embodiments, the printed circuit board 210 is mountable in a module slot of the computer system. The printed circuit board 210 of certain such embodiments has a plurality of edge connections electrically coupled to corresponding contacts of the module slot and to the various components of the memory module 10, thereby providing electrical connections between the computer system and the components of the memory module 10.

[0075] In certain embodiments, the plurality of memory devices 30 are arranged in a first number of ranks 32. For example, in certain embodiments, the memory devices 30 are arranged in four ranks 32a, 32b, 32c, 32d, as schematically illustrated by Figure 9A. In certain other embodiments, the memory devices 30 are arranged in two ranks 32a, 32b, as schematically illustrated by Figure 9B. Other numbers of ranks 32 of the memory devices 30 are also compatible with embodiments described herein.

[0076] As schematically illustrated by Figures 9A and 9B, in certain embodiments, the circuit 40 receives a set of input command signals (e.g., refresh, precharge) and address signals (e.g., bank address signals, row address signals, column address signals, gated column address strobe signals, chip-select signals) from the memory controller 20 of the computer system. In response to the set of input address and command signals, the circuit 40 generates a set of output address and command signals.

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[0077] In certain embodiments, the set of output address and command signals corresponds to a first number of ranks in which the plurality of memory devices 30 of the memory module 10 are arranged, and the set of input address and command signals corresponds to a second number of ranks per memory module for which the computer system is configured. The second number of ranks in certain embodiments is smaller than the first number of ranks. For example, in the exemplary embodiment as schematically illustrated by Figure 9A, the first number of ranks is four while the second number of ranks is two. In the exemplary embodiment of Figure 9B, the first number of ranks is two while the second number of ranks is one. Thus, in certain embodiments, even though the memory module 10 actually has the first number of ranks of memory devices 30, the memory module 10 simulates a virtual memory module by operating as having the second number of ranks of memory devices 30. In certain embodiments, the memory module 10 simulates a virtual memory module when the number of memory devices 30 of the memory module 10 is larger than the number of memory devices 30 per memory module for which the computer system is configured to utilize. In certain embodiments, the circuit 40 comprises logic (e.g., address decoding logic, command decoding logic) which translates between a system memory domain of the computer system and a physical memory domain of the memory module 10.

[0078] In certain embodiments, the computer system is configured for a number of ranks per memory module which is smaller than the number of ranks in which the memory devices 30 of the memory module 10 are arranged. In certain such embodiments, the computer system is configured for two ranks of memory per memory module (providing two chip-select signals CS_0, CS_1) and the plurality of memory modules 30 of the memory module 10 are arranged in four ranks, as schematically illustrated by Figure 9A. In certain other such embodiments, the computer system is configured for one rank of memory per memory module (providing one chip-select signal CS_0) and the plurality of memory modules 30 of the memory module 10 are arranged in two ranks, as schematically illustrated by Figure 9B.

[0079] In the exemplary embodiment schematically illustrated by Figure 9A, the memory module 10 has four ranks of memory devices 30 and the computer system is configured for two ranks of memory devices per memory module. The memory module 10 receives row/column address signals or signal bits (A_0-A_{n+1}), bank address signals (BA_0-

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BA_m), chip-select signals (CS_0 and CS_1), and command signals (e.g., refresh, precharge, etc.) from the computer system. The A_0-A_n row/column address signals are received by the register 230, which buffers these address signals and sends these address signals to the appropriate ranks of memory devices 30. The circuit 40 receives the two chip-select signals (CS_0, CS_1) and one row/column address signal (A_{n+1}) from the computer system. Both the circuit 40 and the register 230 receive the bank address signals (BA_0-BA_m) and at least one command signal (e.g., refresh, precharge, etc.) from the computer system.

Logic Tables

[0080] Table 1 provides a logic table compatible with certain embodiments described herein for the selection among ranks of memory devices 30 using chip-select signals.

Table 1:

State	CS_0	CS_1	A_{n+1}	Command	CS_{0A}	CS_{0B}	CS_{1A}	CS_{1B}
1	0	1	0	Active	0	1	1	1
2	0	1	1	Active	1	0	1	1
3	0	1	x	Active	0	0	1	1
4	1	0	0	Active	1	1	0	1
5	1	0	1	Active	1	1	1	0
6	1	0	x	Active	1	1	0	0
7	1	1	x	x	1	1	1	1

Note:

1. CS_0, CS_1, CS_{0A}, CS_{0B}, CS_{1A}, and CS_{1B} are active low signals.
2. A_{n+1} is an active high signal.
3. 'x' is a Don't Care condition.
4. Command involves a number of command signals that define operations such as refresh, precharge, and other operations.

[0081] In Logic State 1: CS_0 is active low, A_{n+1} is non-active, and Command is active. CS_{0A} is pulled low, thereby selecting Rank 0.

[0082] In Logic State 2: CS_0 is active low, A_{n+1} is active, and Command is active. CS_{0B} is pulled low, thereby selecting Rank 1.

[0083] In Logic State 3: CS_0 is active low, A_{n+1} is Don't Care, and Command is active high. CS_{0A} and CS_{0B} are pulled low, thereby selecting Ranks 0 and 1.

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[0084] In Logic State 4: CS_1 is active low, A_{n+1} is non-active, and Command is active. CS_{1A} is pulled low, thereby selecting Rank 2.

[0085] In Logic State 5: CS_1 is active low, A_{n+1} is active, and Command is active. CS_{1B} is pulled low, thereby selecting Rank 3.

[0086] In Logic State 6: CS_1 is active low, A_{n+1} is Don't Care, and Command is active. CS_{1A} and CS_{1B} are pulled low, thereby selecting Ranks 2 and 3.

[0087] In Logic State 7: CS_0 and CS_1 are pulled non-active high, which deselects all ranks, i.e., CS_{0A}, CS_{0B}, CS_{1A}, and CS_{1B} are pulled high.

[0088] The "Command" column of Table 1 represents the various commands that a memory device (e.g., a DRAM device) can execute, examples of which include, but are not limited to, activation, read, write, precharge, and refresh. In certain embodiments, the command signal is passed through to the selected rank only (e.g., state 4 of Table 1). In such embodiments, the command signal (e.g., read) is sent to only one memory device or the other memory device so that data is supplied from one memory device at a time. In other embodiments, the command signal is passed through to both associated ranks (e.g., state 6 of Table 1). In such embodiments, the command signal (e.g., refresh) is sent to both memory devices to ensure that the memory content of the memory devices remains valid over time. Certain embodiments utilize a logic table such as that of Table 1 to simulate a single memory device from two memory devices by selecting two ranks concurrently.

[0089] Table 2 provides a logic table compatible with certain embodiments described herein for the selection among ranks of memory devices 30 using gated CAS signals.

Table 2:

CS*	RAS*	CAS*	WE*	Density Bit	A_{10}	Command	CAS0*	CAS1*
1	x	x	x	x	x	NOP	x	x
0	1	1	1	x	x	NOP	1	1
0	0	1	1	0	x	ACTIVATE	1	1
0	0	1	1	1	x	ACTIVATE	1	1
0	1	0	1	0	x	READ	0	1
0	1	0	1	1	x	READ	1	0
0	1	0	0	0	x	WRITE	0	1

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0	1	0	0	1	x	WRITE	1	0
0	0	1	0	0	0	PRECHARGE	1	1
0	0	1	0	1	0	PRECHARGE	1	1
0	0	1	0	x	1	PRECHARGE	1	1
0	0	0	0	x	x	MODE REG SET	0	0
0	0	0	1	x	x	REFRESH	0	0

[0090] In certain embodiments in which the density bit is a row address bit, for read/write commands, the density bit is the value latched during the activate command for the selected bank.

Serial-Presence-Detect Device

[0091] Memory modules typically include a serial-presence detect (SPD) device 240 (e.g., an electrically-erasable-programmable read-only memory or EEPROM device) comprising data which characterize various attributes of the memory module, including but not limited to, the number of row addresses the number of column addresses, the data width of the memory devices, the number of ranks, the memory density per rank, the number of memory devices, and the memory density per memory device. The SPD device 240 communicates this data to the basic input/output system (BIOS) of the computer system so that the computer system is informed of the memory capacity and the memory configuration available for use and can configure the memory controller properly for maximum reliability and performance.

[0092] For example, for a commercially-available 512-MB (64M x 8-byte) memory module utilizing eight 512-Mb memory devices each with a 64M x 8-bit configuration, the SPD device contains the following SPD data (in appropriate bit fields of these bytes):

Byte 3: Defines the number of row address bits in the DRAM device in the memory module [13 for the 512-Mb memory device].

Byte 4: Defines the number of column address bits in the DRAM device in the memory module [11 for the 512-Mb memory device].

Byte 13: Defines the bit width of the primary DRAM device used in the memory module [8 bits for the 512-Mb (64M x 8-bit) memory device].

Byte 14: Defines the bit width of the error checking DRAM device used in the memory module [8 bits for the 512-Mb (64M x 8-bit) memory device].

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Byte 17: Defines the number of banks internal to the DRAM device used in the memory module [4 for the 512-Mb memory device].

[0093] In a further example, for a commercially-available 1-GB (128M x 8-byte) memory module utilizing eight 1-Gb memory devices each with a 128M x 8-bit configuration, as described above, the SPD device contains the following SPD data (in appropriate bit fields of these bytes):

Byte 3: Defines the number of row address bits in the DRAM device in the memory module [14 for the 1-Gb memory device].

Byte 4: Defines the number of column address bits in the DRAM device in the memory module [11 for the 1-Gb memory device].

Byte 13: Defines the bit width of the primary DRAM device used in the memory module [8 bits for the 1-Gb (128M x 8-bit) memory device].

Byte 14: Defines the bit width of the error checking DRAM device used in the memory module [8 bits for the 1-Gb (128M x 8-bit) memory device].

Byte 17: Defines the number of banks internal to the DRAM device used in the memory module [4 for the 1-Gb memory device].

[0094] In certain embodiments, the SPD device 240 comprises data which characterize the memory module 10 as having fewer ranks of memory devices than the memory module 10 actually has, with each of these ranks having more memory density. For example, for a memory module 10 compatible with certain embodiments described herein having two ranks of memory devices 30, the SPD device 240 comprises data which characterizes the memory module 10 as having one rank of memory devices with twice the memory density per rank. Similarly, for a memory module 10 compatible with certain embodiments described herein having four ranks of memory devices 30, the SPD device 240 comprises data which characterizes the memory module 10 as having two ranks of memory devices with twice the memory density per rank. In addition, in certain embodiments, the SPD device 240 comprises data which characterize the memory module 10 as having fewer memory devices than the memory module 10 actually has, with each of these memory devices having more memory density per memory device. For example, for a memory module 10 compatible with certain embodiments described herein, the SPD device 240 comprises data which characterizes the memory module 10 as having one-half the number of memory devices that the memory module 10 actually has, with each of these memory devices

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having twice the memory density per memory device. Thus, in certain embodiments, the SPD device 240 informs the computer system of the larger memory array by reporting a memory device density that is a multiple of the memory devices 30 resident on the memory module 10. Certain embodiments described herein advantageously do not require system level changes to hardware (e.g., the motherboard of the computer system) or to software (e.g., the BIOS of the computer system).

[0095] Figure 9C schematically illustrates an exemplary memory module 10 in accordance with certain embodiments described herein. The memory module 10 comprises a pair of substantially identical memory devices 31, 33. Each memory device 31, 33 has a first bit width, a first number of banks of memory locations, a first number of rows of memory locations, and a first number of columns of memory locations. The memory module 10 further comprises an SPD device 240 comprising data that characterizes the pair of memory devices 31, 33. The data characterize the pair of memory devices 31, 33 as a virtual memory device having a second bit width equal to twice the first bit width, a second number of banks of memory locations equal to the first number of banks, a second number of rows of memory locations equal to the first number of rows, and a second number of columns of memory locations equal to the first number of columns.

[0096] In certain such embodiments, the SPD device 240 of the memory module 10 is programmed to describe the combined pair of lower-density memory devices 31, 33 as one virtual or pseudo-higher-density memory device. In an exemplary embodiment, two 512-Mb memory devices, each with a 128M x 4-bit configuration, are used to simulate one 1-Gb memory device having a 128M x 8-bit configuration. The SPD device 240 of the memory module 10 is programmed to describe the pair of 512-Mb memory devices as one virtual or pseudo-1-Gb memory device.

[0097] For example, to fabricate a 1-GB (128M x 8-byte) memory module, sixteen 512-Mb (128M x 4-bit) memory devices can be used. The sixteen 512-Mb (128M x 4-bit) memory devices are combined in eight pairs, with each pair serving as a virtual or pseudo-1-Gb (128M x 8-bit) memory device. In certain such embodiments, the SPD device 240 contains the following SPD data (in appropriate bit fields of these bytes):

Byte 3: 13 row address bits.
Byte 4: 12 column address bits.

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Byte 13: 8 bits wide for the primary virtual 1-Gb (128M x 8-bit) memory device.
Byte 14: 8 bits wide for the error checking virtual 1-Gb (128M x 8-bit) memory device.
Byte 17: 4 banks.

[0098] In this exemplary embodiment, bytes 3, 4, and 17 are programmed to have the same values as they would have for a 512-MB (128M x 4-byte) memory module utilizing 512-Mb (128M x 4-bit) memory devices. However, bytes 13 and 14 of the SPD data are programmed to be equal to 8, corresponding to the bit width of the virtual or pseudo-higher-density 1-Gb (128M x 8-bit) memory device, for a total capacity of 1-GB. Thus, the SPD data does not describe the actual-lower-density memory devices, but instead describes the virtual or pseudo-higher-density memory devices. The BIOS accesses the SPD data and recognizes the memory module as having 4 banks of memory locations arranged in 2^{13} rows and 2^{12} columns, with each memory location having a width of 8 bits rather than 4 bits.

[0099] In certain embodiments, when such a memory module 10 is inserted in a computer system, the computer system's memory controller then provides to the memory module 10 a set of input address and command signals which correspond to the number of ranks or the number of memory devices reported by the SPD device 240. For example, placing a two-rank memory module 10 compatible with certain embodiments described herein in a computer system compatible with one-rank memory modules, the SPD device 240 reports to the computer system that the memory module 10 only has one rank. The circuit 40 then receives a set of input address and command signals corresponding to a single rank from the computer system's memory controller, and generates and transmits a set of output address and command signals corresponding to two ranks to the appropriate memory devices 30 of the memory module 10.

[0100] Similarly, when a two-rank memory module 10 compatible with certain embodiments described herein is placed in a computer system compatible with either one- or two-rank memory modules, the SPD device 240 reports to the computer system that the memory module 10 only has one rank. The circuit 40 then receives a set of input address and command signals corresponding to a single rank from the computer system's memory controller, and generates and transmits a set of output address and command signals corresponding to two ranks to the appropriate memory devices 30 of the memory module 10.

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[0101] Furthermore, a four-rank memory module 10 compatible with certain embodiments described herein simulates a two-rank memory module whether the memory module 10 is inserted in a computer system compatible with two-rank memory modules or with two- or four-rank memory modules. Thus, by placing a four-rank memory module 10 compatible with certain embodiments described herein in a module slot that is four-rank-ready, the computer system provides four chip-select signals, but the memory module 10 only uses two of the chip-select signals.

[0102] In certain embodiments, the circuit 40 comprises the SPD device 240 which reports the CAS latency (CL) to the memory controller of the computer system. The SPD device 240 of certain embodiments reports a CL which has one more cycle than does the actual operational CL of the memory array. In certain embodiments, data transfers between the memory controller and the memory module are registered for one additional clock cycle by the circuit 40. The additional clock cycle of certain embodiments is added to the transfer time budget with an incremental overall CAS latency. This extra cycle of time in certain embodiments advantageously provides sufficient time budget to add a buffer which electrically isolates the ranks of memory devices 30 from the memory controller 20. The buffer of certain embodiments comprises combinatorial logic, registers, and logic pipelines. In certain embodiments, the buffer adds a one-clock cycle time delay, which is equivalent to a registered DIMM, to accomplish the address decoding. The one-cycle time delay of certain such embodiments provides sufficient time for read and write data transfers to provide the functions of the data path multiplexer/demultiplexer. Thus, for example, a DDR2 400-MHz memory system in accordance with embodiments described herein has an overall CAS latency of four, and uses memory devices with a CAS latency of three. In still other embodiments, the SPD device 240 does not utilize this extra cycle of time.

Memory Density Multiplication

[0103] In certain embodiments, two memory devices having a memory density are used to simulate a single memory device having twice the memory density, and an additional address signal bit is used to access the additional memory. Similarly, in certain embodiments, two ranks of memory devices having a memory density are used to simulate a single rank of memory devices having twice the memory density, and an additional address

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signal bit is used to access the additional memory. As used herein, such simulations of memory devices or ranks of memory devices are termed as "memory density multiplication," and the term "density transition bit" is used to refer to the additional address signal bit which is used to access the additional memory by selecting which rank of memory devices is enabled for a read or write transfer operation.

[0104] For example, for computer systems which are normally limited to using memory modules which have a single rank of 128M x 4-bit memory devices, certain embodiments described herein enable the computer system to utilize memory modules which have double the memory (e.g., two ranks of 128M x 4-bit memory devices). The circuit 40 of certain such embodiments provides the logic (e.g., command and address decoding logic) to double the number of chip selects, and the SPD device 240 reports a memory device density of 256M x 4-bit to the computer system.

[0105] In certain embodiments utilizing memory density multiplication embodiments, the memory module 10 can have various types of memory devices 30 (e.g., DDR1, DDR2, DDR3, and beyond). The circuit 40 of certain such embodiments utilizes implied translation logic equations having variations depending on whether the density transition bit is a row, column, or internal bank address bit. In addition, the translation logic equations of certain embodiments vary depending on the type of memory module 10 (e.g., UDIMM, RDIMM, FBDIMM, etc.). Furthermore, in certain embodiments, the translation logic equations vary depending on whether the implementation multiplies memory devices per rank or multiplies the number of ranks per memory module.

[0106] Table 3A provides the numbers of rows and columns for DDR-1 memory devices, as specified by JEDEC standard JESD79D, "Double Data Rate (DDR) SDRAM Specification," published February 2004, and incorporated in its entirety by reference herein.

Table 3A:

	128-Mb	256-Mb	512-Mb	1-Gb
Number of banks	4	4	4	4
Number of row address bits	12	13	13	14
Number of column address bits for "x 4" configuration	11	11	12	12
Number of column address bits for "x 8" configuration	10	10	11	11

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Number of column address bits for "x 16" configuration	9	9	10	10

[0107] As described by Table 3A, 512-Mb (128M x 4-bit) DRAM devices have 2^{13} rows and 2^{12} columns of memory locations, while 1-Gb (128M x 8-bit) DRAM devices have 2^{14} rows and 2^{11} columns of memory locations. Because of the differences in the number of rows and the number of columns for the two types of memory devices, complex address translation procedures and structures would typically be needed to fabricate a 1-GB (128M x 8-byte) memory module using sixteen 512-Mb (128M x 4-bit) DRAM devices.

[0108] Table 3B shows the device configurations as a function of memory density for DDR2 memory devices.

Table 3B:

	Number of Rows	Number of Columns	Number of Internal Banks	Page Size (x4s or x8s)
256 Mb	13	11	4	1 KB
512 Mb	14	11	4	1 KB
1 Gb	14	11	8	1 KB
2 Gb	15	11	8	1 KB
4 Gb	16	11	8	1 KB

Table 4 lists the corresponding density transition bit for the density transitions between the DDR2 memory densities of Table 3B.

Table 4:

Density Transition	Density Transition Bit
256 Mb to 512 Mb	A_{13}
512 Mb to 1 Gb	BA_2
1 Gb to 2 Gb	A_{14}
2 Gb to 4 Gb	A_{15}

Other certain embodiments described herein utilize a transition bit to provide a transition from pairs of physical 4-Gb memory devices to simulated 8-Gb memory devices.

[0109] In an example embodiment, the memory module comprises one or more pairs of 256-Mb memory devices, with each pair simulating a single 512-Mb memory device. The simulated 512-Mb memory device has four internal banks while each of the two 256-Mb memory devices has four internal banks, for a total of eight internal banks for the pair of 256-Mb memory devices. In certain embodiments, the additional row address bit is translated by

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the circuit 40 to the rank selection between each of the two 256-Mb memory devices of the pair. Although there are eight total internal banks in the rank-converted memory array, the computer system is only aware of four internal banks. When the memory controller activates a row for a selected bank, the circuit 40 activates the same row for the same bank, but it does so for the selected rank according to the logic state of the additional row address bit A_{13}.

[0110] In another example embodiment, the memory module comprises one or more pairs of 512-Mb memory devices, with each pair simulating a single 1-Gb memory device. The simulated 1-Gb memory device has eight internal banks while each of the two 512-Mb memory devices has four internal banks, for a total of eight internal banks for the pair of 512-Mb memory devices. In certain embodiments, the mapped BA_2 (bank 2) bit is used to select between the two ranks of 512-Mb memory devices to preserve the internal bank geometry expected by the memory controller of the computer system. The state of the BA_2 bit selects the upper or lower set of four banks, as well as the upper and lower 512-Mb rank.

[0111] In another example embodiment, the memory module comprises one or more pairs of 1-Gb memory devices, with each pair simulating a single 2-Gb memory device. Each of the two 1-Gb memory devices has eight internal banks for a total of sixteen internal banks, while the simulated 2-Gb memory device has eight internal banks. In certain embodiments, the additional row address bit translates to the rank selection between the two 1-Gb memory devices. Although there are sixteen total internal banks per pair of 1-Gb memory devices in the rank-converted memory array, the memory controller of the computer system is only aware of eight internal banks. When the memory controller activates a row of a selected bank, the circuit 40 activates the same row for the same bank, but is does so for the selected rank according to the logic state of the additional row address bit A_{14}.

[0112] The circuit 40 of certain embodiments provides substantially all of the translation logic used for the decoding (e.g., command and address decoding). In certain such embodiments, there is a fully transparent operational conversion from the "system memory" density domain of the computer system to the "physical memory" density domain of the memory module 10. In certain embodiments, the logic translation equations are programmed in the circuit 40 by hardware, while in certain other embodiments, the logic

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translation equations are programmed in the circuit 40 by software. Examples 1 and 2 provide exemplary sections of Verilog code compatible with certain embodiments described herein. As described more fully below, the code of Examples 1 and 2 includes logic to reduce potential problems due to "back-to-back adjacent read commands which cross memory device boundaries or "BBARX." Persons skilled in the art are able to provide additional logic translation equations compatible with embodiments described herein.

[0113] An exemplary section of Verilog code compatible with memory density multiplication from 512 Mb to 1 Gb using DDR2 memory devices with the BA_2 density transition bit is listed below in Example 2. The exemplary code of Example 2 corresponds to a circuit 40 which receives one chip-select signal from the computer system and which generates two chip-select signals.

[0114] Example 2:

```
always @(posedge clk_in)
  begin
            rs0N_R <= rs0_in_N;     // cs0
            rasN_R <= ras_in_N;
            casN_R <= cas_in_N;
            weN_R <= we_in_N;
  end

// Gated Chip Selects
assign      pcs0a_1  = (~rs0_in_N & ~ras_in_N & ~cas_in_N)                          // ref,md reg set
                     |(~rs0_in_N & ras_in_N & cas_in_N)                            // ref exit, pwr dn
                     |(~rs0_in_N & ~ras_in_N & cas_in_N & ~we_in_N & a10_in)       // pchg all
                     |(~rs0_in_N & ~ras_in_N & cas_in_N & ~we_in_N & ~a10_in & ~ba2_in)// pchg single bnk
                     |(~rs0_in_N & ~ras_in_N & cas_in_N & we_in_N      & ~ba2_in)  // activate
                     |(~rs0_in_N & ras_in_N & ~cas_in_N              & ~ba2_in)    // xfr
                     ;
assign      pcs0b_1  = (~rs0_in_N & ~ras_in_N & ~cas_in_N)                          // ref,md reg set
                     |(~rs0_in_N & ras_in_N & cas_in_N)                            // ref exit, pwr dn
                     |(~rs0_in_N & ~ras_in_N & cas_in_N & ~we_in_N & a10_in)       // pchg all
                     |(~rs0_in_N & ~ras_in_N & cas_in_N & ~we_in_N & ~a10_in & ba2_in)// pchg single bnk
                     |(~rs0_in_N & ~ras_in_N & cas_in_N & we_in_N      & ba2_in)   // activate
                     |(~rs0_in_N & ras_in_N & ~cas_in_N              & ba2_in) // xfr
                     ;
//---------------------------------------
  always @(posedge clk_in)
   begin
            a4_r <= a4_in ;
            a5_r <= a5_in ;
            a6_r <= a6_in ;
            a10_r <= a10_in ;
            ba0_r <= ba0_in ;
            ba1_r <= ba1_in ;
            ba2_r <= ba2_in ;
            q_mrs_cmd_cyc1 <= q_mrs_cmd ;
  end
////////////////////////////////////////////////////////////////
// determine the cas latency
////////////////////////////////////////////////////////////////
assign q_mrs_cmd_r = (!rasN_R & !casN_R & !weN_R)
              & !rs0N_R
            & (!ba0_r & !ba1_r)
```


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```
                ;       // md reg set cmd

always @(posedge clk_in)
 if (~reset_N)          // lmr
        cl3 <= 1'b1 ;
 else if (q_mrs_cmd_cyc1)       // load mode reg cmd
 begin
        cl3 <= (~a6_r & a5_r & a4_r ) ;
 end

always @(posedge clk_in)
 if (~reset_N)          // reset
        cl2 <= 1'b0 ;
 else if (q_mrs_cmd_cyc1)       // load mode reg cmd
 begin
        cl2 <= (~a6_r & a5_r & ~a4_r ) ;
 end

always @(posedge clk_in)
 if (~reset_N)          // reset
        cl4 <= 1'b0 ;
 else if (q_mrs_cmd_cyc1)       // load mode reg cmd
 begin
        cl4 <= (a6_r & ~a5_r & ~a4_r ) ;
 end

always @(posedge clk_in)
 if (~reset_N)          cl5 <= 1'b0 ;
 else if (q_mrs_cmd_cyc1)       // load mode reg cmd
 begin
        cl5 <= (a6_r & ~a5_r & a4_r ) ;
 end

assign          pre_cyc2_enfet = (wr_cmd_cyc1 & acs_cyc1 & cl3)   // wr brst cl3 preamble
                        ;
assign          pre_cyc3_enfet = (rd_cmd_cyc2 & cl3)              // rd brst cl3 preamble
                        | (wr_cmd_cyc2 & cl3)                     // wr brst cl3 1st pair
                        | (wr_cmd_cyc2 & cl4)                     // wr brst cl4 preamble

                        ;

assign          pre_cyc4_enfet = (wr_cmd_cyc3 & cl3)              // wr brst cl3 2nd pair
                        | (wr_cmd_cyc3 & cl4)                     // wr brst cl4 1st pair

                        | (rd_cmd_cyc3 & cl3)                     // rd brst cl3 1st pair
                        | (rd_cmd_cyc3 & cl4)                     // rd brst cl4 preamble
                        ;

assign          pre_cyc5_enfet = (rd_cmd_cyc4  & cl3)             // rd brst cl3 2nd pair
                        | (wr_cmd_cyc4  & cl4)                    // wr brst cl4 2nd pair

                        | (rd_cmd_cyc4  & cl4)                    // rd brst cl4 1st pair
                        ;

// dq
assign          pre_dq_cyc = pre_cyc2_enfet
                  | pre_cyc3_enfet
                  | pre_cyc4_enfet
                  | pre_cyc5_enfet
                  ;

assign          pre_dq_ncyc = enfet_cyc2
                    | enfet_cyc3
                    | enfet_cyc4
                    | enfet_cyc5
                    ;

// dqs
```


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```
assign                  pre_dqsa_cyc = (pre_cyc2_enfet & ~ba2_r)
                            |(pre_cyc3_enfet & ~ba2_cyc2)
                            |(pre_cyc4_enfet & ~ba2_cyc3)
                            |(pre_cyc5_enfet & ~ba2_cyc4)
                            ;
assign                  pre_dqsb_cyc = (pre_cyc2_enfet & ba2_r)
                            |(pre_cyc3_enfet & ba2_cyc2)
                            |(pre_cyc4_enfet & ba2_cyc3)
                            |(pre_cyc5_enfet & ba2_cyc4)
                            ;

assign                  pre_dqsa_ncyc = (enfet_cyc2 & ~ba2_cyc2)
                            |(enfet_cyc3 & ~ba2_cyc3)
                            |(enfet_cyc4 & ~ba2_cyc4)
                            |(enfet_cyc5 & ~ba2_cyc5)
                            ;
assign                  pre_dqsb_ncyc = (enfet_cyc2 & ba2_cyc2)
                            |(enfet_cyc3 & ba2_cyc3)
                            |(enfet_cyc4 & ba2_cyc4)
                            |(enfet_cyc5 & ba2_cyc5)
                            ;

always @(posedge clk_in)
  begin
            acs_cyc2 <= acs_cyc1 ;          // cs active
            ba2_cyc2 <= ba2_r ;
            ba2_cyc3 <= ba2_cyc2 ;
            ba2_cyc4 <= ba2_cyc3 ;
            ba2_cyc5 <= ba2_cyc4 ;

            rd_cmd_cyc2 <= rd_cmd_cyc1 & acs_cyc1;
            rd_cmd_cyc3 <= rd_cmd_cyc2 ;
            rd_cmd_cyc4 <= rd_cmd_cyc3 ;
            rd_cmd_cyc5 <= rd_cmd_cyc4 ;
            rd_cmd_cyc6 <= rd_cmd_cyc5 ;
            rd_cmd_cyc7 <= rd_cmd_cyc6 ;

            wr_cmd_cyc2 <= wr_cmd_cyc1 & acs_cyc1;
            wr_cmd_cyc3 <= wr_cmd_cyc2 ;
            wr_cmd_cyc4 <= wr_cmd_cyc3 ;
            wr_cmd_cyc5 <= wr_cmd_cyc4 ;
  end

 always @(negedge clk_in)
  begin
            dq_ncyc <= dq_cyc;
            dqs_ncyc_a <= dqs_cyc_a;
            dqs_ncyc_b <= dqs_cyc_b;
  end

// DQ FET enables
assign          enq_fet1  = dq_cyc  | dq_ncyc       ;
assign          enq_fet2  = dq_cyc  | dq_ncyc  ;
assign          enq_fet3  = dq_cyc  | dq_ncyc       ;
assign          enq_fet4  = dq_cyc  | dq_ncyc  ;
assign          enq_fet5  = dq_cyc  | dq_ncyc  ;
// DQS FET enables
assign          ens_fet1a = dqs_cyc_a  | dqs_ncyc_a   ;
assign          ens_fet2a = dqs_cyc_a  | dqs_ncyc_a   ;
assign          ens_fet3a = dqs_cyc_a  | dqs_ncyc_a   ;
assign          ens_fet1b = dqs_cyc_b  | dqs_ncyc_b   ;
assign          ens_fet2b = dqs_cyc_b  | dqs_ncyc_b   ;
assign          ens_fet3b = dqs_cyc_b  | dqs_ncyc_b   ;
```

[0115] Another exemplary section of Verilog code compatible with memory density multiplication from 256 Mb to 512 Mb using DDR2 memory devices and gated CAS

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signals with the row A_{13} density transition bit is listed below in Example 3. The exemplary code of Example 3 corresponds to a circuit 40 which receives one gated CAS signal from the computer system and which generates two gated CAS signals.

[0116] Example 3:

```
// latched a13 flags cs0, banks 0-3
  always @(posedge clk_in)
   if (actv_cmd_R & ~rs0N_R & ~bnk1_R & ~bnk0_R ) // activate
   begin
            l_a13_00 <= a13_r;
   end
  always @(posedge clk_in)
   if (actv_cmd_R & ~rs0N_R & ~bnk1_R &  bnk0_R)    // activate
   begin
            l_a13_01 <= a13_r;
   end
  always @(posedge clk_in)
   if (actv_cmd_R & ~rs0N_R & bnk1_R & ~bnk0_R)     // activate
   begin
            l_a13_10 <= a13_r;
   end
  always @(posedge clk_in)
   if (actv_cmd_R & ~rs0N_R & bnk1_R & bnk0_R)      // activate
   begin
            l_a13_11 <= a13_r;
   end
// gated cas
assign cas_i = ~(casN_R);
assign  cas0_o = ( ~rasN_R & cas_i)
            |( rasN_R &  ~l_a13_00 & ~bnk1_R & ~bnk0_R & cas_i)
            |( rasN_R &  ~l_a13_01 & ~bnk1_R &  bnk0_R & cas_i)
            |( rasN_R &  ~l_a13_10 &  bnk1_R & ~bnk0_R & cas_i)
            |( rasN_R &  ~l_a13_11 &  bnk1_R &  bnk0_R & cas_i)
            ;
assign  cas1_o = ( ~rasN_R  & cas_i)
            |( rasN_R & l_a13_00          & ~bnk1_R & ~bnk0_R & cas_i)
            |( rasN_R & l_a13_01          & ~bnk1_R &  bnk0_R & cas_i)
            |( rasN_R & l_a13_10          &  bnk1_R & ~bnk0_R & cas_i)
            |( rasN_R & l_a13_11          &  bnk1_R &  bnk0_R & cas_i)
            ;
assign      pcas_0_N = ~cas0_o;
assign      pcas_1_N = ~cas1_o;

assign      rd0_o_R1 = rasN_R & cas0_o & weN_R & ~rs0N_R;  // rnk0 rd cmd cyc

assign      rd1_o_R1 = rasN_R & cas1_o & weN_R & ~rs0N_R;  // rnk1 rd cmd cyc

assign      wr0_o_R1 = rasN_R & cas0_o & ~weN_R & ~rs0N_R; // rnk0 wr cmd cyc

assign      wr1_o_R1 = rasN_R & cas1_o & ~weN_R & ~rs0N_R ; // rnk1 wr cmd cyc

  always @(posedge clk_in)
   begin
            rd0_o_R2 <= rd0_o_R1 ;
            rd0_o_R3 <= rd0_o_R2;
            rd0_o_R4 <= rd0_o_R3;
            rd0_o_R5 <= rd0_o_R4;

            rd1_o_R2 <= rd1_o_R1 ;
            rd1_o_R3 <= rd1_o_R2;
            rd1_o_R4 <= rd1_o_R3;
            rd1_o_R5 <= rd1_o_R4;

            wr0_o_R2 <= wr0_o_R1 ;
```


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```
            wr0_o_R3 <= wr0_o_R2;
            wr0_o_R4 <= wr0_o_R3;

            wr1_o_R2 <= wr1_o_R1 ;
            wr1_o_R3 <= wr1_o_R2;
            wr1_o_R4 <= wr1_o_R3;
end

always @(posedge clk_in)
 begin
 if (
    (rd0_o_R2 & ~rd1_o_R4)                                          // pre-am rd if no ped on rnk 1
   | rd0_o_R3                                                       // 1st cyc of rd brst
   | rd0_o_R4                                                       // 2nd cyc of rd brst
   | (rd0_o_R5 & ~rd1_o_R2 & ~rd1_o_R3)                             // post-rd cyc if no ped on rnk 1
   | (wr0_o_R1)                                                     // pre-am wr
   | wr0_o_R2 | wr0_o_R3                                            // wr brst 1st & 2nd cyc
   | (wr0_o_R4)                                                     // post-wr cyc  (chgef9)
   | wr1_o_R1 | wr1_o_R2 | wr1_o_R3 | wr1_o_R4 // rank 1  (chgef9)
    )
                        en_fet_a <= 1'b1;                           // enable fet
 else
                        en_fet_a <= 1'b0;                           // disable fet
 end

always @(posedge clk_in)
            begin
            if (
                  (rd1_o_R2 & ~rd0_o_R4)
                | rd1_o_R3
                | rd1_o_R4
                | (rd1_o_R5 & ~rd0_o_R2 & ~rd0_o_R3)
              | (wr1_o_R1)                                          // (chgef8)
              | wr1_o_R2  | wr1_o_R3
       | (wr1_o_R4)                                                 // post-wr cyc          (chgef9)
       | wr0_o_R1 | wr0_o_R2 | wr0_o_R3 | wr0_o_R4                 // rank 0  (chgef9)
                  )
                        en_fet_b <= 1'b1;                           //
            else
                        en_fet_b <= 1'b0;
            end
```

[0117] In certain embodiments, the chipset memory controller of the computer system uses the inherent behavioral characteristics of the memory devices (e.g., DDR2 memory devices) to optimize throughput of the memory system. For example, for each internal bank in the memory array, a row (e.g., 1KB page) is advantageously held activated for an extended period of time. The memory controller, by anticipating a high number of memory accesses or hits to a particular region of memory, can exercise this feature to advantageously eliminate time-consuming pre-charge cycles. In certain such embodiments in which two half-density memory devices are transparently substituted for a single full-density memory device (as reported by the SPD device 240 to the memory controller), the memory devices advantageously support the "open row" feature.

[0118] Figure 10A schematically illustrates an exemplary memory module 10 which doubles the rank density in accordance with certain embodiments described herein.

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The memory module 10 has a first memory capacity. The memory module 10 comprises a plurality of substantially identical memory devices 30 configured as a first rank 32a and a second rank 32b. In certain embodiments, the memory devices 30 of the first rank 32a are configured in pairs, and the memory devices 30 of the second rank 32b are also configured in pairs. In certain embodiments, the memory devices 30 of the first rank 32a are configured with their respective DQS pins tied together and the memory devices 30 of the second rank 32b are configured with their respective DQS pins tied together, as described more fully below. The memory module 10 further comprises a circuit 40 which receives a first set of address and command signals from a memory controller (not shown) of the computer system. The first set of address and command signals is compatible with a second memory capacity substantially equal to one-half of the first memory capacity. The circuit 40 translates the first set of address and command signals into a second set of address and command signals which is compatible with the first memory capacity of the memory module 10 and which is transmitted to the first rank 32a and the second rank 32b.

[0119] The first rank 32a of Figure 10A has 18 memory devices 30 and the second rank 32b of Figure 10A has 18 memory devices 30. Other numbers of memory devices 30 in each of the ranks 32a, 32b are also compatible with embodiments described herein.

[0120] In the embodiment schematically illustrated by Figure 10A, the memory module 10 has a width of 8 bytes (or 64 bits) and each of the memory devices 30 of Figure 10A has a bit width of 4 bits. The 4-bit-wide ("x 4") memory devices 30 of Figure 10A have one-half the width, but twice the depth of 8-bit-wide ("x 8") memory devices. Thus, each pair of "x 4" memory devices 30 has the same density as a single "x 8" memory device, and pairs of "x 4" memory devices 30 can be used instead of individual "x 8" memory devices to provide the memory density of the memory module 10. For example, a pair of 512-Mb 128M x 4-bit memory devices has the same memory density as a 1-Gb 128M x 8-bit memory device.

[0121] For two "x 4" memory devices 30 to work in tandem to mimic a "x 8" memory device, the relative DQS pins of the two memory devices 30 in certain embodiments are advantageously tied together, as described more fully below. In addition, to access the

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memory density of a high-density memory module 10 comprising pairs of "x 4" memory devices 30, an additional address line is used. While a high-density memory module comprising individual "x 8" memory devices with the next-higher density would also utilize an additional address line, the additional address lines are different in the two memory module configurations.

[0122] For example, a 1-Gb 128M x 8-bit DDR-1 DRAM memory device uses row addresses A_{13}-A_0 and column addresses A_{11} and A_9-A_0. A pair of 512-Mb 128M x 4-bit DDR-1 DRAM memory devices uses row addresses A_{12}-A_0 and column addresses A_{12}, A_{11}, and A_9-A_0. In certain embodiments, a memory controller of a computer system utilizing a 1-GB 128M x 8 memory module 10 comprising pairs of the 512-Mb 128M x 4 memory devices 30 supplies the address and command signals including the extra row address (A_{13}) to the memory module 10. The circuit 40 receives the address and command signals from the memory controller and converts the extra row address (A_{13}) into an extra column address (A_{12}).

[0123] Figure 10B schematically illustrates an exemplary circuit 40 compatible with embodiments described herein. The circuit 40 is used for a memory module 10 comprising pairs of "x 4" memory devices 30 which mimic individual "x 8" memory devices. In certain embodiments, each pair has the respective DQS pins of the memory devices 30 tied together. In certain embodiments, as schematically illustrated by Figure 10B, the circuit 40 comprises a programmable-logic device (PLD) 42, a first multiplexer 44 electrically coupled to the first rank 32a of memory devices 30, and a second multiplexer 46 electrically coupled to the second rank 32b of memory devices 30. In certain embodiments, the PLD 42 and the first and second multiplexers 44, 46 are discrete elements, while in other certain embodiments, they are integrated within a single integrated circuit. Persons skilled in the art can select an appropriate PLD 42, first multiplexer 44, and second multiplexer 46 in accordance with embodiments described herein.

[0124] In the exemplary circuit 40 of Figure 10B, during a row access procedure (CAS is high), the first multiplexer 44 passes the A_{12} address through to the first rank 32, the second multiplexer 46 passes the A_{12} address through to the second rank 34, and the PLD 42 saves or latches the A_{13} address from the memory controller. In certain embodiments, a copy

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of the A_{13} address is saved by the PLD 42 for each of the internal banks (e.g., 4 internal banks) per memory device 30. During a subsequent column access procedure (CAS is low), the first multiplexer 44 passes the previously-saved A_{13} address through to the first rank 32a as the A_{12} address and the second multiplexer 46 passes the previously-saved A_{13} address through to the second rank 32b as the A_{12} address. The first rank 32a and the second rank 32b thus interpret the previously-saved A_{13} row address as the current A_{12} column address. In this way, in certain embodiments, the circuit 40 translates the extra row address into an extra column address in accordance with certain embodiments described herein.

[0125] Thus, by allowing two lower-density memory devices to be used rather than one higher-density memory device, certain embodiments described herein provide the advantage of using lower-cost, lower-density memory devices to build "next-generation" higher-density memory modules. Certain embodiments advantageously allow the use of lower-cost readily-available 512-Mb DDR-2 SDRAM devices to replace more expensive 1-Gb DDR-2 SDRAM devices. Certain embodiments advantageously reduce the total cost of the resultant memory module.

[0126] Figure 11A schematically illustrates an exemplary memory module 10 which doubles number of ranks in accordance with certain embodiments described herein. The memory module 10 has a first plurality of memory locations with a first memory density. The memory module 10 comprises a plurality of substantially identical memory devices 30 configured as a first rank 32a, a second rank 32b, a third rank 32c, and a fourth rank 32d. The memory module 10 further comprises a circuit 40 which receives a first set of address and command signals from a memory controller (not shown). The first set of address and command signals is compatible with a second plurality of memory locations having a second memory density. The second memory density is substantially equal to one-half of the first memory density. The circuit 40 translates the first set of address and command signals into a second set of address and command signals which is compatible with the first plurality of memory locations of the memory module 10 and which is transmitted to the first rank 32a, the second rank 32b, the third rank 32c, and the fourth rank 32d.

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[0127] Each rank 32a, 32b, 32c, 32d of Figure 11A has 9 memory devices 30. Other numbers of memory devices 30 in each of the ranks 32a, 32b, 32c, 32d are also compatible with embodiments described herein.

[0128] In the embodiment schematically illustrated by Figure 11A, the memory module 10 has a width of 8 bytes (or 64 bits) and each of the memory devices 30 of Figure 11A has a bit width of 8 bits. Because the memory module 10 has twice the number of 8-bit-wide ("x 8") memory devices 30 as does a standard 8-byte-wide memory module, the memory module 10 has twice the density as does a standard 8-byte-wide memory module. For example, a 1-GB 128M x 8-byte memory module with 36 512-Mb 128M x 8-bit memory devices (arranged in four ranks) has twice the memory density as a 512-Mb 128M x 8-byte memory module with 18 512-Mb 128M x 8-bit memory devices (arranged in two ranks).

[0129] To access the additional memory density of the high-density memory module 10, the two chip-select signals (CS_0, CS_1) are used with other address and command signals to gate a set of four gated CAS signals. For example, to access the additional ranks of four-rank 1-GB 128M x 8-byte DDR-1 DRAM memory module, the CS_0 and CS_1 signals along with the other address and command signals are used to gate the CAS signal appropriately, as schematically illustrated by Figure 11A. Figure 11B schematically illustrates an exemplary circuit 40 compatible with embodiments described herein. In certain embodiments, the circuit 40 comprises a programmable-logic device (PLD) 42 and four "OR" logic elements 52, 54, 56, 58 electrically coupled to corresponding ranks 32a, 32b, 32c, 32d of memory devices 30.

[0130] In certain embodiments, the PLD 42 comprises an ASIC, an FPGA, a custom-designed semiconductor device, or a CPLD. In certain embodiments, the PLD 42 and the four "OR" logic elements 52, 54, 56, 58 are discrete elements, while in other certain embodiments, they are integrated within a single integrated circuit. Persons skilled in the art can select an appropriate PLD 42 and appropriate "OR" logic elements 52, 54, 56, 58 in accordance with embodiments described herein.

[0131] In the embodiment schematically illustrated by Figure 11B, the PLD 42 transmits each of the four "enabled CAS" ($ENCAS_0a$, $ENCAS_0b$, $ENCAS_1a$, $ENCAS_1b$) signals to a corresponding one of the "OR" logic elements 52, 54, 56, 58. The CAS signal is

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also transmitted to each of the four "OR" logic elements 52, 54, 56, 58. The CAS signal and the "enabled CAS" signals are "low" true signals. By selectively activating each of the four "enabled CAS" signals which are inputted into the four "OR" logic elements 52, 54, 56, 58, the PLD 42 is able to select which of the four ranks 32a, 32b, 32c, 32d is active.

[0132] In certain embodiments, the PLD 42 uses sequential and combinatorial logic procedures to produce the gated CAS signals which are each transmitted to a corresponding one of the four ranks 32a, 32b, 32c, 32d. In certain other embodiments, the PLD 42 instead uses sequential and combinatorial logic procedures to produce four gated chip-select signals (e.g., CS_0a, CS_0b, CS_1a, and CS_1b) which are each transmitted to a corresponding one of the four ranks 32a, 32b, 32c, 32d.

Tied Data Strobe Signal Pins

[0133] For proper operation, the computer system advantageously recognizes a 1-GB memory module comprising 256-Mb memory devices with 64M x 4-bit configuration as a 1-GB memory module having 512-Mb memory devices with 64M x 8-bit configuration (e.g., as a 1-GB memory module with 128M x 8-byte configuration). This advantageous result is desirably achieved in certain embodiments by electrically connecting together two output signal pins (e.g., DQS or data strobe pins) of the two 256-Mb memory devices such that both output signal pins are concurrently active when the two memory devices are concurrently enabled. The DQS or data strobe is a bi-directional signal that is used during both read cycles and write cycles to validate or latch data. As used herein, the terms "tying together" or "tied together" refer to a configuration in which corresponding pins (e.g., DQS pins) of two memory devices are electrically connected together and are concurrently active when the two memory devices are concurrently enabled (e.g., by a common chip-select or CS signal). Such a configuration is different from standard memory module configurations in which the output signal pins (e.g., DQS pins) of two memory devices are electrically coupled to the same source, but these pins are not concurrently active since the memory devices are not concurrently enabled. However, a general guideline of memory module design warns against tying together two output signal pins in this way.

[0134] Figures 12 and 13 schematically illustrate a problem which may arise from tying together two output signal pins. Figure 12 schematically illustrates an exemplary

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memory module 305 in which a first DQS pin 312 of a first memory device 310 is electrically connected to a second DQS pin 322 of a second memory device 320. The two DQS pins 312, 322 are both electrically connected to a memory controller 330.

[0135] Figure 13 is an exemplary timing diagram of the voltages applied to the two DQS pins 312, 322 due to non-simultaneous switching. As illustrated by Figure 13, at time t_1, both the first DQS pin 312 and the second DQS pin 322 are high, so no current flows between them. Similarly, at time t_4, both the first DQS pin 312 and the second DQS pin 322 are low, so no current flows between them. However, for times between approximately t_2 and approximately t_3, the first DQS pin 312 is low while the second DQS pin 322 is high. Under such conditions, a current will flow between the two DQS pins 312, 322. This condition in which one DQS pin is low while the other DQS pin is high can occur for fractions of a second (e.g., 0.8 nanoseconds) during the dynamic random-access memory (DRAM) read cycle. During such conditions, the current flowing between the two DQS pins 312, 322 can be substantial, resulting in heating of the memory devices 310, 320, and contributing to the degradation of reliability and eventual failure of these memory devices.

[0136] A second problem may also arise from tying together two output signal pins. Figure 14 schematically illustrates another exemplary memory module 305 in which a first DQS pin 312 of a first memory device 310 is electrically connected to a second DQS pin 322 of a second memory device 320. The two DQS pins 312, 322 of Figure 14 are both electrically connected to a memory controller (not shown). The DQ (data input/output) pin 314 of the first memory device 310 and the corresponding DQ pin 324 of the second memory device 320 are each electrically connected to the memory controller by the DQ bus (not shown). Typically, each memory device 310, 320 will have a plurality of DQ pins (e.g., eight DQ pins per memory device), but for simplicity, Figure 14 only shows one DQ pin for each memory device 310, 320.

[0137] Each of the memory devices 310, 320 of Figure 14 utilizes a respective on-die termination or "ODT" circuit 332, 334 which has termination resistors (e.g., 75 ohms) internal to the memory devices 310, 320 to provide signal termination. Each memory device 310, 320 has a corresponding ODT signal pin 362, 364 which is electrically connected to the memory controller via an ODT bus 340. The ODT signal pin 362 of the first memory device

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310 receives a signal from the ODT bus 340 and provides the signal to the ODT circuit 332 of the first memory device 310. The ODT circuit 332 responds to the signal by selectively enabling or disabling the internal termination resistors 352, 356 of the first memory device 310. This behavior is shown schematically in Figure 14 by the switches 342, 344 which are either closed (dash-dot line) or opened (solid line). The ODT signal pin 364 of the second memory device 320 receives a signal from the ODT bus 340 and provides the signal to the ODT circuit 334 of the second memory device 320. The ODT circuit 334 responds to the signal by selectively enabling or disabling the internal termination resistors 354, 358 of the second memory device 320. This behavior is shown schematically in Figure 14 by the switches 346, 348 which are either closed (dash-dot line) or opened (solid line). The switches 342, 344, 346, 348 of Figure 14 are schematic representations of the operation of the ODT circuits 332, 334, and do not signify that the ODT circuits 332, 334 necessarily include mechanical switches.

[0138] Examples of memory devices 310, 320 which include such ODT circuits 332, 334 include, but are not limited to, DDR2 memory devices. Such memory devices are configured to selectively enable or disable the termination of the memory device in this way in response to signals applied to the ODT signal pin of the memory device. For example, when the ODT signal pin 362 of the first memory device 310 is pulled high, the termination resistors 352, 356 of the first memory device 310 are enabled. When the ODT signal pin 362 of the first memory device 310 is pulled low (e.g., grounded), the termination resistors 352, 356 of the first memory device 310 are disabled. By selectively disabling the termination resistors of an active memory device, while leaving the termination resistors of inactive memory devices enabled, such configurations advantageously preserve signal strength on the active memory device while continuing to eliminate signal reflections at the bus-die interface of the inactive memory devices.

[0139] In certain configurations, as schematically illustrated by Figure 14, the DQS pins 312, 322 of each memory device 310, 320 are selectively connected to a voltage VTT through a corresponding termination resistor 352, 354 internal to the corresponding memory device 310, 320. Similarly, in certain configurations, as schematically illustrated by Figure 14, the DQ pins 314, 324 are selectively connected to a voltage VTT through a

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corresponding termination resistor 356, 358 internal to the corresponding memory device 310, 320. In certain configurations, rather than being connected to a voltage VTT, the DQ pins 314, 324 and/or the DQS pins 312, 322 are selectively connected to ground through the corresponding termination resistors 352, 354, 356, 358. The resistances of the internal termination resistors 352, 354, 356, 358 are selected to clamp the voltages so as to reduce the signal reflections from the corresponding pins. In the configuration schematically illustrated by Figure 14, each internal termination resistor 352, 354, 356, 358 has a resistance of approximately 75 ohms.

[0140] When connecting the first memory device 310 and the second memory device 320 together to form a double word width, both the first memory device 310 and the second memory device 320 are enabled at the same time (e.g., by a common CS signal). Connecting the first memory device 310 and the second memory device 320 by tying the DQS pins 312, 322 together, as shown in Figure 14, results in a reduced effective termination resistance for the DQS pins 312, 322. For example, for the exemplary configuration of Figure 14, the effective termination resistance for the DQS pins 312, 322 is approximately 37.5 ohms, which is one-half the desired ODT resistance (for 75-ohm internal termination resistors) to reduce signal reflections since the internal termination resistors 352, 354 of the two memory devices 310, 320 are connected in parallel. This reduction in the termination resistance can result in signal reflections causing the memory device to malfunction.

[0141] Figure 15 schematically illustrates an exemplary memory module 400 in accordance with certain embodiments described herein. The memory module 400 comprises a first memory device 410 having a first data strobe (DQS) pin 412 and a second memory device 420 having a second data strobe (DQS) pin 422. The memory module 400 further comprises a first resistor 430 electrically coupled to the first DQS pin 412. The memory module 400 further comprises a second resistor 440 electrically coupled to the second DQS pin 422 and to the first resistor 430. The first DQS pin 412 is electrically coupled to the second DQS pin 422 through the first resistor 430 and through the second resistor 440.

[0142] In certain embodiments, the memory module 400 is a 1-GB unbuffered Double Data Rate (DDR) Synchronous Dynamic RAM (SDRAM) high-density dual in-line memory module (DIMM). Figures 16A and 16B schematically illustrate a first side 462 and

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a second side 464, respectively, of such a memory module 400 with eighteen 64M x 4-bit, DDR-1 SDRAM FBGA memory devices on each side of a 184-pin glass-epoxy printed circuit board (PCB) 460. In certain embodiments, the memory module 400 further comprises a phase-lock-loop (PLL) clock driver 470, an EEPROM for serial-presence detect (SPD) data 480, and decoupling capacitors (not shown) mounted on the PCB in parallel to suppress switching noise on VDD and VDDQ power supply for DDR-1 SDRAM. By using synchronous design, such memory modules 400 allow precise control of data transfer between the memory module 400 and the system controller. Data transfer can take place on both edges of the DQS signal at various operating frequencies and programming latencies. Therefore, certain such memory modules 400 are suitable for a variety of high-performance system applications.

[0143] In certain embodiments, the memory module 400 comprises a plurality of memory devices configured in pairs, each pair having a first memory device 410 and a second memory device 420. For example, in certain embodiments, a 128M x 72-bit DDR SDRAM high-density memory module 400 comprises thirty-six 64M x 4-bit DDR-1 SDRAM integrated circuits in FBGA packages configured in eighteen pairs. The first memory device 410 of each pair has the first DQS pin 412 electrically coupled to the second DQS pin 422 of the second memory device 420 of the pair. In addition, the first DQS pin 412 and the second DQS pin 422 are concurrently active when the first memory device 410 and the second memory device 420 are concurrently enabled.

[0144] In certain embodiments, the first resistor 430 and the second resistor 440 each has a resistance advantageously selected to reduce the current flow between the first DQS pin 412 and the second DQS pin 422 while allowing signals to propagate between the memory controller and the DQS pins 412, 422. In certain embodiments, each of the first resistor 430 and the second resistor 440 has a resistance in a range between approximately 5 ohms and approximately 50 ohms. For example, in certain embodiments, each of the first resistor 430 and the second resistor 440 has a resistance of approximately 22 ohms. Other resistance values for the first resistor 430 and the second resistor 440 are also compatible with embodiments described herein. In certain embodiments, the first resistor 430 comprises a single resistor, while in other embodiments, the first resistor 430 comprises a plurality of

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resistors electrically coupled together in series and/or in parallel. Similarly, in certain embodiments, the second resistor 440 comprises a single resistor, while in other embodiments, the second resistor 440 comprises a plurality of resistors electrically coupled together in series and/or in parallel.

[0145] Figures 17A and 17B schematically illustrate an exemplary embodiment of a memory module 400 in which the first resistor 430 and the second resistor 440 are used to reduce the current flow between the first DQS pin 412 and the second DQS pin 422. As schematically illustrated by Figure 17A, the memory module 400 is part of a computer system 500 having a memory controller 510. The first resistor 430 has a resistance of approximately 22 ohms and the second resistor 440 has a resistance of approximately 22 ohms. The first resistor 430 and the second resistor 440 are electrically coupled in parallel to the memory controller 510 through a signal line 520 having a resistance of approximately 25 ohms. The first resistor 430 and the second resistor 440 are also electrically coupled in parallel to a source of a fixed termination voltage (identified by VTT in Figures 17A and 17B) by a signal line 540 having a resistance of approximately 47 ohms. Such an embodiment can advantageously be used to allow two memory devices having lower bit widths (e.g., 4-bit) to behave as a single virtual memory device having a higher bit width (e.g., 8-bit).

[0146] Figure 17B schematically illustrates exemplary current-limiting resistors 430, 440 in conjunction with the impedances of the memory devices 410, 420. During an exemplary portion of a data read operation, the memory controller 510 is in a high-impedance condition, the first memory device 410 drives the first DQS pin 412 high (e.g., 2.7 volts), and the second memory device 420 drives the second DQS pin 422 low (e.g., 0 volts). The amount of time for which this condition occurs is approximated by the time between t_2 and t_3 of Figure 13, which in certain embodiments is approximately twice the tDQSQ (data strobe edge to output data edge skew time, e.g., approximately 0.8 nanoseconds). At least a portion of this time in certain embodiments is caused by simultaneous switching output (SSO) effects.

[0147] In certain embodiments, as schematically illustrated by Figure 17B, the DQS driver of the first memory device 410 has a driver impedance R_1 of approximately

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17 ohms, and the DQS driver of the second memory device 420 has a driver impedance R_4 of approximately 17 ohms. Because the upper network of the first memory device 410 and the first resistor 430 (with a resistance R_2 of approximately 22 ohms) is approximately equal to the lower network of the second memory device 420 and the second resistor 440 (with a resistance R_3 of approximately 22 ohms), the voltage at the midpoint is approximately 0.5 * (2.7 - 0) = 1.35 volts, which equals VTT, such that the current flow across the 47-ohm resistor of Figure 17B is approximately zero.

[0148] The voltage at the second DQS pin 422 in Figure 17B is given by V_{DQS2} = 2.7 * $R_4/(R_1+R_2+R_3+R_4)$ = 0.59 volts and the current flowing through the second DQS pin 422 is given by I_{DQS2} = 0.59 / R_4 = 34 milliamps. The power dissipation in the DQS driver of the second memory device 420 is thus P_{DQS2} = 34 mA * 0.59 V = 20 milliwatts. In contrast, without the first resistor 430 and the second resistor 440, only the 17-ohm impedances of the two memory devices 410, 420 would limit the current flow between the two DQS pins 412, 422, and the power dissipation in the DQS driver of the second memory device 420 would be approximately 107 milliwatts. Therefore, the first resistor 430 and the second resistor 440 of Figures 17A and 17B advantageously limit the current flowing between the two memory devices during the time that the DQS pin of one memory device is driven high and the DQS pin of the other memory device is driven low.

[0149] In certain embodiments in which there is overshoot or undershoot of the voltages, the amount of current flow can be higher than those expected for nominal voltage values. Therefore, in certain embodiments, the resistances of the first resistor 430 and the second resistor 440 are advantageously selected to account for such overshoot/undershoot of voltages.

[0150] For certain such embodiments in which the voltage at the second DQS pin 422 is V_{DQS2} = 0.59 volts and the duration of the overdrive condition is approximately 0.8 nanoseconds at maximum, the total surge is approximately 0.59 V * 1.2 ns = 0.3 V-ns. For comparison, the JEDEC standard for overshoot/undershoot is 2.4 V-ns, so certain embodiments described herein advantageously keep the total surge within predetermined standards (e.g., JEDEC standards).

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[0151] Figure 18 schematically illustrates another exemplary memory module 600 compatible with certain embodiments described herein. The memory module 600 comprises a termination bus 605. The memory module 600 further comprises a first memory device 610 having a first data strobe pin 612, a first termination signal pin 614 electrically coupled to the termination bus 605, a first termination circuit 616, and at least one data pin 618. The first termination circuit 616 selectively electrically terminating the first data strobe pin 612 and the first data pin 618 in response to a first signal received by the first termination signal pin 614 from the termination bus 605. The memory module 600 further comprises a second memory device 620 having a second data strobe pin 622 electrically coupled to the first data strobe pin 612, a second termination signal pin 624, a second termination circuit 626, and at least one data pin 628. The second termination signal pin 624 is electrically coupled to a voltage, wherein the second termination circuit 626 is responsive to the voltage by not terminating the second data strobe pin 622 or the second data pin 628. The memory module 600 further comprises at least one termination assembly 630 having a third termination signal pin 634, a third termination circuit 636, and at least one termination pin 638 electrically coupled to the data pin 628 of the second memory device 620. The third termination signal pin 634 is electrically coupled to the termination bus 605. The third termination circuit 636 selectively electrically terminates the data pin 628 of the second memory device 620 through the termination pin 638 in response to a second signal received by the third termination signal pin 634 from the termination bus 605.

[0152] Figure 19 schematically illustrates a particular embodiment of the memory module 600 schematically illustrated by Figure 18. The memory module 600 comprises an on-die termination (ODT) bus 605. The memory module 600 comprises a first memory device 610 having a first data strobe (DQS) pin 612, a first ODT signal pin 614 electrically coupled to the ODT bus 605, a first ODT circuit 616, and at least one data (DQ) pin 618. The first ODT circuit 616 selectively electrically terminates the first DQS pin 612 and the DQ pin 618 of the first memory device 610 in response to an ODT signal received by the first ODT signal pin 614 from the ODT bus 605. This behavior of the first ODT circuit 616 is schematically illustrated in Figure 14 by the switches 672, 676 which are selectively closed (dash-dot line) or opened (solid line).

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[0153] The memory module 600 further comprises a second memory device 620 having a second DQS pin 622 electrically coupled to the first DQS pin 612, a second ODT signal pin 624, a second ODT circuit 626, and at least one DQ pin 628. The first DQS pin 612 and the second DQS pin 622 are concurrently active when the first memory device 610 and the second memory device 620 are concurrently enabled. The second ODT signal pin 624 is electrically coupled to a voltage (e.g., ground), wherein the second ODT circuit 626 is responsive to the voltage by not terminating the second DQS pin 622 or the second DQ pin 624. This behavior of the second ODT circuit 626 is schematically illustrated in Figure 14 by the switches 674, 678 which are opened.

[0154] The memory module 600 further comprises at least one termination assembly 630 having a third ODT signal pin 634 electrically coupled to the ODT bus 605, a third ODT circuit 636, and at least one termination pin 638 electrically coupled to the DQ pin 628 of the second memory device 620. The third ODT circuit 636 selectively electrically terminates the DQ pin 628 of the second memory device 620 through the termination pin 638 in response to an ODT signal received by the third ODT signal pin 634 from the ODT bus 605. This behavior of the third ODT circuit 636 is schematically illustrated in Figure 19 by the switch 680 which is either closed (dash-dot line) or opened (solid line).

[0155] In certain embodiments, the termination assembly 630 comprises discrete electrical components which are surface-mounted or embedded on the printed-circuit board of the memory module 600. In certain other embodiments, the termination assembly 630 comprises an integrated circuit mounted on the printed-circuit board of the memory module 600. Persons skilled in the art can provide a termination assembly 630 in accordance with embodiments described herein.

[0156] Certain embodiments of the memory module 600 schematically illustrated by Figure 19 advantageously avoid the problem schematically illustrated by Figure 12 of electrically connecting the internal termination resistances of the DQS pins of the two memory devices in parallel. As described above in relation to Figure 14, Figures 18 and 19 only show one DQ pin for each memory device for simplicity. Other embodiments have a plurality of DQ pins for each memory device. In certain embodiments, each of the first ODT circuit 616, the second ODT circuit 626, and the third ODT circuit 636 are responsive to a

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high voltage or signal level by enabling the corresponding termination resistors and are responsive to a low voltage or signal level (e.g., ground) by disabling the corresponding termination resistors. In other embodiments, each of the first ODT circuit 616, the second ODT circuit 626, and the third ODT circuit 636 are responsive to a high voltage or signal level by disabling the corresponding termination resistors and are responsive to a low voltage or signal level (e.g., ground) by enabling the corresponding termination resistors. Furthermore, the switches 672, 674, 676, 678, 680 of Figure 18 are schematic representations of the enabling and disabling operation of the ODT circuits 616, 626, 636 and do not signify that the ODT circuits 616, 626, 636 necessarily include mechanical switches.

[0157] The first ODT signal pin 614 of the first memory device 610 receives an ODT signal from the ODT bus 605. In response to this ODT signal, the first ODT circuit 616 selectively enables or disables the termination resistance for both the first DQS pin 612 and the DQ pin 618 of the first memory device 610. The second ODT signal pin 624 of the second memory device 620 is tied (e.g., directly hard-wired) to the voltage (e.g., ground), thereby disabling the internal termination resistors 654, 658 on the second DQS pin 622 and the second DQ pin 628, respectively, of the second memory device 620 (schematically shown by open switches 674, 678 in Figure 19). The second DQS pin 622 is electrically coupled to the first DQS pin 612, so the termination resistance for both the first DQS pin 612 and the second DQS pin 622 is provided by the termination resistor 652 internal to the first memory device 510.

[0158] The termination resistor 656 of the DQ pin 618 of the first memory device 610 is enabled or disabled by the ODT signal received by the first ODT signal pin 614 of the first memory device 610 from the ODT bus 605. The termination resistance of the DQ pin 628 of the second memory device 620 is enabled or disabled by the ODT signal received by the third ODT signal pin 634 of the termination assembly 630 which is external to the second memory device 620. Thus, in certain embodiments, the first ODT signal pin 614 and the third ODT signal pin 634 receive the same ODT signal from the ODT bus 605, and the termination resistances for both the first memory device 610 and the second memory device 620 are selectively enabled or disabled in response thereto when these memory devices are concurrently enabled. In this way, certain embodiments of the memory module 600

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schematically illustrated by Figure 19 provides external or off-chip termination of the second memory device 620.

[0159] Certain embodiments of the memory module 600 schematically illustrated by Figure 19 advantageously allow the use of two lower-cost readily-available 512-Mb DDR-2 SDRAM devices to provide the capabilities of a more expensive 1-GB DDR-2 SDRAM device. Certain such embodiments advantageously reduce the total cost of the resultant memory module 600.

[0160] Certain embodiments described herein advantageously increase the memory capacity or memory density per memory slot or socket on the system board of the computer system. Certain embodiments advantageously allow for higher memory capacity in systems with limited memory slots. Certain embodiments advantageously allow for flexibility in system board design by allowing the memory module 10 to be used with computer systems designed for different numbers of ranks (e.g., either with computer systems designed for two-rank memory modules or with computer systems designed for four-rank memory modules). Certain embodiments advantageously provide lower costs of board designs.

[0161] In certain embodiments, the memory density of a memory module is advantageously doubled by providing twice as many memory devices as would otherwise be provided. For example, pairs of lower-density memory devices can be substituted for individual higher-density memory devices to reduce costs or to increase performance. As another example, twice the number of memory devices can be used to produce a higher-density memory configuration of the memory module. Each of these examples can be limited by the number of chip select signals which are available from the memory controller or by the size of the memory devices. Certain embodiments described herein advantageously provide a logic mechanism to overcome such limitations.

[0162] Various embodiments of the present invention have been described above. Although this invention has been described with reference to these specific embodiments, the descriptions are intended to be illustrative of the invention and are not intended to be limiting. Various modifications and applications may occur to those skilled in the art without departing from the true spirit and scope of the invention.

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WE CLAIM:

1. A circuit for use on a memory module, the memory module including a plurality of memory devices and operable in a computer system to perform memory operations in response to memory commands from a memory controller, the circuit comprising:

a register device to receive a set of input control/address signals associated with a respective memory command from the memory controller and to generate a set of output control/address signals in response to the set of input control/address signals, the set of output control/address signals being provided to the plurality of memory devices; and

logic to monitor the memory commands from the memory controller and to selectively isolate one or more first memory devices among the plurality of memory devices from the memory controller in response to the respective memory command so as to reduce a load of the memory module to the computer system while one or more second memory devices among the plurality of memory devices are communicating with the memory controller in response to the set of output control/address signals.

2. The circuit of claim 1, wherein the circuit further comprises multiple groups of DQ-DQS paths, and wherein the logic selectively isolate one or more first memory devices by disabling at least one first group of DQ-DQS paths corresponding to the one or more first memory devices.

3. The circuit of Claim 2, wherein the logic is further configured to enable at least one second group of DQ-DQS paths in response to the respective memory command so as to allow the one or more second memory devices to communicate data with the memory controller in response to the output control/address signals.

4. The circuit of claim 1, wherein the logic is further configured to translate between a system memory domain and a physical memory device domain such that a number of signals in the set of output control/address signals is greater than a number of signals in the set of input control/address signals.

5. The circuit of Claim 4, wherein the set of input control/address signals include at least one chip-select signal and the set of output control/address signals include a greater number of chip-select signals.

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6. The circuit of Claim 1, wherein the logic element includes a buffer circuit to electrically and selectively isolate the one or more first memory devices from the memory controller and to selectively allow one or more second memory devices to communicate data with the memory controller, the buffer circuit adding a time delay to a data signal from the one or more second memory devices to the memory controller.

7. The circuit of Claim 6, wherein the logic provides functions of a data path multiplexer /demultiplexer using the time delay.

8. The circuit of Claim 6, wherein the time delay is about one clock cycle.

9. The circuit of Claim 1, wherein the respective memory command is a read command or a write command.

10. A method of operating a circuit in a memory module, the memory module including a plurality of memory devices and operable to perform memory operations in response to memory commands from a memory controller, the method comprising:

receiving a set of input control/address signals associated with a respective memory command from the memory controller;

generating a set of output control/address signals in response to the set of input control/address signals;

providing the set of output control/address signals to the plurality of memory devices;

monitoring the memory commands from the memory controller; and

selectively isolating one or more first memory devices among the plurality of memory devices from the memory controller in response to the respective memory command so as to reduce a load of the memory module to the memory controller while one or more second memory devices among the plurality of memory devices are communicating with the memory controller in response to the set of output control/address signals.

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LOAD-REDUCING CIRCUIT FOR MEMORY MODULE

ABSTRACT OF THE DISCLOSURE

A circuit is mountable on a memory module that includes a plurality of memory devices and that is operable in a computer system to perform memory operations in response to memory commands from a memory controller. The circuit comprises a register device configured to receive a set of input control/address signals associated with a respective memory command (e.g., a read command or a write command) from the memory controller and to generate a set of output control/address signals in response to the set of input control/address signals. The set of output control/address signals are provided to the plurality of memory devices. The circuit further comprises logic to monitor the memory commands from the memory controller and to selectively isolate one or more first memory devices among the plurality of memory devices from the memory controller in response to the respective memory command so as to reduce a load of the memory module to the computer system while one or more second memory devices among the plurality of memory devices are communicating with the memory controller in response to the set of output control/address signals.

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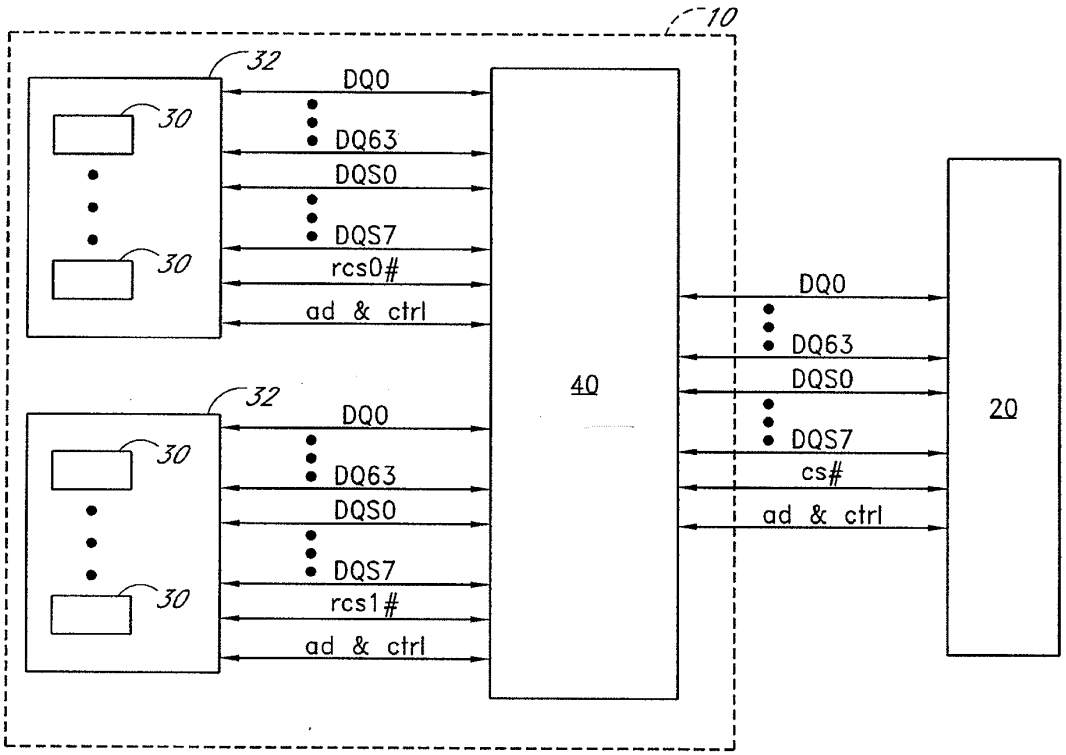

10
32
30
30
DQ0
DQ63
DQS0
DQS7
rcs0#
ad & ctrl
32
30
30
DQ0
DQ63
DQS0
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40
DQ0
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DQS0
DQS7
cs#
ad & ctrl
20

FIG. 1

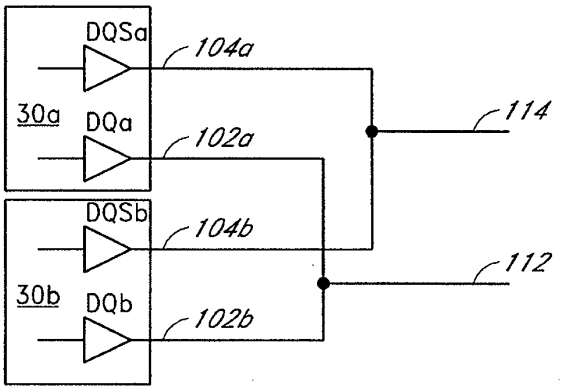


FIG. 2

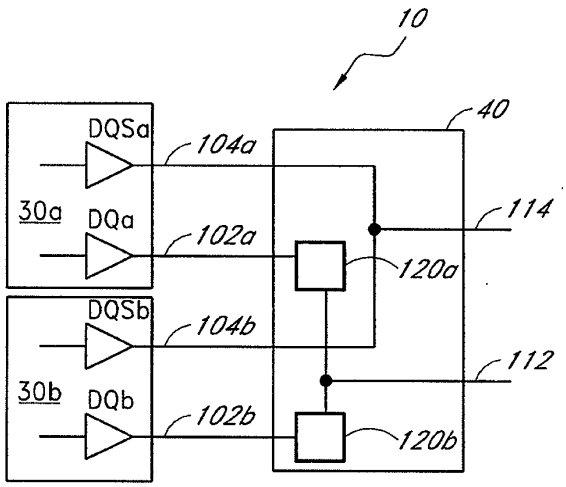

10
40
DQSa
104a
30a
DQa
102a
114
120a
DQSb
104b
112
30b
DQb
102b
120b

FIG. 3A

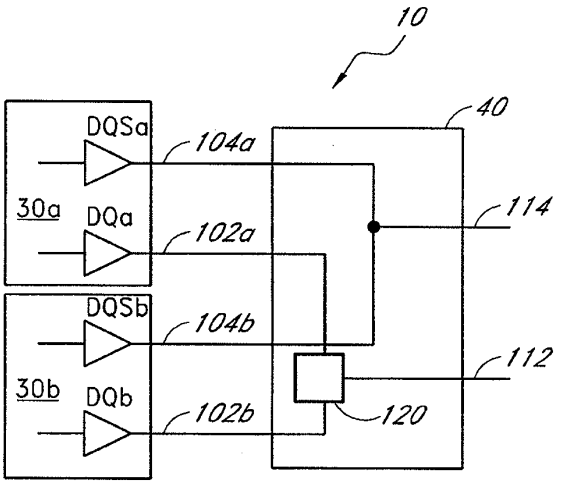

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30a
DQa
102a
114
DQSb
104b
112
30b
DQb
102b
120

FIG. 3B

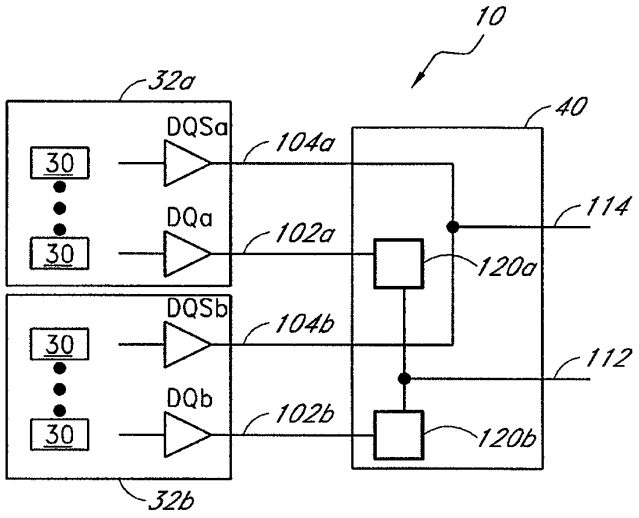

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32a
40
DQSa
104a
30
DQa
102a
30
114
120a
DQSb
104b
30
112
DQb
102b
30
120b
32b

FIG. 4A

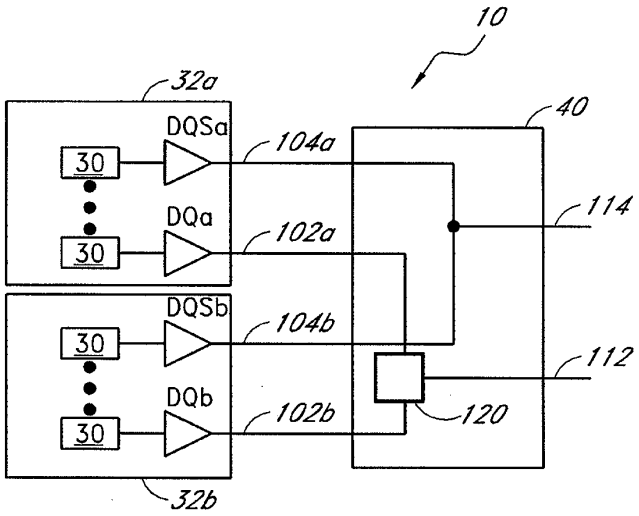

10
32a
40
DQSa
104a
30
DQa
102a
30
114
DQSb
104b
30
112
DQb
102b
30
120
32b

FIG. 4B

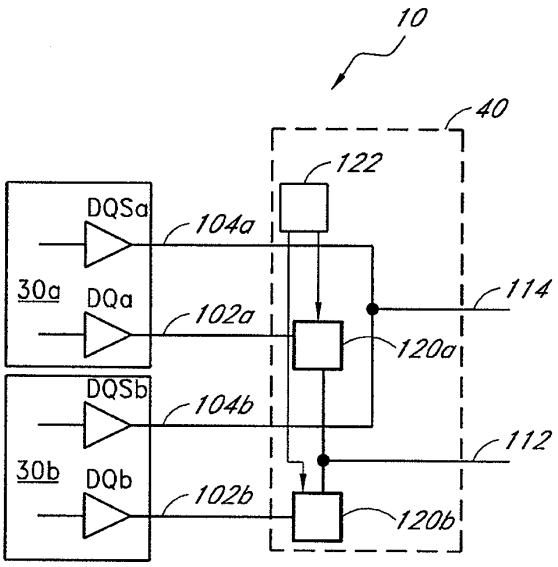

10
40
122
DQSa
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DQa
102a
114
120a
DQSb
104b
112
30b
DQb
102b
120b

FIG. 5A

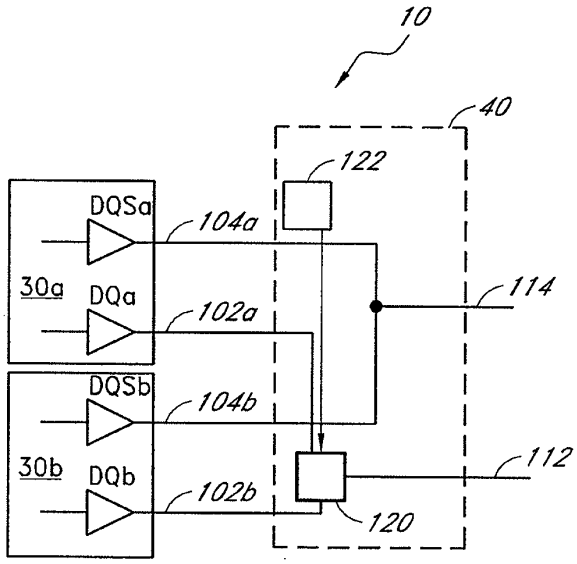

10
40
122
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30a
DQa
102a
114
DQSb
104b
112
30b
DQb
102b
120

FIG. 5B

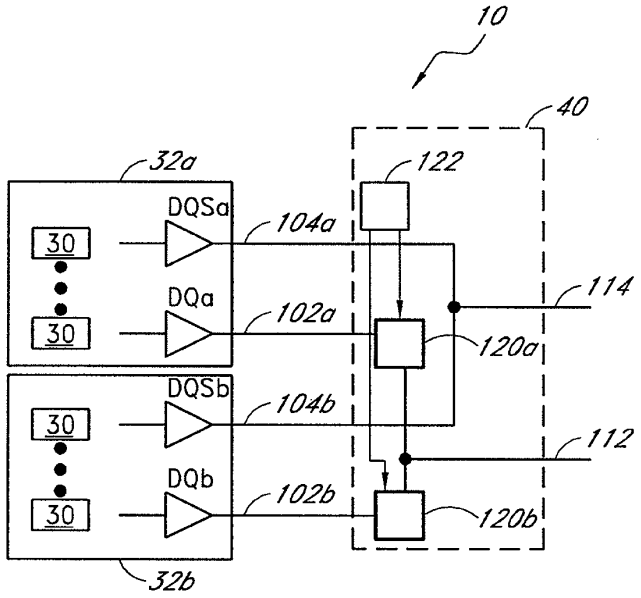

10
40
32a
122
DQSa
104a
30
DQa
102a
30
114
120a
DQSb
104b
30
112
DQb
102b
30
120b
32b

FIG. 5C

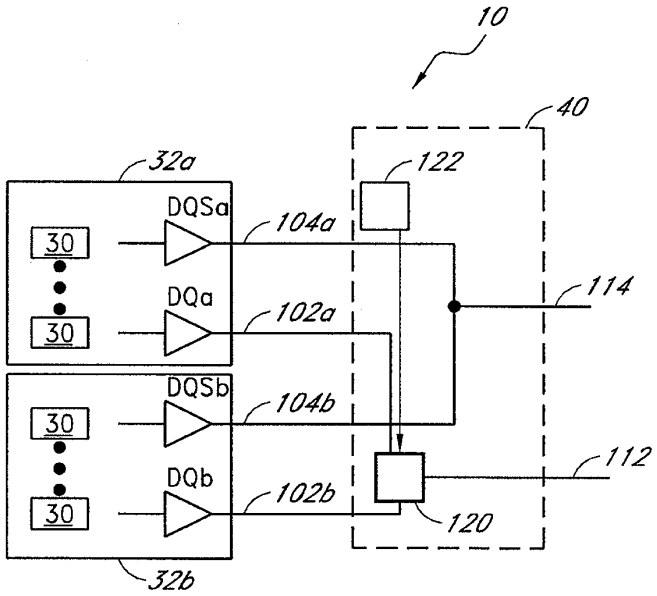

10
40
32a
122
DQSa
104a
30
DQa
102a
30
114
DQSb
104b
30
112
DQb
102b
30
120
32b

FIG. 5D

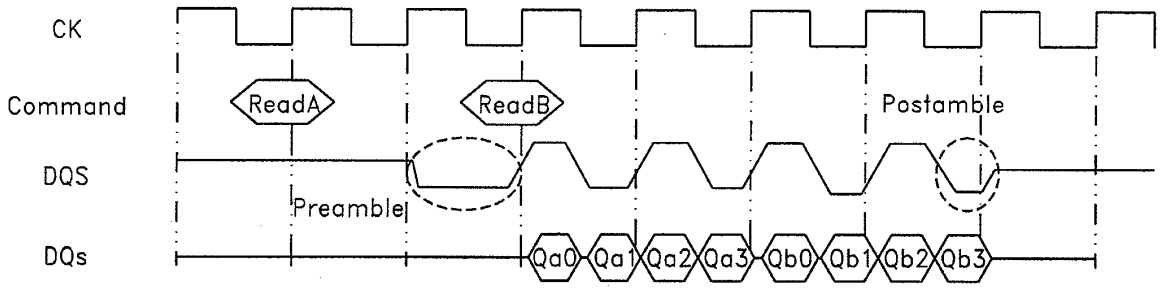

CK
Command
ReadA
ReadB
Postamble
DQS
Preamble
DQs
Qa0
Qa1
Qa2
Qa3
Qb0
Qb1
Qb2
Qb3

FIG. 6A

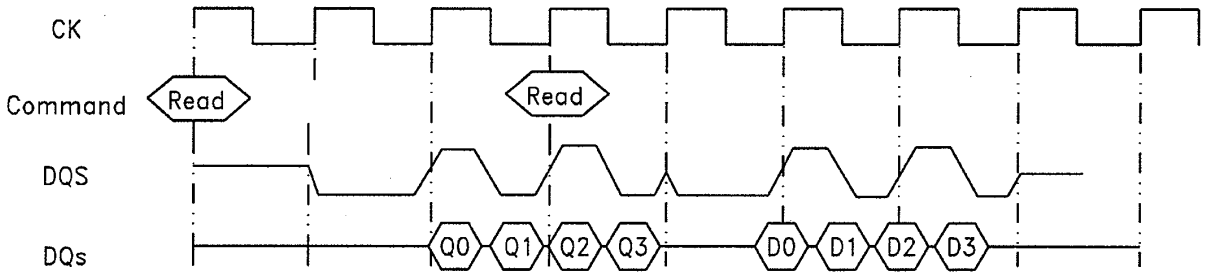

CK
Command
Read
Read
DQS
DQs
Q0
Q1
Q2
Q3
D0
D1
D2
D3

FIG. 6B

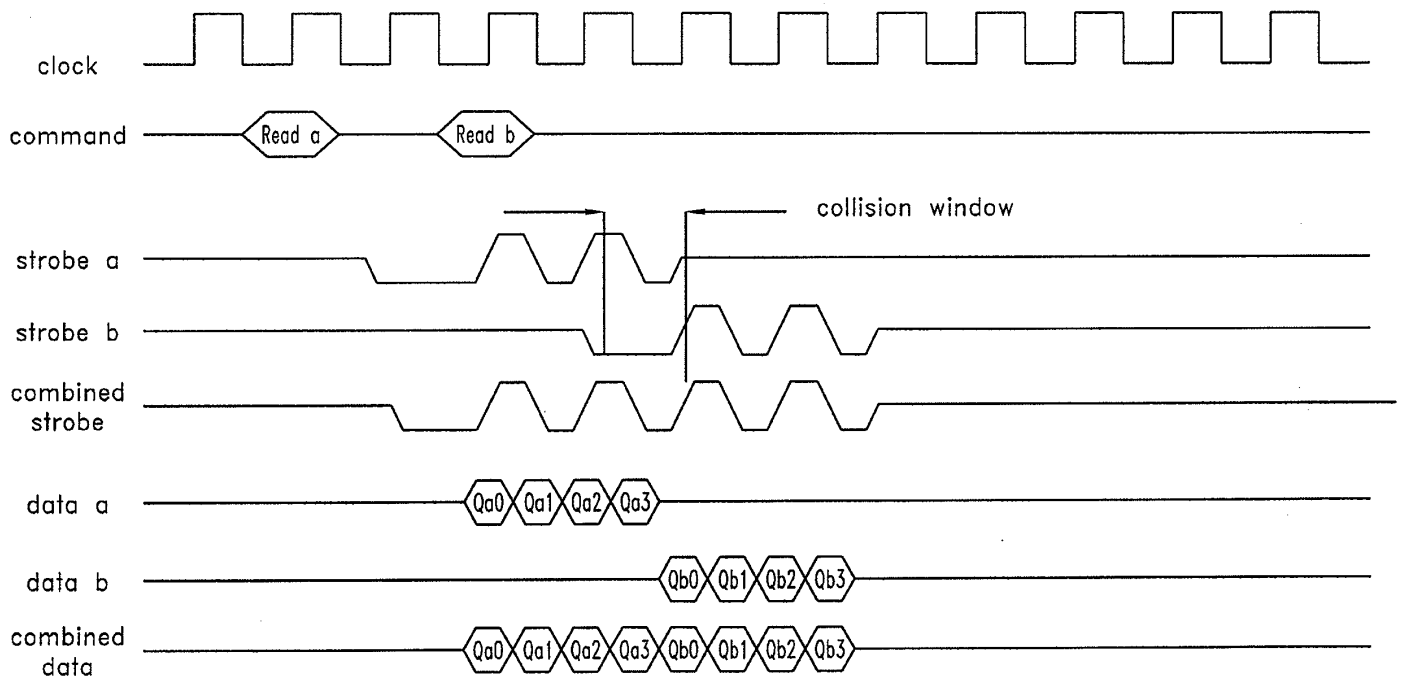

clock
command
Read a
Read b
collision window
strobe a
strobe b
combined strobe
data a
Qa0
Qa1
Qa2
Qa3
data b
Qb0
Qb1
Qb2
Qb3
combined data
Qa0
Qa1
Qa2
Qa3
Qb0
Qb1
Qb2
Qb3

FIG. 7

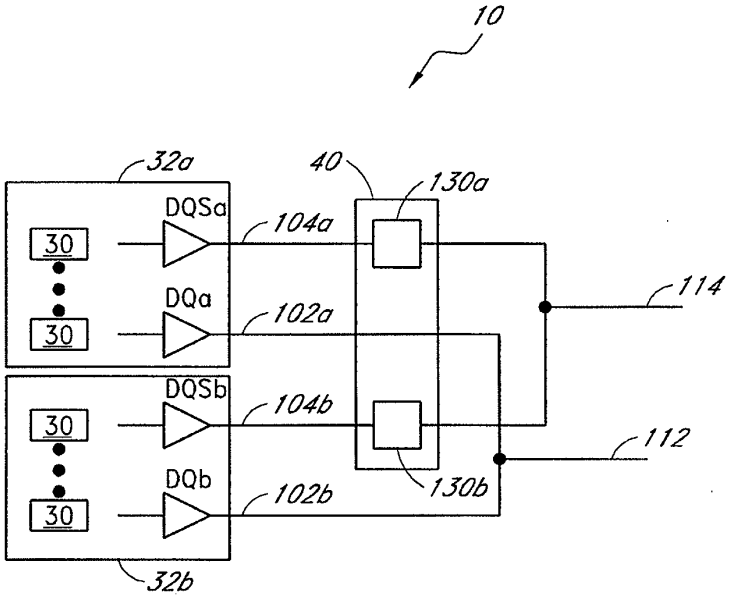

10
32a
40
130a
DQSa
104a
30
30
DQa
102a
114
DQSb
104b
30
30
112
DQb
102b
130b
32b

FIG. 8A

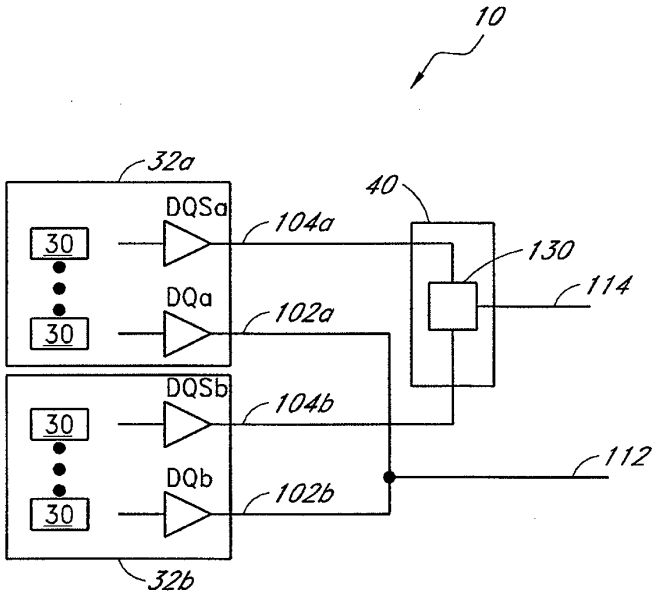

10
32a
40
DQSa
104a
130
30
30
114
DQa
102a
DQSb
104b
30
30
112
DQb
102b
32b

FIG. 8B

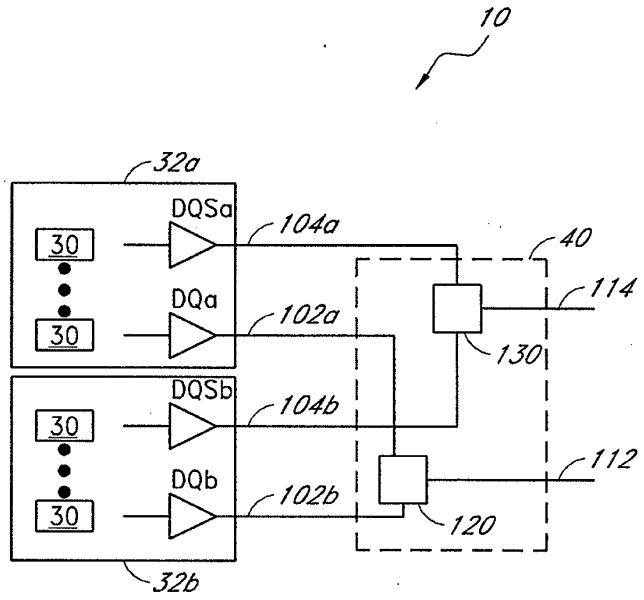

10
32a
DQSa
104a
40
30
DQa
102a
114
30
130
DQSb
104b
30
112
DQb
102b
30
120
32b

FIG. 8C

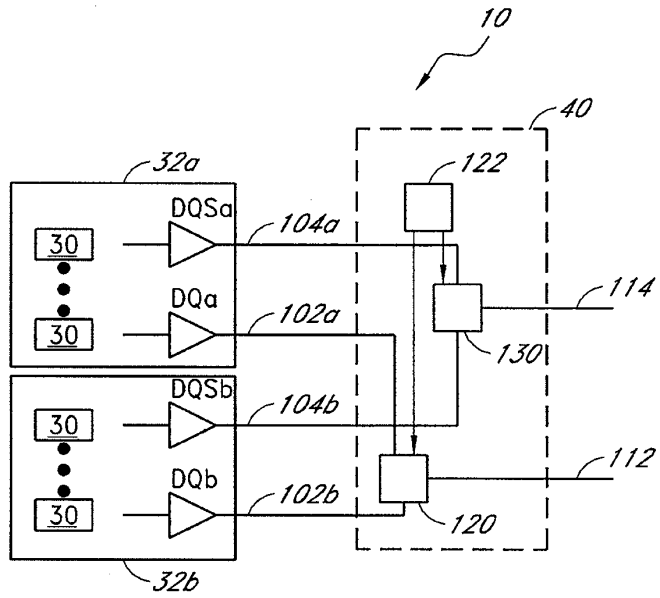

10
40
32a
122
DQSa
104a
30
114
DQa
102a
30
130
DQSb
104b
30
112
DQb
102b
30
120
32b

FIG. 8D

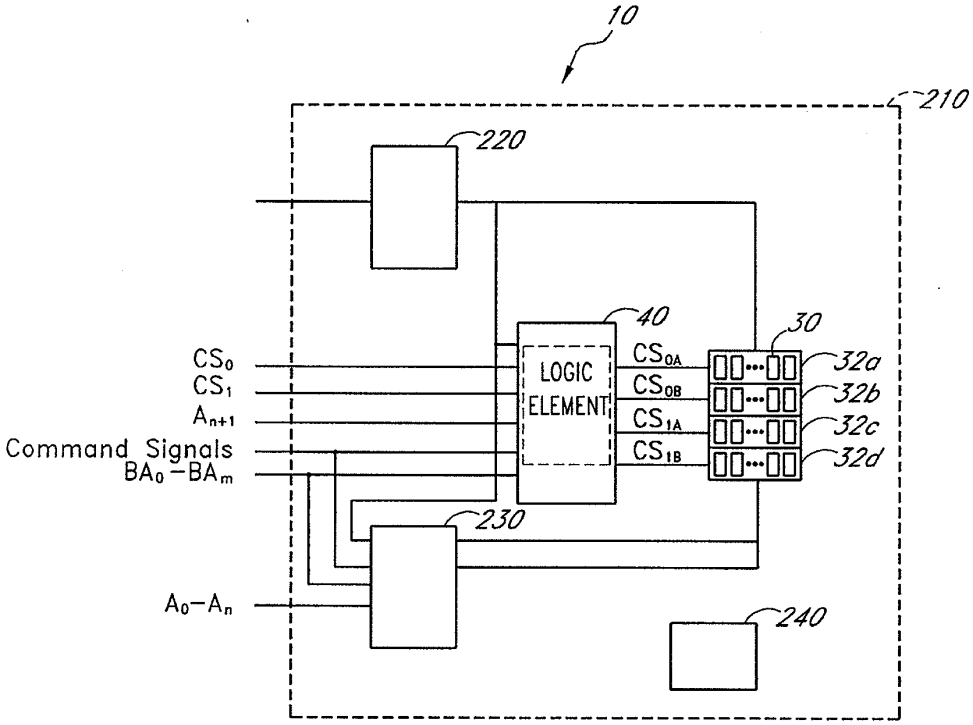

10
210
220
40
30
LOGIC ELEMENT
CS_0
CS_1
A_{n+1}
Command Signals
BA_0-BA_m
CS_{0A}
CS_{0B}
CS_{1A}
CS_{1B}
32a
32b
32c
32d
230
A_0-A_n
240

FIG. 9A

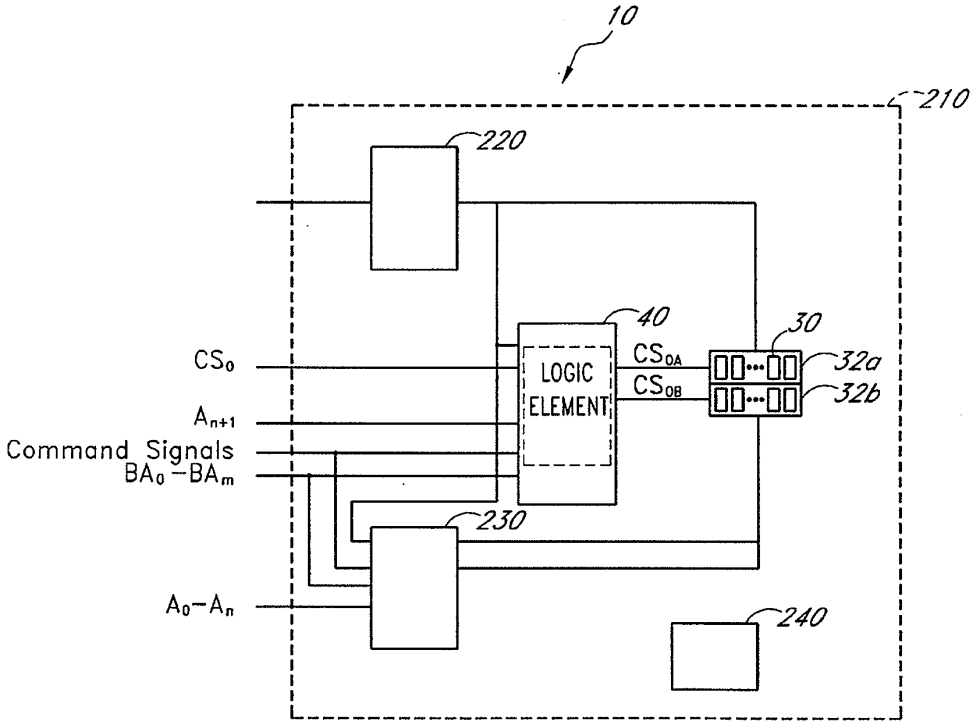

10
210
220
40
30
LOGIC ELEMENT
CS_0
A_{n+1}
Command Signals
BA_0-BA_m
CS_{0A}
CS_{0B}
32a
32b
230
A_0-A_n
240

FIG. 9B

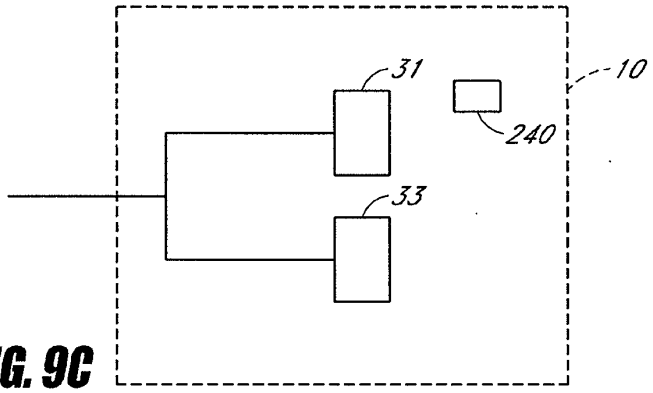


FIG. 9C

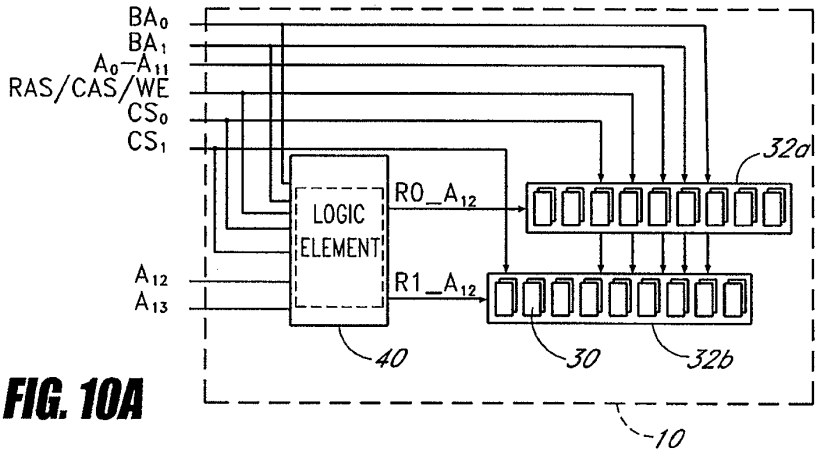


FIG. 10A

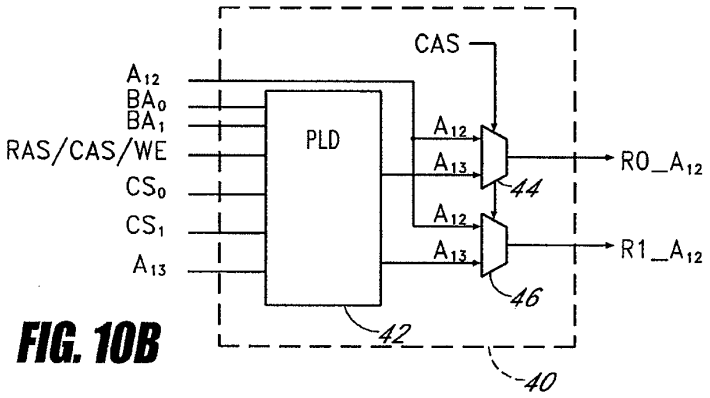


FIG. 10B

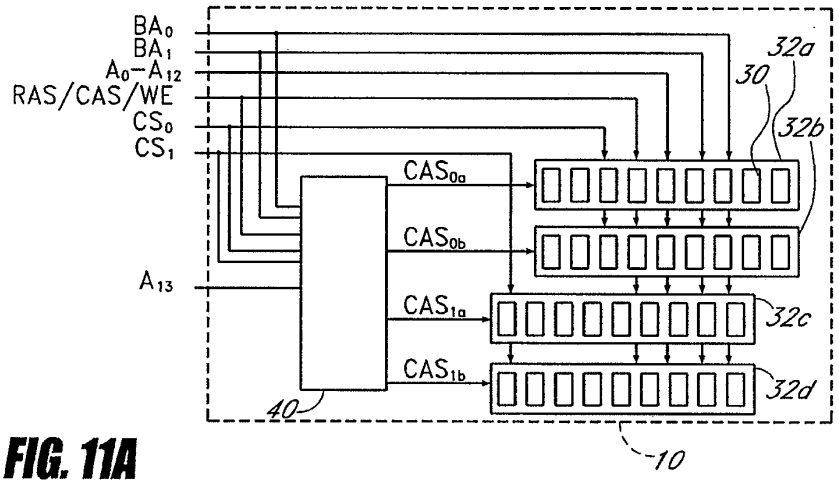


FIG. 11A

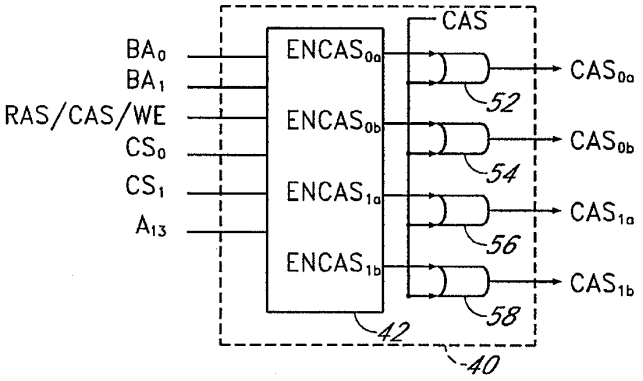


FIG. 11B

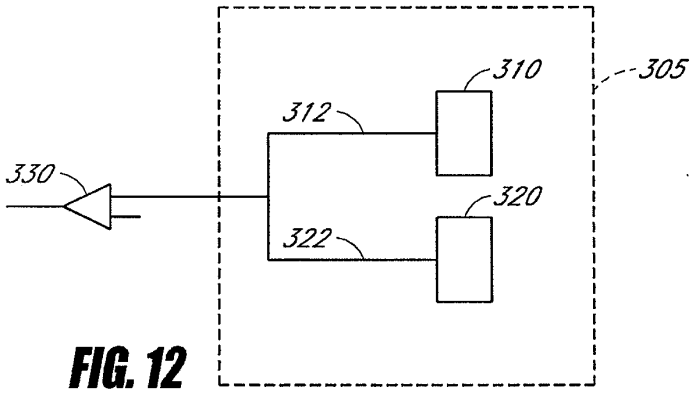


FIG. 12

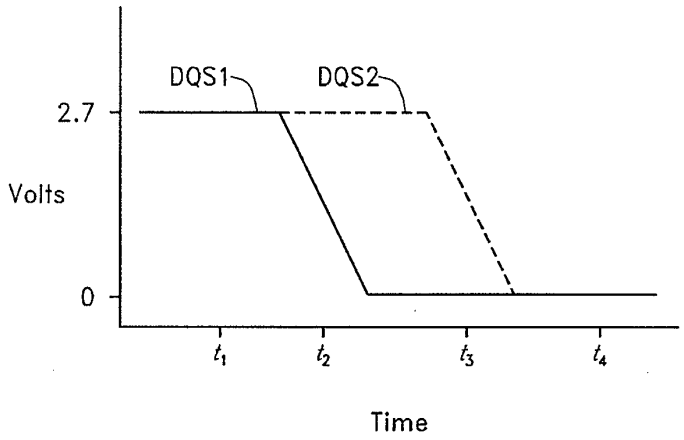


FIG. 13

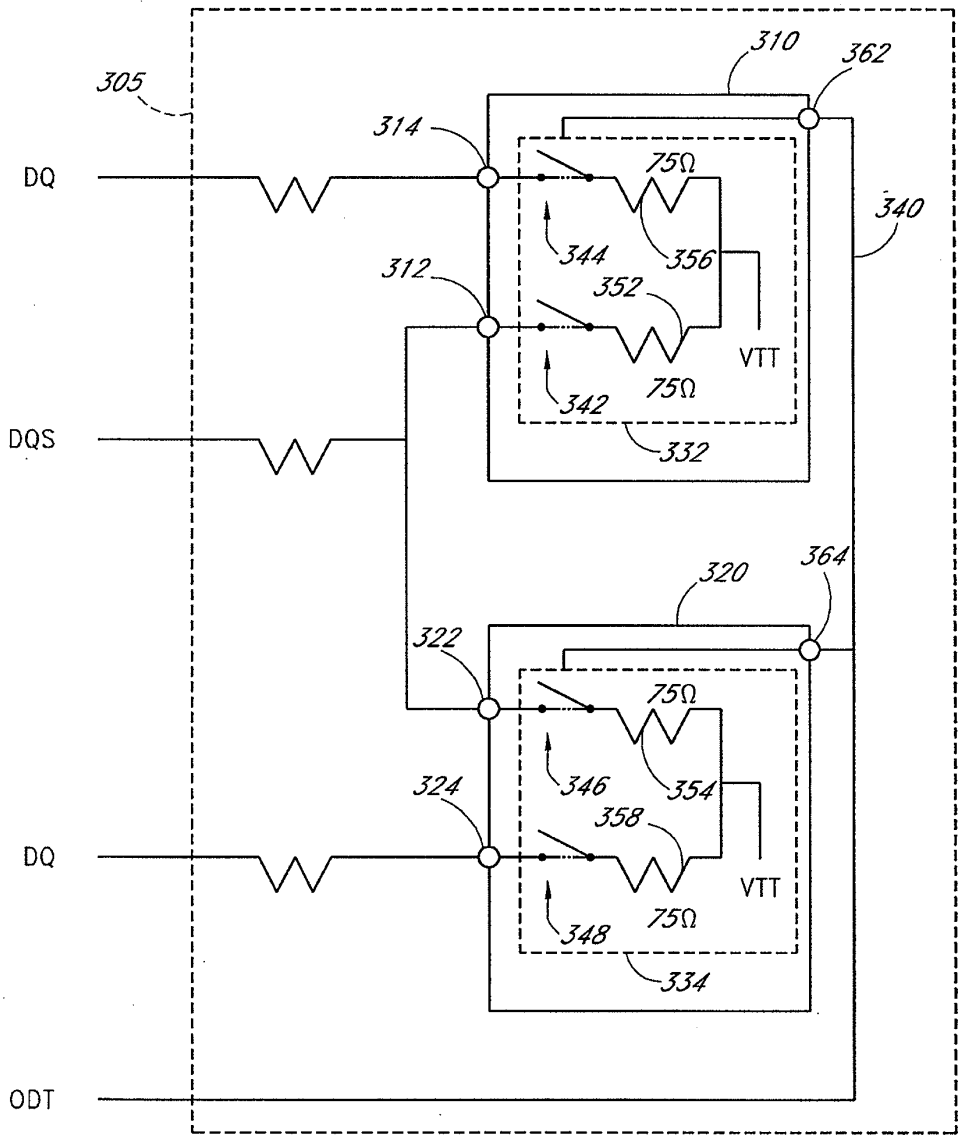

305
310
362
314
75Ω
340
DQ
344
356
312
352
VTT
75Ω
342
DQS
332
320
364
322
75Ω
346
354
324
358
DQ
VTT
75Ω
348
334
ODT

FIG. 14

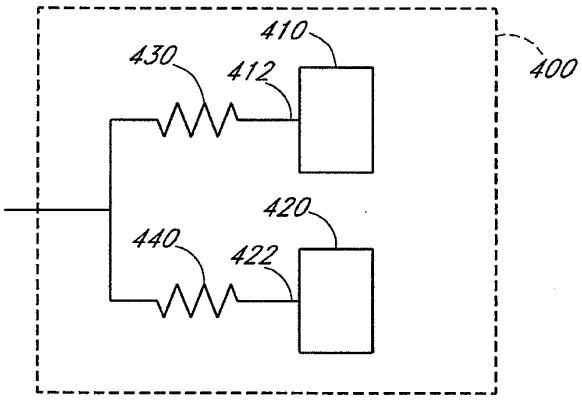


FIG. 15

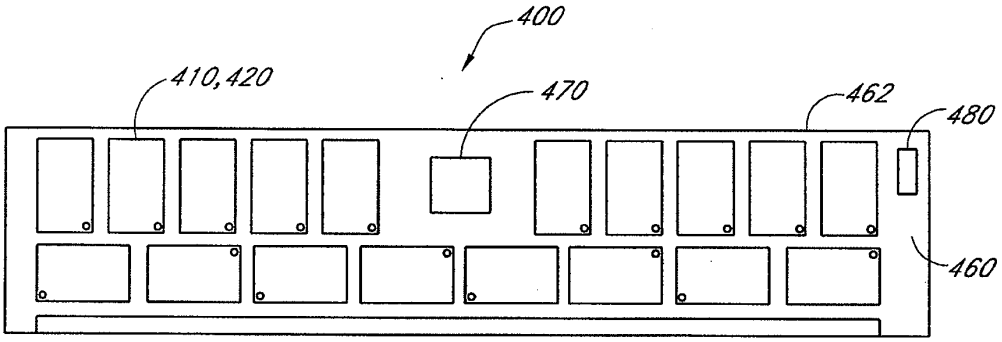


FIG. 16A

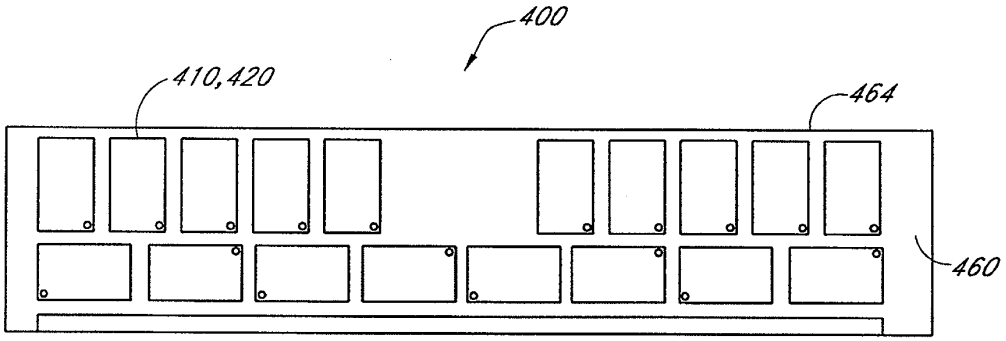


FIG. 16B

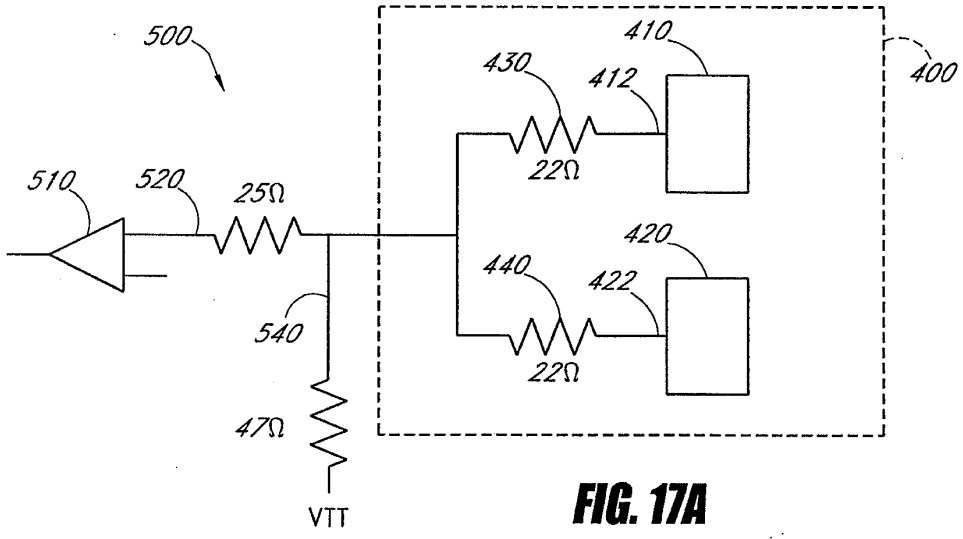


FIG. 17A

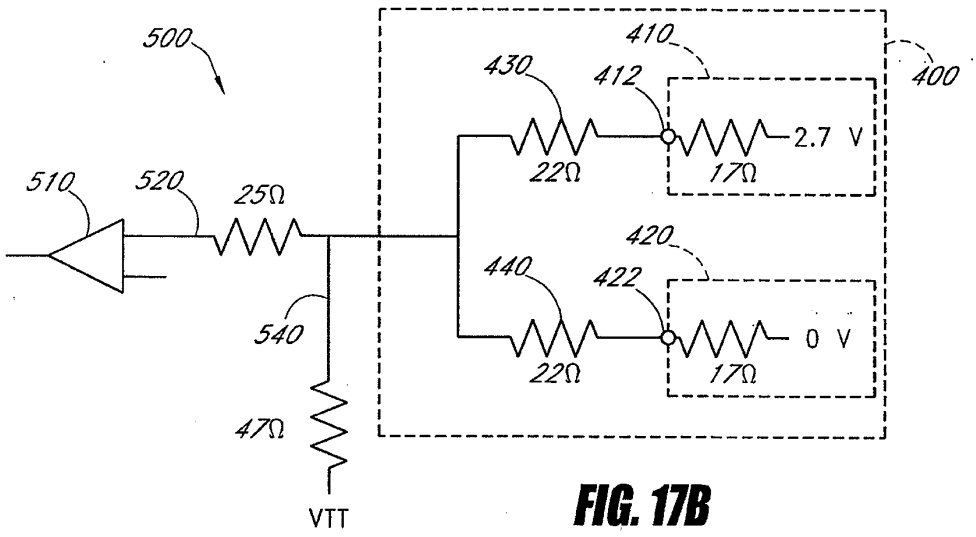


FIG. 17B

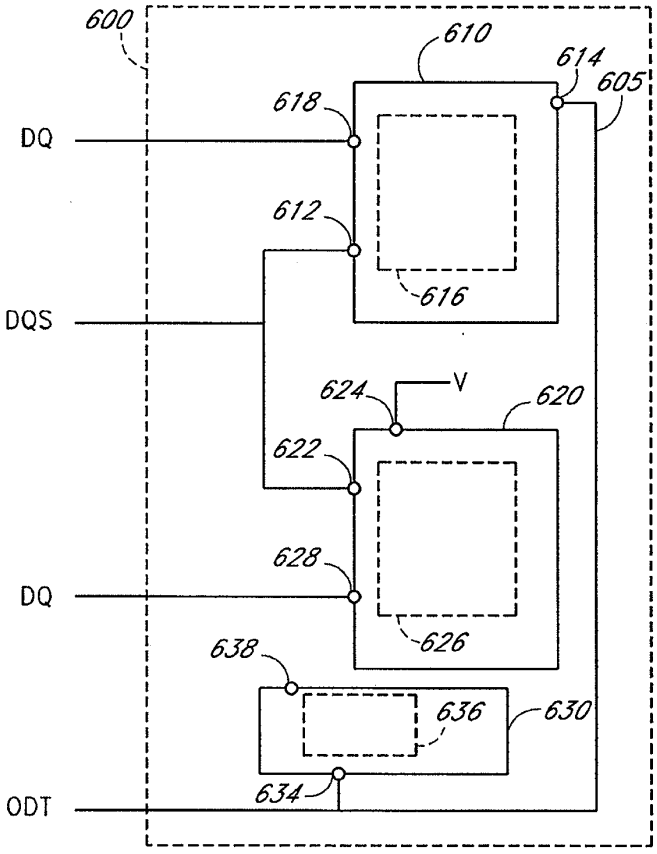

600
610
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DQ
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DQS
624
V
620
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628
DQ
626
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636
630
634
ODT

FIG. 18

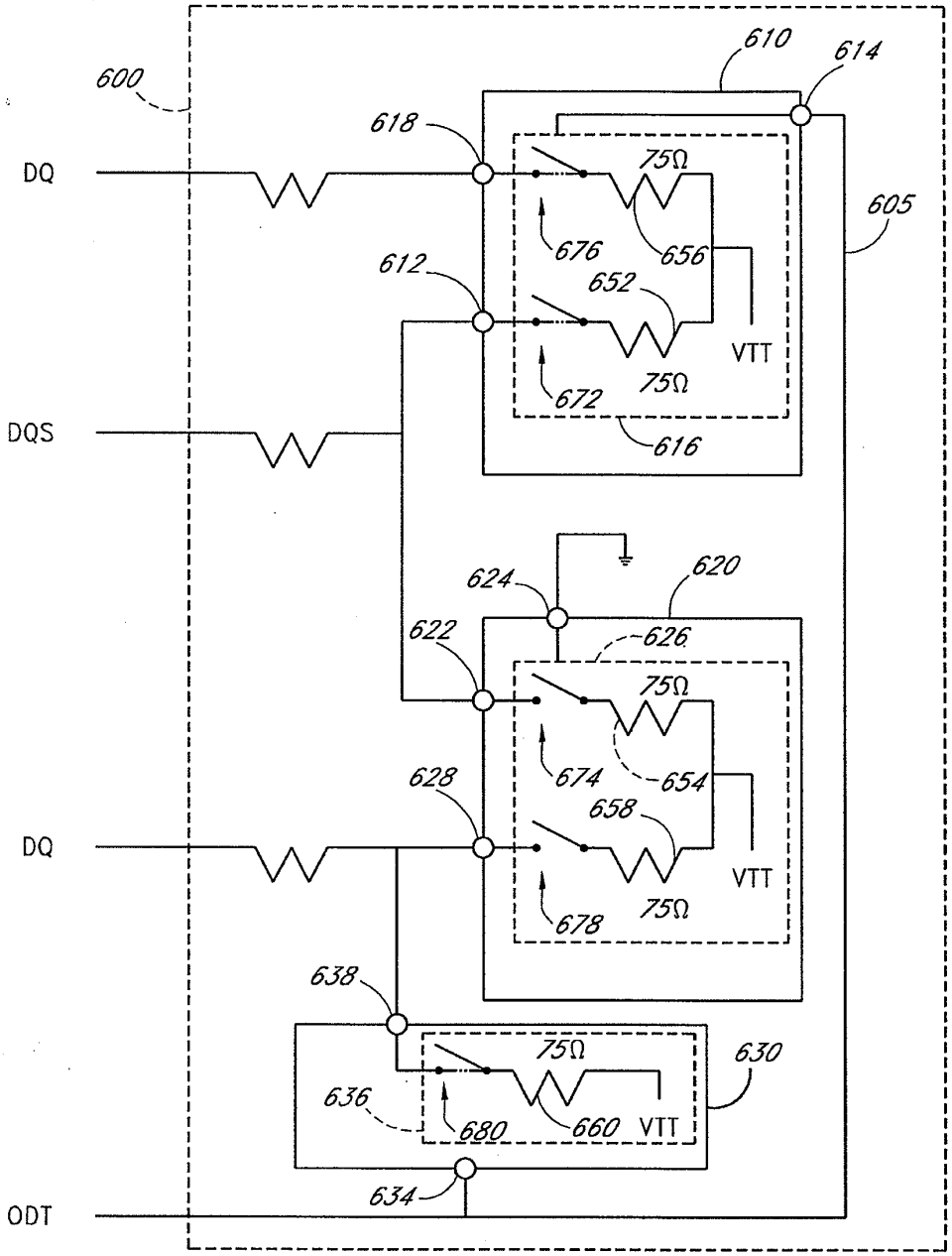

600
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VTT
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DQS
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622
626
75Ω
674
654
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DQ
VTT
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75Ω
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660
VTT
634
ODT

FIG. 19

Electronic Patent Application Fee Transmittal	
Application Number:	
Filing Date:	
Title of Invention:	LOAD-REDUCING CIRCUIT FOR MEMORY MODULE
First Named Inventor/Applicant Name:	Jefferey C. Solomon
Filer:	Jamie Jie Zheng
Attorney Docket Number:	NETL.018P2C7
Filed as Large Entity	

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Utility application filing	1011	1	280	280
Utility Search Fee	1111	1	600	600
Utility Examination Fee	1311	1	720	720
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
		Total in USD ($)		**1600**

Electronic Acknowledgement Receipt

EFS ID:	16636180
Application Number:	13971231
International Application Number:	
Confirmation Number:	2072
Title of Invention:	LOAD-REDUCING CIRCUIT FOR MEMORY MODULE
First Named Inventor/Applicant Name:	Jefferey C. Solomon
Customer Number:	79141
Filer:	Jamie Jie Zheng
Filer Authorized By:	
Attorney Docket Number:	NETL.018P2C7
Receipt Date:	20-AUG-2013
Filing Date:	
Time Stamp:	15:36:51
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	$1600
RAM confirmation Number	2309
Deposit Account	
Authorized User	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)

1	Application Data Sheet	2013-08-20_ApplicationDataSheet_NETL018P2C7.pdf	1438247 af814c44d030e00ced7f70f50810e0511c188fe2	no	7
Warnings:					
Information:					
2		2013-08-20_Specification_NETL018P2C7.pdf	11691549 ce9130252c1812e83d84daeb1d2dfb811b02d436	yes	56
	Multipart Description/PDF files in .zip description				
	Document Description		**Start**	**End**	
	Specification		1	53	
	Claims		54	55	
	Abstract		56	56	
Warnings:					
Information:					
3	Drawings-only black and white line drawings	2013-08-20_Drawings_NETL018P2C7.pdf	542321 af402d9aa0eefd9391b004b980ff65e011911960	no	23
Warnings:					
Information:					
4	Fee Worksheet (SB06)	fee-info.pdf	32767 6796c9372b580f3c94de7b2b138838804657bbbb	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	13704884		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Document code: WFEE

United States Patent and Trademark Office
Sales Receipt for Accounting Date: 09/11/2013

ABALINAN ADJ #00000014 Mailroom Dt: 08/20/2013
Seq No: 2309 Sales Acctg Dt: 08/21/2013 13971231

01	FC : 1011	-280.00	OP
02	FC : 1111	-600.00	OP
03	FC : 1311	-720.00	OP

ASSERTION OF ENTITLEMENT TO SMALL ENTITY STATUS UNDER 37 CFR 1.27
AND
REQUEST FOR REFUND OF EXCESS FEES PAID UNDER 37 CFR 1.26 AND 1.28(a)

Applicant	:	Netlist
App. No.	:	13/971,231
Filed	:	August 20, 2013
For	:	LOAD-REDUCING CIRCUIT FOR MEMORY MODULE
Examiner	:	Unknown
Art Unit	:	Unknown
Conf. No.	:	2072
Docket No.	:	NETL.018P2C7

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

The Assignee of all rights and title in the above-identified patent, Netlist, Inc., is a small entity concern as defined in 37 C.F.R. 1.27(a). Assertion of entitlement to small entity status under 37 C.F.R. 1.27(c) is hereby made in this application.

Applicants hereby request a refund of a portion of the basic filing fee, utility search fee and utility examination fee paid on August 20, 2013 pursuant to 37 C.F.R. § 1.26 and 1.28(a) based on establishment of small entity status.

Applicants acknowledge the duty to file notification of a loss of entitlement to small entity status in the patent prior to paying, or at the time of paying, any maintenance fee due after the date on which status as a small entity is no longer appropriate.

Respectfully submitted,

Date: August 29, 2013

/Jamie J. Zheng/ 51167
Jamie J. Zheng (Reg. No.)
Customer No. 79141

Electronic Acknowledgement Receipt

EFS ID:	16727603
Application Number:	13971231
International Application Number:	
Confirmation Number:	2072
Title of Invention:	LOAD-REDUCING CIRCUIT FOR MEMORY MODULE
First Named Inventor/Applicant Name:	Jefferey C. Solomon
Customer Number:	79141
Filer:	Jamie Jie Zheng
Filer Authorized By:	
Attorney Docket Number:	NETL.018P2C7
Receipt Date:	29-AUG-2013
Filing Date:	
Time Stamp:	19:43:44
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Assertion of entitlement to small entity status	2013-08-29_Small_Entity_Status_Refund_NETL018P2C7.pdf	74842 35c74878a9fcf3be92de4978ee46bd473ca2ea1d	no	1

Warnings:	
Information:	

Total Files Size (in bytes):	74842

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Document code: WFEE

United States Patent and Trademark Office
Sales Receipt for Accounting Date: 09/11/2013

ABALINAN SALE #00000028 Mailroom Dt: 08/29/2013 13971231

01	FC : 4011	70.00	OP
02	FC : 2111	300.00	OP
03	FC : 2311	360.00	OP

Document code: WFEE

United States Patent and Trademark Office
Sales Receipt for Accounting Date: 09/11/2013

ABALINAN RF #30132933 Mailroom Dt: 09/11/2013 13971231

Credit Card Refund Total: $870.00

Master Card XXXXXXXXXXXX1427

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
13/971,231	08/20/2013	2189	730	NETL.018P2C7	10	2

CONFIRMATION NO. 2072

79141
The Law Office of Jamie Zheng, Ph.D Esq.
P.O. Box 60573
Palo Alto, CA 94306

FILING RECEIPT

OC000000063798629

Date Mailed: 09/17/2013

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Inventor(s)

Jefferey C. Solomon, Irvine, CA;
Jayesh R. Bhakta, Residence Not Provided;

Applicant(s)

Netlist, Inc., Irvine, CA

Assignment For Published Patent Application

Netlist, Inc., Irvine, CA

Power of Attorney: None

Domestic Priority data as claimed by applicant

This application is a CON of 13/287,081 11/01/2011 PAT 8516188
which is a CON of 13/032,470 02/22/2011 PAT 8081536
which is a CON of 12/955,711 11/29/2010 PAT 7916574
which is a CON of 12/629,827 12/02/2009 PAT 7881150
which is a CON of 12/408,652 03/20/2009 PAT 7636274
which is a CON of 11/335,875 01/19/2006 PAT 7532537
which claims benefit of 60/645,087 01/19/2005
and is a CIP of 11/173,175 07/01/2005 PAT 7289386
which claims benefit of 60/588,244 07/15/2004
and is a CIP of 11/075,395 03/07/2005 PAT 7286436
which claims benefit of 60/550,668 03/05/2004
and claims benefit of 60/575,595 05/28/2004
and claims benefit of 60/590,038 07/21/2004

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.) - None.

Samsung Electronics Co., Ltd.
Ex. 1052, p. 98

Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

If Required, Foreign Filing License Granted: 09/11/2013

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 13/971,231**

Projected Publication Date: To Be Determined - pending completion of Missing Parts

Non-Publication Request: No

Early Publication Request: No

**** SMALL ENTITY ****

Title

LOAD-REDUCING CIRCUIT FOR MEMORY MODULE

Preliminary Class

711

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific

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countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

LICENSE FOR FOREIGN FILING UNDER

Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

GRANTED

The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where the conditions for issuance of a license have been met, regardless of whether or not a license may be required as set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign AssetsControl, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

SelectUSA

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The U.S. offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to promote and facilitate business investment. SelectUSA provides information assistance to the international investor community; serves as an ombudsman for existing and potential investors; advocates on behalf of U.S. cities, states, and regions competing for global investment; and counsels U.S. economic development organizations on investment attraction best practices. To learn more about why the United States is the best country in the world to develop

technology, manufacture products, deliver services, and grow your business, visit http://www.SelectUSA.gov or call +1-202-482-6800.

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PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number: 13/971,231

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY FEE($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	70		N/A	
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	300		N/A	
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	360		N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	10 minus 20 =	*	x 40 =	0.00	OR		
INDEPENDENT CLAIMS (37 CFR 1.16(h))	2 minus 3 =	*	x 210 =	0.00			
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			0.00			
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				0.00			
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	730		TOTAL	

APPLICATION AS AMENDED - PART II

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
AMENDMENT A	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE($)	ADDITIONAL FEE($)	OR	RATE($)	ADDITIONAL FEE($)
AMENDMENT B	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
13/971,231	08/20/2013	Jefferey C. Solomon	NETL.018P2C7

CONFIRMATION NO. 2072

79141
The Law Office of Jamie Zheng, Ph.D Esq.
P.O. Box 60573
Palo Alto, CA 94306

FORMALITIES LETTER

OC000000063798630

Date Mailed: 09/17/2013

NOTICE TO FILE MISSING PARTS OF NONPROVISIONAL APPLICATION

FILED UNDER 37 CFR 1.53(b)

Filing Date Granted

Items Required To Avoid Abandonment:

An application number and filing date have been accorded to this application. The item(s) indicated below, however, are missing. Applicant is given **TWO MONTHS** from the date of this Notice within which to file all required items below to avoid abandonment. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a).

- A mailing address for each inventor has not been submitted. A new application data sheet (ADS) in compliance with 37 CFR 1.76 or inventor's oath or declaration in compliance with 37 CFR 1.63 identifying the mailing address and residence (if the inventor lives at a location which is different from where the inventor customarily receives mail) is required.
  Jayesh R. Bhakta

The applicant needs to satisfy supplemental fees problems indicated below.

The required item(s) identified below must be timely submitted to avoid abandonment:

- A surcharge (for late submission of the basic filing fee, search fee, examination fee or inventor's oath or declaration) as set forth in 37 CFR 1.16(f) of $ **70** for a small entity in compliance with 37 CFR 1.27, must be submitted.

SUMMARY OF FEES DUE:

Total fee(s) required within **TWO MONTHS** from the date of this Notice is $ **70** for a small entity
- $ **70** Surcharge.

Items Required To Avoid Processing Delays:

Applicant is notified that the above-identified application contains the deficiencies noted below. No period for reply is set forth in this notice for correction of these deficiencies. However, if a deficiency relates to the inventor's oath or declaration, the applicant must file an oath or declaration in compliance with 37 CFR 1.63, or a substitute statement in compliance with 37 CFR 1.64, executed by or with respect to each actual inventor no later than the expiration of the time period set in the "Notice of Allowability" to avoid abandonment. See 37 CFR 1.53(f).

- A properly executed inventor's oath or declaration has not been received for the following inventor(s):
  Jefferey C. Solomon

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Jayesh R. Bhakta

Applicant may submit the inventor's oath or declaration at any time before the Notice of Allowance and Fee(s) Due, PTOL-85, is mailed.

Replies must be received in the USPTO within the set time period or must include a proper Certificate of Mailing or Transmission under 37 CFR 1.8 with a mailing or transmission date within the set time period. For more information and a suggested format, see Form PTO/SB/92 and MPEP 512.

Replies should be mailed to:

Mail Stop Missing Parts
Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

Registered users of EFS-Web may alternatively submit their reply to this notice via EFS-Web.
https://sportal.uspto.gov/authenticate/AuthenticateUserLocalEPF.html

For more information about EFS-Web please call the USPTO Electronic Business Center at **1-866-217-9197** or visit our website at http://www.uspto.gov/ebc.

If you are not using EFS-Web to submit your reply, you must include a copy of this notice.

/fasrat/

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

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RESPONSE TO NOTICE TO FILE MISSING PARTS

Applicant	:	Netlist
App. No.	:	13/971,231
Filed	:	August 20, 2013
For	:	LOAD-REDUCING CIRCUIT FOR MEMORY MODULE
Examiner	:	Unknown
Art Unit	:	2189
Conf. No.	:	2072
Docket No.	:	NETL.018P2C7

CERTIFICATE OF EFS WEB TRANSMISSION

I hereby certify that this correspondence and any other attachment noted on the Automated Acknowledgement Receipt, is being transmitted from within the Pacific Time zone to the Commissioner for Patents via the EFS Web Server on:

October 18, 2013

(Date)

/Jamie J. Zheng/

Jamie J. Zheng, Reg. No. 51167

Mail Stop Missing Parts
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

In response to the Notice to File Missing Parts mailed on September 10, 2013, Applicant herewith submits the following:

(X) A revised application data sheet showing change made to correct an error in the original application data sheet where the state of residence for inventor Jayesh Bhakta was not entered.

(X) Signed declaration

(X) Surcharge paid via EFS Web.

The Commissioner is hereby authorized to charge any additional fees to Deposit Account No. 50-5963 for Inscape IP, APC.

Date: October 18, 2013

/Jamie J. Zheng/ 51167

Jamie J. Zheng (Reg. No.)
Customer No. 79141
(650) 273-6008

PTO/AIA/14 (08-12)
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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	NETL.018P2C7
	Application Number	
Title of Invention	LOAD-REDUCING CIRCUIT FOR MEMORY MODULE	

The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76.
This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.

Secrecy Order 37 CFR 5.2

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

Inventor Information:

Inventor 1 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Jefferey	C.	Solomon	

Residence Information (Select One) ◉ US Residency ○ Non US Residency ○ Active US Military Service

City	Irvine	State/Province	CA	Country of Residence	US

Mailing Address of Inventor:

Address 1	16 Silver Fir		
Address 2			
City	Irvine	State/Province	CA
Postal Code	92604	Country	US

Inventor 2 Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Jayesh	R.	Bhakta	

Residence Information (Select One) ◉ US Residency ○ Non US Residency ○ Active US Military Service

City	Cerritos	State/Province	CA	Country of Residence	US

Mailing Address of Inventor:

Address 1	12220 Rose Street		
Address 2			
City	Cerritos	State/Province	CA
Postal Code	90703	Country	US

All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the **Add** button. Add

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below.
For further information see 37 CFR 1.33(a).

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	NETL.018P2C7
	Application Number	
Title of Invention	LOAD-REDUCING CIRCUIT FOR MEMORY MODULE	

☐ **An Address is being provided for the correspondence Information of this application.**			
Customer Number	79141		
Email Address	jz@jzpatent.com	Add Email	Remove Email

Application Information:

Title of the Invention	LOAD-REDUCING CIRCUIT FOR MEMORY MODULE		
Attorney Docket Number	NETL.018P2C7	**Small Entity Status Claimed**	☒
Application Type	Nonprovisional		
Subject Matter	Utility		
Suggested Class (if any)		**Sub Class (if any)**	
Suggested Technology Center (if any)			
Total Number of Drawing Sheets (if any)	23	**Suggested Figure for Publication (if any)**	8D

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)
☐ **Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32).
Either enter Customer Number or complete the Representative Name section below. If both sections are completed the customer Number will be used for the Representative Information during processing.

Please Select One:	◉ Customer Number	○ US Patent Practitioner	○ Limited Recognition (37 CFR 11.9)
Customer Number	79141		

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, or 365(c) or indicate National Stage entry from a PCT application. Providing this information in the application data sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78.

Prior Application Status	Pending		Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
	Continuation of	13287081	2011-11-01

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	NETL.018P2C7
	Application Number	
Title of Invention	LOAD-REDUCING CIRCUIT FOR MEMORY MODULE	

Prior Application Status	Patented				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
13287081	Continuation of	13032470	2011-02-22	8081536	2011-12-20
Prior Application Status	Patented				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
13032470	Continuation of	12955711	2010-11-29	7916574	2011-03-29
Prior Application Status	Patented				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
12955711	Continuation of	12629827	2009-12-02	7881150	2011-02-01
Prior Application Status	Patented				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
12629827	Continuation of	12408652	2009-03-20	7636274	2009-12-22
Prior Application Status	Patented				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
12408652	Continuation of	11335875	2006-01-19	7532537	2009-05-12
Prior Application Status	Expired				Remove
Application Number	Continuity Type		Prior Application Number		Filing Date (YYYY-MM-DD)
11335875	non provisional of		60645087		2005-01-19
Prior Application Status	Patented				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
11335875	Continuation in part of	11173175	2005-07-01	7289386	2007-10-30
Prior Application Status	Expired				Remove
Application Number	Continuity Type		Prior Application Number		Filing Date (YYYY-MM-DD)
11173175	non provisional of		60588244		2004-07-15
Prior Application Status	Patented				Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
11173175	Continuation in part of	11075395	2005-03-07	7286436	2007-10-23
Prior Application Status	Expired				Remove
Application Number	Continuity Type		Prior Application Number		Filing Date (YYYY-MM-DD)
11075395	non provisional of		60550668		2004-03-05
Prior Application Status	Expired				Remove
Application Number	Continuity Type		Prior Application Number		Filing Date (YYYY-MM-DD)
11075395	non provisional of		60575595		2004-05-28

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	NETL.018P2C7
	Application Number	
Title of Invention	LOAD-REDUCING CIRCUIT FOR MEMORY MODULE	

Prior Application Status	Expired		Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
11075395	non provisional of	60590038	2004-07-21

Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the **Add** button. Add

Foreign Priority Information:

This section allows for the applicant to claim benefit of foreign priority and to identify any prior foreign application for which priority is not claimed. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55(a).

Remove

Application Number	Country[i]	Filing Date (YYYY-MM-DD)	Priority Claimed
			(•) Yes ( ) No

Additional Foreign Priority Data may be generated within this form by selecting the **Add** button. Add

Authorization to Permit Access:

☐ Authorization to Permit Access to the Instant Application by the Participating Offices

If checked, the undersigned hereby grants the USPTO authority to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the World Intellectual Property Office (WIPO), and any other intellectual property offices in which a foreign application claiming priority to the instant patent application is filed access to the instant patent application. See 37 CFR 1.14(c) and (h). This box should not be checked if the applicant does not wish the EPO, JPO, KIPO, WIPO, or other intellectual property office in which a foreign application claiming priority to the instant patent application is filed to have access to the instant patent application.

In accordance with 37 CFR 1.14(h)(3), access will be provided to a copy of the instant patent application with respect to: 1) the instant patent application-as-filed; 2) any foreign application to which the instant patent application claims priority under 35 U.S.C. 119(a)-(d) if a copy of the foreign application that satisfies the certified copy requirement of 37 CFR 1.55 has been filed in the instant patent application; and 3) any U.S. application-as-filed from which benefit is sought in the instant patent application.

In accordance with 37 CFR 1.14(c), access may be provided to information concerning the date of filing this Authorization.

Applicant Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	NETL.018P2C7
	Application Number	
Title of Invention	LOAD-REDUCING CIRCUIT FOR MEMORY MODULE	

Applicant 1 Remove

If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section.

Clear

(●) Assignee	( ) Legal Representative under 35 U.S.C. 117	( ) Joint Inventor
( ) Person to whom the inventor is obligated to assign.	( ) Person who shows sufficient proprietary interest	

If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:

Name of the Deceased or Legally Incapacitated Inventor :

If the Applicant is an Organization check here. ☒

Organization Name	Netlist, Inc.		
Mailing Address Information:			
Address 1	51 Discovery, #150		
Address 2			
City	Irvine	**State/Province**	CA
Country	US	Postal Code	92618
Phone Number	949-435-0025	Fax Number	
Email Address	gsasaki@netlist.com		

Additional Applicant Data may be generated within this form by selecting the Add button. Add

Non-Applicant Assignee Information:

Providing assignment information in this section does not subsitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Assignee 1

Complete this section only if non-applicant assignee information is desired to be included on the patent application publication in accordance with 37 CFR 1.215(b). Do not include in this section an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest), as the patent application publication will include the name of the applicant(s).

Remove

If the Assignee is an Organization check here. ☐

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	NETL.018P2C7
	Application Number	
Title of Invention	LOAD-REDUCING CIRCUIT FOR MEMORY MODULE	

Prefix	**Given Name**	Middle Name	**Family Name**	Suffix

Mailing Address Information:

Address 1			
Address 2			
City		**State/Province**	
Country i		Postal Code	
Phone Number		Fax Number	
Email Address			

Additional Assignee Data may be generated within this form by selecting the Add button. Add

Remove

Signature:

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications

Signature	/Jamie J. Zheng/			Date (YYYY-MM-DD)	2013-10-18
First Name	Jamie	Last Name	Zheng	Registration Number	51167

Additional Signature may be generated within this form by selecting the Add button. Add

This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

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Ex. 1052, p. 112

Customer No. 79141
Attorney Docket No.: NETL.018P2C7

Modified PTO/AIA/01 (06-12)

DECLARATION FOR UTILITY OR DESIGN APPLICATION

Title of Invention	LOAD-REDUCING CIRCUIT FOR MEMORY MODULE

As a below named inventor, I hereby declare that:

This declaration is directed to:

☐ The attached application, or

■ United States application or PCT international application number 13/971,231 filed on August 20, 2013.

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

Note to Inventor: 37 C.F.R. § 1.63(c) states: "A person may not execute an oath or declaration for an application unless that person has reviewed and understands the contents of the application, including the claims, and is aware of the duty to disclose to the Office all information known to the person to be material to patentability as defined in § 1.56."

First Inventor (Legal Name): Jeffrey C. Solomon

Signature: Jeffrey C. Solomon Date (Optional): 10-14-2013

Second Inventor (Legal Name): Jayesh R. Bhakta

Signature: Jayesh Bhakta Date (Optional): 10-14-2013

Electronic Patent Application Fee Transmittal

Application Number:	13971231
Filing Date:	20-Aug-2013
Title of Invention:	LOAD-REDUCING CIRCUIT FOR MEMORY MODULE
First Named Inventor/Applicant Name:	Jefferey C. Solomon
Filer:	Jamie Jie Zheng
Attorney Docket Number:	NETL.018P2C7

Filed as Small Entity

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Late Filing Fee for Oath or Declaration	2051	1	70	70
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
			Total in USD ($)	**70**

Electronic Acknowledgement Receipt

EFS ID:	17174430
Application Number:	13971231
International Application Number:	
Confirmation Number:	2072
Title of Invention:	LOAD-REDUCING CIRCUIT FOR MEMORY MODULE
First Named Inventor/Applicant Name:	Jefferey C. Solomon
Customer Number:	79141
Filer:	Jamie Jie Zheng
Filer Authorized By:	
Attorney Docket Number:	NETL.018P2C7
Receipt Date:	19-OCT-2013
Filing Date:	20-AUG-2013
Time Stamp:	03:06:15
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	$70
RAM confirmation Number	8605
Deposit Account	
Authorized User	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)

1	Applicant Response to Pre-Exam Formalities Notice	2013-10-18_Rsps_NTFMP_NETL018P2C7.pdf	75766 7322aced2c896a3dab2391476076362817511930	no	1
Warnings:					
Information:					
2	Application Data Sheet	2013-10-18_ApplicationDataSheet_Rev_NETL018P2C7.pdf	2792327 a82a001993275b7139f8e2df66a5a6434048f9fc	no	7
Warnings:					
Information:					
This is not an USPTO supplied ADS fillable form					
3	Oath or Declaration filed	2013-10-15_Declaration_Signed_NETL018P2C7.pdf	393053 6d21a4c728c4e7fe0fa43f25a82f93f87bdf6da3	no	1
Warnings:					
The page size in the PDF is too large. The pages should be 8.5 x 11 or A4. If this PDF is submitted, the pages will be resized upon entry into the Image File Wrapper and may affect subsequent processing					
Information:					
4	Fee Worksheet (SB06)	fee-info.pdf	29957 726d7f9fda165057ec0da15d7f08359ee61ad100	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	3291103		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

<u>New Applications Under 35 U.S.C. 111</u>
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

<u>National Stage of an International Application under 35 U.S.C. 371</u>
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

<u>New International Application Filed with the USPTO as a Receiving Office</u>
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number: 13/971,231

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY FEE($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	70		N/A	
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	300		N/A	
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	360		N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	10 minus 20 =	*	x 40 =	0.00	OR		
INDEPENDENT CLAIMS (37 CFR 1.16(h))	2 minus 3 =	*	x 210 =	0.00			
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			0.00			
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				0.00			
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	730		TOTAL	

APPLICATION AS AMENDED - PART II

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
AMENDMENT A	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE($)	ADDITIONAL FEE($)	OR	RATE($)	ADDITIONAL FEE($)
AMENDMENT B	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.

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United States Patent and Trademark Office
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Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
13/971,231	08/20/2013	2189	800	NETL.018P2C7	10	2

CONFIRMATION NO. 2072

79141
The Law Office of Jamie Zheng, Ph.D Esq.
P.O. Box 60573
Palo Alto, CA 94306

UPDATED FILING RECEIPT

OC000000064541118

Date Mailed: 10/28/2013

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Inventor(s)

Jefferey C. Solomon, Irvine, CA;
Jayesh R. Bhakta, Cerritos, CA;

Applicant(s)

Netlist, Inc., Irvine, CA

Assignment For Published Patent Application

Netlist, Inc., Irvine, CA

Power of Attorney: None

Domestic Priority data as claimed by applicant

This application is a CON of 13/287,081 11/01/2011 PAT 8516188
which is a CON of 13/032,470 02/22/2011 PAT 8081536
which is a CON of 12/955,711 11/29/2010 PAT 7916574
which is a CON of 12/629,827 12/02/2009 PAT 7881150
which is a CON of 12/408,652 03/20/2009 PAT 7636274
which is a CON of 11/335,875 01/19/2006 PAT 7532537
which claims benefit of 60/645,087 01/19/2005
and is a CIP of 11/173,175 07/01/2005 PAT 7289386
which claims benefit of 60/588,244 07/15/2004
and is a CIP of 11/075,395 03/07/2005 PAT 7286436
which claims benefit of 60/550,668 03/05/2004
and claims benefit of 60/575,595 05/28/2004
and claims benefit of 60/590,038 07/21/2004

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.) - None.

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Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

If Required, Foreign Filing License Granted: 09/11/2013

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 13/971,231**

Projected Publication Date: 02/06/2014

Non-Publication Request: No

Early Publication Request: No

**** SMALL ENTITY ****

Title

LOAD-REDUCING CIRCUIT FOR MEMORY MODULE

Preliminary Class

711

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific

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countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

LICENSE FOR FOREIGN FILING UNDER

Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

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This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

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NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

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United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
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Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
13/971,231	08/20/2013	Jefferey C. Solomon	NETL.018P2C7

CONFIRMATION NO. 2072

79141
The Law Office of Jamie Zheng, Ph.D Esq.
P.O. Box 60573
Palo Alto, CA 94306

PUBLICATION NOTICE

OC000000066486320

Title:LOAD-REDUCING CIRCUIT FOR MEMORY MODULE

Publication No.US-2014-0040569-A1
Publication Date:02/06/2014

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

The publication may be accessed through the USPTO's publically available Searchable Databases via the Internet at www.uspto.gov. The direct link to access the publication is currently http://www.uspto.gov/patft/.

The publication process established by the Office does not provide for mailing a copy of the publication to applicant. A copy of the publication may be obtained from the Office upon payment of the appropriate fee set forth in 37 CFR 1.19(a)(1). Orders for copies of patent application publications are handled by the USPTO's Office of Public Records. The Office of Public Records can be reached by telephone at (703) 308-9726 or (800) 972-6382, by facsimile at (703) 305-8759, by mail addressed to the United States Patent and Trademark Office, Office of Public Records, Alexandria, VA 22313-1450 or via the Internet.

In addition, information on the status of the application, including the mailing date of Office actions and the dates of receipt of correspondence filed in the Office, may also be accessed via the Internet through the Patent Electronic Business Center at www.uspto.gov using the public side of the Patent Application Information and Retrieval (PAIR) system. The direct link to access this status information is currently http://pair.uspto.gov/. Prior to publication, such status information is confidential and may only be obtained by applicant using the private side of PAIR.

Further assistance in electronically accessing the publication, or about PAIR, is available by calling the Patent Electronic Business Center at 1-866-217-9197.

Office of Data Managment, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

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PTO/SB/08a/b(07-09)
Approved for use through 7/31/2012. OMB 0651-0031
US Patent & Trademark Office; U.S. DEPARTMENT OF COMMERCE
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Substitute for form 1449/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 1 of 3

Complete if Known	
Application Number	13/971,231
Filing Date	August 20, 2013
First Named Inventor	Jayesh R. Bhakta
Art Unit	2189
Examiner Name	Unknown
Attorney Docket Number	NETL.018P2C7

US PATENT DOCUMENTS

Examiner Initials *	Cite No. [1]	Document Number Number-Kind Code [2] (if known)	Publication Date (MM-DD-YYYY)	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	1	5345412	09-06-1994	Shiratsuchi	
	2	5537584	07-16-1996	Miyai et al.	
	3	5617559	04-01-1997	Le et al.	
	4	5649159	07-15-1997	Le et al.	
	5	5717851	02-10-1998	Yishay et al.	
	6	5724604	03-03-1998	Moyer	
	7	5729716	05-17-1998	Lee et al.	
	8	5784705	07-21-1998	Leung, Wingyu	
	9	5802541	09-01-1998	Reed	
	10	5973392	10-26-1999	Senba et al.	
	11	6173357	01-09-2011	Ju	
	12	6260127	07-10-2001	Olarig et al.	
	13	6446158	09-03-2002	Karabatsos	
	14	6553449	04-22-2003	Dodd et al.	
	15	6618791	09-09-2003	Dodd et al.	
	16	6717855	04-06-2004	Underwood	
	17	6788592	09-07-2004	Nakata et al.	
	18	6948084	09-20-2005	Manapat et al	
	19	7130308	10-31-2006	Haddock et al.	
	20	7133960	11-07-2006	Thompson et al.	
	21	7379361	05-27-2008	Co et al.	
	22	20050010737	01-01-2005	Ware et al.	
	23	20070293094	12-01-2007	Aekins, Robert A.	

US PATENT APPLICATIONS

Examiner Initials *	Cite No. [1]	Document Number Number-Kind Code [2] (if known)	Filing Date (MM-DD-YYYY)	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	24	95/001,758	09-14-2011	Owned by Netlist, Inc.	
	25	13/154,172	06-06-2011	Owned by Netlist, Inc.	
	26	13/287,042	11-01-2011	Owned by Netlist, Inc.	
	27	13/473,413	05-16-2012	Owned by Netlist, Inc.	
	28	13/032,470	02-22-2011	Owned by Netlist, Inc.	
	29	13/287,081	11-01-2011	Owned by Netlist, Inc.	
	30	13/971,231	08-20-2013	Owned by Netlist, Inc.	
	31	13/412,243	03-05-2012	Owned by Netlist, Inc.	
	32	13/183,253	07-14-2011	Owned by Netlist, Inc.	
	33	13/745,790	01-19-2013	Owned by Netlist, Inc.	

EXAMINER **DATE CONSIDERED**

* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1] Applicant's unique citation designation number (optional). [2] See Kinds Codes of USPTO Patents Documents at www.uspto.gov or MPEP 901.04. [3] Enter Office that issued the document, by the two-letter code (WIPO Standard ST. 3). [4] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5] Kind of document by the appropriate symbols as indicated on the document and WIPO Standard ST. 16 if possible. [6] Applicant is to place a check mark here if English language Translation is attached.

PTO/SB/08a/b(07-09)
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US Patent & Trademark Office; U.S. DEPARTMENT OF COMMERCE
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Substitute for form 1449/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 2 of 3

Complete if Known	
Application Number	13/971,231
Filing Date	August 20, 2013
First Named Inventor	Jayesh R. Bhakta
Art Unit	2189
Examiner Name	Unknown
Attorney Docket Number	NETL.018P2C7

US PATENT APPLICATIONS

Examiner Initials *	Cite No. [1]	Document Number Number-Kind Code [2] (if known)	Filing Date (MM-DD-YYYY)	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	34	14/229,844	3/29/2014	Owned by Netlist, Inc.	
	35	12/504,131	7/16/2009	Owned by Netlist, Inc.	
	36	12/761,179	4/15/2010	Owned by Netlist, Inc.	
	37	13/970,606	8/20/2013	Owned by Netlist, Inc.	
	38	13/288,850	11/3/2011	Owned by Netlist, Inc.	
	39	13/411,344	3/2/2012	Owned by Netlist, Inc.	

FOREIGN PATENT DOCUMENTS

Examiner Initials *	Cite No. [1]	Foreign Patent Document Country Code[3]-Number[4]-Kind Code [5] (if known)	Publication Date (MM-DD-YYYY)	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]
	40	JP2009237492	9/9/97	Toshiba Corp.		
	41	JP2000285674	10/13/00	Fujitsu Ltd.		
	42	JP2002184176	6/28/02	NEC Tohoku Ltd.		
	43	JP2003007963	1/10/03	Hitachi, Ltd.		
	44	JP2008046989	2/28/08	Fujitsu Ltd.		

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
	45	Anonymous. (December 1996). "Applications Note: Understanding DRAM Operation," IBM, 10 pages.	
	46	Behrens, S. "HP Printer Memory Explained", The ZonkPage, Last Updated 01-21-2004. Accessed 02-10-2013, Retrieved from the Internet: URL <http://warshaft.com/hpmem.htm>. 7pp.	
	47	Non-Final Office Action, U.S. Pat. App. 13/412,243, January 2, 2014, 20 pages	
	48	Non-Final Office Action, U.S. Pat. App. 12/761,179, September 13, 2012, 20 pages	
	49	Non-final office action, U.S. Patent Application No. 13/288,850, October 14, 2013, 24 pages	
	50	Non-final office action, U.S. Patent Application No. 13/411,344, December 31, 2013, 28 pages	
	51	Non-final office action, U.S. Patent Application No. 13/473,413, November 17, 2011, 46 pages	
	52	Response to non-final office action dated September 13, 2012 for U.S. Patent Application No. 12/761,179, filed March 13, 2013, 16 pages	

EXAMINER **DATE CONSIDERED**

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Substitute for form 1449/PTO				Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(Use as many sheets as necessary)*				Application Number	13/971,231
				Filing Date	August 20, 2013
				First Named Inventor	Jayesh R. Bhakta
				Art Unit	2189
				Examiner Name	Unknown
Sheet	3	of	3	Attorney Docket Number	NETL.018P2C7

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
	53	Response to non-final office action dated October 14, 2013 for U.S. Patent Application No. 13/288,850, filed January 14, 2014, 15 pages	
	54	Response to non-final office action dated 12/31/2013 for U.S. Patent Application No. 13/411,344, filed March 31, 2014, 12 pages	
	55	Patent Owner's Response to Office Action mailed November 13, 2012 for Reexamination Control Nos.95/000,578; 95/000,579, and 95/001,339, filed January 14, 2013, 96 pages.	
	56	Patent Owner's Response to Office Action mailed December 19, 2012 for Reexamination Control No. 95/001,758, filed March 19, 2013, 61 pages	
	57	Patent Owner's Response to Office Action mailed September 26, 2013 for Reexamination Control No. 95/001,758, filed November 26, 2013, 85 pages	
	58	Third Party Requester's Comments after Non-Final Action mailed September 26, 2013 for Reexamination Control No. 95/001,758, filed December 26, 2013,	
	59	Reexamination Control No. 95/002,399, filed April 25, 2013, and its entire file history	
	60	Patent Owner's Appeal Brief for Reexamination Control Nos. 95/000,546 and 95/000,577, filed October 2, 2013, 46 pages	
	61	Patent Trial and Appeal Board Decision on Appeal for Reexamination Control No.95/001/337, mailed January 16, 2014, 30 pages	
	62	Patent Trial and Appeal Board Decision on Appeal for Reexamination Control No.95/001/381, mailed January 16, 2014, 24 pages	
	63	Action Closing Prosecution mailed March 27, 2014 for Reexamination Control No. 95/001,758, filed September 14, 2011, 40 pages	
	64	Action Closing Prosecution mailed March 27, 2014 for Reexamination Control No. 95/001,339, filed June 8, 2010, 106 pages	
	65	Notice of Allowance, U.S. Pat. App. 12/761,179, July 11, 2013, 37 pages	
	66	Notice of Allowance, U.S. Pat. App. 12/504,131, February 12, 2013, 52 pages	

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 1 of 1

Complete if Known	
Application Number	13/971,231
Filing Date	August 20, 2013
First Named Inventor	Jayesh R. Bhakta
Art Unit	2189
Examiner Name	Unknown
Attorney Docket Number	NETL.018P2C7

US PATENT DOCUMENTS

Examiner Initials *	Cite No. [1]	Document Number / Number-Kind Code [2] (if known)	Publication Date (MM-DD-YYYY)	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	1	20080025137	01-31-2008	Natarajan et al.	
	2	2006233012	10-19-2006	Tomonori et al.	

FOREIGN PATENT DOCUMENTS

Examiner Initials *	Cite No. [1]	Foreign Patent Document	Publication Date (MM-DD-YYYY)	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]
	3	EP 1 816 570 A2	08-08-2007	Rambus, Inc.		

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
	4	International Search Report and Written Opinion, PCT/US2011/059209, January 31, 2013	

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Electronic Acknowledgement Receipt

EFS ID:	18697660
Application Number:	13971231
International Application Number:	
Confirmation Number:	2072
Title of Invention:	LOAD-REDUCING CIRCUIT FOR MEMORY MODULE
First Named Inventor/Applicant Name:	Jefferey C. Solomon
Customer Number:	79141
Filer:	Jamie Jie Zheng
Filer Authorized By:	
Attorney Docket Number:	NETL.018P2C7
Receipt Date:	07-APR-2014
Filing Date:	20-AUG-2013
Time Stamp:	19:52:13
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Transmittal Letter	2014-04-07_IDS_Cover_NETL018P2C7.pdf	55713 fb51323fedbfda34cc6d07c2f3e070b8c4d0f950	no	2
Warnings:					
Information:					

2	Information Disclosure Statement (IDS) Form (SB08)	2014-04-07_IDS1_NETL018P2C7.pdf	153758 144ceca778da744e69c982014275ca8f12ba3314	no	3
Warnings:					
Information:					
This is not an USPTO supplied IDS fillable form					
3	Information Disclosure Statement (IDS) Form (SB08)	2014-04-07_IDS2_NETL018P2C7.pdf	97875 77219edb3677df5ded3135bd081bb7fc49125710	no	1
Warnings:					
Information:					
This is not an USPTO supplied IDS fillable form					
4	Information Disclosure Statement (IDS) Form (SB08)	2014-04-07_IDS3_NETL018P2C7.pdf	93080 eb90c6d7ebd20b85fa88cf9b2a38d5840fb5b5ce	no	1
Warnings:					
Information:					
This is not an USPTO supplied IDS fillable form					
		Total Files Size (in bytes):	400426		

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New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

INFORMATION DISCLOSURE STATEMENT

Applicant	:	BHAKTA et al.
App. No.	:	13/971,231
Filed	:	August 20, 2013
For	:	LOAD-REDUCING CIRCUIT FOR MEMORY MODULE
Examiner	:	BANSAL, GURTEJ
Art Unit	:	2189
Conf No.	:	2072

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Enclosed for filing in the above-identified application are three Forms PTO/SB/08a/b Equivalent listing 77 references. Copies of foreign documents and/or their translation and non-patent literature have been submitted together with corresponding Information Disclosure Statements in the commonly-owned co-pending U.S. Pat. App. No. 13/287,042, which are available on PAIR.

The applicants would appreciate the Examiner initialing and returning the Form PTO/SB/08a/b Equivalent indicating that the information has been considered and made of record herein.

The information contained in this Information Disclosure Statement is not to be construed as a representation that: (i) a complete search has been made; (ii) additional information material to this application does not exist; (iii) the information, protocols, results and the like reported by third parties are accurate or enabling; or (iv) the above information constitutes prior art to the subject invention.

This Information Disclosure Statement is believed to be submitted before the mailing of the first Office Action. The Commissioner is authorized to charge the fee set forth in 37 C.F.R. § 1.17(p) to Deposit Account No. 50-5963.

Respectfully submitted,

Dated: April 7, 2014

/Jamie J. Zheng/ 51167

Jamie J. Zheng (Reg. No.)
Customer No. 79141
(650) 273-6008

Samsung Electronics Co., Ltd.
Ex. 1052, p. 131

PTO/SB/08a/b(07-09)
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Substitute for form 1449/PTO				Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(Use as many sheets as necessary)*				Application Number	13/971,231
				Filing Date	August 20, 2013
				First Named Inventor	Jayesh R. Bhakta
				Art Unit	2189
				Examiner Name	Unknown
Sheet	1	of	1	Attorney Docket Number	NETL.018P2C7

US PATENT DOCUMENTS

Examiner Initials *	Cite No. [1]	Document Number / Number-Kind Code [2] (if known)	Publication Date (MM-DD-YYYY)	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	1	6717855	04-06-2004	Underwood	

FOREIGN PATENT DOCUMENTS

Examiner Initials *	Cite No. [1]	Foreign Patent Document	Publication Date (MM-DD-YYYY)	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
	2	Action Closing Prosecution mailed October 1, 2012, for Control Nos. 95/000,546 and 95/000,577, filed May 11, '2010 and October 20, 2010 respectively, 39 pages.	
	3	Non-Final Office Action mailed November 13, 2012, for Control Nos. 95/001,339, 95/000,578 and 95/000,579, filed April 20, 2010, October 20, 2010 and October 21, 2010 respectively, 81 pages	
	4	Order Granting Request for Inter Partes Reexamination and Non-Final Office Action mailed December 7,2012, for Control No. 95/002,399, filed September 15, 2012, 89 pages.	
	5	Non-Final Office Action mailed December 19, 2012, for Control No. 95/001,758, filed September 14, 2011, 36 Pages.	
	6	Request for Inter Partes Reexamination; Reexam U.S. Patent Application No. 95/001,758, for U.S. Patent No. 7,864,627, filed September 15, 2011, 814 pages (submitted in four parts.)	
	7	Request for Inter Partes Reexamination; Reexam U.S. Patent Application No. 95/001,381, for U.S. Patent No. 7,532,537, filed June 9, 2010, 247 pages	

EXAMINER **DATE CONSIDERED**

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PTO/SB/08a/b(07-09)
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US Patent & Trademark Office; U.S. DEPARTMENT OF COMMERCE
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 1 of 1

Complete if Known	
Application Number	13/971,231
Filing Date	August 20, 2013
First Named Inventor	Jayesh R. Bhakta
Art Unit	2189
Examiner Name	Unknown
Attorney Docket Number	NETL.018P2C7

US PATENT DOCUMENTS

Examiner Initials *	Cite No. [1]	Document Number / Number-Kind Code [2] (if known)	Publication Date (MM-YYYY)	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	1	2003/0070052	04-2003	Lai, Jiin	
	2	2004/0098528	05-2004	Janzen, Jefferey W.	
	3	2002/0048195	04-2002	Klein, Dean A.	

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
	4	Non-Final Office Action, dated January 2, 2014, for U.S. Pat. App. No. 13/287,042 filed November 1, 2011, 42 pages	
	5	Response to Non-Final Office Action dated January 2, 2014 for U.S. Pat. App. No. 13/287,042, filed April 2, 2014, 12 pages	

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Electronic Acknowledgement Receipt

EFS ID:	18704500
Application Number:	13971231
International Application Number:	
Confirmation Number:	2072
Title of Invention:	LOAD-REDUCING CIRCUIT FOR MEMORY MODULE
First Named Inventor/Applicant Name:	Jefferey C. Solomon
Customer Number:	79141
Filer:	Jamie Jie Zheng
Filer Authorized By:	
Attorney Docket Number:	NETL.018P2C7
Receipt Date:	08-APR-2014
Filing Date:	20-AUG-2013
Time Stamp:	14:53:47
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Transmittal Letter	2014-04-08_IDS_Cover_NETL018P2C7.pdf	54999 6f5529ec3a84ddd9a34c4a9a6975d730708a1dba	no	2
Warnings:					
Information:					

2	Information Disclosure Statement (IDS) Form (SB08)	2014-04-08_IDS_NETL018P2C7.pdf	92232 af2ed60caa03fa353024f616c0e181c05eb912d5	no	1
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Information:					
This is not an USPTO supplied IDS fillable form					
3	Non Patent Literature	2014-01-02_NFOA_NETL018P1C6.pdf	2348292 127ee6aa81f352113c242f877f736f1ff7ac948b	no	42
Warnings:					
Information:					
4	Non Patent Literature	2014-04-02_Rsps_NFOA_NETL018P1C6.pdf	146023 fc425b898e830757f902cd1d25ae548fddbbda50	no	12
Warnings:					
Information:					
		Total Files Size (in bytes):	2641546		

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<u>New Applications Under 35 U.S.C. 111</u>
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

<u>National Stage of an International Application under 35 U.S.C. 371</u>
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<u>New International Application Filed with the USPTO as a Receiving Office</u>
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Applicant	:	BHAKTA et al.
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Filed	:	August 20, 2013
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Examiner	:	BANSAL, GURTEJ
Art Unit	:	2189
Conf No.	:	2072

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Enclosed for filing in the above-identified application is a Form PTO/SB/08a/b Equivalent listing 5 references. Copies of foreign documents and/or their translation and non-patent literature are submitted herewith.

The applicants would appreciate the Examiner initialing and returning the Form PTO/SB/08a/b Equivalent indicating that the information has been considered and made of record herein.

The information contained in this Information Disclosure Statement is not to be construed as a representation that: (i) a complete search has been made; (ii) additional information material to this application does not exist; (iii) the information, protocols, results and the like reported by third parties are accurate or enabling; or (iv) the above information constitutes prior art to the subject invention.

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Respectfully submitted,

Dated: April 8, 2014

/Jamie J. Zheng/ 51167

Jamie J. Zheng (Reg. No.)
Customer No. 79141
(650) 273-6008

Samsung Electronics Co., Ltd.
Ex. 1052, p. 137

PTO/SB/08a/b(07-09)
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Sheet 1 of 1

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First Named Inventor	Jayesh R. Bhakta
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Examiner Name	Unknown
Attorney Docket Number	NETL.018P2C7

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	1.	20060262586	11-23-2006	Solomon, et al	
	2.	20080162790	07-03-2008	Im, Jeon-Taek	
	3.	20090103387	04-23-2009	Shau, Jeng-Jye	

FOREIGN PATENT DOCUMENTS

Examiner Initials *	Cite No. [1]	Foreign Patent Document	Publication Date (MM-DD-YYYY)	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]
	4.	JPH10092169 A	9/9/97	Toshiba Corp.		
	5.	JP2000311485 A	10/13/00	Fujitsu Ltd.		

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	6.	Office Action mailed April 2, 2014, for Japanese Patent Application No. 2012-520662 and English translation thereof, 7 pages	

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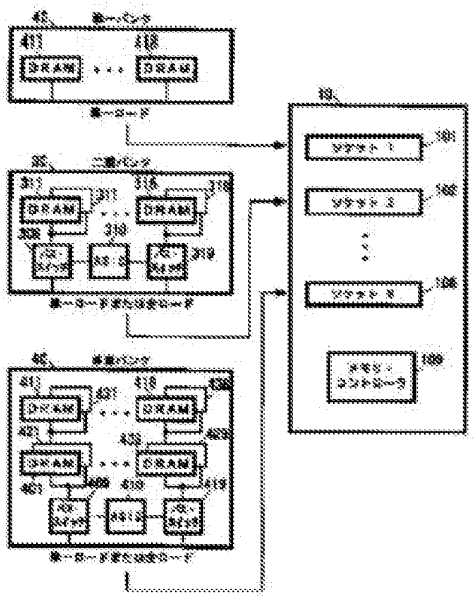
(21)Application number : **09-181302**
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(30)Priority
Priority number : **96 676609** Priority date : **08.07.1996** Priority country : **US**

(54) MEMORY MODULE

(57)Abstract:
PROBLEM TO BE SOLVED: To minimize a data line load by providing a bus switch between a system and a RAM and then comprising a logic circuit to produce a signal for enabling this switch into an ASIC.
SOLUTION: DRAM chips 301 to 304 and DRAM chips 311 to 314 are connected to a bus switch 309, while DRAM chips 305 to 308 and DRAM chips 315 to 318 are connected to a bus switch 319. A couple of bus switches are connected to ASIC 310 which is connected to a RAS pin and a CAS pin. A data bus load can be minimized by forming a bank DIMM 30 or DIMM 40 by utilizing bus switches 309, 319 or bus switches 409, 419.



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審査請求　未請求　請求項の数４　ＯＬ　（全 ７ 頁）

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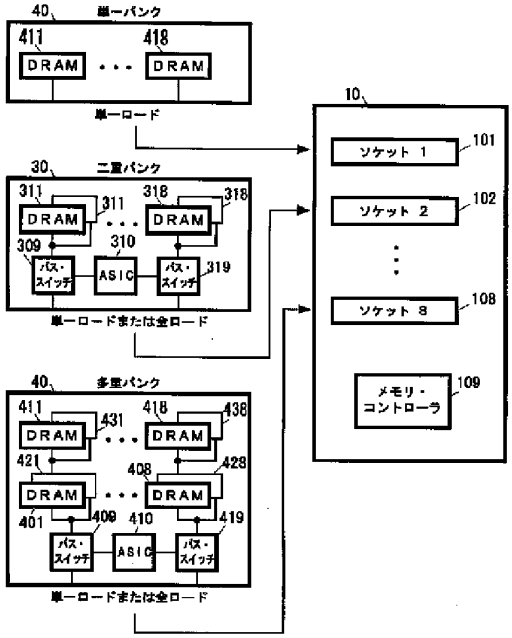
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最終頁に続く

(54)【発明の名称】　メモリ・モジュール

(57)【要約】
【課題】　複数のＤＲＡＭを有する高密度モジュール上のデータ線負荷を最小にし、データ線容量性負荷に起因する性能低下なしに、システムの最大のメモリ密度を可能にすること。
【解決手段】　システム・ボード１０上のコネクタ１０１～１０８と相互接続されるタブを有するプリント回路カード２０～４０と、プリント回路カードに取り付けられた複数のバンクのランダム・アクセス・メモリ・デバイス３０１～３１８、４０１～４３８と、選択されたランダム・アクセス・メモリ・デバイスと接続された、イネーブル信号に応答する１つまたは複数のバス・スイッチ３０９、３１９、４０９、４１９と、システムの行アドレス・ストローブ信号および列アドレス・ストローブ信号に応答して、１つまたは複数のバス・スイッチのイネーブル信号を生成する、論理手段とを含む。



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【特許請求の範囲】
【請求項１】システム・ボード上のコネクタと相互接続される接点タブを有し、カード・データ・バスを有するプリント回路カードと、
前記プリント回路カードに取り付けられ、前記カード・データ・バスに接続された、複数バンクのランダム・アクセス・メモリ・デバイスと、
前記複数バンクのランダム・アクセス・メモリ・デバイスのうちの選択されたものが前記カード・データ・バスを介して接続された、イネーブル信号に応答する、１つまたは複数のバス・スイッチと、
システムの行アドレス・ストローブ信号および列アドレス・ストローブ信号に応答して、前記１つまたは複数のスイッチの前記イネーブル信号を生成する、論理手段とを含む、メモリ・モジュール。
【請求項２】前記１つまたは複数のバス・スイッチおよび前記論理手段が、前記プリント回路カードに取り付けられることを特徴とする、請求項１に記載の高密度メモリ・モジュール。
【請求項３】第２のプリント回路カードを含み、前記第１および第２のプリント回路カードが異なる数のメモリ・バンクを有することを特徴とする、請求項１に記載の高密度メモリ・モジュール。
【請求項４】前記１つまたは複数のバス・スイッチのそれぞれが、前記カード・データ・バスの信号線１本につき１つの複数の電界効果トランジスタ（ＦＥＴ）と、前記イネーブル信号に応答して前記ＦＥＴをバイアスするための手段とを含むことを特徴とする、請求項１に記載の高密度メモリ・モジュール。
【発明の詳細な説明】
【０００１】
【発明の属する技術分野】本発明は、全般的にはコンピュータ用の高密度メモリ・モジュールに関し、具体的には、最小限のメモリ・バス負荷を有する多重バンク・メモリ・モジュールに関する。
【０００２】
【従来の技術】ＳＩＭＭ（シングル・インライン・メモリ・モジュール）やＤＩＭＭ（デュアル・インライン・メモリ・モジュール）などの高密度メモリ・モジュールは、多くの応用分野で追加のシステム性能を達成できるので、ハイ・エンド・パーソナル・コンピュータ（ＰＣ）、ネットワーク・サーバおよびワークステーションで需要がある。しかし、最大システム密度は、下記の１つまたは複数によって不自然に制限されることがしばしばである。
・システムが有するメモリ・モジュール「スロット」の数が限られている。
・システムが有するメモリ「バンク」の数が（メモリ・コントローラからの選択信号線の不足が原因で）限られている。
・高密度メモリ・チップ（たとえば６４メガビット（Ｍｂ）、２５６Ｍｂおよびそれ以上）は、非常に高価であるか、簡単に入手できないか、その両方である。
・高密度メモリ・チップは、システムのメモリ・インターフェース電圧より低い動作電圧を有する場合がある。
・標準ランダム・アクセス・メモリ・デバイス（ＲＡＭ）（ダイナミックＲＡＭ（ＤＲＡＭ）、シンクロナスＤＲＡＭ（ＳＤＲＡＭ）およびスタティックＲＡＭ（ＳＲＡＭ）を含む）の積層化／立体化または大型モジュールの使用は、システム限界をはるかに超えるデータ線容量をもたらす。以前の解決は、最後の問題以外の上記の問題のすべてについて提供されてきたが、これらの解決は、データ線負荷の問題が原因で応用性が制限されている。メモリ拡張を制限されているシステムで安価なＲＡＭチップをよりよく利用するために必要なものは、データ線の容量性負荷を最小にし、その結果、ＲＡＭチップのバンクを有する大型メモリ・モジュールをシステムに追加できるようにする方法である。
【０００３】
【発明が解決しようとする課題】したがって、本発明の目的は、データ線ごとに複数のランダム・アクセス・メモリ・デバイスを有する高密度モジュールでのデータ線負荷を最小にするための解決を提供することである。
【０００４】本発明のもう１つの目的は、データ線の容量性負荷に起因する性能低下なしに、密度を制限されているシステムのメモリ密度を最大にすることである。
【０００５】
【課題を解決するための手段】本発明によれば、データ線容量を許容可能なシステム限界まで減らす解決法には、２つの部分がある。第１の部分には、インライン・バス・スイッチを有するメモリ・モジュールの設計が含まれる。バス・スイッチは、モジュール・タブ（システム）とランダム・アクセス・メモリ・デバイス（ＲＡＭ）の間に置かれ、高インピーダンス（オフ）またはアクティブ（活動）状態のいずれかになる。高インピーダンス状態の時には、メモリ・モジュールの実効負荷は、ビット・スイッチ・デバイスの負荷になる。アクティブ（たとえば、リード／ライト・サイクル）の時には、ＲＡＭ負荷の他に、最小限のキャパシタンス／抵抗がメモリ・バスに追加される。一時に１つのメモリ・モジュールだけがアクティブになる。
【０００６】本発明による解決の第２の部分は、バス・スイッチをイネーブルする信号を生成する論理回路を特定用途向け集積回路（ＡＳＩＣ）に組み込むことである。バス・スイッチは、メモリ・モジュールへの行アドレス・ストローブ（ＲＡＳ）選択線の立ち下がりエッジでアクティブになり、ＲＡＳ選択線または列アドレス・ストローブ（ＣＡＳ）選択線のうちの最後の線がインアクティブ（非活動）状態になるまで活動状態にとどまり、これによって、高速ページ・モード（ＦＰＭ）動作

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とＥＤＯ（拡張データ出力）動作の両方がサポートされる。ＡＳＩＣの回路は、システムのＲＡＳ選択線とＣＡＳ選択線をデコードし、信号を駆動してバス・スイッチをイネーブルすることによって、この作業を実行する。論理回路は、リード／ライト・サイクル、ＲＯＲ（RAS only refresh）サイクル、ＣＢＲ（CAS before RAS refresh）サイクルおよびヒドン・リフレッシュ（hidden refresh）サイクルを区別し、それ相応にバス・スイッチをアクティブにしなければならない。ＣＢＲサイクルが発生する時には、バス・スイッチはインアクティブのままになる。ヒドン・リフレッシュ・サイクルでは、バス・スイッチはアクティブにされ、リフレッシュ・サイクルが完了するまでアクティブのままになる。これは、リード動作またはライト動作が存在する可能性があるので必要である。

【０００７】

【発明の実施の形態】本発明を、ＤＩＭＭを使用する特定の実施例に関して説明するが、当業者であれば、ＳＩＭＭなどの他のメモリ・モジュールを本発明の実施に使用できることを諒解するであろう。このようなモジュールは、通常は、コンピュータ・システム基板上のコネクタに挿入するための接点タブを有するプリント回路カードとして実施される。

【０００８】ここで図面、具体的には図１を参照すると、８つのメモリ・モジュール・ソケット１０１～１０８とメモリ・コントローラ１０９を有する通常のシステム・ボード１０が示されている。たとえば８つの４ＭｂのＤＲＡＭチップ２０１～２０８を有する通常の単一バンクＤＩＭＭ　２０は、通常はメモリ・コントローラ１０９に最も近いメモリ・モジュール・ソケット１０１から始めて、メモリ・モジュール・ソケット１０１～１０８のすべてに単一バンクＤＩＭＭ　２０が挿入されるまで順番に、メモリ・モジュール・ソケット１０１～１０８のうちの１つに挿入することができる。したがって、この例では、システム・ボードは、４メガバイト（ＭＢ）の最小構成と３２ＭＢの最大構成を有する。

【０００９】本発明によれば、二重バンクＤＩＭＭ　３０または多重バンクＤＩＭＭ　４０によって、単一バンクＤＩＭＭ　２０を置換することができる。二重バンクＤＩＭＭ　３０の場合、バス・スイッチ３０９および３１９に接続された、８つのＤＲＡＭチップ３０１～３０８の第１のグループと、８つのＤＲＡＭチップ３１１～３１８の第２のグループがある。ＤＲＡＭチップ３０１～３０４およびＤＲＡＭチップ３１１～３１４はバス・スイッチ３０９に接続され、ＤＲＡＭチップ３０５～３０８およびＤＲＡＭチップ３１５～３１８はバス・スイッチ３１９に接続される。２つのバス・スイッチは、ＡＳＩＣ　３１０に接続され、ＡＳＩＣ３１０は、このモジュールのＲＡＳピンおよびＣＡＳピンに接続される。この概念は、多重バンクＤＩＭＭ　４０の場合に拡張され、この例では、ＤＲＡＭチップの４つのグループすなわち、ＤＲＡＭチップ４０１～４０８、ＤＲＡＭチップ４１１～４１８、ＤＲＡＭチップ４２１～４２８およびＤＲＡＭチップ４３１～４３８がある。ＤＲＡＭチップ４０１～４０４、ＤＲＡＭチップ４１１～４１４、ＤＲＡＭチップ４２１～４２４およびＤＲＡＭチップ４３１～４３４は、バス・スイッチ４０９に接続され、ＤＲＡＭチップ４０５～４０８、ＤＲＡＭチップ４１５～４１８、ＤＲＡＭチップ４２５～４２８およびＤＲＡＭチップ４３５～４３８は、バス・スイッチ４１９に接続される。二重バンクＤＩＭＭ　３０の場合と同様に、バス・スイッチ４０９および４１９は、ＡＳＩＣ　４１０に接続され、ＡＳＩＣ　４１０は、このモジュールのＲＡＳピンおよびＣＡＳピンに接続される。

【００１０】二重バンクＤＩＭＭ　３０を使用する場合、システムの最小構成は８ＭＢに増加し、最大構成は６４ＭＢに増加する。多重バンクＤＩＭＭ　４０を使用すると、図示の４バンクのＤＲＡＭチップの例では、最小構成は１６ＭＢ、最大構成は１２８ＭＢに増加する。より高密度のデバイス（たとえば１６Ｍｂ、６４Ｍｂなど）を使用すると、最大メモリ密度のかなりの増加がもたらされるはずである。これは、下の表からわかるように、最小限のデータ・バス負荷で達成される。

【００１１】

【表１】

データ・バス負荷の比較＊（最大値）			
	１バンク	２バンク	４バンク
従来技術	８	１６	３２
本発明	８	９	１１

＊ＤＩＭＭ当たりのＤＲＡＭ等価負荷の数として表す（通常は７ｐＦ／ＤＲＡＭ）

【００１２】これは、二重バンクＤＩＭＭ　３０の場合にはバス・スイッチ３０９および３１９、多重バンクＤＩＭＭ　４０の場合にはバス・スイッチ４０９および４１９を使用することによって達成される。ＡＳＩＣ　３

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１０および４１０は、バス・スイッチとシステム・ボードの間のインターフェースを提供する。

【００１３】ここで図２に移ると、バス・スイッチの一般化された論理図が示されている。バス・スイッチには、信号線ごとに１つずつ、複数のＦＥＴが含まれる。１つまたは複数のインバータ５０が、ＦＥＴをオンにバイアスするのに使用される。インバータ５０への入力ＢＥＮ（ＮはＢＥの反転を表す）は、バス・スイッチのイネーブル入力である。イネーブル入力がロウになると、インバータの出力はハイになり、その結果、正バイアスがＦＥＴのゲートに印加され、ＦＥＴが導通する。このバス・スイッチを介する遅延は、１ナノ秒（ｎｓ）未満であり、これによって、正しいメモリ動作が保証される。

【００１４】図３のブロック図からわかるように、ＡＳＩＣ　６０（図１のＡＳＩＣ　３１０および４１０に対応する）は、システムのＲＡＳ信号（ＳＹＳ＿ＲＡＳ）とＣＡＳ信号（ＳＹＳ＿ＣＡＳ）を受け取り、バス・スイッチ６１および６２のイネーブル入力へのＲＣ＿ＳＥＬＥＣＴ信号を生成する。バス・スイッチ６１および６２は、カード・データ・バス６３とプリント回路カードの接点タブ６４の間のインターフェースを提供する。接点タブ６４はシステム・ボードのソケット１～８に挿入されるモジュール２０、３０、４０のプリント回路カードのエッジに設けられている。

【００１５】ＲＣ＿ＳＥＬＥＣＴ信号は、アクティブ・ロウの信号であり、独自の機能を有する。通常のメモリ・リード・サイクルおよびメモリ・ライト・サイクルの間、ＲＣ＿ＳＥＬＥＣＴ信号は、図４に示されるように、システムのＲＡＳ選択線のアクティブ（立ち下がり）エッジでアクティブにされ、システムのＲＡＳ選択線とＣＡＳ選択線の両方がインアクティブになるまでアクティブのままになる。

【００１６】ヒドン・リフレッシュ・サイクル中は、図５からわかるように、ヒドン・リフレッシュ・サイクルの性質が原因で、ＲＣ＿ＳＥＬＥＣＴ信号はアクティブになる。ヒドン・リフレッシュ・サイクルの第１の部分は、ＲＡＳが立ち上がってから立ち下がる（ＣＢＲリフレッシュ・サイクルの開始）までシステムのＣＡＳ選択線がアクティブのままになるメモリ・サイクルである。ＲＣ＿ＳＥＬＥＣＴ論理回路は、ＣＡＳ外乱をフィルタリングし、インアクティブのままになる。

【００１７】ＣＢＲリフレッシュ中は、図６からわかるように、システムのＣＡＳ選択線が、システムのＲＡＳ選択線がアクティブになるより前にアクティブになる。ＲＣ＿ＳＥＬＥＣＴ信号は、ＣＢＲサイクル中はインアクティブのままになる。

【００１８】ＲＯＲサイクル中は、図７からわかるように、システムのＲＡＳ選択線がアクティブになり、ＲＣ＿ＳＥＬＥＣＴ信号上に駆動される。バス・スイッチがアクティブになっても、データがその時点で駆動されていないので、システム動作には影響しない。

【００１９】所与の応用分野で必要であれば、追加回路を追加して、ＲＯＲサイクル中にバス・スイッチがアクティブにならないようにすることができる。

【００２０】図８のＡＳＩＣの内部ロジックには、システムのＣＡＳ選択線ＣＡＳ＿Ｎ（Ｎは反転を表わす）のアクティブ（すなわち立ち下がり）エッジでシステムＲＡＳ選択線（ＡＮＹ＿ＲＡＳ）の状態をラッチするＤ型のフリップフロップ７０が含まれる。ＡＮＹ＿ＲＡＳ信号は、ＡＮＤゲート７１によって生成され、バッファ７２を介してフリップフロップ７０のＤ入力に供給されるが、ＡＮＹ＿ＣＡＳ信号は、ＡＮＤゲート７３によって生成され、インバータ７４を介してフリップフロップ７０のクロック入力に供給される。フリップフロップ７０の出力は、インバータ７６を介して２入力ＮＡＮＤゲート７５に接続され、マルチプレクサ７７の入力「０」にも接続される。インバータ７６の出力は、信号ＣＢＲ＿ＢＩＴ＿Ｎである。信号ＡＮＹ＿ＲＡＳは、インバータ７８によって反転され、インバータ７８の出力は、２入力ＮＡＮＤゲート７５のもう一方の入力に接続される。２入力ＮＡＮＤゲート７５の出力は、信号ＲＣ＿ＡＣＴＩＶＥであり、マルチプレクサ７７の入力「１」に接続される。フリップフロップ７０は、システムのＲＡＳ選択線とＣＡＳ選択線がインアクティブであり、フリップフロップ７０の「Ｑ」出力が論理「１」である時に、ＮＡＮＤゲート７９の出力によってリセットされる。マルチプレクサ７７の選択線は、４つのゲート（インバータ８０と３つのバッファ８１～８３）によって遅延されたシステムのＣＡＳ選択線ＤＥＬＹ＿ＣＡＳによって選択される。これは、フリップフロップ７０が信号ＡＮＹ＿ＲＡＳの状態をラッチする時間を与えるために行われる。

【００２１】各サイクルの初期の開始時に、マルチプレクサ７７は、「１」入力位置にセットされる。これによって、システムのＲＡＳ選択線をすばやく流すことができるようになる。システムのＣＡＳ選択線がアクティブになった時には、マルチプレクサ７７は、「０」入力位置に切り替わり、これによって、フリップフロップ７０の出力が選択される。

【００２２】図１に戻って、本発明の実装は、ＤＲＡＭチップのバンク群を１つのプリント回路カードに取り付け、ＡＳＩＣとバス・スイッチを別のキャリアに取り付けることによって、変更することができる。たとえば、ＡＳＩＣとバス・スイッチは、システム・ボード１０に直接に取り付けることができるが、これにはシステム・ボードの変更が必要である。代替案は、ＤＲＡＭカードを受けるコネクタを備えた別のプリント回路カードにＡＳＩＣとバス・スイッチを取り付けることである。どちらの代替案でも、ＤＲＡＭチップだけでＤＲＡＭカード

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を製造することができる。

【図面の簡単な説明】

【図１】システム・メモリ・ボードと、従来の単一バンクＤＩＭＭと本発明による多重バンクＤＩＭＭの両方を示すブロック図である。

【図２】図１に示された本発明の実施例に使用されるバス・スイッチを一般化した論理ブロック図である。

【図３】図１の実施例でのＡＳＣＩとバス・スイッチの関係を示すブロック図である。

【図４】通常のリード／ライト・サイクルの場合の、ＲＣ＿ＳＥＬＥＣＴ出力信号を生成するＡＳＩＣ論理回路の動作を示すタイミング図である。

【図５】ヒドン・リフレッシュの場合の、ＲＣ＿ＳＥＬＥＣＴ出力信号を生成するＡＳＩＣ論理回路の動作を示すタイミング図である。

【図６】ＣＢＲの場合の、ＲＣ＿ＳＥＬＥＣＴ出力信号を生成するＡＳＩＣ論理回路の動作を示すタイミング図である。

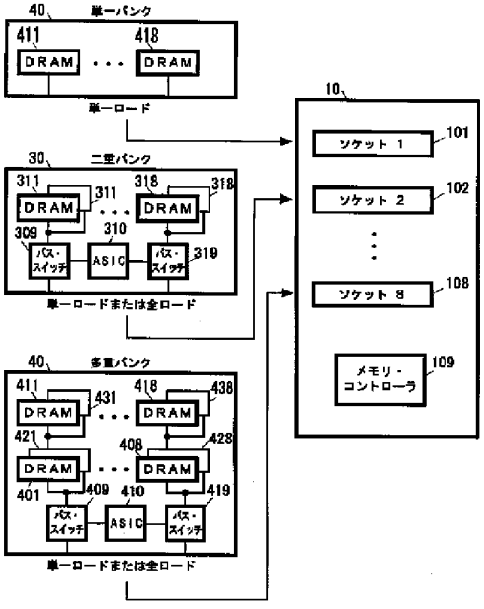
【図７】ＲＯＲの場合の、ＲＣ＿ＳＥＬＥＣＴ出力信号を生成するＡＳＩＣ論理回路の動作を示すタイミング図である。

【図８】本発明の好ましい実施例によるＡＳＣＩの論理回路を示す論理ブロック図である。

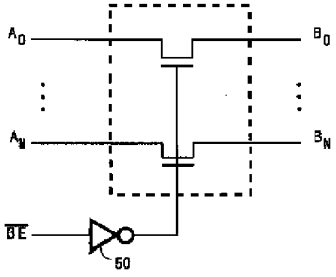
【符号の説明】

６０　ＡＳＩＣ
６１　バス・スイッチ
６２　バス・スイッチ
６３　カード・データ・バス
６４　タブ
７２　バッファ
７３　ＡＮＤゲート
７４　インバータ
７５　２入力ＮＡＮＤゲート
７６　インバータ
７７　マルチプレクサ
７８　インバータ
７９　ＮＡＮＤゲート
８０　インバータ
８１　バッファ
８２　バッファ
８３　バッファ

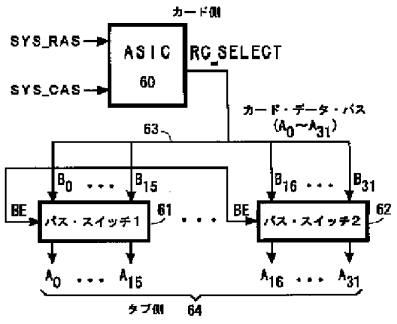
【図１】



【図２】

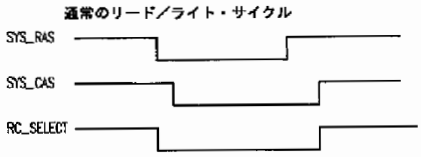


【図３】

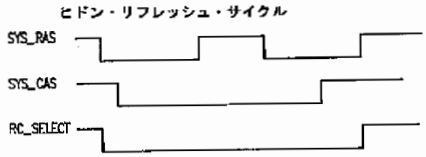


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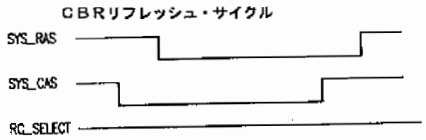
【図４】



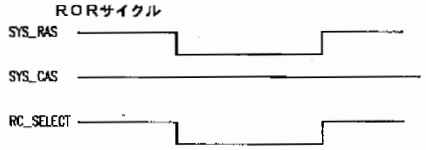
【図５】



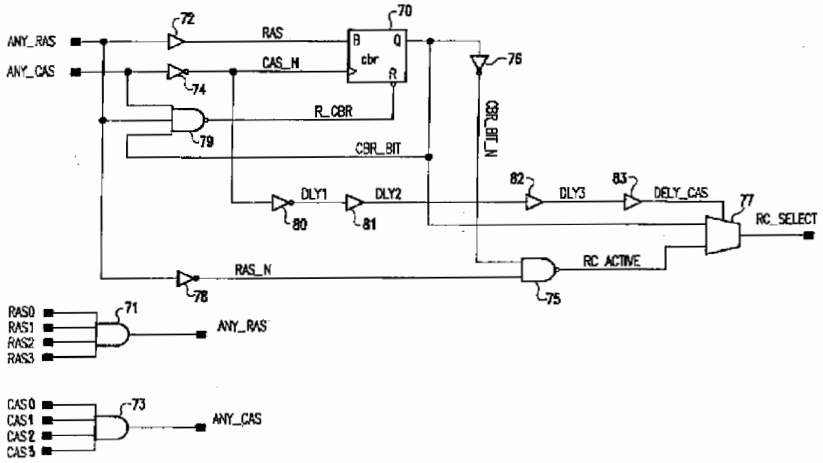
【図６】



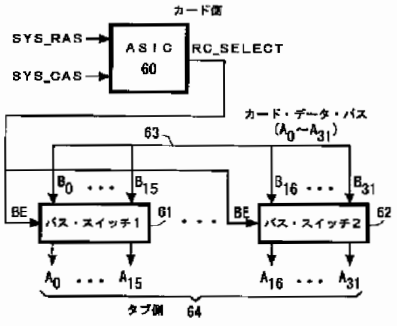
【図７】



【図８】



【手続補正書】
【提出日】平成９年７月２３日
【手続補正１】
【補正対象書類名】図面
【補正対象項目名】図３
【補正方法】変更
【補正内容】
【図３】



フロントページの続き

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Espacenet

Bibliographic data: JP2000311485 (A) — 2000-11-07

MEMORY MODULE SYSTEM CONNECTING ONLY SELECTED MEMORY MODULE TO DATA LINE AND DATA INPUT/OUTPUT METHOD UTILIZING THE SYSTEM

No documents available for this priority number.

Inventor(s): KIN CHIKYOKU ± (KIN CHIKYOKU)

Applicant(s): SAMSUNG ELECTRONICS CO LTD ± (SAMSUNG ELECTRONICS CO LTD)

Classification: **- international:** ***G06F12/00; G06F12/06; G06F13/16; G11C11/401; G11C11/407; G11C5/00; G11C7/10;*** (IPC1-7): G06F13/16; G11C11/401; G11C11/407
- cooperative: **G11C5/04**; **G11C7/1006**

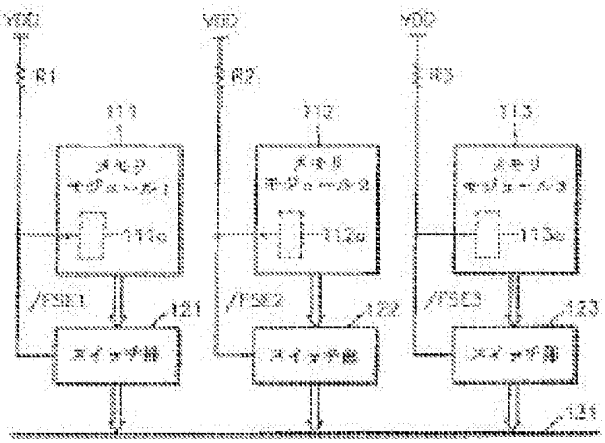
Application number: JP20000072737 20000315

Priority number(s): KR19990012027 19990407

Also published as: JP4319320 (B2) GB2348722 (A) GB2348722 (B) US6526473 (B1) TW475110 (B) KR20000065601 (A) FR2792105 (A1) FR2792105 (B1) DE19960005 (A1) less

Abstract of JP2000311485 (A)

PROBLEM TO BE SOLVED: To improve data write and read rates by generating a connection control signal by activation while data having burst length specified by a write mode is inputted. SOLUTION: As resistors R1-R3 arranged at the outside of memory modules 1-3, 111-113 are made high resistance value, voltage levels of first to third connection control signals /FSE1-/FSE3 are decided by an internal signal of the memory module 1-3, 111-113 connected to the resistors, but when an internal signal is in a floating state, voltage levels of the first to third connection control signal /FSE1-/FSE3 are made external power source voltage VDD through the resistors R1-R3, that is, made a high state.; Therefore, when the module 111 is selected, second, third connection control signals /FSE2, /FSE3 are made non-activated and second, third switches 122, 124 are turned off, loads of data pins of modules 2, 3, 112, 113 are separated from a data base line 131.


VDD
VDD
VDD
R1
R2
R3
111
112
113
111a
112a
113a
121
122
123
131

US006526473B1

(12) **United States Patent**
Kim

(10) **Patent No.: US 6,526,473 B1**
(45) **Date of Patent: Feb. 25, 2003**

(54) **MEMORY MODULE SYSTEM FOR CONTROLLING DATA INPUT AND OUTPUT BY CONNECTING SELECTED MEMORY MODULES TO A DATA LINE**

(75) Inventor: **Chi-wook Kim**, Suwon (KR)

(73) Assignee: **Samsung Electronics Co., Ltd.**, Suwon (KR)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/440,728**

(22) Filed: **Nov. 16, 1999**

(30) **Foreign Application Priority Data**

Apr. 7, 1999 (KR) 99-12027

(51) **Int. Cl.**[7] **G06F 12/02**

(52) **U.S. Cl.** **711/105**; 711/5; 711/111; 711/209; 365/230.03; 710/131

(58) **Field of Search** 711/5, 105, 111, 711/209; 365/230.03, 230.08; 710/131

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Assistant Examiner—Jasmine Song
(74) *Attorney, Agent, or Firm*—F. Chau & Associates, LLP

(57) **ABSTRACT**

A memory module system for connecting only selected memory modules to a data line to control data input and output is disclosed. The memory module system has a multiplicity of memory modules for outputting data to a data bus line, and more particularly, only the memory modules outputting data is electrically connected to the data bus line in response to activation of a predetermined connection control signal. The connection control signal has an activation width corresponding to a burst length of the output data. Only selected memory modules are connected to the data line during the data burst length, so that load per data pin is minimized, to thereby improve speed of writing and reading data.

27 Claims, 13 Drawing Sheets

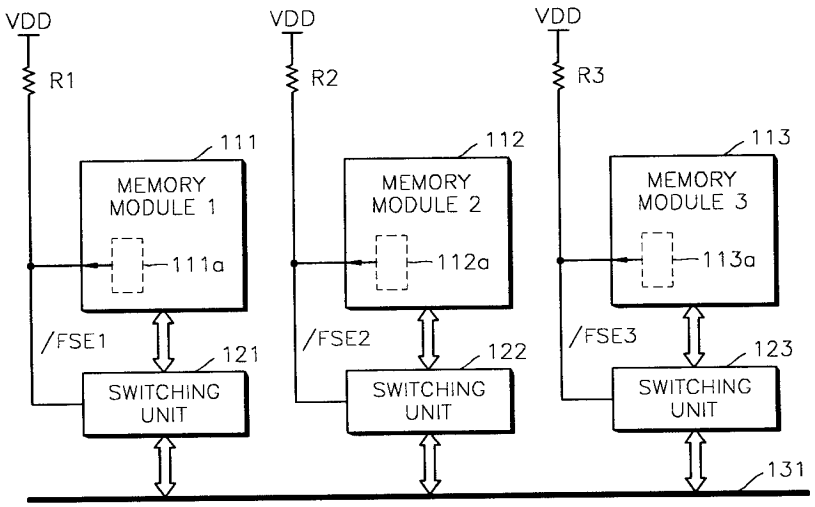


FIG. 1

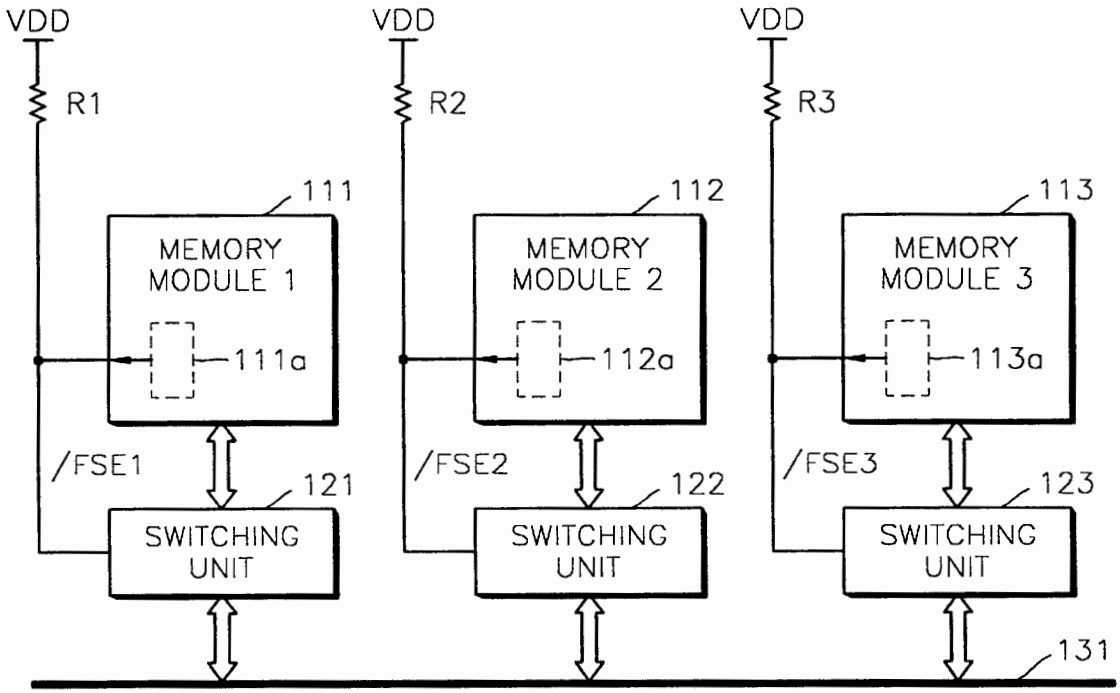

VDD
VDD
VDD
R1
R2
R3
111
112
113
MEMORY MODULE 1
MEMORY MODULE 2
MEMORY MODULE 3
111a
112a
113a
/FSE1
/FSE2
/FSE3
121
122
123
SWITCHING UNIT
SWITCHING UNIT
SWITCHING UNIT
131

FIG. 2

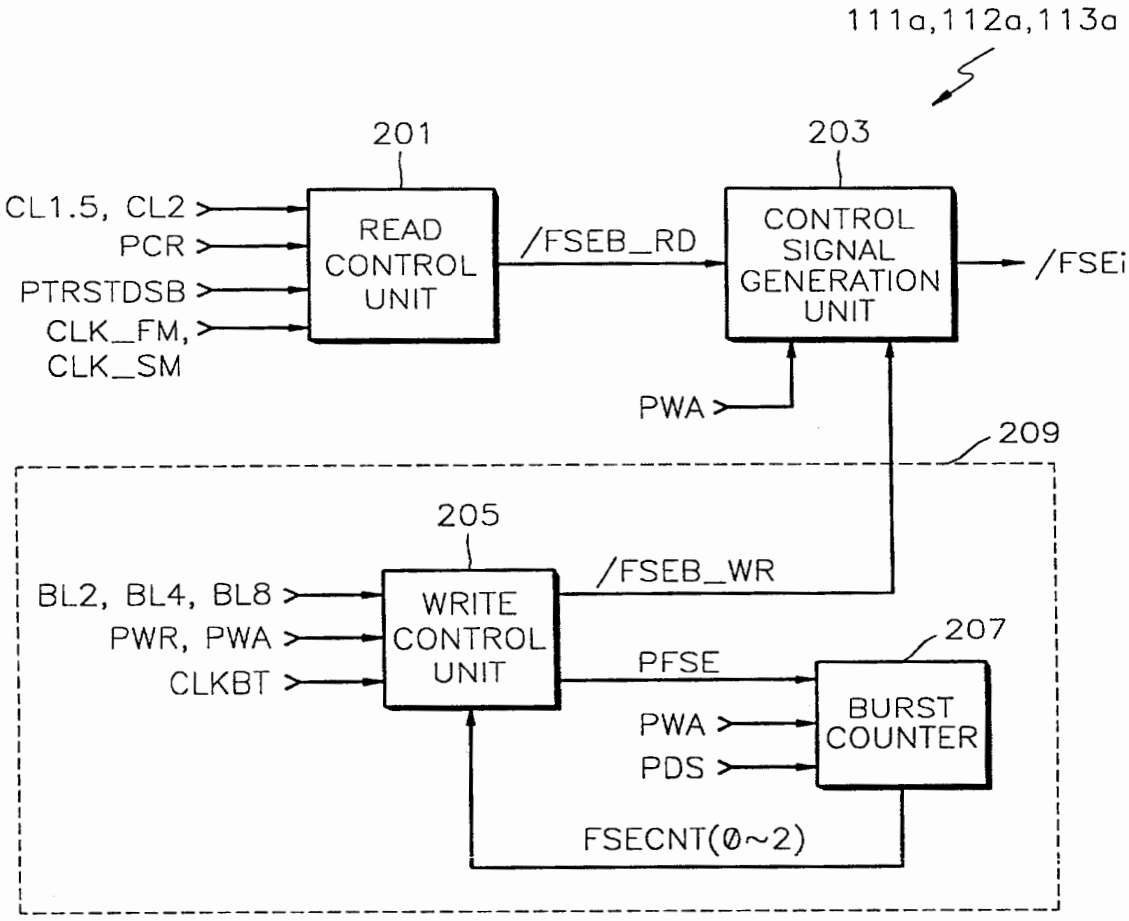

111a,112a,113a
201
203
CL1.5, CL2
PCR
PTRSTDSB
CLK_FM,
CLK_SM
READ CONTROL UNIT
/FSEB_RD
CONTROL SIGNAL GENERATION UNIT
/FSEi
PWA
209
205
BL2, BL4, BL8
PWR, PWA
CLKBT
WRITE CONTROL UNIT
/FSEB_WR
207
PFSE
PWA
PDS
BURST COUNTER
FSECNT(0~2)

FIG. 3

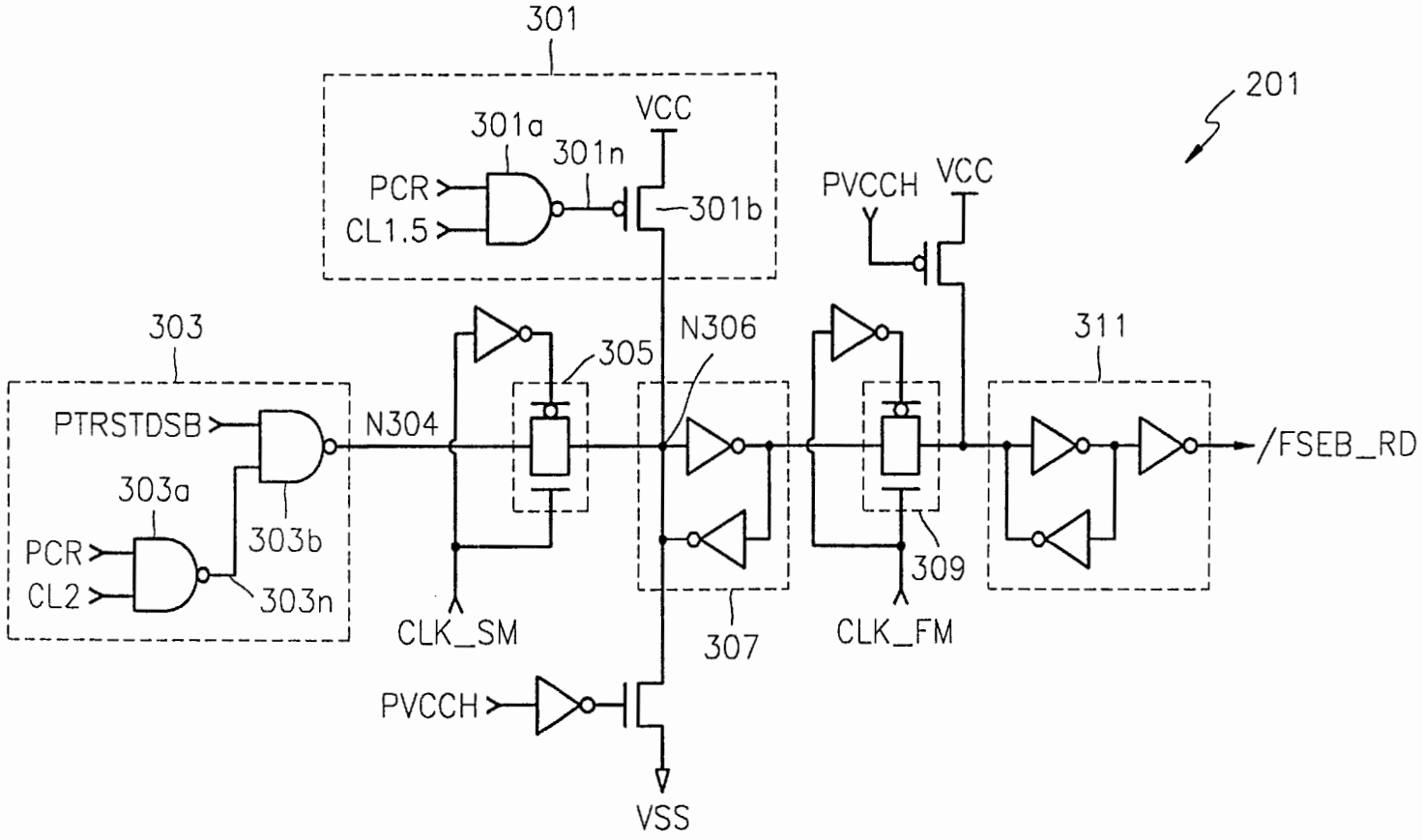

301
301a
301n
VCC
PCR
CL1.5
301b
201
PVCCH
VCC
303
305
N306
311
PTRSTDSB
N304
/FSEB_RD
303a
303b
PCR
CL2
303n
309
CLK_SM
307
CLK_FM
PVCCH
VSS

FIG. 4

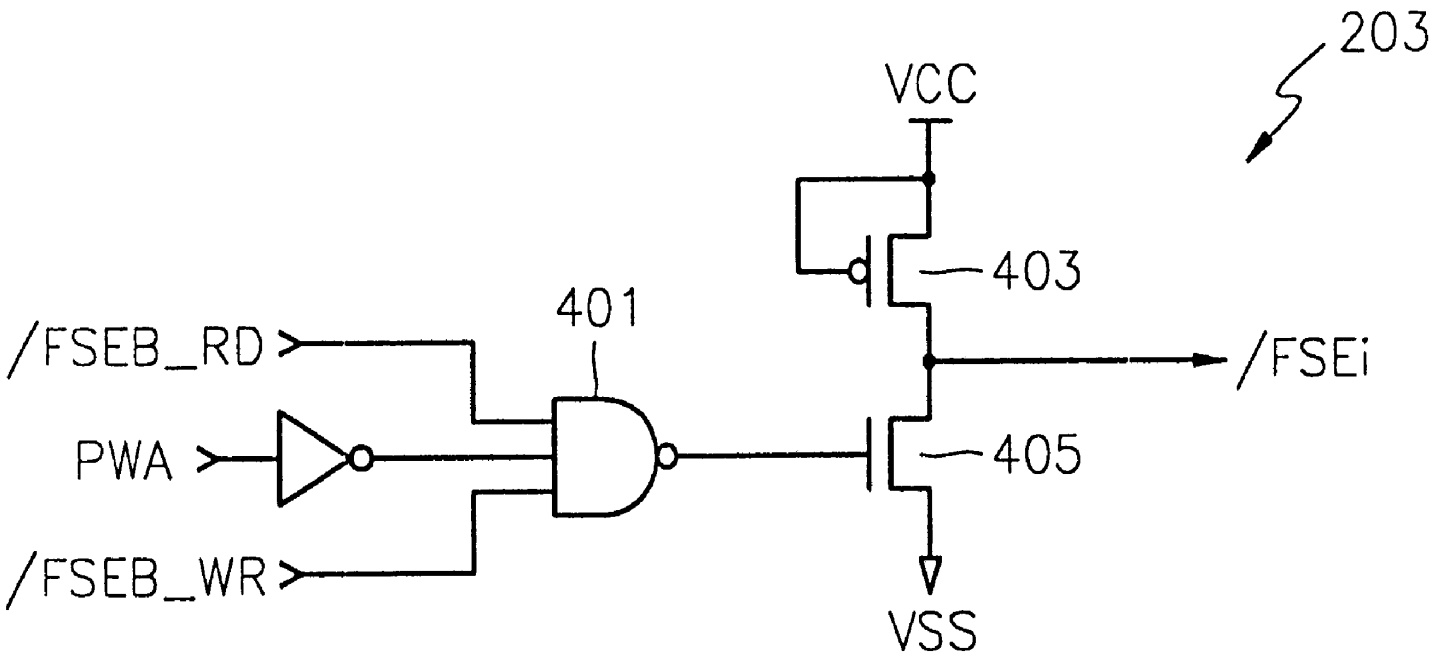
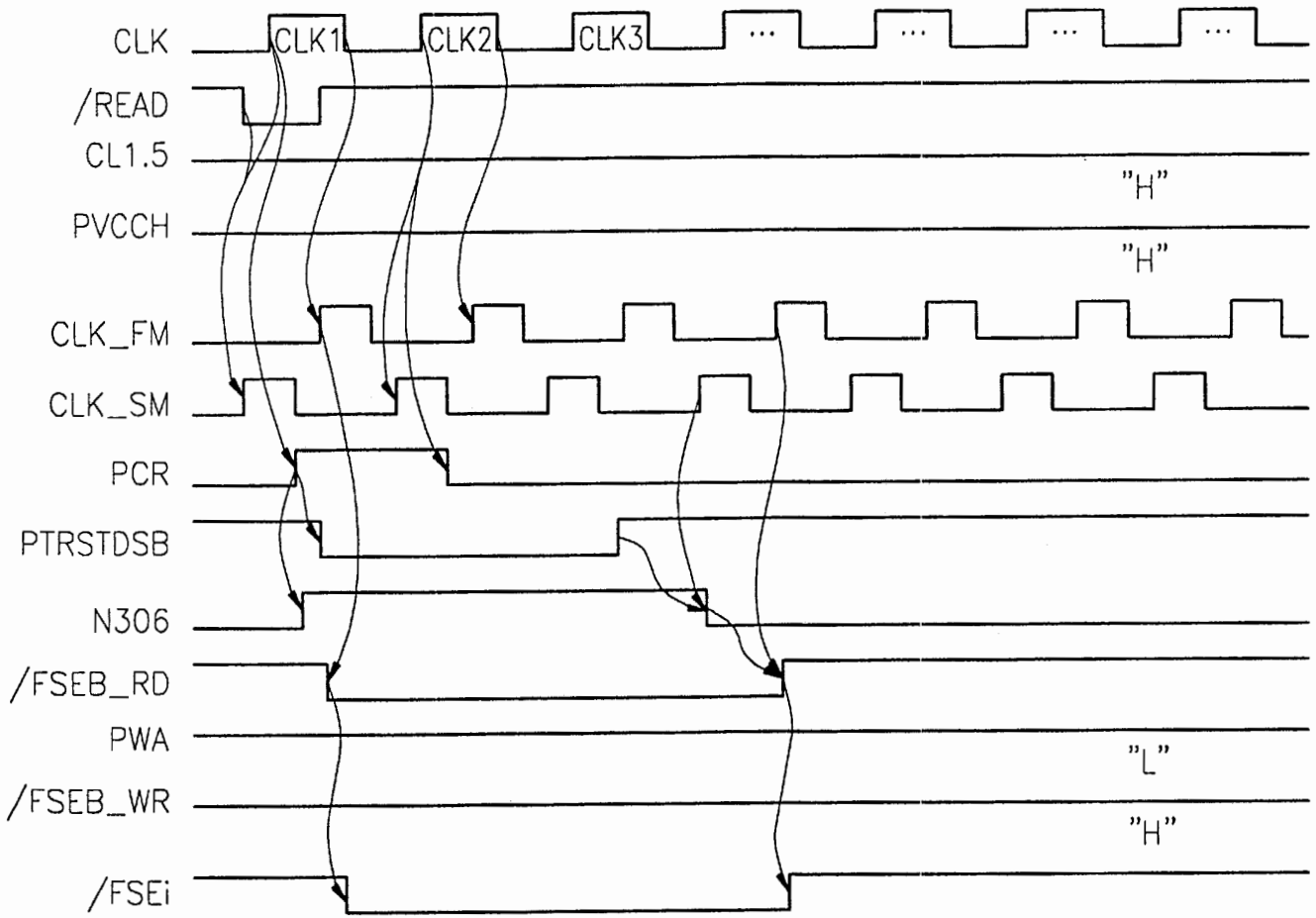


FIG. 5



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FIG. 6

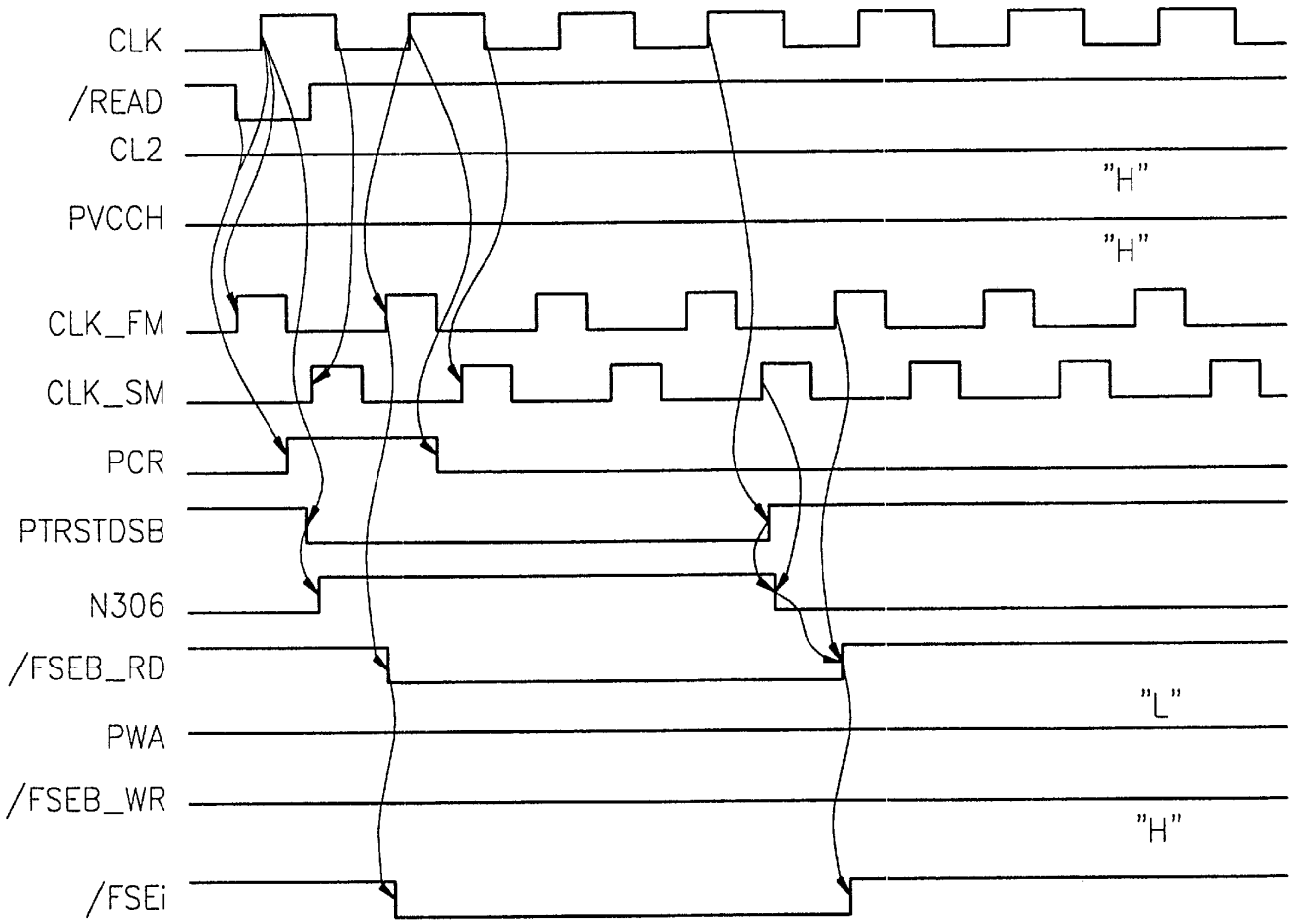

CLK
/READ
CL2
PVCCH
CLK_FM
CLK_SM
PCR
PTRSTDSB
N306
/FSEB_RD
PWA
/FSEB_WR
/FSEi
"H"
"H"
"L"
"H"

FIG. 7

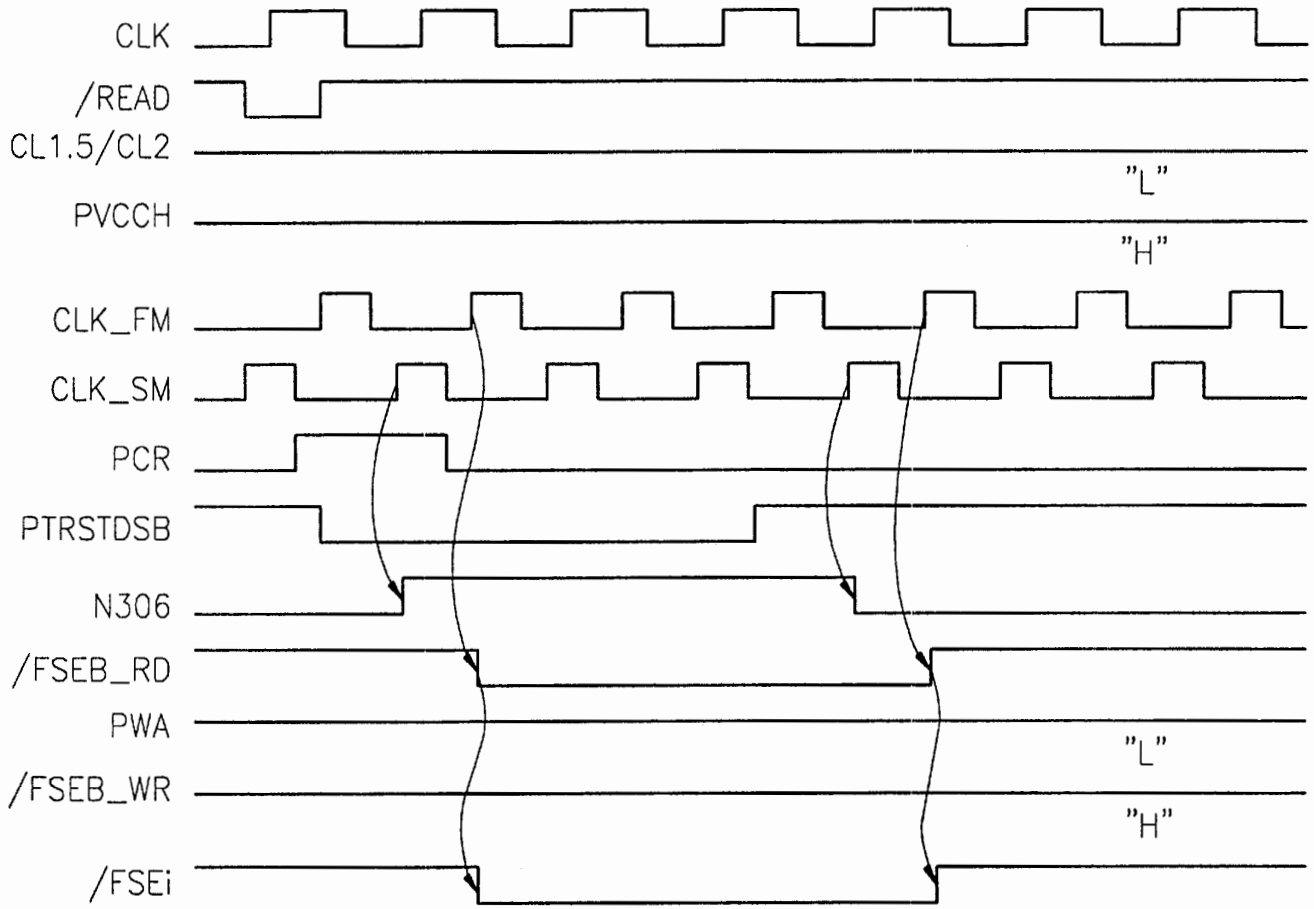

CLK
/READ
CL1.5/CL2
"L"
PVCCH
"H"
CLK_FM
CLK_SM
PCR
PTRSTDSB
N306
/FSEB_RD
PWA
"L"
/FSEB_WR
"H"
/FSEi

FIG. 8

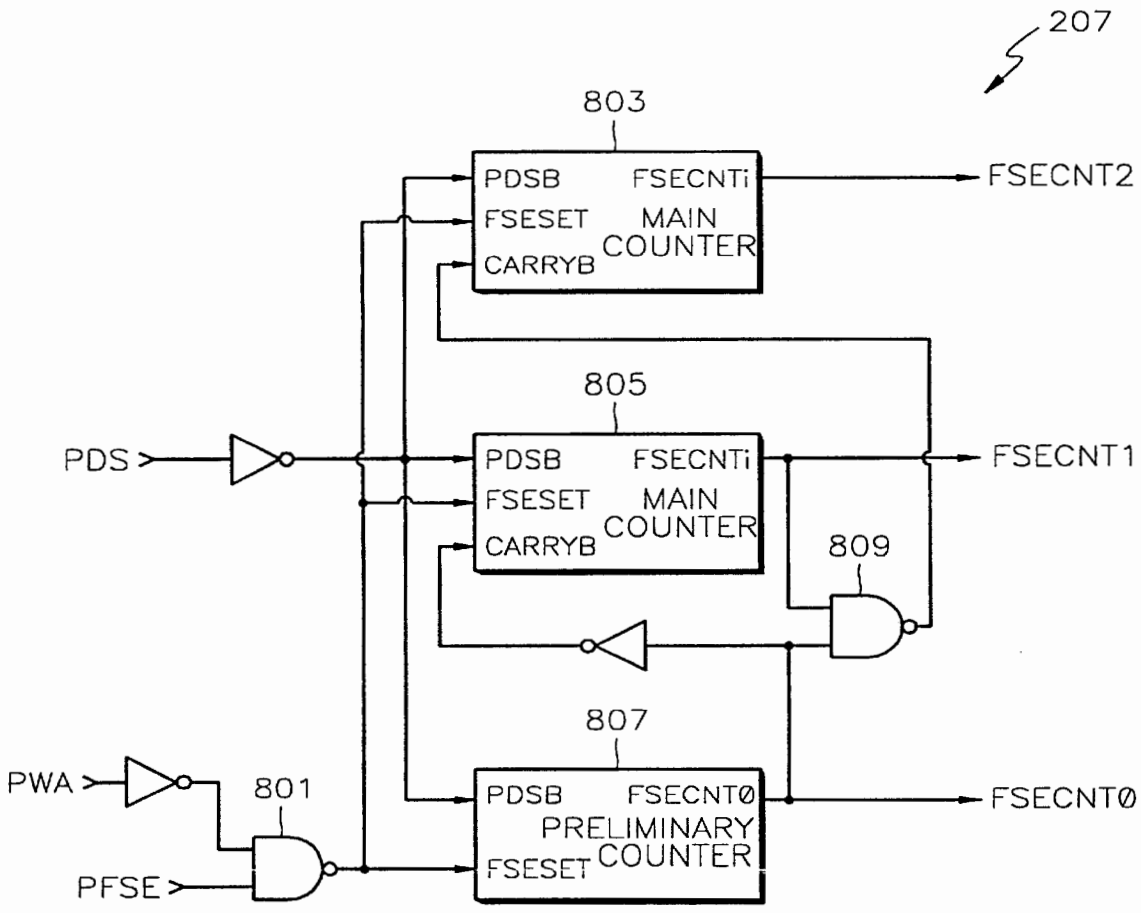

207
803
PDSB
FSECNTi
FSESET
MAIN
COUNTER
CARRYB
FSECNT2
805
PDS
PDSB
FSECNTi
FSESET
MAIN
COUNTER
CARRYB
FSECNT1
809
807
PWA
801
PDSB
FSECNT0
PRELIMINARY
COUNTER
FSESET
FSECNT0
PFSE

FIG. 9

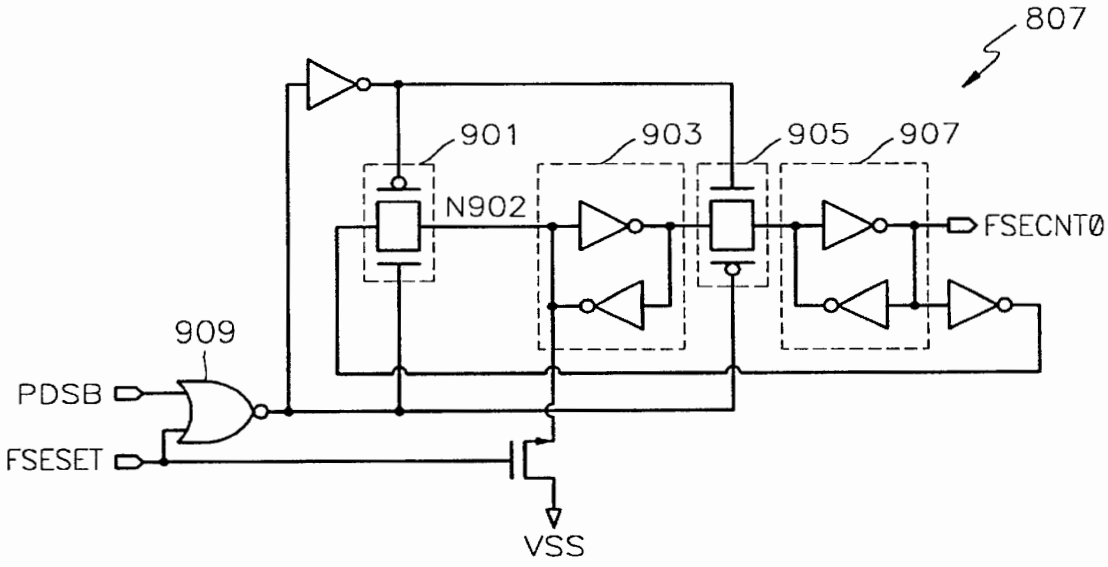

807
901
903
905
907
N902
FSECNT0
909
PDSB
FSESET
VSS

FIG. 10

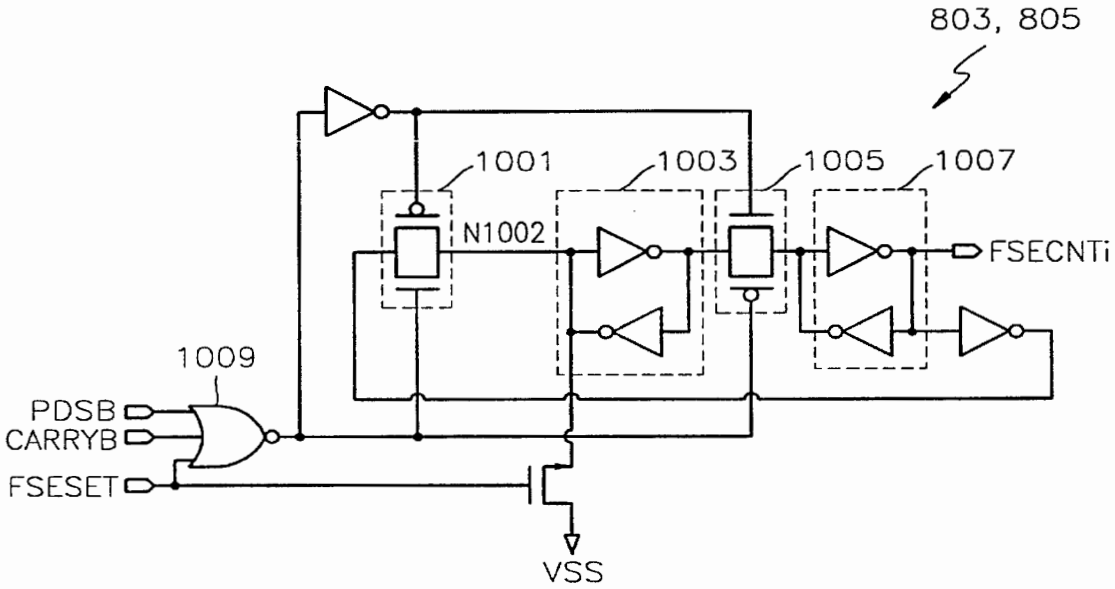

803, 805
1001
1003
1005
1007
N1002
FSECNTi
1009
PDSB
CARRYB
FSESET
VSS

FIG. 11

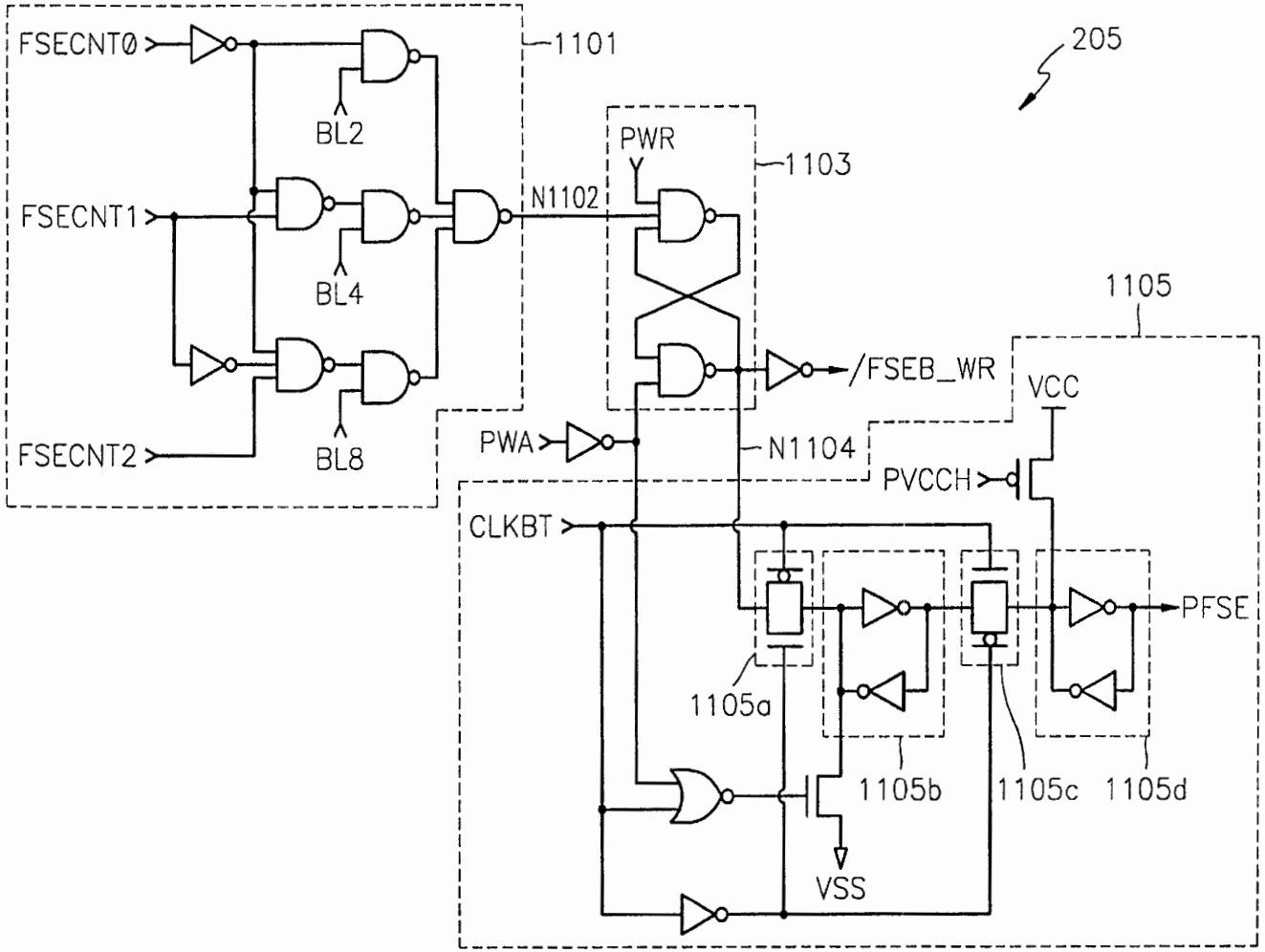

FSECNT0
FSECNT1
FSECNT2
BL2
BL4
BL8
1101
205
PWR
1103
N1102
/FSEB_WR
1105
VCC
PWA
N1104
PVCCH
CLKBT
PFSE
1105a
1105b
1105c
1105d
VSS

FIG. 12

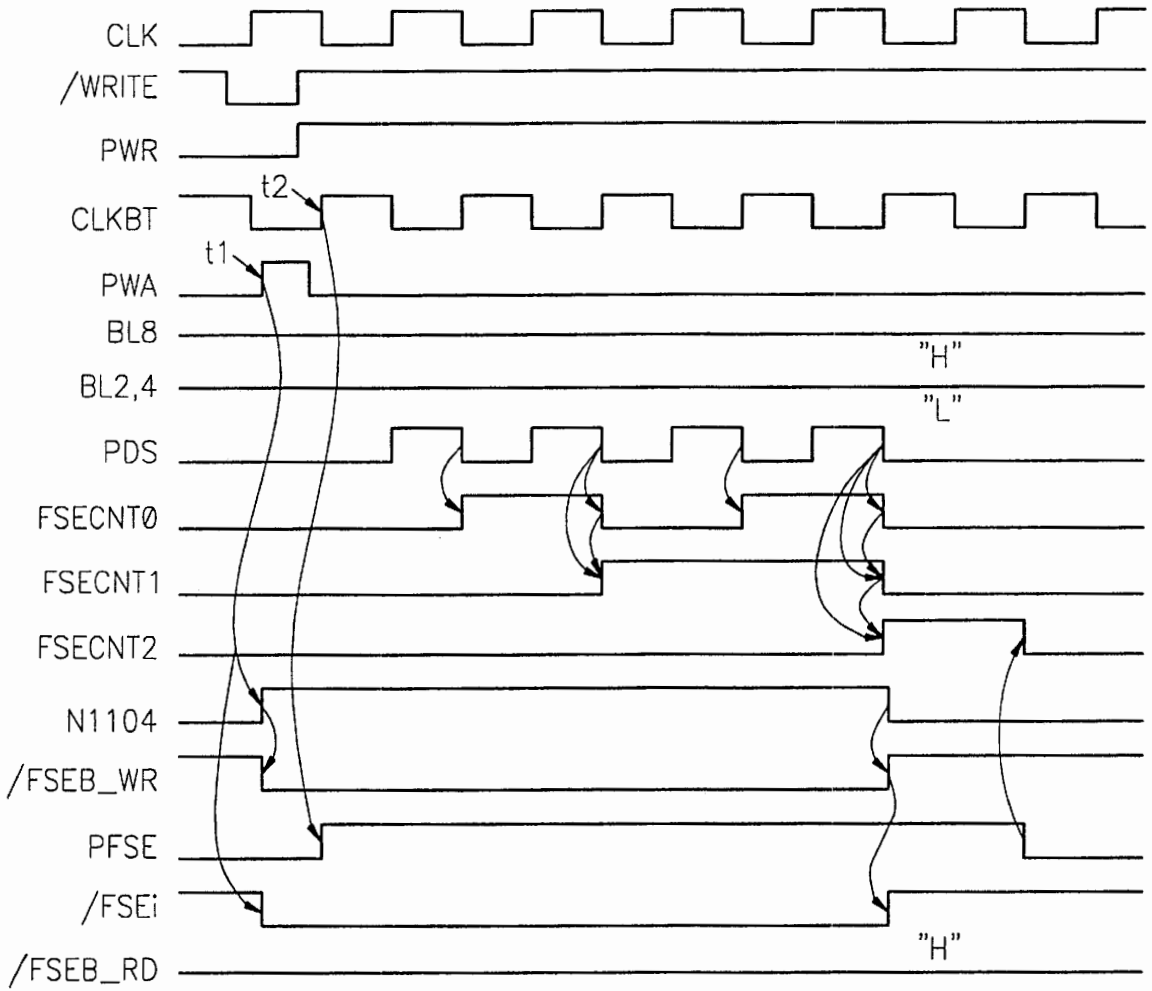

CLK
/WRITE
PWR
t2
CLKBT
t1
PWA
BL8
"H"
BL2,4
"L"
PDS
FSECNT0
FSECNT1
FSECNT2
N1104
/FSEB_WR
PFSE
/FSEi
"H"
/FSEB_RD

FIG. 13

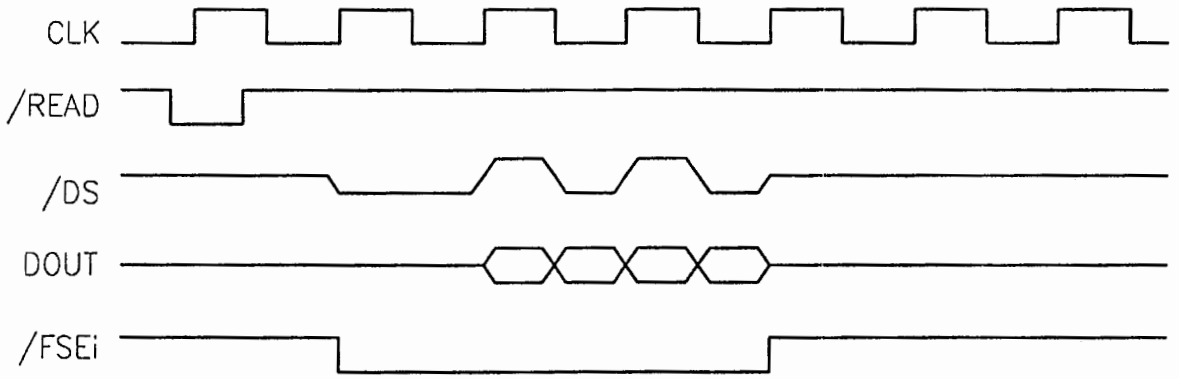


FIG. 14

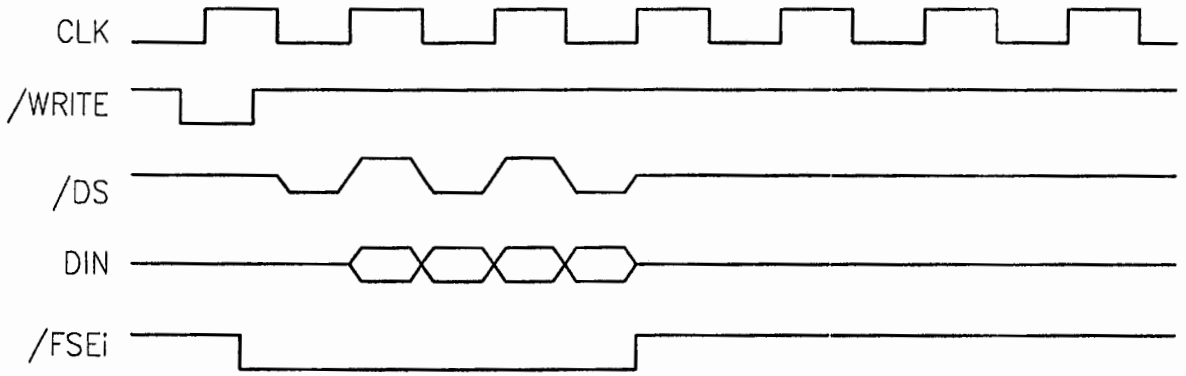
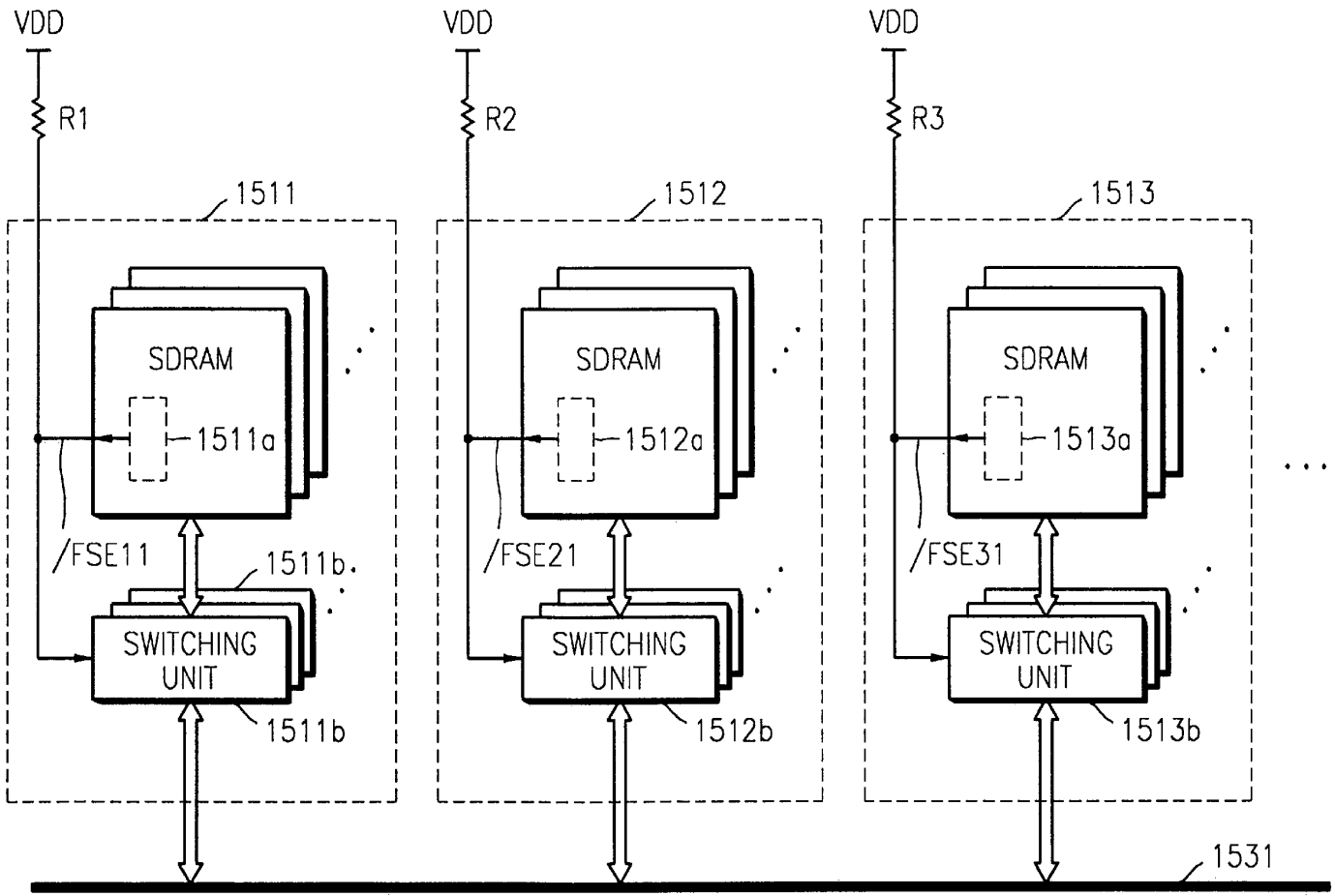


FIG. 15



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MEMORY MODULE SYSTEM FOR CONTROLLING DATA INPUT AND OUTPUT BY CONNECTING SELECTED MEMORY MODULES TO A DATA LINE

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a system with memory modules for controlling data input and output, and more particularly, to a system having a multiplicity of memory modules for controlling data input and output from and to a common data line by connecting selected memory modules to the common data line.

2. Description of the Related Art

A semiconductor memory device such as a dynamic random access memory (DRAM) can be used as a main memory in a system such as a computer. A memory using semiconductor memory devices generally has memory modules, such as dual in-line memory modules (DIMM) and single in-line memory modules (SIMM). A memory may be required to include a plurality of memory modules for operations of a system. In such a system, each of the memory modules uses a common data line. For instance, assuming that a main memory has a capacity of 32M bytes and is made with DIMMs each of which has a capacity of 8M bytes and made of four 16M (1M×16) DRAMs, the main memory of 32M bytes requires four slots, i.e., four DIMMs. Since the number of data bus lines is 64 and the number of data pins per DIMM is 64, the main memory of 32M bytes requires a multiplicity of data pins. Thus, four DIMMs constituting the main memory of 32M bytes use a common data bus line of a system. As the capacity of the main memory is increased, the necessity of using a common data line is increased.

The capacitance per data pin of a DIMM module is 20~25 pF. Thus, when the 32M byte memory is composed of four DlMMs of 1M×64, the capacitance per data pin becomes approximately 80~100 pF. Thus, the capacitance per data pin is so great that an increase in the load of an output driver increases power consumption, and that speed for writing and reading data is remarkably reduced.

SUMMARY OF THE INVENTION

It is an object of the present invention to provide a memory module with minimized load capacitance per data pin to improve speed of writing and reading data and of the memory module.

To achieve the above and other objects, according to an aspect of the present invention, there is provided a memory module system for controlling data output to a data bus line, the system comprising a multiplicity of memory modules each of which includes a control signal generation circuit for generating a connection control signal having a width of activation corresponding to a burst length of output data, wherein the control signal generation circuit has a read control unit for activating input data during output of data of a predetermined burst length in a read mode to generate a read control signal, the read control unit receiving CAS latency information, a read command signal and burst length information of read data, and a multiplicity of switching units for electrically connecting output terminals of the memory modules to the data bus line in response to activation of the connection control signal. In the memory module system according to the present invention, the memory modules for receiving outputting data are electrically connected to the data bus line in response to activation of the connection control signals. The control signal generation circuit further comprises a write information generation unit. The write information generation unit receives a write command signal and burst length information of write data, and it is activated in a write mode during inputting data of a predetermined burst length to generate a write control signal.

In a memory module system for controlling data input and output according to the present invention, selected memory modules are connected to a data line during a data burst length in which data is input and output. Thus, load is minimized per data pin, so that speed of writing and reading data is improved.

BRIEF DESCRIPTION OF THE DRAWINGS

The above and other objects and advantages of the present invention will become more apparent by describing in detail a preferred embodiment thereof with reference to the attached drawings in which:

FIG. **1** is a block diagram schematically showing a system having a multiplicity of memory modules according to a first embodiment of the present invention;

FIG. **2** is a block diagram of one of the control signal generation circuits of FIG. **1**;

FIG. **3** is a circuit diagram of the read control unit of FIG. **2**;

FIG. **4** is a circuit diagram of the control signal generation unit of FIG. **2**;

FIGS. **5** through **7** are timing diagrams of control and data signals in FIGS. **3** and **4** in a read mode having CAS latencies of 1.5, 2 and 2.5, respectively;

FIG. **8** is a circuit diagram of the burst counter of FIG. **2**;

FIG. **9** is a circuit diagram of the preliminary counter of FIG. **8**;

FIG. **10** is a detailed circuit diagram of one of the main counters of FIG. **8**;

FIG. **11** is a circuit diagram of the write control unit of FIG. **2**;

FIG. **12** is a timing diagram of control and data signals related to the burst counter of FIG. **2**;

FIG. **13** is a timing diagram of external signals of memory modules in a read mode of a DDR mode in a system of the present invention;

FIG. **14** is a timing diagram of external signals of memory modules in a write mode of a DDR mode in a system of the present invention; and

FIG. **15** is a block diagram schematically showing a system having a multiplicity of memory modules according to a second embodiment of the present invention.

DESCRIPTION OF PREFERRED EMBODIMENTS

Referring to FIG. **1**, a first embodiment of a memory module system according to the present invention has a multiplicity of memory modules. For convenience, three memory modules, i.e., first through third memory modules **111**, **112** and **113**, are shown. The first through third memory modules **111**, **112** and **113** are selected, so that output data is transferred to a common data bus line **131** through switching units **121**, **122** and **123**.

Each of the switching units includes switches, through which data is output from a corresponding memory module.

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Also, the data output through the switches is transferred to the data line bus **131**. Each of the switching units **121**, **122** and **123** is turned on when data is input to and output from the corresponding memory module. However, when data is not input to or output from the corresponding memory module, each of the switching units **121**, **122** and **123** is turned off. For instance, assuming that the first memory module **111** is selected, to input or output data to or from the first memory module **111**, a first connection control signal /FSE**1** is activated to logic "low", so that the first switching unit **121** is turned on. Thus, output data of the first memory module **111** is transferred to the data bus line **131** through the first switching unit **121**. At this time, second and third connection control signals /FSE**2** and /FSE**3** are deactivated to logic "high" by an external power supply voltage VDD applied through resistors R**2** and R**3**, respectively. The resistors R**2** and R**3** may be external to the memory modules **112** and **113**.

In detail, the resistors R**1** to R**3** have relatively high resistances. Thus, voltage levels of the first through third connection control signals /FSE**1**, /FSE**2** and /FSE**3** are determined by the first through third memory modules **111**, **112** and **113**, respectively. However, when signals to determine the voltage levels of the connection control signals /FSE**1**, /FSE**2** and /FSE**3** in the respective memory modules are in floating state, the voltage levels of the first through third connection control signals /FSE**1**, /FSE**2** and /FSE**3** become an external power supply voltage VDD, i.e., logic "high", applied through the resistors R**1** to R**3** connected to the respective memory modules. That is, when the first memory module **111** is selected, the second and the third connection control signals /FSE**2** and /FSE**3** become logic "high". The second and the third connection control signals /FSE**2** and /FSE**3** deactivated to the "high" then turn off the second and the third switching units **122**, **123**. Thus, load of data pins of the second and third memory modules **112** and **113** is separated from the data bus line **131**. In other words, memory modules other than the selected memory module are separated from the data line **131**, to thereby reduce load of the data bus line **131**.

Preferably, each of the first through third connection control signals /FSE**1**, /FSE**2** and /FSE**3** is generated by the corresponding memory modules **111**, **112** and **113**. Control signal generation circuits **111***a*, **112***a* and **113***a* which are included in the corresponding memory modules **111**, **112** and **113** generate the first through third connection control signals /FSE**1**, /FSE**2** and /FSE**3**, respectively. Also, activation intervals of the first through third connection control signals /FSE**1**, /FSE**2** and /FSE**3** are preferably determined by burst lengths of input or output data. Also, the first through third connection control signals /FSE**1**, /FSE**2** and /FSE**3** may be provided from a control unit (not shown) which transfers the input data from the outside of the memory modules.

FIG. **2** is a block diagram illustrating a preferred embodiment of a control signal generation circuit according to the present invention. As described above, the control signal generation circuits **111***a*, **112***a* and **113***a* each having the same configuration as in FIG. **2** are included in the memory modules **111**, **112** and **113**, respectively. For convenience, the first through third connection control signals /FSE**1**, /FSE**2** and /FSE**3** are indicated by /FSEi.

Referring to FIG. **2**, the control signal generation circuit includes a read control unit **201**, a control signal generation unit **203**, a write control unit **205** and a burst counter **207**. The read control unit **201** receives column address strobe (CAS) latency signals CL**1.5** and CL**2**, a read command signal PCR and a read strobe signal PTRSTDSB, and generates a read control signal /FSEB_RD. The CAS latency signals CL**1.5** and CL**2** include /CAS latency information, and the read command signal PCR introduces a read command for a read mode. The read strobe signal PTRSTDSB includes information on a burst length of read data, for example, information on burst signals BL**2**, BL**4** and BL**8** input to the write control unit **205**. Also, the read control signal /FSEB_RD is activated in response to the burst length of the read data in the read mode. The read control unit **201** will be described in detail with reference to FIG. **3**.

The control signal generation unit **203** supplies the connection control signal /FSEi in response to the read control signal /FSEB_RD and a write control signal /FSEB_WR. The write control signal /FSEB_WR supplied by the write control unit **205**, is activated for an interval corresponding to a burst length of data input in a write mode. Thus, the connection control signal /FSEi is activated in response to the read control signal /FSEB_RD in the read mode, and also activated in response to the write control signal /FSEB_WR in the write mode. The control signal generation unit **203** will be described in detail, with reference to FIG. **4**.

The write control unit **205** receives burst signals BL**2**, BL**4** and BL**8** and first and second write command signals PWA and PWR, and generates a write control signal /FSEB_WR and a counter control signal PFSE. Here, the burst signals BL**2**, BL**4** and BL**8** include information on burst lengths of data in a write mode. The first write command signal PWA is a pulse indicating that a memory module enters into a write mode, in response to a write command. The second write command signal PWR indicates that a memory module is in a write mode.

The write control signal /FSEB_WR which is activated for an interval corresponding to the data burst length in which data is input in the write mode, is supplied to the control signal generation unit **203**. Also, the counter control signal PFSE which is supplied to the burst counter **207**, is activated in response to an inverted clock signal CLKBT which is firstly generated after generating the write command signal, and deactivated after receiving a predetermined number of data. The inverted clock signal CLKBT is an inverted signal of an external clock signal CLK (not shown). The write control unit **205** will be described in detail with reference to FIG. **11**.

The burst counter **207** is enabled in response to the activation of the counter control signal PFSE. The burst counter **207** receives a first write command signal PWA and a data strobe signal PDS, and counts the number of input data. Also, a counting signal FSECNTi (where, i=0 to 2) indicating the number of input data is supplied to the write control unit **205**. The data strobe signal PDS indicating an input of data, is formed by an external data strobe signal of a memory module. The data strobe signal PDS indicates an input or output of one of the data by one transition in a double data rate (DDR). The memory module system of the present invention will be described in the DDR mode. The number of input data can be indicated by a combination of the counting signals FSECNTi, where i=0 to 2. The burst counter **207** will be described in detail with reference to FIG. **8**.

A control signal generation circuit which generates the connection control signal /FSEi can be realized with the read control unit **201** and the control signal generation unit **203** of FIG. **2** in a read mode. A write information generation unit

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209 for activating the write control signal /FSEB_WR for an interval corresponding to the burst length of data input may be realized in a write mode with the write control unit 205 and the burst counter 207. Thus, the control signal generation circuit for generating the connection control signal /FSEi may be realized in the write mode with the write information generation unit 209 and the control signal generation unit 203 of FIG. 2.

FIG. 3 is a circuit diagram of a preferred embodiment of the read control unit 201 in FIG. 2. Referring to FIG. 3, the read control unit 201 includes a first latency response unit 301, a second latency response unit 303, a first transfer unit 309, a first latch unit 307, a second transfer unit 305 and a second latch unit 311.

The first latency response unit 301 is enabled in response to a CAS latency shorter than a predetermined latency. According to a preferred embodiment of the present invention, the first latency response unit 301 is enabled, when the CAS latency is 1.5. The first latency response unit 301 includes a logic gate 301*a* and a drive transistor 301*b*. The logic gate 301*a* is enabled by activation of CL1.5 indicating the CAS latency of 1.5, and responds to a read command signal PCR. The read command signal PCR is activated in response to a first clock signal from generation of a read command, and. is maintained in the activated state during a period of one clock. The drive transistor 301*b* is gated by an output signal 301*n* of the logic gate 301*a*. Thus, the transistor 301*b* outputs an output signal to the first latch unit 307 in response to activation of the read command signal PCR. Preferably, the logic gate 301*a* is a NAND gate, and the transistor 301*b* is a PMOS transistor.

When the CAS latency is two or more, the second latency response unit 303 is enabled. An output signal N304 of the second latency response unit 303 maintains a logic "high" state by activation of a read strobe signal PTRSTDSB. The second latency response unit 303 includes logic gates 303*a* and 303*b*. The logic gate 303*a* is enabled by activation of CL2 indicating the CAS latency of 2, and responds to the read command signal PCR. Also, the logic gate 303*b* is enabled by the output signal 303*n* of the logic gate 303*a*, and responds to the read strobe signal PTRSTDSB. Preferably, the logic gates 303*a* and 303*b* are NAND gates. The second transfer unit 305 transfers the output signal N304 of the second latency response unit 303 in response to a first clock signal CLK_SM.

The first latch unit 307 latches either the output signal of the first latency response unit 301 or the output signal N304 of the second latency response unit 303 transferred by the second transfer unit 305. The first transfer unit 309 transfers signals latched by the first latch unit 307 in response to a second clock signal CLK_FM. The second latch unit 311 latches a signal N306 transferred by the first transfer unit 309, and outputs the latched signal as a read control signal /FSEB_RD.

Here, the first and the second clock signals CLK_SM and CLK_FM are pulse signals generated in response to rising and falling transitions of the external clock signal CLK. The first and the second clock signals CLK_SM and CLK_FM which control data output timing, have timing with respect to the external clock signal CLK as shown in FIGS. 5 through 7.

FIG. 4 is a circuit diagram illustrating a preferred embodiment of the control signal generation unit 203 of FIG. 2. Referring to FIG. 4, the control signal generation unit 203 includes a NAND gate 401, a PMOS transistor 403 and an NMOS transistor 405. The NAND gate 401 receives an inverted signal of the read control signal /FSEB_RD, an inverted signal of the write control signal /FSEB_WR and the first write command signal PWA. That is, the NAND gate 401 is enabled by the first write command signal PWA, and acts as a logic gate responding to the read control signal /FSEB_RD or the write control signal /FSEB_WR.

The NMOS transistor 405 is gated by an output signal of the NAND gate 401. Thus, the NMOS transistor 405 acts for driving connection control signal in response to the read control signal /FSEB_RD or the write control signal /FSEB_WR.

The PMOS transistor 403 has source and gate terminals which are in common connected. A drain terminal of the PMOS transistor 403 and a drain terminal of the NMOS transistor 405 are in common connected to generate the connection control signal /FSEi.

In a precharge state, the read control signal /FSEB_RD and the write control signal /FSEB_WR are both logic "high" and the first write command signal PWA is logic low. Thus, the output signal of the NAND gate 401 becomes low and the NMOS transistor 405 is turned off. The connection control signal /FSEi becomes logic "high" in response to an external power supply voltage VDD applied through a resistor outside a memory module.

An embodiment of a control signal generation circuit for generating a connection control signal can be realized with the read control unit 201 in FIG. 3 and the control signal generation unit 203 in FIG. 4 in a read mode.

FIGS. 5 through 7 are timing diagrams of control signals and data signals in FIGS. 3 and 4 in a read mode in which CAS latencies are 1.5, 2, and 2.5, respectively. Assuming that a data burst length is 4, and the memory modules operate in a DDR mode, the operation of the read control unit 201 when the CAS latency is 1.5, will FIG. 5 be described with reference to FIGS. 3, 4 and 5.

Referring to FIG. 5, a logic state of the CAS latency signal CL1.5 is high, and a logic state of the CAS latency signal CL2 is low. Activation of /READ signal to low state indicates a generation of a read command. The read command signal PCR is activated for one clock period in response to a rising edge of the first clock pulse CLK1 after the generation of the read command. Thus, the output signal N306 of the first latency response unit 301 becomes logic "high" in response to the read command signal PCR, and is latched to high by the first latch unit 307. That is, when the read command is generated, the output signal N306 of the first latency response unit 301 is latched to high by the first latch unit 307, regardless of a level of the clock signal.

The read strobe signal PTRSTDSB is activated to logic "low" in response to activation of the read command signal, and is activated to logic "high" after a period of time corresponding to the data burst length. The output signal N304 of the second latency response unit 303 is transferred to the first latch unit 307 by the second transfer unit 305 turned on in response to the first clock signal CLK_SM. Thus, when the read strobe signal PTRSTDSB is activated to logic "low", the input signal at the terminal N306 of the first latch unit 307 is maintained at logic "high" even when the read command signal PCR is deactivated to logic "low".

Data latched by the first latch unit 307 is transferred to the second latch unit 311 by the first transfer unit 309 turned on in response to the second clock signal CLK_FM. The output signal of the second latch unit 311 is connected to an output terminal of the read control signal /FSEB_RD. Thus, the read control signal /FSEB_RD is activated to logic "low" in response to the generation of the read command, and then

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deactivated to high in a period of time corresponding to the burst length. That is, a time period of the activation of the read control signal /FSEB_RD corresponds to that of the burst length.

In a read mode, the first write command signal PWA is maintained at logic "low", and the write control signal /FSEB_WR is maintained at logic "high". Thus, in the read mode, activation of the connection control signal /FSEi depends on activation of the read control signal /FSEB_RD.

In a preferred embodiment of the present invention, when the CAS latency is 1.5, the input signal N306 of the first latch unit 307 is activated regardless of the clock signal, and the activation is maintained by the read strobe signal PTRSTDSB. When the read control signal /FSEB_RD is activated in response to the first clock signal CLK_SM, the connection control signal /FSEi is not activated until a first data burst is read, despite of the CAS latency of 1.5.

The operation of the read control unit 201 with the CAS latency of 2 will now be described, with reference to FIGS. 3, 4 and 6. A logic state of the CAS latency signal CL2 is high, and a logic state of the CAS latency signal CL1.5 is low. Thus, the output signal N306 of the first latency response unit 301 does not respond to the read command signal PCR.

The output signal N304 of the second latency response unit 303 is activated to high in response to an activation of the read command signal PCR, and is transferred to the first latency unit 307 in response to an activation of the first clock signal CLK_SM. The logic state of the input signal N306 of the first latch unit 307 is maintained at high in response to activations of both the read strobe signal PTRSTDSB and the first clock signal CLK_SM.

Thus, the read control signal /FSEB_RD, similar to the case of the CAS latency of 1.5, is activated to low in response to a generation of the read command, and deactivated to high after a period corresponding to the burst length. That is, the read control signal /FSEB_RD is activated for an interval corresponding to the burst length.

The operation of the read control unit 201 when the CAS latency is 2 or more, i.e., the logic states of the CAS latency signals CL1.5 and CL2 are low, will now be described with reference to FIGS. 3, 4 and 7. The output signal N304 of the second latency response unit 303 becomes high after the read strobe signal PTRSTDSB is activated to low. The output signal N304 of the second latency response unit 303 is transferred to the first latch unit 307 in response to activation of the first clock signal CLK_SM. When the read strobe signal PTRSTDSB is deactivated to high, the input signal N306 of the first latch unit 307 becomes low. Thus, the read control signal /FSEB_RD is activated or deactivated by the read strobe signal PTRSTDSB, unlike the case in which the CAS latency is 1.5 or 2.

As described above, the control signal generation circuit according to a preferred embodiment of the present invention generates a connection control signal activated in response to the data burst length in which data is read from a memory module in a read mode. Also, only the memory module selected by the connection control signal is connected to a data line during the data burst length in which data is output.

FIG. 8 is a circuit diagram illustrating an embodiment of the burst counter 207 of FIG. 2. In FIG. 8, a burst counter capable of counting eight data bursts is shown. The burst counter 207 shown in FIG. 8 includes one preliminary counter 807 and two main counters 803 and 805. The preliminary counter 807 and the main counters 803 and 805 are reset by activation of a counter control signal PFSE. That is, when a write command is generated so that the counter control signal PFSE is activated to high, the preliminary counter 807 and the main counters 803 and 805 are reset. Output signals of the preliminary counter 807 and the main counters 803 and 805, i.e., first through third counting signals FSECNT0~2 are reset to low.

As described above, a data strobe signal PDS indicates inputs of external data during rising and falling transitions in a DDR mode. Structure and operation of the burst counter 207 in a DDR mode will now be described.

In an embodiment of the present invention, data is input during rising and falling edges of the data strobe signal PDS, and the data is continuously input when a phase transition of the data strobe signal PDS is repeated. The first counting signal FSECNT0 performs the phase transition at every falling edge of the input data strobe signal. Also, when carries CARRYBs of the main counters 803 and 805 are activated to low, the second and the third counting signals FSECNT1~2 repeat the phase transition every two inputs of data.

Referring to FIG. 8, the carry CARRYB of the main counter 805 is activated to low, when the first counting signal FSECNT0 is activated to high. The carry CARRYB of the main counter 803 is activated to low, when the first and the second counting signals FSECNT0~1 are high.

The preliminary counter 807 and the main counters 803 and 805 of FIG. 8 will now be described with reference to FIGS. 9 and 10, respectively. FIG. 9 is a detailed circuit diagram illustrating an embodiment of the preliminary counter 807 of FIG. 8. Referring to FIG. 9, the preliminary counter 807 includes first and second transfer units 901 and 905, first and second latch units 903 and 907, and a NOR gate 909. The NOR gate 909 performs an OR operation on a reset signal FSESET and an inverted signal PDSB of the data strobe signal PDS and inverts the OR-operated signals. The reset signal FSESET is connected to the counter control signal PFSE. Thus, when the reset signal FSESET is disabled to low, the preliminary counter 807 is enabled to respond to the phase transition of the inverted signal PDSB. That is, when a phase of the inverted signal PDSB is transited from high to low, the first transfer unit 901 is turned on. When the phase of the inverted signal PDSB is transited from low to high, the second transfer unit 905 is turned on. Whenever the inverted signal PDSB is deactivated, the first counting signal FSECNT0 repeats the phase transition.

FIG. 10 is a detailed circuit diagram illustrating an embodiment of the main counters 803 and 805 of FIG. 8. The main counters 803 and 805 may have the same structure as shown in FIG. 10. For convenience, output signals of the main counters 803 and 805, i.e., second and third counting signals FSECNT1~2, are indicated by a counting signal FSECNTi.

A main counter has a structure and operation similar to those of the preliminary counter 807 of FIG. 9. However, a NOR gate 1009 with three input terminals is used, to which a reset signal FSESET, an inverted signal PDSB and a carry CARRYB are provided. Thus, when the reset signal FSESET and the carry CARRYB are low, the main counter is enabled in response to a phase transition of the inverted signal PDSB. That is, when the reset signal FSESET and the carry CARRYB are low, the counting signal FSECNTi repeats the phase transition whenever the inverted signal PDSB is deactivated.

FIG. 11 is a detailed circuit diagram illustrating an embodiment of the write control unit 205 of FIG. 2. Refer-

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ring to FIG. **11**, the write control unit **205** includes a counting response unit **1101**, a latch unit **1103** and a counter control signal generation unit **1105**. The counting response unit **1101** indicates a data burst of input data. That is, a phase of an output signal N**1102** is transited when a predetermined number of data is input.

When the first write command signal PWA is activated to high, the latch unit **1103** is enabled to respond to the output signal N**1102** of the counting response unit **1101**. When the second write command signal PWR becomes high, an output signal N**1104** of the latch unit **1103** is latched to high. At this time, a write control signal /FSEB_WR connected to an output terminal inverting the output signal N**1104** of the latch unit **1103** is activated to low. When the first write command signal PWA becomes low, the output signal N**1104** of the latch unit **1103** is maintained at high. When the second write command signal PWR is high and the predetermined number of data is input so that the output signal N**1102** of the counting response unit **1101** is transited to low, the output signal N**1104** of the latch unit **1103** becomes low, and the write control signal /FSEB_WR is deactivated to high.

The counter control signal generation unit **1105** includes first and second transfer units **1105***a* and **1105** and first and second latches **1105***b* and **1105***d*. The first transfer unit **1105***a* transfers the output signal N**1104** of the latch unit **1103** in response to a falling edge of an inverted clock signal CLKBT. The first latch unit **1105***b* latches a signal transferred by the first transfer unit **1105***a*. The second transfer unit **1105***c* transfers an output signal of the first latch **1105***b* in response to a rising edge of the inverted clock signal CLKBT. Also, the second latch **1105***d* latches a signal transferred by the second transfer unit **1105***c*, and generates a counter control signal PFSE. Here, the inverted clock signal CLKBT is an inverted signal of an external clock signal CLK.

FIG. **12** is a timing diagram of signals related to the burst counter illustrated in FIGS. **2** and **8** through **11** in a write mode. FIG. **12** shows a case of a data burst of 8 in a DDR mode. Operation of the write control unit **205**, the burst counter **207**, the preliminary counter **807** and the main counters **803** and **805** of the burst counter **207** will be described with reference to FIG. **12**.

The data burst is 8, that is, burst signal BL**8** is high and burst signals BL**2** and BL**4** are low. The DDR mode indicates that data is input in every phase transition of the data strobe signal PDS. When the first write command signal PWA becomes high (t1), the output signal N**104** of the latch unit **1103** is latched to high, and the write control signal /FSEB_WR is activated to low. When the second write command signal PWR is activated to high and activation and deactivation of the data strobe signal PDS are performed four times, i.e., 8 data are input, both the first and second counting signals FSECNT**0**~**1** become low and the third counting signal FSECNT**2** becomes high. At this time, the phase of the output signal N**1102** of the counting response unit **1101** is transited to low from high, and the output signal N**1104** of the latch unit **1103** becomes low. The write control signal /FSEB_WR is deactivated to high. The counter control signal PFSE is deactivated to low in response to a rising edge of the inverted clock signal CLKBT. The preliminary counter **807** and the main counters **803** and **805** are reset, so that the first through third counting signals FSECNT**0**~**2** become low.

Referring to FIG. **4** again, a connection control signal /FSEi is activated and deactivated in response to the write control signal /FSEB_WR in a write mode. During the write mode the read control signal /FSEB_RD is deactivated to high.

FIG. **13** is a timing diagram of external signals of memory modules when reading data in a DDR mode in a system of the present invention. Referring to FIG. **13**, the CAS latency is 2, and the burst length is 4. When a predetermined preamble interval, i.e., 1 clock cycle, passes after a read command is input, i.e., a signal /READ is activated, an external data strobe signal /DS is activated to low. The connection control signal /FSEi is also enabled to low, so that switching units **121**, **122** and **123** (see FIG. **1**) connected to the activated memory modules are turned on. First, data are output from the memory modules, and then the output data are transferred to the data line **131** (see FIG. **1**). When a postamble interval, i.e., a half clock, passes after the last data of a data burst is output, the external data strobe signal /DS becomes high impedance state. At this time, the connection control signal /FSEi of low is disabled to high, to thereby turn off the switching units **121**, **122** and **123**.

FIG. **14** is a timing diagram of external signals of memory modules in a write mode of a DDR mode in a system of the present invention. In FIG. **14**, the burst length is 4. In a ¼ clock cycle after a write command is input, i.e., a signal /WRITE is activated, the connection control signal /FSEi is enabled to low. Activated memory modules receive data corresponding to the burst length from a control unit (not shown) through the data bus line **131** (see FIG. **1**). When data holding time passes after last data is received, the connection control signal /FSEi of low is disabled to high to turn off the corresponding switching units **121**, **122** and **123**.

As described above, a control signal generation circuit according to a preferred embodiment of the present invention generates a connection control signal activated during an interval corresponding to the burst length in which data is written in a write mode. Only the memory module selected by the connection control signal is connected to a data line during the data burst length in which data is input.

FIG. **15** is a block diagram illustrating a second embodiment of the memory module system according to the present invention. Structure and operation of the memory module system according to the second embodiment are similar to those of the first embodiment. Switching units **1511***b*, **1512***b* and **1513***b* corresponding to the switching units **121**, **122** and **123** of FIG. **1** are installed in memory modules **1511**, **1512** and **1513**, respectively.

As shown in FIG. **15**, a multiplicity of SDRAMs (synchronous DRAMs) are installed in each of the memory modules. Also, a multiplicity of switching units each corresponding to each of the SDRAMs are installed in each of the memory modules. Connection control signals /FSE**11**, /FSE**21** and /FSE**31** controlling the switching units are generated by the SDRAMs included in the memory modules. For convenience, the connection control signals /FSE**11**, /FSE**21** and /FSE**31** are shown for controlling the switching units **1511***b*, **1512***b* and **1513***b*, respectively, each of which connects with a first SDRAM in a memory module. In FIG. **15**, although not shown, switching units connected to other SDRAMs exist, and connection control signals for controlling the switching units are generated from the corresponding SDRAMs. A switching unit may preferably have as many switches as output terminals for outputting data from an SDRAM corresponding to the switching unit. The data output through the multiple switches are transferred to a data bus line **1531**. Structure and operation of control signal generation circuits **1511***a*, **1512***a* and **1513***a* of the second embodiment in FIG. **15** are the same as those of the control signal generation circuits **111***a*, **112***a* and **113***a* of the first embodiment in FIGS. **2** through **14**.

Having described preferred embodiments of a memory module system of the present invention, it is noted that

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modification and variations can be made by persons skilled in the art in light of the above teachings. For example, the switches which are arranged outside the SDRAM may be arranged in the SDRAM. Also, other integrated memory circuit devices such as DRAMs or SRAMs may be used instead of SDRAMs. In a DDR mode, the counter circuit of the first embodiment of the present invention counts eight data by using one preliminary counter and two main counters. However, the number of main counters may be increased to increase the number of counted data.

Also, in a memory module system of the present invention, only selected memory modules are connected to a data line during a time period of data burst length in which data is input and output, so that load per data pin is minimized and data writing and reading speed is improved.

What is claimed is:

1. A memory module system for controlling data output to a data bus, the system comprising:

a multiplicity of memory modules each of which includes a control signal generation circuit for generating a connection control signal having a width of activation corresponding to a burst length of output data, wherein the control signal generation circuit has a read control unit for activating input data during output of data of a predetermined burst length in a read mode to generate a read control signal, the read control unit receiving CAS latency information, a read command signal and burst length information of read data; and

a multiplicity of switching units for electrically connecting output terminals of the memory modules to the data bus in response to activation of the connection control signal;

wherein the read control unit comprises:

a first latency response unit for being enabled in a first CAS latency;

a second latency response unit for being enabled in a second CAS latency;

a first latch unit for latching one of an output signal of the first latency response unit and an output signal of the second latency response unit; and

a first transfer unit for transferring a latched signal by the first latch unit to generate the read control signal in response to a first internal clock signal that is synchronized with a first external clock signal.

2. The memory module system of claim **1**, wherein the first CAS latency is 1.5, and the second CAS latency is 2.

3. The memory module system of claim **2**, wherein the connection control signal is activated in response to activation of a read strobe signal including the burst length information in case of a third CAS latency that is greater than the first and the second CAS latencies.

4. The memory module system of claim **1**, wherein the first latency response unit comprises:

a logic gate responding to activation of the first CAS latency and a read command signal; and

a drive transistor for driving an output signal to the first latch unit in response to an output signal of the logic gate.

5. The memory module system of claim **1**, wherein the second latency response unit comprises a logic gate responding to a predetermined read strobe signal which is activated during a period corresponding to the burst length of data.

6. The memory module system of claim **1**, wherein the memory modules are synchronized with a second external clock signal, and the read control unit further comprises:

a second transfer unit for transferring the output signal of the second latency response unit in response to a second internal clock signal synchronized with the second external clock signal; and

a second latch unit for latching a signal transferred by the first transfer unit to generate the read control signal.

7. The memory module system of claim **1**, wherein the connection control signal is activated by a read strobe signal including the first CAS latency and the burst length information.

8. The memory module system of claim **1**, wherein the control single generation circuit further comprising a control signal generation unit for generating the connection control signal in response to activation of the read control signal output from the read control unit.

9. The memory module system of claim **8**, wherein the control signal generation unit comprises:

a logic gate responding to the read control signal; and

a drive transistor for activating the connection control signal in accordance with the activation of the read control signal, the drive transistor being gated by an output signal of the logic gate.

10. A memory module system for controlling data output to a data bus, comprising:

a multiplicity of memory modules; and

a multiplicity of switching units for electrically connecting only memory module outputting data to the data bus in response to activation of a connection control signal, wherein the connection control signal is generated in the memory module outputting data and has a width of activation corresponding to a burst length of the output data;

wherein the connection control signal, with respect to a first and a second CAS latencies, is activated in response to a CAS latency and a read command signal, and the activation is maintained by a read strobe signal including the burst length information, and the connection control signal, with respect to a third CAS latency longer than the first and the second CAS latencies, is activated in response to activation of the read strobe signal.

11. A memory module system for controlling data input from a data bus, comprising:

a multiplicity of memory modules each of which includes a control signal generation circuit for generating a connection control signal having an activation width corresponding to a burst length of input data, wherein the control signal generation circuit includes a write information generation unit for receiving a write command signal and burst length information of write data, the write information generation unit being activated in a write mode during inputting data of a predetermined burst length to generate a write control signal; and

a multiplicity of switches for electrically connecting input terminals of the memory modules to the data bus in response to activation of the connection control signal;

wherein the write information generation unit comprises:

a write control unit for receiving the write command signal and for supplying the write control signal and a counter control signal; and

a burst counter for counting the number of external input data to supply the counted data to the write control unit, wherein the burst counter is enabled in response to activation of the counter control signal;

wherein the write control unit comprises:

a counting response unit for generating an output signal in response to input of data of a predetermined burst length in response to an output signal of the burst counter;

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a latch unit for being enabled in response to the write command signal, for latching the output signal of the counting response unit, and for supplying the write control signal; and

a counting control signal generation unit for being enabled in response to the write command signal and for inputting the write control signal to supply the counter control signal.

12. The memory module system of claim **11**, wherein the memory modules are synchronized with an external clock signal, and the latch unit comprises:

a first logic gate for being enabled by a first write command signal to generate the write control signal; and

a second logic gate for being enabled by a second write command signal and for responding to an output signal of the counting response unit;

wherein the data of the burst length is input, and then the write control signal is deactivated by the output signal of the counting response unit.

13. The memory module system of claim **11**, wherein the counting control signal generation unit comprises:

a first transfer unit for transferring an output signal of the latch unit in response to a first transition of the external clock signal;

a first latch for latching a signal transferred by the first transfer unit;

a second transfer unit for transferring the signal latched by the first latch in response to a second transition of the external clock signal; and

a second latch for latching the signal transferred by the first transfer unit to generate the counter control signal;

wherein a direction of the first transition is opposite to that of the second transition.

14. The memory module system of claim **11**, wherein the control signal generation circuit further comprises a control signal generation unit for being activated in response to the write command signal, and the activation is maintained by the write control signal.

15. The memory module system of claim **14**, wherein the control signal generation unit comprises:

a logic gate responding to the write information signal; and

a drive transistor for activating the connection control signal in response to the activation of the write control signal, the drive transistor being gated by an output signal of the logic gate.

16. A semiconductor memory device comprising:

a multiplicity of integrated memory circuit devices including a control signal generation circuit for generating a connection control signal having an activation width corresponding to a burst length of output data, wherein the control signal generation circuit comprises a read control unit for activating input data during output of data of a predetermined burst length in a read mode to generate a read control signal, the read control unit receiving CAS latency information, a read command signal and burst length information of data to be read; and

at least one switching unit for connecting output terminals of the integrated memory circuit devices where data is output and a data bus in response to activation of the connection control signal;

wherein the read control unit comprises:

a first latency response unit for being enabled in a first CAS latency;

a second latency response unit for being enabled in a second CAS latency;

a first latch unit for latching one of an output signal of the first latency response unit and an output signal of the second latency response unit; and

a first transfer unit for transferring a latched signal by the first latch unit to generate the read control signal in response to a first internal clock signal that is synchronized with a first external clock signal.

17. The semiconductor memory device of claim **16**, wherein the first CAS latency is 1.5, and the second CAS latency is 2.

18. The semiconductor memory device of claim **16**, wherein the first latency response unit comprises:

a logic gate responding to the activation of the first CAS latency and a predetermined read command signal; and

a drive transistor for driving an output signal to the first latch unit in response to an output signal of the logic gate.

19. The semiconductor memory device of claim **16**, wherein the second latency response unit comprises a logic gate responding to a predetermined read strobe signal, wherein activation of the read strobe signal is maintained during a period corresponding to a burst length of minimum data.

20. The semiconductor memory device of claim **16**, wherein the semiconductor memory device is synchronized with a second external clock signal, and the read control further comprises:

a second transfer unit for transferring the output signal of the second latency response unit to the first latch unit in response to a second internal clock signal synchronized with the second external clock signal; and

a second latch unit for latching a signal transferred by the first transfer unit to generate the read control signal.

21. The semiconductor memory device of claim **16**, wherein activation of the read control signal is maintained by a read strobe signal including the first CAS latency and the burst length information.

22. The semiconductor memory device of claim **21**, wherein the read control signal, with respect to a third CAS latency longer than the first and the second CAS latencies, is activated in response to activation of the read strobe signal including the burst length information.

23. A semiconductor memory device comprising:

a multiplicity of the integrated memory circuits including at least one control signal generation circuit for generating a connection control signal having an activation width corresponding to a burst length of input data, wherein the control signal generation circuit includes a write information generation unit for receiving burst length information of write command and write data, the control signal generation circuit being activated during input of data of a predetermined burst length in a write mode to generate a write control signal; and

at least one switching unit for connecting input terminals of the integrated memory circuits where data is input and a data bus in response to activation of the connection control signal;

wherein the write information generation unit comprises:

a write control unit for receiving the write command signal to supply the write control signal and a counter control signal; and

a burst counter for counting the number of external input data to supply the counted data to the write control unit, wherein the burst counter is enabled in response to activation of the counter control signal;

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wherein the write control unit comprises:

a counting response unit for generating an output signal responding to input of data having a predetermined burst length in response to an output signal of the burst counter;

a latch unit for being enabled in response to the write command signal to latch the output signal of the counting response unit, and for supplying the write control signal; and

a counting control signal generation unit for being enabled in response to the write command signal and for inputting the write control signal to supply the counter control signal.

24. The semiconductor memory device of claim **23**, wherein the semiconductor memory device is synchronized with an external clock signal, and the latch unit comprises:

a first logic gate for being enabled by a first write command signal to generate the write control signal; and

a second logic gate for being enabled by a second write command signal to respond to an output signal of the counting response unit;

wherein the write control signal is deactivated by the output signal of the counting response unit after input of data having a predetermined burst length.

25. The semiconductor memory device of claim **23**, wherein the counting control signal generation unit comprises:

a first transfer unit for transferring an output signal of the latch unit in response to a first transition of the external clock signal;

a first latch for latching a signal transferred by the first transfer unit;

a second transfer unit for transferring a signal latched by the first latch in response to a second transition of the external clock signal; and

a second latch for latching a signal transferred by the first transfer unit, to generate the counter control signal;

wherein a direction of the first transition is opposite to that of the second transition.

26. The semiconductor memory device of claim **23**, wherein the control signal generation circuit further comprises a control signal generation unit for generating the connection control signal activated in response to the write command signal and for maintaining the activation in accordance with the write control signal.

27. The semiconductor memory device of claim **26**, wherein the control signal generation unit comprises:

a logic gate responding to the write information signal; and

a drive transistor for activating the connection control signal in accordance with activation of the write control signal, the drive transistor being gated by an output signal by the logic gate.

* * * * *

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Electronic Acknowledgement Receipt

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Title of Invention:	LOAD-REDUCING CIRCUIT FOR MEMORY MODULE
First Named Inventor/Applicant Name:	Jefferey C. Solomon
Customer Number:	79141
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1	Transmittal Letter	2014-04-22_IDS_Cover_NETL018P2C7.pdf	58274 69dc86a78547a0d577ae92c57302778c1ef8210d	no	2
Warnings:					
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2	Information Disclosure Statement (IDS) Form (SB08)	2014-04-22_IDS_NETL018P2C7.pdf	93754 1dbbda6f5e7c8888e7d3d2f9a22cd50c76ad53f9	no	1
Warnings:					
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3	Non Patent Literature	4_1998-10-04_JP10-092169_A.pdf	401788 be7f040f479b2883e24237de412322f657033e4f	no	8
Warnings:					
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4	Non Patent Literature	5_JP2000311485.pdf	1419060 724c6967dfd9e530d631995c0a61eebc313563ea	no	24
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5	Non Patent Literature	6_2014-04-17_Office_Action_NT001JP.pdf	215909 58be10b16ae80bc1f78fbffdbfabb14a44a1bc3c	no	7
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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

INFORMATION DISCLOSURE STATEMENT

Applicant	:	BHAKTA et al.
App. No.	:	13/971,231
Filed	:	August 20, 2013
For	:	LOAD-REDUCING CIRCUIT FOR MEMORY MODULE
Examiner	:	Unknown
Art Unit	:	2189
Conf No.	:	2072

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Enclosed for filing in the above-identified application is a Form PTO/SB/08a/b Equivalent listing 6 references. Copies of foreign documents and/or their translation and non-patent literature are submitted herewith.

The applicants would appreciate the Examiner initialing and returning the Form PTO/SB/08a/b Equivalent indicating that the information has been considered and made of record herein.

The information contained in this Information Disclosure Statement is not to be construed as a representation that: (i) a complete search has been made; (ii) additional information material to this application does not exist; (iii) the information, protocols, results and the like reported by third parties are accurate or enabling; or (iv) the above information constitutes prior art to the subject invention.

This Information Disclosure Statement is being filed before the receipt of a first Office Action on the merits, and presumably no fee is required. If a first Office Action on the merits

was mailed before the mailing date of this Statement, the Commissioner is authorized to charge the fee set forth in 37 C.F.R. § 1.17(p) to Deposit Account No. 50-5963.

Respectfully submitted,

Dated: April 22, 2014

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13/971,231	08/20/2013	Jefferey C. Solomon	NETL.018P2C7	2072

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

jz@jzpatent.com

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Office Action Summary	Application No. 13/971,231	Applicant(s) SOLOMON ET AL.	
	Examiner GURTEJ BANSAL	Art Unit 2189	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08/20/2013*.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5)☒ Claim(s) *1-10* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☒ Claim(s) *1-10* is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☒ The drawing(s) filed on *08/20/2013* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☒ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date *04/07/2014; 04/07/2014; 04/07/2014; 04/08/2014; 04/22/2014*.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

4) ☐ Other: _____.

Samsung Electronics Co., Ltd.
Ex. 1052, p. 176

DETAILED ACTION

Remarks

The present application is being examined under the pre-AIA first to invent provisions.

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory double patenting rejection is appropriate where the claims at issue are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the reference application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of

activities undertaken within the scope of a joint research agreement. A terminal disclaimer must be signed in compliance with 37 CFR 1.321(b).

The USPTO internet Web site contains terminal disclaimer forms which may be used. Please visit http://www.uspto.gov/forms/. The filing date of the application will determine what form should be used. A web-based eTerminal Disclaimer may be filled out completely online using web-screens. An eTerminal Disclaimer that meets all requirements is auto-processed and approved immediately upon submission. For more information about eTerminal Disclaimers, refer to http://www.uspto.gov/patents/process/file/efs/guidance/eTD-info-I.jsp.

1. Claims 1-10 are provisionally rejected on the ground of nonstatutory double patenting as being unpatentable over claims 1, 6 and 8 of copending Application No. 13/287,042. Although the claims at issue are not identical, they are not patentably distinct from each other because claims 1, 6 and 8 of 13/287,042 anticipate the claims of present application.

"A later patent claim is not patentably distinct from an earlier patent claim if the later claim is obvious over, or anticipated by, the earlier claim. In re Longi, 759 F.2d at 896,225 USPQ at 651 (affirming a holding of obviousness-type double patenting because the claims at issue were obvious over claims in four prior art patents); In re Berq, 140 F.3d at 1437, 46 USPQ2d at 1233 (Fed. Cir. 1998) (affirming a holding of obviousness-type double patenting where a patent application claim to a genus is anticipated by a patent claim to a species within that genus). " ELI LILLY AND COMPANY v BARR LABORATORIES, INC., United States Court of Appeals for the

Federal Circuit, ON PETITION FOR REHEARING EN BANC (DECIDED: May 30, 2001).

This is a provisional nonstatutory double patenting rejection because the patentably indistinct claims have not in fact been patented.

Claim Rejections - 35 USC § 103

The following is a quotation of pre-AIA 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-10 are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Lai (US 2003/0070052), in view of Janzen (US 2004/0098528).

As per claims 1 and 10, Lai teaches a circuit for use on a memory module, the memory module including a plurality of memory devices and operable in a computer system to perform memory operations in response to memory commands from a memory controller, the circuit comprising:

Lai teaches logic (fig. 3, 108) to monitor the memory commands from the memory controller ([0012], describes a memory controller reading and writing) and to selectively isolate one or more first memory devices among the plurality of memory devices from the memory controller in response to the respective memory command so as to reduce a load of the memory module to the computer system while one or more second memory devices among the plurality of memory devices are communicating with

the memory controller in response to the set of output signals (As illustrated in fig. 3 with each memory device being isolated from the common set of DQ and DQS lines; [0035]).

Lai does not explicitly teach a register device to receive a set of control/address input signals associated with a respective memory command from the memory controller and to generate a set of control/address output signals in response to the set of control/address input signals, the set of control/address output signals being provided to the plurality of memory devices.

However, Janzen teaches a register device to receive a set of control/address input signals associated with a respective memory command from the memory controller (As illustrated in fig. 2 and described in [0025], lines 1-6) and to generate a set of control/address output signals in response to the set of control/address input signals, the set of control/address output signals being provided to the plurality of memory devices ([0025], lines 1-6 describe how the signals are reclocked).

It would have been obvious to a person of ordinary skill in the art at the time of the invention to have combined the register device of Janzen with the with the circuit of Lai because it allows for heavier loads to be placed on system buses without making the address and control lines too heavily loaded ([0025]).

As per claim 2, Lai teaches wherein the circuit further comprises multiple groups of DQ-DQS paths, and wherein the logic selectively isolate one or more first memory devices by disabling at least one first group of DQ-DQS paths corresponding to the one or more first memory devices (As illustrated in fig. 2, wherein when data is sent to one, the DQ-DQS would be disabled because no data would be transmitted thereon).

As per claim 3, Lai teaches wherein the logic is further configured to enable at least one second group of DQ-DQS paths in response to the respective memory command so as to allow the one or more second memory devices to communicate data with the memory controller in response to the output control/address signals (As illustrated in fig. 2, wherein when data is sent to one, the DQ-DQS would be disabled because no data would be transmitted thereon).

As per claim 4, Janzen teaches wherein the logic is further configured to translate between a system memory domain and a physical memory device domain such that a number of signals in the set of output control/address signals is greater than a number of signals in the set of input control/address signals (As illustrated in fig. 2 with input signals 260 being reclocked to each of the memory modules on both DIMMS).

As per claim 5, Lai teaches wherein the set of input control/address signals include at least one chip-select signal and the set of output control/address signals include a greater number of chip-select signals (As illustrated in fig. 2, one of the signals must be used to indicate which memory module is to receive data and as illustrated in fig. 4 and fig. 5 each respective memory module has a chip-select signal).

As per claim 6, Lai teaches wherein the logic element includes a buffer circuit to electrically and selectively isolate the one or more first memory devices from the memory controller and to selectively allow one or more second memory devices to communicate data with the memory controller (As illustrated in fig. 2), the buffer circuit adding a time delay to a data signal from the one or more second memory devices to

the memory controller ([0037] describes how the buffer implements a time delay when reading data).

As per claim 7, Lai teaches wherein the logic provides functions of a data path multiplexer /demultiplexer using the time delay (As illustrated in fig. 10).

As per claim 8, Lai teaches wherein the time delay is about one clock cycle ([0037]-[0038], describes a delay of ¼ clock cycle which is about 1 clock cycle).

As per claim 9, Lai teaches wherein the respective memory command is a read command or a write command (fig. 4 and fig. 5).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to GURTEJ BANSAL whose telephone number is (571)270-5588. The examiner can normally be reached on Monday - Friday, 7:30 a.m. - 5:00 p.m., EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Reginald Bragdon can be reached on (571)272-4204. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

GURTEJ BANSAL
Examiner
Art Unit 2189

/GURTEJ BANSAL/
Examiner, Art Unit 2189

Notice of References Cited	Application/Control No. 13/971,231	Applicant(s)/Patent Under Reexamination SOLOMON ET AL.	
	Examiner GURTEJ BANSAL	Art Unit 2189	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-2003/0070052	04-2003	Lai, Jiin	711/167
*	B	US-2004/0098528	05-2004	Janzen, Jeffery W.	710/305
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

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Ex. 1052, p. 184

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT
(Use as many sheets as necessary)

Sheet 1 of 1

Complete if Known	
Application Number	13/971,231
Filing Date	August 20, 2013
First Named Inventor	Jayesh R. Bhakta
Art Unit	2189
Examiner Name	Unknown
Attorney Docket Number	NETL.018P2C7

US PATENT DOCUMENTS

Examiner Initials *	Cite No. [1]	Document Number / Number-Kind Code [2] (if known)	Publication Date (MM-DD-YYYY)	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	1.	20060262586	11-23-2006	Solomon, et al	
	2.	20080162790	07-03-2008	Im, Jeon-Taek	
	3.	20090103387	04-23-2009	Shau, Jeng-Jye	

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Examiner Initials *	Cite No. [1]	Foreign Patent Document	Publication Date (MM-DD-YYYY)	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]
	4.	JPH10092169 A	9/9/97	Toshiba Corp.		
	5.	JP2000311485 A	10/13/00	Fujitsu Ltd.		

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
	6.	Office Action mailed April 2, 2014, for Japanese Patent Application No. 2012-520662 and English translation thereof, 7 pages	

EXAMINER /Gurtej Bansal/ (05/11/2014) **DATE CONSIDERED** 05/11/2014

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Sheet 1 of 3

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First Named Inventor	Jayesh R. Bhakta
Art Unit	2189
Examiner Name	Unknown
Attorney Docket Number	NETL.018P2C7

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	1	5345412	09-06-1994	Shiratsuchi	
	2	5537584	07-16-1996	Miyai et al.	
	3	5617559	04-01-1997	Le et al.	
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	19	7130308	10-31-2006	Haddock et al.	
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	21	7379361	05-27-2008	Co et al.	
	22	20050010737	01-01-2005	Ware et al.	
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Examiner Initials *	Cite No. [1]	Document Number Number-Kind Code [2] (if known)	Filing Date (MM-DD-YYYY)	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	24	95/001,758	09-14-2011	Owned by Netlist, Inc.	
	25	13/154,172	06-06-2011	Owned by Netlist, Inc.	
	26	13/287,042	11-01-2011	Owned by Netlist, Inc.	
	27	13/473,413	05-16-2012	Owned by Netlist, Inc.	
	28	13/032,470	02-22-2011	Owned by Netlist, Inc.	
	29	13/287,081	11-01-2011	Owned by Netlist, Inc.	
	30	13/971,231	08-20-2013	Owned by Netlist, Inc.	
	31	13/412,243	03-05-2012	Owned by Netlist, Inc.	
	32	13/183,253	07-14-2011	Owned by Netlist, Inc.	
	33	13/745,790	01-19-2013	Owned by Netlist, Inc.	

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Sheet 2 of 3

Complete if Known	
Application Number	13/971,231
Filing Date	August 20, 2013
First Named Inventor	Jayesh R. Bhakta
Art Unit	2189
Examiner Name	Unknown
Attorney Docket Number	NETL.018P2C7

US PATENT APPLICATIONS

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	34	14/229,844	3/29/2014	Owned by Netlist, Inc.	
	35	12/504,131	7/16/2009	Owned by Netlist, Inc.	
	36	12/761,179	4/15/2010	Owned by Netlist, Inc.	
	37	13/970,606	8/20/2013	Owned by Netlist, Inc.	
	38	13/288,850	11/3/2011	Owned by Netlist, Inc.	
	39	13/411,344	3/2/2012	Owned by Netlist, Inc.	

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	40	JP2009237492	9/9/97	Toshiba Corp.		
	41	JP2000285674	10/13/00	Fujitsu Ltd.		
	42	JP2002184176	6/28/02	NEC Tohoku Ltd.		
	43	JP2003007963	1/10/03	Hitachi, Ltd.		
	44	JP2008046989	2/28/08	Fujitsu Ltd.		

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
	45	Anonymous. (December 1996). "Applications Note: Understanding DRAM Operation," IBM, 10 pages.	
	46	Behrens, S. "HP Printer Memory Explained", The ZonkPage, Last Updated 01-21-2004. Accessed 02-10-2013, Retrieved from the Internet: URL <http://warshaft.com/hpmem.htm>. 7pp.	
	47	Non-Final Office Action, U.S. Pat. App. 13/412,243, January 2, 2014, 20 pages	
	48	Non-Final Office Action, U.S. Pat. App. 12/761,179, September 13, 2012, 20 pages	
	49	Non-final office action, U.S. Patent Application No. 13/288,850, October 14, 2013, 24 pages	
	50	Non-final office action, U.S. Patent Application No. 13/411,344, December 31, 2013, 28 pages	
	51	Non-final office action, U.S. Patent Application No. 13/473,413, November 17, 2011, 46 pages	
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First Named Inventor	Jayesh R. Bhakta
Art Unit	2189
Examiner Name	Unknown
Attorney Docket Number	NETL.018P2C7

Sheet	3	of	3

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	53	Response to non-final office action dated October 14, 2013 for U.S. Patent Application No. 13/288,850, filed January 14, 2014, 15 pages	
	54	Response to non-final office action dated 12/31/2013 for U.S. Patent Application No. 13/411,344, filed March 31, 2014, 12 pages	
	55	Patent Owner's Response to Office Action mailed November 13, 2012 for Reexamination Control Nos.95/000,578; 95/000,579, and 95/001,339, filed January 14, 2013, 96 pages.	
	56	Patent Owner's Response to Office Action mailed December 19, 2012 for Reexamination Control No. 95/001,758, filed March 19, 2013, 61 pages	
	57	Patent Owner's Response to Office Action mailed September 26, 2013 for Reexamination Control No. 95/001,758, filed November 26, 2013, 85 pages	
	58	Third Party Requester's Comments after Non-Final Action mailed September 26, 2013 for Reexamination Control No. 95/001,758, filed December 26, 2013,	
	59	Reexamination Control No. 95/002,399, filed April 25, 2013, and its entire file history	
	60	Patent Owner's Appeal Brief for Reexamination Control Nos. 95/000,546 and 95/000,577, filed October 2, 2013, 46 pages	
	61	Patent Trial and Appeal Board Decision on Appeal for Reexamination Control No.95/001/337, mailed January 16, 2014, 30 pages	
	62	Patent Trial and Appeal Board Decision on Appeal for Reexamination Control No.95/001/381, mailed January 16, 2014, 24 pages	
	63	Action Closing Prosecution mailed March 27, 2014 for Reexamination Control No. 95/001,758, filed September 14, 2011, 40 pages	
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	65	Notice of Allowance, U.S. Pat. App. 12/761,179, July 11, 2013, 37 pages	
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EXAMINER /Gurtej Bansal/ (05/11/2014) **DATE CONSIDERED** 05/11/2014

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First Named Inventor	Jayesh R. Bhakta
Art Unit	2189
Examiner Name	Unknown
Attorney Docket Number	NETL.018P2C7

US PATENT DOCUMENTS

Examiner Initials *	Cite No. [1]	Document Number / Number-Kind Code [2] (if known)	Publication Date (MM-DD-YYYY)	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	1	20080025137	01-31-2008	Natarajan et al.	
	2	2006233012	10-19-2006	Tomonori et al.	

FOREIGN PATENT DOCUMENTS

Examiner Initials *	Cite No. [1]	Foreign Patent Document	Publication Date (MM-DD-YYYY)	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]
	3	EP 1 816 570 A2	08-08-2007	Rambus, Inc.		

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
	4	International Search Report and Written Opinion, PCT/US2011/059209, January 31, 2013	

EXAMINER /Gurtej Bansal/ (05/11/2014) **DATE CONSIDERED** 05/11/2014

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PTO/SB/08a/b(07-09)
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Substitute for form 1449/PTO				Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(Use as many sheets as necessary)*				Application Number	13/971,231
				Filing Date	August 20, 2013
				First Named Inventor	Jayesh R. Bhakta
				Art Unit	2189
				Examiner Name	Unknown
Sheet	1	of	1	Attorney Docket Number	NETL.018P2C7

US PATENT DOCUMENTS					
Examiner Initials *	Cite No. [1]	Document Number Number-Kind Code [2] (if known)	Publication Date (MM-YYYY)	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	1	2003/0070052	04-2003	Lai, Jiin	
	2	2004/0098528	05-2004	Janzen, Jefferey W.	
	3	2002/0048195	04-2002	Klein, Dean A.	

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
	4	Non-Final Office Action, dated January 2, 2014, for U.S. Pat. App. No. 13/287,042 filed November 1, 2011, 42 pages	
	5	Response to Non-Final Office Action dated January 2, 2014 for U.S. Pat. App. No. 13/287,042, filed April 2, 2014, 12 pages	

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 1 of 1

Complete if Known	
Application Number	13/971,231
Filing Date	August 20, 2013
First Named Inventor	Jayesh R. Bhakta
Art Unit	2189
Examiner Name	Unknown
Attorney Docket Number	NETL.018P2C7

US PATENT DOCUMENTS

Examiner Initials *	Cite No. [1]	Document Number / Number-Kind Code [2 (if known)]	Publication Date (MM-DD-YYYY)	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	1	6717855	04-06-2004	Underwood	

FOREIGN PATENT DOCUMENTS

Examiner Initials *	Cite No. [1]	Foreign Patent Document	Publication Date (MM-DD-YYYY)	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]

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Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
	2	Action Closing Prosecution mailed October 1, 2012, for Control Nos. 95/000,546 and 95/000,577, filed May 11, '2010 and October 20, 2010 respectively, 39 pages.	
	3	Non-Final Office Action mailed November 13, 2012, for Control Nos. 95/001,339, 95/000,578 and 95/000,579, filed April 20, 2010, October 20, 2010 and October 21, 2010 respectively, 81 pages	
	4	Order Granting Request for Inter Partes Reexamination and Non-Final Office Action mailed December 7,2012, for Control No. 95/002,399, filed September 15, 2012, 89 pages.	
	5	Non-Final Office Action mailed December 19, 2012, for Control No. 95/001,758, filed September 14, 2011, 36 Pages.	
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EXAMINER /Gurtej Bansal/ (05/11/2014) **DATE CONSIDERED** 05/11/2014

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Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13971231	SOLOMON ET AL.
	Examiner	Art Unit
	GURTEJ BANSAL	2189

CPC- SEARCHED		
Symbol	Date	Examiner

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner
711	5; 147	05/15/2014	GB

SEARCH NOTES		
Search Notes	Date	Examiner
Text Search in EAST (See Attached)	05/15/2014	GB
NPL Search in Google Scholar (See Attached)	05/15/2014	GB
Inventor Search in eDAN	05/15/2014	GB
Consulted Alex Sofocleous (SPE)	05/15/2014	GB

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner

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CONFIRMATION NO. 2072

SERIAL NUMBER	FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
13/971,231	08/20/2013 RULE	711	2189	NETL.018P2C7

APPLICANTS

Netlist, Inc., Irvine, CA, Assignee (with 37 CFR 1.172 Interest);

INVENTORS

Jefferey C. Solomon, Irvine, CA;
Jayesh R. Bhakta, Cerritos, CA;

**** CONTINUING DATA ***************************

This application is a CON of 13/287,081 11/01/2011 PAT 8516188
which is a CON of 13/032,470 02/22/2011 PAT 8081536
which is a CON of 12/955,711 11/29/2010 PAT 7916574
which is a CON of 12/629,827 12/02/2009 PAT 7881150
which is a CON of 12/408,652 03/20/2009 PAT 7636274
which is a CON of 11/335,875 01/19/2006 PAT 7532537
which claims benefit of 60/645,087 01/19/2005
and is a CIP of 11/173,175 07/01/2005 PAT 7289386
which claims benefit of 60/588,244 07/15/2004
and is a CIP of 11/075,395 03/07/2005 PAT 7286436
which claims benefit of 60/550,668 03/05/2004
and claims benefit of 60/575,595 05/28/2004
and claims benefit of 60/590,038 07/21/2004

**** FOREIGN APPLICATIONS ***************************

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Foreign Priority claimed	35 USC 119(a-d) conditions met	Verified and Acknowledged	Met after Allowance	STATE OR COUNTRY	SHEETS DRAWINGS	TOTAL CLAIMS	INDEPENDENT CLAIMS
☐ Yes ☑ No	☐ Yes ☑ No	/GURTEJ BANSAL/ Examiner's Signature	☐ Initials	CA	23	10	2

ADDRESS

The Law Office of Jamie Zheng, Ph.D Esq.
P.O. Box 60573
Palo Alto, CA 94306
UNITED STATES

TITLE

LOAD-REDUCING CIRCUIT FOR MEMORY MODULE

FILING FEE RECEIVED	FEES: Authority has been given in Paper	
800	No._____ to charge/credit DEPOSIT ACCOUNT No._____ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____

BIB (Rev. 05/07).

A hands-on experience of the voice of customer analysis in maternity care from Iran
S Aghlmand, A Lameei, R Small - International journal of health ..., 2010 - emeraldinsight.com
... 5. **Ranking DQs**. ... This part **ranks** the target organisation and its competitor(s) based on how they meet each of the selected **DQs**. ... From the **rank** order, the twenty highest-ranked **DQs** were selected with approximately 70 per cent cumulative weight, to design a three-part ...
Cited by 9 Related articles All 6 versions Cite Save

Systematic review of the quality of patient information on the internet regarding inflammatory bowel disease treatments
M Langille, A Bernard, C Rodgers, S Hughes... - Clinical ..., 2010 - Elsevier
... Table 3. Top 6 Websites as Ranked by the **DQS** With the Corresponding GQS and Google **Rank** Positions. ... In general, there was a low to moderate relationship between the **ranking** within the Google search and **ranking** according to the **DQS** (r = 0.39, 0.64, and 0.35 for the first ...
Cited by 13 Related articles All 8 versions Cite Save

Chirality-induced forbidden reflections in X-ray resonant scattering [PDF] from msu.ru
VE Dmitrienko, EN Ovchinnikova - Acta Crystallographica Section A: ..., 2001 - scripts.iucr.org
... **rank** tensors might also appear for dipole-dipole transitions owing to thermal atomic motion or point defects (Dmitrienko et al., **1999** [Dmitrienko, VE, Ovchinnikova, EN & Ishida, K. (**1999**). ... In the Cartesian coordinates, the symmetric part of the third-**rank** tensor, f **dqs** jmn = f ...
Cited by 31 Related articles All 9 versions Cite Save

Memory module
JH Cho, JJ Lee, JJ Lee, B So - US Patent 7,072,201, 2006 - Google Patents
... The CA signals, **rank** control signals RCs, and the data signals **DQs** are buffered by the buffer 38 ... signals RC1, RC2, RC3 and RC4 are buffered signals supplied to each of the **ranks** RC1–RC4 ... signals CA2 a and CA2 b and also buffers the third and fourth **rank** control signals ...
Cited by 49 Related articles All 4 versions Cite Save

DDR DRAM data coherence scheme
DM Yuan, GB Wang - US Patent 6,453,381, 2002 - Google Patents
... burst address is odd 74, data from the register strobed with a positive **DQS** edge is connected to odd BLSA's and data from the register strobed with a negative **DQS** edge is ... Multi-**rank** memory module that emulates a memory module having a different number of **ranks**. ...
Cited by 26 Related articles All 2 versions Cite Save

On the quantification of robot redundancy
J Lenarcic - Robotics and Automation, **1999**. Proceedings, **1999** ..., **1999** - ieeexplore.ieee.org
... 0-7803-51 80-0-5199 $10.00 0 **1999** IEEE ... Let the joint increment corresponding to the secondary tasks be collected in vector **dqs** and let the secondary tasks be entirely ... in the null space of J,. The degree of redundancy D < 1 can mathematically be determined as D = **rank**(N,, 1 ...
Cited by 5 Related articles All 2 versions Cite Save

Circuit for providing chip-select signals to a plurality of **ranks** of a DDR memory module
JR Bhakta, JC Solomon - US Patent 8,081,537, 2011 - Google Patents
... 2A schematically illustrates an exemplary memory module which doubles the **rank** density in ... 3A schematically illustrates an exemplary memory module which doubles number of **ranks** in accordance ... the DQ data signal lines of two memory devices and their **DQS** data strobe ...
Cited by 1 Related articles All 3 versions Cite Save

[PPT] High performance cluster computing [PPT] from postech.ac.kr
R Buyya - New Jersey: Prentice, **1999** - dpnm.postech.ac.kr
... The Commodity Supercomputing! Cluster Computing - Research Projects. Beowulf (CalTech and NASA) - USA; CCS (Computing Centre Software) - Paderborn, Germany; Condor - Wisconsin State University, USA; **DQS** (Distributed Queuing System) - Florida State University, US ...
Cited by 965 Related articles All 4 versions Cite Save More

Circuit for providing chip-select signals to a plurality of **ranks** of a DDR memory module
JR Bhakta, JC Solomon - US Patent 8,081,535, 2011 - Google Patents
... 2A schematically illustrates an exemplary memory module which doubles the **rank** density in ... 3A schematically illustrates an exemplary memory module which doubles number of **ranks** in accordance ... the DQ data signal lines of two memory devices and their **DQS** data strobe ...
Cited by 1 Related articles All 5 versions Cite Save

System and method for dynamic **rank** specific timing adjustments for double data rate (DDR) components
DS McGinnis, DA Thompson, JF Zumkehr - US Patent 7,127,584, 2006 - Google Patents
... The timing measurements are then passed to a **DQS** Measurement Function, which calculates a DQS_OFFSET ... For example, memories are typically arranged in multiple **ranks** of components, which are usually ... time to be used with the data tenure for any given **rank** within the ...
Cited by 19 Related articles All 2 versions Cite Save

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1 2 3 4 5 6 7 8 9 10 Next

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EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	4529	711/5.ccls. 711/147.ccls.	US-PGPUB; USPAT	OR	OFF	2014/05/15 16:09
S1	4386	711/5.ccls. 711/147.ccls.	US-PGPUB; USPAT	OR	OFF	2013/12/02 23:37
S2	4481	DQS	US-PGPUB; USPAT	OR	OFF	2013/12/02 23:38
S3	88990	DS	US-PGPUB; USPAT	OR	OFF	2013/12/02 23:38
S4	32759	DQ	US-PGPUB; USPAT	OR	OFF	2013/12/02 23:38
S5	3171	S2 and S4	US-PGPUB; USPAT	OR	OFF	2013/12/02 23:38
S6	134822	rank	US-PGPUB; USPAT	OR	ON	2013/12/02 23:38
S7	329	S5 and S6	US-PGPUB; USPAT	OR	ON	2013/12/02 23:38
S8	201	US-4218740-$.DID. OR US-4368515-$.DID. OR US-4392212-$.DID. OR US-4633429-$.DID. OR US-4670748-$.DID. OR US-4706214-$.DID. OR US-4866603-$.DID. OR US-4958322-$.DID. OR US-4961172-$.DID. OR US-4961204-$.DID. OR US-4980850-$.DID. OR US-5247643-$.DID. OR US-5272664-$.DID. OR US-5345412-$.DID. OR US-5357478-$.DID. OR US-5388072-$.DID. OR US-5392252-$.DID. OR US-5426753-$.DID. OR US-5483497-$.DID. OR US-5485589-$.DID. OR US-5495435-$.DID. OR US-5513135-$.DID. OR US-5532954-$.DID. OR US-5541448-$.DID. OR US-5572691-$.DID. OR US-5581498-$.DID. OR US-5590071-$.DID. OR US-5602999-$.DID. OR US-5638534-$.DID. OR US-5655153-$.DID. OR US-5699542-$.DID. OR US-5702984-$.DID. OR US-5703826-$.DID. OR US-5745914-$.DID. OR US-5764590-$.DID. OR US-5784705-$.DID. OR US-5802395-$.DID. OR US-5805520-$.DID. OR US-5822251-$.DID. OR US-5909388-$.DID. OR US-5926827-$.DID. OR US-5926839-$.DID. OR US-5953215-$.DID. OR US-	US-PGPUB; USPAT; USOCR	OR	OFF	2013/12/03 00:02

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		OR US-7356639-$.DID. OR US-7370238-$.DID. OR US-7437591-$.DID. OR US-7461182-$.DID. OR US-7471538-$.DID. OR US-7532537-$.DID. OR US-7619912-$.DID. OR US-7636274-$.DID. OR US-7864627-$.DID. OR US-7881150-$.DID. OR US-7916574-$.DID. OR US-8001434-$.DID. OR US-20010003198-$.DID. OR US-20010050857-$.DID. OR US-20010052057-$.DID. OR US-20020088633-$.DID. OR US-20030063514-$.DID. OR US-20030090359-$.DID. OR US-20030090879-$.DID. OR US-20030191995-$.DID. OR US-20030210575-$.DID. OR US-20040000708-$.DID. OR US-20040037158-$.DID. OR US-20040201968-$.DID. OR US-20050036378-$.DID. OR US-20050154820-$.DID. OR US-20050281096-$.DID. OR US-20060044860-$.DID. OR US-20060117152-$.DID. OR US-20060126369-$.DID. OR US-20060129755-$.DID. OR US-20060179206-$.DID. OR US-20060259711-$.DID. OR US-20060262586-$.DID. OR US-20060267172-$.DID. OR US-20060277355-$.DID. OR US-20080162790-$.DID. OR US-20090103387-$.DID. OR US-20100070690-$.DID. OR US-20100091540-$.DID. OR US-20100128507-$.DID. OR US-20110016250-$.DID. OR US-20110016269-$.DID. OR US-20110090749-$.DID. OR US-20110125966-$.DID. OR WO-1992002879-$.DID. OR WO-1994007242-$.DID. OR WO-1995034030-$.DID. OR WO-1999000734-$.DID. OR WO-2002058069-$.DID. OR WO-2002063804-$.DID. OR WO-2003017283-$.DID. OR WO-2003069484-$.DID. OR WO-2006055497-$.DID. OR US-2003254-$.DID. OR US-1969279-$.DID. OR US-2097152-$.DID. OR US-4194204-$.DID.				
S9	1184	multiplex$3 with (DQS and DQ)	US-PGPUB; USPAT	OR	ON	2013/12/03 00:07
S10	359	multiplex$3 with (DQS and DQ) with delay$3	US-PGPUB; USPAT	OR	ON	2013/12/03 00:08
S11	850	multiplex$3 with DQS and delay with delay$3	US-PGPUB; USPAT	OR	ON	2013/12/03 00:12
S12	562	multiplex$3 with DQS and DQ with delay$3	US-PGPUB; USPAT	OR	ON	2013/12/03 00:12
S13	401	multiplex$3 with DQS same DQ with	US-	OR	ON	2013/12/03

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		delay$3	PGPUB; USPAT			00:12
S14	0	13/287042.app.	US-PGPUB; USPAT	OR	ON	2013/12/03 00:25
S15	0	13/287042.ap.	US-PGPUB; USPAT	OR	ON	2013/12/03 00:25
S16	0	"13287042".ap.	US-PGPUB; USPAT	OR	ON	2013/12/03 00:25
S17	0	"13287042".app.	US-PGPUB; USPAT	OR	ON	2013/12/03 00:25
S18	294	multiplex$3 with DQS same delay$3 with data with signals	US-PGPUB; USPAT	OR	ON	2013/12/03 00:28
S19	307	multiplex$3 with DQS same delay$3 with data with (signals lines)	US-PGPUB; USPAT	OR	ON	2013/12/03 00:28
S20	9	multiplex$3 with DQS same delay$3 with data with (signals lines) same2 rank	US-PGPUB; USPAT	OR	ON	2013/12/03 00:28
S21	26	multiplex$3 with DQS same delay$3 with data with (signals lines) and rank	US-PGPUB; USPAT	OR	ON	2013/12/03 00:29
S22	238	multiplex$3 with DQS same delay$3 with data with (signals lines) same memory	US-PGPUB; USPAT	OR	ON	2013/12/03 00:30
S23	347	isolat$3 with DQ with DQS	US-PGPUB; USPAT	OR	ON	2013/12/03 00:47
S24	21	isolat$3 with DQ with DQS same Rank	US-PGPUB; USPAT	OR	ON	2013/12/03 00:47
S25	1353	DQS with select$3 with (memory rank)	US-PGPUB; USPAT	OR	ON	2013/12/03 00:50
S26	54	chip$1select with rank and DQ and DQS	US-PGPUB; USPAT	OR	ON	2013/12/03 18:25
S27	56	chip$1select same rank and DQ and DQS	US-PGPUB; USPAT	OR	ON	2013/12/03 18:26
S28	61	chip$1select and rank and DQ and DQS	US-PGPUB; USPAT	OR	ON	2013/12/03 18:27
S29	5	rank with DQ with DQS with low	US-PGPUB; USPAT	OR	ON	2013/12/03 18:39
S30	300	rank with DQ with DQS	US-PGPUB; USPAT	OR	ON	2013/12/03 18:40
S31	82	rank and (DQ with DQS) with off	US-PGPUB; USPAT	OR	ON	2013/12/03 19:03
S32	271	rank and (DQ with DQS) with high	US-	OR	ON	2013/12/03

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			PGPUB; USPAT			19:07
S33	29	rank with (DQ with DQS) with high	US-PGPUB; USPAT	OR	ON	2013/12/03 19:07
S34	1	"6873533".pn.	US-PGPUB; USPAT	OR	ON	2013/12/03 19:07
S35	7	rank with (DQ with DQS) with terminat$3	US-PGPUB; USPAT	OR	ON	2013/12/03 19:10
S36	20	rank with (DQ with DQS) with isolat$3	US-PGPUB; USPAT	OR	ON	2013/12/03 19:11
S37	21	rank same (DQ with DQS) with isolat$3	US-PGPUB; USPAT	OR	ON	2013/12/03 19:11
S38	57	rank same (DQ with DQS) with high	US-PGPUB; USPAT	OR	ON	2013/12/03 19:11
S39	7	rank same (DQ with DQS) with (mux multiplexer)	US-PGPUB; USPAT	OR	ON	2013/12/03 19:15
S40	37	rank and (DQ with DQS) with (mux multiplexer)	US-PGPUB; USPAT	OR	ON	2013/12/03 19:16
S41	1040	(DQ with DQS) with (mux multiplexer)	US-PGPUB; USPAT	OR	ON	2013/12/03 19:21
S42	1024	(DQ with DQS) with (mux multiplexer) and memory	US-PGPUB; USPAT	OR	ON	2013/12/03 19:21
S43	634	(DQ with DQS) with (mux multiplexer) same memory	US-PGPUB; USPAT	OR	ON	2013/12/03 19:21
S44	231	(DQ with DQS) with (mux multiplexer) with memory	US-PGPUB; USPAT	OR	ON	2013/12/03 19:21
S45	1	"20040098428".pn.	US-PGPUB; USPAT	OR	ON	2013/12/03 19:40
S46	1	"20040098528".pn.	US-PGPUB; USPAT	OR	ON	2013/12/03 19:41
S47	1	"20030070052".pn.	US-PGPUB; USPAT	OR	ON	2013/12/03 19:42
S48	1	"20050047250".pn.	US-PGPUB; USPAT	OR	ON	2013/12/03 20:07
S49	1599	G06F12/0607.cpc. G06F12/0813.cpc.	US-PGPUB; USPAT	OR	OFF	2013/12/20 11:11
S50	2437	latency with memory adj controller with memory	US-PGPUB; USPAT	OR	ON	2014/04/04 14:15
S51	59	latency with memory adj controller with	US-	OR	ON	2014/04/04

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		(measur$3 test$3)	PGPUB; USPAT			14:16
S52	22	rank same (DQ with DQS) with isolat$3	US-PGPUB; USPAT	OR	ON	2014/04/04 15:16
S53	22	isolat$3 with DQ with DQS same Rank	US-PGPUB; USPAT	OR	ON	2014/04/04 15:29
S54	26	multiplex$3 with DQS same delay$3 with data with (signals lines) and rank	US-PGPUB; USPAT	OR	ON	2014/04/04 15:29
S55	1	"6553450".pn.	US-PGPUB; USPAT	OR	ON	2014/04/04 15:33
S56	1	"6742098".pn.	US-PGPUB; USPAT	OR	ON	2014/04/04 15:48
S60	644	isolat$3 with load with memory	US-PGPUB; USPAT	OR	ON	2014/04/04 15:58
S61	46	isolat$3 with load with memory with controller	US-PGPUB; USPAT	OR	ON	2014/04/04 15:58
S62	28	US-5345412-$.DID. OR US-5537584-$.DID. OR US-5617559-$.DID. OR US-5649159-$.DID. OR US-5717851-$.DID. OR US-5724604-$.DID. OR US-5729716-$.DID. OR US-5784705-$.DID. OR US-5802541-$.DID. OR US-5973392-$.DID. OR US-6173357-$.DID. OR US-6260127-$.DID. OR US-6446158-$.DID. OR US-6553449-$.DID. OR US-6618791-$.DID. OR US-6717855-$.DID. OR US-6788592-$.DID. OR US-6948084-$.DID. OR US-7130308-$.DID. OR US-7133960-$.DID. OR US-7379361-$.DID. OR US-20050010737-$.DID. OR US-20070293094-$.DID. OR US-3412243-$.DID. OR US-2201420-$.DID. OR US-2761179-$.DID. OR US-2201346-$.DID. OR US-2504131-$.DID.	US-PGPUB; USPAT	OR	ON	2014/05/05 00:39
S63	2355572	read$only with non$1volatile with main memory	US-PGPUB; USPAT	OR	OFF	2014/05/08 19:12
S64	2126	read$only with non$1volatile with main with memory	US-PGPUB; USPAT	OR	OFF	2014/05/08 19:12
S65	1	"20080080261".pn.	US-PGPUB; USPAT	OR	OFF	2014/05/11 20:14

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S57	3448	711/5.ccls. 711/147.ccls.	USPAT; UPAD	OR	OFF	2014/04/04 15:50
S58	171076	isolat$3.clm.	USPAT; UPAD	OR	OFF	2014/04/04 15:52

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S59	45	S57 and S58	USPAT; UPAD	OR	OFF	2014/04/04 15:52

5/ 15/ 2014 4:14:14 PM
C:\ Users\ gbansal\ Documents\ EAST\ Workspaces\ 13971231.wsp

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Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13971231	SOLOMON ET AL.
	Examiner	Art Unit
	GURTEJ BANSAL	2189

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	05/15/2014								
	1	✓								
	2	✓								
	3	✓								
	4	✓								
	5	✓								
	6	✓								
	7	✓								
	8	✓								
	9	✓								
	10	✓								

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PTO/SB/08a/b(07-09)
Approved for use through 7/31/2012. OMB 0651-0031
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet	1	of	1

Complete if Known	
Application Number	13/971,231
Filing Date	August 20, 2013
First Named Inventor	Jayesh R. Bhakta
Art Unit	2189
Examiner Name	Unknown
Attorney Docket Number	NETL.018P2C7

US PATENT DOCUMENTS

Examiner Initials *	Cite No. [1]	Document Number / Number-Kind Code [2] (if known)	Publication Date (MM-DD-YYYY)	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	1.	6011710	01-04-2000	Wiggers	
	2.	20010008006	07-12-2001	Klein	
	3.	20050257109	11-17-2005	Averbuj	
	4.	20070070669	03-29-2007	Tsern	

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
	5.	Petition for Inter Partes Review filed on 6/24/2014 for U.S. Patent No. 8,516,185, IPR Case Number IPR2014-01029, and all associated documents including cited references and expert declarations, available at https://ptabtrials.uspto.gov	
	6.	Petition for Inter Partes Review filed on 6/22/2014 for U.S. Patent No. 7,881,150, IPR Case Number IPR2014-00882 and IPR Case Number IPR2014-01011, and all associated documents including cited references and expert declarations, available at https://ptabtrials.uspto.gov	
	7.	Petition for Inter Partes Review filed on 6/24/2014 for U.S. Patent No. 8,081,536, IPR Case Number IPR2014-00883, and all associated documents including cited references and expert declarations, available at https://ptabtrials.uspto.gov	
	8.	Altera, ACEX iK, Programmable Logic Device Family, Data Sheet, May 2003, Ver 3.4	
	9.	Horowitz, "The Art of Electronics," Cambridge Univ. Press, 1989, selected pages	
	10.	Jacob, Bruce L.; "Synchronous DRAM Architectures, Organizations, and Alternative Technologies". University of Maryland, Dec. 10, 2002.	
	11.	JEDEC Standard No. 21-C Section 4.5.7, 168 Pin Registered SDRAM DIMM Family, Release 7	
	12.	JEDEC 21-C, Section 4.6.1, 278 Pin Buffered SDRAM DIMM Family	
	13.	JEDEC Standard No. 21-C Section 4.1.2.5, Appendix E, "Specific PD's for Synchronous DRAM (SDRAM)," pp. 1-25,	

EXAMINER **DATE CONSIDERED**

* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1] Applicant's unique citation designation number (optional). [2] See Kinds Codes of USPTO Patents Documents at www.uspto.gov or MPEP 901.04. [3] Enter Office that issued the document, by the two-letter code (WIPO Standard ST. 3). [4] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5] Kind of document by the appropriate symbols as indicated on the document and WIPO Standard ST. 16 if possible. [6] Applicant is to place a check mark here if English language Translation is attached.

Electronic Acknowledgement Receipt

EFS ID:	19804557
Application Number:	13971231
International Application Number:	
Confirmation Number:	2072
Title of Invention:	LOAD-REDUCING CIRCUIT FOR MEMORY MODULE
First Named Inventor/Applicant Name:	Jefferey C. Solomon
Customer Number:	79141
Filer:	Jamie Jie Zheng
Filer Authorized By:	
Attorney Docket Number:	NETL.018P2C7
Receipt Date:	07-AUG-2014
Filing Date:	20-AUG-2013
Time Stamp:	15:04:45
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Transmittal Letter	2014-08-07_IDS_Cover_NETL018P2C7.pdf	69133 7fd42a789c9c54bab3e3bfb790e98918312a2eba	no	2
Warnings:					
Information:					

2	Information Disclosure Statement (IDS) Form (SB08)	2014-08-07_IDS_NETL018P2C7.pdf	99609 5f620d727d73b8124f5aef3ffa2ed15213f53efe	no	1
Warnings:					
Information:					
This is not an USPTO supplied IDS fillable form					
3	Non Patent Literature	2003-05_Altera_ACEX_1K_Datasheet.pdf	23673114 d3153cf33657081c125ece8a06e13d43ffad67cd	no	86
Warnings:					
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Information:					
4	Non Patent Literature	1989_Horowitz_Art_of_Electronics.pdf	804824 4fe58ae9db8168f345983f24ffe9b752877cc2c4	no	15
Warnings:					
Information:					
5	Non Patent Literature	2002-12-10_Jacob_SDRAM_Architectures.pdf	5974132 f24bc23ec4f9e3bb8affeb17f74c9bc8fe428859	no	22
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6	Non Patent Literature	0000_JEDEC_21-C_4-5-7_168_Pin_RSDRAM.pdf	801227 346b9c985eafcea6da69a3ad7b3fca4d79e5f17b	no	8
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Information:					
7	Non Patent Literature	0000_JEDEC_21C_4-6-1-278_Pin.pdf	4025672 757e358ba523ebc1c7f068d3e3cf053495422252	no	24
Warnings:					
Information:					
8	Non Patent Literature	0000_JEDEC_21-C_4-1-2-5_Appendix_E.pdf	3114809 cff2ebcdb681dc41dd4ad0494d49109d2e25e34d	no	25
Warnings:					
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Information:					
		Total Files Size (in bytes):	38562520		

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New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

INFORMATION DISCLOSURE STATEMENT

Applicant	:	Netlist, Inc.
App. No.	:	13/971,231
Filed	:	August 20, 2013
For	:	LOAD-REDUCING CIRCUIT FOR MEMORY MODULE
Examiner	:	Unknown
Art Unit	:	2189
Conf No.	:	2072

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Enclosed for filing in the above-identified application is a Form PTO/SB/08a/b Equivalent listing 13 references. Copies of foreign documents and/or their translation and non-patent literature are submitted herewith.

The applicants would appreciate the Examiner initialing and returning the Form PTO/SB/08a/b Equivalent indicating that the information has been considered and made of record herein.

The information contained in this Information Disclosure Statement is not to be construed as a representation that: (i) a complete search has been made; (ii) additional information material to this application does not exist; (iii) the information, protocols, results and the like reported by third parties are accurate or enabling; or (iv) the above information constitutes prior art to the subject invention.

No item of information contained in this information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of

information contained in this information disclosure statement was known to any individual designated in 37 CFR § **1.56(c)** more than three months prior to the filing of this information disclosure statement. Therefore, no fee should be required. The Commissioner is authorized to charge the fee set forth in 37 C.F.R. § 1.17(p) to Deposit Account No. 50-5963.

Respectfully submitted,

Dated: August 7, 2014

/Jamie J. Zheng/ 51167

Jamie J. Zheng (Reg. No.)
Customer No. 79141
(650) 273-6008

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Ex. 1052, p. 209

Document code: WFEE

United States Patent and Trademark Office
Sales Receipt for Accounting Date: 08/11/2014

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Electronically filed **

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	:	Netlist, Inc.
App. No.	:	13/971,231
Filed	:	August 20, 2013
For	:	LOAD-REDUCING CIRCUIT FOR MEMORY MODULE
Examiner	:	BANSAL, GURTEJ
Art Unit	:	2189
Conf. No.	:	2072
Docket No.	:	NETL.018P2C7

CERTIFICATE OF EFS WEB TRANSMISSION

I hereby certify that this correspondence and any other attachment noted on the Automated Acknowledgement Receipt, is being transmitted from within the Pacific Time zone to the Commissioner for Patents via the EFS Web Server on:

November 20, 2014

(Date)

/Jamie J. Zheng/

Jamie J. Zheng, Reg. No. 51167

RESPONSE TO NON-FINAL OFFICE ACTION DATED MAY 20, 2014

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

The enclosed Amendment is in response to the Non-Final Office Action dated May 20, 2014 for the above-identified patent application.

The Commissioner is hereby authorized to charge any required fee(s) to Deposit Account No. 50-5963.

AMENDMENTS to the SPECIFICATION begin on Page 2 of this paper.

AMENDMENTS to the CLAIMS begin on Page 4 of this paper.

REMARKS begin on Page 11 of this paper.

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IN THE SPECIFICATION

Please replace the title with the following:

"MEMORY MODULE WITH LOAD REDUCING CIRCUIT AND METHOD OF OPERATION"

Please amend the Abstract as follows:

A ~~circuit is mountable on a~~ memory module ~~that~~ includes a plurality of memory devices and ~~that~~ is operable in a computer system to perform memory operations in response to memory commands from a memory controller of the computer system. The ~~circuit~~ memory module comprises a register device configured to receive a set of input control/address signals associated with a respective memory command (e.g., a read command or a write command) from the memory controller and to generate a set of output control/address signals in response to the set of input control/address signals. The set of output control/address signals are provided to the plurality of memory devices. The ~~circuit~~ memory module further comprises ~~logic~~ a circuit ~~to monitor the memory commands from the memory controller and~~ to selectively isolate one or more first memory devices among the plurality of memory devices from the memory controller in response to the respective memory command so as to reduce a load of the memory module to the computer system while one or more second memory devices among the plurality of memory devices are communicating with the memory controller in response to the set of output control/address signals.

Please amend paragraph [0011] under the Summary of the Invention as follows:

In certain embodiments, a ~~circuit is mountable on a~~ memory module ~~that~~ includes a plurality of memory devices and ~~that~~ is operable in a computer system to perform memory operations in response to memory commands from a memory controller of the computer system. The ~~circuit~~ memory module comprises a register device configured to receive a set of input control/address signals associated with a respective memory command (e.g., a read command or a write command) from the memory controller and to generate a set of output control/address signals in response to the set of input control/address signals. The set of

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output control/address signals are provided to the plurality of memory devices. The ~~circuit~~ memory module further comprises ~~logic~~ a circuit ~~to monitor the memory commands from the memory controller and~~ to selectively isolate one or more first memory devices among the plurality of memory devices from the memory controller in response to the respective memory command so as to reduce a load of the memory module to the computer system while one or more second memory devices among the plurality of memory devices are communicating with the memory controller in response to the set of output control/address signals.

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AMENDMENTS TO THE CLAIMS

1-10. (Cancelled)

11. A memory module operable in a computer system to perform memory operations in response to memory commands from a memory controller of the computer system, the memory module being coupled to the memory controller via a memory bus, the memory bus including a control/address (C/A) bus and a data bus, the data bus including a set of data (DQ) and data strobe (DQS) signal lines, comprising:

a plurality of memory devices including a first set of memory devices and a second set of memory devices;

a register device to receive from the memory controller a first set of input C/A signals associated with a first memory command via the C/A bus and subsequently a second set of input C/A signals associated with a second memory command via the C/A bus, the first memory command to make the memory module receive or output a first data burst and the second memory command to make the memory module receive or output a second data burst, the register to generate a first set of output C/A signals in response to the first set of input C/A signals and a second set of output C/A signals in response to the second set of input C/A signals, the first set of output C/A signals causing the first set of memory devices to receive or output the first data burst, the second set of output C/A signals causing the second set of memory devices to receive or output the second data burst; and

a circuit coupled between the data bus and the plurality of memory devices, the circuit being coupled to the first set of memory devices via a first set of module DQ and DQS signal lines and to the second set of memory devices via a second set of module DQ and DQS signal lines, wherein the circuit in response to the first memory command couples the first set of module DQ and DQS signal lines to respective DQ and DQS signal lines of the data bus and isolates the second set of module DQ and DQS signal lines from the data bus as the memory module is receiving or outputting the first data burst in response to the first memory command, and wherein the circuit in response to the second memory command couples the second set of module DQ and DQS signal lines to respective DQ and DQS signal lines of the data bus and isolates the first set of module DQ and DQS signal lines from the data bus as the

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memory module is receiving or outputting the second data burst in response to the second memory command.

12. The memory module of claim 11, wherein the circuit isolates both the first set of module DQ and DQS signal lines and the second set of module DQ and DQS signal lines from the data bus when the memory module is not being accessed by the memory system.

13. The memory module of claim 11, wherein the circuit further comprises multiple groups of DQ-DQS paths including a first group of DQ-DQS paths corresponding to the first set of module DQ and DQS signal lines and a second group of DQ-DQS paths corresponding to the second set of module DQ and DQS signal lines, wherein the circuit enables the first group of DQ-DQS paths as disabling the second group of DQ-DQS paths in response to the first memory command, and wherein the circuit enables the second group of DQ-DQS paths as disabling the first group of DQ-DQS paths in response to the second memory command.

14. The memory module of claim 13, wherein the register device is to translate between a system memory domain of the computer system and a physical memory device domain of the memory module, the system memory domain having a smaller number of ranks than the physical memory device domain, and wherein the first set of the plurality of memory devices and the second set of the plurality of memory devices belong to a same rank in the system memory domain and to different ranks in the physical memory device domain.

15. The memory module of claim 14, wherein the first set of input C/A signals include at least one chip-select signal and the register device outputs a greater number of chip-select signals than the at least one chip-select signal, the greater number of chip-select signals including a first chip select signal and a second chip select signal, the first chip-select signal being provided to the first set of memory devices and having an active value to select the first set of memory devices to receive or output the first data burst in response to the first memory command, the second chip-select signal being provided to the second set of memory devices and having a non-active value to keep the second set of memory devices from receiving or outputting data as the first set of memory devices are receiving or outputting the first data burst in response to the first memory command.

16. The memory module of claim 11, wherein the first memory command is a first read command and the second memory command is a second read command, wherein the first read command and the second read command are back to back adjacent read commands, and

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wherein the first set of memory devices output the first data burst together with a first burst of data strobes in response to the first read command, wherein the second set of memory devices output the second data burst together with a second burst of data strobes in response to the second read command, wherein the second data burst follows the first data burst on the data bus, and wherein the circuit prevents the first burst of data strobes and the second burst of data strobes from colliding with each other.

17. The memory module of claim 16, wherein each of the first burst of data strobes and the second burst of data strobes includes a pre-amble interval and a post-amble interval, and wherein the circuit combines the first burst of data strobes and the second burst of data strobes by skipping the post-amble interval of the first burst of data strobes and the pre-amble interval of the second burst of data strobes.

18. The memory module of claim 11, wherein the memory bus further includes an on-die termination (ODT) bus for conveying an ODT signal from the memory controller, each ODT signal corresponding to a respective memory command from the memory controller, wherein each memory device of the plurality of memory devices includes an ODT control input to allow a signal at the control input to enable or disable an ODT circuit in the memory device, and wherein the plurality of memory devices include at least one memory device having its respective control input configured to keep the ODT circuits in the at least one memory device disabled regardless of the ODT signal from the memory controller.

19. The memory module of claim 17, further comprising a termination assembly external to the plurality of memory devices and controlled in response to the ODT signal, wherein one or more DQ pins of the at least one memory device are coupled to the termination assembly so that one or more DQ signal paths between the at least one memory device and the memory controller can be terminated by the termination assembly.

20. The memory module of claim 11, wherein the circuit is to receive from the memory controller a third set of input C/A signals associated with a third memory command via the C/A bus, the third memory command being one of a refresh or precharge command, wherein the register to generate a third set of output C/A signals in response to the third set of input C/A signals, the third set of output C/A signals causing both the first set of memory devices and the second set of memory devices to perform one of a refresh operation and a pre-charge operation, and wherein the circuit in response to the third memory command couples the first

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set of module DQ and DQS signal lines to respective DQ and DQS signal lines of the data bus and couples the second set of module DQ and DQS signal lines to respective DQ and DQS signal lines of the data bus.

21. A method of operating a memory module in response to memory commands from a memory controller, the memory module having a plurality of memory devices including a first set of memory devices and a second set of memory devices, the memory module being coupled to the memory controller via a memory bus, the memory bus including a control/address (C/A) bus and a data bus, the data bus including a set of data (DQ) and data strobe (DQS) signal lines, the first set of memory devices having a first set of DQ and DQS pins, the second set of memory devices having a second set of DQ and DQS pins, the method comprising:

receiving from the memory controller a first set of input C/A signals associated with a first memory command via the C/A bus, the first memory command to cause the memory module to receive or output a first data burst;

generating a first set of output C/A signals in response to the first set of input C/A signals, the first set of output C/A signals causing the first set of memory devices to receive or output the first data burst,;

receiving from the memory controller a second set of input control/address signals associated with a second memory command via the C/A bus, the second memory command to cause the memory module to receive or output a second data burst

generating a second set of output C/A signals in response to the second set of input C/A signals, the second set of output C/A signals causing the second set of memory devices to receive or output the second data burst;

in response to the first memory command, coupling the first set DQ and DQS pins to respective DQ and DQS signal lines of the data bus and isolating the second set of module DQ and DQS pins from the data bus as the memory module is receiving or outputting the first data burst in response to the first memory command; and

in response to the second memory command, coupling the second set DQ and DQS pins to respective DQ and DQS signal lines of the data bus and isolating the first set of DQ and DQS pins from the data bus as the memory module is receiving or outputting the second data burst in response to the second memory command.

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22. The method of claim 21, further comprising isolating both the first set of DQ and DQS pins and the second set of DQ and DQS pins from the data bus when the memory module is not being accessed by the memory system.

23. The method of claim 21, wherein the memory module further comprises multiple groups of DQ-DQS paths including a first group of DQ-DQS paths corresponding to the first set of DQ and DQS pins and a second group of DQ-DQS paths corresponding to the second set of DQ and DQS pins, the method further comprising enabling the first group of DQ-DQS paths as disabling the second group of DQ-DQS paths in response to the first memory command, and enabling the second group of DQ-DQS paths as disabling the first group of DQ-DQS paths in response to the second memory command.

24. The method of claim 23, further comprising translating between a system memory domain and a physical memory device domain, the system memory domain having a smaller number of ranks than the physical memory device domain, and wherein the first set of the plurality of memory devices and the second set of the plurality of memory devices belong to a same rank in the system memory domain and to different ranks in the physical memory device domain.

25. The method of claim 24, wherein the first set of input C/A signals include at least one chip-select signal and the register device outputs a greater number of chip-select signals than the at least one chip-select signal, the greater number of chip-select signals including a first chip select signal and a second chip select signal, the first chip-select signal being provided to the first set of memory devices and having an active value to select the first set of memory devices to receive or output the first data burst in response to the first memory command, the second chip-select signal being provided to the second set of memory devices and having a non-active value to keep the second set of memory devices from receiving or outputting data as the first set of memory devices are receiving or outputting the first data burst in response to the first memory command.

26. The method of claim 21, wherein the first memory command is a first read command and the second memory command is a second read command, wherein the first read command and the second read command are back to back adjacent read commands, and wherein the first set of memory devices output the first data burst together with a first burst of data strobes in response to the first read command, wherein the second set of memory devices

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output the second data burst together with a second burst of data strobes in response to the second read command, wherein the second data burst follows the first data burst on the data bus, the method further comprising combining the first burst of data strobes and the second burst of data strobes to form a third burst of data strobes on the data bus.

27. The method of claim 26, wherein each of the first burst of data strobes and the second burst of data strobes includes a pre-amble interval and a post-amble interval, and wherein combining the first burst of data strobes and the second burst of data strobes comprises skipping the post-amble interval of the first burst of data strobes and the pre-amble interval of the second burst of data strobes.

28. The method of claim 21, wherein the memory bus further includes an on-die termination (ODT) bus for conveying an ODT signal corresponding to each memory command from the memory controller, wherein each of the plurality of memory devices includes ODT circuits and an ODT control input to allow a signal at the control input to enable or disable the ODT circuits in the memory device, the method further comprising keeping the ODT circuits in at least one of the plurality of memory devices disabled regardless of the ODT signal from the memory controller.

29. The method of claim 27, further comprising controlling a termination assembly external to the plurality of memory devices according to the ODT signal, wherein one or more DQ pins of the at least one memory device are coupled to the termination assembly so that one or more DQ signal paths between the at least one memory device and the memory controller can be terminated by the termination assembly.

30. The method of claim 21, further comprising:

receiving from the memory controller a third set of input C/A signals associated with a third memory command via the C/A bus, the third memory command being one of a refresh or precharge command;

generating a third set of output C/A signals in response to the third set of input C/A signals, the third set of output C/A signals causing both the first set of memory devices and the second set of memory devices to perform one of a refresh operation and a pre-charge operation; and

in response to the third memory command, coupling the first set of module DQ and DQS signal lines to respective DQ and DQS signal lines of the data bus and coupling the

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second set of module DQ and DQS signal lines to respective DQ and DQS signal lines of the data bus.

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REMARKS

This amendment responds to the Non-Final Office Action mailed May 20, 2014. In the Office Action, the Examiner:

- provisionally rejected claims 1-10 on the ground of nonstatutory double patenting as being unpatentable over claims 1, 6 and 8 of co-pending Application No. 13/287,042; and
- rejected claims 1-10 under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Lai (US 2003/0070052), in view of Janzen (US 2004/0098528);

I. AMENDMENTS TO THE SPECIFICATION

The title has been changed, and the Abstract and the Summary of the Invention have been amended. No new matter is added.

II. AMENDMENTS TO THE CLAIMS

Claims 1-20 are cancelled, and new claims 11-30 are presented. No new matter is added.

III. REJECTION OF CLAIMS 1-10 ON THE GROUND OF NONSTATUTORY DOUBLE PATENTING

Claims 1-10 are rejected on the ground of nonstatutory double patenting as being unpatentable over claims 1, 6 and 8 of co-pending Application No. 13/287,042, now U.S. Patent No. 8,756,364.

Claims 1-10 are cancelled. Applicant files herewith a terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) to overcome any nonstatutory double patenting rejection the Examiner may raise with regard to the new claims 11-30.

IV. REJECTION OF CLAIMS 1-10 UNDER PRE-AIA 35 U.S.C. 103(A) AS BEING UNPATENTABLE OVER LAI, IN VIEW OF JANZEN

New claims 11-30 are presented to replace original claims 1-10, which are cancelled. New claim 11 recites a memory module comprising a plurality of memory devices including a first set of memory devices and a second set of memory devices and a register device to

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receive from the memory controller a first set of input C/A signals associated with a first memory command via the C/A bus and subsequently a second set of input control/address signals associated with a second memory command via the C/A bus, the first memory command to cause the memory module to receive or output a first data burst and the second memory command to cause the memory module to receive or output a second data burst.

New claim 11 then requires the register to generate a first set of output C/A signals in response to the first set of input C/A signals and a second set of output C/A signals in response to the second set of input C/A signals, the first set of output C/A signals causing the first set of memory devices to receive or output the first data burst, the second set of output C/A signals causing the second set of memory devices to receive or output the second data burst.

New claim 11 further requires a circuit coupled between the data bus and the plurality of memory devices. The circuit is coupled to the first set of memory devices via a first set of module DQ and DQS signal lines and to the second set of memory devices via a second set of module DQ and DQS signal lines. New claim 11 further requires the circuit to respond to the first memory command by coupling the first set of module DQ and DQS signal lines to respective DQ and DQS signal lines of the data bus and by isolating the second set of module DQ and DQS signal lines from the data bus as the memory module is receiving or outputting the first data burst in response to the first memory command (*emphasis added*). New claim 11 then requires the circuit to respond to the second memory command by coupling the second set of module DQ and DQS signal lines to respective DQ and DQS signal lines of the data bus and by isolating the first set of module DQ and DQS signal lines from the data bus as the memory module is receiving or outputting the second data burst in response to the second memory command (*emphasis added*).

The above features of new claim 11 are not disclosed or taught by Lai in view of Janzen. In Lai, the buffer chip 108 or FET switch circuit 118 does not isolate either one of the two memory banks 104 and 106 from the data bus in response to a memory command. Instead, the buffer chip 108 comprises "a plurality of first-in first-out (FIFO) buffers" to "double the data rate for reading and writing" of each of the two memory banks 104 and 106, which are of DDR SDRAM structure (Lai, paragraph [0035]). Similarly, the FET switches 118 is "to double the transmission rate of the first data selection signal (DQSA) and the data

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selection (*sic*) signal (MDA) of the first memory bank 114" and the second memory bank 116 (Lai, paragraph [0039]).

Nowhere in Lai it is mentioned that the buffer chip 108 or FET switch circuit 118 chooses which of the two memory banks 104 and 106 to connect to the memory bus, or which of the two memory banks 104 and 106 to isolate from the memory bus, based on a memory command. Instead, the buffer chip may lock data of the memory data signal MD and transmit the respective data units in the data signal MD to the two memory banks 104, 106 respectively according to data selection signal (DQS) and the data mask signal (DQM)" (Lai, FIG. 5; paragraph [0038]). Neither of the data selection signal (DQS) and the data mask signal (DQM) constitutes a memory command, which, according to the Specification of the instant application and to the common understanding of DDR memory operations, involves a number of command signals that define memory operations such as read, write, refresh, precharge, and other operations (Specification, Table 1 and Table 2).

Lai also does not isolate either one of the two memory banks 104 and 106 as the memory module is receiving or outputting a data burst in response a memory command. In fact, to make the memory module of Lai receive or output data units at quad data rate, Lai requires both memory banks be activated by the chip select signal (0,1) at the same time (Lai, FIGS. 4, 5, 7, and 8, showing chip select signal (0,1) being pulled low). Thus, for each memory command, Lai requires both of the two memory banks 104 and 106 to receive or output units of data, because otherwise the memory module in Lai with the double data rate memory banks 104, 106 would not be able to receive or output a quad data rate data signal (MD).

Thus, during a read operation, the buffer chip 108 or FET switch circuit 118 interleaves units of data from the two memory banks 104, 106 and outputs the read data MD onto the data bus at twice the frequency as each of the two memory banks 104 and 106 outputs read data MDA and MDB, respectively (Lai, FIGS. 4 and 7; paragraphs [0037] and [0039]). As stated in Lai, the "signals between the memory controller 102 and buffer chip 108 operate and *(sic)* four times faster than a baseline rate." "Therefore, four units of data are capable of being transmitted within one memory clock cycle" (Lai, paragraph [0036]). Note that the memory banks 104, 106 are of the DDR SDRAM structure (paragraph [0035]), so each of the memory banks 104, 106 can only transmit two units of data per memory clock cycle. Therefore, for each read command, both of the two memory banks 104, 106 need to

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feed data units to the buffer chip 108 or FET switch circuit 118. Thus, unlike what is claimed in new claim 11, neither of the memory banks 104, 106 can be isolated from the memory bus as the memory module of Lai is outputting read data MD onto the data bus.

During a write operation, the buffer chip may lock data of the memory data signal MD and transmit the respective data units in the data signal MD to the two memory banks 104, 106 respectively according to data selection signal (DQS) and the data mask signal (DQM" (Lai, FIG. 5; paragraph [0038]). As discussed above, the memory data signal has four units of data per memory cycle while each of the memory banks 104, 106 can only receive two units of data per memory cycle. Thus, if only one of the memory banks 104, 106 is receiving the memory data signal MD, half of the data units in the memory data signal would be lost. Therefore, unlike what is claimed in claim 11, neither of the memory banks 104, 106 can be isolated from the memory bus as the memory module in Lai is receiving the memory data signal MD.

Since Janzen does not make up for the above deficiencies of Lai, new claim 11 is patentable over Lai in view of Janzen.

New claims 12-20 depend from new claim 11 and include further limitations in addition to the limitations in new claim 11. Therefore, new claims 12-20 are patentable for at least the same reasons new claim 11 is patentable.

The above arguments with regard to new claim 11 apply to new claim 21. Therefore, new claim 21 is also patentable.

New claims 22-30 depend from new claim 21 and include further limitations in addition to the limitations in new claim 21. Therefore, new claims 22-30 are patentable for at least the same reasons new claim 21 is patentable.

By responding in the foregoing remarks only to particular positions asserted by the Examiner, the Applicants do not necessarily acquiesce in other positions that have not been explicitly addressed. In addition, the Applicants' arguments for the patentability of a claim should not be understood as implying that no other reasons for the patentability of that claim exist.

In light of the above amendments and remarks, the Applicants respectfully request that the Examiner reconsider this application with a view towards allowance. The Examiner

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is invited to call the undersigned attorney at (650) 273-6008, if a telephone call could help resolve any remaining items.

Respectfully submitted,

Date: November 20, 2014

/Jamie J. Zheng/ 51167

Jamie J. Zheng (Reg. No.)

Customer Number 79141

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Electronic Patent Application Fee Transmittal

Application Number:	13971231
Filing Date:	20-Aug-2013
Title of Invention:	LOAD-REDUCING CIRCUIT FOR MEMORY MODULE
First Named Inventor/Applicant Name:	Jefferey C. Solomon
Filer:	Jamie Jie Zheng
Attorney Docket Number:	NETL.018P2C7

Filed as Small Entity

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Extension - 3 months with $0 paid	2253	1	700	700

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
Statutory or Terminal Disclaimer	1814	1	160	160
		Total in USD ($)		**860**

Electronic Acknowledgement Receipt

EFS ID:	20760901
Application Number:	13971231
International Application Number:	
Confirmation Number:	2072
Title of Invention:	LOAD-REDUCING CIRCUIT FOR MEMORY MODULE
First Named Inventor/Applicant Name:	Jefferey C. Solomon
Customer Number:	79141
Filer:	Jamie Jie Zheng
Filer Authorized By:	
Attorney Docket Number:	NETL.018P2C7
Receipt Date:	20-NOV-2014
Filing Date:	20-AUG-2013
Time Stamp:	22:37:54
Application Type:	Utility under 35 USC 111(a)

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1	Power of Attorney	2014-11-20_AIA82A_transmittal_POA_NETL018P2C7.pdf	195878 9810e347cb8c574bb978a1df7199b060a06c8688	no	3
Warnings:					
Information:					
2	Power of Attorney	AIA_General_POA_Netlist.pdf	133545 f8258889ee9edc63b1cc17705b3158faaed49e9e	no	1
Warnings:					
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3	Terminal Disclaimer Filed	11-20-2014_Terminal_Disclaimer_NETL018P2C7.pdf	159887 e42c26b67482b7efc5d165a8de3bc715302560da	no	2
Warnings:					
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4		2014-11-20_Rsps_NFOA_NETL018P2C7.pdf	152528 22b8b5afe9f405ac53df7376b0421feff39da133	yes	15

Multipart Description/PDF files in .zip description

Document Description	Start	End
Amendment/Req. Reconsideration-After Non-Final Reject	1	1
Specification	2	3
Claims	4	10
Applicant Arguments/Remarks Made in an Amendment	11	15

Warnings:					
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5	Fee Worksheet (SB06)	fee-info.pdf	32358 1331c26e6f22b02efbfd7e0ebf1f4da40bd4ade4	no	2
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TERMINAL DISCLAIMER TO OBVIATE A DOUBLE PATENTING REJECTION OVER A "PRIOR" PATENT	Docket Number (Optional) NETL.018P2C7

In re Application of: Netlist, Inc.

Application No.: 13/971,231

Filed: August 20, 2013

For: LOAD-REDUCING CIRCUIT FOR MEMORY MODULE

The applicant, Netlist, Inc., owner of 100 percent interest in the instant application hereby disclaims, except as provided below, the terminal part of the statutory term of any patent granted on the instant application which would extend beyond the expiration date of the full statutory term of **prior patent** No. 8,756,364 as the term of said **prior patent** is presently shortened by any terminal disclaimer. The applicant hereby agrees that any patent so granted on the instant application shall be enforceable only for and during such period that it and the **prior patent** are commonly owned. This agreement runs with any patent granted on the instant application and is binding upon the grantee, its successors or assigns.

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is found invalid by a court of competent jurisdiction;
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has all claims canceled by a reexamination certificate;
is reissued; or
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I hereby acknowledge that any willful false statements made are punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

2. ☑ The undersigned is an attorney or agent of record. Reg. No. 51167

/Jamie J. Zheng/ — Signature
November 20, 2014 — Date

Jamie J. Zheng — Typed or printed name

Title
650-273-6008 — Telephone Number

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Application Number	13/971,231
Filing Date	8/20/2013
First Named Inventor	Jefferey C. Solomon
Title	LOAD-REDUCING CIRCUIT FOR MEMORY MODULE
Art Unit	2072
Examiner Name	BANSAL, GURTEJ
Attorney Docket Number	NETL.018P2C7

SIGNATURE of Applicant or Patent Practitioner

Signature	/Jamie J. Zheng/	Date	NOVEMBER 11, 2014
Name	Jamie J. Zheng	Telephone	650-273-6008
Registration Number	51,167		

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4(d) for signature requirements and certifications.

☐ *Total of _____ forms are submitted.

This collection of information is required by 37 CFR 1.31, 1.32 and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Doc Code: PA..

Document Description: Power of Attorney

PTO/AIA/82B(07-12)
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POWER OF ATTORNEY BY APPLICANT

I hereby revoke all previous powers of attorney given in the application identified in the attached transmittal letter.

☐ I hereby appoint Practitioner(s) associated with the following Customer Number as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the application referenced in the attached transmittal letter (form PTO/AIA/82A or equivalent):

OR

☐ I hereby appoint Practitioner(s) named below as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the application referenced in the attached transmittal letter (form PTO/AIA/82A or equivalent):

Name	Registration Number	Name	Registration Number

Please recognize or change the correspondence address for the application identified in the attached transmittal letter to:

☐ The address associated with the above-mentioned Customer Number.

OR

☐ The address associated with Customer Number:

OR

☐ Firm or Individual Name					
Address					
City		State		Zip	
Country					
Telephone		Email			

I am the Applicant:

☐ Inventor or Joint Inventor

☐ Legal Representative of a Deceased or Legally Incapacitated Inventor

☐ Assignee or Person to Whom the Inventor is Under an Obligation to Assign

☐ Person Who Otherwise Shows Sufficient Proprietary Interest (*e.g.,* a petition under 37 CFR 1.46(b)(2) was granted in the application or is concurrently being filed with this document)

SIGNATURE of Applicant for Patent

Signature		Date	
Name		Telephone	
Title and Company			

NOTE: Signature - This form must be signed by the applicant in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications. Submit multiple forms for more than one signature, see below *.

☐ *Total of _____ forms are submitted.

This collection of information is required by 37 CFR 1.31, 1.32 and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

GENERAL POWER OF ATTORNEY BY APPLICANT FOR UNITED STATES PATENT

I hereby revoke all previous powers of attorney given in the application referenced in the attached transmittal letter (form PTO/AIA/82A or equivalent).

I hereby appoint the practitioner associated with the following Customer Number :

79141

as my/our attorney or agent, and to transact all business in the United States Patent and Trademark Office in connection with the application referenced in the attached transmittal letter (form PTO/AIA/82A or equivalent).

Please recognize or change the **correspondence address** for the application referenced in the attached transmittal letter to the address associated with the above-mentioned **Customer Number.**

I am the Applicant:

☐ Inventor or Joint Inventor

☐ Legal Representative of a Deceased or Legally Incapacitated Inventor

■ Assignee or Person to Whom the Inventor is Under an Obligation to Assign

☐ Person Who Otherwise Shows Sufficient Proprietary Interest (e.g., a petition under 37 CFR 1.46(b)(2) was granted in the application or is currently being filed in this document)

SIGNATURE of Applicant for Patent

Signature		Date: January 9, 2013
Name	**Gail Sasaki**	
Title	Vice President and Chief Financial Officer	
Company	Netlist, Inc.	

Note: Signature - this form must be signed by the Applicant or a person authorized to act on behalf of Applicant.

Submit multiple forms for more than one signature
Total of __ forms are submitted.

PTO/SB/06 (09-11)
Approved for use through 1/31/2014. OMB 0651-0032
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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 13/971,231	Filing Date 08/20/2013	☐ To be Mailed

ENTITY: ☐ LARGE ☒ SMALL ☐ MICRO

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT **11/20/2014**

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	* 20	Minus	** 20	= 0	X $40 =	0
Independent (37 CFR 1.16(h))	* 2	Minus	***3	= 0	X $210 =	0
☐ Application Size Fee (37 CFR 1.16(s))						
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
					TOTAL ADD'L FEE	0

AMENDMENT

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =	
☐ Application Size Fee (37 CFR 1.16(s))						
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
					TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

LIE
/LINDA A. WASHINGTON/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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Substitute for form 1449/PTO				**Complete if Known**	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(Use as many sheets as necessary)*				Application Number	13/971,231
				Filing Date	August 20, 2013
				First Named Inventor	Jayesh R. Bhakta
				Art Unit	2189
				Examiner Name	BANSAL, GURTEJ
Sheet	1	of	1	Attorney Docket Number	NETL.018P2C7

US PATENT DOCUMENTS

Examiner Initials *	Cite No. [1]	Document Number / Number-Kind Code [2] (if known)	Publication Date (MM-DD-YYYY)	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	1.	6747887	06-08-2004	Halbert et al.	
	2.	7093066	08-15-2006	Klein	
	3.	6832303	12/14/2004	Tanaka	

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
	4.	Inter Partes Review Case No. IPR2014-00882, Corrected Petition for Inter Partes Review of U.S. Patent No. 7,881,150, filed on July 8, 2014.	
	5.	Inter Partes Review Case No. IPR2014-00882, Exhibit 1007 to Petition for Inter Partes Review, "Declaration of Dr. Srinivasan Jagannathan," filed on June 22, 2014.	
	6.	Inter Partes Review Case No. IPR2014-00883, Corrected Petition for Inter Partes Review of U.S. Patent No. 8,081,536, filed on July 8, 2014.	
	7.	Inter Partes Review Case No. IPR2014-00883, Exhibit 1011 to Petition for Inter Partes Review, "Declaration of Dr. Srinivasan Jagannathan," filed on June 21, 2014.	
	8.	Inter Partes Review Case No. IPR2014-01011, Corrected Petition for Inter Partes Review of U.S. Patent No. 7,881,150, filed on July 8, 2014.	
	9.	Inter Partes Review Case No. IPR2014-01011, Exhibit 1007 to Petition for Inter Partes Review, "Declaration of Dr. Srinivasan Jagannathan." filed on June 22, 2014.	
	10.	McCluskey, Edward J., *Logic Design Principles with Emphasis on Testable Semicustom Circuits*, Prentice Hall, 1986, pp. 104-107 and 119-120.	
	11.	MICRON, DDR SDRAM DIMM Module: MT16VDDT3264A – 256 MB; MT16VDDT6464A – 512 MB, Data Sheet, 2002, Micron Technology, Inc.	
	12.	U.S. District Court Northern District of California, Case No. 4:13-CV-05889-YGR, *Netlist, Inc. v. Smart Storage Systems, Inc., and Diablo Technologies, Inc.*, Smart Storage Systems, Inc.'s Invalidity Contentions, dated June 6, 2014	
	13.	U.S. District Court Northern District of California, Case No. 4:13-CV-05889-YGR, *Netlist, Inc. v. Smart Storage Systems, Inc., and Diablo Technologies, Inc.*, Exhibits F.1-F.5 to "Smart Storage Systems, Inc.'s Invalidity Contentions," dated June 6, 2014.	
	14.	U.S. District Court Northern District of California, Case No. 4:13-CV-05889-YGR, *Netlist, Inc. v. Smart Storage Systems, Inc., and Diablo Technologies, Inc.*, Exhibits G.1-G.6 to "Smart Storage Systems, Inc.'s Invalidity Contentions," dated June 6, 2014.	
	15.	U.S. District Court Northern District of California, Case No. 4:13-CV-05889-YGR, *Netlist, Inc. v. Smart Storage Systems, Inc., and Diablo Technologies, Inc.*, Exhibit H to "Smart Storage Systems, Inc.'s Invalidity Contentions," dated June 6, 2014.	

EXAMINER **DATE CONSIDERED**

* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1] Applicant's unique citation designation number (optional). [2] See Kinds Codes of USPTO Patents Documents at www.uspto.gov or MPEP 901.04. [3] Enter Office that issued the document, by the two-letter code (WIPO Standard ST. 3). [4] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5] Kind of document by the appropriate symbols as indicated on the document and WIPO Standard ST. 16 if possible. [6] Applicant is to place a check mark here if English language Translation is attached.

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Substitute for form 1449/PTO				Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(Use as many sheets as necessary)*				Application Number	13/971,231
				Filing Date	August 20, 2013
				First Named Inventor	Jayesh R. Bhakta
				Art Unit	2189
				Examiner Name	BANSAL, GURTEJ
Sheet	2	of	1	Attorney Docket Number	NETL.018P2C7

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
	16.	U.S. District Court Northern District of California, Case No. 4:13-CV-05889-YGR, *Netlist, Inc. v. Smart Storage Systems, Inc., and Diablo Technologies, Inc.,* Diablo Technologies, Inc.'s Invalidity Contentions, dated June 6, 2014.	
	17.	U.S. District Court Northern District of California, Case No. 4:13-CV-05889-YGR, *Netlist, Inc. v. Smart Storage Systems, Inc., and Diablo Technologies, Inc.,* Exhibits F-1 to F-5 to "Diablo Technologies, Inc.'s Invalidity Contentions," dated June 6, 2014.	
	18.	U.S. District Court Northern District of California, Case No. 4:13-CV-05889-YGR, *Netlist, Inc. v. Smart Storage Systems, Inc., and Diablo Technologies, Inc.,* Exhibits G-1 to G-6 to "Diablo Technologies, Inc.'s Invalidity Contentions," dated June 6, 2014.	
	19.	U.S. District Court Northern District of California, Case No. 4:13-CV-05889-YGR, *Netlist, Inc. v. Smart Storage Systems, Inc., and Diablo Technologies, Inc.,* Exhibit H to "Diablo Technologies, Inc.'s Invalidity Contentions," dated June 6, 2014.	

EXAMINER **DATE CONSIDERED**

* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1] Applicant's unique citation designation number (optional). [2] See Kinds Codes of USPTO Patents Documents at www.uspto.gov or MPEP 901.04. [3] Enter Office that issued the document, by the two-letter code (WIPO Standard ST. 3). [4] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5] Kind of document by the appropriate symbols as indicated on the document and WIPO Standard ST. 16 if possible. [6] Applicant is to place a check mark here if English language Translation is attached.

Electronic Patent Application Fee Transmittal

Application Number:	13971231
Filing Date:	20-Aug-2013
Title of Invention:	LOAD-REDUCING CIRCUIT FOR MEMORY MODULE
First Named Inventor/Applicant Name:	Jefferey C. Solomon
Filer:	Jamie Jie Zheng
Attorney Docket Number:	NETL.018P2C7

Filed as Small Entity

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
Submission- Information Disclosure Stmt	2806	1	90	90
		Total in USD ($)		**90**

Electronic Acknowledgement Receipt

EFS ID:	20816951
Application Number:	13971231
International Application Number:	
Confirmation Number:	2072
Title of Invention:	LOAD-REDUCING CIRCUIT FOR MEMORY MODULE
First Named Inventor/Applicant Name:	Jefferey C. Solomon
Customer Number:	79141
Filer:	Jamie Jie Zheng
Filer Authorized By:	
Attorney Docket Number:	NETL.018P2C7
Receipt Date:	27-NOV-2014
Filing Date:	20-AUG-2013
Time Stamp:	01:47:09
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	$90
RAM confirmation Number	8168
Deposit Account	
Authorized User	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)

1	Transmittal Letter	2014-11-26_IDS_Cover_NETL018P2C7.pdf	54357 901eec77f9e61a9b47a11bd1763390dd3502daf5	no	2
Warnings:					
Information:					
2	Information Disclosure Statement (IDS) Form (SB08)	2014-11-26_IDS_NETL018P2C7.pdf	124611 7ff94f702e4e8209808f97d89a0e651bf2510c0d	no	2
Warnings:					
Information:					
This is not an USPTO supplied IDS fillable form					
3	Non Patent Literature	20140708_Corrected_Petition_for_Inter_Partes_Review_IPR2014400882.pdf	5916394 ca7955bd18406ea9f2e6a8ef2a1589895a9b43a4	no	67
Warnings:					
Information:					
4	Non Patent Literature	Exhibit_1007_Declaration_IPR201400882.pdf	23268956 d5246ffbde107498b9ef92db0dcff1b8260eb27a	no	392
Warnings:					
Information:					
5	Non Patent Literature	20140708_Corrected_Petition_for_Inter_Partes_Review_IPR2014400883.pdf	6432014 d0e71763e1fea5859087c84c1ee77fcc75618896	no	68
Warnings:					
Information:					
6	Non Patent Literature	Exhibit_1011_IPR201400883.pdf	14560728 fb06579024a277e530bb09684f84c99d8bad6f29	no	266
Warnings:					
Information:					
7	Non Patent Literature	20140708_Corrected_Petition_for_Inter_Partes_Review_IPR2014401011.pdf	6392456 7ac563fe82a2624343712ca50ac41363d6c50fe3	no	68
Warnings:					
Information:					
8	Non Patent Literature	McCluskey_1986.pdf	2063520 65a221b1bdf55ee1a8405d71c7abad8727c74168	no	9
Warnings:					
Information:					
9	Non Patent Literature	Micron_2002.pdf	625881 5e9f78c41b214887c1f21776a02eacf5ac96a605	no	26

Warnings:					
Information:					
10	Non Patent Literature	20140606_Smart_Storage_Invalidity_Contentions.pdf	13104462 83f1b654d7f616ae16cad08de6f4a383f0f23f7b	no	85
Warnings:					
Information:					
11	Non Patent Literature	Exhibit_F1_F5.pdf	2996579 6dd1be41b8dd93ee6334946c9a6217b76c857dce	no	154
Warnings:					
Information:					
12	Non Patent Literature	Exhibit_G1_G6.pdf	814795 f3816f131e664f7c7386b336a28043f2ba245fa3	no	79
Warnings:					
Information:					
13	Non Patent Literature	Exhibit_H_Smart_Storage.pdf	452099 b3c4e028d034619877cbee4afa57879e9dbfb613	no	3
Warnings:					
Information:					
14	Non Patent Literature	20140606_DIABLO_Invalidity_Contentions.pdf	1703900 ed2e5f223734481110116 61f8139988b2fca4464	no	41
Warnings:					
Information:					
15	Non Patent Literature	Exhibit_F.pdf	2358744 9d1eef457c9c36d7ca24b6cf55b8044d6b370205	no	178
Warnings:					
Information:					
16	Non Patent Literature	Exhibit_G.pdf	1201560 d2cc352a3768ba3172145adbea8b7b0147a8ca58	no	137
Warnings:					
Information:					
17	Non Patent Literature	Exhibit_H_Diablo.pdf	45048 81f1e4da57ee373a3d87d4c1e42a28642560bda9	no	3
Warnings:					
Information:					
18	Fee Worksheet (SB06)	fee-info.pdf	30183 c573c381d01822ce77b07caf8151f37385bbe41e	no	2

Warnings:	
Information:	
Total Files Size (in bytes):	82146287

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

INFORMATION DISCLOSURE STATEMENT

Applicant	:	Netlist, Inc.
App. No.	:	13/971,231
Filed	:	August 20, 2013
For	:	LOAD-REDUCING CIRCUIT FOR MEMORY MODULE
Examiner	:	BANSAL, GURTEJ
Art Unit	:	2189
Conf No.	:	2072

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Enclosed for filing in the above-identified application is a Form PTO/SB/08a/b Equivalent listing 19 references. Copies of foreign documents and/or their translation and non-patent literature are submitted herewith.

The applicants would appreciate the Examiner initialing and returning the Form PTO/SB/08a/b Equivalent indicating that the information has been considered and made of record herein.

The information contained in this Information Disclosure Statement is not to be construed as a representation that: (i) a complete search has been made; (ii) additional information material to this application does not exist; (iii) the information, protocols, results and the like reported by third parties are accurate or enabling; or (iv) the above information constitutes prior art to the subject invention.

The Commissioner is authorized to charge any required fees to Deposit Account No. 50-5963.

Respectfully submitted,

Dated: November 26, 2014

/Jamie J. Zheng/ 51167

Jamie J. Zheng (Reg. No.)
Customer No. 79141
(650) 273-6008

Samsung Electronics Co., Ltd.
Ex. 1052, p. 247

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
13/971,231	08/20/2013	Jefferey C. Solomon	NETL.018P2C7

CONFIRMATION NO. 2072

79141
The Law Office of Jamie Zheng, Ph.D Esq.
P.O. Box 60573
Palo Alto, CA 94306

POA ACCEPTANCE LETTER

OC000000072067297

Date Mailed: 12/03/2014

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 11/20/2014.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

/dtdinh/

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

Application Number	Application/Control No.	Applicant(s)/Patent under Reexamination	
	13/971,231	SOLOMON ET AL.	

Document Code - DISQ	Internal Document – DO NOT MAIL

TERMINAL DISCLAIMER	☒ APPROVED	☐ DISAPPROVED
Date Filed : 11/20/14	**This patent is subject to a Terminal Disclaimer**	

Approved/Disapproved by:

Lawana Hixon

U.S. Patent and Trademark Office

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United States Patent and Trademark Office
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NOTICE OF ALLOWANCE AND FEE(S) DUE

79141 7590 01/09/2015

The Law Office of Jamie Zheng, Ph.D Esq.
P.O. Box 60573
Palo Alto, CA 94306

EXAMINER
BANSAL, GURTEJ

ART UNIT	PAPER NUMBER
2139	

DATE MAILED: 01/09/2015

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/971,231	08/20/2013	Jefferey C. Solomon	NETL.018P2C7	2072

TITLE OF INVENTION: LOAD-REDUCING CIRCUIT FOR MEMORY MODULE

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	SMALL	$480	$0	$0	$480	04/09/2015

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PTOL-85 (Rev. 02/11)

Samsung Electronics Co., Ltd.
Ex. 1052, p. 250

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

79141 7590 01/09/2015
The Law Office of Jamie Zheng, Ph.D Esq.
P.O. Box 60573
Palo Alto, CA 94306

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/971,231	08/20/2013	Jefferey C. Solomon	NETL.018P2C7	2072

TITLE OF INVENTION: LOAD-REDUCING CIRCUIT FOR MEMORY MODULE

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	SMALL	$480	$0	$0	$480	04/09/2015

EXAMINER	ART UNIT	CLASS-SUBCLASS
BANSAL, GURTEJ	2139	711-105000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
- ❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.
1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. The following fee(s) are submitted:
- ❑ Issue Fee
- ❑ Publication Fee (No small entity discount permitted)
- ❑ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**
- ❑ A check is enclosed.
- ❑ Payment by credit card. Form PTO-2038 is attached.
- ❑ The director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)
- ❑ Applicant certifying micro entity status. See 37 CFR 1.29
  NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
- ❑ Applicant asserting small entity status. See 37 CFR 1.27
  NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
- ❑ Applicant changing to regular undiscounted fee status.
  NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

PTOL-85 Part B (10-13) Approved for use through 10/31/2013. OMB 0651-0033 U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Samsung Electronics Co., Ltd.
Ex. 1052, p. 251

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/971,231	08/20/2013	Jefferey C. Solomon	NETL.018P2C7	2072

79141 7590 01/09/2015

The Law Office of Jamie Zheng, Ph.D Esq.
P.O. Box 60573
Palo Alto, CA 94306

EXAMINER	
BANSAL, GURTEJ	
ART UNIT	PAPER NUMBER
2139	

DATE MAILED: 01/09/2015

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

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Ex. 1052, p. 252

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 13/971,231	Applicant(s) SOLOMON ET AL.	
	Examiner GURTEJ BANSAL	Art Unit 2139	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *Applicant Amendment dated 12/03/2014*.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on_____.
2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.
3. ☒ The allowed claim(s) is/are *11-30*. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov .
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☐ All b) ☐ Some *c) ☐ None of the:
   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date 08/07/2014; 11/27/2014
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
5. ☐ Examiner's Amendment/Comment
6. ☐ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/GURTEJ BANSAL/
Primary Examiner, Art Unit 2139

Samsung Electronics Co., Ltd.
Ex. 1052, p. 254

Memory module with a **circuit** providing load **isolation** and memory domain translation
JC Solomon, JR Bhakta - US Patent 7,636,274, 2009 - Google Patents
... Memory module with a **circuit** providing load **isolation** and memory domain translation US 7636274 B2. Abstract. **...** memory module of claim 39 , wherein the **circuit** is configurable to selectively **isolate** both the **...** to be responsive to the set of input signals by selectively **isolating** one or **...**
Cited by 74 Related articles All 4 versions Cite Save

Programmable dynamic random access memory (DRAM)
S Schaefer - US Patent 5,457,659, 1995 - Google Patents
... Programmable **DQS** preamble. US7349269, Aug 31, 2005, Mar 25, 2008, Micron Technology, Inc. Programmable **DQS** preamble. **... Isolation circuit**. **...** Asynchronously-accessible memory device with mode selection **circuitry** for burst or pipelined operation. **...**
Cited by 74 Related articles All 2 versions Cite Save

Circuit providing load **isolation** and memory domain translation for memory module
JR Bhakta, JC Solomon - US Patent 7,881,150, 2011 - Google Patents
... The method further comprises activating the **circuit** to selectively **isolate** at least one of the loads of **...** used to reduce the current flow between the first **DQS** pin and the second **DQS** pin. **...** As used herein, the term "**isolation**" is a broad term which includes, without limitation, electrical **...**
Cited by 13 Related articles All 5 versions Cite Save

Dynamic redundancy for random access memory assemblies
TJ Dell, MW Kellogg - US Patent 5,996,096, 1999 - Google Patents
... In order to **isolate** the ASIC and DRAM data drivers, some kind of switch is needed, However, because a **...** re-mapping **circuitry** is implemented as an ASIC device and dotted directly to the RAM devices (all **DQs**) as well **...** Signal sharing **circuit** with microelectric die **isolation** features. **...**
Cited by 48 Related articles All 2 versions Cite Save

Circuit and method for reading data transfers that are sent with a source synchronous clock signal
PW Coteus, FD Ferraiolo, KC Gower - US Patent 6,807,125, 2004 - Google Patents
... The concepts of the present invention can also be further extended to provide a mode in which a greater range of possible arrivals of dq and **dqs** signals, (higher elasticity) are safely captured at the **...** Memory module with a **circuit** providing load **isolation** and memory **...**
Cited by 28 Related articles All 4 versions Cite Save

Circuit providing load **isolation** and memory domain translation for memory module
JR Bhakta, JC Solomon - US Patent 7,916,574, 2011 - Google Patents
... Circuit providing load **isolation** and memory domain translation for memory module US 7916574 B1. **...** The method further comprises activating the **circuit** to selectively **isolate** at least one of **...** of example memory modules comprising a **circuit** which multiplexes the **DQS** data strobe **...**
Cited by 5 Related articles All 5 versions Cite Save

Memory system with switching for data **isolation**
MM Deneroff, KM Sarocky, DL McCall... - US Patent ..., 2001 - Google Patents
... said memory module not requiring switches disposed on said memory module for data **isolation** and not **...** be placed in the memory system without affecting performance since the switches **isolate** unused DIMM **...** of **DQS**, and output data is referenced to both edges of **DQS**, as well **...**
Cited by 65 Related articles All 2 versions Cite Save

High-speed data-rate converting and switching **circuit**
C Karabatsos - US Patent 6,854,042, 2005 - Google Patents
... DQSA1are directed to memory Bank A. Similarly, strobes DQSB and DQSB1, generated by **DQS circuitry** 202, are **...** SW 37, 38, 39 **isolate** the internals of the device from the BUS to which **...** This low capacitance and the **isolation** feature allows the BUS to operate at high frequencies **...**
Cited by 28 Related articles All 2 versions Cite Save

Memory system with switching for data **isolation**
MM Deneroff, DL McCall, DE McCracken... - US Patent ..., 2000 - Google Patents
... Memory system with switching for data **isolation** US 6115278 A. Abstract. A memory system that **...** be placed in the memory system without affecting performance since the switches **isolate** unused DIMM **...** edges of **DQS**, and output data is referenced to both edges of **DQS**, as well as **...**
Cited by 34 Related articles All 2 versions Cite Save

Tri-directional, high-speed bus switch
C Karabatsos - US Patent 6,737,891, 2004 - Google Patents

Samsung Electronics Co., Ltd.
Ex. 1052, p. 255

... A port may be connected to the corresponding B port, with both A and B ports **isolated** from the **...** Furthermore, strobe signals are generated which appear at **DQS** CA and **DQS** CB. **...** Note that this **circuitry** provides for a high impedance of FET switch FS1, **isolating** port Cn from ports **...**
Cited by 12 Related articles All 4 versions Cite Save

Samsung Electronics Co., Ltd.
Ex. 1052, p. 256

PTO/SB/08a/b(07-09)
Approved for use through 7/31/2012. OMB 0651-0031
US Patent & Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 1 of 1

Complete if Known	
Application Number	13/971,231
Filing Date	August 20, 2013
First Named Inventor	Jayesh R. Bhakta
Art Unit	2189
Examiner Name	Unknown
Attorney Docket Number	NETL.018P2C7

US PATENT DOCUMENTS

Examiner Initials *	Cite No. [1]	Document Number / Number-Kind Code [2] (if known)	Publication Date (MM-DD-YYYY)	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	1.	6011710	01-04-2000	Wiggers	
	2.	20010008006	07-12-2001	Klein	
	3.	20050257109	11-17-2005	Averbuj	
	4.	20070070669	03-29-2007	Tsern	

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
	5.	Petition for Inter Partes Review filed on 6/24/2014 for U.S. Patent No. 8,516,185, IPR Case Number IPR2014-01029, and all associated documents including cited references and expert declarations, available at https://ptabtrials.uspto.gov	
	6.	Petition for Inter Partes Review filed on 6/22/2014 for U.S. Patent No. 7,881,150, IPR Case Number IPR2014-00882 and IPR Case Number IPR2014-01011, and all associated documents including cited references and expert declarations, available at https://ptabtrials.uspto.gov	
	7.	Petition for Inter Partes Review filed on 6/24/2014 for U.S. Patent No. 8,081,536, IPR Case Number IPR2014-00883, and all associated documents including cited references and expert declarations, available at https://ptabtrials.uspto.gov	
	8.	Altera, ACEX iK, Programmable Logic Device Family, Data Sheet, May 2003, Ver 3.4	
	9.	Horowitz, "The Art of Electronics," Cambridge Univ. Press, 1989, selected pages	
	10.	Jacob, Bruce L.; "Synchronous DRAM Architectures, Organizations, and Alternative Technologies". University of Maryland, Dec. 10, 2002.	
	11.	JEDEC Standard No. 21-C Section 4.5.7, 168 Pin Registered SDRAM DIMM Family, Release 7	
	12.	JEDEC 21-C, Section 4.6.1, 278 Pin Buffered SDRAM DIMM Family	
	13.	JEDEC Standard No. 21-C Section 4.1.2.5, Appendix E, "Specific PD's for Synchronous DRAM (SDRAM)," pp. 1-25,	

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* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1] Applicant's unique citation designation number (optional). [2] See Kinds Codes of USPTO Patents Documents at www.uspto.gov or MPEP 901.04. [3] Enter Office that issued the document, by the two-letter code (WIPO Standard ST. 3). [4] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5] Kind of document by the appropriate symbols as indicated on the document and WIPO Standard ST. 16 if possible. [6] Applicant is to place a check mark here if English language Translation is attached.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /G.B./

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13971231	SOLOMON ET AL.
	Examiner	Art Unit
	GURTEJ BANSAL	2189

CPC- SEARCHED		
Symbol	Date	Examiner

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner
711	5; 147	05/15/2014	GB

SEARCH NOTES		
Search Notes	Date	Examiner
Text Search in EAST (See Attached)	05/15/2014	GB
NPL Search in Google Scholar (See Attached)	05/15/2014	GB
Inventor Search in eDAN	05/15/2014	GB
Consulted Alex Sofocleous (SPE)	05/15/2014	GB
Updated Text Search in EAST (See Attached)	12/16/2014	GB
Updated Text Search in EAST (See Attached)	01/02/2015	GB
UPdated NPL Search in Google Scholar (See Attached)	01/02/2015	GB

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner
711	5; 147	01/02/2015	GB

/GURTEJ BANSAL/ Examiner.Art Unit 2189	

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PTO/SB/08a/b(07-09)
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Substitute for form 1449/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 1 of 1

Complete if Known	
Application Number	13/971,231
Filing Date	August 20, 2013
First Named Inventor	Jayesh R. Bhakta
Art Unit	2189
Examiner Name	BANSAL, GURTEJ
Attorney Docket Number	NETL.018P2C7

US PATENT DOCUMENTS

Examiner Initials *	Cite No. [1]	Document Number / Number-Kind Code [2] (if known)	Publication Date (MM-DD-YYYY)	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	1.	6747887	06-08-2004	Halbert et al.	
	2.	7093066	08-15-2006	Klein	
	3.	6832303	12/14/2004	Tanaka	

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
	4.	Inter Partes Review Case No. IPR2014-00882, Corrected Petition for Inter Partes Review of U.S. Patent No. 7,881,150, filed on July 8, 2014.	
	5.	Inter Partes Review Case No. IPR2014-00882, Exhibit 1007 to Petition for Inter Partes Review, "Declaration of Dr. Srinivasan Jagannathan," filed on June 22, 2014.	
	6.	Inter Partes Review Case No. IPR2014-00883, Corrected Petition for Inter Partes Review of U.S. Patent No. 8,081,536, filed on July 8, 2014.	
	7.	Inter Partes Review Case No. IPR2014-00883, Exhibit 1011 to Petition for Inter Partes Review, "Declaration of Dr. Srinivasan Jagannathan," filed on June 21, 2014.	
	8.	Inter Partes Review Case No. IPR2014-01011, Corrected Petition for Inter Partes Review of U.S. Patent No. 7,881,150, filed on July 8, 2014.	
	9.	Inter Partes Review Case No. IPR2014-01011, Exhibit 1007 to Petition for Inter Partes Review, "Declaration of Dr. Srinivasan Jagannathan." filed on June 22, 2014.	
	10.	McCluskey, Edward J., *Logic Design Principles with Emphasis on Testable Semicustom Circuits*, Prentice Hall, 1986, pp. 104-107 and 119-120.	
	11.	MICRON, DDR SDRAM DIMM Module: MT16VDDT3264A – 256 MB; MT16VDDT6464A – 512 MB, Data Sheet, 2002, Micron Technology, Inc.	
	12.	U.S. District Court Northern District of California, Case No. 4:13-CV-05889-YGR, *Netlist, Inc. v. Smart Storage Systems, Inc., and Diablo Technologies, Inc.*, Smart Storage Systems, Inc.'s Invalidity Contentions, dated June 6, 2014	
	13.	U.S. District Court Northern District of California, Case No. 4:13-CV-05889-YGR, *Netlist, Inc. v. Smart Storage Systems, Inc., and Diablo Technologies, Inc.*, Exhibits F.1-F.5 to "Smart Storage Systems, Inc.'s Invalidity Contentions," dated June 6, 2014.	
	14.	U.S. District Court Northern District of California, Case No. 4:13-CV-05889-YGR, *Netlist, Inc. v. Smart Storage Systems, Inc., and Diablo Technologies, Inc.*, Exhibits G.1-G.6 to "Smart Storage Systems, Inc.'s Invalidity Contentions," dated June 6, 2014.	
	15.	U.S. District Court Northern District of California, Case No. 4:13-CV-05889-YGR, *Netlist, Inc. v. Smart Storage Systems, Inc., and Diablo Technologies, Inc.*, Exhibit H to "Smart Storage Systems, Inc.'s Invalidity Contentions," dated June 6, 2014.	

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Substitute for form 1449/PTO				Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(Use as many sheets as necessary)*				Application Number	13/971,231
				Filing Date	August 20, 2013
				First Named Inventor	Jayesh R. Bhakta
				Art Unit	2189
				Examiner Name	BANSAL, GURTEJ
Sheet	2	of	1	Attorney Docket Number	NETL.018P2C7

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
	16.	U.S. District Court Northern District of California, Case No. 4:13-CV-05889-YGR, *Netlist, Inc. v. Smart Storage Systems, Inc., and Diablo Technologies, Inc.,* Diablo Technologies, Inc.'s Invalidity Contentions, dated June 6, 2014.	
	17.	U.S. District Court Northern District of California, Case No. 4:13-CV-05889-YGR, *Netlist, Inc. v. Smart Storage Systems, Inc., and Diablo Technologies, Inc.,* Exhibits F-1 to F-5 to "Diablo Technologies, Inc.'s Invalidity Contentions," dated June 6, 2014.	
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EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	3613	DQS and DQ	US-PGPUB; USPAT	OR	OFF	2015/01/01 23:10
L2	1574	DQS and DQ with (coupl$3 connect$3 isolat$3 select$3)	US-PGPUB; USPAT	OR	OFF	2015/01/01 23:10
L3	1309	DQS and DQ with (connect$3 isolat$3 select$3)	US-PGPUB; USPAT	OR	OFF	2015/01/01 23:11
L4	1108	DQS and DQ with (coupl$3 isolat$3 select$3)	US-PGPUB; USPAT	OR	OFF	2015/01/01 23:11
L5	569	DQS and DQ with (coupl$3 isolat$3)	US-PGPUB; USPAT	OR	OFF	2015/01/01 23:12
L6	149	DQS and DQ with (decoupl$3 isolat$3)	US-PGPUB; USPAT	OR	OFF	2015/01/01 23:15
L7	149	DQS and DQ with (decoupl$3 isolat$3 detach$3)	US-PGPUB; USPAT	OR	OFF	2015/01/01 23:17
L8	167	DQS and DQ with (decoupl$3 isolat$3 detach$3 disconnect$3)	US-PGPUB; USPAT	OR	OFF	2015/01/01 23:17
L9	20	DQS and DQ with (disconnect$3)	US-PGPUB; USPAT	OR	OFF	2015/01/01 23:18
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L11	3	"6747887".pn. "7093066".pn. "6832303".pn.	US-PGPUB; USPAT	OR	OFF	2015/01/02 00:03
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S3	88990	DS	US-PGPUB; USPAT	OR	OFF	2013/12/02 23:38
S4	32759	DQ	US-PGPUB; USPAT	OR	OFF	2013/12/02 23:38
S5	3171	S2 and S4	US-PGPUB;	OR	OFF	2013/12/02 23:38

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			USPAT			
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S7	329	S5 and S6	US-PGPUB; USPAT	OR	ON	2013/12/02 23:38
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S9	1184	multiplex$3 with (DQS and DQ)	US-PGPUB; USPAT	OR	ON	2013/12/03 00:07
S10	359	multiplex$3 with (DQS and DQ) with delay$3	US-PGPUB; USPAT	OR	ON	2013/12/03 00:08
S11	850	multiplex$3 with DQS and delay with delay$3	US-PGPUB; USPAT	OR	ON	2013/12/03 00:12
S12	562	multiplex$3 with DQS and DQ with delay$3	US-PGPUB; USPAT	OR	ON	2013/12/03 00:12
S13	401	multiplex$3 with DQS same DQ with delay$3	US-PGPUB; USPAT	OR	ON	2013/12/03 00:12
S14	0	13/287042.app.	US-PGPUB; USPAT	OR	ON	2013/12/03 00:25
S15	0	13/287042.ap.	US-PGPUB; USPAT	OR	ON	2013/12/03 00:25
S16	0	"13287042".ap.	US-PGPUB; USPAT	OR	ON	2013/12/03 00:25
S17	0	"13287042".app.	US-PGPUB; USPAT	OR	ON	2013/12/03 00:25
S18	294	multiplex$3 with DQS same delay$3 with data with signals	US-PGPUB; USPAT	OR	ON	2013/12/03 00:28
S19	307	multiplex$3 with DQS same delay$3 with data with (signals lines)	US-PGPUB; USPAT	OR	ON	2013/12/03 00:28
S20	9	multiplex$3 with DQS same delay$3 with data with (signals lines) same2 rank	US-PGPUB; USPAT	OR	ON	2013/12/03 00:28
S21	26	multiplex$3 with DQS same delay$3 with data with (signals lines) and rank	US-PGPUB; USPAT	OR	ON	2013/12/03 00:29
S22	238	multiplex$3 with DQS same delay$3 with	US-	OR	ON	2013/12/03

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		data with (signals lines) same memory	PGPUB; USPAT			00:30
S23	347	isolat$3 with DQ with DQS	US-PGPUB; USPAT	OR	ON	2013/12/03 00:47
S24	21	isolat$3 with DQ with DQS same Rank	US-PGPUB; USPAT	OR	ON	2013/12/03 00:47
S25	1353	DQS with select$3 with (memory rank)	US-PGPUB; USPAT	OR	ON	2013/12/03 00:50
S26	54	chip$1select with rank and DQ and DQS	US-PGPUB; USPAT	OR	ON	2013/12/03 18:25
S27	56	chip$1select same rank and DQ and DQS	US-PGPUB; USPAT	OR	ON	2013/12/03 18:26
S28	61	chip$1select and rank and DQ and DQS	US-PGPUB; USPAT	OR	ON	2013/12/03 18:27
S29	5	rank with DQ with DQS with low	US-PGPUB; USPAT	OR	ON	2013/12/03 18:39
S30	300	rank with DQ with DQS	US-PGPUB; USPAT	OR	ON	2013/12/03 18:40
S31	82	rank and (DQ with DQS) with off	US-PGPUB; USPAT	OR	ON	2013/12/03 19:03
S32	271	rank and (DQ with DQS) with high	US-PGPUB; USPAT	OR	ON	2013/12/03 19:07
S33	29	rank with (DQ with DQS) with high	US-PGPUB; USPAT	OR	ON	2013/12/03 19:07
S34	1	"6873533".pn.	US-PGPUB; USPAT	OR	ON	2013/12/03 19:07
S35	7	rank with (DQ with DQS) with terminat$3	US-PGPUB; USPAT	OR	ON	2013/12/03 19:10
S36	20	rank with (DQ with DQS) with isolat$3	US-PGPUB; USPAT	OR	ON	2013/12/03 19:11
S37	21	rank same (DQ with DQS) with isolat$3	US-PGPUB; USPAT	OR	ON	2013/12/03 19:11
S38	57	rank same (DQ with DQS) with high	US-PGPUB; USPAT	OR	ON	2013/12/03 19:11
S39	7	rank same (DQ with DQS) with (mux multiplexer)	US-PGPUB; USPAT	OR	ON	2013/12/03 19:15
S40	37	rank and (DQ with DQS) with (mux multiplexer)	US-PGPUB; USPAT	OR	ON	2013/12/03 19:16
S41	1040	(DQ with DQS) with (mux multiplexer)	US-	OR	ON	2013/12/03

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			PGPUB; USPAT			19:21
S42	1024	(DQ with DQS) with (mux multiplexer) and memory	US-PGPUB; USPAT	OR	ON	2013/12/03 19:21
S43	634	(DQ with DQS) with (mux multiplexer) same memory	US-PGPUB; USPAT	OR	ON	2013/12/03 19:21
S44	231	(DQ with DQS) with (mux multiplexer) with memory	US-PGPUB; USPAT	OR	ON	2013/12/03 19:21
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S47	1	"20030070052".pn.	US-PGPUB; USPAT	OR	ON	2013/12/03 19:42
S48	1	"20050047250".pn.	US-PGPUB; USPAT	OR	ON	2013/12/03 20:07
S49	1599	G06F12/0607.cpc. G06F12/0813.cpc.	US-PGPUB; USPAT	OR	OFF	2013/12/20 11:11
S50	2437	latency with memory adj controller with memory	US-PGPUB; USPAT	OR	ON	2014/04/04 14:15
S51	59	latency with memory adj controller with (measur$3 test$3)	US-PGPUB; USPAT	OR	ON	2014/04/04 14:16
S52	22	rank same (DQ with DQS) with isolat$3	US-PGPUB; USPAT	OR	ON	2014/04/04 15:16
S53	22	isolat$3 with DQ with DQS same Rank	US-PGPUB; USPAT	OR	ON	2014/04/04 15:29
S54	26	multiplex$3 with DQS same delay$3 with data with (signals lines) and rank	US-PGPUB; USPAT	OR	ON	2014/04/04 15:29
S55	1	"6553450".pn.	US-PGPUB; USPAT	OR	ON	2014/04/04 15:33
S56	1	"6742098".pn.	US-PGPUB; USPAT	OR	ON	2014/04/04 15:48
S60	644	isolat$3 with load with memory	US-PGPUB; USPAT	OR	ON	2014/04/04 15:58
S61	46	isolat$3 with load with memory with controller	US-PGPUB; USPAT	OR	ON	2014/04/04 15:58
S62	28	US-5345412-$.DID. OR US-5537584-$.DID. OR US-5617559-$.DID. OR US-5649159-$.DID. OR US-5717851-$.DID. OR US-5724604-$.DID. OR US-5729716-	US-PGPUB; USPAT	OR	ON	2014/05/05 00:39

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		$.DID. OR US-5784705-$.DID. OR US-5802541-$.DID. OR US-5973392-$.DID. OR US-6173357-$.DID. OR US-6260127-$.DID. OR US-6446158-$.DID. OR US-6553449-$.DID. OR US-6618791-$.DID. OR US-6717855-$.DID. OR US-6788592-$.DID. OR US-6948084-$.DID. OR US-7130308-$.DID. OR US-7133960-$.DID. OR US-7379361-$.DID. OR US-20050010737-$.DID. OR US-20070293094-$.DID. OR US-3412243-$.DID. OR US-2201420-$.DID. OR US-2761179-$.DID. OR US-2201346-$.DID. OR US-2504131-$.DID.				
S63	2355572	read$only with non$1volatile with main memory	US-PGPUB; USPAT	OR	OFF	2014/05/08 19:12
S64	2126	read$only with non$1volatile with main with memory	US-PGPUB; USPAT	OR	OFF	2014/05/08 19:12
S65	1	"20080080261".pn.	US-PGPUB; USPAT	OR	OFF	2014/05/11 20:14
S66	4529	711/5.ccls. 711/147.ccls.	US-PGPUB; USPAT	OR	OFF	2014/05/15 16:09

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L12	3626	711/5.ccls. 711/147.ccls.	USPAT; UPAD	OR	OFF	2015/01/02 00:11
L13	5815	isolates.clm.	USPAT; UPAD	OR	OFF	2015/01/02 00:12
L14	0	L12 and "L143"	USPAT; UPAD	OR	OFF	2015/01/02 00:12
L15	7	L12 and L13	USPAT; UPAD	OR	OFF	2015/01/02 00:12
L16	0	L12 and L13 and DQS.clm.	USPAT; UPAD	OR	OFF	2015/01/02 00:15
S57	3448	711/5.ccls. 711/147.ccls.	USPAT; UPAD	OR	OFF	2014/04/04 15:50
S58	171076	isolat$3.clm.	USPAT; UPAD	OR	OFF	2014/04/04 15:52
S59	45	S57 and S58	USPAT; UPAD	OR	OFF	2014/04/04 15:52

1/ 2/ 2015 12:15:22 AM
C:\ Users\ gbansal\ Documents\ EAST\ Workspaces\ 13971231.wsp

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Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13971231	SOLOMON ET AL.
	Examiner	**Art Unit**
	GURTEJ BANSAL	2139

CPC						
Symbol					**Type**	**Version**
G06F		12	/	00	F	2013-01-01
G11C		5	/	04	I	2013-01-01
G06F		13	/	00	I	2013-01-01
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CPC Combination Sets							
Symbol					**Type**	**Set**	**Ranking**	**Version**
			/					
			/					

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	20	
/GURTEJ BANSAL/ Primary Examiner.Art Unit 2139	01/01/2015	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	11	1

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Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13971231	SOLOMON ET AL.
	Examiner	**Art Unit**
	GURTEJ BANSAL	2139

US ORIGINAL CLASSIFICATION		INTERNATIONAL CLASSIFICATION										
CLASS	SUBCLASS	CLAIMED					NON-CLAIMED					
711	5	G	0	6	F	12 / 00 (2006.01.01)						

CROSS REFERENCE(S)					
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)				
711	147				

NONE		Total Claims Allowed:
(Assistant Examiner)	(Date)	20
/GURTEJ BANSAL/ Primary Examiner.Art Unit 2139	01/01/2015	O.G. Print Claim(s): 11 / O.G. Print Figure: 1
(Primary Examiner)	(Date)	

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Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13971231	SOLOMON ET AL.
	Examiner	**Art Unit**
	GURTEJ BANSAL	2139

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☒ T.D. ☐ R.1.47

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
	1	9	17												
	2	3	18												
	3	10	19												
	4	4	20												
	5	11	21												
	6	12	22												
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	10	18	26												
1	11	19	27												
2	12	13	28												
5	13	20	29												
6	14	14	30												
7	15														
8	16														

NONE (Assistant Examiner)	(Date)	**Total Claims Allowed:** 20	
/GURTEJ BANSAL/ Primary Examiner.Art Unit 2139 (Primary Examiner)	01/01/2015 (Date)	O.G. Print Claim(s) 11	O.G. Print Figure 1

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UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
13/971,231	08/20/2013	2139	800	NETL.018P2C7	10	2

CONFIRMATION NO. 2072

CORRECTED FILING RECEIPT

79141
The Law Office of Jamie Zheng, Ph.D Esq.
P.O. Box 60573
Palo Alto, CA 94306

OC000000073472062

Date Mailed: 02/19/2015

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Inventor(s)

Jefferey C. Solomon, Irvine, CA;
Jayesh R. Bhakta, Cerritos, CA;

Applicant(s)

Netlist, Inc., Irvine, CA

Assignment For Published Patent Application

Netlist, Inc., Irvine, CA

Power of Attorney: The patent practitioners associated with Customer Number 79141

Domestic Priority data as claimed by applicant

This application is a CON of 13/287,081 11/01/2011 PAT 8516188
which is a CON of 13/032,470 02/22/2011 PAT 8081536
which is a CON of 12/955,711 11/29/2010 PAT 7916574
which is a CON of 12/629,827 12/02/2009 PAT 7881150
which is a CON of 12/408,652 03/20/2009 PAT 7636274
which is a CON of 11/335,875 01/19/2006 PAT 7532537
which claims benefit of 60/645,087 01/19/2005
and is a CIP of 11/173,175 07/01/2005 PAT 7289386
which claims benefit of 60/588,244 07/15/2004
and is a CIP of 11/075,395 03/07/2005 PAT 7286436
which claims benefit of 60/550,668 03/05/2004
and claims benefit of 60/575,595 05/28/2004
and claims benefit of 60/590,038 07/21/2004

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.) - None.

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Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

If Required, Foreign Filing License Granted: 09/11/2013

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 13/971,231**

Projected Publication Date: Not Applicable

Non-Publication Request: No

Early Publication Request: No

**** SMALL ENTITY ****

Title

MEMORY MODULE WITH LOAD REDUCING CIRCUIT AND METHOD OF OPERATION

Preliminary Class

711

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

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Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific

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countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

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Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

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Doc code: RCEX
Doc description: Request for Continued Examination (RCE)

PTO/SB/30EFS (07-09)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

REQUEST FOR CONTINUED EXAMINATION(RCE)TRANSMITTAL
(Submitted Only via EFS-Web)

Application Number	13/971,231	Filing Date	2013-08-20	Docket Number (if applicable)	NETL.018P2C7	Art Unit	2139
First Named Inventor	Jefferey C. Solomon			Examiner Name	Bansal, Gurtej		

This is a Request for Continued Examination (RCE) under 37 CFR 1.114 of the above-identified application.
Request for Continued Examination (RCE) practice under 37 CFR 1.114 does not apply to any utility or plant application filed prior to June 8, 1995, or to any design application. The Instruction Sheet for this form is located at WWW.USPTO.GOV

SUBMISSION REQUIRED UNDER 37 CFR 1.114

Note: If the RCE is proper, any previously filed unentered amendments and amendments enclosed with the RCE will be entered in the order in which they were filed unless applicant instructs otherwise. If applicant does not wish to have any previously filed unentered amendment(s) entered, applicant must request non-entry of such amendment(s).

☐ Previously submitted. If a final Office action is outstanding, any amendments filed after the final Office action may be considered as a submission even if this box is not checked.

- ☐ Consider the arguments in the Appeal Brief or Reply Brief previously filed on _____
- ☐ Other _____

☒ Enclosed

- ☒ Amendment/Reply
- ☒ Information Disclosure Statement (IDS)
- ☐ Affidavit(s)/ Declaration(s)
- ☐ Other _____

MISCELLANEOUS

☐ Suspension of action on the above-identified application is requested under 37 CFR 1.103(c) for a period of months _____
(Period of suspension shall not exceed 3 months; Fee under 37 CFR 1.17(i) required)

☐ Other _____

FEES

☒ **The RCE fee under 37 CFR 1.17(e) is required by 37 CFR 1.114 when the RCE is filed.**
The Director is hereby authorized to charge any underpayment of fees, or credit any overpayments, to Deposit Account No 505963

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT REQUIRED

☒ Patent Practitioner Signature

☐ Applicant Signature

PTO/SB/30EFS (07-09)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Signature of Registered U.S. Patent Practitioner			
Signature	/Jamie J. Zheng/	Date (YYYY-MM-DD)	2015-03-23
Name	Jamie J. Zheng	Registration Number	51167

This collection of information is required by 37 CFR 1.114. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

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2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

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Electronically filed **

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	:	Netlist, Inc.
App. No.	:	13/971,231
Filed	:	August 20, 2013
For	:	MEMORY MODULE WITH LOAD REDUCING CIRCUIT AND METHOD OF OPERATION
Examiner	:	BANSAL, GURTEJ
Art Unit	:	2139
Conf. No.	:	2072
Docket No.	:	NETL.018P2C7

CERTIFICATE OF EFS WEB TRANSMISSION

I hereby certify that this correspondence and any other attachment noted on the Automated Acknowledgement Receipt, is being transmitted from within the Pacific Time zone to the Commissioner for Patents via the EFS Web Server on:

March 23, 2015

(Date)

/Jamie J. Zheng/

Jamie J. Zheng, Reg. No. 51167

AMENDMENT AND REQUEST FOR CONTINUED EXAMINATION

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

A Request for Continued Examination (RCE) is filed herewith for the above-identified patent application. Please amend the application as follows prior to continued examination.

The Commissioner is hereby authorized to charge any required fee(s) to Deposit Account No. 50-5963.

AMENDMENTS to the SPECIFICATION begin on Page 2 of this paper.
AMENDMENTS to the CLAIMS begin on Page 4 of this paper.
REMARKS begin on Page 11 of this paper.

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IN THE SPECIFICATION

Please amend paragraphs [0011]-[0013] under the Summary of the Invention as follows:

[0011] In certain embodiments, a memory module includes a plurality of memory devices and is operable in a computer system to perform memory operations in response to memory commands from a memory controller of the computer system. The memory module being coupled to the memory controller via a memory bus, the memory bus including a control/address (C/A) bus and a data bus. The memory module comprises a register device configured to receive a set of input control/address signals associated with a respective memory command (e.g., a read command or a write command) from the memory controller and to generate a set of output control/address signals in response to the set of input control/address signals. The set of output control/address signals are provided to the plurality of memory devices. The memory module further comprises a circuit coupled between the data bus and the plurality of memory devices, the circuit to selectively isolate one or more first memory devices among the plurality of memory devices from the data bus ~~memory controller~~ in response to the respective memory command so as to reduce a load of the memory module to the computer system while one or more second memory devices among the plurality of memory devices are communicating with the memory controller in response to the set of output control/address signals.

[0012] In certain embodiments, the circuit further comprises DQ-DQS paths, and ~~the~~ logic that selectively isolates the one or more first memory devices by disabling at least one first group of DQ-DQS paths ~~so as to isolate the one or more first memory devices~~. In certain embodiments, the logic is further configured to enable at least one second group of DQ-DQS paths in response to the respective memory command so as to allow the one or more second memory devices to communicate data with the memory controller in response to the output control/address signals. In certain embodiments, the ~~logic element~~ circuit includes a buffer circuit to electrically and selectively isolate the one or more first memory devices from the memory controller and to selectively allow one or more second memory devices to communicate data with the memory controller, the buffer circuit adding a time delay (e.g., one clock cycle) to a data signal from the one or more second memory devices to the memory controller. In certain embodiments, the logic provides functions of a data path

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multiplexer/demultiplexer using the time delay. In certain embodiments, the logic is further configured to translate between a system memory domain and a physical memory device domain by generating a greater number of output control/address signals than the number of input control/address signals in response to the respective memory command. In certain embodiments, the logic receives one or more input chip select signals associated with the respective memory command, the one or more input chip select signals being less in number than chip-select signals in the output control/address signals.

[0013] In certain embodiments, a method of operating ~~a circuit in~~ a memory module comprises receiving a set of input control/address signals associated with a respective memory command from the memory controller, generating a set of output control/address signals in response to the set of input control/address signals, and providing the set of output control/address signals to a plurality of memory devices operable to perform memory operations in response to memory commands from a memory controller. The method further comprises monitoring the memory commands from the memory controller, and selectively isolating one or more first memory devices among the plurality of memory devices from the memory controller in response to the respective memory command so as to reduce a load of the memory module to the memory controller while one or more second memory devices among the plurality of memory devices are communicating with the memory controller in response to the set of output control/address signals. In certain embodiments, the method further comprises disabling at least one first group of DQ-DQS paths to isolate the one or more first memory devices and selectively enabling at least one second group of DQ-DQS paths to allow the one or more second memory devices to communicate data with the memory controller in response to the output control/address signals. In certain embodiments, the set of input control/address signals include at least one chip-select signal and the set of output control/address signals include a greater number of chip-select signals. _____

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AMENDMENTS TO THE CLAIMS

1-10. (Cancelled)

11. (Currently Amended) A memory module operable in a computer system to perform memory operations in response to memory commands from a memory controller of the computer system, the memory module being coupled to the memory controller via a memory bus, the memory bus including a control/address (C/A) bus and a data bus, the data bus including a set of data (DQ) and data strobe (DQS) signal lines, comprising:

a plurality of memory devices including a first set of memory devices and a second set of memory devices;

a register device to receive from the memory controller a first set of input C/A signals associated with a first memory command via the C/A bus and subsequently a second set of input C/A signals associated with a second memory command via the C/A bus, the first memory command to cause ~~make~~ the memory module receive or output a first data burst and the second memory command to cause ~~make~~ the memory module receive or output a second data burst, the register to generate a first set of output C/A signals in response to the first set of input C/A signals and a second set of output C/A signals in response to the second set of input C/A signals, the first set of output C/A signals causing the first set of memory devices to receive or output the first data burst, the second set of output C/A signals causing the second set of memory devices to receive or output the second data burst; and

a circuit coupled between the data bus and the plurality of memory devices, the circuit being coupled to the first set of memory devices via a first set of module DQ and DQS signal lines and to the second set of memory devices via a second set of module DQ and DQS signal lines, wherein the circuit in response to the first memory command couples the first set of module DQ and DQS signal lines to respective DQ and DQS signal lines of the data bus and isolates the second set of module DQ and DQS signal lines from the data bus as the memory module is receiving or outputting the first data burst in response to the first memory command, and wherein the circuit in response to the second memory command couples the second set of module DQ and DQS signal lines to respective DQ and DQS signal lines of the data bus and isolates the first set of module DQ and DQS signal lines from the data bus as the

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memory module is receiving or outputting the second data burst in response to the second memory command.

12. (Previously Presented) The memory module of claim 11, wherein the circuit isolates both the first set of module DQ and DQS signal lines and the second set of module DQ and DQS signal lines from the data bus when the memory module is not being accessed by the memory system.

13. (Currently Amended) The memory module of claim 11, wherein the circuit further comprises multiple groups of DQ-DQS paths including a first group of DQ-DQS paths corresponding to the first set of module DQ and DQS signal lines and a second group of DQ-DQS paths corresponding to the second set of module DQ and DQS signal lines, wherein the circuit enables the first group of DQ-DQS paths and ~~as~~ disabling the second group of DQ-DQS paths in response to the first memory command, and wherein the circuit enables the second group of DQ-DQS paths and ~~as~~ disabling the first group of DQ-DQS paths in response to the second memory command.

14. (Previously Presented) The memory module of claim 13, wherein the register device is to translate between a system memory domain of the computer system and a physical memory device domain of the memory module, the system memory domain having a smaller number of ranks than the physical memory device domain, and wherein the first set of the plurality of memory devices and the second set of the plurality of memory devices belong to a same rank in the system memory domain and to different ranks in the physical memory device domain.

15. (Previously Presented) The memory module of claim 14, wherein the first set of input C/A signals include at least one chip-select signal and the register device outputs a greater number of chip-select signals than the at least one chip-select signal, the greater number of chip-select signals including a first chip select signal and a second chip select signal, the first chip-select signal being provided to the first set of memory devices and having an active value to select the first set of memory devices to receive or output the first data burst in response to the first memory command, the second chip-select signal being provided to the second set of memory devices and having a non-active value to keep the second set of memory devices from receiving or outputting data as the first set of memory devices are receiving or outputting the first data burst in response to the first memory command.

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16. (Previously Presented) The memory module of claim 11, wherein the first memory command is a first read command and the second memory command is a second read command, wherein the first read command and the second read command are back to back adjacent read commands, and wherein the first set of memory devices output the first data burst together with a first burst of data strobes in response to the first read command, wherein the second set of memory devices output the second data burst together with a second burst of data strobes in response to the second read command, wherein the second data burst follows the first data burst on the data bus, and wherein the circuit prevents the first burst of data strobes and the second burst of data strobes from colliding with each other.

17. (Previously Presented) The memory module of claim 16, wherein each of the first burst of data strobes and the second burst of data strobes includes a pre-amble interval and a post-amble interval, and wherein the circuit combines the first burst of data strobes and the second burst of data strobes by skipping the post-amble interval of the first burst of data strobes and the pre-amble interval of the second burst of data strobes.

18. (Previously Presented) The memory module of claim 11, wherein the memory bus further includes an on-die termination (ODT) bus for conveying an ODT signal from the memory controller, each ODT signal corresponding to a respective memory command from the memory controller, wherein each memory device of the plurality of memory devices includes an ODT control input to allow a signal at the control input to enable or disable an ODT circuit in the memory device, and wherein the plurality of memory devices include at least one memory device having its respective control input configured to keep the ODT circuits in the at least one memory device disabled regardless of the ODT signal from the memory controller.

19. (Previously Presented) The memory module of claim 17, further comprising a termination assembly external to the plurality of memory devices and controlled in response to the ODT signal, wherein one or more DQ pins of the at least one memory device are coupled to the termination assembly so that one or more DQ signal paths between the at least one memory device and the memory controller can be terminated by the termination assembly.

20. (Previously Presented) The memory module of claim 11, wherein the circuit is to receive from the memory controller a third set of input C/A signals associated with a third

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memory command via the C/A bus, the third memory command being one of a refresh or precharge command, wherein the register to generate a third set of output C/A signals in response to the third set of input C/A signals, the third set of output C/A signals causing both the first set of memory devices and the second set of memory devices to perform one of a refresh operation and a pre-charge operation, and wherein the circuit in response to the third memory command couples the first set of module DQ and DQS signal lines to respective DQ and DQS signal lines of the data bus and couples the second set of module DQ and DQS signal lines to respective DQ and DQS signal lines of the data bus.

21. (Previously Presented) A method of operating a memory module in response to memory commands from a memory controller, the memory module having a plurality of memory devices including a first set of memory devices and a second set of memory devices, the memory module being coupled to the memory controller via a memory bus, the memory bus including a control/address (C/A) bus and a data bus, the data bus including a set of data (DQ) and data strobe (DQS) signal lines, the first set of memory devices having a first set of DQ and DQS pins, the second set of memory devices having a second set of DQ and DQS pins, the method comprising:

receiving from the memory controller a first set of input C/A signals associated with a first memory command via the C/A bus, the first memory command to cause the memory module to receive or output a first data burst;

generating a first set of output C/A signals in response to the first set of input C/A signals, the first set of output C/A signals causing the first set of memory devices to receive or output the first data burst,;

receiving from the memory controller a second set of input control/address signals associated with a second memory command via the C/A bus, the second memory command to cause the memory module to receive or output a second data burst

generating a second set of output C/A signals in response to the second set of input C/A signals, the second set of output C/A signals causing the second set of memory devices to receive or output the second data burst;

in response to the first memory command, coupling the first set DQ and DQS pins to respective DQ and DQS signal lines of the data bus and isolating the second set of module DQ and DQS pins from the data bus as the memory module is receiving or outputting the first data burst in response to the first memory command; and

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in response to the second memory command, coupling the second set DQ and DQS pins to respective DQ and DQS signal lines of the data bus and isolating the first set of DQ and DQS pins from the data bus as the memory module is receiving or outputting the second data burst in response to the second memory command.

22. (Previously Presented) The method of claim 21, further comprising isolating both the first set of DQ and DQS pins and the second set of DQ and DQS pins from the data bus when the memory module is not being accessed by the memory system.

23. (Currently Amended) The method of claim 21, wherein the memory module further comprises multiple groups of DQ-DQS paths including a first group of DQ-DQS paths corresponding to the first set of DQ and DQS pins and a second group of DQ-DQS paths corresponding to the second set of DQ and DQS pins, the method further comprising enabling the first group of DQ-DQS paths and ~~as~~ disabling the second group of DQ-DQS paths in response to the first memory command, and enabling the second group of DQ-DQS paths and ~~as~~ disabling the first group of DQ-DQS paths in response to the second memory command.

24. (Previously Presented) The method of claim 23, further comprising translating between a system memory domain and a physical memory device domain, the system memory domain having a smaller number of ranks than the physical memory device domain, and wherein the first set of the plurality of memory devices and the second set of the plurality of memory devices belong to a same rank in the system memory domain and to different ranks in the physical memory device domain.

25. (Previously Presented) The method of claim 24, wherein the first set of input C/A signals include at least one chip-select signal and the register device outputs a greater number of chip-select signals than the at least one chip-select signal, the greater number of chip-select signals including a first chip select signal and a second chip select signal, the first chip-select signal being provided to the first set of memory devices and having an active value to select the first set of memory devices to receive or output the first data burst in response to the first memory command, the second chip-select signal being provided to the second set of memory devices and having a non-active value to keep the second set of memory devices from receiving or outputting data as the first set of memory devices are receiving or outputting the first data burst in response to the first memory command.

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26. (Previously Presented) The method of claim 21, wherein the first memory command is a first read command and the second memory command is a second read command, wherein the first read command and the second read command are back to back adjacent read commands, and wherein the first set of memory devices output the first data burst together with a first burst of data strobes in response to the first read command, wherein the second set of memory devices output the second data burst together with a second burst of data strobes in response to the second read command, wherein the second data burst follows the first data burst on the data bus, the method further comprising combining the first burst of data strobes and the second burst of data strobes to form a third burst of data strobes on the data bus.

27. (Previously Presented) The method of claim 26, wherein each of the first burst of data strobes and the second burst of data strobes includes a pre-amble interval and a post-amble interval, and wherein combining the first burst of data strobes and the second burst of data strobes comprises skipping the post-amble interval of the first burst of data strobes and the pre-amble interval of the second burst of data strobes.

28. (Previously Presented) The method of claim 21, wherein the memory bus further includes an on-die termination (ODT) bus for conveying an ODT signal corresponding to each memory command from the memory controller, wherein each of the plurality of memory devices includes ODT circuits and an ODT control input to allow a signal at the control input to enable or disable the ODT circuits in the memory device, the method further comprising keeping the ODT circuits in at least one of the plurality of memory devices disabled regardless of the ODT signal from the memory controller.

29. (Previously Presented) The method of claim 27, further comprising controlling a termination assembly external to the plurality of memory devices according to the ODT signal, wherein one or more DQ pins of the at least one memory device are coupled to the termination assembly so that one or more DQ signal paths between the at least one memory device and the memory controller can be terminated by the termination assembly.

30. (Previously Presented) The method of claim 21, further comprising:

receiving from the memory controller a third set of input C/A signals associated with a third memory command via the C/A bus, the third memory command being one of a refresh or precharge command;

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generating a third set of output C/A signals in response to the third set of input C/A signals, the third set of output C/A signals causing both the first set of memory devices and the second set of memory devices to perform one of a refresh operation and a pre-charge operation; and

in response to the third memory command, coupling the first set of module DQ and DQS signal lines to respective DQ and DQS signal lines of the data bus and coupling the second set of module DQ and DQS signal lines to respective DQ and DQS signal lines of the data bus.

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REMARKS

This amendment and request for continued examination is filed after the Notice of Allowance dated January 9, 2015.

Paragraphs [0011]-[0013] under the Summary of the Invention are amended to correspond with the allowed claims. Claims 11, 13 and 23 are amended for wording consistency and to correct typographical errors. No new matter is added.

In light of the above amendments and remarks, the Applicants respectfully request that the Examiner reconsider this application with a view towards allowance. The Examiner is invited to call the undersigned attorney at (650) 273-6008, if a telephone call could help resolve any remaining items.

Respectfully submitted,

/Jamie J. Zheng/

Date: March 23, 2015

Jamie J. Zheng (Reg. No. 51167)
Customer Number 79141

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INFORMATION DISCLOSURE STATEMENT

Applicant	:	Netlist, Inc.
App. No.	:	13/971,231
Filed	:	August 20, 2013
For	:	LOAD-REDUCING CIRCUIT FOR MEMORY MODULE
Examiner	:	BANSAL, GURTEJ
Art Unit	:	2139
Conf No.	:	2072

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Enclosed for filing in the above-identified application is a Form PTO/SB/08a/b Equivalent listing 54 references. Copies of foreign documents and/or their translation and non-patent literature are submitted herewith.

The applicants would appreciate the Examiner initialing and returning the Form PTO/SB/08a/b Equivalent indicating that the information has been considered and made of record herein.

The information contained in this Information Disclosure Statement is not to be construed as a representation that: (i) a complete search has been made; (ii) additional information material to this application does not exist; (iii) the information, protocols, results and the like reported by third parties are accurate or enabling; or (iv) the above information constitutes prior art to the subject invention.

This Information Disclosure Statement is being filed before the receipt of a first Office Action on the merits, and presumably no fee is required. If a first Office Action on the merits

was mailed before the mailing date of this Statement, the Commissioner is authorized to charge the fee set forth in 37 C.F.R. § 1.17(p) to Deposit Account No. 50-5963.

Respectfully submitted,

Dated: March 23, 2015

/Jamie J. Zheng/ 51167

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet	1	of	3

Complete if Known	
Application Number	13/971,231
Filing Date	August 20, 2013
First Named Inventor	Jayesh R. Bhakta
Art Unit	2139
Examiner Name	Unknown
Attorney Docket Number	NETL.018P2C7

US PATENT DOCUMENTS

Examiner Initials *	Cite No. [1]	Document Number Number-Kind Code [2] (if known)	Publication Date (MM-DD-YYYY)	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	1.	5388240	02-01-1995	IBM Corporation	
	2.	5463590	10-31-1995	Watanabe	
	3.	5953280	09-14-1999	Matsui	
	4.	6188641	02-13-2001	Uchida	
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	6.	6480439	11-12-2002	Tokutome et al.	
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	10.	8130560	03-06-2012	Rajan	
	11.	8189328	05-29-2012	Kanapathippillai	
	12.	8233303	07-31-2012	Best	
	13.	8250295	08-21-2012	Amidi et al.	
	14.	8417870	04-09-2013	Lee et al.	
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	21.	RE36229	06-15-1999	Cady	

US PATENT APPLICATIONS

Examiner Initials *	Cite No. [1]	Application Number	Filing Date (MM-DD-YYYY)	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	22.	13/411,344	3/2/2012	Lee	Entire Prosecution History
	23.	13/970,606	8/20/2013	Netlist, Inc.	Entire Prosecution History
	24.	13/971,231	8/20/2013	Netlist, Inc.	Entire Prosecution History
	25.	14/229,844	3/29/2014	Netlist, Inc.	Entire Prosecution History
	26.	14/324,990	7/7/2014	Netlist, Inc.	Entire Prosecution History
	27.	14/337,168	7/21/2014	Netlist, Inc.	Entire Prosecution History

NON PATENT LITERATURE DOCUMENTS

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Substitute for form 1449/PTO				Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(Use as many sheets as necessary)*				Application Number	13/971,231
				Filing Date	August 20, 2013
				First Named Inventor	Jayesh R. Bhakta
				Art Unit	2139
				Examiner Name	Unknown
Sheet	2	of	3	Attorney Docket Number	NETL.018P2C7

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
	28.	Inter Partes Review of U.S. Patent No. 7,881,150, IPR Case No. IPR2014-00882, Patent Owner's Preliminary Response Pursuant to 37 C.F.R. § 42.107, filed October 7, 2014	
	29.	Inter Partes Review of U.S. Patent No. 7,881,150, IPR Case No. IPR2014-00882, Decision – Institution of Inter Partes Review 37 C.F.R. § 42.108, issued December 16, 2014	
	30.	Inter Partes Review of U.S. Patent No. 8,081,536, IPR Case No. IPR2014-00883, Patent Owner's Preliminary Response Pursuant to 37 C.F.R. § 42.107, filed October 7, 2014	
	31.	Inter Partes Review of U.S. Patent No. 8,081,536, IPR Case No. IPR2014-00883, Decision – Institution of Inter Partes Review 37 C.F.R. § 42.108, issued December 16, 2014	
	32.	Inter Partes Review of U.S. Patent No. 7,881,150, IPR Case No. IPR2014-01011, Patent Owner's Preliminary Response Pursuant to 37 C.F.R. § 42.107, filed October 7, 2014	
	33.	Inter Partes Review of U.S. Patent No. 7,881,150, IPR Case No. IPR2014-01011, Decision – Institution of Inter Partes Review 37 C.F.R. § 42.108, issued December 16, 2014	
	34.	Inter Partes Review of U.S. Patent No. 7,881,150, IPR Case No. IPR2014-01011, Exhibit 3001 to Decision – Institution of Inter Partes Review, Excerpts from IEEE Dictionary, issued December 16, 2014	
	35.	Inter Partes Review of U.S. Patent No. 7,881,150, IPR Case No. IPR2014-01011, Exhibit 3002 to Decision – Institution of Inter Partes Review, Excerpts from IEEE Dictionary, issued December 16, 2014	
	36.	Inter Partes Review of U.S. Patent No. 7,881,150, IPR Case No. IPR2014-01011, Exhibit 3003 to Decision – Institution of Inter Partes Review, Excerpts from Oxford English Dictionary, issued December 16, 2014	
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	39.	Inter Partes Review Case No. IPR2014-01029, Petition for Inter Partes Review of U.S. Patent No. 8,516,185, filed on June 24, 2014.	
	40.	Inter Partes Review Case No. IPR2014-01029, Exhibit 1008 to Petition for Inter Partes Review, "Declaration of Charles J. Neuhauser, Ph.D. under 37 C.F.R. § 1.68," filed on June 24, 2014.	
	41.	Inter Partes Review Case No. IPR2014-01029, Supplemental Petition for Inter Partes Review of U.S. Patent No. 8,516,185, filed on July 23, 2014.	
	42.	Inter Partes Review Case No. IPR2014-01029, Patent Owner's Preliminary Response pursuant to 37 C.F.R. § 42.107, filed on October 17, 2014.	
	43.	Inter Partes Review Case No. IPR2014-01029, Decision Denying Institution of Inter Partes Review 37 C.F.R. § 42.108, issued December 16, 2014.	
	44.	Inter Partes Review Case No. IPR2014-01029, Petitioner's Request for Rehearing pursuant to 37 C.F.R. § 42.71, filed on January 15, 2015.	

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(Use as many sheets as necessary)

Sheet	3	of	3

Complete if Known	
Application Number	13/971,231
Filing Date	August 20, 2013
First Named Inventor	Jayesh R. Bhakta
Art Unit	2139
Examiner Name	Unknown
Attorney Docket Number	NETL.018P2C7

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
	45.	Inter Partes Review Case No. IPR2014-01029, Decision Denying Request for Rehearing, Issued on March 3, 2015.	
	46.	Inter Partes Review Case No. IPR2014-01369, Corrected Petition for Inter Partes Review of Claims 1-19 of U.S. Patent No. 8,516,185, filed on September 22, 2014.	
	47.	Inter Partes Review Case No. IPR2014-01369, Exhibit 1008 to Corrected Petition for Inter Partes Review, "Declaration of Dr. Nader Bagherzadeh under 37 C.F.R. § 1.68," filed on September 22, 2014.	
	48.	Inter Partes Review Case No. IPR2014-01369, Exhibit 1013 to Corrected Petition for Inter Partes Review, "Webster's II New College Dictionary," filed on September 22, 2014.	
	49.	Inter Partes Review Case No. IPR2014-01369, Exhibit 1014 to Corrected Petition for Inter Partes Review, "Standard Dictionary of Electrical and Electronics Terms," IEEE 1988, filed on September 22, 2014.	
	50.	Inter Partes Review Case No. IPR2014-01369, Decision Denying Institution of Inter Partes Review 37 C.F.R. § 42.108, issued March 9, 2014.	
	51.	U.S. District Court Northern District of California, Case No. 4:13-CV-05889-YGR, Netlist, Inc. v. Smart Storage Systems, Inc., and Diablo Technologies, Inc., Smart Storage Systems, Inc.'s Invalidity Contentions, dated June 6, 2014	
	52.	U.S. District Court Northern District of California, Case No. 4:13-CV-05889-YGR, Netlist, Inc. v. Smart Storage Systems, Inc., and Diablo Technologies, Inc., Exhibits E.1-E.7 to "Smart Storage Systems, Inc.'s Invalidity Contentions," dated June 6, 2014.	
	53.	U.S. District Court Northern District of California, Case No. 4:13-CV-05889-YGR, Netlist, Inc. v. Smart Storage Systems, Inc., and Diablo Technologies, Inc., Diablo Technologies, Inc.'s Invalidity Contentions, dated June 6, 2014.	
	54.	U.S. District Court Northern District of California, Case No. 4:13-CV-05889-YGR, Netlist, Inc. v. Smart Storage Systems, Inc., and Diablo Technologies, Inc., Exhibits D-1 to D6 to "Diablo Technologies, Inc.'s Invalidity Contentions," dated June 6, 2014.	

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Electronic Patent Application Fee Transmittal

Application Number:	13971231
Filing Date:	20-Aug-2013
Title of Invention:	MEMORY MODULE WITH LOAD REDUCING CIRCUIT AND METHOD OF OPERATION
First Named Inventor/Applicant Name:	Jefferey C. Solomon
Filer:	Jamie Jie Zheng
Attorney Docket Number:	NETL.018P2C7

Filed as Small Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
Request for Continued Examination	2801	1	600	600
		Total in USD ($)		**600**

Electronic Acknowledgement Receipt

EFS ID:	21855848
Application Number:	13971231
International Application Number:	
Confirmation Number:	2072
Title of Invention:	MEMORY MODULE WITH LOAD REDUCING CIRCUIT AND METHOD OF OPERATION
First Named Inventor/Applicant Name:	Jefferey C. Solomon
Customer Number:	79141
Filer:	Jamie Jie Zheng
Filer Authorized By:	
Attorney Docket Number:	NETL.018P2C7
Receipt Date:	23-MAR-2015
Filing Date:	20-AUG-2013
Time Stamp:	21:03:25
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	$600
RAM confirmation Number	7971
Deposit Account	
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Request for Continued Examination (RCE)	2015-03-23_RCE_Transmittal_NETL018P2C7.pdf	697426 87ecfd2c1030c5e125d345e2670fe6eab087ea71	no	3
Warnings:					
Information:					
2	Amendment Submitted/Entered with Filing of CPA/RCE	2015-03-23_Amendment_RCE_NETL018P2C7.pdf	1920920 b9160d70ea1c1bbb73a476a7e8b3cd2b9305cbc0	no	11
Warnings:					
Information:					
3	Transmittal Letter	2015-03-23_IDS_Cover_NETL018P2C7.pdf	58297 126a2293f9cf6c83debf44e9b6914b9435c762fc	no	2
Warnings:					
Information:					
4	Information Disclosure Statement (IDS) Form (SB08)	2015-03-23_IDS_NETL018P2C7.pdf	154492 2fe4b9bd4d25775fa51eab82b33636a37896a60c	no	3
Warnings:					
Information:					
This is not an USPTO supplied IDS fillable form					
5	Non Patent Literature	preliminary_response_00882.pdf	2565336 09849b7c0ebed5bc8e16e07aa3c7f6bcc8622d43	no	60
Warnings:					
Information:					
6	Non Patent Literature	institution_decision_00882.pdf	1039322 bb3172e918ca8d935eb711d76a14c9d1e8926b30	no	34
Warnings:					
Information:					
7	Non Patent Literature	preliminary_response_00883.pdf	2381661 e987bf2019f017ddc8eedcc402681f32012a084e	no	56
Warnings:					
Information:					

8	Non Patent Literature	institution_decision_00883.pdf	916263 f37827a35a9c0307408f73270c78a89a47547468	no	27
Warnings:					
Information:					
9	Non Patent Literature	preliminary_response_01011.pdf	2875716 9b7e44610d7ab045113fa3e8561b4513572d3c64	no	62
Warnings:					
Information:					
10	Non Patent Literature	institution_decision_01011.pdf	903751 56c0309df8f7babb1cc544ee91b4036b8b1ddb9e	no	31
Warnings:					
Information:					
11	Non Patent Literature	Exhibit-3001.pdf	902406 e357e8723caa0a5b86ae1bc9abc1a080ef5e7493	no	63
Warnings:					
Information:					
12	Non Patent Literature	Exhibit-3002.pdf	2525056 7db2e7e7374fa995780d3676ac75e787c35f802c	no	133
Warnings:					
Information:					
13	Non Patent Literature	Exhibit-3003.pdf	283811 2fee627ab3350b948eff30ae20dc6c3ca5b05107	no	1
Warnings:					
Information:					
14	Non Patent Literature	Exhibit-3004.pdf	266334 3c5bba2f090727ef8b8212b3f715b448dad3c53a	no	1
Warnings:					
Information:					
15	Non Patent Literature	1986-McCluskey.pdf	2063520 65a221b1bdf55ee1a8405d71c7abad8727c74168	no	9
Warnings:					
Information:					
16	Non Patent Literature	2014-06-24_Petition_IPR2014-01029.pdf	995769 5f532e07581069892a1ca0f985e08ec811c3dade	no	64
Warnings:					
Information:					

17	Non Patent Literature	2014-06-24_Neuhauser_Decl_IPR2014-01029.pdf	3815549 306b26730565c7483c19319199c8b10dfeee8b33	no	173
Warnings:					
Information:					
18	Non Patent Literature	2014-07-23_Supp_Petition_IPR2014-01029.pdf	1058145 12b230bca6dbf7f1e89206150d7ba6fc10dbf2be	no	65
Warnings:					
Information:					
19	Non Patent Literature	2014-10-17_Prelim_Rsps_IPR2014-01029.pdf	3272498 de4f42dccc84d138ce64e88f09df639d62db5988	no	56
Warnings:					
Information:					
20	Non Patent Literature	2014-12-16_decision_denying_Institution.pdf	672087 c4cff0575c18a15433ae803328bede744a08e537	no	22
Warnings:					
Information:					
21	Non Patent Literature	2015-01-15_Rehearing_Request_01029.pdf	562731 0550b2bfc97abde738165c0c16f6e9dcaa9c7e6b	no	17
Warnings:					
Information:					
22	Non Patent Literature	2015-03-03_Rehearing_Decision_01029.pdf	123320 0dd30f650e976ea8d1b3fb3080171b7f25af65e7	no	7
Warnings:					
Information:					
23	Non Patent Literature	2014-09-22_Corrected_Petition_IPR2014-01369.pdf	912271 db81c4f9f7c8d687e8a242440bc7084a9a7c5c8c	no	66
Warnings:					
Information:					
24	Non Patent Literature	2014-09-22_Bagherzadeh_Decl_IPR2014-01369.pdf	9565317 7441d826caca8489a47bec3be76aa7cc703e7204	no	396
Warnings:					
Information:					
25	Non Patent Literature	2014-09-22_Exhibit-1013.pdf	1716301 f98f2639ee453b16d439416ea5935d6c108ad156	no	6
Warnings:					
Information:					

26	Non Patent Literature	2014-09-22_Exhibit-1014.pdf	2001462 e75d557231316ea02a8d5912e06741f6351e938e	no	5
Warnings:					
Information:					
27	Non Patent Literature	2015-03-09_Institution_Decision_01369.pdf	867692 0ac8262b507e89a629812f6a13849fa9c274493a	no	27
Warnings:					
Information:					
28	Non Patent Literature	2014-06-06_Smart_Storage_Invalidity_Contentions.pdf	2718276 dcea87ec2ecef9b8e701c8b6ab2647ff7c1ebce8	no	85
Warnings:					
Information:					
29	Non Patent Literature	SSS_Inv_Cont_Exh_E1-E4.pdf	19588217 36ef069bffef590c8a2c24abf3992f2abb1b5bd1	no	122
Warnings:					
Information:					
30	Non Patent Literature	SSS_Inv_Cont_Exh_E5-E7.pdf	14371632 9ca9401a280e47bc201747138cb24482a9f231ae	no	82
Warnings:					
Information:					
31	Non Patent Literature	20140606_DIABLO_Invalidity_Contentions.pdf	1703900 ed2e5f22373448111011661f8139988b2fca4464	no	41
Warnings:					
Information:					
32	Non Patent Literature	Diablo_EXHIBIT_D1-D6.pdf	4503878 846616191878fef35456447c0ccb84fc865a3ddf	no	145
Warnings:					
The page size in the PDF is too large. The pages should be 8.5 x 11 or A4. If this PDF is submitted, the pages will be resized upon entry into the Image File Wrapper and may affect subsequent processing					
Information:					
33	Fee Worksheet (SB06)	fee-info.pdf	30603 56b896e067a4117f2e01f5513d999f1f620efceb	no	2
Warnings:					
Information:					
			Total Files Size (in bytes):	88033959	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Applicant	:	Netlist, Inc.
App. No.	:	13/971,231
Filed	:	August 20, 2013
For	:	LOAD-REDUCING CIRCUIT FOR MEMORY MODULE
Examiner	:	BANSAL, GURTEJ
Art Unit	:	2139
Conf No.	:	2072

REQUEST AND AUTHORIZATION TO CHARGE DEPOSIT ACCOUNT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

The Commissioner is hereby requested and authorized to charge all required fees, fees under § 1.17, or all required extension of time fees, for any concurrent or future submission made in the above-referenced patent application to Deposit Account No. 50-5963.

Respectfully submitted,

Dated: March 23, 2015

/Jamie J. Zheng/ 51167

Jamie J. Zheng (Reg. No.)
Customer No. 79141
(650) 273-6008

Electronic Acknowledgement Receipt

EFS ID:	21856218
Application Number:	13971231
International Application Number:	
Confirmation Number:	2072
Title of Invention:	MEMORY MODULE WITH LOAD REDUCING CIRCUIT AND METHOD OF OPERATION
First Named Inventor/Applicant Name:	Jefferey C. Solomon
Customer Number:	79141
Filer:	Jamie Jie Zheng
Filer Authorized By:	
Attorney Docket Number:	NETL.018P2C7
Receipt Date:	23-MAR-2015
Filing Date:	20-AUG-2013
Time Stamp:	22:49:23
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Miscellaneous Incoming Letter	2015-03-23_DA_Request_NETL018P2C7.pdf	53215 1c236e37f901d9c79defd7b8b0adca02c4d3e04d	no	1
Warnings:					
Information:					

Total Files Size (in bytes):	53215

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/06 (09-11)
Approved for use through 1/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 13/971,231	Filing Date 08/20/2013	☐ To be Mailed

ENTITY: ☐ LARGE ☒ SMALL ☐ MICRO

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT **03/23/2015**

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	* 20	Minus	** 20	= 0	X $40 =	0
Independent (37 CFR 1.16(h))	* 2	Minus	***3	= 0	X $210 =	0
☐ Application Size Fee (37 CFR 1.16(s))						
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
					TOTAL ADD'L FEE	0

AMENDMENT

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =	
☐ Application Size Fee (37 CFR 1.16(s))						
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
					TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

LIE
/SHEILA D. CHAPMAN/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

79141 7590 04/02/2015

The Law Office of Jamie Zheng, Ph.D Esq.
P.O. Box 60573
Palo Alto, CA 94306

EXAMINER
BANSAL, GURTEJ

ART UNIT	PAPER NUMBER
2139	

DATE MAILED: 04/02/2015

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/971,231	08/20/2013	Jefferey C. Solomon	NETL.018P2C7	2072

TITLE OF INVENTION: MEMORY MODULE WITH LOAD REDUCING CIRCUIT AND METHOD OF OPERATION

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	SMALL	$480	$0	$0	$480	07/02/2015

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PTOL-85 (Rev. 02/11)

Samsung Electronics Co., Ltd.
Ex. 1052, p. 306

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

79141 7590 04/02/2015
The Law Office of Jamie Zheng, Ph.D Esq.
P.O. Box 60573
Palo Alto, CA 94306

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/971,231	08/20/2013	Jefferey C. Solomon	NETL.018P2C7	2072

TITLE OF INVENTION: MEMORY MODULE WITH LOAD REDUCING CIRCUIT AND METHOD OF OPERATION

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	SMALL	$480	$0	$0	$480	07/02/2015

EXAMINER	ART UNIT	CLASS-SUBCLASS
BANSAL, GURTEJ	2139	711-105000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
- ❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.
1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. The following fee(s) are submitted:
- ❑ Issue Fee
- ❑ Publication Fee (No small entity discount permitted)
- ❑ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**
- ❑ A check is enclosed.
- ❑ Payment by credit card. Form PTO-2038 is attached.
- ❑ The director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)
- ❑ Applicant certifying micro entity status. See 37 CFR 1.29 — NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
- ❑ Applicant asserting small entity status. See 37 CFR 1.27 — NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
- ❑ Applicant changing to regular undiscounted fee status. — NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

PTOL-85 Part B (10-13) Approved for use through 10/31/2013. OMB 0651-0033 U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Samsung Electronics Co., Ltd.
Ex. 1052, p. 307

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/971,231	08/20/2013	Jefferey C. Solomon	NETL.018P2C7	2072

79141 7590 04/02/2015

The Law Office of Jamie Zheng, Ph.D Esq.
P.O. Box 60573
Palo Alto, CA 94306

EXAMINER	
BANSAL, GURTEJ	
ART UNIT	PAPER NUMBER
2139	

DATE MAILED: 04/02/2015

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

Samsung Electronics Co., Ltd.
Ex. 1052, p. 308

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

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The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
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3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 13/971,231	Applicant(s) SOLOMON ET AL.	
	Examiner GURTEJ BANSAL	Art Unit 2139	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *RCE dated 03/23/2015* .
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on_____.
2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.
3. ☒ The allowed claim(s) is/are *11-30*. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov .
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☐ All b) ☐ Some *c) ☐ None of the:
   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date 03/23/2015
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
5. ☐ Examiner's Amendment/Comment
6. ☐ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/GURTEJ BANSAL/
Primary Examiner, Art Unit 2139

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Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13971231	SOLOMON ET AL.
	Examiner	**Art Unit**
	GURTEJ BANSAL	2139

CPC						
Symbol					**Type**	**Version**
G06F		12	/	00	F	2013-01-01
G11C		5	/	04	I	2013-01-01
G06F		13	/	00	I	2013-01-01
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CPC Combination Sets							
Symbol					**Type**	**Set**	**Ranking**	**Version**
			/					
			/					

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	20	
/GURTEJ BANSAL/ Primary Examiner.Art Unit 2139	03/30/2015	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	11	1

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Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13971231	SOLOMON ET AL.
	Examiner	**Art Unit**
	GURTEJ BANSAL	2139

US ORIGINAL CLASSIFICATION		INTERNATIONAL CLASSIFICATION										
CLASS	SUBCLASS	CLAIMED					NON-CLAIMED					
711	5	G	0	6	F	12 / 00 (2006.01.01)						

CROSS REFERENCE(S)					
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)				
711	147				

NONE (Assistant Examiner)	(Date)	**Total Claims Allowed:** 20	
/GURTEJ BANSAL/ Primary Examiner.Art Unit 2139 (Primary Examiner)	03/30/2015 (Date)	O.G. Print Claim(s) 11	O.G. Print Figure 1

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Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13971231	SOLOMON ET AL.
	Examiner	**Art Unit**
	GURTEJ BANSAL	2139

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☒ T.D. ☐ R.1.47

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
	1	9	17												
	2	3	18												
	3	10	19												
	4	4	20												
	5	11	21												
	6	12	22												
	7	15	23												
	8	16	24												
	9	17	25												
	10	18	26												
1	11	19	27												
2	12	13	28												
5	13	20	29												
6	14	14	30												
7	15														
8	16														

NONE (Assistant Examiner)	(Date)	**Total Claims Allowed:** 20	
/GURTEJ BANSAL/ Primary Examiner.Art Unit 2139 (Primary Examiner)	03/30/2015 (Date)	O.G. Print Claim(s) 11	O.G. Print Figure 1

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EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	25	rank same (DQ with DQS) with isolat$3	US-PGPUB; USPAT	OR	ON	2015/03/30 14:21
L2	29	multiplex$3 with DQS same delay$3 with data with (signals lines) and rank	US-PGPUB; USPAT	OR	ON	2015/03/30 14:23
L3	1	"5388240".pn.	US-PGPUB; USPAT	OR	ON	2015/03/30 14:24
L4	18	"5388240".pn. "5463590".pn. "5953280".pn. "6188641".pn. "6205516".pn. "64804393".pn. "7464225".pn. "7865674".pn. "8089795".pn. "8130560".pn. "8189328".pn. "8233303".pn. "8250295".pn. "8417870".pn. "8516185".pn. "8516188".pn. "8756364".pn. "20070058409".pn. "20080104352".pn. "20080104352".pn.	US-PGPUB; USPAT	OR	ON	2015/03/30 14:28
L5	69	chip$1select same rank and DQ and DQS	US-PGPUB; USPAT	OR	ON	2015/03/30 14:31
L6	10	rank same (DQ with DQS) with (mux multiplexer)	US-PGPUB; USPAT	OR	ON	2015/03/30 14:32
S1	4386	711/5.ccls. 711/147.ccls.	US-PGPUB; USPAT	OR	OFF	2013/12/02 23:37
S2	4481	DQS	US-PGPUB; USPAT	OR	OFF	2013/12/02 23:38
S3	88990	DS	US-PGPUB; USPAT	OR	OFF	2013/12/02 23:38
S4	32759	DQ	US-PGPUB; USPAT	OR	OFF	2013/12/02 23:38
S5	3171	S2 and S4	US-PGPUB; USPAT	OR	OFF	2013/12/02 23:38
S6	134822	rank	US-PGPUB; USPAT	OR	ON	2013/12/02 23:38
S7	329	S5 and S6	US-PGPUB; USPAT	OR	ON	2013/12/02 23:38
S8	201	US-4218740-$.DID. OR US-4368515-$.DID. OR US-4392212-$.DID. OR US-	US-PGPUB;	OR	OFF	2013/12/03 00:02

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		4633429-$.DID. OR US-4670748-$.DID. OR US-4706214-$.DID. OR US-4866603-$.DID. OR US-4958322-$.DID. OR US-4961172-$.DID. OR US-4961204-$.DID. OR US-4980850-$.DID. OR US-5247643-$.DID. OR US-5272664-$.DID. OR US-5345412-$.DID. OR US-5357478-$.DID. OR US-5388072-$.DID. OR US-5392252-$.DID. OR US-5426753-$.DID. OR US-5483497-$.DID. OR US-5485589-$.DID. OR US-5495435-$.DID. OR US-5513135-$.DID. OR US-5532954-$.DID. OR US-5541448-$.DID. OR US-5572691-$.DID. OR US-5581498-$.DID. OR US-5590071-$.DID. OR US-5602999-$.DID. OR US-5638534-$.DID. OR US-5655153-$.DID. OR US-5699542-$.DID. OR US-5702984-$.DID. OR US-5703826-$.DID. OR US-5745914-$.DID. OR US-5764590-$.DID. OR US-5784705-$.DID. OR US-5802395-$.DID. OR US-5805520-$.DID. OR US-5822251-$.DID. OR US-5909388-$.DID. OR US-5926827-$.DID. OR US-5926839-$.DID. OR US-5953215-$.DID. OR US-5958025-$.DID. OR US-5959930-$.DID. OR US-5963464-$.DID. OR US-5966736-$.DID. OR US-5974493-$.DID. OR US-6018787-$.DID. OR US-6044032-$.DID. OR US-6070217-$.DID. OR US-6070227-$.DID. OR US-6097652-$.DID. OR US-6108745-$.DID. OR US-6115278-$.DID. OR US-6134638-$.DID. OR US-6151271-$.DID. OR US-6154418-$.DID. OR US-6154419-$.DID. OR US-6185654-$.DID. OR US-6209074-$.DID. OR US-6226709-$.DID. OR US-6226736-$.DID. OR US-6233650-$.DID. OR US-6247088-$.DID. OR US-6317352-$.DID. OR US-6349051-$.DID. OR US-6400637-$.DID. OR US-6408356-$.DID. OR US-6414868-$.DID. OR US-6415374-$.DID. OR US-6438062-$.DID. OR US-6446158-$.DID. OR US-6446184-$.DID. OR US-6453381-$.DID. OR US-6470417-$.DID. OR US-6487102-$.DID. OR US-6502161-$.DID. OR US-6518794-$.DID. OR US-6526473-$.DID. OR US-6530007-$.DID. OR US-6530033-$.DID. OR US-6553450-$.DID. OR US-6618320-$.DID. OR US-6621496-$.DID. OR US-6625081-$.DID. OR US-6625687-$.DID. OR US-6636935-$.DID. OR US-6646949-$.DID. OR US-6658509-$.DID. OR US-6674684-$.DID. OR US-6681301-$.DID. OR US-6683372-$.DID. OR US-6697888-$.DID. OR US-6705877-$.DID. OR US-6717885-$.DID. OR US-6721843-$.DID. OR US-6721860-$.DID. OR US-6738880-$.DID. OR US-6742098-$.DID. OR US-6754797-$.DID. OR US-6785189-$.DID. OR US-6788592-$.DID. OR US-6807125-$.DID. OR US-6807650-$.DID. OR US-6813196-$.DID. OR US-6832284-$.DID. OR US-6834014-$.DID. OR US-6854042-$.DID. OR US-6880094-$.DID.	USPAT; USOCR					

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		OR US-6889304-$.DID. OR US-6912615-$.DID. OR US-6912628-$.DID. OR US-6925028-$.DID. OR US-6944694-$.DID. OR US-6950366-$.DID. OR US-6954281-$.DID. OR US-6961281-$.DID. OR US-6981089-$.DID. OR US-6982892-$.DID. OR US-6982893-$.DID. OR US-6990043-$.DID. OR US-6996686-$.DID. OR US-7007130-$.DID. OR US-7007175-$.DID. OR US-7046538-$.DID. OR US-7047361-$.DID. OR US-7054179-$.DID. OR US-7065626-$.DID. OR US-7072231-$.DID. OR US-7073041-$.DID. OR US-7078793-$.DID. OR US-7120727-$.DID. OR US-7124260-$.DID. OR US-7127584-$.DID. OR US-7130952-$.DID. OR US-7133960-$.DID. OR US-7133972-$.DID. OR US-7142461-$.DID. OR US-7149841-$.DID. OR US-7167967-$.DID. OR US-7181591-$.DID. OR US-7200021-$.DID. OR US-7227910-$.DID. OR US-7266639-$.DID. OR US-7272709-$.DID. OR US-7281079-$.DID. OR US-7286436-$.DID. OR US-7289386-$.DID. OR US-7346750-$.DID. OR US-7356639-$.DID. OR US-7370238-$.DID. OR US-7437591-$.DID. OR US-7461182-$.DID. OR US-7471538-$.DID. OR US-7532537-$.DID. OR US-7619912-$.DID. OR US-7636274-$.DID. OR US-7864627-$.DID. OR US-7881150-$.DID. OR US-7916574-$.DID. OR US-8001434-$.DID. OR US-20010003198-$.DID. OR US-20010050857-$.DID. OR US-20010052057-$.DID. OR US-20020088633-$.DID. OR US-20030063514-$.DID. OR US-20030090359-$.DID. OR US-20030090879-$.DID. OR US-20030191995-$.DID. OR US-20030210575-$.DID. OR US-20040000708-$.DID. OR US-20040037158-$.DID. OR US-20040201968-$.DID. OR US-20050036378-$.DID. OR US-20050154820-$.DID. OR US-20050281096-$.DID. OR US-20060044860-$.DID. OR US-20060117152-$.DID. OR US-20060126369-$.DID. OR US-20060129755-$.DID. OR US-20060179206-$.DID. OR US-20060259711-$.DID. OR US-20060262586-$.DID. OR US-20060267172-$.DID. OR US-20060277355-$.DID. OR US-20080162790-$.DID. OR US-20090103387-$.DID. OR US-20100070690-$.DID. OR US-20100091540-$.DID. OR US-20100128507-$.DID. OR US-20110016250-$.DID. OR US-20110016269-$.DID. OR US-20110090749-$.DID. OR US-20110125966-$.DID. OR WO-1992002879-				

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S9	1184	multiplex$3 with (DQS and DQ)	US-PGPUB; USPAT	OR	ON	2013/12/03 00:07
S10	359	multiplex$3 with (DQS and DQ) with delay$3	US-PGPUB; USPAT	OR	ON	2013/12/03 00:08
S11	850	multiplex$3 with DQS and delay with delay$3	US-PGPUB; USPAT	OR	ON	2013/12/03 00:12
S12	562	multiplex$3 with DQS and DQ with delay$3	US-PGPUB; USPAT	OR	ON	2013/12/03 00:12
S13	401	multiplex$3 with DQS same DQ with delay$3	US-PGPUB; USPAT	OR	ON	2013/12/03 00:12
S14	0	13/287042.app.	US-PGPUB; USPAT	OR	ON	2013/12/03 00:25
S15	0	13/287042.ap.	US-PGPUB; USPAT	OR	ON	2013/12/03 00:25
S16	0	"13287042".ap.	US-PGPUB; USPAT	OR	ON	2013/12/03 00:25
S17	0	"13287042".app.	US-PGPUB; USPAT	OR	ON	2013/12/03 00:25
S18	294	multiplex$3 with DQS same delay$3 with data with signals	US-PGPUB; USPAT	OR	ON	2013/12/03 00:28
S19	307	multiplex$3 with DQS same delay$3 with data with (signals lines)	US-PGPUB; USPAT	OR	ON	2013/12/03 00:28
S20	9	multiplex$3 with DQS same delay$3 with data with (signals lines) same2 rank	US-PGPUB; USPAT	OR	ON	2013/12/03 00:28
S21	26	multiplex$3 with DQS same delay$3 with data with (signals lines) and rank	US-PGPUB; USPAT	OR	ON	2013/12/03 00:29
S22	238	multiplex$3 with DQS same delay$3 with data with (signals lines) same memory	US-PGPUB; USPAT	OR	ON	2013/12/03 00:30
S23	347	isolat$3 with DQ with DQS	US-PGPUB; USPAT	OR	ON	2013/12/03 00:47
S24	21	isolat$3 with DQ with DQS same Rank	US-PGPUB; USPAT	OR	ON	2013/12/03 00:47
S25	1353	DQS with select$3 with (memory rank)	US-	OR	ON	2013/12/03

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			PGPUB; USPAT			00:50
S26	54	chip$1select with rank and DQ and DQS	US-PGPUB; USPAT	OR	ON	2013/12/03 18:25
S27	56	chip$1select same rank and DQ and DQS	US-PGPUB; USPAT	OR	ON	2013/12/03 18:26
S28	61	chip$1select and rank and DQ and DQS	US-PGPUB; USPAT	OR	ON	2013/12/03 18:27
S29	5	rank with DQ with DQS with low	US-PGPUB; USPAT	OR	ON	2013/12/03 18:39
S30	300	rank with DQ with DQS	US-PGPUB; USPAT	OR	ON	2013/12/03 18:40
S31	82	rank and (DQ with DQS) with off	US-PGPUB; USPAT	OR	ON	2013/12/03 19:03
S32	271	rank and (DQ with DQS) with high	US-PGPUB; USPAT	OR	ON	2013/12/03 19:07
S33	29	rank with (DQ with DQS) with high	US-PGPUB; USPAT	OR	ON	2013/12/03 19:07
S34	1	"6873533".pn.	US-PGPUB; USPAT	OR	ON	2013/12/03 19:07
S35	7	rank with (DQ with DQS) with terminat$3	US-PGPUB; USPAT	OR	ON	2013/12/03 19:10
S36	20	rank with (DQ with DQS) with isolat$3	US-PGPUB; USPAT	OR	ON	2013/12/03 19:11
S37	21	rank same (DQ with DQS) with isolat$3	US-PGPUB; USPAT	OR	ON	2013/12/03 19:11
S38	57	rank same (DQ with DQS) with high	US-PGPUB; USPAT	OR	ON	2013/12/03 19:11
S39	7	rank same (DQ with DQS) with (mux multiplexer)	US-PGPUB; USPAT	OR	ON	2013/12/03 19:15
S40	37	rank and (DQ with DQS) with (mux multiplexer)	US-PGPUB; USPAT	OR	ON	2013/12/03 19:16
S41	1040	(DQ with DQS) with (mux multiplexer)	US-PGPUB; USPAT	OR	ON	2013/12/03 19:21
S42	1024	(DQ with DQS) with (mux multiplexer) and memory	US-PGPUB; USPAT	OR	ON	2013/12/03 19:21
S43	634	(DQ with DQS) with (mux multiplexer) same memory	US-PGPUB; USPAT	OR	ON	2013/12/03 19:21
S44	231	(DQ with DQS) with (mux multiplexer)	US-	OR	ON	2013/12/03

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		with memory	PGPUB; USPAT			19:21
S45	1	"20040098428".pn.	US-PGPUB; USPAT	OR	ON	2013/12/03 19:40
S46	1	"20040098528".pn.	US-PGPUB; USPAT	OR	ON	2013/12/03 19:41
S47	1	"20030070052".pn.	US-PGPUB; USPAT	OR	ON	2013/12/03 19:42
S48	1	"20050047250".pn.	US-PGPUB; USPAT	OR	ON	2013/12/03 20:07
S49	1599	G06F12/0607.cpc. G06F12/0813.cpc.	US-PGPUB; USPAT	OR	OFF	2013/12/20 11:11
S50	2437	latency with memory adj controller with memory	US-PGPUB; USPAT	OR	ON	2014/04/04 14:15
S51	59	latency with memory adj controller with (measur$3 test$3)	US-PGPUB; USPAT	OR	ON	2014/04/04 14:16
S52	22	rank same (DQ with DQS) with isolat$3	US-PGPUB; USPAT	OR	ON	2014/04/04 15:16
S53	22	isolat$3 with DQ with DQS same Rank	US-PGPUB; USPAT	OR	ON	2014/04/04 15:29
S54	26	multiplex$3 with DQS same delay$3 with data with (signals lines) and rank	US-PGPUB; USPAT	OR	ON	2014/04/04 15:29
S55	1	"6553450".pn.	US-PGPUB; USPAT	OR	ON	2014/04/04 15:33
S56	1	"6742098".pn.	US-PGPUB; USPAT	OR	ON	2014/04/04 15:48
S60	644	isolat$3 with load with memory	US-PGPUB; USPAT	OR	ON	2014/04/04 15:58
S61	46	isolat$3 with load with memory with controller	US-PGPUB; USPAT	OR	ON	2014/04/04 15:58
S62	28	US-5345412-$.DID. OR US-5537584-$.DID. OR US-5617559-$.DID. OR US-5649159-$.DID. OR US-5717851-$.DID. OR US-5724604-$.DID. OR US-5729716-$.DID. OR US-5784705-$.DID. OR US-5802541-$.DID. OR US-5973392-$.DID. OR US-6173357-$.DID. OR US-6260127-$.DID. OR US-6446158-$.DID. OR US-6553449-$.DID. OR US-6618791-$.DID. OR US-6717855-$.DID. OR US-6788592-$.DID. OR US-6948084-$.DID. OR US-7130308-$.DID. OR US-7133960-$.DID. OR US-7379361-$.DID. OR US-20050010737-$.DID. OR US-	US-PGPUB; USPAT	OR	ON	2014/05/05 00:39

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S63	2355572	read$only with non$1volatile with main memory	US-PGPUB; USPAT	OR	OFF	2014/05/08 19:12
S64	2126	read$only with non$1volatile with main with memory	US-PGPUB; USPAT	OR	OFF	2014/05/08 19:12
S65	1	"20080080261".pn.	US-PGPUB; USPAT	OR	OFF	2014/05/11 20:14
S66	4529	711/5.ccls. 711/147.ccls.	US-PGPUB; USPAT	OR	OFF	2014/05/15 16:09
S67	3613	DQS and DQ	US-PGPUB; USPAT	OR	OFF	2015/01/01 23:10
S68	1574	DQS and DQ with (coupl$3 connect$3 isolat$3 select$3)	US-PGPUB; USPAT	OR	OFF	2015/01/01 23:10
S69	1309	DQS and DQ with (connect$3 isolat$3 select$3)	US-PGPUB; USPAT	OR	OFF	2015/01/01 23:11
S70	1108	DQS and DQ with (coupl$3 isolat$3 select$3)	US-PGPUB; USPAT	OR	OFF	2015/01/01 23:11
S71	569	DQS and DQ with (coupl$3 isolat$3)	US-PGPUB; USPAT	OR	OFF	2015/01/01 23:12
S72	149	DQS and DQ with (decoupl$3 isolat$3)	US-PGPUB; USPAT	OR	OFF	2015/01/01 23:15
S73	149	DQS and DQ with (decoupl$3 isolat$3 detach$3)	US-PGPUB; USPAT	OR	OFF	2015/01/01 23:17
S74	167	DQS and DQ with (decoupl$3 isolat$3 detach$3 disconnect$3)	US-PGPUB; USPAT	OR	OFF	2015/01/01 23:17
S75	20	DQS and DQ with (disconnect$3)	US-PGPUB; USPAT	OR	OFF	2015/01/01 23:18
S76	3	"20010008006".pn. "20050257109".pn. "20070070669".pn.	US-PGPUB; USPAT	OR	OFF	2015/01/02 00:02
S77	3	"6747887".pn. "7093066".pn. "6832303".pn.	US-PGPUB; USPAT	OR	OFF	2015/01/02 00:03

EAST Search History (Interference)

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L7	1049	G06F12/0607.cpc. G06F12/0813.cpc.	USPAT; UPAD	OR	OFF	2015/03/30 14:34
L8	181517	isolat$3.clm.	USPAT;	OR	OFF	2015/03/30

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			UPAD			14:34
L9	5909	isolates.clm.	USPAT; UPAD	OR	OFF	2015/03/30 14:34
L10	0	L7 and L9	USPAT; UPAD	OR	OFF	2015/03/30 14:34
S57	3448	711/5.ccls. 711/147.ccls.	USPAT; UPAD	OR	OFF	2014/04/04 15:50
S58	171076	isolat$3.clm.	USPAT; UPAD	OR	OFF	2014/04/04 15:52
S59	45	S57 and S58	USPAT; UPAD	OR	OFF	2014/04/04 15:52
S78	3626	711/5.ccls. 711/147.ccls.	USPAT; UPAD	OR	OFF	2015/01/02 00:11
S79	5815	isolates.clm.	USPAT; UPAD	OR	OFF	2015/01/02 00:12
S80	0	S78 and "L143"	USPAT; UPAD	OR	OFF	2015/01/02 00:12
S81	7	S78 and S79	USPAT; UPAD	OR	OFF	2015/01/02 00:12
S82	0	S78 and S79 and DQS.clm.	USPAT; UPAD	OR	OFF	2015/01/02 00:15

3/ 30/ 2015 2:34:48 PM
C:\ Users\ gbansal\ Documents\ EAST\ Workspaces\ 13971231.wsp

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Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13971231	SOLOMON ET AL.
	Examiner	Art Unit
	GURTEJ BANSAL	2189

CPC- SEARCHED		
Symbol	Date	Examiner
G06F 12/0607	03/30/2015	GB
G06F 12/0813	03/30/2015	GB

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner
711	5; 147	05/15/2014	GB

SEARCH NOTES		
Search Notes	Date	Examiner
Text Search in EAST (See Attached)	05/15/2014	GB
NPL Search in Google Scholar (See Attached)	05/15/2014	GB
Inventor Search in eDAN	05/15/2014	GB
Consulted Alex Sofocleous (SPE)	05/15/2014	GB
Updated Text Search in EAST (See Attached)	12/16/2014	GB
Updated Text Search in EAST (See Attached)	01/02/2015	GB
UPdated NPL Search in Google Scholar (See Attached)	01/02/2015	GB
Updated Text Search in EAST (See Attached)	03/30/2015	GB
Updated NPL Search in Google Scholar (See Attached)	03/30/2015	GB

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner
711	5; 147	01/02/2015	GB
	G06F 12/0813		

/GURTEJ BANSAL/ Examiner.Art Unit 2189	

EAST Search History

EAST Search History (Prior Art)

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L1	25	rank same (DQ with DQS) with isolat$3	US-PGPUB; USPAT	OR	ON	2015/03/30 14:21
L2	29	multiplex$3 with DQS same delay$3 with data with (signals lines) and rank	US-PGPUB; USPAT	OR	ON	2015/03/30 14:23
L3	1	"5388240".pn.	US-PGPUB; USPAT	OR	ON	2015/03/30 14:24
L4	18	"5388240".pn. "5463590".pn. "5953280".pn. "6188641".pn. "6205516".pn. "64804393".pn. "7464225".pn. "7865674".pn. "8089795".pn. "8130560".pn. "8189328".pn. "8233303".pn. "8250295".pn. "8417870".pn. "8516185".pn. "8516188".pn. "8756364".pn. "20070058409".pn. "20080104352".pn. "20080104352".pn.	US-PGPUB; USPAT	OR	ON	2015/03/30 14:28
L5	69	chip$1select same rank and DQ and DQS	US-PGPUB; USPAT	OR	ON	2015/03/30 14:31
L6	10	rank same (DQ with DQS) with (mux multiplexer)	US-PGPUB; USPAT	OR	ON	2015/03/30 14:32
S1	4386	711/5.ccls. 711/147.ccls.	US-PGPUB; USPAT	OR	OFF	2013/12/02 23:37
S2	4481	DQS	US-PGPUB; USPAT	OR	OFF	2013/12/02 23:38
S3	88990	DS	US-PGPUB; USPAT	OR	OFF	2013/12/02 23:38
S4	32759	DQ	US-PGPUB; USPAT	OR	OFF	2013/12/02 23:38
S5	3171	S2 and S4	US-PGPUB; USPAT	OR	OFF	2013/12/02 23:38
S6	134822	rank	US-PGPUB; USPAT	OR	ON	2013/12/02 23:38
S7	329	S5 and S6	US-PGPUB; USPAT	OR	ON	2013/12/02 23:38
S8	201	US-4218740-$.DID. OR US-4368515-$.DID. OR US-4392212-$.DID. OR US-	US-PGPUB;	OR	OFF	2013/12/03 00:02

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S9	1184	multiplex$3 with (DQS and DQ)	US-PGPUB; USPAT	OR	ON	2013/12/03 00:07
S10	359	multiplex$3 with (DQS and DQ) with delay$3	US-PGPUB; USPAT	OR	ON	2013/12/03 00:08
S11	850	multiplex$3 with DQS and delay with delay$3	US-PGPUB; USPAT	OR	ON	2013/12/03 00:12
S12	562	multiplex$3 with DQS and DQ with delay$3	US-PGPUB; USPAT	OR	ON	2013/12/03 00:12
S13	401	multiplex$3 with DQS same DQ with delay$3	US-PGPUB; USPAT	OR	ON	2013/12/03 00:12
S14	0	13/287042.app.	US-PGPUB; USPAT	OR	ON	2013/12/03 00:25
S15	0	13/287042.ap.	US-PGPUB; USPAT	OR	ON	2013/12/03 00:25
S16	0	"13287042".ap.	US-PGPUB; USPAT	OR	ON	2013/12/03 00:25
S17	0	"13287042".app.	US-PGPUB; USPAT	OR	ON	2013/12/03 00:25
S18	294	multiplex$3 with DQS same delay$3 with data with signals	US-PGPUB; USPAT	OR	ON	2013/12/03 00:28
S19	307	multiplex$3 with DQS same delay$3 with data with (signals lines)	US-PGPUB; USPAT	OR	ON	2013/12/03 00:28
S20	9	multiplex$3 with DQS same delay$3 with data with (signals lines) same2 rank	US-PGPUB; USPAT	OR	ON	2013/12/03 00:28
S21	26	multiplex$3 with DQS same delay$3 with data with (signals lines) and rank	US-PGPUB; USPAT	OR	ON	2013/12/03 00:29
S22	238	multiplex$3 with DQS same delay$3 with data with (signals lines) same memory	US-PGPUB; USPAT	OR	ON	2013/12/03 00:30
S23	347	isolat$3 with DQ with DQS	US-PGPUB; USPAT	OR	ON	2013/12/03 00:47
S24	21	isolat$3 with DQ with DQS same Rank	US-PGPUB; USPAT	OR	ON	2013/12/03 00:47
S25	1353	DQS with select$3 with (memory rank)	US-	OR	ON	2013/12/03

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			PGPUB; USPAT			00:50
S26	54	chip$1select with rank and DQ and DQS	US-PGPUB; USPAT	OR	ON	2013/12/03 18:25
S27	56	chip$1select same rank and DQ and DQS	US-PGPUB; USPAT	OR	ON	2013/12/03 18:26
S28	61	chip$1select and rank and DQ and DQS	US-PGPUB; USPAT	OR	ON	2013/12/03 18:27
S29	5	rank with DQ with DQS with low	US-PGPUB; USPAT	OR	ON	2013/12/03 18:39
S30	300	rank with DQ with DQS	US-PGPUB; USPAT	OR	ON	2013/12/03 18:40
S31	82	rank and (DQ with DQS) with off	US-PGPUB; USPAT	OR	ON	2013/12/03 19:03
S32	271	rank and (DQ with DQS) with high	US-PGPUB; USPAT	OR	ON	2013/12/03 19:07
S33	29	rank with (DQ with DQS) with high	US-PGPUB; USPAT	OR	ON	2013/12/03 19:07
S34	1	"6873533".pn.	US-PGPUB; USPAT	OR	ON	2013/12/03 19:07
S35	7	rank with (DQ with DQS) with terminat$3	US-PGPUB; USPAT	OR	ON	2013/12/03 19:10
S36	20	rank with (DQ with DQS) with isolat$3	US-PGPUB; USPAT	OR	ON	2013/12/03 19:11
S37	21	rank same (DQ with DQS) with isolat$3	US-PGPUB; USPAT	OR	ON	2013/12/03 19:11
S38	57	rank same (DQ with DQS) with high	US-PGPUB; USPAT	OR	ON	2013/12/03 19:11
S39	7	rank same (DQ with DQS) with (mux multiplexer)	US-PGPUB; USPAT	OR	ON	2013/12/03 19:15
S40	37	rank and (DQ with DQS) with (mux multiplexer)	US-PGPUB; USPAT	OR	ON	2013/12/03 19:16
S41	1040	(DQ with DQS) with (mux multiplexer)	US-PGPUB; USPAT	OR	ON	2013/12/03 19:21
S42	1024	(DQ with DQS) with (mux multiplexer) and memory	US-PGPUB; USPAT	OR	ON	2013/12/03 19:21
S43	634	(DQ with DQS) with (mux multiplexer) same memory	US-PGPUB; USPAT	OR	ON	2013/12/03 19:21
S44	231	(DQ with DQS) with (mux multiplexer)	US-	OR	ON	2013/12/03

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		with memory	PGPUB; USPAT			19:21
S45	1	"20040098428".pn.	US-PGPUB; USPAT	OR	ON	2013/12/03 19:40
S46	1	"20040098528".pn.	US-PGPUB; USPAT	OR	ON	2013/12/03 19:41
S47	1	"20030070052".pn.	US-PGPUB; USPAT	OR	ON	2013/12/03 19:42
S48	1	"20050047250".pn.	US-PGPUB; USPAT	OR	ON	2013/12/03 20:07
S49	1599	G06F12/0607.cpc. G06F12/0813.cpc.	US-PGPUB; USPAT	OR	OFF	2013/12/20 11:11
S50	2437	latency with memory adj controller with memory	US-PGPUB; USPAT	OR	ON	2014/04/04 14:15
S51	59	latency with memory adj controller with (measur$3 test$3)	US-PGPUB; USPAT	OR	ON	2014/04/04 14:16
S52	22	rank same (DQ with DQS) with isolat$3	US-PGPUB; USPAT	OR	ON	2014/04/04 15:16
S53	22	isolat$3 with DQ with DQS same Rank	US-PGPUB; USPAT	OR	ON	2014/04/04 15:29
S54	26	multiplex$3 with DQS same delay$3 with data with (signals lines) and rank	US-PGPUB; USPAT	OR	ON	2014/04/04 15:29
S55	1	"6553450".pn.	US-PGPUB; USPAT	OR	ON	2014/04/04 15:33
S56	1	"6742098".pn.	US-PGPUB; USPAT	OR	ON	2014/04/04 15:48
S60	644	isolat$3 with load with memory	US-PGPUB; USPAT	OR	ON	2014/04/04 15:58
S61	46	isolat$3 with load with memory with controller	US-PGPUB; USPAT	OR	ON	2014/04/04 15:58
S62	28	US-5345412-$.DID. OR US-5537584-$.DID. OR US-5617559-$.DID. OR US-5649159-$.DID. OR US-5717851-$.DID. OR US-5724604-$.DID. OR US-5729716-$.DID. OR US-5784705-$.DID. OR US-5802541-$.DID. OR US-5973392-$.DID. OR US-6173357-$.DID. OR US-6260127-$.DID. OR US-6446158-$.DID. OR US-6553449-$.DID. OR US-6618791-$.DID. OR US-6717855-$.DID. OR US-6788592-$.DID. OR US-6948084-$.DID. OR US-7130308-$.DID. OR US-7133960-$.DID. OR US-7379361-$.DID. OR US-20050010737-$.DID. OR US-	US-PGPUB; USPAT	OR	ON	2014/05/05 00:39

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S63	2355572	read$only with non$1volatile with main memory	US-PGPUB; USPAT	OR	OFF	2014/05/08 19:12
S64	2126	read$only with non$1volatile with main with memory	US-PGPUB; USPAT	OR	OFF	2014/05/08 19:12
S65	1	"20080080261".pn.	US-PGPUB; USPAT	OR	OFF	2014/05/11 20:14
S66	4529	711/5.ccls. 711/147.ccls.	US-PGPUB; USPAT	OR	OFF	2014/05/15 16:09
S67	3613	DQS and DQ	US-PGPUB; USPAT	OR	OFF	2015/01/01 23:10
S68	1574	DQS and DQ with (coupl$3 connect$3 isolat$3 select$3)	US-PGPUB; USPAT	OR	OFF	2015/01/01 23:10
S69	1309	DQS and DQ with (connect$3 isolat$3 select$3)	US-PGPUB; USPAT	OR	OFF	2015/01/01 23:11
S70	1108	DQS and DQ with (coupl$3 isolat$3 select$3)	US-PGPUB; USPAT	OR	OFF	2015/01/01 23:11
S71	569	DQS and DQ with (coupl$3 isolat$3)	US-PGPUB; USPAT	OR	OFF	2015/01/01 23:12
S72	149	DQS and DQ with (decoupl$3 isolat$3)	US-PGPUB; USPAT	OR	OFF	2015/01/01 23:15
S73	149	DQS and DQ with (decoupl$3 isolat$3 detach$3)	US-PGPUB; USPAT	OR	OFF	2015/01/01 23:17
S74	167	DQS and DQ with (decoupl$3 isolat$3 detach$3 disconnect$3)	US-PGPUB; USPAT	OR	OFF	2015/01/01 23:17
S75	20	DQS and DQ with (disconnect$3)	US-PGPUB; USPAT	OR	OFF	2015/01/01 23:18
S76	3	"20010008006".pn. "20050257109".pn. "20070070669".pn.	US-PGPUB; USPAT	OR	OFF	2015/01/02 00:02
S77	3	"6747887".pn. "7093066".pn. "6832303".pn.	US-PGPUB; USPAT	OR	OFF	2015/01/02 00:03

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S57	3448	711/5.ccls. 711/147.ccls.	USPAT; UPAD	OR	OFF	2014/04/04 15:50
S58	171076	isolat$3.clm.	USPAT;	OR	OFF	2014/04/04

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			UPAD			15:52
S59	45	S57 and S58	USPAT; UPAD	OR	OFF	2014/04/04 15:52
S78	3626	711/5.ccls. 711/147.ccls.	USPAT; UPAD	OR	OFF	2015/01/02 00:11
S79	5815	isolates.clm.	USPAT; UPAD	OR	OFF	2015/01/02 00:12
S80	0	S78 and "L143"	USPAT; UPAD	OR	OFF	2015/01/02 00:12
S81	7	S78 and S79	USPAT; UPAD	OR	OFF	2015/01/02 00:12
S82	0	S78 and S79 and DQS.clm.	USPAT; UPAD	OR	OFF	2015/01/02 00:15

3/ 30/ 2015 2:33:35 PM
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Sheet 1 of 3

Complete if Known	
Application Number	13/971,231
Filing Date	August 20, 2013
First Named Inventor	Jayesh R. Bhakta
Art Unit	2139
Examiner Name	Unknown
Attorney Docket Number	NETL.018P2C7

US PATENT DOCUMENTS

Examiner Initials *	Cite No. [1]	Document Number / Number-Kind Code [2] (if known)	Publication Date (MM-DD-YYYY)	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	1.	5388240	02-01-1995	IBM Corporation	
	2.	5463590	10-31-1995	Watanabe	
	3.	5953280	09-14-1999	Matsui	
	4.	6188641	02-13-2001	Uchida	
	5.	6205516	03-20-2001	Usami	
	6.	6480439	11-12-2002	Tokutome et al.	
	7.	7464225	12-09-2008	Tsern	
	8.	7865674	01-04-2011	Gower et al.	
	9.	8089795	01-03-2012	Rajan	
	10.	8130560	03-06-2012	Rajan	
	11.	8189328	05-29-2012	Kanapathippillai	
	12.	8233303	07-31-2012	Best	
	13.	8250295	08-21-2012	Amidi et al.	
	14.	8417870	04-09-2013	Lee et al.	
	15.	8516185	08-20-2013	Lee et al.	
	16.	8516188	08-20-2013	Solomon et al.	
	17.	8756364	06-17-2014	Bhakta et al.	
	18.	20070058409	03-15-2007	Ruckerbauer	
	19.	20080104352	05-01-2008	Talbot	
	20.	20080104352	05-01-2008	Talbot	
	21.	RE36229	06-15-1999	Cady	

US PATENT APPLICATIONS

Examiner Initials *	Cite No. [1]	Application Number	Filing Date (MM-DD-YYYY)	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	22.	13/411,344	3/2/2012	Lee	Entire Prosecution History
	23.	13/970,606	8/20/2013	Netlist, Inc.	Entire Prosecution History
	24.	13/971,231	8/20/2013	Netlist, Inc.	Entire Prosecution History
	25.	14/229,844	3/29/2014	Netlist, Inc.	Entire Prosecution History
	26.	14/324,990	7/7/2014	Netlist, Inc.	Entire Prosecution History
	27.	14/337,168	7/21/2014	Netlist, Inc.	Entire Prosecution History

NON PATENT LITERATURE DOCUMENTS

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Filing Date	August 20, 2013
First Named Inventor	Jayesh R. Bhakta
Art Unit	2139
Examiner Name	Unknown
Attorney Docket Number	NETL.018P2C7

Sheet 2 of 3

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	28.	Inter Partes Review of U.S. Patent No. 7,881,150, IPR Case No. IPR2014-00882, Patent Owner's Preliminary Response Pursuant to 37 C.F.R. § 42.107, filed October 7, 2014	
	29.	Inter Partes Review of U.S. Patent No. 7,881,150, IPR Case No. IPR2014-00882, Decision – Institution of Inter Partes Review 37 C.F.R. § 42.108, issued December 16, 2014	
	30.	Inter Partes Review of U.S. Patent No. 8,081,536, IPR Case No. IPR2014-00883, Patent Owner's Preliminary Response Pursuant to 37 C.F.R. § 42.107, filed October 7, 2014	
	31.	Inter Partes Review of U.S. Patent No. 8,081,536, IPR Case No. IPR2014-00883, Decision – Institution of Inter Partes Review 37 C.F.R. § 42.108, issued December 16, 2014	
	32.	Inter Partes Review of U.S. Patent No. 7,881,150, IPR Case No. IPR2014-01011, Patent Owner's Preliminary Response Pursuant to 37 C.F.R. § 42.107, filed October 7, 2014	
	33.	Inter Partes Review of U.S. Patent No. 7,881,150, IPR Case No. IPR2014-01011, Decision – Institution of Inter Partes Review 37 C.F.R. § 42.108, issued December 16, 2014	
	34.	Inter Partes Review of U.S. Patent No. 7,881,150, IPR Case No. IPR2014-01011, Exhibit 3001 to Decision – Institution of Inter Partes Review, Excerpts from IEEE Dictionary, issued December 16, 2014	
	35.	Inter Partes Review of U.S. Patent No. 7,881,150, IPR Case No. IPR2014-01011, Exhibit 3002 to Decision – Institution of Inter Partes Review, Excerpts from IEEE Dictionary, issued December 16, 2014	
	36.	Inter Partes Review of U.S. Patent No. 7,881,150, IPR Case No. IPR2014-01011, Exhibit 3003 to Decision – Institution of Inter Partes Review, Excerpts from Oxford English Dictionary, issued December 16, 2014	
	37.	Inter Partes Review of U.S. Patent No. 7,881,150, IPR Case No. IPR2014-01011, Exhibit 3004 to Decision – Institution of Inter Partes Review, Excerpts from Oxford English Dictionary, issued December 16, 2014	
	38.	McCluskey, Edward J., *Logic Design Principles with Emphasis on Testable Semicustom Circuits*, Prentice Hall, 1986, pp. 104-107 and 119-120.	
	39.	Inter Partes Review Case No. IPR2014-01029, Petition for Inter Partes Review of U.S. Patent No. 8,516,185, filed on June 24, 2014.	
	40.	Inter Partes Review Case No. IPR2014-01029, Exhibit 1008 to Petition for Inter Partes Review, "Declaration of Charles J. Neuhauser, Ph.D. under 37 C.F.R. § 1.68," filed on June 24, 2014.	
	41.	Inter Partes Review Case No. IPR2014-01029, Supplemental Petition for Inter Partes Review of U.S. Patent No. 8,516,185, filed on July 23, 2014.	
	42.	Inter Partes Review Case No. IPR2014-01029, Patent Owner's Preliminary Response pursuant to 37 C.F.R. § 42.107, filed on October 17, 2014.	
	43.	Inter Partes Review Case No. IPR2014-01029, Decision Denying Institution of Inter Partes Review 37 C.F.R. § 42.108, issued December 16, 2014.	
	44.	Inter Partes Review Case No. IPR2014-01029, Petitioner's Request for Rehearing pursuant to 37 C.F.R. § 42.71, filed on January 15, 2015.	

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Sheet	3	of	3

Complete if Known	
Application Number	13/971,231
Filing Date	August 20, 2013
First Named Inventor	Jayesh R. Bhakta
Art Unit	2139
Examiner Name	Unknown
Attorney Docket Number	NETL.018P2C7

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
	45.	Inter Partes Review Case No. IPR2014-01029, Decision Denying Request for Rehearing, Issued on March 3, 2015.	
	46.	Inter Partes Review Case No. IPR2014-01369, Corrected Petition for Inter Partes Review of Claims 1-19 of U.S. Patent No. 8,516,185, filed on September 22, 2014.	
	47.	Inter Partes Review Case No. IPR2014-01369, Exhibit 1008 to Corrected Petition for Inter Partes Review, "Declaration of Dr. Nader Bagherzadeh under 37 C.F.R. § 1.68," filed on September 22, 2014.	
	48.	Inter Partes Review Case No. IPR2014-01369, Exhibit 1013 to Corrected Petition for Inter Partes Review, "Webster's II New College Dictionary," filed on September 22, 2014.	
	49.	Inter Partes Review Case No. IPR2014-01369, Exhibit 1014 to Corrected Petition for Inter Partes Review, "Standard Dictionary of Electrical and Electronics Terms," IEEE 1988, filed on September 22, 2014.	
	50.	Inter Partes Review Case No. IPR2014-01369, Decision Denying Institution of Inter Partes Review 37 C.F.R. § 42.108, issued March 9, 2014.	
	51.	U.S. District Court Northern District of California, Case No. 4:13-CV-05889-YGR, Netlist, Inc. v. Smart Storage Systems, Inc., and Diablo Technologies, Inc., Smart Storage Systems, Inc.'s Invalidity Contentions, dated June 6, 2014	
	52.	U.S. District Court Northern District of California, Case No. 4:13-CV-05889-YGR, Netlist, Inc. v. Smart Storage Systems, Inc., and Diablo Technologies, Inc., Exhibits E.1-E.7 to "Smart Storage Systems, Inc.'s Invalidity Contentions," dated June 6, 2014.	
	53.	U.S. District Court Northern District of California, Case No. 4:13-CV-05889-YGR, Netlist, Inc. v. Smart Storage Systems, Inc., and Diablo Technologies, Inc., Diablo Technologies, Inc.'s Invalidity Contentions, dated June 6, 2014.	
	54.	U.S. District Court Northern District of California, Case No. 4:13-CV-05889-YGR, Netlist, Inc. v. Smart Storage Systems, Inc., and Diablo Technologies, Inc., Exhibits D-1 to D6 to "Diablo Technologies, Inc.'s Invalidity Contentions," dated June 6, 2014.	

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Memory module with a circuit providing **load isolation** and memory domain translation
JC Solomon, JR Bhakta - US Patent 7,636,274, 2009 - Google Patents
... Memory module with a circuit providing **load isolation** and memory domain translation US 7636274 B2. Abstract. A memory module ... Each memory device has a corresponding **load**. ... method further comprises activating the circuit to selectively **isolate** at least one of the **loads** of the ...
Cited by 86 Related articles All 4 versions Cite Save

Circuit providing **load isolation** and memory domain translation for memory module
JC Solomon, JR Bhakta - US Patent 7,881,150, 2011 - Google Patents
... The circuit 40 selectively isolates one or more of the **loads** of the memory devices ... which includes, without limitation, electrical **load**, such as capacitive **load**, inductive **load**, or impedance **load**. As used herein, the term "**isolation**" is a broad term which includes, without limitation ...
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Circuit providing **load isolation** and memory domain translation for memory module
JC Solomon, JR Bhakta - US Patent 7,916,574, 2011 - Google Patents
... The circuit 40 selectively isolates one or more of the **loads** of the memory devices ... which includes, without limitation, electrical **load**, such as capacitive **load**, inductive **load**, or impedance **load**. As used herein, the term "**isolation**" is a broad term which includes, without limitation ...
Cited by 7 Related articles All 5 versions Cite Save

Dual-port buffer-to-memory interface
JB Halbert, JM Dodd, C Lam, RM Bonella - US Patent 6,742,098, 2004 - Google Patents
... The exemplary embodiments also allow the memory devices to be **isolated** from the full capacitive **loading** effects of the system memory data bus. ... Memory module with a circuit providing **load isolation** and memory domain translation. ...
Cited by 170 Related articles All 4 versions Cite Save

Circuit providing **load isolation** and memory domain translation for memory module
JC Solomon, JR Bhakta - US Patent 8,072,837, 2011 - Google Patents
... The circuit 40 selectively isolates one or more of the **loads** of the memory devices ... which includes, without limitation, electrical **load**, such as capacitive **load**, inductive **load**, or impedance **load**. As used herein, the term "**isolation**" is a broad term which includes, without limitation ...
Cited by 2 Related articles All 3 versions Cite Save

Load-reducing circuit for memory module
JC Solomon, JR Bhakta - US Patent App. 13/971,231, 2013 - Google Patents
... In certain embodiments described herein, selectively **isolating** the **loads** of the ranks of memory devices 30 advantageously decreases ... In certain embodiments, **load isolation** advantageously provides system memory with reduced electrical **loading**, thereby improving ...
Cited by 1 Related articles All 2 versions Cite Save

RECONFIGURABLE **LOAD**-REDUCED MEMORY BUFFER
S Chiu, M Arafa - US Patent 20,140,313,838, 2014 - freepatentsonline.com
... For smaller memory **loads**, the buffer can operate in switch mode by turning on the switch, and ... Moreover, this mode of operation may give a lower DIMM **loading** to the host bus for a ... by software, thus enabling the mode change depending on the application or the work **load**. ...
Cite Save More

System for communicating with synchronous device
I Abrosimov, A Deas - US Patent App. 10/425,629, 2003 - Google Patents
... The time t **dq** of delay is preferably close to a half of a range of the vernier in the ... It shall be noted that the **DQS** signal have very strict parameters providing the accuracy of ±0.2 ps as compared ... Memory module with a circuit providing **load isolation** and memory domain translation. ...
Cited by 27 Related articles All 2 versions Cite Save

System for controlling multiple memory types
PM Mehta, JR Magro - US Patent 6,681,301, 2004 - Google Patents
... 4 is replaced by driven **DQS** strobe (line 5 in FIG. 5). As with a non-×4 read operation, the **DQ** and **DQS** signals are provided by the DIMM 170. ... Programmable **DQS** preamble. ... Memory module with a circuit providing **load isolation** and memory domain translation. ...

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High performance high capacity memory systems
JJ Shau - US Patent App. 11/933,556, 2007 - Google Patents
... signals that are allowed to communicate with the system level signal, and **isolate** the loadings ... is turned off, the loadings on the chip level signal (Dc) are **isolated** from the ... The major function of the bidirectional multiplexer (BM1) used by the present invention is **loading isolation**. ...
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(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13971231	08/20/2013	Jefferey C. Solomon	NETL.018P2C7	2072

TITLE OF INVENTION:

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	SMALL	$480	$0	$0	$480	07/02/2015

EXAMINER	ART UNIT	CLASS-SUBCLASS

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☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

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1 JAMIE J. ZHENG, Ph.D, Esq.
2
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(A) NAME OF ASSIGNEE: Netlist, Inc.

(B) RESIDENCE: (CITY and STATE OR COUNTRY): Irvine, CA

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ■ Corporation or other private group entity ☐ Government

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☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

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Typed or printed name Jamie J. Zheng Registration No. 51,167

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2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Patent Application Fee Transmittal

Application Number:	13971231
Filing Date:	20-Aug-2013
Title of Invention:	MEMORY MODULE WITH LOAD REDUCING CIRCUIT AND METHOD OF OPERATION
First Named Inventor/Applicant Name:	Jefferey C. Solomon
Filer:	Jamie Jie Zheng
Attorney Docket Number:	NETL.018P2C7

Filed as Small Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Utility Appl Issue Fee	2501	1	480	480

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
		Total in USD ($)		**480**

Electronic Acknowledgement Receipt

EFS ID:	21961160
Application Number:	13971231
International Application Number:	
Confirmation Number:	2072
Title of Invention:	MEMORY MODULE WITH LOAD REDUCING CIRCUIT AND METHOD OF OPERATION
First Named Inventor/Applicant Name:	Jefferey C. Solomon
Customer Number:	79141
Filer:	Jamie Jie Zheng
Filer Authorized By:	
Attorney Docket Number:	NETL.018P2C7
Receipt Date:	02-APR-2015
Filing Date:	20-AUG-2013
Time Stamp:	20:54:00
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	$480
RAM confirmation Number	7004
Deposit Account	
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Issue Fee Payment (PTO-85B)	2015-04-02_Issue_Fee_Transmittal_NETL018P2C7.pdf	74229 e8ef5fe764f568389c565bfb79e2c9e743d4c193	no	2
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	30652 46706b2b29fe24af4b45c994c62cfb8e2d57e6c9	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	104881		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

<u>New Applications Under 35 U.S.C. 111</u>
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

<u>National Stage of an International Application under 35 U.S.C. 371</u>
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

<u>New International Application Filed with the USPTO as a Receiving Office</u>
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Electronically filed **

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	:	Netlist, Inc.
App. No.	:	13/971,231
Filed	:	August 20, 2013
For	:	MEMORY MODULE WITH LOAD REDUCING CIRCUIT AND METHOD OF OPERATION
Examiner	:	BANSAL, GURTEJ
Art Unit	:	2139
Conf. No.	:	2072
Docket No.	:	NETL.018P2C7

CERTIFICATE OF EFS WEB TRANSMISSION

I hereby certify that this correspondence and any other attachment noted on the Automated Acknowledgement Receipt, is being transmitted from within the Pacific Time zone to the Commissioner for Patents via the EFS Web Server on:

April 2, 2015

(Date)

/Jamie J. Zheng/

Jamie J. Zheng, Reg. No. 51167

AMENDMENT UNDER 37 C.F.R. 1.312

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicant hereby submits the following amendment under 37 C.F.R. 1.312.

The Commissioner is hereby authorized to charge any required fee(s) to Deposit Account No. 50-5963.

AMENDMENTS to the SPECIFICATION begin on Page 2 of this paper.

REMARKS begin on Page 3 of this paper.

Samsung Electronics Co., Ltd.
Ex. 1052, p. 342

IN THE SPECIFICATION

Please amend paragraph [0011] under the Summary of the Invention as follows:

[0011] In certain embodiments, a memory module includes a plurality of memory devices and is operable in a computer system to perform memory operations in response to memory commands from a memory controller of the computer system. The memory module is to be ~~being~~ coupled to the memory controller via a memory bus, the memory bus including a control/address (C/A) bus and a data bus. The memory module comprises a register device configured to receive a set of input control/address signals associated with a respective memory command (e.g., a read command or a write command) from the memory controller and to generate a set of output control/address signals in response to the set of input control/address signals. The set of output control/address signals are provided to the plurality of memory devices. The memory module further comprises a circuit coupled between the data bus and the plurality of memory devices, the circuit to selectively isolate one or more first memory devices among the plurality of memory devices from the data bus in response to the respective memory command so as to reduce a load of the memory module to the computer system while one or more second memory devices among the plurality of memory devices are communicating with the memory controller in response to the set of output control/address signals.

Samsung Electronics Co., Ltd.
Ex. 1052, p. 343

REMARKS

This amendment under 37 C.F.R. 1.312 is filed after the Notice of Allowance dated April 2, 2015.

Paragraph [0011] under the Summary of the Invention are amended to correct a grammatical/typographical error. No new matter is added.

The undersigned attorney can be reached at (650) 273-6008, if a telephone call could help resolve any remaining items.

Respectfully submitted,

Date: April 2, 2015 /Jamie J. Zheng/ 51167

Jamie J. Zheng (Reg. No.)
Customer Number 79141

Samsung Electronics Co., Ltd.
Ex. 1052, p. 344

Electronic Acknowledgement Receipt

EFS ID:	21961235
Application Number:	13971231
International Application Number:	
Confirmation Number:	2072
Title of Invention:	MEMORY MODULE WITH LOAD REDUCING CIRCUIT AND METHOD OF OPERATION
First Named Inventor/Applicant Name:	Jefferey C. Solomon
Customer Number:	79141
Filer:	Jamie Jie Zheng
Filer Authorized By:	
Attorney Docket Number:	NETL.018P2C7
Receipt Date:	02-APR-2015
Filing Date:	20-AUG-2013
Time Stamp:	21:13:55
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Amendment after Notice of Allowance (Rule 312)	2015-04-02_312_Amendment_NETL018P2C7.pdf	580403 efa07f26f0dd2c2937ed2170b7653d78fdd26090	no	3

Warnings:	
Information:	

Total Files Size (in bytes):	580403

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New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

OK TO ENTER: /G.B./ (04/15/2015)

Electronically filed **

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	:	Netlist, Inc.
App. No.	:	13/971,231
Filed	:	August 20, 2013
For	:	MEMORY MODULE WITH LOAD REDUCING CIRCUIT AND METHOD OF OPERATION
Examiner	:	BANSAL, GURTEJ
Art Unit	:	2139
Conf. No.	:	2072
Docket No.	:	NETL.018P2C7

CERTIFICATE OF EFS WEB TRANSMISSION

I hereby certify that this correspondence and any other attachment noted on the Automated Acknowledgement Receipt, is being transmitted from within the Pacific Time zone to the Commissioner for Patents via the EFS Web Server on:

April 2, 2015

(Date)

/Jamie J. Zheng/

Jamie J. Zheng, Reg. No. 51167

AMENDMENT UNDER 37 C.F.R. 1.312

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicant hereby submits the following amendment under 37 C.F.R. 1.312.

The Commissioner is hereby authorized to charge any required fee(s) to Deposit Account No. 50-5963.

AMENDMENTS to the SPECIFICATION begin on Page 2 of this paper.

REMARKS begin on Page 3 of this paper.

Samsung Electronics Co., Ltd.
Ex. 1052, p. 347

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/971,231	08/20/2013	Jefferey C. Solomon	NETL.018P2C7	2072

79141 7590 04/20/2015

The Law Office of Jamie Zheng, Ph.D Esq.
P.O. Box 60573
Palo Alto, CA 94306

EXAMINER	
BANSAL, GURTEJ	

ART UNIT	PAPER NUMBER
2139	

NOTIFICATION DATE	DELIVERY MODE
04/20/2015	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

jz@jzpatent.com

Samsung Electronics Co., Ltd.
Ex. 1052, p. 348

UNITED STATES DEPARTMENT OF COMMERCE
U.S. Patent and Trademark Office
Address : COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450

APPLICATION NO./ CONTROL NO.	FILING DATE	FIRST NAMED INVENTOR / PATENT IN REEXAMINATION	ATTORNEY DOCKET NO.
13/971,231	20 August, 2013	SOLOMON ET AL.	NETL.018P2C7

		EXAMINER	
The Law Office of Jamie Zheng, Ph.D Esq. P.O. Box 60573 Palo Alto, CA 94306		GURTEJ BANSAL	
		ART UNIT	PAPER
		2139	20150415

DATE MAILED:

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner for Patents

The amendment dated April 2, 2015 has been entered.

/GURTEJ BANSAL/
Primary Examiner, Art Unit 2139

PTO-90C (Rev.04-03)

PTO/SB/08a/b(07-09)
Approved for use through 7/31/2012. OMB 0651-0031
US Patent & Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 1 of 1

Complete if Known	
Application Number	13/971,231
Filing Date	August 20, 2013
First Named Inventor	Jayesh R. Bhakta
Art Unit	2189
Examiner Name	Unknown
Attorney Docket Number	NETL.018P2C7

US PATENT DOCUMENTS

Examiner Initials *	Cite No. [1]	Document Number / Number-Kind Code [2] (if known)	Publication Date (MM-DD-YYYY)	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	1	20080025137	01-31-2008	~~Natarajan et al.~~ Rajan; Suresh Natarajan ; et al.	
	2	2006233012	10-19-2006	~~Tomonori et al.~~ Sekiguchi; Tomonori ; et al.	

Change(s) applied to document,
/S.X.S/
2/25/2015

FOREIGN PATENT DOCUMENTS

Examiner Initials *	Cite No. [1]	Foreign Patent Document	Publication Date (MM-DD-YYYY)	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]
	3	EP 1 816 570 A2	08-08-2007	Rambus, Inc.		

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
	4	International Search Report and Written Opinion, PCT/US2011/059209, January 31, 2013	

EXAMINER /Gurtej Bansal/ (05/11/2014) **DATE CONSIDERED** 05/11/2014

* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1] Applicant's unique citation designation number (optional). [2] See Kinds Codes of USPTO Patents Documents at www.uspto.gov or MPEP 901.04. [3] Enter Office that issued the document, by the two-letter code (WIPO Standard ST. 3). [4] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5] Kind of document by the appropriate symbols as indicated on the document and WIPO Standard ST. 16 if possible. [6] Applicant is to place a check mark here if English language Translation is attached.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /G.B./

PTO/SB/08a/b(07-09)
Approved for use through 7/31/2012. OMB 0651-0031
US Patent & Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 1 of 3

Complete if Known	
Application Number	13/971,231
Filing Date	August 20, 2013
First Named Inventor	Jayesh R. Bhakta
Art Unit	2189
Examiner Name	Unknown
Attorney Docket Number	NETL.018P2C7

US PATENT DOCUMENTS

Examiner Initials *	Cite No. [1]	Document Number Number-Kind Code [2] (if known)	Publication Date (MM-DD-YYYY)	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	1	5345412	09-06-1994	Shiratsuchi	
	2	5537584	07-16-1996	Miyai et al.	
	3	5617559	04-01-1997	Le et al.	
	4	5649159	07-15-1997	Le et al.	
	5	5717851	02-10-1998	Yishay et al.	
	6	5724604	03-03-1998	Moyer	
Change(s) applied to document, /S.X.S./ 2/25/2015	7	5729716	~~05-17-1998~~ 3/1998	Lee et al.	
	8	5784705	07-21-1998	Leung, Wingyu	
	9	5802541	09-01-1998	Reed	
	10	5973392	10-26-1999	Senba et al.	
~~Change(s) applied~~ to document, /S.X.S./ 2/25/2015	11	6173357	~~01-09-2011~~ 1/2001	Ju	
	12	6260127	07-10-2001	Olarig et al.	
	13	6446158	09-03-2002	Karabatsos	
	14	6553449	04-22-2003	Dodd et al.	
	15	6618791	09-09-2003	Dodd et al.	
	16	6717855	04-06-2004	Underwood	
	17	6788592	09-07-2004	Nakata et al.	
	18	6948084	09-20-2005	Manapat et al	
	19	7130308	10-31-2006	Haddock et al.	
	20	7133960	11-07-2006	Thompson et al.	
	21	7379361	05-27-2008	Co et al.	
	22	20050010737	01-01-2005	Ware et al.	
	23	20070293094	12-01-2007	Aekins, Robert A.	

US PATENT APPLICATIONS

Examiner Initials *	Cite No. [1]	Document Number Number-Kind Code [2] (if known)	Filing Date (MM-DD-YYYY)	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	24	95/001,758	09-14-2011	Owned by Netlist, Inc.	
	25	13/154,172	06-06-2011	Owned by Netlist, Inc.	
	26	13/287,042	11-01-2011	Owned by Netlist, Inc.	
	27	13/473,413	05-16-2012	Owned by Netlist, Inc.	
	28	13/032,470	02-22-2011	Owned by Netlist, Inc.	
	29	13/287,081	11-01-2011	Owned by Netlist, Inc.	
	30	13/971,231	08-20-2013	Owned by Netlist, Inc.	
	31	13/412,243	03-05-2012	Owned by Netlist, Inc.	
	32	13/183,253	07-14-2011	Owned by Netlist, Inc.	
	33	13/745,790	01-19-2013	Owned by Netlist, Inc.	

EXAMINER /Gurtej Bansal/ (05/11/2014) **DATE CONSIDERED** 05/11/2014

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ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /G.B./

PTO/SB/08a/b(07-09)
Approved for use through 7/31/2012. OMB 0651-0031
US Patent & Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Substitute for form 1449/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet	1	of	3

Complete if Known	
Application Number	13/971,231
Filing Date	August 20, 2013
First Named Inventor	Jayesh R. Bhakta
Art Unit	2139
Examiner Name	Unknown
Attorney Docket Number	NETL.018P2C7

Change(s) applied to document, /J.H./ 4/23/2015

US PATENT DOCUMENTS

Examiner Initials *	Cite No. [1]	Document Number Number-Kind Code [2] (if known)	Publication Date (MM-DD-YYYY)	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	1.	5388240	02-01-1995	~~IBM Corporation~~	Olderdissen et al.
	2.	5463590	10-31-1995	Watanabe	
	3.	5953280	09-14-1999	Matsui	
	4.	6188641	02-13-2001	Uchida	
	5.	6205516	03-20-2001	Usami	
	6.	6480439	11-12-2002	Tokutome et al.	
	7.	7464225	12-09-2008	Tsern	
	8.	7865674	01-04-2011	Gower et al.	
	9.	8089795	01-03-2012	Rajan	
	10.	8130560	03-06-2012	Rajan	
	11.	8189328	05-29-2012	Kanapathippillai	
	12.	8233303	07-31-2012	Best	
	13.	8250295	08-21-2012	Amidi et al.	
	14.	8417870	04-09-2013	Lee et al.	
	15.	8516185	08-20-2013	Lee et al.	
	16.	8516188	08-20-2013	Solomon et al.	
	17.	8756364	06-17-2014	Bhakta et al.	
	18.	20070058409	03-15-2007	Ruckerbauer	
	19.	20080104352	05-01-2008	Talbot	
	20.	20080104352	05-01-2008	Talbot	
	21.	RE36229	06-15-1999	Cady	

US PATENT APPLICATIONS

Examiner Initials *	Cite No. [1]	Application Number	Filing Date (MM-DD-YYYY)	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	22.	13/411,344	3/2/2012	Lee	Entire Prosecution History
	23.	13/970,606	8/20/2013	Netlist, Inc.	Entire Prosecution History
	24.	13/971,231	8/20/2013	Netlist, Inc.	Entire Prosecution History
	25.	14/229,844	3/29/2014	Netlist, Inc.	Entire Prosecution History
	26.	14/324,990	7/7/2014	Netlist, Inc.	Entire Prosecution History
	27.	14/337,168	7/21/2014	Netlist, Inc.	Entire Prosecution History

NON PATENT LITERATURE DOCUMENTS

EXAMINER /Gurtej Bansal/ (03/30/2015) **DATE CONSIDERED** 03/30/2015

* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1] Applicant's unique citation designation number (optional). [2] See Kinds Codes of USPTO Patents Documents at www.uspto.gov or MPEP 901.04. [3] Enter Office that issued the document, by the two-letter code (WIPO Standard ST. 3). [4] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5] Kind of document by the appropriate symbols as indicated on the document and WIPO Standard ST. 16 if possible. [6] Applicant is to place a check mark here if English language Translation is attached.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /G.B./

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/971,231	05/19/2015	9037774	NETL.018P2C7	2072

79141 7590 04/29/2015

The Law Office of Jamie Zheng, Ph.D Esq.
P.O. Box 60573
Palo Alto, CA 94306

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 0 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site http://pair.uspto.gov for additional applicants):

Netlist, Inc., Irvine, CA, Assignee (with 37 CFR 1.172 Interest);
Jefferey C. Solomon, Irvine, CA;
Jayesh R. Bhakta, Cerritos, CA;

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The USA offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to encourage and facilitate business investment. To learn more about why the USA is the best country in the world to develop technology, manufacture products, and grow your business, visit SelectUSA.gov.

Samsung Electronics Co., Ltd.
Ex. 1052, p. 353

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PATENT

OPAP AKIMA-16
AUG 1 3 2015
PATENT & TRADEMARK OFFICE

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent No.	:	9,037,774
Issued	:	May 19, 2015
Assignee	:	Netlist, Inc.
App. No.	:	13/971,231
Filed	:	August 20, 2013
For	:	MEMORY MODULE WITH LOAD REDUCING CIRCUIT AND METHOD OF OPERATION
Examiner	:	BANSAL, GURTEJ
Art Unit	:	2139
Conf. No.	:	2072
Docket No.	:	NETL.018P2C7

REQUEST FOR CERTIFICATE OF CORRECTION

Certificate of Correction Branch
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir or Madam:

Applicant hereby requests that the enclosed Certificate of Correction be issued in the above-referenced patent.

The Commissioner is hereby authorized to charge any required fee(s) to Deposit Account No. 50-5963.

The undersigned attorney can be reached at (650) 273-6008, if a telephone call could help resolve any issues.

Respectfully submitted,

Date: August 10, 2015

By: _____

Jamie J. Zheng
Registration No. 51,167
Customer No. 79,141

PTO/SB/44 (09-07)
Approved for use through 08/31/2013. OMB 0651-0033
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.
(Also Form PTO-1050)

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 9,037,774

APPLICATION NO.: 13/971,231

ISSUE DATE : May 19, 2015

INVENTOR(S) : Jeffrey C. Solomon and Jayesh R. Bhakta

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

On the front page, Inventor Jefferey C. Solomon should be Jeffrey C. Solomon

Column 41, lines 52 and 54, insert --to-- between "memory module" and "receive."

Column 42, lines 54 and 57, "disabling" should be changed to -disables--.

Column 42, line 59, the claim reference numeral '5' should read -1-.

Column 43, line 39, the claim reference numeral '9' should read -1-.

Column 43, line 41, change "the" before "ODT" to -an-- and insert the following text after "ODT signal"

from the memory controller

Column 44, line 11, delete the word "module" before "DQ and DQS pins."

Column 44, lines 45 and 47, cancel the text "module DQ and DQS signal lines" and insert the following text after "set of"

DQ and DQS pins

Column 45, line 3, cancel the text "register device outputs" and insert the following text before "a greater number of"

method further comprises outputting

Column 46, line 15, the claim reference numeral '19' should read -11-.

Column 46, line 17, change "the" before "ODT" to -an-- and insert the following text after "ODT signal"

from the memory controller

MAILING ADDRESS OF SENDER (Please do not use customer number below):
Jamie Zheng, PO Box 60573, Palo Alto, CA 94306

This collection of information is required by 37 CFR 1.322, 1.323, and 1.324. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1.0 hour to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Attention Certificate of Corrections Branch, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

UNITED STATES PATENT AND TRADEMARK OFFICE

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79141 e 2015-12-14

Jamie J. Zheng, Ph.D Esq.
P.O. Box 60573
Palo Alto, CA 94306

Paper No.

Application No.:	**13/971,231**	**Date Mailed:**	**2015-12-14** **ELECTRONIC**
First Named Inventor:	Jefferey C. Solomon	Examiner:	BANSAL, GURTEJ
Attorney Docket No.:	NETL.018P2C7	Art Unit:	2139
Confirmation No.:	2072	Filing Date:	08/20/2013

Please find attached an Office communication concerning this application or proceeding.

Commissioner for Patents

PTO-90c (Rev.08-06)

Response to the Request for Certificate of Correction	Patent No. 9037774	Applicant(s) SOLOMON ET AL.
	Issue Date 19 May, 2015	Docket No. NETL.018P2C7

This is in response to the request for a Certificate of Correction filed 13 August, 2015

☒ **Request Approval- In- Part** – Consideration has been given to your request for the issuance of a Certificate of Correction under the provisions of 37 CFR 1.322 and/or 37 CFR 1.323. The Request is improper and approved in part for the reason(s) below:

☐ **Supersede/Vacate** – The Certificate of Correction issued in error, in that error(s) was made in identifying the patent number and/or keying text/corrections. See 'Other Comments' below:

1. ☐ Assignees' names and addresses (assignment data) printed in a patent, are based solely on information supplied in the appropriate space for identifying the assignment data on the Issue Fee Transmittal Form (PTOL-85b). Any request for a patent to be corrected to state the name of the assignee, must state that the assignment was submitted for recordation as set forth in in 37 CFR 3.11 before issuance of the patent. The petition fee set forth in 37 CFR 1.17(i)(1) (currently $140, $70, $35 for large, small and micro entities, respectively.

2. ☐ The alleged error in , is in fact an Amendment and/or Change made by the examiner and considered to be in accordance with the permissible amendments enumerated in the Manual of Patent Examining Procedure (MPEP) Section 1302.04. Applicant did not file objection or amendment under 37 CFR 1.312 prior to payment of the issue fee.

3. ☒ A petition under CFR 1.182 is required to correct the alleged errors in spelling or order of inventor's names, since inventor's names are printed solely in accordance with the type-written names, and in the order of the type-written names on the Application Data Sheet (ADS).

4. ☐ With respect to the alleged error in changing the inventor name on the patent due to clerical error in ADS/OATH of related patents. The inventor's name is printed in accordance with the OATH/ADS submitted at the time of filing the application. However, your attention is directed to C.F.R. 1.324, wherein a request is being made to change, add or delete inventor(s), after issuance of the patent.

5. ☐ With respect to the alleged error in , comparison of the printed patent with the corresponding location in the application file reveals that there is no discrepancy.

6. ☐ With respect to 37 CFR 1.72, the title should be brief but technically accurate and descriptive and should contain fewer than 500 characters. Inasmuch as the words "new," "improved," "improvement of," and "improvement in" are not considered as part of the title of an invention, these words should not be included at the beginning of the title of the invention and will be deleted when the Office enters the title into the Office's computer records, and when any patent issues.

7. ☐ The fee for correction under 37 CFR 1.323 is set forth in 37 CFR 1.20(a). ☐ Partial fee ☐ No fee was received with your request. Full fee payment is required before further action is taken on this request.

8. ☐ With respect to the request for corrected Letters Patent (Grant), corrections to the original Letters Patent are made under the provisions of Rule 1.322(b), not Rule1.323, unless a petition is granted.

9. ☐ Other Comments:

Further correspondence concerning this matter should be filed and directed to the Certificates of Correction Branch.

Legal Instrument Examiner: **/EVA E. JAMES/** Phone: (571)272-3422

Certificates of Correction Branch email: CustomerServiceCoC@uspto.gov CoC Central Phone Number: (703) 756-1814

If applicable, information regarding a petition under 37 CFR 1.183 should be directed to the attention of the Commissioner for Patents using the FAX number (571) 273-8300

Samsung Electronics Co., Ltd.
Ex. 1052, p. 357

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 9,037,774 B2
APPLICATION NO. : 13/971231
DATED : May 19, 2015
INVENTOR(S) : Jeffrey C. Solomon and Jayesh R. Bhakta

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In the claims

Column 41, lines 52 and 54, insert --to-- between "memory module" and "receive.".

Column 42, lines 54 and 57, "disabling" should be changed to --disables--.

Column 42, line 59, the claim reference numeral '5' should read -1-.

Column 43, line 39, the claim reference numeral '9' should read -1-.

Column 43, line 41, change "the" before "ODT" to --an-- and insert the following text after "ODT signal"

--from the memory controller--

Column 44, line 11, delete the word "module" before "DQ and DQS pins."

Column 44, lines 45 and 47, cancel the text "module DQ and DQS signal lines" and insert the following text after "set of"

--DQ and DQS pins--

Column 45, line 3, cancel the text "register device outputs" and insert the following text before "a greater number of"

--method further comprises outputting--

Column 46, line 15, the claim reference numeral '19' should read -11-.

Signed and Sealed this
Twenty-ninth Day of December, 2015

Michelle K. Lee

Michelle K. Lee
Director of the United States Patent and Trademark Office

Column 46, line 17, change “the” before “ODT” to --an-- and insert the following text after “ODT signal”

--from the memory controller--

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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY.DOCKET NO./TITLE	REQUEST ID
13/971,231	08/20/2013	Jefferey C. Solomon	129980-5021US	67119

Acknowledgement of Loss of Entitlement to Entity Status Discount

The entity status change request below filed through Private PAIR on 07/06/2018 has been accepted.

CERTIFICATIONS:

Change of Entity Status:

X Applicant changing to regular undiscounted fee status.

NOTE: Checking this box will be taken to be notification of loss of entitlement to small or micro entity status, as applicable.

This portion must be completed by the signatory or signatories making the entity status change in accordance with 37 CFR 1.4(d)(4).

Signature:	/Jamie J. Zheng/
Name:	Jamie J. Zheng
Registration Number:	51167