PC2100 and PC1600 DDR SDRAM Registered DIMM

Design Specification

Revision 1.3

January 2002

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Product Description

This specification defines the electrical and mechanical requirements for 184-pin, 2.5 Volt, PC1600/PC2100, 64/72 bit-wide, Registered Double Data Rate Synchronous DRAM Dual In-Line Memory Modules (DDR SDRAM DIMMs).These SDRAM DIMMs are intended for use as main memory when installed in systems such as servers and workstations. PC1600/PC2100 refers to the JEDEC standard DIMM naming convention in which PC1600 indicates a 184-pin DIMM running at 100 MHz clock speed and offering 1600MB/s bandwidth.

Reference design examples are included which provide an initial basis for Registered DIMM designs. Modifications to these reference designs may be required to meet all system timing, signal integrity, and thermal requirements for PC1600/PC2100 support. All registered DIMM implementations must use simulations and lab verification to ensure proper timing requirements and signal integrity in the design.

This specification largely follows the JEDEC defined 184-pin Registered DDR SDRAM DIMM product (refer to JEDEC Standards Manual 21-C, at http://www.jedec.org).

Product Family Attributes

DIMM organization	x72 ECC, x64
DIMM dimensions (nominal)	5.25" x 1.2”/1.7"
Pin count	184
SDRAMs supported	64Mb, 128Mb, 256Mb, 512Mb, 1Gb
Capacity	64MB, 128MB, 256MB, 512MB, 1GB, 2GB, 4GB
Serial PD	Consistent with JC 42.5 Rev 0
Voltage options	2.5 volt (V_{DD}/V_{DDQ})
Interface	SSTL_2

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Environmental Requirements

DDR SDRAM Registered DIMMs are intended for use in standard office environments that have limited capacity for heating and air conditioning.

Environmental Parameters

Symbol	Parameter	Rating	Units	Notes
T_{OPR}	Operating temperature (ambient)	0 to +55	°C	1
H_{OPR}	Operating humidity (relative)	10 to 90	%	1
T_{STG}	Storage temperature	-50 to +100	°C	1
H_{STG}	Storage humidity (without condensation)	5 to 95	%	1
P_{BAR}	Barometric pressure (operating & storage)	105 to 69	K Pascal	1, 2

1. Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Up to 9850 ft.

Architecture

Pin Description

Pin Name	Description	Pin Name	Description
A0 - A15	SDRAM address bus	CK0	SDRAM clock (positive line of differential pair)
BA0 - BA1	SDRAM bank select	$\overline{CK0}$	SDRAM clock (negative line of differential pair)
DQ0 - DQ63	DIMM memory data bus	SCL	IIC serial bus clock for EEPROM
CB0 - CB7	DIMM ECC check bits	SDA	IIC serial bus data line for EEPROM
$\overline{RAS}$	SDRAM row address strobe	SA0 - SA2	IIC slave address select for EEPROM
$\overline{CAS}$	SDRAM column address strobe	V_{DD}	SDRAM positive power supply
$\overline{WE}$	SDRAM write strobe	V_{DDQ}	SDRAM I/O Driver positive power supply
$\overline{S}0$ - $\overline{S}3$	SDRAM chip select lines (Physical. banks 0, 1, 2, and 3)	V_{REF}	SDRAM I/O reference supply
CKE0 - CKE1	SDRAM clock enable lines	V_{SS}	Power supply return (ground)
DQS0 - DQS8	SDRAM low data strobes	V_{DDSPD}	Serial EEPROM positive power supply (Supports both 2.5 Volt and 3.3 Volt operation)
DM(0-8)/DQS(9-17)	SDRAM low data masks/high data strobes (x4, x8-based x72 DIMMs)	NC	Spare Pins (no connect)
V_{DDID}	V_{DD} Identification Flag	$\overline{RESET}$	Reset pin (forces register inputs low)
Test	Used by memory bus analysis tools (unused on memory DIMMs)		

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Input/Output Functional Description

Symbol	Type	Polarity	Function
CK0	SSTL	Positive Edge	Positive line of the differential pair of system clock inputs that drives input to the on-DIMM PLL. (All DDR SDRAM addr/cntl inputs are sampled on the rising edge of their associated clocks.)
$\overline{CK0}$	SSTL	Negative Edge	Negative line of the differential pair of system clock inputs that drives the input to the on-DIMM PLL.
CKE0, CKE1	SSTL	Active High	Activates the SDRAM CK signal when high and deactivates the CK signal when low. By deactivating the clocks, CKE low initiates the Power Down mode, or the Self Refresh mode.
$\overline{S0}$, $\overline{S1}$, $\overline{S2}$, $\overline{S3}$	SSTL	Active Low	Enables the associated SDRAM command decoder when low and disables decoder when high. When decoder is disabled, new commands are ignored but previous operations continue.
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	SSTL	Active Low	When sampled at the positive rising edge of the clock, $\overline{CAS}$, $\overline{RAS}$, and $\overline{WE}$ define the operation to be executed by the SDRAM.
V_{REF}	Supply		Reference voltage for SSTL2 inputs
V_{DDQ}	Supply		Isolated power supply for the DDR SDRAM output buffers to provide improved noise immunity
BA0,BA1	SSTL	—	Selects which SDRAM bank of four is activated.
A0 - A9, A11 A10/AP, A12- A15	SSTL	—	During a Bank Activate command cycle, A0-A15 defines the row address (RA0-RA15) when sampled at the rising clock edge. During a Read or Write command cycle, A0-A12 defines the column address (CA0-CA12) when sampled at the rising clock edge. In addition to the column address, AP is used to invoke autoprecharge operation at the end of the burst read or write cycle. If AP is high, autoprecharge is selected and BA0, BA1 defines the bank to be precharged. If AP is low, autoprecharge is disabled. During a Precharge command cycle, AP is used in conjunction with BA0, BA1 to control which bank(s) to precharge. If AP is high, all banks will be precharged regardless of the state of BA0 or BA1. If AP is low, BA0 and BA1 are used to define which bank to precharge.
DQ0 - DQ63, CB0 - CB7	SSTL	—	Data and Check Bit Input/Output pins
DM0-DM8	SSTL	Active High	Masks write data when high, issued concurrently with input data. Both DM and DQ have a write latency of one clock once the write command is registered into the SDRAM.
V_{DD}, V_{SS}	Supply		Power and ground for the DDR SDRAM input buffers and core logic
DQS0-DQS8	SSTL	Negative and Positive Edge	Data strobe for input and output data.
SA0 - 2		—	These signals are tied at the system planar to either V_{SS} or V_{DD} to configure the serial SPD EEPROM address range.
SDA		—	This bidirectional pin is used to transfer data into or out of the SPD EEPROM. A resistor must be connected from the SDA bus line to V_{DD} to act as a pullup.
SCL		—	This signal is used to clock data into and out of the SPD EEPROM. A resistor may be connected from the SCL bus time to V_{DD} to act as a pullup.
V_{DDSPD}	Supply		Serial EEPROM positive power supply (wired to a separate power pin at the connector which supports both 2.3 Volt and 3.3 Volt operation).
$\overline{RESET}$	LV-CMOS	Active Low	This signal is asynchronous and driven low to the register to guarantee that the register outputs are low.

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184-Pin DDR SDRAM DIMM Pin Assignments

Front Side (left side 1 - 52, right side 53 - 92)			Back Side (left side 93 -144, right side 145 -184)			Front Side (left side 1 - 52, right side 53 - 92)			Back Side (left side 93 -144, right side 145 -184)		
Pin #	x64 Non-Parity	x72 ECC	Pin #	x64 Non-Parity	x72 ECC	Pin #	x64 Non-Parity	x72 ECC	Pin #	x64 Non-Parity	x72 ECC
1	V_{REF}	V_{REF}	93	V_{SS}	V_{SS}	48	A0	A0	140	NC	DM8,DQS17
2	DQ0	DQ0	94	DQ4	DQ4	49	NC	CB2	141	A10	A10
3	V_{SS}	V_{SS}	95	DQ5	DQ5	50	V_{SS}	V_{SS}	142	NC	CB6
4	DQ1	DQ1	96	V_{DDQ}	V_{DDQ}	51	NC	CB3	143	V_{DDQ}	V_{DDQ}
5	DQS0	DQS0	97	DM0,DQS9	DM0,DQS9	52	BA1	BA1	144	NC	CB7
6	DQ2	DQ2	98	DQ6	DQ6	KEY			KEY		
7	V_{DD}	V_{DD}	99	DQ7	DQ7	53	DQ32	DQ32	145	V_{SS}	V_{SS}
8	DQ3	DQ3	100	V_{SS}	V_{SS}	54	V_{DDQ}	V_{DDQ}	146	DQ36	DQ36
9	NC,A15	NC,A15	101	NC	NC	55	DQ33	DQ33	147	DQ37	DQ37
10	$\overline{RESET}$	$\overline{RESET}$	102	NC,TEST	NC,TEST	56	DQS4	DQS4	148	V_{DD}	V_{DD}
11	V_{SS}	V_{SS}	103	NC	NC	57	DQ34	DQ34	149	DM4,DQS13	DM4,DQS13
12	DQ8	DQ8	104	V_{DDQ}	V_{DDQ}	58	V_{SS}	V_{SS}	150	DQ38	DQ38
13	DQ9	DQ9	105	DQ12	DQ12	59	BA0	BA0	151	DQ39	DQ39
14	DQS1	DQS1	106	DQ13	DQ13	60	DQ35	DQ35	152	V_{SS}	V_{SS}
15	V_{DDQ}	V_{DDQ}	107	DM1,DQS10	DM1,DQS10	61	DQ40	DQ40	153	DQ44	DQ44
16	NC (CK1)[1]	NC (CK1)[1]	108	V_{DD}	V_{DD}	62	V_{DDQ}	V_{DDQ}	154	$\overline{RAS}$	$\overline{RAS}$
17	NC ($\overline{CK1}$)[1]	NC ($\overline{CK1}$)[1]	109	DQ14	DQ14	63	$\overline{WE}$	$\overline{WE}$	155	DQ45	DQ45
18	V_{SS}	V_{SS}	110	DQ15	DQ15	64	DQ41	DQ41	156	V_{DDQ}	V_{DDQ}
19	DQ10	DQ10	111	CKE1	CKE1	65	$\overline{CAS}$	$\overline{CAS}$	157	$\overline{S}0$	$\overline{S}0$
20	DQ11	DQ11	112	V_{DDQ}	V_{DDQ}	66	V_{SS}	V_{SS}	158	$\overline{S}1$	$\overline{S}1$
21	CKE0	CKE0	113	NC(BA2)	NC(BA2)	67	DQS5	DQS5	159	DM5,DQS14	DM5,DQS14
22	V_{DDQ}	V_{DDQ}	114	DQ20	DQ20	68	DQ42	DQ42	160	V_{SS}	V_{SS}
23	DQ16	DQ16	115	A12,NC	A12,NC	69	DQ43	DQ43	161	DQ46	DQ46
24	DQ17	DQ17	116	V_{SS}	V_{SS}	70	V_{DD}	V_{DD}	162	DQ47	DQ47
25	DQS2	DQS2	117	DQ21	DQ21	71	NC, $\overline{S}2$	NC, $\overline{S}2$	163	NC, $\overline{S}3$	NC, $\overline{S}3$
26	V_{SS}	V_{SS}	118	A11	A11	72	DQ48	DQ48	164	V_{DDQ}	V_{DDQ}
27	A9	A9	119	DM2,DQS11	DM2,DQS11	73	DQ49	DQ49	165	DQ52	DQ52
28	DQ18	DQ18	120	V_{DD}	V_{DD}	74	V_{SS}	V_{SS}	166	DQ53	DQ53
29	A7	A7	121	DQ22	DQ22	75	NC ($\overline{CK2}$)[1]	NC ($\overline{CK2}$)[1]	167	A13,NC	A13,NC
30	V_{DDQ}	V_{DDQ}	122	A8	A8	76	NC (CK2)[1]	NC (CK2)[1]	168	V_{DD}	V_{DD}
31	DQ19	DQ19	123	DQ23	DQ23	77	V_{DDQ}	V_{DDQ}	169	DM6,DQS15	DM6,DQS15
32	A5	A5	124	V_{SS}	V_{SS}	78	DQS6	DQS6	170	DQ54	DQ54
33	DQ24	DQ24	125	A6	A6	79	DQ50	DQ50	171	DQ55	DQ55
34	V_{SS}	V_{SS}	126	DQ28	DQ28	80	DQ51	DQ51	172	V_{DDQ}	V_{DDQ}

NC = No Connect; NU = Not Useable; DU = Do Not Use

1. These pins reserved for unbuffered DDR DIMMs. Systems supporting both unbuffered and registered DIMMs may be connected to an active signal on the baseboard.
2. The TEST pin is reserved for bus analysis probes and is not connected on normal memory modules (DIMMs)

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184-Pin DDR SDRAM DIMM Pin Assignments

Front Side (left side 1 - 52, right side 53 - 92)			Back Side (left side 93 -144, right side 145 -184)			Front Side (left side 1 - 52, right side 53 - 92)			Back Side (left side 93 -144, right side 145 -184)		
Pin #	x64 Non-Parity	x72 ECC	Pin #	x64 Non-Parity	x72 ECC	Pin #	x64 Non-Parity	x72 ECC	Pin #	x64 Non-Parity	x72 ECC
35	DQ25	DQ25	127	DQ29	DQ29	81	V_{SS}	V_{SS}	173	NC,A14	NC,A14
36	DQS3	DQS3	128	V_{DDQ}	V_{DDQ}	82	V_{DDID}	V_{DDID}	174	DQ60	DQ60
37	A4	A4	129	DM3,DQS12	DM3,DQS12	83	DQ56	DQ56	175	DQ61	DQ61
38	V_{DD}	V_{DD}	130	A3	A3	84	DQ57	DQ57	176	V_{SS}	V_{SS}
39	DQ26	DQ26	131	DQ30	DQ30	85	V_{DD}	V_{DD}	177	DM7,DQS16	DM7,DQS16
40	DQ27	DQ27	132	V_{SS}	V_{SS}	86	DQS7	DQS7	178	DQ62	DQ62
41	A2	A2	133	DQ31	DQ31	87	DQ58	DQ58	179	DQ63	DQ63
42	V_{SS}	V_{SS}	134	NC	CB4	88	DQ59	DQ59	180	V_{DDQ}	V_{DDQ}
43	A1	A1	135	NC	CB5	89	V_{SS}	V_{SS}	181	SA0	SA0
44	NC	CB0	136	V_{DDQ}	V_{DDQ}	90	NC	NC	182	SA1	SA1
45	NC	CB1	137	CK0	CK0	91	SDA	SDA	183	SA2	SA2
46	V_{DD}	V_{DD}	138	$\overline{CK0}$	$\overline{CK0}$	92	SCL	SCL	184	V_{DDSPD}	V_{DDSPD}
47	NC	DQS8	139	V_{SS}	V_{SS}						

NC = No Connect; NU = Not Useable; DU = Do Not Use

1. These pins reserved for unbuffered DDR DIMMs. Systems supporting both unbuffered and registered DIMMs may be connected to an active signal on the baseboard.
2. The TEST pin is reserved for bus analysis probes and is not connected on normal memory modules (DIMMs)

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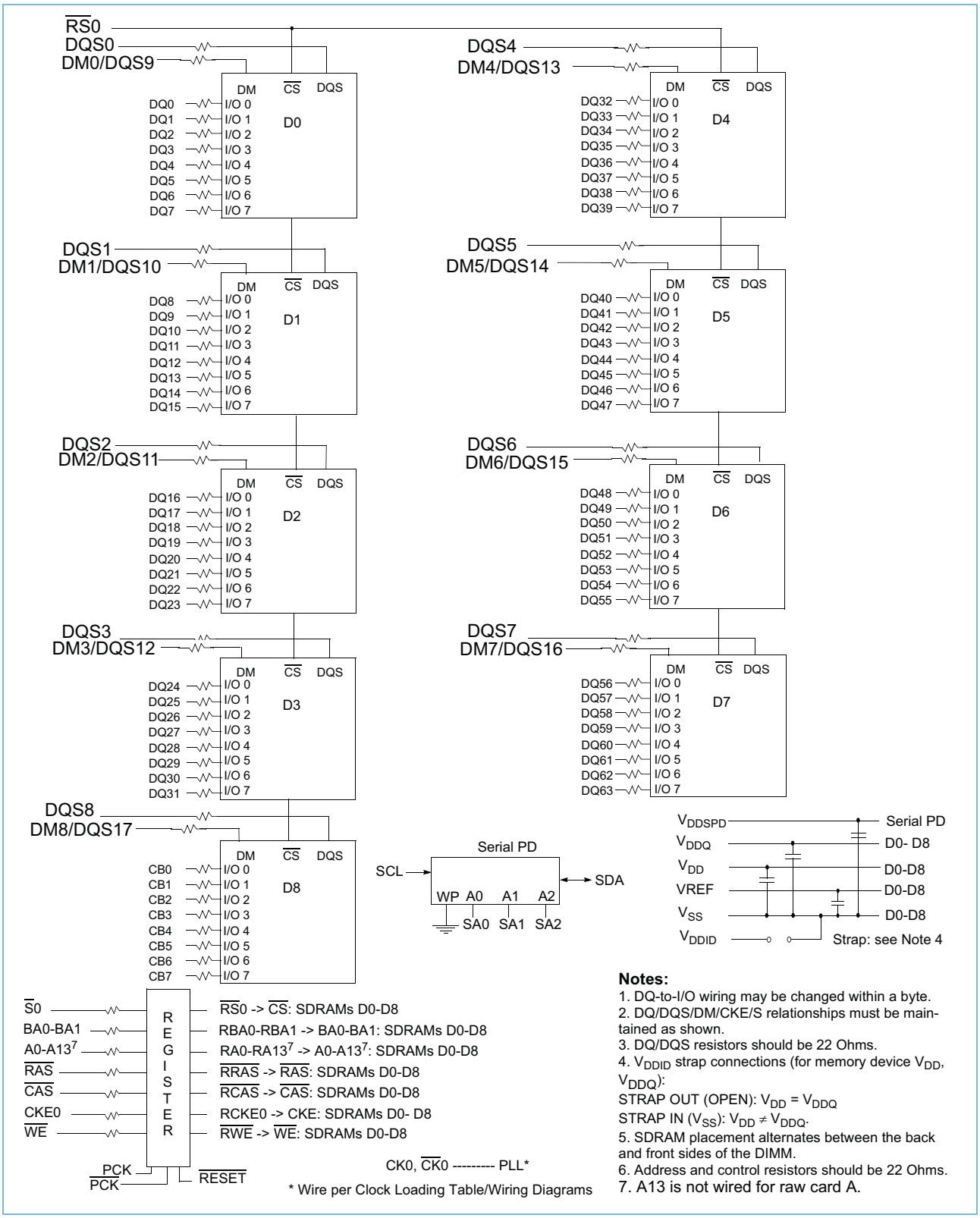
Block Diagram: Raw Card Version A/L (x72 DIMM, populated as one physical bank of x8 DDR SDRAMs)



Notes:
1. DQ-to-I/O wiring may be changed within a byte.
2. DQ/DQS/DM/CKE/S relationships must be maintained as shown.
3. DQ/DQS resistors should be 22 Ohms.
4. V_{DDID} strap connections (for memory device V_{DD}, V_{DDQ}):
STRAP OUT (OPEN): $V_{DD} = V_{DDQ}$
STRAP IN (V_{SS}): $V_{DD} \neq V_{DDQ}$.
5. SDRAM placement alternates between the back and front sides of the DIMM.
6. Address and control resistors should be 22 Ohms.
7. A13 is not wired for raw card A.

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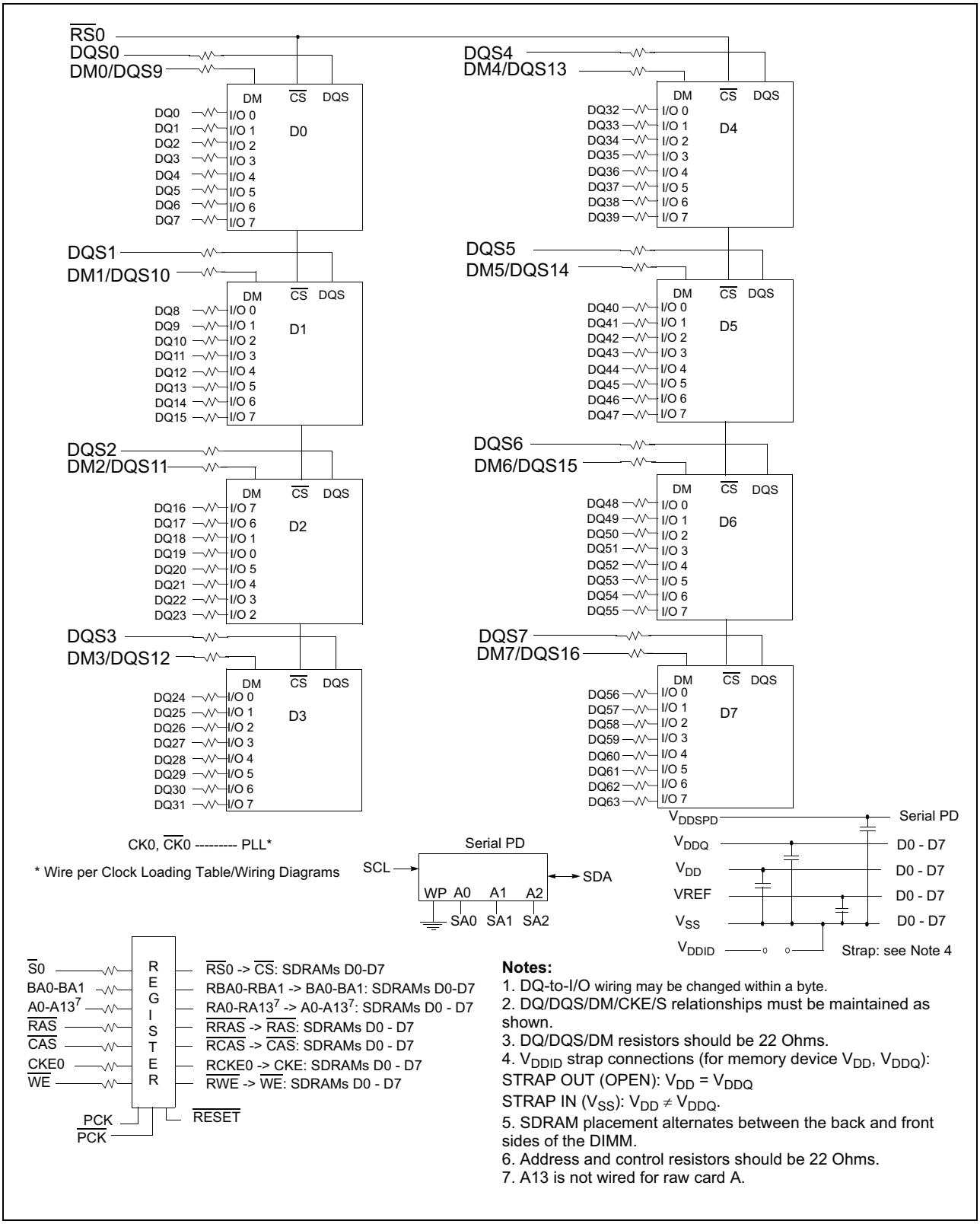
Block Diagram: Raw Card Version A/L (x64 DIMM, populated as one physical bank of x8 DDR SDRAMs)



Notes:
1. DQ-to-I/O wiring may be changed within a byte.
2. DQ/DQS/DM/CKE/S relationships must be maintained as shown.
3. DQ/DQS/DM resistors should be 22 Ohms.
4. V_{DDID} strap connections (for memory device V_{DD}, V_{DDQ}):
STRAP OUT (OPEN): $V_{DD} = V_{DDQ}$
STRAP IN (V_{SS}): $V_{DD} \neq V_{DDQ}$.
5. SDRAM placement alternates between the back and front sides of the DIMM.
6. Address and control resistors should be 22 Ohms.
7. A13 is not wired for raw card A.

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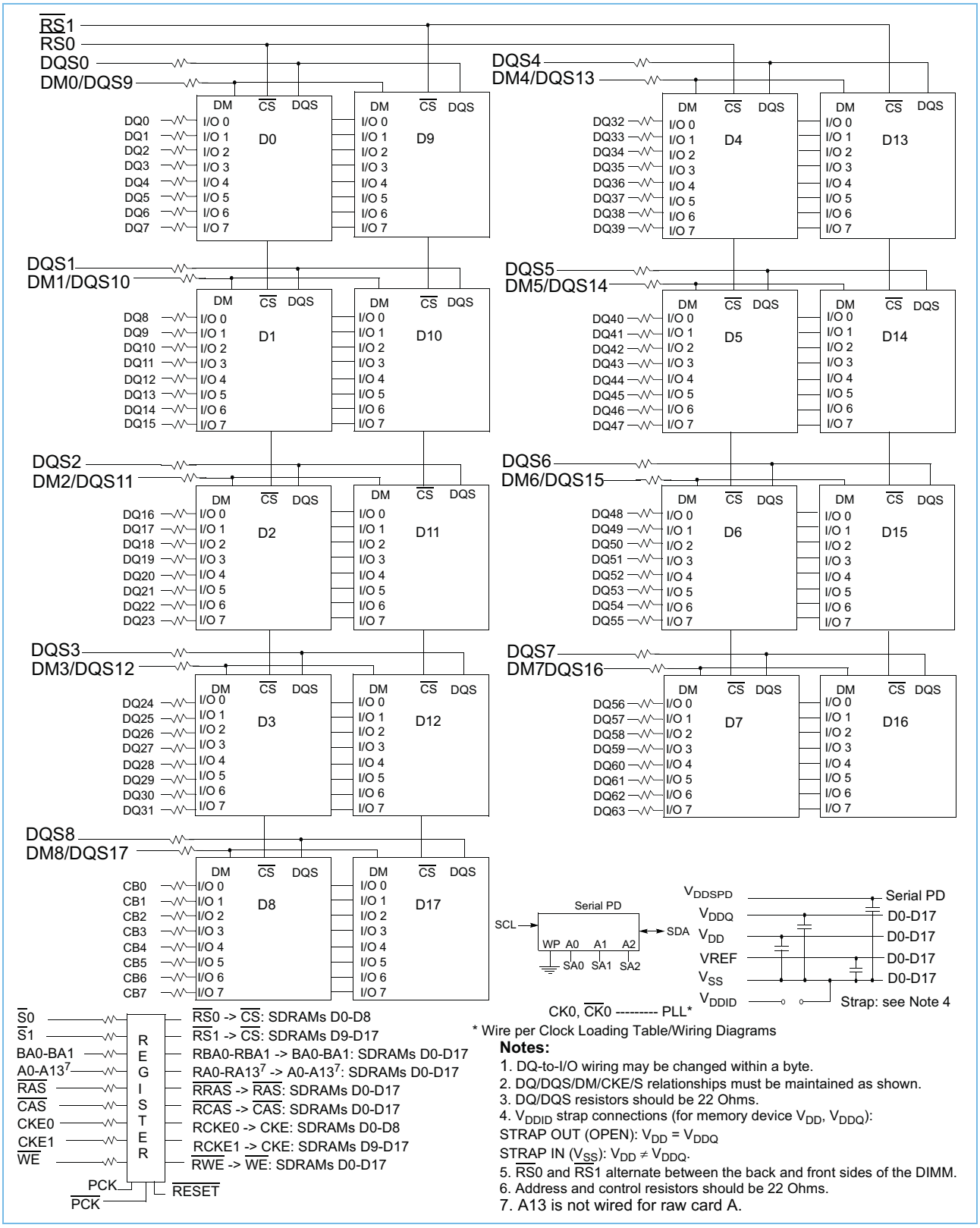
Block Diagram: Raw Card Version A/L (x72 DIMM, populated as two physical banks of x8 DDR SDRAMs)



* Wire per Clock Loading Table/Wiring Diagrams

Notes:

1. DQ-to-I/O wiring may be changed within a byte.
2. DQ/DQS/DM/CKE/S relationships must be maintained as shown.
3. DQ/DQS resistors should be 22 Ohms.
4. V_{DDID} strap connections (for memory device V_{DD}, V_{DDQ}):
   STRAP OUT (OPEN): $V_{DD} = V_{DDQ}$
   STRAP IN (V_{SS}): $V_{DD} \neq V_{DDQ}$.
5. RS0 and RS1 alternate between the back and front sides of the DIMM.
6. Address and control resistors should be 22 Ohms.
7. A13 is not wired for raw card A.

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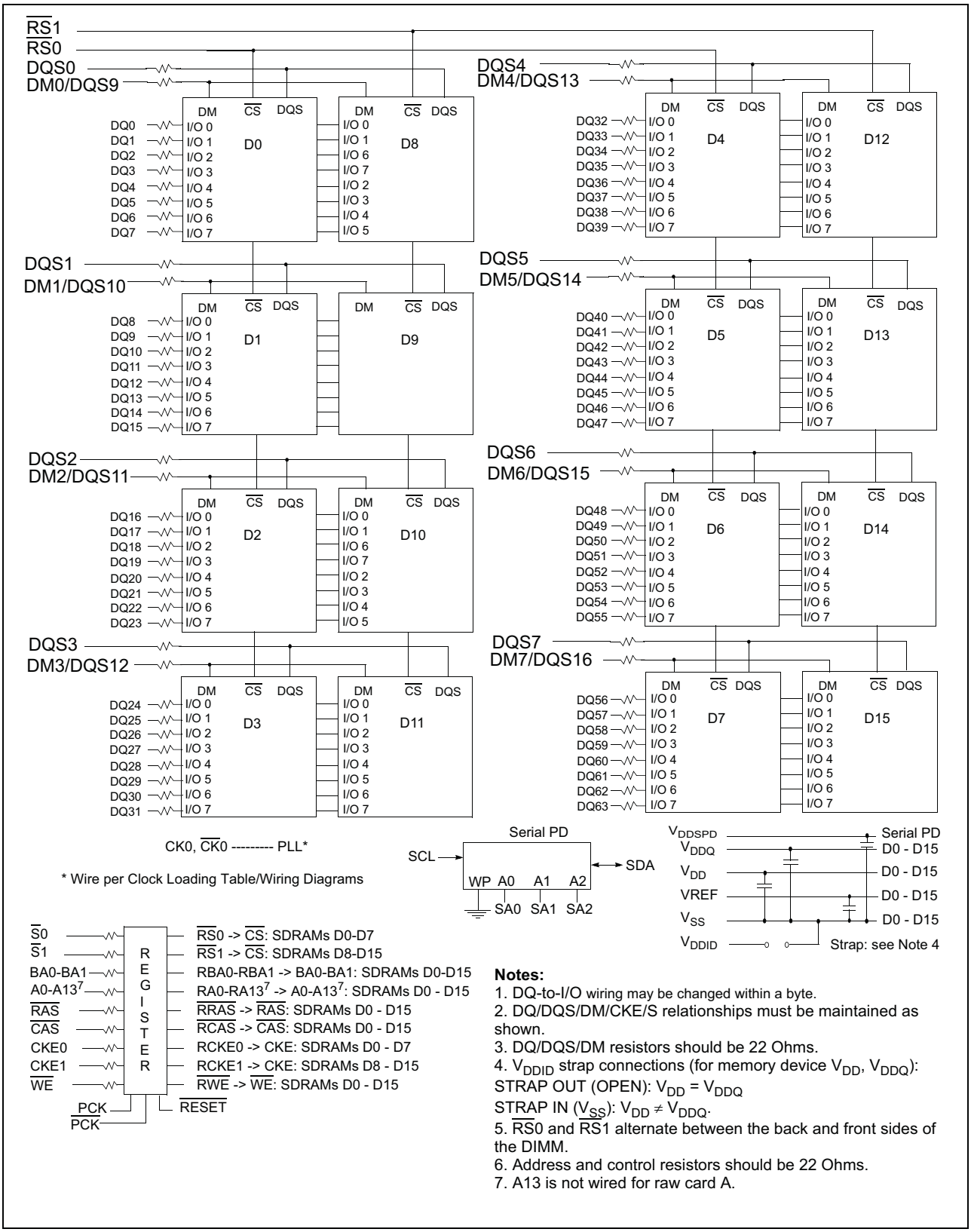
Block Diagram: Raw Card Version A/L (x64 DIMM, populated as two physical banks of x8 DDR SDRAMs)



Notes:

1. DQ-to-I/O wiring may be changed within a byte.
2. DQ/DQS/DM/CKE/S relationships must be maintained as shown.
3. DQ/DQS/DM resistors should be 22 Ohms.
4. V_{DDID} strap connections (for memory device V_{DD}, V_{DDQ}):
STRAP OUT (OPEN): $V_{DD} = V_{DDQ}$
STRAP IN (V_{SS}): $V_{DD} \neq V_{DDQ}$.
5. RS0 and RS1 alternate between the back and front sides of the DIMM.
6. Address and control resistors should be 22 Ohms.
7. A13 is not wired for raw card A.

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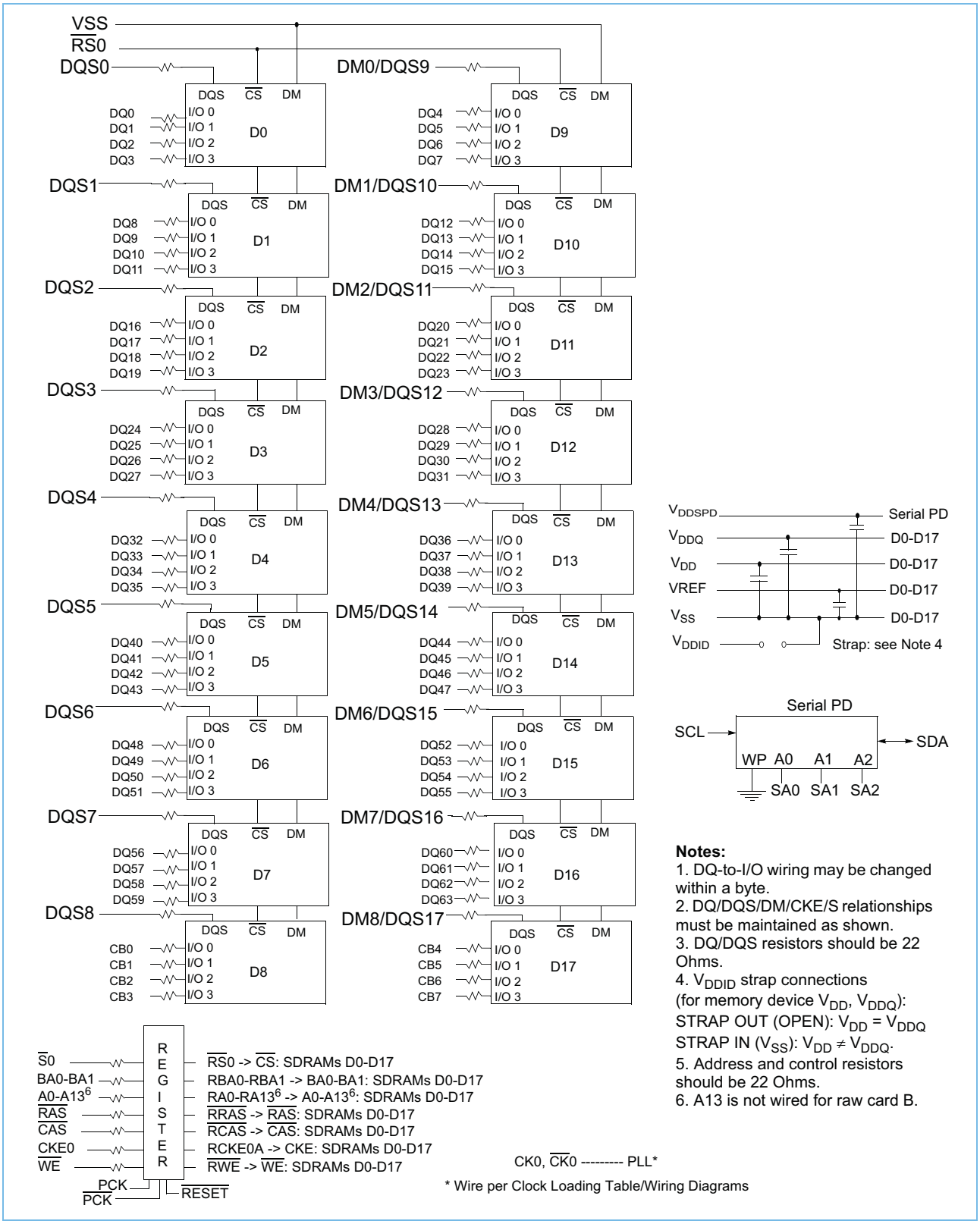
Block Diagram: Raw Card Version B/M (Populated as one physical bank of x4 DDR SDRAMs)



Notes:
1. DQ-to-I/O wiring may be changed within a byte.
2. DQ/DQS/DM/CKE/S relationships must be maintained as shown.
3. DQ/DQS resistors should be 22 Ohms.
4. V_{DDID} strap connections (for memory device V_{DD}, V_{DDQ}):
STRAP OUT (OPEN): $V_{DD} = V_{DDQ}$
STRAP IN (V_{SS}): $V_{DD} \neq V_{DDQ}$.
5. Address and control resistors should be 22 Ohms.
6. A13 is not wired for raw card B.

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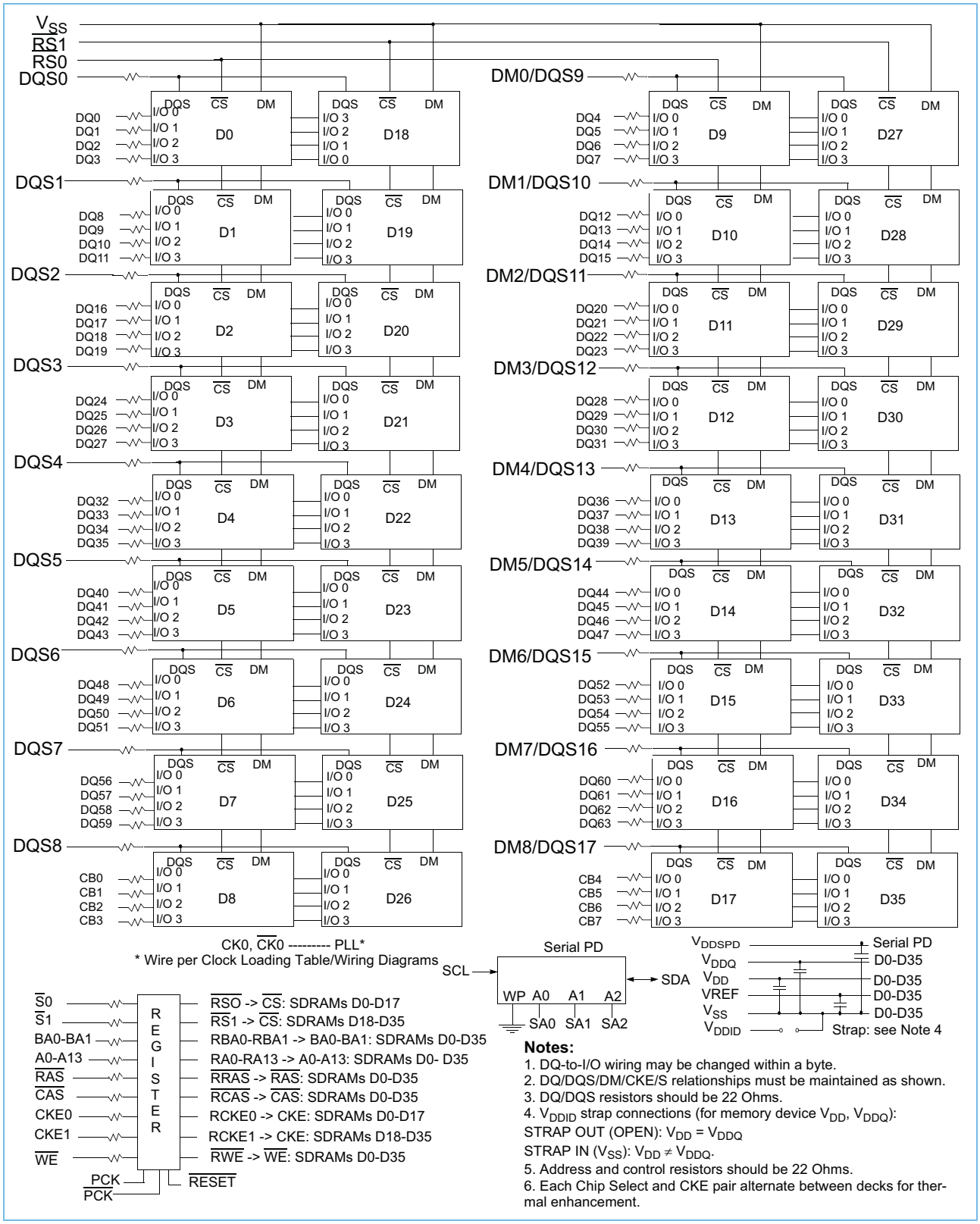
Block Diagram: Raw Card Version N (Populated as two physical banks of x4 DDR SDRAMs)



Notes:

1. DQ-to-I/O wiring may be changed within a byte.
2. DQ/DQS/DM/CKE/S relationships must be maintained as shown.
3. DQ/DQS resistors should be 22 Ohms.
4. V_{DDID} strap connections (for memory device V_{DD}, V_{DDQ}):
STRAP OUT (OPEN): $V_{DD} = V_{DDQ}$
STRAP IN (V_{SS}): $V_{DD} \neq V_{DDQ}$.
5. Address and control resistors should be 22 Ohms.
6. Each Chip Select and CKE pair alternate between decks for thermal enhancement.

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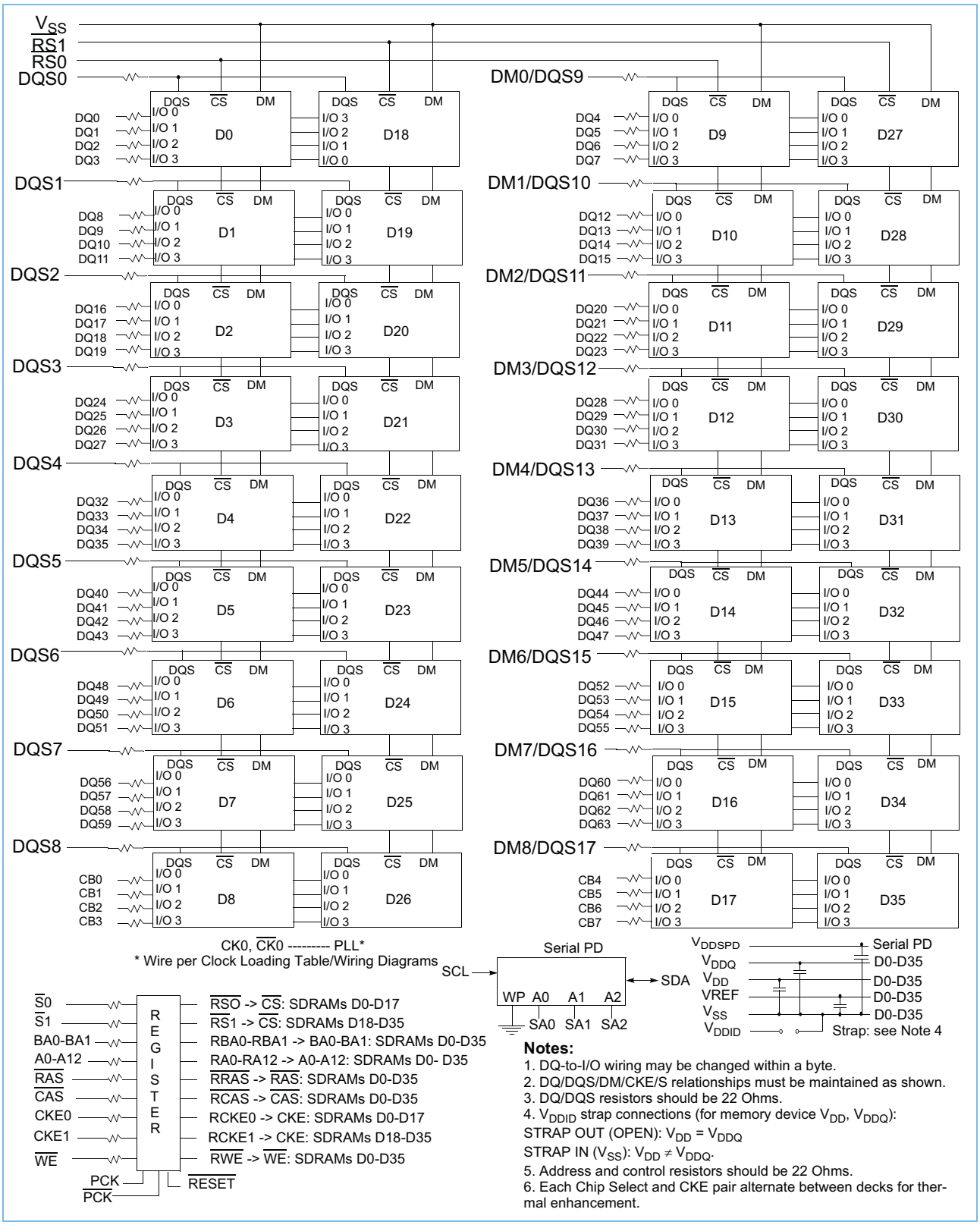
Block Diagram: Raw Card Version C/E (Populated as two physical banks of x4 DDR SDRAMs)



Notes:

1. DQ-to-I/O wiring may be changed within a byte.
2. DQ/DQS/DM/CKE/S relationships must be maintained as shown.
3. DQ/DQS resistors should be 22 Ohms.
4. V_{DDID} strap connections (for memory device V_{DD}, V_{DDQ}):
   STRAP OUT (OPEN): $V_{DD} = V_{DDQ}$
   STRAP IN (V_{SS}): $V_{DD} \neq V_{DDQ}$.
5. Address and control resistors should be 22 Ohms.
6. Each Chip Select and CKE pair alternate between decks for thermal enhancement.

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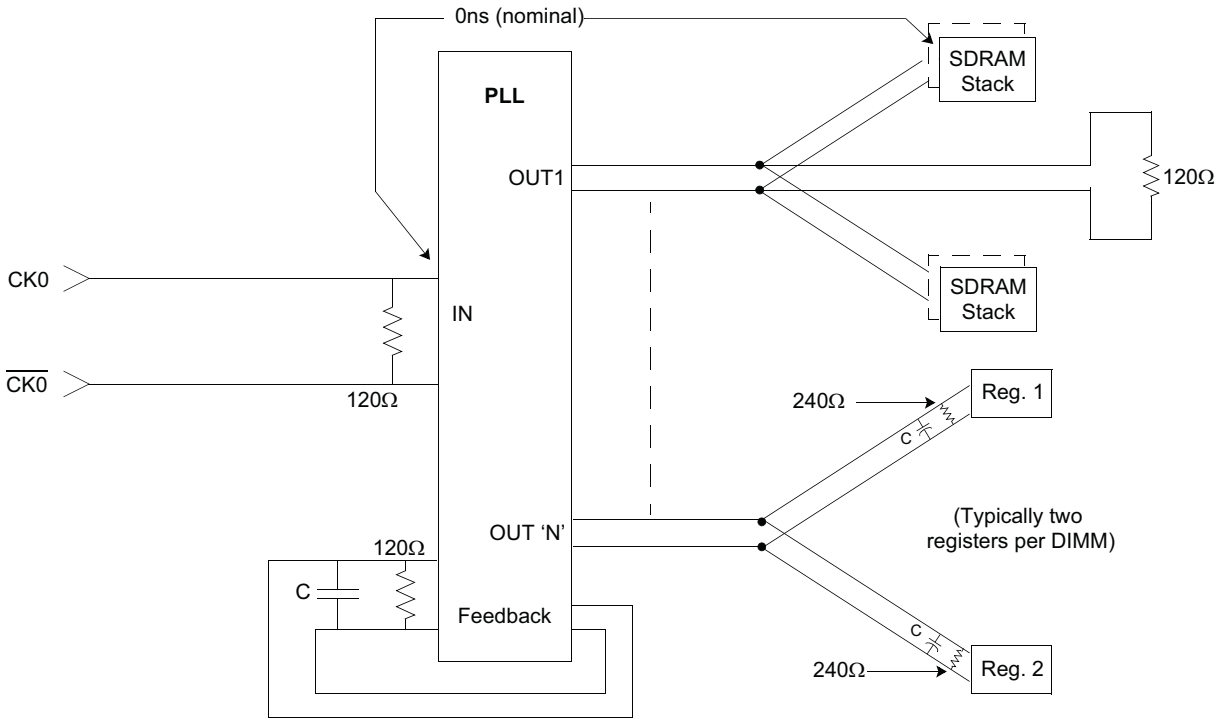
Differential Clock Net Wiring (CK0, $\overline{CK0}$)



1. The clock delay from the input of the PLL clock to the input of any SDRAM or register will be set to 0ns (nominal). See “Clocking Timing Methodology” on page 74.
2. Input, output, and feedback clock lines are terminated from line to line as shown, and not from line to ground.
3. Only one PLL output is shown per output type. Any additional PLL outputs will be wired in a similar manner.
4. Termination resistors for the PLL feedback path clocks are located as close to the input pin of the PLL as possible.

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Register Functional Assignments

Raw Card Versions A, B, and L (Two SSTV16857 1:1 Registers)				Raw Card Versions C and E (Two SSTV16859 1:2 Registers)			
Register 1		Register 2		Register 1		Register 2	
In	Out	In	Out	In	Out	In	Out
A1	RA1	A0	RA0	A1	RA1A	A0	RA0A
A2	RA2	A10	RA10		RA1B		RA0B
A3	RA3	$\overline{S0}$	$\overline{RS0}$	A2	RA2A	A10	RA10A
A4	RA4	$\overline{S1}$	$\overline{RS1}$		RA2B		RA10B
A5	RA5	$\overline{CAS}$	$\overline{RCAS}$	A3	RA3A	$\overline{S0}$	$\overline{RS0A}$
A6	RA6	$\overline{RAS}$	$\overline{RRAS}$		RA3B		$\overline{RS0B}$
A7	RA7	BA0	RBA0	A4	RA4A	$\overline{S1}$	$\overline{RS1A}$
A8	RA8	BA1	RBA1		RA4B		$\overline{RS1B}$
A9	RA9	$\overline{WE}$	$\overline{RWE}$	A5	RA5A	$\overline{CAS}$	$\overline{RCASA}$
A11	RA11				RA5B		$\overline{RCASB}$
A12[1]	RA12			A6	RA6A	$\overline{RAS}$	$\overline{RRASA}$
A13[2]	RA13				RA6B		$\overline{RRASB}$
CKE0	RCKE0			A7	RA7A	BA0	RBA0A
CKE1	RCKE1				RA7B		RBA0B
				A8	RA8A	BA1	RBA1A
					RA8B		RBA1B
				A9	RA9A	$\overline{WE}$	$\overline{RWEA}$
					RA9B		$\overline{RWEB}$
				A11	RA11A		
					RA11B		
				A12[1]	RA12A		
					RA12B		
				CKE0	RCKE0A		
					RCKE0B		
				CKE1	RCKE1A		
					RCKE1B		

1. Only used with 256Mbit, 512Mbit, 1Gbit DDR SDRAMs.
2. Only used with 1Gbit DDR SDRAMs.

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Register Functional Assignments

Raw Card Versions M (Two SSTV16857 1:1 Registers)				Raw Card Versions N (One SSTV32852[3] 1:2 Registers)			
Register 1		Register 2		Register 1			
In	Out	In	Out	In	Out	In	Out
A2	RA2	A0	RA0	A1	RA1A	CKE0	RCKE0A
A3	RA3	A1	RA1		RA1B		RCKE0B
A4	RA4	A10	RA10	A2	RA2A	CKE1	RCKE1A
A5	RA5	S0	R$\overline{S}$0		RA2B		RCKE1B
A6	RA6	$\overline{CAS}$	R$\overline{CAS}$	A3	RA3A	A0	RA0A
A7	RA7	$\overline{RAS}$	R$\overline{RAS}$		RA3B		RA0B
A8	RA8	BA0	RBA0	A4	RA4A	A10	RA10A
A9	RA9	BA1	RBA1		RA4B		RA10B
A11	RA11	$\overline{WE}$	$\overline{RWE}$	A5	RA5A	$\overline{S}$0	$\overline{RS0}$A
A12[1]	RA12				RA5B		$\overline{RS0}$B
A13[2]	RA13			A6	RA6A	$\overline{S}$1	$\overline{RS1}$A
CKE0	RCKE0				RA6B		$\overline{RS1}$B
				A7	RA7A	$\overline{CAS}$	$\overline{RCAS}$A
					RA7B		$\overline{RCAS}$B
				A8	RA8A	$\overline{RAS}$	$\overline{RRAS}$A
					RA8B		$\overline{RRAS}$B
				A9	RA9A	BA0	RBA0A
					RA9B		RBA0B
				A11	RA11A	BA1	RBA1A
					RA11B		RBA1B
				A12[1]	RA12A	$\overline{WE}$	$\overline{RWE}$A
					RA12B		$\overline{RWE}$B
				A13[2]	RA13A		
					RA13B		

1. Only used with 256Mbit, 512Mbit, 1Gbit DDR SDRAMs.
2. Only used with 1Gbit DDR SDRAMs
3. Reference to the JC40 nomenclature and ballots for support chips (Registers and PLLs)

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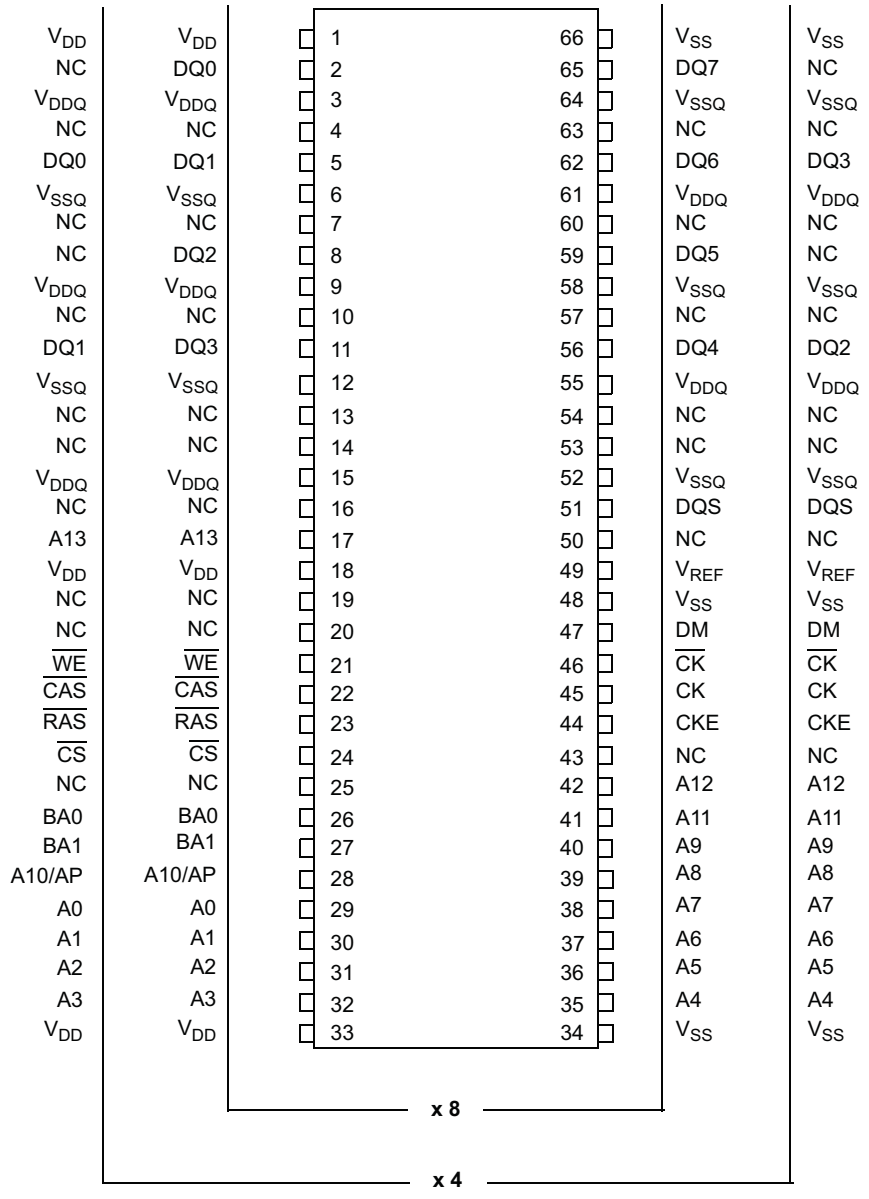
Component Details

Pin Assignments for 64Mb, 128Mb, 256Mb, 512Mb and 1Gb DDR SDRAM Planar Components (Top View)



Note: This pin assignment is for use with planar DIMMs.

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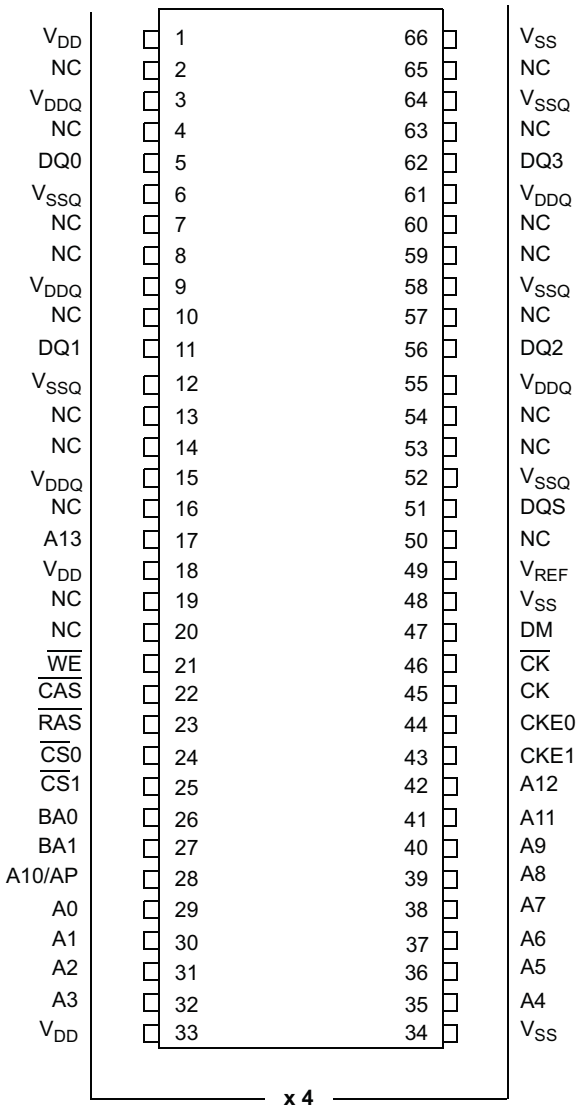
Pin Assignments for 64Mb, 128Mb, 256Mb, 512Mb and 1Gb DDR SDRAM 2-High Stack Package (Top View)



Note: This pin assignment is for use with stacked DIMMs.

DDR SDRAM Component Specifications

The DDR SDRAM components used with this DIMM design specification are intended to be consistent with JEDEC standard JESD79. DDR SDRAM component specification violations also violate the DDR SDRAM Registered DIMM specifications.

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Register Component Specifications

Please refer to the vendor register data sheets for all technical specifications and requirements. Below is a chart explaining which registers should be used on each DIMM type.

DIMM Register Use

Raw Card Version	# of Banks	# of SDRAMs per output	Register Type	Package	Quantity
A/L	1	9	SSTV16857 (1:1 14-bit SSTL)	TSSOP	2
	2	18	SSTV16857 (1:1 14-bit SSTL)	TSSOP	2
B/M	1	18	SSTV16857 (1:1 14-bit SSTL)	TSSOP	2
N	2	18	SSTV32852 (1:2 24-bit SSTL)	BGA	1
C/E	2	18	SSTV16859 (1:2 13-bit SSTL)	TSSOP	2

The following specifications for the register are critical for proper operation of the DDR SDRAM Registered DIMMs. These are meant to be a subset of the parameters for the device. Detailed information on both the 1:1 and 1:2 registers, including driver characteristics, has been standardized at the JEDEC JC-40 Committee, as SSTV16857 (1:1), SSTV16859 (1:2) and SSTV32852(1:2).

Critical Register Specifications

Register	Symbol	Parameter	Conditions	T_A = 0-70° C V_{DD} = 2.5V ± 0.2V		Units	Notes
				Min	Max		
SSTV16857 (1:1 14-bit) and SSTV16859 (1:2 13-bit) and SSTV32852 (1:2 24-bit)	t_{CK}	Clock Frequency		60	170	MHz	
	t_{PD}	Clock to Output Time	30pF to GND and 50 Ohms to V_{TT}	1.1	2.8	ns	4
	t_{RST}	Reset to Output Time		—	5	ns	
	t_{SL}	Output Slew Rate	30pF to GND and 50 Ohms to $V_{TT}/2$	0.5	4	V/ns	
	t_{su}	Setup time, fast slew rate (see Notes 1 and 3)		0.75	—	ns	1, 3
		Setup time, slow slew rate (see Notes 2 and 3)		0.9	—	ns	2, 3
	t_h	Hold time, fast slew rate (see Notes 1 and 3)		0.75	—		1, 3
		Hold time, slow slew rate (see Notes 2 and 3)		0.9	—		2, 3
	$C_{IN(CK)}$	Clock Input Capacitance		2.5	3.5	pF	
	$C_{IN(data)}$	Data Input Capacitance		2.5	3.5	pF	

1. For data signal, input slew rate ≥ 1 V/ns.
2. For data signal, input slew rate ≥ 0.5 V/ns and < 1V/ns.
3. For CLK and $\overline{CLK}$ signals, input slew rates are ≥ 1 V/ns.
4. For the SSTV32852, t_{PD} is 3.1ns max

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Register Sourcing

This document is not intended to be an approved vendor list for support chip components. Although it is recommended that all DDR SDRAM RDIMM registers meet the specifications documented above, it is up to each DIMM producer to select the registers and register vendors which meet these requirements, and to guarantee robustly designed DIMMs. In order to facilitate industry consistency, the functionality and technical requirements of both the 1:1 and 1:2 registers have been standardized at JEDEC in JC-40, as SSTV16857 (1:1), SSTV16859 (1:2) and SSTV32852(1:2).

PLL Component Specifications

Please refer to the vendor PLL data sheets for all technical specifications and requirements. Below is a chart explaining which PLLs are used on each DIMM type.

DIMM PLL Use

Raw Card Version	# of Banks	# of SDRAMs per output	PLL Type	Package	Quantity
A/L	1	2[1]	CDCV857 (1:10, 2.5 Volt)	TSSOP	1
	2	2	CDCV857 (1:10, 2.5 Volt)	TSSOP	1
B/M	1	2	CDCV857 (1:10, 2.5 Volt)	TSSOP	1
N	2	4	CDCV857 (1:10, 2.5 Volt)	TSSOP	1
C/E	2	4	CDCV857 (1:10, 2.5 Volt)	TSSOP	1

1. In the case of the One-Bank A/L Card, a padding capacitor is added across each SDRAM clock and $\overline{\text{clock}}$ pair to ensure that timing is the same for One and Two-Bank DIMMs. Also, on X64 A cards, a padding capacitor is used across the clock pair for the depopulated ninth SDRAM(s) position(s).

The following specifications for the PLL are critical for proper operation of the DDR SDRAM Registered DIMMs. These are meant to be a subset of the parameters for the device. Detailed information on this part, including driver characteristics, has been standardized at the JEDEC JC-40 Committee, as CDCV857 (Item #25).

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Critical PLL Specifications

Device	Symbol	Parameter	Conditions	T_A = 0-70° C V_{DD} = 2.5V ± 0.2V		Units	Notes
				Min	Max		
CDCV857 (1:10, 2.5 Volt)	f_{CK}	Operating Clock Frequency		60	170	MHz	1
	f_{CK}	Application Clock Frequency		95	170	MHz	1
	t_{SPE}	Static Phase Error	Application Load	-50	50	ps	2
	t_{SK}	Output Clock Skew	Application Load	—	100	ps	2
	t_{SL}	Output Slew Rate		1	3	V/ns	2
	t_{jit}(per)	Period		-75	75	ps	3, 4
	t_{jit}(cc)	Cycle-to-Cycle					
	t_{jit}(hper)	Half-period		-100	100		4
	t_{STAB}	PLL Stabilization Time			100	µs	
	C_{IN}	Input Capacitance		2.5	3.5	pF	

1. The PLL used on the registered DIMM needs to support SSC synthesizers with a Modulation Frequency of 30 to 50KHz and a Clock Frequency Deviation of -0.5%. PLL designs should target the following values:
   - Greater than 2MHz PLL loop bandwidth
   - Less than -0.031 degrees of phase angle
2. The application load is defined in *Differential Clock Net Structures* on page 38.
3. Period jitter defines the largest variation in clock period, around a nominal clock period.
4. Period jitter and half-period jitter are independent from each other.

PLL Sourcing

This document is not intended to be an approved vendor list for support chip components. Although it is recommended that all DDR SDRAM Registered DIMM PLLs meet the specifications documented above, it is up to each DIMM producer to select the PLL and PLL vendors which meet these requirements, and to guarantee robustly operating DIMMs. In order to facilitate industry consistency, the functionality and technical requirements of this part have been standardized at JEDEC in JC-40, as CDCV857 (Item #25).

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Registered DIMM Details

DDR SDRAM Module Configurations (Reference Designs) (Part 1 of 3)

Raw Card Version	DIMM		SDRAM		# of SDRAMs	SDRAM Package Type	# of Physical Banks	# of Banks in SDRAM	# of Address bits row/col	FET Switch
	Capacity	Organization	Density	Organization						
A	64MB	8Mx72	64Mbit	8Mx8	9	66 lead TSOP	1	4	12/9	No
	128MB	16Mx72	128Mbit	16Mx8	9	66 lead TSOP	1	4	12/10	No
	256MB	32Mx72	256Mbit	32Mx8	9	66 lead TSOP	1	4	13/10	No
	512MB	64Mx72	512Mbit	64Mx8	9	66 lead TSOP	1	4	13/11	No
	128MB	16Mx72	64Mbit	8Mx8	18	66 lead TSOP	2	4	12/9	No
	256MB	32Mx72	128Mbit	16Mx8	18	66 lead TSOP	2	4	12/10	No
	512MB	64Mx72	256Mbit	32Mx8	18	66 lead TSOP	2	4	13/10	No
	1GB	128Mx72	512Mbit	64Mx8	18	66 lead TSOP	2	4	13/11	No
	64MB	8Mx64	64Mbit	8Mx8	8	66 lead TSOP	1	4	12/9	No
	128MB	16Mx64	128Mbit	16Mx8	8	66 lead TSOP	1	4	12/10	No
	256MB	32Mx64	256Mbit	32Mx8	8	66 lead TSOP	1	4	13/10	No
	512MB	64Mx64	512Mbit	64Mx8	8	66 lead TSOP	1	4	13/11	No
	128MB	16Mx64	64Mbit	8Mx8	16	66 lead TSOP	2	4	12/9	No
	256MB	32Mx64	128Mbit	16Mx8	16	66 lead TSOP	2	4	12/10	No
	512MB	64Mx64	256Mbit	32Mx8	16	66 lead TSOP	2	4	13/10	No
	1GB	128Mx64	512Mbit	64Mx8	16	66 lead TSOP	2	4	13/11	No

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DDR SDRAM Module Configurations (Reference Designs) (Part 2 of 3)

Raw Card Version	DIMM		SDRAM		# of SDRAMs	SDRAM Package Type	# of Physical Banks	# of Banks in SDRAM	# of Address bits row/col	FET Switch
	Capacity	Organization	Density	Organization						
L	64MB	8Mx72	64Mbit	8Mx8	9	66 lead TSOP	1	4	12/9	No
	128MB	16Mx72	128Mbit	16Mx8	9	66 lead TSOP	1	4	12/10	No
	256MB	32Mx72	256Mbit	32Mx8	9	66 lead TSOP	1	4	13/10	No
	512MB	64Mx72	512Mbit	64Mx8	9	66 lead TSOP	1	4	13/11	No
	1GB	128Mx72	1Gb	128Mx8	9	66 lead TSOP	1	4	14/11	No
	128MB	16Mx72	64Mbit	8Mx8	18	66 lead TSOP	2	4	12/9	No
	256MB	32Mx72	128Mbit	16Mx8	18	66 lead TSOP	2	4	12/10	No
	512MB	64Mx72	256Mbit	32Mx8	18	66 lead TSOP	2	4	13/10	No
	1GB	128Mx72	512Mbit	64Mx8	18	66 lead TSOP	2	4	13/11	No
	2GB	256Mx72	1Gb	128Mx8	18	66 lead TSOP	2	4	14/11	No
	64MB	8Mx64	64Mbit	8Mx8	8	66 lead TSOP	1	4	12/9	No
	128MB	16Mx64	128Mbit	16Mx8	8	66 lead TSOP	1	4	12/10	No
	256MB	32Mx64	256Mbit	32Mx8	8	66 lead TSOP	1	4	13/10	No
	512MB	64Mx64	512Mbit	64Mx8	8	66 lead TSOP	1	4	13/11	No
	1GB	128Mx64	1Gb	128Mx8	8	66 lead TSOP	1	4	14/11	No
	128MB	16Mx64	64Mbit	8Mx8	16	66 lead TSOP	2	4	12/9	No
	256MB	32Mx64	128Mbit	16Mx8	16	66 lead TSOP	2	4	12/10	No
	512MB	64Mx64	256Mbit	32Mx8	16	66 lead TSOP	2	4	13/10	No
	1GB	128Mx64	512Mbit	64Mx8	16	66 lead TSOP	2	4	13/11	No
	2GB	256Mx64	1Gb	128Mx8	16	66 lead TSOP	2	4	14/11	No
B	128MB	16Mx72	64Mbit	16Mx4	18	66 lead TSOP	1	4	12/10	No
	256MB	32Mx72	128Mbit	32Mx4	18	66 lead TSOP	1	4	12/11	No
	512MB	64Mx72	256Mbit	64Mx4	18	66 lead TSOP	1	4	13/11	No
	1GB	128Mx72	512Mbit	128Mx4	18	66 lead TSOP	1	4	13/12	No
M	128MB	16Mx72	64Mbit	16Mx4	18	66 lead TSOP	1	4	12/10	No
	256MB	32Mx72	128Mbit	32Mx4	18	66 lead TSOP	1	4	12/11	No
	512MB	64Mx72	256Mbit	64Mx4	18	66 lead TSOP	1	4	13/11	No
	1GB	128Mx72	512Mbit	128Mx4	18	66 lead TSOP	1	4	13/12	No
	2GB	256Mx72	1Gb	256Mx4	18	66 lead TSOP	1	4	14/12	No
C	256MB	32Mx72	64Mbit	16Mx4	36	66 lead stacked TSOP	2	4	12/10	No
	512MB	64Mx72	128Mbit	32Mx4	36	66 lead stacked TSOP	2	4	12/11	No
	1GB	128Mx72	256Mbit	64Mx4	36	66 lead stacked TSOP	2	4	13/11	No
	2GB	256Mx72	512Mbit	128Mx4	36	66 lead stacked TSOP	2	4	13/12	No

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DDR SDRAM Module Configurations (Reference Designs) (Part 3 of 3)

Raw Card Version	DIMM		SDRAM		# of SDRAMs	SDRAM Package Type	# of Physical Banks	# of Banks in SDRAM	# of Address bits row/col	FET Switch
	Capacity	Organization	Density	Organization						
N	256MB	32Mx72	64Mbit	16Mx4	36	66 lead stacked TSOP	2	4	12/10	No
	512MB	64Mx72	128Mbit	32Mx4	36	66 lead stacked TSOP	2	4	12/11	No
	1GB	128Mx72	256Mbit	64Mx4	36	66 lead stacked TSOP	2	4	13/11	No
	2GB	256Mx72	512Mbit	128Mx4	36	66 lead stacked TSOP	2	4	13/12	No
	4GB	512Mx72	1Gb	256Mx4	36	66 lead stacked TSOP	2	4	14/12	No
E	256MB	32Mx72	64Mbit	16Mx4	36	66 lead stacked TSOJ	2	4	12/10	No
	512MB	64Mx72	128Mbit	32Mx4	36	66 lead stacked TSOJ	2	4	12/11	No
	1GB	128Mx72	256Mbit	64Mx4	36	66 lead stacked TSOJ	2	4	13/11	No
	2GB	256Mx72	512Mbit	128Mx4	36	66 lead stacked TSOJ	2	4	13/12	No

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Input Loading Matrix

Signal Names	Input Device	Raw Card Version		
		A/L	B/M	C/E/N
Clock (CK0)	PLL	1	1	1
CKE0	Register	1	1	1
CKE1	Register	1 or 0	N/A	1
Addr/RAS/CAS/BA/WE	Register	1	1	1
Chip Selects	Register	1	1	1
DQ/DQS	DDR SDRAM	1 or 2	1	2
DM	DDR SDRAM	1 or 2	N/A	N/A
SCL/SDA/SA	EEPROM	1	1	1

DDR Registered Design File Releases

‘Reference’ Design file updates will be released as needed. This Registered DIMM specification will reflect the most recent Design files, but may also be updated to reflect clarifications to the specification only; in these cases the Design files will not be updated. The following table outlines the most recent Design file releases.

Note: Future Design file releases will include both a date and a revision label. All changes to the Design file are also documented in detail within the ‘read-me’ file.

Raw Card Version	Specification Revision	Applicable Design File	Notes
A	0.6	A0	Release on 12/15/99
	1.0	A1	Release on 03/31/00
B	0.6	B1	Release on 11/26/99
	1.0	B2	Release on 03/31/00
C	0.9[1]	C1	Release on 02/25/00
	0.95 (JEDEC ballot)	C2[2]	Release on 06/23/00
	1.0	C3[2]	Release on 08/01/00
E	1.0	TBD	Original Release
L	1.2	1.0	Release on 10/05/01
M	1.2	1.0	Release on 10/05/01
N	1.3	N0	Release on 11/30/01

1. With exception of the cross section which utilized Revision 0.6.
2. The C2 release is missing the gnd via connection for impedance coupons. The C3 release corrects this error. This omission has no bearing on the use of this design level in system applications.

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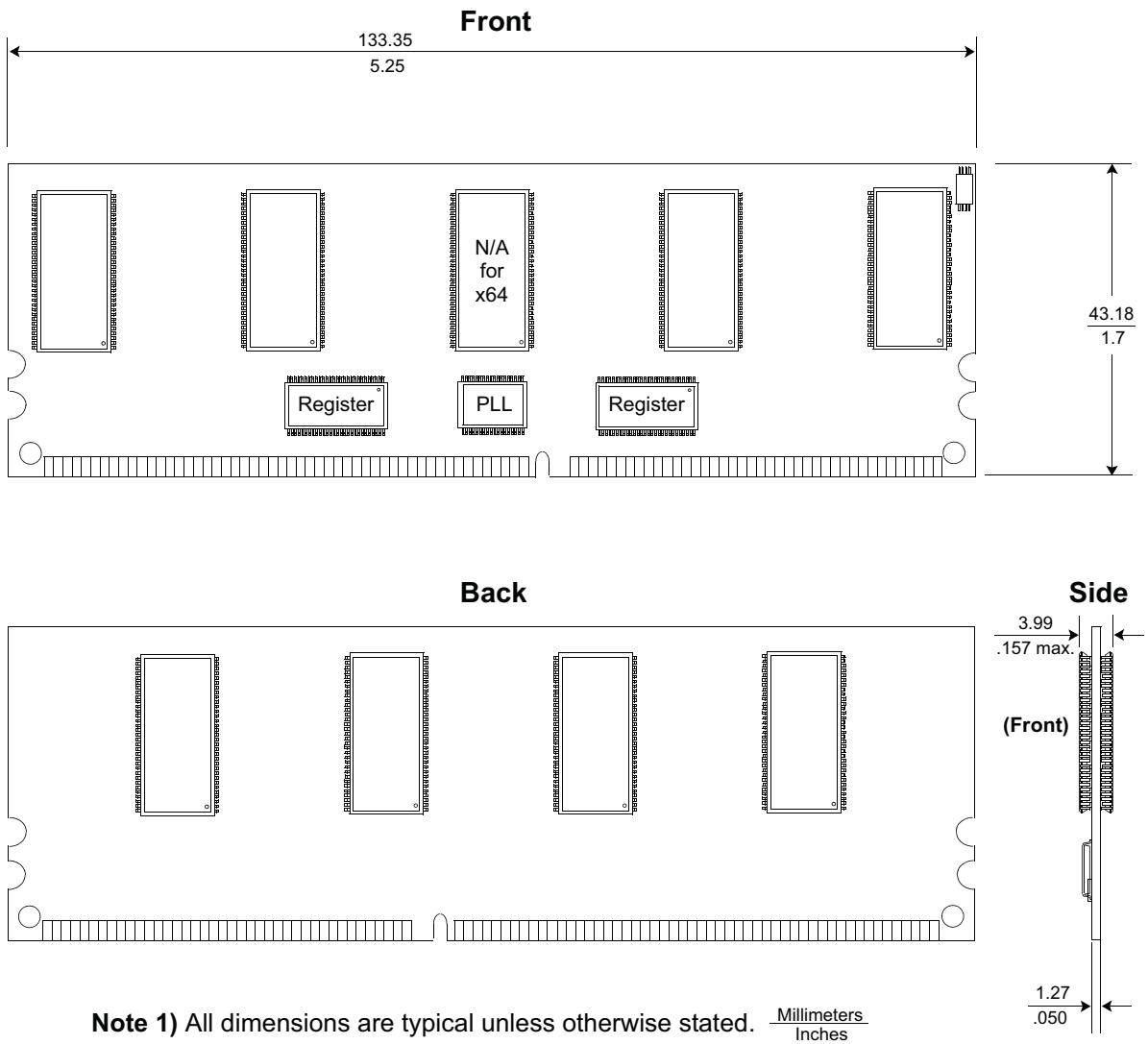
Component Types and Placement

Components shall be surface mounted on both sides of the PCB and positioned on the PCB to meet the minimum and maximum trace lengths required for DDR SDRAM signals. Bypass capacitors for DDR SDRAM devices must be located near the device power pins. In two-bank, x4 based DDR SDRAM designs, the second DDR SDRAM bank devices will be stacked on the first DDR SDRAM bank devices.

The following layouts suggest placement for the Raw Card Versions A, B, C, E, L,M and N. Exact spacing is not provided, but should be based on manufacturing constraints and signal routing constraints imposed by this design guide.

Example Raw Card Versions A (1 Physical Bank) Component Placement



Note 1) All dimensions are typical unless otherwise stated. Millimeters / Inches
Note 2) All dimensions are reference only and should be referred to JEDEC Publication95 MO-206 for detailed dimensions.

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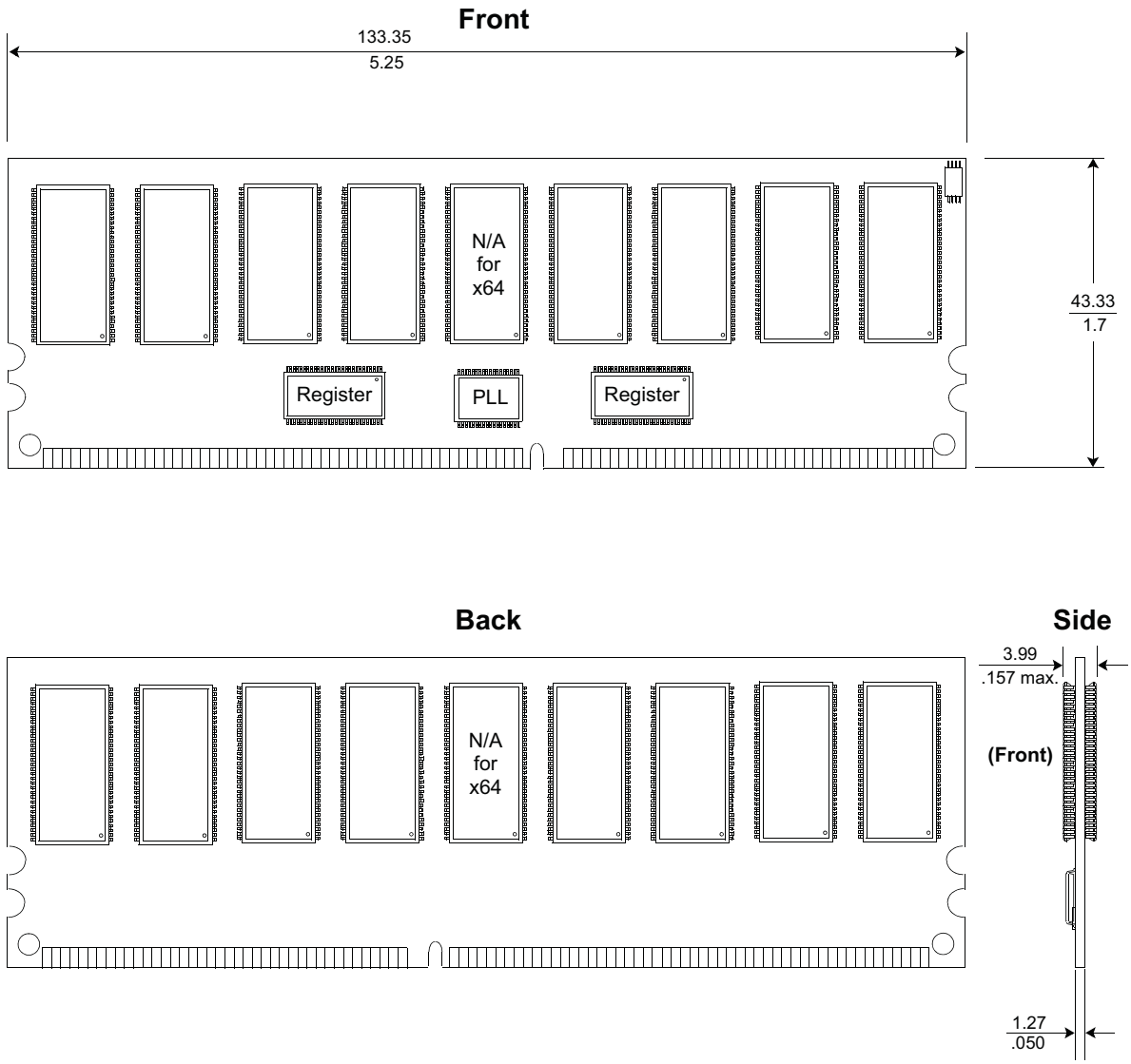
Example Raw Card Versions A (2 Physical Banks) Component Placement



Note 1) All dimensions are typical unless otherwise stated. Millimeters / Inches

Note 2) All dimensions are reference only and should be referred to JEDEC Publication95 MO-206 for detailed dimensions.

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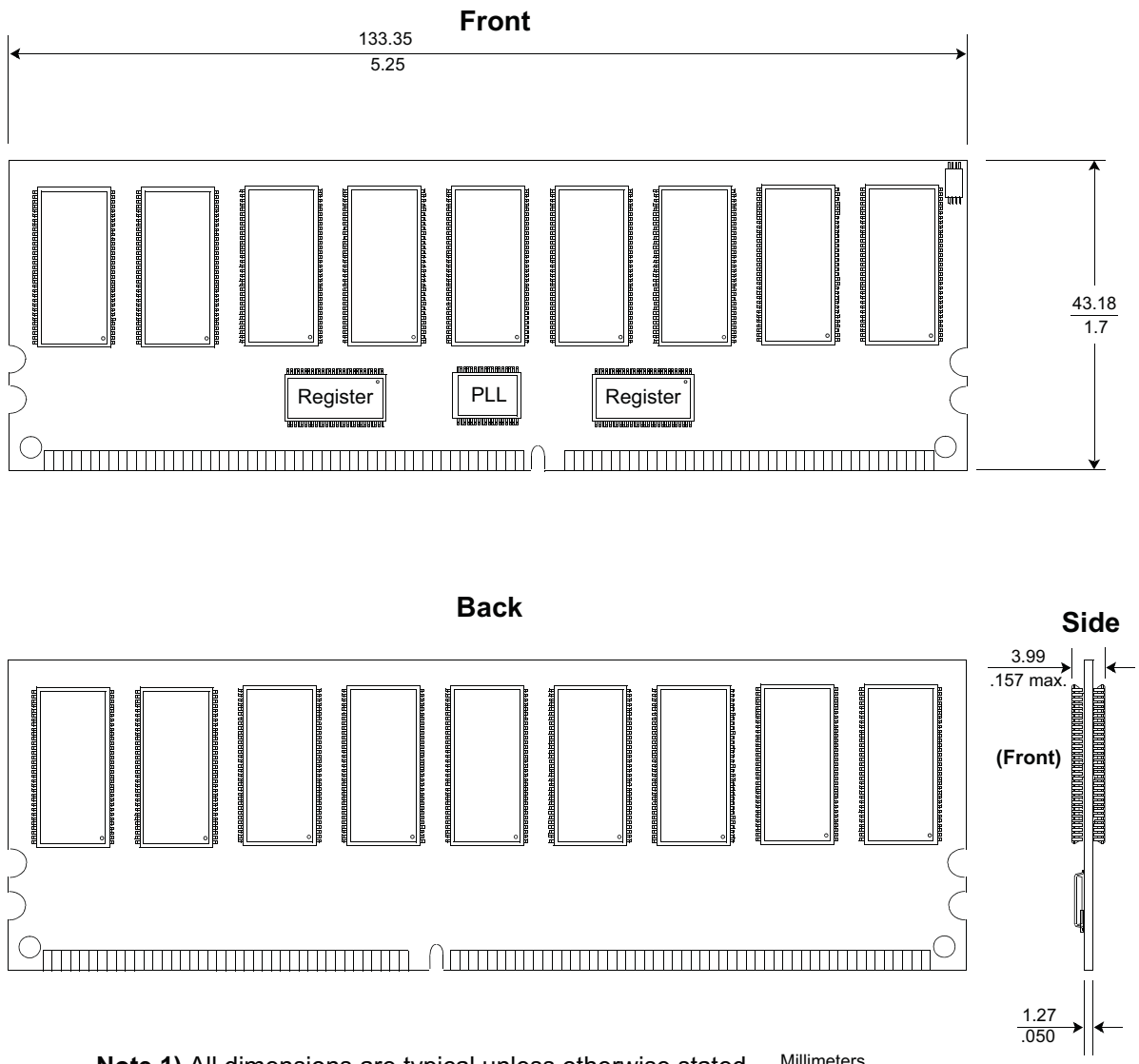
Example Raw Card Version B Component Placement



Note 1) All dimensions are typical unless otherwise stated. Millimeters / Inches

Note 2) All dimensions are reference only and should be referred to JEDEC Publication95 MO-206 for detailed dimensions.

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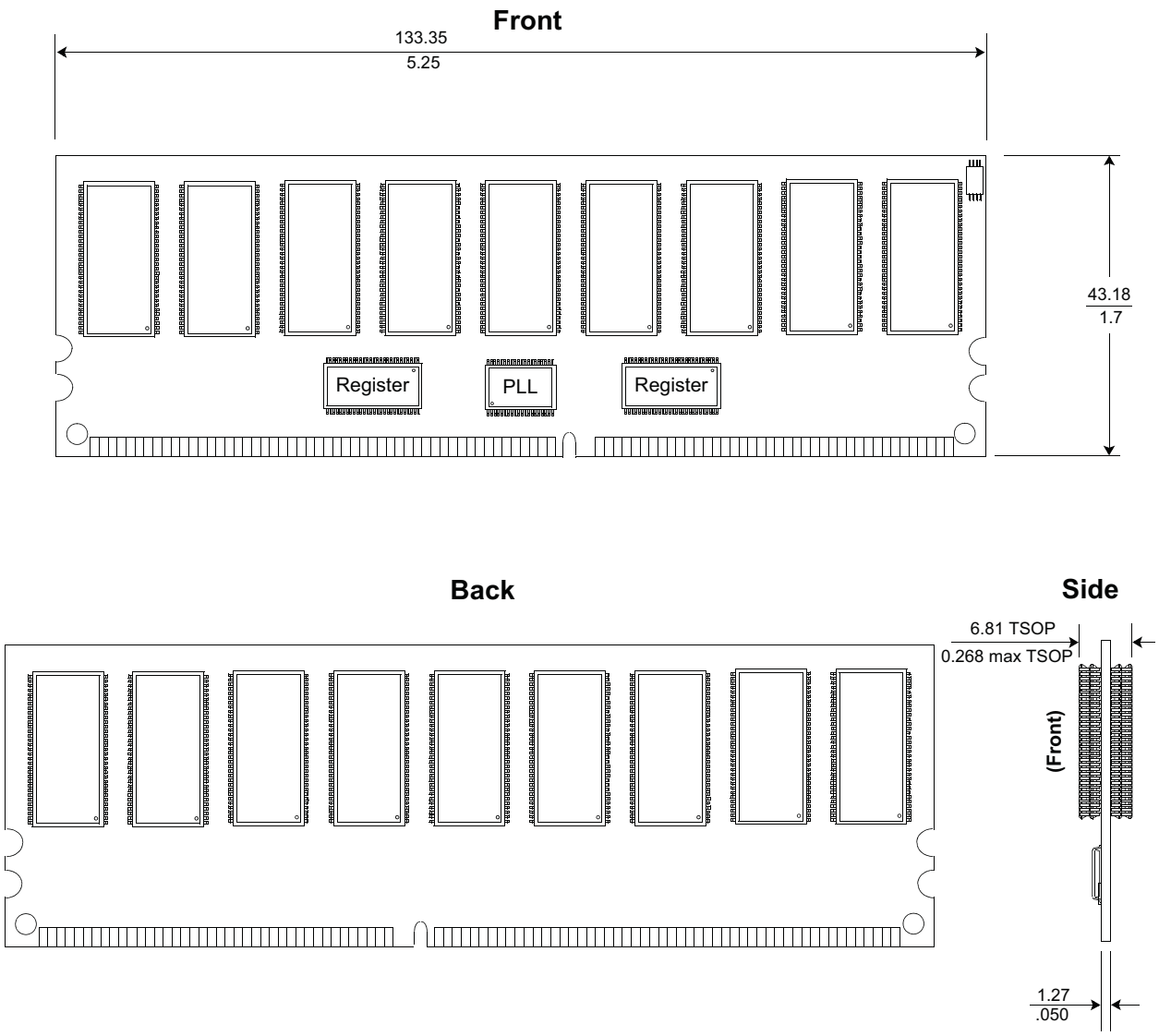
Example Raw Card Version C/E Component Placement



Note 1) All dimensions are typical unless otherwise stated. Millimeters / Inches

Note 2) All dimensions are reference only and should be referred to JEDEC Publication95 MO-206 for detailed dimensions.

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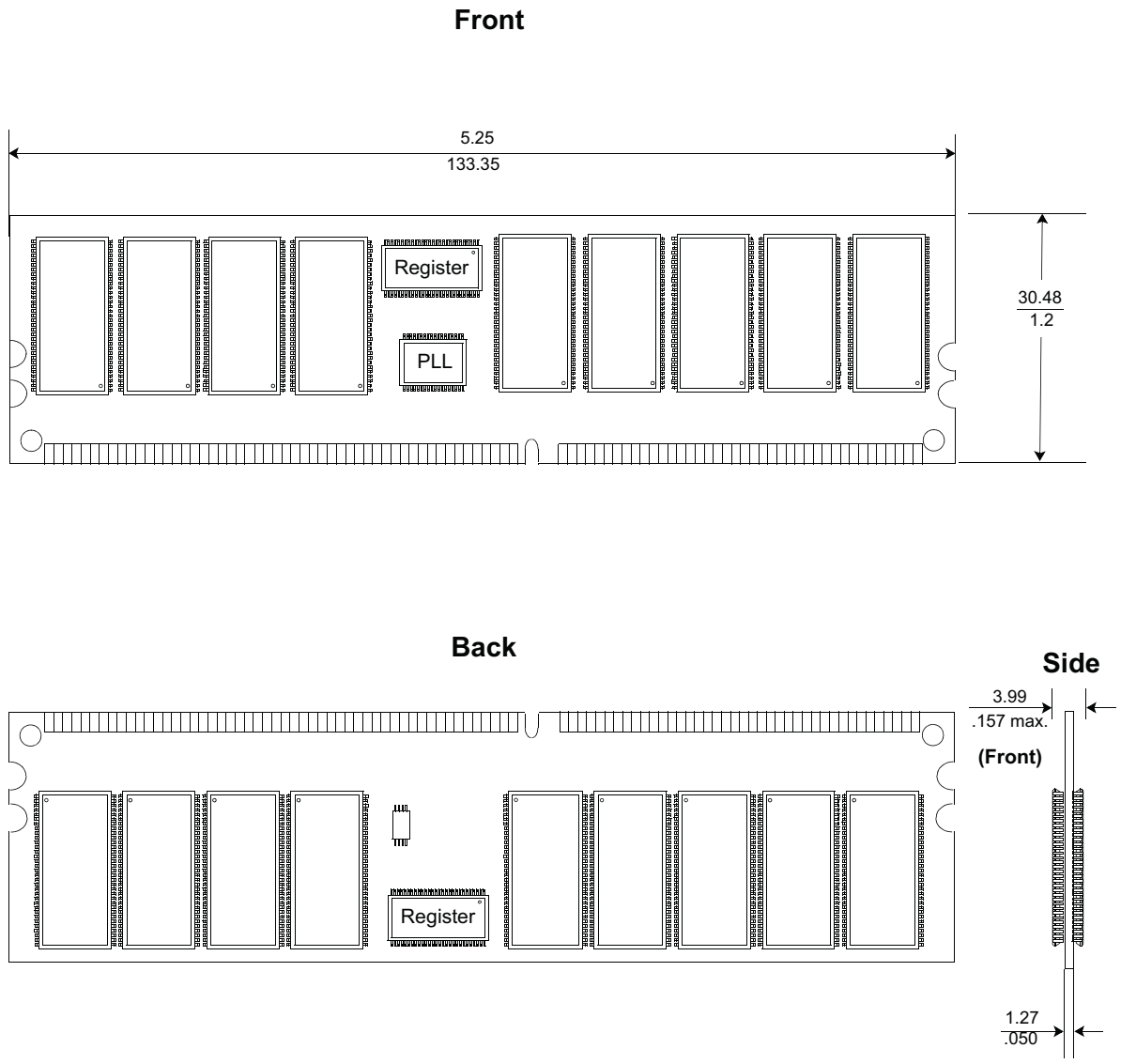
Example Raw Card Versions L (2 Physical Banks) and M Component Placement



Note 1) All dimensions are typical unless otherwise stated. Millimeters / Inches

Note 2) All dimensions are reference only and should be referred to JEDEC Publication95 MO-206 for detailed dimensions.

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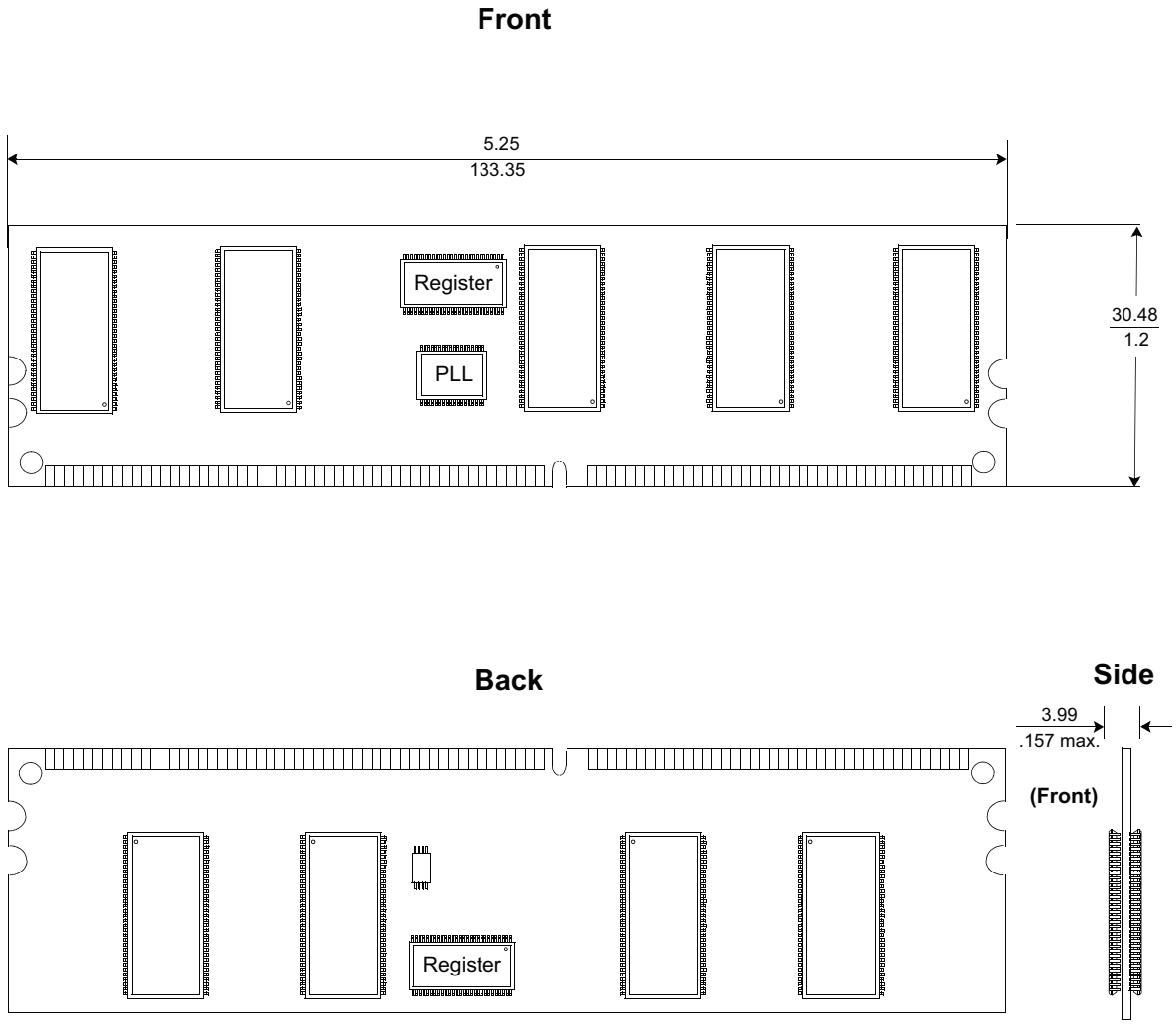
Example Raw Card Versions L (1 Physical Banks) Component Placement



Note 1) All dimensions are typical unless otherwise stated. Millimeters / Inches

Note 2) All dimensions are reference only and should be referred to JEDEC Publication95 MO-206 for detailed dimensions.

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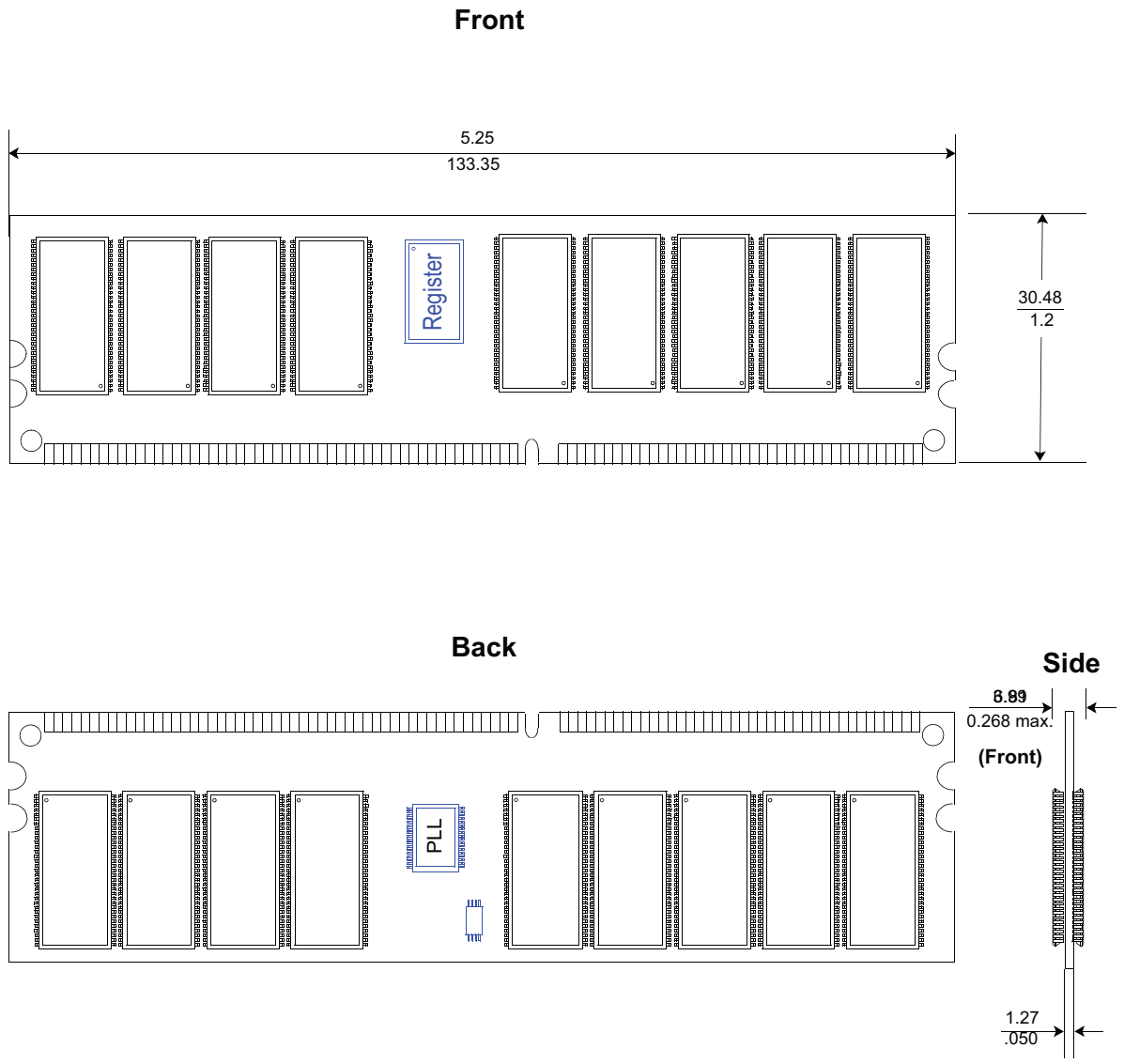
Example Raw Card Versions N (2 Physical Banks) Component Placement



Note 1) All dimensions are typical unless otherwise stated. Millimeters / Inches

Note 2) All dimensions are reference only and should be referred to JEDEC Publication95 MO-206 for detailed dimensions.

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DIMM Wiring Details

Signal Groups

This specification categorizes DDR SDRAM timing-critical signals into seven groups. The following table summarizes the signals contained in each group.

Signal Group	Signals In Group	Raw Card Version	Page
PLL Input / Unused Clocks	CK, $\overline{CK}$	A, B, C, E, L, M, N	39
PLL Output	PCK[9:0]	A, B, C, E, L, M	40, 42. 43, 44
		N	41, 45
Data	DQ[63:0], CB[7:0]	B, C, E, M, N	44
		A, L	44-45
DQS	DQS[17:0]	B, C, E, M, N	44
		A, L	44-45
DM	DM[8:0]	A, L	45
Address and Control	A[12:0], BA[1:0], RAS, CAS, WE	A, B	46, 47
	A[13:0], BA[1:0], RAS, CAS, WE	L, M	48, 49
	A[13:0], BA[1:0], RAS, CAS, WE	N	54, 55
	A[12:0], BA[1:0], RAS, CAS, WE	C, E	62, 63
Chip Select, Clock Enable	$\overline{CS}$[0-1], CKE[0-1]	A	58, 59
		L	52, 57
		B	60, 61
		M	54, 55
		N	60, 61
		C, E	64, 65

General Net Structure Routing Guidelines

Net structures and lengths must satisfy signal quality and setup/hold time requirements for the memory interface. Net structure diagrams for each signal group are shown in the following sections. Each diagram is accompanied by a trace length table that lists the minimum and maximum allowable lengths for each trace segment and/or net.

The general routing requirements are as follows

- Route all signal traces except clocks using 4/6 rules, i.e., 4 mil traces and 6 mil minimum spacing between adjacent traces.
- Route clocks using 4 mil lines and 6 mil spaces between differential clock pairs.
- Route clocks using at least 90% of the total trace length in the inner layers.

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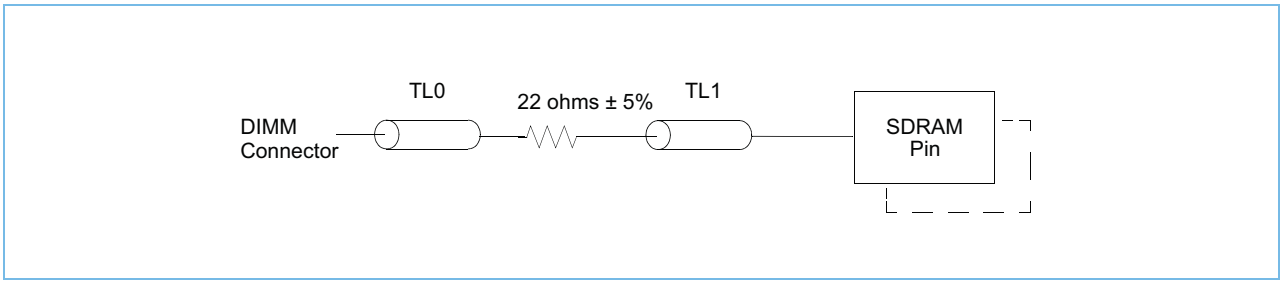
Explanation of Net Structure Diagrams

The net structure routing diagrams provide a reference design example for each raw card version. These designs provide an initial basis for registered DIMM designs. The diagrams should be used to determine individual signal wiring on a DIMM for any supported configuration. Only transmission lines (represented as cylinders and labeled with trace length designators “TL”) represent physical trace segments. All other lines are zero in length. To verify DIMM functionality, a full simulation of all signal integrity and timing is required. **The given net structures and trace lengths are not inclusive for all solutions.**

Once the net structure has been determined, the permitted trace lengths for the net structure can be read from the table below each net structure routing diagram. Some configurations require the use of multiple net structure routing diagrams to account for varying load quantities on the same signal. All diagrams define one load as one SDRAM input. **It is highly recommended that the net structure routing data in this document be simulated by the user.**

Net Structure Example

A 512MB double-sided x72 DIMM using 128Mbit, 32Mx4 SDRAM devices would have a data net structure as shown in the following diagram.



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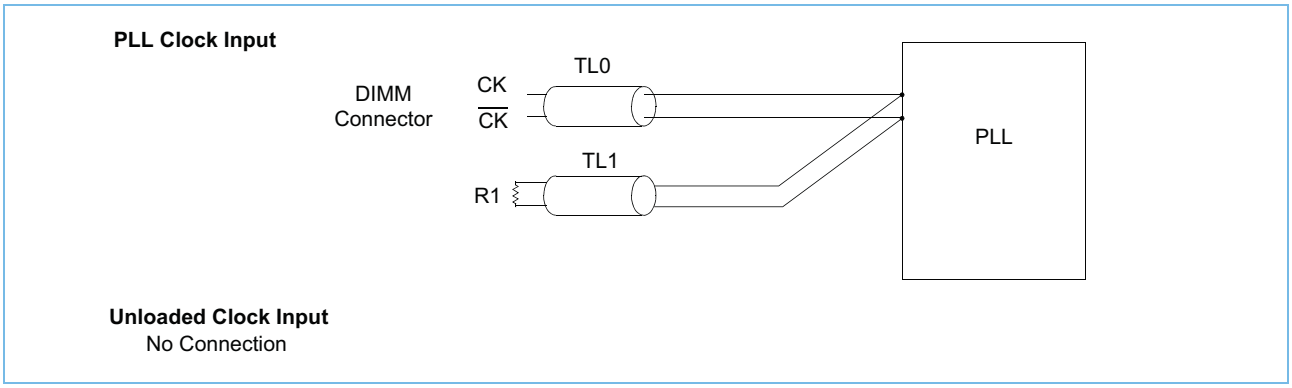
Differential Clock Net Structures

CK, $\overline{CK}$

DDR SDRAM clock signals must be carefully routed to meet the following requirements:

- Signal quality
- Rise/Fall time
- Cross point of the differential pair into the SDRAM and register
- JEDEC-compatible reference delays
- Minimal segment length differences (less than 100 mils total) between clocks of the same function
- PLL input net segment length is newly defined and optimized for high speed DDR Registered DIMMs.

Net Structure Routing for PLL Input



Clock Net Lengths for PLL Input Net Structures

Raw Card	TL0	TL1	R1 (Ohms)	Notes
A, B, C, E, L, M, N	1.00	0.20	120	1, 2, 3

1. All distances are given in inches and must be kept within a tolerance of ± 0.01 inch.
2. All capacitances are given in pF and must be kept within a tolerance of ± 5%.
3. The termination resistor and loading capacitor are both placed after the pin of the PLL.

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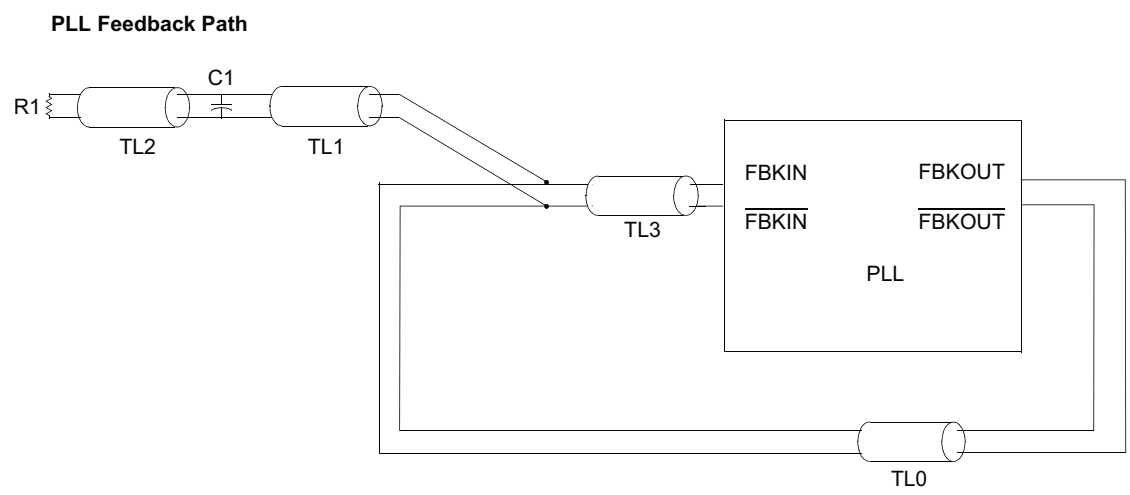
Net Structure Routing for PLL Feedback Path



Trace Lengths for PLL Feedback Path Net Structure

Raw Card	TL0		TL1	TL2	TL3		R1 (Ohms)	C1 [pF]	Notes
	Min	Max			Min	Max			
A, B	2.92	3.02	0.04	0.29	0.05	0.09	120	Not populated	1, 2, 3
C, E	2.93	3.02	0.04	0.29	0.05	0.09	120	5.6	1, 2, 3
L	3.00	3.00	0.04	0.06	0.09	0.09	120	Not populated	1, 2, 3
M	3.00	3.00	0.05	0.13	0.05	0.06	120	Not populated	1, 2, 3

1. All distances are given in inches and must be kept within a tolerance of ± 0.01 inch.
2. All capacitances are given in pF and must be kept within a tolerance of ± 5%.
3. The termination resistor and loading capacitor are both placed as close to the pin of the PLL as possible.

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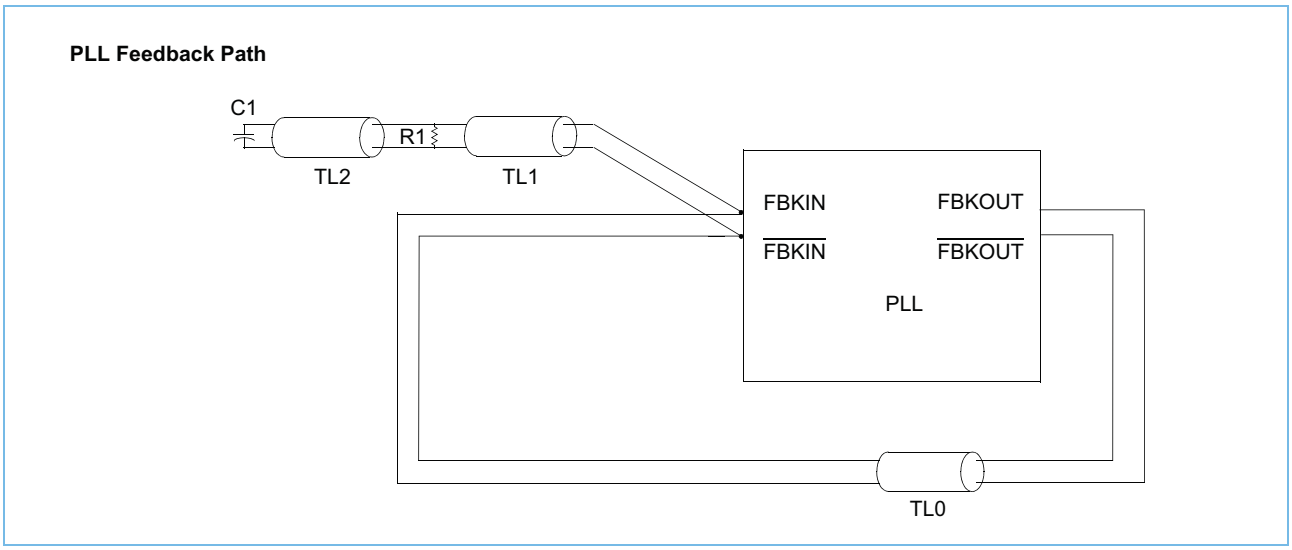
Net Structure Routing for PLL Feedback Path (Raw Card N)



Trace Lengths for PLL Feedback Path Net Structure

Raw Card	TL0		TL1	TL2	R1 (Ohms)	C1 [pF]	Notes
	Min	Max					
N	3.00	3.00	0.15	0.05	120	Not populated	1, 2, 3

1. All distances are given in inches and must be kept within a tolerance of ± 0.01 inch.
2. All capacitances are given in pF and must be kept within a tolerance of ± 5%.
3. The termination resistor and loading capacitor are both placed as close to the pin of the PLL as possible.

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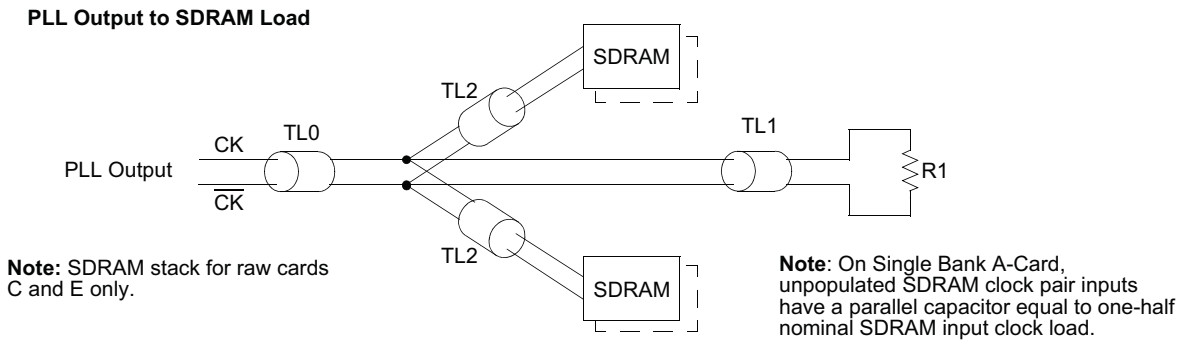
Net Structure Routing for PLL Output to SDRAM Load



Trace Lengths for PLL Clock Output to SDRAM Load Net Structure

Raw Card	TL0		TL1		TL2		R1 Ohms	Notes
	Min	Max	Min	Max	Min	Max		
A	2.46	2.50	0.49	0.58	0.29	0.30	120	1, 2
B	2.46	2.49	0.49	0.57	0.29	0.31	120	1, 2
C/E	2.51	2.52	0.57	0.57	0.29	0.31	120	1, 2
L	2.50	2.51	0.58	0.58	0.30	0.30	120	1, 2
M	2.46	2.50	0.54	0.57	0.30	0.31	120	1, 2
N	2.46	2.50	0.54	0.57	0.30	0.31	120	1, 2

1. All distances are in inches and should be kept within a tolerance of ± 0.01 inch.
2. All capacitances are given in pF and should be kept within a tolerance of ± 5%.

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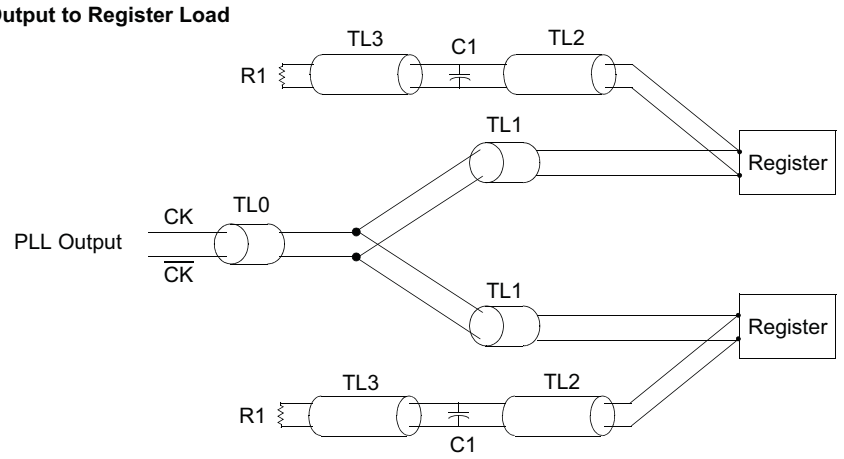
Net Structure Routing for PLL Output to Register Load

PLL Output to Register Load



Unloaded PLL Output

All PLL outputs are used in each design.

Trace Lengths for PLL Clock Output to Register Load Net Structure

Raw Card	TL0		TL1		TL2		TL3		R1 [Ohms[	C1 [pF]	Notes
	Min	Max	Min	Max	Min	Max	Min	Max			
A	0.05	0.05	2.71	2.72	0.13	0.15	0.07	0.07	240	Not populated	1, 2
B	0.05	0.05	2.71	2.72	0.13	0.15	0.07	0.07	240	Not populated	1, 2
C/E	0.05	0.05	3.51	3.51	0.13	0.14	0.07	0.07	240	Not populated	1, 2
L	0.05	0.05	2.71	2.71	0.10	0.11	0.06	0.06	240	TBD	1, 2
M	0.10	0.11	2.68	2.70	0.14	0.14	0.06	0.06	240	TBD	1, 2

1. All distances are in inches and should be kept within a tolerance of ± 0.01 inch.
2. All capacitances are given in pF and should be kept within a tolerance of ± 5%.

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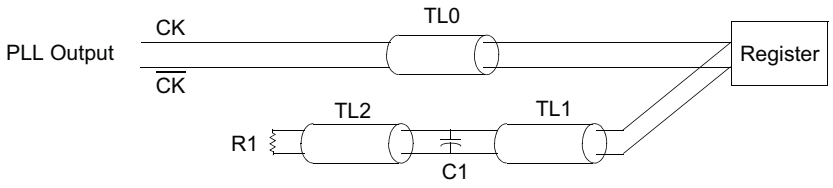
Net Structure Routing for PLL Output to Register Load (Raw Card N)

PLL Output to Register Load



Unloaded PLL Output

All PLL outputs are used in each design.

Trace Lengths for PLL Clock Output to Register Load Net Structure

Raw Card	TL0		TL1		TL2		R1 [Ohms[	C1 [pF]	Notes
	Min	Max	Min	Max	Min	Max			
N	2.80	2.80	0.14	0.14	0.06	0.06	240	TBD	1, 2

1. All distances are in inches and should be kept within a tolerance of ± 0.01 inch.
2. All capacitances are given in pF and should be kept within a tolerance of ± 5%.

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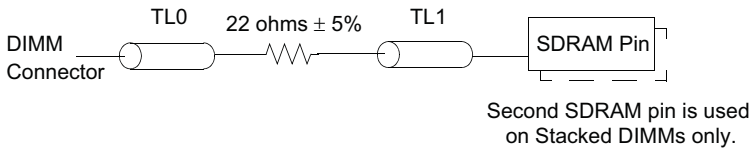
Data Net Structures

DQ[63:0], CB[7:0]
DQS[17:0]

Special attention has been paid to balancing data nets within a DDR SDRAM, within a particular DIMM, and across the DIMM family. Data nets have been placed in order to bound the data strobe nets. Because data travels with the data strobe, the placement of the strobe in the middle of the narrow window aids in data timing. Although it is not necessary to ensure consistent delays between SDRAMs and/or card types, doing so facilitates system design, system simulation, and DIMM specifications. We recommend consistent delays for all nets, as described in the following tables.

Net Structure Routing for Data and DQS (Raw Cards B, C, E, M and N)



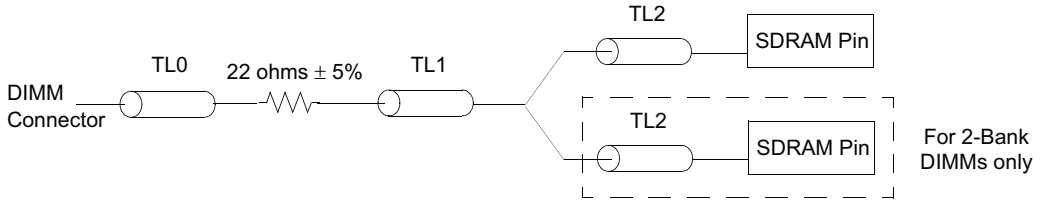
Trace Lengths for Data and DQS Net Structure (Raw Cards B, C, E and M)

Raw Card	TL0		TL1		Total		Notes
	Min	Max	Min	Max	Min	Max	
B	0.13	0.19	0.95	1.02	1.13	1.14	1, 2
C/E	0.13	0.19	0.95	1.02	1.13	1.15	1, 2
M	0.13	0.17	0.70	0.77	0.86	0.92	1, 2
N	0.13	0.17	0.70	0.77	0.86	0.92	1, 2

1. All distances are given in inches and should be kept within a tolerance of ± 0.01 inch
2. Total Min and Total Max refer to the min and max respectively of L0 + L1.

DQ[63:0], CB[7:0]
DQS[8:0]

Net Structure Routing for Data and DQS (Raw Cards A and L)



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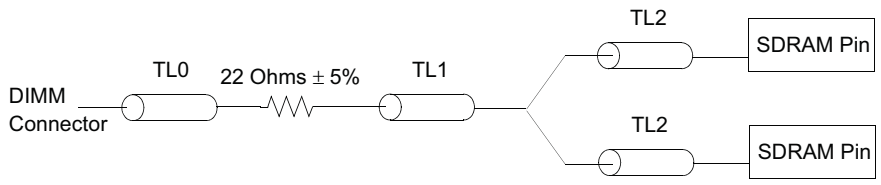
Trace Lengths for Data and DQS Net Structure (Raw Cards A and L)

Raw Card	TL0		TL1		TL2		Total		Notes
	Min	Max	Min	Max	Min	Max	Min	Max	
A	0.13	0.19	0.59	0.65	0.37	0.37	1.15	1.15	1, 2
L	0.20	0.20	0.50	0.50	0.25	0.25	0.93	0.94	1, 2

1. All distances are given in inches and should be kept within a tolerance of ± 0.01 inch
2. Total Min and Total Max refer to the min and max respectively of L0 + L1 + L2

DM[8:0]

Net Structure Routing for DM (Raw Cards A and L)



Trace Lengths for DM Net Structure (Raw Cards A and L)

Raw Card	TL0		TL1		TL2	Total		Notes
	Min	Max	Min	Max		Min	Max	
A	0.13	0.19	0.67	0.69	0.44	1.25	1.30	1, 2
L	0.19	0.20	0.51	0.51	0.31	1.01	1.02	1, 2

1. All distances are given in inches and should be kept within a tolerance of ± 0.01 inch
2. Total Min and Total Max refer to the min and max respectively of L0 + L1.

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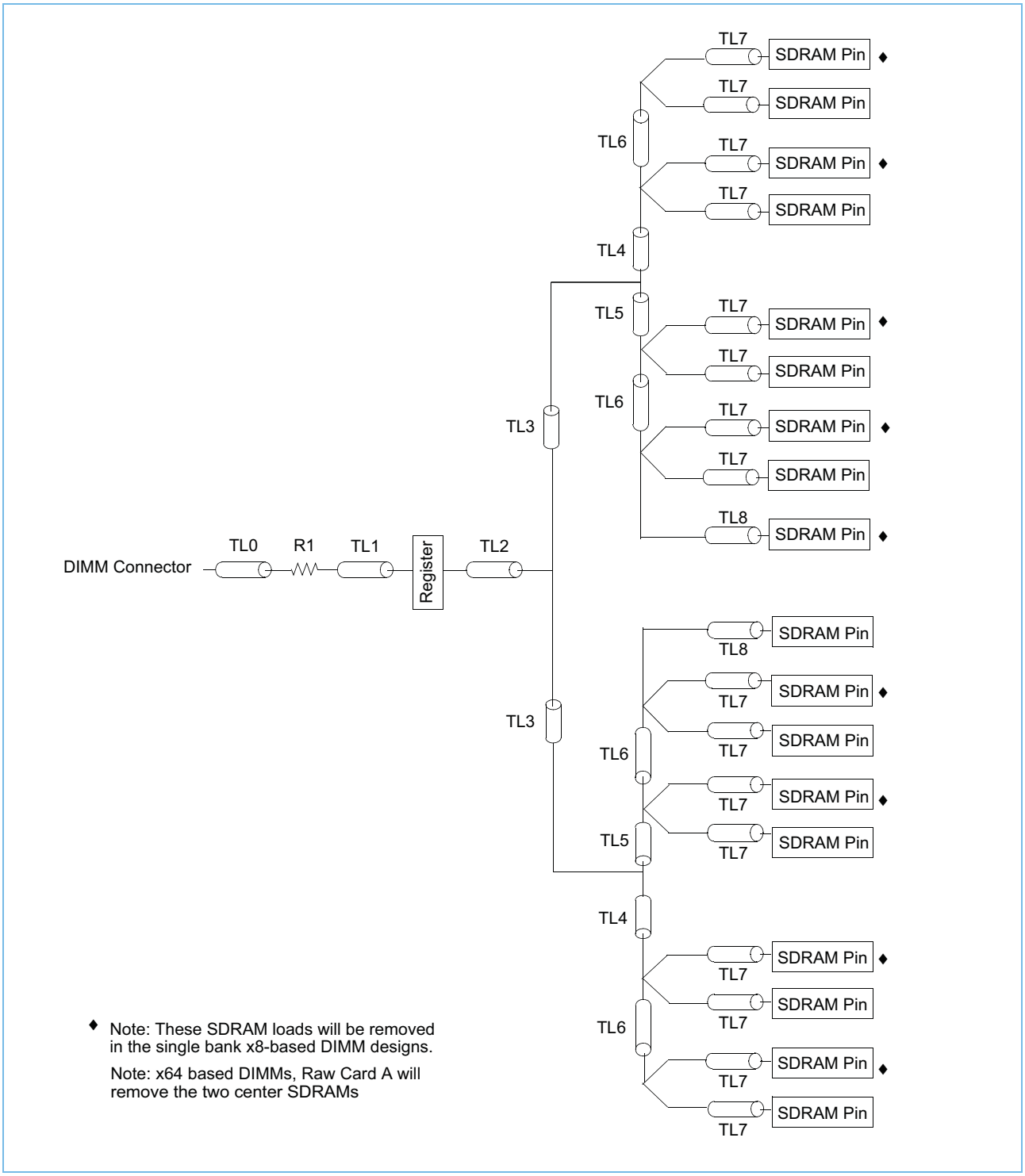
Net Structure Routing for Address and Control (Raw Cards A and B)

A[12:0], BA[1:0], $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$



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Trace Lengths for Address and Control Net Structure (Raw Cards A and B)

A[12:0], BA[1:0], $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$

Raw Card	TL0		TL1		TL2		TL3		TL4		TL5		TL6		TL7		TL8		R1 [Ohms]	Notes
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
A	0.13	0.26	0.56	0.66	0.62	1.37	1.39	2.57	0.40	0.56	0.14	0.15	0.48	0.63	0.20	0.32	0.49	0.72	22	1
B	0.13	0.28	0.54	0.67	0.66	1.38	1.31	2.55	0.40	0.53	0.12	0.15	0.50	0.64	0.20	0.29	0.49	0.72	22	

1. All distances are given in inches and should be kept within a tolerance of ± 0.01 inch

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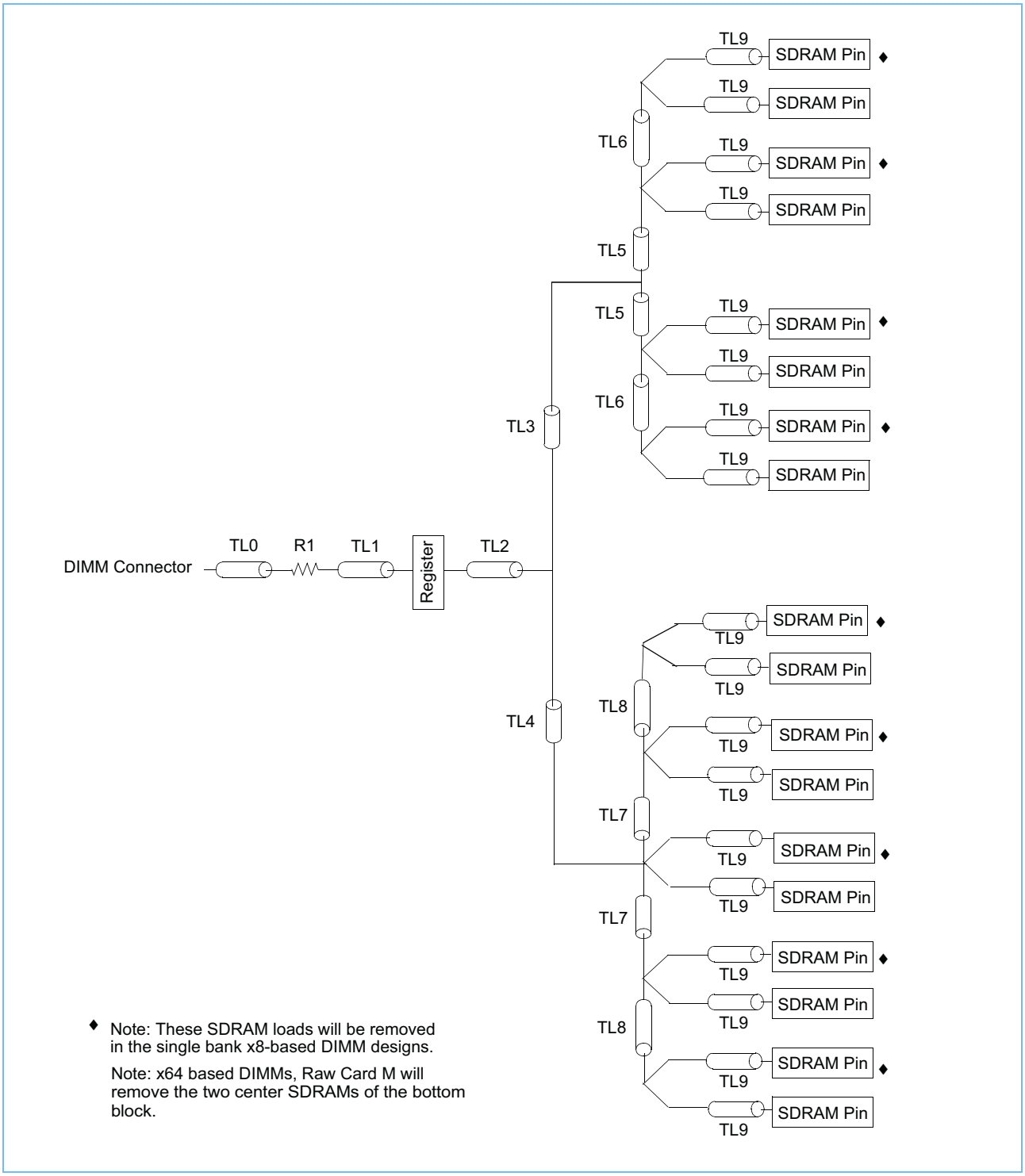
Net Structure Routing for Address and Control (Raw Cards L, and M)

A[13:0], BA[1:0], $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$



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Trace Lengths for Address and Control Net Structure (Raw Cards L and M)

A[13:0], BA [1:0], $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$

Raw Card	TL0		TL1		TL2		TL3		TL4		TL5		TL6		TL7		TL8		TL9		R1 (Ohms)
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
L	0.14	0.21	1.16	1.96	0.05	0.27	1.55	2.25	1.54	1.80	0.19	0.42	0.48	0.59	0.51	0.53	0.50	0.54	0.17	0.37	22
M	0.13	0.20	1.34	1.91	0.12	0.23	2.13	2.17	1.69	1.86	0.21	0.38	0.52	0.54	0.52	0.53	0.52	0.53	0.20	0.30	22

1. All distances are given in inches and should be kept within a tolerance of ± 0.01 inches.
2. For Raw Card L, min(TL3 - TL4) = -0.02", max(TL3 - TL4) = 0.55",
   and for Raw Card M, min(TL3 - TL4) = 0.27", max(TL3 - TL4) = 0.46"

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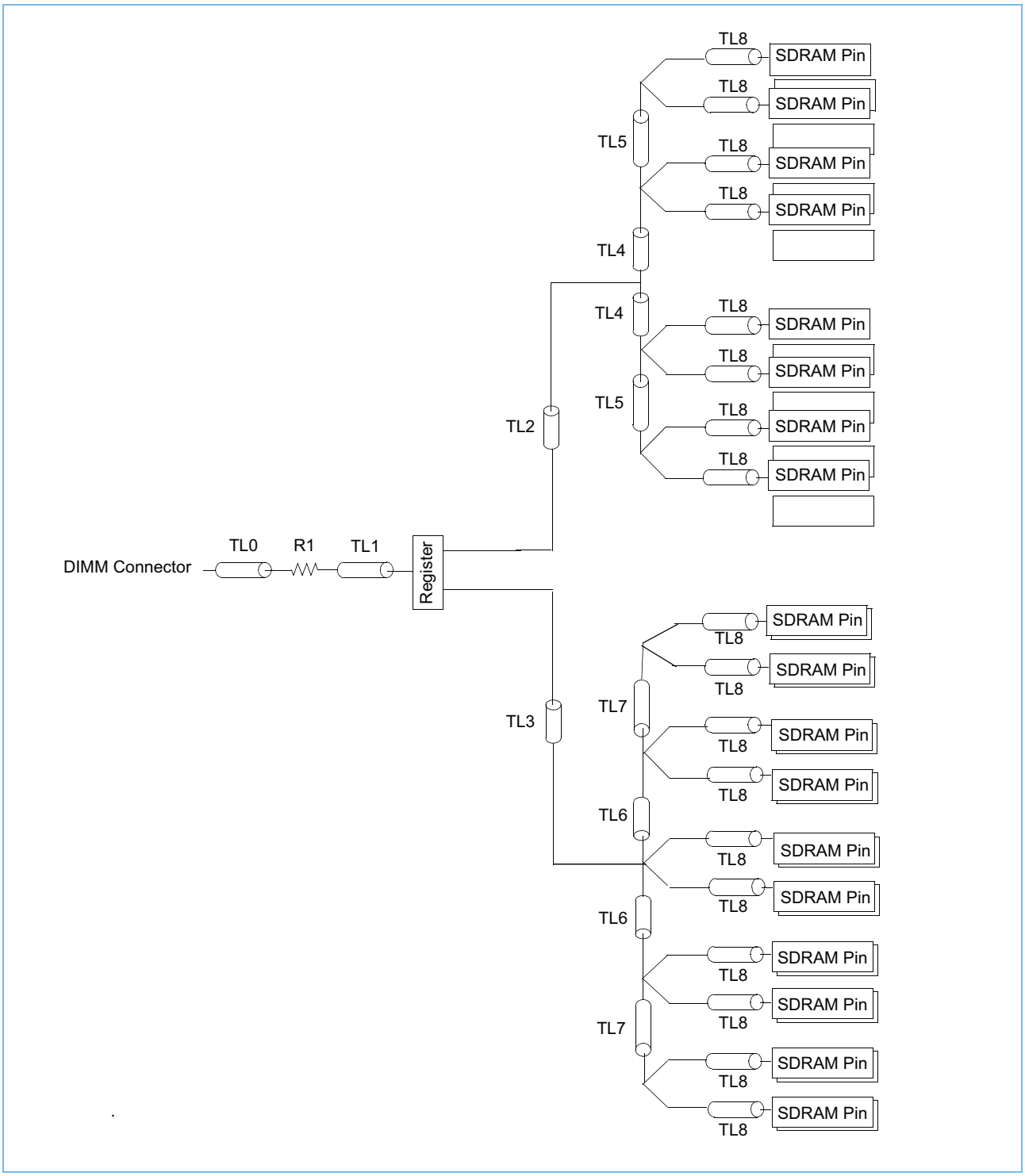
Net Structure Routing for Address and Control (Raw Card N)

A[13:0], BA[1:0],$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$



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Trace Lengths for Address and Control Net Structure (Raw Card N)

A[13:0], BA [1:0], $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$

Raw Card	TL0		TL1		TL2		TL3		TL4		TL5		TL6		TL7		TL8		R1 (Ohms)	note
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
N	0.13	0.21	1.79	1.80	2.06	2.07	1.66	1.67	0.20	0.39	0.53	0.54	0.53	0.54	0.53	0.54	0.20	0.30	22	
	0.13	0.21	1.79	2.07	2.06	2.07	1.66	1.67	0.20	0.39	0.53	0.54	0.53	0.54	0.53	0.54	0.20	0.30	22	A13 only
1. All distances are given in inches and should be kept within a tolerance of ± 0.01 inches.																				

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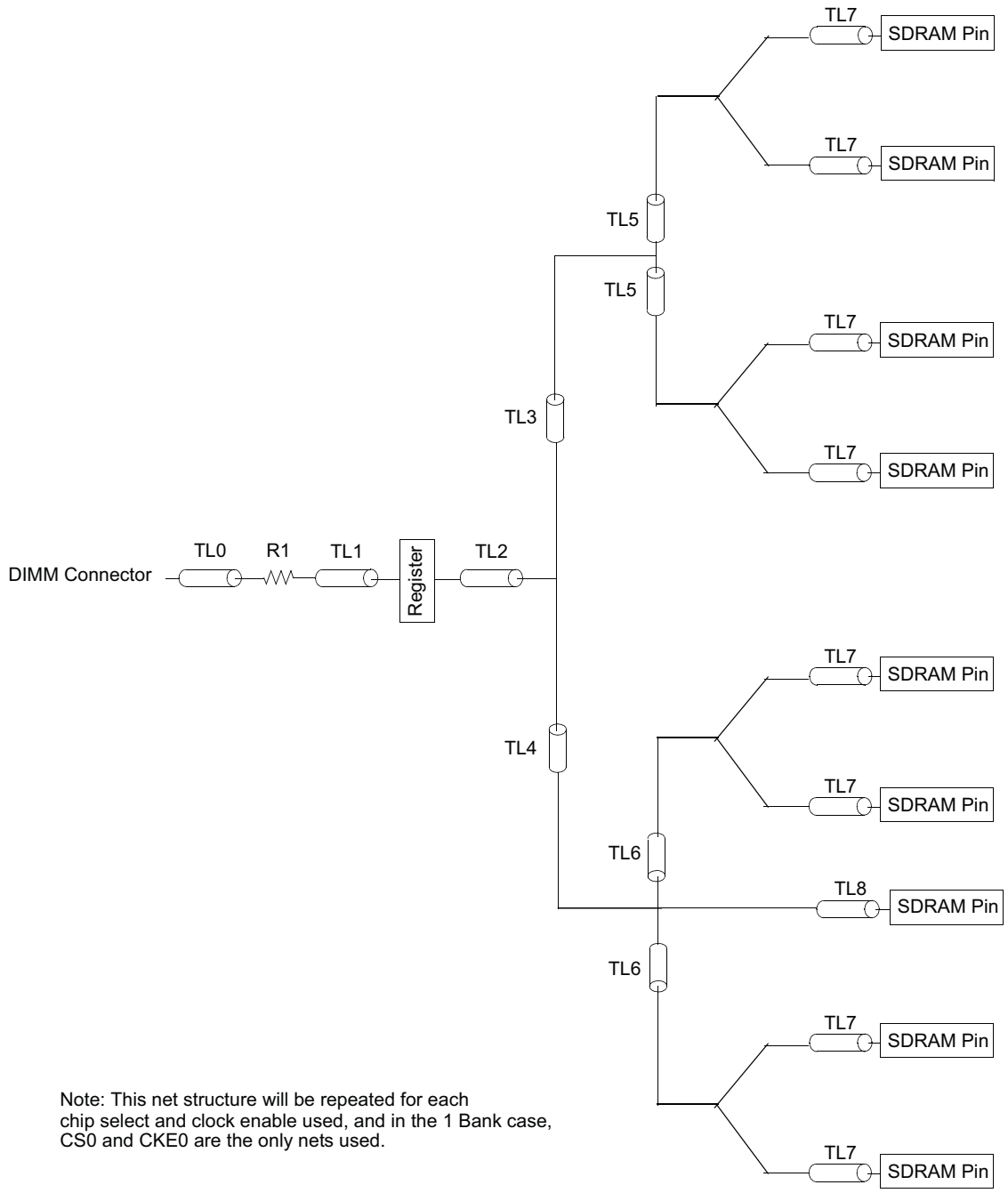
Net Structure Routing for $\overline{CS}$ and CKE (Raw Card L)

$\overline{CS}$[1:0], CKE[1:0]



Note: This net structure will be repeated for each chip select and clock enable used, and in the 1 Bank case, CS0 and CKE0 are the only nets used.

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Trace Lengths for $\overline{CS}$ and CKE Net Structure (Raw Card L)

A[13:0], BA [1:0], $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$

Raw Card	TL0		TL1		TL2		TL3		TL4		TL5		TL6		TL7		TL8		TL9		R1 (Ohms)
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
L	0.14	0.21	1.16	1.96	0.05	0.27	1.55	2.25	1.54	1.80	0.19	0.42	0.48	0.59	0.51	0.53	0.50	0.54	0.17	0.37	22

1. All distances are given in inches and should be kept within a tolerance of ± 0.01 inches.
2. For Raw Card L, min(TL3 - TL4) = -0.02", max(TL3 - TL4) = 0.55"

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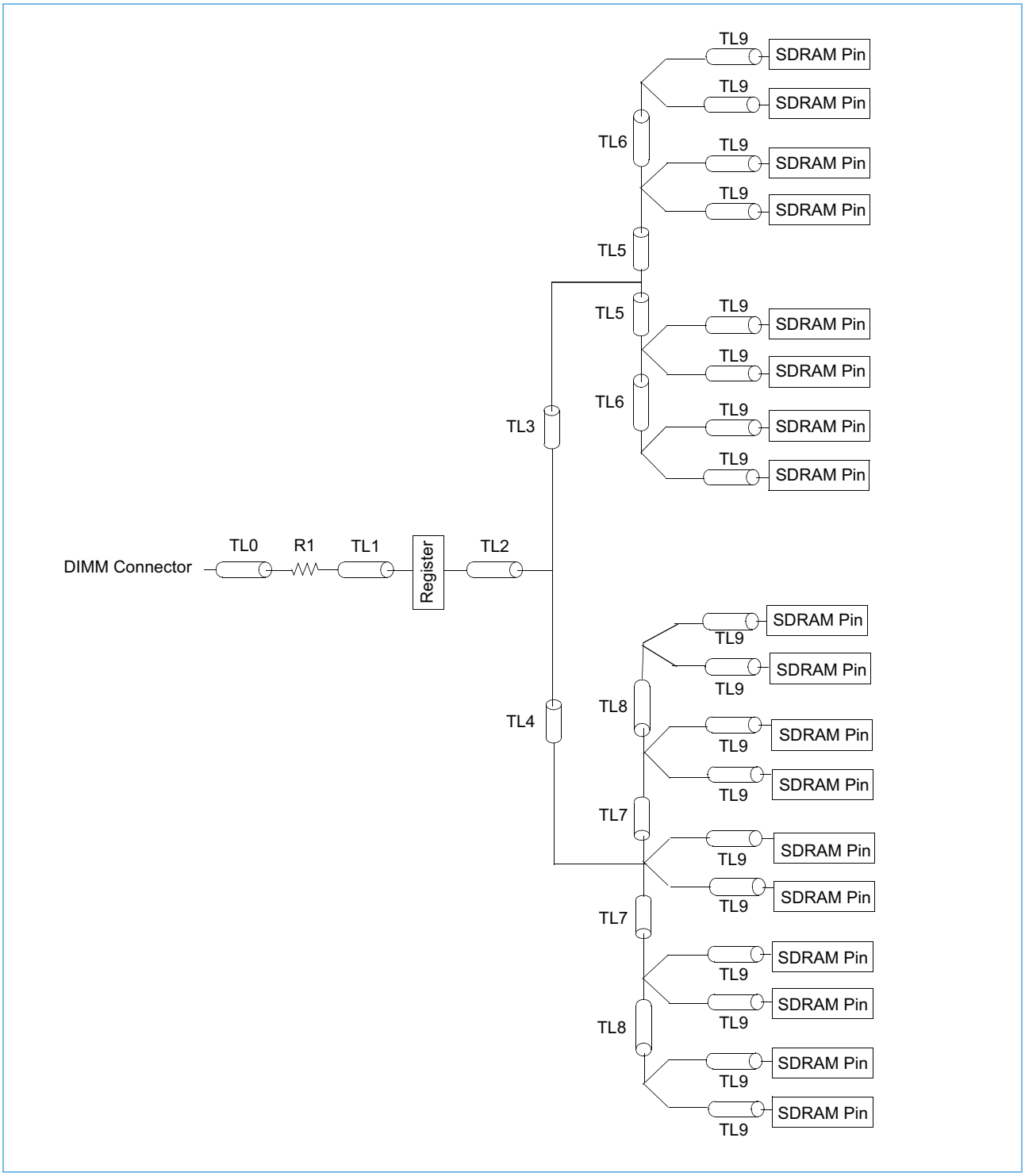
Net Structure Routing for $\overline{CS}$ and CKE (Raw Card M)

$\overline{CS}$[0], CKE[0]



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Trace Lengths for $\overline{CS}$ and CKE Net Structure (Raw Card M)

CS[0], CKE [0]

Raw Card	TL0		TL1		TL2		TL3		TL4		TL5		TL6		TL7		TL8		TL9		R1 (Ohms)
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
M	0.13	0.20	1.34	1.46	0.12	0.23	2.13	2.17	1.69	1.86	0.21	0.38	0.52	0.53	0.52	0.53	0.52	0.53	0.20	0.30	22

1. All distances are given in inches and should be kept within a tolerance of ± 0.01 inches.
2. For Raw Card M, min(TL3 - TL4) = 0.29", max(TL3 - TL4) = 0.41"

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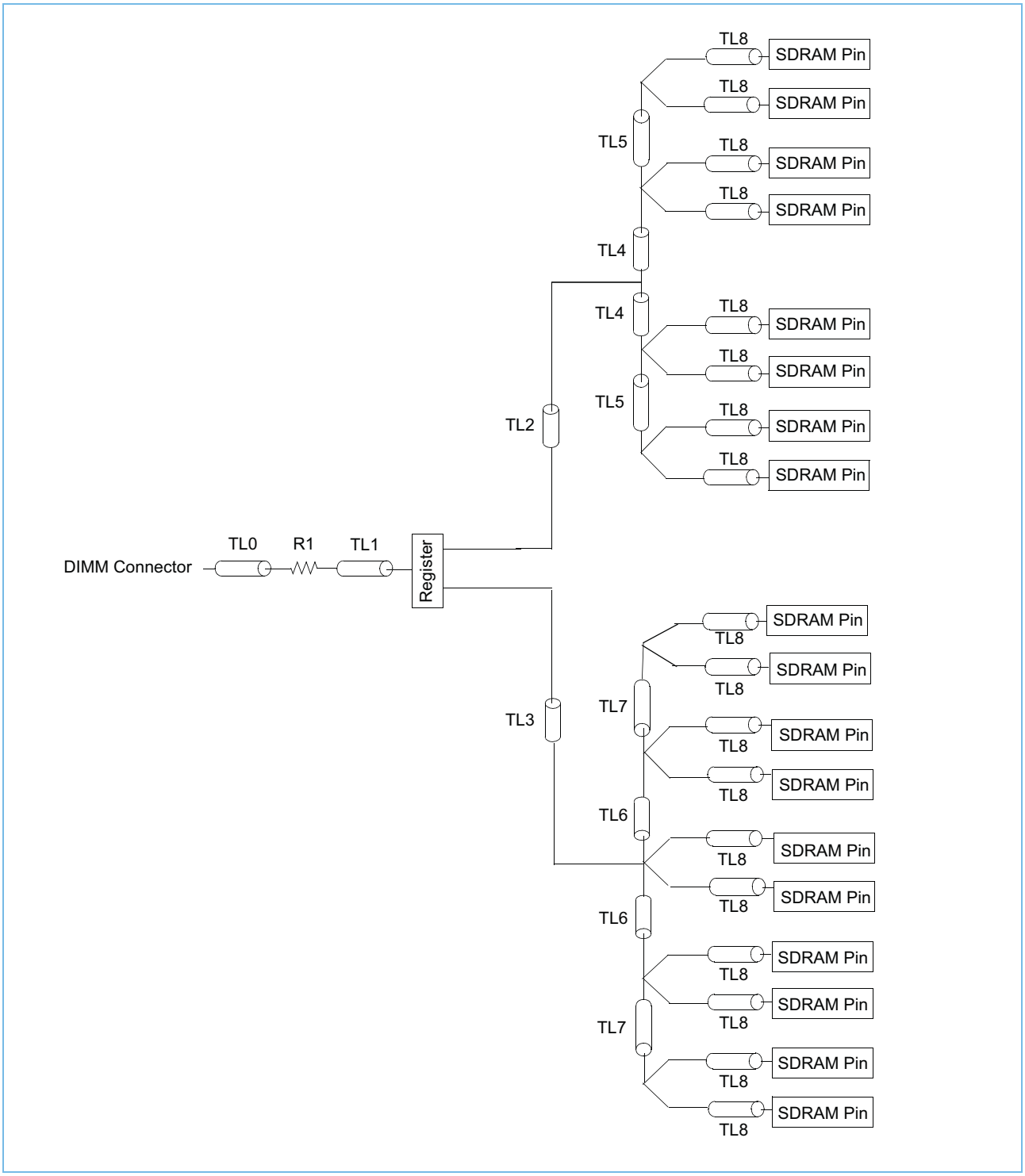
Net Structure Routing for $\overline{CS}$ and CKE (Raw Card N)

$\overline{CS}$[1:0], CKE[1:0]



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Trace Lengths for $\overline{CS}$ and CKE Net Structure (Raw Card N)

CS[1:0], CKE [1:0]

Raw Card	TL0		TL1		TL2		TL3		TL4		TL5		TL6		TL7		TL8		R1 (Ohms)
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
N	0.13	0.21	1.79	1.80	2.06	2.07	1.66	1.67	0.20	0.39	0.53	0.54	0.53	0.54	0.53	0.54	0.22	0.35	22

1. All distances are given in inches and should be kept within a tolerance of ± 0.01 inches.

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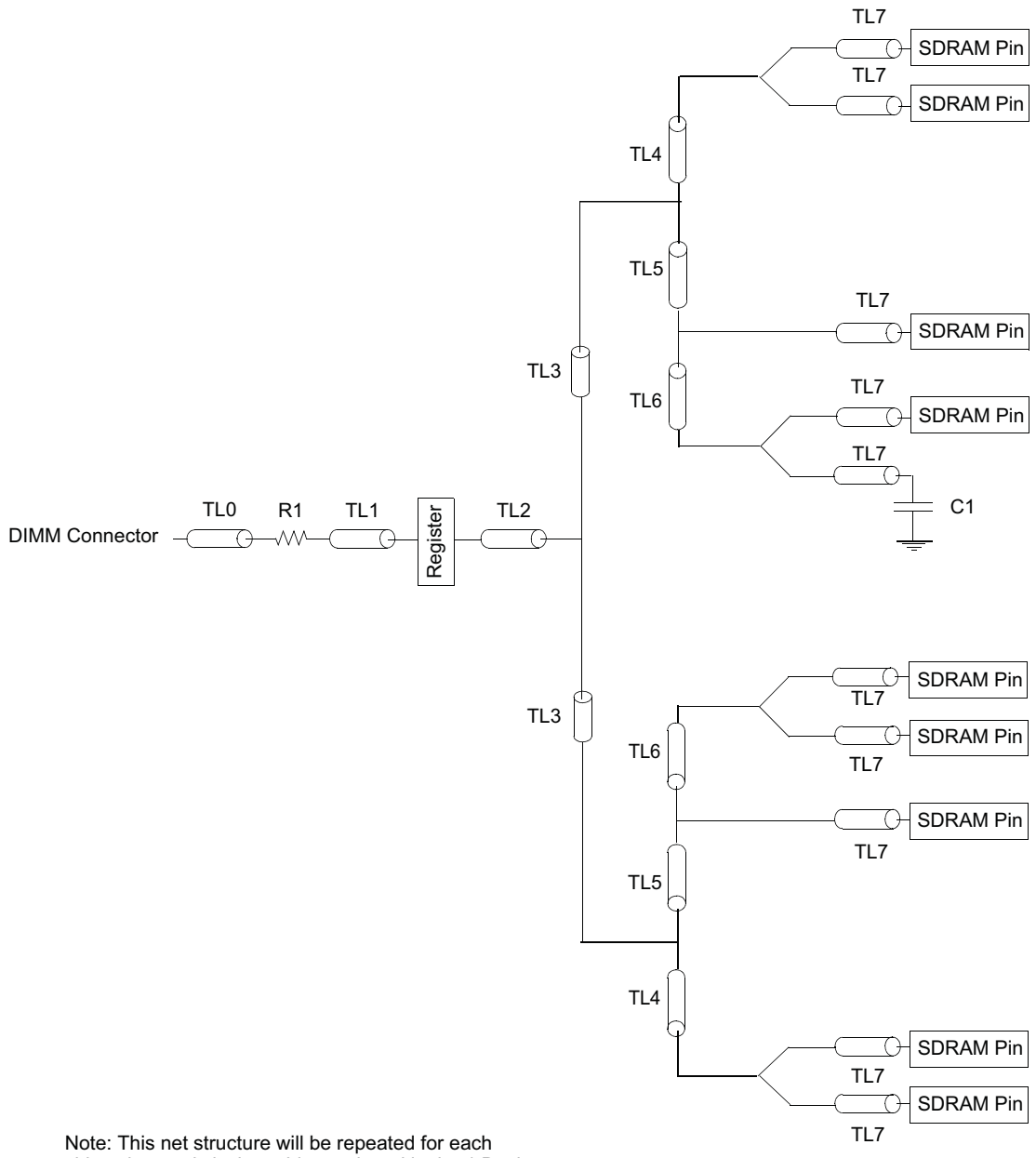
Net Structure Routing for $\overline{CS}$ and CKE (Raw Card A)

$\overline{CS}$ [1:0], CKE [1:0]



Note: This net structure will be repeated for each chip select and clock enable used, and in the 1 Bank case, CS0 and CKE0 are the only nets used.

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Trace Lengths for $\overline{CS}$ and CKE (Raw Card A)

CS [1:0], CKE [1:0]

Raw Card	TL0		TL1		TL2		TL3		TL4		TL5		TL6		TL7		C1 [pF]	R1 [Ohms]	Notes
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max			
A	0.12	0.21	0.60	0.65	1.16	1.43	1.67	2.10	0.15	0.28	0.53	0.69	0.23	0.77	0.08	0.78	3.0	22	1

1. All distances are given in inches and should be kept within a tolerance of ± 0.01 inch

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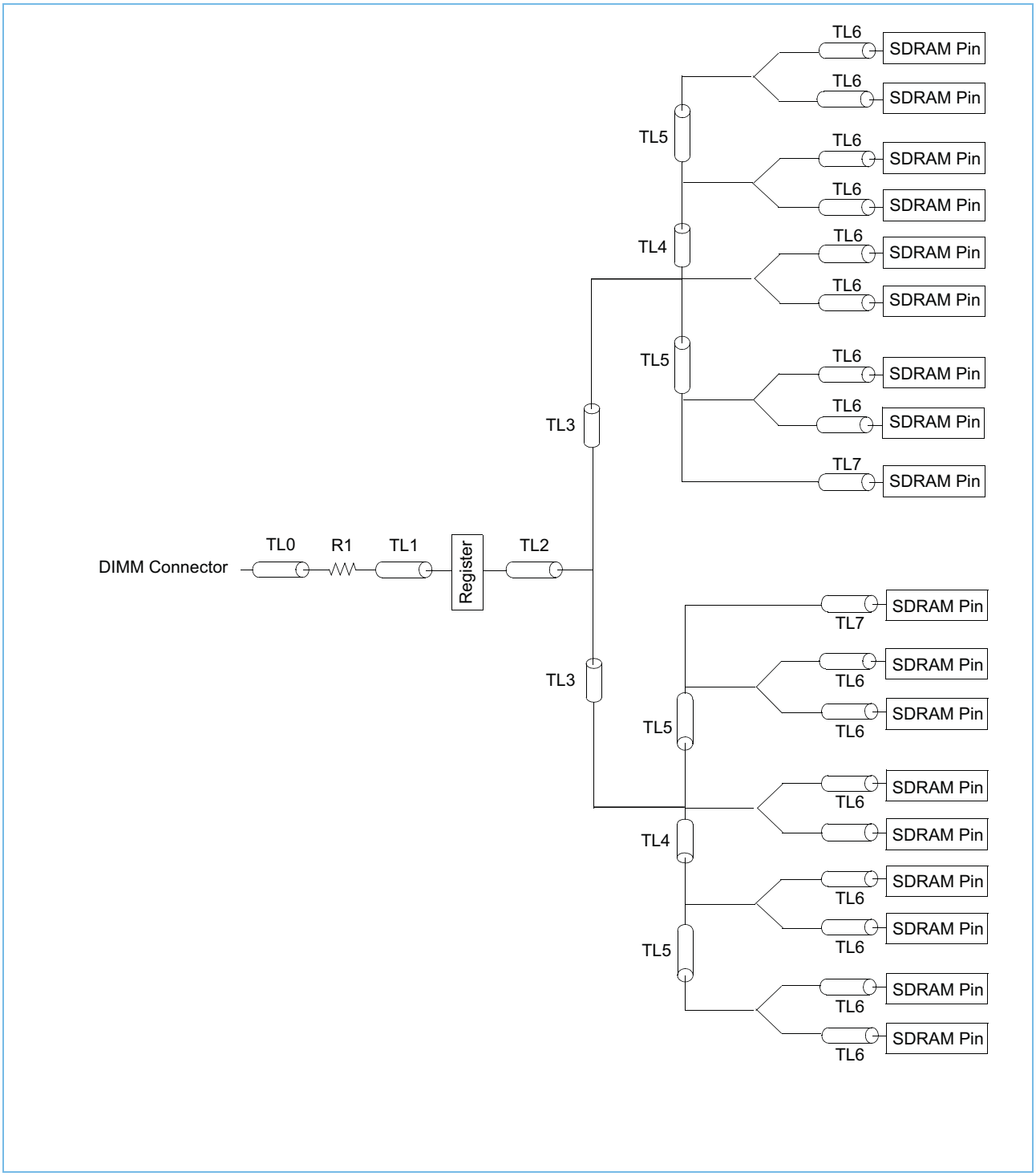
Net Structure Routing for $\overline{CS}$ and CKE (Raw Card B)

$\overline{CS}$ [0], CKE [0]



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Trace Lengths for $\overline{CS}$ and CKE (Raw Card B)

$\overline{CS}$ [0], CKE [0]

Raw Card	TL0		TL1		TL2		TL3		TL4		TL5		TL6		TL7		R1 [Ohms]	Notes
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
B	0.13	0.16	0.612	0.65	1.17	1.23	1.43	1.68	0.58	0.72	0.40	0.58	0.15	0.35	0.56	0.76	22	1

1. All distances are given in inches and should be kept within a tolerance of ± 0.01 inch

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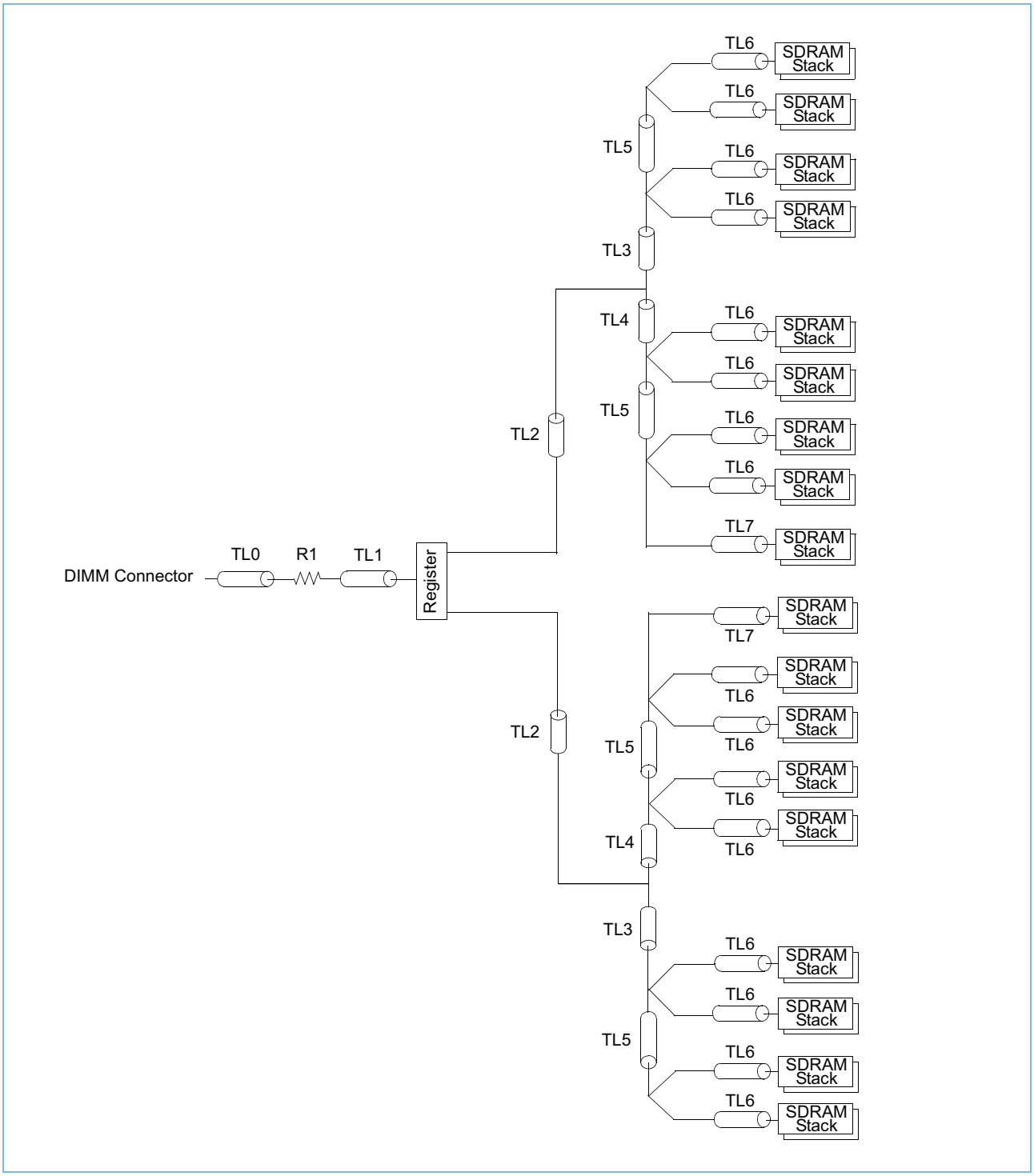
Net Structure Routing for Address and Control (Raw Cards C and E)

A[12:0], BA[1:0], $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$



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Trace Lengths for Address and Control Net Structure (Raw Cards C and E)

A[12:0], BA[1:0], $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$

Raw Card	TL0		TL1		TL2		TL3		TL4		TL5		TL6		TL7		R1 (Ohms)	Notes
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
C	0.13	0.25	0.56	0.66	0.70	2.81	0.40	0.58	0.07	0.23	0.48	0.61	0.20	0.35	0.49	0.74	22	1
E	0.13	0.23	0.56	0.66	0.70	2.81	0.40	0.58	0.07	0.15	0.48	0.61	0.20	0.35	0.49	0.74	22	1

1. All distances are given in inches and should be kept within a tolerance of ± 0.01 inch.

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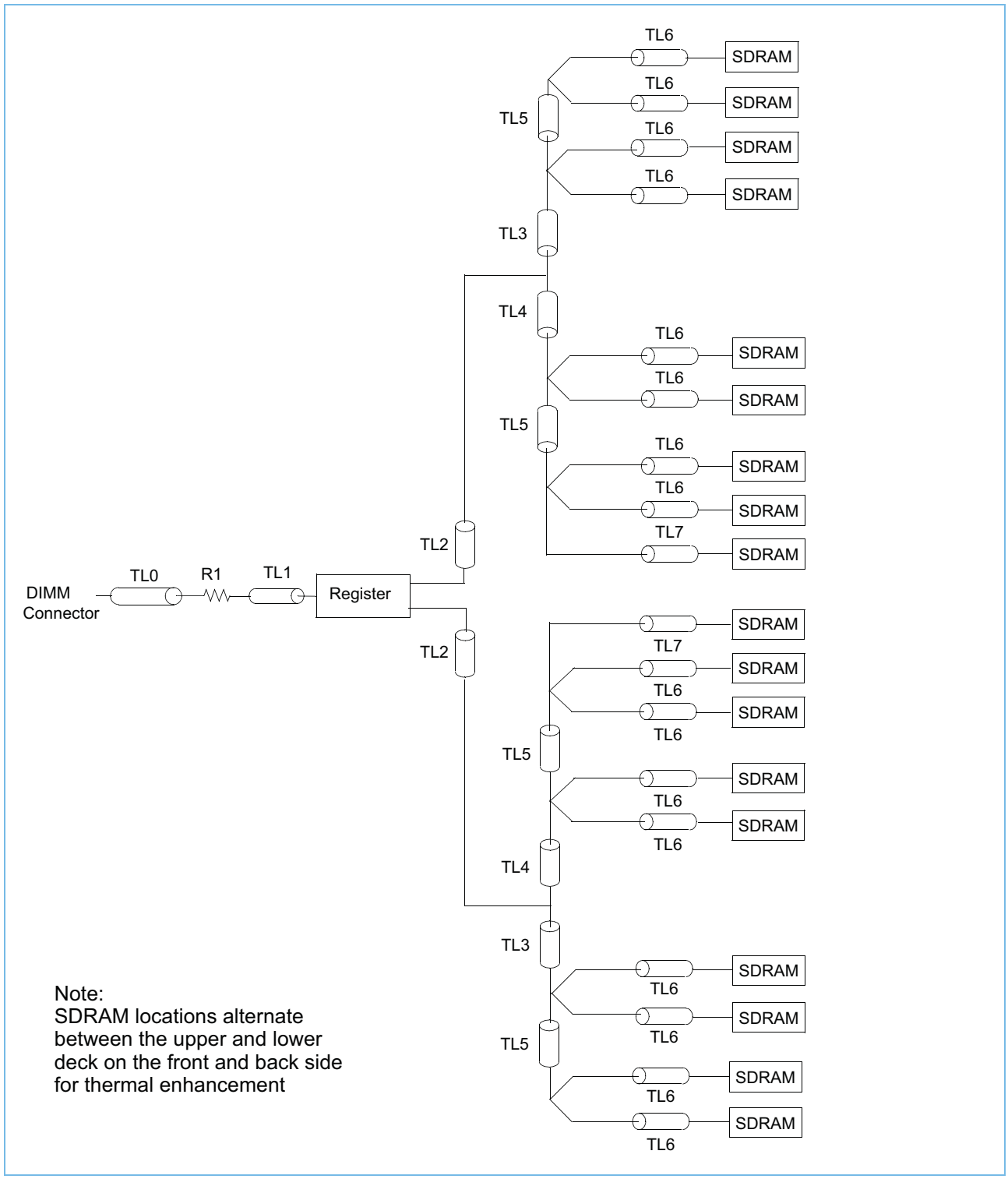
Net Structure Routing for $\overline{CS}$ and CKE (Raw Cards C and E)

$\overline{CS}$[1:0], CKE [1:0]



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Trace Lengths for $\overline{CS}$ and CKE Net Structure (Raw Cards C and E)

$\overline{CS}$[1:0], CKE [1:0]

Raw Card	TL0		TL1		TL2		TL3		TL4		TL5		TL6		TL7		R1 (Ohms)
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
C	0.14	0.19	0.50	0.51	2.14	3.14	0.45	0.61	0.08	0.23	0.42	0.57	0.11	0.45	0.68	0.83	22
E	0.14	0.19	0.50	0.51	2.14	3.14	0.45	0.61	0.08	0.23	0.42	0.57	0.11	0.45	0.68	0.83	22
1. All distances are given in inches and should be kept within a tolerance of ± 0.01 inches.																	

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Cross Section Recommendations

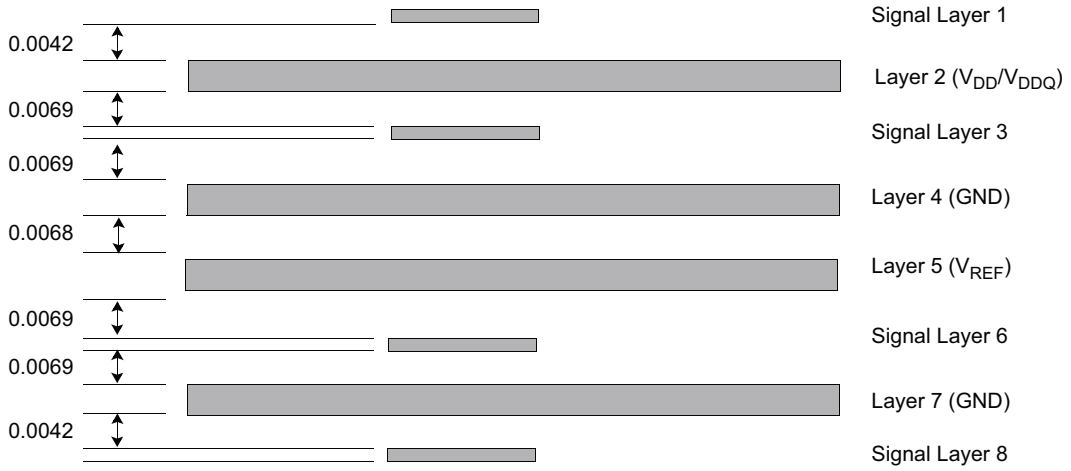
The DIMM printed circuit board design uses eight layers of glass epoxy material. PCBs must contain full ground plane and full power plane layers. The PCB stackup must be designed with 4 mil wide traces.

Note: The PCB edge connector contacts shall be gold-plated and not chamfered.

PCB Electrical Specifications

Parameter	Min	Max	Units
Trace velocity: S0 (outer layers)	1.6	2.2	ns/ft
Trace velocity: S0 (inner layers)	2.0	2.2	ns/ft
Trace impedance: Z_0 (all layers)	54	66	Ohms

Example Eight Layer Stackup



Note: This diagram is intended as an example only. Each DIMM manufacturer can determine the thickness of their layers based on their own impedance calculations.

Impedance Measurement Coupons

In order to allow DIMM manufacturers to verify and monitor the trace impedance (Z_0) listed above, measurement coupons have been added to each of the Registered DIMM designs. There are four single-ended coupons located on each of the four signal layers, as well as a pair of nets wired on the clock signal layer as a differential pair. These nets are all located on the right side of the DIMM.The single ended nets use the EEPROM wires, while the differential pair has been designed in for this purpose. Each net is two inches in length and has a via near a large ground via placed at the bottom of the DIMM. Each net is clearly labeled 1,2,3,4, or DIFF. A Time Domain Reflectometer (T.D.R.) can be used to perform these measurements (for the differential net, odd mode must be used) before DIMM assembly.

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Timing Budget

The post-register timings on the Registered DIMMs are critical. The following table describes a preliminary post-register timing budget for a typical DDR PC1600 Registered DIMM. This method is 'Time to Vm' that uses the register timing into its specified test load (instead of t_{CO}, open circuit) and adds or subtracts the timing into the SDRAM net and loads.

DIMM Post-Register Timing

Symbol	Parameter	Time (ns) Set-up	Time (ns) Hold	Notes
t_{CLK}	Clock cycle time	10.0	N/A	1
t_{PD}	Maximum time for the signal to exit the register. This is measured from the rising edge of the register clock input (the falling edge of $\overline{CK}$) to the register output into a standard register test load (30 pF to GND, 50 Ohms to V_{TT}.	- 2.8	1.1	1, 2
$t_{NETDELAY}$	Maximum time for the signal to propagate from the register to any SDRAM. The switching point for a rising edge is VREF ± 100mV.	- 2.0	0.5	1, 2, 3
t_{REG}	Shift in the register clock in relationship to the SDRAM. The input clocks to the registers and the SDRAM are intended to track, but some error is likely.	- 0.10	- 0.10	1
t_{IS}	Setup time required for the SDRAM inputs	- 1.1	NA	1
t_{IH}	Hold time required for the SDRAM inputs	NA	- 1.1	1
t_{Skew*}	Clock jitter and skew on the DIMM	- 0.275	- 0.2	1, 4
t_{SS}	Simultaneous Switch effect	- 0.35	NA	1, 2
t_{XTALK}	Crosstalk Adder	- 0.10	NA	
Margin		**3.275**	**0.2**	1

1. The timing values shown are consistent with registers available at the time this specification was written. All registers must meet the combined delay values and ensure positive margin, although the specific delay value for each term may vary.
2. The timing values for $t_{NETDELAY}$, t_{PD}, and t_{SS}, when added together, define the overall delay from clock at the register to the time when the last re-driven signal arrives at the SDRAM (setup time), or earliest re-driven signal changes state after clock (hold time).
3. The $T_{NETDELAY}$ is determined via simulation analysis. The register driver is simulated into both the standard test load and the actual DIMM net and SDRAM loads and the difference is the actual net delay of the DIMM.
4. See the tables below.

*DIMM Clock Contributions (t_{Skew})

t_{Skew} for Setup		Units
DIMM PLL Jitter	0.075	ns
DIMM PLL Skew	0.100	ns
DIMM Clock Net Skew	0.100	ns
Total	0.275	ns

t_{Skew} for Hold		Units
DIMM PLL Skew	0.100	ns
DIMM Clock Net Skew	0.100	ns
Total	0.200	ns

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Serial PD Definition

The Serial Presence Detect function MUST be implemented on the PC DDR SDRAM Registered DIMM. The component used and the data contents must adhere to the most recent version of the JEDEC DDR SDRAM Serial Presence Detect Specifications. Please refer to this document for all technical specifications and requirements of the serial presence detect devices.

The following table is intended to be an **example** of the SPD data for a PC1600 512MB (64M x 72), 184 Pin Registered SDRAM DDR DIMM using two physical banks of 32M x 8 DDR200 devices with 13/10/2 addressing and $\overline{CAS}$ latencies of 2 and 2.5.

Serial Presence Detect Example Raw Card Version ‘A’ (Part 1 of 3)

64M x 72 DDR

Byte #	Description	SPD Entry Value	Serial PD Data Entry (Hexadecimal)	Notes
0	Number of Serial PD Bytes Written during Production	128	80	
1	Total number of bytes in Serial PD Device	256	08	
2	Fundamental Memory Type	SDRAM DDR	07	
3	Number of Row Addresses on Assembly	13	0D	
4	Number of Column Addresses on Assembly	10	0A	
5	Number of Physical Banks on DIMM	2	02	
6 - 7	Data Width of Assembly	x72	4800	
8	Voltage Interface Level of this Assembly	SSTL 2.5V	04	
9	SDRAM Device Cycle Time at Maximum CL (CLX = 2.5)	8.0ns	80	1
10	SDRAM Device Access Time from Clock at CL=2.5	± 0.8ns	80	
11	DIMM Configuration Type	ECC	02	
12	Refresh Rate/Type	7.8µs/SR	82	
13	Primary SDRAM Device Width	x8	08	
14	Error Checking SDRAM Device Width	x8	08	
15	SDRAM Device Attributes: Minimum Clock Delay, Random Column Access	1 Clock	01	
16	SDRAM Device Attributes: Burst Lengths Supported	2, 4, 8	0E	
17	SDRAM Device Attributes: Number of Device Banks	4	04	
18	SDRAM Device Attributes: $\overline{CAS}$ Latency	2, 2.5	0C	
19	SDRAM Device Attributes: $\overline{CS}$ Latency	0	01	
20	SDRAM Device Attributes: $\overline{WE}$ Latency	1	02	
21	SDRAM Module Attributes	Registered with PLL, Differential clock	26	

1. In a registered DIMM, data is delayed an additional clock cycle due to the on-DIMM pipeline register (that is, Device CL [clock cycles] + 1 = DIMM $\overline{CAS}$ latency).
2. cc = Checksum Data byte, 00-FF (Hex).
3. “R” = Alphanumeric revision code, A-Z, 0-9.
4. rr = ASCII coded revision code byte “R”.
5. ww = Binary coded decimal week code, 01-52 (Decimal) 01-34 (Hex).
6. yy = Binary coded decimal year code, 00-99 (Decimal) 00-63 (Hex).
7. ss = Serial number data byte, 00-FF (Hex).

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Serial Presence Detect Example Raw Card Version 'A' (Part 2 of 3)

64M x 72 DDR

Byte #	Description	SPD Entry Value	Serial PD Data Entry (Hexadecimal)	Notes
22	SDRAM Device Attributes: General	$V_{DD} \pm 0.2V$	00	
23	Minimum Clock Cycle at CLX-0.5 (CL = 2)	10.0ns	A0	1
24	Maximum Data Access Time (t_{AC}) from Clock at CLX-0.5 (CL = 2)	± 0.8ns	80	
25	Minimum Clock Cycle Time at CLX-1 (CL = 1.5)	N/A	00	
26	Maximum Data Access Time (t_{AC}) from Clock at CLX-1 (CL = 1.5)	N/A	00	
27	Minimum Row Precharge Time (t_{RP})	20.0ns	50	
28	Minimum Row Active to Row Active Delay (t_{RRD})	15.0ns	3C	
29	Minimum $\overline{RAS}$ to $\overline{CAS}$ Delay (t_{RCD})	20.0ns	50	
30	Minimum Active to Precharge Time (t_{RAS})	50.0ns	32	
31	Module Bank Density	256MB	40	
32	Address and Command Setup Time before Clock	1.1ns	B0	
33	Address and Command Hold Time after Clock	1.1ns	B0	
34	Data/Data Mask Input Setup Time before Data Strobe	0.6ns	60	
35	Data/Data Mask Input Hold Time after Data Strobe	0.6ns	60	
36 - 40	Reserved for VCSDRAM	Undefined	00	
41	Minimum Active/Auto-Refresh Time (t_{RC})	70ns	86	
42	SDRAM Device Minimum Auto-Refresh to Active/Auto-Refresh Command Period (t_{RFC})	80ns	50	
43	SDRAM Device Maximum Cycle Time (t_{ck}max)	12ns	30	
44	SDRAM Device Maximum DQS-DQ Skew time (t_{DQSQ})	0.6ns	3C	
45	SDRAM Device Maximum Read Data Hold Skew Factor (t_{QHS})	1.0ns	A0	
46 - 61	Superset Information (may be used in future)	Undefined	00	
62	SPD Revision	0	00	
63	Checksum for Bytes 0 - 62	Checksum Data	cc	2
64 - 71	Manufacturers' JEDEC ID Code			
72	Module Manufacturing Location			
73 - 90	Module Part Number			3, 4

1. In a registered DIMM, data is delayed an additional clock cycle due to the on-DIMM pipeline register (that is, Device CL [clock cycles] + 1 = DIMM $\overline{CAS}$ latency).
2. cc = Checksum Data byte, 00-FF (Hex).
3. "R" = Alphanumeric revision code, A-Z, 0-9.
4. rr = ASCII coded revision code byte "R".
5. ww = Binary coded decimal week code, 01-52 (Decimal) 01-34 (Hex).
6. yy = Binary coded decimal year code, 00-99 (Decimal) 00-63 (Hex).
7. ss = Serial number data byte, 00-FF (Hex).

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Serial Presence Detect Example Raw Card Version ‘A’ (Part 3 of 3)

64M x 72 DDR

Byte #	Description	SPD Entry Value	Serial PD Data Entry (Hexadecimal)	Notes
91 - 92	Module Revision Code	“R” plus ASCII blank	rr20	4
93 - 94	Module Manufacturing Date	Year/Week Code	yyww	5, 6
95 - 98	Module Serial Number	Serial Number	ssssssss	7
99 - 127	Reserved	Undefined	00	
128 - 255	Open for Customer Use	Undefined	00	

1. In a registered DIMM, data is delayed an additional clock cycle due to the on-DIMM pipeline register (that is, Device CL [clock cycles] + 1 = DIMM CAS latency).
2. cc = Checksum Data byte, 00-FF (Hex).
3. “R” = Alphanumeric revision code, A-Z, 0-9.
4. rr = ASCII coded revision code byte “R”.
5. ww = Binary coded decimal week code, 01-52 (Decimal) 01-34 (Hex).
6. yy = Binary coded decimal year code, 00-99 (Decimal) 00-63 (Hex).
7. ss = Serial number data byte, 00-FF (Hex).

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Product Label

The following label should be applied to all DDR-compatible DIMMs, to describe the performance and reference design attributes of the module. The label can be in the form of a stick-on label, silk screened onto the assembly, or marked using an alternate customer-readable format. A minimum font size of eight points should be used, and the number can be printed in one, or more, rows on the label. Note that in addition to this label, the manufacturer's name and DIMM assembly part number shall also appear on the DIMM.

Format:

PCwwwwm-aabcd-ef

Where:

wwww: Module Bandwidth
- 1600: 1.6 GB/sec
- 2100: 2.1 GB/sec

m: Module Type
- R = Registered DIMM
- U = Unbuffered DIMM (no registers on DIMM)

aa: SDRAM CAS Latency, with no decimal point (25 = 2.5ns $\overline{CAS}$ Latency)

b: SDRAM minimum t_{RCD} specification (in clocks)

c: SDRAM minimum t_{RP} specification (in clocks)

d: JEDEC SPD Encoding Level used on this DIMM

e: Gerber file used for this design (if applicable)
- A: Reference design for R/C 'A' is used for this assembly
- B: Reference design for R/C 'B' is used for this assembly
- C: Reference design for R/C 'C' is used for this assembly
- E: Reference design for R/C 'E' is used for this assembly
- L: Reference design for R/C 'L' is used for this assembly
- M: Reference design for R/C 'M' is used for this assembly
- N: Reference design for R/C 'N' is used for this assembly
- Z: None of the 'Reference' designs were used on this assembly

f: Revision number of the reference design used:
- 1: 1st revision (1st release)
- 2: 2nd revision (2nd release)
- 3: 3rd revision (3rd release)
- Blank: Not Applicable (used with 'Z' above)

Example:

PC1600R-25330-A1
is a PC1600 DDR Registered DIMM
with CL = 2.5, t_{RCD} = 3, t_{RP} = 3
using the latest JEDEC SPD Encoding Level 0.0
and produced based on the 'A' raw card Gerber, 1st release

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DIMM Mechanical Specifications

JEDEC has standardized detailed mechanical information for the 184 Pin DIMM family. This information can be accessed on the worldwide web as follows:

1. Go to http://www.jedec.org.
2. Click on ‘Free Standards’
3. Type ‘MO-206’ in the box under ‘By Document Number:’
4. Click on ‘Find’
5. Click on ‘Open File’ to open the PDF for this product family.

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Supporting Hardware

Clock Reference Board

To facilitate the measurement of clock arrival time to the DDR SDRAM for both DDR Unbuffered and Registered SDRAM DIMMs, a ‘Clock Reference Board’ will be released. This board includes the following:

- A frequency synthesizer *to provide 100MHz and 133MHz clocks*
- A clock buffer *to re-drive clocks to the module socket and reference nets*
- A 184P DIMM socket, with three clock inputs wired and *CS and CKE pins tied inactive*
- A ‘Registered’ DIMM reference net *consistent with the JEDEC-approved Registered DIMM Clock Input net structure*
- An ‘Unbuffered’ DIMM reference net *consistent with the JEDEC-approved Unbuffered DIMM clock input structure*
- A clock buffer ‘standard test load’ *to permit characterization of the clock buffer into its test load*

This clock reference board will be made generally available in the industry, and should be used by module producers, as well as system designers, to ensure modules meet the intended clock timings defined in this specification. Every effort will be taken to minimize clock variations and clock skew on these boards.

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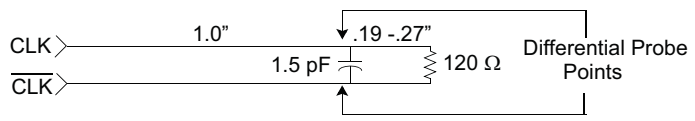
Application Notes

Clocking Timing Methodology

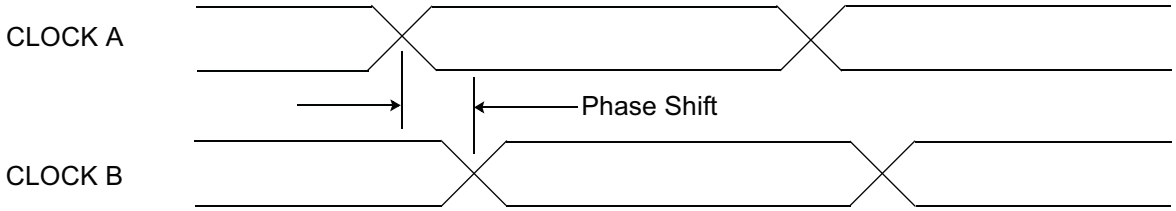
The clock to SDRAM delay is intended to be optimized for high speed operation, while permitting a variety of component layout options. As with Registered DIMMs, the entire clock delay is present between the clock tab pin and the PLL input, and is accomplished via a trace length and a series resistor. This delay should be modeled by the module supplier, to ensure accuracy, if a raw card other than one of the 'reference designs' is utilized. The clock proposed 'Reference Net' below is provided for use during module simulation to ensure an accurate clock delay, since measurement of the delay is impractical (due to the reflections at the clock tab pin).

Registered DIMM Differential Clock Reference Net



Note: Lengths in inches
Z_0 = 60.0 Ohms
t_0 = 2.2 ns/ft

Timing phase shift in two different DDR clock-pair signals is always measured between the two crossing points of the two-clock pairs as follows:



The clock delay from the input of the PLL to the input of any SDRAM is designed to be 0ns (nominal). The clock arrival time at the PLL input should not be adjusted, although sources of timing variation include PLL input capacitance, padding capacitor and termination resistor tolerances, and DIMM impedance variations (the latter items have a minor affect). Due to these variations, it is possible that there will be a difference between the input of the PLL and the input of the SDRAM. A reasonable target for this variation is +/–100ps (mean value).

The most important factor in clock measurements is to ensure consistent clock arrival times at the SDRAM. The clock reference board Registered DIMM reference net provides the standard net delay for this measurment. The DIMM suppliers must adjust the value of the PLL feedback capacitor to place the clock arrival at the SDRAM on the DIMM within ±100ps of the clock arrival at the Registered DIMM clock reference net (measured as a 'mean', since the PLL and source jitter makes this measurement difficult). This value is a target for DIMM suppliers and does not include worst case contributions of PLL skew, PLL phase error, feedback capacitor variations, and DIMM variations.

On DDR DIMMs, the clock to the register should be in phase with the SDRAM clock. The target range for variation is ±100ps. The actual delay may vary as a result of the input capacitance of the SDRAMs, the register clock input capacitance, PLL output skew variations of the PCB parasitics, and measurement skew (the later two having secondary effects). In the case when the register clocks arrive prior to the SDRAM input clock, this

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relationship may be adjusted by increasing the value of the register clock padding capacitor.

All changes defined above require simulation to verify the targeted results. Simulation of the clock nets will allow each DIMM manufacturer to determine the most effective method for achieving a 0ps nominal relationship between the register input clock and the SDRAM input clock. It is critical that this analysis be done in order to maintain the required rise-time characteristics as well as signal integrity at the input of both the SDRAM and the registers. In cases where the register clock cannot be placed in the ideal timing window, post-register timings will need to be adjusted, by the DIMM producer, to ensure robust module operation. (See Post Register Timing Example in this document for summarized clock contributions to the RDIMM budget.)

Revision Log (Part 1 of 8)

Revision Info	Page of Revision	Description of Change
Revision 0.2		Initial Release.
Revision 0.6	All	Combined Raw Card A and E into Raw Card A
		Added Raw Card E and K for TSOJ support
	1	Added x64 to organizations
		Removed support for 1Gbit SDRAMs
	6-14	Added DM support for all Raw Cards (except x4 based)
		Added CKE1 support to all 2 Bank Raw Cards
		Updated DQS/DM/DQ series resistor to 18 Ohms
		Updated Address and control series resistor to 22 Ohms
		Added 47kOhm pull down resistor to the WP on the EEPROM
		Added several notes for clarification
	15	Indicated 0ns between PLL input and SDRAM input is ‘nominal’
		Reversed order of the capacitor and resistor on the register input clock
		Added note indicating location of terminating resistor and padding capacitor
		Updated register clock net resistor termination value
	16	Fixed typo on location of A10 on the 1:2 register
		Removed note indicating use of CKE1
	20	Updated DIMM register use chart
		Changed ‘clock to output’ time specification into a standard test load versus no load. Also updated this value accordingly
		Updated setup and hold times to reflect changes with input slew rate
		Updated 1:2 register to indicate that it is only 13 bits
	21	Updated DIMM PLL use chart
	22	Updated max slew rate specification for the PLL
		Added cycle to cycle, half period, and half period cycle to cycle jitter parameters to the PLL specification
		Removed average pulse width symmetry and duty cycle parameters
		Indicated clock frequency deviation for spread spectrum is a negative percentage of the clock
	23-24	Updated Raw Card Versions --Merged A and D into A --Merged F and J into F --Added E and K

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Revision Log (Part 2 of 8)

Revision Info	Page of Revision	Description of Change
Revision 0.6 Continued	25	Updated Input loading matrix (CKE1, DM changes)
		Added target release dates for Design files
		Changed naming convention for gerbers to design files
	33-49	Add preliminary Raw Card A and B net segment lengths
		Updated DQ/DQS/DM series resistor to 18 Ohms
		Updated address and control series resistor to 22 Ohms
		Move terminating resistor and padding capacitor for all clock inputs to after the pin of the devices
	38-41	Updated data net structures to accurately reflect current designs
	44	Added a new net structure for CKE and CS on Raw Cards A, B and F
	49	Changed V_{DD} and V_{DDQ} power plane locations in stack-up
	50	Updated post register timing example with up to date data
		Changed example to 'Time to Vm' instead of using tco into no load
		Added clarification notes
	51-52	Added DIMM SPD example
	56	Added differential clock reference net
		Updated wording in register to SDRAM clock relationship paragraph
Revision 0.9	2-3, 5	Removed WP feature for upper 128 bytes in the EEPROM
	4	Corrected typo on pins 75 and 76
	6-16	Removed 47K resistor on WP Changed DQ/DQS/DM series resistor from 18 ohms to 22 ohms Removed V_{DDQ} to V_{REF} decoupling
	15	Changed terminating resistor on the register clock net from 120 ohms to 240 ohms
	20	Updated register t_{PD} Maximum to 2.8 (fixed 2.7 typo)
	22	Updated PLL specification parameters
	24	Corrected addressing on Raw Card F
	25	Updated current design file release schedule
	21-22	Updated support chip vendor list
	35-48	Added Design File C and E net structure length information
	36	Changed register clock net terminating resistor to 240 ohms
	41-44	Added post register net structure length information for Design Files A and B
	47	Updated CKE/CS net structure for Design Files C and E in order to reflect nine SDRAM loads per register output
	49	Changed stack-up: combined V_{DD} and V_{DDQ} planes and added an additional ground plane
	50	Updated post register timing budget with JEDEC changes to SDRAM input setup and hold specs. Fixed typo on DIMM PLL jitter
	53	Updated label so that Raw Card type and Revision would follow the last dash
	56	Updated Registered DIMM differential clock net to one inch from the DIMM connector to loading capacitor representing the PLL input pins

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Revision Info	Page of Revision	Description of Change
0.95	All	Changed all references of PC200 and PC266 at the DIMM level to PC1600 and PC2100
	2	Updated V_{DDSPD} description to include operation at 3.3 Volts
	3	Added V_{DDSPD} functional description
	6-14	Corrected WP on EEPROM block diagram (placed WP inside the EEPROM)
		Updated $\overline{S}$ to $\overline{CS}$ on all block diagrams
	11-14	Corrected CB labeling on the D8/26 and D17/35 SDRAM block diagram
	17-18	Changed CLK and $\overline{CLK}$ to CK and $\overline{CK}$ for consistency
	20	Added wording about IV driver characteristics and added the JEDEC item # for the registers
	21	Removed vendor names from the register sourcing
		Added PLL JEDEC item #
	22	Removed vendor names from the PLL sourcing
	23-24	Removed # of bank bits from the SDRAM Module Configuration Table
	25	Updated Design file release schedule according to the latest specification and applicable releases
	29-31	Updated TSOP stacked thickness
	34-50	Rounded all net lengths to two decimal places
	35-50	Indicated that all data for Raw Cards H&K is TBD
	51	Changed wording to indicate an “Example Eight Layer Stack”
		Added note indicating thicknesses are an example only
		Updated cross section to match production level raw card releases
		Added new section on impedance measurement coupons
	55	Updated product label to indicate Module Bandwidth instead of SDRAM frequency characteristics
1.0	1	Added full JEDEC website reference
	1-57	Updated subscripts for consistency
	2	Added FETEN, and changed address support to A12 only
	3	Added FETEN Removed A13 Removed SSTL parentheses
	4-5	CK1 and CK2 clocks flagged with note that systems may drive these pins Indicated A13 at the DIMM connector was NC for these raw cards Added WP in parentheses on pin 90 BA2 changed to NC(BA2)
	6-14	Changed EEPROM to Serial PD in the block diagram schematics
	7	Added overbar to the RESET on the register
	12-14	Added $\overline{FETEN}$ to block diagrams
	15	Updated wording in Note 4 to better describe the location of the terminating resistors
	16	Fixed typos in register pin description
	17-18	Added $\overline{QFC}$ to SDRAM pin assignments, pin 19
	19	Added conditions for output slew rate

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Revision Info	Page of Revision	Description of Change
1.0 Continued	20	Fixed typo indicating raw card C/E has two banks Added a note to the DIMM PLL Use Table describing clock padding capacitors
	21	Fixed typo - Raw Card C changed to Raw Card F
	24	Fixed typo - Raw Card F has one register on CKE1 Added note describing FET switch loading Updated DDR RDIMM design file release table to indicate raw card compliance with Revision 1.0 of the specification Added description of C3 raw card version Standardized date format in all “Released on ...” dates in the Notes column
	25-30	Flipped the PLL so that Pin 1 is on the left bottom side, the same as the design files Moved serial EEPROM to the top right corner to be consistent with design files Moved components to more accurately reflect the design file component placement
	28, 30	Updated TSOP stack thickness values to encompass industry standard values
	32, 36, 37	Updated DQ resistor tolerance to ± 5%
	33	Updated CK[2:0] to CK[0] Updated TL1 value to match design file Revised TL1 value
	34	Corrected typo on length designators Added min and max values for TL0 Corrected TL2 length Added TL3 lengths Corrected TL2 max value for A card and TL1 max and min for B card (PLL to SDRAM) Corrected A and B cards’ min TL2 length (PLL to Register)
	36	Corrected Total lengths
	41	Corrected numerous net lengths
	43	Changed shown lengths to two decimal places
	45	Changed TL4 min value
	47	Changed TL0 max value on C card and TL4 max value on E card
	50	Corrected mistake in cross section to match design file releases Removed extra “example” label
	51	Updated PC200 DIMM to PC1600 naming convention
	52	Corrected JEDEC reference for DDR SPDs
	54	Updated 1 GB/sec typo to 1.6 GB/sec Added comment on DIMM manufacturer’s label
	55	Updated side width callouts to go to edges of DRAMs Moved components to more accurately reflect the design file component placement
1.1	i	Deleted “Prepared By IBM, Micron Technology, and Server Works”
	ii	Removed disclaimer
	iii	Added overbar to CS
	1	Change description on JEDEC SPD spec to JC 42.5, rev 0 Added 64 bit version

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Revision Log (Part 5 of 8)

Revision Info	Page of Revision	Description of Change
1.1 Continued	2	Added A13 Changed $\overline{S0}$ - $\overline{S3}$ to $\overline{S}0$ - $\overline{S}3$
	3	Changed $\overline{S0}$ - $\overline{S3}$ to $\overline{S}0$ - $\overline{S}3$ Added A13; increased row addresses to R13 and column addresses to C12
	4	Pin 103 now $\overline{FETEN}$ or NC, pin 167 now A13/NC and pin 115 definition clarified as A12/NC Changed note 1 to permit NC pins 103 and 157 “be connected to inactive signals on the base-board.” Changed $\overline{S0}$ - $\overline{S3}$ to $\overline{S}0$ - $\overline{S}3$
	6, 7, 10	$\overline{CS}0$ changed to $\overline{S}0$ and $\overline{S}0$ changed to $\overline{CS}$ Clarified V_{SS} TO V_{DDSPD} connection
	8, 9, 11, 14	Corrected subscript notation on voltages $\overline{CS}0$, $\overline{CS}1$, changed to S0, S1 changed to CS, CS1 Clarified V_{SS} to V_{DDSPD} connection Corrected subscript notation on voltages Changed $\overline{FETEN}$ pin from TBD to 103
	12	Corrected subscript notation on voltages $\overline{CS}0$, $\overline{CS}1$, changed to $\overline{S}0$, $\overline{S}1$ and $\overline{S}0$, $\overline{S}1$ changed to $\overline{CS}$ Clarified V_{SS} to V_{DDSPD} connection Corrected subscript notation on voltages Corrected block diagram error on DM0 AND DQS0 Changed $\overline{FETEN}$ pin from TBD to 103
	13	Corrected subscript notation on voltages $\overline{CS}0$ - $\overline{CS}1$ changed to $\overline{S}0$ - $\overline{S}1$ and $\overline{S0}$ - $\overline{S1}$ changed to $\overline{CS}$. Also $\overline{S}0$, $\overline{S}1$ and address register outputs incorrectly identified Clarified V_{SS} to V_{DDSPD} connection Corrected subscript notation on voltages Corrected block diagram error on DMO and DQS0 Changed $\overline{FETEN}$ pin from TBD to 103
	16	Corrected typo showing A1/RA1 assigned to Register 2 rather than Register 1 Removed reference to card D Added Card E to 1:2 register group Changed $\overline{CS}0$, $\overline{CS}1$ to $\overline{S}0$, $\overline{S}1$
	17, 18	256MB now 256Mb
	19	Changed CLK and CLK to CLK and $\overline{CLK}$
	20	Clarified use of padding capacitors in note 1 on Card A
	21	Changed Max t_{jit}(hper) to 100ps; was -100ps Added “or by external control $\overline{FETEN}$ at DIMM connector pin 103”
	25-30	Changed hole spacing to correct JEDEC standard of 128.95/5.077 Changed hole size to correct JEDEC standard of 2.50/0.098 Changed overall DIMM height to 43.18 Showed more realistic PLL physical size

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Revision Log (Part 6 of 8)

Revision Info	Page of Revision	Description of Change
1.1 Continued	31, 33	Changed CK[0] to CK, $\overline{CK}$
	31, 41, 43, 44, 45, 48	Added overbar to CS[0:1]
	34	Corrected errors on clock feedback notation TL0 Min. for cards C, E, H, K changed to 2.93 Added note clarifying use of padding capacitor on A-card
	43	Changed TL7 to reflect max and min values for card A
	51	Corrected t_{REG} setup time to -0.10 and changed Margin to 3.275
	52	Removed reference to JEDEC Ballot JC 42.5-5-99-129 item 894A Added that example was for PC1600 and DDR 200
	53	Changed bytes 32 and 33 to reflect correct times -1.2 ns Corrected definition of bytes 34 and 35 Changed byte 40 to 61 (in 36-61 row) and added reserved “for VCSDRAM” Added new definitions for bytes 41 through 45 Added bytes 46-61 as Superset Information
	56	Changed card overall height dimension to “nom” - was max Showed more realistic PLL physical size
	58	Clarified differential probe points and cross-point timing measurements and measurement methodology

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Revision Info	Page of Revision	Description of Change
1.2	5	Added 1.2” height to DIMM dimension. Added 1Gb SDRAM to SDRAM supported.
	10, 11, 12, 13	Added Raw Card L. Changed A12 to A13. Added Note 7.
	14	Added Raw Card M. Changed A12 to A13. Added Note 6.
	18	Added Raw Card L to the left table. Added In: A13 - Out: RA13. Changed Note 1 to include 1Gb. Added Note 2 for 1Gb. Added the reference to JC-40 naming conventions and package type.
	19	Added Table for Raw Card M. Added the reference to JC-40 naming conventions and package type.
	20	Added 1Gb Changed Pin17 to A13.
	21	Added 1Gb Changed Pin17 to A13. Changed the reference from the ballot JC-42.3-98-227A to the standard JESD 79.
	22, 23, 24	Added Raw Card L and M. Added the reference to JC-40 naming conventions and package type.
	26	Added Raw Card L and M module configurations. Added 1GB and 2GB DIMM configurations for Raw Card L and M.
	28	Added Raw Card L and M.
	33	Added Raw Card L and M Component Placement.
	34	Added Raw Card L Component Placement.
	36, 38, 39, 42, 42, 44, 45	Added Raw Card L and M and its trace length in the tables.
	48, 49	Added Raw Card L and M Net Structure Routing for Address and Control.
	52, 54, 55	Added Raw Card L and M Net Structure Routing for $\overline{CS}$ and CKE
	71	Added Raw Card L and M to Product label.
		Added 1.2” height drawing.
1.3		Removed all Raw Card F/H/K relative comments, Block Diagram and Tables
		Corrected the errata
	11	Added Raw Card N Block Diagram
	15	Corrected to One SSTV32852 from two SSTV32852 and added the note
	18, 19	Added SSTV32852 Register specification and DIMM PLL use
	24	Changed the Design File name
	36	Added Net structure routing for PLL feedback Path (Raw Card N)
	40	Added Net structure routing for PLL Output to Register load (Raw Card N)

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Revision Info	Page of Revision	Description of Change
1.3	41	Added Trace Length for Data and DQS Net structure (Raw Card N)
	47	Added Net Structure Routing for Address and Control (Raw Card N)
	48	Added Trace Length for Address and Control Net structure (Raw Card N)
	53	Added Net Structure Routing for $\overline{CS}$ and CKE (Raw Card N)
	54	Added Trace Length for $\overline{CS}$ and CKE (Raw Card N)
	68	Added Product label for Raw Card N

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