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(54) **MULTI-RANK MEMORY MODULE THAT EMULATES A MEMORY MODULE HAVING A DIFFERENT NUMBER OF RANKS**

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(58) **Field of Classification Search** ..... None
See application file for complete search history.

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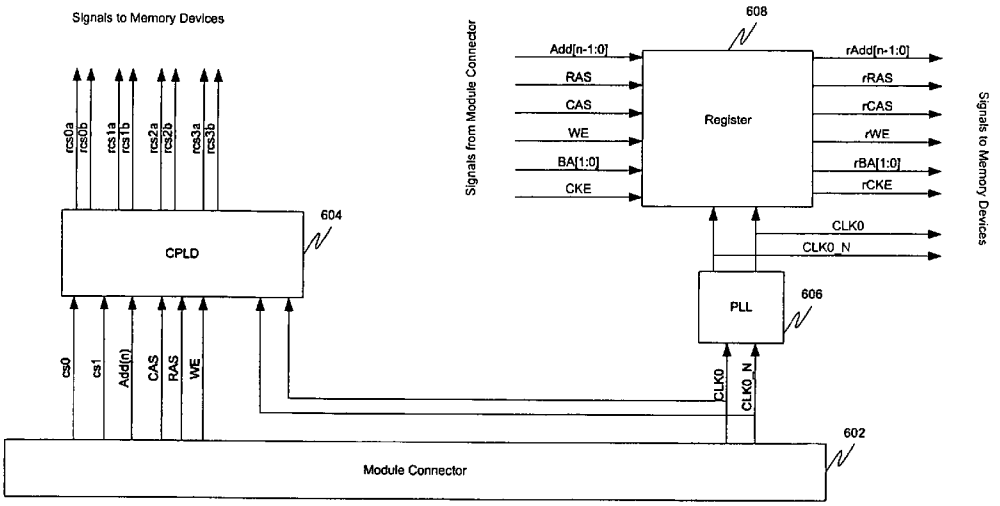
(57) **ABSTRACT**

A transparent four rank memory module has a front side and a back side. The front side has a third memory rank stacked on a first memory rank. The back side has a fourth memory rank stacked on a second memory rank. An emulator coupled to the memory module activates and controls one individual memory rank from either the first memory rank, the second memory rank, the third memory rank, or the fourth memory rank based on the signals received from a memory controller.

8 Claims, 10 Drawing Sheets



Row Address Decoding

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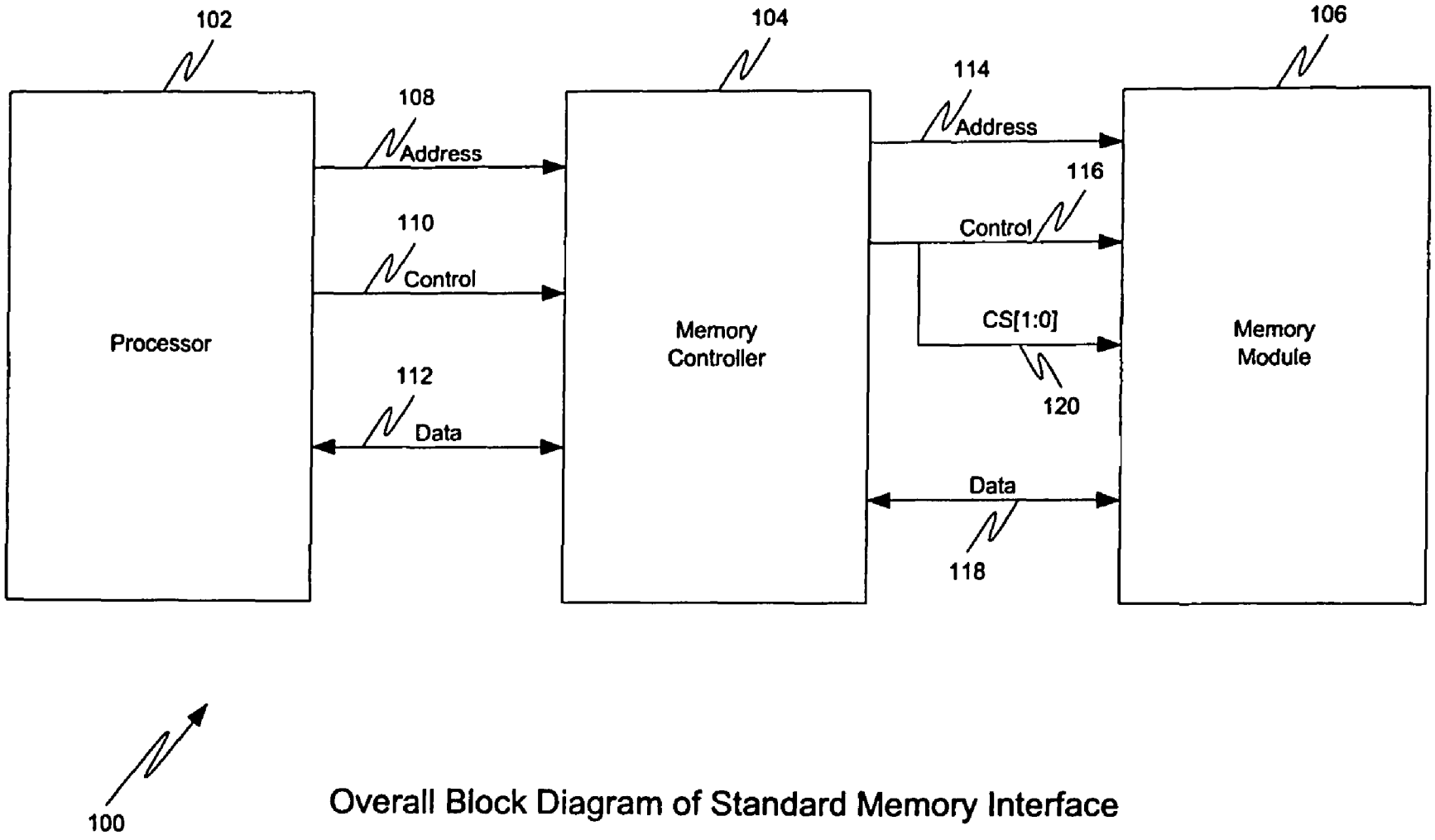
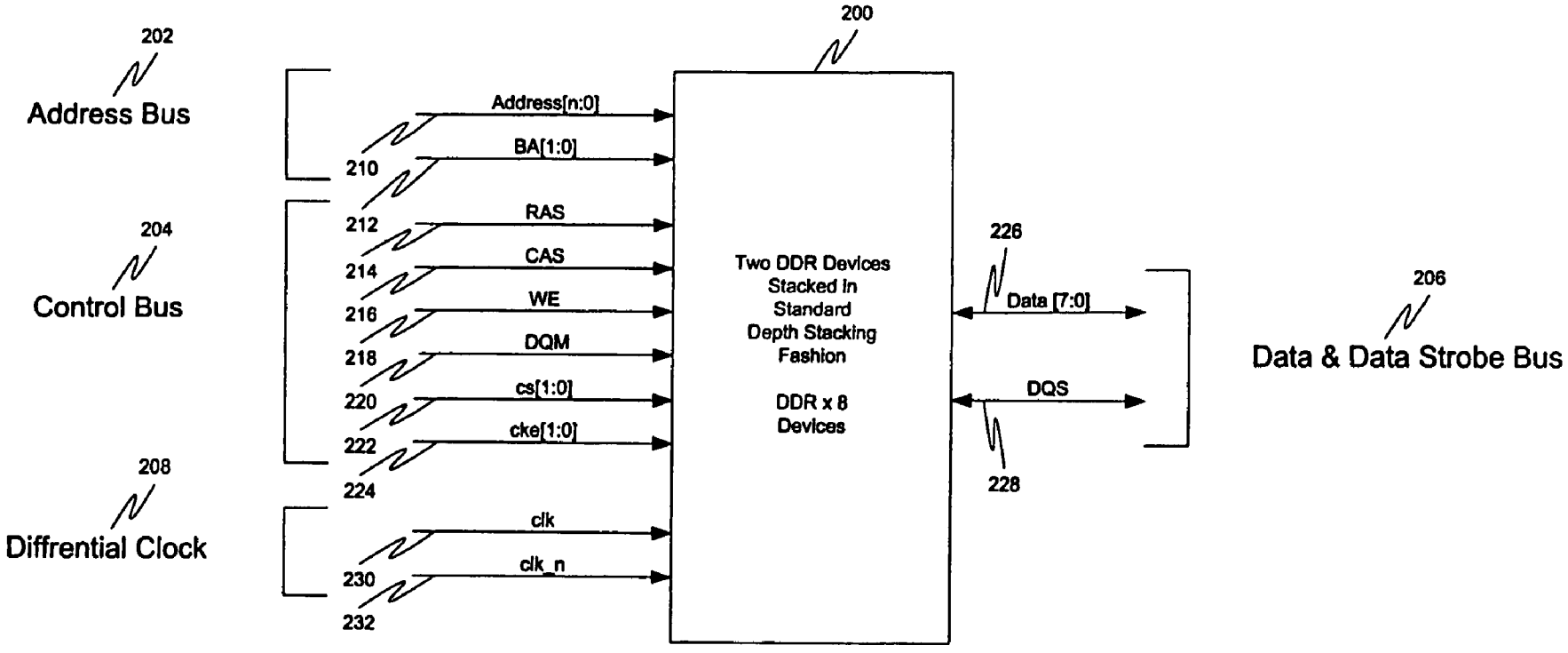


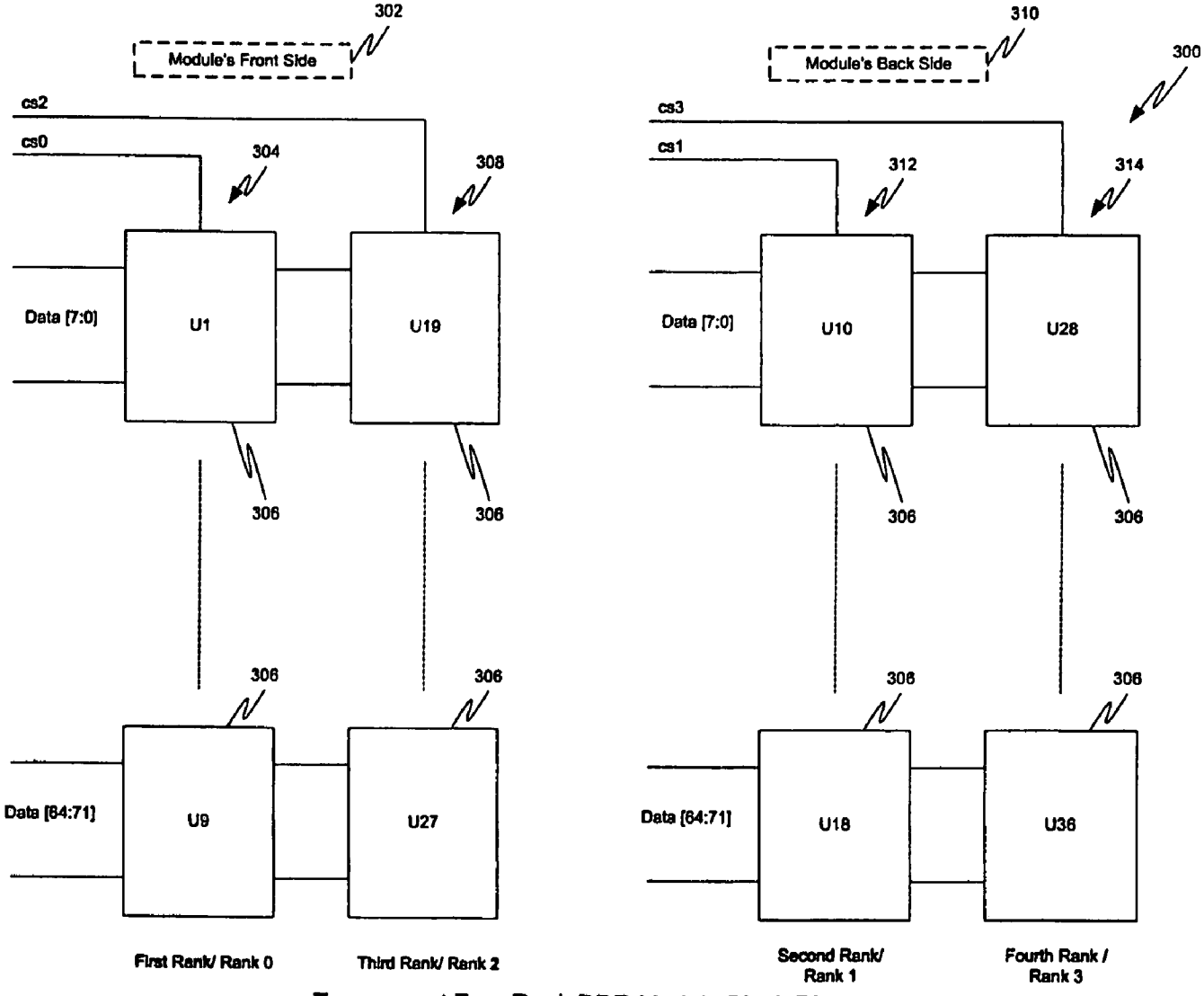
Overall Block Diagram of Standard Memory Interface

FIG. 1 - PRIOR ART

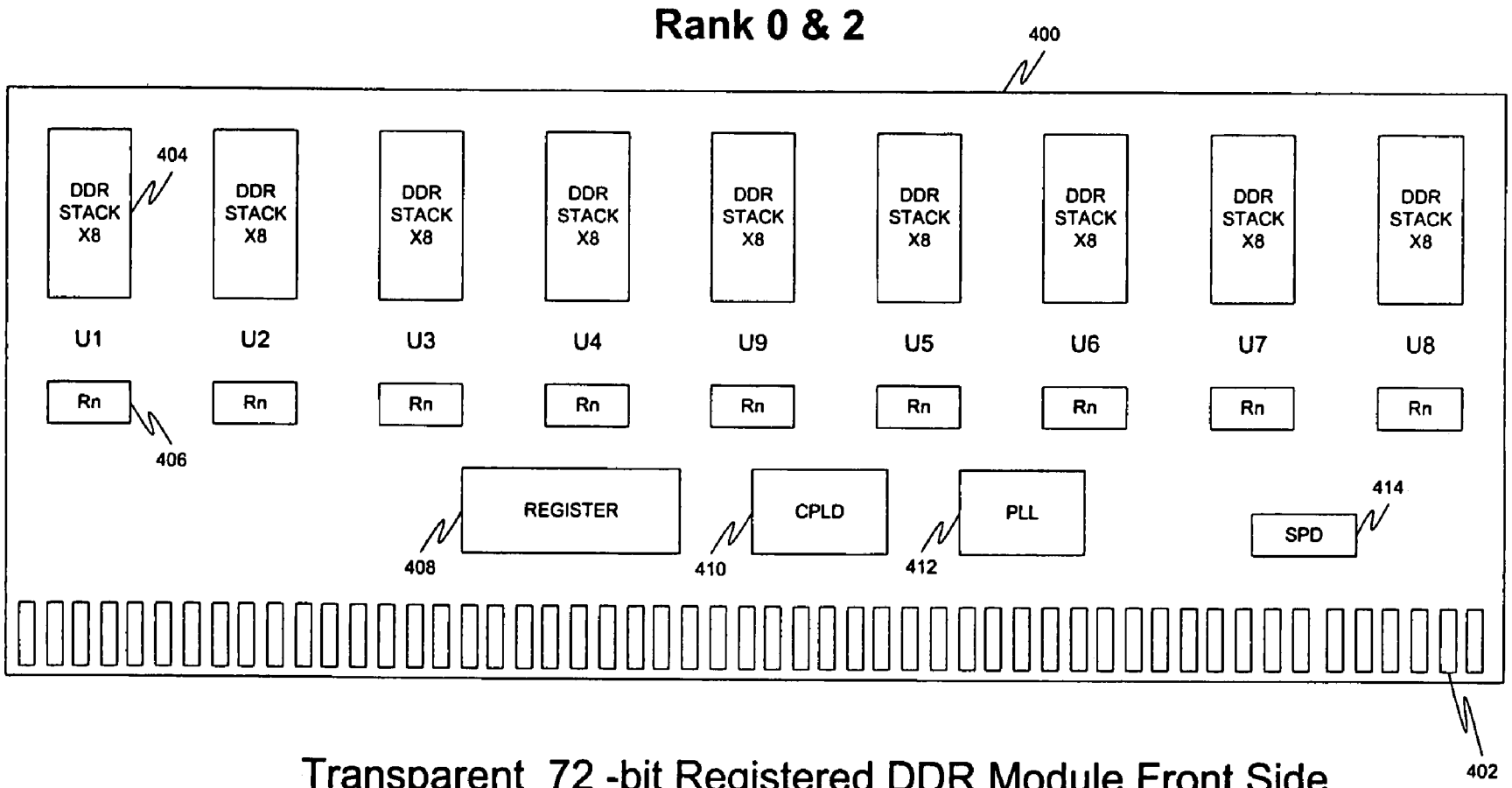


Standard DDR Device Depth Stacking Block Diagram

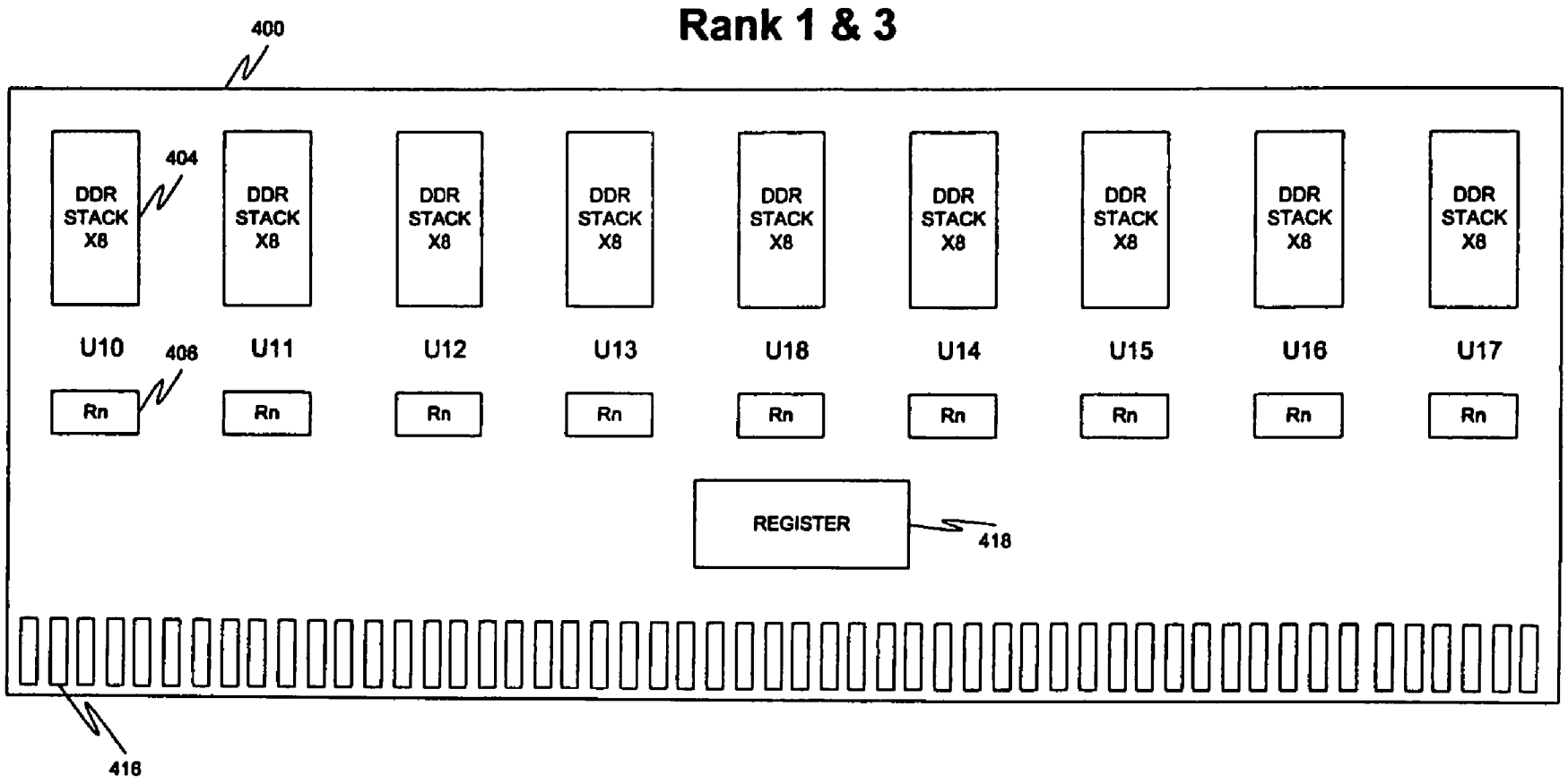
FIG. 2



Transparent Four Rank DDR Module Block Diagram
FIG. 3



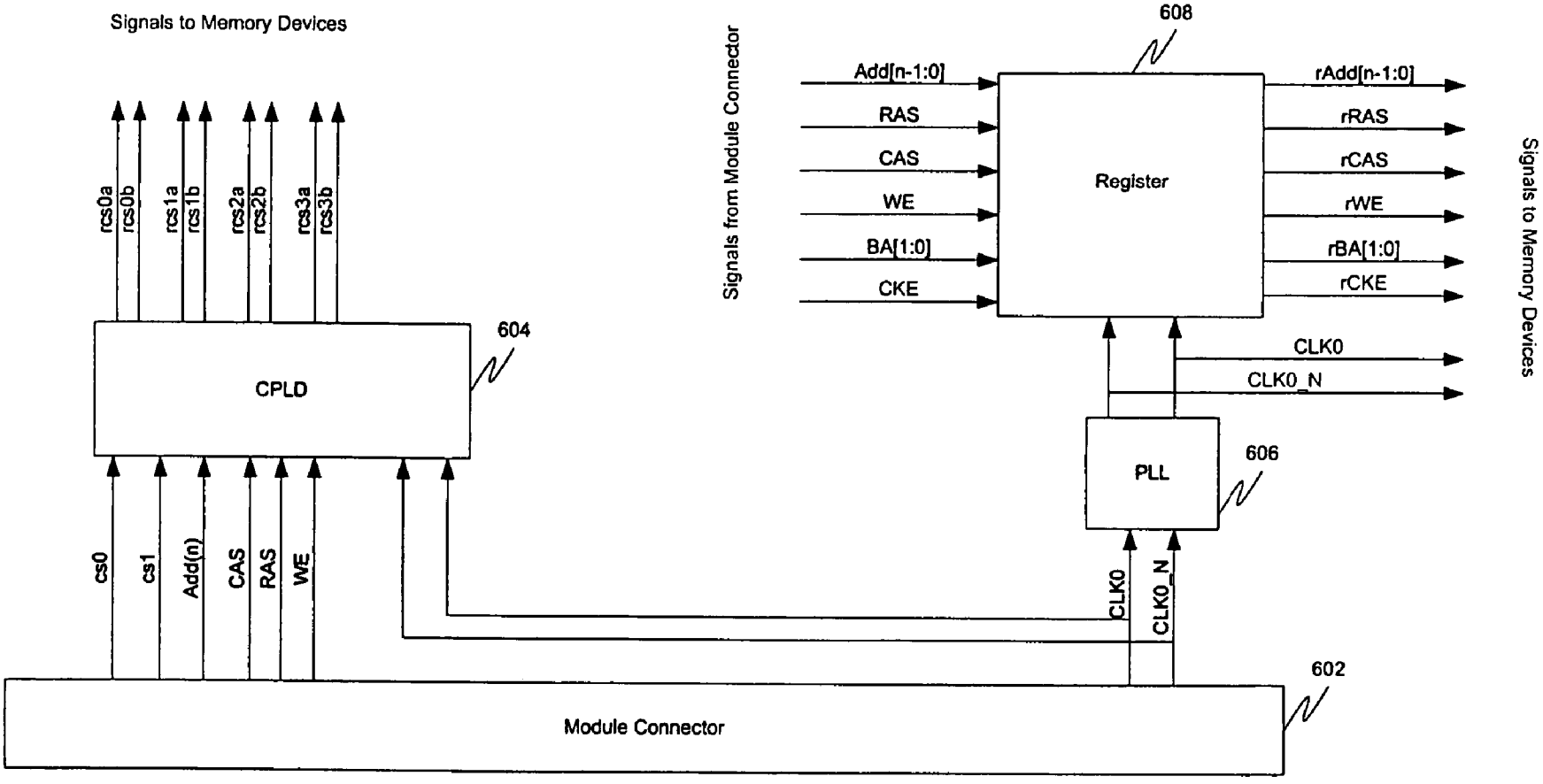
Transparent 72 -bit Registered DDR Module Front Side
FIG. 4A



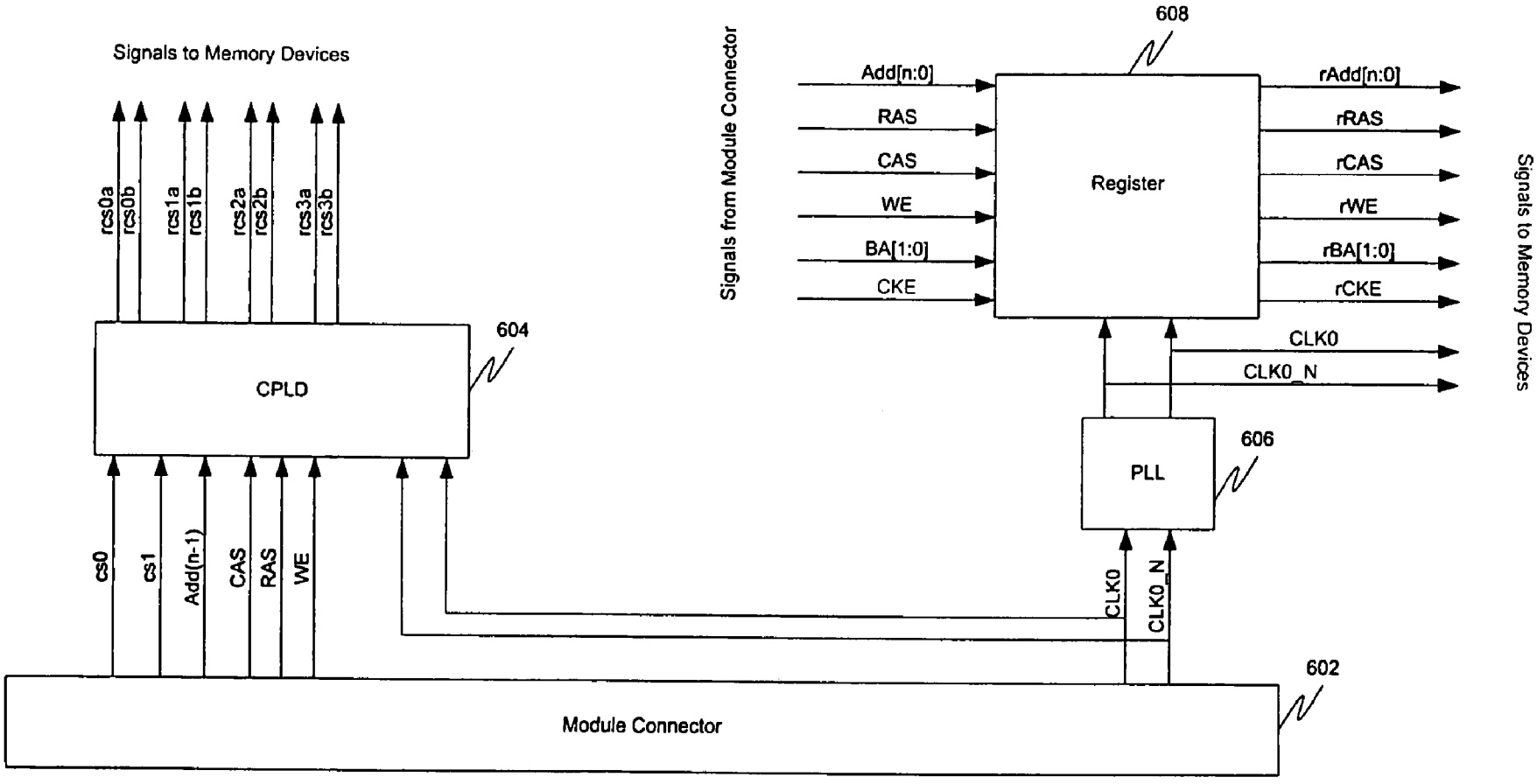
Transparent 72 -bit Registered DDR Module Back Side
FIG.4B

Add(n)	CS1	CS0	Active Bank
0	1	0	0
0	0	1	1
1	1	0	2
1	0	1	3

Truth Table
FIG.5



Row Address Decoding
FIG.6A



Column Address Decoding
FIG.6B

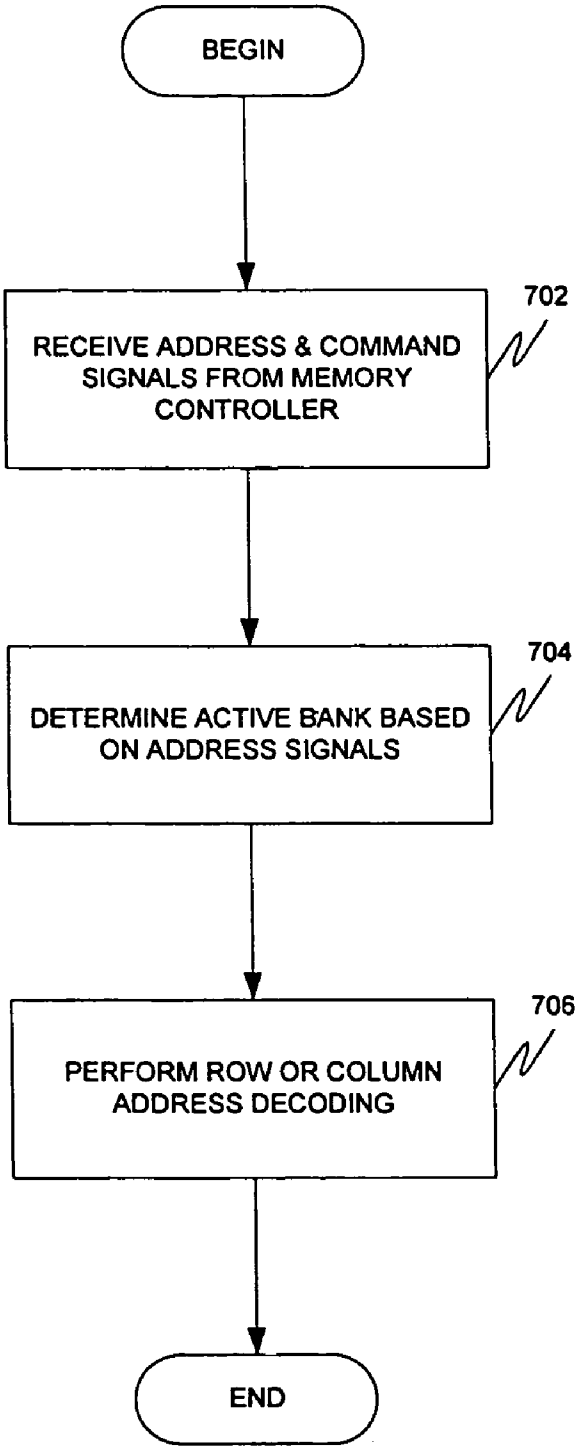
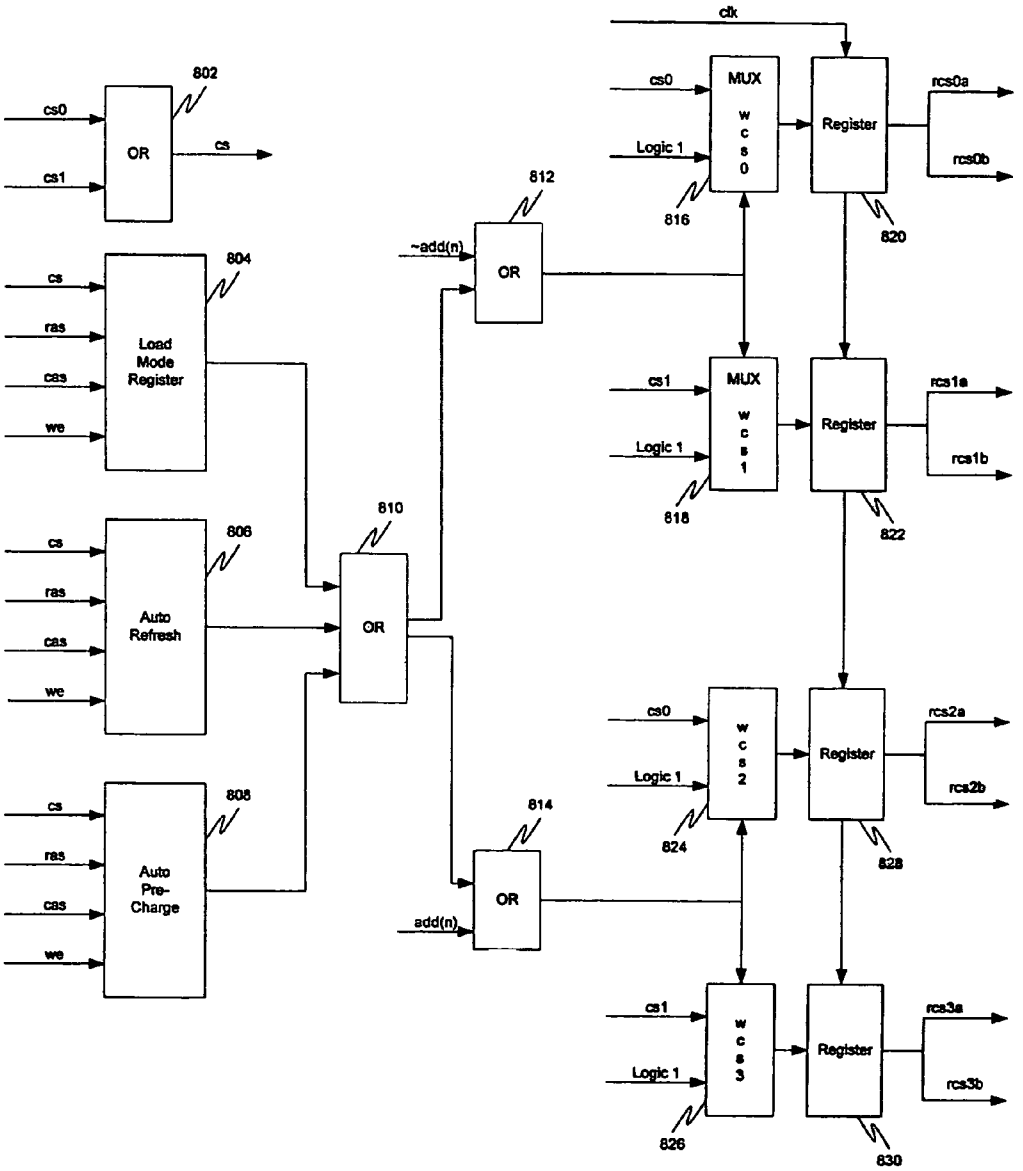

BEGIN
RECEIVE ADDRESS & COMMAND SIGNALS FROM MEMORY CONTROLLER
702
DETERMINE ACTIVE BANK BASED ON ADDRESS SIGNALS
704
PERFORM ROW OR COLUMN ADDRESS DECODING
706
END

FIG.7



Bank EmulatorBlock Diagram
FIG.8

MULTI-RANK MEMORY MODULE THAT EMULATES A MEMORY MODULE HAVING A DIFFERENT NUMBER OF RANKS

FIELD OF THE INVENTION

The present invention relates to computer memory. More particularly, the present invention relates to a four rank memory module.

BACKGROUND OF THE INVENTION

Computers use memory devices for the storage and retrieval of information. These memory devices are often mounted on a memory module to expand the memory capacity of a computer. Sockets on a main board accommodate those memory modules also known as single inline memory modules ("SIMMs") or dual in-line memory modules ("DIMMs").

FIG. **1** is a diagram schematically illustrating a standard memory interface system overview in accordance with a prior art. The system **100** includes a processor **102**, a memory controller **104**, and a memory module **106**. The processor **102** communicates with the memory controller **104** with an address bus **108**, a control signal bus **110**, and a data bus **112**. The memory controller **104** communicates with the memory module **106** with a controller address bus **114**, a controller control signal bus **116**, and a controller data bus **118**. Common system implementations **100** have typically two memory chip selects routed per socket. Common memory module **106** may have two chip selects (one per rank) or four chip selects (two per rank). In one implementation, each chip select from the controller is connected to the corresponding chip select on the memory module. In the second implementation, each chip select from the controller is connected to the two chip selects (those that control one rank) on the memory module. The system chip select signals control individual memory modules ranks. The memory module **106** is coupled to the memory controller **104** through a memory socket.

Standard memory modules such as memory module **106** have either one rank or two rank of memory devices. Each memory device comes in a variety of configurations and families such as 128 Mbit, 256 Mbit, 512 Mbit, and 1024 Mbit double data rate ("DDR") synchronous dynamic random access memory ("SDRAM") families. Each of these families is further divided into three distinct flavors such as x4, x8, and x16 data bits. For example, a single 128 Mbit DDR SDRAM family comes in three flavors of:

32M×4 (32 Mega cell of 4-bit each=32M×4-bit=128 Mbit)
16M×8 (16 Mega cell of 8-bit each=16M×8-bit=128 Mbit)
8M×16 (8 Mega cell of 16-bit each=8M×16-bit=128 Mbit)

The example above illustrates that all three different data bits flavors result in the same density of 128 Mbit. As the number of data bits doubles the cell numbers decrease by half. One can build memory modules with similar densities using different data bits flavors.

One method of building a 512 M Byte standard memory module with error correction code ("ECC") (64-bit data plus 8-bit ECC=72-bit) includes using 256 Mbit density families of 32M×8 to achieve the density of 512 M Byte as follow:

Rank 0=9×(32M×8) devices=32M×72-bit which equates to 32M×8 Bytes+1 Byte of ECC. This yields a total density of 32M×8 Bytes=256 M Byte.

Rank 1=9×(32M×8) devices=32M×72-bit which equates to 32M×8 Bytes+1 Byte of ECC. This yields a total density of 32M×8 Bytes=256 M Byte.

Therefore, a two rank memory module with 18 device placements will achieve the 512 M Byte density. Furthermore, it should be noted that a standard DDR 184-pin memory module can only fit nine thin shrink small outline package ("TSSOP") placements per side, or a total of 18 placements of TSSOP per module, considering both front and back sides based on a standard defined height limits by Joint Electron Device Engineering Council ("JEDEC").

Therefore, a two rank memory module with 18 device placements will achieve the 512M Byte density. Furthermore, it should be noted that a standard DDR 184-pin memory module can only fit nine TSSOP placements per side, or a total of 18 placements of TSSOP per module, considering both front and back sides based on a standard defined height limits by JEDEC.

Because memory devices with lower densities are cheaper and more readily available, it may be advantageous to build the above same density memory module using lower densities devices. However, in order to achieve a density of, for example, 512 M Bytes using 128 Mbit density of 16M×8 instead, the memory module needs four ranks configured as follows:

Rank 0=9×(16M×8) devices=16M×72-bit which equates to 16M×8 Bytes+1 of ECC. This would give us a total density of 16M×8 Bytes=128 M Byte.

Rank 1=9×(16M×8) devices=16M×72-bit which equates to 16M×8 Bytes+1 Byte of ECC. This would give us a total density of 16M×8 Bytes=128 M Byte.

Rank 2=9×(16M×8) devices=16M×72-bit which equates to 16M×8 Bytes+1 Byte of ECC. This would give us a total density of 16M×8 Bytes=128 M Byte.

Rank 3=9×(16M×8) devices=16M×72-bit which equates to 16M×8 Bytes+1 Byte of ECC. This would give us a total density of 16M×8 Bytes=128 M Byte.

In order to achieve the above configuration, 4 rows of 9 devices each, totaling 36 placements, are required. As mentioned above, on a standard 184-pin DDR memory module, there is only enough space for 18 TSSOP devices.

The only solution would be, to stack two memory devices together to achieve an extra rank on the same placement space. Although this would solve the placement problem of 36 TSSOP devices, the memory module would still possess four memory ranks. As explained earlier, all standard memory modules have only two chip select signals per memory socket routed. Therefore, such memory module would not be viable.

A need therefore exists for a transparent four rank memory module fitting into a memory socket having two chip select signals routed. A primary purpose of the present invention is to solve these needs and provide further, related advantages.

BRIEF DESCRIPTION OF THE INVENTION

A transparent four rank memory module has a front side and a back side. The front side has a third memory rank stacked on a first memory rank. The back side has a fourth memory rank stacked on a second memory rank. An emulator coupled to the memory module activates and controls one individual memory rank from either the first memory rank, the second memory rank, the third memory rank, or the fourth memory rank based on the signals received from a memory controller.

BRIEF DESCRIPTION OF THE DRAWINGS

The accompanying drawings, which are incorporated into and constitute a part of this specification, illustrate one or

more embodiments of the present invention and, together with the detailed description, serve to explain the principles and implementations of the invention.

In the drawings:

FIG. **1** is a block diagram schematically illustrating a standard memory interface system in accordance with a prior art.

FIG. **2** is a diagram schematically illustrating a stacked DDR device in accordance with one embodiment of the present invention.

FIG. **3** is a diagram schematically illustrating a transparent four rank DDR memory module in accordance with one embodiment of the present invention.

FIG. **4**A is a diagram schematically illustrating the front side of a transparent 72-bit registered DDR module in accordance with one embodiment of the present invention.

FIG. **4**B is a diagram schematically illustrating the back side of a transparent 72-bit registered DDR module in accordance with one embodiment of the present invention.

FIG. **5** is a truth table for a transparent four rank memory module in accordance with one embodiment of the present invention.

FIG. **6**A is a block diagram schematically illustrating a row address decoding system for a transparent four rank memory module in accordance with one embodiment of the present invention.

FIG. **6**B is a block diagram schematically illustrating a column address decoding system for a transparent four rank memory module in accordance with one embodiment of the present invention.

FIG. **7** is a flow diagram schematically illustrating a method for emulating a two rank memory module.

FIG. **8** is a block diagram schematically illustrating a CPLD in a transparent four rank DDR memory module in accordance with one embodiment of the present invention

DETAILED DESCRIPTION

Embodiments of the present invention are described herein in the context of a memory module. Those of ordinary skill in the art will realize that the following detailed description of the present invention is illustrative only and is not intended to be in any way limiting. Other embodiments of the present invention will readily suggest themselves to such skilled persons having the benefit of this disclosure. Reference will now be made in detail to implementations of the present invention as illustrated in the accompanying drawings. The same reference indicators will be used throughout the drawings and the following detailed description to refer to the same or like parts.

In the interest of clarity, not all of the routine features of the implementations described herein are shown and described. It will, of course, be appreciated that in the development of any such actual implementation, numerous implementation-specific decisions must be made in order to achieve the developer's specific goals, such as compliance with application- and business-related constraints, and that these specific goals will vary from one implementation to another and from one developer to another. Moreover, it will be appreciated that such a development effort might be complex and time-consuming, but would nevertheless be a routine undertaking of engineering for those of ordinary skill in the art having the benefit of this disclosure.

In accordance with one embodiment of the present invention, the components, process steps, and/or data structures may be implemented using various types of operating systems (OS), computing platforms, firmware, computer programs, computer languages, and/or general-purpose machines. The method can be run as a programmed process running on processing circuitry. The processing circuitry can take the form of numerous combinations of processors and operating systems, or a stand-alone device. The process can be implemented as instructions executed by such hardware, hardware alone, or any combination thereof. The software may be stored on a program storage device readable by a machine.

In addition, those of ordinary skill in the art will recognize that devices of a less general purpose nature, such as hardwired devices, field programmable logic devices (FPLDs), including field programmable gate arrays (FPGAs) and complex programmable logic devices (CPLDs), application specific integrated circuits (ASICs), or the like, may also be used without departing from the scope and spirit of the inventive concepts disclosed herein.

FIG. **2** is a block diagram of an example of a standard stacked DDR 8 bit memory device **200** used in a memory module in accordance with one embodiment of the present invention. The memory device **200** interfaces with a memory controller (not shown) with three buses: an address bus **202**, a control bus **204**, and a data bus **206**. A differential clock bus **208** is also coupled to the DDR memory device **200**.

The address bus **202** conveys the following signals: address [n:0] **210** and BA[1:0] **212**.

The control bus **204** conveys the following signals: RAS **214**, CAS **216**, WE **218**, DQM **220**, CS[1:0] **222**, and CKE [1:0] **224**.

The data bus **206** conveys the following signals: data signals [7:0] **226** and DQS **228**.

The differential clock bus **208** includes two signals: clk **230**, and clk_n **232**.

FIG. **3** illustrates a block diagram of stacked 8 bit memory devices on the front and back side of a memory module **300** in accordance with one embodiment of the present invention. The memory module's front side **302** includes a first rank 304 of memory devices **306** (U**1** through U**9**). The first rank 304 is stacked with a third rank 308 of memory devices **306** (U**19** through U**27**). As illustrated in FIG. **3**, data bus [7:0] is connected to both ranks' memory devices **306** (U**1** and U**19**). The remaining data buses are connected to their respective ranks' memory devices **306**. A chip select signal is coupled to each rank of memory devices. As illustrated in FIG. **3**, chip select signal cs**0** is connected to the first rank 304 (from U**1** to U**9**) and chip select signal cs**2** is connected to the third rank 308 (from U**19** to U**27**).

The memory module's back side **310** includes a second rank 312 of memory devices **306** (U**10** through U**18**). The second rank 312 is stacked with a fourth rank 314 of memory devices **306** (U**28** through U**36**). As illustrated in FIG. **3**, data bus [7;0] is connected to both ranks' memory devices **306** (U**10** and U**28**). The remaining data buses are connected to their respective ranks' memory devices **306**. A chip select signal is coupled to each rank of memory devices. As illustrated in FIG. **3**, chip select signal cs**1** is connected to the second rank 312 (from U**10** to U**18**) and chip select signal cs**3** is connected to the fourth rank 314 (from U**28** to U**36**).

FIG. **3** also illustrates a total of four chip select signals (cs**0**, cs**1**, cs**2**, and cs**3**). As illustrated in FIG. **2**, the stacked memory device **200** has only two chip select signals: cs[1:0] **222**. In accordance with one embodiment of the invention, the present invention allows the four rank memory modules to communicate with a memory socket having only two chip select signals routed.

FIG. **4**A illustrates a schematic diagram of the front side of a transparent 72 bit registered DDR module **400** in accordance with one embodiment of the present invention. The

memory module **400** includes 92 contact pins **402** on the front side for connecting with a memory socket (not shown). The memory module **400** as illustrated in FIG. **4**A includes nine 8 bit stacked memory devices **404**, nine corresponding Resistor Network (Rn) **406**, a register **408**, a CPLD **410**, a PLL **412**, and a SPD **414**. The stacking of the 8 bit stacked memory devices **404** was previously illustrated in FIG. **3**. Memory devices **404** (U**1** through U**9**) are mounted on a surface of the front side of the memory module **400**. Memory devices **404** (U**19** through U**27**) are respectively stacked on memory devices **404** (U**1** through U**9**). Therefore the front side of the four rank memory modules **400** includes two ranks (rank 0 and rank 2).

The register **408** is used to synchronize the incoming address and control signals with respect to differential clock signals **208** (clk and clk_n). Also, the register **408** may eliminate the loading of 36 devices in case of stacking or loading of 18 devices in case of monolithic memory devices from the main controller by separating the controller side signaling with memory side signal loading fan-out.

The PLL **412** is used to generate a zero-delay buffer off of system side input differential clock signals **208** (clk and clk_n). By using a PLL, the system side will not see the loading effect of either 18 differential clock loads or 36 differentials clock loads in the case of stacking memory devices.

The SPD **414** is a simple I2C interface EEPROM to hold information regarding memory module for BIOS during the power-up sequence.

The CPLD **410** emulates a two rank memory module on the four rank memory module **400**. CPLD **410** allows a system having a memory socket with only two chip select signals routed to interface with a four rank memory module where typically a two rank memory module couples with the memory socket. The CPLD **410** determines which rank from the four ranks to activate based upon the address and command signals from a memory controller coupled to the memory module **410**. The algorithm of CPLD **410** is further described in FIGS. **5** and **7**.

FIG. **4**B illustrates a schematic diagram of the back side of the transparent 72 bit registered DDR module **400** in accordance with one embodiment of the present invention. The memory module **400** includes 92 contact pins **416** on the back side for connecting with a memory socket (not shown). Therefore, memory module **400** has a total of 184 different contact pins on the front and back side. The memory module **400** as illustrated in FIG. **4**B includes nine 8 bit stacked memory devices **404**, nine corresponding Resistor Network (Rn) **406**, another register **418**. The stacking of the 8 bit stacked memory devices **404** was previously illustrated in FIG. **3**. Memory devices **404** (U**10** through U**18**) are mounted on a surface of the back side of the memory module **400**. Memory devices **404** (U**28** through U**36**) are respectively stacked on memory devices **404** (U**10** through U**18**). Therefore the back side of the four rank memory module **400** includes two ranks (rank 1 and rank 3).

FIG. **5** illustrates a truth table used in the process of the CPLD **410** to determine which rank is active (rank 0, rank 1, rank 2, or rank 3). CPLD **410** utilized three variables to determine the active rank: the highest address number Add (n), a first chip select signal (CS**0**), and a second chip select signal (CS**1**). As previously mentioned, each memory socket includes two active chip select signals (CS**0** and CS**1**). CPLD **410** combines these two variables (CS**0** and CS**1**) with the address number signal **210** from the address bus **202** to determine the active rank. Add(n) includes the highest binary digit from the address number signal **210**. For example, the highest address number Add(n) when the address signal **210** is 10010 would be the first digit to the left: "1".

As illustrated in FIG. **5**, rank 0 is active when the Add(n) is 0, CS**1** is 1, and CS**0** is 0. Rank 1 is active when the Add(n) is 0, CS**1** is 0, and CS**0** is 1. Rank 2 is active when the Add(n) is 1, CS**1** is 1, and CS**0** is 0. Rank 3 is active when the Add(n) is 1, CS**1** is 0, and CS**0** is 1.

Because the row address and column address may differ between different memory device densities, the CPLD may employ two different decoding schemes: a Row Address Decoding scheme, and a Column Address Decoding scheme. The following non-limiting example is used for illustration purposes.

A 512 MByte memory module may be build with either two rank of 256 MByte density per rank or four ranks of 128 MByte density per rank. However, a 128 Mbit DDR SDRAM has different characteristics from a 256 Mbit DDR SDRAM device.

A 128 Mbit DDR SDRAM (16M×8) has the following characteristics:

Configuration	4M × 8 × 4
Refresh Rate	4K
Row Address	A0-A11
Column Address	A0-A9

A 256 Mbit DDR SDRAM (32M×8) has the following characteristics:

Configuration	8M × 8 × 4
Refresh Rate	8K
Row Address	A0-A12
Column Address	A0-A9

The size of the column addresses (A**0**-A**9**) for both 128 Mbit DDR SDRAM and 256 Mbit DDR SDRAM devices match. However, the size of the row address for the 128 Mbit DDR SDRAM differs by one row address line from the 256 Mbit DDR SDRAM (A**12**). The CPLD **410** uses a Row Address Decoding scheme to emulate a two rank based on 256 Mbit DDR SDRAM Device Technology memory module with a four rank based on 128 Mbit DDR SDRAM Device Technology memory module. Under this scheme, address lines A**0**-A**11** go to module register **408** and **418** and address lines A**12** goes into CPLD **410** along with CS**0** and CS**1** for proper decoding. Therefore, the extra address line A**12** is used by the CPLD to determine which rank (from the four ranks) is active. The decoding is performed as previously illustrated in FIG. **5** above. For example, if address bus (A**12**-A**0**) has "1000010101010" and CS**0** is "0" and CS**1** is "1", then rank 2 is activated. In this present example, Add(n) for A**12** is "1". The Row Address Decoding scheme is further illustrated in FIG. **6**A.

FIG. **6**A illustrates a method for decoding row addresses in accordance with one embodiment of the present invention. A module connector **602** (for example, the contact pins **402** and **416**) sends signals to the CPLD **604**, PLL **606**, and register **608**. The signals sent to CPLD **604** include cs**0**, cs**1**, Add(n), CAS, RAS, WE, CLK**0**, and CLK**0**_N. The signals sent to PLL **606** include CLK**0**, and CLK**0**_N. PLL relays the CLK**0** and CLK**0**_N signals to register **608** and memory devices **306**. Register **608** also receives the following signals from module connector **602**: Add[n−1;0], RAS, CAS, WE, BA[1:0], CKE.

As illustrated in the example above, the 256 Mbit memory devices has an extra row address line (A**12**) when compared to the 128 Mbit memory devices. Register **608** of a four rank memory module emulating a two bank memory module receives an address with an address size matching the address size of the lower density memory devices (128 Mbit), i.e. A**0**-A**11**. In other words, the address signal from the module connector **608** does not include the extra row address line A**12**.

CPLD **604** also ensures that all commands for a two rank memory module conveyed by the module connector **602** are also performed on the four rank memory modules. For example, CPLD **604** generates rcs**2** and rcs**3**, besides rcs**0** and rcs**1** off of CS**0**, CS**1** and Add(n) from the memory controller side. CPLD **604** also generates rcs**2** when CS**0** Auto Precharge all Banks Commands are issued. CPLD **604** also generates rcs**3** when CS**1** Auto Precharge all Banks Commands are issued. CPLD **604** also generates rcs**2** when CS**0** Auto Refresh Commands are issued. CPLD **604** also generates rcs**3** when CS**1** Auto Refresh Commands are issued. CPLD **604** also generates rcs**2** when CS**0** Load Mode Register Commands are issued. CPLD **604** also generates rcs**3** when CS**1** Load Mode Register Commands are issued.

However, as previously mentioned, a memory module may also be built using two device families which only differs in their column address size, and have the same row address size. The following example illustrates this situation and describes the Column Decoding Scheme.

A 1024 Mbyte memory module may be build with either two rank of 512 MByte density per rank or four ranks of 256 MByte density per rank. However, the 256 Mbit DDR SDRAM has different characteristics from a 512 Mbit DDR SDRAM.

A 256 Mbit DDR SDRAM (32M×8) has the following characteristics:

Configuration	8M × 8 × 4
Refresh Rate	8K
Row Address	A0-A12
Column Address	A0-A9

A 512 Mbit DDR SDRAM (64M×8) has the following characteristics:

Configuration	16M × 8 × 4
Refresh Rate	8K
Row Address	A0-A12
Column Address	A0-A9, A11

The size of the row addresses (A**0**-A**9**) for both 256 Mbit DDR SDRAM and 512 Mbit DDR SDRAM devices match. However, the size of the column address for the 256 Mbit DDR SDRAM differ by one address line from the 512 Mbit DDR SDRAM (A**11**). The CPLD **410** uses the Column Address Decoding scheme to emulate a two ranks 512 Mbit based DDR SDRAM device Technology memory module with a four ranks 256 Mbit based DDR SDRAM device Technology memory module. Under this scheme, address lines A**0**-A**12** go to module register **408** and **418** and address lines A**11** goes into CPLD **410** along with CS**0** and CS**1** for proper decoding. Therefore, the address line A**11** is used by the CPLD to determine which rank (from the four ranks) is active. The decoding is performed as previously illustrated in FIG. **5** above. For example, if address bus (A**11**, A**9**-A**0**) has "100110101010" and CS**0** is "0" and CS**1** is "1", then rank 2 is activated. In this present example, Add(n) for A**11** is "1". The Column Address Decoding scheme is further illustrated in FIG. **6**B.

FIG. **6**B illustrates a method for decoding column addresses in accordance with one embodiment of the present invention. A module connector **602** (for example, the contact pins **402** and **416**) sends signals to the CPLD **604**, PLL **606**, and register **608**. The signals sent to CPLD **604** include CS**0**, CS**1**, Add(n−1), CAS, RAS, WE, CLK**0**, and CLK**0**_N. The signals sent to PLL **606** include CLK**0**, and CLK**0**_N. PLL relays CLK**0** and CLK**0**_N signals to register **608** and memory devices **306**. Register **608** also receives the following signals from module connector **602**: Add[n;0], RAS, CAS, WE, BA[1:0], CKE.

As illustrated in the example above, the 512 Mbit memory devices has an extra column address line (A**11**) when compared to the 256 Mbit memory devices. Register **608** of a four rank memory module emulating a two rank memory module receives an address with an address size matching the address size of the lower density memory devices (256 Mbit), i.e. A**0**-A**12**.

CPLD **604** also ensures that all commands for a two rank memory module conveyed by the module connector **602** are also performed on the four rank memory modules. For example, CPLD **604** generates rcs**2** and rcs**3**, besides rcs**0** and rcs**1** off of CS**0**, CS**1** and Add(n) from the memory controller side. CPLD **604** also generates rcs**2** when CS**0** Auto Precharge all Banks Commands are issued. CPLD **604** also generates rcs**3** when CS**1** Auto Precharge all Banks Commands are issued. CPLD **604** also generates rcs**2** when CS**0** Auto Refresh Commands are issued. CPLD **604** also generates rcs**3** when CS**1** Auto Refresh Commands are issued. CPLD **604** also generates rcs**2** when CS**0** Load Mode Register Commands are issued. CPLD **604** also generates rcs**3** when CS**1** Load Mode Register Commands are issued.

It should be noted that the internal circuitry in the CPLD **410** for Row Address Decoding and Column Address Decoding are different. In particular, in the Column Address Decoding scheme, a unique decoding circuitry is required because in a standard DDR memory module there is only one set of address lines and memory organized as a matrix in such that in order to access an x4, x8 or x16 cell, two set of addresses needs to be provided. First, the Row address needs to be provided with the proper control and command signals then on a separate cycle, the Column address needs to be provided with its proper control and command signals in order to read or write to that particular cell.

FIG. **7** illustrates a method for emulating a two rank memory module with a four rank memory module in accordance with one embodiment of the present invention. At **702**, the memory module receives a command signal and address signal from a memory controller. The memory controller addressed the command signal and address signal to a two rank memory module. The command signal includes CS**0**, CS**1**, CKE, CAS, RAS, and WE. The address signal includes Add(n). At **704**, the CPLD of the four rank memory module determines which rank should be active based on the address and command signals (cs**0**, cs**1**, and Add(n)). This determination was previously described using the truth table illustrated in FIG. **5**. At **706**, the CPLD performs either a Row Address Decoding scheme or a Column Address Decoding scheme as previously described to relay the command signals.

It should be noted that the physical address lines and logical address lines are different in this methodology. This is a non-linear addressing versus SRAM which uses linear

addressing. In this methodology, a much lower number of pins are used to access the same amount of memory locations as a SRAM device with longer latency due to multiple cycle of providing the Row and Column logical addresses.

FIG. **8** is a block diagram schematically illustrating the internal circuitry of a CPLD used in the transparent four rank DDR memory module. CS**0** signal and CS**1** signal generate a CS internal signal through logical device **802**. The CS signal is transmitted to Load mode register **804**, auto refresh **806**, and auto precharge detection **808** sub circuitries.

The Load Mode Register circuitry **804** also receives Chip Select (CS) signal, Row Address Strobe (RAS) signal, Column Address Strobe (CAS) signal, and Write Enable signal (WE). This module **804** detects load mode register cycle if inputs are asserted properly to indicate LMR command.

The Auto Refresh circuitry **806** receives Chip Select (CS) signal, Row Address Strobe (RAS) signal, Column Address Strobe (CAS) signal, and Write Enable signal (WE). This module **806** detects auto refresh cycle if inputs are asserted properly to indicate Auto Refresh command.

The Auto Precharge circuitry **808** receives Chip Select (CS) signal, Row Address Strobe (RAS) signal, Column Address Strobe (CAS) signal, and Write Enable (WE) signal. This module **808** detects auto precharge cycle if inputs are asserted properly to indicate auto precharge command.

The output of all three sub circuitries (LMR **804**, auto refresh **806** and auto precharge **808**) will go to a logical device OR **810** which will drive another level of OR logic **812** and **814** along with either highest address line (**814**) or it's inverted state (**812**).

The inverted state drives both MUX wcs**0** and wcs**1** blocks **816** and **818** which goes to a respective register **820** and **822** and gets fan-out into rcs**0***a* and rcs**0***b* or rcs**1***a* or rcs**1***b* eventually.

The non-inverted state will drive both MUX wcs**2** and wcs**3** blocks **824** and **826** which goes to a respective register **828** and **830** and gets fan-out into rcs**2***a* and rcs**2***b* or rcs**3***a* or rcs**3***b* eventually.

Many other families of memory devices or densities of memory devices (not shown) may be used to build the four rank memory module. Those of ordinary skill in the art will appreciate that the example of four rank memory module described above is not intended to be limiting and that other configuration can be used without departing from the inventive concepts herein disclosed.

While embodiments and applications of this invention have been shown and described, it would be apparent to those skilled in the art having the benefit of this disclosure that many more modifications than mentioned above are possible without departing from the inventive concepts herein. The invention, therefore, is not to be restricted except in the spirit of the appended claims.

What is claimed is:

1. A memory module connectable to a computer system, the memory module comprising:

a board;

a plurality of double-data-rate (DDR) memory devices mounted to the board, the plurality of DDR memory devices arranged in a first number of ranks;

a circuit that is coupled to said board and that receives from the computer system a set of input control signals that includes a set of first chip select signals and an address signal and that generates a set of second chip select signals based at least in part upon values of said set of first chip select signals and a portion of the address signal;

wherein a number of chip select signals of the set of second chip select signals corresponds to a first number of DDR memory devices arranged in the first number of ranks;

wherein a number of chip select signals of the set of first chip select signals corresponds to a second number of DDR memory devices arranged in a second number of ranks, the second number of DDR memory devices smaller than the first number of DDR memory devices and the second number of ranks less than the first number of ranks;

wherein at least one signal of the set of second chip select signals has a value to selectively activate a respective rank of the first number of ranks;

wherein the circuit provides one or more of the received set of input control signals to said at least one respective activated rank;

wherein the set of input control signals further includes RAS, CAS, WE, BA;

wherein the circuit includes an emulator and a register; and wherein the emulator receives from the computer system at least a portion of the set of input control signals that includes RAS, CAS, WE, the set of first chip select signals and the portion of the address signal;

wherein the emulator generates the set of second chip select signals in response to the at least a portion of the set of input control signals received by the emulator;

wherein the register receives at least another portion of the set of input control signals that includes RAS, CAS, WE, BA and the remaining portion of the address signal; and

wherein the register provides one or more of the input control signals received by the register to said at least one respective activated rank.

2. The memory module of claim **1**,

wherein a number of DDR devices per rank in the first number of ranks is the same as a number of DDR devices per rank in the second number of ranks.

3. The memory module of claim **1**,

wherein a number of DDR devices per rank in the first number of ranks and the number of DDR devices per rank in the second number of ranks is 9.

4. The memory module of claim **1**,

wherein the first number of ranks is twice the second number of ranks.

5. The memory module of claim **1**,

wherein the first number of ranks is four and the second number of ranks is two.

6. The memory module of claim **1**,

wherein the first set of chip select signals consists of two signals and the second set of chip select signals consist of four signals.

7. The memory module of claim **1**,

wherein the address signal includes multiple bits and the portion of the address signal includes a portion of the multiple bits.

8. The memory module of claim **1**,

wherein the first rank and the second rank have the same memory density.

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