

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.,
Petitioner,

v.

NETLIST, INC.,
Patent Owner.

Case No. IPR2023-00455
Patent No. 9,858,215

PATENT OWNER PRELIMINARY RESPONSE

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Statutes

35 U.S.C. §102	34, 35
35 U.S.C. §311(b)	34, 35, 36
35 U.S.C. § 325(d)	49, 50

EXHIBIT LIST

Exhibit No.	Document
EX2001	Crisp, R., “Direct Rambus Technology: The New Main Memory Standard,” <i>IEEE Micro</i> , pp. 18-28 (1997)
EX2002	Datasheet for Samsung’s RIMM MR16R1624 (Wolfe Deposition Exhibit 2100)
EX2003	Deposition Transcript of Dr. Andrew Wolfe from IPR2022-00615
EX2004	Samsung datasheet on Rambus Direct RDRAM (Dec. 2001)
EX2005	Deposition Transcript of SungJoo Park in <i>Netlist, Inc. v. Samsung Electronics Co., Ltd.</i> , 2:21-cv-00463-JRG (E.D. Tex. November 23, 2022) (excerpt)
EX2006	Ex. 7 to Park Depo
EX2007	<i>Frequently Asked Questions</i> , What is the difference between a "bank" and a "rank?", Micron, https://web.archive.org/web/20141231144416/https://www.micron.com/support/faqs (last accessed Mar. 7, 2023).
EX2008	Reserved
EX2009	“XDR Architecture “ by Rambus (last modified December 2005), downloaded from https://web.archive.org/web/20110724044154/http://www.rambus.com/assets/documents/products/dl_0161_v0_8.pdf
EX2010	IDT, “DDR4 LRDIMMs Unprecedented Memory Bandwidth on Samsung DDR4 LRDIMM Enabled by IDT’s Register and Data Buffer,” downloaded from https://www.renesas.com/us/en/document/whp/ddr4-lrdimms-both-memory-capacity-and-speed

EX2011	“HyperCloud HCDIMM: Scaling the High Density Memory Cliff,” July 14, 2012, downloaded from https://web.archive.org/web/20120915083048/http://www.netlist.com/media/blog/hypercloud-memory-scaling-the-high-density-memory-cliff/
EX2012	<i>What is a Memory Rank</i> , Crucial: Micron, https://www.crucial.com/support/articles-faq-memory/what-is-a-memory-rank (last accessed Mar. 7, 2023)
EX2013	<i>Lecture 15: DRAM Main Memory Systems</i> , University of Utah, https://my.eng.utah.edu/~cs6810/pres/11-6810-15.pdf
EX2114	“Configuring and using DDR3 memory with HP ProLiant Gen8 Servers: Best Practice Guidelines for ProLiant Servers with Intel Xeon Processors” by HP, downloaded from https://web.archive.org/web/20121023195754/http://h20000.www2.hp.com/bc/docs/support/SupportManual/c03293145/c03293145.pdf
EX2015	Ganesh, B. et al., <i>Fully-Buffered DIMM Memory Architectures: Understanding Mechanisms, Overheads and Scaling</i> , HPCA (2007)
EX2116	Datasheet for Micron DDR2 SDRAM FBDIMM MT36HTF51272FD
EX2017	U.S. Patent No. 7,356,639 (“Perego-639”)
EX2018	Redline Comparison of EX1035 (U.S. Patent No. 7,363,422 to Perego) With Related U.S. Patent No. 7,356,639
EX2019	US District Court – Judicial Caseload Profile (as of December 31, 2022)
EX2020	JESD79-2B
EX2021	Amended Docket Control Order in <i>Netlist, Inc. v. Samsung Electronics Co. Ltd.</i> , 2:22-cv-00293-JRG (E.D. Tex. Feb. 1, 2023)

EX2022	Cover pleading of Samsung's invalidity contentions in <i>Netlist, Inc. v. Samsung Electronics Co. Ltd.</i> , 2:22-cv-00293-JRG (E.D. Tex. April 13, 2023)
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I. INTRODUCTION¹

The Board should deny the petition because it fails to demonstrate a reasonable likelihood of success. For instance, Petitioner has not shown a reasonable likelihood that Perego, alone or in combination, involves a memory module having multiple ranks of memory devices as required by the claims. As another example, in Perego, subsets of memory devices involved in a transaction are determined by addresses. EX1071, 14:62-65, 15:37-45. The claims, however, require that the data bursts be in response to “control signals.” *See* Pet. xv. 1.f.1-1.f.2. Nor has Petitioner presented any evidence that the “first control signals” used to enable communication of a first data burst and the “second control signals” used to enable communication of a second data burst are different as required by element 1.f.2. There is no explanation, for example, why the “first” and “second” control signals, being allegedly associated with the first and memory devices coupled to different channels would necessarily or even obviously be different. Pet. 77. Nor is there any explanation why signals sent to enable or disable different multiplexing or demultiplexing circuits, transceivers or I/O latches would be different. Pet. 80. This is not about weight of evidence, but a complete failure in proof.

Addition of Ellsberry, Halbert or Matsui² does not cure the above

¹ All emphases are added unless otherwise noted.

deficiencies. Petitioner has also not provided any competent reasons why a POSITA would have combined Perego with those secondary references as proposed. For example, the Petition argues that a POSITA would look to Ellsberry for implementation details of rank multiplication; but even if the concept of “rank” were applicable in Perego, Perego provides details on how to select subsets of memory devices for a particular transaction already and there is no need to resort to rank multiplication. As another example, Petitioner apparently suggests that a POSITA would have looked to Halbert for elements 1.d.2-1.d.3 which require a first rank be selected to respond to a first memory command but not to a second memory command whereas a second rank be selected to respond to a second memory command and not to a first memory command. Pet. xiv. The two ranks of Halbert, however, respond to each read/write command concurrently, and therefore does not disclose or suggest elements 1.d.2-1.d.3. Finally, Matsui2 is cited specifically for the additional limitations in claim 7, and therefore does not cure any of the missing elements in independent claims.

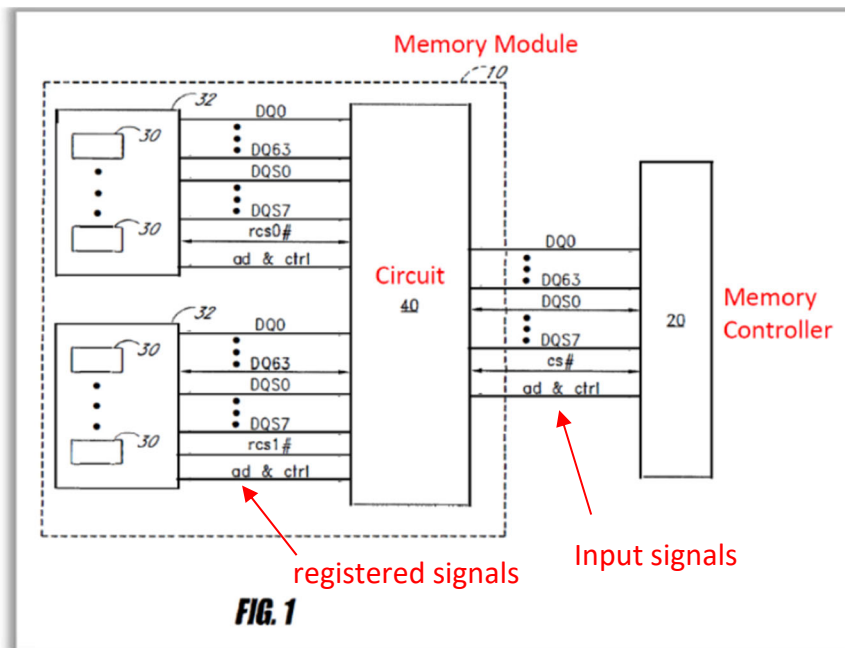
For these and reasons stated below, the Board should deny institution.

II. OVERVIEW OF THE '215 PATENT

The '215 patent, titled “Memory Module With Data Buffering,” relates to a buffered multi-rank memory module that effects selective data bursts between one rank of the memory device and the memory controller via the data buffer, in response

to control signals sent by a logic to the data buffer. EX1001, field (54), abstract. The data buffer control signals are outputted by a logic on the module, which is “configurable to receive a set of input address and control signals associated with [the] read or write memory command and output registered address and control signals [in addition to] data buffer control signals.” *Id.*

Figure 1, reproduced below with annotation, illustrates such a memory module. EX1001, 5:18-20.

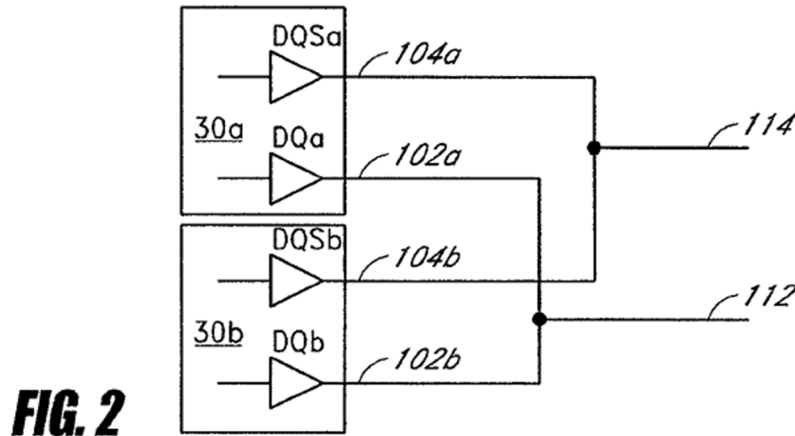


As shown in Figure 1, “[t]he memory module 10 is connectable to a memory controller 20 of a computer system (not shown).” *Id.*, 5:20-21. In the Figure 1 example, the memory module 10 includes multiple memory devices 30 arranged in two ranks 32, each rank having multiple memory devices 30. *See* Fig. 1, 6:30-33. Other number of ranks are possible. *Id.*, 6:33-36.

The memory module 10 also includes a circuit 40 electrically coupled to the memory devices 30 and to the memory controller 20 of the computer system. *Id.*, 5:24-27. The circuit 40 includes a logic that translates between a system memory domain of the computer system and a physical memory domain of the memory module 10. *Id.*, 5:29-32. This may be achieved by the logic receiving input data signals, chip-select signals and other control/address signals from the memory controller 20, and outputting corresponding registered data signals, registered chip-select signals and other registered control/address signals to the memory devices 30. *See* EX1001, Fig. 1, 19:52-20:21; *see also id.*, 16:62-18:40 (showing how the logic translates the input control/address and chip-select signals).

The memory module also includes an SPD device 240 that can report the CAS latency (CL) of the memory module to the memory controller 20. *Id.*, 20:24-26. The reported CL value of the memory module may be “one more cycle than does the actual operational CL of the memory array,” for example to account for the fact that in some embodiments, “data transfers between the memory controller 20 and the memory module are registered for one additional clock cycle by the circuit 40.” *Id.*, 20:26-29. The extra cycle time provides for time needed by a data buffer to perform address decoding, and/or data path multiplexing/demultiplexing, for example. *Id.*, 20:32-42.

Figure 2, reproduced below, illustrates a circuit diagram of two memory devices in two respective ranks of a memory module. EX1001, 6:62-65.



As shown in Figure 2, the memory devices 30a, 30b have DQ data signal lines 102a, 102b and DQS data strobe signal lines 104a, 104b. EX1001, 6:62-7:2. As further shown in Figure 2, the memory devices 30a, 30b have their DQ data signal lines 102a, 102b electrically coupled to a common DQ line 112 and their DQS data strobe signal lines 104a, 104b electrically coupled to a common DQS line 114. *Id.*, 7:5-9. The common DQ line 112 and the common DQS line 114 are electrically coupled to the memory controller 20 of the computer system. *Id.*, 7:10-12.

As described in the '215 patent, the circuit 40 selectively isolates the loads of at least some of the memory devices 30 from the computer system. EX1001, 7:14-16. In embodiments where the memory devices 30 are arranged in a plurality of

ranks, the circuit 40 selectively isolates the loads of one, some, or all of the ranks of the memory module 10 from the computer system. *Id.*, 7:16–29.

III. SKILL LEVEL OF A POSITA

For purposes of this preliminary response only, Patent Owner applies the skill level proposed by Petitioner.

IV. CLAIM CONSTRUCTION

Netlist disagrees with Petitioner’s proposed construction for “rank,” in particular, that a rank could include a single memory device. *Contra* Pet. 27-28. Netlist notes, however, the Petition is deficient also for reasons independent of this claim construction dispute.

To support its proposed construction for “rank,” Petitioner cites to a 2008 textbook by Jacob to argue that a rank could consist of “one or more DRAM devices” Pet. 29. The citation, however, comes from a 2008 document, three years after even Petitioner’s acknowledged priority date. To the extent the understanding in 2008 is relevant to the understanding of the term “rank,” Petitioner’s corporate witness (Mr. Park) testified, in no uncertain term that, in the context of DRAM memory modules, each rank would include more than one DRAM device:

Q: It says, quote, “a rank of memory is defined as the collection of SDRAMs,” plural, “driven by a given rank select signal.”

Do you see that?

A: Yes, I see that.

Q: Sir, this statement is incorrect; the accepted definition of rank in 2007 or 2008 in the concept of DRAM memory modules includes a single DRAM; correct?

A: *No, that's not right.*

EX2005, 87:1-17 (objections omitted); *see also id.* 86:18-23 & EX2006, p.146 (page 146 of Ex. 7 to Park deposition reflected a proposal by Samsung in 2007); EX2013 (college lecture notes defining “rank” as “a collection of **DRAM chips** that work together to respond to a request and keep the data bus full”).

Moreover, the Jacob textbook as a whole does not support Petitioner’s construction of a “rank.” Specifically, the passage relied on by Petitioner relates to the old concept “bank.” EX1070, p.413. Later in the same paragraph, the textbook notes that the term “rank” has replaced “bank” and that “the word *rank* is **now used** to denote a set of DRAM devices that operate in lockstep to respond to a given command.” *Id.* That is, the textbook associates “rank” with a “set of DRAM devices,” and consistently does so in the context of memory modules in other parts of the textbook. *Id.*; *see also* EX1070, 421 (“a DRAM memory module can be organized as multiple ranks of DRAM devices on the same memory module, **with each rank consisting of multiple DRAM device**”); *id.*, 318 (“Each rank is **a set of DRAM devices** that operate in unison”), 319 Fig. 7.5 (“Each rank is a set of ganged

DRAM devices”).

The patent’s specification also consistently and repeatedly references ranks composed of multiple memory devices. *See* EX1058, abstract (“memory devices [plural] in each of the plurality of N-bit wide ranks”), Figs. 1, 4A-4B, 5C-5D, 6:31-33 (each rank 32 has multiple memory devices 30), 12:44-50 (“a first rank 32a of memory devices 30” and “a second rank 32b of memory devices 30”).

Petitioner argues that the claim language of the ‘215 patent suggests otherwise. Pet. 28 (citing EX1001, 37:32-38). The context of that disclosure is provided on the next page.

1. A memory module operable in a computer system to communicate data with a memory controller of the computer system via a memory bus in response to memory commands received from the memory controller, the memory commands including a first memory command and a subsequent second memory command, the first memory command to cause the memory module to receive or output a first data burst and the second memory command to cause the memory module to receive or output a second data burst, the memory module comprising:

- a printed circuit board having a plurality of edge connections configured to be electrically coupled to a corresponding plurality of contacts of a module slot of the computer system;

- a register coupled to the printed circuit board and configured to receive and buffer first command and address signals representing the first memory command, and to receive and buffer second command and address signals representing the second memory command;

- a plurality of memory integrated circuits mounted on the printed circuit board and arranged in a plurality of ranks including a first rank and a second rank, the plurality of memory integrated circuits including at least one first memory integrated circuit in the first rank and at least one second memory integrated circuit in the second rank, wherein the first rank is selected to receive or output the first data burst in response to the first memory command and is not selected to communicate data with the memory controller in response to the second memory command, and wherein the second rank is selected to receive or output the second data burst in response to the second memory command and is not selected to communicate data with the memory controller in response to the first memory command;

- a buffer coupled between the at least one first memory integrated circuit and the memory bus, and between the at least one second memory integrated circuit and the memory bus; and

- logic coupled to the buffer and configured to respond to the first memory command by providing first control signals to the buffer to enable communication of the first data burst between the at least one first memory integrated circuit and the memory controller through the buffer, wherein the logic is further configured to respond to the second memory command by providing second control signals to the buffer to enable communication of the second data burst between the at least one second memory integrated circuit and the memory controller through the buffer, the second control signals being different from the first control signals.

In certain embodiments, the printed circuit board has a plurality of edge connections configured to be electrically coupled to a corresponding plurality of contacts of a module slot of the computer system. The register is configured to receive and buffer first command and address signals representing the first memory command, and to receive and buffer second command and address signals representing the second memory command. The plurality of memory integrated circuits are arranged in a plurality of ranks including a first rank and a second rank, and including at least one first memory integrated circuit in the first rank and at least one second memory integrated circuit in the second rank. The first rank is selected to receive or output the first data burst in response to the first memory command and is not selected to communicate data with the memory controller in response to the second memory command. The second rank is selected to receive or output the second data burst in response to the second memory command and is not selected to communicate data with the memory controller in response to the first memory command.

(EX1001 col. 37)

(EX1001, 3:25-43)

As is clear from the context, the disclosures for “at least one ... memory integrated circuit” in the ’215 patent do not define the term “rank.” Rather, the disclosures provide context that a claimed “buffer” can be, but need not be, coupled

to multiple memory devices in the rank. That is, the buffer can be coupled to just “one” memory IC in the rank. *See* EX1001, 37:35-38, 37:46-50 (“a buffer coupled between the at least one first memory integrated circuit and the memory bus, and between the at least one second memory integrated circuit and the memory bus”) (highlighted yellow). The ’215 claim also specifies that the buffer, in response to a memory command, “enable[s] communication of the first[/second] data burst between the at least one first[/second] memory integrated circuit” and the memory controller. *Id.*, 37:54-56, 37:59-61 (highlighted in green). The ’215 specification is in accord, with the disclosures (green) immediately following the discussion of at least a first memory IC in a first (second) rank (yellow) referencing the first and second data burst (green). *Id.*, 3:25-53. The disclosures just provide the context for later-recited first/second memory ICs and their structures and functions.

Petitioner also argues that the ’215 patent describes a single-device “rank” embodiment. Pet. 29-30. The cited passage states “[i]n certain embodiments, the command signal is passed through to the selected rank only (e.g., state 4 of **Table 1**). In such embodiments, the command signal (e.g., read) is sent to only one memory device or the other memory device so that data is supplied from one memory device at a time.” EX1001, 16:66-17:8. The referenced Table 1 is a logic table “for the selection among **ranks of memory devices** [] using chip-select signals,”

indicating that the description that follows pertains to ranks of multiple memory devices. *Id.*, 16:22-42.

Table 1 provides a logic table compatible with certain embodiments described herein for the selection among ranks of memory devices 30 using chip-select signals.

TABLE 1

State	CS ₀	CS ₁	A _{n+1}	Command	CS _{0A}	CS _{0B}	CS _{1A}	CS _{1B}
1	0	1	0	Active	0	1	1	1
2	0	1	1	Active	1	0	1	1
3	0	1	x	Active	0	0	1	1
4	1	0	0	Active	1	1	0	1
5	1	0	1	Active	1	1	1	0
6	1	0	x	Active	1	1	0	0
7	1	1	x	x	1	1	1	1

Note:

1. CS₀, CS₁, CS_{0A}, CS_{0B}, CS_{1A}, and CS_{1B} are active low signals.

2. A_{n+1} is an active high signal.

3. 'x' is a Don't Care condition.

4. Command involves a number of command signals that define operations such as refresh, precharge, and other operations.

In state 4 above, the rank corresponding to CS_{1A} is chosen; and within that selected rank, “the command signal (e.g., read) is sent to only one memory device or the other memory device so that data is supplied from one memory device at a time.” EX1001, 16:51-53, 17:1-4. Read in context, the embodiments described with reference to Table 1 refer to transmitting a command signal to one of the multiple memory devices in the selected rank (i.e., the subject matter of claim 16 of U.S. 7,619,912). Again, these may be one of two devices corresponding to one another in different ranks but connected to the same buffer device. Thus, the passage does not support Petitioner’s proposal that a rank on a memory module may include a single DDR device.

V. ASSERTED PRIOR ART

A. Perego

Perego discloses a memory system with point-to-point topology including a “memory module having a buffer device (e.g., having a configurable width) isolating data, control, and address signals of the memory devices from the connector interface.” EX1071, 4:38-45; Abstract; 5:35-55; 8:10-17, 8:20-26. Buffer device 350 is coupled to memory controller interface 375, which includes a “plurality of memory subsystem ports 378a-378n.” *Id.*, 4:63-5:15. Perego’s configurable width buffer device is connected to ports 378a-378n of the memory controller via a point-to-point links 320. *Id.*, 5:12-21. Perego repeatedly and consistently emphasizes the benefits of its point-to-point architecture over a conventional JEDEC-style bus. *See, e.g.*, 3:47-56, 4:65-5:1, 5:6-15, 5:32-55, 6:15-19, 13:49-59, 21:46-50, Figs. 3A/3B, Fig. 5A.

Perego’s buffer communicates to the plurality of memory devices on the buffered module via channels 370. *Id.*, 5:4-6, 6:13-24, 7:65-67; Fig. 3B. But in contrast to a conventional registered DIMM (“RDIMM”), in Perego’s architecture, control/address information is transmitted to the module via packets and multiplexed with data when transmitted across the configurable width interface 590 or the point-to-point link interface 510. *E.g., id.*, 13:49-59 (configurable width interface 590 may “extract the address and control information from the data”). In the example of a

“normal memory read operation,” Perego explains that “device 350 receives control, and address *information* from controller 310 via point-to-point link 320*a*, and *in response, transmits corresponding signals to one or more, or all of memory devices 360* via channels 370,” *id.*, 6:12-19, but the same paragraph contrasts this approach with that of the conventional RDIMM buffer. *See id.*, 6:27-30 (“By way of comparison, buffers disposed on the conventional DIMM module in U.S. Pat. No. 5,513,135 are employed to buffer or register control signals such as RAS, and CAS, etc., and address signals.”).²

Perego discloses that regardless of the module width, “[a]module's full set of data stored on the associated memory devices is available[.]” EX1071, 7:54-56. “With wider interface widths, different subsets of memory devices and memory cells may be accessed through different sets of interface connections. With narrower data or interface widths, the different subsets of memory devices and memory cells are accessed through a common set of interface connections.” *Id.*, 7:56-62. Address bits are used to specify the memory devices to be accessed at narrower interface width. *Id.*, 7:62-64.

² Petitioner argues that the ‘135 patent (EX1081) is an example of a JEDEC-compliant RDIMM that Perego allegedly would make upgradeable with its invention. Pet. 33-34.

Perego also teaches that power is saved by powering only selected memory devices. *Id.*, 20:51-57. Accordingly, for example, in Figure 4B, “two channels 415*c* and 415*d* may transfer information simultaneously and the memory devices on the other two channels 415*a* and 415*b* remain in a ready or standby state until called upon to perform memory access operations.” *Id.*, 21:16-20. Because devices not in use are not powered or activated (20:51-57), no translated commands need to be (or can be) sent to those dormant devices such that they “remain in a ready or standby state until called upon to perform memory access operations” (21:16-20).

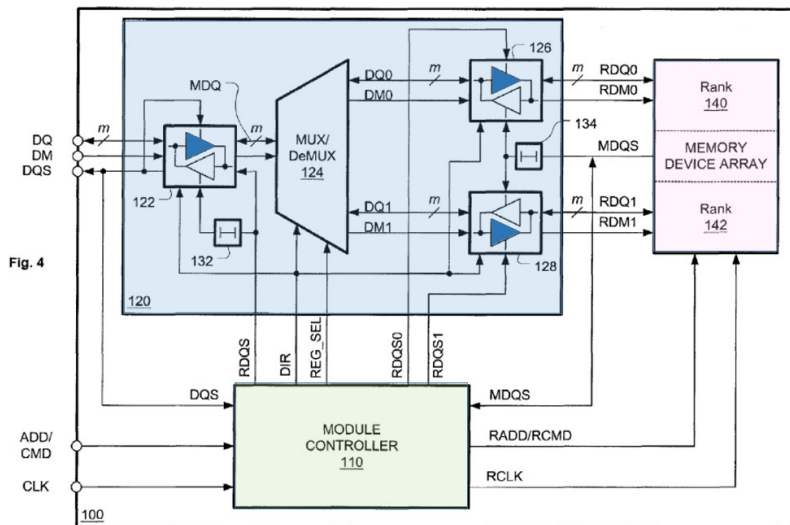
B. Ellsberry

Ellsberry discloses a memory module architecture, as depicted in Figure 2, that “permits transparent bank switching of memory devices.” EX1073, [0001]. As depicted in Figure 2, Control ASIC 204 (red) “receives memory addresses and commands over the DIMM interface 202” from the system memory controller, and switch ASICs 206 and 208 (purple) “receive data information from the DIMM interface 202 via data buses 230 & 232, respectively.” *Id.*, [0028]-[0029]. Each switch ASIC is connected to a number of memory banks (e.g., Bank 0-3 below). *Id.* Switch ASICs 206 and 208 receive respectively data byte group N and data byte group 0, provided “simultaneously” by the DIMM interface 202. *Id.*, [0030], Fig. 2 (depicting at least two data groups); Fig. 5 (depicting nine data groups).

Control ASIC 204 sends command signals to memory devices in different memory banks via bus 220. *Id.*, [0030]. Each ASIC switch includes two data ports, Port A and Port B, coupled respectively to data busses 234 and 236. Ellsberry discloses that in column addressing scheme, memory devices coupled to both ports A and B are read but only the data from the target memory device is multiplexed onto the DIMM interface. EX1073, [0033]. In contrast, in row addressing mode, read command is sent to the targeted memory devices and NOP is sent to the non-targeted memory devices. *Id.* In either case, however, to the extent JEDEC-compliant chip select signals are sent to the memory devices, the chip select signals will assume an active signal value (“L”). *See, e.g.*, EX1064, p.49 (“L” for CS for read/write and NOP).

C. Halbert

Halbert describes “a group of buffered memory module architectures.” EX1078, 3:42-43. Halbert’s Figure 4 configuration relied on by Petitioner includes “a module controller 110 [green]; a data interface circuit 120 [blue]; and a memory device array 140/142 [mauve].” *Id.*, 4:36-39.



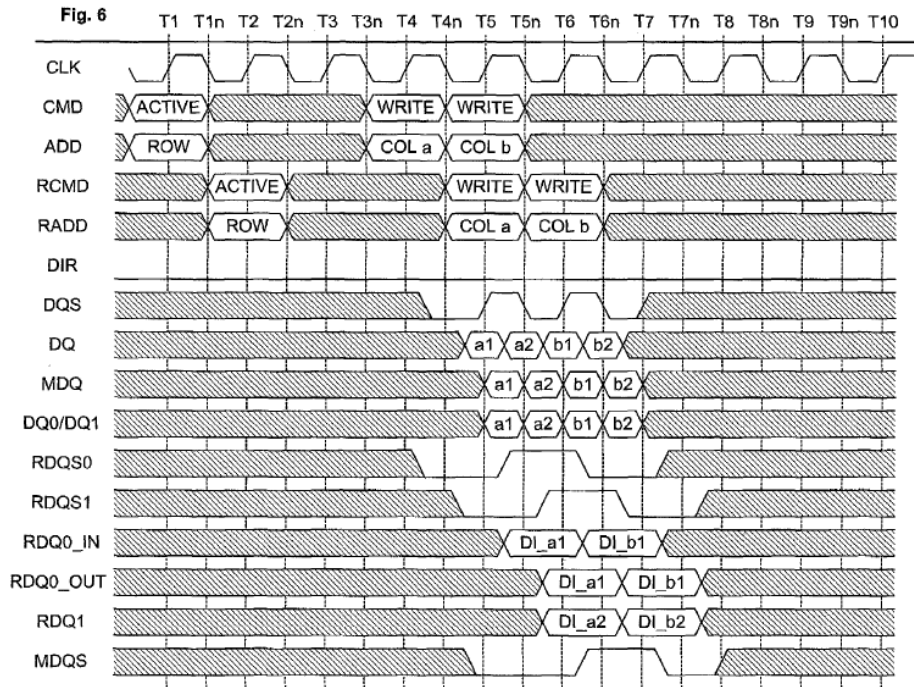
In the above configuration, “[d]ata interface circuit 120 provides for m-bit-wide data transfers between the module and the system memory data bus, and for R×m-bit-wide data transfers between the interface circuit and the memory device array.” *Id.*, 4:49-52. In Figure 4, R equals 2 for the two ranks 140 and 142. *Id.*, 4:52-55. In Halbert, “*multiple ranks ...will perform memory operations with the interface circuit concurrently.*” *Id.*, 4:57-59.

Halbert's data interface circuit 120 in Figure 4 has one bi-directional buffer 122 that can receive (for write operations) or drive (for read operations) m-bit-wide data signals DQ on the system memory data bus. *Id.*, 4:60-64. Data buffer 122 can also drive a data strobe signal DQS onto the memory data bus for read operations. *Id.*, 5:4-5.

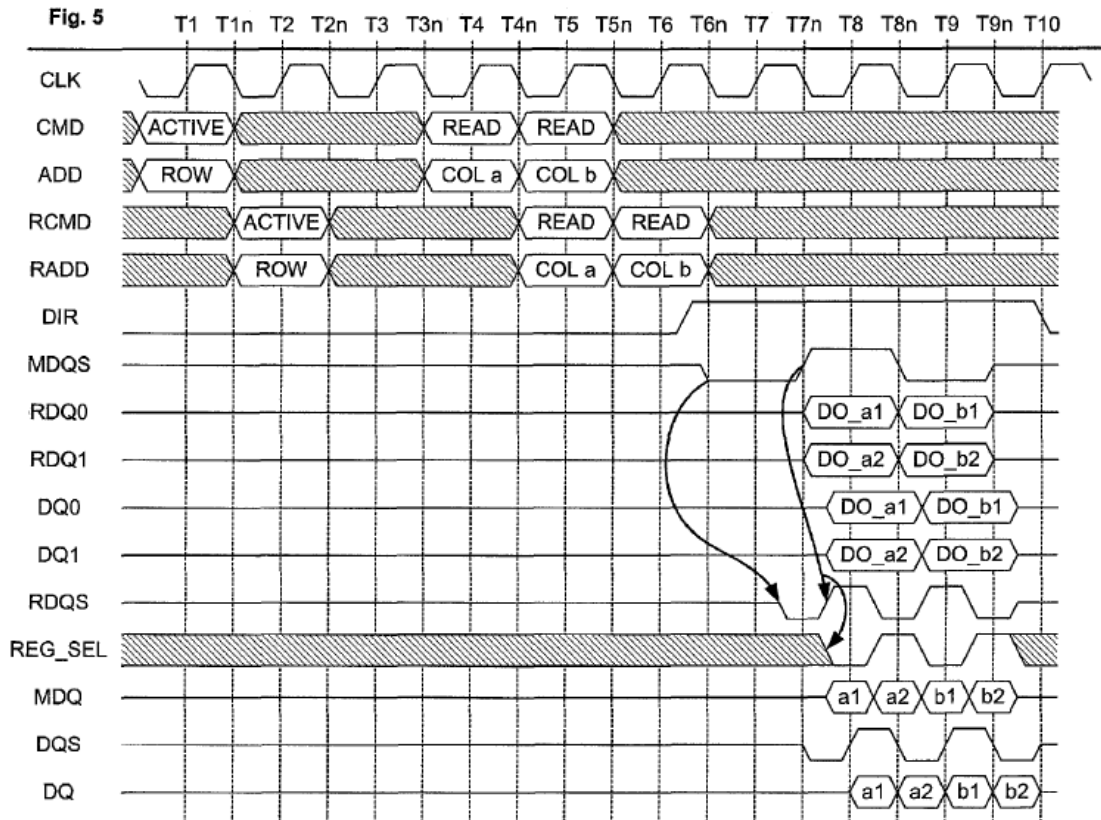
Halbert's data interface circuit 120 further includes two bi-directional data registers 126 and 128 that each receive from (for read) or drive to (for write) a

corresponding memory rank (140 and 142 respectively) m-bit-wide words (*e.g.*, RDQ0 or RDQ1), “over a dedicated point-to-point module data bus.” *Id.*, 5:6-11. Registers 126 and 128 can also drive registered data-mask signals (*e.g.*, RDM0 or RDM1) to the corresponding memory rank. *Id.*, 5:11-14.

Between the buffer 122 and registers 126 and 128 is a MUX/DeMux 124, which multiplexes data signals DQ0 or DQ1 received from registers 126 and 128 in read operations, and de-multiplexes data signals MDQ from buffer 122 into DQ0 or DQ1 for delivery to registers 126 and 128 respectively in write operations. *Id.*, 5:15-22. In a write operation, transitions of registered strobing signals RDQS0 and RDQS1 cause registers 126 and 128 to latch m-bits of DQ0 and DQ1 respectively in consecutive clock cycles. *Id.*, 5:54-61. “Both register contents are then written to memory device array 140/142 **during a single device write cycle**” in response to MDQS signaled to memory device array. *Id.*, 5:61-65. Consistent with the above description, Halbert presents a “timing diagram for two consecutive write operations” in Figure 6. As seen from Figure 6, write data associated with each WRITE command is broken into two subsets, *e.g.*, a1 and a2, and b1 and b2. The first subset (*e.g.*, a1 and b1) is latched into register 126 and written to rank 140 while the second subset (*e.g.*, a2 and b2) is latched into register 128 and written to rank 142.



Similarly in a read operation, 2m bits of data are read into the data registers per read cycle, and are then driven m-bits at a time through MUX 124. *Id.*, 5:40-48. Then, in response to register data strobe RDQS, “buffer 122 latches data from MUX 124 and drives that data onto the memory data bus.” *Id.*, 5:48-50. A timing diagram for a read operation is shown in Figure 5. *Id.*, 5:66-6:65 (detailed description of the various signals and their timing). Like the write operation, datasets for each READ operation is also broken into two subsets and read concurrently from ranks 140 and 142.



VI. PETITIONER HAS NOT SHOWN A REASONABLE LIKELIHOOD OF SUCCESS TO PREVAIL UNDER GROUND 1

A. Perego does not disclose or suggest a memory module having “ranks”

“The term rank was created by JEDEC ... to distinguish between the number of memory banks *on a module* as opposed to the number of memory banks on a component, or memory chip.” EX2012 at 1; EX1069 at 2 (“The last bus, the chip-select bus, is essential in a JEDEC-style memory system, as it enables the intended recipient of a memory request” by having “a separate wire for every rank of DRAM in the system” so that “[t]he chip-select signal ... passes over a wire unique to each

small set of DRAMs and enables or disables the DRAMs in that rank”). Rank therefore is a concept specific to JEDEC-style *memory modules*. *Id.*

Perego never mentions the word “rank,” as Dr. Wolfe acknowledges. EX2003, 204:16-21. Dr. Wolfe asserts, however, that Perego discloses the concept of a rank. *Id.* It does not, because Perego operates on an individual device basis. *See* EX1071, 9:64-10:4 (using individual device select lines for devices in a common channel). Moreover, in Perego, the number of devices involved in a given transaction is not fixed as in the concept of “rank,” but is dynamically configurable based on operating conditions. *E.g.*, EX1071, 10:22-26, 10:31-33, 14:60-65, 15:31-45, 21:16-28, 21:29-38 (“memory system 700 may concentrate bandwidth as it is required while in operation. For example, memory system 700 may employ only one of channels 415*a*-415*d* and match throughput to the corresponding point-to-point link. As bandwidth requirements increase, memory system 700 may dynamically activate more of channels 415*a*-415*d* and increase the throughput on the point-to-point link along with the number of channels accordingly to meet the bandwidth requirements for a given operation.”). A POSITA would also not have a motivation to modify Perego’s architecture to be compatible with JEDEC’s RDIMM as Petitioner asserts (see Pet. 33-35) because doing so would eliminate Perego’s purported invention of a “configurable width buffered module” that utilizes a point-to-point configuration whose width can be configured dynamically.

1. Perego does not disclose “ranks” of memory devices

Petitioner relies on Perego’s disclosures 15:37-45 for allegedly suggesting the concept “rank.” Pet. 67. But Petitioner’s own expert, Dr. Wolfe, disagrees that the passage “specifies how ranks are selected or enabled.” EX2003, 202:8-204:10 (discussing 15:37-40 and then 15:40-45, “Q: So you don’t think this paragraph has anything to do with grouping devices into different ranks? A: I do not think that this paragraph specifies how ranks are selected or enabled.”). Dr. Wolfe further explains that “independent banks” referenced in that paragraph refers to “the number of page registers which can be activated corresponding to different addresses” and not to “ranks” as Petitioner alleges. EX2003, 203:15-204:3. Given Dr. Wolfe’s admission, Perego, 15:37-45, indisputably does not suggest or render obvious the claim limitation “ranks,” contrary to Petitioner’s assertion. *Contra* Pet. 56.

Petitioner then suggests that devices connected to each of interfaces 520a and 520b, a single channel, and/or two channels, can be a rank. Pet. 57-62. As a preliminary matter, Petitioner has not provided any competent evidence that the devices connected to a single channel or interface “act together” in response to a single read/write command as it defines. For instance, in Figure 5F, although both memory devices 652 and 653 are connected to channel DQ1, “[b]oth memory cells 652a and 653b are not accessed via channel DQ1 during a single access operation in an embodiment of the present invention.” EX1071, 20:30-33. Likewise in Figure

5E, there is no evidence that devices 652 and 653 are accessed in a single operation. *See id.*, 20:11-16.

Moreover, unlike the traditional JEDEC-compliant DIMMs, Perego's memory modules are "configurable width buffered module[s]." EX1071, title; EX2003, 43:12-20 (a JEDEC compliant memory module does not ordinarily have a configurable buffer width). That means Perego's modules do not have a fixed width. Yet, under Petitioner's own definition for "rank," a rank refers to a set of DRAM devices "on a memory module that act together in response to command signals, including chip-select signals, to read or write the full bit-width of the memory module." Pet. 27-28. With a memory module having a configurable width and purportedly JEDEC-compliant SDRAMs (in order to satisfy other limitations, see Pet. 33-35) having fixed widths, the number of devices in a purported "rank" would necessarily change as the "full bit-width of the memory module" changes. For instance, Perego observes:

The number of signal lines of channels 370 may be increased or decreased as the memory device access width changes. Channels 370 (FIG. 3C) may be subdivided into several addressable subsets. ***The address of the transaction will determine which target subset of channels 370 will be utilized for the data transfer portion of the transaction.*** In addition, ***the number of transceiver circuits included in interface 520a and 520b that are employed to communicate with***

one or more memory devices may be configured based on the desired serialization ratio. Typically, configuration of the transceivers may be effectuated by enabling or disabling how many transceivers are active in a given transfer between one or more memory devices and configurable width buffer device 391.

EX1071, 14:62-15:6. As another example, Perego discloses

memory system 700 may concentrate bandwidth as it is required while in operation. For example, memory system 700 may employ only one of channels 415a-415d and match throughput to the corresponding point-to-point link. As bandwidth requirements increase, memory system 700 may dynamically activate more of channels 415a-415d and increase the throughput on the point-to-point link along with the number of channels accordingly to meet the bandwidth requirements for a given operation.

EX1071, 21:29-38; *see also id.*, 17:1-8 (width of configurable width buffer device can be changed even after it has been used for a particular width, all in general without need to power-down or reset configurable width buffer device), 10:22-33 (in quad-channel module 450, channels 415c and 415d may operate in parallel with channels 415a and 415b, or all four may operate simultaneously); Pet. 59 (Petitioner apparently equates W_{DP} to memory module bit width).

Nothing in the '215 patent or any JEDEC documents suggests, however, a rank of memory devices refers to a group of memory devices that is dynamically

reconstituted to account for the changing memory bit width. *See, e.g.*, EX1001, Figs. 1, 4A-4B, 5C-5D, 8A-8D, 9A-9B, 10A-10B, 11A-11B and associated text. Moreover, while Perego recognizes addressable subsets of a channel for a given transaction based on addresses, (*see* EX1071, 14:62-15:6), Samsung's definition for a rank requires the use of chip-select signals. *See* Pet. 27-28; EX2006 [Park Ex. 7], p. 146 (Samsung previously defining a rank of memory as "the collection of SDRAMs driven by a given rank select signal"). Perego, however, never mentions "chip-select" signals, lines or the alike. *See* EX1071 *generally*. Hence, Petitioner has not provided any competent evidence that the interfaces or channels it points to are ranks as it defines.

2. Perego's Rambus-style memory module organization is incongruent with JEDEC's rank concept

Petitioner also argues that it would have been obvious to arrange Perego's memory devices into ranks in light of the JEDEC specification. Pet. 62. But Petitioner's own evidence distinguishes JEDEC-style memory organization and Rambus-style memory organization as two distinct approaches. EX1069, pp. 11-16. This is not an issue of weighing competing evidence presented by Petitioner and Patent Owner. This is an issue of the Petitioner ignoring the express teachings of its own evidence.

As EX1069 observed, a distinguishing feature of Rambus memory organization, compared to JEDEC, is its lack of chip-select network. EX1069, p.11 (in Rambus memory systems, “there is no separate chip select network”); p.12 (“In the Rambus memory organization, there is no chip select network”). In contrast, in JEDEC, “there is a chip-select network that uses one unique wire per DRAM rank” *Id.*, p. 9. Hence, Perego, an example of a Rambus memory organization, does not disclose or suggest a rank of memory devices, a concept unique to JEDEC-style memory systems and intricately intertwined with the notion of “chip-select” signals. *See* Pet. 27-28 (under Petitioner’s definition, the set of DRAMs in a rank would “act together in response to command signals, including chip-select signals, to read or write the full bit-width of the memory module”).

Even in later Rambus iterations that added separate control and address busses, no chip-select bus was introduced. EX1069, p.9; EX2001 (no chip-select signals mentioned for Rambus Direct); EX2009 (no chip-select mentioned in Rambus’ XDR architecture). Instead, Rambus memory systems, including Perego, use “device identification” to select devices that “share the same channel.” EX1071, 9:67-10:4; *see also* EX1069, p.12 (devices in Rambus’s system would know whether a packet is intended for it via unique identification number contained in the packet); EX2009, p. 16 (noting “the memory controller is mainly concerned with addressing a rank of devices instead of a single device,” and hence to accommodate XDR’s

dynamic point-to-point link with configurable width DRAMs, “the memory controller will need to vary the number of Sub-Row (SR) and/or Sub-Column (SC) address bits within the Request Packet as device width and device count are varied”). In other words, *Perego’s devices operate on an individual basis*, and do not “act together” as required by the concept of “rank.” Pet. 26; EX2001, 21 (“a single direct RDRAM spans the entire width of the channel”), 23 (“Because a Direct RDRAM spans the entire channel, the CPU accesses each RDRAM independently. So each RDRAM directly adds to the number of memory banks accessible to the memory controller.”); EX2009, p. 16 (noting the design changes needed on the memory controller side in order to address “a single device” instead of “a rank of devices”).

The operation on an individual device basis is why Perego can afford the flexibility of dynamically having different memory devices and/or channels operate independently, in parallel or simultaneously, depending on the application or the processing need. *E.g.*, EX1071, 10:22-26, 10:31-33, 14:62-65 (“Channels 370 ... may be subdivided into several addressable subsets. The address of the transaction will determine which target subset of channels 370 will be utilized for the data transfer portion of the transaction.”), 14:65-15:6 (“the number of transceiver circuits included in interface 520a and 520b that are employed to communicate with one or more memory devices may be configured based on the desired serialization ratio”), 21:16-24 (dynamic grouping or device utilization for different applications and

during different processing windows), 21:28-38 (a memory module may start out with one channel and then “[a]s bandwidth requirements increase, memory system 700 may dynamically activate more of channels 415a-415d and increase the throughput on the point-to-point link along with the number of channels ...”).

In this manner, Perego’s memory module data output width can also be adjusted dynamically. *E.g.*, EX1071, 5:32-44 (when a second memory module is removed from a memory system, the bandwidth of the first memory module doubles to retain the same overall system bandwidth: “when the second memory module is removed from the system ... the plurality of point-to-point connections are routed to the first memory module to retain system bandwidth between memory modules and the controller or increase the bandwidth to the first memory module”).

Modifying Perego to fit into the JEDEC framework that has fixed ranks and fixed bandwidth would require changing the fundamental operating principle of Perego, which is evidence of non-obviousness. *Univ. of Md. Biotechnology Inst. v. Presens Precision Sensing GmbH*, 711 F. App’x. 1007, 1011 (Fed. Cir. 2017) (quoting *In re Ratti*, 270 F.2d 810, 813 (CCPA 1959) (*en banc*) (not obvious where “the ‘suggested combination of references would require a substantial reconstruction and redesign of the elements shown’ in [one of them], or a ‘change in its basic principles’” under which it was designed to operate).

This is notwithstanding the fact that a POSITA might allegedly know how to implement ranks in Matsui1, which utilized a conventional multi-drop connection with parallel control/address busses with a fixed memory module data width (that is a JEDEC-style memory module). *See* EX1072, Fig. 1. Perego does not have the same configuration, and what is applicable to one form of memory module says nothing about whether a POSITA would have viewed the same applicable in a completely different design. *Cf., Innogenetics N.V. v. Abbott Laboratories*, 512 F.3d 1363, 1373 (Fed. Cir. 2008) (“knowledge of a problem and motivation to solve it are entirely different from motivation to combine particular references to reach the particular claimed method”).

Indeed, if the design goal is to obtain JEDEC compliant RDIMM with JEDEC compliant SDRAMs (*see, e.g.,* Pet. 32-34), such modules would have been readily available. *E.g.,* EX1062; EX1066. Petitioner has not provided any evidence that a POSITA would have been motivated to undertake the substantial effort to redesign Perego in order to obtain something that was already available.

3. Petitioner has not shown that Figure 4B would disclose all limitations under its own theory(ies)

Petitioner also suggests that Netlist previously conceded Perego Figure 4B disclosed two ranks. Pet. 61. What Netlist said was, given Petitioner’s requirement that a rank refers to a set of memory devices that would act together and because

Perego describes channels 415c and d (or 415a and b) would operate together, then—even under Petitioner’s suggested modification in IPR2022-00615 where each channel includes but one device—there would be two devices in a rank. EX1019, p.43; EX1020, ¶¶93-94. At any rate, neither channels 415c-d nor channels 415a-b would meet Petitioner’s own definition of a rank.

For instance, according to Petitioner, the data width accessed in a memory transaction (W_A) corresponds to the bit-width of each rank of memory device “when only ‘one’ of the ‘one or more channels 370’ ... is used for a read or write operation.” Pet. 59. Accordingly, where channels c/d (or a/b) collectively form a rank—that is, more than one channel is used for a read/write operation, the data width accessed in a memory transaction would differ from the bit-width of a rank of memory device under Petitioner’s own reasoning. Yet, under Petitioner’s definition, a rank is “an independent set of ... memory devices on a memory module that act together ... to *read or write full bit-width of the memory module.*” Pet. 27-28. Petitioner does not explain why channels 415c/d together read or write *full bit-width of the memory module* under its own theory, given that if each channel width equals the width of the full module, two channels would have a data width twice that of the memory module.

Second, although much of the Petition’s theory relies on the module width to be 64 bits, the data width in Perego’s Figure 4B is 16 bits. *See* Pet. 39 (“A POSITA

would have understood that a data width of $W_{DP}=64$ corresponds to the 64-bit data width of a JEDEC-compliant registered DIMM module.”); 57-59 (each rank 64 bit wide). Petitioner does not give any reason for further modifying Perego’s Figure 4B to a 64-bit wide data path, other than to argue that the 64-bit width is that of a JEDEC-compliant RDIMM so that it could argue that a POSITA would modify Perego to be JEDEC compliant. But that reasoning is circular and is clearly using the claims as a roadmap for assembling the elements. That is textbook hindsight.

B. Perego uses addresses, and not “control signals,” to enable communication of data bursts between memory ICs and the memory controller

Element 1.f.1 requires “logic coupled to the buffer and configured to respond to the first memory command by providing first control signals to the buffer to enable communication of the first data burst between the at least one first memory integrated circuit and the memory controller through the buffer,” and element 1.f.2 recites “wherein the logic is further configured to respond to the second memory command by providing second control signals to the buffer to enable communication of the second data burst between the at least one second memory integrated circuit and the memory controller through the buffer.” Pet. xv., 1.f.1-1.f.2.

The Petition does not specifically identify what the alleged first and second control signals are. Pet. 76-80. Instead, it merely alleges that “a POSITA would have understood that the buffer device’s logic sends ‘control signals’ to interfaces

520a/b to activate only the channel transferring the data burst between the memory controller and the targeted rank.” Pet. 79. Perego discloses, however, “the target subset of secondary channel signal lines may be selected via address bits provided as part of the primary channel request.” EX1071, 15:37-40; *see also*, 16:62-65 (“Channel 370 ... may be subdivided into several addressable subsets. The address of the transaction will determine which target subset of channels 370 will be utilized for the data transfer portion of the transaction.”). But there is no showing that address information is the same as control signals.

Petitioner also argues that control signals are sent “to the transceivers [in interfaces 5201/b, 10 and 590], multiplexing/demultiplexing circuits, and to the input and output latches to selectively activate those circuit elements of the buffer according to the targeted rank and direction of the read and write operation.” Pet. 80. But again, Petitioner relies on the address information, instead of “control signals.” *Id.*, (citing EX1071, 14:62-15:6 which reference “[t]he address of the transaction”); *see also* 15:34-40 (address used to determine target subset of signal lines). Indeed, Petitioner concedes that “the targeted rank can be determined by the logic using the address information, in addition to the input chip-select signals” Pet. 80. But Perego does not mention chip-select signals at all (*see* EX1071 *generally*), and Petitioner does not explain why address information is a control signal (*cf.*, ‘417 patent, claim 1 (reciting “address and control signal lines”);

EX1069, p.2 (noting that in a JEDEC-compliant system, there are separate control bus and address bus)).

There is also no showing whatsoever that the address information, or the purported chip-select signal, is ever “provid[ed] ... to the buffer.” Pet. 76-80.

In summary, Petitioner has not made any showing that the logic provides “control signals” to the buffer to enable communication of data between memory ICs and the memory controller, as required by 1f.1-1.f.2.

C. Petition has not made a *prima facie* case that the first and second control signals are different

Petitioner has also made no showing that the first and second controls signals are different. Pet. 80. For example, if transceivers and multiplexer and demultiplexer are controlled by, *e.g.*, an “enable” signal, to activate a communication, then the first and second control signals would be the same even though they are sent to different components/circuits in the buffer. For example, Petitioner cites EX1071, 17:4-44 which states “[t]he multiplexing logic is used during read operations, and the demultiplexing logic is used during write operations.” But the disclosure does not say what the control signals are or how they differ when used with multiplexing and demultiplexing logics. Similarly, the disclosure in 17:61-62 and Figures 5A-5B is silent on the type of control signals used.

Petitioner also asserts the first and second control signals are different allegedly “because the ‘first’ rank is selected to receive or output a ‘first’ data burst, and the ‘second’ rank is selected to receive or output the ‘second’ data burst, where the ‘first’ and ‘second’ ranks are coupled to different channels of Perego’s buffer device[.]” Pet. 77. But there is no explanation why the control signals need to or should be different if the first and second ranks are coupled to different channels of Perego’s buffer device. Nor is that answer provided by the assertion that “each rank of memory devices would receive a separate chip-select signal that selects the memory devices in that rank[.]” Pet. 72, Pet. 77 (referring back to elements 1.d.2-1.d.3). The claimed “control signals” are those provided to the data buffer, and not signals such as chip-select signals provided to the memory devices. As such, Petitioner has made no showing that the first and second control signals are different.

VII. PETITIONER FAILS TO ESTABLISH A REASONABLE LIKELIHOD OF SUCCESS ON GROUND 2

Petitioner also argues that Perego in view of Ellsberry renders challenged claims obvious. A POSITA would not have modified Perego in view of Ellsberry because Elleberry is not a proper IPR reference and because Perego and Ellsberry have different architectures.

A. Ellsberry is not a “printed publication” under §311(b)

Petitioner asserts that the ‘215 patent is not entitled to a priority date before July 1, 2005. Even if true, Ellsberry is a *patent application* published after that date. EX1073, cover (published in December 2006). Consequently, Ellsberry does not qualify as a patent or a printed publication required under §311(b).

In particular, under the AIA, an IPR petition may be only "on the basis of prior art consisting of patents or printed publications." 35 U.S.C. §311(b). Ellsberry is not a patent; so the question is whether it qualifies as “printed publications.” It does not.

Pre-AIA patent law only refers to certain art as “printed publication.” In particular, pre-AIA 35 U.S.C. §102 provides that the prior art includes inventions that "w[ere]...described in a *printed publication*...before" the invention, §102(a), or "in a *printed publication*...more than one year prior to the date of [one's] application for patent," §102(b). The critical date for a "printed publication" is the date it is "*published, i.e., accessible to the public.*" *Samsung Elecs. Co. v. Infobridge Pte. Ltd.*, 929 F.3d 1363, 1368, 1370 (Fed. Cir. 2019) (emphasis added).

There can be no dispute that Ellsberry became a printed publication on its publication date of December 2006, after even Petitioner’s alleged invention date of July 1, 2005. EX1073, cover.

While Ellsberry is prior art under §102(e), that does not make it into a “printed publication” before the invention date: §102(e) does not even mention “printed publication” or describe a qualifying application as a printed publication before its date of publication. Netlist is also not aware of any Federal Circuit cases that specifically characterize a patent application as a printed publication before its publication date. And Petitioner—who bears the burden of establishing that its Petition satisfies the requirements in §311(b)—has not cited any authority to the contrary. It simply assumes that a §102(e) patent application qualifies as a printed publication as of its effective filing date. Pet. 20. Yet, the Federal Circuit has made clear that prior art becomes a “printed publication” only when it became published. *In re Klopfenstein*, 380 F.3d 1345, 1348 n.2 (Fed. Cir. 2004) (quoting *In re Cronyn*, 890 F.2d 1158, 1160 (Fed. Cir. 1989) (“The statutory phrase ‘printed publication’ has been interpreted to mean that before the [relevant] date the reference must have been sufficiently accessible to the public interested in the art; dissemination and public accessibility are the keys to the legal *determination whether a prior art reference was “published.”*)).

Consequently, because documents are “printed publication” prior art only as of the date they became published and available to the public (*id.*) and because Ellsberry is a patent application published after the invention date, it does not qualify

as either “patents” or “printed publications” required by §311(b). Thus, Ground 2 fails.

B. Petitioner has presented no competent evidence that a POSITA would have combined Perego and Ellsberry

Petitioner first argues that a POSITA would have combined the two references because they are allegedly analogous art. But that reason is insufficient as a matter of law. *Microsoft Corporation v. Enfish, LLC*, 662 F. App’x 981 (Fed. Cir. 2016) (affirming the Board’s decision that the petitioner in an *inter partes* review did not prove certain challenged claims unpatentable where Petitioner argued that a person of ordinary skill would have combined the references because they were “directed to the same art or same techniques, viz., . . . they ‘discuss[ed] information search and retrieval using computer databases’ or ‘describe[d] storing data in databases, allowing users to query the data, and using indexes to facilitate those queries,” which the Federal Circuit held that those assertions were “inadequate to show persuasively that a relevant skilled artisan would have been motivated to combine the references”).

Petitioner then argues that a POSITA would have looked to Ellsberry because of its relevance to JEDEC standards. Pet. 115. But as noted above, Perego is not about being JEDEC compliant. *See* Section VI.A.2. Moreover, a general reference to JEDEC standards and even to JESD79-2 does not explain what is allegedly

missing from Perego to prompt a POSITA to look to Ellsberry to arrive at the inventions. No such reasoning is given at all.

Petitioner then argues that a POSITA would have looked to Ellsberry for implementation details on rank multiplication. Pet. 115. But first, Perego does not involve the concept of rank, let alone rank multiplication. Second, even if a channel can be a rank, Perego already has ways to target a specific channel, even individual devices, through address information. Indeed, if the desire is to use cheaper, SDRAMs of a different type (*see* Pet. 115), Perego already teaches how to do it: via a buffer that can translate between different protocols. *See* EX1071, 10:59-67. Petitioner provides no explanation why a POSITA would ignore the existing solution in Perego and would instead look to Ellsberry that has a completely different architecture for a solution. *South-Tek Sys., LLC v. Engineered Corrosion Sols., LLC*, 748 F. App'x. 1003, 1007 (Fed. Cir. 2018) (“Given the redundant functions of Viking’s drum drip and Wood’s condensate drain, the Board found a [POSITA] would not have been motivated to add a condensate drain to Viking in addition to the system’s drum drip drain.”); *Ex parte Fritsche*, Appeal No. 2015-001835, at 5 (PTAB, Nov. 14, 2016) (no reason for the combination because “although providing a movable section of an air vent may allow air flow to be distributed to different parts of an automobile, [primary reference] already provides such a movable section that achieves the same function”); *Univ. of Md. Biotechnology Inst.*, 711 F. App'x.

at 1011 (quoting *In re Ratti*, 270 F.2d at 813) (*en banc*) (not obvious where “the ‘suggested combination of references would require a substantial reconstruction and redesign of the elements shown’ in [one of them], or a ‘change in its basic principles’” under which it was designed to operate).

Petitioner also ignores the significant structural differences in Perego and Ellsberry. As Petitioner acknowledges, Perego involves a centralized data buffer while Ellsberry has a distributed data buffer architecture. Pet. 115-116. While Petitioner attempts to waive aside that significant difference by characterizing them as “known alternatives for data buffering,” the fact is the difference has a significant impact on latency and signal integrity. For instance, IDT, a data buffer supplier noted the following when comparing DDR3 LRDIMM’s centralized memory buffer design and DDR4 LRDIMM’s distributed buffer design.

DDR3 LRDIMM Design	Characteristic	Downside
Centralized memory buffer	Longer I/O trace lengths	Longer stubs connected to memory channel cause worse signal reflections, resulting in poorer signal integrity
		Longer traces cause increased latency
		Longer traces cause longer I/O bus turnaround time
Component latency	Delay is approximately 2.5ns	Longer propagation delay adds to latency

DDR4 LRDIMM Design	Characteristic	Upside
Distributed buffers	Shorter I/O trace lengths	Shorter stubs connected to memory channel cause less pronounced signal reflections, resulting in improved signal integrity
		Shorter traces reduce latency
		Shorter traces reduce I/O bus turnaround time
Component latency	Delay is approximately 1.2ns	50% less latency than DDR3 memory buffer,

(EX2010, 2).

In particular, IDT notes that distributed buffer architecture provides “less pronounced signal reflections, resulting in improved signal integrity,” “reduce[d] latency,” “reduce[d] I/O bus turnaround time” and “50% less latency than DDR3 memory buffer.” EX2010, 2; *see also* EX2011 (performance difference comparison between DDR3 HCDIMM with distributed buffer technology and DDR3 LRDIMM with a centralized buffer). At the same time, Perego includes latency-reduction features such as data cache that is absent from Ellsberry. EX1071, 12:5-9 (“Employing a cache 560 may improve memory access time by providing storage of most frequently referenced data and associated tag addresses with lower access

latency characteristics than those of the memory devices.”). There is no analysis at all on how to reconcile the different architectural features and how those different features would affect the resulting latency or why the required latency would follow in the combination.

Indeed, Petitioner does not even assert that Perego lacks any particular implementation detail that it argues would have motivated a POSITA to consult Ellsberry, but merely asserts that a POSITA would look to Ellsberry for alleged implementation detail for memory modules with data buffers. Pet. 115-116. Yet, the fact is Perego describes in detail the features needed for its invention. *See* EX1071 *generally*. Petitioner’s apparent attempt to “[d]efin[e] the problem in terms of its solution reveals improper hindsight in the selection of the prior art relevant to obviousness.” *Monarch Knitting Mach. Corp. v. Sulzer Morat GmbH*, 139 F.3d 877, 880 (Fed. Cir. 1998).

Petitioner’s assertion of predictability in general is also insufficient to make out a *prima facie* case of obviousness. As articles comparing performance of centralized buffer and distributed buffer have made clear, the difference in performance is large and unpredictable. EX2010, 2 (comparing DDR4’s LRDIMMs with a distributed buffer topology with DDR3 LRDIMMs with a central buffer topology); EX2011, 3; EX2014, 27 (Netlist’s DDR3 HDIMM with a distributed buffer topology outperformed DDR3 LRDIMMs with a centralized structure).

Sample Memory Configurations (2CPU)	Total Memory (GB)	Number of DIMMs	DIMM Size	DIMM Ranks	DIMM Type (UDIMM, RDIMM, LRDIMM)	Data Rate	DIMMs per Channel	Unloaded Latency (ns)	Loaded Latency (ns)	Throughput (GB/s)	Idle Power (W)	Loaded Power (W)
24 x 16GB 2R 1333 H	384	24	16GB	2R	HDIMM	1333	2	65.7	114.0	72.4	144.5	286.1
16 x 32GB 4R 1333 L	512	16	32GB	4R	LRDIMM	1333	2	66.8	138.9	68.1	35.3	110.8

To the extent Petitioner bases the combinability on the allegation that Ellsberry is JEDEC compliant and a POSITA would look to it for JEDEC compliance, Petitioner does not explain why a POSITA would modify Perego to make it comply with JEDEC. Pet. 115. Perego, a Rambus architecture, is designed to be different from JEDEC. EX1069, pp. 11-16 (contrasting Rambus memory organization and JEDEC memory organization, noting Rambus memory organization is revolutionary in that it resembles more a computer bus architecture than a typical memory bus architecture). Those two systems are based on different design principles, (*id.*) and forcing Rambus architecture to fit into the JEDEC framework would require fundamental redesign of Perego's/Rambus's system. At the same time, given the standardization, a JEDEC-compliant system—if desired—would have been readily available, thus obviating the need to incur significant costs to redesign Perego. That is evidence of non-obviousness. *Univ. of Md. Biotechnology Inst.*, 711 F. App'x. at 1011 (Fed. Cir. 2017) (quoting *In re Ratti*, 270 F.2d at 813 (*en banc*) (not obvious where “the ‘suggested combination of references would require a substantial reconstruction and redesign of the elements shown’ in

[one of them], or a ‘change in its basic principles’” under which it was designed to operate).

Further, because of their significant structural differences, Petitioner has not provided any competent and non-conclusory evidence that combining Perego and Ellsberry is anything but predictable.

C. Ellsberry does not cure the deficiency of Perego

Petitioner cites Ellsberry for its disclosure of “rank multiplication,” and in particular, for its disclosure of the “rank” concept. But as noted above, the two have completely different architectures. For instance, Ellsberry does not involve a memory module with a configurable width, a point-to-point topology, or an operation based on channels. Simply put, while “rank” or “bank” may have applicability in Ellsberry, that concept is simply absent from Perego, which, as explained in Section VI.A.2, operates on a device-by-device basis, rather than on the basis of a group of predetermined memory devices acting together in response to a read/write command.

Petitioner also cites Ellsberry for the latency-related limitations, relying on Ellsberry’s disclosure of “if cl_mode=subtract, cl = cl-1 to DDRs.” Pet. 119-120. As a preliminary matter, nothing in Ellsberry suggests that the CL parameter—set via the mode register command—is ever sent to Ellsberry’s switch ASICs (the purported data buffers). See EX1073, Fig. 2 (registered command, address and

clocks are sent via control ASIC to memory devices directly), Fig. 8A (MRS-mode register set command—differs from EMRS command), [0044] & Fig. 9 (only mentioning squelching or suppressing certain parameters of extended mode register set (EMRS), and even then, the POSTED CAS_n is passed through to the memory devices). That is, there is no indication that Ellsberry's data buffer even receives CL, let alone transferring data in accordance with that parameter.

Furthermore, neither Ellsberry nor Petitioner explains, however, when “cl_mode=subtract” occurs, what is the operating steps and condition for “cl_mode=subtract,” and whether this operating condition would apply in Perego's vastly different architecture. Pet. 119-120. Petitioner simply assumes that a POSITA would have blindly applied any teaching from Ellsberry to Perego without examining its applicability. *Id.* That is improper and a complete failure in proof.

Petitioner then suggests that because Ellsberry teaches the use of SPD to report features that are emulated, latency-related information would be reported. Pet. 120. But in fact, Ellsberry does not mention SPD reporting a CAS latency that is one clock cycle more than the operational CAS latency of the device (or even that SPD reporting the CAS latency of the memory module instead of the device), as Petitioner asserts. *See* EX1073, [0034]. Nor does Perego mention reporting such information in its description of the information exchanged between the memory

controller and the SPD. *See* EX1071, 12:20-34. Petitioner’s argument for claim 4 therefore falls under the controlling case law of *Arendi*.

As to additional limitations in claims 12-13, concerning cross-the-rank back-to-back read operations, those teachings appear only in the subject matter patents. Ellsberry says nothing about how to configure the buffer to time the first and second read strobes to avoid collisions. *See* EX1073 generally. Indeed, there is not even any indication that Ellsberry ever considered the cross-rank back-to-back read operation as a problem, let alone offering a solution to it. In that regard, Petitioner’s citation to Fig. 27 of JESD79-2 is also not on point, because there is no indication that this concerned a cross-rank back-to-back read operation, as opposed to back-to-back operations in the same device (but from the same or different banks of the memory device). *See* EX1064, p.1 (JESD79-2 is a specification for individual DDR2 SDRAMs, and therefore does not concern different devices in different ranks), p.28 (“The operation is allowed regardless of same or different banks as long as the banks are activated”); EX2007-p.2 (banks refer to memory sub-arrays within a DRAM device).

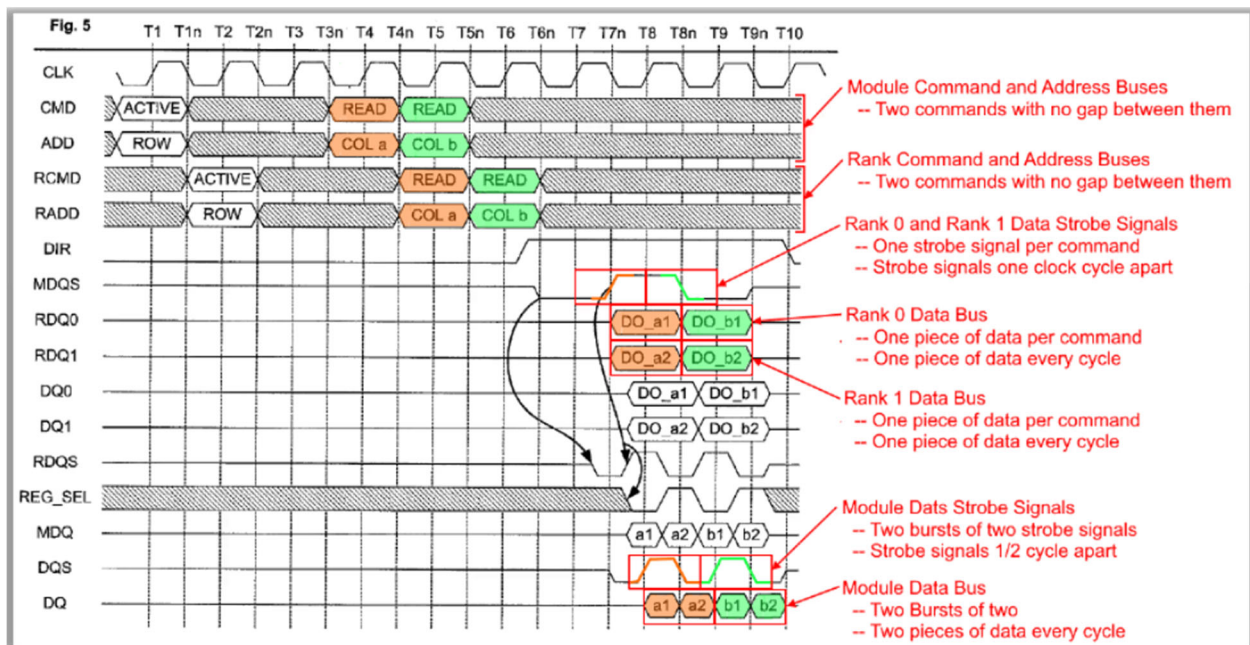
VIII. PETITIONER HAS NOT MADE A *PRIMA FACIE* CASE OF OBVIOUSNESS FOR GROUND 3

A. Halbert does not cure the deficiency of Perego

Halbert would not cure the deficiencies of Perego. For example, Petitioner cites Halbert for element 1.d.2-1.d.3, which require “the first rank [be] selected to receive or output the first data burst in response to the first memory command and [be] not selected to communicate data with the memory controller in response to the second memory command” whereas “the second rank [be] selected to receive or output the second data burst in response to the second memory command and [be] not selected to communicate data with the memory controller in response to the first memory command.” Pet. xiv, 1.d.2-1.d.3.

Halbert does not teach this, because the two ranks in Halbert always respond to the read/write commands together. *See* EX1078, Figs. 5-6. That is, Halbert does not disclose an implementation in which one rank of memory device is selected to respond to one read/write command but not the other read/write command(s). Specifically, Halbert aims to “widen[] the data bus on the memory module as compared to the width of the system memory data bus,” as this “allow[s] a faster system memory data bus to operate at full speed with slower memory devices.” EX1078, [0023]. This is achieved by accessing, via 2m data lines, the slower memory devices in multiple ranks 140 and 142 simultaneously and in parallel, while

the data interface circuit 120 interfaces such parallel memory device accesses with faster serial data transfers to or from the system memory controller. *Id.*, [0027]-[0033]. Accordingly, “multiple ranks will receive the same address and commands, and will perform memory operations with the interface circuit concurrently.” *Id.*, [0030]. A corresponding timing diagram for a read operation with annotation is shown below.



As is clear from the timing diagram and the associated description, in response to each read (or write) command, both ranks participate in the read/write operation. See EX1078, Figs. 5-6.

Because other claims depend on independent claim 1 (and claim 16 with similar missing limitations), addition of Halbert would not render the other claims obvious either.

B. Petitioner has not stated a *prima facie* reason to combine Perego and Halbert

Petitioner suggests that “a POSITA would have been motivated to use Halbert’s rank-based arrangements in Perego’s module ...since they ‘allow the memory devices to be isolated from the full capacitive loading effects of the system memory data bus ... [and] avoid arrangements of competing memory banks that load each other” Pet. 127. But according to Petitioner, “[a] POSITA would [already] have understood that the input and output latches 597f-m [of Perego] isolate the load of the ‘memory devices’ from the memory controller ... since the memory controller only sees the load of the latches 597f-m.” IPR2023-00454 Pet. 97. Similarly, by buffering all control/address and data signals between the memory controller and memory devices, Perego’s memory devices in different channels are already isolated from one another due to the intervening buffer device. *See* EX1071, Figs. 3A-3C. In other words, Perego already has the feature that Petitioner alleges would have motivated a POSITA to incorporate from Halbert. But a POSITA would not have been motivated to make the combination given the redundancy to the existing features. *South-Tek Sys., LLC*, 748 F. App’x. at 1007 (“Given the redundant functions of Viking’s drum drip and Wood’s condensate drain, the Board found a [POSITA] would not have been motivated to add a condensate drain to Viking in addition to the system’s drum drip drain.”).

Petitioner also provides no detail whatsoever on how it suggests a POSITA should incorporate Halbert's design in Perego. For instance, is Petitioner proposing to modify Perego so that it adopts the multi-rank participation per read/write operation as in Halbert? If so, as explained in Section A above, the resulting configuration would not satisfy element 1.d.2-1.d.3. Or is Petitioner suggesting that, contrary to its assertion for Ground 1, Perego actually does not disclose or suggest the concept of rank, but a POSITA would have nevertheless looked to Halbert to incorporate the rank concept into Perego's design? If so, why would a POSITA be motivated to modify Perego to incorporate the rank concept? Perego operates on an individual device level, with "individual device identification values" even when multiple devices share the same channel. *See* EX1071, 9:64-10:4; EX1069, p.12 (having a unique identification number for each DRAM is needed to identify recipient of a request packet because Rambus memory organization does not involve "chip-select network"). Modifying Perego to incorporate Halbert's "rank-based arrangement," in which a predetermined set of memory devices act together in response to a received command, would require changing of Perego's operating principles. *Univ. of Md. Biotechnology Inst.*, 711 F. App'x. at 1011 (quoting *In re Ratti*, 270 F.2d 810 at 813) (*en banc*) (not obvious where "the 'suggested combination of references would require a substantial reconstruction and redesign of the elements shown' in [one of them], or a 'change in its basic principles'" under

which it was designed to operate). As such, the proposed modification would not be obvious to a POSITA. *Id.*

IX. PETITIONER HAS NOT MADE A *PRIMA FACIE* CASE OF OBVIOUSNESS FOR GROUND 4

Petitioner suggests that a POSITA would have combined Perego and Matsui2 to “effectively prevent[] reflection between the data bus and each memory device[]” at high speed. Pet. 132. But Matsui does not utilize the same point-to-point topology as Perego, or configurable width buffer. And Perego already discloses how to terminate signal lines, including data signal lines from the memory devices. *See* Figs. 4A-4B. Petitioner does not explain why those solutions are inadequate, and a POSITA would look to Matsui2 instead. *South-Tek Sys., LLC v. Engineered Corrosion Sols., LLC*, 748 F. App’x. 1003, 1007 (Fed. Cir. 2018) (“Given the redundant functions of Viking’s drum drip and Wood’s condensate drain, the Board found a [POSITA] would not have been motivated to add a condensate drain to Viking in addition to the system’s drum drip drain.”).

X. DISCRETIONARY DENIAL IS WARRANTED

A. 325(d) Favors Denial

The Board uses a two-part framework in evaluating whether to exercise discretion under 35 U.S.C. § 325(d). Under Part 1, the Board considers “whether the same or substantially the same art previously was presented to the Office or whether the same or substantially the same arguments previously were presented to the

Office.” *Advanced Bionics, LLC v. MED-EL Elektromedizinische Geräte GmbH*, IPR2019-01469, Paper 6 at 8 (P.T.A.B. Feb. 13, 2020). Under Part 2, if either condition in Part 1 is satisfied, the Board considers “whether the petitioner has demonstrated that the Office erred in a manner material to the patentability of challenged claims.” *Id.* Applying the *Advanced Bionics* framework confirms that the Petition should be denied institution under §325(d).

Petitioner admits that Ellsberry and Halbert³ were disclosed in an IDS during prosecution. Pet., 135; *see also* EX1002, 329 (#110, Halbert’s parent), 331 (#198, Ellsberry). Petitioner’s sole argument against Part 1 being satisfied is that the references “were buried in an IDS,” but that applies an incorrect standard. *See Nespresso USA, Inc. v. K-Fee System GMBH*, IPR2021-01221, Paper 9 at 13 (P.T.A.B. Jan. 18, 2022) (“The precedential decision in *Advanced Bionics* unambiguously instructs, however, ‘**Previously presented art** includes art made of record by the Examiner, and art provided to the Office by an applicant, **such as on an Information Disclosure Statement (IDS)**, in the prosecution history of the

³ Petitioner admits that “family members of...Halbert were disclosed,” but not only were multiple “family members” cited, the prior publication of Halbert was actually cited. *See* EX1077; EX1078, p.1 (listing EX1077 under “Prior Publication Data”); Pet. 136 (referencing “Halbert’s publication”).

challenged patent.”) (quoting *Advanced Bionics*, Paper 6 at 7-8); *Roku, Inc. v. Universal Electronics, Inc.*, IPR2019-01619, Paper 17 at 6-7 (P.T.A.B. May 25, 2021) (denying rehearing request because the Board “did not misapprehend *Advanced Bionics* in finding that Herz was previously was presented to the Office” as a result of being cited in an IDS).

Moreover, the interview notes stated that the examiner discussed “***Applicant cited prior art in IDS***” with the applicant, and had reached agreement as to the limitations that needed to be added to distinguish those art. EX1002, 295, 436. Halbert and Ellsberry, as well as Perego and JEDEC standards (discussed below), are part of the applicant cited prior art. *See id.*, 314-315 (S127 included US-6742098 (Halbert parent)), 323 (S169 included 20060277355 (Ellsberry)), 363 (S8 included US 6502161 (Perego parent)), 364 (S8 included US 7356639 (Perego-639)); 331, 358 (examiner stating that he considered all the references on the IDS except where lined through, and Ellsberry and Halbert’s publication were not lined through). One cannot speculate that the examiner did not consider the reference when the record indicated that he did consider them. Thus, both Ellsberry and Halbert qualify as previously presented art under *Advanced Bionics*. *See Nespresso*, Paper 9 at 13-14 (P.T.A.B. Jan. 18, 2022) (denying institution because, even though the references “appear[ed] on a relatively long list of documents presented to the Examiner in an

IDS....Clear intrinsic evidence informs, ‘All references’ submitted in the IDSs were ‘considered except where lined through, as certified by [the examiner].’”).

Petitioner also admits that “family members of Perego...were disclosed” during prosecution. Pet., 135. Indeed, Perego (EX1071) is materially the same as Perego-639 (EX2017), a continuation-in-part of Perego that was considered by the examiner during prosecution of the ’215 Patent. *See id.*, 1:4-6; EX1001, 3 (listing Perego-639); EX1002, 330. As shown by a redline of Perego-639 against Perego, the entirety of Perego’s specification was maintained in Perego-639. *See* EX2018. Thus, for the same reasons as stated for Ellsberry and Halbert, Perego also qualifies as the same or substantially the same art presented to the office.

Furthermore, the JEDEC standard is also the same as art presented to the office. Petitioner admits as much, stating that “[a] POSITA would have been familiar with these JEDEC standards,” and that “[t]he prior art also refers to these JEDEC standards.” Pet., 9-10 (citing passages from Perego and Ellsberry discussing JEDEC standards), *id.*, 114 (asserting that Ellsberry “expressly incorporates by reference the corresponding JEDEC standards, including JESD79-2 (EX1064)).

Finally, it is of no consequence that Matsui2 was not cited during prosecution. Matsui2 is only relied upon for a single ground (Ground 4), and for a single dependent claim (claim 7). Pet., 131-134. Matsui2’s inclusion is irrelevant in light of the fact that the Petition has failed to make a *prima facie* case that claim 1 (or any

claim of the '215 Patent) is obvious in light of Ground 1. *See* Sections VI-VIII, *supra*. Thus, *Advanced Bionics* Part 1 is satisfied. *See also Nespresso USA*, Paper 9, at 13-14 (institution denied even though only three of the five references “appear[ed] on a relatively long list of documents presented to the Examiner in an IDS”).

Turning to Part 2 of *Advanced Bionics*, the Petition does not show that the Office erred in its examination. *See Advanced Bionics*, IPR2019-01469, Paper 6 at 10 (noting that this inquiry “focus[es] on the petitioner’s evidence of previous Office error”). Petitioner does not specifically identify any errors and instead conclusory rests on its arguments for Grounds 1-4. Pet. 136. However, as discussed above, the Office did not err, as none of the references in the Petition render the challenged claims obvious. Petitioner’s arguments at most show that a reasonable mind could differ in the conclusion, which is not sufficient to show material error under the *Advanced Bionics* framework. Discretionary denial is warranted.

B. 314(a) Favors Denial

The Petition should be denied under §314(a) pursuant to the *Fintiv* factors in light of parallel litigation between the parties.

1. Likelihood of a stay – Petitioner has sought a stay pending a Ninth Circuit appeal on a contract action. The motion has been pending since last fall, and it is unlikely that the court will grant it. Petitioner has not sought a stay based on the

IPRs; nor is such a request likely granted because, as stated below, trial will likely occur long before any final written decision is issued. This factor weighs against institution.

2. Proximity of the court's trial date to a final written decision – Trial in the parallel litigation is currently scheduled for April 15, 2024. Ex. 2021, 1. Thus, it is very likely that trial will conclude before the issuance of any final written decision, as the statutory deadline will be fifteen months from the date of this POPR, which is August 9, 2024. *Allergan, Inc. v. BTL Healthcare Technologies A.S.*, PGR2021-00016, Paper 16 at 13-19 (P.T.A.B. June 16, 2021) (denying institution under 314(a) because of the significant overlap with parallel ITC proceeding which would end four months before a final written decision). Furthermore, the most recent published median time-to-trial for EDTX is only 19 months (placing the start of trial at March 1, 2024), which is much shorter than Petitioner's out-of-date, COVID-19 influenced statistic. *Compare* EX2019, 35, *with* EX1092, 35. Having to litigate in parallel with an IPR proceeding would be an unnecessary waste of time and resources, particularly in light of the weakness of the Petition.

This factor weighs against institution. *Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 11 at 9 (PTAB March 20, 2020) (precedential) ("If the court's trial date is earlier than the projected statutory deadline, the Board generally has weighed this fact in favor of exercising authority to deny institution under *NHK*."); *Samsung*

Electronics Co., Ltd. v. California Institute of Technology, IPR2023-00130, Paper 10 at 16 (P.T.A.B. May 4, 2023) (“Regardless of whether we consider the scheduled trial date or the trial date expected based on time-to-trial statistics, the trial in the Underlying Litigation would commence several months before the expected date of our final written decision.”).

3. Investment in the parallel proceeding by the court and the parties –

The parties have already exchanged infringement and invalidity contentions, and fact discovery is underway. EX2021. Furthermore, by the time of the institution decision, claim construction will be underway. This factor weighs against institution.

4. Overlap with parallel proceedings – There is a significant overlap between the validity issues present here and the issues to be decided by the district court. Petitioner is accused of infringing all challenged claims of the ’215 Patent, and has served invalidity contentions against all challenged claims, including Perego, JESD79-2, Ellsberry, Halbert, and Matsui² as prior art references. EX2022, 1, 17-20. Furthermore, Petitioner has not submitted a *Sotera* stipulation stating that, if this IPR is instituted, it will not pursue any grounds it has or could have raised in the Petition (although that would still not outweigh the other factors). Additionally, Petitioner’s past conduct—including pursuing invalidity grounds that is clearly covered by the *Sotera* stipulation even after being notified of the violation by

Netlist—strongly indicates that it has no intention of honoring the stipulation until being told by the district court, at which point resources have already been wasted. This factor weighs against institution.

5. Whether the Petitioner and the defendant in the parallel proceedings are the same party – Petitioner is a defendant in the parallel litigation. This weighs against institution.

6. Other circumstances – The merits of the Petition are weak, which weighs against institution. As such, a denial of institution under the *Fintiv* factors would not be in conflict with Director Vidal’s 2022 Memorandum. Petitioner has not demonstrated a reasonable likelihood of success, let alone that the merits of the Petition are *compelling*. *CommScope Techs. LLC v. Dali Wireless, Inc.*, IPR2022-01242, Paper 23 at 3 (P.T.A.B. Feb. 23, 2023) (precedential) (“[T]he compelling merits standard is a higher standard...”). Discretionary denial is warranted.

XI. CONCLUSION

Based on the foregoing, the Board should decline to institute an *inter partes* review.

Dated: May 9, 2023

Respectfully submitted,

/Hong Zhong/

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CERTIFICATE OF WORD COUNT

I hereby certify, pursuant to 37 C.F.R. section 42.24, that the foregoing Patent Owner Preliminary Response contains 11,441 words, excluding the words in the table of contents, table of authorities, mandatory notices under section 42.8, this certificate of word count, certificate of service or exhibit list. The word count is based on the word count of the Microsoft Word program used to prepare the Patent Owner Preliminary Response.

/Hong Zhong/
H. Annita Zhong (66,530)

CERTIFICATE OF SERVICE

I hereby certify, pursuant to 37 C.F.R. section 42.6, that on May 9, 2023, a complete copy of the **PATENT OWNER'S PRELIMINARY RESPONSE and EXHIBITS 2001-2007 and 2009-2022** were served upon the following, by ELECTRONIC MAIL:

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