

FAQs

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+ Are Verilog models available for Micron modules?

+ Can a parity module be used in a system that is not designed to use parity?

+ Can Micron provide models for the module connectors?

+ Can Micron provide module Gerber files to customers?

+ Does Micron provide Hyperlynx models?

+ Does Micron provide VHDL models for modules?

+ Does the model that I'm downloading support all the drive strengths listed in the data sheet?

+ How do I tell if I have the correct IBIS or HSPICE model for a given die revision indicator?

+ How does Micron validate the quality of its IBIS and HSPICE models?



- + What does the model revision number indicate when it changes from a 1.x level to a 2.x level?

+ What is a board (.brd) file?

+ What is a Gerber file?

+ What is a "rank"?

+ What is an EBD (.ebd) file?

+ What is an IBIS (.ibs) file?

+ What is the advantage of multiple banks within a component?

- What is the difference between a "bank" and a "rank?"

Banks are specific to individual DRAM components and refer to sub-arrays within the DRAM component. Ranks are specific to memory modules and refer to a sub-array made of multiple DRAM components.

+ What makes up an IBIS model for a module?

+ What trace lengths and termination values does Micron suggest I use on my memory interface?

+ Why are IBIS models for DRAM components regularly posted to micron.com but not IBIS models for modules?

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