DDR2 SDRAM FBDIMM

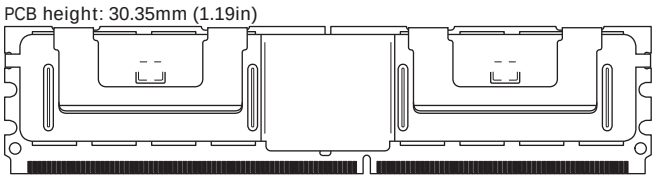
MT36HTF51272FD – 4GB

For components data sheets, refer to Micron's Web site: www.micron.com

Features

- 240-pin, fully buffered dual in-line memory module (FBDIMM)
- Fast data transfer rates: PC2-5300 or PC2-6400
- 4GB (512 Meg x 72)
- Supports ECC error detection and correction
- Vdd = +1.8V for DRAM
- Vref = 0.9V SDRAM command and address termination
- Vcc = 1.5V for advanced memory buffer (AMB)
- Vddspd = +3.0V to +3.6V for AMB and EEPROM
- Quad rank, using 1Gb (128Mb x 8) devices
- Serial presence-detect (SPD) with EEPROM
- Gold edge contacts
- Lead-free
- Supports 95°C operation with 2X refresh
- 4.0 Gb/s or 4.8 Gb/s link transfer rates
- High-speed, differential, point-to-point link between host memory controller and the AMB
- Fault-tolerant; can work around a bad bit lane in each direction
- High-density scaling with up to 8 FBDIMM devices per channel
- SMBus interface to AMB for configuration register access
- In-band and out-of-band command access
- Deterministic protocol
  - Enables memory controller to optimize DRAM accesses for maximum performance
  - Delivers precise control and repeatable memory behavior
- Automatic DDR2 SDRAM bus and channel calibration
- Transmitter de-emphasis to reduce ISI
- MBIST and IBIST test functions
- Transparent mode for DRAM test support

Figure 1: 240-Pin FBDIMM (MO-256)



Options	Marking
• Package	
– 240-pin DIMM (lead-free)	Y
• Frequency/CAS latency	
– 2.5ns @ CL = 5 (DDR2-800)	-80E
– 3.0ns @ CL = 5 (DDR2-667)	-667

Table 1: Key Timing Parameters

Speed Grade	Industry Nomenclature	Data Rate (MT/s)			^{t}RCD (ns)	^{t}RP (ns)	^{t}RC (ns)
		CL = 5	CL = 4	CL = 3			
-80E	PC2-6400	800	533	–	12.5	12.5	55
-667	PC2-5300	667	533	400	15	15	55

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Table 2: Addressing

Parameter	4GB
Refresh count	8K
Row address	16K A[13:0]
Device bank address	8 BA[2:0]
Device configuration	1Gb (128Mb x 8)
Column address	1K A[11, 9:0]
Module rank address	4 S0#[3:0]

Table 3: Part Numbers and Timing Parameters – 4GB Modules

Base device: MT47H128M8,[1] DDR2 SDRAM

Part Number[2]	Module Density	Configuration	Module Bandwidth	Memory Clock/Data Rate	Clock Cycles (CL-^{t}RCD-^{t}RP)	Link Transfer Rate
MT36HTF51272FDY-80E__	4GB	512 Meg x 72	6.4 GB/s	2.5ns/800 MT/s	5-5-5	4.8 GT/s
MT36HTF51272FDY-667__	4GB	512 Meg x 72	5.3 GB/s	3.0ns/667 MT/s	5-5-5	4.0 GT/s

Notes:
1. The data sheet for the base device can be found on Micron's Web site.
2. All part numbers end with a four-place code (not shown) that designates component, PCB, and AMB revisions. Consult factory for current revision codes.
   Example: MT36HTF51272FDY-667E1D6.

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Pin Assignments and Descriptions

Table 4: Pin Assignments

240-Pin DDR2 FBDIMM Front								240-Pin DDR2 FBDIMM Back							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	Vdd	31	PN3	61	PN9#	91	PS9#[1]	121	Vdd	151	SN3	181	SN9#	211	SS9#[1]
2	Vdd	32	PN3#	62	Vss	92	Vss	122	Vdd	152	SN3#	182	Vss	212	Vss
3	Vdd	33	Vss	63	PN10	93	PS5	123	Vdd	153	Vss	183	SN10	213	SS5
4	Vss	34	PN4	64	PN10#	94	PS5#	124	Vss	154	SN4	184	SN10#	214	SS5#
5	Vdd	35	PN4#	65	Vss	95	Vss	125	Vdd	155	SN4#	185	Vss	215	Vss
6	Vdd	36	Vss	66	PN11	96	PS6	126	Vdd	156	Vss	186	SN11	216	SS6
7	Vdd	37	PN5	67	PN11#	97	PS6#	127	Vdd	157	SN5	187	SN11#	217	SS6#
8	Vss	38	PN5#	68	Vss	98	Vss	128	Vss	158	SN5#	188	Vss	218	Vss
9	Vcc	39	Vss	69	Vss	99	PS7	129	Vcc	159	Vss	189	Vss	219	SS7
10	Vcc	40	PN13[1]	70	PS0	100	PS7#	130	Vcc	160	SN13[1]	190	SS0	220	SS7#
11	Vss	41	PN13#[1]	71	PS0#	101	Vss	131	Vss	161	SN13#[1]	191	SS0#	221	Vss
12	Vcc	42	Vss	72	Vss	102	PS8	132	Vcc	162	Vss	192	Vss	222	SS8
13	Vcc	43	Vss	73	PS1	103	PS8#	133	Vcc	163	Vss	193	SS1	223	SS8#
14	Vss	44	NC	74	PS1#	104	Vss	134	Vss	164	NC	194	SS1#	224	Vss
15	Vtt	45	NC	75	Vss	105	NC	135	Vtt	165	NC	195	Vss	225	NC
16	NC	46	Vss	76	PS2	106	NC	136	NC	166	Vss	196	SS2	226	NC
17	RESET#	47	Vss	77	PS2#	107	Vss	137	M_TEST (NU)	167	Vss	197	SS2#	227	Vss
18	Vss	48	PN12[1]	78	Vss	108	Vdd	138	Vss	168	SN12[1]	198	Vss	228	SCK
19	NC	49	PN12#[1]	79	PS3	109	Vdd	139	NC	169	SN12#[1]	199	SS3	229	SCK#
20	NC	50	Vss	80	PS3#	110	Vss	140	NC	170	Vss	200	SS3#	230	Vss
21	Vss	51	PN6	81	Vss	111	Vdd	141	Vss	171	SN6	201	Vss	231	Vdd
22	PN0	52	PN6#	82	PS4	112	Vdd	142	SN0	172	SN6#	202	SS4	232	Vdd
23	PN0#	53	Vss	83	PS4#	113	Vdd	143	SN0#	173	Vss	203	SS4#	233	Vdd
24	Vss	54	PN7	84	Vss	114	Vss	144	Vss	174	SN7	204	Vss	234	Vss
25	PN1	55	PN7#	85	Vss	115	Vdd	145	SN1	175	SN7#	205	Vss	235	Vdd
26	PN1#	56	Vss	86	NC	116	Vdd	146	SN1#	176	Vss	206	NC	236	Vdd
27	Vss	57	PN8	87	NC	117	Vtt	147	Vss	177	SN8	207	NC	237	Vtt
28	PN2	58	PN8#	88	Vss	118	SA2	148	SN2	178	SN8#	208	Vss	238	Vddspd
29	PN2#	59	Vss	89	Vss	119	SDA	149	SN2#	179	Vss	209	Vss	239	SA0
30	Vss	60	PN9	90	PS9[1]	120	SCL	150	Vss	180	SN9	210	SS9[1]	240	SA1

Notes: 1. The following signals are cyclical redundancy code (CRC) bits and, thus, appear out of the normal sequence: PN12/PN12#, SN12/SN12#, PN13/PN13#, SN13/SN13#, PS9/PS9#, and SS9/SS9#.

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Table 5: Pin Descriptions

Symbol	Type	Description
PS[9:0]	Input	Primary southbound data, positive lines.
PS#[9:0]	Input	Primary southbound data, negative lines.
SCK	Input	System clock input, positive line.
SCK#	Input	System clock input, negative line.
SCL	Input	**Serial clock for SPD EEPROM:** SCL is used to synchronize communication to and from the SPD EEPROM.
SN[13:0]	Input	Secondary northbound data, positive lines.
SN#[13:0]	Input	Secondary northbound data, negative lines.
SS[9:0]	Output	Secondary southbound data, positive lines.
SS#[9:0]	Output	Secondary southbound data, negative lines.
PN[13:0]	Output	Primary northbound data, positive lines.
PN#[13:0]	Output	Primary northbound data, negative lines.
SA[2:0]	I/O	**Serial address inputs:** These pins are used to configure the SPD EEPROM address range on the I_bC bus.
SDA	I/O	**Serial data:** SDA is a bidirectional pin used to transfer addresses and data into and out of the SPD EEPROM on the module on the I2C bus.
RESET#	Supply	**Reset:** Asynchronously forces all registered outputs LOW when RESET# is LOW. This signal can be used during power-up to ensure that CKE is LOW and DQ are High-Z.
Vcc	Supply	AMB core power and AMB channel interface power (1.5V).
Vdd	Supply	**Power supply:** 1.8V ±0.1V. The component Vdd and Vddq are connected to the module Vdd.
Vddspd	Supply	**SPD EEPROM power supply:** +1.7V to +3.6V.
Vss	Supply	Ground.
Vtt	Supply	DRAM address/command/clock termination power (Vdd/2).
M_TEST	–	The M_TEST pin provides an external connection for testing the margin of Vref, which is produced by a voltage divider on the module. It is not intended to be used in normal system operation and must not be connected (NU) in a system. This test pin may have other features on future card designs and will be included in this specification at that time.
NU	–	**Not used:** These pins are not used in specific module configuration/operations.
NC	–	**No connect:** These pins are not connected on the module.

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Block Diagrams

Figure 2: System Block Diagram

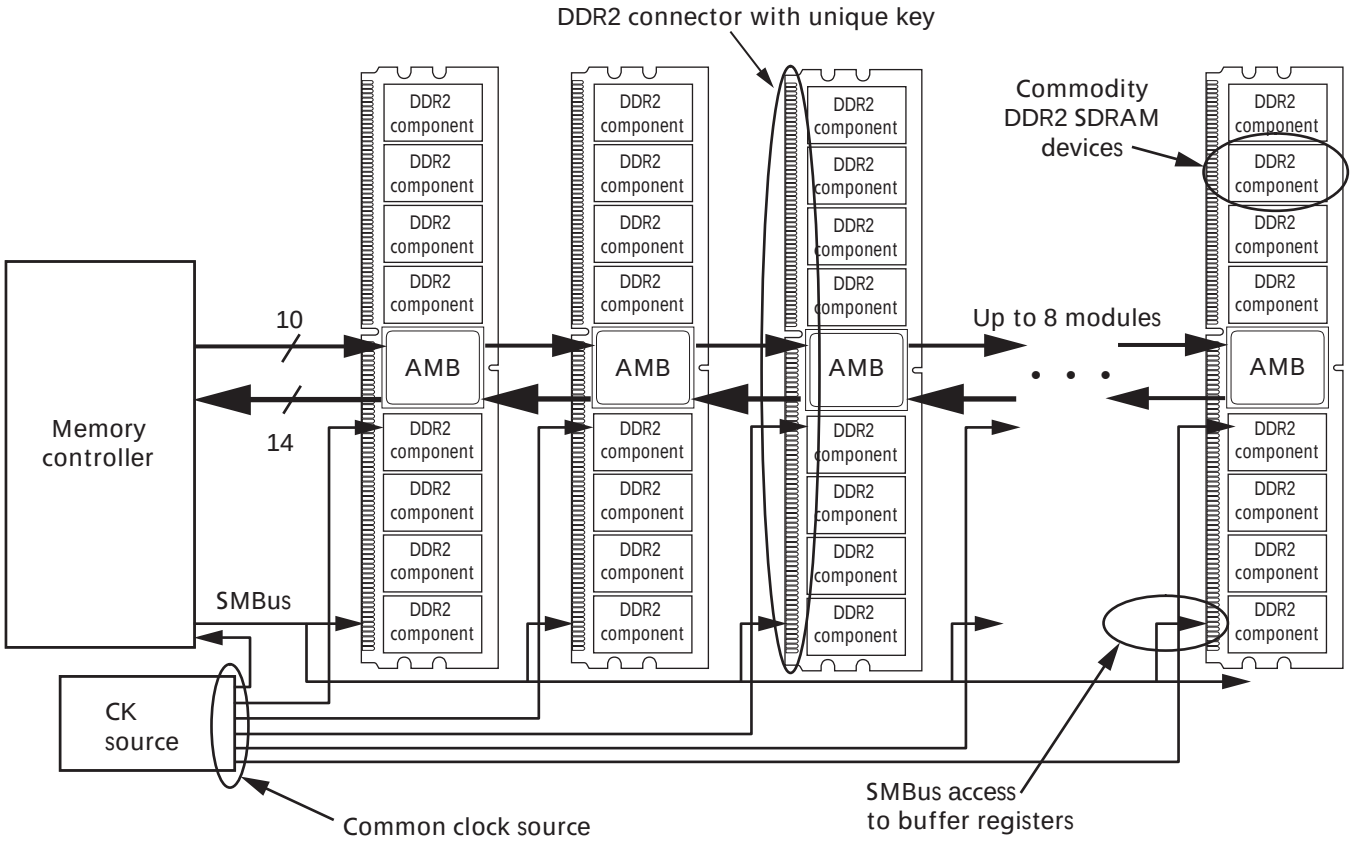

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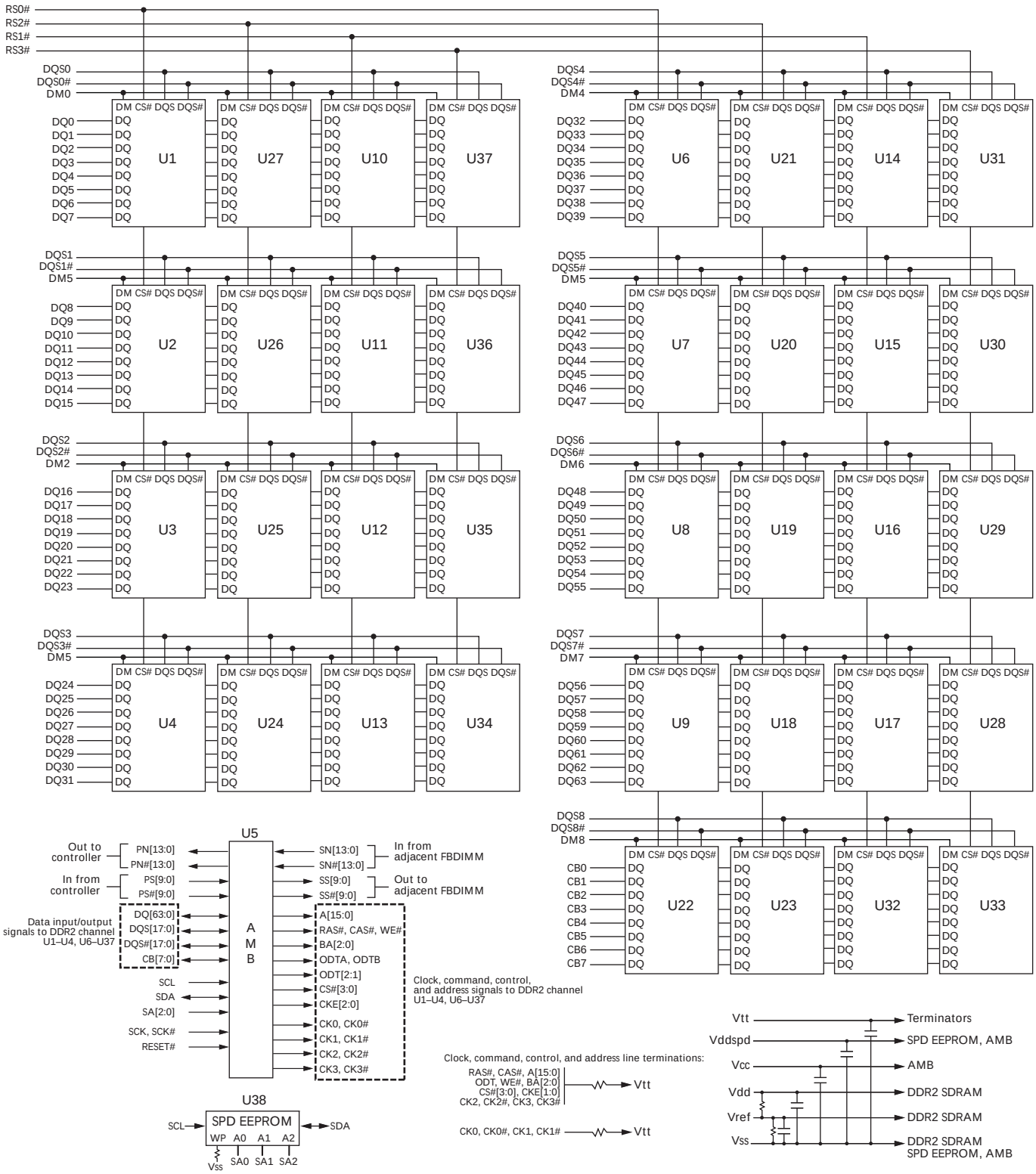
Figure 3: Functional Block Diagram



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General Description

Micron® FBDIMMs conform to the current proposed industry specifications for FBDIMM devices. The following specifications contain detailed information about FBDIMM design, interfaces, and theory of operation and are listed for the convenience of system designers. Refer to the JEDEC Web site for available specifications.

- FBDIMM Design Specification – pending JEDEC approval
- FBDIMM: Architecture and Protocol – JESD206
- FBDIMM: Advanced Memory Buffer (AMB) – JESD82-20
- Design for Test, Design for Validation (DF*x*) Specification
- Serial Presence-Detect (SPD) for Fully Buffered DIMM – JEDEC Standard No. 21-C, page 4.1.2.7-1

The MT36HTF51272FD DDR2 SDRAM module is a high-bandwidth, large-capacity channel solution that has a narrow host interface. FBDIMM devices use DDR2 SDRAM devices isolated from the channel behind an AMB buffer on the FBDIMM. Memory device capacity remains high, and total memory capacity scales with DDR2 SDRAM bit density.

As shown in Figure 2 on page 5, the FBDIMM channel provides a communication path from a host controller to an array of DDR2 SDRAM devices, with the DDR2 SDRAM devices buffered behind an AMB device. The physical isolation of the DDR2 SDRAM devices from the channel provides the flexibility needed to enhance the communication path and significantly increase reliability and availability of the memory subsystem.

Advanced Memory Buffer

The AMB isolates the DDR2 SDRAM devices from the channel. This single-chip AMB component, located in the center of each FBDIMM, acts as a repeater and buffer for all signals and commands exchanged among the host controller and DDR2 SDRAM devices, including data input and output. The AMB communicates with the host controller and adjacent FBDIMMs on a system board using an industry-standard, high-speed, differential, 1.5V, point-to-point interface. The AMB also enables buffering of memory traffic to support large memory capacities. Refer to the JEDEC JESD82-20 specification for further information.

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Electrical Specifications

Stresses greater than those listed in Table 6 may cause permanent damage to the module. This is a stress rating only, and functional operation of the module at these or any other conditions outside those indicated in each device's data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may adversely affect reliability.

Table 6: Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units	Notes
Vin, Vout	Voltage on any pin relative to Vss	–0.3	+1.75	V	1
Vcc	Voltage on Vcc pin relative to Vss	–0.3	+1.75	V	
Vdd	Voltage on Vdd pin relative to Vss	–0.5	+2.3	V	
Vtt	Voltage on Vtt pin relative to Vss	–0.5	+2.3	V	
T_C	DDR2 SDRAM device operating case temperature	0	+95	°C	2, 3
	AMB device operating case temperature	0	+110	°C	

Notes:
1. Vin should not be greater than Vcc.
2. T_C is specified at 95°C only when using 2X refresh timing (^tREFI = 7.8µs at or below 85°C; ^tREFI = 3.9µs above 85°C); refer to the DDR2 SDRAM component data sheet.
3. See applicable DDR2 SDRAM component data sheet for ^tREFI and extended mode register settings. The ^tREFI parameter is used to specify the doubled refresh interval necessary to sustain <85°C operation.

Table 7: Input Voltage and Operating Conditions

Parameter	Symbol	Min	Nom	Max	Units	Notes
AMB supply voltage	Vcc	1.46	1.5	1.54	V	
DDR2 SDRAM supply voltage	Vdd	1.7	1.8	1.9	V	
Termination voltage	Vtt	0.48 × Vdd	0.5 × Vdd	0.52 × Vdd	V	
EEPROM supply voltage	Vddspd	3.0	3.3	3.6	V	1
SPD input high (logic 1) voltage	Vih(DC)	2.1	–	Vddspd	V	2
SPD input low (logic 0) voltage	Vil(DC)	–	–	0.8	V	2
RESET# input high (logic 1) voltage	Vih(DC)	1.0	–	–	V	3
RESET# input low (logic 0) voltage	Vil(DC)	–	–	0.5	V	2
Leakage current (RESET#)	II	–90	–	+90	µA	3
Leakage current (link)	II	–5	–	+5	µA	4

Notes:
1. Applies to AMB and SPD.
2. Applies to SMB and SPD bus signals.
3. Applies to AMB CMOS signal RESET#.
4. For all other AMB-related DC parameters, please refer to the high-speed differential link interface specification.

Table 8: Clock Rates

FBDIMM Link Data Rate	Reference Clock	DRAM Clock	DRAM Data Rate
4.0 Gb/s	167 MHz	333 MHz	667 Mb/s
4.8 Gb/s	200 MHz	400 MHz	800 Mb/s

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Idd Conditions and Specifications

Table 9: Idd Conditions

Symbol	Condition
Idd_Idle_0	**Idle current, single, or last DIMM:** L0 state; Idle (0% bandwidth); Primary channel enabled; Secondary channel disabled; CKE HIGH; Command and address lines stable; DDR2 SDRAM clock active
Idd_Idle_1	**Idle current, first DIMM:** L0 state; Idle (0% bandwidth); Primary and secondary channels enabled; CKE HIGH; Command and address lines stable; DDR2 SDRAM clock active
Idd_Active_1	**Active power:** L0 state; 50% DRAM bandwidth; 67% READ; 33% WRITE; Primary and secondary channels enabled; DDR2 SDRAM clock active; CKE HIGH
Idd_Active_2	**Active power, data pass-through:** L0 state; 50% DRAM bandwidth to downstream DIMM; 67% READ; 33% WRITE; Primary and secondary channels enabled; DDR2 SDRAM clock active; CKE HIGH; Command and address lines stable
Idd_Training	**Training:** Primary and secondary channels enabled; 100% toggle on all channel lanes; DRAM idle (0% bandwidth) CKE HIGH; Command and address lines stable; DDR2 SDRAM clock active
Idd_IBIST	**IBIST over all IBIST modes:** DRAM idle (0% bandwidth); Primary channel enabled; Secondary channel enabled; CKE HIGH; Command and address lines stable; DDR2 SDRAM clock active
Idd_EI	**Electrical idle:** DRAM idle (0% bandwidth); Primary channel disabled; Secondary channel disabled; CKE LOW; Command and address lines floated; DDR2 SDRAM clock active; ODT and CKE driven LOW

Notes: 1. Actual test conditions may vary from published JEDEC test conditions.

Table 10: Idd Specifications – 4GB DDR2-800

Symbol	Idd_Idle_0	Idd_Idle_1	Idd_Active_1	Idd_Active_2	Idd_Training	Idd_IBIST	Idd_EI	Units
Icc	TBD	TBD	TBD	TBD	TBD	TBD	TBD	mA
Idd	TBD	TBD	TBD	TBD	TBD	TBD	TBD	mA
Total power	TBD	TBD	TBD	TBD	TBD	TBD	TBD	W

Table 11: Idd Specifications – 4GB DDR2-667

Symbol	Idd_Idle_0	Idd_Idle_1	Idd_Active_1	Idd_Active_2	Idd_Training	Idd_IBIST	Idd_EI	Units
Icc	2600	3400	3900	3700	4000	4500	2500	mA
Idd	2140	2140	2515	2140	2140	2140	452	mA
Total power	8.2	9.4	10.9	10.9	9.9	11.2	4.8	W

Notes: 1. Total power is based on maximum voltage levels, Icc @ 1.575V and Idd @ 1.9V.

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Serial Presence-Detect

Table 12: Serial Presence-Detect EEPROM DC Operating Conditions

Parameter/Condition	Symbol	Min	Max	Units
EEPROM and AMB supply voltage	Vddspd	3.0	3.6	V
Input high voltage: Logic 1; All inputs	Vih	Vddspd × 0.7	Vddspd + 0.5	V
Input low voltage: Logic 0; All inputs	Vil	–0.6	Vddspd × 0.3	V
Output low voltage: Iout = 3mA	Vol	–	0.4	V
Input leakage current: Vin = GND to Vdd	Ili	0.10	3.0	µA
Output leakage current: Vout = GND to Vdd	Ilo	0.05	3.0	µA
Standby current	Isb	1.6	4.0	µA
Power supply current, READ: SCL clock frequency = 100 kHz	Iccr	0.4	1.0	mA
Power supply current, WRITE: SCL clock frequency = 100 kHz	Iccw	2.0	3.0	mA

Table 13: Serial Presence-Detect EEPROM AC Operating Conditions

Parameter/Condition	Symbol	Min	Max	Units	Notes
SCL LOW to SDA data-out valid	^{t}AA	0.2	0.9	µs	1
Time the bus must be free before a new transition can start	^{t}BUF	1.3	–	µs	
Data-out hold time	^{t}DH	200	–	ns	
SDA fall time	^{t}F	–	300	ns	2
SDA rise time	^{t}R	–	300	ns	2
Data-in hold time	^{t}HD:DAT	0	–	µs	
Start condition hold time	^{t}H:STA	0.6	–	µs	
Clock HIGH period	^{t}HIGH	0.6	–	µs	
Noise suppression time constant at SCL, SDA inputs	^{t}I	–	50	ns	
Clock LOW period	^{t}LOW	1.3	–	µs	
SCL clock frequency	^{f}SCL	–	400	kHz	
Data-in setup time	^{t}SU:DAT	100	–	ns	
Start condition setup time	^{t}SU:STA	0.6	–	µs	3
Stop condition setup time	^{t}SU:STO	0.6	–	µs	
WRITE cycle time	^{t}WRC	–	10	ms	4

Notes:
1. To avoid spurious start and stop conditions, a minimum delay is placed between SCL = 1 and the falling or rising edge of SDA.
2. This parameter is sampled.
3. For a restart condition or following a WRITE cycle.
4. The SPD EEPROM WRITE cycle time (^{t}WRC) is the time from a valid stop condition of a write sequence to the end of the EEPROM internal ERASE/PROGRAM cycle. During the WRITE cycle, the EEPROM bus interface circuit is disabled, SDA remains HIGH due to pull-up resistance, and the EEPROM does not respond to its slave address.

Serial Presence-Detect Data

For the latest serial presence-detect data, refer to Micron's SPD page: www.micron.com/SPD.

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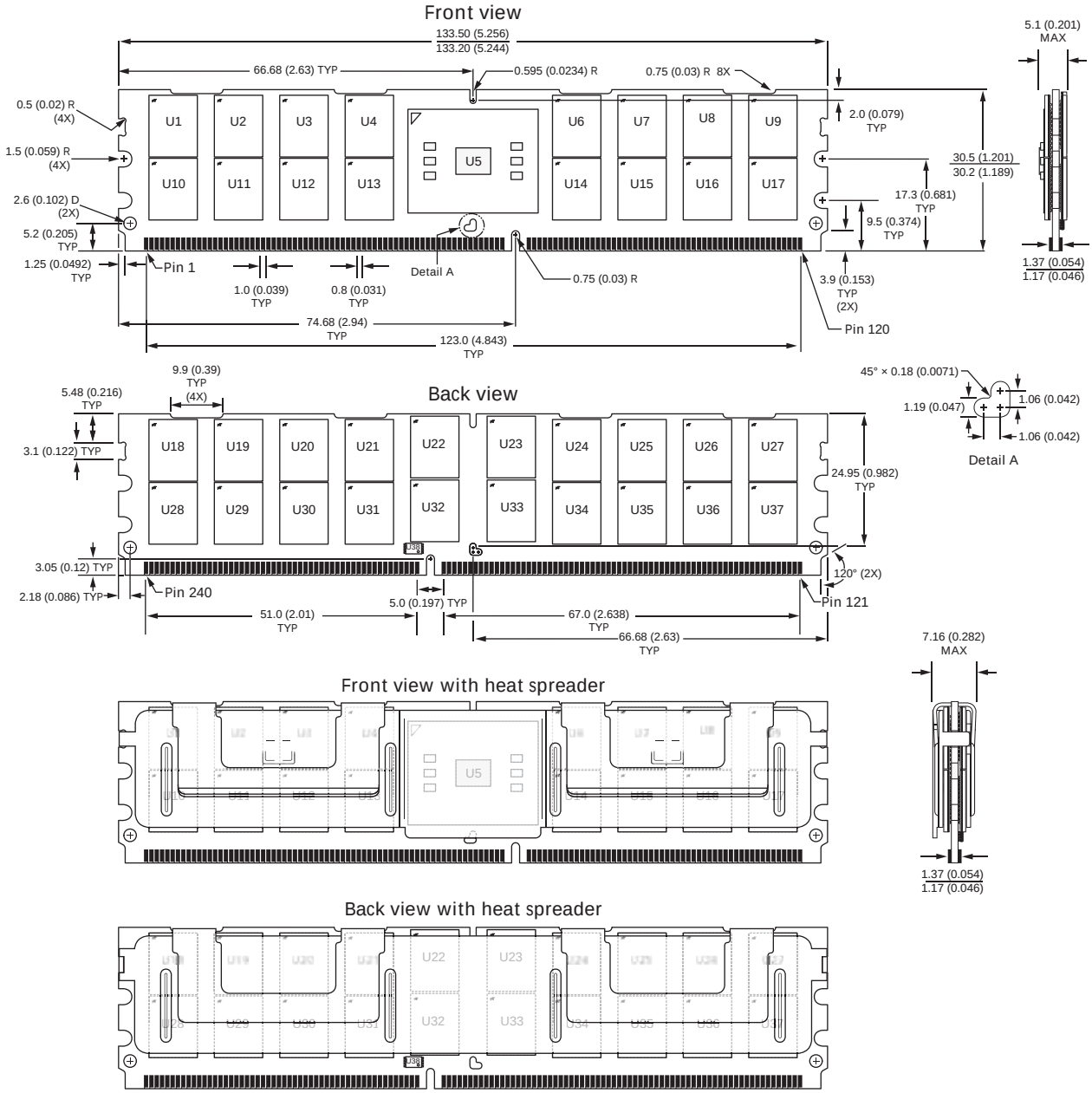
Module Dimensions

Figure 4: 240-Pin DDR2 FBDIMM



Notes:
1. All dimensions are in millimeters (inches); MAX/MIN or typical (TYP) where noted.
2. The dimensional diagram is for reference only. Refer to the JEDEC MO document for additional design dimensions.

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