

**UNITED STATES DISTRICT COURT
EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION**

NETLIST, INC.

Plaintiff,

v.

SAMSUNG ELECTRONICS CO., LTD, et al.

Defendants.

Civil Case No. 2:22cv00293-JRG
(Lead Case)

JURY TRIAL DEMANDED

NETLIST, INC.

Plaintiff,

v.

MICRON TECHNOLOGY TEXAS, LLC, et al.

Defendants.

Civil Case No. 2:22cv-00294-JRG
(Member Case)

JURY TRIAL DEMANDED

DEFENDANTS' P.R. 3-3 INVALIDITY CONTENTIONS

Pursuant to the Docket Control Order in this case (Dkt. 66), agreed amendment thereto (Dkt. 67), and Local Patent Rule 3-3, Defendants Samsung Electronics Co., Ltd. ("SEC") and Samsung Electronics America, Inc. ("SEA") and Samsung Semiconductor, Inc. ("SSI") (collectively, "Samsung") and Micron Technology, Inc., Micron Semiconductor Products, Inc., and Micron Technology Texas, LLC (collectively, "Micron") (collectively, "Defendants") hereby provide their Invalidity Contentions, which include the accompanying claim charts concerning U.S. Patent Nos. 7,619,912 ("the '912 Patent"); 9,858,215 ("the '215 patent"); and 11,093,417 ("the '417 patent") (collectively, the "Asserted Patents") to Plaintiff Netlist, Inc. ("Plaintiff" or "Netlist").

The citation of prior art herein and the accompanying exhibits are not intended to reflect Defendants' claim construction contentions, which will be disclosed in due course in accordance with the Docket Control Order and may instead reflect Plaintiff's apparent (and potentially erroneous) claim constructions based on its Infringement Contentions.

I. Introduction

As disclosed in its respective P. R. 3-1 Infringement Contentions served on Defendants, Plaintiff asserts the following patents and claims:

Patent	Claims
U.S. Patent No. 7,619,912	<u>1</u> , 3, 4, 6, 8, 10, 11, <u>15</u> , <u>16</u> , 18, 19, 20, 22, 24, 27, <u>28</u> , 29, 31, 32, 34, 36, 37, 38, <u>39</u> , 40, 41, 43, 45, 46, 47, 50, 52, 53, 54, 55, 56, 57, 58, 59, 60, 62, 63, 64, 65, 69, 70, 71, 72, 73, 74, 75, <u>77</u> , <u>80-87</u> , <u>88-89</u> , <u>90-91</u>
U.S. Patent No. 9,858,215	<u>1</u> , 2-20, <u>21</u> -29
U.S. Patent No. 11,093,417	<u>1</u> , 2-15

The claims identified above are referenced to as "the Asserted Claims" unless reference is made specifically with respect to particularly identified one or more of the Asserted Patents and/or one or more of the Asserted Claims.

As further detailed in and supported by these Invalidity Contentions, Defendants contend that each of the Asserted Claims is invalid under at least 35 U.S.C. §§ 101, 102, 103, and/or 112.¹ Defendants reserve the right to prove the invalidity of the Asserted Claims on bases other than those required to be disclosed in these disclosures pursuant to P.R. 3-3.

II. Amendment / Supplementation

Defendants' Invalidity Contentions pertain to the Asserted Claims as identified in

¹ References to Title 35 of the United States Code are to statutes prior to amendment under the America Invents Act ("AIA"), as the Asserted Patents have effective filing dates prior to applicable AIA effective dates.

Plaintiff's Infringement Contentions. To the extent the Court later allows Plaintiff to amend its infringement contentions and/or assert one or more claims other than the Asserted Claims, Defendants reserve the right to modify, amend, or supplement these Invalidity Contentions accordingly to, for example, show the invalidity of any such newly Asserted Claims.

These Invalidity Contentions are based on Defendants' current understanding of the Asserted Claims and Plaintiff's apparent view of the scope of those claims as shown, for example, in Plaintiff's Infringement Contentions. A *Markman* Order in this case has not yet been issued, and in no way shall these Invalidity Contentions be taken as any admission or acquiescence by Defendants as to the proper scope of the Asserted Claims and/or proper claim constructions of terms and phrases recited in those claims. By identifying prior art that anticipates and/or renders obvious the Asserted Claims, Defendants do not admit that the claim limitations are capable of construction, do not admit that any claim limitations are supported with an appropriate written description and enabling disclosure in the applicable patent specifications, and do not adopt Plaintiff's apparent claim constructions or admit the accuracy of any particular claim construction.² Defendants reserve all rights to later challenge or oppose any claim constructions advanced by Plaintiff and to present their own claim construction positions.

Defendants further reserve the right to revise these Invalidity Contentions in view of the Court's construction of terms and phrases recited in one or more of the Asserted Claims, additional information obtained during discovery, additional infringement theories put forth by

² Defendants do not concede that Plaintiff's apparent interpretation of the claims is correct, but rather assert the well-established principle that whatever infringes a claim if later in time anticipates if earlier in time. *Bristol-Myers Squibb Co. v. Ben Venue Labs., Inc.*, 246 F.3d 1368, 1378 (Fed. Cir. 2001). Thus, where Plaintiff for purposes of its infringement case alleges that a feature of an accused product meets a particular limitation recited in one or more of the Asserted Claims, then that feature, should it be found in the prior art, would also cause that limitation to be met for invalidity purposes.

Plaintiff during fact and/or expert discovery, any findings as to the priority date(s) of the Asserted Claims, and/or positions that Plaintiff, its fact witnesses, or its expert witness(es) may take concerning claim construction, infringement, and/or invalidity issues.

Defendants further reserve the right to supplement their accompanying P.R. 3-4(b) document production should they later discover additional prior art documents, information, testimony, prior art systems and related documentation, and/or software or hardware code, including information provided by third parties after the date of service of these Invalidity Contentions.

Defendants may further rely on inventor admissions concerning the scope or state of the prior art relevant to the Asserted Claims, the patent prosecution histories of the Asserted Patents, related patents and/or patent applications, any deposition or trial testimony of the named inventors on the Asserted Patents, and the papers filed and any evidence produced or submitted by Plaintiff in connection with these cases or other related litigation. Defendants reserve the right to contend that one or more of the Asserted Claims are invalid under 35 U.S.C. § 102(f) in the event Defendants obtain evidence that one or more of the named inventors did not invent the subject matter in the Asserted Claims.

Prior art not included in these Invalidity Contentions, whether known or not known to Defendants, may become relevant. In particular, Defendants are currently unaware of the extent, if any, to which Plaintiff will contend that limitations of the Asserted Claims are not disclosed in the prior art identified in these Invalidity Contentions. Accordingly, Defendants reserve the right to identify other references that would disclose the allegedly missing limitation(s) of the claimed method, device, or system.

The references identified in these Invalidity Contentions, which include the attached claim charts, may disclose the elements of the Asserted Claims explicitly and/or inherently, and/or they may be relied upon to show the state of the art in the relevant time frame. References identified in these Invalidity Contentions, as well as the “References Cited” on the face of the Asserted Patents and the patents cited within the body of the Asserted Patents, may be used to illustrate, but not limit the scope of, the state of the art to which the Asserted Patents pertain (i.e., at a time prior to the date of alleged inventions of the Asserted Claims of the Asserted Patents). Moreover, Defendants reserve the ability to rely on later identified sources of information, including but not limited to witness testimony and other discovery, to establish the state of the art in the relevant time frame pertaining to the Asserted Patents.

Because discovery has just recently begun, Defendants anticipate that additional prior art and invalidity bases may be found. Defendants’ investigation and analysis of the prior art is continuing, and thus Defendants reserve the right to supplement, amend, and/or revise the information provided herein as Defendants conduct further investigation and/or analysis, including identifying, charting, and relying on additional references.

Additionally, in view of likely third-party discovery that will be taken, Defendants reserve the right to present additional items of prior art under 35 U.S.C. §§ 102(a), (b), (e), and/or (g) and/or § 103 located during discovery or further investigation, and to assert contentions of invalidity under 35 U.S.C. §§ 102(c), (d), or (f). For example, Defendants expect to issue subpoenas to third parties believed to have knowledge, documents, and/or other evidence concerning invalidity of one or more of the Asserted Claims.

In addition to the positions and prior art identified in these Invalidity Contentions (including the accompanying invalidity claim charts), Defendants also incorporate by reference

all invalidity contentions, prior art,³ and invalidity claim charts (including, without limitation, all anticipation positions, obviousness positions (including all prior art combinations and motivations to combine), indefiniteness positions, written description positions, and non-enablement positions) concerning one or more of the Asserted Patents, as disclosed at any time. This includes without limitation disclosures in previous or related litigation, in United States Patent & Trademark Office (“USPTO”) proceedings, by the Plaintiff, by any other parties accused of patent infringement by the Plaintiff, or by the named inventors or any individuals associated with the prosecution and/or post-grant review of the Asserted Patents.

Specifically, for example, Defendants identify, as prior art upon which they may rely to show the invalidity of the Asserted Claims, the prior art references disclosed by parties in any other litigation (including inter partes review and/or reexamination proceedings) involving one or more of the Asserted Patents, any patent related to any of the Asserted Patents, and/or any other patent allegedly assigned to Netlist claiming priority to the Asserted Patents (collectively, “Other Netlist Proceedings”). To the extent any Defendant has stipulated or stipulates in the future that it will not pursue certain invalidity grounds in these actions concerning patent claims subject to instituted *inter partes* review proceedings, the relevant Defendant(s) will abide by those stipulation(s), and nothing in these contentions should be read as suggesting otherwise. Rather, these contentions are intended to put Plaintiff on notice of the grounds of invalidity, within the scope of P.R. 3-3, that one or more Defendants may assert in these actions, including because the conditions of any relevant stipulation are not met (*e.g.*, if the corresponding *inter partes* review is not instituted) or because the grounds fall outside the scope

³ Prior art appearing in the file histories of the Asserted Patents is not required to be separately produced by Defendants under P. R. 3-4(b).

of such stipulation(s).

Likewise, while Defendants will abide by any orders or guidance provided by the Court regarding the extent to which any stipulations preclude certain references or combinations of references, Defendants note that the law regarding whether “Admitted Prior Art” and JEDEC-related references may be used in an *inter partes* review is subject to cases pending before the Federal Circuit and the Patent Trial and Appeal Board. See Br. of Appellant Qualcomm Incorporated at 13, *Qualcomm Inc. v. Apple Inc.*, No. 23-1208 (Fed. Cir. March 20, 2023) (“Did the Board err in interpreting Section 311(b) to permit Apple’s Ground 2, which consists of so-called applicant admitted prior art (AAPA) in view one or more prior art patents or printed publications?”); Transcript of Record of Oral Hearing at 19-32, IPR2022-00062, IPR2022-00064 (P.T.A.B. March 8, 2023) (discussing whether certain JEDEC-related references constitute “printed publications”). Further developments regarding the law may impact the Court’s prior orders and guidance regarding Defendants’ stipulations.

Plaintiff has a duty to produce to Defendants all relevant documents from the Other Netlist Proceedings including but not limited to all prior art, invalidity contentions, and expert reports on invalidity (among other relevant items).

Defendants reserve the right to supplement or otherwise amend these Invalidity Contentions in response to any relevant discovery provided by third parties, Plaintiff, opening or rebuttal expert reports, fact or expert depositions, or in response to any claim construction ruling(s) issued by this Court (regardless of how and when such ruling is made). Defendants also reserve the right to supplement or otherwise amend these Invalidity Contentions in response to any rebuttal evidence disclosed by Plaintiff or as otherwise may be necessary or appropriate under the circumstances.

III. P. R. 3-3(a) – Identification of Prior Art

Pursuant to P.R. 3-3(a), and subject to Defendants’ reservation of rights, Defendants identify each item of prior art that anticipates or renders obvious the Asserted Claims below.⁴

A. U.S. Patent No. 7,619,912

Invalidity claim charts identifying disclosures in the references identified in Tables 1-A, 2-A, 3-A, and 4-A as to the Asserted Claims of the ’912 patent are provided in attached Exhibits A1 through A14.

Table 1-A: Prior Art Patents and Printed Publications for the ’912 Patent

Patent No. or Title (Primary Inventor/Author)	Date of Issue/ Publication	Filing Date
Asserted Patent’s Admitted Prior Art (“APA”)		
U.S. Patent App. Pub. No. 2006/0117152 (“Amidi”)	Jun. 1, 2006	Jan. 5, 2004
U.S. Patent App. Pub. No. 2006/0277355 (“Ellsberry”)	Dec. 7, 2006	Jun. 1, 2005
U.S. Patent No. 7,240,145 (“Holman”)	Jul. 3, 2007	Dec. 5, 1997
JEDEC Standards, including without limitation JEDEC Standard JESD79, Double Data Rate (DDR) SDRAM Specification (June 2000) (“JESD79”), JEDEC Standard JESD79-2, DDR SDRAM Specification (September 2003) (“JESD79-2”), JEDEC Standard JESD21-C, PC2100 and PC1600 DDR SDRAM Registered DIMM Design Specification (January 2002) (“JESD 21-C”), JEDEC Standard DDR SDRAM Specification, JESD79C (March 2003) (“JESD79C”)	June 2000 - September 2003	
U.S. Patent No. 7,363,422 (“Perego”)	Apr. 22, 2008	Jan. 28, 2004
U.S. Patent No. 5,926,827 (“Dell ’827”)	Jul. 20, 1999	Feb. 9, 1996

⁴ Defendants’ disclosure of prior art is premised on the alleged priority dates of the Asserted Patents as identified in Plaintiff’s infringement contentions. Defendants contend Plaintiff is not entitled to the alleged priority dates and reserve the right to modify, amend, or supplement their invalidity contentions with additional prior art references if any Asserted Claim is shown to not be entitled to the respective alleged priority date or if Plaintiff alleges any other priority date for any of the Asserted Claims. Notwithstanding that reservation of rights, Defendants also reserve the right to argue that they have been unduly prejudiced should Plaintiff allege a different priority date for any of the Asserted Claims, and that accordingly Plaintiff should not be allowed to do so.

Patent No. or Title (Primary Inventor/Author)	Date of Issue/ Publication	Filing Date
U.S. Patent No. 6,209,074 (“Dell ’074”)	Mar. 27, 2001	Apr. 28, 1998
Micron DDR SDRAM RDIMM, MT36VDDF12872 & MT36VDDF25672 Data Sheet, <i>see</i> PRIOR_ART-00338461	2002-2004	
DDR SDRAM Specification, JDEC Standard No. 79C, March 2003	Mar. 2003	
U.S. Patent No. 6,961,281 (“Wong”)	Nov. 1, 2005	Sep. 12, 2003
U.S. Patent No. 6,996, 686 (“Doblar”)	Feb. 7, 2006	Dec. 23, 2002
U.S. Patent No. 6,757,751 (“Gene”)	Jun. 29, 2004	Aug. 11, 2000
U.S. Patent No. 6,742,098 (“Halbert”)	May 25, 2004	Oct. 3, 2000
U.S. Patent No. 7,181,584 (“LaBerge”)	Feb. 20, 2007	Feb. 5, 2004
U.S. Patent No. 6,286,077 (“Choi”)	Sep. 4, 2001	Dec. 22, 1998
U.S. Patent No. 7,020,739 (“Mukaida”)	Mar. 28, 2006	Dec. 5, 2001
U.S. Patent App. Pub. No. 2007/0043922 (“Lee”)	Feb. 22, 2007	Apr. 25, 2003
U.S. Patent No. 7,414,312 (“Nguyen”)	Aug. 19, 2008	May 24, 2005

Table 2-A: Prior Art Systems and Inventions for the ’912 patent

Name of System or Invention	Date of Sale / Offer for Sale / Public Use / Known by Others
Kentron’s Quad Band Memory System (“QBM”), <i>see, e.g.</i> , PRIOR_ART-00337193; PRIOR_ART-00337196; PRIOR_ART-00337221; PRIOR_ART-00337244; PRIOR_ART-00337259; PRIOR_ART-00337830; PRIOR_ART-00337884; PRIOR_ART-00337910; PRIOR_ART-00337049; and PRIOR_ART-00337512	At least as early as 1999-2005
DDR3 Functional Outlook, <i>see, e.g.</i> , PRIOR_ART-00006576	At least as early as March 2005 (disclosed by Dr. William Wu Shen of Infineon Technologies North America Corp.)
Micron DDR SDRAM RDIMM, MT36VDDF12872 & MT36VDDF25672 Products, <i>see, e.g.</i> , PRIOR_ART-00338461	At least as early as 2002

For each of the prior art devices identified above, Defendants have listed and produced one or more documents as evidence of the relevant features and functionality. Defendants have obtained or are in the process of obtaining the identified devices and will make them available for inspection. To the extent that one or more documents (*e.g.*, user manual) may be used to

describe aspects of a particular device, that device is a single reference for prior art purposes under 35 U.S.C. § 102. Some or all of the corroborating references may also separately qualify as prior art publications under 35 U.S.C. § 102 and may be used as invalidating references under 35 U.S.C. §§ 102 and/or 103.

Further, Defendants are actively searching for information regarding at least the following devices and inventions:

- Kentron's Quad Band Memory System

Discovery is ongoing, and Defendants may serve third parties with document subpoenas. One or more of these devices, along with related documentation, may be invalidating, and Defendants reserve the right to supplement these contentions accordingly.

In addition, Defendants identify, responsive to Plaintiff's infringement contentions, the following patents, publications, and systems as evidence of the state of the art as it relates to memory modules:

- JEDEC Standards, including without limitation JEDEC Standard JESD79, Double Data Rate (DDR) SDRAM Specification (June 2000) ("JESD79"), JEDEC Standard JESD79-2, DDR SDRAM Specification (September 2003) ("JESD79-2"), JEDEC Standard JESD21-C, PC2100 and PC1600 DDR SDRAM Registered DIMM Design Specification (January 2002) ("JESD 21-C"), JEDEC Standard DDR SDRAM Specification, JESD79C (March 2003) ("JESD79C")
- U.S. Patent App. Pub. No. 20060117152 ("Amidi")
- U.S. Patent App. Pub. No. 2006/0277355 ("Ellsberry")
- U.S. Patent No. 7,240,145 ("Holman")

- U.S. Patent No. 7,363,422 (“Perego ’422”)
- U.S. Patent No. 5,926,827 (“Dell ’827”)
- U.S. Patent No. 6,209, 074 (“Dell ’074”)
- Micron DDR SDRAM RDIMM, MT36VDDF12872 & MT36VDDF25672 Product (“Micron RDIMM”)
- DDR SDRAM Specification, JEDEC Standard No. 79C, March 2003
- U.S. Patent No. 6,961,281 (“Wong”)
- U.S. Patent No. 6,996, 686 (“Doblar”)
- U.S. Patent No. 6,757,751 (“Gene”)
- U.S. Patent No. 6,742,098 (“Halbert”)
- U.S. Patent No. 7,181,584 (“LaBerge”)
- U.S. Patent No. 6,286,077 (“Choi”)
- U.S. Patent No. 7,020,739 (“Mukaida”)
- U.S. Patent App. Pub. No. 2007/0043922 (“Lee”)
- U.S. Patent No. 7,414,312 (“Nguyen”)
- DDR3 Functional Outlook

Each of these references show that the concept of “rank multiplication” is not novel and was well-known for many years before the alleged priority date of the ’912 patent. In light of the references discussed herein, the Asserted Claims of the ’912 patent cannot be valid.

Defendants continue to investigate each of the identified devices, including through potential discovery needed to be obtained via third party subpoenas, and reserve the right to supplement these contentions and accompanying claim charts after further investigation.

Defendants' reference to a particular product, device, or software program in these contentions should be interpreted as a reference to the system itself and any corresponding patents, publications, or product literature relating to the cited system. Upon information and belief, the systems were publicly disclosed, used, sold, or offered for sale in the United States before the alleged priority date of the Asserted Claims of the '912 patent. Defendants' investigation of such prior art systems is still ongoing and discovery has not yet been received from third parties who may have information concerning such prior art systems. Accordingly, subsequent discovery may reveal information that affects the disclosures and contentions herein. For example, subsequent discovery may provide additional information regarding whether or not any of the third party prior art systems anticipate or render obvious the Asserted Claims of the '912 patent. As such, Defendants reserve all rights to supplement their invalidity contentions.

Many of the inventive, research, design, and development activities concerning these systems and technologies occurred in the United States before the alleged priority date of the Asserted Claims of the '912 patent. Defendants have obtained, and are in the process of obtaining, additional information regarding the dates by which the cited products and services were publicly disclosed, used, sold, or offered for sale, the circumstances under which the research, design, and development activities were conducted, and the identities of the particular individuals involved in such activities through publicly available patents, publications, and product literature. The actual dates, circumstances, and identities of individuals will be the subject of third party discovery during this lawsuit, which Defendants reserve the right to rely upon to corroborate the prior art status of the prior art identified herein. Defendants reserve the right to modify, amend, or supplement these contentions if additional information becomes

available during the course of this lawsuit. Furthermore, Defendants will make all such devices, software programs, or other products in Defendants' possession, custody, or control available for inspection by Plaintiff.

Consequently, Defendants reserve the right to amend, modify, or supplement these Invalidity Contentions should additional information become available to them through discovery.

Table 3-A provides additional bases for invalidity of the '912 patent under pre-AIA 35 U.S.C. § 102(f), on the grounds that the inventors of the '912 patent did not themselves invent the subject matter claimed in the '912 patent. The prior art under § 102(f) is identified in Table 3 by the name of the person(s) from whom the invention was derived. The circumstances under which the invention was derived are explained below.

Table 3-A: Prior Art under pre-AIA § 102(f) for the '912 patent

Prior Art Disclosing Technical Features	Name of Person(s) from Whom Invention was Derived
Kentron's Quad Band Memory System ("QBM")	Kentron Technologies Inc. employee(s) (<i>e.g.</i> , Chris Karabatsos, Vasilios Karabatsos, Bob Goodman, Badawi Dweik)
Proposals and disclosures made at JEDEC committee meetings during the time period 2001-2005 (" <i>JEDEC Proposals</i> ")	Entities and persons attending JEDEC committee meetings where related technology was discussed (including the JC-45 committee meetings). For example: • One or more employees of Elpida • One or more employees of Micron • One or more employees of Infineon • One or more employees of Agilent • One or more employees of IBM

QBM

Between at least 1999 and 2004, Kentron Technologies Inc. ("Kentron") invented and developed memory modules based on its Quad Band Memory ("QBM") technology, including

before the earliest alleged priority date of the '912 patent. During this time period, Kentron formed the QBM Alliance, an alliance of technology partners aimed at positioning QBM as an industry standard. *See, e.g.*, PRIOR_ART-00337960; PRIOR_ART-337961; PRIOR_ART-00337964. The technical details of the QBM system were regularly disclosed to QBM Alliance members during this time period. *See, e.g.*, PRIOR_ART-00337989; PRIOR_ART-00337991. Netlist became a QBM Alliance member in February 2002. *See, e.g.*, PRIOR_ART-00337966, PRIOR_ART-00337987; PRIOR_ART-00337995; PRIOR_ART-00338026. Because it was a QBM Alliance member, Netlist knew about the technical features of the QBM system and derived the claimed subject matter of the '912 patent from the QBM features. The technical features of QBM are shown in the following documents: PRIOR_ART-00337136- PRIOR_ART-00337259. The invalidity claim chart identifying disclosures from these documents as to the Asserted Claims of the '912 patent is provided in attached Exhibit A11.

JEDEC Proposals

Netlist was a member of JEDEC since February 2001 and Mr. Jayesh R. Bhakta, named inventor of the '912 patent, served as Netlist's representative to JEDEC. On information and belief, Netlist's members, including Mr. Bhakta, regularly attended JEDEC meetings for at least the JC-45 committee prior to the priority date of the '912 patent.

By virtue of his attendance at those meetings, active involvement in JEDEC and otherwise, Mr. Bhakta was aware of JEDEC presentations prior to the priority date for the '912 patent such as those related to Fully Buffered DIMM (FBDIMM) presented at the March 8-9, 2005 meeting of JC-45, which Mr. Bhakta attended.

Draft specifications, ballots and presentations distributed to the members of the JC-45 committees of JEDEC were distributed to many (20+) key members of the interested public with the expectation they would be freely disclosed to and discussed with others.

After attending the March 8-9, 2005 meeting and listening to these ideas from other members of JEDEC, Mr. Bhakta returned to Netlist and drafted non-provisional application no. 11/173,175, which provides the earliest possible priority date for the '912 patent given the many deficiencies in the earlier non-provisional and provisional patent disclosures.

Table 4 below provides additional bases for invalidity of the '912 patent under pre-AIA 35 U.S.C. § 102(g)(2), on the grounds that the alleged invention of the '912 patent was made in this country before the alleged invention date of the '912 patent by another inventor who had not abandoned, suppressed, or concealed it. The prior art under § 102(g)(2) is identified in Table 4 by the name of the person(s) or entities involved in the making of the invention before the applicants of the '912 patent. The circumstances surrounding the making of the invention before the applicants of the '912 patent are explained below.

Table 4-A: Prior Art under pre-AIA § 102(g)(2) for the '912 patent

Prior Art Disclosing Technical Features	Person(s)/Entity(ies) Involved
Kentron's Quad Band Memory System ("QBM")	Kentron Technologies Inc. employee(s) (<i>e.g.</i> , Chris Karabatsos, Vasilios Karabatsos, Bob Goodman, Badawi Dweik)
Proposals and disclosures made at JEDEC committee meetings during the time period 2001-2005 (" <i>JEDEC Proposals</i> ")	Entities and persons attending JEDEC committee meetings where related technology was discussed (including the JC-45 committee meetings). For example: • One or more employees of Elpida • One or more employees of Micron • One or more employees of Infineon • One or more employees of Agilent • One or more employees of IBM

QBM

Between at least 1999 and 2005, Kentron Technologies Inc. (“Kentron”) invented and developed memory modules based on its Quad Band Memory (“QBM”) technology, including before the earliest alleged priority date of the ’912 patent. During this time, Kentron formed the QBM Alliance, an alliance of technology partners aimed at positioning QBM as an industry standard. *See, e.g.*, PRIOR_ART-00337960; PRIOR_ART-337961; PRIOR_ART-00337964. The technical details of the QBM system were regularly disclosed to QBM Alliance members during this time period. *See, e.g.*, PRIOR_ART-00337989; PRIOR_ART-00337991. Netlist became a QBM Alliance member in February 2002. *See, e.g.*, PRIOR_ART-00337966, PRIOR_ART-00337987; PRIOR_ART-00337995; PRIOR_ART-00338026. Because it was a QBM Alliance member, Netlist knew about the technical features of the QBM system and used the technical features of the QBM system to draft the provisional application to which the ’912 patent claims priority as well as the claims of the ’912 patent. The technical features of QBM are shown in the following documents: PRIOR_ART-00337136-PRIOR_ART-00337259. The invalidity claim chart identifying disclosures from these documents as to the Asserted Claims of the ’912 patent is provided in attached Exhibit A11. Kentron did not abandon, suppress, or conceal its invention of QBM. Kentron presented the technical features of QBM to JEDEC, described the features in newsletters to its QBM Alliance members, and filed patents covering the technology. *See, e.g.*, PRIOR_ART-00338011, PRIOR_ART-00338024.

JEDEC Proposals

Netlist was a member of JEDEC since February 2001 and Mr. Jayesh R. Bhakta, named inventor of the ’912 patent, served as Netlist’s representative to JEDEC. On information and

belief, Netlist's members, including Mr. Bhakta, regularly attended JEDEC meetings for at least the JC-45 committee prior to the priority date of the '912 patent.

By virtue of his attendance at those meetings, active involvement in JEDEC and otherwise, Mr. Bhakta was aware of JEDEC presentations prior to the priority date for the '912 patent such as those related to Fully Buffered DIMM (FBDIMM) presented at the March 8-9, 2005 meeting of JC-45, which Mr. Bhakta attended.

Draft specifications, ballots and presentations distributed to the members of the JC-45 committees of JEDEC were distributed to many (20+) key members of the interested public with the expectation they would be freely disclosed to and discussed with others.

After attending the March 8-9, 2005 meeting and listening to these ideas from other members of JEDEC, Mr. Bhakta returned to Netlist and drafted non-provisional application no. 11/173,175, which provides the earliest possible priority date for the '912 patent given the many deficiencies in the earlier non-provisional and provisional patent disclosures.

With discovery ongoing, Defendants reserve the right to amend, modify, or supplement these Invalidity Contentions with additional 35 U.S.C. §102(f) and/or (g) allegations should additional information become available through discovery supporting such allegations.

B. U.S. Patent Nos. 9,858,215 and 11,093,417

Invalidity claim charts identifying disclosures in the references identified in Tables 1-B, 2-B, 3-B, and 4-B as to the Asserted Claims of the '215 and '417 patents are provided in attached Exhibits B1 through B21 (the '215 Patent) and Exhibits C1 through C18 (the '417 Patent).

Table 1-B: Prior Art Patents and Printed Publications for the '215 and '417 Patents

Patent No. or Title (Primary Inventor/Author)	Date of Issue/ Publication	Filing Date
The '215 Patent's Admitted Prior Art ("APA")		

Patent No. or Title (Primary Inventor/Author)	Date of Issue/ Publication	Filing Date
U.S. Patent Application Publication No. 2003/0204688 (“Lee ’688”)	10/30/2003	4/25/2003
U.S. Patent Application Publication No. 2006/0117152 (“Amidi”)	6/1/2006	1/5/2004
U.S. Patent Application Publication No. 2003/0145156 (“Khandekar”)	7/31/2003	1/28/2002
U.S. Patent No. 6,862,653 (“Dodd”)	3/1/2005	9/18/2000
U.S. Patent Application Publication No. 2003/0117864 (“Hampel”)	6/26/2003	10/22/2002
U.S. Patent No. 7,240,145 (“Holman”)	7/3/2007	2/28/2006
U.S. Patent No. 6,757,751 (“Gene”)	6/29/2004	8/11/2000
U.S. Patent No. 6,961,281 (“Wong ’281”)	11/1/2005	9/12/2003
U.S. Patent Application Publication No. 2002/0112119 (“Halbert ’119”)	8/15/2002	3/13/2002
JEDEC Standards, including without limitation JEDEC Standard JESD79, Double Data Rate (DDR) SDRAM Specification (June 2000) (“JESD79”), JEDEC Standard JESD79-2, DDR SDRAM Specification (September 2003) (“JESD79-2”), JEDEC Standard JESD21-C, PC2100 and PC1600 DDR SDRAM Registered DIMM Design Specification (January 2002) (“JESD 21-C”), JEDEC Standard DDR SDRAM Specification, JESD79C (March 2003) (“JESD79C”)	June 2002-March 2003	
FBDIMM Architecture & Protocol, including without limitation FB-DIMM Draft Specification: Architecture & Protocol, Revision 0.0 (“ <i>FBDIMM AP Rev. 0.0</i> ”) (December 3, 2003) and FB-DIMM Draft Specification: Architecture & Protocol, Revision 0.1 (“ <i>FBDIMM AP Rev. 0.1</i> ”) (February 13, 2004)	12/3/2003-2/13/2004	
U.S. Patent No. 6,205,062 (“Kim ’062”)	3/20/2001	11/9/1999
U.S. Patent No. 6,262,938 (“Lee ’938”)	7/17/2001	3/3/2000
U.S. Patent No. 6,392,909 (“Jang”)	5/21/2002	5/27/2001
U.S. Patent No. 6,529,423 (“Yoon”)	3/4/2003	2/22/2000
U.S. Patent No. 6,564,287 (“Lee ’287”)	5/13/2003	9/5/2000
U.S. Patent No. 7,289,383 (“Cornelius”)	10/30/2007	8/23/2004
U.S. Patent No. 7,433,258 (“Rao”)	10/7/2008	10/8/2004
U.S. Patent No. 5,581,498 (“Ludwig”)	12/3/1996	10/20/1994
U.S. Patent No. 5,712,811 (“Kim ’811”)	1/27/1998	1/6/1996
U.S. Patent No. 5,926,827 (“Dell ’827”)	7/20/1999	2/9/1996
U.S. Patent No. 6,414,868 (“Wong ’868”)	7/2/2002	6/7/1999

Patent No. or Title (Primary Inventor/Author)	Date of Issue/ Publication	Filing Date
U.S. Patent No. 6,446,184 (“Dell ’184”)	9/3/2002	1/30/2001
U.S. Patent No. 6,493,250 (“Halbert ’250”)	12/10/2002	12/28/2000
U.S. Patent No. 6,529,993 (“Rogers”)	3/4/2003	10/12/2000
U.S. Patent No. 6,615,345 (“LaBerge ’345”)	9/2/2003	7/29/1999
U.S. Patent No. 6,820,163 (“McCall”)	11/16/2004	9/18/2000
U.S. Patent No. 7,334,150 (“Ruckerbauer”)	2/19/2008	12/3/2004
U.S. Patent No. 7,024,518 (“Halbert ’518”)	4/4/2006	3/13/2002
U.S. Patent No. 7,043,617 (“Williams ’617”)	5/9/2006	2/22/2000
U.S. Patent No. 7,092,299 (“Kwak”)	8/15/2006	5/3/2004
U.S. Patent No. 7,149,841 (“LaBerge ’841”)	12/12/2006	3/31/2003
U.S. Patent No. 7,206,896 (“Perego ’896”)	4/17/2007	4/29/2005
U.S. Patent No. 7,212,424 (“Johnson ’424”)	5/1/2007	5/21/2005
U.S. Patent No. 7,222,224 (“Woo”)	5/22/2007	5/21/2004
U.S. Patent No. 7,363,422 (“Perego ’422”)	4/22/2008	1/28/2004
U.S. Patent No. 7,366,827 (“Lee ’827”)	4/29/2008	4/25/2003
U.S. Patent Application Publication No. 2001/0008006 (“Klein”)	6/12/2001	2/13/2001
U.S. Patent Application Publication No. 2002/0118578 (“Janzen ’578”)	8/29/2002	2/23/2001
U.S. Patent Application Publication No. 2002/0188816 (“Johnson ’816”)	12/12/2002	6/6/2001
U.S. Patent Application Publication No. 2003/0039151 (“Matsui ’151”)	2/27/2003	8/23/2002
U.S. Patent Application Publication No. 2003/0133331 (“LaBerge ’331”)	7/17/2003	1/14/2002
U.S. Patent Application Publication No. 2004/0034755 (“LaBerge ’755”)	2/19/2004	8/16/2002
U.S. Patent Application Publication No. 2005/0050255 (“Jeddeloh”)	3/5/2005	8/28/2003
U.S. Patent Application Publication No. 2005/0198449 (“Haskell”)	9/8/2005	3/5/2004
U.S. Patent Application Publication No. 2005/0257109 (“Averbuj”)	11/17/2005	7/29/2003
U.S. Patent Application Publication No. 2006/0195631 (“Rajamani”)	8/31/2006	1/31/2005
U.S. Patent Application Publication No. 2006/0277355 (“Ellsberry”)	12/7/2006	6/1/2005
Micron DDR SDRAM RDIMM, MT36VDDF12872 & MT36VDDF25672 Data Sheet, see PRIOR_ART-00338461	2002-2004	
Synchronous DRAM Architectures, Organizations, and Alternative Technologies (Bruce Jacob)	12/10/2002	
The ’417 Patent’s Admitted Prior Art (“APA”)		

Patent No. or Title (Primary Inventor/Author)	Date of Issue/ Publication	Filing Date
U.S. Patent No. 7,103,742 (“Mailloux”)	9/5/2006	12/3/1997
U.S. Patent No. 6,851,032 (“LaBerge ’032”)	2/1/2005	8/16/2002
U.S. Patent No. 6,154,821 (“Barth”)	11/28/2000	3/10/1998
U.S. Patent No. 6,226,755 (“Reeves”)	5/1/2001	1/26/1999
U.S. Patent No. 6,742,098 (“Halbert ’098”)	5/25/2004	10/3/2000
U.S. Patent No. 6,940,782 (“Matsui ’782”)	9/6/2005	6/13/2003
U.S. Patent No. 7,196,948 (“Vemula”)	3/27/2007	3/7/2005
U.S. Patent Application Publication No. 2002/0133666 (“Janzen ’666”)	9/19/2002	3/13/2001
U.S. Patent Application Publication No. 2004/0103258 (“Blockmon”)	5/27/2004	11/27/2002
U.S. Patent Application Publication No. 2004/0260864 (“Lee ’864”)	12/23/2004	6/19/2003
U.S. Patent Application Publication No. 2005/0044304 (“James”)	2/24/2005	8/20/2003
International Patent Application Publication No. WO 96/020446 (“Williams ’446”)	7/4/1996	12/22/1995
International Patent Application Publication No. WO 01/037090 (“Wong ’090”)	5/25/2001	11/15/2000
DDR SDRAM RDIMM Design Specification JEDEC Standard 21-C (4.20.4) (“JEDEC Standard 21-C”)	January 2002	
DDR2 SDRAM Specification JEDEC Standard JESD79-2A (“JESD79-2A”)	January 2004	
U.S. Patent. No. 7,155,627 (“Matsui ’627”)	12/26/2006	8/22/2003
U.S. Patent Application Publication No. 2021/0149829 (“Lee ’829”)	5/20/2021	12/7/2020

Table 2-B: Prior Art Systems and Inventions for the ’215 and ’417 Patents

Name of System or Invention	Date of Sale / Offer for Sale / Public Use / Known by Others
Kentron’s Quad Band Memory System (“QBM”), <i>see, e.g.</i> , PRIOR_ART-00337193; PRIOR_ART-00337196; PRIOR_ART-00337221; PRIOR_ART-00337244; PRIOR_ART-00337259; PRIOR_ART-00337830; PRIOR_ART-00337884; PRIOR_ART-00337910; PRIOR_ART-00337049; and PRIOR_ART-00337512	At least as early as 1999-2005 (sale and/or offer for sale made by Kentron)
DDR3 Functional Outlook, <i>see, e.g.</i> , PRIOR_ART-00006576	At least as early as March 2005 (disclosed by Dr. William Wu Shen of Infineon Technologies North America Corp.)

Name of System or Invention	Date of Sale / Offer for Sale / Public Use / Known by Others
Micron DDR SDRAM RDIMM, MT36VDDF12872 & MT36VDDF25672 Products, <i>see, e.g.</i> , PRIOR_ART-00338461	At least as early as 2002

For each of the prior art devices identified above, Defendants have listed and produced one or more documents as evidence of the relevant features and functionality. Defendants have obtained or are in the process of obtaining the identified devices and will make them available for inspection. To the extent that one or more documents (*e.g.*, user manual) may be used to describe aspects of a particular device, that device is a single reference for prior art purposes under 35 U.S.C. § 102. Some or all of the corroborating references may also separately qualify as prior art publications under 35 U.S.C. § 102 and may be used as invalidating references under 35 U.S.C. §§ 102 and/or 103.

Further, Defendants are actively searching for information regarding at least the following devices and inventions:

- Kentron’s Quad Band Memory System (“QBM”)

Discovery is ongoing, and Defendants may serve third parties with document subpoenas. One or more of these devices, along with related documentation, may be invalidating, and Defendants reserve the right to supplement these contentions accordingly.

In addition, Defendants identify, responsive to Plaintiff’s infringement contentions, the following patents, publications, and systems as examples of evidence of the state of the art as it relates to memory modules:

- U.S. Patent No. 7,363,422 (“Perego ’422”);
- U.S. Patent Application Publication No. 2006/0277355 (“Ellsberry”);
- U.S. Patent No. 7,024,518 (“Halbert ’518”);

- U.S. Patent. No. 7,155,627 (“Matsui ’627”);
- U.S. Patent Application Publication No. 2003/0039151 (“Matsui 151”);
- JEDEC JESD79 standard for DDR SDRAM (June 2000) (“JESD79”);
- JEDEC JESD21-C design specification for DDR SDRAM Registered DIMM (January 2002) (“JESD Standard 21-C”);
- JEDEC JESD79-2 standard for DDR2 SDRAM (Sept. 2003) (“JESD79-2”);
- JEDEC JESD21-C Design Specification for DDR2 SDRAM Registered DIMM, Rev. 3.2 (Oct. 4, 2005);
- Micron DDR SDRAM RDIMM, MT36VDDF12872 & MT36VDDF25672 Product (“Micron RDIMM”)
- DDR3 Functional Outlook
- Harold S. Stone, *Microcomputer Interfacing* (1982);
- Bruce Jacob, *Synchronous DRAM Architectures, Organizations, and Alternative Technologies* (Dec. 10, 2002);

Each of these references show that the concept of incorporating data buffers with multiple memory ranks and/or CAS latency is not novel. Indeed, these concepts have been well-known for many years before the alleged priority date(s) of the ’215 and ’417 patents. In light of the references discussed herein, the asserted claims of the Asserted Patents cannot be valid.

Defendants continue to investigate each of the identified devices, including through potential discovery needing to be obtained via third party subpoenas, and reserve the right to supplement these contentions and accompanying claim charts after further investigation.

Defendants’ reference to a particular product, device, or software program in these contentions should be interpreted as a reference to the system itself and any corresponding

patents, publications, or product literature relating to the cited system. Upon information and belief, the systems were publicly disclosed, used, sold, or offered for sale in the United States before the alleged priority date of the Asserted Claims of the '215 and '417 patents. Defendants' investigation of such prior art systems is still ongoing and discovery has not yet been received from third parties who may have information concerning such prior art systems. Accordingly, subsequent discovery may reveal information that affects the disclosures and contentions herein. For example, subsequent discovery may provide additional information regarding whether or not any of the third party prior art systems anticipate or render obvious the Asserted Claims of the '215 and '417 patents. As such, Defendants reserve all rights to supplement their invalidity contentions.

Many of the inventive, research, design, and development activities concerning these systems and technologies occurred in the United States before the alleged priority date of the Asserted Claims of the '215 and '417 patents. Defendants have obtained, and are in the process of obtaining, additional information regarding the dates by which the cited products and services were publicly disclosed, used, sold, or offered for sale, the circumstances under which the research, design, and development activities were conducted, and the identities of the particular individuals involved in such activities through publicly available patents, publications, and product literature. The actual dates, circumstances, and identities of individuals will be the subject of third party discovery during this lawsuit, which Defendants reserve the right to rely upon to corroborate the prior art status of the prior art identified herein. Defendants reserve the right to modify, amend, or supplement these contentions if additional information becomes available during the course of this lawsuit. Furthermore, Defendants will

make all such devices, software programs, or other products in Defendants’ possession, custody, or control available for inspection by Plaintiff.

Consequently, Defendants reserve the right to amend, modify, or supplement these Invalidity Contentions should additional information become available to them through discovery.

Table 3-B provides additional bases for invalidity of the ’215 and ’417 patents under pre-AIA 35 U.S.C. § 102(f), on the grounds that the inventors of the ’215 and ’417 patents did not themselves invent the subject matter claimed in the ’215 and ’417 patents. The prior art under § 102(f) is identified in Table 3-B by the name of the person(s) from whom the invention was derived. The circumstances under which the invention was derived are explained below.

Table 3-B: Prior Art under pre-AIA § 102(f) for the ’215 and ’417 patents

Prior Art Disclosing Technical Features	Name of Person(s) from Whom Invention was Derived
Kentron’s Quad Band Memory System (“QBM”)	Kentron Technologies Inc. employee(s) (e.g., Chris Karabatsos, Vasilios Karabatsos, Bob Goodman, Badawi Dweik)
Proposals and disclosures made at JEDEC committee meetings during the time period 2001-2005 (“JEDEC Proposals”)	Entities and persons attending JEDEC committee meetings where related technology was discussed (including the JC-45 committee meetings). For example: • One or more employees of Elpida • One or more employees of Micron • One or more employees of Infineon • One or more employees of Agilent • One or more employees of IBM

QBM

Between at least 1999 and 2004, Kentron Technologies Inc. (“Kentron”) invented and developed memory modules based on its Quad Band Memory (“QBM”) technology, including before the earliest alleged priority date of the ’215 and ’417 patents. During this time period,

Kentron formed the QBM Alliance, an alliance of technology partners aimed at positioning QBM as an industry standard. *See, e.g.,* PRIOR_ART-00337960; PRIOR_ART-337961; PRIOR_ART-00337964. The technical details of the QBM system were regularly disclosed to QBM Alliance members during this time period. *See, e.g.,* PRIOR_ART-00337989; PRIOR_ART-00337991. Netlist became a QBM Alliance member in February 2002. *See, e.g.,* PRIOR_ART-00337966, PRIOR_ART-00337987; PRIOR_ART-00337995; PRIOR_ART-00338026. Because it was a QBM Alliance member, Netlist knew about the technical features of the QBM system and derived the claimed subject matter of the '215 and '417 patents from the QBM features. The technical features of QBM are shown in the following documents: PRIOR_ART-00337136-PRIOR_ART-00337259. The invalidity claim charts identifying disclosures from these documents as to the Asserted Claims of the '215 and '417 patents is provided in attached Exhibit B7 and C7.

JEDEC Proposals

Netlist was a member of JEDEC since February 2001 and Mr. Jayesh R. Bhakta, named inventor of the '215 and 417 patent, served as Netlist's representative to JEDEC. On information and belief, Netlist's members, including Mr. Bhakta, regularly attended JEDEC meetings for at least the JC-45 committee prior to the priority date of the '215 and '417 patents.

By virtue of his attendance at those meetings, active involvement in JEDEC and otherwise, Mr. Bhakta was aware of JEDEC presentations prior to the respective priority dates for the '215 and 417 patent such as those related to Fully Buffered DIMM (FBDIMM) presented at the March 8-9, 2005 meeting of JC-45, which Mr. Bhakta attended.

Draft specifications, ballots and presentations distributed to the members of the JC-45 committees of JEDEC were distributed to many (20+) key members of the interested public with

the expectation they would be freely disclosed to and discussed with others. After attending the March 8-9, 2005 meeting and listening to these ideas from other members of JEDEC, Mr. Bhakta returned to Netlist and drafted non-provisional application no. 11/173,175, which provides the earliest possible priority date for the '215 and 417 patents given the many deficiencies in the earlier non-provisional and provisional patent disclosures.

Table 4-B below provides additional bases for invalidity of the '215 and '417 patents under pre-AIA 35 U.S.C. § 102(g)(2), on the grounds that the alleged inventions of the '215 and '417 patents were made in this country before the alleged invention date of the '215 and '417 patents by another inventor who had not abandoned, suppressed, or concealed it. The prior art under § 102(g)(2) is identified in Table 4-B by the name of the person(s) or entities involved in the making of the invention before the applicants of the '215 and '417 patents. The circumstances surrounding the making of the invention before the applicants of the '215 and '417 patents are explained below.

Table 4-B: Prior Art under pre-AIA § 102(g)(2) for the '215 and '417 Patents

Prior Art Disclosing Technical Features	Person(s)/Entity(ies) Involved
Quad Band Memory ("QBM") System ("QBM")	Kentron Technologies Inc. employee(s) (e.g., Chris Karabatsos, Vasilios Karabatsos, Bob Goodman, Badawi Dweik)
Proposals and disclosures made at JEDEC committee meetings during the time period 2001-2005 (" <i>JEDEC Proposals</i> ")	Entities and persons attending JEDEC committee meetings where related technology was discussed (including the JC-45 committee meetings). For example: • One or more employees of Elpida • One or more employees of Micron • One or more employees of Infineon • One or more employees of Agilent • One or more employees of IBM

QBM

Between at least 1999 and 2005, Kentron Technologies Inc. (“Kentron”) invented and developed memory modules based on its Quad Band Memory (“QBM”) technology, including before the earliest alleged priority date of the ’215 and ’417 patents. During this time, Kentron formed the QBM Alliance, an alliance of technology partners aimed at positioning QBM as an industry standard. *See, e.g.*, PRIOR_ART-00337989; PRIOR_ART-00337991. Netlist became a QBM Alliance member in February 2002. *See, e.g.*, PRIOR_ART-00337966, PRIOR_ART-00337987; PRIOR_ART-00337995; PRIOR_ART-00338026. Because it was a QBM Alliance member, Netlist knew about the technical features of the QBM system and used the technical features of the QBM system to draft the provisional application to which the ’912 patent claims priority as well as the claims of the ’215 and ’417 patents. The technical features of QBM are shown in the following documents: PRIOR_ART-00337136-PRIOR_ART-00337259. The invalidity claim charts identifying disclosures from these documents as to the Asserted Claims of the ’215 and ’417 patents are provided in attached Exhibit B7 and C7. Kentron did not abandon, suppress, or conceal its invention of QBM. Kentron presented the technical features of QBM to JEDEC, described the features in newsletters to its QBM Alliance members, and filed patents covering the technology. *See, e.g.*, PRIOR_ART-00338011, PRIOR_ART-00338024.

JEDEC Proposals

Netlist was a member of JEDEC since February 2001 and Mr. Jayesh R. Bhakta, named inventor of the ’215 and 417 patent, served as Netlist’s representative to JEDEC. On

information and belief, Netlist's members, including Mr. Bhakta, regularly attended JEDEC meetings for at least the JC-45 committee prior to the priority date of the '215 and '417 patents.

By virtue of his attendance at those meetings, active involvement in JEDEC and otherwise, Mr. Bhakta was aware of JEDEC presentations prior to the respective priority dates for the '215 and 417 patent such as those related to Fully Buffered DIMM (FBDIMM) presented at the March 8-9, 2005 meeting of JC-45, which Mr. Bhakta attended.

Draft specifications, ballots and presentations distributed to the members of the JC-45 committees of JEDEC were distributed to many (20+) key members of the interested public with the expectation they would be freely disclosed to and discussed with others.

After attending the March 8-9, 2005 meeting and listening to these ideas from other members of JEDEC, Mr. Bhakta returned to Netlist and drafted non-provisional application no. 11/173,175, which provides the earliest possible priority date for the '215 and 417 patents given the many deficiencies in the earlier non-provisional and provisional patent disclosures. With discovery ongoing, Defendants reserve the right to amend, modify, or supplement these Invalidity Contentions with additional 35 U.S.C. §102(f) and/or (g) allegations should additional information become available through discovery supporting such allegations.

IV. P. R. 3-3(b) – Invalidity Grounds

Pursuant to P.R. 3-3(b), Defendants contend that certain prior art references below anticipate one or more Asserted Claims and that to the extent the identified prior art references do not anticipate the Asserted Claims, those claims are invalid as obvious under 35 U.S.C. §103. Each anticipatory prior art reference, either alone or in combination with other prior art, also renders the Asserted Claims invalid as obvious. In particular, each anticipatory prior art reference may be combined with (1) information generally known to persons skilled in the art at

the time of the alleged invention, and/or (2) any of the other anticipatory prior art references. To the extent that Plaintiff contends that any of the anticipatory prior art fails to disclose one or more limitations of the Asserted Claims, Defendants contend that any difference between the reference and the corresponding patent claims would have been obvious to one of ordinary skill in the art. Thus, all anticipation charts should be interpreted as both reflecting anticipation by the reference as well as invalidity due to single reference obviousness, to the extent that Plaintiff contends that any limitation is missing.

A. Anticipation

As stated above, Defendants incorporate by reference all other invalidity contentions related to the Asserted Patents served on or otherwise provided to Plaintiff, whether past or future. In accordance with P.R. 3-3(a), prior art references anticipating the Asserted Claims are provided below. The prior art listed below anticipates the Asserted Claims under the proper construction of the claims and/or under Plaintiff's apparent interpretation of the claims as set forth by Plaintiff in its Complaint and Infringement Contentions.

1. U.S. Patent No. 7,619,912

The Asserted Claims of the '912 patent are anticipated and/or rendered obvious by prior art. Pursuant to P.R. 3-3(a), Defendants identify the prior art references that anticipate or render obvious the '912 patent Asserted Claims in the claim charts of Exhibits A1 through A14 (collectively "Appendix A") which are hereby incorporated by reference as if fully set forth herein. The claim charts of Appendix A provide an explanation showing how these prior art references teach or suggest each and every element of the '912 patent Asserted Claims. For each

reference or combination of references suggested by each chart, Defendants indicate whether the prior art renders the claim anticipated and/or obvious pursuant to P.R. 3-3(b).

In addition to contending that the '912 patent Asserted Claims are invalid in view of the prior art references cited in the claim charts of Appendix A, Defendants further contend that the '912 patent Asserted Claims are invalid as anticipated and/or obvious under U.S.C. §§ 102(a) and/or (b) in view of public knowledge and uses and/or offers for sale of products and services related to the subject matter of the cited references. As discovery is ongoing, Defendants continue to investigate these items and to reserve the right to amend or supplement these contentions to include additional information or documents regarding such products and/or systems.

In addition to contending that the '912 patent Asserted Claims are invalid in view of the explicit disclosures of the prior art references cited in the claim charts of Appendix A (e.g., references related to JEDEC), Defendants further contend that the knowledge of skill evidenced by those references render those claims invalid.

Defendants' reference to a particular memory module, circuit, software program, device or product in the claim charts of Appendix A should be interpreted as a reference to the product itself and any corresponding patents, publications, or product literature cited in Appendix A that relates to the cited memory module, circuit, software program, device, or product. In addition, Defendants may rely on other documents or things that have not yet been located to support its contentions regarding such prior art memory module(s), circuit(s), software program(s), device(s) or product(s) that are referenced in the charts.

Defendants incorporate by reference, as if set forth fully herein, all prior art cited during the prosecution of the '912 patent, all prior art cited during reexamination proceedings of the

'912 patent, all prior art as described in any future *inter partes* review proceedings of the '912 patent, and all prior art disclosed during previous litigation proceedings.

Defendants further identify and hereby incorporate by reference as if set forth fully herein the prior art references and invalidity contentions as described in any Other Netlist Proceedings wherein invalidity contentions have been, or will be, provided regarding the '912 patent, its foreign counterparts, or any parent or child patent of the '912 patent. Defendants reserve the right to use any and all portions of the publication, related publications, commercial embodiments of the publication, and other evidence that is discovered in these lawsuits to demonstrate and/or evidence the components, functionality, and capabilities of the devices and systems disclosed in the references charted.

Where Defendants identify a particular figure in a prior art reference, the identification should be understood to encompass the caption and description of the figure, as well as any text relating to the figure in addition to the figure itself. Similarly, where an identified portion of text refers to a figure or other material, the identification should be understood to include the referenced figure or other material as well. It should be recognized that a person of ordinary skill in the art would generally read a prior art reference as a whole and in the context of other publications, literature, and general knowledge in the field. To understand and interpret any specific statement or disclosure in a prior art reference, a person of ordinary skill in the art would rely upon other information including other publications and general scientific or engineering knowledge. Defendants therefore reserve the right to rely upon other unidentified portions of the prior art references and on other publications and expert testimony to provide context and to aid understanding and interpretation of the identified portions.

Defendants also reserve the right to rely upon other portions of the prior art references, other publications, and the testimony of experts to establish that the alleged inventions would have been obvious to a person of ordinary skill in the art, including the basis of modifying or combining certain cited references. To the extent any limitation is deemed not to be exactly met by an item of prior art, then any purported differences are such that the claimed subject matter as a whole would have been obvious to one skilled in the art at the time of the alleged invention, in view of the state of the art and knowledge of those skilled in the art. To the extent that an element of an Asserted Claim is not anticipated, the claim is rendered obvious by combination with one or more other prior art references identified in Appendix A.

2. U.S. Patent No. 9,858,215

The Asserted Claims of the '215 patent are anticipated and/or rendered obvious by prior art. Pursuant to P.R. 3-3(a), Defendants identify the prior art references that anticipate or render obvious the '215 patent Asserted Claims in the claim charts of Exhibits B1 through B21 (collectively "Appendix B") which are hereby incorporated by reference as if fully set forth herein. The claim charts of Appendix B provide an explanation showing how these prior art references teach or suggest each and every element of the '215 patent Asserted Claims. For each reference or combination of references suggested by each chart, Defendants indicate whether the prior art renders the claim anticipated and/or obvious pursuant to P.R. 3-3(b).

In addition to contending that the '215 patent Asserted Claims are invalid in view of the prior art references cited in the claim charts of Appendix B, Defendants further contend that the '215 patent Asserted Claims are invalid as anticipated and/or obvious under U.S.C. §§ 102(a) and/or (b) in view of public knowledge and uses and/or offers for sale of products and

services related to the subject matter of the cited references. As discovery is ongoing, Defendants continue to investigate these items and to reserve the right to amend or supplement these contentions to include additional information or documents regarding such products and/or systems.

In addition to contending that the '215 patent Asserted Claims are invalid in view of the explicit disclosures of the prior art references cited in the claim charts of Appendix B (e.g., references related to JEDEC), Defendants further contend that the knowledge of skill evidenced by those references render those claims invalid. Defendants' reference to a particular memory module, circuit, software program, device or product in the claim charts of Appendix B should be interpreted as a reference to the product itself and any corresponding patents, publications, or product literature cited in Appendix B that relates to the cited memory module, circuit, software program, device, or product. In addition, Defendants may rely on other documents or things that have not yet been located to support its contentions regarding such prior art memory module(s), circuit(s), software program(s), device(s) or product(s) that are referenced in the charts.

Defendants incorporate by reference, as if set forth fully herein, all prior art cited during the prosecution of the '215 patent, all prior art as described in any future *inter partes* review proceedings of the '215 patent, and all prior art disclosed during previous litigation proceedings. Defendants further identify and hereby incorporate by reference as if set forth fully herein the prior art references and invalidity contentions as described in any Other Netlist Proceedings wherein invalidity contentions have been, or will be, provided regarding the '215 patent, its foreign counterparts, or any parent or child patent of the '215 patent. Defendants reserve the right to use any and all portions of the publication, related publications, commercial embodiments of the publication, and other evidence that is discovered in these lawsuits to

demonstrate and/or evidence the components, functionality, and capabilities of the devices and systems disclosed in the references charted.

Where Defendants identify a particular figure in a prior art reference, the identification should be understood to encompass the caption and description of the figure, as well as any text relating to the figure in addition to the figure itself. Similarly, where an identified portion of text refers to a figure or other material, the identification should be understood to include the referenced figure or other material as well. It should be recognized that a person of ordinary skill in the art would generally read a prior art reference as a whole and in the context of other publications, literature, and general knowledge in the field. To understand and interpret any specific statement or disclosure in a prior art reference, a person of ordinary skill in the art would rely upon other information including other publications and general scientific or engineering knowledge. Defendants therefore reserve the right to rely upon other unidentified portions of the prior art references and on other publications and expert testimony to provide context and to aid understanding and interpretation of the identified portions.

Defendants also reserve the right to rely upon other portions of the prior art references, other publications, and the testimony of experts to establish that the alleged inventions would have been obvious to a person of ordinary skill in the art, including the basis of modifying or combining certain cited references. To the extent any limitation is deemed not to be exactly met by an item of prior art, then any purported differences are such that the claimed subject matter as a whole would have been obvious to one skilled in the art at the time of the alleged invention, in view of the state of the art and knowledge of those skilled in the art. To the extent that an element of an Asserted Claim is not anticipated, the claim is rendered obvious by combination with one or more other prior art references identified in Appendix B.

3. U.S. Patent No. 11,093,417

The Asserted Claims of the '417 patent are anticipated and/or rendered obvious by prior art. Pursuant to P.R. 3-3(a), Defendants identify the prior art references that anticipate or render obvious the '417 patent Asserted Claims in the claim charts of Exhibits C-1 through C18 (collectively "Appendix C") which are hereby incorporated by reference as if fully set forth herein. The claim charts of Appendix C provide an explanation showing how these prior art references teach or suggest each and every element of the '417 patent Asserted Claims. For each reference or combination of references suggested by each chart, Defendants indicate whether the prior art renders the claim anticipated and/or obvious pursuant to P.R. 3-3(b).

In addition to contending that the '417 patent Asserted Claims are invalid in view of the prior art references cited in the claim charts of Appendix C, Defendants further contend that the '417 patent Asserted Claims are invalid as anticipated and/or obvious under U.S.C. §§ 102(a) and/or (b) in view of public knowledge and uses and/or offers for sale of products and services related to the subject matter of the cited references. As discovery is ongoing, Defendants continue to investigate these items and to reserve the right to amend or supplement these contentions to include additional information or documents regarding such products and/or systems.

In addition to contending that the '417 patent Asserted Claims are invalid in view of the explicit disclosures of the prior art references cited in the claim charts of Appendix C (e.g., references related to JEDEC), Defendants further contend that the knowledge of skill evidenced by those references render those claims invalid.

Defendants' reference to a particular memory module, circuit, software program, device or product in the claim charts of Appendix C should be interpreted as a reference to the product itself and any corresponding patents, publications, or product literature cited in Appendix C that relates to the cited memory module, circuit, software program, device, or product. In addition, Defendants may rely on other documents or things that have not yet been located to support its contentions regarding such prior art memory module(s), circuit(s), software program(s), device(s) or product(s) that are referenced in the charts.

Defendants incorporate by reference, as if set forth fully herein, all prior art cited during the prosecution of the '417 patent, all prior art as described in any future *inter partes* review proceedings of the '417 patent, and all prior art disclosed during previous litigation proceedings. Defendants further identify and hereby incorporate by reference as if set forth fully herein the prior art references and invalidity contentions as described in any Other Netlist Proceedings wherein invalidity contentions have been, or will be, provided regarding the '417 patent, its foreign counterparts, or any parent or child patent of the '417 patent. Defendants reserve the right to use any and all portions of the publication, related publications, commercial embodiments of the publication, and other evidence that is discovered in these lawsuits to demonstrate and/or evidence the components, functionality, and capabilities of the devices and systems disclosed in the references charted.

Where Defendants identify a particular figure in a prior art reference, the identification should be understood to encompass the caption and description of the figure, as well as any text relating to the figure in addition to the figure itself. Similarly, where an identified portion of text refers to a figure or other material, the identification should be understood to include the referenced figure or other material as well. It should be recognized that a person of ordinary

skill in the art would generally read a prior art reference as a whole and in the context of other publications, literature, and general knowledge in the field. To understand and interpret any specific statement or disclosure in a prior art reference, a person of ordinary skill in the art would rely upon other information including other publications and general scientific or engineering knowledge. Defendants therefore reserve the right to rely upon other unidentified portions of the prior art references and on other publications and expert testimony to provide context and to aid understanding and interpretation of the identified portions.

Defendants also reserve the right to rely upon other portions of the prior art references, other publications, and the testimony of experts to establish that the alleged inventions would have been obvious to a person of ordinary skill in the art, including the basis of modifying or combining certain cited references. To the extent any limitation is deemed not to be exactly met by an item of prior art, then any purported differences are such that the claimed subject matter as a whole would have been obvious to one skilled in the art at the time of the alleged invention, in view of the state of the art and knowledge of those skilled in the art. To the extent that an element of an Asserted Claim is not anticipated, the claim is rendered obvious by combination with one or more other prior art references identified in Appendix C.

B. Obviousness

As stated above, Defendants incorporate by reference all other invalidity contentions related to the Asserted Patents served on or otherwise provided to Plaintiff, whether past or in the future. In addition to certain claims being anticipated at least under Plaintiff's apparent claim constructions as indicated above, the Asserted Claims are also invalid as obvious over the same teachings identified for anticipation. Further, the Asserted Claims are obvious over various combinations of the references shown in the claim charts accompanying or incorporated by

reference into this disclosure. No Asserted Claim goes beyond combining known elements to achieve predictable results or does more than choose between clear alternatives known to those of skill in the art. Thus, to the extent that an Asserted Claim is not anticipated, it is nevertheless invalid as obvious. Specifically, Defendants assert that any charted or incorporated reference in combination with one or more other charted or incorporated references renders the Asserted Claims obvious.

Motivations to combine, as well as the general state of the art, may be found in a variety of places including in the references defined above, and the specification of the Asserted Patents. For example, each piece of prior art relates to the design and/or structure and/or function of memory related devices, such as DIMMs. A person of ordinary skill in the art at the time of the alleged invention would have been motivated to combine any one piece of identified prior art with any other identified piece of prior art. For at least this reason, it would have been obvious to a person of skill in the art at the time of the alleged invention of the Asserted Claims to combine the various references cited herein so as to practice the Asserted Claims and there is a motivation in the art to make such a combination.

Motivations to combine various prior art references are present in the references themselves, the common knowledge of one of ordinary skill in the art, the prior art as a whole, or the nature of the problems allegedly addressed by the Asserted Patents. Further reasons to combine the references identified in these charts include the nature of the problem being solved, the express, implied, and/or inherent teachings of the prior art, the knowledge of persons of ordinary skill in the art, the fact that the prior art is generally directed towards methods and systems for the design and/or structure and/or function of memory related devices (*e.g.*, DIMMs) that such combinations would have yielded predictable results, and that such combinations

would have represented known alternatives to a person of ordinary skill in the art.

In *KSR International Co. v. Teleflex, Inc.*, the United States Supreme Court held that, among other things, “[t]he combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results.” 127 S. Ct. 1727, 1739 (2007); *see also id.* at 1731 (“[A] court must ask whether the improvement is more than the predictable use of prior art elements according to their established functions.”). In particular, a patent is obvious where “the content of the prior art, the scope of the patent claim, and the level of ordinary skill are not in material dispute, and the obviousness of the claim is apparent in light of these factors.” *Id.* at 1745–46. The Supreme Court found that “if a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill.” *Id.* at 1731.

Moreover, the Supreme Court recognizes that market pressures will motivate a person of ordinary skill to survey known art for solutions to problems. *Id.* at 1732 (“When there is a design need or market pressure to solve a problem and there are a finite number of identified, predictable solutions, a person of ordinary skill in the art has good reason to pursue the known options within his or her technical grasp.”). When a person of ordinary skill uses an identified, predictable solution to solve a problem, “it is likely the product not of innovation but of ordinary skill and common sense.” *Id.*

In addition, when a work is available in one field of endeavor, design incentives and other market forces can prompt variations of it, either in the same field or a different one. *Id.* at 1740. If a person of ordinary skill can implement a predictable variation, U.S.C. § 103 bars its patentability. *Id.* The rationale to combine or modify prior art references is significantly

stronger when references seek to solve similar problems, come from the same field, and correspond well. *In re Inland Steel Co.*, 265 F.3d 1354, 1362 (Fed. Cir. 2001).

Although the law does not require evidence of motivation to combine, motivation exists to combine one or more of the references disclosed herein with each other. In addition to the specific motivations identified herein, motivation to modify a particular reference or to combine any two or more of the identified references comes from (a) the nature of the problem being solved, (b) the teachings of the prior art, (c) the knowledge of persons of ordinary skill in the art, (d) the fact that all of the references teach systems, apparatuses, and methods related to the subject matter and address the same technical issues described in the Asserted Patents, and (e) one would be motivated by considerations of efficiency, effectiveness, convenience, cost-savings, and accessibility, to combine the various teachings. Additionally, one would be motivated to address the alleged problems or achieve the purported objectives identified in the Background sections of the Asserted Patents.

To the extent not anticipated, the Asserted Claims represent no more than the result of ordinary innovation over the prior art. Moreover, no showing of a specific motivation to combine prior art is required to combine the references disclosed above and in the attached charts, as each combination of art would have no unexpected results, and at most would simply represent a known alternative to one of ordinary skill in the art. *See KSR*, 127 S.Ct. at 1739-40 (rejecting the Federal Circuit’s “rigid” application of the teaching, suggestion, or motivation to combine test, instead espousing an “expansive and flexible” approach). Indeed, the Supreme Court held that a person of ordinary skill in the art is “a person of ordinary creativity, not an automaton” and “in many cases a person of ordinary skill in the art will be able to fit the teachings of multiple patents together like pieces of a puzzle.” *Id.* at 1742. Nevertheless, in

keeping with the Local Patent Rules, and in addition to the information contained in the section immediately above and elsewhere in these contentions, additional motivation and reason to combine the cited art are identified. A person having ordinary skill in any or all of these fields would be aware of all prior art in those fields, including but not limited to the identified prior art references and systems, and would have been motivated to combine the teachings of prior art with the field.

In sum, motivations to modify or combine the identified references including the references listed above can be found via, for example, discussions in the cited references, the state of the art discussed in the references, and the knowledge of one of ordinary skill in the art. One of ordinary skill in the art would have been motivated to combine these references, because these references relate to common objectives and subject matter. The references share commonalities in terms of their general subject matter as well as the types of equipment, products, systems, and/or methods used. Further, the prior art references explicitly or implicitly reference other prior art references, share common authors or inventors, were published in the same journals, were compiled by a common author of a compilation or reference book, were presented at the same conferences, and/or were developed at common companies, schools, or organizations which would motivate one of ordinary skill in the art to combine them. These references are within the field of the Asserted Patents and are directed to similar subject matter within the field. Additionally, the references, and any products, devices, or processes described in the references, existed and/or were invented in the same time period providing further motivation for combination. These disclosures were provided without prejudice to any arguments or objections concerning the relevance of motivation to combine in connection with any invalidity contentions.

Defendants reserve the right to further specify the motivations to combine the prior art in response to positions that Plaintiff may take later in this case and as discovery, including third party discovery, proceeds. Defendants may rely on any and all portions of the prior art, other documents, and expert testimony to establish that a person of ordinary skill in the art would have been motivated to modify or combine the prior art so as to render the claims invalid as obvious. Moreover, Defendants reserve the right to rely on later identified sources of information, including but not limited to witness testimony and other discovery, to establish the state of the art in the relevant time frame pertaining to the Asserted Patents.

While Defendants reserve the right to rely on any combination of the references reflected in their charts or incorporated herein by reference, Defendants provide the following exemplary and non-exhaustive references and/or combinations evidencing invalidity of the claims of the Asserted Patents. The combinations of prior art listed below render obvious the Asserted Claims under the proper construction of the claims and/or under Plaintiff's apparent interpretation of the claims as set forth by Plaintiff in its Complaint and Infringement Contentions.

1. U.S. Patent No. 7,619,912

Pursuant to P.R. 3-3(a) and (b), Defendants identify in Appendix A the prior art references that render obvious the Asserted Claims of the '912 patent and include below exemplary combinations showing the obviousness of the '912 patent Asserted Claims in view of the prior art. To the extent Plaintiff contends that an element is not disclosed in any one of the anticipatory references described in Appendix A, the limitation would have been obvious in light of the disclosures within the reference and the knowledge of one of ordinary skill in the art at the time of the '912 patent. Moreover, to the extent Plaintiff contends that an element is not disclosed in any one of the anticipatory references described in Appendix A, such reference may be combined with

any other references listed in Appendix A for such element, thereby rendering the claims invalid for obviousness.

To the extent a finder of fact determines that a limitation of any of the '912 patent Asserted Claims is not disclosed by one of the references identified above pursuant to P.R. 3-3(a), the claim is nevertheless unpatentable as obvious because they contain nothing that constitutes a patentable innovation. To the extent a finder of fact determines that a limitation of the '912 patent Asserted Claims is not anticipated, it does not go beyond combining familiar elements according to known methods to achieve predictable results or does more than choose between clear alternatives known to those of ordinary skill in the art.

(a) Obviousness Rationale

For at least the reasons described in these contentions, it would have been obvious to one of ordinary skill in the art to combine any of a number of prior art references, including any combination of those prior art references identified in Appendix A along with the knowledge of one of ordinary skill in the art to meet the limitations of the '912 patent Asserted Claims. Moreover, as mentioned above, Defendants have not yet completed their search or discovery concerning additional prior art. As such, Defendants' inclusion of exemplary combinations does not preclude them from identifying other invalidating combinations as appropriate, and Defendants reserve the right to identify additional specific combinations as well as to detail and explain such combinations.

To the extent not anticipated, the '912 patent Asserted Claims represent no more than the result of ordinary variations of the prior art. Defendants further believe that no showing of a specific motivation to combine prior art is required to combine the references disclosed above and in the attached charts, as each combination of art would have no unexpected results, and at most

would simply represent a known alternative to one of ordinary skill in the art. *See KSR Int'l Co. v. Teleflex, Inc.*, 550 U.S. 398, 415-16 (2007) (rejecting the Federal Circuit's "rigid" application of the teaching, suggestion, or motivation to combine test, instead espousing an "expansive and flexible" approach). Indeed, the Supreme Court held that a person of ordinary skill in the art is "a person of ordinary creativity, not an automaton" and "in many cases a person of ordinary skill in the art will be able to fit the teachings of multiple patents together like pieces of a puzzle." *Id.* at 420-21. Nevertheless, in addition to the information contained elsewhere in these contentions, Defendants identify motivation and reason to combine the cited art.

One or more combinations of the prior art references identified in Appendix A would have been obvious because these references would have been combined using: known methods to yield predictable results; known techniques in the same way; a simple substitution of one known, equivalent element for another to obtain predictable results; and/or a teaching, suggestion, or motivation in the prior art generally. In addition, it would have been obvious to try combining the prior art references identified above because there were only a finite number of predictable solutions and/or because known work in one field of endeavor prompted variations based on predictable design incentives and/or market forces either in the same field or a different one. Further, the combinations of the prior art references identified in Appendix A would have been obvious because the combinations represent known potential options with a reasonable expectation of success.

Additional evidence that there would have been a motivation to combine the prior art references identified above includes the interrelated teachings of multiple prior art references; common authorship; the effects of demands known to the design community or present in the marketplace; the existence of a known problem for which there was an obvious solution

encompassed by the '912 patent Asserted Claims; the existence of a known need or problem in the field of the endeavor at the time of the alleged invention(s); and the background knowledge that would have been possessed by a person having ordinary skill in the art.

Thus, the motivation to combine the teachings of the prior art references disclosed in Appendix A is found in the references themselves and also in: (1) the nature of the problem being solved; (2) the express, implied and inherent teachings of the prior art; (3) the knowledge of persons of ordinary skill in the art; (4) the predictable results obtained in combining the different elements of the prior art; (5) the predictable results obtained in simple substitution of one known element for another; (6) the use of a known technique to improve similar devices, methods, or products in the same way; (7) the predictable results obtained in applying a known technique to a known device, method, or product ready for improvement; (8) the finite number of identified predictable solutions that had a reasonable expectation of success; and (9) known work in various technological fields that could be applied to the same or different technological fields based on design incentives or other market forces.

Additionally, it would be obvious to one of ordinary skill in the art to consult and/or combine any of the prior art listed in Appendix A because all of these references relate to the same area of technology and/or are from analogous art. The '912 patent Asserted Claims are directed to a memory module that performs rank multiplication. '912 patent at Abstract, 12:11-23:26. The '912 patent Asserted Claims merely unite old elements, well known in the field, with no change in their respective function or result. Given the interrelated teachings of the prior art, the effects of demands known to the design community or present in the marketplace, and the background knowledge possessed by a person having ordinary skill in the art, it would have been obvious for one of ordinary skill in the art to combine these familiar elements, disclosed and/or

embodied in the prior art listed above to practice the '912 patent Asserted Claims.

All of the '912 patent Asserted Claims are directed to a memory module connectable to a computer system that employs rank multiplication to improve a memory module's capacity. Such technology, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, was widely known before the alleged priority date of the '912 Patent, as evidenced by the references in Appendix A. *See, e.g.,* Ex. A1 (the '912 Patent's Admitted Prior Art).

One of ordinary skill in the art would have been motivated to combine any of the references in Appendix A because at the time of the alleged invention improving a memory module's capacity was a common problem with well-known solutions. *See, e.g.,* '912 patent at 4:42-5:5; *see also* Amidi at [0008]-[0011]; Ellsberry at [0005], [0012]; Holman at 2:43-54; JEDEC Standards (*see, e.g.,* JEDEC Standard 21-C at 4.20.4-5, 4.20.4-25 through 4.20.4-27, JESD79 at 1, 2, 8; JESD79-2 at 10, 12; JESD79C at 1, 7, 8); Perego '422 at 1:18-30; Dell '827 at 1:21-57; Dell '074 at 1:53-2:21; MicronRDIMM at 1, 6-8, 18-20; JESD79C at 1, 2, 5, 8; QBM (*see, e.g.,* QBM Specification Rev. 0.93 at 5-9; QBM2 Interface Overview at 3; QBM2 Technical Features Overview at 3-5; QBM Doubling DDR Memory Bandwidth at 10; QBM2 Technology Overview at 17); DDR3 Functional Outlook at 11, 19-20.

Further, it was common knowledge to one of ordinary skill in the art at the time of the alleged invention that rank multiplication can improve performance and/or cost of the memory module. *See, e.g.,* '912 patent at 4:42-5:5; *see also* Amidi at [0008]-[0011]; Ellsberry at [0005], [0012]; Holman at 2:43-54; JEDEC Standards (*see, e.g.,* JEDEC Standard 21-C at 4.20.4-5, 4.20.4-25 through 4.20.4-27, JESD79 at 1, 2, 8; JESD79-2 at 10, 12; JESD79C at 1, 7, 8); Perego '422 at 1:18-30; Dell '827 at 1:21-57; Dell '074 at 1:53-2:21; MicronRDIMM at 1, 6-8, 18-20;

JESD79C at 1, 2, 5, 8; QBM (*see, e.g.*, QBM Specification Rev. 0.93 at 5-9; QBM2 Interface Overview at 3; QBM2 Technical Features Overview at 3-5; QBM Doubling DDR Memory Bandwidth at 10; QBM2 Technology Overview at 17); DDR3 Functional Outlook at 11, 19-20.

One of ordinary skill in the art would have been motivated to combine any of the references in Appendix A at the time of the alleged invention. Common problems with conventional techniques for improving a memory module's capacity were known to persons of ordinary skill in the art and rank multiplication was a well-known solution to achieve improved performance. *See, e.g.*, '912 patent at 4:42-5:5; *see* Amidi at [0008]-[0011]; Ellsberry at [0005], [0012]; Holman at 2:43-54; JEDEC Standards (*see, e.g.*, JEDEC Standard 21-C at 4.20.4-5, 4.20.4-25 through 4.20.4-27, JESD79 at 1, 2, 8; JESD79-2 at 10, 12; JESD79C at 1, 7, 8); Perego '422 at 1:18-30, 2:15-25; Dell '827 at 1:21-57; Dell '074 at 1:53-2:21; MicronRDIMM at 1, 6-8, 18-20; JESD79C at 1, 2, 5, 8; QBM (*see, e.g.*, QBM Specification Rev. 0.93 at 5-9; QBM2 Interface Overview at 3; QBM2 Technical Features Overview at 3-5; QBM Doubling DDR Memory Bandwidth at 10; QBM2 Technology Overview at 17); DDR3 Functional Outlook at 11, 19-20.

It was well-known to one of ordinary skill in the art before the time of the '912 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that a memory module can be connectable to a computer system. *See* citations identified for claim element [16pre] provided in attached Exhibits A1 through A14.

It was well-known to one of ordinary skill in the art before the time of the '912 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that a memory module can include a printed circuit board. *See* citations identified for claim element [16.1] provided in attached Exhibits A1 through A14.

It was well-known to one of ordinary skill in the art before the time of the '912 patent, at

least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that a memory module can include a first number of DDR memory devices coupled to the printed circuit board and arranged in a first number of ranks. *See* citations identified for claim element [16.2] provided in attached Exhibits A1 through A14.

It was well-known to one of ordinary skill in the art before the time of the '912 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that a memory module can include a circuit coupled to the printed circuit board, the circuit comprising a logic element and a register. *See* citations identified for claim element [16.3] provided in attached Exhibits A1 through A14.

It was well-known to one of ordinary skill in the art before the time of the '912 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that a memory module can include a logic element, wherein the logic element can receive input signals from a computer system comprising row/column address signals, bank address signals, and chip-select signals. *See* citations identified for claim element [16.4] provided in attached Exhibits A1 through A14.

It was well-known to one of ordinary skill in the art before the time of the '912 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that a memory module can include a logic element, wherein the logic element can receive input signals from a computer system comprising at least one row address signal, bank address signals, at least one chip-select signal, and at least one command signal of the plurality of input signals. *See* citations identified for claim element [39.5] provided in attached Exhibits A1 through A14.

It was well-known to one of ordinary skill in the art before the time of the '912 patent, at

least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that a memory module can include a logic element, wherein the logic element can receive input signals that are configured to control a second number of DDR memory devices arranged in a second number of ranks, the second number of DDR memory devices smaller than the first number of DDR memory devices and the second number of ranks less than the first number of ranks. *See* citations identified for claim element [16.5] provided in attached Exhibits A1 through A14.

It was well-known to one of ordinary skill in the art before the time of the '912 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that a memory module can include a circuit, wherein the circuit can generate a set of output signals in response to the set of input signals, the output signals are configured to control DDR memory devices arranged in the first number of ranks. *See* citations identified for claim element [16.6] and [16.7] provided in attached Exhibits A1 through A14.

It was well-known to one of ordinary skill in the art before the time of the '912 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that a memory module can include a circuit, wherein the circuit further responds to a command signal and the set of input signals from the computer system by selecting one or two ranks of the first number of ranks and transmitting the command signal to at least one DDR memory device of the selected one or two ranks of the first number of ranks. *See* citations identified for claim element [16.8] provided in attached Exhibits A1 through A14..

It was well-known to one of ordinary skill in the art before the time of the '912 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that a memory module can include a phase-lock loop device coupled to

the printed circuit board, the phase-lock loop device operatively coupled to the plurality of DDR memory devices, the logic element, and the register. *See* citations identified for claim element [16.9] provided in attached Exhibits A1 through A14.

It was well-known to one of ordinary skill in the art before the time of the '912 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that a memory module can include a circuit, wherein the circuit can transmit the command signal to only one DDR memory device at a time. *See* citations identified for claim element [16.10] provided in attached Exhibits A1 through A14.

It was well-known to one of ordinary skill in the art before the time of the '912 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that a memory module can include a phase-lock loop device, wherein the phase-lock loop device transmits a PLL clock signal to the plurality of DDR memory devices, the logic element, and the register in response to signals received from the computer system. *See* citations identified for claim element [1.10] provided in attached Exhibits A1 through A14.

It was well-known to one of ordinary skill in the art before the time of the '912 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that a memory module can include a register, wherein the register (1) receives, from the computer system, and (ii) buffers, in response to the PLL clock signal, a plurality of row/column address signals and the bank address signals, and (iii) transmits the buffered plurality of row/column address signals and the buffered bank address signals to the plurality of DDR memory devices. *See* citations identified for claim element [1.11] provided in attached Exhibits A1 through A14.

It was well-known to one of ordinary skill in the art before the time of the '912 patent, at

least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that a memory module can include a logic element, wherein the at least one row/column address signal received by the logic element comprises at least one row address signal received by the logic element, and wherein the plurality of row/column address signals received by the register are separate from the at least one row address signal received by the logic element. . See citations identified for claim element [1.12] provided in attached Exhibits A1 through A14.

It was well-known to one of ordinary skill in the art before the time of the '912 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that a memory module can include a logic element, wherein the logic element generates gated column access strobe (CAS) or chip-select signals of the output control signals in response to at least in part to (i) the at least one row address signal, (ii) the bank address signal, (iii) the at least one chip-select signal of the set of input control signals, and (iv) the PLL clock signal. See citations identified for claim element [1.13] provided in attached Exhibits A1 through A14.

It was well-known to one of ordinary skill in the art before the time of the '912 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that a memory module can receive a set of input control signals and generate a set of output control signals, the set of input control signals comprising a first number of chip-select signals and the set of output control signals comprising a second number of chip-select signals greater than the first number of chip-select signals. See citations identified for claim element [3] provided in attached Exhibits A1 through A14.

It was well-known to one of ordinary skill in the art before the time of the '912 patent, at

least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that a memory module can receive two chip-select signals and generate four chip-select signals. *See* citations identified for claim element [4] provided in attached Exhibits A1 through A14.

It was well-known to one of ordinary skill in the art before the time of the '912 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that a memory module can include a logic element, wherein the logic element comprises an application-specific integrated circuit, a field-programmable gate array, a custom-designed semiconductor device, or a complex programmable-logic device. *See* citations identified for claim element [6] provided in attached Exhibits A1 through A14.

It was well-known to one of ordinary skill in the art before the time of the '912 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that a memory module can include a logic element, a register, and a phase-lock loop device, wherein two or more of the logic element, register and phase-lock loop device are portions of a single component. *See* citations identified for claim element [8] provided in attached Exhibits A1 through A14.

It was well-known to one of ordinary skill in the art before the time of the '912 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that a memory module can include a plurality of DDR memory devices, wherein the plurality of DDR memory devices are arranged as a first set and a second set on the first side of the printed circuit board, and a third set and a fourth set on the second side of the printed circuit board, the second set of memory devices spaced from the first set, and the fourth set of memory devices spaced from the third set. *See* citations identified for claim element [10]

provided in attached Exhibits A1 through A14.

It was well-known to one of ordinary skill in the art before the time of the '912 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that a memory module can have a first and a second set of DDR memory devices on the first side of the printed circuit board, and a third and a fourth set of DDR memory devices on the second side of the printed circuit board, wherein the second set of DDR memory devices are spaced from the first set in a direction along the first side of the circuit board and the fourth set of DDR memory devices are spaced from the third set in a direction along the second side of the circuit board. See citations identified for claim element [11] provided in attached Exhibits A1 through A14.

It was well-known to one of ordinary skill in the art before the time of the '912 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that a memory module can transmit received command signal to two ranks of the first number of ranks at time. See citations identified for claim element [18] provided in attached Exhibits A1 through A14.

It was well-known to one of ordinary skill in the art before the time of the '912 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that a memory module can receive and generate command signals, wherein the command signal comprises a refresh command signal. See citations identified for claim element [19] provided in attached Exhibits A1 through A14.

It was well-known to one of ordinary skill in the art before the time of the '912 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that a memory module can receive a command signal, wherein the

command signal comprises a read command signal or a write command signal, the set of input signals comprises a density bit which is a row address bit, and the circuit is configured to store the row address bit during an activate command for a selected bank. *See* citations identified for claim element [22] provided in attached Exhibits A1 through A14.

It was well-known to one of ordinary skill in the art before the time of the '912 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that a memory module can receive a set of input signals and generate a set of output signals, wherein the set of input signals are configured to control two ranks of memory devices and the set of output signals are configured to control four ranks of memory devices. *See* citations identified for claim element [34] provided in attached Exhibits A1 through A14.

It was well-known to one of ordinary skill in the art before the time of the '912 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that a memory module can receive and generate command signals, wherein the input and output command signal is a precharge signal. *See* citations identified for claim element [37] provided in attached Exhibits A1 through A14.

It was well-known to one of ordinary skill in the art before the time of the '912 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that a memory module can receive and generate command signals, wherein the input and output command signal is a read signal or a write signal. *See* citations identified for claim element [38] provided in attached Exhibits A1 through A14.

It was well-known to one of ordinary skill in the art before the time of the '912 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that a memory module can include a plurality of DDR memory devices,

wherein each DDR memory device comprise one or more banks, and the plurality of DDR memory devices are arranged in two or more ranks selectable by a first number of chip-select signals. *See* citations identified for claim element [39.2] provided in attached Exhibits A1 through A14.

It was well-known to one of ordinary skill in the art before the time of the '912 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that a memory module can include an integrated circuit element, wherein the integrated circuit element receives a plurality of input signals from the computer system and generates output signals, the input and output signals comprising row address signals, column address signals, bank address signals, and command signals. In addition, the input signals can include a second number of chip-select signals less than the first number of chip-select signals in the output signals. *See* citations identified for claim element [39.4] and [39.6] provided in attached Exhibits A1 through A14.

It was well-known to one of ordinary skill in the art before the time of the '912 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that a memory module can include a register, wherein the register receives a plurality of row address signals. *See* citations identified for claim element [39.9] and [39.10] provided in attached Exhibits A1 through A14.

It was well-known to one of ordinary skill in the art before the time of the '912 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that a memory module can simulate a virtual memory module having a second number of DDR memory devices. *See* citations identified for claim element [40] provided in attached Exhibits A1 through A14.

It was well-known to one of ordinary skill in the art before the time of the '912 patent, at

least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that a memory module can include a plurality of DDR memory devices, wherein the plurality of DDR memory devices has at least one attribute selected from a group consisting of a number of row address bits per DDR memory device, a number of column address bits per DDR memory device, a number of bank address bits per DDR memory device, a number of DDR memory devices, a data width per DDR memory device, a memory density per DDR memory device, a number of ranks of DDR memory devices, and a memory density per rank. *See* citations identified for claim element [52.1] provided in attached Exhibits A1 through A14.

It was well-known to one of ordinary skill in the art before the time of the '912 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that a memory module can include a read-only nonvolatile memory device storing data accessible to the computer system, wherein the data characterizes the plurality of DDR memory devices as having at least one value of the at least one attribute that is different from the actual value of the at least one attribute of the plurality of DDR memory devices. *See* citations identified for claim element [52.3] provided in attached Exhibits A1 through A14. *See also* U.S. Pat. No. 6,961,282 (Wong) at 6:13-23, 7:48-62.

It was well-known to one of ordinary skill in the art before the time of the '912 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that a memory module can include a plurality of DDR memory devices, wherein each DDR memory device is a DDR dynamic random-access memory (DRAM) chip package with a bit width, and each rank of the first number of ranks comprises a plurality of the DDR DRAM chip packages having a total bit width equal to the summed bit widths of the DDR DRAM chip packages of the rank. *See* citations identified for claim element [55.1] provided in

attached Exhibits A1 through A14. *See also* U.S. Pat. No. 7,414,312 (Nguyen) at Abstract.

It was well-known to one of ordinary skill in the art before the time of the '912 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that a memory module can include means for characterizing the plurality of DDR memory devices as having one or more attributes that are different from the actual attributes of the memory devices. *See* citations identified for claim element [56] provided in attached Exhibits A1 through A14.

It was well-known to one of ordinary skill in the art before the time of the '912 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that a memory module can receive and generate control signals, wherein the set of input control signals corresponds to a first memory density and the set of output control signals corresponds to a second memory density, the first memory density greater than the second memory density. *See* citations identified for claim element [57] provided in attached Exhibits A1 through A14.

It was well-known to one of ordinary skill in the art before the time of the '912 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that a memory module can include a plurality of register devices. *See* citations identified for claim element [58] provided in attached Exhibits A1 through A14.

It was well-known to one of ordinary skill in the art before the time of the '912 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that a memory module can include a logic element, wherein the chip-select signals generated by the logic element are the first number of chip-select signals of the set of output control signals, the first number of chip-select signals generated by the logic element

equal to the first number of ranks, and the at least one chip-select signal of the set of input control signals comprises a second number of chip-select signals equal to the second number of ranks. *See* citations identified for claim element [59] provided in attached Exhibits A1 through A14.

It was well-known to one of ordinary skill in the art before the time of the '912 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that a memory module can include a logic element, wherein the at least one row address signal and the bank address signals in the set of input signals are (i) received by the logic element during an activate command operation and (ii) are used by the logic element for a subsequent read or write command operation. *See* citations identified for claim element [60] provided in attached Exhibits A1 through A14.

It was well-known to one of ordinary skill in the art before the time of the '912 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that a memory module can include a serial-presence detect (SPD) device storing data accessible to the computer system, wherein the data characterizes the plurality of DDR memory devices as having one or more attributes that are different from the actual attributes of the memory devices. *See* citations identified for claim element [62.3] provided in attached Exhibits A1 through A14.

It was well-known to one of ordinary skill in the art before the time of the '912 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that a memory module can include a register, wherein the register receives the input command signal of the set of input control signals. *See* citations identified for claim element [72] provided in attached Exhibits A1 through A14.

It was well-known to one of ordinary skill in the art before the time of the '912 patent, at

least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that a memory module can include a logic element, wherein the logic element responds to at least (i) a row address bit of the at least one row/column address signal, (ii) the bank signals, and (iii) the at least one chip-select signal of the set of input control signals and (iv) the PLL clock signal by generating a first number of chip-select signals of the set of output control signals, the first number of chip-select signals generated by the logic element equal to the first number of ranks, and the at least one chip-select signal of the set of input control signals comprises a second number of chip-select signals equal to the second number of ranks. *See* citations identified for claim element [77.13] provided in attached Exhibits A1 through A14.

It was well-known to one of ordinary skill in the art before the time of the '912 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that a memory module can be operable to perform successive read accesses from different ranks of the plurality of DDR memory devices. *See* citations identified for claim element [83] provided in attached Exhibits A1 through A14. *See also* U.S. Pat. No. 6,286,077 (Choi) at 5:4-6; U.S. Pat. No. 6,742,098 (Halbert) at Fig. 3, Fig. 5, 2:37-50, 5:58-6:6; U.S. Pat. No. 7,020,739 (Mukaida) at 2:51-59.

It was well-known to one of ordinary skill in the art before the time of the '912 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that a memory module can be operable to perform back-to-back adjacent read commands which cross DDR memory device boundaries. *See* citations identified for claim element [84] provided in attached Exhibits A1 through A14. *See also* U.S. Pat. No. 6,286,077 (Choi) at 5:4-6; U.S. Pat. No. 6,742,098 (Halbert) at Fig. 3, Fig. 5, 2:37-50, 5:58-6:6; U.S. 7,020,739 (Mukaida) at 2:51-59.

It was well-known to one of ordinary skill in the art before the time of the '912 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that a memory module can receive bank address signals, wherein the bank address signals include bank address signals received during an activate command operation and bank address signals received during a read or write command operation subsequent to the activate command operation, and the rank-selecting signals are used for the read or write command operation. *See* citations identified for claim element [85] provided in attached Exhibits A1 through A14.

In addition, the prior art also provided sets of finite, identified, predictable solutions for known problems that would have been obvious to those of ordinary skill to try with a reasonable expectation of success. For example, it would have been obvious to one of ordinary skill in the art at the time of the alleged invention for a memory module to have a printed circuit board, plurality of DDR memory devices, circuit, and phase-lock loop device. It would have been obvious for those DDR memory devices to be arranged in first and second numbers of ranks. It would have been obvious for the circuit to have a logic element that receives input signals comprising a row/column address signal, bank address signal, and chip-select signal configured to control a second number of DDR memory devices arranged in ranks. It would have been obvious for the circuit's logic element to generate output signals configured to control the first number of DDR memory devices in ranks. It would have been obvious for the circuit to respond to a command signal and input signals by selecting one or two of the first number of ranks and to transmit the command signal to at least one DDR memory device of the selected one or two ranks. It would have been obvious for the phase-lock loop device to be operatively coupled to the DDR memory devices, logic element, and register. It would have been obvious for the command signal to be

transmitted to only one DDR memory device at a time. *See* citations identified for claim provided in attached Exhibits A1 through A14.

The prior art references provide motivations to combine because they describe the field of the '912 patent, teach improvements, explain desired features, and even expressly state that one of ordinary skill in the art would be able to apply their teachings to related systems or methods. *See, e.g.*, '912 patent at 5:42-45, 6:12-30, 6:39-54, 14:14-16, 21:50-53, 22:64-23:5, 25:4-5, 25:23-25, 31:24-32, 32:51-57; Amidi at [0001], [0008]-[0011], [0071]-[0072]; Ellsberry at [0001], [0005], [0012], [0058]; Holman at 1:36-41, 2:43-54; JEDEC Standards (*see, e.g.*, JEDEC Standard 21-C at 4.20.4-5, 4.20.4-25 through 4.20.4-27, JESD79 at 1, 2, 8; JESD79-2 at 10, 12; JESD79C at 1, 7, 8); Perego '422 at 1:10-30, 2:15-25, 3:23-40, 15:31-45, 22:10-21; Dell '827 at 1:11-57, 6:31-37; Dell '074 at 1:15-2:21, 2:40-3:4, 9:39-45; MicronRDIMM at 1, 6-8, 18-20; JESD79C at 1, 2, 5, 8; QBM (*see, e.g.*, QBM Specification Rev. 0.93 at 5-9; QBM2 Interface Overview at 3; QBM2 Technical Features Overview at 3-5; QBM Doubling DDR Memory Bandwidth at 10; QBM2 Technology Overview at 17); DDR3 Functional Outlook at 11, 19-20.

Further, the prior art references provide motivations to combine because they explicitly suggest utilizing the teachings and disclosures of other references.

In accordance with these advances, the prior art could have been combined according to methods known to those of ordinary skill within the field of the Asserted Patents to yield predictable results. The substitution of one element in a memory module could have been predictably achieved by one of ordinary skill at the time of the alleged invention. One of ordinary skill in the art would have been aware of these various applications, including rank multiplication techniques and structures, and would have been able to select appropriate attributes of one for

inclusion in another. Those of ordinary skill in the art could have employed known techniques to improve similar prior art devices in the same way as claimed in the '912 Patent.

In addition, one of ordinary skill in the art would be motivated to combine the prior art references because the elements found in the Asserted Claims are well known in the art. Indeed, the listed inventors of the Asserted Patents admitted as much in the specification of the '912 Patent. *See* citations identified in attached Exhibit A1.

Any reference or combination of references that anticipates or makes obvious an asserted independent claim also makes obvious any asserted claim dependent on that independent claim, as the element of each dependent '912 patent Asserted Claim was known by a person of ordinary skill at the time of the alleged invention, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, and it would have been obvious to combine those known elements with the independent claims at least as a matter of common sense and routine innovation. Accordingly, Defendants contend that each Asserted Claim would have been obvious not only by the combinations described in these contentions, but also by any combination of references that renders obvious an Asserted Claim.

In addition to the specific examples of motivation provided above, Defendants reserve the right to rely on the disclosures of the references listed in Appendix A for additional motivation to combine. The above-identified examples of combinations are given merely to illustrate various motivations to combine and are not intended to provide an exhaustive list of every possible combination to which the motivation may apply. Defendants reserve the right to contend that the above-described motivations to combine apply to other combinations at the appropriate time, i.e., in expert reports regarding invalidity.

For at least the reasons described above, it would have been obvious to one of ordinary

skill in the art to combine each prior art reference listed in Appendix A with any other reference or references listed in Appendix A along with the knowledge of one of ordinary skill in the art to arrive at the inventions claims in the '912 patent. For example, and without limitation, the Asserted Claims of the '912 patent would have been obvious to one of ordinary skill in the art in view of the following combinations:

Patent No. or Title (Primary Inventor/Author)	In Combination with One or More of: (Patent No. or Title (Primary Inventor/Author))
The '912 Patent's Admitted Prior Art ("APA")	• U.S. Patent App. Pub. No. 20060117152 ("Amidi") • U.S. Patent App. Pub. No. 2006/0277355 ("Ellsberry") • U.S. Patent No. 7,240,145 ("Holman") • JEDEC Standards • U.S. Patent No. 7,363,422 ("Perego '422") • U.S. Patent No. 5,926,827 ("Dell'827") • U.S. Patent No. 6,209,074 ("Dell'074") • Micron DDR SDRAM RDIMM, MT36VDDF12872 & MT36VDDF25672 Product • DDR SDRAM Specification, JEDEC Standard No. 79C, March 2003 • Kentron's Quad Band Memory System ("QBM") • U.S. Patent No. 6,961,281 ("Wong") • U.S. Patent No. 6,996, 686 ("Doblar") • U.S. Patent No. 6,757,751 ("Gene") • U.S. Patent No. 6,742,098 ("Halbert") • U.S. Patent No. 7,181,584 ("LaBerge") • U.S. Patent No. 6,286,077 ("Choi") • U.S. Patent No. 7,020,739 ("Mukaida") • U.S. Patent App. Pub. No. 2007/0043922 ("Lee") • U.S. Patent No. 7,414,312 ("Nguyen") • DDR Functional Outlook; and/or • The knowledge of a person of ordinary skill in the art.
U.S. Patent App. Pub. No. 20060117152 ("Amidi")	• Asserted Patent's Admitted Prior Art ("APA") • U.S. Patent App. Pub. No. 2006/0277355 ("Ellsberry")

	• U.S. Patent No. 7,240,145 (“Holman”) • JEDEC Standards • U.S. Patent No. 7,363,422 (“Perego ’422”) • U.S. Patent No. 5,926,827 (“Dell’827”) • U.S. Patent No. 6,209,074 (“Dell’074”) • Micron DDR SDRAM RDIMM, MT36VDDF12872 & MT36VDDF25672 Product • DDR SDRAM Specification, JDEC Standard No. 79C, March 2003 • Kentron’s Quad Band Memory System (“QBM”) • U.S. Patent No. 6,961,281 (“Wong”) • U.S. Patent No. 6,996, 686 (“Doblar”) • U.S. Patent No. 6,757,751 (“Gene”) • U.S. Patent No. 6,742,098 (“Halbert”) • U.S. Patent No. 7,181,584 (“LaBerge”) • U.S. Patent No. 6,286,077 (“Choi”) • U.S. Patent No. 7,020,739 (“Mukaida”) • U.S. Patent App. Pub. No. 2007/0043922 (“Lee”) • U.S. Patent No. 7,414,312 (“Nguyen”) • DDR Functional Outlook; and/or • The knowledge of a person of ordinary skill in the art.
U.S. Patent App. Pub. No. 2006/0277355 (“Ellsberry”)	• Asserted Patent’s Admitted Prior Art (“APA”) • U.S. Patent App. Pub. No. 20060117152 (“Amidi”) • U.S. Patent No. 7,240,145 (“Holman”) • JEDEC Standards • U.S. Patent No. 7,363,422 (“Perego ’422”) • U.S. Patent No. 5,926,827 (“Dell’827”) • U.S. Patent No. 6,209,074 (“Dell’074”) • Micron DDR SDRAM RDIMM, MT36VDDF12872 & MT36VDDF25672 Product • DDR SDRAM Specification, JDEC Standard No. 79C, March 2003 • Kentron’s Quad Band Memory System (“QBM”) • U.S. Patent No. 6,961,281 (“Wong”) • U.S. Patent No. 6,996, 686 (“Doblar”) • U.S. Patent No. 6,757,751 (“Gene”) • U.S. Patent No. 6,742,098 (“Halbert”)

	• U.S. Patent No. 7,181,584 (“LaBerge”) • U.S. Patent No. 6,286,077 (“Choi”) • U.S. Patent No. 7,020,739 (“Mukaida”) • U.S. Patent App. Pub. No. 2007/0043922 (“Lee”) • U.S. Patent No. 7,414,312 (“Nguyen”) • DDR Functional Outlook; and/or • The knowledge of a person of ordinary skill in the art.
U.S. Patent No. 7,240,145 (“Holman”)	• Asserted Patent’s Admitted Prior Art (“APA”) • U.S. Patent App. Pub. No. 20060117152 (“Amidi”) • U.S. Patent App. Pub. No. 2006/0277355 (“Ellsberry”) • JEDEC Standards • U.S. Patent No. 7,363,422 (“Perego ’422”) • U.S. Patent No. 5,926,827 (“Dell’827”) • U.S. Patent No. 6,209,074 (“Dell’074”) • Micron DDR SDRAM RDIMM, MT36VDDF12872 & MT36VDDF25672 Product • DDR SDRAM Specification, JDEC Standard No. 79C, March 2003 • Kentron’s Quad Band Memory System (“QBM”) • U.S. Patent No. 6,961,281 (“Wong”) • U.S. Patent No. 6,996, 686 (“Doblar”) • U.S. Patent No. 6,757,751 (“Gene”) • U.S. Patent No. 6,742,098 (“Halbert”) • U.S. Patent No. 7,181,584 (“LaBerge”) • U.S. Patent No. 6,286,077 (“Choi”) • U.S. Patent No. 7,020,739 (“Mukaida”) • U.S. Patent App. Pub. No. 2007/0043922 (“Lee”) • U.S. Patent No. 7,414,312 (“Nguyen”) • DDR Functional Outlook; and/or • The knowledge of a person of ordinary skill in the art.
JEDEC Standards	• Asserted Patent’s Admitted Prior Art (“APA”) • U.S. Patent App. Pub. No. 20060117152 (“Amidi”) • U.S. Patent App. Pub. No. 2006/0277355 (“Ellsberry”)

	• U.S. Patent No. 7,240,145 (“Holman”) • U.S. Patent No. 7,363,422 (“Perego ’422”) • U.S. Patent No. 5,926,827 (“Dell’827”) • U.S. Patent No. 6,209,074 (“Dell’074”) • Micron DDR SDRAM RDIMM, MT36VDDF12872 & MT36VDDF25672 Product • DDR SDRAM Specification, JDEC Standard No. 79C, March 2003 • Kentron’s Quad Band Memory System (“QBM”) • U.S. Patent No. 6,961,281 (“Wong”) • U.S. Patent No. 6,996, 686 (“Doblar”) • U.S. Patent No. 6,757,751 (“Gene”) • U.S. Patent No. 6,742,098 (“Halbert”) • U.S. Patent No. 7,181,584 (“LaBerge”) • U.S. Patent No. 6,286,077 (“Choi”) • U.S. Patent No. 7,020,739 (“Mukaida”) • U.S. Patent App. Pub. No. 2007/0043922 (“Lee”) • U.S. Patent No. 7,414,312 (“Nguyen”) • DDR Functional Outlook; and/or • The knowledge of a person of ordinary skill in the art.
U.S. Patent No. 7,363,422 (“Perego ’422”)	• Asserted Patent’s Admitted Prior Art (“APA”) • U.S. Patent App. Pub. No. 20060117152 (“Amidi”) • U.S. Patent App. Pub. No. 2006/0277355 (“Ellsberry”) • U.S. Patent No. 7,240,145 (“Holman”) • JEDEC Standards • U.S. Patent No. 5,926,827 (“Dell’827”) • U.S. Patent No. 6,209,074 (“Dell’074”) • Micron DDR SDRAM RDIMM, MT36VDDF12872 & MT36VDDF25672 Product • DDR SDRAM Specification, JDEC Standard No. 79C, March 2003 • Kentron’s Quad Band Memory System (“QBM”) • U.S. Patent No. 6,961,281 (“Wong”) • U.S. Patent No. 6,996, 686 (“Doblar”) • U.S. Patent No. 6,757,751 (“Gene”) • U.S. Patent No. 6,742,098 (“Halbert”)

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U.S. Patent No. 5,926,827 (“Dell’827”)	• Asserted Patent’s Admitted Prior Art (“APA”) • U.S. Patent App. Pub. No. 20060117152 (“Amidi”) • U.S. Patent App. Pub. No. 2006/0277355 (“Ellsberry”) • U.S. Patent No. 7,240,145 (“Holman”) • JEDEC Standards • U.S. Patent No. 7,363,422 (“Perego ’422”) • U.S. Patent No. 6,209,074 (“Dell’074”) • Micron DDR SDRAM RDIMM, MT36VDDF12872 & MT36VDDF25672 Product • DDR SDRAM Specification, JDEC Standard No. 79C, March 2003 • Kentron’s Quad Band Memory System (“QBM”) • U.S. Patent No. 6,961,281 (“Wong”) • U.S. Patent No. 6,996, 686 (“Doblar”) • U.S. Patent No. 6,757,751 (“Gene”) • U.S. Patent No. 6,742,098 (“Halbert”) • U.S. Patent No. 7,181,584 (“LaBerge”) • U.S. Patent No. 6,286,077 (“Choi”) • U.S. Patent No. 7,020,739 (“Mukaida”) • U.S. Patent App. Pub. No. 2007/0043922 (“Lee”) • U.S. Patent No. 7,414,312 (“Nguyen”) • DDR Functional Outlook; and/or • The knowledge of a person of ordinary skill in the art.
U.S. Patent No. 6,209,074 (“Dell’074”)	• Asserted Patent’s Admitted Prior Art (“APA”) • U.S. Patent App. Pub. No. 20060117152 (“Amidi”) • U.S. Patent App. Pub. No. 2006/0277355 (“Ellsberry”) • U.S. Patent No. 7,240,145 (“Holman”)

	• JEDEC Standards • U.S. Patent No. 7,363,422 (“Perego ’422”) • U.S. Patent No. 5,926,827 (“Dell’827”) • Micron DDR SDRAM RDIMM, MT36VDDF12872 & MT36VDDF25672 Product • DDR SDRAM Specification, JDEC Standard No. 79C, March 2003 • Kentron’s Quad Band Memory System (“QBM”) • U.S. Patent No. 6,961,281 (“Wong”) • U.S. Patent No. 6,996, 686 (“Doblar”) • U.S. Patent No. 6,757,751 (“Gene”) • U.S. Patent No. 6,742,098 (“Halbert”) • U.S. Patent No. 7,181,584 (“LaBerge”) • U.S. Patent No. 6,286,077 (“Choi”) • U.S. Patent No. 7,020,739 (“Mukaida”) • U.S. Patent App. Pub. No. 2007/0043922 (“Lee”) • U.S. Patent No. 7,414,312 (“Nguyen”) • DDR Functional Outlook; and/or • The knowledge of a person of ordinary skill in the art.
Micron DDR SDRAM RDIMM, MT36VDDF12872 & MT36VDDF25672 Datasheet	• Asserted Patent’s Admitted Prior Art (“APA”) • U.S. Patent App. Pub. No. 20060117152 (“Amidi”) • U.S. Patent App. Pub. No. 2006/0277355 (“Ellsberry”) • U.S. Patent No. 7,240,145 (“Holman”) • JEDEC Standards • U.S. Patent No. 7,363,422 (“Perego ’422”) • U.S. Patent No. 5,926,827 (“Dell’827”) • U.S. Patent No. 6,209,074 (“Dell’074”) • DDR SDRAM Specification, JDEC Standard No. 79C, March 2003 • Kentron’s Quad Band Memory System (“QBM”) • U.S. Patent No. 6,961,281 (“Wong”) • U.S. Patent No. 6,996, 686 (“Doblar”) • U.S. Patent No. 6,757,751 (“Gene”) • U.S. Patent No. 6,742,098 (“Halbert”) • U.S. Patent No. 7,181,584 (“LaBerge”) • U.S. Patent No. 6,286,077 (“Choi”) • U.S. Patent No. 7,020,739 (“Mukaida”)

	• U.S. Patent App. Pub. No. 2007/0043922 (“Lee”) • U.S. Patent No. 7,414,312 (“Nguyen”) • DDR Functional Outlook; and/or • The knowledge of a person of ordinary skill in the art.
Micron DDR SDRAM RDIMM, MT36VDDF12872 and/or MT36VDDF25672 Products	• Asserted Patent’s Admitted Prior Art (“APA”) • U.S. Patent App. Pub. No. 20060117152 (“Amidi”) • U.S. Patent App. Pub. No. 2006/0277355 (“Ellsberry”) • U.S. Patent No. 7,240,145 (“Holman”) • JEDEC Standards • U.S. Patent No. 7,363,422 (“Perego ’422”) • U.S. Patent No. 5,926,827 (“Dell’827”) • U.S. Patent No. 6,209,074 (“Dell’074”) • DDR SDRAM Specification, JDEC Standard No. 79C, March 2003 • Kentron’s Quad Band Memory System (“QBM”) • U.S. Patent No. 6,961,281 (“Wong”) • U.S. Patent No. 6,996, 686 (“Doblar”) • U.S. Patent No. 6,757,751 (“Gene”) • U.S. Patent No. 6,742,098 (“Halbert”) • U.S. Patent No. 7,181,584 (“LaBerge”) • U.S. Patent No. 6,286,077 (“Choi”) • U.S. Patent No. 7,020,739 (“Mukaida”) • U.S. Patent App. Pub. No. 2007/0043922 (“Lee”) • U.S. Patent No. 7,414,312 (“Nguyen”) • DDR Functional Outlook; and/or • The knowledge of a person of ordinary skill in the art.
DDR SDRAM Specification, JDEC Standard No. 79C, March 2003	• Asserted Patent’s Admitted Prior Art (“APA”) • U.S. Patent App. Pub. No. 20060117152 (“Amidi”) • U.S. Patent App. Pub. No. 2006/0277355 (“Ellsberry”) • U.S. Patent No. 7,240,145 (“Holman”) • JEDEC Standards • U.S. Patent No. 7,363,422 (“Perego ’422”) • U.S. Patent No. 5,926,827 (“Dell’827”) • U.S. Patent No. 6,209,074 (“Dell’074”)

	• Micron DDR SDRAM RDIMM, MT36VDDF12872 & MT36VDDF25672 Product • Kentron's Quad Band Memory System ("QBM") • U.S. Patent No. 6,961,281 ("Wong") • U.S. Patent No. 6,996, 686 ("Doblar") • U.S. Patent No. 6,757,751 ("Gene") • U.S. Patent No. 6,742,098 ("Halbert") • U.S. Patent No. 7,181,584 ("LaBerge") • U.S. Patent No. 6,286,077 ("Choi") • U.S. Patent No. 7,020,739 ("Mukaida") • U.S. Patent App. Pub. No. 2007/0043922 ("Lee") • U.S. Patent No. 7,414,312 ("Nguyen") • DDR Functional Outlook; and/or • The knowledge of a person of ordinary skill in the art.
Kentron's Quad Band Memory System ("QBM")	• Asserted Patent's Admitted Prior Art ("APA") • U.S. Patent App. Pub. No. 20060117152 ("Amidi") • U.S. Patent App. Pub. No. 2006/0277355 ("Ellsberry") • U.S. Patent No. 7,240,145 ("Holman") • JEDEC Standards • U.S. Patent No. 7,363,422 ("Perego '422") • U.S. Patent No. 5,926,827 ("Dell '827") • U.S. Patent No. 6,209,074 ("Dell '074") • Micron DDR SDRAM RDIMM, MT36VDDF12872 & MT36VDDF25672 Product • U.S. Patent No. 6,961,281 ("Wong") • U.S. Patent No. 6,996, 686 ("Doblar") • U.S. Patent No. 6,757,751 ("Gene") • U.S. Patent No. 6,742,098 ("Halbert") • U.S. Patent No. 7,181,584 ("LaBerge") • U.S. Patent No. 6,286,077 ("Choi") • U.S. Patent No. 7,020,739 ("Mukaida") • U.S. Patent App. Pub. No. 2007/0043922 ("Lee") • U.S. Patent No. 7,414,312 ("Nguyen") • DDR Functional Outlook; and/or • The knowledge of a person of ordinary skill in the art.

U.S. Patent No. 6,961,281 (“Wong”)	• Asserted Patent’s Admitted Prior Art (“APA”) • U.S. Patent App. Pub. No. 20060117152 (“Amidi”) • U.S. Patent App. Pub. No. 2006/0277355 (“Ellsberry”) • U.S. Patent No. 7,240,145 (“Holman”) • JEDEC Standards • U.S. Patent No. 7,363,422 (“Perego ’422”) • U.S. Patent No. 5,926,827 (“Dell’827”) • U.S. Patent No. 6,209,074 (“Dell’074”) • Micron DDR SDRAM RDIMM, MT36VDDF12872 & MT36VDDF25672 Product • DDR SDRAM Specification, JDEC Standard No. 79C, March 2003 • Kentron’s Quad Band Memory System (“QBM”) • U.S. Patent No. 6,996, 686 (“Doblar”) • U.S. Patent No. 6,757,751 (“Gene”) • U.S. Patent No. 6,742,098 (“Halbert”) • U.S. Patent No. 7,181,584 (“LaBerge”) • U.S. Patent No. 6,286,077 (“Choi”) • U.S. Patent No. 7,020,739 (“Mukaida”) • U.S. Patent App. Pub. No. 2007/0043922 (“Lee”) • U.S. Patent No. 7,414,312 (“Nguyen”) • DDR Functional Outlook; and/or • The knowledge of a person of ordinary skill in the art.
U.S. Patent No. 6,996, 686 (“Doblar”)	• Asserted Patent’s Admitted Prior Art (“APA”) • U.S. Patent App. Pub. No. 20060117152 (“Amidi”) • U.S. Patent App. Pub. No. 2006/0277355 (“Ellsberry”) • U.S. Patent No. 7,240,145 (“Holman”) • JEDEC Standards • U.S. Patent No. 7,363,422 (“Perego ’422”) • U.S. Patent No. 5,926,827 (“Dell ’827”) • U.S. Patent No. 6,209,074 (“Dell ’074”) • Micron DDR SDRAM RDIMM, MT36VDDF12872 & MT36VDDF25672 Product • DDR SDRAM Specification, JDEC Standard No. 79C, March 2003

	• Kentron’s Quad Band Memory System (“QBM”) • U.S. Patent No. 6,961,281 (“Wong”) • U.S. Patent No. 6,757,751 (“Gene”) • U.S. Patent No. 6,742,098 (“Halbert”) • U.S. Patent No. 7,181,584 (“LaBerge”) • U.S. Patent No. 6,286,077 (“Choi”) • U.S. Patent No. 7,020,739 (“Mukaida”) • U.S. Patent App. Pub. No. 2007/0043922 (“Lee”) • U.S. Patent No. 7,414,312 (“Nguyen”) • DDR Functional Outlook; and/or • The knowledge of a person of ordinary skill in the art.
U.S. Patent No. 6,757,751 (“Gene”)	• Asserted Patent’s Admitted Prior Art (“APA”) • U.S. Patent App. Pub. No. 20060117152 (“Amidi”) • U.S. Patent App. Pub. No. 2006/0277355 (“Ellsberry”) • U.S. Patent No. 7,240,145 (“Holman”) • JEDEC Standards • U.S. Patent No. 7,363,422 (“Perego ’422”) • U.S. Patent No. 5,926,827 (“Dell ’827”) • U.S. Patent No. 6,209,074 (“Dell d’074”) • Micron DDR SDRAM RDIMM, MT36VDDF12872 & MT36VDDF25672 Product • DDR SDRAM Specification, JEDEC Standard No. 79C, March 2003 • Kentron’s Quad Band Memory System (“QBM”) • U.S. Patent No. 6,961,281 (“Wong”) • U.S. Patent No. 6,996, 686 (“Doblar”) • U.S. Patent No. 6,742,098 (“Halbert”) • U.S. Patent No. 7,181,584 (“LaBerge”) • U.S. Patent No. 6,286,077 (“Choi”) • U.S. Patent No. 7,020,739 (“Mukaida”) • U.S. Patent App. Pub. No. 2007/0043922 (“Lee”) • U.S. Patent No. 7,414,312 (“Nguyen”) • DDR Functional Outlook; and/or • The knowledge of a person of ordinary skill in the art.
U.S. Patent No. 6,742,098 (“Halbert”)	• Asserted Patent’s Admitted Prior Art (“APA”)

	• U.S. Patent App. Pub. No. 20060117152 (“Amidi”) • U.S. Patent App. Pub. No. 2006/0277355 (“Ellsberry”) • U.S. Patent No. 7,240,145 (“Holman”) • JEDEC Standards • U.S. Patent No. 7,363,422 (“Perego ’422”) • U.S. Patent No. 5,926,827 (“Dell ’827”) • U.S. Patent No. 6,209,074 (“Dell ’074”) • Micron DDR SDRAM RDIMM, MT36VDDF12872 & MT36VDDF25672 Product • DDR SDRAM Specification, JEDEC Standard No. 79C, March 2003 • Kentron’s Quad Band Memory System (“QBM”) • U.S. Patent No. 6,961,281 (“Wong”) • U.S. Patent No. 6,996, 686 (“Doblar”) • U.S. Patent No. 6,757,751 (“Gene”) • U.S. Patent No. 7,181,584 (“LaBerge”) • U.S. Patent No. 6,286,077 (“Choi”) • U.S. Patent No. 7,020,739 (“Mukaida”) • U.S. Patent App. Pub. No. 2007/0043922 (“Lee”) • U.S. Patent No. 7,414,312 (“Nguyen”) • DDR Functional Outlook; and/or • The knowledge of a person of ordinary skill in the art.
U.S. Patent No. 7,181,584 (“LaBerge”)	• Asserted Patent’s Admitted Prior Art (“APA”) • U.S. Patent App. Pub. No. 20060117152 (“Amidi”) • U.S. Patent App. Pub. No. 2006/0277355 (“Ellsberry”) • U.S. Patent No. 7,240,145 (“Holman”) • JEDEC Standards • U.S. Patent No. 7,363,422 (“Perego ’422”) • U.S. Patent No. 5,926,827 (“Dell ’827”) • U.S. Patent No. 6,209,074 (“Dell ’074”) • Micron DDR SDRAM RDIMM, MT36VDDF12872 & MT36VDDF25672 Product • DDR SDRAM Specification, JEDEC Standard No. 79C, March 2003

	• Kentron’s Quad Band Memory System (“QBM”) • U.S. Patent No. 6,961,281 (“Wong”) • U.S. Patent No. 6,996, 686 (“Doblar”) • U.S. Patent No. 6,757,751 (“Gene”) • U.S. Patent No. 6,742,098 (“Halbert”) • U.S. Patent No. 6,286,077 (“Choi”) • U.S. Patent No. 7,020,739 (“Mukaida”) • U.S. Patent App. Pub. No. 2007/0043922 (“Lee”) • U.S. Patent No. 7,414,312 (“Nguyen”) • DDR Functional Outlook; and/or • The knowledge of a person of ordinary skill in the art.
U.S. Patent No. 6,286,077 (“Choi”)	• Asserted Patent’s Admitted Prior Art (“APA”) • U.S. Patent App. Pub. No. 20060117152 (“Amidi”) • U.S. Patent App. Pub. No. 2006/0277355 (“Ellsberry”) • U.S. Patent No. 7,240,145 (“Holman”) • JEDEC Standards • U.S. Patent No. 7,363,422 (“Perego ’422”) • U.S. Patent No. 5,926,827 (“Dell ’827”) • U.S. Patent No. 6,209,074 (“Dell ’074”) • Micron DDR SDRAM RDIMM, MT36VDDF12872 & MT36VDDF25672 Product • DDR SDRAM Specification, JEDEC Standard No. 79C, March 2003 • Kentron’s Quad Band Memory System (“QBM”) • U.S. Patent No. 6,961,281 (“Wong”) • U.S. Patent No. 6,996, 686 (“Doblar”) • U.S. Patent No. 6,757,751 (“Gene”) • U.S. Patent No. 6,742,098 (“Halbert”) • U.S. Patent No. 7,181,584 (“LaBerge”) • U.S. Patent No. 7,020,739 (“Mukaida”) • U.S. Patent App. Pub. No. 2007/0043922 (“Lee”) • U.S. Patent No. 7,414,312 (“Nguyen”) • DDR Functional Outlook; and/or • The knowledge of a person of ordinary skill in the art.
U.S. Patent No. 7,020,739 (“Mukaida”)	• Asserted Patent’s Admitted Prior Art (“APA”)

	• U.S. Patent App. Pub. No. 20060117152 (“Amidi”) • U.S. Patent App. Pub. No. 2006/0277355 (“Ellsberry”) • U.S. Patent No. 7,240,145 (“Holman”) • JEDEC Standards • U.S. Patent No. 7,363,422 (“Perego ’422”) • U.S. Patent No. 5,926,827 (“Dell ’827”) • U.S. Patent No. 6,209,074 (“Dell ’074”) • Micron DDR SDRAM RDIMM, MT36VDDF12872 & MT36VDDF25672 Product • DDR SDRAM Specification, JEDEC Standard No. 79C, March 2003 • Kentron’s Quad Band Memory System (“QBM”) • U.S. Patent No. 6,961,281 (“Wong”) • U.S. Patent No. 6,996, 686 (“Doblar”) • U.S. Patent No. 6,757,751 (“Gene”) • U.S. Patent No. 6,742,098 (“Halbert”) • U.S. Patent No. 7,181,584 (“LaBerge”) • U.S. Patent No. 6,286,077 (“Choi”) • U.S. Patent App. Pub. No. 2007/0043922 (“Lee”) • U.S. Patent No. 7,414,312 (“Nguyen”) • DDR Functional Outlook; and/or • The knowledge of a person of ordinary skill in the art.
U.S. Patent App. Pub. No. 2007/0043922 (“Lee”)	• Asserted Patent’s Admitted Prior Art (“APA”) • U.S. Patent App. Pub. No. 20060117152 (“Amidi”) • U.S. Patent App. Pub. No. 2006/0277355 (“Ellsberry”) • U.S. Patent No. 7,240,145 (“Holman”) • JEDEC Standards • U.S. Patent No. 7,363,422 (“Perego ’422”) • U.S. Patent No. 5,926,827 (“Dell ’827”) • U.S. Patent No. 6,209,074 (“Dell ’074”) • Micron DDR SDRAM RDIMM, MT36VDDF12872 & MT36VDDF25672 Product • DDR SDRAM Specification, JEDEC Standard No. 79C, March 2003

	• Kentron’s Quad Band Memory System (“QBM”) • U.S. Patent No. 6,961,281 (“Wong”) • U.S. Patent No. 6,996, 686 (“Doblar”) • U.S. Patent No. 6,757,751 (“Gene”) • U.S. Patent No. 6,742,098 (“Halbert”) • U.S. Patent No. 7,181,584 (“LaBerge”) • U.S. Patent No. 6,286,077 (“Choi”) • U.S. Patent No. 7,020,739 (“Mukaida”) • U.S. Patent No. 7,414,312 (“Nguyen”) • DDR Functional Outlook; and/or • The knowledge of a person of ordinary skill in the art.
U.S. Patent No. 7,414,312 (“Nguyen”)	• Asserted Patent’s Admitted Prior Art (“APA”) • U.S. Patent App. Pub. No. 20060117152 (“Amidi”) • U.S. Patent App. Pub. No. 2006/0277355 (“Ellsberry”) • U.S. Patent No. 7,240,145 (“Holman”) • JEDEC Standards • U.S. Patent No. 7,363,422 (“Perego ’422”) • U.S. Patent No. 5,926,827 (“Dell’827”) • U.S. Patent No. 6,209,074 (“Dell’074”) • Micron DDR SDRAM RDIMM, MT36VDDF12872 & MT36VDDF25672 Product • DDR SDRAM Specification, JEDEC Standard No. 79C, March 2003 • Kentron’s Quad Band Memory System (“QBM”) • U.S. Patent No. 6,961,281 (“Wong”) • U.S. Patent No. 6,996, 686 (“Doblar”) • U.S. Patent No. 6,757,751 (“Gene”) • U.S. Patent No. 6,742,098 (“Halbert”) • U.S. Patent No. 7,181,584 (“LaBerge”) • U.S. Patent No. 6,286,077 (“Choi”) • U.S. Patent No. 7,020,739 (“Mukaida”) • U.S. Patent App. Pub. No. 2007/0043922 (“Lee”) • DDR Functional Outlook; and/or • The knowledge of a person of ordinary skill in the art.
DDR Functional Outlook	• Asserted Patent’s Admitted Prior Art (“APA”)

	• U.S. Patent App. Pub. No. 20060117152 (“Amidi”) • U.S. Patent App. Pub. No. 2006/0277355 (“Ellsberry”) • U.S. Patent No. 7,240,145 (“Holman”) • JEDEC Standards • U.S. Patent No. 7,363,422 (“Perego ’422”) • U.S. Patent No. 5,926,827 (“Dell ’827”) • U.S. Patent No. 6,209,074 (“Dell ’074”) • Micron DDR SDRAM RDIMM, MT36VDDF12872 & MT36VDDF25672 Product • DDR SDRAM Specification, JEDEC Standard No. 79C, March 2003 • Kentron’s Quad Band Memory System (“QBM”) • U.S. Patent No. 6,961,281 (“Wong”) • U.S. Patent No. 6,996, 686 (“Doblar”) • U.S. Patent No. 6,757,751 (“Gene”) • U.S. Patent No. 6,742,098 (“Halbert”) • U.S. Patent No. 7,181,584 (“LaBerge”) • U.S. Patent No. 6,286,077 (“Choi”) • U.S. Patent No. 7,020,739 (“Mukaida”) • U.S. Patent App. Pub. No. 2007/0043922 (“Lee”) • U.S. Patent No. 7,414,312 (“Nguyen”); and/or • The knowledge of a person of ordinary skill in the art.
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As mentioned above, Defendants have not yet completed their search or discovery concerning additional prior art. Moreover, the exemplary combinations are provided based on Defendants’ current understanding of the Asserted Claims and Plaintiff’s apparent view of the scope of those claims as shown, for example, in Plaintiff’s Infringement Contentions. Further, a *Markman* Order has not yet been issued in this case. As such, Defendants’ inclusion of exemplary combinations does not preclude them from identifying other invalidating combinations as appropriate, and Defendants reserve the right to identify additional specific combinations as well as to detail and explain such combinations.

2. U.S. Patent No. 9,858,215

Pursuant to P.R. 3-3(a) and (b), Defendants identify in Appendix B the prior art references that render obvious the Asserted Claims of the '215 patent and include below exemplary combinations showing the obviousness of the '215 patent Asserted Claims in view of the prior art. To the extent Plaintiff contends that an element is not disclosed in any one of the anticipatory references described in Appendix B, the limitation would have been obvious in light of the disclosures within the reference and the knowledge of one of ordinary skill in the art at the time of the '215 patent. Moreover, to the extent Plaintiff contends that an element is not disclosed in any one of the anticipatory references described in Appendix B, such reference may be combined with any other references listed in Appendix B for such element, thereby rendering the claims invalid for obviousness.

To the extent a finder of fact determines that a limitation of any of the '215 patent Asserted Claims is not disclosed by one of the references identified above pursuant to P.R. 3-3(a), the claim is nevertheless unpatentable as obvious because they contain nothing that constitutes a patentable innovation. To the extent a finder of fact determines that a limitation of the '215 patent Asserted Claims is not anticipated, it does not go beyond combining familiar elements according to known methods to achieve predictable results or does more than choose between clear alternatives known to those of ordinary skill in the art.

(a) Obviousness Rationale

For at least the reasons described in these contentions, it would have been obvious to one of ordinary skill in the art to combine any of a number of prior art references, including any combination of those prior art references identified in Appendix B along with the knowledge of one of ordinary skill in the art to meet the limitations of the '215 patent Asserted Claims.

Moreover, as mentioned above, Defendants have not yet completed their search or discovery concerning additional prior art. As such, Defendants' inclusion of exemplary combinations does not preclude them from identifying other invalidating combinations as appropriate, and Defendants reserve the right to identify additional specific combinations as well as to detail and explain such combinations.

To the extent not anticipated, the '215 patent Asserted Claims represent no more than the result of ordinary variations of the prior art. Defendants further believe that no showing of a specific motivation to combine prior art is required to combine the references disclosed above and in the attached charts, as each combination of art would have no unexpected results, and at most would simply represent a known alternative to one of ordinary skill in the art. *See KSR Int'l Co. v. Teleflex, Inc.*, 550 U.S. 398, 415-16 (2007) (rejecting the Federal Circuit's "rigid" application of the teaching, suggestion, or motivation to combine test, instead espousing an "expansive and flexible" approach). Indeed, the Supreme Court held that a person of ordinary skill in the art is "a person of ordinary creativity, not an automaton" and "in many cases a person of ordinary skill in the art will be able to fit the teachings of multiple patents together like pieces of a puzzle." *Id.* at 420-21. Nevertheless, in addition to the information contained elsewhere in these contentions, Defendants identify motivation and reason to combine the cited art.

One or more combinations of the prior art references identified in Appendix B would have been obvious because these references would have been combined using: known methods to yield predictable results; known techniques in the same way; a simple substitution of one known, equivalent element for another to obtain predictable results; and/or a teaching, suggestion, or motivation in the prior art generally. In addition, it would have been obvious to try combining the prior art references identified above because there were only a finite number

of predictable solutions and/or because known work in one field of endeavor prompted variations based on predictable design incentives and/or market forces either in the same field or a different one. Further, the combinations of the prior art references identified in Appendix B would have been obvious because the combinations represent known potential options with a reasonable expectation of success.

Additional evidence that there would have been a motivation to combine the prior art references identified above includes the interrelated teachings of multiple prior art references; common authorship; the effects of demands known to the design community or present in the marketplace; the existence of a known problem for which there was an obvious solution encompassed by the '215 patent Asserted Claims; the existence of a known need or problem in the field of the endeavor at the time of the alleged invention(s); and the background knowledge that would have been possessed by a person having ordinary skill in the art.

Thus, the motivation to combine the teachings of the prior art references disclosed in Appendix B is found in the references themselves and also in: (1) the nature of the problem being solved; (2) the express, implied and inherent teachings of the prior art; (3) the knowledge of persons of ordinary skill in the art; (4) the predictable results obtained in combining the different elements of the prior art; (5) the predictable results obtained in simple substitution of one known element for another; (6) the use of a known technique to improve similar devices, methods, or products in the same way; (7) the predictable results obtained in applying a known technique to a known device, method, or product ready for improvement; (8) the finite number of identified predictable solutions that had a reasonable expectation of success; and (9) known work in various technological fields that could be applied to the same or different technological fields based on design incentives or other market forces.

Additionally, it would be obvious to one of ordinary skill in the art to consult and/or combine any of the prior art listed in Appendix B because all of these references relate to the same area of technology and/or are from analogous art. The '215 patent Asserted Claims are generally directed to a memory module with data buffering. *See, e.g.*, '215 patent at Title, Abstract, 20:48-22:57. The '215 patent Asserted Claims merely unite old elements, well-known in the field, with no change in their respective function or result. Given the interrelated teachings of the prior art, the effects of demands known to the design community or present in the marketplace, and the background knowledge possessed by a person having ordinary skill in the art, it would have been obvious for one of ordinary skill in the art to combine these familiar elements, disclosed and/or embodied in the prior art listed above to practice the '215 patent Asserted Claims.

The '215 Patent purports to describe “devices and methods for improving the performance, the memory capacity, or both, of memory modules.” '215 patent at 1:42-45. All of the '215 patent Asserted Claims generally concern a memory module operable in a computer system which purportedly configured to buffer certain control signals. Such technology, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff’s infringement contentions, was widely known before the alleged priority date of the '215 Patent, as evidenced by the references in Appendix B. *See, e.g.*, '215 patent at 1:46-56, 1:57-2:40, 2:41-47, 2:59-67, 6:4-23, 6:60-7:13, 9:7-17, 13:51-14:18, 17:57-18:9, 18:10-29, 21:35-40; *see also* Ex. B1 (the '215 Patent’s Admitted Prior Art).

One of ordinary skill in the art would have been motivated to combine any of the references in Appendix B because at the time of the alleged invention improving a memory module’s capacity (density) was a common problem with well-known solutions. *See, e.g.*, '215

patent at 2:48-58, 13:51-14:4; Ellsberry at Abstract, [0005], [0010], [0012]; Holman at 2:43-54; Perego '422 at 1:18-30; Amidi at [0002], [0008]; Halbert '518 at 3:32-41; Halbert '119 at [0022]; Halbert '250 at 3:35-42; Rao at 2:1-8; MicronRDIMM at 1, 6-8, 18-20; JEDEC Standards (*see, e.g.*, JEDEC Standard 21-C at 4.20.4-5, 4.20.4-25 through 4.20.4-27, JESD79 at 1, 2, 8; JESD79-2 at 10, 12; JESD79C at 1, 7, 8); QBM (*see, e.g.*, QBM Specification Rev. 0.93 at 5, 9; QBM2 Interface Overview at 3; QBM2 Technical Features Overview at 3-5; QBM Doubling DDR Memory Bandwidth at 10); Mailloux at 1:31-35, 2:26-46; LaBerge '032 at 1:42-65; FBDIMM Architecture & Protocol (*see, e.g.*, FBDIMM AP Rev. 0.1 at 7); Dell '074 at 1:44-67; Gene at 1:61-2:22; Wong '281 at 2:4-19; Wong '868 at 1:57-2:10, 2:66-3:4; Johnson at 1:36-52; Kim at Abstract, 1:6-11, 3:21-26; McCall at 1:8-20; *see also* Appendix B.

Further, it was common knowledge to one of ordinary skill in the art at the time of the alleged invention that memory density (rank) multiplication can improve performance and/or reduce costs of the memory modules. *See, e.g.*, '215 patent at 13:51-14:18; *see also* Amidi at [0008]-[0011]; Ellsberry at Abstract, [0005], [0010], [0012]; Holman at 1:58-2:6, 2:43-54; Perego '422 at 1:18-30; Halbert '518 at 3:32-41; Halbert '119 at Abstract; Halbert '250 at 3:35-42; MicronRDIMM at 1, 6-8, 18-20; JEDEC Standards (*see, e.g.*, JESD79C at 1, 2, 5, 8); QBM; *see also* Appendix B. Furthermore, it was well known to one of ordinary skill in the art at the time of the alleged invention that the use of buffer devices to isolate signals (e.g., data, control, and address signals) of memory devices also improves memory capacity and enhances performance, among other advantageous effects. *See, e.g.*, Perego '422 at 3:23-40, 4:38-45, 6:12-56; Perego '896 at 5:46-6:11, 6:62-7:18, 11:3-18, 12:4-19; Mailloux at 12:65-13:13, 13:26-30, 14:46-15:3; Halbert '518 at 3:42-57, 4:23-35, 9:4-19; LaBerge '841 at 2:23-27; Halbert '119 at [0023], [0024], [0026]; Halbert '250 at Abstract, 9:28-37; McCall at 1:47-54, 2:12-38;

Ellsberry at [0039]; Klein at [0022], [0026], [0028], [0039]; JEDEC Standards; JEDEC Standard 21-C at 7, 71; JESD79-2A at 14, 51; QBM (*see, e.g.*, QBM Specification Rev. 0.93 at 6, 9-11, 34, 36; QBM2 Interface Overview at 3; QBM Informational Showing Item #1133 at 4-8; QBM Informational Showing Item #1341 at 3, 9, 15; QBM2 Technical Features Overview at 3-5, 14; QBM2 Technical Highlights at 19; QBM Platform Conference at 17-22; QBM Doubling DDR Memory Bandwidth at 8; QBM Doubling DDR Memory Bandwidth at 11-13; QBM2 Technology Overview at 5, 8, 11, 12, 15, 17; QBM Interim JEDEC Meeting at 6, 11); DDR3 Functional Outlook at 6, 10-12, 14-20, 22; Dodd at 1:64-2:13; Averbuj at [0048]; *see also* Appendix B.

One of ordinary skill in the art would have been motivated to combine any of the references in Appendix B at the time of the alleged invention. Common problems with conventional techniques for improving a memory module's capacity or density, improve performance, flexibility, and other memory characteristics were known to persons of ordinary skill in the art and implementing memory density multiplication, signal buffering, and data isolation were well-known solutions to achieve improved performance and capacity. *See, e.g.*, '215 patent at 13:51-14:18; *see also* Amidi at [0008]-[0011]; Ellsberry at Abstract, [0005], [0010], [0012]; Holman at 1:58-2:6, 2:43-54; Perego '422 at 1:18-30, 3:23-40, 4:38-45, 6:12-56; Perego '896 at 5:46-6:11, 6:62-7:18, 11:3-18, 12:4-19; Halbert '518 at 3:42-57, 4:23-35, 9:4-19; LaBerge '841 at 2:23-27; Halbert '119 at [0023], [0024], [0026]; Halbert '250 at Abstract, 3:32-41, 9:28-37; McCall at 1:47-54, 2:12-38; Mailloux at 1:31-35, 2:26-46, 12:65-13:13, 13:26-30, 14:46-15:3; Klein at [0039]; DDR3 Functional Outlook at 6, 10-12, 14-20, 22; MicronRDIMM at 1, 6-8, 18-20; QBM (*see, e.g.*, QBM Specification Rev. 0.93 at 6, 9-11, 34, 36; QBM2 Interface Overview at 3; QBM Informational Showing Item #1133 at 4-8; QBM Informational

Showing Item #1341 at 3, 9, 15; QBM2 Technical Features Overview at 3-5, 14; QBM2 Technical Highlights at 19; QBM Platform Conference at 17-22; QBM Doubling DDR Memory Bandwidth at 8; QBM Doubling DDR Memory Bandwidth at 11-13; QBM2 Technology Overview at 5, 8, 11, 12, 15, 17; QBM Interim JEDEC Meeting at 6, 11); JEDEC Standards; JEDEC Standard 21-C at 7, 25-27, 71; JESD79-2A at 14, 51; FBDIMM Architecture & Protocol (*see, e.g.*, FBDIMM AP Rev. 0.1 at 7); Jacob at 1, 2; *see also* Appendix B.

It was well-known to one of ordinary skill in the art before the time of the '215 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that a memory module can be operable in a computer system to communicate data with a memory controller of the computer system via a memory bus in response to memory commands received from the memory controller. *See* citations identified for claim element 1[pre] provided in attached Exhibits B1 through B21.

It was well-known to one of ordinary skill in the art before the time of the '215 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that memory commands can include a first memory command and a subsequent second memory command, the first memory command to cause the memory module to receive or output a first data burst and the second memory command to cause the memory module to receive or output a second data burst. *See* citations identified for claim element 1[pre] provided in attached Exhibits B1 through B21.

It was well-known to one of ordinary skill in the art before the time of the '215 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that a memory module can include a printed circuit board having a plurality of edge connections configured to be electrically coupled to a corresponding plurality of

contacts of a module slot of the computer system. *See* citations identified for claim element 1[a] provided in attached Exhibits B1 through B21.

It was well-known to one of ordinary skill in the art before the time of the '215 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that a memory module can include a register coupled to the printed circuit board and configured to receive and buffer first command and address signals representing the first memory command, and to receive and buffer second command and address signals representing the second memory command. *See* citations identified for claim element 1[b] provided in attached Exhibits B1 through B21.

It was well-known to one of ordinary skill in the art before the time of the '215 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that a memory module can include a plurality of memory integrated circuits mounted on the printed circuit board and arranged in a plurality of ranks including a first rank and a second rank, the plurality of memory integrated circuits including at least one first memory integrated circuit in the first rank and at least one second memory integrated circuit in the second rank. *See* citations identified for claim element 1[c] provided in attached Exhibits B1 through B21.

It was well-known to one of ordinary skill in the art before the time of the '215 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that the first rank can be selected to receive or output the first data burst in response to the first memory command and not be selected to communicate data with the memory controller in response to the second memory command. *See* citations identified for claim element 1[c] provided in attached Exhibits B1 through B21.

It was well-known to one of ordinary skill in the art before the time of the '215 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that the second rank can be selected to receive or output the second data burst in response to the second memory command and not be selected to communicate data with the memory controller in response to the first memory command. *See* citations identified for claim element 1[c] provided in attached Exhibits B1 through B21.

It was well-known to one of ordinary skill in the art before the time of the '215 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that a memory module can include a buffer coupled between the at least one first memory integrated circuit and the memory bus, and between the at least one second memory integrated circuit and the memory bus. *See* citations identified for claim element 1[d] provided in attached Exhibits B1 through B21.

It was well-known to one of ordinary skill in the art before the time of the '215 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that a memory module can include logic coupled to the buffer and configured to respond to the first memory command by providing first control signals to the buffer to enable communication of the first data burst between the at least one first memory integrated circuit and the memory controller through the buffer. *See* citations identified for claim element 1[e] provided in attached Exhibits B1 through B21.

It was well-known to one of ordinary skill in the art before the time of the '215 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that the logic can be configured to respond to the second memory command by providing second control signals to the buffer to enable communication of the

second data burst between the at least one second memory integrated circuit and the memory controller through the buffer, the second control signals being different from the first control signals. *See* citations identified for claim element 1[e] provided in attached Exhibits B1 through B21.

It was well-known to one of ordinary skill in the art before the time of the '215 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, a method of operating a memory module coupled to a memory controller via a memory bus, and that the memory module can comprise memory integrated circuits arranged in ranks and mounted on a printed circuit board having a plurality of edge connections coupled to the memory bus, and that the memory integrated circuits can include at least one first memory integrated circuit in a first rank and at least one second memory integrated circuit in a second rank. *See* citations identified for claim element 21[pre] provided in attached Exhibits B1 through B21.

It was well-known to one of ordinary skill in the art before the time of the '215 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that a method for operating a memory module can include receiving at one or more circuits coupled to the printed circuit board a first set of input command and address signals representing a first memory command from the memory controller via the memory bus, the first memory command to cause the memory module to receive or output a first data burst. *See* citations identified for claim element 21[a] provided in attached Exhibits B1 through B21.

It was well-known to one of ordinary skill in the art before the time of the '215 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that a method for operating a memory module can include generating a

first set of output command and address signals in response to the first set of input command and address signals, the first set of output command and address signals selecting the first rank to receive or output the first data burst. *See* citations identified for claim element 21[b] provided in attached Exhibits B1 through B21.

It was well-known to one of ordinary skill in the art before the time of the '215 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that a method for operating a memory module can include receiving at the one or more circuits a second set of input command and address signals representing a second memory command from the memory controller via the memory bus, the second memory command to cause the memory module to receive or output a second data burst. *See* citations identified for claim element 21[c] provided in attached Exhibits B1 through B21.

It was well-known to one of ordinary skill in the art before the time of the '215 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that a method for operating a memory module can include generating a second set of output command and address signals in response to the second set of input command and address signals, the second set of output command and address signals selecting the second rank to receive or output the second data burst. *See* citations identified for claim element 21[d] provided in attached Exhibits B1 through B21.

It was well-known to one of ordinary skill in the art before the time of the '215 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that a method for operating a memory module can include, in response to the first memory command, providing first control signals to a buffer to enable communication of the first data burst between the at least one first memory integrated circuit and

the memory controller through the buffer. *See* citations identified for claim element 21[e] provided in attached Exhibits B1 through B21.

It was well-known to one of ordinary skill in the art before the time of the '215 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that a method for operating a memory module can include, in response to the second memory command, providing second control signals to the buffer to enable communication of the second data burst between the at least one second memory integrated circuit and the memory controller through the buffer, the second control signals being different from the first control signals. *See* citations identified for claim element 21[f] provided in attached Exhibits B1 through B21.

It was well-known to one of ordinary skill in the art before the time of the '215 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that the buffer can be configured to isolate both the at least one first memory integrated circuit and the at least one second memory integrated circuit from the memory bus when the memory module is not being accessed by the memory controller. *See* citations identified for claims 2, 22 provided in attached Exhibits B1 through B21.

It was well-known to one of ordinary skill in the art before the time of the '215 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that a memory module can have an overall CAS latency greater than an actual operational CAS latency of each of the plurality of memory integrated circuits. *See* citations identified for claims 3 and 24 provided in attached Exhibits B1 through B21; Yoon at Fig. 3, Fig. 5, 1:31-67, 2:1-24, 2:63-3:12, 5:25-36, 7:12-32; Lee '287 at 1:17-25, 6:19-7:14, 7:61-65, 8:8-15, 10:5-13; Lee '938 at 1:45-67, 5:20-41, 10:17-48, 12:35-61; Jang at 1:28-50, 2:4-11,

5:48-6:13.

It was well-known to one of ordinary skill in the art before the time of the '215 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that a memory module can further comprise an SPD device that reports an overall CAS latency of the memory module to the memory controller, the overall CAS latency having one more clock cycle than an actual operational CAS latency of each of the plurality of memory integrated circuits. *See* citations identified for claim 4 provided in attached Exhibits B1 through B21; Lee '287 at 1:17-35, 2:25-47, 4:28-49, 7:5-14, 7:61-65, 8:8-15, 8:64- 9:4; 10:5-13; Lee '938 at Abstract, 1:45-67, 5:20-67, 7:18--64, 10:17-67, 12:35-61; Jang at Abstract, Fig. 1, Fig. 2, 1:28-50, 2:4-11, 3:7-48, 3:49-4:53, 4:54-5:9 5:10-6:13.

It was well-known to one of ordinary skill in the art before the time of the '215 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that a memory module can be a dual in-line memory module (DIMM), and the plurality of memory integrated circuits can be double-data-rate dynamic random access memory (DRAM) circuits. *See* citations identified for claims 5 and 27 provided in attached Exhibits B1 through B21.

It was well-known to one of ordinary skill in the art before the time of the '215 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that a memory module can determine a latency value, wherein the communication of the first data burst between the at least one first memory integrated circuit and the memory controller can be enabled in accordance with the latency value. *See* citations identified for claim 6 provided in attached Exhibits B1 through B21; Yoon at Abstract, Fig. 1, Fig. 3, Fig. 5, 1:31-2:39, 2:63-3:12, 3:20-45, 4:16-5:15; Lee '287 at 1:17-62, 2:25-59, 4:10-63,

4:64-5:27, 5:45-6:8; Lee '938 at Abstract, 1:45-67, 5:20-41, 7:57-64, 10:17-52, 12:35-61; Jang at Abstract, Fig. 1, Fig. 2, 1:28-50, 2:4-11, 3:7-48, 3:49-67; 4:54-5:13.

It was well-known to one of ordinary skill in the art before the time of the '215 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that a memory module can be further coupled to the memory controller using an on-die-termination (ODT) bus, wherein each of the plurality of memory devices can include an ODT circuit, the memory module can further comprise a termination circuit external to any of the plurality of memory devices, wherein the termination circuit can be coupled to the ODT bus and to the ODT circuit of at least one of the plurality of memory devices, wherein the termination circuit can be configured to provide external termination of the at least one of the plurality of memory devices in response to an ODT signal on the ODT bus, and wherein the ODT circuit in the at least one of the plurality of memory devices can be disabled. *See* citations identified for claim 7 provided in attached Exhibits B1 through B21.

It was well-known to one of ordinary skill in the art before the time of the '215 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that a memory module can have a buffer comprising combinatorial logic, registers, and logic pipelines, and which is configured to register an additional clock cycle for transferring the first data burst or the second data burst through the buffer. *See* citations identified for claims 8, 17, and 20 provided in attached Exhibits B1 through B21; Lee '287 at 3:16-4:9, 4:64-5:27, 5:45-60, 9:5-25, 9:42-10:13; Lee '938 at 7:41-8:12, 9:40-59.

It was well-known to one of ordinary skill in the art before the time of the '215 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that a first memory command can include at least one first chip select

signal and a second memory command that can include at least one second chip select signal.

See citations identified for claim 9 provided in attached Exhibits B1 through B21.

It was well-known to one of ordinary skill in the art before the time of the '215 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that a memory module can produce at least third and fourth chip select signals in response to the first memory command, the third chip select signal being provided to the at least one first memory integrated circuit and having an active value to cause the at least one first memory integrated circuit to receive or output data signals in response to the first memory command, the fourth chip-select signal being provided to the at least one second memory integrated circuit and having a non-active value to keep the at least one second memory integrated circuit from receiving or outputting data signals in response to the first memory command. See citations identified for claim 10 provided in attached Exhibits B1 through B21.

It was well-known to one of ordinary skill in the art before the time of the '215 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that a memory module can produce at least fifth and sixth chip select signals in response to the second memory command, the fifth chip select signal being provided to the at least one first memory integrated circuit and having a non-active value to keep the at least one first memory integrated circuit from receiving or outputting data signals in response to the first memory command, the sixth chip select signal being provided to the at least one second memory integrated circuit and having an active value to cause the at least one second memory integrated circuit to receive or output data signals in response to the second memory command. See citations identified for claim 11 provided in attached Exhibits B1 through B21.

It was well-known to one of ordinary skill in the art before the time of the '215 patent, at

least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that in a memory module, the first memory command can be a first read command and the second memory command can be a second read command, wherein the first read command and the second read command can be back to back adjacent read commands, and wherein the memory module can output the first data burst together with a first burst of data strobe signals in response to the first read command, wherein memory module can output the second data burst together with a second burst of data strobe signals in response to the second read command, wherein the second data burst can follow the first data burst on the memory bus, and wherein the buffer can be configured to prevent the first burst of data strobe signals and the second burst of data strobe signals from colliding with each other. *See* citations identified for claim 12 provided in attached Exhibits B1 through B21.

It was well-known to one of ordinary skill in the art before the time of the '215 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that in a memory module, each of the first burst of data strobe signals and the second burst of data strobe signals can include a pre-amble interval and a post-amble interval, and wherein the buffer can be configured to combine the first burst of data strobe signals and the second burst of data strobe signals into a combined burst of data strobe signals that does not include the post-amble interval of the first burst of data strobe signals and the pre-amble interval of the second burst of data strobe signals. *See* citations identified for claim 13 provided in attached Exhibits B1 through B21.

It was well-known to one of ordinary skill in the art before the time of the '215 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that a memory module can have a buffer that includes circuit

components configurable to provide a first data path or a second data path depending on whether the first rank or the second rank is selected to communicate data with the memory controller.

See citations identified for claims 14 and 26 provided in attached Exhibits B1 through B21.

It was well-known to one of ordinary skill in the art before the time of the '215 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that a memory module can have at least one circuit components that is configured to provide the first data path in response to the first control signals, and is configured to provide the second data path in response to the second control signals. See citations identified for claim 15 provided in attached Exhibits B1 through B21.

It was well-known to one of ordinary skill in the art before the time of the '215 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that a memory module can include a logic configured to enable the communication of the first data burst between the at least one first memory integrated circuit and the memory controller in accordance with a latency value. See citations identified for claim 16 provided in attached Exhibits B1 through B21; Yoon at Abstract, Fig. 1, Fig. 3, Fig. 5, 1:31-2:39, 2:63-3:12, 3:20-45, 4:16-5:15; Lee '287 at 1:17-62, 2:25-59, 4:10-63, 4:64-5:27, 5:45-6:8; Lee '938 at Abstract, 1:45-67, 5:20-41, 7:57-64, 10:17-52, 12:35-61; Jang at Abstract, Fig. 1, Fig. 2, 1:28-50, 2:4-11, 3:7-48, 3:49-67; 4:54-5:13.

It was well-known to one of ordinary skill in the art before the time of the '215 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that a memory module can include a logic further configured to determine the latency value. See citations identified for claim 18 provided in attached Exhibits B1 through B21; Yoon at 1:31-67, 2:25-39, 2:63-3:12, 3:20-45, 4:16-47, 4:48-54, 4:55-5:15; Lee

‘287 at 1:17-25, 2:25-59, 3:41-4:9, 4:10-49, 4:64-5:27, 5:45-6:8, 9:28-42; Lee ‘938 at Abstract, 1:45-67, 2:7-31, 3:8-30, 4:25-56, 5:13-67, 7:57-64, 10:6-31, 10:32-44, 12:35-61; Jang at Abstract, Fig. 1, Fig. 2, 1:28-50, 2:4-11, 3:7-48, 3:49-4:53, 4:54-5:9 5:10-6:13.

It was well-known to one of ordinary skill in the art before the time of the ’215 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff’s infringement contentions, that a memory module can include a logic configured to enable the communication of the second data burst between the at least one second memory integrated circuit and the memory controller in accordance with the latency value. *See* citations identified for claim 19 provided in attached Exhibits B1 through B21; Yoon at Abstract, Fig. 1, Fig. 3, Fig. 5, 1:31-2:39, 2:63-3:12, 3:20-45, 4:16-5:15; Lee ‘287 at 1:17-62, 2:25-59, 4:10-63, 4:64-5:27, 5:45-6:8; Lee ‘938 at Abstract, 1:45-67, 5:20-41, 7:57-64, 10:17-52, 12:35-61; Jang at Abstract, Fig. 1, Fig. 2, 1:28-50, 2:4-11, 3:7-48, 3:49-67; 4:54-5:13.

It was well-known to one of ordinary skill in the art before the time of the ’215 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff’s infringement contentions, that, in the method of operating a memory module, the first set of input command and address signals can include at least one input chip-select signal, the method can further comprise generating a first chip select signal and a second chip select signal in response to the first set of input command and address signals, the first chip-select signal being provided to the at least one first memory integrated circuit and having an active value to cause the at least one first memory integrated circuit to receive or output data signals in response to the first memory command, the second chip-select signal being provided to the at least one second memory integrated circuit and having a non-active value to keep the at least one second memory integrated circuit from receiving or outputting data signals in response to the first memory

command. See citations identified for claim 23 provided in attached Exhibits B1 through B21.

It was well-known to one of ordinary skill in the art before the time of the '215 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that a method of operating a memory module can further comprise reporting an overall CAS latency of the memory module to the memory controller, the overall CAS latency having one more clock cycle than an actual operational CAS latency of the memory integrated circuits. See citations identified for claim 25 provided in attached Exhibits B1 through B21; Lee '287 at 1:17-35, 2:25-47, 4:28-49, 7:5-14, 7:61-65, 8:8-15, 8:64- 9:4; 10:5-13; Lee '938 at Abstract, 1:45-67, 5:20-67, 7:18--64, 10:17-67, 12:35-61; Jang at Abstract, Fig. 1, Fig. 2, 1:28-50, 2:4-11, 3:7-48, 3:49-4:53, 4:54-5:9 5:10-6:13.

In addition, the prior art also provided sets of finite, identified, predictable solutions for known problems that would have been obvious to those of ordinary skill to try with a reasonable expectation of success. For example, it would have been obvious to one of ordinary skill in the art at the time of alleged invention to mount or couple the disclosed memory integrated circuits, register, and circuits of a memory module to a printed circuit board having a plurality of edge connections configured to be electrically coupled to a corresponding plurality of contacts of a module slot of the computer system. It would have been also obvious to one of ordinary skill in the art at the time of alleged invention to arrange the disclosed memory integrated circuits in a plurality of ranks including at least a first rank and a second rank. It would have been also obvious to one of ordinary skill in the art at the time of alleged invention that the disclosed memory integrated circuits are double-data-rate dynamic random access memory (DRAM) circuits, while the disclosed memory module is a dual in-line memory module (DIMM). It would have been also obvious to one of ordinary skill in the art at the time of alleged invention to

utilize readily-available DRAM devices. It would have been also obvious to one of ordinary skill in the art at the time of alleged invention to utilize or integrate in the disclosed memory module various traditional and common at the time memory module components or devices, including without limitation an SPD device, an on-die-termination (ODT) bus, ODT circuits, combinatorial logic, registers, logic pipelines, buffers, and alike. It would have been also obvious to one of ordinary skill in the art at the time of alleged invention that the disclosed memory module can use various traditional and common memory commands and signals, including without limitation command and address signals, (memory) control signals, ODT signals, chip select signals, receive or output data signals, data strobe signals, activation commands, read commands, write commands, precharge commands, and refresh commands. It would have been also obvious to one of ordinary skill in the art at the time of alleged invention that the disclosed memory module receives and buffers any of such commands or signals.

The prior art references provide motivations to combine because they describe the field of the '215 patent, teach improvements, explain desired features, and even expressly state that one of ordinary skill in the art would be able to apply their teachings to related systems or methods. *See, e.g.*, '215 patent at 1:47-2:47, 6:4-23, 6:52-59, 8:65-9:17, 13:28-35, 14:57-60, 17:57-18:29, 23:6-9, 28:23-26, 28:50-53, 29:47-50, 35:43-45, 37:7-10; *see also* Amidi at [0002], [0011], [0025]-[0028], [0071]; Ellsberry at [0002]-[0005], [0010], [0012], [0023]-[0027]; Holman at 2:43-54; LaBerge '032 at 2:58-62, 3:52-56, 4:17-20, 6:17-21, 6:54-58; Perego '422 at 1:12-2:3, 2:7-30; Perego '896 at 1:18-2:6, 3:24-60, 9:35-50; Halbert '518 at 3:32-41; Halbert '119 at [0058], [0062]; Halbert '250 at 10:54-62; Rao at 2:1-8, 4:52-67; Klein at [0024], [0029]; Dodd at 1:8-14; Khandekar at [0001]-[0003]; Hampel at [0003], [0011], [0059]; Lee '688 at [0003], [0021]-[0034], [0081]; Mailloux at 10:14-20; 10:26-32, 12:44-54, 13:62-67, 18:40-54,

20:1-7; JEDEC Standards; JEDEC Standard 21-C at 4.20.4–5; JESD79 at 1, 2, 8; JESD79-2 at 10, 12; JESD79C at 1, 7, 8; QBM (*see, e.g.* QBM Specification Rev. 0.93 at 5, 9; QBM2 Interface Overview at 3; QBM2 Technical Features Overview at 3-5; QBM Doubling DDR Memory Bandwidth at 10); DDR3 Functional Outlook at 6, 10-12, 14-20, 22; Matsui '151 at [0001], [0010]-[0021]; Matsui '627 at 1:7-10, 2:28-8:37; Kim '811 at Abstract, 1:6-11, 3:21-36, 4:7-41; Kim '062 at Abstract, 1:11-24, 3:39-4:10, 4:16-5:20, 6:12-7:14, Kwak at 1:12-2:47, 3:25-4:11, 7:21-31; Janzen '578 at [0001], [0007], [0017], [0038]; LaBerge '331 at [0002], [0005]-[0009], [0017]-[0022]; LaBerge '755 at Abstract, [0002], [0005]-[0008], [0016]-[0018], [0022]; LaBerge '841 at 1:6-64, 2:15-50, 2:54-3:3, 3:36-56; Johnson '816 at [0002], [0004]-[0006], [0009], [0017], [0019]; Jeddeloh at Abstract, [0001]-[0012]; Dell '184 at Abstract, 1:23-27, 1:30-2:45, 2:48-3:5, Fig. 1; Dell '827 at 1:1267, 2:23-63, Fig. 1; Lee '827 at 1:16-67, 2:21-3:24; Lee '938 at 1:11-30, 2:30-3:45, 6:57-7:17; FBDIMM Architecture & Protocol (*see, e.g.* FBDIMM AP Rev. 0.1 at 3, 7, 17, 55, 87; FBDIMM AP Rev 0.0 at 9, 12, 21, 52, 78); Williams '617 at 1:13-2:6, 2:28-22, 3:8-67, Ludwig at 1:9-40, 1:43-2:60, 3:29-58, Johnson '424 at 1:6-2:34; Haskell at [0007]-[0008], [0027]; Averbuj at Abstract, [0004], [0011], [0081]; Rajamani at [0019], [0144]; Janzen '578 at [0002]-[0006], [0039]; Woo at 9:57-67; Ruckerbauer at 5:62-6:31, 6:39-48; McCall at 1:6-28, 3:47-53; LaBerge '345 at 7:34-40; Cornelius at 4:30-40, 8:62-9:3; Rogers at 2:49-52, 14:50-54, 15:49-58; Yoon at 1:8-25, 7:32-37; Wong '868 at 1:8-2:10, 5:21-23; Jang at 1:8-50, 5:42-47; Synchronous DRAM Architectures, Organizations, and Alternative Technologies at 5-9, 20-22; Lee '287 at Abstract, 1:14-62, 6:11-36; Wong '868 at 1:57-2:10, 2:66-3:4; Barth at 1:7-3:49; Reeves at 1:7-2:67, 6:64-7:27; Halbert '098 at 2:5-49, 3:21-65; Matsui '782 at Abstract, 1:7-2:25; Vemula at 1:6-2:17; Janzen '666 at [0001], [0008], [0009]; Blockmon at [0001]-[0010], [0027]; Lee '864 at [0001], [0002], [0007], [0008], [0009];

James at [0001]-[0005], [0010], [0011]; Williams '446 at 1:6-3:10, 5:23-7:2; Wong '090 at 1:8-2:26; and *see also* exemplary citations in Appendix B. Further, the prior art references provide motivations to combine because they explicitly suggest utilizing the teachings and disclosures of other references.

In accordance with these advances, the prior art could have been combined according to methods known to those of ordinary skill within the field of the Asserted Patents to yield predictable results. The substitution of one element in a memory module could have been predictably achieved by one of ordinary skill at the time of the alleged invention. One of ordinary skill in the art would have been aware of these various applications, including, for example, memory density multiplication techniques and structures, data or signal buffering, memory devices' isolation from other components, and would have been able to select appropriate attributes of one for inclusion in another. Those of ordinary skill in the art could have employed known techniques to improve similar prior art devices in the same way as claimed in the '215 patent.

In addition, one of ordinary skill in the art would be motivated to combine the prior art references because the elements found in the '215 patent Asserted Claims are well-known in the art. Indeed, the named inventors of the '215 patent admitted as much in the specification of the '215 patent. *See* the '215 patent at 1:47-2:47, 2:59-67, 6:4-23, 6:52-59, 6:60-7:13, 8:65-9:17, 9:7-17, 13:28-35, 13:51-14:18, 14:57-60, 17:57-18:29, 21:35-40, 23:6-9, 28:23-26, 28:50-53, 29:47-50, 35:43-45, 37:7-10.

Any reference or combination of references that anticipates or makes obvious an asserted independent claim also makes obvious any asserted claim dependent on that independent claim, as the element of each dependent '215 patent Asserted Claim was known by a person of ordinary

skill at the time of the alleged invention, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, and it would have been obvious to combine those known elements with the independent claims at least as a matter of common sense and routine innovation. Accordingly, Defendants contend that each Asserted Claim would have been obvious not only by the combinations described in these contentions, but also by any combination of references that renders obvious an Asserted Claim.

In addition to the specific examples of motivation provided above, Defendants reserve the right to rely on the disclosures of the references listed in Appendix B for additional motivation to combine. The above-identified examples of combinations are given merely to illustrate various motivations to combine and are not intended to provide an exhaustive list of every possible combination to which the motivation may apply. Defendants reserve the right to contend that the above-described motivations to combine apply to other combinations at the appropriate time, i.e., in expert reports regarding invalidity.

For at least the reasons described above, it would have been obvious to one of ordinary skill in the art to combine each prior art reference listed in Appendix B with any other reference or references listed in Appendix B along with the knowledge of one of ordinary skill in the art to arrive at the inventions claims in the '215 patent. For example, and without limitation, the Asserted Claims of the '215 patent would have been obvious to one of ordinary skill in the art in view of the following combinations:

Patent No. or Title (Primary Inventor/Author)	In Combination with One or More of: (Patent No. or Title (Primary Inventor/Author))
The '215 Patent's Admitted Prior Art ("APA")	• U.S. Patent Application Publication No. 2003/0204688 ("Lee '688"); • U.S. Patent Application Publication No. 2006/0117152 ("Amidi"); • U.S. Patent Application Publication No.

	2003/0145156 (“Khandekar”); • U.S. Patent No. 6,493,250 (“Halbert ’250”); • U.S. Patent No. 6,862,653 (“Dodd”); • U.S. Patent Application Publication No. 2003/0117864 (“Hampel”); • U.S. Patent No. 7,240,145 (“Holman”); • U.S. Patent Application Publication No. 2002/0112119 (“Halbert ’119”); • U.S. Patent Application Publication No. 2001/0008006 (“Klein”); • U.S. Patent No. 7,363,422 (“Perego ’422”); • JEDEC Standards; • Synchronous DRAM Architectures, Organizations, and Alternative Technologies (Bruce Jacob); • U.S. Patent Application Publication No. 2005/0198449 (“Haskell”); • FBDIMM Architecture & Protocol; • U.S. Patent No. 6,615,345 (“LaBerge ’345”); • U.S. Patent Application Publication No. 2006/0277355 (“Ellsberry”); • U.S. Patent No. 7,024,518 (“Halbert ’518”); • U.S. Patent Application Publication No. 2003/0039151 (“Matsui ’151”); • U.S. Patent No. 5,712,811 (“Kim ’811”); • U.S. Patent No. 7,334,150 (“Ruckerbauer”); • DDR SDRAM RDIMM Design Specification JEDEC Standard 21-C (4.20.4) (“JEDEC Standard 21-C”); • DDR2 SDRAM Specification JEDEC Standard JESD79-2A (“JESD79-2A”); • Micron DDR SDRAM RDIMM, MT36VDDF12872 & MT36VDDF25672 Product; • Kentron’s Quad Band Memory System (“QBM”); and/or • The knowledge of a person of ordinary skill in the art.
U.S. Patent No. 7,363,422 (“Perego ’422”)	• JEDEC Standards; • U.S. Patent Application Publication No. 2006/0277355 (“Ellsberry”); • U.S. Patent No. 7,024,518 (“Halbert ’518”); • Kentron’s Quad Band Memory System (“QBM”);

	• FBDIMM Architecture & Protocol; • U.S. Patent No. 6,564,287 (“Lee ’287”); • U.S. Patent No. 6,615,345 (“LaBerge ’345”); • U.S. Patent Application Publication No. 2003/0039151 (“Matsui ’151”); • U.S. Patent No. 5,712,811 (“Kim ’811”); • The ’215 Patent’s Admitted Prior Art (“APA”); • U.S. Patent Application Publication No. 2006/0117152 (“Amidi”); • U.S. Patent Application Publication No. 2003/0204688 (“Lee ’688”); • U.S. Patent Application Publication No. 2003/0145156 (“Khandekar”); • U.S. Patent Application Publication No. 2002/0112119 (“Halbert ’119”); • U.S. Patent No. 6,862,653 (“Dodd”); • U.S. Patent No. 7,240,145 (“Holman”); • DDR SDRAM RDIMM Design Specification JEDEC Standard 21-C (4.20.4) (“JEDEC Standard 21-C”); • U.S. Patent No. 7,155,627 (“Matsui ’627”); • DDR2 SDRAM Specification JEDEC Standard JESD79-2A (“JESD79-2A”); • U.S. Patent No. 7,092,299 (“Kwak”); • U.S. Patent Application Publication No. 2002/0118578 (“Janzen ’578”); • Synchronous DRAM Architectures, Organizations, and Alternative Technologies (Bruce Jacob); • U.S. Patent Application Publication No. 2003/0133331 (“LaBerge ’331”); • U.S. Patent Publication. No. 2002/0188816 (“Johnson ’816”); • U.S. Patent Application Publication No. 2004/0034755 (“LaBerge ’755”); • U.S. Patent Application Publication No. 2005/0050255 (“Jeddeloh”); • Micron DDR SDRAM RDIMM, MT36VDDF12872 & MT36VDDF25672 Product; • U.S. Patent No. 6,446,184 (“Dell ’184”); • U.S. Patent No. 7,149,841 (“LaBerge ’841”); • U.S. Patent No. 7,366,827 (“Lee ’827”); • U.S. Patent No. 7,043,617 (“Williams ’617”);
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	• U.S. Patent No. 7,433,258 (“Rao”); • U.S. Pat. No. 5,581,498 (“Ludwig”); • U.S. Patent No. 5,926,827 (“Dell ’827”); • DDR3 Functional Outlook; • U.S. Patent Application Publication No. US 2006/0195631 (“Rajamani”); • U.S. Patent Application Publication No. 2005/0198449 (“Haskell”); • U.S. Patent Application Publication No. 2005/0257109 (“Averbuj”); • U.S. Patent No. 6,820,163 (“McCall”); • U.S. Patent No. 7,222,224 (“Woo”); • U.S. Patent No. 7,334,150 (“Ruckerbauer”); • U.S. Patent No. 7,289,383 (“Cornelius”); • U.S. Patent No. 6,392,909 (“Jang”); • U.S. Patent No. 6,529,423 (“Yoon”); • U.S. Patent No. 6,262,938 (“Lee ’938”); • U.S. Patent No. 7,206,896 (“Perego ’896”); • U.S. Patent No. 6,205,062 (“Kim ’062”); • U.S. Patent No. 7,212,424 (“Johnson ’424”); - and/or • The knowledge of a person of ordinary skill in the art.
U.S. Patent Application Publication No. 2003/0204688 (“Lee ’688”)	• The ’215 Patent’s Admitted Prior Art (“APA”); • U.S. Patent Application Publication No. 2006/0117152 (“Amidi”); • U.S. Patent Application Publication No. 2003/0145156 (“Khandekar”); • DDR3 Functional Outlook; • U.S. Patent No. 6,862,653 (“Dodd”); • U.S. Patent Application Publication No. 2003/0117864 (“Hampel”); • U.S. Patent No. 6,615,345 (“LaBerge ’345”); • U.S. Patent No. 6,493,250 (“Halbert ’250”); • U.S. Patent No. 7,240,145 (“Holman”); • U.S. Patent Application Publication No. 2002/0112119 (“Halbert ’119”); • JEDEC Standards; • DDR3 Functional Outlook; • DDR SDRAM RDIMM Design Specification JEDEC Standard 21-C (4.20.4) (“JEDEC Standard 21-C”); • Kentron’s Quad Band Memory System (“QBM”);

	• FBDIMM Architecture & Protocol; • U.S. Patent Application Publication No. 2005/0198449 (“Haskell”); • U.S. Patent No. 7,149,841 (“LaBerge ’841”); • Synchronous DRAM Architectures, Organizations, and Alternative Technologies (Bruce Jacob); • U.S. Patent Application Publication No. US 2006/0195631 (“Rajamani”); • U.S. Patent Application Publication No. 2003/0039151 (“Matsui ’151”); • U.S. Patent No. 7,433,258 (“Rao”); • U.S. Patent No. 5,712,811 (“Kim ’811”); • U.S. Patent No. 7,043,617 (“Williams ’617”); • U.S. Patent No. 7,289,383 (“Cornelius”); • U.S. Patent No. 6,205,062 (“Kim ’062”); • DDR2 SDRAM Specification JEDEC Standard JESD79-2A (“JESD79-2A”); • Micron DDR SDRAM RDIMM, MT36VDDF12872 & MT36VDDF2672 Product; • U.S. Patent No. 7,092,299 (“Kwak”); • U.S. Patent No. 5,712,811 (“Kim ’811”); • U.S. Patent No. 7,149,841 (“LaBerge ’841”); • U.S. Patent No. 7,363,422 (“Perego ’422”); • U.S. Patent No. 7,222,224 (“Woo”); • U.S. Patent Application Publication No. 2006/0277355 (“Ellsberry”); • U.S. Patent No. 7,024,518 (“Halbert ’518”); • U.S. Patent Publication. No. 2002/0188816 (“Johnson ’816”); • U.S. Patent No. 6,414,868 (“Wong ’868”); • U.S. Patent Application Publication No. 2004/0034755 (“LaBerge ’755”); • U.S. Patent Application Publication No. 2003/0133331 (“LaBerge ’331”); • U.S. Patent Application Publication No. 2005/0050255 (“Jeddeloh”); • U.S. Patent No. 5,926,827 (“Dell ’827”); • U.S. Patent Application Publication No. 2005/0257109 (“Averbuj”); • U.S. Patent No. 6,392,909 (“Jang”); • U.S. Patent No. 7,206,896 (“Perego ’896”); • U.S. Patent No. 6,529,423 (“Yoon”);
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	• U.S. Patent No. 6,564,287 (“Lee ’287”); • U.S. Patent No. 6,262,938 (“Lee ’938”); • U.S. Patent No. 7,366,827 (“Lee ’827”); • U.S. Patent No. 7,212,424 (“Johnson ’424”); • U.S. Patent Application Publication No. 2001/0008006 (“Klein”); and/or • The knowledge of a person of ordinary skill in the art.
U.S. Patent Application Publication No. 2006/0117152 (“Amidi”)	• The ’215 Patent’s Admitted Prior Art (“APA”); • U.S. Patent Application Publication No. 2003/0204688 (“Lee ’688”); • U.S. Patent Application Publication No. 2003/0145156 (“Khandekar”); • DDR3 Functional Outlook; • U.S. Patent No. 6,862,653 (“Dodd”); • U.S. Patent Application Publication No. 2003/0117864 (“Hampel”); • U.S. Patent No. 6,493,250 (“Halbert ’250”); • U.S. Patent No. 7,240,145 (“Holman”); • U.S. Patent Application Publication No. 2002/0112119 (“Halbert ’119”); • FBDIMM Architecture & Protocol; • U.S. Patent No. 7,206,896 (“Perego ’896”); • JEDEC Standards; • U.S. Patent No. 6,615,345 (“LaBerge ’345”); • U.S. Patent No. 7,222,224 (“Woo”); • DDR SDRAM RDIMM Design Specification JEDEC Standard 21-C (4.20.4) (“JEDEC Standard 21-C”); • DDR2 SDRAM Specification JEDEC Standard JESD79-2A (“JESD79-2A”); • Kentron’s Quad Band Memory System (“QBM”); • U.S. Patent No. 7,433,258 (“Rao”); • U.S. Pat. No. 5,581,498 (“Ludwig”); • U.S. Patent No. 7,043,617 (“Williams ’617”); • U.S. Patent No. 6,529,993 (“Rogers”); • U.S. Patent No. 5,926,827 (“Dell ’827”); • U.S. Patent Application Publication No. 2005/0257109 (“Averbuj”); • U.S. Patent Application Publication No. US 2006/0195631 (“Rajamani”); • U.S. Patent No. 5,712,811 (“Kim ’811”); • U.S. Patent No. 6,414,868 (“Wong ’868”);

	• Synchronous DRAM Architectures, Organizations, and Alternative Technologies (Bruce Jacob); • Micron DDR SDRAM RDIMM, MT36VDDF12872 & MT36VDDF25672 Product; • U.S. Patent No. 7,363,422 (“Perego ’422”); • JEDEC Standards; • U.S. Patent Application Publication No. 2006/0277355 (“Ellsberry”); • U.S. Patent No. 7,024,518 (“Halbert ’518”); • U.S. Patent Application Publication No. 2003/0039151 (“Matsui ’151”); • U.S. Patent No. 6,820,163 (“McCall”); • U.S. Patent Application Publication No. 2005/0198449 (“Haskell”);; • U.S. Patent Publication. No. 2002/0188816 (“Johnson ’816”); • U.S. Patent No. 7,334,150 (“Ruckerbauer”); • U.S. Patent No. 7,092,299 B2 (“Kwak”); • U.S. Patent No. 7,289,383 (“Cornelius”); • U.S. Patent No. 7,149,841 (“LaBerge ’841”); • U.S. Patent No. 6,564,287 (“Lee ’287”); • U.S. Patent No. 6,262,938 (“Lee ’938”); • U.S. Patent No. 7,366,827 (“Lee ’827”); • U.S. Patent No. 7,212,424 (“Johnson ’424”); • U.S. Patent Application Publication No. 2001/0008006 (“Klein”); and/or • The knowledge of a person of ordinary skill in the art.
U.S. Patent Application Publication No. 2003/0145156 (“Khandekar”)	• The ’215 Patent’s Admitted Prior Art (“APA”); • U.S. Patent Application Publication No. 2003/0204688 (“Lee ’688”); • U.S. Patent Application Publication No. 2006/0117152 (“Amidi”); • U.S. Patent No. 6,862,653 (“Dodd”); • U.S. Patent Application Publication No. 2003/0117864 (“Hampel”); • U.S. Patent No. 7,240,145 (“Holman”); • DDR3 Functional Outlook; • FBDIMM Architecture & Protocol; • U.S. Patent Application Publication No. 2002/0112119 (“Halbert ’119”); • JEDEC Standards;

	• DDR SDRAM RDIMM Design Specification JEDEC Standard 21-C (4.20.4) (“JEDEC Standard 21-C”); • DDR2 SDRAM Specification JEDEC Standard JESD79-2A (“JESD79-2A”); • Kentron’s Quad Band Memory System (“QBM”); • U.S. Patent No. 7,149,841 (“LaBerge ’841”) • U.S. Patent No. 7,363,422 (“Perego ’422”); • JEDEC Standards; • U.S. Patent Application Publication No. 2006/0277355 (“Ellsberry”); • U.S. Patent No. 7,024,518 (“Halbert ’518”); • U.S. Patent Application Publication No. 2003/0039151 (“Matsui ’151”); • U.S. Patent No. 6,493,250 (“Halbert ’250”); • U.S. Patent Publication. No. 2002/0188816 (“Johnson ’816”); • U.S. Patent No. 6,615,345 (“LaBerge ’345”); • U.S. Patent Application Publication No. 2004/0034755 (“LaBerge ’755”); • U.S. Patent No. 7,222,224 (“Woo”); • Synchronous DRAM Architectures, Organizations, and Alternative Technologies (Bruce Jacob); • Micron DDR SDRAM RDIMM, MT36VDDF12872 & MT36VDDF25672 Product; • U.S. Patent Application Publication No. 2003/0133331 (“LaBerge ’331”) • U.S. Patent No. 7,206,896 (“Perego ’896”); • U.S. Patent No. 6,414,868 (“Wong ’868”); • U.S. Patent No. 7,433,258 (“Rao”); • U.S. Patent No. 7,043,617 (“Williams ’617”); • U.S. Pat. No. 5,581,498 (“Ludwig”); • U.S. Patent No. 5,926,827 (“Dell ’827”); • U.S. Patent Application Publication No. 2005/0257109 (“Averbuj”); • U.S. Patent No. 6,529,993 (“Rogers”); • U.S. Patent Application Publication No. US 2006/0195631 (“Rajamani”); • U.S. Patent No. 6,820,163 (“McCall”); • U.S. Patent Application Publication No. 2005/0198449 (“Haskell”);
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	• U.S. Patent No. 7,334,150 (“Ruckerbauer”); • U.S. Patent No. 6,564,287 (“Lee ’287”); • U.S. Patent No. 7,092,299 (“Kwak”); • U.S. Patent No. 5,712,811 (“Kim ’811”); • U.S. Patent Application Publication No. 2001/0008006 (“Klein”); and/or • The knowledge of a person of ordinary skill in the art. The knowledge of a person of ordinary skill in the art.
U.S. Patent No. 6,862,653 (“Dodd”)	• The ’215 Patent’s Admitted Prior Art (“APA”); • U.S. Patent Application Publication No. 2003/0204688 (“Lee ’688”); • U.S. Patent Application Publication No. 2006/0117152 (“Amidi”); • U.S. Patent Application Publication No. 2003/0145156 (“Khandekar”); • DDR3 Functional Outlook; • U.S. Patent Application Publication No. 2003/0117864 (“Hampel”); • FBDIMM Architecture & Protocol; • U.S. Patent No. 7,240,145 (“Holman”); • U.S. Patent Application Publication No. 2002/0112119 (“Halbert ’119”); • U.S. Patent Application Publication No. 2001/0008006 (“Klein”); • DDR SDRAM RDIMM Design Specification JEDEC Standard 21-C (4.20.4) (“JEDEC Standard 21-C”); • DDR2 SDRAM Specification JEDEC Standard JESD79-2A (“JESD79-2A”); • Kentron’s Quad Band Memory System (“QBM”); • U.S. Patent No. 7,363,422 (“Perego ’422”); • JEDEC Standards; • U.S. Patent No. 6,615,345 (“LaBerge ’345”); • U.S. Patent Application Publication No. 2006/0277355 (“Ellsberry”); • U.S. Patent No. 5,712,811 (“Kim ’811”); • U.S. Patent No. 7,024,518 (“Halbert ’518”); • U.S. Patent Application Publication No. 2003/0039151 (“Matsui ’151”); • U.S. Patent No. 7,149,841 (“LaBerge ’841”); • Synchronous DRAM Architectures, Organizations, and Alternative Technologies

	(Bruce Jacob); • Micron DDR SDRAM RDIMM, MT36VDDF12872 & MT36VDDF25672 Product; • U.S. Patent No. 7,206,896 (“Perego ’896”); • U.S. Patent No. 7,212,424 (“Johnson ’424”); • U.S. Patent No. 7,366,827 (“Lee ’827”); • U.S. Patent No. 6,446,184 (“Dell ’184”); • U.S. Patent No. 6,414,868 (“Wong ’868”); • U.S. Patent No. 6,205,062 (“Kim ’062”); • U.S. Patent No. 6,493,250 (“Halbert ’250”); • U.S. Patent No. 5,926,827 (“Dell ’827”); • U.S. Patent Application Publication No. 2005/0257109 (“Averbuj”); • U.S. Patent No. 6,564,287 (“Lee ’287”); • U.S. Patent Application Publication No. 2004/0034755 (“LaBerge ’755”); • U.S. Patent Application Publication No. 2002/0118578 (“Janzen ’578”); • U.S. Patent Application Publication No. 2005/0198449 (“Haskell”); • U.S. Patent No. 7,222,224 (“Woo”); • U.S. Patent No. 7,334,150 (“Ruckerbauer”); • U.S. Patent Application Publication No. 2003/0133331 (“LaBerge ’331”); • U.S. Patent No. 7,092,299 (“Kwak”); • U.S. Patent Application Publication No. 2005/0050255 (“Jeddeloh”); and/or • The knowledge of a person of ordinary skill in the art.
U.S. Patent No. 7,240,145 (“Holman”)	• The ’215 Patent’s Admitted Prior Art (“APA”); • U.S. Patent Application Publication No. 2003/0204688 (“Lee ’688”); • U.S. Patent Application Publication No. 2006/0117152 (“Amidi”); • Synchronous DRAM Architectures, Organizations, and Alternative Technologies (Bruce Jacob); • DDR3 Functional Outlook; • U.S. Patent No. 6,615,345 (“LaBerge ’345”); • U.S. Patent Application Publication No. 2003/0145156 (“Khandekar”); • U.S. Patent No. 6,493,250 (“Halbert ’250”); • U.S. Patent No. 6,862,653 (“Dodd”);

	• U.S. Patent Application Publication No. 2003/0117864 (“Hampel”); • U.S. Patent Application Publication No. 2002/0112119 (“Halbert ’119”); • JEDEC Standards; • DDR SDRAM RDIMM Design Specification JEDEC Standard 21-C (4.20.4) (“JEDEC Standard 21-C”); • FBDIMM Architecture & Protocol; • DDR2 SDRAM Specification JEDEC Standard JESD79-2A (“JESD79-2A”); • Kentron’s Quad Band Memory System (“QBM”); • U.S. Patent No. 7,363,422 (“Perego ’422”); • U.S. Patent Application Publication No. 2006/0277355 (“Ellsberry”); • U.S. Patent No. 7,024,518 (“Halbert ’518”); • U.S. Patent Application Publication No. 2003/0039151 (“Matsui ’151”); • U.S. Patent No. 5,712,811 (“Kim ’811”); • U.S. Patent No. 7,149,841 (“LaBerge ’841”); • Synchronous DRAM Architectures, Organizations, and Alternative Technologies (Bruce Jacob); • Micron DDR SDRAM RDIMM, MT36VDDF12872 & MT36VDDF25672 Product; • U.S. Patent No. 7,206,896 (“Perego ’896”) • U.S. Patent No. 7,366,827 (Lee ’827); • U.S. Patent No. 7,212,424 (“Johnson ’424”); • U.S. Patent No. 7,334,150 (“Ruckerbauer”); • U.S. Patent No. 6,446,184 (“Dell ’184”); • U.S. Patent No. 6,414,868 (“Wong ’868”); • U.S. Patent No. 6,205,062 (“Kim ’062”); • U.S. Patent No. 5,926,827 (“Dell ’827”); • U.S. Patent Application Publication No. 2005/0257109 (“Averbuj”); • U.S. Patent No. 6,564,287 (“Lee ’287”); • U.S. Patent Application Publication No. 2004/0034755 (“LaBerge ’755”); • U.S. Patent Application Publication No. 2002/0118578 (“Janzen ’578”); • U.S. Patent Application Publication No. 2005/0198449 (“Haskell”);
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	• U.S. Patent Application Publication No. 2003/0133331 (“LaBerge ’331”); • U.S. Patent No. 7,092,299 (“Kwak”); • U.S. Patent Application Publication No. 2005/0050255 (“Jeddeloh”); and/or • The knowledge of a person of ordinary skill in the art.
U.S. Patent Application Publication No. 2003/0117864 (“Hampel”)	• The ’215 Patent’s Admitted Prior Art (“APA”); • U.S. Patent Application Publication No. 2003/0204688 (“Lee ’688”); • DDR3 Functional Outlook; • U.S. Patent No. 6,446,184 (“Dell ’184”); • U.S. Patent Application Publication No. 2006/0117152 (“Amidi”); • U.S. Patent Application Publication No. 2003/0145156 (“Khandekar”); • U.S. Patent No. 6,862,653 (“Dodd”); • U.S. Patent No. 6,820,163 (“McCall”); • U.S. Patent No. 6,493,250 (“Halbert ’250”); • U.S. Patent No. 7,240,145 (“Holman”); • U.S. Patent Application Publication No. 2002/0112119 (“Halbert ’119”); • U.S. Patent Application Publication No. 2001/0008006 (“Klein”); • JEDEC Standards; • U.S. Patent Application Publication No. US 2006/0195631 (“Rajamani”); • FBDIMM Architecture & Protocol; • U.S. Patent No. 6,615,345 (“LaBerge ’345”); • DDR SDRAM RDIMM Design Specification JEDEC Standard 21-C (4.20.4) (“JEDEC Standard 21-C”); • Synchronous DRAM Architectures, Organizations, and Alternative Technologies (Bruce Jacob); • Kentron’s Quad Band Memory System (“QBM”); • Micron DDR SDRAM RDIMM, MT36VDDF12872 & MT36VDDF25672 Product; • U.S. Patent No. 7,043,617 (“Williams ’617”); • U.S. Patent No. 7,206,896 (“Perego ’896”); • U.S. Patent No. 6,529,423 (“Yoon”); • U.S. Patent No. 6,564,287 (“Lee ’287”);

	• U.S. Patent No. 7,433,258 (“Rao”); • U.S. Patent No. 7,289,383 (“Cornelius”); • U.S. Patent No. 6,392,909 (“Jang”); • U.S. Patent No. 6,262,938 (“Lee ’938”); • U.S. Patent No. 7,212,424 (“Johnson ’424”); • U.S. Patent No. 5,712,811 (“Kim ’811”); • U.S. Patent No. 6,205,062 (“Kim ’062”); • U.S. Patent No. 7,222,224 (“Woo”); • U.S. Patent No. 7,363,422 (“Perego ’422”); • U.S. Patent No. 7,334,150 (“Ruckerbauer”); • U.S. Patent Application Publication No. 2006/0277355 (“Ellsberry”); • U.S. Patent Application Publication No. 2005/0050255 (“Jeddeloh”); • U.S. Patent No. 7,212,424 (“Johnson ’424”); • U.S. Patent No. 5,926,827 (“Dell ’827”); • U.S. Patent Application Publication No. 2002/0118578 (“Janzen ’578”); • U.S. Patent Application Publication No. 2005/0198449 (“Haskell”); • U.S. Patent Publication. No. 2002/0188816 (“Johnson ’816”); • U.S. Patent No. 6,414,868 (“Wong ’868”); • U.S. Patent No. 7,092,299 (“Kwak”); • U.S. Patent Application Publication No. 2003/0133331 (“LaBerge ’331”); • U.S. Patent Application Publication No. 2004/0034755 (“LaBerge ’755”); • U.S. Patent Application Publication No. 2005/0257109 (“Averbuj”); • U.S. Patent No. 7,024,518 (“Halbert ’518”) • U.S. Patent Application Publication No. 2003/0039151 (“Matsui ’151”); • U.S. Patent No. 7,149,841 (“LaBerge ’841”); • U.S. Patent No. 7,366,827 (Lee ’827); • DDR2 SDRAM Specification JEDEC Standard JESD79-2A (“JESD79-2A”); and/or • The knowledge of a person of ordinary skill in the art.
U.S. Patent Application Publication No. 2002/0112119 (“Halbert ’119”)	• The ’215 Patent’s Admitted Prior Art (“APA”); • U.S. Patent Application Publication No. 2003/0204688 (“Lee ’688”); • U.S. Patent Application Publication No. 2006/0117152 (“Amidi”);

	• DDR3 Functional Outlook; • FBDIMM Architecture & Protocol; • U.S. Patent Application Publication No. 2003/0145156 (“Khandekar”); • U.S. Patent No. 6,862,653 (“Dodd”); • U.S. Patent Application Publication No. 2003/0117864 (“Hampel”); • U.S. Patent No. 7,240,145 (“Holman”); • U.S. Patent Application Publication No. 2001/0008006 (“Klein”); • Micron DDR SDRAM RDIMM, MT36VDDF12872 & MT36VDDF25672 Product; • U.S. Patent No. 6,493,250 (“Halbert ’250”); • JEDEC Standards; • U.S. Patent No. 7,334,150 (“Ruckerbauer”); • DDR SDRAM RDIMM Design Specification JEDEC Standard 21-C (4.20.4) (“JEDEC Standard 21-C”); • DDR2 SDRAM Specification JEDEC Standard JESD79-2A (“JESD79-2A”); • U.S. Patent Publication. No. 2002/0188816 (“Johnson ’816”); • U.S. Patent No. 7,092,299 (“Kwak”); U.S. Patent No. 7,206,896 (Perego ’896) • U.S. Patent No. 6,529,423 (“Yoon”); • U.S. Patent No. 6,564,287 (“Lee ’287”); • U.S. Patent No. 7,222,224 (“Woo”); • U.S. Patent No. 5,712,811 (“Kim ’811”); • U.S. Patent No. 6,205,062 (“Kim ’062”); • U.S. Patent No. 5,926,827 (“Dell ’827”); • U.S. Patent Application Publication No. 2002/0118578 (“Janzen ’578”); • U.S. Patent Application Publication No. 2005/0198449 (“Haskell”); • U.S. Patent Application Publication No. 2003/0133331 (“LaBerge ’331”); • U.S. Patent Application Publication No. 2005/0257109 (“Averbuj”); • U.S. Patent Application Publication No. 2005/0050255 (“Jeddeloh”); • Synchronous DRAM Architectures, Organizations, and Alternative Technologies (Bruce Jacob);
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	• U.S. Patent No. 6,615,345 (“LaBerge ’345”); • U.S. Patent No. 7,363,422 (“Perego ’422”); • U.S. Patent Application Publication No. 2006/0277355 (“Ellsberry”); • U.S. Patent No. 7,024,518 (“Halbert ’518”) • U.S. Patent Application Publication No. 2003/0039151 (“Matsui ’151”); • U.S. Patent No. 7,043,617 (“Williams ’617”); • U.S. Patent No. 7,433,258 (“Rao”); • U.S. Patent No. 7,289,383 (“Cornelius”); • U.S. Patent No. 6,262,938 (“Lee ’938”); • U.S. Patent No. 7,212,424 (“Johnson ’424”); • U.S. Patent No. 7,366,827 (Lee ’827); • Kentron’s Quad Band Memory System (“QBM”); and/or • The knowledge of a person of ordinary skill in the art.
U.S. Patent No. 7,024,518 (“Halbert ’518”)	• The ’215 Patent’s Admitted Prior Art (“APA”); • U.S. Patent Application Publication No. 2003/0204688 (“Lee ’688”); • U.S. Patent Application Publication No. 2006/0117152 (“Amidi”); • FBDIMM Architecture & Protocol; • DDR3 Functional Outlook; • U.S. Patent Application Publication No. 2003/0145156 (“Khandekar”); • U.S. Patent No. 6,862,653 (“Dodd”); • U.S. Patent Application Publication No. 2003/0117864 (“Hampel”); • U.S. Patent No. 7,240,145 (“Holman”); • U.S. Patent Application Publication No. 2001/0008006 (“Klein”); • Micron DDR SDRAM RDIMM, MT36VDDF12872 & MT36VDDF25672 Product; • U.S. Patent No. 6,493,250 (“Halbert ’250”); • JEDEC Standards; • U.S. Patent No. 7,334,150 (“Ruckerbauer”); • DDR SDRAM RDIMM Design Specification JEDEC Standard 21-C (4.20.4) (“JEDEC Standard 21-C”); • DDR2 SDRAM Specification JEDEC Standard JESD79-2A (“JESD79-2A”); • U.S. Patent Publication. No. 2002/0188816

	(“Johnson ’816”); • U.S. Patent No. 7,092,299 (“Kwak”);U.S. Patent No. 7,206,896 (Perego ’896) • U.S. Patent No. 6,529,423 (“Yoon”); • U.S. Patent No. 6,564,287 (“Lee ’287”); • U.S. Patent No. 7,222,224 (“Woo”); • U.S. Patent No. 5,712,811 (“Kim ’811”); • U.S. Patent No. 6,205,062 (“Kim ’062”); • U.S. Patent No. 5,926,827 (“Dell ’827”); • U.S. Patent Application Publication No. 2002/0118578 (“Janzen ’578”); • U.S. Patent Application Publication No. 2005/0198449 (“Haskell”); • U.S. Patent Application Publication No. 2003/0133331 (“LaBerge ’331”); • U.S. Patent Application Publication No. 2005/0257109 (“Averbuj”); • U.S. Patent Application Publication No. 2005/0050255 (“Jeddeloh”); • Synchronous DRAM Architectures, Organizations, and Alternative Technologies (Bruce Jacob); • U.S. Patent No. 6,615,345 (“LaBerge ’345”); • U.S. Patent No. 7,363,422 (“Perego ’422”); • U.S. Patent Application Publication No. 2006/0277355 (“Ellsberry”); • U.S. Patent Application Publication No. 2002/0112119 (“Halbert ’119”); • U.S. Patent Application Publication No. 2003/0039151 (“Matsui ’151”); • U.S. Patent No. 7,043,617 (“Williams ’617”); • U.S. Patent No. 7,433,258 (“Rao”); • U.S. Patent No. 7,289,383 (“Cornelius”); • U.S. Patent No. 6,262,938 (“Lee ’938”); • U.S. Patent No. 7,212,424 (“Johnson ’424”); • U.S. Patent No. 7,366,827 (Lee ’827); • Kentron’s Quad Band Memory System (“QBM”); and/or • The knowledge of a person of ordinary skill in the art.
DDR SDRAM RDIMM Design Specification JEDEC Standard 21-C (4.20.4) (“JEDEC Standard 21-C”)	• The ’215 Patent’s Admitted Prior Art (“APA”); • U.S. Patent Application Publication No. 2003/0204688 (“Lee ’688”); • U.S. Patent Application Publication No. 2006/0117152 (“Amidi”);

	• DDR3 Functional Outlook; • FBDIMM Architecture & Protocol; • U.S. Patent Application Publication No. 2003/0145156 (“Khandekar”); • U.S. Patent No. 6,862,653 (“Dodd”); • U.S. Patent Application Publication No. 2003/0117864 (“Hampel”); • U.S. Patent No. 7,240,145 (“Holman”); • U.S. Patent No. 5,712,811 (“Kim ’811”); • Synchronous DRAM Architectures, Organizations, and Alternative Technologies (Bruce Jacob); • Micron DDR SDRAM RDIMM, MT36VDDF12872 & MT36VDDF25672 Product; • U.S. Patent Application Publication No. 2005/0198449 (“Haskell”); • U.S. Patent No. 6,493,250 (“Halbert ’250”); • U.S. Patent Application Publication No. 2002/0112119 (“Halbert ’119”); • U.S. Patent No. 7,334,150 (“Ruckerbauer”); • U.S. Patent No. 7,366,827 (Lee ’827); • U.S. Patent No. 7,043,617 (“Williams ’617”); • U.S. Patent No. 7,433,258 (“Rao”); • U.S. Patent No. 7,289,383 (“Cornelius”); • U.S. Patent No. 6,262,938 (“Lee ’938”); • U.S. Patent No. 7,149,841 (“LaBerge ’841”); • U.S. Patent No. 7,206,896 (Perego ’896); • U.S. Patent No. 6,564,287 (“Lee ’287”); • U.S. Patent No. 5,926,827 (“Dell ’827”); • U.S. Patent No. 7,222,224 (“Woo”); • U.S. Patent Application Publication No. 2001/0008006 (“Klein”); • U.S. Patent No. 6,615,345 (“LaBerge ’345”); • U.S. Patent No. 7,363,422 (“Perego ’422”); • JEDEC Standards; • DDR2 SDRAM Specification JEDEC Standard JESD79-2A (“JESD79-2A”); • U.S. Patent Publication. No. 2002/0188816 (“Johnson ’816”); • U.S. Patent No. 7,092,299 (“Kwak”); • U.S. Patent Application Publication No. 2006/0277355 (“Ellsberry”); • U.S. Patent No. 7,024,518 (“Halbert ’518”)
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	• U.S. Patent Application Publication No. 2003/0039151 (“Matsui ’151”); • Kentron’s Quad Band Memory System (“QBM”); and/or • The knowledge of a person of ordinary skill in the art.
DDR2 SDRAM Specification JEDEC Standard JESD79-2A (“JESD79-2A”)	• The ’215 Patent’s Admitted Prior Art (“APA”); • U.S. Patent Application Publication No. 2003/0204688 (“Lee ’688”); • U.S. Patent Application Publication No. 2006/0117152 (“Amidi”); • DDR3 Functional Outlook; • U.S. Patent Application Publication No. 2003/0145156 (“Khandekar”); • U.S. Patent No. 6,862,653 (“Dodd”); • U.S. Patent Application Publication No. 2003/0117864 (“Hampel”); • U.S. Patent No. 7,240,145 (“Holman”); • U.S. Patent Application Publication No. 2002/0112119 (“Halbert ’119”); • FBDIMM Architecture & Protocol; • U.S. Patent Application Publication No. 2001/0008006 (“Klein”); • U.S. Patent No. 6,564,287 (“Lee ’287”); • DDR SDRAM RDIMM Design Specification JEDEC Standard 21-C (4.20.4) (“JEDEC Standard 21-C”); • Synchronous DRAM Architectures, Organizations, and Alternative Technologies (Bruce Jacob); • Micron DDR SDRAM RDIMM, MT36VDDF12872 & MT36VDDF25672 Product; • U.S. Patent No. 6,615,345 (“LaBerge ’345”); • U.S. Patent No. 7,212,424 (“Johnson ’424”); • U.S. Patent No. 7,334,150 (“Ruckerbauer”); • U.S. Patent No. 6,493,250 (“Halbert ’250”); • U.S. Patent No. 7,363,422 (“Perego ’422”); • JEDEC Standards; • U.S. Patent No. 5,926,827 (“Dell ’827”); • U.S. Patent Application Publication No. 2002/0118578 (“Janzen ’578”); • U.S. Patent Application Publication No. 2005/0198449 (“Haskell”);

	• U.S. Patent Application Publication No. 2003/0133331 (“LaBerge ’331”); • U.S. Patent Application Publication No. 2006/0277355 (“Ellsberry”); • U.S. Patent No. 7,222,224 (“Woo”); • U.S. Patent No. 7,024,518 (“Halbert ’518”) • U.S. Patent Application Publication No. 2003/0039151 (“Matsui ’151”); • U.S. Patent No. 5,712,811 (“Kim ’811”); • Kentron’s Quad Band Memory System (“QBM”); and/or • The knowledge of a person of ordinary skill in the art.
JEDEC Standards	• The ’215 Patent’s Admitted Prior Art (“APA”); • U.S. Patent Application Publication No. 2003/0204688 (“Lee ’688”); • U.S. Patent Application Publication No. 2006/0117152 (“Amidi”); • DDR3 Functional Outlook; • U.S. Patent Application Publication No. 2003/0145156 (“Khandekar”); • U.S. Patent No. 6,862,653 (“Dodd”); • U.S. Patent Application Publication No. 2003/0117864 (“Hampel”); • U.S. Patent No. 6,615,345 (“LaBerge ’345”); • U.S. Patent No. 7,240,145 (“Holman”); • U.S. Patent Application Publication No. 2002/0112119 (“Halbert ’119”); • U.S. Patent Application Publication No. 2001/0008006 (“Klein”); • U.S. Patent No. 6,493,250 (“Halbert ’250”); • Kentron’s Quad Band Memory System (“QBM”); • FBDIMM Architecture & Protocol; • U.S. Patent No. 7,206,896 (“Perego ’896”); • U.S. Patent No. 6,529,423 (“Yoon”); • Synchronous DRAM Architectures, Organizations, and Alternative Technologies (Bruce Jacob); • Micron DDR SDRAM RDIMM, MT36VDDF12872 & MT36VDDF25672 Product; • U.S. Patent No. 7,155,627 (“Matsui ’627”); • U.S. Patent No. 7,334,150 (“Ruckerbauer”);

	• U.S. Patent No. 5,926,827 (“Dell ’827”); • U.S. Patent Application Publication No. 2005/0257109 (“Averbuj”); • U.S. Patent No. 5,926,827 (“Dell ’827”); • U.S. Patent Application Publication No. 2002/0118578 (“Janzen ’578”); • U.S. Patent Application Publication No. 2005/0198449 (“Haskell”); • U.S. Patent Application Publication No. 2003/0133331 (“LaBerge ’331”); • U.S. Patent No. 6,262,938 (“Lee ’938”); • U.S. Patent No. 5,712,811 (“Kim ’811”); • U.S. Patent No. 6,205,062 (“Kim ’062”); • U.S. Patent No. 7,222,224 (“Woo”); • U.S. Patent Application Publication No. 2005/0050255 (“Jeddeloh”); • U.S. Patent No. 7,363,422 (“Perego ’422”); • U.S. Patent Application Publication No. 2006/0277355 (“Ellsberry”); • U.S. Patent No. 7,024,518 (“Halbert ’518”) • U.S. Patent Application Publication No. 2003/0039151 (“Matsui ’151”); • U.S. Patent No. 7,212,424 (“Johnson ’424”); • U.S. Patent No. 7,366,827 (Lee ’827); and/or • The knowledge of a person of ordinary skill in the art.
Kentron’s Quad Band Memory System (“QBM”)	• The ’215 Patent’s Admitted Prior Art (“APA”); • U.S. Patent Application Publication No. 2003/0204688 (“Lee ’688”); • DDR3 Functional Outlook; • U.S. Patent Application Publication No. 2006/0117152 (“Amidi”); • U.S. Patent Application Publication No. 2003/0145156 (“Khandekar”); • U.S. Patent No. 6,862,653 (“Dodd”); • U.S. Patent Application Publication No. 2003/0117864 (“Hampel”); • U.S. Patent No. 6,493,250 (“Halbert ’250”); • U.S. Patent No. 7,240,145 (“Holman”); • U.S. Patent Application Publication No. 2002/0112119 (“Halbert ’119”); • U.S. Patent Application Publication No. 2001/0008006 (“Klein”); • JEDEC Standards;

	• FBDIMM Architecture & Protocol; • U.S. Patent No. 6,615,345 (“LaBerge ’345”); • DDR SDRAM RDIMM Design Specification JEDEC Standard 21-C (4.20.4) (“JEDEC Standard 21-C”); • Synchronous DRAM Architectures, Organizations, and Alternative Technologies (Bruce Jacob); • Micron DDR SDRAM RDIMM, MT36VDDF12872 & MT36VDDF25672 Product; • U.S. Patent No. 7,206,896 (“Perego ’896”) • U.S. Patent No. 6,529,423 (“Yoon”); • U.S. Patent No. 6,564,287 (“Lee ’287”); • U.S. Patent No. 6,262,938 (“Lee ’938”); • U.S. Patent No. 5,712,811 (“Kim ’811”); • U.S. Patent No. 6,205,062 (“Kim ’062”); • U.S. Patent No. 7,222,224 (“Woo”); • U.S. Patent No. 7,363,422 (“Perego ’422”); • U.S. Patent No. 7,334,150 (“Ruckerbauer”); • U.S. Patent Application Publication No. 2006/0277355 (“Ellsberry”); • U.S. Patent Application Publication No. 2005/0050255 (“Jeddeloh”); • U.S. Patent No. 7,212,424 (“Johnson ’424”); • U.S. Patent No. 5,926,827 (“Dell ’827”); • U.S. Patent Application Publication No. 2002/0118578 (“Janzen ’578”); • U.S. Patent Application Publication No. 2005/0198449 (“Haskell”); • U.S. Patent Application Publication No. 2003/0133331 (“LaBerge ’331”); • U.S. Patent Application Publication No. 2005/0257109 (“Averbuj”); • U.S. Patent No. 7,024,518 (“Halbert ’518”) • U.S. Patent Application Publication No. 2003/0039151 (“Matsui ’151”); • U.S. Patent No. 7,366,827 (Lee ’827); • DDR2 SDRAM Specification JEDEC Standard JESD79-2A (“JESD79-2A”); and/or • The knowledge of a person of ordinary skill in the art.
U.S. Patent Application Publication No. 2006/0277355 (“Ellsberry”)	• The ’215 Patent’s Admitted Prior Art (“APA”); • U.S. Patent Application Publication No.

	2006/0117152 (“Amidi”); • U.S. Patent Application Publication No. 2003/0204688 (“Lee ’688”); • U.S. Patent Application Publication No. 2003/0145156 (“Khandekar”); • U.S. Patent No. 6,862,653 (“Dodd”); • U.S. Patent Application Publication No. 2003/0117864 (“Hampel”); • U.S. Patent No. 7,240,145 (“Holman”); • U.S. Patent Application Publication No. 2002/0112119 (“Halbert ’119”); • U.S. Patent No. 7,024,518 (“Halbert ’518”); • U.S. Patent No. 6,493,250 (“Halbert ’250”); • JEDEC Standards; • FBDIMM Architecture & Protocol; • DDR SDRAM RDIMM Design Specification JEDEC Standard 21-C (4.20.4) (“JEDEC Standard 21-C”); • DDR3 Functional Outlook; • DDR2 SDRAM Specification JEDEC Standard JESD79-2A (“JESD79-2A”); • U.S. Patent Publication. No. 2002/0188816 (“Johnson ’816”); • U.S. Patent No. 7,092,299 (“Kwak”); • Kentron’s Quad Band Memory System (“QBM”); • U.S. Patent No. 7,043,617 (“Williams ’617”); • U.S. Patent No. 7,433,258 (“Rao”); • U.S. Patent No. 6,615,345 (“LaBerge ’345”); • U.S. Pat. No. 5,581,498 (“Ludwig”); • U.S. Patent No. 6,529,993 (“Rogers”); • U.S. Patent No. 5,926,827 (“Dell ’827”); • U.S. Patent Application Publication No. 2002/0118578 (“Janzen ’578”); • U.S. Patent Application Publication No. 2005/0198449 (“Haskell”); • U.S. Patent Application Publication No. 2003/0133331 (“LaBerge ’331”); • U.S. Patent No. 7,149,841 (“LaBerge ’841”); • U.S. Patent No. 7,206,896 (“Perego ’896”); • U.S. Patent Application Publication No. 2005/0257109 (“Averbuj”); • U.S. Patent No. 7,334,150 (“Ruckerbauer”); • U.S. Patent Application Publication No. US 2006/0195631 (“Rajamani”);
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	• U.S. Patent No. 5,712,811 (“Kim ’811”); • U.S. Patent No. 6,414,868 (“Wong ’868”); • Synchronous DRAM Architectures, Organizations, and Alternative Technologies (Bruce Jacob); • Micron DDR SDRAM RDIMM, MT36VDDF12872 & MT36VDDF25672 Product; • U.S. Patent No. 6,564,287 (“Lee ’287”); • U.S. Patent No. 7,222,224 (“Woo”); • U.S. Patent No. 7,363,422 (“Perego ’422”); • U.S. Patent Application Publication No. 2001/0008006 (“Klein”); • U.S. Patent Application Publication No. 2003/0039151 (“Matsui ’151”); and/or • The knowledge of a person of ordinary skill in the art.
U.S. Patent No. 6,493,250 (“Halbert ’250”)	• The ’215 Patent’s Admitted Prior Art (“APA”); • U.S. Patent Application Publication No. 2006/0277355 (“Ellsberry”); • U.S. Patent Application Publication No. 2006/0117152 (“Amidi”); • DDR3 Functional Outlook; • U.S. Patent Application Publication No. 2003/0204688 (“Lee ’688”); • U.S. Patent Application Publication No. 2003/0145156 (“Khandekar”); • U.S. Patent No. 6,862,653 (“Dodd”); • U.S. Patent Application Publication No. 2003/0117864 (“Hampel”); • U.S. Patent No. 7,240,145 (“Holman”); • U.S. Patent Application Publication No. 2002/0112119 (“Halbert ’119”); • U.S. Patent No. 7,334,150 (“Ruckerbauer”); • JEDEC Standards; • FBDIMM Architecture & Protocol; • U.S. Patent No. 6,615,345 (“LaBerge ’345”); • U.S. Patent No. 7,363,422 (“Perego ’422”); • U.S. Patent Application Publication No. 2006/0277355 (“Ellsberry”); • U.S. Patent No. 7,024,518 (“Halbert ’518”); • DDR SDRAM RDIMM Design Specification JEDEC Standard 21-C (4.20.4) (“JEDEC Standard 21-C”);

	• DDR2 SDRAM Specification JEDEC Standard JESD79-2A (“JESD79-2A”); • U.S. Patent Publication. No. 2002/0188816 (“Johnson ’816”); • U.S. Patent No. 7,092,299 (“Kwak”); • Kentron’s Quad Band Memory System (“QBM”); • Micron DDR SDRAM RDIMM, MT36VDDF12872 & MT36VDDF25672 Product; • U.S. Patent No. 7,043,617 (“Williams ’617”); • U.S. Patent No. 7,366,827 (Lee ’827); • U.S. Patent No. 7,289,383 (“Cornelius”); • U.S. Patent No. 6,262,938 (“Lee ’938”); • U.S. Patent No. 6,564,287 (“Lee ’287”); • U.S. Patent No. 7,222,224 (“Woo”); • U.S. Patent No. 7,433,258 (“Rao”); • U.S. Patent No. 6,529,993 (“Rogers”); • U.S. Pat. No. 5,581,498 (“Ludwig”); • U.S. Patent No. 5,926,827 (“Dell ’827”); • U.S. Patent Application Publication No. 2002/0118578 (“Janzen ’578”); • U.S. Patent Application Publication No. 2005/0198449 (“Haskell”); • U.S. Patent Application Publication No. 2003/0133331 (“LaBerge ’331”); • U.S. Patent Application Publication No. 2005/0257109 (“Averbuj”); • U.S. Patent Application Publication No. US 2006/0195631 (“Rajamani”); • U.S. Patent No. 5,712,811 (“Kim ’811”); • U.S. Patent No. 6,414,868 (“Wong ’868”); • U.S. Patent No. 7,149,841 (“LaBerge ’841”); • U.S. Patent No. 7,206,896 (“Perego ’896”); • Synchronous DRAM Architectures, Organizations, and Alternative Technologies (Bruce Jacob); • U.S. Patent No. 7,363,422 (“Perego ’422”); • U.S. Patent Application Publication No. 2001/0008006 (“Klein”) • U.S. Patent Application Publication No. 2003/0039151 (“Matsui ’151”); and/or • The knowledge of a person of ordinary skill in the art.
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U.S. Patent Application Publication No. 2001/0008006 (“Klein”)	• The ’215 Patent’s Admitted Prior Art (“APA”); • U.S. Patent Application Publication No. 2006/0117152 (“Amidi”); • U.S. Patent Application Publication No. 2003/0204688 (“Lee ’688”); • U.S. Patent Application Publication No. 2003/0145156 (“Khandekar”); • U.S. Patent No. 6,564,287 (“Lee ’287”); • U.S. Patent No. 7,222,224 (“Woo”); • U.S. Patent No. 7,149,841 (“LaBerge ’841”); • U.S. Patent No. 7,206,896 (“Perego ’896”); • U.S. Patent No. 6,862,653 (“Dodd”); • DDR3 Functional Outlook; • U.S. Patent Application Publication No. 2003/0117864 (“Hampel”); • U.S. Patent No. 6,493,250 (“Halbert ’250”); • U.S. Patent No. 7,240,145 (“Holman”); • U.S. Patent Application Publication No. 2002/0112119 (“Halbert ’119”); • JEDEC Standards; • FBDIMM Architecture & Protocol; • U.S. Patent No. 6,615,345 (“LaBerge ’345”); • U.S. Patent No. 7,155,627 (“Matsui ’627”); • DDR SDRAM RDIMM Design Specification JEDEC Standard 21-C (4.20.4) (“JEDEC Standard 21-C”); • DDR2 SDRAM Specification JEDEC Standard JESD79-2A (“JESD79-2A”); • U.S. Patent Publication. No. 2002/0188816 (“Johnson ’816”); • Kentron’s Quad Band Memory System (“QBM”); • Micron DDR SDRAM RDIMM, MT36VDDF12872 & MT36VDDF25672 Product; • U.S. Patent No. 7,092,299 (“Kwak”); • U.S. Patent No. 7,433,258 (“Rao”); • U.S. Pat. No. 5,581,498 (“Ludwig”); • U.S. Patent No. 7,043,617 (“Williams ’617”); • U.S. Patent No. 6,529,993 (“Rogers”); • U.S. Patent No. 5,926,827 (“Dell ’827”); • U.S. Patent Application Publication No. 2002/0118578 (“Janzen ’578”); • U.S. Patent Application Publication No.
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	2005/0198449 (“Haskell”); • U.S. Patent Application Publication No. 2003/0133331 (“LaBerge ’331”); • U.S. Patent Application Publication No. 2005/0257109 (“Averbuj”); • U.S. Patent Application Publication No. US 2006/0195631 (“Rajamani”); • U.S. Patent No. 5,712,811 (“Kim ’811”); • U.S. Patent No. 6,414,868 (“Wong ’868”); • Synchronous DRAM Architectures, Organizations, and Alternative Technologies (Bruce Jacob); • U.S. Patent Application Publication No. 2003/0039151 (“Matsui ’151”); • U.S. Patent No. 7,024,518 (“Halbert ’518”); • U.S. Patent No. 7,212,424 (“Johnson ’424”); • U.S. Patent No. 7,334,150 (“Ruckerbauer”); • U.S. Patent No. 7,363,422 (“Perego ’422”); • U.S. Patent Application Publication No. 2006/0277355 (“Ellsberry”); and/or • The knowledge of a person of ordinary skill in the art.
DDR3 Functional Outlook	• The ’215 Patent’s Admitted Prior Art (“APA”); • U.S. Patent No. 7,363,422 (“Perego ’422”); • JEDEC Standards; • U.S. Patent Application Publication No. 2006/0277355 (“Ellsberry”); • U.S. Patent No. 7,024,518 (“Halbert ’518”); • U.S. Patent Application Publication No. 2002/0112119 (“Halbert ’119”); • Kentron’s Quad Band Memory System (“QBM”); • Micron DDR SDRAM RDIMM, MT36VDDF12872 & MT36VDDF25672 Product; • FBDIMM Architecture & Protocol; • U.S. Patent No. 6,615,345 (“LaBerge ’345”); • U.S. Patent Application Publication No. 2003/0039151 (“Matsui ’151”); • U.S. Patent No. 5,712,811 (“Kim ’811”); • U.S. Patent Application Publication No. 2006/0117152 (“Amidi”); • U.S. Patent Application Publication No. 2003/0204688 (“Lee ’688”);

	• U.S. Patent Application Publication No. 2003/0145156 (“Khandekar”); • U.S. Patent No. 6,862,653 (“Dodd”); • U.S. Patent No. 7,240,145 (“Holman”); • DDR SDRAM RDIMM Design Specification JEDEC Standard 21-C (4.20.4) (“JEDEC Standard 21-C”); • U.S. Patent No. 7,155,627 (“Matsui ’627”); • DDR2 SDRAM Specification JEDEC Standard JESD79-2A (“JESD79-2A”); • U.S. Patent No. 7,092,299 (“Kwak”); • U.S. Patent Application Publication No. 2002/0118578 (“Janzen ’578”); • Synchronous DRAM Architectures, Organizations, and Alternative Technologies (Bruce Jacob); • U.S. Patent Application Publication No. 2003/0133331 (“LaBerge ’331”); • U.S. Patent Publication. No. 2002/0188816 (“Johnson ’816”); • U.S. Patent Application Publication No. 2004/0034755 (“LaBerge ’755”); • U.S. Patent Application Publication No. 2005/0050255 (“Jeddeloh”); • U.S. Patent No. 6,446,184 (“Dell ’184”); • U.S. Patent No. 7,149,841 (“LaBerge ’841”); • U.S. Patent No. 7,366,827 (“Lee ’827”); • U.S. Patent No. 7,043,617 (“Williams ’617”); • U.S. Patent No. 7,433,258 (“Rao”); • U.S. Pat. No. 5,581,498 (“Ludwig”); • U.S. Patent No. 5,926,827 (“Dell ’827”); • U.S. Patent Application Publication No. US 2006/0195631 (“Rajamani”); • U.S. Patent Application Publication No. 2005/0198449 (“Haskell”); • U.S. Patent Application Publication No. 2005/0257109 (“Averbuj”); • U.S. Patent No. 6,820,163 (“McCall”); • U.S. Patent No. 6,564,287 (“Lee ’287”); • U.S. Patent No. 7,222,224 (“Woo”); • U.S. Patent No. 7,334,150 (“Ruckerbauer”); • U.S. Patent No. 7,289,383 (“Cornelius”); • U.S. Patent No. 6,392,909 (“Jang”); • U.S. Patent No. 6,529,423 (“Yoon”);
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	• U.S. Patent No. 6,262,938 (“Lee ’938”); • U.S. Patent No. 7,206,896 (“Perego ’896”); • U.S. Patent No. 6,205,062 (“Kim ’062”); • U.S. Patent No. 7,212,424 (“Johnson ’424”); and/or • The knowledge of a person of ordinary skill in the art.
FBDIMM Architecture & Protocol	• The ’215 Patent’s Admitted Prior Art (“APA”); • U.S. Patent No. 7,363,422 (“Perego ’422”); • JEDEC Standards; • U.S. Patent Application Publication No. 2006/0277355 (“Ellsberry”); • U.S. Patent No. 7,024,518 (“Halbert ’518”); • Kentron’s Quad Band Memory System (“QBM”); • DDR3 Functional Outlook; • U.S. Patent No. 6,615,345 (“LaBerge ’345”); • U.S. Patent Application Publication No. 2003/0039151 (“Matsui ’151”); • U.S. Patent No. 5,712,811 (“Kim ’811”); • U.S. Patent Application Publication No. 2006/0117152 (“Amidi”); • U.S. Patent No. 7,212,424 (“Johnson ’424”); • U.S. Patent No. 7,149,841 (“LaBerge ’841”); • U.S. Patent No. 7,366,827 (“Lee ’827”); • U.S. Patent Application Publication No. 2003/0204688 (“Lee ’688”); • U.S. Patent Application Publication No. 2003/0145156 (“Khandekar”); • U.S. Patent No. 6,862,653 (“Dodd”); • U.S. Patent No. 7,240,145 (“Holman”); • DDR SDRAM RDIMM Design Specification JEDEC Standard 21-C (4.20.4) (“JEDEC Standard 21-C”); • U.S. Patent No. 7,155,627 (“Matsui ’627”); • DDR2 SDRAM Specification JEDEC Standard JESD79-2A (“JESD79-2A”); • U.S. Patent No. 7,092,299 (“Kwak”); • U.S. Patent Application Publication No. 2002/0118578 (“Janzen ’578”); • Synchronous DRAM Architectures, Organizations, and Alternative Technologies (Bruce Jacob); • U.S. Patent Application Publication No.

	2003/0133331 (“LaBerge ’331”); • U.S. Patent Publication. No. 2002/0188816 (“Johnson ’816”); • U.S. Patent Application Publication No. 2004/0034755 (“LaBerge ’755”); • U.S. Patent Application Publication No. 2005/0050255 (“Jeddeloh”); • U.S. Patent No. 6,446,184 (“Dell ’184”); • U.S. Patent Application Publication No. 2005/0257109 (“Averbuj”); • U.S. Patent No. 6,820,163 (“McCall”); • U.S. Patent No. 6,564,287 (“Lee ’287”); • U.S. Patent No. 7,222,224 (“Woo”); • U.S. Patent No. 7,334,150 (“Ruckerbauer”); • U.S. Patent No. 7,289,383 (“Cornelius”); • U.S. Patent No. 6,392,909 (“Jang”); • U.S. Patent No. 6,529,423 (“Yoon”); • U.S. Patent No. 6,262,938 (“Lee ’938”); • U.S. Patent No. 7,206,896 (“Perego ’896”); • U.S. Patent No. 6,205,062 (“Kim ’062”); • U.S. Patent No. 7,043,617 (“Williams ’617”); • Micron DDR SDRAM RDIMM, MT36VDDF12872 & MT36VDDF25672 Product; • U.S. Patent No. 7,433,258 (“Rao”); • U.S. Pat. No. 5,581,498 (“Ludwig”); • U.S. Patent No. 5,926,827 (“Dell ’827”); • U.S. Patent Application Publication No. US 2006/0195631 (“Rajamani”); • U.S. Patent Application Publication No. 2005/0198449 (“Haskell”); • and/or • The knowledge of a person of ordinary skill in the art.
Micron DDR SDRAM RDIMM, MT36VDDF12872 & MT36VDDF25672 Datasheet	• The ’215 Patent’s Admitted Prior Art (“APA”); • U.S. Patent Application Publication No. 2003/0204688 (“Lee ’688”); • DDR3 Functional Outlook; • U.S. Patent Application Publication No. 2006/0117152 (“Amidi”); • FBDIMM Architecture & Protocol; • U.S. Patent Application Publication No. 2003/0145156 (“Khandekar”); • U.S. Patent No. 6,862,653 (“Dodd”);

	• U.S. Patent Application Publication No. 2003/0117864 (“Hampel”); • U.S. Patent No. 6,493,250 (“Halbert ’250”); • U.S. Patent No. 7,240,145 (“Holman”); • U.S. Patent Application Publication No. 2002/0112119 (“Halbert ’119”); • U.S. Patent Application Publication No. 2001/0008006 (“Klein”); • JEDEC Standards; • U.S. Patent No. 6,615,345 (“LaBerge ’345”); • DDR SDRAM RDIMM Design Specification JEDEC Standard 21-C (4.20.4) (“JEDEC Standard 21-C”); • Synchronous DRAM Architectures, Organizations, and Alternative Technologies (Bruce Jacob); • Kentron’s Quad Band Memory System (“QBM”); • U.S. Patent No. 7,206,896 (“Perego ’896”) • U.S. Patent No. 6,529,423 (“Yoon”); • U.S. Patent No. 6,564,287 (“Lee ’287”); • U.S. Patent No. 6,262,938 (“Lee ’938”); • U.S. Patent No. 5,712,811 (“Kim ’811”); • U.S. Patent No. 6,205,062 (“Kim ’062”); • U.S. Patent No. 7,222,224 (“Woo”); • U.S. Patent No. 7,363,422 (“Perego ’422”); • U.S. Patent No. 7,334,150 (“Ruckerbauer”); • U.S. Patent Application Publication No. 2006/0277355 (“Ellsberry”); • U.S. Patent Application Publication No. 2005/0050255 (“Jeddeloh”); • U.S. Patent No. 7,212,424 (“Johnson ’424”); • U.S. Patent No. 5,926,827 (“Dell ’827”); • U.S. Patent Application Publication No. 2002/0118578 (“Janzen ’578”); • U.S. Patent Application Publication No. 2005/0198449 (“Haskell”); • U.S. Patent Application Publication No. 2003/0133331 (“LaBerge ’331”); • U.S. Patent Application Publication No. 2005/0257109 (“Averbuj”); • U.S. Patent No. 7,024,518 (“Halbert ’518”) • U.S. Patent Application Publication No. 2003/0039151 (“Matsui ’151”);
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	• U.S. Patent No. 7,366,827 (Lee '827); • DDR2 SDRAM Specification JEDEC Standard JESD79-2A ("JESD79-2A"); and/or • The knowledge of a person of ordinary skill in the art.
Micron DDR SDRAM RDIMM, MT36VDDF12872 and/or MT36VDDF25672 Products	• The '215 Patent's Admitted Prior Art ("APA"); • U.S. Patent Application Publication No. 2003/0204688 ("Lee '688"); • DDR3 Functional Outlook; • U.S. Patent Application Publication No. 2006/0117152 ("Amidi"); • FBDIMM Architecture & Protocol; • U.S. Patent Application Publication No. 2003/0145156 ("Khandekar"); • U.S. Patent No. 6,862,653 ("Dodd"); • U.S. Patent Application Publication No. 2003/0117864 ("Hampel"); • U.S. Patent No. 6,493,250 ("Halbert '250"); • U.S. Patent No. 7,240,145 ("Holman"); • U.S. Patent Application Publication No. 2002/0112119 ("Halbert '119"); • U.S. Patent Application Publication No. 2001/0008006 ("Klein"); • JEDEC Standards; • U.S. Patent No. 6,615,345 ("LaBerge '345"); • DDR SDRAM RDIMM Design Specification JEDEC Standard 21-C (4.20.4) ("JEDEC Standard 21-C"); • Synchronous DRAM Architectures, Organizations, and Alternative Technologies (Bruce Jacob); • Kentron's Quad Band Memory System ("QBM"); • U.S. Patent No. 7,206,896 ("Perego '896") • U.S. Patent No. 6,529,423 ("Yoon"); • U.S. Patent No. 6,564,287 ("Lee '287"); • U.S. Patent No. 6,262,938 ("Lee '938"); • U.S. Patent No. 5,712,811 ("Kim '811"); • U.S. Patent No. 6,205,062 ("Kim '062"); • U.S. Patent No. 7,222,224 ("Woo"); • U.S. Patent No. 7,363,422 ("Perego '422"); • U.S. Patent No. 7,334,150 ("Ruckerbauer"); • U.S. Patent Application Publication No. 2006/0277355 ("Ellsberry");

	• U.S. Patent Application Publication No. 2005/0050255 (“Jeddeloh”); • U.S. Patent No. 7,212,424 (“Johnson ’424”); • U.S. Patent No. 5,926,827 (“Dell ’827”); • U.S. Patent Application Publication No. 2002/0118578 (“Janzen ’578”); • U.S. Patent Application Publication No. 2005/0198449 (“Haskell”); • U.S. Patent Application Publication No. 2003/0133331 (“LaBerge ’331”); • U.S. Patent Application Publication No. 2005/0257109 (“Averbuj”); • U.S. Patent No. 7,024,518 (“Halbert ’518”); • U.S. Patent Application Publication No. 2003/0039151 (“Matsui ’151”); • U.S. Patent No. 7,366,827 (Lee ’827); • DDR2 SDRAM Specification JEDEC Standard JESD79-2A (“JESD79-2A”); and/or • The knowledge of a person of ordinary skill in the art.
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As mentioned above, Defendants have not yet completed their search or discovery concerning additional prior art. Moreover, the exemplary combinations are provided based on Defendants’ current understanding of the Asserted Claims and Plaintiff’s apparent view of the scope of those claims as shown, for example, in Plaintiff’s Infringement Contentions. Further, a *Markman* Order has not yet been issued in this case. As such, Defendants’ inclusion of exemplary combinations does not preclude them from identifying other invalidating combinations as appropriate, and Defendants reserve the right to identify additional specific combinations as well as to detail and explain such combinations.

3. U.S. Patent No. 11,093,417

Pursuant to P.R. 3-3(a) and (b), Defendants identify in Appendix C the prior art references that render obvious the Asserted Claims of the ’417 patent and include below exemplary

combinations showing the obviousness of the '417 patent Asserted Claims in view of the prior art. To the extent Plaintiff contends that an element is not disclosed in any one of the anticipatory references described in Appendix C, the limitation would have been obvious in light of the disclosures within the reference and the knowledge of one of ordinary skill in the art at the time of the '417 patent. Moreover, to the extent Plaintiff contends that an element is not disclosed in any one of the anticipatory references described in Appendix C, such reference may be combined with any other references listed in Appendix C for such element, thereby rendering the claims invalid for obviousness.

To the extent a finder of fact determines that a limitation of any of the '417 patent Asserted Claims is not disclosed by one of the references identified above pursuant to P.R. 3-3(a), the claim is nevertheless unpatentable as obvious because they contain nothing that constitutes a patentable innovation. To the extent a finder of fact determines that a limitation of the '417 patent Asserted Claims is not anticipated, it does not go beyond combining familiar elements according to known methods to achieve predictable results or does more than choose between clear alternatives known to those of ordinary skill in the art.

(a) Obviousness Rationale

For at least the reasons described in these contentions, it would have been obvious to one of ordinary skill in the art to combine any of a number of prior art references, including any combination of those prior art references identified in Appendix C along with the knowledge of one of ordinary skill in the art to meet the limitations of the '417 patent Asserted Claims. Moreover, as mentioned above, Defendants have not yet completed their search or discovery concerning additional prior art. As such, Defendants' inclusion of exemplary combinations does not preclude them from identifying other invalidating combinations as appropriate, and Defendants

reserve the right to identify additional specific combinations as well as to detail and explain such combinations.

To the extent not anticipated, the '417 patent Asserted Claims represent no more than the result of ordinary variations of the prior art. Defendants further believe that no showing of a specific motivation to combine prior art is required to combine the references disclosed above and in the attached charts, as each combination of art would have no unexpected results, and at most would simply represent a known alternative to one of ordinary skill in the art. *See KSR Int'l Co. v. Teleflex, Inc.*, 550 U.S. 398, 415-16 (2007) (rejecting the Federal Circuit's "rigid" application of the teaching, suggestion, or motivation to combine test, instead espousing an "expansive and flexible" approach). Indeed, the Supreme Court held that a person of ordinary skill in the art is "a person of ordinary creativity, not an automaton" and "in many cases a person of ordinary skill in the art will be able to fit the teachings of multiple patents together like pieces of a puzzle." *Id.* at 420-21. Nevertheless, in addition to the information contained elsewhere in these contentions, Defendants identify motivation and reason to combine the cited art.

One or more combinations of the prior art references identified in Appendix C would have been obvious because these references would have been combined using: known methods to yield predictable results; known techniques in the same way; a simple substitution of one known, equivalent element for another to obtain predictable results; and/or a teaching, suggestion, or motivation in the prior art generally. In addition, it would have been obvious to try combining the prior art references identified above because there were only a finite number of predictable solutions and/or because known work in one field of endeavor prompted variations based on predictable design incentives and/or market forces either in the same field or a different one. Further, the combinations of the prior art references identified in Appendix C would have been

obvious because the combinations represent known potential options with a reasonable expectation of success.

Additional evidence that there would have been a motivation to combine the prior art references identified above includes the interrelated teachings of multiple prior art references; common authorship; the effects of demands known to the design community or present in the marketplace; the existence of a known problem for which there was an obvious solution encompassed by the '417 patent Asserted Claims; the existence of a known need or problem in the field of the endeavor at the time of the alleged invention(s); and the background knowledge that would have been possessed by a person having ordinary skill in the art.

Thus, the motivation to combine the teachings of the prior art references disclosed in Appendix C is found in the references themselves and also in: (1) the nature of the problem being solved; (2) the express, implied and inherent teachings of the prior art; (3) the knowledge of persons of ordinary skill in the art; (4) the predictable results obtained in combining the different elements of the prior art; (5) the predictable results obtained in simple substitution of one known element for another; (6) the use of a known technique to improve similar devices, methods, or products in the same way; (7) the predictable results obtained in applying a known technique to a known device, method, or product ready for improvement; (8) the finite number of identified predictable solutions that had a reasonable expectation of success; and (9) known work in various technological fields that could be applied to the same or different technological fields based on design incentives or other market forces.

Additionally, it would be obvious to one of ordinary skill in the art to consult and/or combine any of the prior art listed in Appendix C because all of these references relate to the same area of technology and/or are from analogous art. The '417 patent Asserted Claims are generally

directed to a memory module with data buffering. '417 patent at Title, Abstract, 22:62-25:3. The '417 patent Asserted Claims merely unite old elements, well known in the field, with no change in their respective function or result. Given the interrelated teachings of the prior art, the effects of demands known to the design community or present in the marketplace, and the background knowledge possessed by a person having ordinary skill in the art, it would have been obvious for one of ordinary skill in the art to combine these familiar elements, disclosed and/or embodied in the prior art listed above to practice the '417 patent Asserted Claims.

The '417 patent purports to describe “devices and methods for improving the performance, the memory capacity, or both, of memory modules.” '417 patent at 1:47-50. All of the '417 patent Asserted Claims generally concern a memory module operable in a computer system that is purportedly configured to buffer certain control signals. Such technology, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff’s infringement contentions, was widely known before the alleged priority date of the '417 Patent, as evidenced by the references in Appendix C. *See, e.g.*, '417 patent at 1:54-63, 1:64-2:46, 2:47-53, 2:65-3:6, 6:51-7:3, 7:40-60, 9:54-10:4, 15:63-16:30, 20:4-23, 20:24-43, 23:49-54; *see also* C1 (the '417 Patent’s Admitted Prior Art).

One of ordinary skill in the art would have been motivated to combine any of the references in Appendix C because at the time of the alleged invention improving a memory module’s capacity (density) was a common problem with a well-known solution. *See, e.g.*, '417 patent at 2:54-64, 15:63-16:16; *see also* Mailloux at 1:31-35, 2:26-46; LaBerge '032 at 1:42-65; Ellsberry at Abstract, [0005], [0010], [0012]; Perego '422 at 1:18-30; Amidi at [0002], [0008]; Halbert '518 at 3:32-41; Halbert '119 at [0022]; Halbert '250 at 3:35-42; Rao at 2:1-8; MicronRDIMM at 1, 6-8, 18-20; JEDEC Standards; JEDEC Standard 21-C at 4.20.4-5, 4.20.4-25 through 4.20.4-27,

JESD79 at 1, 2, 8; JESD79-2 at 10, 12; JESD79C at 1, 7, 8; QBM (see, e.g. QBM Specification Rev. 0.93 at 5, 9; QBM2 Interface Overview at 3; QBM2 Technical Features Overview at 3-5; QBM Doubling DDR Memory Bandwidth at 10); FBDIMM Architecture & Protocol (see, e.g. FBDIMM AP Rev. 0.1 at 7); Dell '074 at 1:44-67; Gene at 1:61-2:22; Wong '281 at 2:4-19; Wong '868 at 1:57-2:10, 2:66-3:4; Johnson at 1:36-52; Kim at Abstract, 1:6-11, 3:21-26; McCall at 1:8-20; *see also* Appendix C.

Further, it was common knowledge to one of ordinary skill in the art at the time of the alleged invention that memory density (rank) multiplication can improve performance and/or reduce costs of the memory modules. *See, e.g.,* '417 patent at 15:63-16:30; *see also* LaBerge '032 at 1:42-65; Amidi at [0008]-[0011]; Ellsberry at Abstract, [0005], [0010], [0012]; Perego '422 at 1:18-30; Halbert '518 at 3:32-41; Halbert '119 at Abstract; Halbert '250 at 3:35-42; MicronRDIMM at 1, 6-8, 18-20; JEDEC Standards (see, e.g., JESD79C at 1, 2, 5, 8); QBM (see, e.g. QBM Specification Rev. 0.93 at 5, 9; QBM2 Interface Overview at 3; QBM2 Technical Features Overview at 3-5; QBM Doubling DDR Memory Bandwidth at 10); *see also* Appendix C. Furthermore, it was well known to one of ordinary skill in the art at the time of the alleged invention that the use of buffer devices to isolate signals (e.g., data, control, and address signals) of memory devices also improves memory capacity and enhances performance, among other advantageous effects. *See, e.g.,* Mailloux at 12:65-13:13, 13:26-30, 14:46-15:3; Perego '422 at 3:23-40, 4:38-45, 6:12-56; Halbert '518 at 3:42-57, 4:23-35, 9:4-19; Halbert '119 at [0023], [0024], [0026]; Halbert '250 at Abstract, 9:28-37; Ellsberry at [0039]; Klein at [0022], [0026], [0028], [0039]; JEDEC Standards JEDEC Standard 21-C at 7, 71; JESD79-2A at 14, 51; QBM (see, e.g., QBM Specification Rev. 0.93 at 6, 9-11, 34, 36; QBM2 Interface Overview at 3; QBM Informational Showing Item #1133 at 4-8; QBM Informational Showing Item #1341 at 3, 9, 15;

QBM2 Technical Features Overview at 3-5, 14; QBM2 Technical Highlights at 19; QBM Platform Conference at 17-22; QBM Doubling DDR Memory Bandwidth at 8; QBM Doubling DDR Memory Bandwidth at 11-13; QBM2 Technology Overview at 5, 8, 11, 12, 15, 17; QBM Interim JEDEC Meeting at 6, 11); DDR3 Functional Outlook at 6, 10-12, 14-20, 22; Dodd at 1:64-2:13; Averbuj at [0048]; *see also* Appendix C.

It was also common knowledge to one of ordinary skill in the art at the time of the alleged invention that to ensure proper data communication and memory operation, data transfer to or from memory modules must account for latency values, including a CAS latency value, among others. *See, e.g.*, LaBerge '032 at 2:18-29, 4:53-5:10, 5:12-35, 5:36-60, 5:61-6:13, 6:39-51, Fig. 4; Perego '422 at 11:56-12:3, 12:20-34, 12:65-13:5, 13:18-28, 17:61-67, 18:65-19:4; Mailloux at 2:30-38, 4:10-24, 6:24-50, 6:53-7:56, 9:24-38, 12:18-25, 17:52-56; Reeves at 6:64-7:27; Blockmon at [0007]-[0010], [0027]; Jacob at 10, 15, 16; LaBerge '331 at Absrtact, [0007], [0009], [0023], [0024]; LaBerge '755 at [0005]-[0008], [0023]-[0030]; Williams at 1:19-2:27, 6:21-34, 8:1-54; Kim at 1:25-59, 3:25-56, 4:19-54, 5:5-20; Lee '287 at Title, Abstract, 1:17-25, 7:10-15, 7:61-65, 8:8-15, 8:58-63, 8:64-9:4, 9:55-10:-13; Lee '938 at Title, Abstract, 1:12-67, 5:13-67, 6:1-4, 7:57-64, 9:49-59, 9:66-10:31, 12:36-61. 10:6-31, 12:35-61; Jang at Title, Abstract, Fig. 1, Fig. 2, Fig. 7, 1:28-50, 1:54-2:11, 2:22-28, 2:29-40, 3:7-14, 3:15-28, 3:40-48, 5:48-6:13; Yoon at Abstract, Fig. 3, Fig. 5, 1:31-67, 2:1-40, 2:63-3:12, 3:20-45, 3:66-7:32; Rao at 1:18-48, 3:4-4:51, 5:3-37; *see also* Appendix C.

One of ordinary skill in the art would have been motivated to combine any of the references in Appendix C at the time of the alleged invention. Common problems with conventional techniques for improving a memory module's capacity or density, improving performance, flexibility, and other memory characteristics were known to persons of ordinary skill in the art and

implementing memory density multiplication, signal buffering, and data isolation were well-known solutions to achieve improved performance and capacity. *See, e.g.*, '417 patent at 15:63-16:30; *see also* Mailloux at 1:31-35, 2:26-46, 12:65-13:13, 13:26-30, 14:46-15:3; LaBerge '032 at 1:42-65; Amidi at [0008]-[0011]; Ellsberry at Abstract, [0005], [0010], [0012], [0039]; Perego '422 at 1:18-30, 3:23-40, 4:38-45, 6:12-56; Halbert '518 at 3:32-41, 3:42-57, 4:23-35, 9:4-19; Halbert '119 at [0022], [0023], [0024], [0026]; Halbert '250 at Abstract, 3:32-41, 9:28-37; Klein at [0039]; MicronRDIMM at 1, 6-8, 18-20; JEDEC Standards (*see, e.g.*, JEDEC Standard 21-C at 7, 25-27, 71; JESD79-2A at 14, 51); DDR3 Functional Outlook at 6, 10-12, 14-20, 22; QBM (*see, e.g.*, QBM Specification Rev. 0.93 at 6, 9-11, 34, 36; QBM2 Interface Overview at 3; QBM Informational Showing Item #1133 at 4-8; QBM Informational Showing Item #1341 at 3, 9, 15; QBM2 Technical Features Overview at 3-5, 14; QBM2 Technical Highlights at 19; QBM Platform Conference at 17-22; QBM Doubling DDR Memory Bandwidth at 8; QBM Doubling DDR Memory Bandwidth at 11-13; QBM2 Technology Overview at 5, 8, 11, 12, 15, 17; QBM Interim JEDEC Meeting at 6, 11); FBDIMM Architecture & Protocol (*see, e.g.*, FBDIMM AP Rev. 0.1 at 7); Jacob at 1, 2; *see also* Appendix C.

It was well-known to one of ordinary skill in the art before the time of the '417 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that a memory module can operate in a computer system to communicate data with a memory controller of the computer system via a N-bit wide memory bus in response to read or write memory commands received from the memory controller, the memory bus including address and control signal lines and data signal lines. *See* citations identified for claim element [1pre] provided in attached Exhibits C1 through C18.

It was well-known to one of ordinary skill in the art before the time of the '417 patent, at

least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that a memory module can include a printed circuit board having a plurality of edge connections configured to be electrically coupled to a corresponding plurality of contacts of a module slot of the computer system. See citations identified for claim element [1a] provided in attached Exhibits C1 through C18.

It was well-known to one of ordinary skill in the art before the time of the '417 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that a memory module can include logic coupled to the printed circuit board and configurable to receive a set of input address and control signals associated with a read or write memory command via the address and control signal lines and to output a set of registered address and control signals in response to the set of input address and control signals, the set of input address and control signals including a plurality of input chip select signals and other input address and control signals, the plurality of input chip select signals including one chip select signal having an active signal value and one or more other input chip select signals each having a non-active signal value, the set of registered address and control signals including a plurality of registered chip select signals corresponding to respective ones of the plurality of input chip select signals and other registered address and control signals corresponding to respective ones of the other input address and control signals, the plurality of registered chip select signals including one registered chip select signal having an active signal value and one or more other registered chip select signals each having a non-active signal value, wherein the logic is further configurable to output data buffer control signals in response to the read or write memory command. See citations identified for claim element [1b] provided in attached Exhibits C1 through C18.

It was well-known to one of ordinary skill in the art before the time of the '417 patent, at

least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that a memory module can include memory devices mounted on the printed circuit board and arranged in a plurality of N-bit wide ranks, wherein the plurality of N-bit wide ranks correspond to respective ones of the plurality of registered chip select signals such that each of the plurality of registered chip select signals is received by memory devices one respective N-bit wide rank of the plurality of N-bit-wide ranks, wherein one of the plurality of N-bit wide ranks including memory devices receiving the registered chip select signal having the active signal value and the other registered address and control signals is configured to receive or output a burst of N-bit wide data signals in response to the read or write command. See citations identified for claim element [1c] provided in attached Exhibits C1 through C18.

It was well-known to one of ordinary skill in the art before the time of the '417 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that a memory module can include circuitry coupled between the data signal lines in the N-bit wide memory bus and corresponding data pins of memory devices in each of the plurality of N-bit wide ranks, the circuitry being configurable to transfer the burst of N-bit wide data signals between the N-bit wide memory bus and the memory devices in the one of the plurality of N-bit wide ranks in response to the data buffer control signals and in accordance with an overall CAS latency of the memory module. See citations identified for claim element [1d] provided in attached Exhibits C1 through C18; Yoon at Abstract, Fig. 1, Fig. 3, Fig. 5, 1:31-2:39, 2:63-3:12, 3:20-45, 4:16-5:15; Lee '287 at 1:17-62, 2:25-59, 4:10-63, 4:64-5:27, 5:45-6:8; Lee '938 at Abstract, 1:45-67, 5:20-41, 7:57-64, 10:17-52, 12:35-61; Jang at Abstract, Fig. 1, Fig. 2, 1:28-50, 2:4-11, 3:7-48, 3:49-67; 4:54-5:13.

It was well-known to one of ordinary skill in the art before the time of the '417 patent, at

least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that, in a memory module, data transfers through the circuitry can be registered for an amount of time delay such that the overall CAS latency of the memory module is greater than an actual operational CAS latency of each of the memory devices. See citations identified for claim element [2] provided in attached Exhibits C1 through C18; Yoon at Fig. 3, Fig. 5, 1:31-67, 2:1-24, 2:63-3:12, 5:25-36, 7:12-32; Lee '287 at 1:17-25, 6:19-7:14, 7:61-65, 8:8-15, 10:5-13; Lee '938 at 1:45-67, 5:20-41, 10:17-48, 12:35-61; Jang at 1:28-50, 2:4-11, 5:48-6:13.

It was well-known to one of ordinary skill in the art before the time of the '417 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that, in a memory module, the burst of N-bit wide data signals can include a set of consecutively transmitted data bits for each data signal line in the memory bus, and the set of consecutively transmitted data bits can be successively transferred through the circuitry in response to the data buffer control signals. See citations identified for claim element [3] provided in attached Exhibits C1 through C18.

It was well-known to one of ordinary skill in the art before the time of the '417 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that, in a memory module, each of the memory devices can be 4-bits wide, and each of the plurality of ranks can be 64-bits or 72-bits wide and include 16 or 18 memory devices configured in pairs. See citations identified for claim element [4] provided in attached Exhibits C1 through C18.

It was well-known to one of ordinary skill in the art before the time of the '417 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that, in a memory module, the memory devices can be organized in four

ranks and the set of input address and control signals include four chip select signals, one for each of the four ranks. *See* citations identified for claim element [5] provided in attached Exhibits C1 through C18.

It was well-known to one of ordinary skill in the art before the time of the '417 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that, in a memory module, the circuitry can include logic pipelines configurable to enable the data transfers between the memory devices and the memory bus through the circuitry. *See* citations identified for claim element [6] provided in attached Exhibits C1 through C18.

It was well-known to one of ordinary skill in the art before the time of the '417 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that, in a memory module, the logic is further configured to report the overall CAS latency to the memory controller in response to a mode register set command received from the memory controller. *See* citations identified for claim element [7] provided in attached Exhibits C1 through C18; *see also* Lee '287 at 1:17-25, 2:25-47, 4:28-49, 7:61-65, 8:8-15, 8:64-9:4; 10:5-13; Lee '938 at Abstract, 1:45-67, 5:20-41, 7:57-64, 10:6-16, 10:17-50, 12:35-61; Jang at Abstract, Fig. 1, Fig. 2, 1:28-50, 1:54-2:11, 3:29-49, 5:10-47, 5:48-6:13.

It was well-known to one of ordinary skill in the art before the time of the '417 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that a memory module can have a specified data rate, and the burst of N-bit wide data signals can be transferred between the one of the plurality of N-bit wide ranks and the memory controller at the specified data rate. *See* citations identified for claim element [8] provided in attached Exhibits C1 through C18.

It was well-known to one of ordinary skill in the art before the time of the '417 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that a memory module can further comprise a phase locked loop clock driver configured to output a clock signal in response to one or more signals received from the memory controller, wherein the predetermined amount of time delay is at least one clock cycle time delay. *See* citations identified for claim element [9] provided in attached Exhibits C1 through C18.

It was well-known to one of ordinary skill in the art before the time of the '417 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that, in a memory module, the memory devices can be dynamic random access memory devices configured to operate synchronously with the clock signal, and wherein each memory device in the one of the plurality of N-bit wide ranks is configured to receive or output a respective set of bits of the burst of N-bit wide data signals on both edges of each of a respective set of data strobes. *See* citations identified for claim element [10] provided in attached Exhibits C1 through C18.

It was well-known to one of ordinary skill in the art before the time of the '417 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that, in a memory module, the circuitry can include data paths, and can be configurable to enable the data paths in response to the data buffer control signals so that the burst of N-bit wide data signals are transferred via the data paths. *See* citations identified for claim element [11] provided in attached Exhibits C1 through C18.

It was well-known to one of ordinary skill in the art before the time of the '417 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's

infringement contentions, that, in a memory module, the data paths can be disabled when no data signals associated with any memory command are being transferred through the circuitry. *See* citations identified for claim element [12] provided in attached Exhibits C1 through C18.

It was well-known to one of ordinary skill in the art before the time of the '417 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that, in a memory module, each of the memory devices can have a corresponding load, and the circuitry is configured to isolate the loads of the memory devices from the memory bus. *See* citations identified for claim element [13] provided in attached Exhibits C1 through C18.

It was well-known to one of ordinary skill in the art before the time of the '417 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that a memory module can have a specified data rate, and the burst of N-bit wide data signals can be transferred through the data paths at the specified data rate. *See* citations identified for claim element [14] provided in attached Exhibits C1 through C18.

It was well-known to one of ordinary skill in the art before the time of the '417 patent, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, that, in a memory module, the read or write command can be a write memory command, the burst of N-bit wide data signals can include a respective series of write data bits received by the circuitry from a respective one of the data signal lines, and the respective series of write data bits can be successively transferred via a respective one of the data paths. *See* citations identified for claim element [15] provided in attached Exhibits C1 through C18.

In addition, the prior art also provided sets of finite, identified, predictable solutions for known problems that would have been obvious to those of ordinary skill to try with a reasonable

expectation of success. For example, it would have been obvious to one of ordinary skill in the art at the time that of alleged invention to mount or couple the disclosed memory devices and circuitry of a memory module to a printed circuit board having a plurality of edge connections configured to be electrically coupled to a corresponding plurality of contacts of a module slot of the computer system. It would have been also obvious to one of ordinary skill in the art at the time of alleged invention to arrange the disclosed memory devices in a plurality of N-bit wide ranks including circuitry coupled between the data signal lines in the N-bit wide memory bus and corresponding data pins of memory devices in each of the plurality of N-bit wide ranks. It would have been also obvious to one of ordinary skill in the art at the time of alleged invention that the disclosed memory devices are 4-bits wide, and each of the plurality of ranks is 64-bits or 72-bits wide and includes 16 or 18 memory devices configured in pairs, including organized in four ranks. It would have been also obvious to one of ordinary skill in the art at the time of alleged invention for a memory module to have a specified data rate, and a burst of N-bit wide data signals is transferred between one of a plurality of N-bit wide ranks and the memory controller at the specified data rate. It would have been also obvious to one of ordinary skill in the art at the time of alleged invention to utilize or integrate in the disclosed memory module various traditional and common at the time memory module components or devices, including without limitation logic, logic pipelines, a phase locked loop clock driver, and alike. It would have been also obvious to one of ordinary skill in the art at the time of alleged invention that the disclosed memory module can use various traditional and common memory commands and signals, including without limitation address and (memory) control signals, registered address and (memory) control signals, chip select signals, registered chip select signals, clock signals, receive or output data signals, data strobe signals, activation commands, read commands, write commands, mode register set commands, precharge commands,

and refresh commands. It would have been also obvious to one of ordinary skill in the art at the time of alleged invention that the disclosed memory module receives and buffers any of such commands or signals.

The prior art references provide motivations to combine because they describe the field of the '417 patent, teach improvements, explain desired features, and even expressly state that one of ordinary skill in the art would be able to apply their teachings to related systems or methods. *See, e.g.*, '417 patent at 1:54-2:53, 6:51-7:3, 7:32-39, 9:46-10:4, 15:40-47, 17:2-5, 20:4-43, 26:3-6, 33:21-24, 33:48-51, 34:44-47, 40:38-40, 42:2-4; *see also* Amidi at [0002], [0011], [0025]-[0028], [0071]; Ellsberry at [0002]-[0005], [0010], [0012], [0023]-[0027]; Holman at 2:43-54; LaBerge '032 at 2:58-62, 3:52-56, 4:17-20, 6:17-21, 6:54-58; Perego '422 at 1:12-2:3, 2:7-30; Perego '896 at 1:18-2:6, 3:24-60, 9:35-50; Halbert '518 at 3:32-41; Halbert '119 at [0058], [0062]; Halbert '250 at 10:54-62; Rao at 2:1-8, 4:52-67; Klein at [0024], [0029]; Dodd at 1:8-14; Khandekar at [0001]-[0003]; Hampel at [0003], [0011], [0059]; Lee '688 at [0003], [0021]-[0034], [0081]; Mailloux at 10:14-20; 10:26-32, 12:44-54, 13:62-67, 18:40-54, 20:1-7; JEDEC Standards; JEDEC Standard 21-C at 4.20.4-5; JESD79 at 1, 2, 8; JESD79-2 at 10, 12; JESD79C at 1, 7, 8; QBM (*see, e.g.* QBM Specification Rev. 0.93 at 5, 9; QBM2 Interface Overview at 3; QBM2 Technical Features Overview at 3-5; QBM Doubling DDR Memory Bandwidth at 10); DDR3 Functional Outlook at 6, 10-12, 14-20, 22; Matsui '151 at [0001], [0010]-[0021]; Matsui '627 at 1:7-10, 2:28-8:37; Kim '811 at Abstract, 1:6-11, 3:21-36, 4:7-41; Kim '062 at Abstract, 1:11-24, 3:39-4:10, 4:16-5:20, 6:12-7:14, Kwak at 1:12-2:47, 3:25-4:11, 7:21-31; Janzen '578 at [0001], [0007], [0017], [0038]; LaBerge '331 at [0002], [0005]-[0009], [0017]-[0022]; LaBerge '755 at Abstract, [0002], [0005]-[0008], [0016]-[0018], [0022]; LaBerge '841 at 1:6-64, 2:15-50, 2:54-3:3, 3:36-56; Johnson '816 at [0002], [0004]-[0006], [0009], [0017], [0019]; Jeddeloh at Abstract,

[0001]-[0012]; Dell '184 at Abstract, 1:23-27, 1:30-2:45, 2:48-3:5, Fig. 1; Dell '827 at 1:1267, 2:23-63, Fig. 1; Lee '827 at 1:16-67, 2:21-3:24; Lee '938 at 1:11-30, 2:30-3:45, 6:57-7:17; Williams '617 at 1:13-2:6, 2:28-22, 3:8-67, Ludwig at 1:9-40, 1:43-2:60, 3:29-58, Johnson '424 at 1:6-2:34; Haskell at [0007]-[0008], [0027]; Averbuj at Abstract, [0004], [0011], [0081]; Rajamani at [0019], [0144]; Janzen '578 at [0002]-[0006], [0039]; Woo at 9:57-67; Ruckerbauer at 5:62-6:31, 6:39-48; McCall at 1:6-28, 3:47-53; LaBerge '345 at 7:34-40; Cornelius at 4:30-40, 8:62-9:3; Rogers at 2:49-52, 14:50-54, 15:49-58; Yoon at 1:8-25, 7:32-37; Wong at 1:8-2:10, 5:21-23; Jang at 1:8-50, 5:42-47; Synchronous DRAM Architectures, Organizations, and Alternative Technologies at 5-9, 20-22; Lee '287 at Abstract, 1:14-62, 6:11-36; Wong '868 at 1:57-2:10, 2:66-3:4; Barth at 1:7-3:49; Reeves at 1:7-2:67, 6:64-7:27; Halbert '098 at 2:5-49, 3:21-65; Matsui '782 at Abstract, 1:7-2:25; Vemula at 1:6-2:17; Janzen '666 at [0001], [0008], [0009]; Blockmon at [0001]-[0010], [0027]; Lee '864 at [0001], [0002], [0007], [0008], [0009]; James at [0001]-[0005], [0010], [0011]; Williams '446 at 1:6-3:10, 5:23-7:2; Wong '090 at 1:8-2:26; and *see also* exemplary citations in Appendix C.

Further, the prior art references provide motivations to combine because they explicitly suggest utilizing the teachings and disclosures of other references. In accordance with these advances, the prior art could have been combined according to methods known to those of ordinary skill within the field of the Asserted Patents to yield predictable results. The substitution of one element in a memory module could have been predictably achieved by one of ordinary skill at the time of the alleged invention. One of ordinary skill in the art would have been aware of these various applications, including, for example, memory density multiplication techniques and structures, data or signal buffering, memory devices' isolation from other components, and would have been able to select appropriate attributes of one for inclusion in another. Those of ordinary

skill in the art could have employed known techniques to improve similar prior art devices in the same way as claimed in the '417 patent.

In addition, one of ordinary skill in the art would be motivated to combine the prior art references because the elements found in the '417 patent Asserted Claims are well known in the art. Indeed, the named inventors of the '417 patent admitted as much in the specification of the '417 Patent. *See* '417 patent at 1:54-2:53, 2:65-3:6, 6:51-7:3, 7:32-39, 7:40-60, 9:46-10:4, 15:40-47, 15:63-16:30, 17:2-5, 20:4-43, 23:49-54, 26:3-6, 33:21-24, 33:48-51, 34:44-47, 40:38-40, 42:2-4.

Any reference or combination of references that anticipates or makes obvious an asserted independent claim also makes obvious any asserted claim dependent on that independent claim, as the element of each dependent '417 patent Asserted Claim was known by a person of ordinary skill at the time of the alleged invention, at least partially based on, but not limited by, the claim constructions implicit in Plaintiff's infringement contentions, and it would have been obvious to combine those known elements with the independent claims at least as a matter of common sense and routine innovation. Accordingly, Defendants contend that each Asserted Claim would have been obvious not only by the combinations described in these contentions, but also by any combination of references that renders obvious an Asserted Claim.

In addition to the specific examples of motivation provided above, Defendants reserve the right to rely on the disclosures of the references listed in Appendix C for additional motivation to combine. The above-identified examples of combinations are given merely to illustrate various motivations to combine and are not intended to provide an exhaustive list of every possible combination to which the motivation may apply. Defendants reserve the right to contend that the above-described motivations to combine apply to other combinations at the appropriate time, i.e.,

in expert reports regarding invalidity.

For at least the reasons described above, it would have been obvious to one of ordinary skill in the art to combine each prior art reference listed in Appendix C with any other reference or references listed in Appendix C along with the knowledge of one of ordinary skill in the art to arrive at the inventions claimed in the '417 patent. For example, and without limitation, the Asserted Claims of the '417 patent would have been obvious to one of ordinary skill in the art in view of the following combinations:

Patent No. or Title (Primary Inventor/Author)	In Combination with One or More of: (Patent No. or Title (Primary Inventor/Author))
The '417 Patent's Admitted Prior Art ("APA")	• U.S. Patent No. 7,103,742 ("Mailloux"); • U.S. Patent Application Publication No. 2006/0117152 ("Amidi"); • U.S. Patent No. 6,851,032 ("LaBerge '032") ; • U.S. Patent No. 7,363,422 ("Perego '422"); • U.S. Patent No. 7,024,518 ("Halbert '518"); • U.S. Patent Application Publication No. 2002/0112119 ("Halbert '119"); • DDR SDRAM RDIMM Design Specification JEDEC Standard 21-C (4.20.4) ("JEDEC Standard 21-C"); • U.S. Patent Application Publication No. 2001/0008006 ("Klein"); • FBDIMM Architecture & Protocol; • Kentron's Quad Band Memory System ("QBM"); • U.S. Patent No. 6,493,250 ("Halbert '250"); • DDR3 Functional Outlook; • U.S. Patent No. 6,154,821 ("Barth"); • U.S. Patent No. 6,226,755 ("Reeves"); • U.S. Patent No. 6,742,098 ("Halbert '098"); • U.S. Patent No. 6,940,782 ("Matsui '782"); • U.S. Patent No. 7,196,948 ("Vemula"); • U.S. Patent Application Publication No. 2002/0133666 ("Janzen '666"); • U.S. Patent Application Publication No. 2004/0103258 ("Blockmon"); • U.S. Patent Application Publication No.

	2004/0260864 (“Lee ’864”); • U.S. Patent Application Publication No. 2005/0044304 (“James”); • International Patent Application Publication No. WO 96/020446 (“Williams ’446”); • U.S. Patent Application Publication No. 2006/0117152 (“Amidi”); • U.S. Patent Application Publication No. 2003/0204688 (“Lee ’688”); • U.S. Patent No. 7,240,145 (“Holman”); • DDR SDRAM RDIMM Design Specification JEDEC Standard 21-C (4.20.4) (“JEDEC Standard 21-C”); • DDR2 SDRAM Specification JEDEC Standard JESD79-2A (“JESD79-2A”); • U.S. Patent No. 7,092,299 (“Kwak”); • U.S. Patent Application Publication No. 2002/0118578 (“Janzen ’578”); • Synchronous DRAM Architectures, Organizations, and Alternative Technologies (Bruce Jacob); • U.S. Patent No. 6,446,184 (“Dell ’184”); • U.S. Patent No. 7,149,841 (“LaBerge ’841”); • U.S. Patent No. 7,366,827 (“Lee ’827”); • U.S. Patent No. 7,043,617 (“Williams ’617”); • U.S. Patent No. 7,433,258 (“Rao”); • U.S. Pat. No. 5,581,498 (“Ludwig”); • U.S. Patent No. 5,926,827 (“Dell ’827”); • U.S. Patent Application Publication No. US 2006/0195631 (“Rajamani”); • U.S. Patent Application Publication No. 2005/0198449 (“Haskell”); • U.S. Patent Application Publication No. 2005/0257109 (“Averbuj”); • U.S. Patent No. 7,222,224 (“Woo”); • U.S. Patent No. 7,289,383 (“Cornelius”); • U.S. Patent No. 6,529,423 (“Yoon”); • U.S. Patent No. 7,206,896 (“Perego ’896”); • U.S. Patent No. 6,205,062 (“Kim ’062”); • U.S. Patent No. 7,212,424 (“Johnson ’424”); • Micron DDR SDRAM RDIMM, MT36VDDF12872 & MT36VDDF25672 Product; • International Patent Application Publication No. WO 01/037090 (“Wong ’090”); and/or
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	• The knowledge of a person of ordinary skill in the art.
U.S. Patent No. 7,103,742 (“Mailloux”)	• The ’417 Patent’s Admitted Prior Art (“APA”); • U.S. Patent Application Publication No. 2006/0117152 (“Amidi”); • U.S. Patent Application Publication No. 2001/0008006 (“Klein”); • U.S. Patent No. 6,851,032 (“LaBerge ’032”) ; • U.S. Patent No. 7,363,422 (“Perego ’422”); • U.S. Patent No. 7,024,518 (“Halbert ’518”); • U.S. Patent Application Publication No. 2002/0112119 (“Halbert ’119”); • U.S. Patent No. 6,493,250 (“Halbert ’250”); • DDR SDRAM RDIMM Design Specification JEDEC Standard 21-C (4.20.4) (“JEDEC Standard 21-C”); • U.S. Patent No. 6,742,098 (“Halbert ’098”); • U.S. Patent Application Publication No. 2004/0103258 (“Blockmon”); • International Patent Application Publication No. WO 96/020446 (“Williams ’446”); • Synchronous DRAM Architectures, Organizations, and Alternative Technologies (Bruce Jacob); • U.S. Patent No. 6,446,184 (“Dell ’184”); • U.S. Patent No. 6,205,062 (“Kim ’062”); • JEDEC Standards; • DDR2 SDRAM Specification JEDEC Standard JESD79-2A (“JESD79-2A”); • U.S. Patent Application Publication No. 2006/0277355 (“Ellsberry”); • U.S. Patent Application Publication No. 2004/0260864 (“Lee ’864”); • International Patent Application Publication No. WO 01/037090 (“Wong ’090”); • U.S. Patent No. 6,154,821 (“Barth”); • U.S. Patent No. 6,226,755 (“Reeves”); • U.S. Patent No. 6,940,782 (“Matsui ’782”); • U.S. Patent No. 7,196,948 (“Vemula”); • U.S. Patent Application Publication No. 2002/0133666 (“Janzen ’666”); • U.S. Patent Application Publication No. 2003/0204688 (“Lee ’688”); • U.S. Patent No. 7,240,145 (“Holman”); • U.S. Patent No. 7,092,299 (“Kwak”);

	• U.S. Patent Application Publication No. 2002/0118578 ("Janzen '578"); • U.S. Patent No. 7,149,841 ("LaBerge '841"); • U.S. Patent No. 7,366,827 ("Lee '827"); • U.S. Patent No. 7,043,617 ("Williams '617"); • U.S. Patent No. 7,433,258 ("Rao"); • U.S. Pat. No. 5,581,498 ("Ludwig"); • U.S. Patent No. 5,926,827 ("Dell '827"); • U.S. Patent Application Publication No. US 2006/0195631 ("Rajamani"); • U.S. Patent Application Publication No. 2005/0198449 ("Haskell"); • U.S. Patent Application Publication No. 2005/0257109 ("Averbuj"); • FBDIMM Architecture & Protocol; • U.S. Patent No. 7,155,627 ("Matsui '627"); • U.S. Patent No. 7,222,224 ("Woo"); • U.S. Patent No. 7,289,383 ("Cornelius"); • U.S. Patent No. 6,529,423 ("Yoon"); • U.S. Patent No. 7,206,896 ("Perego '896"); • U.S. Patent No. 7,212,424 ("Johnson '424"); • U.S. Patent No. 5,712,811 ("Kim '811"); • U.S. Patent No. 7,334,150 ("Ruckerbauer"); • Kentron's Quad Band Memory System ("QBM"); • Micron DDR SDRAM RDIMM, MT36VDDF12872 & MT36VDDF25672 Product; • DDR3 Functional Outlook; and/or • The knowledge of a person of ordinary skill in the art.
U.S. Patent Application Publication No. 2006/0117152 ("Amidi")	• The '417 Patent's Admitted Prior Art ("APA"); • U.S. Patent No. 7,103,742 ("Mailloux"); • U.S. Patent No. 6,851,032 ("LaBerge '032"); • U.S. Patent No. 7,363,422 ("Perego '422"); • U.S. Patent No. 7,024,518 ("Halbert '518"); • U.S. Patent No. 6,493,250 ("Halbert '250"); • U.S. Patent Application Publication No. 2002/0112119 ("Halbert '119"); • DDR SDRAM RDIMM Design Specification JEDEC Standard 21-C (4.20.4) ("JEDEC Standard 21-C"); • DDR2 SDRAM Specification JEDEC Standard JESD79-2A ("JESD79-2A");

	• U.S. Patent No. 6,742,098 (“Halbert ’098”); • U.S. Patent Application Publication No. 2004/0103258 (“Blockmon”); • International Patent Application Publication No. WO 96/020446 (“Williams ’446”); • Synchronous DRAM Architectures, Organizations, and Alternative Technologies (Bruce Jacob); • U.S. Patent No. 6,446,184 (“Dell ’184”); • U.S. Patent No. 6,205,062 (“Kim ’062”); • JEDEC Standards; • U.S. Patent Application Publication No. 2006/0277355 (“Ellsberry”); • U.S. Patent Application Publication No. 2004/0260864 (“Lee ’864”); • International Patent Application Publication No. WO 01/037090 (“Wong ’090”); • U.S. Patent No. 6,154,821 (“Barth”); • U.S. Patent No. 6,226,755 (“Reeves”); • U.S. Patent No. 6,940,782 (“Matsui ’782”); • U.S. Patent No. 7,196,948 (“Vemula”); • U.S. Patent Application Publication No. 2002/0133666 (“Janzen ’666”); • U.S. Patent Application Publication No. 2003/0204688 (“Lee ’688”); • U.S. Patent No. 7,240,145 (“Holman”); • U.S. Patent No. 7,092,299 (“Kwak”); • U.S. Patent Application Publication No. 2002/0118578 (“Janzen ’578”); • U.S. Patent No. 7,149,841 (“LaBerge ’841”); • U.S. Patent No. 7,366,827 (“Lee ’827”); • U.S. Patent No. 7,043,617 (“Williams ’617”); • U.S. Patent No. 7,433,258 (“Rao”); • U.S. Pat. No. 5,581,498 (“Ludwig”); • U.S. Patent No. 5,926,827 (“Dell ’827”); • U.S. Patent Application Publication No. US 2006/0195631 (“Rajamani”); • U.S. Patent Application Publication No. 2005/0198449 (“Haskell”); • U.S. Patent Application Publication No. 2001/0008006 (“Klein”); • FBDIMM Architecture & Protocol; • U.S. Patent Application Publication No. 2005/0257109 (“Averbuj”);
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	• U.S. Patent No. 7,222,224 (“Woo”); • U.S. Patent No. 7,289,383 (“Cornelius”); • U.S. Patent No. 6,529,423 (“Yoon”); • U.S. Patent No. 7,206,896 (“Perego ’896”); • U.S. Patent No. 7,212,424 (“Johnson ’424”); • U.S. Patent No. 5,712,811 (“Kim ’811”); • U.S. Patent No. 7,334,150 (“Ruckerbauer”); • Kentron’s Quad Band Memory System (“QBM”); • Micron DDR SDRAM RDIMM, MT36VDDF12872 & MT36VDDF25672 Product; • DDR3 Functional Outlook; and/or • The knowledge of a person of ordinary skill in the art of a person of ordinary skill in the art.
U.S. Patent No. 6,851,032 (“LaBerge ’032”)	• The ’417 Patent’s Admitted Prior Art (“APA”); • U.S. Patent No. 7,103,742 (“Mailloux”); • U.S. Patent Application Publication No. 2006/0117152 (“Amidi”); • U.S. Patent No. 7,363,422 (“Perego ’422”); • U.S. Patent No. 7,024,518 (“Halbert ’518”); • U.S. Patent Application Publication No. 2002/0112119 (“Halbert ’119”); • DDR SDRAM RDIMM Design Specification JEDEC Standard 21-C (4.20.4) (“JEDEC Standard 21-C”); • DDR2 SDRAM Specification JEDEC Standard JESD79-2A (“JESD79-2A”); • U.S. Patent No. 6,742,098 (“Halbert ’098”); • U.S. Patent Application Publication No. 2004/0103258 (“Blockmon”); • International Patent Application Publication No. WO 96/020446 (“Williams ’446”); • Synchronous DRAM Architectures, Organizations, and Alternative Technologies (Bruce Jacob); • U.S. Patent No. 6,446,184 (“Dell ’184”); • U.S. Patent No. 6,205,062 (“Kim ’062”); • JEDEC Standards; • U.S. Patent Application Publication No. 2006/0277355 (“Ellsberry”); • U.S. Patent Application Publication No. 2004/0260864 (“Lee ’864”); • International Patent Application Publication No.

	WO 01/037090 (“Wong ’090”); • U.S. Patent No. 6,154,821 (“Barth”); • U.S. Patent No. 6,226,755 (“Reeves”); • U.S. Patent No. 6,940,782 (“Matsui ’782”); • U.S. Patent No. 7,196,948 (“Vemula”); • U.S. Patent Application Publication No. 2002/0133666 (“Janzen ’666”); • U.S. Patent Application Publication No. 2001/0008006 (“Klein”); • U.S. Patent Application Publication No. 2003/0204688 (“Lee ’688”); • U.S. Patent No. 7,240,145 (“Holman”); • U.S. Patent No. 7,092,299 (“Kwak”); • U.S. Patent Application Publication No. 2002/0118578 (“Janzen ’578”); • U.S. Patent No. 7,149,841 (“LaBerge ’841”); • U.S. Patent No. 7,366,827 (“Lee ’827”); • U.S. Patent No. 7,043,617 (“Williams ’617”); • U.S. Patent No. 7,433,258 (“Rao”); • U.S. Pat. No. 5,581,498 (“Ludwig”); • U.S. Patent No. 5,926,827 (“Dell ’827”); • U.S. Patent Application Publication No. US 2006/0195631 (“Rajamani”); • FBDIMM Architecture & Protocol; • U.S. Patent Application Publication No. 2005/0198449 (“Haskell”); • U.S. Patent No. 6,493,250 (“Halbert ’250”); • U.S. Patent Application Publication No. 2005/0257109 (“Averbuj”); • U.S. Patent No. 7,155,627 (“Matsui ’627”); • U.S. Patent No. 7,222,224 (“Woo”); • U.S. Patent No. 7,289,383 (“Cornelius”); • U.S. Patent No. 6,529,423 (“Yoon”); • U.S. Patent No. 7,206,896 (“Perego ’896”); • U.S. Patent No. 7,212,424 (“Johnson ’424”); • U.S. Patent No. 5,712,811 (“Kim ’811”); • U.S. Patent No. 7,334,150 (“Ruckerbauer”); • Kentron’s Quad Band Memory System (“QBM”); • Micron DDR SDRAM RDIMM, MT36VDDF12872 & MT36VDDF25672 Product; • DDR3 Functional Outlook; and/or • The knowledge of a person of ordinary skill in
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	the art.
U.S. Patent No. 7,363,422 (“Perego ’422”)	• The ’417 Patent’s Admitted Prior Art (“APA”); • U.S. Patent No. 7,103,742 (“Mailloux”); • U.S. Patent Application Publication No. 2006/0117152 (“Amidi”); • DDR2 SDRAM Specification JEDEC Standard JESD79-2A (“JESD79-2A”); • U.S. Patent No. 6,851,032 (“LaBerge ’032”) ; • U.S. Patent No. 7,024,518 (“Halbert ’518”); • U.S. Patent Application Publication No. 2002/0112119 (“Halbert ’119”); • DDR SDRAM RDIMM Design Specification JEDEC Standard 21-C (4.20.4) (“JEDEC Standard 21-C”); • U.S. Patent No. 6,742,098 (“Halbert ’098”); • U.S. Patent Application Publication No. 2004/0103258 (“Blockmon”); • International Patent Application Publication No. WO 96/020446 (“Williams ’446”); • Synchronous DRAM Architectures, Organizations, and Alternative Technologies (Bruce Jacob); • U.S. Patent No. 6,446,184 (“Dell ’184”); • U.S. Patent No. 6,205,062 (“Kim ’062”); • JEDEC Standards; • U.S. Patent No. 6,493,250 (“Halbert ’250”); • U.S. Patent Application Publication No. 2006/0277355 (“Ellsberry”); • U.S. Patent Application Publication No. 2004/0260864 (“Lee ’864”); • International Patent Application Publication No. WO 01/037090 (“Wong ’090”); • U.S. Patent No. 6,154,821 (“Barth”); • U.S. Patent No. 6,226,755 (“Reeves”); • U.S. Patent No. 6,940,782 (“Matsui ’782”); • U.S. Patent No. 7,196,948 (“Vemula”); • U.S. Patent Application Publication No. 2002/0133666 (“Janzen ’666”); • U.S. Patent Application Publication No. 2001/0008006 (“Klein”); • U.S. Patent Application Publication No. 2003/0204688 (“Lee ’688”); • U.S. Patent No. 7,240,145 (“Holman”); • U.S. Patent No. 7,092,299 (“Kwak”); • U.S. Patent Application Publication No.

	2002/0118578 ("Janzen '578"); • U.S. Patent No. 7,149,841 ("LaBerge '841"); • U.S. Patent No. 7,366,827 ("Lee '827"); • U.S. Patent No. 7,043,617 ("Williams '617"); • U.S. Patent No. 7,433,258 ("Rao"); • U.S. Pat. No. 5,581,498 ("Ludwig"); • U.S. Patent No. 5,926,827 ("Dell '827"); • U.S. Patent Application Publication No. US 2006/0195631 ("Rajamani"); • U.S. Patent Application Publication No. 2005/0198449 ("Haskell"); • FBDIMM Architecture & Protocol; • U.S. Patent Application Publication No. 2005/0257109 ("Averbuj"); • U.S. Patent No. 7,222,224 ("Woo"); • U.S. Patent No. 7,289,383 ("Cornelius"); • U.S. Patent No. 6,529,423 ("Yoon"); • U.S. Patent No. 7,206,896 ("Perego '896"); • U.S. Patent No. 7,212,424 ("Johnson '424"); • U.S. Patent No. 5,712,811 ("Kim '811"); • U.S. Patent No. 7,334,150 ("Ruckerbauer"); • Kentron's Quad Band Memory System ("QBM"); • Micron DDR SDRAM RDIMM, MT36VDDF12872 & MT36VDDF25672 Product; • DDR3 Functional Outlook; and/or • The knowledge of a person of ordinary skill in the art.
U.S. Patent No. 7,024,518 ("Halbert '518")	• The '417 Patent's Admitted Prior Art ("APA"); • U.S. Patent No. 7,103,742 ("Mailloux"); • U.S. Patent Application Publication No. 2006/0117152 ("Amidi"); • U.S. Patent No. 6,851,032 ("LaBerge '032") ; • U.S. Patent No. 7,363,422 ("Perego '422"); • U.S. Patent Application Publication No. 2002/0112119 ("Halbert '119"); • DDR SDRAM RDIMM Design Specification JEDEC Standard 21-C (4.20.4) ("JEDEC Standard 21-C"); • DDR2 SDRAM Specification JEDEC Standard JESD79-2A ("JESD79-2A"); • U.S. Patent Application Publication No. 2001/0008006 ("Klein");

	• U.S. Patent No. 6,742,098 (“Halbert ’098”); • U.S. Patent Application Publication No. 2004/0103258 (“Blockmon”); • International Patent Application Publication No. WO 96/020446 (“Williams ’446”); • Synchronous DRAM Architectures, Organizations, and Alternative Technologies (Bruce Jacob); • U.S. Patent No. 6,446,184 (“Dell ’184”); • U.S. Patent No. 6,205,062 (“Kim ’062”); • JEDEC Standards; • U.S. Patent Application Publication No. 2006/0277355 (“Ellsberry”); • U.S. Patent Application Publication No. 2004/0260864 (“Lee ’864”); • International Patent Application Publication No. WO 01/037090 (“Wong ’090”); • FBDIMM Architecture & Protocol; • U.S. Patent No. 6,154,821 (“Barth”); • U.S. Patent No. 6,226,755 (“Reeves”); • U.S. Patent No. 6,940,782 (“Matsui ’782”); • U.S. Patent No. 7,196,948 (“Vemula”); • U.S. Patent Application Publication No. 2002/0133666 (“Janzen ’666”); • U.S. Patent Application Publication No. 2003/0204688 (“Lee ’688”); • U.S. Patent No. 7,240,145 (“Holman”); • U.S. Patent No. 7,092,299 (“Kwak”); • U.S. Patent Application Publication No. 2002/0118578 (“Janzen ’578”); • U.S. Patent No. 7,149,841 (“LaBerge ’841”); • U.S. Patent No. 7,366,827 (“Lee ’827”); • U.S. Patent No. 7,043,617 (“Williams ’617”); • U.S. Patent No. 7,433,258 (“Rao”); • U.S. Pat. No. 5,581,498 (“Ludwig”); • U.S. Patent No. 5,926,827 (“Dell ’827”); • U.S. Patent Application Publication No. US 2006/0195631 (“Rajamani”); • U.S. Patent Application Publication No. 2005/0198449 (“Haskell”); • U.S. Patent Application Publication No. 2005/0257109 (“Averbuj”); • U.S. Patent No. 6,493,250 (“Halbert ’250”); • U.S. Patent No. 7,222,224 (“Woo”);
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	• U.S. Patent No. 7,289,383 (“Cornelius”); • U.S. Patent No. 6,529,423 (“Yoon”); • U.S. Patent No. 7,206,896 (“Perego ’896”); • U.S. Patent No. 7,212,424 (“Johnson ’424”); • U.S. Patent No. 5,712,811 (“Kim ’811”); • U.S. Patent No. 7,334,150 (“Ruckerbauer”); • Kentron’s Quad Band Memory System (“QBM”); • Micron DDR SDRAM RDIMM, MT36VDDF12872 & MT36VDDF25672 Product; • DDR3 Functional Outlook; and/or • The knowledge of a person of ordinary skill in the art.
U.S. Patent Application Publication No. 2006/0277355 (“Ellsberry”)	• The ’417 Patent’s Admitted Prior Art (“APA”); • U.S. Patent No. 7,103,742 (“Mailloux”); • U.S. Patent Application Publication No. 2006/0117152 (“Amidi”); • U.S. Patent Application Publication No. 2001/0008006 (“Klein”); • U.S. Patent No. 6,493,250 (“Halbert ’250”); • U.S. Patent No. 6,851,032 (“LaBerge ’032”); • U.S. Patent No. 7,363,422 (“Perego ’422”); • U.S. Patent No. 7,024,518 (“Halbert ’518”); • DDR SDRAM RDIMM Design Specification JEDEC Standard 21-C (4.20.4) (“JEDEC Standard 21-C”); • DDR2 SDRAM Specification JEDEC Standard JESD79-2A (“JESD79-2A”); • U.S. Patent No. 6,742,098 (“Halbert ’098”); • U.S. Patent Application Publication No. 2004/0103258 (“Blockmon”); • International Patent Application Publication No. WO 96/020446 (“Williams ’446”); • Synchronous DRAM Architectures, Organizations, and Alternative Technologies (Bruce Jacob); • U.S. Patent No. 6,446,184 (“Dell ’184”); • U.S. Patent No. 6,205,062 (“Kim ’062”); • JEDEC Standards; • FBDIMM Architecture & Protocol; • U.S. Patent Application Publication No. 2004/0260864 (“Lee ’864”); • International Patent Application Publication No.

	WO 01/037090 (“Wong ’090”); • U.S. Patent No. 6,154,821 (“Barth”); • U.S. Patent No. 6,226,755 (“Reeves”); • U.S. Patent No. 6,940,782 (“Matsui ’782”); • U.S. Patent No. 7,196,948 (“Vemula”); • U.S. Patent Application Publication No. 2002/0133666 (“Janzen ’666”); • U.S. Patent Application Publication No. 2003/0204688 (“Lee ’688”); • U.S. Patent No. 7,240,145 (“Holman”); • U.S. Patent No. 7,092,299 (“Kwak”); • U.S. Patent Application Publication No. 2002/0118578 (“Janzen ’578”); • U.S. Patent No. 7,149,841 (“LaBerge ’841”); • U.S. Patent No. 7,366,827 (“Lee ’827”); • U.S. Patent No. 7,043,617 (“Williams ’617”); • U.S. Patent No. 7,433,258 (“Rao”); • U.S. Pat. No. 5,581,498 (“Ludwig”); • U.S. Patent No. 5,926,827 (“Dell ’827”); • U.S. Patent Application Publication No. US 2006/0195631 (“Rajamani”); • U.S. Patent Application Publication No. 2005/0198449 (“Haskell”); • U.S. Patent Application Publication No. 2005/0257109 (“Averbuj”); • FBDIMM Architecture & Protocol; • U.S. Patent No. 7,222,224 (“Woo”); • U.S. Patent No. 7,289,383 (“Cornelius”); • U.S. Patent No. 6,529,423 (“Yoon”); • U.S. Patent No. 7,206,896 (“Perego ’896”); • U.S. Patent No. 7,212,424 (“Johnson ’424”); • U.S. Patent No. 5,712,811 (“Kim ’811”); • U.S. Patent No. 7,334,150 (“Ruckerbauer”); • Kentron’s Quad Band Memory System (“QBM”); • Micron DDR SDRAM RDIMM, MT36VDDF12872 & MT36VDDF25672 Product; • DDR3 Functional Outlook; and/or • The knowledge of a person of ordinary skill in the art.
U.S. Patent No. 6,493,250 (“Halbert ’250”)	• The ’417 Patent’s Admitted Prior Art (“APA”); • U.S. Patent No. 7,103,742 (“Mailloux”); • U.S. Patent Application Publication No.

	2006/0117152 (“Amidi”); • U.S. Patent No. 6,851,032 (“LaBerge ’032”) ; • U.S. Patent No. 7,363,422 (“Perego ’422”); • U.S. Patent No. 7,024,518 (“Halbert ’518”); • DDR SDRAM RDIMM Design Specification JEDEC Standard 21-C (4.20.4) (“JEDEC Standard 21-C”); • DDR2 SDRAM Specification JEDEC Standard JESD79-2A (“JESD79-2A”); • U.S. Patent No. 6,742,098 (“Halbert ’098”); • U.S. Patent Application Publication No. 2004/0103258 (“Blockmon”); • International Patent Application Publication No. WO 96/020446 (“Williams ’446”); • Synchronous DRAM Architectures, Organizations, and Alternative Technologies (Bruce Jacob); • U.S. Patent No. 6,446,184 (“Dell ’184”); • U.S. Patent No. 6,205,062 (“Kim ’062”); • JEDEC Standards; • FBDIMM Architecture & Protocol; • U.S. Patent Application Publication No. 2004/0260864 (“Lee ’864”); • International Patent Application Publication No. WO 01/037090 (“Wong ’090”); • U.S. Patent No. 6,154,821 (“Barth”); • U.S. Patent No. 6,226,755 (“Reeves”); • U.S. Patent No. 6,940,782 (“Matsui ’782”); • U.S. Patent No. 7,196,948 (“Vemula”); • U.S. Patent Application Publication No. 2002/0133666 (“Janzen ’666”); • U.S. Patent Application Publication No. 2003/0204688 (“Lee ’688”); • U.S. Patent No. 7,240,145 (“Holman”); • U.S. Patent No. 7,092,299 (“Kwak”); • U.S. Patent Application Publication No. 2002/0118578 (“Janzen ’578”); • U.S. Patent No. 7,149,841 (“LaBerge ’841”); • U.S. Patent No. 7,366,827 (“Lee ’827”); • U.S. Patent No. 7,043,617 (“Williams ’617”); • U.S. Patent No. 7,433,258 (“Rao”); • U.S. Pat. No. 5,581,498 (“Ludwig”); • U.S. Patent No. 5,926,827 (“Dell ’827”); • U.S. Patent Application Publication No. US
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	2006/0195631 (“Rajamani”); • U.S. Patent Application Publication No. 2005/0198449 (“Haskell”); • U.S. Patent Application Publication No. 2005/0257109 (“Averbuj”); • FBDIMM Architecture & Protocol; • U.S. Patent No. 7,222,224 (“Woo”); • U.S. Patent Application Publication No. 2001/0008006 (“Klein”); • U.S. Patent No. 7,289,383 (“Cornelius”); • U.S. Patent No. 6,529,423 (“Yoon”); • U.S. Patent No. 7,206,896 (“Perego ’896”); • U.S. Patent No. 7,212,424 (“Johnson ’424”); • U.S. Patent No. 5,712,811 (“Kim ’811”); • U.S. Patent No. 7,334,150 (“Ruckerbauer”); • Kentron’s Quad Band Memory System (“QBM”); • Micron DDR SDRAM RDIMM, MT36VDDF12872 & MT36VDDF25672 Product; • DDR3 Functional Outlook; and/or • The knowledge of a person of ordinary skill in the art.
U.S. Patent Application Publication No. 2001/0008006 (“Klein”)	• The ’417 Patent’s Admitted Prior Art (“APA”); • U.S. Patent No. 7,103,742 (“Mailloux”); • U.S. Patent Application Publication No. 2006/0117152 (“Amidi”); • U.S. Patent No. 6,493,250 (“Halbert ’250”); • U.S. Patent No. 6,851,032 (“LaBerge ’032”) ; • U.S. Patent No. 7,363,422 (“Perego ’422”); • U.S. Patent No. 7,024,518 (“Halbert ’518”); • DDR SDRAM RDIMM Design Specification JEDEC Standard 21-C (4.20.4) (“JEDEC Standard 21-C”); • DDR2 SDRAM Specification JEDEC Standard JESD79-2A (“JESD79-2A”); • U.S. Patent No. 6,742,098 (“Halbert ’098”); • U.S. Patent Application Publication No. 2004/0103258 (“Blockmon”); • International Patent Application Publication No. WO 96/020446 (“Williams ’446”); • Synchronous DRAM Architectures, Organizations, and Alternative Technologies (Bruce Jacob);

	• U.S. Patent No. 6,446,184 (“Dell ’184”); • U.S. Patent No. 6,205,062 (“Kim ’062”); • JEDEC Standards; • FBDIMM Architecture & Protocol; • U.S. Patent Application Publication No. 2004/0260864 (“Lee ’864”); • International Patent Application Publication No. WO 01/037090 (“Wong ’090”); • U.S. Patent No. 6,154,821 (“Barth”); • U.S. Patent No. 6,226,755 (“Reeves”); • U.S. Patent No. 6,940,782 (“Matsui ’782”); • U.S. Patent No. 7,196,948 (“Vemula”); • U.S. Patent Application Publication No. 2002/0133666 (“Janzen ’666”); • U.S. Patent Application Publication No. 2003/0204688 (“Lee ’688”); • U.S. Patent No. 7,240,145 (“Holman”); • U.S. Patent No. 7,092,299 (“Kwak”); • U.S. Patent Application Publication No. 2002/0118578 (“Janzen ’578”); • U.S. Patent No. 7,149,841 (“LaBerge ’841”); • U.S. Patent No. 7,366,827 (“Lee ’827”); • U.S. Patent No. 7,043,617 (“Williams ’617”); • U.S. Patent No. 7,433,258 (“Rao”); • U.S. Pat. No. 5,581,498 (“Ludwig”); • U.S. Patent No. 5,926,827 (“Dell ’827”); • U.S. Patent Application Publication No. US 2006/0195631 (“Rajamani”); • U.S. Patent Application Publication No. 2005/0198449 (“Haskell”); • U.S. Patent Application Publication No. 2005/0257109 (“Averbuj”); • FBDIMM Architecture & Protocol; • U.S. Patent No. 7,222,224 (“Woo”); • U.S. Patent No. 7,289,383 (“Cornelius”); • U.S. Patent No. 6,529,423 (“Yoon”); • U.S. Patent No. 7,206,896 (“Perego ’896”); • U.S. Patent No. 7,212,424 (“Johnson ’424”); • U.S. Patent No. 5,712,811 (“Kim ’811”); • U.S. Patent No. 7,334,150 (“Ruckerbauer”); • Kentron’s Quad Band Memory System (“QBM”);
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	• Micron DDR SDRAM RDIMM, MT36VDDF12872 & MT36VDDF25672 Product; • DDR3 Functional Outlook; and/or • The knowledge of a person of ordinary skill in the art.
JEDEC Standards	• The '417 Patent's Admitted Prior Art ("APA"); • U.S. Patent No. 7,103,742 ("Mailloux"); • U.S. Patent Application Publication No. 2006/0117152 ("Amidi"); • U.S. Patent No. 6,493,250 ("Halbert '250"); • U.S. Patent No. 6,851,032 ("LaBerge '032") ; • U.S. Patent Application Publication No. 2001/0008006 ("Klein"); • U.S. Patent No. 7,363,422 ("Perego '422"); • U.S. Patent No. 7,024,518 ("Halbert '518"); • DDR SDRAM RDIMM Design Specification JEDEC Standard 21-C (4.20.4) ("JEDEC Standard 21-C"); • DDR2 SDRAM Specification JEDEC Standard JESD79-2A ("JESD79-2A"); • U.S. Patent No. 6,742,098 ("Halbert '098"); • U.S. Patent Application Publication No. 2004/0103258 ("Blockmon"); • International Patent Application Publication No. WO 96/020446 ("Williams '446"); • Synchronous DRAM Architectures, Organizations, and Alternative Technologies (Bruce Jacob); • U.S. Patent No. 6,446,184 ("Dell '184"); • U.S. Patent No. 6,205,062 ("Kim '062"); • FBDIMM Architecture & Protocol; • U.S. Patent Application Publication No. 2006/0277355 ("Ellsberry"); • U.S. Patent Application Publication No. 2004/0260864 ("Lee '864"); • International Patent Application Publication No. WO 01/037090 ("Wong '090"); • U.S. Patent No. 6,154,821 ("Barth"); • U.S. Patent No. 6,226,755 ("Reeves"); • U.S. Patent No. 6,940,782 ("Matsui '782"); • U.S. Patent No. 7,196,948 ("Vemula"); • U.S. Patent Application Publication No. 2002/0133666 ("Janzen '666");

	• U.S. Patent Application Publication No. 2003/0204688 (“Lee ’688”); • U.S. Patent No. 7,240,145 (“Holman”); • U.S. Patent No. 7,092,299 (“Kwak”); • U.S. Patent Application Publication No. 2002/0118578 (“Janzen ’578”); • U.S. Patent No. 7,149,841 (“LaBerge ’841”); • U.S. Patent No. 7,366,827 (“Lee ’827”); • U.S. Patent No. 7,043,617 (“Williams ’617”); • U.S. Patent No. 7,433,258 (“Rao”); • U.S. Pat. No. 5,581,498 (“Ludwig”); • U.S. Patent No. 5,926,827 (“Dell ’827”); • U.S. Patent Application Publication No. US 2006/0195631 (“Rajamani”); • U.S. Patent Application Publication No. 2005/0198449 (“Haskell”); • U.S. Patent Application Publication No. 2005/0257109 (“Averbuj”); • FBDIMM Architecture & Protocol; • U.S. Patent No. 7,222,224 (“Woo”); • U.S. Patent No. 7,289,383 (“Cornelius”); • U.S. Patent No. 6,529,423 (“Yoon”); • U.S. Patent No. 7,206,896 (“Perego ’896”); • U.S. Patent No. 7,212,424 (“Johnson ’424”); • U.S. Patent No. 5,712,811 (“Kim ’811”); • U.S. Patent No. 7,334,150 (“Ruckerbauer”); • Kentron’s Quad Band Memory System (“QBM”); • Micron DDR SDRAM RDIMM, MT36VDDF12872 & MT36VDDF25672 Product; • DDR3 Functional Outlook; and/or • The knowledge of a person of ordinary skill in the art.
DDR2 SDRAM Specification JEDEC Standard JESD79-2A (“JESD79-2A”)	• The ’417 Patent’s Admitted Prior Art (“APA”); • U.S. Patent No. 7,103,742 (“Mailloux”); • U.S. Patent Application Publication No. 2006/0117152 (“Amidi”); • U.S. Patent No. 6,493,250 (“Halbert ’250”); • U.S. Patent No. 6,851,032 (“LaBerge ’032”) ; • U.S. Patent Application Publication No. 2001/0008006 (“Klein”); • U.S. Patent No. 7,363,422 (“Perego ’422”); • U.S. Patent No. 7,024,518 (“Halbert ’518”);

	• DDR SDRAM RDIMM Design Specification JEDEC Standard 21-C (4.20.4) (“JEDEC Standard 21-C”); • U.S. Patent No. 6,742,098 (“Halbert ’098”); • U.S. Patent Application Publication No. 2004/0103258 (“Blockmon”); • International Patent Application Publication No. WO 96/020446 (“Williams ’446”); • Synchronous DRAM Architectures, Organizations, and Alternative Technologies (Bruce Jacob); • U.S. Patent No. 6,446,184 (“Dell ’184”); • U.S. Patent No. 6,205,062 (“Kim ’062”); • FBDIMM Architecture & Protocol; • U.S. Patent Application Publication No. 2006/0277355 (“Ellsberry”); • U.S. Patent Application Publication No. 2004/0260864 (“Lee ’864”); • International Patent Application Publication No. WO 01/037090 (“Wong ’090”); • U.S. Patent No. 6,154,821 (“Barth”); • U.S. Patent No. 6,226,755 (“Reeves”); • U.S. Patent No. 6,940,782 (“Matsui ’782”); • U.S. Patent No. 7,196,948 (“Vemula”); • U.S. Patent Application Publication No. 2002/0133666 (“Janzen ’666”); • U.S. Patent Application Publication No. 2003/0204688 (“Lee ’688”); • U.S. Patent No. 7,240,145 (“Holman”); • U.S. Patent No. 7,092,299 (“Kwak”); • U.S. Patent Application Publication No. 2002/0118578 (“Janzen ’578”); • U.S. Patent No. 7,149,841 (“LaBerge ’841”); • U.S. Patent No. 7,366,827 (“Lee ’827”); • U.S. Patent No. 7,043,617 (“Williams ’617”); • U.S. Patent No. 7,433,258 (“Rao”); • U.S. Pat. No. 5,581,498 (“Ludwig”); • U.S. Patent No. 5,926,827 (“Dell ’827”); • U.S. Patent Application Publication No. US 2006/0195631 (“Rajamani”); • U.S. Patent Application Publication No. 2005/0198449 (“Haskell”); • U.S. Patent Application Publication No. 2005/0257109 (“Averbuj”); • FBDIMM Architecture & Protocol;
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	• U.S. Patent No. 7,222,224 (“Woo”); • U.S. Patent No. 7,289,383 (“Cornelius”); • U.S. Patent No. 6,529,423 (“Yoon”); • U.S. Patent No. 7,206,896 (“Perego ’896”); • U.S. Patent No. 7,212,424 (“Johnson ’424”); • U.S. Patent No. 5,712,811 (“Kim ’811”); • U.S. Patent No. 7,334,150 (“Ruckerbauer”); • Kentron’s Quad Band Memory System (“QBM”); • Micron DDR SDRAM RDIMM, MT36VDDF12872 & MT36VDDF25672 Product; • DDR3 Functional Outlook; and/or • The knowledge of a person of ordinary skill in the art.
U.S. Patent Application Publication No. 2002/0112119 (“Halbert ’119”)	• The ’417 Patent’s Admitted Prior Art (“APA”); • U.S. Patent No. 7,103,742 (“Mailloux”); • U.S. Patent Application Publication No. 2006/0117152 (“Amidi”); • DDR2 SDRAM Specification JEDEC Standard JESD79-2A (“JESD79-2A”); • U.S. Patent No. 6,493,250 (“Halbert ’250”); • U.S. Patent No. 6,851,032 (“LaBerge ’032”) ; • U.S. Patent Application Publication No. 2001/0008006 (“Klein”); • U.S. Patent No. 7,363,422 (“Perego ’422”); • U.S. Patent No. 7,024,518 (“Halbert ’518”); • DDR SDRAM RDIMM Design Specification JEDEC Standard 21-C (4.20.4) (“JEDEC Standard 21-C”); • DDR2 SDRAM Specification JEDEC Standard JESD79-2A (“JESD79-2A”); • U.S. Patent No. 6,742,098 (“Halbert ’098”); • U.S. Patent Application Publication No. 2004/0103258 (“Blockmon”); • International Patent Application Publication No. WO 96/020446 (“Williams ’446”); • Synchronous DRAM Architectures, Organizations, and Alternative Technologies (Bruce Jacob); • U.S. Patent No. 6,446,184 (“Dell ’184”); • U.S. Patent No. 6,205,062 (“Kim ’062”); • JEDEC Standards; • FBDIMM Architecture & Protocol;

	• U.S. Patent Application Publication No. 2006/0277355 (“Ellsberry”); • U.S. Patent Application Publication No. 2004/0260864 (“Lee ’864”); • International Patent Application Publication No. WO 01/037090 (“Wong ’090”); • U.S. Patent No. 6,154,821 (“Barth”); • U.S. Patent No. 6,226,755 (“Reeves”); • U.S. Patent No. 6,940,782 (“Matsui ’782”); • U.S. Patent No. 7,196,948 (“Vemula”); • U.S. Patent Application Publication No. 2002/0133666 (“Janzen ’666”); • U.S. Patent Application Publication No. 2003/0204688 (“Lee ’688”); • U.S. Patent No. 7,240,145 (“Holman”); • U.S. Patent No. 7,092,299 (“Kwak”); • U.S. Patent Application Publication No. 2002/0118578 (“Janzen ’578”); • U.S. Patent No. 7,149,841 (“LaBerge ’841”); • U.S. Patent No. 7,366,827 (“Lee ’827”); • U.S. Patent No. 7,043,617 (“Williams ’617”); • U.S. Patent No. 7,433,258 (“Rao”); • U.S. Pat. No. 5,581,498 (“Ludwig”); • U.S. Patent No. 5,926,827 (“Dell ’827”); • U.S. Patent Application Publication No. US 2006/0195631 (“Rajamani”); • U.S. Patent Application Publication No. 2005/0198449 (“Haskell”); • U.S. Patent Application Publication No. 2005/0257109 (“Averbuj”); • FBDIMM Architecture & Protocol; • U.S. Patent No. 7,222,224 (“Woo”); • U.S. Patent No. 7,289,383 (“Cornelius”); • U.S. Patent No. 6,529,423 (“Yoon”); • U.S. Patent No. 7,206,896 (“Perego ’896”); • U.S. Patent No. 7,212,424 (“Johnson ’424”); • U.S. Patent No. 5,712,811 (“Kim ’811”); • U.S. Patent No. 7,334,150 (“Ruckerbauer”); • Kentron’s Quad Band Memory System (“QBM”); • Micron DDR SDRAM RDIMM, MT36VDDF12872 & MT36VDDF25672 Product; • DDR3 Functional Outlook; and/or
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	2002/0118578 ("Janzen '578"); • U.S. Patent No. 7,149,841 ("LaBerge '841"); • U.S. Patent No. 7,366,827 ("Lee '827"); • U.S. Patent No. 7,043,617 ("Williams '617"); • U.S. Patent No. 7,433,258 ("Rao"); • U.S. Pat. No. 5,581,498 ("Ludwig"); • U.S. Patent No. 5,926,827 ("Dell '827"); • U.S. Patent Application Publication No. US 2006/0195631 ("Rajamani"); • U.S. Patent Application Publication No. 2005/0198449 ("Haskell"); • U.S. Patent Application Publication No. 2005/0257109 ("Averbuj"); • FBDIMM Architecture & Protocol; • U.S. Patent No. 7,222,224 ("Woo"); • U.S. Patent No. 7,289,383 ("Cornelius"); • U.S. Patent No. 6,529,423 ("Yoon"); • U.S. Patent No. 7,206,896 ("Perego '896"); • U.S. Patent No. 7,212,424 ("Johnson '424"); • U.S. Patent No. 5,712,811 ("Kim '811"); • U.S. Patent No. 7,334,150 ("Ruckerbauer"); • Kentron's Quad Band Memory System ("QBM"); • Micron DDR SDRAM RDIMM, MT36VDDF12872 & MT36VDDF25672 Product; • DDR3 Functional Outlook; and/or • The knowledge of a person of ordinary skill in the art.
Kentron's Quad Band Memory System ("QBM")	• The '417 Patent's Admitted Prior Art ("APA"); • U.S. Patent No. 7,103,742 ("Mailloux"); • U.S. Patent Application Publication No. 2006/0117152 ("Amidi"); • DDR2 SDRAM Specification JEDEC Standard JESD79-2A ("JESD79-2A"); • U.S. Patent Application Publication No. 2001/0008006 ("Klein"); • U.S. Patent No. 6,493,250 ("Halbert '250"); • U.S. Patent No. 6,851,032 ("LaBerge '032"); • U.S. Patent No. 7,363,422 ("Perego '422"); • U.S. Patent No. 7,024,518 ("Halbert '518"); • U.S. Patent Application Publication No. 2002/0112119 ("Halbert '119"); • DDR SDRAM RDIMM Design Specification

	JEDEC Standard 21-C (4.20.4) (“JEDEC Standard 21-C”); • U.S. Patent No. 6,742,098 (“Halbert ’098”); • U.S. Patent Application Publication No. 2004/0103258 (“Blockmon”); • International Patent Application Publication No. WO 96/020446 (“Williams ’446”); • Synchronous DRAM Architectures, Organizations, and Alternative Technologies (Bruce Jacob); • U.S. Patent No. 6,446,184 (“Dell ’184”); • U.S. Patent No. 6,205,062 (“Kim ’062”); • JEDEC Standards; • U.S. Patent Application Publication No. 2006/0277355 (“Ellsberry”); • U.S. Patent Application Publication No. 2004/0260864 (“Lee ’864”); • International Patent Application Publication No. WO 01/037090 (“Wong ’090”); • U.S. Patent No. 6,154,821 (“Barth”); • U.S. Patent No. 6,226,755 (“Reeves”); • U.S. Patent No. 6,940,782 (“Matsui ’782”); • U.S. Patent No. 7,196,948 (“Vemula”); • U.S. Patent Application Publication No. 2002/0133666 (“Janzen ’666”); • U.S. Patent Application Publication No. 2003/0204688 (“Lee ’688”); • U.S. Patent No. 7,240,145 (“Holman”); • U.S. Patent No. 7,092,299 (“Kwak”); • U.S. Patent Application Publication No. 2002/0118578 (“Janzen ’578”); • U.S. Patent No. 7,149,841 (“LaBerge ’841”); • U.S. Patent No. 7,366,827 (“Lee ’827”); • U.S. Patent No. 7,043,617 (“Williams ’617”); • U.S. Patent No. 7,433,258 (“Rao”); • U.S. Pat. No. 5,581,498 (“Ludwig”); • U.S. Patent No. 5,926,827 (“Dell ’827”); • U.S. Patent Application Publication No. US 2006/0195631 (“Rajamani”); • U.S. Patent Application Publication No. 2005/0198449 (“Haskell”); • FBDIMM Architecture & Protocol; • U.S. Patent Application Publication No. 2005/0257109 (“Averbuj”); • U.S. Patent No. 7,222,224 (“Woo”);
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	• U.S. Patent No. 7,289,383 (“Cornelius”); • U.S. Patent No. 6,529,423 (“Yoon”); • U.S. Patent No. 7,206,896 (“Perego ’896”); • U.S. Patent No. 7,212,424 (“Johnson ’424”); • U.S. Patent No. 5,712,811 (“Kim ’811”); • U.S. Patent No. 7,334,150 (“Ruckerbauer”); • Micron DDR SDRAM RDIMM, MT36VDDF12872 & MT36VDDF25672 Product; • DDR3 Functional Outlook; and/or • The knowledge of a person of ordinary skill in the art.
DDR3 Functional Outlook	• The ’417 Patent’s Admitted Prior Art (“APA”); • U.S. Patent No. 7,103,742 (“Mailloux”); • U.S. Patent Application Publication No. 2006/0117152 (“Amidi”); • DDR2 SDRAM Specification JEDEC Standard JESD79-2A (“JESD79-2A”); • U.S. Patent No. 6,851,032 (“LaBerge ’032”) ; • U.S. Patent No. 7,363,422 (“Perego ’422”); • U.S. Patent No. 6,493,250 (“Halbert ’250”); • U.S. Patent No. 7,024,518 (“Halbert ’518”); • U.S. Patent Application Publication No. 2002/0112119 (“Halbert ’119”); • U.S. Patent No. 7,155,627 (“Matsui ’627”); • DDR SDRAM RDIMM Design Specification JEDEC Standard 21-C (4.20.4) (“JEDEC Standard 21-C”); • U.S. Patent Application Publication No. 2021/0149829 (“Lee ’829”); • U.S. Patent No. 6,742,098 (“Halbert ’098”); • U.S. Patent Application Publication No. 2004/0103258 (“Blockmon”); • International Patent Application Publication No. WO 96/020446 (“Williams ’446”); • Synchronous DRAM Architectures, Organizations, and Alternative Technologies (Bruce Jacob); • U.S. Patent No. 6,446,184 (“Dell ’184”); • U.S. Patent No. 6,205,062 (“Kim ’062”); • JEDEC Standards; • U.S. Patent Application Publication No. 2006/0277355 (“Ellsberry”); • U.S. Patent Application Publication No.

	2004/0260864 (“Lee ’864”); • International Patent Application Publication No. WO 01/037090 (“Wong ’090”); • U.S. Patent No. 6,154,821 (“Barth”); • U.S. Patent No. 6,226,755 (“Reeves”); • U.S. Patent No. 6,940,782 (“Matsui ’782”); • U.S. Patent No. 7,196,948 (“Vemula”); • U.S. Patent Application Publication No. 2002/0133666 (“Janzen ’666”); • U.S. Patent Application Publication No. 2003/0204688 (“Lee ’688”); • U.S. Patent No. 7,240,145 (“Holman”); • U.S. Patent No. 7,092,299 (“Kwak”); • U.S. Patent Application Publication No. 2002/0118578 (“Janzen ’578”); • U.S. Patent No. 7,149,841 (“LaBerge ’841”); • U.S. Patent No. 7,366,827 (“Lee ’827”); • U.S. Patent No. 7,043,617 (“Williams ’617”); • U.S. Patent No. 7,433,258 (“Rao”); • U.S. Pat. No. 5,581,498 (“Ludwig”); • U.S. Patent No. 5,926,827 (“Dell ’827”); • U.S. Patent Application Publication No. US 2006/0195631 (“Rajamani”); • U.S. Patent Application Publication No. 2005/0198449 (“Haskell”); • U.S. Patent Application Publication No. 2005/0257109 (“Averbuj”); • U.S. Patent Application Publication No. 2001/0008006 (“Klein”); • FBDIMM Architecture & Protocol; • U.S. Patent No. 7,222,224 (“Woo”); • U.S. Patent No. 7,289,383 (“Cornelius”); • U.S. Patent No. 6,529,423 (“Yoon”); • U.S. Patent No. 7,206,896 (“Perego ’896”); • U.S. Patent No. 7,212,424 (“Johnson ’424”); • U.S. Patent No. 5,712,811 (“Kim ’811”); • U.S. Patent No. 7,334,150 (“Ruckerbauer”); • U.S. Patent Application Publication No. 2021/0149829 (“Lee ’829”); • Micron DDR SDRAM RDIMM, MT36VDDF12872 & MT36VDDF25672 Product; • Kentron’s Quad Band Memory System (“QBM”); and/or
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	• The knowledge of a person of ordinary skill in the art.
FBDIMM Architecture & Protocol	• The '417 Patent's Admitted Prior Art ("APA"); • U.S. Patent No. 7,103,742 ("Mailloux"); • U.S. Patent Application Publication No. 2006/0117152 ("Amidi"); • U.S. Patent No. 6,851,032 ("LaBerge '032"); • U.S. Patent No. 7,363,422 ("Perego '422"); • U.S. Patent No. 6,493,250 ("Halbert '250"); • U.S. Patent No. 7,024,518 ("Halbert '518"); • U.S. Patent Application Publication No. 2002/0112119 ("Halbert '119"); • DDR SDRAM RDIMM Design Specification JEDEC Standard 21-C (4.20.4) ("JEDEC Standard 21-C"); • U.S. Patent No. 6,742,098 ("Halbert '098"); • U.S. Patent Application Publication No. 2004/0103258 ("Blockmon"); • International Patent Application Publication No. WO 96/020446 ("Williams '446"); • Synchronous DRAM Architectures, Organizations, and Alternative Technologies (Bruce Jacob); • DDR2 SDRAM Specification JEDEC Standard JESD79-2A ("JESD79-2A"); • U.S. Patent No. 6,446,184 ("Dell '184"); • U.S. Patent No. 6,205,062 ("Kim '062"); • JEDEC Standards; • Kentron's Quad Band Memory System ("QBM"); • U.S. Patent Application Publication No. 2006/0277355 ("Ellsberry"); • U.S. Patent Application Publication No. 2004/0260864 ("Lee '864"); • International Patent Application Publication No. WO 01/037090 ("Wong '090"); • U.S. Patent No. 6,154,821 ("Barth"); • U.S. Patent No. 6,226,755 ("Reeves"); • U.S. Patent No. 6,940,782 ("Matsui '782"); • U.S. Patent No. 7,196,948 ("Vemula"); • U.S. Patent Application Publication No. 2002/0133666 ("Janzen '666"); • U.S. Patent Application Publication No. 2003/0204688 ("Lee '688"); • U.S. Patent No. 7,240,145 ("Holman");

	• U.S. Patent No. 7,092,299 (“Kwak”); • U.S. Patent Application Publication No. 2002/0118578 (“Janzen ’578”); • U.S. Patent No. 7,149,841 (“LaBerge ’841”); • U.S. Patent No. 7,366,827 (“Lee ’827”); • U.S. Patent No. 7,043,617 (“Williams ’617”); • U.S. Patent No. 7,433,258 (“Rao”); • U.S. Pat. No. 5,581,498 (“Ludwig”); • U.S. Patent No. 5,926,827 (“Dell ’827”); • U.S. Patent Application Publication No. US 2006/0195631 (“Rajamani”); • U.S. Patent Application Publication No. 2005/0198449 (“Haskell”); • U.S. Patent Application Publication No. 2005/0257109 (“Averbuj”); • U.S. Patent Application Publication No. 2001/0008006 (“Klein”); • U.S. Patent Application Publication No. 2021/0149829 (“Lee ’829”); • U.S. Patent No. 7,222,224 (“Woo”); • U.S. Patent No. 7,289,383 (“Cornelius”); • U.S. Patent No. 6,529,423 (“Yoon”); • U.S. Patent No. 7,206,896 (“Perego ’896”); • U.S. Patent No. 7,212,424 (“Johnson ’424”); • U.S. Patent No. 5,712,811 (“Kim ’811”); • U.S. Patent No. 7,334,150 (“Ruckerbauer”); • Micron DDR SDRAM RDIMM, MT36VDDF12872 & MT36VDDF25672 Product; • DDR3 Functional Outlook; and/or • The knowledge of a person of ordinary skill in the art.
Micron DDR SDRAM RDIMM, MT36VDDF12872 & MT36VDDF25672 Datasheet	• The ’417 Patent’s Admitted Prior Art (“APA”); • U.S. Patent No. 7,103,742 (“Mailloux”); • U.S. Patent Application Publication No. 2006/0117152 (“Amidi”); • DDR2 SDRAM Specification JEDEC Standard JESD79-2A (“JESD79-2A”); • U.S. Patent Application Publication No. 2001/0008006 (“Klein”); • U.S. Patent No. 6,493,250 (“Halbert ’250”); • U.S. Patent No. 6,851,032 (“LaBerge ’032”); • U.S. Patent No. 7,363,422 (“Perego ’422”); • U.S. Patent No. 7,024,518 (“Halbert ’518”);

	• U.S. Patent Application Publication No. 2002/0112119 (“Halbert ’119”); • Kentron’s Quad Band Memory System (“QBM”); • DDR SDRAM RDIMM Design Specification JEDEC Standard 21-C (4.20.4) (“JEDEC Standard 21-C”); • U.S. Patent No. 6,742,098 (“Halbert ’098”); • U.S. Patent Application Publication No. 2004/0103258 (“Blockmon”); • International Patent Application Publication No. WO 96/020446 (“Williams ’446”); • Synchronous DRAM Architectures, Organizations, and Alternative Technologies (Bruce Jacob); • U.S. Patent No. 6,446,184 (“Dell ’184”); • U.S. Patent No. 6,205,062 (“Kim ’062”); • JEDEC Standards; • U.S. Patent Application Publication No. 2006/0277355 (“Ellsberry”); • U.S. Patent Application Publication No. 2004/0260864 (“Lee ’864”); • International Patent Application Publication No. WO 01/037090 (“Wong ’090”); • U.S. Patent No. 6,154,821 (“Barth”); • U.S. Patent No. 6,226,755 (“Reeves”); • U.S. Patent No. 6,940,782 (“Matsui ’782”); • U.S. Patent No. 7,196,948 (“Vemula”); • U.S. Patent Application Publication No. 2002/0133666 (“Janzen ’666”); • U.S. Patent Application Publication No. 2003/0204688 (“Lee ’688”); • U.S. Patent No. 7,240,145 (“Holman”); • U.S. Patent No. 7,092,299 (“Kwak”); • U.S. Patent Application Publication No. 2002/0118578 (“Janzen ’578”); • U.S. Patent No. 7,149,841 (“LaBerge ’841”); • U.S. Patent No. 7,366,827 (“Lee ’827”); • U.S. Patent No. 7,043,617 (“Williams ’617”); • U.S. Patent No. 7,433,258 (“Rao”); • Kentron’s Quad Band Memory System (“QBM”); • U.S. Pat. No. 5,581,498 (“Ludwig”); • U.S. Patent No. 5,926,827 (“Dell ’827”); • U.S. Patent Application Publication No. US
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	2006/0195631 (“Rajamani”); • U.S. Patent Application Publication No. 2005/0198449 (“Haskell”); • FBDIMM Architecture & Protocol; • U.S. Patent Application Publication No. 2005/0257109 (“Averbuj”); • U.S. Patent No. 7,222,224 (“Woo”); • U.S. Patent No. 7,289,383 (“Cornelius”); • U.S. Patent No. 6,529,423 (“Yoon”); • U.S. Patent No. 7,206,896 (“Perego ’896”); • U.S. Patent No. 7,212,424 (“Johnson ’424”); • U.S. Patent No. 5,712,811 (“Kim ’811”); • U.S. Patent No. 7,334,150 (“Ruckerbauer”); • DDR3 Functional Outlook; and/or • The knowledge of a person of ordinary skill in the art.
Micron DDR SDRAM RDIMM, MT36VDDF12872 and/or MT36VDDF25672 Products	• The ’417 Patent’s Admitted Prior Art (“APA”); • U.S. Patent No. 7,103,742 (“Mailloux”); • U.S. Patent Application Publication No. 2006/0117152 (“Amidi”); • DDR2 SDRAM Specification JEDEC Standard JESD79-2A (“JESD79-2A”); • U.S. Patent Application Publication No. 2001/0008006 (“Klein”); • U.S. Patent No. 6,493,250 (“Halbert ’250”); • U.S. Patent No. 6,851,032 (“LaBerge ’032”) ; • U.S. Patent No. 7,363,422 (“Perego ’422”); • U.S. Patent No. 7,024,518 (“Halbert ’518”); • U.S. Patent Application Publication No. 2002/0112119 (“Halbert ’119”); • DDR SDRAM RDIMM Design Specification JEDEC Standard 21-C (4.20.4) (“JEDEC Standard 21-C”); • U.S. Patent No. 6,742,098 (“Halbert ’098”); • U.S. Patent Application Publication No. 2004/0103258 (“Blockmon”); • International Patent Application Publication No. WO 96/020446 (“Williams ’446”); • Synchronous DRAM Architectures, Organizations, and Alternative Technologies (Bruce Jacob); • U.S. Patent No. 6,446,184 (“Dell ’184”); • U.S. Patent No. 6,205,062 (“Kim ’062”); • JEDEC Standards;

	• U.S. Patent Application Publication No. 2006/0277355 (“Ellsberry”); • U.S. Patent Application Publication No. 2004/0260864 (“Lee ’864”); • International Patent Application Publication No. WO 01/037090 (“Wong ’090”); • U.S. Patent No. 6,154,821 (“Barth”); • U.S. Patent No. 6,226,755 (“Reeves”); • U.S. Patent No. 6,940,782 (“Matsui ’782”); • U.S. Patent No. 7,196,948 (“Vemula”); • U.S. Patent Application Publication No. 2002/0133666 (“Janzen ’666”); • U.S. Patent Application Publication No. 2003/0204688 (“Lee ’688”); • U.S. Patent No. 7,240,145 (“Holman”); • U.S. Patent No. 7,092,299 (“Kwak”); • U.S. Patent Application Publication No. 2002/0118578 (“Janzen ’578”); • U.S. Patent No. 7,149,841 (“LaBerge ’841”); • U.S. Patent No. 7,366,827 (“Lee ’827”); • U.S. Patent No. 7,043,617 (“Williams ’617”); • U.S. Patent No. 7,433,258 (“Rao”); • U.S. Pat. No. 5,581,498 (“Ludwig”); • U.S. Patent No. 5,926,827 (“Dell ’827”); • U.S. Patent Application Publication No. US 2006/0195631 (“Rajamani”); • U.S. Patent Application Publication No. 2005/0198449 (“Haskell”); • FBDIMM Architecture & Protocol; • U.S. Patent Application Publication No. 2005/0257109 (“Averbuj”); • U.S. Patent No. 7,222,224 (“Woo”); • U.S. Patent No. 7,289,383 (“Cornelius”); • U.S. Patent No. 6,529,423 (“Yoon”); • U.S. Patent No. 7,206,896 (“Perego ’896”); • U.S. Patent No. 7,212,424 (“Johnson ’424”); • U.S. Patent No. 5,712,811 (“Kim ’811”); • U.S. Patent No. 7,334,150 (“Ruckerbauer”); • DDR3 Functional Outlook; and/or • The knowledge of a person of ordinary skill in the art.
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As mentioned above, Defendants have not yet completed their search or discovery

concerning additional prior art. Moreover, the exemplary combinations are provided based on Defendants' current understanding of the Asserted Claims and Plaintiff's apparent view of the scope of those claims as shown, for example, in Plaintiff's Infringement Contentions. Further, a *Markman* Order has not yet been issued in this case. As such, Defendants' inclusion of exemplary combinations does not preclude them from identifying other invalidating combinations as appropriate, and Defendants reserve the right to identify additional specific combinations as well as to detail and explain such combinations.

C. Double Patenting

As stated above, Defendants incorporate by reference all other invalidity contentions related to the Asserted Patents served on or otherwise provided to Plaintiff, whether past or future. In addition to certain claims being anticipated or obvious at least under Plaintiff's apparent claim constructions as indicated above, the Asserted Claims are also invalid under the doctrine of obviousness-type double patenting.

4. U.S. Patent No. 7, 619,912

As demonstrated in Exhibits A13 and A14, the following exemplary patents commonly assigned to Netlist render the Asserted Claims of the '912 patent invalid under the doctrine of obviousness-type double patenting:

Patent No. or Title (Primary Inventor/Author)	Date of Issue/ Publication	Filing Date	Expiration Date
U.S. Patent Publication No. 7,286,436 (“the ’436 patent”)	Oct. 23, 2007	Mar. 7, 2005	May 15, 2025
U.S. Patent Publication No. 7,289,386 (“the ’386 patent”)	Oct. 30, 2007	Jul. 1, 2005	Mar. 28, 2025
U.S. Patent Publication No. 7,864,627 (“the ’627 patent”)	Jan. 4, 2011	Oct. 12, 2009	Mar. 7, 2025
U.S. Patent Publication No. 7,916,574 (“the ’574 patent”)	Mar. 29, 2011	Nov. 29, 2010	Mar. 7, 2025
U.S. Patent Publication No. 7,636,274 (“the ’274 patent”)	Dec. 22, 2009	Mar. 20, 2009	Mar. 7, 2025
U.S. Patent Publication No. 7,881,150 (“the ’150 patent”)	Feb. 1, 2011	Dec. 2, 2009	Mar. 7, 2025
U.S. Patent Publication No. 8,081,535 (“the ’535 patent”)	Dec. 20, 2011	Nov. 24, 2010	Mar. 7, 2025
U.S. Patent Publication No. 8,081,537 (“the ’537 patent”)	Dec. 20, 2011	Jun. 6, 2011	Mar. 7, 2025

For reasons stated in Section IV.B.1, these patents alone or together render obvious the ’912 patent. In addition, as explained in Section IV.B.1, each of the aforementioned patents in combination with one or more of the following prior art references render the asserted claims of the ’912 patent obvious.

- Admitted Prior Art (“APA”)
- U.S. Patent App. Pub. No. 20060117152 (“Amidi”)
- U.S. Patent App. Pub. No. 2006/0277355 (“Ellsberry”)
- U.S. Patent No. 7,240,145 (“Holman”)
- JEDEC Standards, including without limitation JEDEC Standard JESD79, Double Data Rate (DDR) SDRAM Specification (June 2000) (“JESD79”), JEDEC Standard JESD79-2, DDR SDRAM Specification (September 2003) (“JESD79-2”), JEDEC Standard JESD21-C, PC2100 and PC1600 DDR SDRAM Registered DIMM Design Specification (January 2002) (“JESD 21-

C”), JEDEC Standard DDR SDRAM Specification, JESD79C (March 2003)
 (“JESD79C”)

- U.S. Patent No. 7,363,422 (“Perego ’422”)
- U.S. Patent No. 5,926,827 (“Dell ’827”)
- U.S. Patent No. 6,209, 074 (“Dell ’074”)
- Micron DDR SDRAM RDIMM, MT36VDDF12872 & MT36VDDF25672 Product (“Micron RDIMM”)
- DDR SDRAM Specification, JDEC Standard No. 79C, March 2003
- Kentron’s Quad Band Memory System (“QBM”)
- U.S. Patent No. 6,961,281 (“Wong”)
- U.S. Patent No. 6,996, 686 (“Doblar”)
- U.S. Patent No. 6,757,751 (“Gene”)
- U.S. Patent No. 6,742,098 (“Halbert”)
- U.S. Patent No. 7,181,584 (“LaBerge”)
- U.S. Patent No. 6,286,077 (“Choi”)
- U.S. Patent No. 7,020,739 (“Mukaida”)
- U.S. Patent App. Pub. No. 2007/0043922 (“Lee”)
- U.S. Patent No. 7,414,312 (“Nguyen”); and/or
- DDR3 Functional Outlook

5. U.S. Patent No. 9,858,215

As demonstrated in Exhibit B21, the following exemplary patents commonly assigned to Netlist render the Asserted Claims of the ’215 patent invalid under the doctrine of obviousness-type double patenting:

Patent No. or Title (Primary Inventor/Author)	Date of Issue/ Publication	Filing Date	Expiration Date
U.S. Patent Publication No. 9,037,774 (“Solomon ‘774”)	8/20/2013	4/15/2010	3/7/2025
U.S. Patent Publication No. 7,289,386 (“Bhakta”)	3/23/2006	7/1/2005	3/28/2025
U.S. Patent Publication No. 8,516,185 (“Lee ‘185”)	8/20/2013	4/15/2010	1/13/2030
U.S. Patent Publication No. 9,606,907 (“Lee ‘907”)	3/28/2017	8/20/2013	7/5/2030

For reasons stated in Section IV.B.2, these patents alone or together render obvious the ’215 patent. In addition, as explained in Section IV.B.2, each of the aforementioned patents in combination with one or more of the following prior art references render the asserted claims of the ’215 patent obvious.

- The ’215 Patent’s Admitted Prior Art (“APA”)
- U.S. Patent Application Publication No. 2003/0204688 (“Lee ’688”)
- U.S. Patent Application Publication No. 2006/0117152 (“Amidi”)
- U.S. Patent Application Publication No. 2003/0145156 (“Khandekar”)
- U.S. Patent No. 6,862,653 (“Dodd”)
- U.S. Patent No. 6,757,751 (“Gene”)
- U.S. Patent Application Publication No. 2003/0117864 (“Hampel”)
- U.S. Patent No. 7,240,145 (“Holman”)
- U.S. Patent Application Publication No. 2002/0112119 (“Halbert ’119”)
- JEDEC Standards
- FBDIMM Architecture & Protocol
- U.S. Patent No. 6,205,062 (“Kim ’062”)
- U.S. Patent No. 6,262,938 (“Lee ’938”)
- U.S. Patent No. 6,392,909 (“Jang”)

- U.S. Patent No. 6,529,423 (“Yoon”)
- U.S. Patent No. 6,564,287 (“Lee ’287”)
- U.S. Patent No. 7,289,383 (“Cornelius”)
- U.S. Patent No. 7,433,258 (“Rao”)
- U.S. Patent No. 5,581,498 (“Ludwig”)
- U.S. Patent No. 5,712,811 (“Kim ’811”)
- U.S. Patent No. 5,926,827 (“Dell ’827”)
- U.S. Patent No. 6,414,868 (“Wong ’868”)
- U.S. Patent No. 6,446,184 (“Dell ’184”)
- U.S. Patent No. 6,493,250 (“Halbert ’250”)
- U.S. Patent No. 6,529,993 (“Rogers”)
- U.S. Patent No. 6,615,345 (“LaBerge ’345”)
- U.S. Patent No. 6,820,163 (“McCall”)
- U.S. Patent No. 7,334,150 (“Ruckerbauer”)
- U.S. Patent No. 7,024,518 (“Halbert ’518”)
- U.S. Patent No. 7,043,617 (“Williams ’617”)
- U.S. Patent No. 7,092,299 (“Kwak”)
- U.S. Patent No. 7,149,841 (“LaBerge ’841”)
- U.S. Patent No. 7,206,896 (“Perego ’896”)
- U.S. Patent No. 7,212,424 (“Johnson ’424”)
- U.S. Patent No. 7,222,224 (“Woo”)
- U.S. Patent No. 7,363,422 (“Perego ’422”)
- U.S. Patent No. 7,366,827 (“Lee ’827”)
- U.S. Patent Application Publication No. 2001/0008006 (“Klein”)

- U.S. Patent Application Publication No. 2002/0118578 (“Janzen ’578”)
- U.S. Patent Application Publication No. 2002/0188816 (“Johnson ’816”)
- U.S. Patent Application Publication No. 2003/0039151 (“Matsui ’151”)
- U.S. Patent Application Publication No. 2003/0133331 (“LaBerge ’331”)
- U.S. Patent Application Publication No. 2004/0034755 (“LaBerge ’755”)
- U.S. Patent Application Publication No. 2005/0050255 (“Jeddeloh”)
- U.S. Patent Application Publication No. 2005/0198449 (“Haskell”)
- U.S. Patent Application Publication No. 2005/0257109 (“Averbuj”)
- U.S. Patent Application Publication No. 2006/0195631 (“Rajamani”)
- U.S. Patent Application Publication No. 2006/0277355 (“Ellsberry”)
- Synchronous DRAM Architectures, Organizations, and Alternative Technologies (Bruce Jacob)
- U.S. Patent No. 7,103,742 (“Mailloux”)
- U.S. Patent No. 6,851,032 (“LaBerge ’032”)
- U.S. Patent No. 6,154,821 (“Barth”)
- U.S. Patent No. 6,226,755 (“Reeves”)
- U.S. Patent No. 6,742,098 (“Halbert ’098”)
- U.S. Patent No. 6,940,782 (“Matsui ’782”)
- U.S. Patent No. 7,196,948 (“Vemula”)
- U.S. Patent Application Publication No. 2002/0133666 (“Janzen ’666”)
- U.S. Patent Application Publication No. 2004/0103258 (“Blockmon”)
- U.S. Patent Application Publication No. 2004/0260864 (“Lee ’864”)
- International Patent Application Publication No. WO 96/020446 (“Williams ’446”)
- International Patent Application Publication No. WO 01/037090 (“Wong ’090”)

- DDR SDRAM RDIMM Design Specification JEDEC Standard 21-C (4.20.4) (“JEDEC Standard 21-C”)
- DDR2 SDRAM Specification JEDEC Standard JESD79-2A (“JESD79-2A”)
- U.S. Patent. No. 7,155,627 (“Matsui ’627”)
- U.S. Patent Application Publication No. 2021/0149829 (“Lee ’829”)
- Kentron’s Quad Band Memory System (“QBM”)
- Micron DDR SDRAM RDIMM, MT36VDDF12872 & MT36VDDF25672 Product (“Micron RDIMM”)
- DDR3 Functional Outlook; and/or
- The knowledge of a person of ordinary skill in the art.

6. U.S. Patent No. 11,093,417

As demonstrated in Exhibit C18, the following exemplary patents commonly assigned to Netlist render the Asserted Claims of the ’417 patent invalid under the doctrine of obviousness-type double patenting:

Patent No. or Title (Primary Inventor/Author)	Date of Issue/ Publication	Filing Date	Expiration Date
U.S. Patent Publication No. 10,489,314 (“Solomon ’314”)	11/26/2019	12/28/2017	3/7/2025
U.S. Patent Publication No. 9,037,774 (“Solomon ’774”)	8/20/2013	4/15/2010	3/7/2025
U.S. Patent Publication No. 9,858,215 (“the ’215 patent”)	1/2/2018	5/18/2016	9/15/2025

For reasons stated in Section IV.B.3, these patents alone or together render obvious the ’417 patent. In addition, as explained in Section IV.B.3, each of the aforementioned patents in combination with one or more of the following prior art references render the asserted claims of the ’417 patent obvious.

- The ’417 Patent’s Admitted Prior Art (“APA”)

- U.S. Patent No. 7,103,742 (“Mailloux”)
- U.S. Patent Application Publication No. 2006/0117152 (“Amidi”)
- U.S. Patent No. 6,851,032 (“LaBerge ’032”)
- U.S. Patent No. 7,363,422 (“Perego ’422”)
- U.S. Patent No. 6,493,250 (“Halbert ’250”)
- U.S. Patent No. 7,024,518 (“Halbert ’518”)
- U.S. Patent Application Publication No. 2002/0112119 (“Halbert ’119”)
- DDR SDRAM RDIMM Design Specification JEDEC Standard 21-C (4.20.4) (“JEDEC Standard 21-C”)
- U.S. Patent No. 6,742,098 (“Halbert ’098”)
- U.S. Patent Application Publication No. 2004/0103258 (“Blockmon”)
- International Patent Application Publication No. WO 96/020446 (“Williams ’446”)
- Synchronous DRAM Architectures, Organizations, and Alternative Technologies (Bruce Jacob)
- DDR2 SDRAM Specification JEDEC Standard JESD79-2A (“JESD79-2A”)
- U.S. Patent No. 6,446,184 (“Dell ’184”)
- U.S. Patent No. 6,205,062 (“Kim ’062”)
- JEDEC Standards
- Kentron’s Quad Band Memory System (“QBM”)
- U.S. Patent Application Publication No. 2006/0277355 (“Ellsberry”)
- U.S. Patent Application Publication No. 2004/0260864 (“Lee ’864”)
- International Patent Application Publication No. WO 01/037090 (“Wong ’090”)
- U.S. Patent No. 6,154,821 (“Barth”)

- U.S. Patent No. 6,226,755 (“Reeves”)
- U.S. Patent No. 6,940,782 (“Matsui ’782”)
- U.S. Patent No. 7,196,948 (“Vemula”)
- U.S. Patent Application Publication No. 2002/0133666 (“Janzen ’666”)
- U.S. Patent Application Publication No. 2003/0204688 (“Lee ’688”);
- U.S. Patent No. 7,240,145 (“Holman”)
- U.S. Patent No. 7,092,299 (“Kwak”)
- U.S. Patent Application Publication No. 2002/0118578 (“Janzen ’578”)
- U.S. Patent No. 7,149,841 (“LaBerge ’841”)
- U.S. Patent No. 7,366,827 (“Lee ’827”)
- U.S. Patent No. 7,043,617 (“Williams ’617”)
- U.S. Patent No. 7,433,258 (“Rao”)
- U.S. Pat. No. 5,581,498 (“Ludwig”)
- U.S. Patent No. 5,926,827 (“Dell ’827”)
- U.S. Patent Application Publication No. US 2006/0195631 (“Rajamani”)
- U.S. Patent Application Publication No. 2005/0198449 (“Haskell”)
- U.S. Patent Application Publication No. 2005/0257109 (“Averbuj”)
- U.S. Patent Application Publication No. 2001/0008006 (“Klein”)
- U.S. Patent Application Publication No. 2021/0149829 (“Lee ’829”)
- U.S. Patent No. 7,222,224 (“Woo”)
- U.S. Patent No. 7,289,383 (“Cornelius”)
- U.S. Patent No. 6,529,423 (“Yoon”)
- U.S. Patent No. 7,206,896 (“Perego ’896”)

- U.S. Patent No. 7,212,424 (“Johnson ’424”)
- U.S. Patent No. 5,712,811 (“Kim ’811”)
- U.S. Patent No. 7,334,150 (“Ruckerbauer”)
- U.S. Patent No. 6,757,751 (“Gene”)
- U.S. Patent No. 6,961,281 (“Wong ’281”)
- U.S. Patent No. 6,414,868 (“Wong ’868”)
- U.S. Patent No. 6,820,163 (“McCall”)
- FBDIMM Architecture & Protocol
- Micron DDR SDRAM RDIMM, MT36VDDF12872 & MT36VDDF25672 Product (“Micron RDIMM”)
- DDR3 Functional Outlook; and/or
- The knowledge of a person of ordinary skill in the art.

V. P.R. 3-3(c) – Claim Charts

Pursuant to Rule 3-3(d), Defendants identify invalidity claim charts identifying disclosures in the references identified in Section III supra as to the Asserted Claims of the Asserted Patents are provided in attached Appendix A (’912 patent), Appendix B (’215 patent), and Appendix C (’417 patent).

Defendants have identified relevant portions and/or features of the prior art. However, the identified prior art may contain additional descriptions of or alternative support for the claim limitations. Defendants may rely on uncited portions or features of the identified prior art, other documents, and expert testimony, to provide context or to aid in understanding the identified prior art and the state of the art. Citations to a particular figure in a reference include the caption and description of the figure and any text relating to the figure. Similarly, citations to particular

text referring to a figure include the figure and caption as well. Portions relevant to dependent claims incorporate by reference the citations to the chain of claims from which that dependent claim derives. Likewise, portions related to subsequent limitations that refer to claim elements identified, described, and/or cited to in earlier limitations may rely on the citations related to those portions of the claim chart that identify and/or describe these elements.

Throughout the invalidity claim charts in Appendices A-C, Defendants provide examples of where references disclose subject matter recited in preambles of the Asserted Claims, regardless whether the preambles limit the claims. Defendants reserve the right to argue that the preambles are or are not limitations. Further, where an entry in a claim chart corresponding to a given limitation refers back to the discussion of another claim, the entry incorporates all evidence cited for the other claim.

VI. P. R. 3-3(d) – Other Grounds for Invalidity

A. U.S. Patent No. 7,619,912

Pursuant to Rule 3-3(d), Defendants hereby identify grounds of invalidity for the '912 Patent based on lack of written description under 35 U.S.C. § 112, first paragraph; lack of enablement under 35 U.S.C. § 112, first paragraph; indefiniteness under 35 U.S.C. § 112, second paragraph; and indefiniteness under 35 U.S.C. § 112, sixth paragraph. These contentions shall not be construed as an admission that any claim construction advanced by Defendants in this case is in any way inconsistent, flawed, or erroneous. Nor should these contentions prevent Defendants from advancing claim construction and/or non-infringement positions in lieu of, or in addition to, invalidity positions. Further, these contentions shall not be construed as an admission of or acquiescence to Plaintiff's purported construction of the claim language or of other positions advanced by Plaintiff during the course of this litigation. Defendants' invalidity contentions under

35 U.S.C. § 112 may depend, in part, on the Court’s claim construction, as well as Plaintiff’s alleged scope of the ’912 patent Asserted Claims. Consequently, Defendants only identify the issues under 35 U.S.C. § 112 of which they are presently aware.

1. Lack of Written Description and/or Enablement Under 35 U.S.C. § 112, ¶ 1

The ’912 Patent does not provide sufficient written description to establish that the inventors were in possession of the alleged inventions recited in the ’912 patent Asserted Claims at the time the ’912 patent was filed. *Ariad Pharms., Inc. v. Eli Lilly & Co.*, 598 F.3d 1336, 1351 (Fed. Cir. 2010). In other words, the applicants did not describe their purported inventions in a manner that “reasonably conveys to those skilled in the art that the inventor had possession of the claimed subject matter as of the filing date.” *Id.* One of ordinary skill in the art would not have understood that the inventors were in possession of the full scope of the claimed apparatus and methods.

The specification of the ’912 patent also ’912 not enable one of ordinary skill in the art to make and/or use certain recited elements of the ’912 patent Asserted Claims without undue experimentation. To the extent the following limitations are definite (under 35 U.S.C. § 112, ¶ 2), the application that became the ’912 patent fails to sufficiently describe or enable them as required by 35 U.S.C. § 112, ¶ 1:⁵

Term	Relevant Claim(s)
“rank”	1, 15, 16, 28, 39, 77, 80, 82, 86, 88, 90
“logic element”	1, 6, 8, 15, 16, 24, 27, 28, 29, 39, 43, 45, 59, 60, 77, 80, 82, 86, 88, 90

⁵ Listed claims also include all Asserted Claims dependent thereon, even if those claims are not individually listed.

Term	Relevant Claim(s)
“buffer”	1, 15, 28, 39, 77 80, 82, 86, 88, 90
“in the direction along the first side”	11, 47
“in the direction along the second side”	11, 47
“register”	1, 8, 15, 16, 27, 28, 39, 45, 58, 72, 77, 80, 82, 86, 88, 90
“receiving a set of input [control] signals from the computer system, the set of input [control] signals comprising at least one row/column address signal, bank address signals, [and at least one/a] chip-select signal[, and an input command signal]”	1, 15, 16, 28, 77, 80, 82, 86, 88
“the set of input control signals corresponding to a second number of DDR memory devices”	1, 77, 80, 82
“generating a [set/plurality] of output [control] signals in response to the [set/plurality of input [control] signals”	1, 15, 16, 28, 39, 77, 80, 82, 86, 88, 90
“the set of output control signals corresponding to the first number of DDR memory devices”	1, 77, 80, 82
“responds to a first command signal and the set of input control signals from the computer system by generating and transmitting a second command signal and the set of output control signals to the plurality of memory devices”	1, 77, 80, 82
“the first command signal and the set of input control signals corresponding to the second number of ranks and the second command signal and the set of output control signals corresponding to the first number of ranks”	1, 77, 80, 82
“the phase-lock loop device operatively coupled to the plurality of DDR [memory/DRAM] devices, the logic element, and the register”	1, 15, 16, 28, 77, 80, 82, 86, 88
“in respons[e/ive] to signals received from the computer system, the phase-lock loop (PLL) device transmits a PLL clock signal to the plurality of DDR [DRAM] memory devices, the logic element, and the register”	1, 15, 28, 39, 77, 82, 86, 88, 90
“the register (i) receives, from the computer system, and (ii) buffers, in response to the PLL clock signal, a plurality of row/column address signals and the bank address signals”	1, 15, 28, 77, 82, 86, 88
“transmits the buffered plurality of row/column address signals and the buffered bank address signals to the plurality of DDR memory devices”	1, 77, 82
“the [at least one] row/column address signal received by the logic element comprises [at least one/a] row address signal received by the logic element”	1, 15, 28, 39, 77, 80, 82, 86, 90
“the plurality of row[/column] address signals received by the register are separate from the [at least one] row address signal received by the logic element”	1, 15, 28, 39, 77, 80, 82, 86, 90

Term	Relevant Claim(s)
“generates gated column access strobe (CAS) signals or chip-select signals of the output control signals in response to at least in part to (i) the at least one row address signal, (ii) the bank address signals, and (iii) the at least one chip-select signal of the [set/plurality] of input [control] signals and (iv) the PLL clock signal.”	1, 15, 28, 39
“wherein the set of input control signals comprises a first number of chip-select signals and wherein the set of output control signals comprises a second number of chip-select signals”	3
“custom-designed semiconductor device”	6, 24, 29, 41
“spaced from”	10, 11, 46, 47
“a direction along the [first/second] side”	11, 47
“the set of input signals configured to control a second number of DDR [memory/DRAM] devices”	15, 16, 28, 86, 88
“the set of output signals configured to control the first number of DDR [memory/DRAM] devices”	15, 16, 28, 86, 88
“the circuit further responds to a command signal and the set of input signals from the computer system by selecting one or two ranks”	15, 16, 86
“transmits the buffered plurality of row/column address signals and the buffered bank address signals to the at least one DDR [memory/DRAM] device of the selected one or two ranks of the first number of ranks”	15, 28, 86, 88
“the command signal is transmitted to only one DDR memory device at a time”	16
“the command signal is transmitted to two ranks of the first number of ranks at a time”	18
“the command signal is transmitted to the two ranks of the first number of ranks concurrently”	20
“the set of input signals comprises a density bit which is a row address bit”	22
“the circuit is configured to store the row address bit during an activate command for a selected bank”	22
“double-data-rate (DDR) dynamic random access memory (DRAM) devices”	28
“the circuit further responds to the set of input control signals from the computer system by selecting at least one rank of the first number of ranks”	28, 88
“the set of input control signals comprises fewer chip-select signals than does the set of output control signals”	31
“wherein the set of input control signals comprises two chip-select signals and the set of output control signals comprises four chip-select signals”	32
“two or more ranks which are selectable by a first number of chip-select signals”	39, 90
“integrated circuit element”	39, 90

Term	Relevant Claim(s)
“the at least one integrated circuit element comprising a logic element, a register, and [a] phase-lock loop device operationally coupled to the plurality of DDR memory devices, the logic element, and the register”	39, 90
“receiving a plurality of input signals from the computer system, the plurality of input signals comprising row address signals, column address signals, bank address signals, command signals, and a second number of chip-select signals less than the first number of chip-select signals”	39, 90
“the at least one integrated circuit element further responsive to the plurality of input signals by selecting at least one rank of the two or more ranks”	39, 90
“transmitting the plurality of output signals to at least one DDR memory device of the selected at least one rank”	39, 90
“the register (i) receives, from among the plurality of input signals, and (ii) buffers, in response to the PLL clock signal, the bank address signals and a plurality of the row address signals”	39, 90
transmits the buffered bank address signals and the buffered [plurality of] row address signals to the at least one DDR memory device of the selected at least one rank	39, 90
“the plurality of output signals corresponds to a first number of DDR memory devices arranged in the two or more ranks which are selectable by the first number of chip-select signals”	40
“the plurality of input signals corresponds to a second number of DDR memory devices arranged in ranks which are selectable by the second number of chip-select signals”	40
“simulates a virtual memory module having the second number of DDR memory devices”	40
“the at least one integrated circuit element is configured to respond to the plurality of input signals by selecting at least one rank of the two or more ranks”	50
“the plurality of DDR [memory/DRAM] devices has [at least one attribute/one or more attributes] selected from a group consisting of a number of row address bits per DDR [memory/DRAM] device, a number of column address bits per DDR [memory/DRAM] device, a number of [internal] bank[s/address bits] per DDR [memory/DRAM] device, a number of DDR [memory/DRAM] devices, a data width per DDR [memory/DRAM] device, a memory density per DDR [memory/DRAM] device, a number of ranks of DDR [memory/DRAM] devices, and a memory density per rank”	52, 62, 63, 64, 69, 73, 81
“a read-only nonvolatile memory device storing data accessible to the computer system”	52, 55
“the data characterizes the plurality of DDR memory devices as having at least one value of the at least one attribute that is different	52

Term	Relevant Claim(s)
from an actual value of the at least one attribute of the plurality of DDR memory devices”	
“the data characterizes the plurality of DDR [memory/DRAM] devices as having fewer ranks of DDR [memory/DRAM] devices than the plurality of DDR [memory/DRAM] devices actually has, and as having a greater memory density per rank than the plurality of DDR [memory/DRAM] devices actually has”	54, 65, 70, 74
“DDR dynamic random-access memory (DRAM) chip package with a bit width”	55
“the data characterizes the memory module as having fewer ranks than the first number of ranks, and as having a greater memory density per rank than the memory module actually has”	55
“means for characterizing the plurality of DDR [memory/DRAM] devices as having one or more attributes that are different from actual attributes of the plurality of DDR [memory/DRAM] devices”	56, 71, 75
“the set of input control signals corresponds to a first memory density, and the set of output control signals corresponds to a second memory density”	57
“the register comprises a plurality of register devices”	58
“the at least one row address signal and the bank address signals are (i) received by the logic element during an activate command operation and (ii) are used by the logic element for a subsequent read or write command operation”	60
“a read-only memory (ROM) serial-presence detect (SPD) device, the SPD device storing data accessible to the computer system”	62, 63, 64, 69, 73, 81
“the data characterizes the plurality of DDR [memory/DRAM] devices as having one or more attributes that are different from [the] one or more attributes of [the] plurality of DDR [memory/DRAM] devices”	62, 63, 64, 69, 73, 81
“the logic element responds to at least (i) a row address bit of the at least one row/column address signal, (ii) the bank signals, and (iii) the at least one chip-select signal of the set of input control signals and (iv) the PLL clock by generating a first number of chip-select signals of the set of output control signals”	77
“wherein operation of the register is responsive at least in part to clock signals received from the phase-lock loop device”	80
“the logic element generates a first number of chips-elect signals of the set of output control signals in response at least in part to clock signals received from the phase-lock loop device”	80
“a plurality of row/column address signals and the bank address signals are received from the computer system and buffered by the register, the register transmitting the buffered plurality of row/column address signals and the buffered bank address signals to the plurality of DDR memory devices”	80

Term	Relevant Claim(s)
“generation of the first number of chip-select signals of the output control signals by the logic element is based on the logic element responsive at least in part to (i) the at least one row address signal, (ii) the bank address signals, and (iii) the at least one chip-select signal of the set of input control signals received by the logic element and (iv) the clock signals received from the phase-lock loop device”	80
“the logic element responds to at least the at least one row address signal, the bank address signals, and the at least one chip-select signal of the set of input control signals and the PLL clock signal by generating a number of rank-selecting signals of the set of output control signals that is greater than double or equal to double the number of chip-select signals of the set of input control signals”	82
“the memory module is operable to perform successive read accesses from different ranks of DDR memory devices”	83
“the memory module is operable to perform back-to-back adjacent read commands which cross DDR memory device boundaries”	84, 87, 89, 91
“the bank address signals include bank address signals received during an activate command operation and bank address signals received during a read or write command operation subsequent to the activate command operation”	85
“and the rank-selecting signals are used for the read or write command operation”	85
“the logic element responds to at least the at least one row address signal, the bank address signals, and the at least one chip-select signal of the set of input signals and the PLL clock signal by generating a number of rank-selecting signals of the set of output signals that is greater than double or equal to double the number of chip-select signals of the set of input signals”	86
“the logic element responds to at least (i) the row address signal, (ii) the bank address signals, (iii) and the one chip-select signal of the set of input control signals and (iv) the PLL clock signal by generating a number of rank-selecting signals of the set of output signals that is greater than double or equal to double the number of chip-select signals of the set of input control signals”	88
“the logic element responds to at least (i) the at least one row signal, (ii) the bank address signals, (iii) and the second number of chip-select signals of the plurality of input signals and (iv) the PLL clock signal by generating the first number of chip-select signals of the plurality of output signals that is greater than double or equal to double the second number of chip-select signals of the plurality of input signals”	90

2. Invalidity Under 35 U.S.C. § 112, ¶ 2

“[T]he second paragraph of § 112 contains two requirements: first, the claim must set forth what the applicant regards as his invention, and second, it must do so with sufficient particularity and distinctness, *i.e.*, the claim must be sufficiently definite.” *Allen Eng’g Corp. v. Bartell Indus., Inc.*, 299 F.3d 1336, 1348 (Fed. Cir. 2002) (internal quotation marks and alteration omitted). “Where it would be apparent to one of skill in the art, based on the specification, that the invention set forth in a claim is not what the patentee regarded as his invention,” the claim is “invalid under § 112, paragraph 2.” *Id.* at 1349. Several of the ’912 patent Asserted Claims are invalid because it would be apparent to one of skill in the art, based on the specification, that the invention set forth in these claims are not what the patentee regarded as his invention. *Id.* These claims are invalid under the “applicant regards” prong of § 112 at least because they contain elements that differ from and/or conflict with the ’912 patent’s written description of the invention, or because they omit elements that one of skill in the art would understand as part of the ’912 patent’s invention based on the specification: 1, 3, 4, 6, 8, 10, 11, 15, 16, 18, 19, 20, 22, 24, 27, 28, 29, 31, 32, 34, 36, 37, 38, 39, 40, 41, 43, 45, 46, 47, 50, 52, 53, 54, 55, 56, 57, 58, 59, 60, 62, 63, 64, 65, 69, 70, 71, 72, 73, 74, 75, 77, 80-87, 88-89, 90-91.

Under § 112, ¶ 2, “a patent is invalid for indefiniteness if its claims, read in light of the specification delineating the patent, and the prosecution history, fail to inform, with reasonable certainty, those skilled in the art about the scope of the invention.” *Nautilus, Inc. v. Biosig Instruments, Inc.*, 572 U.S. 898, 901 (2014). Several of the ’912 patent Asserted Claims are also invalid as indefinite under § 112, ¶ 2 because they fail to inform those skilled in the art about the scope of the invention with reasonable certainty and are indefinite.

The following limitations recited in the '912 patent Asserted Claims are indefinite in whole, in part or in combination:⁶

Term	Relevant Claim(s)
“logic element”	1, 6, 8, 15, 16, 24, 27, 28, 29, 39, 43, 45, 59, 60, 77, 80, 82, 86, 88, 90
“buffer”	1, 15, 28, 39, 77 80, 82, 86, 88, 90
“in the direction along the first side”	11, 47
“in the direction along the second side”	11, 47
“memory module connectable to a computer system”	1, 15, 16, 28, 39, 77, 80, 82, 86, 88, 90
“double-data-rate (DDR) memory devices”	1, 15, 16, 39, 77, 80, 82, 86, 88, 90
“register”	1, 8, 15, 16, 27, 28, 39, 45, 58, 72, 77, 80, 82, 86, 88, 90
“receiving a set of input [control] signals from the computer system, the set of input [control] signals comprising at least one row/column address signal, bank address signals, [and at least one/a] chip-select signal[, and an input command signal]”	1, 15, 16, 28, 77, 80, 82, 86, 88
“the set of input control signals corresponding to a second number of DDR memory devices”	1, 77, 80, 82
“generating a [set/plurality] of output [control] signals in response to the [set/plurality of input [control] signals”	1, 15, 16, 28, 39, 77, 80, 82, 86, 88, 90
“the set of output control signals corresponding to the first number of DDR memory devices”	1, 77, 80, 82
“responds to a first command signal and the set of input control signals from the computer system by generating and transmitting a second command signal and the set of output control signals to the plurality of memory devices”	1, 77, 80, 82
“the first command signal and the set of input control signals corresponding to the second number of ranks and the second command signal and the set of output control signals corresponding to the first number of ranks”	1, 77, 80, 82

⁶ Listed claims also include all Asserted Claims dependent thereon, even if those claims are not individually listed.

Term	Relevant Claim(s)
“the phase-lock loop device operatively coupled to the plurality of DDR [memory/DRAM] devices, the logic element, and the register”	1, 15, 16, 28, 77, 80, 82, 86, 88
“in respons[e/ive] to signals received from the computer system, the phase-lock loop (PLL) device transmits a PLL clock signal to the plurality of DDR [DRAM] memory devices, the logic element, and the register”	1, 15, 28, 39, 77, 82, 86, 88, 90
“the register (i) receives, from the computer system, and (ii) buffers, in response to the PLL clock signal, a plurality of row/column address signals and the bank address signals”	1, 15, 28, 77, 82, 86, 88
“transmits the buffered plurality of row/column address signals and the buffered bank address signals to the plurality of DDR memory devices”	1, 77, 82
“the [at least one] row/column address signal received by the logic element comprises [at least one/a] row address signal received by the logic element”	1, 15, 28, 39, 77, 80, 82, 86, 90
“the plurality of row[/column] address signals received by the register are separate from the [at least one] row address signal received by the logic element”	1, 15, 28, 39, 77, 80, 82, 86, 90
“generates gated column access strobe (CAS) signals or chip-select signals of the output control signals in response to at least in part to (i) the at least one row address signal, (ii) the bank address signals, and (iii) the at least one chip-select signal of the [set/plurality] of input [control] signals and (iv) the PLL clock signal.”	1, 15, 28, 39
“wherein the set of input control signals comprises a first number of chip-select signals and wherein the set of output control signals comprises a second number of chip-select signals”	3
“custom-designed semiconductor device”	6, 24, 29, 41
“two or more of the phase-lock loop device, the register, and the logic element are portions of a single component”	8, 27
“spaced from”	10, 11, 46, 47
“a direction along the [first/second] side”	11, 47
“the set of input signals configured to control a second number of DDR [memory/DRAM] devices”	15, 16, 28, 86, 88
“the set of output signals configured to control the first number of DDR [memory/DRAM] devices”	15, 16, 28, 86, 88
“the circuit further responds to a command signal and the set of input signals from the computer system by selecting one or two ranks”	15, 16, 86
“transmits the buffered plurality of row/column address signals and the buffered bank address signals to the at least one DDR [memory/DRAM] device of the selected one or two ranks of the first number of ranks”	15, 28, 86, 88
“the command signal is transmitted to only one DDR memory device at a time”	16

Term	Relevant Claim(s)
“the command signal is transmitted to two ranks of the first number of ranks at a time”	18
“the command signal is transmitted to the two ranks of the first number of ranks concurrently”	20
“the set of input signals comprises a density bit which is a row address bit”	22
“the circuit is configured to store the row address bit during an activate command for a selected bank”	22
“double-data-rate (DDR) dynamic random access memory (DRAM) devices”	28
“the circuit further responds to the set of input control signals from the computer system by selecting at least one rank of the first number of ranks”	28, 88
“the set of input control signals comprises fewer chip-select signals than does the set of output control signals”	31
“wherein the set of input control signals comprises two chip-select signals and the set of output control signals comprises four chip-select signals”	32
“wherein the input command signal is a read signal or a write signal and the output command signal is a read signal or a write signal”	38
“a first side and second side”	39
“two or more ranks which are selectable by a first number of chip-select signals”	39, 90
“integrated circuit element”	39, 90
“the at least one integrated circuit element comprising a logic element, a register, and [a] phase-lock loop device operationally coupled to the plurality of DDR memory devices, the logic element, and the register”	39, 90
“receiving a plurality of input signals from the computer system, the plurality of input signals comprising row address signals, column address signals, bank address signals, command signals, and a second number of chip-select signals less than the first number of chip-select signals”	39, 90
“the at least one integrated circuit element further responsive to the plurality of input signals by selecting at least one rank of the two or more ranks”	39, 90
“transmitting the plurality of output signals to at least one DDR memory device of the selected at least one rank”	39, 90
“the register (i) receives, from among the plurality of input signals, and (ii) buffers, in response to the PLL clock signal, the bank address signals and a plurality of the row address signals”	39, 90
transmits the buffered bank address signals and the buffered [plurality of] row address signals to the at least one DDR memory device of the selected at least one rank	39, 90

Term	Relevant Claim(s)
“the plurality of output signals corresponds to a first number of DDR memory devices arranged in the two or more ranks which are selectable by the first number of chip-select signals”	40
“the plurality of input signals corresponds to a second number of DDR memory devices arranged in ranks which are selectable by the second number of chip-select signals”	40
“simulates a virtual memory module having the second number of DDR memory devices”	40
“the at least one integrated circuit element is configured to respond to the plurality of input signals by selecting at least one rank of the two or more ranks”	50
“the plurality of DDR [memory/DRAM] devices has [at least one attribute/one or more attributes] selected from a group consisting of a number of row address bits per DDR [memory/DRAM] device, a number of column address bits per DDR [memory/DRAM] device, a number of [internal] bank[s/address bits] per DDR [memory/DRAM] device, a number of DDR [memory/DRAM] devices, a data width per DDR [memory/DRAM] device, a memory density per DDR [memory/DRAM] device, a number of ranks of DDR [memory/DRAM] devices, and a memory density per rank”	52, 62, 63, 64, 69, 73, 81
“a read-only nonvolatile memory device storing data accessible to the computer system”	52, 55
“the data characterizes the plurality of DDR memory devices as having at least one value of the at least one attribute that is different from an actual value of the at least one attribute of the plurality of DDR memory devices”	52
“the data characterizes the plurality of DDR [memory/DRAM] devices as having fewer ranks of DDR [memory/DRAM] devices than the plurality of DDR [memory/DRAM] devices actually has, and as having a greater memory density per rank than the plurality of DDR [memory/DRAM] devices actually has”	54, 65, 70, 74
“DDR dynamic random-access memory (DRAM) chip package with a bit width”	55
“the data characterizes the memory module as having fewer ranks than the first number of ranks, and as having a greater memory density per rank than the memory module actually has”	55
“means for characterizing the plurality of DDR [memory/DRAM] devices as having one or more attributes that are different from actual attributes of the plurality of DDR [memory/DRAM] devices”	56, 71, 75
“the set of input control signals corresponds to a first memory density, and the set of output control signals corresponds to a second memory density”	57
“the register comprises a plurality of register devices”	58

Term	Relevant Claim(s)
“the at least one row address signal and the bank address signals are (i) received by the logic element during an activate command operation and (ii) are used by the logic element for a subsequent read or write command operation”	60
“a read-only memory (ROM) serial-presence detect (SPD) device, the SPD device storing data accessible to the computer system”	62, 63, 64, 69, 73, 81
“the data characterizes the plurality of DDR [memory/DRAM] devices as having one or more attributes that are different from [the] one or more attributes of [the] plurality of DDR [memory/DRAM] devices”	62, 63, 64, 69, 73, 81
“the logic element responds to at least (i) a row address bit of the at least one row/column address signal, (ii) the bank signals, and (iii) the at least one chip-select signal of the set of input control signals and (iv) the PLL clock by generating a first number of chip-select signals of the set of output control signals”	77
“wherein operation of the register is responsive at least in part to clock signals received from the phase-lock loop device”	80
“the logic element generates a first number of chips-elect signals of the set of output control signals in response at least in part to clock signals received from the phase-lock loop device”	80
“a plurality of row/column address signals and the bank address signals are received from the computer system and buffered by the register, the register transmitting the buffered plurality of row/column address signals and the buffered bank address signals to the plurality of DDR memory devices”	80
“generation of the first number of chip-select signals of the output control signals by the logic element is based on the logic element responsive at least in part to (i) the at least one row address signal, (ii) the bank address signals, and (iii) the at least one chip-select signal of the set of input control signals received by the logic element and (iv) the clock signals received from the phase-lock loop device”	80
“the logic element responds to at least the at least one row address signal, the bank address signals, and the at least one chip-select signal of the set of input control signals and the PLL clock signal by generating a number of rank-selecting signals of the set of output control signals that is greater than double or equal to double the number of chip-select signals of the set of input control signals”	82
“the memory module is operable to perform successive read accesses from different ranks of DDR memory devices”	83
“the memory module is operable to perform back-to-back adjacent read commands which cross DDR memory device boundaries”	84, 87, 89, 91
“the bank address signals include bank address signals received during an activate command operation and bank address signals	85

Term	Relevant Claim(s)
received during a read or write command operation subsequent to the activate command operation”	
“and the rank-selecting signals are used for the read or write command operation”	85
“the logic element responds to at least the at least one row address signal, the bank address signals, and the at least one chip-select signal of the set of input signals and the PLL clock signal by generating a number of rank-selecting signals of the set of output signals that is greater than double or equal to double the number of chip-select signals of the set of input signals”	86
“the logic element responds to at least (i) the row address signal, (ii) the bank address signals, (iii) and the one chip-select signal of the set of input control signals and (iv) the PLL clock signal by generating a number of rank-selecting signals of the set of output signals that is greater than double or equal to double the number of chip-select signals of the set of input control signals”	88
“the logic element responds to at least (i) the at least one row signal, (ii) the bank address signals, (iii) and the second number of chip-select signals of the plurality of input signals and (iv) the PLL clock signal by generating the first number of chip-select signals of the plurality of output signals that is greater than double or equal to double the second number of chip-select signals of the plurality of input signals”	90

3. Indefiniteness Under 35 U.S.C. § 112, ¶ 6

Section 112, ¶ 6 allows a patentee to express a claim element “as a means or step for performing a specified function without the recital of structure, material, or acts in support thereof.” 35 U.S.C. § 112, ¶ 6. For such claims, the written description of the patent must disclose with sufficient particularity the corresponding structure for performing the claimed function, and it must clearly link that structure to the claimed function. *Ibormeith IP, LLC v. Mercedes-Benz USA, LLC*, 732 F.3d 1376, 1379 (Fed. Cir. 2013).

Several of the ’912 patent Asserted Claims are invalid under § 112, ¶ 6 because they contain means-plus-function terms and the ’912 patent fails to disclose with sufficient particularity the corresponding structure for performing the claimed function.

The following limitations recited in the '912 patent Asserted Claims are indefinite in whole, in part or in combination:⁷

Term	Relevant Claim(s)
“logic element”	All Asserted Claims
“means for characterizing the plurality of DDR [memory/DRAM] devices as having one or more attributes that are different from actual attributes of the plurality of DDR [memory/DRAM] devices”	56, 71, 75

B. U.S. Patent No. 9,858,215

Pursuant to Rule 3-3(d), Defendants hereby identify grounds of invalidity for the '215 Patent based on lack of written description under 35 U.S.C. § 112, first paragraph; lack of enablement under 35 U.S.C. § 112, first paragraph; indefiniteness under 35 U.S.C. § 112, second paragraph; and indefiniteness under 35 U.S.C. § 112, sixth paragraph. These contentions shall not be construed as an admission that any claim construction advanced by Defendants in this case is in any way inconsistent, flawed, or erroneous. Nor should these contentions prevent Defendants from advancing claim construction and/or non-infringement positions in lieu of, or in addition to, invalidity positions. Further, these contentions shall not be construed as an admission of or acquiescence to Plaintiff's purported construction of the claim language or of other positions advanced by Plaintiff during the course of this litigation. Defendants' invalidity contentions under 35 U.S.C. § 112 may depend, in part, on the Court's claim construction, as well as Plaintiff's alleged scope of the '215 patent Asserted Claims. Consequently, Defendants only identify the issues under 35 U.S.C. § 112 of which they are presently aware.

⁷ Listed claims also include all Asserted Claims dependent thereon, even if those claims are not individually listed.

1. Lack of Written Description and/or Enablement Under 35 U.S.C. § 112, ¶ 1

The '215 Patent does not provide sufficient written description to establish that the inventors were in possession of the alleged inventions recited in the '339 patent Asserted Claims at the time the '215 patent was filed. *Ariad Pharms., Inc. v. Eli Lilly & Co.*, 598 F.3d 1336, 1351 (Fed. Cir. 2010). In other words, the applicants did not describe their purported inventions in a manner that “reasonably conveys to those skilled in the art that the inventor had possession of the claimed subject matter as of the filing date.” *Id.* One of ordinary skill in the art would not have understood that the inventors were in possession of the full scope of the claimed apparatus and methods.

The specification of the '215 patent also does not enable one of ordinary skill in the art to make and/or use certain recited elements of the '215 patent Asserted Claims without undue experimentation. To the extent the following limitations are definite (under 35 U.S.C. § 112, ¶ 2), the application that became the '215 patent fails to sufficiently describe or enable them as required by 35 U.S.C. § 112, ¶ 1:⁸

Term	Relevant Claim(s)
“logic”	1, 8, 16, 18, 19, 20
“rank”	1, 14, 21, 26
“buffer”	1, 8, 12, 13, 14, 17, 20, 21, 26
“register”	1
“a plurality of edge connections configured to be electrically coupled to a corresponding plurality of contacts of a module slot of the computer system”	1
“a register coupled to the printed circuit board and configured to receive and buffer first command and address signals representing the first memory command, and to receive and buffer second command and address signals representing the second memory command”	1

⁸ Listed claims also include all Asserted Claims dependent thereon, even if those claims are not individually listed.

Term	Relevant Claim(s)
“wherein the first rank is selected to receive or output the first data burst in response to the first memory command and is not selected to communicate data with the memory controller in response to the second memory command, and wherein the second rank is selected to receive or output the second data burst in response to the second memory command and is not selected to communicate data with the memory controller in response to the first memory command”	1
“a buffer coupled between the at least one first memory integrated circuit and the memory bus, and between the at least one second memory integrated circuit and the memory bus”	1
“logic coupled to the buffer and configured to respond to the first memory command by providing first control signals to the buffer to enable communication of the first data burst between the at least one first memory integrated circuit and the memory controller through the buffer”	1
“wherein the logic is further configured to respond to the second memory command by providing second control signals to the buffer to enable communication of the second data burst between the at least one second memory integrated circuit and the memory controller through the buffer, the second control signals being different from the first control signals”	1
“a plurality of edge connections coupled to the memory bus”	21
“receiving at one or more circuits coupled to the printed circuit board a first set of input command and address signals representing a first memory command from the memory controller via the memory bus”	21
“generating a first set of output command and address signals in response to the first set of input command and address signals, the first set of output command and address signals selecting the first rank to receive or output the first data burst”	21
“receiving at the one or more circuits a second set of input command and address signals representing a second memory command from the memory controller via the memory bus, the second memory command to cause the memory module to receive or output a second data burst”	21
“generating a second set of output command and address signals in response to the second set of input command and address signals, the second set of output command and address signals selecting the second rank to receive or output the second data burst”	21
“in response to the first memory command, providing first control signals to a buffer to enable communication of the first data burst between the at least one first memory integrated circuit and the memory controller through the buffer;”	21
“and in response to the second memory command, providing second control signals to the buffer to enable communication of the	21

Term	Relevant Claim(s)
second data burst between the at least one second memory integrated circuit and the memory controller through the buffer, the second control signals being different from the first control signals”	
“wherein the buffer is configured to isolate both the at least one first memory integrated circuit and the at least one second memory integrated circuit from the memory bus when the memory module is not being accessed by the memory controller”	2
“wherein the memory module has an overall CAS latency greater than an actual operational CAS latency of each of the plurality of memory integrated circuits”	3
“an SPD device that reports an overall CAS latency of the memory module to the memory controller, the overall CAS latency having one more clock cycle than an actual operational CAS latency of each of the plurality of memory integrated circuits”	4
“wherein the memory module is a dual in-line memory module (DIMM), and wherein the plurality of memory integrated circuits are double-data-rate dynamic random access memory (DRAM) circuits”	5
“determining a latency value, wherein the communication of the first data burst between the at least one first memory integrated circuit and the memory controller is enabled in accordance with the latency value”	6
“wherein the memory module is further coupled to the memory controller using an on-die-termination (ODT) bus, wherein each of the plurality of memory devices includes an ODT circuit, the memory module further comprising a termination circuit external to any of the plurality of memory devices, wherein the termination circuit is coupled to the ODT bus and to the ODT circuit of at least one of the plurality of memory devices, wherein the termination circuit is configured to provide external termination of the at least one of the plurality of memory devices in response to an ODT signal on the ODT bus, and wherein the ODT circuit in the at least one of the plurality of memory devices is disabled”	7
“wherein the buffer comprises combinatorial logic, registers, and logic pipelines, and is configured to register an additional clock cycle for transferring the first data burst or the second data burst through the buffer”	8
“wherein the first memory command includes at least one first chip select signal and the second memory command includes at least one second chip select signal”	9
“wherein the memory module produces at least third and fourth chip select signals in response to the first memory command, the third chip select signal being provided to the at least one first memory integrated circuit and having an active value to cause the at least one first memory integrated circuit to receive or output data	10

Term	Relevant Claim(s)
signals in response to the first memory command, the fourth chip-select signal being provided to the at least one second memory integrated circuit and having a non-active value to keep the at least one second memory integrated circuit from receiving or outputting data signals in response to the first memory command”	
“wherein the memory module produces at least fifth and sixth chip select signals in response to the second memory command, the fifth chip select signal being provided to the at least one first memory integrated circuit and having a non-active value to keep the at least one first memory integrated circuit from receiving or outputting data signals in response to the first memory command, the sixth chip select signal being provided to the at least one second memory integrated circuit and having an active value to cause the at least one second memory integrated circuit to receive or output data signals in response to the second memory command”	11
“wherein the first memory command is a first read command and the second memory command is a second read command, wherein the first read command and the second read command are back to back adjacent read commands, and wherein the memory module outputs the first data burst together with a first burst of data strobe signals in response to the first read command, wherein memory module outputs the second data burst together with a second burst of data strobe signals in response to the second read command, wherein the second data burst follows the first data burst on the memory bus, and wherein the buffer is configured to prevent the first burst of data strobe signals and the second burst of data strobe signals from colliding with each other”	12
“wherein each of the first burst of data strobe signals and the second burst of data strobe signals includes a pre-amble interval and a post-amble interval, and wherein the buffer is configured to combine the first burst of data strobe signals and the second burst of data strobe signals into a combined burst of data strobe signals that does not include the post-amble interval of the first burst of data strobe signals and the pre-amble interval of the second burst of data strobe signals”	13
“wherein the buffer includes circuit components configurable to provide a first data path or a second data path depending on whether the first rank or the second rank is selected to communicate data with the memory controller”	14
“the at least one of the circuit components is configured to provide the first data path in response to the first control signals, and is configured to provide the second data path in response to the second control signals”	15
“wherein the logic is configured to enable the communication of the first data burst between the at least one first memory integrated	16

Term	Relevant Claim(s)
circuit and the memory controller in accordance with a latency value”	
“wherein the buffer comprises combinatorial logic, registers, and logic pipelines and is configured to register an additional clock cycle for transferring the first data burst through the buffer”	17
“wherein the logic is further configured to determine the latency value”	18
“wherein the logic is further configured to enable the communication of the second data burst between the at least one second memory integrated circuit and the memory controller in accordance with the latency value”	19
“wherein the buffer comprises combinatorial logic, registers, and logic pipelines and is configured to register an additional clock cycle for transferring the second data burst through the buffer”	20
“isolating the at least one first memory integrated circuit and the at least one second memory integrated circuit from the memory bus when the memory module is not being accessed by the memory system”	22
“wherein the first set of input command and address signals include at least one input chip-select signal, the method further comprising generating a first chip select signal and a second chip select signal in response to the first set of input command and address signals, the first chip-select signal being provided to the at least one first memory integrated circuit and having an active value to cause the at least one first memory integrated circuit to receive or output data signals in response to the first memory command, the second chip-select signal being provided to the at least one second memory integrated circuit and having a non-active value to keep the at least one second memory integrated circuit from receiving or outputting data signals in response to the first memory command”	23
“wherein the memory module has an overall CAS latency greater than an actual operational CAS latency of the memory integrated circuits”	24
“reporting an overall CAS latency of the memory module to the memory controller, the overall CAS latency having one more clock cycle than an actual operational CAS latency of the memory integrated circuits”	25
“wherein the buffer includes circuit components configurable to provide a first data path or a second data path depending on whether the first rank or the second rank is caused to communicate data with the memory controller”	26
“wherein the memory module is a dual in-line memory module (DIMM), and wherein the plurality of memory integrated circuits are double-data-rate dynamic random access memory (DRAM) circuits”	27

Term	Relevant Claim(s)
“wherein the first memory command is a first read command and the second memory command is a second read command, wherein the first read command and the second read command are back to back adjacent read commands, and wherein the memory module outputs the first data burst together with a first burst of data strobe signals in response to the first read command, wherein the memory module outputs the second data burst together with a second burst of data strobe signals in response to the second read command, wherein the second data burst follows the first data burst on the memory bus, the method further comprising combining the first burst of data strobe signals and the second burst of data strobes to form a third burst of data strobe signals on the memory bus”	28
“wherein each of the first burst of data strobe signals and the second burst of data strobe signals includes a pre-amble interval and a post-amble interval, and wherein the third burst of data strobes does not include the post-amble interval of the first burst of data strobe signals and the pre-amble interval of the second burst of data strobe signals”	29

2. Invalidity Under 35 U.S.C. § 112, ¶ 2

“[T]he second paragraph of § 112 contains two requirements: first, the claim must set forth what the applicant regards as his invention, and second, it must do so with sufficient particularity and distinctness, *i.e.*, the claim must be sufficiently definite.” *Allen Eng’g Corp. v. Bartell Indus., Inc.*, 299 F.3d 1336, 1348 (Fed. Cir. 2002) (internal quotation marks and alteration omitted). “Where it would be apparent to one of skill in the art, based on the specification, that the invention set forth in a claim is not what the patentee regarded as his invention,” the claim is “invalid under § 112, paragraph 2.” *Id.* at 1349. Several of the ’215 patent Asserted Claims are invalid because it would be apparent to one of skill in the art, based on the specification, that the invention set forth in these claims are not what the patentee regarded as his invention. *Id.* These claims are invalid under the “applicant regards” prong of § 112 at least because they contain elements that differ from and/or conflict with the ’215 patent’s written description of the invention, or because they omit elements that one of skill in

the art would understand as part of the '215 patent's invention based on the specification: 1, 2-20, 21-29.

Under § 112, ¶ 2, “a patent is invalid for indefiniteness if its claims, read in light of the specification delineating the patent, and the prosecution history, fail to inform, with reasonable certainty, those skilled in the art about the scope of the invention.” *Nautilus, Inc. v. Biosig Instruments, Inc.*, 572 U.S. 898, 901 (2014). Several of the '215 patent Asserted Claims are also invalid as indefinite under § 112, ¶ 2 because they fail to inform those skilled in the art about the scope of the invention with reasonable certainty and are indefinite.

The following limitations recited in the '215 patent Asserted Claims are indefinite in whole, in part or in combination:⁹

Term	Relevant Claim(s)
“logic”	1, 8, 16, 18, 19, 20
“a register coupled to the printed circuit board and configured to receive and buffer first command and address signals representing the first memory command, and to receive and buffer second command and address signals representing the second memory command”	1
“wherein the first rank is selected to receive or output the first data burst in response to the first memory command and is not selected to communicate data with the memory controller in response to the second memory command, and wherein the second rank is selected to receive or output the second data burst in response to the second memory command and is not selected to communicate data with the memory controller in response to the first memory command;”	1
“a buffer coupled between the at least one first memory integrated circuit and the memory bus, and between the at least one second memory integrated circuit and the memory bus”	1
“logic coupled to the buffer and configured to respond to the first memory command by providing first control signals to the buffer to enable communication of the first data burst between the at least one first memory integrated circuit and the memory controller through the buffer,”	1

⁹ Listed claims also include all Asserted Claims dependent thereon, even if those claims are not individually listed.

Term	Relevant Claim(s)
“wherein the logic is further configured to respond to the second memory command by providing second control signals to the buffer to enable communication of the second data burst between the at least one second memory integrated circuit and the memory controller through the buffer, the second control signals being different from the first control signals”	1
“receiving at one or more circuits coupled to the printed circuit board a first set of input command and address signals representing a first memory command from the memory controller via the memory bus”	21
“generating a first set of output command and address signals in response to the first set of input command and address signals, the first set of output command and address signals selecting the first rank to receive or output the first data burst;”	21
“receiving at the one or more circuits a second set of input command and address signals representing a second memory command from the memory controller via the memory bus, the second memory command to cause the memory module to receive or output a second data burst”	21
“generating a second set of output command and address signals in response to the second set of input command and address signals, the second set of output command and address signals selecting the second rank to receive or output the second data burst”	21
“in response to the first memory command, providing first control signals to a buffer to enable communication of the first data burst between the at least one first memory integrated circuit and the memory controller through the buffer”	21
“and in response to the second memory command, providing second control signals to the buffer to enable communication of the second data burst between the at least one second memory integrated circuit and the memory controller through the buffer, the second control signals being different from the first control signals”	21
“wherein the buffer is configured to isolate both the at least one first memory integrated circuit and the at least one second memory integrated circuit from the memory bus when the memory module is not being accessed by the memory controller”	2
“an SPD device that reports an overall CAS latency of the memory module to the memory controller, the overall CAS latency having one more clock cycle than an actual operational CAS latency of each of the plurality of memory integrated circuits”	4
“determining a latency value, wherein the communication of the first data burst between the at least one first memory integrated circuit and the memory controller is enabled in accordance with the latency value”	6

Term	Relevant Claim(s)
“wherein the buffer comprises combinatorial logic, registers, and logic pipelines, and is configured to register an additional clock cycle for transferring the first data burst or the second data burst through the buffer”	8
“wherein the memory module produces at least fifth and sixth chip select signals in response to the second memory command, the fifth chip select signal being provided to the at least one first memory integrated circuit and having a non-active value to keep the at least one first memory integrated circuit from receiving or outputting data signals in response to the first memory command, the sixth chip select signal being provided to the at least one second memory integrated circuit and having an active value to cause the at least one second memory integrated circuit to receive or output data signals in response to the second memory command”	11
“the at least one of the circuit components is configured to provide the first data path in response to the first control signals, and is configured to provide the second data path in response to the second control signals”	15
“wherein the logic is configured to enable the communication of the first data burst between the at least one first memory integrated circuit and the memory controller in accordance with a latency value”	16
“wherein the buffer comprises combinatorial logic, registers, and logic pipelines and is configured to register an additional clock cycle for transferring the first data burst through the buffer”	17
“wherein the logic is further configured to determine the latency value”	18
“wherein the logic is further configured to enable the communication of the second data burst between the at least one second memory integrated circuit and the memory controller in accordance with the latency value”	19
“wherein the buffer comprises combinatorial logic, registers, and logic pipelines and is configured to register an additional clock cycle for transferring the second data burst through the buffer”	20
“isolating the at least one first memory integrated circuit and the at least one second memory integrated circuit from the memory bus when the memory module is not being accessed by the memory system”	22
“wherein the memory module has an overall CAS latency greater than an actual operational CAS latency of the memory integrated circuits”	24
“wherein the buffer includes circuit components configurable to provide a first data path or a second data path depending on whether the first rank or the second rank is caused to communicate data with the memory controller”	26

Term	Relevant Claim(s)
“wherein the memory module is a dual in-line memory module (DIMM), and wherein the plurality of memory integrated circuits are double-data-rate dynamic random access memory (DRAM) circuits”	27

3. Indefiniteness Under 35 U.S.C. § 112, ¶ 6

Section 112, ¶ 6 allows a patentee to express a claim element “as a means or step for performing a specified function without the recital of structure, material, or acts in support thereof.” 35 U.S.C. § 112, ¶ 6. For such claims, the written description of the patent must disclose with sufficient particularity the corresponding structure for performing the claimed function, and it must clearly link that structure to the claimed function. *Ibormeith IP, LLC v. Mercedes-Benz USA, LLC*, 732 F.3d 1376, 1379 (Fed. Cir. 2013).

Several of the ’215 patent Asserted Claims are invalid under § 112, ¶ 6 because they contain means-plus-function terms and the ’215 patent fails to disclose with sufficient particularity the corresponding structure for performing the claimed function.

The following limitations recited in the ’215 patent Asserted Claims are indefinite in whole, in part or in combination:¹⁰

Term	Relevant Claim(s)
“logic”	1-20
“buffer”	All Asserted Claims

C. U.S. Patent No. 11,093,417

Pursuant to Rule 3-3(d), Defendants hereby identify grounds of invalidity for the ’417 Patent based on lack of written description under 35 U.S.C. § 112, first paragraph; lack of enablement under 35 U.S.C. § 112, first paragraph; indefiniteness under 35 U.S.C. § 112, second

¹⁰ Listed claims also include all Asserted Claims dependent thereon, even if those claims are not individually listed.

paragraph; and indefiniteness under 35 U.S.C. § 112, sixth paragraph. These contentions shall not be construed as an admission that any claim construction advanced by Defendants in this case is in any way inconsistent, flawed, or erroneous. Nor should these contentions prevent Defendants from advancing claim construction and/or non-infringement positions in lieu of, or in addition to, invalidity positions. Further, these contentions shall not be construed as an admission of or acquiescence to Plaintiff's purported construction of the claim language or of other positions advanced by Plaintiff during the course of this litigation. Defendants' invalidity contentions under 35 U.S.C. § 112 may depend, in part, on the Court's claim construction, as well as Plaintiff's alleged scope of the '417 patent Asserted Claims. Consequently, Defendants only identify the issues under 35 U.S.C. § 112 of which they are presently aware.

1. Lack of Written Description and/or Enablement Under 35 U.S.C. § 112, ¶ 1

The '417 patent does not provide sufficient written description to establish that the inventors were in possession of the alleged inventions recited in the '417 patent Asserted Claims at the time the '417 patent was filed. *Ariad Pharms., Inc. v. Eli Lilly & Co.*, 598 F.3d 1336, 1351 (Fed. Cir. 2010). In other words, the applicants did not describe their purported inventions in a manner that "reasonably conveys to those skilled in the art that the inventor had possession of the claimed subject matter as of the filing date." *Id.* One of ordinary skill in the art would not have understood that the inventors were in possession of the full scope of the claimed apparatus and methods.

The specification of the '417 patent also does not enable one of ordinary skill in the art to make and/or use certain recited elements of the '417 patent Asserted Claims without undue experimentation. To the extent the following limitations are definite (under 35 U.S.C. § 112,

¶ 2), the application that became the '417 patent fails to sufficiently describe or enable them as required by 35 U.S.C. § 112, ¶ 1:¹¹

Term	Relevant Claim(s)
“logic”	1, 6, 7,
“circuitry”	1, 2, 3, 6, 11, 12, 13, 15
“a printed circuit board having a plurality of edge connections configured to be electrically coupled to a corresponding plurality of contacts of a module slot of the computer system;”	1
“logic coupled to the printed circuit board and configurable to receive a set of input address and control signals associated with a read or write memory command via the address and control signal lines and to output a set of registered address and control signals in response to the set of input address and control signals,”	1
“the set of input address and control signals including a plurality of input chip select signals and other input address and control signals,”	1
“the plurality of input chip select signals including one chip select signal having an active signal value and one or more other input chip select signals each having a non-active signal value,”	1
“the set of registered address and control signals including a plurality of registered chip select signals corresponding to respective ones of the plurality of input chip select signals and other registered address and control signals corresponding to respective ones of the other input address and control signals,”	1
“the plurality of registered chip select signals including one registered chip select signal having an active signal value and one or more other registered chip select signals each having a non-active signal value,”	1
“wherein the logic is further configurable to output data buffer control signals in response to the read or write memory command;”	1
“wherein the plurality of N-bit wide ranks correspond to respective ones of the plurality of registered chip select signals such that each of the plurality of registered chip select signals is received by memory devices one respective N-bit wide rank of the plurality of N-bit-wide ranks,”	1
“wherein one of the plurality of N-bit wide ranks including memory devices receiving the registered chip select signal having the active signal value and the other registered address and control signals is configured to receive or output a burst of N-bit wide data signals in response to the read or write command;”	1

¹¹ Listed claims also include all Asserted Claims dependent thereon, even if those claims are not individually listed.

Term	Relevant Claim(s)
“circuitry coupled between the data signal lines in the N-bit wide memory bus and corresponding data pins of memory devices in each of the plurality of N-bit wide ranks, the circuitry being configurable to transfer the burst of N-bit wide data signals between the N-bit wide memory bus and the memory devices in the one of the plurality of N-bit wide ranks in response to the data buffer control signals and in accordance with an overall CAS latency of the memory module;”	1
“wherein data transfers through the circuitry are registered for an amount of time delay such that the overall CAS latency of the memory module is greater than an actual operational CAS latency of each of the memory devices.”	1
“wherein each of the memory devices has a corresponding load, and the circuitry is configured to isolate the loads of the memory devices from the memory bus.”	2
“wherein the burst of N-bit wide data signals includes a set of consecutively transmitted data bits for each data signal line in the memory bus, and wherein the set of consecutively transmitted data bits are successively transferred through the circuitry in response to the data buffer control signals.”	3
“wherein each of the memory devices is 4-bits wide, and wherein each of the plurality of ranks is 64-bits or 72-bits wide and includes 16 or 18 memory devices configured in pairs.”	4
“wherein the memory devices are organized in four ranks and the set of input address and control signals include four chip select signals, one for each of the four ranks.”	5
“wherein the circuitry includes logic pipelines configurable to enable the data transfers between the memory devices and the memory bus through the circuitry.”	6
“wherein the logic is further configured to report the overall CAS latency to the memory controller in response to a mode register set command received from the memory controller.”	7
“wherein the memory module has a specified data rate, and wherein the burst of N-bit wide data signals are transferred between the one of the plurality of N-bit wide ranks and the memory controller at the specified data rate.”	8
“further comprising a phase locked loop clock driver configured to output a clock signal in response to one or more signals received from the memory controller, wherein the predetermined amount of time delay is at least one clock cycle time delay.”	9
“wherein the memory devices are dynamic random access memory devices configured to operate synchronously with the clock signal, and wherein each memory device in the one of the plurality of N-bit wide ranks is configured to receive or output a respective set of	10

Term	Relevant Claim(s)
bits of the burst of N-bit wide data signals on both edges of each of a respective set of data strobes.”	
“wherein the circuitry includes data paths, and wherein the circuitry is configurable to enable the data paths in response to the data buffer control signals so that the burst of N-bit wide data signals are transferred via the data paths.”	11
“wherein the data paths are disabled when no data signals associated with any memory command are being transferred through the circuitry.”	12
“wherein each of the memory devices has a corresponding load, and the circuitry is configured to isolate the loads of the memory devices from the memory bus.”	13
“wherein the memory module has a specified data rate, and wherein the burst of N-bit wide data signals are transferred through the data paths at the specified data rate.”	14
“wherein the read or write command is a write memory command, wherein the burst of N-bit wide data signals include a respective series of write data bits received by the circuitry from a respective one of the data signal lines, and wherein the respective series of write data bits are successively transferred via a respective one of the data paths.”	15

2. Invalidity Under 35 U.S.C. § 112, ¶ 2

“[T]he second paragraph of § 112 contains two requirements: first, the claim must set forth what the applicant regards as his invention, and second, it must do so with sufficient particularity and distinctness, *i.e.*, the claim must be sufficiently definite.” *Allen Eng’g Corp. v. Bartell Indus., Inc.*, 299 F.3d 1336, 1348 (Fed. Cir. 2002) (internal quotation marks and alteration omitted). “Where it would be apparent to one of skill in the art, based on the specification, that the invention set forth in a claim is not what the patentee regarded as his invention,” the claim is “invalid under § 112, paragraph 2.” *Id.* at 1349. Several of the ’417 patent Asserted Claims are invalid because it would be apparent to one of skill in the art, based on the specification, that the invention set forth in these claims are not what the patentee regarded as his invention. *Id.* These claims are invalid under the “applicant regards” prong of

§ 112 at least because they contain elements that differ from and/or conflict with the '417 patent's written description of the invention, or because they omit elements that one of skill in the art would understand as part of the '417 patent's invention based on the specification: 1, 2-20, 21-29.

Under § 112, ¶ 2, “a patent is invalid for indefiniteness if its claims, read in light of the specification delineating the patent, and the prosecution history, fail to inform, with reasonable certainty, those skilled in the art about the scope of the invention.” *Nautilus, Inc. v. Biosig Instruments, Inc.*, 572 U.S. 898, 901 (2014). Several of the '417 patent Asserted Claims are also invalid as indefinite under § 112, ¶ 2 because they fail to inform those skilled in the art about the scope of the invention with reasonable certainty and are indefinite.

The following limitations recited in the '417 patent Asserted Claims are indefinite in whole, in part or in combination:¹²

Term	Relevant Claim(s)
“logic”	1, 6, 7,
“circuitry”	1, 2, 3, 6, 11, 12, 13, 15
“logic coupled to the printed circuit board and configurable to receive a set of input address and control signals associated with a read or write memory command via the address and control signal lines and to output a set of registered address and control signals in response to the set of input address and control signals,”	1
“the set of input address and control signals including a plurality of input chip select signals and other input address and control signals,”	1
“the plurality of input chip select signals including one chip select signal having an active signal value and one or more other input chip select signals each having a non-active signal value,”	1
“the set of registered address and control signals including a plurality of registered chip select signals corresponding to respective ones of the plurality of input chip select signals and other registered address and control signals corresponding to respective ones of the other input address and control signals,”	1

¹² Listed claims also include all Asserted Claims dependent thereon, even if those claims are not individually listed.

Term	Relevant Claim(s)
“the plurality of registered chip select signals including one registered chip select signal having an active signal value and one or more other registered chip select signals each having a non-active signal value,”	1
“wherein the plurality of N-bit wide ranks correspond to respective ones of the plurality of registered chip select signals such that each of the plurality of registered chip select signals is received by memory devices one respective N-bit wide rank of the plurality of N-bit-wide ranks,”	1
“wherein one of the plurality of N-bit wide ranks including memory devices receiving the registered chip select signal having the active signal value and the other registered address and control signals is configured to receive or output a burst of N-bit wide data signals in response to the read or write command;”	1
“circuitry coupled between the data signal lines in the N-bit wide memory bus and corresponding data pins of memory devices in each of the plurality of N-bit wide ranks, the circuitry being configurable to transfer the burst of N-bit wide data signals between the N-bit wide memory bus and the memory devices in the one of the plurality of N-bit wide ranks in response to the data buffer control signals and in accordance with an overall CAS latency of the memory module;”	1
“wherein data transfers through the circuitry are registered for an amount of time delay such that the overall CAS latency of the memory module is greater than an actual operational CAS latency of each of the memory devices.”	1
“wherein the burst of N-bit wide data signals includes a set of consecutively transmitted data bits for each data signal line in the memory bus, and wherein the set of consecutively transmitted data bits are successively transferred through the circuitry in response to the data buffer control signals.”	3
“wherein the circuitry includes logic pipelines configurable to enable the data transfers between the memory devices and the memory bus through the circuitry.”	6
“wherein the logic is further configured to report the overall CAS latency to the memory controller in response to a mode register set command received from the memory controller.”	7
“further comprising a phase locked loop clock driver configured to output a clock signal in response to one or more signals received from the memory controller, wherein the predetermined amount of time delay is at least one clock cycle time delay.”	9
“wherein the circuitry includes data paths, and wherein the circuitry is configurable to enable the data paths in response to the data buffer control signals so that the burst of N-bit wide data signals are transferred via the data paths.”	11

Term	Relevant Claim(s)
“wherein the data paths are disabled when no data signals associated with any memory command are being transferred through the circuitry.”	12
“wherein each of the memory devices has a corresponding load, and the circuitry is configured to isolate the loads of the memory devices from the memory bus.”	13
“wherein the read or write command is a write memory command, wherein the burst of N-bit wide data signals include a respective series of write data bits received by the circuitry from a respective one of the data signal lines, and wherein the respective series of write data bits are successively transferred via a respective one of the data paths.”	15

3. Indefiniteness Under 35 U.S.C. § 112, ¶ 6

Section 112, ¶ 6 allows a patentee to express a claim element “as a means or step for performing a specified function without the recital of structure, material, or acts in support thereof.” 35 U.S.C. § 112, ¶ 6. For such claims, the written description of the patent must disclose with sufficient particularity the corresponding structure for performing the claimed function, and it must clearly link that structure to the claimed function. *Ibormeith IP, LLC v. Mercedes-Benz USA, LLC*, 732 F.3d 1376, 1379 (Fed. Cir. 2013).

Several of the ’417 patent Asserted Claims are invalid under § 112, ¶ 6 because they contain means-plus-function terms and the ’417 patent fails to disclose with sufficient particularity the corresponding structure for performing the claimed function.

The following limitations recited in the ’417 patent Asserted Claims are indefinite in whole, in part or in combination:¹³

Term	Relevant Claim(s)
”logic”	1, 6, 7
”circuitry”	1, 2, 3, 6, 11, 12, 13, 15

¹³ Listed claims also include all Asserted Claims dependent thereon, even if those claims are not individually listed.

VII. Priority Date for U.S. Patent No. 7,619,912

Plaintiff is not entitled a priority date any earlier than July 1, 2005, the date that its parent application no. 11/173,175 (now U.S. Pat. No. 7,289,386) was filed.

As explained in the petition associated with IPR2022-00615, neither the '668 provisional (filed 3/5/04), the '595 provisional (filed 7/15/04), nor the '244 provisional (filed 7/15/04) provide support for the full scope of claim 16 of the '912 Patent. For example, the '668 and '595 provisionals do not disclose the claimed “logic element” or that such a “logic element” receives “at least one row/column address signal, bank address signals, and at least one chip-select signal,” as required by claim 16. The '244 provisional is the first priority application disclosing an ASIC Decoder, which could be a “logic element,” but there is no disclosure it receives any “bank address” signals as required by Asserted Claims, confirming that the applicants, at that time, did not have possession of every requirement of the Asserted Claims.

A POSITA would have understood that the next priority application for the '912 Patent, the '436 Patent (filed 3/7/05)— which does not reference the '244 provisional — also fails to provide the necessary support for the Asserted Claims of the 912 Patent, e.g., by lacking any embodiment including “a circuit” comprising “a logic element” and “a register” as required by the Asserted Claims and shown in Figure 1A of the 912 Patent (40 and 60, respectively), and by lacking any Verilog code showing the use of “row” and/or “bank address signals” (like EXAMPLEs 1 and 2 in the '912 Patent). The Verilog code was only added 7/1/05 as part of the continuation-in-part.

Furthermore, the subject matter added by the '386 Patent (filed 7/1/05 as a continuation-in-part of the '436 Patent) includes recognition of the problem of “back-to-back adjacent read commands which cross memory device boundaries” causing a “collision” window when “the last

data strobe of memory device ‘a’ collides with the pre-amble time interval of the data strobe of memory device ‘b’...”

A POSITA would have understood that such a “collision” would cause signal errors and potentially destroy the drivers in the memory devices. A POSITA would have understood from the ’386 Patent that the disclosures in the earlier applications would not have worked in normal operation because their disclosures failed to address these collisions during read operations, making the memory module unusable as a practical matter. Indeed, a POSITA would have known that back-to-back read commands were part of the JEDEC standards, and thus part of the normal operation of memory modules at the time.

The earlier ’436 Patent does not describe how to avoid collisions in this situation. Thus, a memory module made following the disclosure of the ’436 Patent and/or the prior provisional applications would fail — and even possibly “burn” the drivers of the memory devices— during standard back-to-back read operations.

The portions of the ’912 Patent added July 1, 2005, disclose for the first time in this priority chain a solution to the previously-described problems: during back-to-back read operations, “collisions are avoided by a mechanism which electrically isolates the DQS data strobe signal lines 104 of the memory devices from one another...” Because the Asserted Claims do not exclude back-to-back adjacent read commands, so the description added in the July 1, 2005 application was necessary to support and/or enable the full scope of the claim.

VIII. Priority Date for U.S. Patent Nos. 9,858,215 and 11,093,417

Plaintiff is not entitled to a priority date any earlier than July 1, 2005 because the ’215 and ’417 patents’ claims lack §112 support from any application filed before July 1, 2005, the date the continuation-in-part application no. 11/173,175 (now U.S. Pat. No. 7,289,386) was filed.

As explained in the petitions associated with IPR2023-00454 and IPR2023-00455, neither the '668 provisional (filed 3/5/04), the '595 provisional (filed 5/28/04), the '244 provisional (filed 7/15/04), the '038 provisional (filed 7/21/04), nor the '087 provisional (filed 1/19/05) provide §112 support for the full scope of the claims of the '215 and '417 patents.

With respect to the '215 patent, the priority applications prior to July 1, 2005 do not provide written description support for, among other things, “provid[ing] [first/second] control signals to the **buffer** to enable communication of the [first/second] data burst between the at least one [first/second] memory integrated circuit and the memory controller through the **buffer**.” Independent claims 1 and 21 (and thus all claims) require these limitations, and no application filed prior to July 1, 2005 provided §112 support for them. Of the five provisional applications and the one non-provisional application filed prior to July 1, 2005, only one provisional application (U.S. Provisional Application No. 60/645,087 (“087 Provisional”) discloses a “Buffer” (RBDL) through which data (DQ0-DQ63) is communicated. But the 087 Provisional fails to disclose different first/second control signals to the buffer for enabling the communication of data bursts through the buffer in response to memory commands. The 087 Provisional does not mention any “data burst” or “control signals,” much less the specific control signals required by the claims. *Id.* The 087 Provisional also does not name all the inventors listed on the '215 Patent.

Further, although the 087 Provisional refers to “a data path multiplexer/demultiplexer” that provides separate DQ/DQS paths for each rank, it fails to disclose how the multiplexer/demultiplexer specifically enables data bursts through the data buffer in response to memory commands, what its control signals are, and how those control signals differ for the first/second memory commands. A POSITA would have recognized that the buffer need not use

different first/second control signals, even if the second memory commands are directed to different ranks, because, for example, the data could be sent to both of the ranks, and a chip-select signal (e.g., rcs0#, rcs1#) could be used to target one of those ranks. A POSITA would have also recognized that data transfer through the buffer does not necessarily happen in response to memory commands as required by the '215 patent claims and instead could be controlled by other means, such as the “preamble” on the DQS strobe lines. Thus, Plaintiff and the claims of the '215 patent are not entitled to a priority date before July 1, 2005.

With respect to the '417 patent, the priority applications prior to July 1, 2005 do not provide written description support for, among other things, “logic...configurable to output data buffer control signals in response to the read or write memory command” and “circuitry coupled between the data signal lines in the N-bit wide memory bus and corresponding data pins of memory devices in each of the plurality of N-bit wide ranks, the circuitry being configurable to transfer the burst of N-bit wide data signals between the N-bit wide memory bus and the memory devices in the one of the plurality of N-bit wide ranks in response to the data buffer control signals [.]” Independent claim 1 (and thus every claim) requires these limitations, and no application filed prior to July 1, 2005 provided §112 support for them. Of the five provisional applications and the one non-provisional application filed prior to July 1, 2005, only one provisional application (U.S. Provisional Application No. 60/645,087 (“087 Provisional”)) discloses any circuitry or “Buffer” (RBDL) through which data (DQ0-DQ63) is communicated. But the 087 Provisional fails to disclose data buffer control signals for enabling the transfer of data bursts through the buffer in response to read or write memory commands. The 087 Provisional does not mention any “burst of N-bit wide data signals” or “control signals,” much

less the specific “data buffer control signals” required by the claims. The 087 Provisional also does not name all the inventors listed on the 417 Patent.

Further, although the 087 Provisional refers to “a data path multiplexer/demultiplexer” that provides separate DQ/DQS paths for each rank, it fails to disclose how the multiplexer/demultiplexer specifically transfers data bursts through the data buffer in response to read or write memory commands or what its control signals are. A POSITA would have recognized that the buffer (or “circuitry”) need not use “data buffer control signals” to direct a data burst to one of the ranks, even if a memory write command is directed to that one rank, because, for example, the data could be sent to both of the ranks, and a chip-select signal (e.g., rcs0#, rcs1#) could be used to target one of those ranks. A POSITA would have also recognized that data transfer through the buffer does not necessarily happen in response to memory commands as required by the ’417 patent claims and instead could be controlled by other means, such as the “preamble” on the DQS strobe lines. Thus, Plaintiff and the claims of the ’417 patent are not entitled to a priority date before July 1, 2005.

IX. P. R. 3-4 – Productions

Pursuant to P.R. 3-4(a), each Defendant is concurrently producing and/or making available for inspection documents and other materials sufficient to show the operation of any aspects or elements of the Accused Products identified by Plaintiff in its P.R. 3-1(c) charts.

Additionally, and pursuant to P.R. 3-4(b), Defendants are concurrently producing a copy of each item of prior art identified herein. These prior art references and corroborating evidence are cited in attached invalidity claim charts in Appendices A-C. Defendants will also make available for inspection any prior art systems or devices upon request to the extent Defendants acquire such systems or devices. For example, a sample of a Micron MT36VDDF12872

product, which constitutes a prior art system, is available for inspection in the Atlanta, Georgia office of Fish & Richardson, P.C. References that were cited during prosecution of the Asserted Patents may not be contained in Defendants' production as they are not required to be under the local patent rules. Defendants' search for prior art references, additional documentation, and/or corroborating evidence concerning prior art systems and devices is ongoing. Accordingly, Defendants reserve the right to supplement their production as Defendants obtain additional prior art references, documentation, and/or corroborating evidence concerning invalidity during the course of discovery.

Defendants reserve the right to supplement their P. R. 3-4 document production pursuant to the Patent Local Rules and the orders of the Court.

Date: April 13, 2023

Respectfully submitted,

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CERTIFICATE OF SERVICE

I hereby certify that a true and correct copy of the foregoing document was filed electronically in compliance with Local Rule CV-5 on April 13, 2023. As of this date, all counsel of record have consented to electronic service and are being served with a copy of this document through the Court's CM/ECF system under Local Rule CV-5(a)(3)(A).

/s/ Daniel A. Tishman