

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.,

Petitioner,

v.

NETLIST, INC.,

Patent Owner

IPR2023-00455

Patent 9,858,215

**PETITIONER'S AUTHORIZED
REPLY TO PATENT OWNER'S PRELIMINARY RESPONSE**

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1001	U.S. Patent No. 9,858,215 (issued January 2, 2018)
1002	File History of U.S. Patent No. 9,858,215 (filed May 18, 2015)
1003	Declaration of Dr. Andrew Wolfe
1004	Curriculum Vitae of Dr. Andrew Wolfe
1005	U.S. Provisional Application No. 60/645,087 (filed Jan. 19, 2005)
1006	U.S. Provisional Application No. 60/588,244 (filed July 15, 2004)
1007	U.S. Provisional Application No. 60/550,668 (filed March 5, 2004)
1008	U.S. Provisional Application No. 60/575,595 (filed May 28, 2004)
1009	U.S. Provisional Application No. 60/590,038 (filed July 21, 2004)
1010	File History of U.S. Patent No. 7,286,436 (filed March 7, 2005)
1011	U.S. Patent No. 7,286,436 (issued Oct. 23, 2007)
1012	U.S. Patent No. 7,289,386 (issued Oct. 30, 2007)
1013	Affirmance of the Examiner's Decision on Reexamination of '386 Patent (Feb. 25, 2015)
1014	Reexamination Certificate for '386 Patent (Aug. 19, 2016)
1015	U.S. Patent No. 7,619,912 (issued Nov. 17, 2009)
1016	Decision on Reexamination of '912 Patent (June 6, 2016); Decision Under 37 C.F.R. § 41.77(f) (July 27, 2018); and Decision on Rehearing (Jan. 31, 2019)
1017	Reexamination Certificate for '912 Patent (Feb. 8, 2021)
1018	Petition for <i>Inter Partes</i> Review of U.S. Patent No. 7,619,912 (Feb. 17, 2022)

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1019	Patent Owner Preliminary Response to Petition for <i>Inter Partes</i> Review of U.S. Patent No. 7,619,912 (July 21, 2022)
1020	Declaration of Michael C. Brogioli, Ph.D. in Support of Patent Owner Preliminary Response to Petition for <i>Inter Partes</i> Review of U.S. Patent No. 7,619,912 (July 21, 2022)
1021	Reply to Patent Owner Preliminary Response to Petition for <i>Inter Partes</i> Review of U.S. Patent No. 7,619,912 (Aug. 26, 2022)
1022	Sur-Reply to Patent Owner Preliminary Response to Petition for <i>Inter Partes</i> Review of U.S. Patent No. 7,619,912 (Sept. 9, 2022)
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1026	U.S. Patent No. 7,864,627 (issued Jan. 4, 2011)
1027	Decision on Appeal of Reexamination of '627 Patent (May 30, 2016); Decision Under 37 C.F.R. § 41.77(f) (May 31, 2018)
1028	Reexamination Certificate for '627 Patent (Nov. 5, 2018)
1029	U.S. Patent No. 8,756,364 (issued June 17, 2014)
1030	IPR2017-00549 Final Written Decision ('364 Patent) (May 3, 2018)
1031	IPR Certificate for '364 Patent (May 26, 2020)
1032	U.S. Patent No. 7,532,537 (issued May 12, 2009)
1033	IPR2017-00667 Final Written Decision ('537 Patent) (July 18, 2018)

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1034	IPR2017-00668 Final Written Decision ('537 Patent) (July 18, 2018)
1035	IPR Certificate for '537 Patent (Apr. 27, 2020)
1036	U.S. Patent No. 7,636,274 (issued Dec. 22, 2009)
1037	Decision on Appeal of Reexamination of '274 Patent (May 9, 2017)
1038	Reexamination Certificate for '274 Patent (Nov. 5, 2018)
1039	U.S. Patent No. 7,881,150 (issued Feb. 1, 2011)
1040	IPR2014-00882 Final Written Decision on Remand ('150 Patent) (March 29, 2018)
1041	IPR2014-01011 Final Written Decision on Remand ('150 Patent) (March 29, 2018)
1042	IPR2015-01020 Final Written Decision ('150 Patent) (Sept. 28, 2016)
1043	IPR Certificate for '150 Patent (Mar. 6, 2019)
1044	File History of U.S. Patent No. 7,916,574 (filed Nov. 29, 2010)
1045	U.S. Patent No. 7,916,574 (issued Mar. 29, 2011)
1046	U.S. Patent No. 8,081,536 (issued Dec. 20, 2011)
1047	IPR2014-00883 Final Written Decision on Remand ('536 Patent) (March 29, 2018)
1048	IPR2015-01021 Final Written Decision ('536 Patent) (Sept. 28, 2016)
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1050	File History of U.S. Patent No. 8,516,188 (filed Nov. 1, 2011)
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1052	File History of U.S. Patent No. 9,037,774 (filed Aug. 20, 2013)
1053	U.S. Patent No. 9,037,774 (issued May 19, 2015)
1054	File History of U.S. Patent No. 10,489,314 (filed Dec. 28, 2017)
1055	U.S. Patent No. 10,489,314 (issued Nov. 26, 2019)
1056	Decisions Granting Institution of <i>Inter Partes</i> Reviews of U.S. Patent No. 10,489,314 (Nov. 1, 2022)
1057	File History of U.S. Patent No. 11,093,417 (filed Nov. 25, 2019)
1058	U.S. Patent No. 11,093,417 (issued Aug. 17, 2021)
1059	File History of U.S. Patent Application No. 17/403,832 (filed Aug. 16, 2021)
1060	JEDEC JESD79 standard for DDR SDRAM (June 2000)
1061	[intentionally omitted]
1062	JEDEC JESD21-C design specification for DDR SDRAM Registered DIMM (January 2002)
1063	[intentionally omitted]
1064	JEDEC JESD79-2 standard for DDR2 SDRAM (Sept. 2003)
1065	Declaration of Julie Carlson (JESD79-2)
1066	JEDEC JESD21-C design specification for DDR2 SDRAM Registered DIMM, Rev. 3.2 (Oct. 4, 2005)
1067	[intentionally omitted]
1068	Harold S. Stone, <u>Microcomputer Interfacing</u> (1982)
1069	Bruce Jacob, <i>Synchronous DRAM Architectures, Organizations, and Alternative Technologies</i> (Dec. 10, 2002)

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1070	Bruce Jacob et al., <u>Memory Systems: Cache, DRAM, Disk</u> (2008)
1071	U.S. Patent No. 7,363,422 to <u>Perego</u> et al. (filed Jan. 28, 2004)
1072	U.S. Patent No. 7,155,627 to <u>Matsui</u> (filed Aug. 22, 2003)
1073	U.S. Patent Application Publication No. 2006/0277355 to <u>Ellsberry</u> et al. (filed June 1, 2005)
1074	IPR2018-00362 Final Written Decision (June 27, 2019) ('907 Patent)
1075	U.S. Patent No. 9,606,907 (all claims cancelled)
1076	Decision Granting Institution of <i>Inter Partes</i> Review of U.S. Patent No. 10,949,339 (Oct. 19, 2022) (child of U.S. Patent No. 9,606,907, Exhibit 1075)
1077	U.S. Patent Application Publication No. 2002/0112119 to <u>Halbert</u> et al. (published Aug. 15, 2002)
1078	U.S. Patent No. 7,024,518 to <u>Halbert</u> et al. (filed Mar. 13, 2002)
1079	U.S. Patent Application Publication No. 2006/0117152 to <u>Amidi</u> et al. (filed Jan. 5, 2004)
1080	U.S. Patent No. 8,250,295 to <u>Amidi</u> et al. (filed Jan. 5, 2004)
1081	U.S. Patent. No. 5,513,135 to <u>Dell</u> et al. (issued Apr. 30, 1996)
1082	U.S. Patent Application Publication No. 2003/0039151 to <u>Matsui</u> (published Feb. 27, 2003)
1083	[intentionally omitted]
1084	[intentionally omitted]
1085	Amended Complaint in <i>Netlist, Inc. v. Samsung Electronics Co., Ltd. et al.</i> , No. 2:22-cv-00293 (E.D. Tex. filed Aug. 15, 2022)
1086	Waiver of Service in <i>Netlist, Inc. v. Samsung Electronics Co., Ltd. et al.</i> , No. 2:22-cv-00293 (E.D. Tex. filed Aug. 31, 2022)

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1087	[intentionally omitted]
1088	Amended Complaint in <i>Netlist, Inc. v. Micron Technology, Inc. et al.</i> , No. 2:22-cv-00294 (E.D. Tex. filed Aug. 15, 2022)
1089	Micron’s Answer in <i>Netlist, Inc. v. Micron Technology, Inc. et al.</i> , No. 2:22-cv-00294 (E.D. Tex. filed Sept. 7, 2022)
1090	[intentionally omitted]
1091	<i>Interim Procedure for Discretionary Denials in AIA Post-Grant Proceedings with Parallel District Court Litigation</i> (June 21, 2022)
1092	Federal Court Management Statistics (Mar. 31, 2022), available at < https://www.uscourts.gov/statistics/table/na/federal-court-management-statistics/2022/03/31-1 >
1093	Email from counsel for Samsung to counsel for Patent Owner re: stipulation not to pursue certain invalidity defenses if an IPR proceeding is instituted
1094	U.S. Patent & Trademark Office, <i>Changes Under Consideration to Discretionary Institution Practices, Petition Word-Count Limits, and Settlement Practices for America Invents Act Trial Proceedings Before the Patent Trial and Appeal Board</i> , 88 Fed. Reg. 24,503 (Apr. 21, 2023)

CLAIM LISTING

Ref. #	Listing of Challenged Claims
1.a.1	1. A memory module
1.a.2	operable in a computer system to communicate data with a memory controller of the computer system via a memory bus in response to memory commands received from the memory controller,
1.a.3	the memory commands including a first memory command and a subsequent second memory command, the first memory command to cause the memory module to receive or output a first data burst and the second memory command to cause the memory module to receive or output a second data burst,
1.a.4	the memory module comprising:
1.b	a printed circuit board having a plurality of edge connections configured to be electrically coupled to a corresponding plurality of contacts of a module slot of the computer system;
1.c	a register coupled to the printed circuit board and configured to receive and buffer first command and address signals representing the first memory command, and to receive and buffer second command and address signals representing the second memory command;
1.d.1	a plurality of memory integrated circuits mounted on the printed circuit board and arranged in a plurality of ranks including a first rank and a second rank, the plurality of memory integrated circuits including at least one first memory integrated circuit in the first rank and at least one second memory integrated circuit in the second rank,
1.d.2	wherein the first rank is selected to receive or output the first data burst in response to the first memory command and is not selected to communicate data with the memory controller in response to the second memory command, and
1.d.3	wherein the second rank is selected to receive or output the second data burst in response to the second memory command and is not selected to communicate data with the memory controller in response to the first memory command;
1.e	a buffer coupled between the at least one first memory integrated circuit and the memory bus, and between the at least one second memory integrated circuit and the memory bus; and

Ref. #	Listing of Challenged Claims
1.f.1	logic coupled to the buffer and configured to respond to the first memory command by providing first control signals to the buffer to enable communication of the first data bust between the at least one first memory integrated circuit and the memory controller through the buffer,
1.f.2	wherein the logic is further configured to respond to the second memory command by providing second control signals to the buffer to enable communication of the second data burst between the at least one second memory integrated circuit and the memory controller through the buffer, the second control signals being different from the first control signals.
2	The memory module of claim 1, wherein the buffer is configured to isolate both the at least one first memory integrated circuit and the at least one second memory integrated circuit from the memory bus when the memory module is not being accessed by the memory controller.
3	The memory module of claim 1, wherein the memory module has an overall CAS latency greater than an actual operational CAS latency of each of the plurality of memory integrated circuits.
4	The memory module of claim 1, further comprising an SPD device that reports an overall CAS latency of the memory module to the memory controller, the overall CAS latency having one more clock cycle than an actual operational CAS latency of each of the plurality of memory integrated circuits.
5	The memory module of claim 1, wherein the memory module is a dual in-line memory module (DIMM), and wherein the plurality of memory integrated circuits are double-data-rate dynamic random access memory (DRAM) circuits.
6	The memory module of claim 1, further comprising determining a latency value, wherein the communication of the first data burst between the at least one first memory integrated circuit and the memory controller is enabled in accordance with the latency value.

Ref. #	Listing of Challenged Claims
7	The memory module of claim 1, wherein the memory module is further coupled to the memory controller using an on-die-termination (ODT) bus, wherein each of the plurality of memory devices includes an ODT circuit, the memory module further comprising a termination circuit external to any of the plurality of memory devices, wherein the termination circuit is coupled to the ODT bus and to the ODT circuit of at least one of the plurality of memory devices, wherein the termination circuit is configured to provide external termination of the at least one of the plurality of memory devices in response to an ODT signal on the ODT bus, and wherein the ODT circuit in the at least one of the plurality of memory devices is disabled.
8	The memory module of claim 1, wherein the buffer comprises combinatorial logic, registers, and logic pipelines, and is configured to register an additional clock cycle for transferring the first data burst or the second data burst through the buffer.
9	The memory module of claim 1, wherein the first memory command includes at least one first chip select signal and the second memory command includes at least one second chip select signal.
10	The memory module of claim 9, wherein the memory module produces at least third and fourth chip select signals in response to the first memory command, the third chip select signal being provided to the at least one first memory integrated circuit and having an active value to cause the at least one first memory integrated circuit to receive or output data signals in response to the first memory command, the fourth chip-select signal being provided to the at least one second memory integrated circuit and having a non-active value to keep the at least one second memory integrated circuit from receiving or outputting data signals in response to the first memory command.

Ref. #	Listing of Challenged Claims
11	The memory module of claim 10, wherein the memory module produces at least fifth and sixth chip select signals in response to the second memory command, the fifth chip select signal being provided to the at least one first memory integrated circuit and having a non-active value to keep the at least one first memory integrated circuit from receiving or outputting data signals in response to the first [sic: second] memory command, the sixth chip select signal being provided to the at least one second memory integrated circuit and having an active value to cause the at least one second memory integrated circuit to receive or output data signals in response to the second memory command.
12	The memory module of claim 1, wherein the first memory command is a first read command and the second memory command is a second read command, wherein the first read command and the second read command are back to back adjacent read commands, and wherein the memory module outputs the first data burst together with a first burst of data strobe signals in response to the first read command, wherein memory module outputs the second data burst together with a second burst of data strobe signals in response to the second read command, wherein the second data burst follows the first data burst on the memory bus, and wherein the buffer is configured to prevent the first burst of data strobe signals and the second burst of data strobe signals from colliding with each other.
13	The memory module of claim 12, wherein each of the first burst of data strobe signals and the second burst of data strobe signals includes a pre-amble interval and a post-amble interval, and wherein the buffer is configured to combine the first burst of data strobe signals into a combined burst of data strobe signals that does not include the post-amble interval of the first burst of data strobe signals and the pre-amble interval of the second burst of data strobe signals.
14	The memory module of claim 1, wherein the buffer includes circuit components configurable to provide a first data path or a second data path depending on whether the first rank or the second rank is selected to communicate data with the memory controller.
15	The memory module of claim 14, the at least one of the circuit components is configured to provide the first data path in response to the first control signals, and is configured to provide the second data path in response to the second control signals.

Ref. #	Listing of Challenged Claims
16	The memory module of claim 1, wherein the logic is configured to enable the communication of the first data burst between the at least one first memory integrated circuit and the memory controller in accordance with a latency value.
17	The memory module of claim 16, wherein the buffer comprises combinatorial logic, registers, and logic pipelines and is configured to register an additional clock cycle for transferring the first data burst through the buffer.
18	The memory module of claim 16, wherein the logic is further configured to determine the latency value.
19	The memory module of claim 16, wherein the logic is further configured to enable the communication of the second data burst between the at least one second memory integrated circuit and the memory controller in accordance with the latency value.
20	The memory module of claim 19, wherein the buffer comprises combinatorial logic, registers, and logic pipelines and is configured to register an additional clock cycle for transferring the second data burst through the buffer.
21.a	A method of operating a memory module coupled to a memory controller via a memory bus, the memory module comprising memory integrated circuits arranged in ranks and mounted on a printed circuit board having a plurality of edge connections coupled to the memory bus, the memory integrated circuits including at least one first memory integrated circuits including at least one second memory integrated circuit in a second rank, the method comprising:
21.b	receiving at one or more circuits coupled to the printed circuit board a first set of input command and address signals representing a first memory command from the memory controller via the memory bus, the first memory command to cause the memory module to receive or output a first data burst;
21.c	generating a first set of output command and address signals in response to the first set of input command and address signals, the first set of output command and address signals selecting the first rank to receive or output the first data burst;

Ref. #	Listing of Challenged Claims
21.d	receiving at the one or more circuits a second set of input command and address signals representing a second memory command from the memory controller via the memory bus, the second memory command to cause the memory module to receive or output a second data burst;
21.e	generating a second set of output command and address signals in response to the second set of input command and address signals, the second set of output command and address signals selecting the second rank to receive or output the second data burst;
21.f	in response to the first memory command, providing first control signals to a buffer to enable communication of the first data burst between the at least one first memory integrated circuit and the memory controller through the buffer; and
21.g	in response to the second memory command, providing second control signals to the buffer to enable communication of the second data burst between the at least one second memory integrated circuit and the memory controller through the buffer, the second control signals being different from the first control signals.
22	The method of claim 21, further comprising isolating the at least one first memory integrated circuit and the at least one first memory integrated circuit and the at least one second memory integrated circuit from the memory bus when the memory module is not being accessed by the memory system.
23	The method of claim 21, wherein the first set of input command and address signals include at least one input chip-select signal, the method further comprising generating a first chip select signal and a second chip select signal in response to the first set of input command and address signals, the first chip-select signal being provided to the at least one first memory integrated circuit and having an active value to cause the at least one first memory integrated circuit to receive or output data signals in response to the first memory command, the second chip-select signal being provided to the at least one second memory integrated circuit and having a non-active value to keep the at least one second memory integrated circuit from receiving or outputting data signals in response to the first memory command.

Ref. #	Listing of Challenged Claims
24	The method of claim 21, wherein the memory module has an overall CAS latency greater than an actual operational CAS latency of the memory integrated circuits.
25	The method of claim 21, further comprising reporting an overall CAS latency of the memory module to the memory controller, the overall CAS latency having one more clock cycle than an actual operational CAS latency of the memory integrated circuits.
26	The method of claim 21, wherein the buffer includes circuit components configurable to provide a first data path or a second data path depending on whether the first rank or the second rank is caused to communicate data with the memory controller.
27	The method of claim 21, wherein the memory module is a dual in-line memory module (DIMM), and wherein the plurality of memory integrated circuits are double-data-rate dynamic random access memory (DRAM) circuits.
28	The method of claim 21, wherein the first memory command is a first read command and the second memory command is a second read command, wherein the first read command and the second read command are back to back adjacent read commands, and wherein the memory module outputs the first data burst together with a first burst of data strobe signals in response to the first read command, wherein the memory module outputs the second data burst together with a second burst of data strobe signals in response to the second read command, wherein the second data burst follows the first data burst on the memory bus, the method further comprising combining the first burst of data strobe signals and the second burst of data strobes to form a third burst of data strobe signals on the memory bus.
29	The method of claim 28, wherein each of the first burst of data strobe signals and the second burst of data strobe signals includes a pre-amble interval and a post-amble interval, and wherein the third burst of data strobes does not include the post-amble interval of the first burst of data strobe signals and the pre-amble interval of the second burst of data strobe signals.

1. Discretionary denial under *Fintiv* (POPR 53–56)

Petitioner has provided a *Sotera* stipulation, *see* EX1093, mooted *Fintiv* under the Director’s *Interim Procedure*. *See* EX1091, p.3 & n.3, p.7; *Samsung Elecs. Co. v. Netlist, Inc.*, IPR2022-01427, Paper 13, at 6–7 (PTAB Apr. 12, 2023).

2. Discretionary denial under § 325(d) (POPR 49–53)

Under Part 1 of *Advanced Bionics*, Netlist does not dispute that JESD79-2 (part of each Ground) was not cited. Instead, Netlist argues that JESD79-2 “is also the same as art presented to the office” because, citing the Petition, a “POSITA would have been familiar with these JEDEC standards” and Ellsberry “expressly incorporates by reference” JEDEC standards, including JESD79-2. POPR 52. That is insufficient, because there is no evidence of record to suggest that the Examiner considered the portions of JESD79-2 relied on in the Petition, much less “the same *arguments*” for the combinations asserted here. *Wolfspeed, Inc. v. Trs. of Purdue Univ.*, IPR2022-00761, Paper 13, at 8 (PTAB Mar. 30, 2023) (Director). With respect to Perego, Ellsberry, and Halbert, these references (or family members) were submitted with ***hundreds*** of others. Pet. 135. Netlist does not dispute that the claims were never expressly distinguished over those references. Pet. 135–36; EX1003, ¶¶112–16. And the USPTO’s recent proposed rulemaking agrees that “mere citation of a reference” in an IDS is ***not*** “sufficient” for denial under §325(d). EX1094, pp.24511–12.

Under Part 2 of *Advanced Bionics*, the Examiner clearly erred by allowing the claims. “[I]f the record of the Office’s previous consideration of the art is not well developed or silent, then a petitioner may show the Office erred by overlooking something persuasive.” *Advanced Bionics*, IPR2019-01469, Paper 6, at 10. That is the case here. Netlist argues that the references were considered because the Examiner discussed “Applicant cited prior art in IDS.” POPR 51. But the record does not include any indication of which, of the hundreds cited, were actually discussed and no elaboration is provided.

Netlist’s argument that “none of the references in the Petition render the challenged claims obvious,” POPR 53, is incorrect. **First**, for example, Netlist argues that Ground 1 (Perego+JESD79-2) does not teach “ranks” of memory devices (POPR 19–30). There is no record of the Examiner agreeing with this argument, which is clearly wrong. The Board previously found, in the Institution Decision for the related ’912 Patent, that Perego renders obvious “ranks.” EX1023, 41–42. Netlist argues (POPR 21–22) that Perego at 15:37–:45 does not disclose ranks or chip-select signals, citing a snippet of Dr. Wolfe’s testimony, but Dr. Wolfe actually testified that this portion of Perego teaches using both the incoming chip-select signal **and** address signal to select the rank as part of “rank multiplication,” e.g., EX2003, 82:14–83:14, 204:12–:21; Pet. 10–12, 54–62, 79–80; EX1003, ¶¶171–174, 319. Netlist also points to Figure 5F (POPR 21), but the

Petition does not rely on that Figure for “ranks.” Pet. 71–72 (Figure 5E shows two ranks, green and blue). Netlist’s remaining arguments (POPR 23–30), including that Perego is limited to “Rambus” memory (POPR 24–28), ignore that Perego teaches that the invention can use “DDR2” memory devices (which require chip-select signals for selecting a “rank”). EX1071, 10:58; Pet. 32–35, 54–62.

Second, Netlist argues Perego uses “address” information rather than “control” information. POPR 30–33. Again, there is no record of the Examiner agreeing with this argument, which is clearly wrong. As noted above, Perego at 15:37–:45 refers to rank multiplication, which uses incoming chip-select signals to generates additional chip-select signals (control signals) to enable communication with the targeted rank; the address information alone does not target the rank. EX2003, 82:14–83:14, 204:12–:21; Pet. 10–12, 79–80. Indeed, “all DRAMs...are connected to the same address” signals, EX1069, 3, which is why control signals (such as chip-select signals) are needed to “route data” to the targeted rank, Pet. 79–80. Netlist argues the “first and second control signals [c]ould be the same,” POPR 32, but the Petition explains they would be different to “activate only the channel transferring the data burst...[to] the targeted rank,” Pet. 77–80.

Third, Netlist argues the Perego does not disclose a “rank” and thus there would be no motivation to combine with Ellsberry. POPR 36–42. Again, there is no record of the Examiner agreeing with this argument, which is clearly wrong.

As discussed above (pp.2–3), Perego teaches “ranks,” and thus is compatible with Ellsberry’s teachings. Pet. 112–16. Netlist also argues Ellsberry does not teach an overall CAS latency of the memory module greater than the CAS latency of each memory device, POPR 42–44, but the Petition explains why that was obvious in light of the JEDEC standard teaching adding an extra clock cycle so that the buffer has enough time to perform its functions, Pet. 81–82, 119–20. Netlist argues Ellsberry does not teach “cross-the-rank back-to-back read operations,” POPR 44, but that is incorrect because Ellsberry and Perego both teach “rank multiplication,” Pet. 114–15, meaning that two memory devices in different ranks must act like a single memory device in one (“virtual”) rank, resulting in what Netlist refers to as cross-the-rank back-to-back read operations, Pet. 103–04, 124–25.

Fourth, Netlist’s argument that Perego and Ellsberry would not be combined because Perego has a centralized buffer, while Ellsberry has distributed buffers, POPR 38–42, is incorrect because these were known alternatives, Pet. 115–16, and both references teach complying with the JEDEC standards and implementing “rank multiplication,” providing a motivation to combine, *id.*

Dated: June 16, 2023

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CERTIFICATE OF COMPLIANCE

I hereby certify that this **Petitioner's Authorized Reply to Patent Owner's Preliminary Response**, excluding the parts of the brief exempted by 37 C.F.R. § 42.24, complies with the page limits provided by the Board in Exhibit 3001 (June 8, 2023), which stated: "Petitioner may file by June 16, 2023, a four-page reply limited to addressing issues 1 and 4."

Dated: June 16, 2023

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CERTIFICATE OF SERVICE

Pursuant to 37 C.F.R. § 42.6(e), I certify that on this 16th day of June, 2023,

Petitioner's Authorized Reply to Patent Owner's Preliminary Response was served by email on the following counsel for Patent Owner:

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