

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.,
Petitioner,

v.

NETLIST, INC.,
Patent Owner.

Case No. IPR2023-00455
Patent No. 9,858,215

PATENT OWNER'S PRE-INSTITUTION SUR-REPLY

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EXHIBIT LIST

Exhibit No.	Document
EX2001	Crisp, R., “Direct Rambus Technology: The New Main Memory Standard,” <i>IEEE Micro</i> , pp. 18-28 (1997)
EX2002	Datasheet for Samsung’s RIMM MR16R1624 (Wolfe Deposition Exhibit 2100)
EX2003	Deposition Transcript of Dr. Andrew Wolfe from IPR2022-00615
EX2004	Samsung datasheet on Rambus Direct RDRAM (Dec. 2001)
EX2005	Deposition Transcript of SungJoo Park in <i>Netlist, Inc. v. Samsung Electronics Co., Ltd.</i> , 2:21-cv-00463-JRG (E.D. Tex. November 23, 2022) (excerpt)
EX2006	Ex. 7 to Park Depo
EX2007	<i>Frequently Asked Questions</i> , What is the difference between a "bank" and a "rank?", Micron, https://web.archive.org/web/20141231144416/https://www.micron.com/support/faqs (last accessed Mar. 7, 2023).
EX2008	Reserved
EX2009	“XDR Architecture “ by Rambus (last modified December 2005), downloaded from https://web.archive.org/web/20110724044154/http://www.rambus.com/assets/documents/products/dl_0161_v0_8.pdf
EX2010	IDT, “DDR4 LRDIMMs Unprecedented Memory Bandwidth on Samsung DDR4 LRDIMM Enabled by IDT’s Register and Data Buffer,” downloaded from https://www.renesas.com/us/en/document/whp/ddr4-lrdimms-both-memory-capacity-and-speed

EX2011	“HyperCloud HCDIMM: Scaling the High Density Memory Cliff,” July 14, 2012, downloaded from https://web.archive.org/web/20120915083048/http://www.netlist.com/media/blog/hypercloud-memory-scaling-the-high-density-memory-cliff/
EX2012	<i>What is a Memory Rank</i> , Crucial: Micron, https://www.crucial.com/support/articles-faq-memory/what-is-a-memory-rank (last accessed Mar. 7, 2023)
EX2013	<i>Lecture 15: DRAM Main Memory Systems</i> , University of Utah, https://my.eng.utah.edu/~cs6810/pres/11-6810-15.pdf
EX2114	“Configuring and using DDR3 memory with HP ProLiant Gen8 Servers: Best Practice Guidelines for ProLiant Servers with Intel Xeon Processors” by HP, downloaded from https://web.archive.org/web/20121023195754/http://h20000.www2.hp.com/bc/docs/support/SupportManual/c03293145/c03293145.pdf
EX2015	Ganesh, B. et al., <i>Fully-Buffered DIMM Memory Architectures: Understanding Mechanisms, Overheads and Scaling</i> , HPCA (2007)
EX2116	Datasheet for Micron DDR2 SDRAM FBDIMM MT36HTF51272FD
EX2017	U.S. Patent No. 7,356,639 (“Perego-639”)
EX2018	Redline Comparison of EX1035 (U.S. Patent No. 7,363,422 to Perego) With Related U.S. Patent No. 7,356,639
EX2019	US District Court – Judicial Caseload Profile (as of December 31, 2022)
EX2020	JESD79-2B
EX2021	Amended Docket Control Order in <i>Netlist, Inc. v. Samsung Electronics Co. Ltd.</i> , 2:22-cv-00293-JRG (E.D. Tex. Feb. 1, 2023)

EX2022	Cover pleading of Samsung's invalidity contentions in <i>Netlist, Inc. v. Samsung Electronics Co. Ltd.</i> , 2:22-cv-00293-JRG (E.D. Tex. April 13, 2023)
EX2023	IPR2023-00203, Paper 8.

I. Discretionary Denial Under § 325(d) is Warranted

Advanced Bionics Prong I: The Petition relies on JESD79-2 for the “specific ways to issue read and write commands to DDR2 memory devices.” Pet. 32-33. Petitioner contends that the examiner did not consider the relevant portion of JESD79-2, even though Ellsberry—which was before the examiner—“expressly incorporates by reference the corresponding JEDEC standards, including JESD79-2[.]” Reply 1; Pet. 114. Moreover, how DDR2 issue commands are described in *e.g.*, the Jacob paper, (EX1069, 2-4 & 9-11), which was also considered by the examiner, (*see* EX1001, p. 4, right column (Jacob, 2002 paper); EX1002, p.298 (item #10, *i.e.*, EX1069, “Considered” by examiner). That is, the examiner indeed considered the relevant part of JESD79-2, including as they are used in the Petition.

Petitioner does not dispute that Perego, Ellsberry and Halbert were before the examiner, that the examiner conducted searches based on those specific references, and discussed “Applicant cited prior art in IDS” with applicant to reach agreement on patentability. POPR, 51. Petitioner argues, however, discretionary denial is not warranted under the proposed rulemaking because the references were submitted with many other references and not expressly discussed. Reply 1. The (controversial) proposed rulemaking is not in force, and does not govern the proceeding. Instead, the binding precedential *Advanced Bionics* holds that “[p]reviously presented art includes art provided to the Office by an applicant, such as the on an Information

Disclosure Statement (IDS), in the prosecution history of the challenged patent.”
Advanced Bionics, 7-8.

Advanced Bionics Prong II: Petitioner acknowledges that it needs to show “the Office erred by overlooking something persuasive.” Reply 2. The Reply fails to do so, arguing only how its treatment of the art differs from Netlist’s. Reply 2-4. That is insufficient under *Advanced Bionics*, 7-9.

For instance, Petitioner incorrectly argues that the Board has found Perego discloses or renders obvious “rank.” Reply 2. In IPR2022-00615, because of the RPI issue, the POPR only had space to explore one reason why Perego does not disclose “ranks.” In IPR2023-00203, when Netlist provided additional reasoning, the Board declined to reach the merits for the Perego-based grounds. EX2023, Paper 8, 13.

And contrary to Petitioner’s assertion (Reply 2), Dr. Wolfe did not testify that chip-select signals were used together with address signals in Perego to select a rank. EX2003, 82:14-83:14, 204:12-21. Instead, he testified that address bits could be used as chip-selects (*id.*, 81:5-82:13), and that he “do[es] not think” Perego, 15:37-45 “specifies how ranks are selected or enabled.” *Id.*, 202:8-204:10. Concerning Figures 5F and 5E of Perego, the POPR discusses why neither supports Petitioner’s theory. See POPR 21-22. Petitioner further mischaracterizes POPR 24-28: those explain why Perego’s memory modules and buffers do not receive the recited chip-select signal, regardless whether Perego used DDR2 or Rambus memory devices.

Petitioner also disagrees with Netlist's argument on POPR 30-33, pointing again to Perego 15:37-45. Reply 3. But as its own expert testified, that paragraph has nothing to do with selecting or enabling ranks, let alone with rank multiplication. EX2003, 202:8-204:10; *contra* EX1001, 37:38-45 (claims requiring selecting specific ranks). Petitioner ignores that testimony and makes no effort to explain how that testimony squares with its theory or indicates the examiner overlooked something material. Indeed, Perego does not even mention the word "rank," let alone rank multiplication. Petitioner also cannot deny that Perego, 15:37-45 mentions only address information, not chip-select or other control information. POPR 30-31.

Petitioner then suggests that because in a JEDEC-style memory system, "all DRAMs ... are connected to the same address," (EX1069, 3), Perego has to use chip-select signals. Reply 3; EX1069, 2 ("the chip-select bus [] is *essential in a JEDEC-style* memory system"). But nothing in Perego indicates that Perego utilizes a JEDEC-style DIMM in which all DRAMs are connected to the same address; nor has Petitioner pointed to such disclosures. POPR, 36-37; Reply 3; Pet. 79-80. Furthermore, because Perego selects different channels using address information, not control information, (Perego, 15:37-45), Perego does not disclose first and second control signals being different, as explained on POPR 30-33.

Petitioner does not dispute Netlist's arguments concerning Halbert. Regarding combinability of Perego and Ellsberry, Petitioner does not dispute that even if

Perego involved a rank (it does not), Perego already has a way to specify a particular channel and there is no need to look to Ellsberry for that. POPR 37. Petitioner also insists that centralized buffer and distributed buffers are alternatives, but does not dispute the literature that contrasts those architecture and notes their significant differences. POPR 38-42; Reply 4. Indeed, the Board rejected such simplification in IPR2022-00063 FWD when it rejected Samsung's argument that a POSITA would have distributed components in a centralized buffer to distributed buffers.

These, as well as Petitioner's disagreement with Netlist's interpretation of Ellsberry's teaching on CAS latency and JESD79-2, Figure 27, are no more than "disagree[ment] regarding the purported treatment of the art or arguments." *Advanced Bionics*, 8-9. Such agreements do not evidence any material errors made by the examiner. *Id.* As such, 325(d) applies and discretionary denial is appropriate.

II. *Sotera* Stipulation does not moot *Fintiv* analysis.

Petitioner has attempted to evade *Sotera* stipulation in the district court by relying primarily on the asserted IPR references, but sprinkling references to APA, knowledge of POSITAs or system art. The Board should only consider a *Sotera* stipulation if Petitioner is willing to state explicitly which grounds it will pursue in the district court so the Board can evaluate the overlap between the two proceedings.

Dated: June 26, 2023

Respectfully submitted,
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CERTIFICATE OF SERVICE

I hereby certify, pursuant to 37 C.F.R. section 42.6, that on June 26, 2023, a complete copy of the **PATENT OWNER'S PRE-INSTITUTION SUR-REPLY** and **EXHIBIT 2023** were served upon the following, by ELECTRONIC MAIL:

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