RAMBUS

Direct Rambus™ RIMM™ Module Specification Version 1.0

Netlist EX2027
Samsung v Netlist
IPR2023-00455

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Chapter

1 Introduction

1.1 Introduction

This specification defines the electrical and mechanical requirements for 184 pin, 2.5 volt, 600 or 800 MHz, 16-bit and 18-bit, Direct RDRAM RIMM memory modules. A principal use of these RIMM modules is for main memory when installed on personal computer motherboards.

These requirements support interchangeable modules of 1 to 16 RDRAM devices to be used in Rambus Channel. Direct Rambus Channel supports up to three RIMM modules.

1.1.1 RIMM Configurations Supported

RIMM modules can support 1 to 16 Direct RDRAM devices per module. The basic design of the RIMM should not preclude the ability to design any capacity RIMM. However, there are several configuration that should be most popular:

1) Maximum capacity: 16 RDRAM RIMM modules are available for maximum capacity systems.

2) Typical module configurations: 4, 6, 8, and 16 using 64Mb/72Mb RDRAM devices (32MB, 48MB, 64MB, and 128MB) will most likely be the minimum memory size to be shipped with any PC as base memory.

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Chapter 2 Specifications

2.1 Environmental

The RIMM module must operate within a personal computer cabinet in an office or home environment.

2.1.1 Temperature and Humidity Limits

The environmental parameters for both storage and operating conditions are listed in Table 2-1.

Table 2-1: RIMM Module Temperature, Humidity and Barometric Pressure Requirements

Environmental Condition	Limit
Ambient Operating Temperature (Ta)	Application dependent, 0 °C to +55 °C typically
Operating Humidity	10% to 90% relative humidity
Storage Temperature	-50 °C to +100 °C
Storage Humidity	5% to 95% without condensation
Barometric Pressure (operating & storage)	105K - 69K Pascal (up to 3000 meters)

2.1.2 Safety

The RIMM module printed wiring board is to have a flammability rating of 94V-O. Markings should include UL tractability requirements per *UL Recognized Component Directory.*

2.2 Mechanical Design

2.2.1 Dimensions and Tolerances

The module is a multi-layer PC board. PC board thickness is 1.27 ± 0.10mm (0.050 ± 0.004 in) measured at the contact pads. Maximum warpage is 1% (0.01 mm per mm).

The board manufacturer must maintain 28 Ω ± 10% impedance for the loaded and unloaded sections of all RSL signal traces on the module. In addition, the board manufacturer should maintain the impedance of the two high speed CMOS signals (SCK and CMD) to 28 Ω ± 10% for the loaded sections and 28 Ω ± 15% for the unloaded sections.

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2.2.2 Module Drawing

Figure 2-1 shows the RIMM module PCB outline. The maximum module height is 35.0 mm.

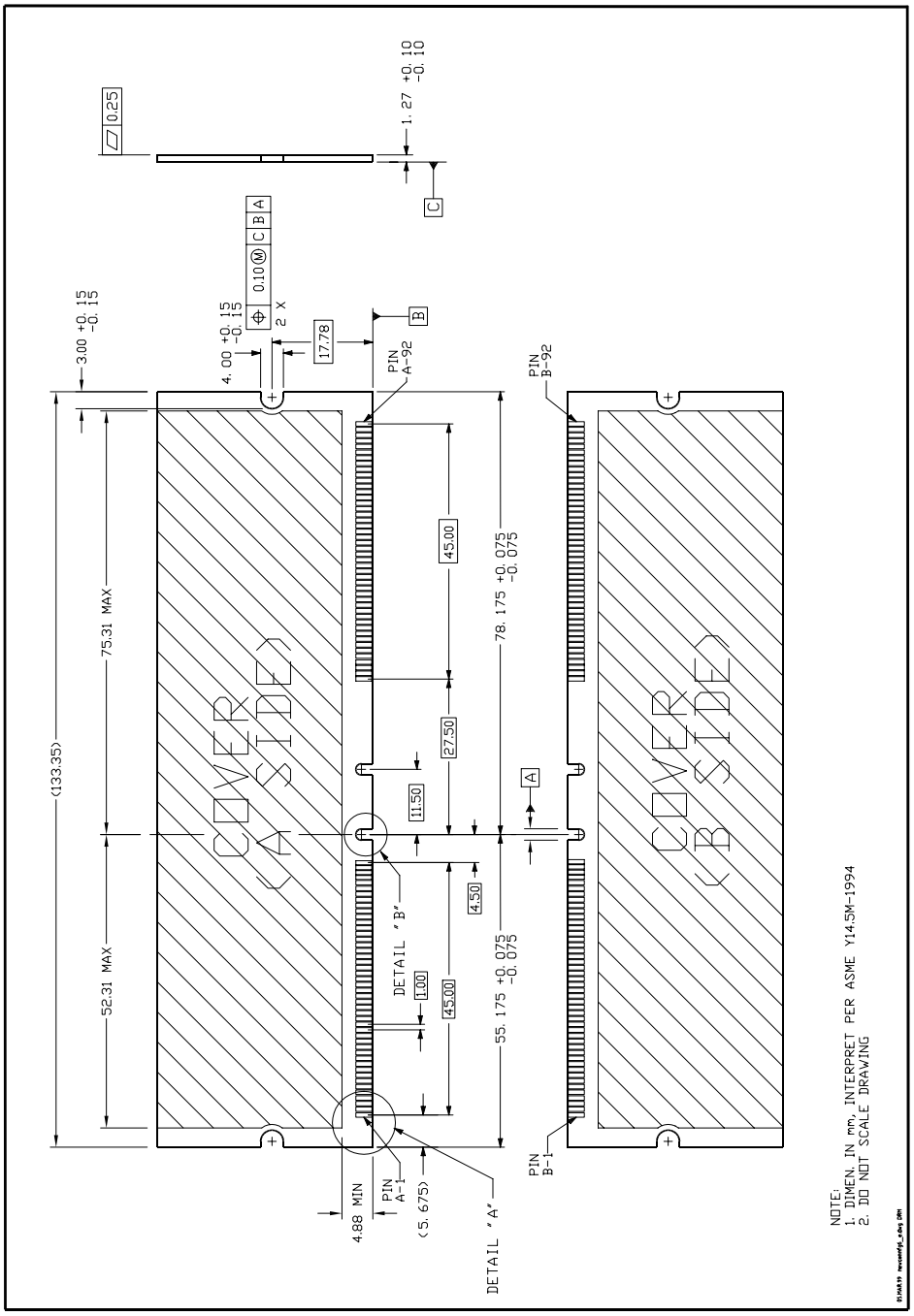

Figure 2-1: RIMM Module Mechanical Drawing 1

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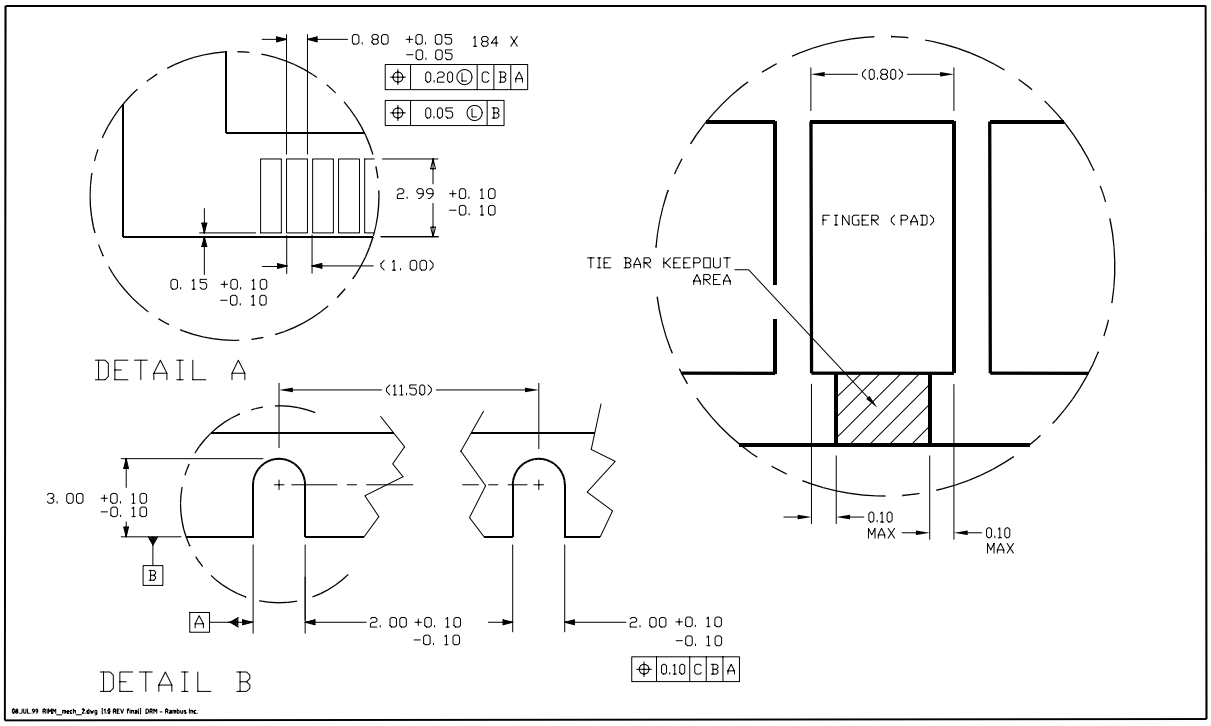

Figure 2-2: RIMM Module Mechanical Drawing 2

The contact region must be clear of solder mask. PCB designers should avoid placing additional vias in this region.

2.2.3 Weight

Weight = 45 grams, maximum.

Center of gravity specifications: a maximum of 35 mm from the bottom edge of the RIMM module.

2.2.4 Plating

Contact pad thicknesses are 0.75 microns (30 micro-inches) gold over a minimum of 2 microns (80 micro-inches) nickel.

2.2.5 Contact Requirement

Leading edge of contact pads specified as the keep out zone must be free of burrs and external tie bars (see Figure 2-2). The tie bar must be offset from the center line.

2.2.6 Keying

The RIMM module will be keyed for insertion orientation, safety, and configuration. To allow for future expansions, there are three possible keying options in the RIMM module designs. The left key which is indicated as DATUM A is fixed, but the center key can be moved 1.0 mm or 2.0 mm to the right. The default is option A as shown in Figure .

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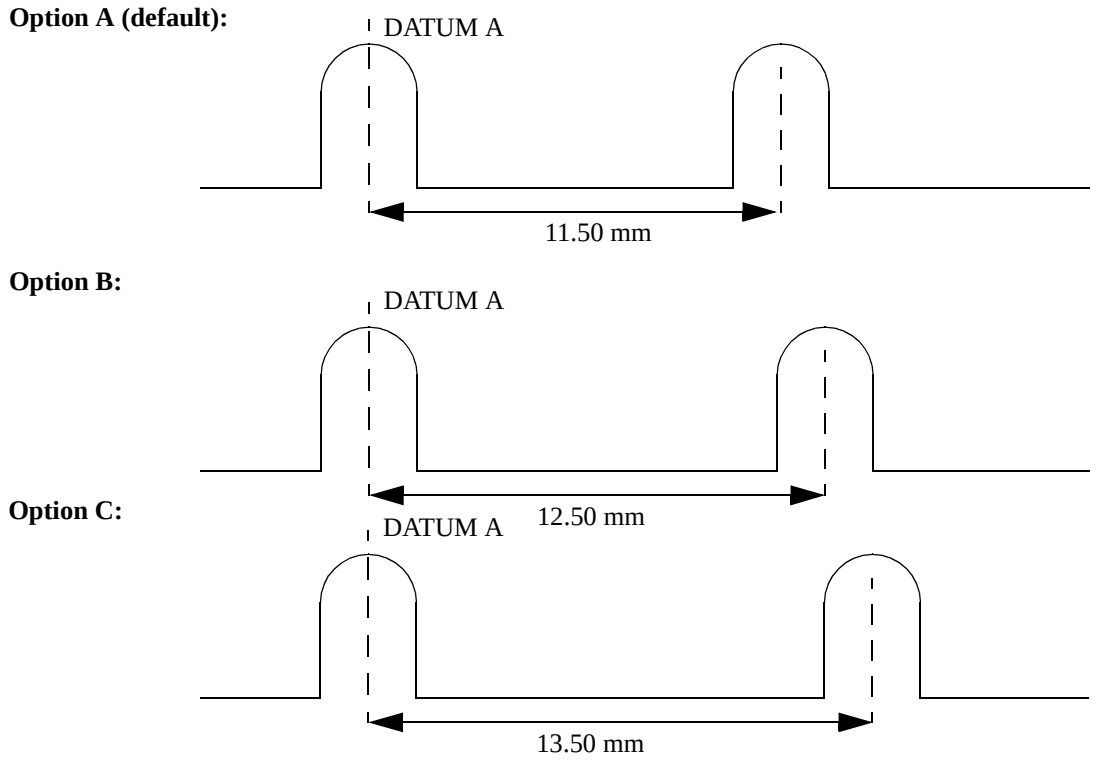

Figure 2-3: Module Keying

The following table describes a few possible options:

Table 2-2: Keying Options

Option	Connector Key	Module Key	Module Description
1	A	A	V_{DD}=2.5V
2	B	B	TBD
3	C	C	TBD

2.3 Reliability Requirement

TBD.

2.4 RIMM Module Validation Requirement

See RIMM Module Validation Specification.

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2.5 Module Pinout

2.5.1 Signal Types

Table 2-3 summarizes the types of signals used in the RIMM module. In the table, RSL stands for Rambus Signaling Levels.

Table 2-3: Device Signal Level Summary

Pin Type	Levels	IO	Polarity
Clock	RSL	I	Active low
Data	RSL	IO	Active low
Request	RSL	I	Active low
Serial	CMOS	I, IO[a]	Active high
Power	Gnd, V_{DD}, V_{REF}, V_{CMOS}	Power	DC voltages

a. SCK and CMD are input only. SIN and SOUT are input/output.

For simplicity, the following definitions are used:

- ClockFromMaster (CFM), ClockToMaster (CTM) and their complements, CFMN and CTMN, are described as Clock.
- Bi-directional DQA[8:0] and DQB[8:0] data signals are collectively referred to as Data. DQ is a synonym for Data.
- Uni-directional ROW[2:0] and COL[4:0] request signals are simply referred to as Request. RQ is a synonym for Request.
- CMOS SCK, CMD, and SIN and SOUT control signals are collectively called Serial.

The RIMM module pinout has the prefixes (Lxxx or Rxxx) for all signals to distinguish the locations of the signals relative to pin A1. Signals with Lxxx prefix (left side of the module) is closer to pin A1, and signals with Rxxx prefix (right side of the module) is closer to pin A92.

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Table 2-4: Module Pinout

Pin	Pin Name	Pin	Pin Name
A1	Gnd	B1	Gnd
A2	LDQA8	B2	LDQA7
A3	Gnd	B3	Gnd
A4	LDQA6	B4	LDQA5
A5	Gnd	B5	Gnd
A6	LDQA4	B6	LDQA3
A7	Gnd	B7	Gnd
A8	LDQA2	B8	LDQA1
A9	Gnd	B9	Gnd
A10	LDQA0	B10	LCFM
A11	Gnd	B11	Gnd
A12	LCTMN	B12	LCFMN
A13	Gnd	B13	Gnd
A14	LCTM	B14	RSRV1 (NC)
A15	Gnd	B15	Gnd
A16	RSRV2 (NC)	B16	LROW2
A17	Gnd	B17	Gnd
A18	LROW1	B18	LROW0
A19	Gnd	B19	Gnd
A20	LCOL4	B20	LCOL3
A21	Gnd	B21	Gnd
A22	LCOL2	B22	LCOL1
A23	Gnd	B23	Gnd
A24	LCOL0	B24	LDQB0
A25	Gnd	B25	Gnd
A26	LDQB1	B26	LDQB2
A27	Gnd	B27	Gnd
A28	LDQB3	B28	LDQB4
A29	Gnd	B29	Gnd
A30	LDQB5	B30	LDQB6
A31	Gnd	B31	Gnd
A32	LDQB7	B32	LDQB8
A33	Gnd	B33	Gnd
A34	LSCK	B34	LCMD
A35	Vcmos	B35	Vcmos
A36	SOUT	B36	SIN
A37	Vcmos	B37	Vcmos
A38	RSRV3 (NC)	B38	RSRV4 (NC)
A39	Gnd	B39	Gnd
A40	RSRV5 (NC)	B40	RSRV6 (NC)
A41	Vdd	B41	Vdd
A42	Vdd	B42	Vdd
A43	RSRV9-(NC)	B43	RSRV10-(NC)
A44	RSRV11-(NC)	B44	RSRV12-(NC)
A45	RSRV13-(NC)	B45	RSRV14-(NC)
A46	RSRV15-(NC)	B46	RSRV16-(NC)

Pin	Pin Name	Pin	Pin Name
A47	RSRV17-(NC)	B47	RSR18V-(NC)
A48	RSRV19-(NC)	B48	RSRV20-(NC)
A49	RSRV21-(NC)	B49	RSRV22-(NC)
A50	RSRV23-(NC)	B50	RSRV24-(NC)
A51	Vref	B51	Vref
A52	Gnd	B52	Gnd
A53	SCL	B53	SA0
A54	Vdd	B54	Vdd
A55	SDA	B55	SA1
A56	SVdd	B56	SVdd
A57	SWP	B57	SA2
A58	Vdd	B58	Vdd
A59	RSCK	B59	RCMD
A60	Gnd	B60	Gnd
A61	RDQB7	B61	RDQB8
A62	Gnd	B62	Gnd
A63	RDQB5	B63	RDQB6
A64	Gnd	B64	Gnd
A65	RDQB3	B65	RDQB4
A66	Gnd	B66	Gnd
A67	RDQB1	B67	RDQB2
A68	Gnd	B68	Gnd
A69	RCOL0	B69	RDQB0
A70	Gnd	B70	Gnd
A71	RCOL2	B71	RCOL1
A72	Gnd	B72	Gnd
A73	RCOL4	B73	RCOL3
A74	Gnd	B74	Gnd
A75	RROW1	B75	RROW0
A76	Gnd	B76	Gnd
A77	RSRV7 (NC)	B77	RROW2
A78	Gnd	B78	Gnd
A79	RCTM	B79	RSRV8 (NC)
A80	Gnd	B80	Gnd
A81	RCTMN	B81	RCFMN
A82	Gnd	B82	Gnd
A83	RDQA0	B83	RCFM
A84	Gnd	B84	Gnd
A85	RDQA2	B85	RDQA1
A86	Gnd	B86	Gnd
A87	RDQA4	B87	RDQA3
A88	Gnd	B88	Gnd
A89	RDQA6	B89	RDQA5
A90	Gnd	B90	Gnd
A91	RDQA8	B91	RDQA7
A92	Gnd	B92	Gnd

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2.6 RIMM Module Block Diagram

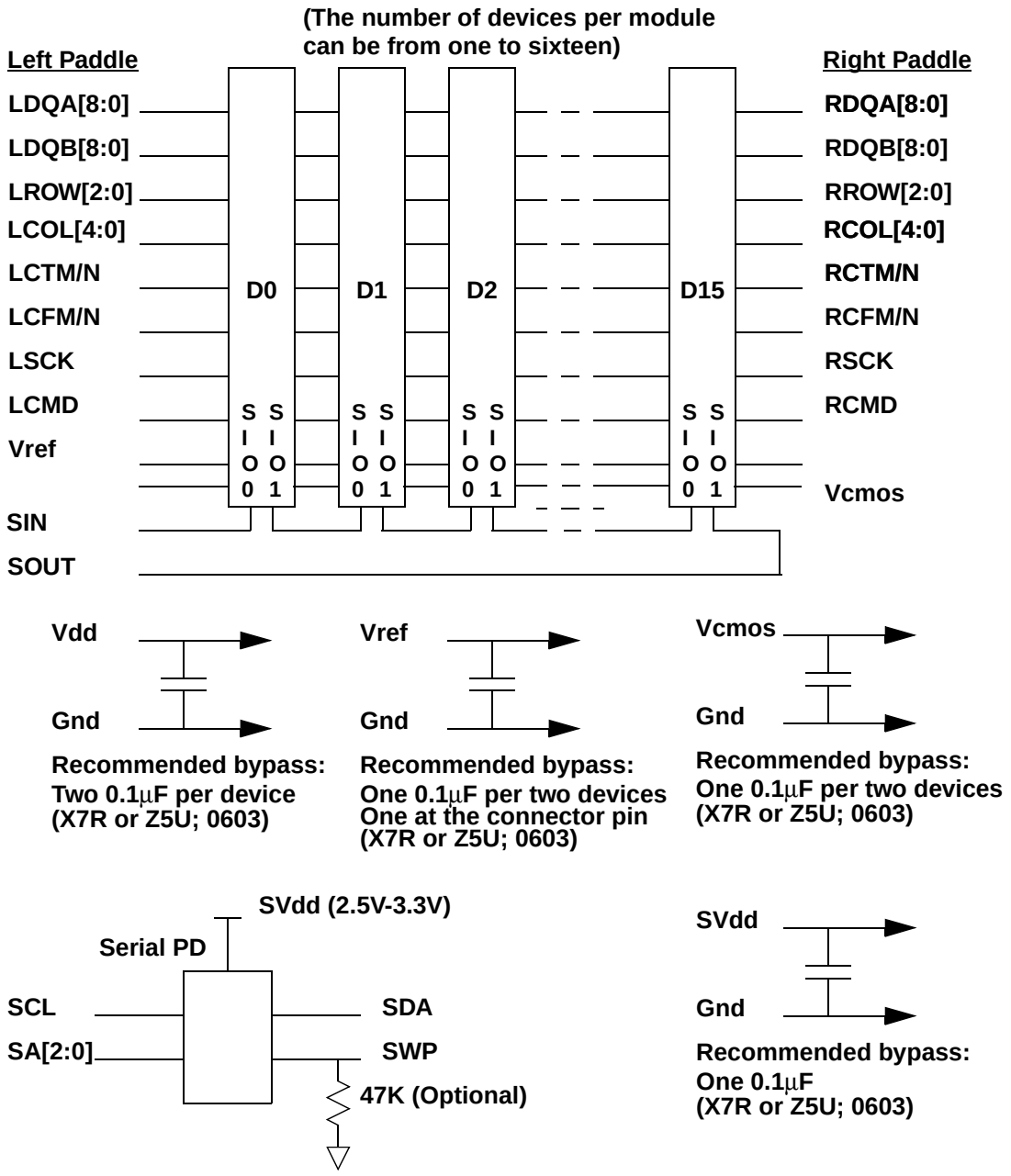

Figure 2-4: RIMM Module Block Diagram

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2.7 RIMM Layout Restrictions

2.7.1 Routing Restrictions

Besides meeting the total delay specified in Table 2-8, the following length restrictions must be met.

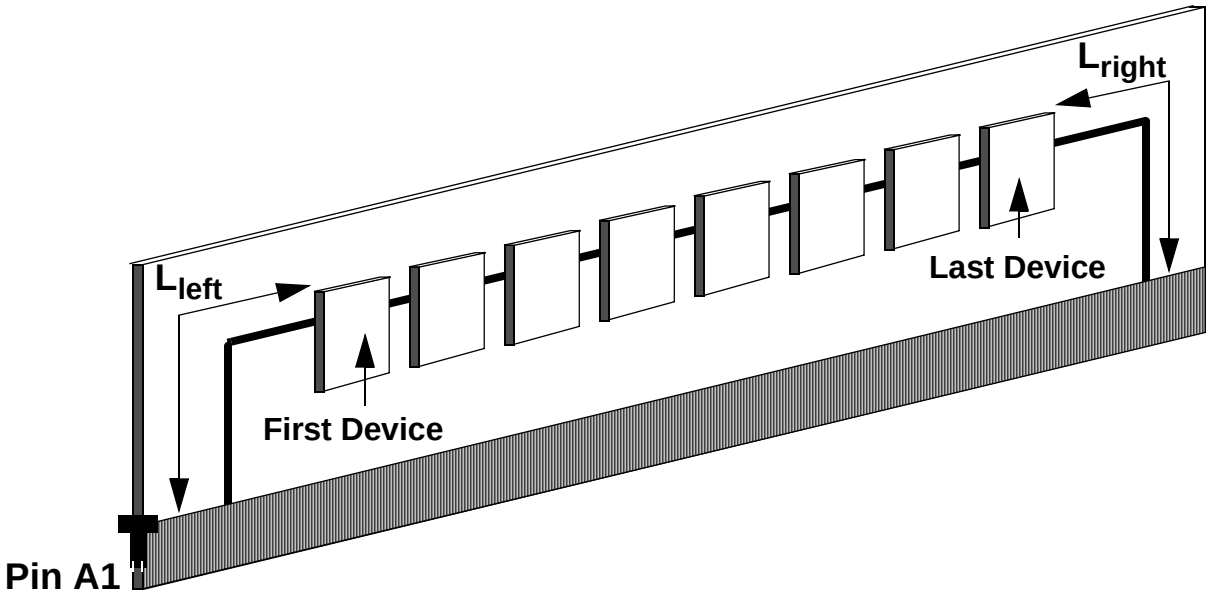

Figure 2-5: Trace Length Definition

Table 2-5: Routing Restrictions

Length	From	To	Length (mm)
L_{left}	Edge of connector finger	The via of the first RDRAM device	60 (max for 4 device module) 35 (max for 6 device module) 41 (max for 8 device module) 35 (max for 12 device module) 35 (max for 16 device module)
L_{right}	The via of the last RDRAM device	Edge of connector finger	60 (max for 4 device module) 35 (max for 6 device module) 41 (max for 8 device module) 35 (max for 12 device module) 35 (max for 16 device module)

The L_{LEFT} and L_{RIGHT} restrictions do not apply to the Continuity RIMM module, provided the signals should have a maximum length as specified by the T_{PD} specification.

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2.7.2 Placement Restrictions

If the RIMM module is to be used with a heatspreader, the following (Figure 2-6 and Figure 2-7) are the dimensions and locations of the mounting holes. In order to fit the heatspreaders currently recommended by Rambus, the RDRAM devices, SPD, capacitors and resistor must be placed in the designated areas as shown in Figure 2-6 and Figure 2-7. Figure 2-6 is for 1.375” tall module, and Figure 2-7 is for 1.25” tall module.

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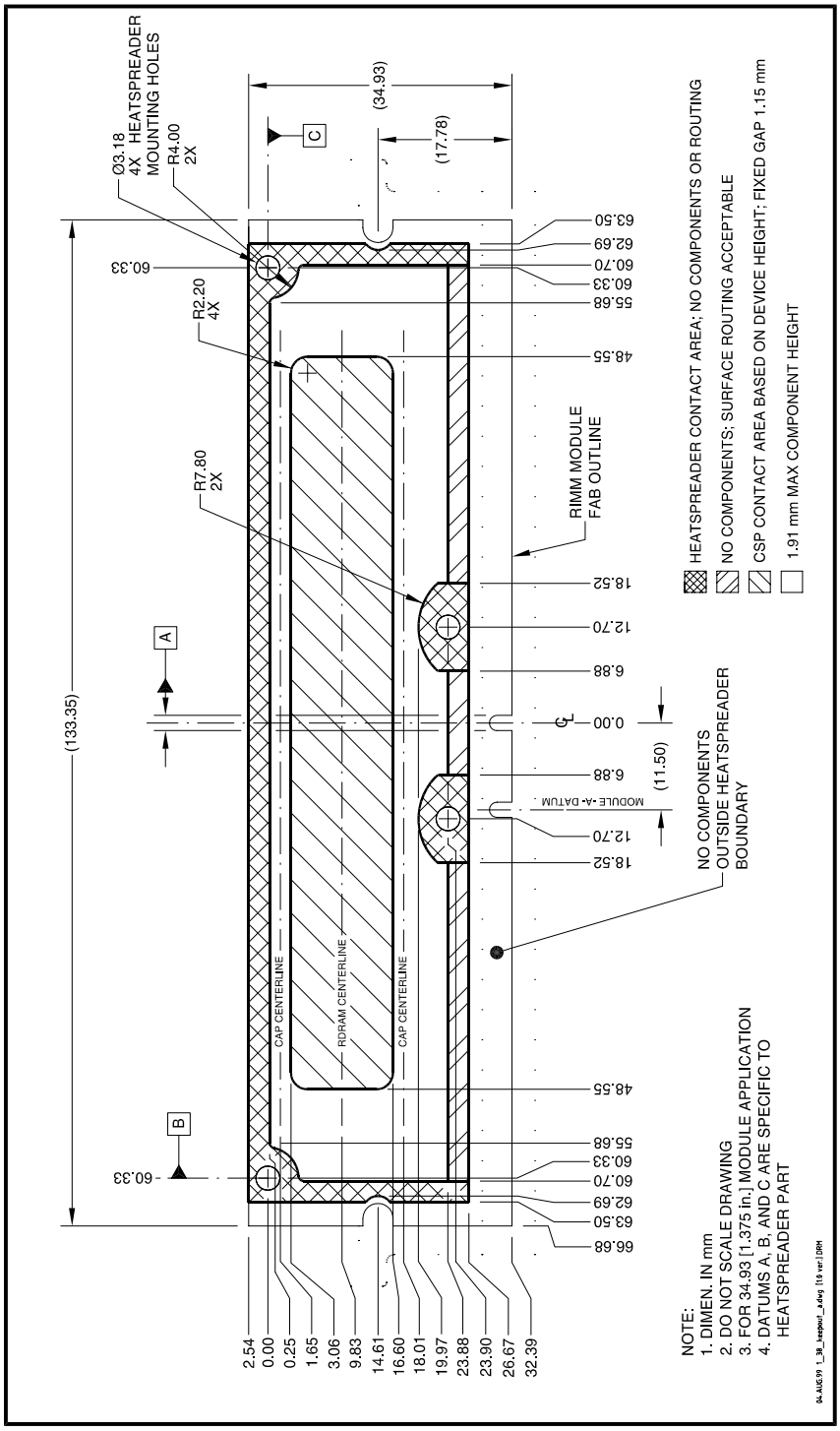

Figure 2-6: 1.375” RIMM Module Mechanical Drawing with Heatspeader and Component Placement Restrictions

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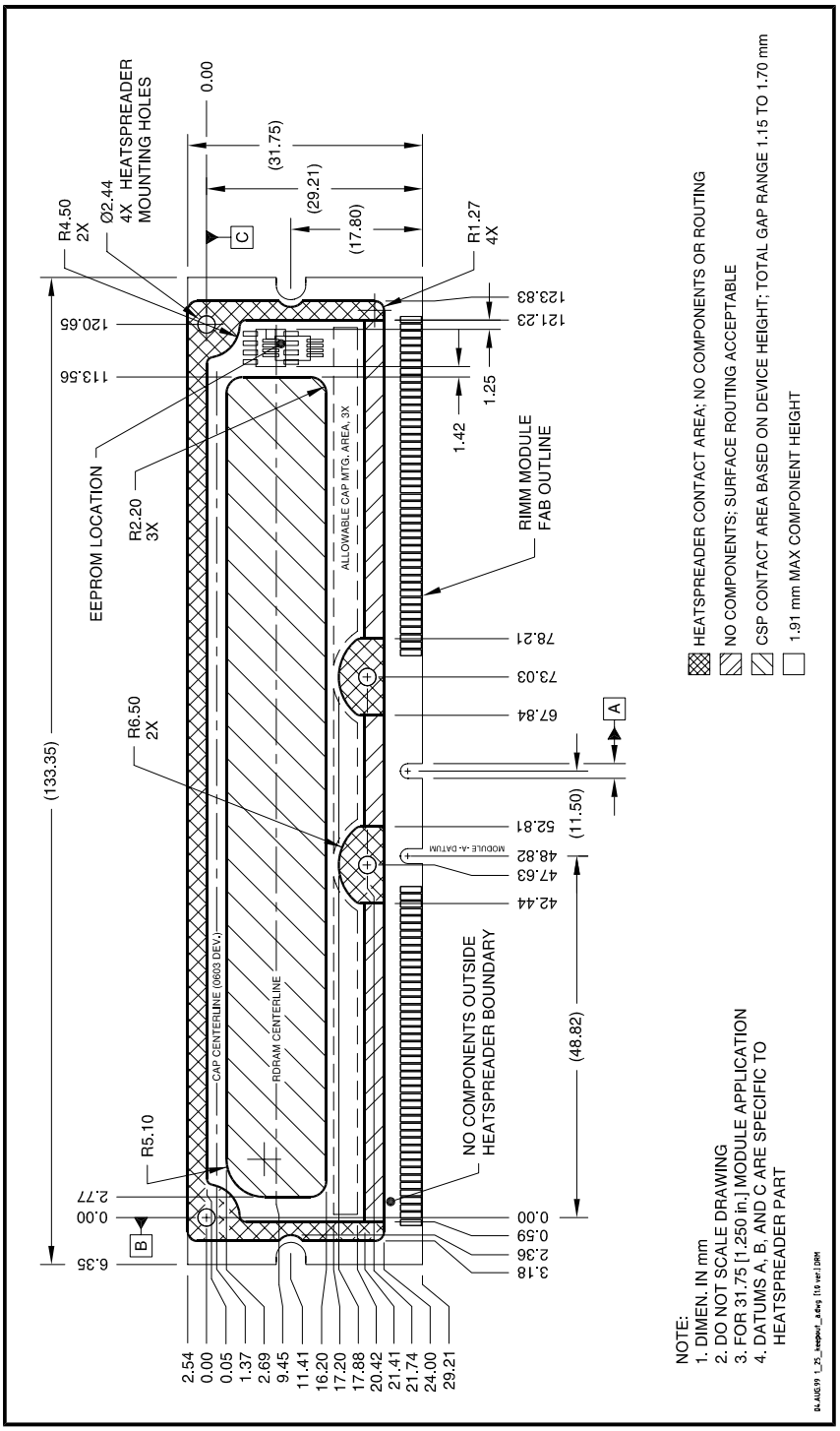

Figure 2-7: 1.25" RIMM Module Mechanical Drawing with Heatspeader and Component Placement Restrictions

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2.8 DC Electrical Specifications

2.8.1 Absolute Maximum Ratings

Table 2-6: Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
$V_{I,ABS}$	Voltage applied to any RSL or CMOS pin with respect to Gnd	-0.3	V_{DD} + 0.3	V
$V_{DD,ABS}$ $V_{DDA,ABS}$	Voltage on Vdd and VddA with respect to Gnd and GndA	-0.5	V_{DD} + 1.0	V

2.9 AC Electrical Specifications

Design verification by virtue of detailed characterizations is necessary at the prototype phase to guarantee, by design, compliance with the RIMM module design requirements. These tests are required at the beginning of the production cycle. These tests should be performed as often as needed in the production cycle to make sure the RIMM module still meets the specifications. It is important to differentiate characterization tests from production tests. The characterization tests are described in this section and specified in Table 2-8.

Table 2-7: Design Characterization Parameters

SYMBOL	DESCRIPTION	MEASUREMENT METHOD
Z	module impedance	TDR, tester, or VNA
t_{PD} (β)	RSL propagation delay	TDT, tester, or VNA
Δt_{PD} ($\Delta\beta$)	variation of prop. delay (clock to any other RSL), related to timing	TDT, tester, or VNA
V_{α}	attenuation (rail-to-rail or f_o attenuation)	function generator/scope, TDT, tester, or VNA
V_{XF} V_{XB}	forward and backward crosstalk	function generator/scope, TDT, tester, or VNA

The following sub-sections describe how to measure some of the electrical parameters of RIMM modules. All the parameters discussed here can be measured in either time domain or frequency domain as shown in Table 2-7. The time domain measurements can be done with TDR, signal generator, and scope. The frequency domain measurements can be done with a vector network analyzer.

The details on frequency domain measurement will be included in a future revision of this document.

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2.9.1 Fixtures & Probes

To perform the measurements, probes with both signal and ground contacts are required. The spacing between the probe tips should match the spacing of the contact pads on the module. A high impedance probe is also required for time domain measurement.

No special fixture is required.

2.9.2 Impedance Measurement

The module impedance can be measured by TDR. The experimental setup is shown in Figure 2-8. Notice that the module needs to be properly biased with V_{DD} and V_{REF}. The bias T is required only if the TDR cannot tolerate the DC voltage V_{REF}.

A TDR with adjustable risetime is preferred, and the risetime should be set to the minimum RSL signal risetime. Alternatively, a low pass filter with adequate bandwidth can be used to change the risetime. Such filtering can be implemented by a hardware filter or software post processing.

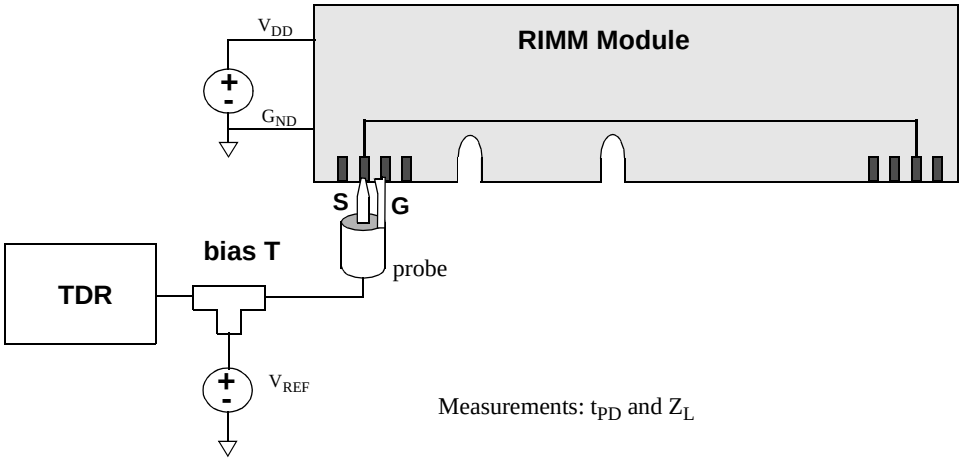

Figure 2-8: Measure Impedance and Propagation Delay by TDR

2.9.3 Propagation Delay Measurement

The propagation delay is measured by the same setup as in impedance measurement. The TDR also measures the roundtrip delay of the module. On a TDR with adjustable risetime, the fastest risetime available should be used.

The delay of the critical signals of the module can be characterized by the Vector Network Analyzer, TDT (Time Domain Transmission) instrument or by the pulse generator and an Oscilloscope. A 400MHz signal must be provided with the pulse generator. The data should be taken from the mid-point of the rising or falling edges.

2.9.4 Delta Propagation Delay Measurement

To measure the variance of propagation delay, the same setup for propagation delay measurement is repeated for all RSL lines and the high-speed CMOS signals. The maximum propagation delay variance is defined as the maximum difference between any

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RSL signals (including clock signals) and the average of all clock signals (CFM, CFMN, CTM, and CTMN).

2.9.5 Attenuation Measurement

The frequency dependent signal attenuation can be measured in time domain with a signal generator and a scope. A sinusoidal signal at the system clock frequency is applied to an RSL line, and the signal amplitudes at both ends of the module are measured with a high impedance probe. Notice that the RSL line should be terminated to its characteristic impedance.

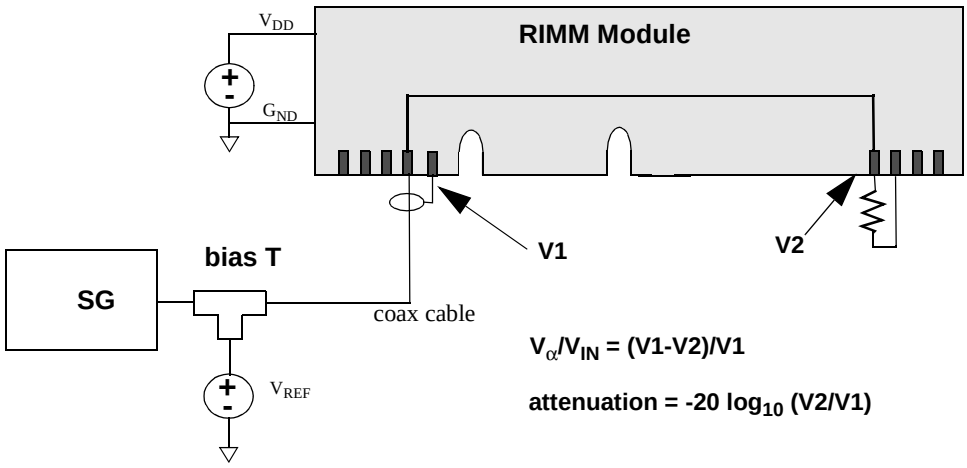

Figure 2-9: Signal Attenuation Measurement

2.9.6 Crosstalk

To measure the crosstalk in time domain, both ends of the quiet victim line must be terminated with its characteristic impedance, as well as the far end of the active signal line. The experimental setup is illustrated in Figure . Signal amplitudes at both ends of the victim line are measured. In addition, the amplitude, V_{IN}, and rise time, t_R, of the input signal are required to compute the backward, Kb, and forward, Kf, crosstalk coefficients.

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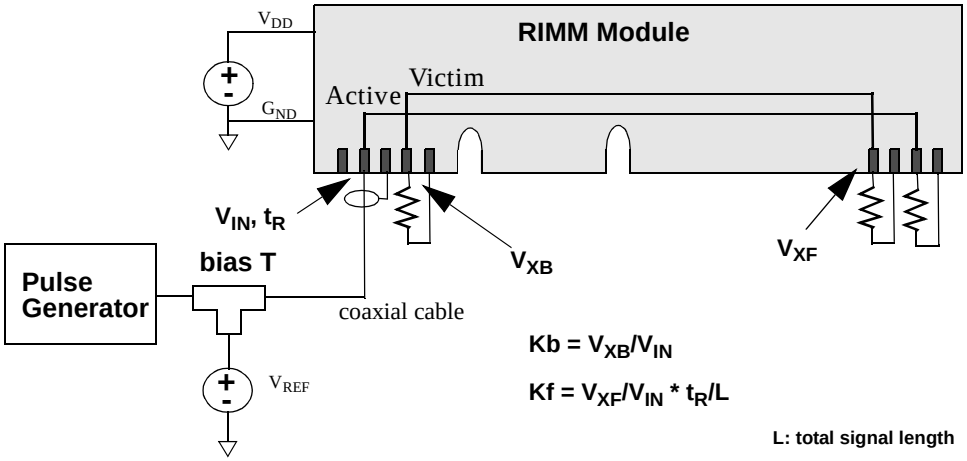

Figure 2-10: Crosstalk Measurement

2.9.7 AC Characteristics

The following AC parameters are for all module sizes unless it is specified.

The 800MHz numbers below apply for the 800MHz speed grade modules when run at ≤ 800MHz.

The 800MHz numbers below also apply for the 711MHz speed grade modules when run at ≤ 711MHz.

The 600MHz numbers below apply for the 600MHz speed grade modules when run at ≤ 600MHz.

Table 2-8: AC Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_{PD}	Average RSL clock delay [a]				
	Continuity Module (0 Device)	-	-	1.015	ns
	600MHz (2 Device Module)	-	-	TBD	ns
	600MHz (4 Device Module)	-	-	1.25	ns
	600MHz (6 Device Module)	-	-	1.40	ns
	600MHz (8 Device Module)	-	-	1.60	ns
	600MHz (12 Device Module)	-	-	1.76	ns
	600MHz (16 Device Module)	-	-	2.10	ns
	800MHz (2 Device Module)	-	-	TBD	ns
	800MHz (4 Device Module)	-	-	1.25	ns
	800MHz (6 Device Module)	-	-	1.40	ns
	800MHz (8 Device Module)	-	-	1.56	ns
	800MHz (12 Device Module)	-	-	1.76	ns
	800MHz (16 Device Module)	-	-	2.06	ns

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Symbol	Parameter	Min	Typ	Max	Unit
ΔT_{PD}	Propagation delay variation of RSL signals with respect to T_{PD} [a,b]				
	Continuity Module (0 Device)	-0.010		0.020	ns
	600MHz (2 Device Module)	TBD		TBD	ns
	600MHz (4 Device Module)	-0.021	-	0.021	ns
	600MHz (6 Device Module)	-0.021	-	0.021	ns
	600MHz (8 Device Module)	-0.021	-	0.021	ns
	600MHz (12 Device Module)	-0.021	-	0.021	ns
	600MHz (16 Device Module)	-0.024	-	0.024	ns
	800MHz (2 Device Module)	TBD		TBD	ns
	800MHz (4 Device Module)	-0.021	-	0.021	ns
	800MHz (6 Device Module)	-0.021	-	0.021	ns
	800MHz (8 Device Module)	-0.021	-	0.021	ns
	800MHz (12 Device Module)	-0.021	-	0.021	ns
	800MHz (16 Device Module)	-0.024	-	0.024	ns
$\Delta T_{PD\text{-}CMOS}$	Propagation delay variation of SCK and CMD signals with respect to an average clock delay [a]	-0.100	-	0.100	ns
Z_L	Loaded channel impedance (RSL,SCK, CMD signals)	25.2	28	30.8	Ω
$Z_{UL\text{-}CMOS}$	Unloaded channel impedance (SCK, CMD only)	23.8	28	32.2	Ω
V_α/V_{IN}	Attenuation limit				
	Continuity Module (0 Device)			8	%
	600MHz (2 Device Module)			TBD	%
	600MHz (4 Device Module)	-	-	8	%
	600MHz (6 Device Module)	-	-	9	%
	600MHz (8 Device Module)	-	-	10	%
	600MHz (12 Device Module)	-	-	18	%
	600MHz (16 Device Module)	-	-	21	%
	800MHz (2 Device Module)	-	-	TBD	%
	800MHz (4 Device Module)	-	-	12	%
	800MHz (6 Device Module)			14	%
	800MHz (8 Device Module)	-	-	16	%
	800MHz (12 Device Module)	-	-	20	%
	800MHz (16 Device Module)	-	-	25	%

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Symbol	Parameter	Min	Typ	Max	Unit
V_{XF}/V_{IN}	Forward crosstalk coefficient (input signal rise time = 300 ps; 20-80%)				
	Continuity Module (0 Device)			2	%
	600MHz (2 Device Module)			TBD	%
	600MHz (4 Device Module)			2	%
	600MHz (6 Device Module)			3	%
	600MHz (8 Device Module)			4	%
	600MHz (12 Device Module)			6	%
	600MHz (16 Device Module)			8	%
	800MHz (2 Device Module)			TBD	%
	800MHz (4 Device Module)			2	%
	800MHz (6 Device Module)			3	%
	800MHz (8 Device Module)			4	%
	800MHz (12 Device Module)			6	%
	800MHz (16 Device Module)			8	%
V_{XB}/V_{IN}	Backward crosstalk coefficient (input signal rise time = 300 ps; 20-80%)				
	Continuity Module (0 Device)			1.25	%
	600MHz (2 Device Module)			TBD	%
	600MHz (4 Device Module)			1.5	%
	600MHz (6 Device Module)			1.8	%
	600MHz (8 Device Module)			2	%
	600MHz (12 Device Module)			2.3	%
	600MHz (16 Device Module)			2.5	%
	800MHz (2 Device Module)			TBD	%
	800MHz (4 Device Module)			1.5	%
	800MHz (6 Device Module)			1.8	%
	800MHz (8 Device Module)			2	%
	800MHz (12 Device Module)			2.3	%
	800MHz (16 Device Module)			2.5	%

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Symbol	Parameter	Min	Typ	Max	Unit
R_{DC}	DC Resistance limit				
	Continuity Module (0 Device)			0.5	Ω
	600MHz (2 Device Module)			TBD	Ω
	600MHz (4 Device Module)	-	-	0.6	Ω
	600MHz (6 Device Module)	-	-	0.7	Ω
	600MHz (8 Device Module)	-	-	0.8	Ω
	600MHz (12 Device Module)	-	-	1.1	Ω
	600MHz (16 Device Module)	-	-	1.2	Ω
	800MHz (2 Device Module)			TBD	Ω
	800MHz (4 Device Module)	-	-	0.6	Ω
	800MHz (6 Device Module)	-	-	0.7	Ω
	800MHz (8 Device Module)	-	-	0.8	Ω
	800MHz (12 Device Module)	-	-	1.1	Ω
	800MHz (16 Device Module)	-	-	1.2	Ω

a. T_{PD} or Average clock delay is defined as the average delay from finger to finger of all RSL clock nets (CTM, CTMN, CFM, and CFMN).

b. If the module meets the following specification, it passes. If the module does not meet these specifications, then the specifications can be adjusted by the next table. Note the equation is not applicable to the continuity module.

Table 2-9: Adjusted ΔT_{PD} specification:

Symbol	Parameter	Adjusted Min/Max	Absolute Min/Max	Unit
ΔT_{PD}	Propagation delay variation of RSL signals with respect to T_{PD}			
	600MHz (4,6,8 Device Module)	+/- [17 + (18*N*ΔZ0)][a]	+/-0.030	ns
	600MHz (12 Device Module)	+/- [20 + (18*N*ΔZ0)]	+/-0.040	ns
	600MHz (16 Device Module)	+/- [24 + (18*N*ΔZ0)]	+/-0.050	ns
	800MHz (4,6,8 Device Module)	+/- [17 + (18*N*ΔZ0)]	+/-0.030	ns
	800MHz (12 Device Module)	+/- [20 + (18*N*ΔZ0)]	+/-0.040	ns
	800MHz (16 Device Module)	+/- [24 + (18*N*ΔZ0)]	+/-0.050	ns

a. Where N = Number of devices
ΔZ0 = delta Z0 % = (max Z0 - min Z0) / (min Z0)
(max Z0 and min Z0 are obtained from the loaded (high impedance) impedance coupons of all RSL layers on the modules)

2.10 RDRAM Component Specifications

To guarantee functionality and compatibility, all devices on a RIMM module must meet their respective specifications.

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2.11 SPD Component Specifications

The SPD function is implemented using 2048 bit EEPROM component such as the National NM24C02L, Catalyst CAT24WC02, SGS Thompson 24C02 or other vendors' equivalent. It is required that the EEPROM device must meet the functional and electrical specifications listed below.

Table 2-10: EEPROM Component Absolute Maximum Ratings

Parameter	Range
All Input or Output Voltages with respect to Ground	4.6 V to -0.3 V
Ambient Storage Temperature	-50 ^{o}C to 100 ^{o}C

Table 2-11: EEPROM Component Operating Conditions

Parameter	Range
Ambient Operating Temperature	0 ^{o}C to 70 ^{o}C
Positive Power Supply	2.2 V to 3.6 V

These devices must also meet their respective component AC and DC specifications. Any violation of these specifications constitutes a violation of the RIMM Module Specification as well.

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