4.1.2.10 – Appendix X: Specific SPDs for DDR2 SDRAM (Revision 1.0)

1.0 Introduction

This appendix describes the serial presence detects for the DDR2 version of the synchronous DRAM modules. These SPDs are those referenced in the SPD standard document for 'Specific Features'. The following SPD fields will occur in the order presented in section 1.1. Futher descriptions of Bytes 0 and 1 are found in the SPD standard. Further description of Byte 2 is found in Appendix A of the SPD standard. All unused entries wiil be coded as 00h. All unused bits in defined bytes will be coded as 0 except where noted.

1.1 Address map

The following is the SPD address map for DDR2 SDRAM. It describes where the individual LUT-entries will be held in the serial EEPROM.

Byte Number	Function Described	Notes
0	Number of Serial PD Bytes written during module production	1
1	Total number of Bytes in Serial PD device	2
2	Fundamental Memory Type (FPM, EDO, SDRAM, DDR, DDR2…)	
3	Number of Row Addresses on this assembly	
4	Number of Column Addresses on this assembly	
5	Number of DIMM Ranks	
6	Data Width of this assembly	
7	Reserved	
8	Voltage Interface Level of this assembly	
9	SDRAM Cycle time at Maximum Supported $\overline{CAS}$ Latency (CL), CL=X	3
10	SDRAM Access from Clock	
11	DIMM configuration type (Non-parity, Parity or ECC)	
12	Refresh Rate/Type	3, 4
13	Primary SDRAM Width	
14	Error Checking SDRAM Width	
15	Reserved	
16	SDRAM Device Attributes: Burst Lengths Supported	
17	SDRAM Device Attributes: Number of Banks on SDRAM Device	3
18	SDRAM Device Attributes: $\overline{CAS}$ Latency	3
19	Reserved	3
20	DIMM Type Information	3
21	SDRAM Module Attributes	
22	SDRAM Device Attributes: General	3
23	Minimum Clock Cycle at CLX-1	3
24	Maximum Data Access Time (tAC) from Clock at CLX-1	3
25	Minimum Clock Cycle at CLX-2	3
26	Maximum Data Access Time (tAC) from Clock at CLX-2	3
27	Minimum Row Precharge Time (tRP)	3
28	Minimum Row Active to Row Active delay (tRRD)	3
29	Minimum $\overline{RAS}$ to $\overline{CAS}$ delay (tRCD)	3
30	Minimum Active to Precharge Time (tRAS)	3
31	Module Rank Density	
32	Address and Command Input Setup Time Before Clock (tIS)	3
33	Address and Command Input Hold Time After Clock (tIH)	3
34	Data Input Setup Time Before Clock (tDS)	3

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Byte Number	Function Described	Notes
35	Data Input Hold Time After Clock (tDH)	3
36	Write recovery time (tWR)	3
37	Internal write to read command delay (tWTR)	3
38	Internal read to precharge command delay (tRTP)	3
39	Memory Analysis Probe Characteristics	
40	Extension of Byte 41 tRC and Byte 42 tRFC	
41	SDRAM Device Minimum Active to Active/Auto Refresh Time (tRC)	3
42	SDRAM Device Minimum Auto-Refresh to Active/Auto-Refresh Command Period (tRFC)	3
43	SDRAM Device Maximum device cycle time (tCKmax)	3
44	SDRAM Device maximum skew between DQS and DQ signals (tDQSQ)	3
45	SDRAM Device Mazimum Read DataHold Skew Facktor (tQHS)	3
46	PLL Relock Time	
47-xx	IDD in SPD(IDD in SPD TG is working to defiene this standard, and a discussion result will be added later	
xx-61	Reserved	
62	SPD Revision	
63	Checksum for Bytes 0-62	
64-71	Manufacturer's JEDEC ID Code	
72	Module Manufacturing Location	5
73-90	Module Part Number	5
91-92	Module Revision Code	5
93-94	Module Manufacturing Date	5
95-98	Module Serial Number	
99-127	Manufacturer's Specific Data	5
128-255	Open for customer use	

1. This will typically be programmed as 128 Bytes.
2. This will typically be programmed as 256 Bytes.
3. From Datasheet.
4. High order bit is Self Refresh "flag". If set to "1", the assembly supports self refresh.
5. These are optional, in accordance with the JEDEC spec.

2.0 Details of each byte

Byte 0: Number of Bytes Utilized by Module Manufacturer

This field describes the total number of bytes used by the module manufacturer for the SPD data and any (optional) specific supplier information. The byte count includes the fields for all required and optional data.

Line #	Number SPD Bytes	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
0	Undefined	0	0	0	0	0	0	0	0	00
1	1	0	0	0	0	0	0	0	1	01
2	2	0	0	0	0	0	0	1	0	02
3	3	0	0	0	0	0	0	1	1	03
4	4	0	0	0	0	0	1	0	0	04
5	5	0	0	0	0	0	1	0	1	05
6	6	0	0	0	0	0	1	1	0	06
-	-	-	-	-	-	-	-	-	-	-
-	-	-	-	-	-	-	-	-	-	-
128	128	1	0	0	0	0	0	0	0	80
-	-	-	-	-	-	-	-	-	-	-
-	-	-	-	-	-	-	-	-	-	-
-	-	-	-	-	-	-	-	-	-	-
254	254	1	1	1	1	1	1	1	0	FE
255	255	1	1	1	1	1	1	1	1	FF

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Byte 1: Total Number of Bytes in Serial PD Device

This field describes the total size of the serial memory used to hold the Serial Presence Detect data. The following lookup table describes the possible serial memory densities (in bytes) along with the corresponding descriptor.

Line #	Serial Memory	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
0	Undefined	0	0	0	0	0	0	0	0	00
1	2 Bytes	0	0	0	0	0	0	0	1	01
2	4 Bytes	0	0	0	0	0	0	1	0	02
3	8 Bytes	0	0	0	0	0	0	1	1	03
4	16 Bytes	0	0	0	0	0	1	0	0	04
5	32 Bytes	0	0	0	0	0	1	0	1	05
6	64 Bytes	0	0	0	0	0	1	1	0	06
7	128 Bytes	0	0	0	0	0	1	1	1	07
8	256 Bytes	0	0	0	0	1	0	0	0	08
9	512 Bytes	0	0	0	0	1	0	0	1	09
10	1024 Bytes	0	0	0	0	1	0	1	0	0A
11	2048 Bytes	0	0	0	0	1	0	1	1	0B
12	4096 Bytes	0	0	0	0	1	1	0	0	0C
13	8192 Bytes	0	0	0	0	1	1	0	1	0D
14	16384 Bytes	0	0	0	0	1	1	1	0	0E
-	-	-	-	-	-	-	-	-	-	-
-	-	-	-	-	-	-	-	-	-	-
254	-	1	1	1	1	1	1	1	0	FE
255	-	1	1	1	1	1	1	1	1	FF

Byte 2: Memory Type

This byte describes the fundamental memory type (or technology) implemented on the module.

Line #	Fundamental Memory Type	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
0	Reserved	0	0	0	0	0	0	0	0	00
1	Standard FPM DRAM	0	0	0	0	0	0	0	1	01
2	EDO	0	0	0	0	0	0	1	0	02
3	Pipelined Nibble	0	0	0	0	0	0	1	1	03
4	SDRAM	0	0	0	0	0	1	0	0	04
5	ROM	0	0	0	0	0	1	0	1	05
6	SGRAM DDR	0	0	0	0	0	1	1	0	06
7	SDRAM DDR	0	0	0	0	0	1	1	1	07
8	DDR-II SDRAM	0	0	0	0	1	0	0	0	08
-	-	-	-	-	-	-	-	-	-	-
253	TBD	1	1	1	1	1	1	0	1	FD
254	TBD	1	1	1	1	1	1	1	0	FE
255	TBD	1	1	1	1	1	1	1	1	FF

Byte 3: Number of Row Addresses

This field describes the Row addressing on the module. bit 0-3 are used to represent the number of row addresses, bit 4-7 are reserved and should be coded as ‘0’

Examples of Byte 3 implementation include:

Number of Row Addresses	Module Organization	Device Used	Byte 3 Contents
13, RA0-RA12	32M x 64	32M x 16	0000 1101
14, RA0-RA13	64M x 64	64M x 8	0000 1110

Line #	Number of Row Addresses	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
0	Undefined	0	0	0	0	0	0	0	0	00
1	1	0	0	0	0	0	0	0	1	01
2	2	0	0	0	0	0	0	1	0	02
3	3	0	0	0	0	0	0	1	1	03
4	4	0	0	0	0	0	1	0	0	04
5	5	0	0	0	0	0	1	0	1	05
6	6	0	0	0	0	0	1	1	0	06
7	7	0	0	0	0	0	1	1	1	07
8	8	0	0	0	0	1	0	0	0	08
9	9	0	0	0	0	1	0	0	1	09
10	10	0	0	0	0	1	0	1	0	0A
11	11	0	0	0	0	1	0	1	1	0B
12	12	0	0	0	0	1	1	0	0	0C
13	13	0	0	0	0	1	1	0	1	0D
14	14	0	0	0	0	1	1	1	0	0E
15	15	0	0	0	0	1	1	1	1	0F
-	-	-	-	-	-	-	-	-	-	-
254	254	1	1	1	1	1	1	1	0	FE
255	255	1	1	1	1	1	1	1	1	FF

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Byte 4: Number of Column Addresses

This field describes the Column addressing on the module. bit 0-3 are used to represent the number of column addresses, bit 4-7 are reserved and should be coded as ‘0’

For example:

Number of Column Addresses	Module Organization	Device Used	Byte 4 Contents
10, CA0-CA9	32M x 64	32M x 16	0000 1010
10, CA0-CA9	64M x 64	64M x 8	0000 1010

Line #	Number of Column Addresses	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
0	Undefined	0	0	0	0	0	0	0	0	00
1	1	0	0	0	0	0	0	0	1	01
2	2	0	0	0	0	0	0	1	0	02
3	3	0	0	0	0	0	0	1	1	03
4	4	0	0	0	0	0	1	0	0	04
5	5	0	0	0	0	0	1	0	1	05
6	6	0	0	0	0	0	1	1	0	06
7	7	0	0	0	0	0	1	1	1	07
8	8	0	0	0	0	1	0	0	0	08
9	9	0	0	0	0	1	0	0	1	09
10	10	0	0	0	0	1	0	1	0	0A
11	11	0	0	0	0	1	0	1	1	0B
12	12	0	0	0	0	1	1	0	0	0C
13	13	0	0	0	0	1	1	0	1	0D
14	14	0	0	0	0	1	1	1	0	0E
15	15	0	0	0	0	1	1	1	1	0F
-	-	-	-	-	-	-	-	-	-	-
254	254	1	1	1	1	1	1	1	0	FE
255	255	1	1	1	1	1	1	1	1	FF

Byte 5: Module Attributes - Number of Ranks, Package and Height

This field describes the number of ranks (Rank: any DRAMs connected to same physical $\overline{CS}$) and package on the SDRAM module, and module height. The number of logical banks for the SDRAM device is defined in Byte 17.

Bit 7 ~ Bit 5	Bit 4	Bit 3	Bit 2 ~ Bit 0
Module Height	DRAM Packgage	Card on Card	# of Ranks
Bit[7, 6, 5] 000 = less than 25.4mm 001 = 25.4mm 010 = greater than 25.4mm and less than 30mm 011 = 30.0mm 100 = 30.5mm 101 = greater than 30.5 mm others :reserved	1 = stack 0 = planar	1 = yes 0 = no	Bit [2, 1, 0] : 000 = 1rank 001 = 2ranks 010 = 3ranks 011 = 4 ranks ..... 111 = 8ranks

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Byte 6: Module Data Width

Byte 6 is used to designate the module's data width. For example:

If the module's Data Width is:	and Byte 6 is:
64	0100 0000
72	0100 1000

Line #	Data Width	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
0	0	0	0	0	0	0	0	0	0	00
-	-	-	-	-	-	-	-	-	-	-
32	32	0	0	1	0	0	0	0	0	20
33	33	0	0	1	0	0	0	0	1	21
-	-	-	-	-	-	-	-	-	-	-
36	36	0	0	1	0	0	1	0	0	24
-	-	-	-	-	-	-	-	-	-	-
64	64	0	1	0	0	0	0	0	0	40
-	-	-	-	-	-	-	-	-	-	-
72	72	0	1	0	0	1	0	0	0	48
-	-	-	-	-	-	-	-	-	-	-
80	80	0	1	0	1	0	0	0	0	50
-	-	-	-	-	-	-	-	-	-	-
128	128	1	0	0	0	0	0	0	0	80
-	-	-	-	-	-	-	-	-	-	-
144	144	1	0	0	1	0	0	0	0	90
-	-	-	-	-	-	-	-	-	-	-
254	254	1	1	1	1	1	1	1	0	FE
255	255	1	1	1	1	1	1	1	1	FF

Byte 7: Reserved

Byte 8: Voltage Interface Level of this assembly

This field describes the module's voltage interface.

Line #	Interface Levels	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
0	TTL/5V tolerant	0	0	0	0	0	0	0	0	00
1	LVTTL (not 5V tolerant)	0	0	0	0	0	0	0	1	01
2	HSTL 1.5V	0	0	0	0	0	0	1	0	02
3	SSTL 3.3V	0	0	0	0	0	0	1	1	03
4	SSTL 2.5V	0	0	0	0	0	1	0	0	04
5	SSTL 1.8V	0	0	0	0	0	1	0	1	05
6	TBD	0	0	0	0	0	1	1	0	06
-	-	-	-	-	-	-	-	-	-	-

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Byte 9: SDRAM Cycle Time

This byte defines the minimum cycle time for the SDRAM module at the highest $\overline{CAS}$ Latency, $\overline{CAS}$ Latency =X, defined in byte 18. If other $\overline{CAS}$ latencies are supported, then the associated minimum cycle times are not related in this version of the SPD standard. Byte 9, Cycle time for CAS Latency=X, is split into two nibbles: the higher order nibble (bits 4-7) designates the cycle time to a granularity of 1ns; the value presented by the lower order nibble (bits 0-3) has a granularity of .1ns and is added to the value designated by the higher nibble. In addition, four lines of the lower order nibble are assigned to support +.25,+.33, +.66 and +.75. For example:

If bits 7:4 are	and bits 3:0 are	then the total time is:
0011	1101	
(3ns)	+ (.75ns)	= 3.75ns

Byte 9, SDRAM Cycle Time, Subfield A: Whole Nanoseconds (Bits 4-7)										
Line #	**Cycle Time**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**	**Hex**
0A	Undefined	0	0	0	0	See Subfield Table B				0_
1A	1ns	0	0	0	1					1_
2A	2ns	0	0	1	0					2_
3A	3ns	0	0	1	1					3_
4A	4ns	0	1	0	0					4_
5A	5ns	0	1	0	1					5_
6A	6ns	0	1	1	0					6_
7A	7ns	0	1	1	1					7_
8A	8ns	1	0	0	0					8_
9A	9ns	1	0	0	1					9_
10A	10ns	1	0	1	0					A_
11A	11ns	1	0	1	1					B_
12A	12ns	1	1	0	0					C_
13A	13ns	1	1	0	1					D_
14A	14ns	1	1	1	0					E_
15A	15ns	1	1	1	1					F_
-	Undefined	1	1	1	1	1	1	1	1	FF

Byte 9, SDRAM Cycle Time Subfield B: Tenths of Nanoseconds (Bits 0-3)										
Line #	**Cycle Time**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**	**Hex**
0B	+0ns	See Subfield Table B				0	0	0	0	_0
1B	+.1ns					0	0	0	1	_1
2B	+.2ns					0	0	1	0	_2
3B	+.3ns					0	0	1	1	_3
4B	+.4ns					0	1	0	0	_4
5B	+.5ns					0	1	0	1	_5
6B	+.6ns					0	1	1	0	_6
7B	+.7ns					0	1	1	1	_7
8B	+.8ns					1	0	0	0	_8
9B	+.9ns					1	0	0	1	_9
10B	+.25ns					1	0	1	0	_A
11B	+.33ns					1	0	1	1	_B
12B	+.66ns					1	1	0	0	_C
13B	+.75ns					1	1	0	1	_D
-	-	-	-	-	-	-	-	-	-	-
-	Undefined	1	1	1	1	1	1	1	1	FF

Byte 10: SDRAM Access from Clock (t_{AC})

This byte defines the maximum clock to data out for the SDRAM module. This is the Clock to data out specification at the highest given $\overline{CAS}$ Latency specified in byte 18 of this SPD specification. If other $\overline{CAS}$ latencies are supported, then the associated Maximum Clock Access times are not related in this version of the SPD standard. The byte is split into two nibbles: the higher order nibble (bits 4-7) designate the access time to a granularity of 0.1ns; the value presented by the lower order nibble (bits 0-3) has the granularity of .01ns and is added to the value designated by the higher nibble. For example:

if bits 7:4 are	and bits 3:0 are	then the total time is:
0011	0101	
(0.3ns)	+ (0.05ns)	= 0.35ns

Byte 10: SDRAM Access from Clock, Subfield A: Tenths of Nanoseconds (Bits 4-7)										
Line #	**Access from Clock**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**	**Hex**
0A	Undefined	0	0	0	0	See Subfield B				0_
1A	.1ns	0	0	0	1					1_
2A	.2ns	0	0	1	0					2_
3A	.3ns	0	0	1	1					3_
4A	.4ns	0	1	0	0					4_
5A	.5ns	0	1	0	1					5_
6A	.6ns	0	1	1	0					6_
7A	.7ns	0	1	1	1					7_
8A	.8ns	1	0	0	0					8_
9A	.9ns	1	0	0	1					9_
10A	RFU	1	0	1	0					A_
11A	-	1	0	1	1					-
-	Undefined	1	1	1	1	1	1	1	1	FF

Byte 10: SDRAM Access from Clock Subfield B: Hundredths of Nanoseconds (Bits 0-3)										
Line #	**Access from Clock**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**	Hex
0B	+0ns	See Subfield A				0	0	0	0	_0
1B	+.01ns					0	0	0	1	_1
2B	+.02ns					0	0	1	0	_2
3B	+.03ns					0	0	1	1	_3
4B	+.04ns					0	1	0	0	_4
5B	+.05ns					0	1	0	1	_5
6B	+.06ns					0	1	1	0	_6
7B	+.07ns					0	1	1	1	_7
8B	+.08ns					1	0	0	0	_8
9B	+.09ns					1	0	0	1	_9
10B	RFU					1	0	1	0	_A
11B	–	-	-	-	-	-	-	-	-	-
-	Undefined	1	1	1	1	1	1	1	1	FF

Byte 11: DIMM Configuration Type

This byte describes the module's error detection and/or correction scheme.

Line #	Error Detection/Correction	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
0	None	0	0	0	0	0	0	0	0	00
1	Parity	0	0	0	0	0	0	0	1	01
2	ECC	0	0	0	0	0	0	1	0	02
3	TBD	0	0	0	0	0	0	1	1	03
4	TBD	0	0	0	0	0	1	0	0	04
5	TBD	0	0	0	0	0	1	0	1	05
6	TBD	0	0	0	0	0	1	1	0	06
-	-	-	-	-	-	-	-	-	-	-
-	-	-	-	-	-	-	-	-	-	-

Byte 12: Refresh Rate/Type

This byte describes the module's refresh rate.

Line #	Refresh Period	Bit 7 (Self Refresh Flag)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
0	Normal (15.625 us)	0	0	0	0	0	0	0	0	00
1	Reduced (.25x)...3.9us	0	0	0	0	0	0	0	1	01
2	Reduced (.5x)...7.8us	0	0	0	0	0	0	1	0	02
3	Extended (2x)...31.3us	0	0	0	0	0	0	1	1	03
4	Extended (4x)...62.5us	0	0	0	0	0	1	0	0	04
5	Extended (8x)...125us	0	0	0	0	0	1	0	1	05
6	TBD	0	0	0	0	0	1	1	0	06
7	TBD	0	0	0	0	0	1	1	1	07
-	-	-	-	-	-	-	-	-	-	-
-	-	-	-	-	-	-	-	-	-	-

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Byte 13: Primary SDRAM Width

Bits 0-7 of this byte indicate the width of the primary data SDRAM. The primary SDRAM is that which is used for data; examples of primary (data) SDRAM widths are x4, x8, x16, and x32. Note that if the module is made with SDRAMs which provide for data and error checking, e.g. x9, x18, and x36, then it is also designated in this field.

This table contains examples of SDRAM DIMM

Module Width	Primary SDRAM Width	Error Checking SDRAM Width	Possible (512Mb based) Module Density	Byte 13 Contents
x72	x8	x8	512MB	0000 1000
x72	x16	x16	256MB	0001 0000
x72	x8	x16	1024MB	0000 1000

Line #	SDRAM Data Width	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
0	Undefined	0	0	0	0	0	0	0	0	00
1	1	0	0	0	0	0	0	0	1	01
2	2	0	0	0	0	0	0	1	0	02
3	3	0	0	0	0	0	0	1	1	03
4	4	0	0	0	0	0	1	0	0	04
5	5	0	0	0	0	0	1	0	1	05
6	6	0	0	0	0	0	1	1	0	06
7	7	0	0	0	0	0	1	1	1	07
8	8	0	0	0	0	1	0	0	0	08
9	9	0	0	0	0	1	0	0	1	09
10	10	0	0	0	0	1	0	1	0	0A
11	11	0	0	0	0	1	0	1	1	0B
12	12	0	0	0	0	1	1	0	0	0C
13	13	0	0	0	0	1	1	0	1	0D
14	14	0	0	0	0	1	1	1	0	0E
15	15	0	0	0	0	1	1	1	1	0F
-	-	-	-	-	-	-	-	-	-	-
254	254	1	1	1	1	1	1	1	0	FE
255	255	1	1	1	1	1	1	1	1	FF

Byte 14: Error Checking SDRAM Width

If the module incorporates error checking and if the primary data SDRAM does not include these bits — i.e. there are separate error checking SDRAMs — then the error checking SDRAM's width is expressed in this byte. Bits 0-7 of this byte relate the error checking SDRAM's width.

The following table contains examples of error checking SDRAM widths

Module Width	Primary SDRAM Width	Error Checking SDRAM Width	Possible (512Mb based) Module Density	Byte 14 Contents
x72	x8	x8	512MB	0000 1000
x72	x16	x16	256MB	0001 0000
x72	x8	x16	1024MB	0001 0000

Line #	Error Checking SDRAM Width	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
0	Undefined	0	0	0	0	0	0	0	0	00
1	1	0	0	0	0	0	0	0	1	01
2	2	0	0	0	0	0	0	1	0	02
3	3	0	0	0	0	0	0	1	1	03
4	4	0	0	0	0	0	1	0	0	04
5	5	0	0	0	0	0	1	0	1	05
6	6	0	0	0	0	0	1	1	0	06
7	7	0	0	0	0	0	1	1	1	07
8	8	0	0	0	0	1	0	0	0	08
9	9	0	0	0	0	1	0	0	1	09
10	10	0	0	0	0	1	0	1	0	0A
11	11	0	0	0	0	1	0	1	1	0B
12	12	0	0	0	0	1	1	0	0	0C
13	13	0	0	0	0	1	1	0	1	0D
14	14	0	0	0	0	1	1	1	0	0E
15	15	0	0	0	0	1	1	1	1	0F
-	-	-	-	-	-	-	-	-	-	-
254	254	1	1	1	1	1	1	1	0	FE
255	255	1	1	1	1	1	1	1	1	FF

Byte 15: Reserved

Byte 16: SDRAM Device Attributes – Burst Lengths Supported

This byte describes which various programmable burst lengths are supported by the devices on the module. If the bit is “1”, then that Burst Length is supported on the module; if the bit is “0”, then that Burst Length is not supported by the module.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TBD	TBD	TBD	TBD	Burst Length = 8	Burst Length = 4	TBD	TBD
0	0	0	0	1 or 0	1 or 0	0	0
1 = Supported on this assembly, 0 = Not supported on this assembly.							

Byte 17: SDRAM Device Attributes – Number of Banks on SDRAM Device

This byte details how many banks are on each SDRAM installed onto the module.

Line #	Number of Banks	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
0	Undefined	0	0	0	0	0	0	0	0	00
-	-	-	-	-	-	-	-	-	-	-
-	-	-	-	-	-	-	-	-	-	-
4	4	0	0	0	0	0	1	0	0	04
-	-	-	-	-	-	-	-	-	-	-
8	8	0	0	0	0	1	0	0	0	08
-	-	-	-	-	-	-	-	-	-	-
255	255	1	1	1	1	1	1	1	1	FF

Byte 18: SDRAM Device Attributes – $\overline{\text{CAS}}$ Latency

This byte describes which of the programmable $\overline{\text{CAS}}$ latencies are acceptable for the module. If the bit is “1”, then that $\overline{\text{CAS}}$ latency is supported on the module; if the bit is “0”, then that $\overline{\text{CAS}}$ latency is not supported by the module.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TBD	TBD	$\overline{\text{CAS}}$ Latency = 5	$\overline{\text{CAS}}$ Latency = 4	$\overline{\text{CAS}}$ Latency = 3	$\overline{\text{CAS}}$ Latency = 2	TBD	TBD
0	0	1 or 0	1 or 0	1 or 0	1 or 0	0	0
1 = Supported on this assembly; 0 = Not supported on this assembly.							

Byte 19: Reserved

Byte 20: DIMM type information

This byte describes the DIMM type information of DDR2 SDRAM.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TBD	TBD	Mini-UDIMM (82.0 mm)*	Mini-RDIMM (82.0 mm)*	Micro-DIMM (45.5 mm)*	SO-DIMM (67.6 mm)*	Regular UDIMM (133.35 mm)*	Regular RDIMM (133.35 mm)*
0	0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0
1 = Supported on this assembly; 0 = Not supported on this assembly. * numbers shown are module width							

Byte 21: SDRAM Modules Attributes

This byte depicts various aspects of the module. It details various unrelated but critical elements pertinent to the module. A given module characteristic is detailed in the designated bit; if the aspect is TRUE, then the bit is “1”. Conversely, if the aspect is FALSE, the designated bit is “0”.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TBD	*Analysis probe installed	TBD	FET Switch External Enable	TBD	TBD	TBD	TBD
0	1 or 0	0	1 or 0	0	0	0	0

1 = Included on this assembly; 0 = Not included on this assembly.

* All normal DIMMs will set bit 6 to 0. If bit 6 is set to a 1 this indicates that a memory bus analysis probe is installed in the slot. The BIOS should ensure that Address and Command bus clocks remain turned for that slot and byte 39 may be optionally consulted to determine probe characteristics

Byte 22: SDRAM Device Attributes – General

This byte depicts various aspects of the SDRAMs on the module. It details various unrelated but critical elements pertinent to the SDRAMs. A given SDRAM characteristic is detailed in the designated bit; if the aspect is TRUE, then the bit is “1”. Conversely, if the aspect is FALSE, the designated bit is “0”.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TBD	TBD	TBD	TBD	TBD	TBD	TBD	Supports Weak Driver
0	0	0	0	0	0	0	1 or 0

Byte 23: Minimum Clock Cycle Time at Reduced $\overline{\text{CAS}}$ Latency, X- 1

The highest $\overline{\text{CAS}}$ latency identified in byte 18 is X and the timing values associated with $\overline{\text{CAS}}$ latency 'X' are found at byte locations 9 and 10. Byte 23 denotes the minimum cycle time at $\overline{\text{CAS}}$ latency X- 1.

For example, if byte 18 denotes $\overline{\text{CAS}}$ latencies of 3 to 4, then X is 4 and X-1 is 3. Byte 23 then denotes the minimum cycle time at $\overline{\text{CAS}}$ latency 3.

Byte 23 is split into two nibbles: the higher order nibble (bits 4-7) designate the cycle time to a granularity of 1ns; the value presented by the lower order nibble (bits 0-3) has a granularity of .1ns and is added to the value designated by the higher nibble. In addition, four lines of the lower order nibble are assigned to support +0.25,+.33, +.66 and +.75. For example:

if bits 7:4 are	and bits 3:0 are	then the total time is
0011	1011	
(3ns)	+ (.75ns)	=3.75ns

Byte 23, SDRAM Minimum Cycle Time @ CL X-1, Subfield A: Whole Nanoseconds (Bits 4-7)										
Line #	**Access from Clock**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**	**Hex**
0A	Undefined	0	0	0	0	See Subfield B				0_
1A	1ns/16ns	0	0	0	1					1_
2A	2ns/17ns	0	0	1	0					2_
3A	3ns	0	0	1	1					3_
4A	4ns	0	1	0	0					4_
5A	5ns	0	1	0	1					5_
6A	6ns	0	1	1	0					6_
7A	7ns	0	1	1	1					7_
8A	8ns	1	0	0	0					8_
9A	9ns	1	0	0	1					9_
10A	10ns	1	0	1	0					A_
11A	11ns	1	0	1	1					B_
12A	12ns	1	1	0	0					C_
13A	13ns	1	1	0	1					D_
14A	14ns	1	1	1	0					E_
15A	15ns	1	1	1	1					F_

Byte 23, SDRAM Minimum Cycle Time @ CL X-1, Subfield B: Tenths of Nanoseconds (Bits 0-3)										
Line #	**Access from Clock**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**	Hex
0B	+0ns	See Subfield A				0	0	0	0	_0
1B	+.1ns					0	0	0	1	_1
2B	+.2ns					0	0	1	0	_2
3B	+.3ns					0	0	1	1	_3
4B	+.4ns					0	1	0	0	_4
5B	+.5ns					0	1	0	1	_5
6B	+.6ns					0	1	1	0	_6
7B	+.7ns					0	1	1	1	_7
8B	+.8ns					1	0	0	0	_8
9B	+.9ns					1	0	0	1	_9
10B	+.25ns					1	0	1	0	_A
11B	+.33ns					1	0	1	1	_B
12B	+.66ns					1	1	0	0	_C
13B	+.75ns					1	1	0	1	_D
-	.	.	.	.	.	.	.	.	.	.
-	Undefined	1	1	1	1	1	1	1	1	FF

Byte 24: Maximum Data Access Time (t_{AC}) from Clock at CL X- 1

The highest $\overline{CAS}$ latency identified in byte 18 is X. Byte 23 denotes the maximum access time from Clock at $\overline{CAS}$ latency X- 1.

For example, if byte 18 denotes supported $\overline{CAS}$ latencies of 3 to 4, then X is 4 and X-1 is 3. Byte 24 then denotes the maximum clock access time from CK at $\overline{CAS}$ latency 3.

Byte 24 is split into two nibbles: the higher order nibble (bits 4-7) designate the access time to a granularity of 0.1ns; the value presented by the lower order nibble (bits 0-3) has the granularity of .01ns and is added to the value designated by the higher nibble. For example:

if bits 7:4 are	and bits 3:0 are	then the total time is:
0011	0101	
(0.3 ns)	+ (0.05 ns)	= 0.35 ns

Byte 24: SDRAM Access from Clock @ X-1, Subfield A: Tenths of Nanoseconds (Bits 4-7)										
Line #	**Access from Clock**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**	**Hex**
0A	Undefined	0	0	0	0	See Subfield B				0_
1A	.1ns	0	0	0	1					1_
2A	.2ns	0	0	1	0					2_
3A	.3ns	0	0	1	1					3_
4A	.4ns	0	1	0	0					4_
5A	.5ns	0	1	0	1					5_
6A	.6ns	0	1	1	0					6_
7A	.7ns	0	1	1	1					7_
8A	.8ns	1	0	0	0					8_
9A	.9ns	1	0	0	1					9_
10A	RFU	1	0	1	0					A_
11A	-	1	0	1	1					-
-	Undefined	1	1	1	1	1	1	1	1	FF

Byte 24: SDRAM Access from Clock @ X-1, Subfield B: Hundredths of Nanoseconds (Bits 0-3)										
Line #	**Access from Clock**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**	Hex
0B	+0ns	See Subfield A				0	0	0	0	_0
1B	+.01ns					0	0	0	1	_1
2B	+.02ns					0	0	1	0	_2
3B	+.03ns					0	0	1	1	_3
4B	+.04ns					0	1	0	0	_4
5B	+.05ns					0	1	0	1	_5
6B	+.06ns					0	1	1	0	_6
7B	+.07ns					0	1	1	1	_7
8B	+.08ns					1	0	0	0	_8
9B	+.09ns					1	0	0	1	_9
10B	RFU					1	0	1	0	_A
11B	–	-	-	-	-	-	-	-	-	-
-	Undefined	1	1	1	1	1	1	1	1	FF

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Byte 25: Minimum Clock Cycle Time at CL X-2

The highest $\overline{CAS}$ latency identified in byte 18 is X. Byte 25 denotes the minimum cycle time at $\overline{CAS}$ latency X-2.

For example, if byte 18 denotes $\overline{CAS}$ latencies of 3 to 5, then X is 5 and X-2 is 3. Byte 25 then denotes the minimum cycle time at $\overline{CAS}$ latency 3.

Byte 25 is split into two nibbles: the higher order nibble (bits 4-7) designates the cycle time to a granularity of 1ns; the value presented by the lower order nibble (bits 0-3) has a granularity of .1ns and is added to the value designated by the higher order nibble. In addition, four lines of the lower order nibble are assigned to support +0.25,+.33, +.66 and +.75. For example:

if bits 7:2 are	and bits 1:0 are	then the total time is
0011	1011	
(3 ns)	+ (.75 ns)	= 3.75 ns

Byte 25, SDRAM Minimum Cycle Time @ CL X-2, Subfield A: Whole Nanoseconds (Bits 4-7)										
Line #	**Access from Clock**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**	**Hex**
0A	Undefined	0	0	0	0	See Subfield B				0_
1A	1ns/16ns	0	0	0	1					1_
2A	2ns/17ns	0	0	1	0					2_
3A	3ns	0	0	1	1					3_
4A	4ns	0	1	0	0					4_
5A	5ns	0	1	0	1					5_
6A	6ns	0	1	1	0					6_
7A	7ns	0	1	1	1					7_
8A	8ns	1	0	0	0					8_
9A	9ns	1	0	0	1					9_
10A	10ns	1	0	1	0					A_
11A	11ns	1	0	1	1					B_
12A	12ns	1	1	0	0					C_
13A	13ns	1	1	0	1					D_
14A	14ns	1	1	1	0					E_
15A	15ns	1	1	1	1					F_

Byte 25, SDRAM Minimum Cycle Time @ CL X-2, Subfield B: Tenths of Nanoseconds (Bits 0-3)										
Line #	**Access from Clock**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**	Hex
0B	+0ns	See Subfield A				0	0	0	0	_0
1B	+.1ns					0	0	0	1	_1
2B	+.2ns					0	0	1	0	_2
3B	+.3ns					0	0	1	1	_3
4B	+.4ns					0	1	0	0	_4
5B	+.5ns					0	1	0	1	_5
6B	+.6ns					0	1	1	0	_6
7B	+.7ns					0	1	1	1	_7
8B	+.8ns					1	0	0	0	_8
9B	+.9ns					1	0	0	1	_9
10B	+.25ns					1	0	1	0	_A
11B	+.33ns					1	0	1	1	_B
12B	+.66ns					1	1	0	0	_C
13B	+.75ns					1	1	0	1	_D
-	.	.	.	.	.	.	.	.	.	.
-	Undefined	1	1	1	1	1	1	1	1	FF

Byte 26: Maximum Data Access Time (t_{AC}) from Clock at CL X-2

The highest $\overline{CAS}$ latency identified in byte 18 is X. Byte 26 denotes the maximum access time from Clock at $\overline{CAS}$ latency X-2.

For example, if byte 18 denotes supported $\overline{CAS}$ latencies of 3 to 5, then X is 5 and X-2 is 3. Byte 26 then denotes the maximum data access time from CK at $\overline{CAS}$ latency 3.

Byte 26 is split into two nibbles: the higher order nibble (bits 4-7) designate the access time to a granularity of 0.1ns; the value presented by the lower order nibble (bits 0-3) has the granularity of .01ns and is added to the value designated by the higher nibble. For example:

if bits 7:4 are	and bits 3:0 are	then the total time is:
0011	0101	
(0.3ns)	+ (0.05ns)	= 0.35ns

Byte 26: SDRAM Access from Clock @ CL = X-2, Subfield A: Tenths of Nanoseconds (Bits 4-7)										
Line #	**Access from Clock**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**	**Hex**
0A	Undefined	0	0	0	0	See Subfield B				0_
1A	.1ns	0	0	0	1					1_
2A	.2ns	0	0	1	0					2_
3A	.3ns	0	0	1	1					3_
4A	.4ns	0	1	0	0					4_
5A	.5ns	0	1	0	1					5_
6A	.6ns	0	1	1	0					6_
7A	.7ns	0	1	1	1					7_
8A	.8ns	1	0	0	0					8_
9A	.9ns	1	0	0	1					9_
10A	RFU	1	0	1	0					A_
11A	-	1	0	1	1					-
-	Undefined	1	1	1	1	1	1	1	1	FF

Byte 26: SDRAM Access from Clock @ CL = X-2, Subfield B: Hundredths of Nanoseconds (Bits 0-3)										
Line #	**Access from Clock**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**	Hex
0B	+0ns	See Subfield A				0	0	0	0	_0
1B	+.01ns					0	0	0	1	_1
2B	+.02ns					0	0	1	0	_2
3B	+.03ns					0	0	1	1	_3
4B	+.04ns					0	1	0	0	_4
5B	+.05ns					0	1	0	1	_5
6B	+.06ns					0	1	1	0	_6
7B	+.07ns					0	1	1	1	_7
8B	+.08ns					1	0	0	0	_8
9B	+.09ns					1	0	0	1	_9
10B	RFU					1	0	1	0	_A
11B	–	-	-	-	-	-	-	-	-	-
-	Undefined	1	1	1	1	1	1	1	1	FF

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Byte 27: Minimum Row Precharge Time (t_{RP})

Byte 27 is used to designate the module's minimum Row Precharge time.

Byte 27 is split into two pieces: the higher order bits (bits 2-7) designate the time to a granularity of 1ns; the value presented by the lower order bits (bits 0-1) has a granularity of .25ns and is added to the value designated by the higher bits. For example:

if bits 7:2 are	and bits 1:0 are	then the total time is
001111 (15ns)	00 +(0.0ns)	= 15.0ns
010010 (18ns)	11 +(.75ns)	= 18.75ns

Byte 27, SDRAM Minimum t_{RP} Time, Subfield A: Whole Nanoseconds (Bits 2-7)								
Nanoseconds	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Undefined	0	0	0	0	0	0	See Subfield B	
1ns	0	0	0	0	0	1		
2ns	0	0	0	0	1	0		
3ns	0	0	0	0	1	1		
4ns	0	0	0	1	0	0		
5ns	0	0	0	1	0	1		
6ns	0	0	0	1	1	0		
7ns	0	0	0	1	1	1		
8ns	0	0	1	0	0	0		
9ns	0	0	1	0	0	1		
10ns	0	0	1	0	1	0		
:	:	:	:	:	:	:		
:	:	:	:	:	:	:		
61ns	1	1	1	1	0	1		
62ns	1	1	1	1	1	0		
63ns	1	1	1	1	1	1		

Byte 27, SDRAM Minimum t_{RP} Time, Subfield B: Quarters of Nanoseconds (Bits 0-1)								
Access from Clock	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
+0ns	See Subfield A						0	0
+.25ns							0	1
+.50ns							1	0
+.75ns							1	1

Byte 28: Minimum Row Active to Row Active Delay (t_{RRD})

This field describes the minimum required delay between different row activations.

Byte 28 is split into two pieces: the higher order bits (bits 2-7) designate the time to a granularity of 1ns; the value presented by the lower order bits (bits 0-1) has a granularity of .25ns and is added to the value designated by the higher bits. For example:

if bits 7:2 are	and bits 1:0 are	then the total time is
000111 (7ns)	10 +(0.5ns)	= 7.5ns
001010 (10ns)	00 +(0.0ns)	= 10ns

Byte 28, SDRAM Minimum t_{RRD} Time, Subfield A: Whole Nanoseconds (Bits 2-7)								
Nanoseconds	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Undefined	0	0	0	0	0	0	See Subfield B	
1ns	0	0	0	0	0	1		
2ns	0	0	0	0	1	0		
3ns	0	0	0	0	1	1		
4ns	0	0	0	1	0	0		
5ns	0	0	0	1	0	1		
6ns	0	0	0	1	1	0		
7ns	0	0	0	1	1	1		
8ns	0	0	1	0	0	0		
9ns	0	0	1	0	0	1		
10ns	0	0	1	0	1	0		
:	:	:	:	:	:	:		
:	:	:	:	:	:	:		
61ns	1	1	1	1	0	1		
62ns	1	1	1	1	1	0		
63ns	1	1	1	1	1	1		

Byte 28, SDRAM Minimum t_{RRD} Time, Subfield B: Quarters of Nanoseconds (Bits 0-1)								
Access from Clock	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
+0ns	See Subfield A						0	0
+.25ns							0	1
+.50ns							1	0
+.75ns							1	1

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Byte 29: Minimum $\overline{RAS}$ to $\overline{CAS}$ Delay (t_{RCD})

This byte describes the minimum delay required between assertions of $\overline{RAS}$ and $\overline{CAS}$.

Byte 29 is split into two pieces: the higher order bits (bits 2-7) designate the time to a granularity of 1ns; the value presented by the lower order bits (bits 0-1) has a granularity of .25ns and is added to the value designated by the higher bits. For example:

if bits 7:2 are	and bits 1:0 are	then the total time is
001111 (15ns)	00 +(0.0ns)	= 15.0ns
010010 (18ns)	11 +(.75ns)	= 18.75ns

Byte 29, SDRAM Minimum t_{RCD} Time, Subfield A: Whole Nanoseconds (Bits 2-7)								
Nanoseconds	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Undefined	0	0	0	0	0	0	See Subfield B	
1ns	0	0	0	0	0	1		
2ns	0	0	0	0	1	0		
3ns	0	0	0	0	1	1		
4ns	0	0	0	1	0	0		
5ns	0	0	0	1	0	1		
6ns	0	0	0	1	1	0		
7ns	0	0	0	1	1	1		
8ns	0	0	1	0	0	0		
9ns	0	0	1	0	0	1		
10ns	0	0	1	0	1	0		
:	:	:	:	:	:	:		
:	:	:	:	:	:	:		
61ns	1	1	1	1	0	1		
62ns	1	1	1	1	1	0		
63ns	1	1	1	1	1	1		

Byte 29, SDRAM Minimum t_{RCD} Time, Subfield B: Quarters of Nanoseconds (Bits 0-1)								
Access from Clock	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
+0ns	See Subfield A						0	0
+.25ns							0	1
+.50ns							1	0
+.75ns							1	1

Byte 30: Minimum Active to Precharge Time (t_{RAS})

This byte identifies the minimum active to precharge time.

Minimum Active to Precharge Time (ns)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
Undefined	0	0	0	0	0	0	0	0	00
1	0	0	0	0	0	0	0	1	01
2	0	0	0	0	0	0	1	0	02
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
25	0	0	0	1	1	0	0	1	19
26	0	0	0	1	1	0	1	0	1A
27	0	0	0	1	1	0	1	1	1B
28	0	0	0	1	1	1	0	0	1C
29	0	0	0	1	1	1	0	1	1D
30	0	0	0	1	1	1	1	0	1E
31	0	0	0	1	1	1	1	1	1F
32	0	0	1	0	0	0	0	0	20
33	0	0	1	0	0	0	0	1	21
34	0	0	1	0	0	0	1	0	22
35	0	0	1	0	0	0	1	1	23
36	0	0	1	0	0	1	0	0	24
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
127	0	1	1	1	1	1	1	1	7F
128	1	0	0	0	0	0	0	0	80
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
254	1	1	1	1	1	1	1	0	FE
255	1	1	1	1	1	1	1	1	FF

Byte 31: Module Rank Density

This byte describes the density of each physical rank on the SDRAM DIMM. This byte will have only one bit set to “1” to represent per rank density. If there are more than one physical rank on the module (as represented in byte 5), then total density can be calculated by multiplying rank density in this field by number ranks described in byte 5.

For example:

Density of Physical Rank	Byte 31 Contents
512MB	1000 0000
256MB	0100 0000

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
512 MB	256 MB	128 MB	16 GB	8 GB	4 GB	2 GB	1 GB
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1
1 = Supported on this assembly; 0 = Not supported on this assembly.							

Byte 32: Address and Command Setup Time Before Clock (tIS)

This field describes the input setup time before the rising edge of the clock. The byte is broken into two nibbles: the higher order nibble (bits 4-7) designate the access time to a granularity of 0.1ns; the value presented by the lower order nibble (bits 0-3) has the granularity of .01ns and is added to the value designated by the higher nibble. For example:

if bits 7:4 are	and bits 3:0 are	then the total time is:
1011 (1.1ns)	0000 + (0ns)	= 1.1ns
1100 (1.2ns)	0101 + (0.05ns)	= 1.25ns

Byte 32: SDRAM Setup Time Before Clock, Subfield A: Tenths of Nanoseconds (Bits 4-7)										
Line #	**Access from Clock**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**	**Hex**
0A	Undefined	0	0	0	0	See Subfield B				0_
1A	.1ns	0	0	0	1					1_
2A	.2ns	0	0	1	0					2_
3A	.3ns	0	0	1	1					3_
4A	.4ns	0	1	0	0					4_
5A	.5ns	0	1	0	1					5_
6A	.6ns	0	1	1	0					6_
7A	.7ns	0	1	1	1					7_
8A	.8ns	1	0	0	0					8_
9A	.9ns	1	0	0	1					9_
10A	1.0ns	1	0	1	0					A_
11A	1.1ns	1	0	1	1					B_
12A	1.2ns	1	1	0	0					C_
13A	RFU	1	1	0	1					D_
-	Undefined	1	1	1	1	1	1	1	1	FF

Byte 32: SDRAM Setup Time Before Clock, Subfield B: Hundredths of Nanoseconds (Bits 0-3)										
Line #	**Access from Clock**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**	Hex
0B	+0ns	See Subfield A				0	0	0	0	_0
1B	+.01ns					0	0	0	1	_1
2B	+.02ns					0	0	1	0	_2
3B	+.03ns					0	0	1	1	_3
4B	+.04ns					0	1	0	0	_4
5B	+.05ns					0	1	0	1	_5
6B	+.06ns					0	1	1	0	_6
7B	+.07ns					0	1	1	1	_7
8B	+.08ns					1	0	0	0	_8
9B	+.09ns					1	0	0	1	_9
10B	RFU					1	0	1	0	_A
11B	–	-	-	-	-	-	-	-	-	-
-	Undefined	1	1	1	1	1	1	1	1	FF

Byte 33: Address and Command Hold Time After Clock (tIH)

This field describes the input hold time after the rising edge of the clock. The byte is broken into two nibbles: the higher order nibble (bits 4-7) designate the access time to a granularity of 0.1ns; the value presented by the lower order nibble (bits 0-3) has the granularity of .01ns and is added to the value designated by the higher nibble. For example:

if bits 7:4 are	and bits 3:0 are	then the total time is:
1011 (1.1ns)	0000 + (0ns)	= 1.1ns
1100 (1.2ns)	0101 + (0.05ns)	= 1.25ns

Byte 33: SDRAM Hold Time After Clock, Subfield A: Tenths of Nanoseconds (Bits 4-7)										
Line #	**Access from Clock**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**	**Hex**
0A	Undefined	0	0	0	0	See Subfield B				0_
1A	.1ns	0	0	0	1					1_
2A	.2ns	0	0	1	0					2_
3A	.3ns	0	0	1	1					3_
4A	.4ns	0	1	0	0					4_
5A	.5ns	0	1	0	1					5_
6A	.6ns	0	1	1	0					6_
7A	.7ns	0	1	1	1					7_
8A	.8ns	1	0	0	0					8_
9A	.9ns	1	0	0	1					9_
10A	1.0ns	1	0	1	0					A_
11A	1.1ns	1	0	1	1					B_
12A	1.2ns	1	1	0	0					C_
13A	RFU	1	1	0	1					D_
-	Undefined	1	1	1	1	1	1	1	1	FF

Byte 33: SDRAM Hold Time After Clock, Subfield B: Hundredths of Nanoseconds (Bits 0-3)										
Line #	**Access from Clock**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**	Hex
0B	+0ns	See Subfield A				0	0	0	0	_0
1B	+.01ns					0	0	0	1	_1
2B	+.02ns					0	0	1	0	_2
3B	+.03ns					0	0	1	1	_3
4B	+.04ns					0	1	0	0	_4
5B	+.05ns					0	1	0	1	_5
6B	+.06ns					0	1	1	0	_6
7B	+.07ns					0	1	1	1	_7
8B	+.08ns					1	0	0	0	_8
9B	+.09ns					1	0	0	1	_9
10B	RFU					1	0	1	0	_A
11B	–	-	-	-	-	-	-	-	-	-
-	Undefined	1	1	1	1	1	1	1	1	FF

Byte 34: Data Input Setup Time Before Strobe (tDS)

This field describes the input setup time before the rising edge of the strobe. The byte is broken into two nibbles: the higher order nibble (bits 4-7) designates the time to a granularity of 0.1ns; the value presented by the lower order nibble (bits 0-3) has the granularity of .01ns and is added to the value designated by the higher nibble. For example:

if bits 7:4 are	and bits 3:0 are	then the total time is:
0010	0101	
(0.2ns)	+(0.05ns)	= 0.25ns

Byte 34: SDRAM Setup Time Before Strobe, Subfield A: Tenths of Nanoseconds (Bits 4-7)										
Line #	**Access from Clock**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**	**Hex**
0A	Undefined	0	0	0	0	See Subfield B				0_
1A	.1ns	0	0	0	1					1_
2A	.2ns	0	0	1	0					2_
3A	.3ns	0	0	1	1					3_
4A	.4ns	0	1	0	0					4_
5A	.5ns	0	1	0	1					5_
6A	.6ns	0	1	1	0					6_
7A	.7ns	0	1	1	1					7_
8A	.8ns	1	0	0	0					8_
9A	.9ns	1	0	0	1					9_
10A	RFU	1	0	1	0					A_
11A	-	1	0	1	1					-
-	Undefined	1	1	1	1	1	1	1	1	FF

Byte 34: SDRAM Setup Time Before Strobe, Subfield B: Hundredths of Nanoseconds (Bits 0-3)										
Line #	**Access from Clock**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**	Hex
0B	+0ns	See Subfield A				0	0	0	0	_0
1B	+.01ns					0	0	0	1	_1
2B	+.02ns					0	0	1	0	_2
3B	+.03ns					0	0	1	1	_3
4B	+.04ns					0	1	0	0	_4
5B	+.05ns					0	1	0	1	_5
6B	+.06ns					0	1	1	0	_6
7B	+.07ns					0	1	1	1	_7
8B	+.08ns					1	0	0	0	_8
9B	+.09ns					1	0	0	1	_9
10B	RFU					1	0	1	0	_A
11B	–	-	-	-	-	-	-	-	-	-
-	Undefined	1	1	1	1	1	1	1	1	FF

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Byte 35: Data Input Hold Time After Strobe (tDH)

This field describes the input hold time after the rising edge of the strobe. The byte is broken into two nibbles: the higher order nibble (bits 4-7) designate the time to a granularity of 0.1ns; the value presented by the lower order nibble (bits 0-3) has the granularity of .01ns and is added to the value designated by the higher nibble. For example:

if bits 7:4 are	and bits 3:0 are	then the total time is:
0010	0101	
(0.2ns)	+ (0.05ns)	= 0.25ns

Byte 35: SDRAM Hold Time After Strobe, Subfield A: Tenths of Nanoseconds (Bits 4-7)										
Line #	**Access from Clock**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**	**Hex**
0A	Undefined	0	0	0	0	See Subfield B				0_
1A	.1ns	0	0	0	1					1_
2A	.2ns	0	0	1	0					2_
3A	.3ns	0	0	1	1					3_
4A	.4ns	0	1	0	0					4_
5A	.5ns	0	1	0	1					5_
6A	.6ns	0	1	1	0					6_
7A	.7ns	0	1	1	1					7_
8A	.8ns	1	0	0	0					8_
9A	.9ns	1	0	0	1					9_
10A	RFU	1	0	1	0					A_
11A	-	1	0	1	1					-
-	Undefined	1	1	1	1	1	1	1	1	FF

Byte 35: SDRAM Hold Time After Strobe, Subfield B: Hundredths of Nanoseconds (Bits 0-3)										
Line #	**Access from Clock**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**	Hex
0B	+0ns	See Subfield A				0	0	0	0	_0
1B	+.01ns					0	0	0	1	_1
2B	+.02ns					0	0	1	0	_2
3B	+.03ns					0	0	1	1	_3
4B	+.04ns					0	1	0	0	_4
5B	+.05ns					0	1	0	1	_5
6B	+.06ns					0	1	1	0	_6
7B	+.07ns					0	1	1	1	_7
8B	+.08ns					1	0	0	0	_8
9B	+.09ns					1	0	0	1	_9
10B	RFU					1	0	1	0	_A
11B	–	-	-	-	-	-	-	-	-	-
-	Undefined	1	1	1	1	1	1	1	1	FF

Byte 36: Write Recovery Time (t_{WR})

This byte describes the write recovery time(t_{WR})

Byte 36 is split into two pieces: the higher order bits (bits 2-7) designate the time to a granularity of 1ns; the value presented by the lower order bits (bits 0-1) has a granularity of .25ns and is added to the value designated by the higher bits. For example:

if bits 7:2 are	and bits 1:0 are	then the total time is
001111 (15ns)	00 +(0.0ns)	= 15.0ns
010010 (18ns)	11 +(.75ns)	= 18.75ns

Byte 36, SDRAM Minimum t_{WR} Time, Subfield A: Whole Nanoseconds (Bits 2-7)								
Nanoseconds	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Undefined	0	0	0	0	0	0	See Subfield B	
1ns	0	0	0	0	0	1		
2ns	0	0	0	0	1	0		
3ns	0	0	0	0	1	1		
4ns	0	0	0	1	0	0		
5ns	0	0	0	1	0	1		
6ns	0	0	0	1	1	0		
7ns	0	0	0	1	1	1		
8ns	0	0	1	0	0	0		
9ns	0	0	1	0	0	1		
10ns	0	0	1	0	1	0		
:	:	:	:	:	:	:		
:	:	:	:	:	:	:		
61ns	1	1	1	1	0	1		
62ns	1	1	1	1	1	0		
63ns	1	1	1	1	1	1		

Byte 36, SDRAM Minimum t_{WR} Time, Subfield B: Quarters of Nanoseconds (Bits 0-1)								
Access from Clock	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
+0ns	See Subfield A						0	0
+.25ns							0	1
+.50ns							1	0
+.75ns							1	1

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Byte 37: Internal write to read command delay (t_{WTR})

This byte describes the internal write to read command delay(t_{WTR})

Byte 37 is split into two pieces: the higher order bits (bits 2-7) designate the time to a granularity of 1ns; the value presented by the lower order bits (bits 0-1) has a granularity of .25ns and is added to the value designated by the higher bits. For example:

if bits 7:2 are	and bits 1:0 are	then the total time is
001010 (10ns)	00 +(0.0ns)	= 10.0ns
000111 (7ns)	10 +(.50ns)	= 7.5ns

Byte 37, SDRAM Minimum t_{WTR} Time, Subfield A: Whole Nanoseconds (Bits 2-7)								
Nanoseconds	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Undefined	0	0	0	0	0	0	See Subfield B	
1ns	0	0	0	0	0	1		
2ns	0	0	0	0	1	0		
3ns	0	0	0	0	1	1		
4ns	0	0	0	1	0	0		
5ns	0	0	0	1	0	1		
6ns	0	0	0	1	1	0		
7ns	0	0	0	1	1	1		
8ns	0	0	1	0	0	0		
9ns	0	0	1	0	0	1		
10ns	0	0	1	0	1	0		
:	:	:	:	:	:	:		
:	:	:	:	:	:	:		
61ns	1	1	1	1	0	1		
62ns	1	1	1	1	1	0		
63ns	1	1	1	1	1	1		

Byte 37, SDRAM Minimum t_{WTR} Time, Subfield B: Quarters of Nanoseconds (Bits 0-1)								
Access from Clock	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
+0ns	See Subfield A						0	0
+.25ns							0	1
+.50ns							1	0
+.75ns							1	1

Byte 38: Internal read to precharge command delay (t_{RTP})

This byte describes internal read to precharge command delay (t_{RTP})

Byte 38 is split into two pieces: the higher order bits (bits 2-7) designate the time to a granularity of 1ns; the value presented by the lower order bits (bits 0-1) has a granularity of .25ns and is added to the value designated by the higher bits. For example:

if bits 7:2 are	and bits 1:0 are	then the total time is
001010 (10ns)	00 +(0.0ns)	= 10.0ns
000111 (7ns)	10 +(.50ns)	= 7.5ns

Byte 38, SDRAM Minimum t_{RTP} Time, Subfield A: Whole Nanoseconds (Bits 2-7)								
Nanoseconds	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Undefined	0	0	0	0	0	0	See Subfield B	
1ns	0	0	0	0	0	1		
2ns	0	0	0	0	1	0		
3ns	0	0	0	0	1	1		
4ns	0	0	0	1	0	0		
5ns	0	0	0	1	0	1		
6ns	0	0	0	1	1	0		
7ns	0	0	0	1	1	1		
8ns	0	0	1	0	0	0		
9ns	0	0	1	0	0	1		
10ns	0	0	1	0	1	0		
:	:	:	:	:	:	:		
:	:	:	:	:	:	:		
61ns	1	1	1	1	0	1		
62ns	1	1	1	1	1	0		
63ns	1	1	1	1	1	1		

Byte 38, SDRAM Minimum t_{RTP} Time, Subfield B: Quarters of Nanoseconds (Bits 0-1)								
Access from Clock	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
+0ns	See Subfield A						0	0
+.25ns							0	1
+.50ns							1	0
+.75ns							1	1

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Byte 39: Memory Analysis Probe Characteristics

This byte describes various functional and parametric characteristics of the memory analysis probe connected to this DIMM slot. These characteristics may be consulted by the BIOS to determine proper bus drive strength to account for additional bus loading of the probe. It also describes functional characteristics of the probe that may be used to configure the memory controller to drive proper diagnostic signals to the probe, such as via the TEST,NC pin

Detailed Features: TBD

Byte 40: Extension of Byte 41 tRC and Byte 42 tRFC

This field describes the extension of Byte 41 tRC and Byte 42 tRFC.

For example:

if module tRFC is:	byte 40								byte 42							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
127.5ns	0	X	X	X	0	1	1	0	0	1	1	1	1	1	1	1
327.5ns	0	X	X	X	0	1	1	1	0	1	0	0	0	1	1	1
if module tRC is:	**byte 40**								**byte 41**							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
63.75ns	0	1	0	1	X	X	X	X	0	0	1	1	1	1	1	1
65ns	0	0	0	0	X	X	X	X	0	1	0	0	0	0	0	1

Byte 40: Subfield A, Extension of Byte 42 tRFC (Bits 0)									
Line #	Minimum Auto refresh to Acitve/Auto refresh Command Period MSB	Bit 7 TBD	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0A	Undefined	0	See Subfield C			See Subfield B			0
1A	256ns+byte 42	0							1

Byte 40: Subfield B, Extension of Byte 42 tRFC (Bits 1-3)									
Line #	Minimum Auto refresh to Active/Auto refresh Command Period LSB	Bit 7 TBD	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0B	+0ns+byte 42	0	See Subfield C			0	0	0	See Subfield A
1B	+.25ns+byte 42	0				0	0	1	
2B	+.33ns+byte 42	0				0	1	0	
3B	+.5ns+byte 42	0				0	1	1	
4B	+.66ns+byte 42	0				1	0	0	
5B	+.75ns+byte 42	0				1	0	1	
6B	RFC	0				1	1	0	
-	Undefined	0				1	1	1	

Byte 40: Subfield C, Extension of Byte 41 tRC (Bits 4-6)									
Line #	Minimum Active to Active refresh Command Period LSB	Bit 7 TBD	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0C	+0ns+byte 41	0	0	0	0	See Subfield B			See Subfield A
1C	+.25ns+byte 41	0	0	0	1				
2C	+.33ns+byte 41	0	0	1	0				
3C	+.5ns+byte 41	0	0	1	1				
4C	+.66ns+byte 41	0	1	0	0				
5C	+.75ns+byte 41	0	1	0	1				
6C	RFC	0	1	1	0				
-	Undefined	0	1	1	1				

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Byte 41: SDRAM Device Minimum Active to Active/Auto Refresh Time (t_{RC})

This byte identifies the minimum active to active or auto refresh time with Byte 40 as extension.

For example:

if module tRC is:	byte 40								byte 41							
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit1	Bit 0
63.75ns	0	1	0	1	X	X	X	X	0	0	1	1	1	1	1	1
65ns	0	0	0	0	X	X	X	X	0	1	0	0	0	0	0	1

Byte 41									
Minimum Active to Active/Auto Refresh Time (ns)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
Undefined	0	0	0	0	0	0	0	0	00
1	0	0	0	0	0	0	0	1	01
2	0	0	0	0	0	0	1	0	02
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
25	0	0	0	1	1	0	0	1	19
26	0	0	0	1	1	0	1	0	1A
27	0	0	0	1	1	0	1	1	1B
28	0	0	0	1	1	1	0	0	1C
29	0	0	0	1	1	1	0	1	1D
30	0	0	0	1	1	1	1	0	1E
31	0	0	0	1	1	1	1	1	1F
32	0	0	1	0	0	0	0	0	20
33	0	0	1	0	0	0	0	1	21
34	0	0	1	0	0	0	1	0	22
35	0	0	1	0	0	0	1	1	23
36	0	0	1	0	0	1	0	0	24
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
127	0	1	1	1	1	1	1	1	7F
128	1	0	0	0	0	0	0	0	80
.	.	.	.	.	.	.	.	.	.
.	.	.	.		.	.	.	.	.
254	1	1	1	1	1	1	1	0	FE
Undefined	1	1	1	1	1	1	1	1	80

Byte 42: SDRAM Device Minimum Auto-Refresh to Active/Auto-Refresh Command Period (tRFC)

This byte identifies the minimum Auto-Refresh to Active/Auto-Refresh Command Period (tRFC) with Byte 40 as extension.

For example:

If the module's tRFC is:	then Byte 40 is:	and Byte 42 is:
75	0XXX 0000	0100 1011
105	0XXX 0000	0110 1001
127.5	0XXX 0110	0111 1111
195	0XXX 0000	1100 0011
327.5	0XXX 0111	0100 0111

Byte 42									
Minimum Auto-Refresh to Active/Auto-Refresh Command Period (ns)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
Undefined	0	0	0	0	0	0	0	0	00
1	0	0	0	0	0	0	0	1	01
2	0	0	0	0	0	0	1	0	02
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
25	0	0	0	1	1	0	0	1	19
26	0	0	0	1	1	0	1	0	1A
27	0	0	0	1	1	0	1	1	1B
28	0	0	0	1	1	1	0	0	1C
29	0	0	0	1	1	1	0	1	1D
30	0	0	0	1	1	1	1	0	1E
31	0	0	0	1	1	1	1	1	1F
32	0	0	1	0	0	0	0	0	20
33	0	0	1	0	0	0	0	1	21
34	0	0	1	0	0	0	1	0	22
35	0	0	1	0	0	0	1	1	23
36	0	0	1	0	0	1	0	0	24
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
127	0	1	1	1	1	1	1	1	7F
128	1	0	0	0	0	0	0	0	80
.	.	.	.	.	.	.	.	.	.
.	.	.	.		.	.	.	.	.
254	1	1	1	1	1	1	1	0	FE
255	1	1	1	1	1	1	1	1	FF

Byte 43: SDRAM Device Maximum Device Cycle Time (tCK max)

This byte identifies the maximum device cycle time at any $\overline{CAS}$ latency. Byte 43 is split into two nibbles: the higher order nibble (bits 4-7) designates the cycle time to a granularity of 1ns; the value presented by the lower order nibble (bits 0-3) has a granularity of .1ns and is added to the value designated by the higher nibble. In addition, four lines of the lower order nibble are assigned to support +.25,+.33, +.66 and +.75.

For example:

If bits 7:4 are	and bits 3:0 are	then the total time is:
1000	0000	
(8ns)	+ (0ns)	= 8.0ns

Byte 43, SDRAM Maximum Cycle Time, Subfield A: Whole Nanoseconds (Bits 4-7)										
Line #	Cycle Time	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
0A	Undefined	0	0	0	0	See Subfield Table B				0_
1A	1ns	0	0	0	1					1_
2A	2ns	0	0	1	0					2_
3A	3ns	0	0	1	1					3_
4A	4ns	0	1	0	0					4_
5A	5ns	0	1	0	1					5_
6A	6ns	0	1	1	0					6_
7A	7ns	0	1	1	1					7_
8A	8ns	1	0	0	0					8_
9A	9ns	1	0	0	1					9_
10A	10ns	1	0	1	0					A_
11A	11ns	1	0	1	1					B_
12A	12ns	1	1	0	0					C_
13A	13ns	1	1	0	1					D_
14A	14ns	1	1	1	0					E_
15A	15ns	1	1	1	1					F_
-	Undefined	1	1	1	1	1	1	1	1	FF

Byte 43, SDRAM Maximum Cycle Time Subfield B: Tenths of Nanoseconds (Bits 0-3)										
Line #	Cycle Time	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
0B	+0ns	See Subfield Table B				0	0	0	0	_0
1B	+.1ns					0	0	0	1	_1
2B	+.2ns					0	0	1	0	_2
3B	+.3ns					0	0	1	1	_3
4B	+.4ns					0	1	0	0	_4
5B	+.5ns					0	1	0	1	_5
6B	+.6ns					0	1	1	0	_6
7B	+.7ns					0	1	1	1	_7
8B	+.8ns					1	0	0	0	_8
9B	+.9ns					1	0	0	1	_9
10B	+.25ns					1	0	1	0	_A
11B	+.33ns					1	0	1	1	_B
12B	+.66ns					1	1	0	0	_C
13B	+.75ns					1	1	0	1	_D
-	-	-	-	-	-	-	-	-	-	-
-	Undefined	1	1	1	1	1	1	1	1	FF

Byte 44: SDRAM Device DQS-DQ Skew for DQS and associated DQ signals (tDQSQ max)

This byte identifies the maximum skew between DQS and all DQ signals for each device, in hundredths of nanoseconds.

Maximum Device DQS-DQ Skew (1/100 ns)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
Undefined	0	0	0	0	0	0	0	0	00
0.01	0	0	0	0	0	0	0	1	01
0.02	0	0	0	0	0	0	1	0	02
0.03	0	0	0	0	0	0	1	1	03
0.04	0	0	0	0	0	1	0	0	04
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
0.50	0	0	1	1	0	0	1	0	32
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
0.60	0	0	0	1	1	1	1	0	1E
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
2.54	1	1	1	1	1	1	1	0	FE
2.55	1	1	1	1	1	1	1	1	FF

Byte 45: SDRAM Device Read Data Hold Skew Factor (tQHS)

This byte identifies the skew factor used in the calculation of read data hold time from edges of DQS, specifically tQH=tHP-tQHS where tQHS is the read data hold skew factor. This SPD byte is split into two nibbles: the higher order nibble(bits 4-7) designate the access time to a granularity of 0.1 ns; the value presented by the lower order nibble (bits 0-3) has the granularity of .01 ns and is added to the value designated by the higher nibble. For example:

Read data Hold Skew Factor(tQHS)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
Undefined	0	0	0	0	0	0	0	0	00
0.01	0	0	0	0	0	0	0	1	01
0.02	0	0	0	0	0	0	1	0	02
0.03	0	0	0	0	0	0	1	1	03
0.04	0	0	0	0	0	1	0	0	04
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
0.50	0	0	1	1	0	0	1	0	32
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
0.60	0	0	0	1	1	1	1	0	1E
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
2.54	1	1	1	1	1	1	1	0	FE
2.55	1	1	1	1	1	1	1	1	FF

Byte 46: PLL Relock Time

This byte describes the relock time of PLLs on the clock inputs.

PLL Relock Time (μs)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Hex
Undefined	0	0	0	0	0	0	0	0	00
1	0	0	0	0	0	0	0	1	01
2	0	0	0	0	0	0	1	0	02
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
25	0	0	0	1	1	0	0	1	19
26	0	0	0	1	1	0	1	0	1A
27	0	0	0	1	1	0	1	1	1B
28	0	0	0	1	1	1	0	0	1C
29	0	0	0	1	1	1	0	1	1D
30	0	0	0	1	1	1	1	0	1E
31	0	0	0	1	1	1	1	1	1F
32	0	0	1	0	0	0	0	0	20
33	0	0	1	0	0	0	0	1	21
34	0	0	1	0	0	0	1	0	22
35	0	0	1	0	0	0	1	1	23
36	0	0	1	0	0	1	0	0	24
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
127	0	1	1	1	1	1	1	1	7F
128	1	0	0	0	0	0	0	0	80
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
254	1	1	1	1	1	1	1	0	FE
255	1	1	1	1	1	1	1	1	FF

Bytes 47- xx: Reserved for Idd in SPD

Bytes (xx + 1) - 61: Reserved

Netlist EX2031-p. 41
Samsung et al. v Netlist
IPR2023-00455
Samsung Ex. 1107, p. 41
Samsung Electronics Co., Ltd. v. Netlist, Inc., IPR2022-00615

Byte 62: SPD Revision

This byte describes the compatibility level of the encoding of the bytes contained in the SPD EEPROM, and the current collection of valid defined bytes. This byte must be coded as 10h for SPDs with revision level 1.0. Software should examine the upper nibble(Encoding Level) to determine if it can correctly interpret the contents of the module SPD. The lower nibble (Additions Level) can optionally be used to determine which additional bytes or attribute bits have been defined; however, since any undefined additional byte must be encoded as 00h or undefined attribute bit must be defined as 0, software can safely detect additional bytes and use safe defaults if a zero encoding is read for these bytes.

SPD Revision	Encoding Level				Additions Level				Hex
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
Revision 0.0	0	0	0	0	0	0	0	0	00
Undefined	0	0	0	0	0	0	0	1	01
...	.	.	.	.	.	.	.	.	.
Revision 1.0	0	0	0	1	0	0	0	0	10
Undefined	0	0	0	0	0	0	0	1	11
...	.	.	.	.	.	.	.	.	...
Undefined	1	1	1	1	1	1	1	1	FF

Byte 63: Checksum for Bytes 0-62

This field designates the checksum for checking data integrity (similar to parity) for bytes 0 - 62. It is written during module production and can be used by the customer to verify the data integrity for these bytes.

Process for Calculating the Checksum

1. Convert binary information, in byte locations 0 - 62, to decimal.
2. Add together (sum) all decimal values for addresses 0 - 62.
3. Divide sum by 256.
4. Convert remainder to binary (will be less than 256).
5. Store result (single byte) in address 63 as “Checksum.”

Note: The same result can be obtained by adding the binary values in addresses 0 - 62 and eliminating all but the low order byte. The low order byte is the “Checksum.”

Example of a Checksum Calculation

SPD Byte Address	Serial PD		Convert to Decimal
0	0010 0100	→	36
1	1111 1110	→	+254
2	0000 0000	→	+ 0
3	0000 0000	→	+ 0
↓	↓	→	+ 0
		→	+ 0
60	0000 0000	→	+ 0
61	0000 0000	→	+ 0
62	0000 0000	→	+ 0
Decimal Total	-	-	290
Divide by 256	-	-	1
Remainder	-	-	34
Convert to binary	0010 0010	←	34
63 (Checksum)	0010 0010	-	-

Bytes 64-71: Module Manufacturer’s JEDEC ID Code

Manufacturers of a given module may include their identifier according to JEDEC spec JEP106. The first byte is utilized, the second byte is filled with zeros. For example, a company whose value is hexadecimal CE would be coded as: “CE000000 00000000.”

Byte 72: Module Manufacturing Location

Manufacturers may include an identifier that uniquely defines the manufacturing location of the memory module. While the SPD spec will not attempt to present a decode table for manufacturing sites, the individual manufacturer may keep track of manufacturing location and its appropriate decode represented in this byte.

Bytes 73-90: Module Part Number

The manufacturer's part number is written in ASCII format within these bytes. Unused digits are coded as ASCII blanks (20h).

Bytes 91-92: Module Revision Code

This refers to the module revision code. While the SPD spec will not attempt to define the format for this information, the individual manufacturer may keep track of the revision code and its appropriate decode represented in this byte.

Bytes 93-94: Module Manufacturing Date

The module manufacturer may include a date code for the module. The JEDEC definitions of bytes 93 and 94 are year and week, respectively. These bytes are coded in binary with year starting from the year of 2000, which is coded as 00h (byte 93). For example, week 19 in 2002 would be coded as 02h (byte 93) and 13h (byte 94).

Bytes 95-98: Module Serial Number

The supplier must include a unique serial number for the module. The supplier may use whatever decode method desired to maintain a unique serial number for each module.

Bytes 99-127: Manufacturer's Specific Data

The module manufacturer may include any additional information desired into the module within these locations.

Bytes 128-255: Open for Customer Use

These bytes are unused by the manufacturer and are open for customer use.

Appendix: ASCII Decode Matrix for SPDs

The following table is a subset of the full ASCII standard which is used for coding bytes in the Serial Presence Detect EEPROM that require ASCII characters:

	Second Hex Digit in Pair															
First Hex Digit in Pair	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
2	Blank Space								(	)				- Dash		
3	0	1	2	3	4	5	6	7	8	9						
4		A	B	C	D	E	F	G	H	I	J	K	L	M	N	O
5	P	Q	R	S	T	U	V	W	X	Y	Z					
6		a	b	c	d	e	f	g	h	i	j	k	l	m	n	o
7	p	q	r	s	t	u	v	w	x	y	z					

Examples:

20h=Blank Space
34h=4
41h=A

SPD Bytes 73-90	
Manufacturer's PN	Coded in ASCII
13M32734BCD-260Y	31334D33323733344243442D323630592020