UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.,
Petitioner
v.
NETLIST, INC.,
Patent Owner

Case No. IPR2023-00454
Patent No. 11,093,417
- and -
Case No. IPR2023-00455
Patent No. 9,858,215

REMOTE DEPOSITION
DR. ANDREW WOLFE

DATE TAKEN: NOVEMBER 5, 2023
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SAMSUNG ELECTRONICS CO., LTD.,

Petitioner

v.

NETLIST, INC.,

Patent Owner

_____

Case No. IPR2020-01624

Patent No. 6,975,132

Remote Deposition of DR. ANDREW WOLFE, the witness herein, at 9:02 Pacific Daylight Time, on Saturday, November 5, 2023, appearing remotely from Santa Clara, California before Renee Harris, California Certified Shorthand Reporter No. 14168, New Jersey Certified Court Reporter No. 30XI00241200, and Registered Professional Reporter.

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PREVIOUSLY MARKED EXHIBITS REFERENCED

EXHIBIT NO.	DESCRIPTION
1001	U.S. Patent No. 9,858,215
1001	U.S. Patent No. 9,858,215
1001	U.S. Patent No. 11,093,417
1003	Declaration, Dr. Wolfe, '215
1003	Declaration, Dr. Wolfe, '417
1062	JEDEC JESD21-C design specification for DDR SDRAM RDIMM (January 2002)
1064	JEDEC JESD79-2 DDR2 standard (September 2003)
1071	U.S. Patent No. 7,363,422 (Perego)
1072	U.S. Patent No. 7,155,627 (Matsui)
1073	U.S. Patent No. 2006/0277355 (Ellsberry)
1074	U.S. Patent No. 7,024,518 (Halbert)

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SANTA CLARA, CALIFORNIA;

SATURDAY, NOVEMBER 5, 2023, 9:02 A.M.;

DR. ANDREW WOLFE,

called as a witness and having been first duly sworn by the Certified Shorthand Reporter, was examined and testified as follows:

EXAMINATION

BY MR. WARRICK:

Q. Good morning, Dr. Wolfe.

I believe you said you have access to the exhibits. I'd like to start off with your declaration in the IPR dealing with the '417 patent. It should be Exhibit 1003. Note the '417 patent in the title.

Do you see that?

A. I do.

Q. And if you could go to paragraph 126 in there, please. It's on page 104.

A. Yes.

Q. And could you just read for us paragraph 126. It's short.

A. "In my opinion, a Skilled Artisan would have understood that the term 'rank' refers to an

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independent set of one or more memory devices on a memory module that act together in response to command signals, including chip select signals, to read or write the full bit-width of the memory module."

Q. Thank you.

And that is the construction that you've endorsed for the term "rank" in the '417 patent; correct?

A. Correct.

Q. And that's also the construction you've endorsed for the '215 patent; correct?

A. Correct.

Q. I'd like to spend a little bit of time with this. Starting with the words "act together," could you explain to me what you mean in your proposed construction by saying that the memory devices must "act together"?

A. Well, you need to read it in context. Since a rank can be one or more memory devices, "act together" means that they are not responding independently, separately to command signals. Which, of course, if you only have one, is natural and would always happen. And if you have more than one, you would have to configure the memory

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devices so that they respond together to command signals.

Q. When you say "respond together," I guess I'm not sure what that means beyond "act together."

Does that -- does that mean they have to respond at the same time? Does it mean something more than that?

A. I think to a skilled artisan they would interpret that in a reasonable manner. So it does not have -- nothing -- no two things ever happen at the exact same instant in time. That's the world we live in. But they would respond in approximately the same time. They would attempt to respond in the same time. And they would respond in a coordinated way.

I mean, the -- again, a person of ordinary skill would use the rank to describe something that's ordinarily and commonly done, not to try to bizarrely limit the field through their use of that word. It's a word that -- that was not created as part of a standards effort or as part of a definitional effort. It was a descriptive word that grew among practitioners to describe the ordinary way that they did things.

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And when they connected one or more memory devices in a way that those memory devices would respond together to command signals, while some other memory devices, one or more, in a different rank, might respond separately to command signals, the word "rank" was used to distinguish one set of one or more memory devices from another set of one or more memory devices.

Q. Dr. Wolfe, do you disagree that the term "rank" arose out of the JEDEC standards and related proceedings?

A. I believe I do, depending by what you mean by "arose out of."

My recollection and my understanding is that because at that time, there were two slightly different memory organizations or structures that were being referred to as "banks" during the late '70s through the '90s, that some engineers at certain companies started to distinguish those by calling groups of memory cells on a chip a "bank" and calling groups of memory cells that were distinguishing between chips a "rank."

And when JEDEC began to update their standards, some of that vocabulary migrated from common usage into the JEDEC standard.

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Q. So you agree that a "bank" and a "rank" are different terms; they don't mean the same thing?

MR. CHANDLER: Object to form.

THE WITNESS: It depends under what context and what time. Certainly, what today most people would call a "rank," when I started developing computer systems, most people called a "bank." And even today, some of us who are older will often refer to the structure that many people call a "rank" today as a "bank" because historically the term was used for that structure of one or more memory devices on a memory module that act together.

That term "rank" is -- and the term "bank" can also in certain contexts used to refer to sets of memory modules in certain computing systems.

So you really have to look at the context and the time frame.

BY MR. WARRICK:

Q. But you would agree that the term "bank" does not imply a rank; right?

MR. CHANDLER: Objection. Form.

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THE WITNESS: Again, it depends on the context, and it depends on the time frame.

BY MR. WARRICK:

Q. Let me put it differently.

It sounds like from what you've said that something that fits your understanding of a rank may also qualify as a bank; right?

A. It depends on the context and a time frame.

Q. But a set of memory devices that qualify as a "bank" with a "b" are not necessarily a "rank" with an "r"; correct?

MR. CHANDLER: Objection. Form.

THE WITNESS: It depends on the context and a time frame.

BY MR. WARRICK:

Q. Is there a situation where the term "bank" necessarily implies a rank, to your knowledge?

A. I don't know what you mean by "necessarily implies." But I certainly could read descriptions of computer systems in the mid-'80s or early '90s that used the term "bank" to refer to what in certain JEDEC standards is today called a "rank."

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Q. I want to go back to something you said earlier about your construction of rank.

You said that the memory devices would respond in a coordinated way.

When you say a "coordinated way," does that mean that there is some type of communication between the memory devices on the memory module?

MR. CHANDLER: Objection. Form.

THE WITNESS: Not necessarily and not commonly, no.

BY MR. WARRICK:

Q. So what does it mean, in your view, for the memory devices to respond in a "coordinated way"?

A. Each memory device might have a different role. For example, one memory device might have to output Bits 0 through 3 while another memory device is outputting Bits 4 through 7.

So they are not doing exactly the same thing, but they are working in coordination in response to the same command signals, responding at approximately the same time, in order to provide Bits 0 through 7 together.

Q. So memory devices that are responding to the same command signals and responding at

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approximately the same time qualify as a rank in your view?

A. No. I've given a complete definition. And again, that's with respect to these patents, the way the word "rank" is used in these patents, in the context of these patents. And the definition would be read by a person of ordinary skill applying some common sense.

So one or more memory devices on a memory module act together in response to command signals, including chip select signals, to read or write the full width of the memory module is something that is ordinarily and commonly called a "rank" in the industry at the time of these patents.

Q. Well, you mentioned earlier that your construction was specific to the context of these patents that are at issue in these two IPRs.

How does that definition differ from what you would called the ordinary understanding in the art of the term "rank"?

A. It is an ordinary understanding in the art of the term "rank." Like many words, "rank" can mean different things in different contexts. It doesn't always have to refer to memories. It

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can refer to people. You know, it's a word that can have different meanings.

And in the context of memory of modules, this is the ordinary meaning.

Q. Your construction also includes the term "independent set." Can you explain for me what you mean by an "independent set" of memory devices.

A. It's really just what I said before, is that it would be common in a computer system that you would have one or more memory devices that are acting together and that also have one or more memory devices that are acting separately.

So when I use the word "independent," I'm identifying that a rank is the one or more memory devices that work together, as distinct from another rank, which would be the other one or more memory devices that operate separately.

So those two ranks are operating independently from each other in the sense that they are not responding at the same time to the same command signals.

Q. So in your view, does the -- does the rank have anything to do with how the memory devices are physically connected in the memory

system?

A. Well, in practice, the way that memory devices respond to signals always has to do with how they are physically connected.

Q. But assuming they are connected such that they can respond to signals, say, from a controller or a buffer and they can do so in what you call a "coordinated way," that would qualify as a rank under your construction, regardless of how they are specifically connected; correct?

MR. CHANDLER: Objection. Form.

THE WITNESS: I don't know. You'd have to show me an example. You know, typically, if you move the connections around to a memory system, it will respond differently. So you would have to re-analyze it.

BY MR. WARRICK:

Q. But if they respond in approximately the same time in response to the same command signals, then those memory devices would be a rank, under your view; correct?

MR. CHANDLER: Objection. Form.

THE WITNESS: Well, in this case, we are talking about the meaning of the term "rank" with respect to memory modules, so they would

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have to be on a memory module.

BY MR. WARRICK:

Q. Okay. So assuming they are on the memory module and they are responding at approximately the same time to the same command signals, then those memory devices would be a rank, under your proposed construction in this case?

MR. CHANDLER: Object to form.

THE WITNESS: Not necessarily. You're leaving out part of my construction. It would have to be -- to respond together to command signals, including chip select signals, to read or write the full bit width of the memory module.

BY MR. WARRICK:

Q. Okay. So maybe we can try this differently.

If a set of memory devices are on the memory module and they respond in approximately the same time to the same command signals, including chip select signals, to read or write the full bit width of the memory module, then that would fit your definition of a "rank," at least for purposes of these patents; correct?

A. In an ordinary situation, it would be.

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If you're trying to describe something that's strange or unusual, I would have to see it to -- to know.

Again, these are -- these constructions are intended to be understood by a reasonable person who is familiar with the art.

Q. But, Dr. Wolfe, you do understand that in proceedings like in inter partes review proceeding before the Patent and Trademark Office, the claim constructions, in part, are to assist the administrative patent judges in understanding the meaning of the patents; isn't that right?

MR. CHANDLER: Objection.

THE WITNESS: I do understand that, and that is the intent here.

BY MR. WARRICK:

Q. And those administrative patent judges are not always persons of ordinary skill in the relevant art; correct?

A. That's correct. And they will be assisted by experts in applying this construction to the evidence. And -- but they are, I do believe, reasonable people.

Q. Dr. Wolfe, taking a step back, you understand -- strike that.

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Can you state your full name so we have it on the record, please.

A. Andrew Wolfe.

Q. And, Dr. Wolfe, you are testifying as an expert on behalf of the petitioner in these two IPRs; correct?

A. Yes. If we're talking about the same two IPRs, yes.

Q. Well, to be specific, IPR2023-454 involving the '417 patent and IPR2023-455, which involves the '215 patent.

A. Those are the IPRs that I'm here to testify about today.

Q. And you're testifying on behalf of Samsung Electronics Company; correct?

A. I believe that's the correct name of the entity, yes.

Q. And you understand you are under oath today?

A. I do.

Q. Any reason that you cannot give full, accurate, and truthful testimony today?

A. No. I have been struggling with bronchitis. If it flares up, I may need a break, but it should not affect any of my answers.

Q. Well, if you need a break, let me know. I just ask, as I suspect you're familiar, that if there's a pending question that you answer it first, and then we can take a break.

A. I will do my best.

Q. Let's take a look at the -- I'm sorry?

A. I didn't say anything.

Q. I'd like to look at the Perego patent. It should be in your folder as Exhibit 1071.

A. Okay.

Q. Great.

And let's go to Figure 4B on page 9 of Perego.

A. Okay.

Q. And first of all, you -- you recognize this document, don't you, Dr. Wolfe?

A. I do.

Q. This is one of the patents that you are alleging is a prior art that, in combination with other art, renders obvious the claims of the '417 and '215 patents?

A. Yes.

Q. So looking at Figure 4B of Perego, is it possible for you to tell me based solely on that figure how many ranks there are?

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MR. CHANDLER: Objection. Form.

THE WITNESS: I wouldn't even try to do that. Why would I try to interpret a figure in a patent without reading a description of it? That wouldn't make any sense.

BY MR. WARRICK:

Q. Fair enough.

So just -- so -- just so we are on the same page, you would have to read the accompanying description to understand how many ranks are depicted in Figure 4B of Perego; right?

A. I don't know if you would or if you wouldn't, but in a proceeding like this, it would be imprudent to attempt to interpret a document without reading it in the context of the reference as a whole.

Q. Now, you have read the entirety of the Perego reference; correct?

A. Yes.

Q. Having read it, how many -- how many ranks do you believe exist in Figure 4B of Perego?

A. I believe there's two; and I've indicated that on page 155 of my declaration.

MR. CHANDLER: And for clarity, you know, there are two IPRs. Be sure the question and

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answers refer to the specific IPR that you're referring to for an exhibit.

MR. WARRICK: Sure.

BY MR. WARRICK:

Q. Just so we're clear, when I'm asking questions about references such as Perego, my understanding is that your answers would be equally applicable in either IPRs; is that fair, Dr. Wolfe?

A. It depends on the question.

Q. So would you interpret Perego differently depending on the patent that it's being asserted against?

A. Not in terms of what it discloses; but in terms of how it applies to claim language, I might.

Q. Okay. You mentioned paragraph -- page 155 of your declaration.

Were you referring to your declaration in the '417 patent IPR?

A. Yes.

Q. And on page 155 of that declaration, you've added color-coding to Figure 4B; correct?

A. Correct.

Q. And that's not part of the original

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reference; correct?

A. The color-coding is not.

Q. Now, in your color-coding, the memory devices across the top of Figure 4B you've characterized as one rank, and the ones on the lower half of Figure 4B you've characterized as a separate rank; correct?

A. Correct.

Q. And is that because they are on separate channels?

MR. CHANDLER: Objection. Form.

THE WITNESS: I don't understand the question. Is what because they are on separate channels?

BY MR. WARRICK:

Q. Your characterization of Figure B as showing two ranks.

MR. CHANDLER: Objection. Form.

THE WITNESS: It's because of the way that they operate as described by Perego; and more specifically, how a person of ordinary skill would understand them to operate if, as Perego suggests, DDR2 memory devices were used in an embodiment.

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BY MR. WARRICK:

Q. But if we were to use Perego as depicted in Figure 4B -- well, back up. Strike that.

The memory devices depicted in Figure 4B are not SDRAM devices; correct?

MR. CHANDLER: Objection. Form.

THE WITNESS: I don't think I would necessarily agree. Perego explains that his teachings that he's explaining with respect to the figures can be used with different kinds of memory, and he specifically mentions DDR2.

BY MR. WARRICK:

Q. But as depicted in Figure 4B with the particular command signals shown, would that not be more consistent with a Rambus-style memory device?

A. Not if one were to re- -- interpret it as a person of ordinary skill in the context of Perego as a whole.

If one were to look at it quite literally, there are certain symbols there that are indicative of Rambus memory devices, but there's a clear explanation in Perego that they can be interpreted more broadly and that a person

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of ordinary skill in the art would understand how to substitute signals from, for example, a JEDEC spec.

Q. But any modifications you would have to make to accommodate a JEDEC spec memory device in place of a Rambus-style memory device are not depicted in Figure 4B; correct?

MR. CHANDLER: Objection. Form.

THE WITNESS: I think it depends on what you mean by "depicted."

I mean, for example, my recollection is that there are RQ signals, perhaps, and DQ signals in a JEDEC standard.

But in any case, it doesn't matter, because the figures are directed towards a person of ordinary skill who is given the guidance that the memory type can be substituted.

BY MR. WARRICK:

Q. There's no chip select signal, for example, shown in Figure 4B of Perego?

MR. CHANDLER: Objection. Form.

THE WITNESS: I think there is a chip select signal. There's not a separate chip select wire. But a person familiar with the

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Rambus spec would understand that there is a chip select signal.

BY MR. WARRICK:

Q. There's no chip select signal disclosed in the Perego reference; correct?

MR. CHANDLER: Object to form.

THE WITNESS: I disagree. There's no -- first place, as I said, the Perego reference refers to the Rambus embodiments; person of ordinary skill in the art would understand where chip select signals are present in a Rambus embodiment, in some of the packetized signals that travel over the illustrated lines.

And Perego also explains to the reader that alternative signaling protocols can be used, including DDR, which a person of ordinary skill in the art would understand has chip select signals; or if they did not understand that for some reason, would go to the standard and would see that there are chip select signals.

BY MR. WARRICK:

Q. When you're talking about the standard, are you referring to JESD79-2?

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A. Yes. As of September 2003.

Q. And that's the standard for DDR2 memory devices; correct?

A. It is the standard for at least certain DDR2 memory devices.

Q. It's not the standard for a JEDEC-style memory bus; correct?

MR. CHANDLER: Objection. Form.

THE WITNESS: I'm not sure what you're trying to say, but I -- it is the standard for a JEDEC-style memory component, which could connect to a DDR2 memory bus.

BY MR. WARRICK:

Q. But it's not the standard for a DDR2 memory bus; correct?

MR. CHANDLER: Objection. Form.

THE WITNESS: I don't know what you mean by a "DDR2 memory bus." I'm not familiar with that being a defined term of art. But certainly a reasonable person could use that descriptively to refer to the pins of DDR2 memory devices.

BY MR. WARRICK:

Q. Looking back at Figure 4B of Perego, am I correct that there are two clock signals shown?

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A. There are more than two clock signals shown.

Q. Am I correct there are two types of clock signals shown in Figure 4B, CFM and CTM?

A. Depends on how -- depends on how you're using the term.

In a Rambus protocol, those are clock lines, and they could have a variety of different kinds of signals on them.

Q. Figure 4B has -- depicts two channels; correct?

MR. CHANDLER: Objection to form.

THE WITNESS: Now, I believe that -- let me see what it says in the patent. I don't think that's right.

BY MR. WARRICK:

Q. How many channels are depicted in Figure 4B of Perego?

A. Figure 4B is described as a quad-channel module. So four.

Q. And in each of the four channels in Figure 4B, there's a CFM line and a CTM line; correct?

A. In a Rambus embodiment, that would be true.

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Q. And those lines carry two clock signals; correct?

MR. CHANDLER: Objection. Form.

THE WITNESS: Again it depends what your context is in talking about signals. But at any one time, they would carry two clock signals. A CFM line would carry a clock signal, and a CTM line could carry a clock signal, in a Rambus embodiment, at any one time.

BY MR. WARRICK:

Q. Are you aware of any other types of signals that would be carried on a CFM or CTM line on a memory module?

A. I don't recall the entirety of the Rambus protocol off the top of my head. I believe it's hundreds of pages.

So I don't know the answer without referring to the documentation.

Q. But as you sit here, you're not aware of any other types of signals that would be conveyed on CFM or CTM lines; correct?

A. I don't know one way or the other without looking at the documentation.

Q. Do DDR2 memory devices require CFM and

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CTM signals?

MR. CHANDLER: Object to form.

THE WITNESS: Not under those names, but they do require clocking signals in two different directions. That's why a person of ordinary skill would rely on their knowledge of JEDEC Standard 79-2 in order to build a DDR embodiment.

BY MR. WARRICK:

Q. So a DDR2 SDRAM memory device requires two clock signals, in your view?

MR. CHANDLER: Objection to form.

THE WITNESS: Again, it depends on how one defines "clock signal." But there are a clock and a clock bar signal provided to the DDR2 memory devices. In addition, there are clocking signals that are referred to as "strobes," that are used to clock data in and out of the chip; and there are a number of those.

BY MR. WARRICK:

Q. Perego describes an ability to access the various memory devices independently; isn't that right?

A. Are you referring to a specific statement

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in Perego? I don't remember the entirety of the text.

Q. Well, in general, Perego describes, for example, a point-to-point topology; correct?

A. Perego describes a point-to-point topology for Rambus embodiments. He doesn't limit his invention in any way to a point-to-point topology. And, in fact, by explaining that his invention can be built with DDR2, he specifically informs a reader that a point-to-point topology is not necessary.

Q. But variable bit widths are central to the types of memory modules described in Perego; correct?

MR. CHANDLER: Objection. Form.

THE WITNESS: I wouldn't say that. I would say that configureable bit widths are a feature of his invention but not a required feature of his disclosure.

BY MR. WARRICK:

Q. Let me ask this: To the extent that, in your view, there are two ranks depicted in Figure 4B of Perego, is the bit width of those ranks fixed?

MR. CHANDLER: Object to form.

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THE WITNESS: It can be. Perego gets configured to a specific bit width, and an embodiment of Perego could have one or more bit widths. A person of ordinary skill would understand it to be that broad. A person of ordinary skill would not look at Figure 4B and read the description with respect to Figure 4B and say, "I can only build that kind of a DIMM if it has multiple bit widths available."

BY MR. WARRICK:

Q. Each memory device in Figure 4B has a fixed bit width, though; correct?

A. Again, it would depend on the embodiments. But in the common embodiments, yes, each memory device in Figure 4B would have a fixed bit width.

Q. And so when you say that Perego could configure ranks with different bit widths, it would do that by including different numbers of the memory devices from the module?

A. I don't think that's what I said.

Q. Then how would Perego configure different -- strike that.

How would Perego configure ranks with

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different bit widths?

A. There's an example shown in Figure 5C of how a set of multiplexers can be used to change the bit width configuration of the module. But, again, it's a feature; it's not necessary to the operation of the module.

Q. In your view, though, a rank will always have a bit width; correct?

A. Again, I -- you know, I -- it's not critical to the definition, but normally a rank would have a bit width.

Q. And that bit width is tied to the number and size of memory devices within the rank; correct?

A. No. No. More than that, because you can have two different memories of the same size, and you can have the same number of memories, each of which is the same size, but those memories have different bit widths; that -- anybody who looks at a JEDEC standard would understand that, that memories of the same size are often available on the market at a variety of bit widths.

Q. Under -- understood. Let me ask a better question.

The bit width of a rank is tied to the

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number and bit widths of the memory devices within the rank; correct?

A. In general. Again, people use these words with common sense. If occasionally you were to only access a portion of a rank, and that was a capability that you had, a person of ordinary skill in the art would not stop calling that a rank.

Q. And you've said earlier that Perego allows you to configure the ranks; correct?

MR. CHANDLER: Object to form.

THE WITNESS: That is a feature of some of his embodiments.

BY MR. WARRICK:

Q. And so for example, in Perego, you can choose how many of the memory devices will participate in a given rank; yes?

MR. CHANDLER: Object to form.

THE WITNESS: It's the interface that it is configurable with. I don't think I've considered whether or not the ranks can be configured, because, again, it's irrelevant, because Perego doesn't require you to have variable-size ranks. It certainly discloses fixed-size ranks.

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I, right now, am not seeing rank reconfiguration. It was the interface that can be reconfigured.

BY MR. WARRICK:

Q. Well, let me ask this, then: Does Figure 4B necessarily depict two and only two ranks?

MR. CHANDLER: Object to form.

THE WITNESS: As described in the text, it does. For -- for one embodiment described in the text, it literally has two ranks. Whether someone could use the same figure with different text to describe something else, I haven't considered that.

BY MR. WARRICK:

Q. But in your -- under your proposed construction, there's nothing about the location of the individual memory devices on the module that determines which rank they can be a part of; correct?

MR. CHANDLER: Object to form.

THE WITNESS: If by "location" you mean their physical placement without respect to their connectivity, I think that's correct.

It's the connectivity and operation of memory devices that would lead a person of

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ordinary skill to determine what rank they are were in -- they are in.

BY MR. WARRICK:

Q. Now, if we look at Figure 4A, which is on the same page of the Perego reference, Exhibit 1071.

Do you see that?

A. I do.

Q. And you've also referenced that in your declaration for the '417 patent, on page 154 of your declaration; correct?

A. Correct.

Q. And in your declaration, you've also color-coded Figure 4A with colors that aren't from the original reference; right?

A. Correct.

Q. And am I correct that through your color-coding and related text, it's your view that Figure 4A depicts two ranks?

A. In --

MR. CHANDLER: Objection --

THE WITNESS: -- a two-channel embodiment, the Figure 4A, that would be correct.

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BY MR. WARRICK:

Q. Now, as between Figures 4A and 4B of Perego, both include channels 415a and 415b; correct?

A. They both include channels that are called 415a and 415b. But in the context of the text, I'm not sure we should assume that they are identical across the embodiments.

Q. So in your view, in Figure 4B, channels 415a and 415b are both part of the same rank, unlike Figure 4A; is that right?

A. It's not really a question of in my view. It's a question of what Perego says.

Perego says that in 4A you can have an embodiment where both channels are in the same rank or where the channels are in two different ranks. Actually, it says you can either have one channel or two channels there, as well.

In 4B, it tells us that there are two ranks and with four channels, that -- that the channels are being paired in that particular situation.

Q. Can you point me to -- to where specifically Perego draws that distinction?

A. I'm not sure what you mean by "that

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distinction."

Q. The distinction between the alleged ranks in Figure 4B versus 4A in the context of channels 415a and 415b.

A. Again, one has to read Perego in its whole context, where it does tell us we can have DDR2 embodiments.

Q. Well, you indicated earlier that Perego tells us that Figure 4B includes four channels and two ranks; yes?

A. Yes. That's primarily described in an embodiment that's described in Column 10, lines 32 through 47.

Q. So Column 10, starting at line 32 of Perego, talks about "alternate embodiments"; correct?

A. Yes.

Q. And specifically, it says, [as read]:

"...channels 415a and b may operate simultaneously with channels 415c and 415d..."?

A. Yes.

Q. And what does that mean, in your view, that they operate simultaneously?

A. I read it to mean that channels a and b

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are operating together; and that channels c and d are operating together; that each is operating as a rank.

Q. But it's an alternate embodiment, so they could also operate independently, in your view?

MR. CHANDLER: Object to form.

THE WITNESS: Perhaps the -- this patent can disclose multiple embodiments. There's -- there's nothing in my opinion that says that every embodiment of Perego discloses the claims, only that there are disclosed embodiments that disclose the claims.

BY MR. WARRICK:

Q. But Perego discloses the flexibility that, for example, the modules shown in Figure 4B could include more than two ranks; yes?

A. A person of ordinary skill could make lots of modifications to Perego based on its teachings, but that doesn't impact my opinion.

Q. Could, for example, the four memory devices -- devices closest to the buffer in 4B be configured as a single rank?

MR. CHANDLER: Objection to form.

THE WITNESS: I'm not sure which ones

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you're talking about.

BY MR. WARRICK:

Q. So in Figure 4B, you see a buffer in the center; correct?

A. Yes.

Q. And we see rows of memory devices on the top half of Figure 4B and rows of memory devices on the lower half; yes?

A. Yes.

Q. So my question is: Could you configure a rank to include the two memory devices immediately to the left of the buffer as well as the two memory devices to the immediate right of the buffer?

MR. CHANDLER: Object to form.

THE WITNESS: I suppose a person of ordinary skill in the art would know how to make the appropriate modifications to do that, but I don't see that taught anywhere in Perego.

BY MR. WARRICK:

Q. But it could be done using the -- the system disclosed in Perego is what you're saying?

MR. CHANDLER: Object to form.

THE WITNESS: Using a modification of the

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system -- of what's taught in Perego, I think it could be done.

Memory systems are very, very flexible. There's a lot of things that could be done that are within the skill of a person of ordinary skill in the art.

BY MR. WARRICK:

Q. Going back to Perego's description in Column 10, starting at line 32, where it says,

"...channels 415a and 415b may operate simultaneously with channels 415c and 415d," does "simultaneously" mean in response to the same memory request?

A. I don't believe that's what's indicated here.

Q. So you think it's talking about "simultaneously" in response to different memory requests?

MR. CHANDLER: Object to form.

THE WITNESS: I believe that what that's saying is that a and b would operate simultaneously and that c and d would operate simultaneously.

BY MR. WARRICK:

Q. Well, assuming that's correct, does that

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mean that Channels 415a and 415b would operate simultaneously in response to the same memory command?

A. The same host command, yes.

Q. When you say a "host command," do you mean the command originating from the buffer?

MR. CHANDLER: Objection.

THE WITNESS: In a DDR2 embodiment, that would be true, yes.

BY MR. WARRICK:

Q. Well, going back to that, we discussed earlier that in Figure 4B, each channel includes two clock lines, CFM and CTM; right?

A. In a Rambus embodiment, that would be the case.

Q. Well, in -- in Figure 4B, as it is shown in Perego, that's what's depicted; correct?

MR. CHANDLER: Objection. Form.

THE WITNESS: Again, that's what's literally depicted, but a person of ordinary skill reading the patent would understand that those are exemplary signals, not limiting.

BY MR. WARRICK:

Q. Well, just so I understand, what you're

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saying is that a person of ordinary skill, in your view, would be able to modify the embodiments of Perego, including the embodiment depicted in 4B.

Am I understanding you correctly?

A. No, not really.

What I'm saying is that Perego specifically says that various kinds of memory can be used in his embodiments, including DDR2; and that a person of ordinary skill would understand that when Perego, in that context, illustrates a set of input sig- -- and output signals to a memory device, that that's exemplary and that they are expected to understand that that would be substituted, under Perego's teachings, for the appropriate memory signals for the device that you're using in the embodiment.

Q. And Figure 4B, to use your word, is exemplary; correct?

A. It is -- yes, it is exemplary.

Q. And in the example of Figure 4B, each channel includes two clock signal lines, CFM and CTM; correct?

A. That is literally what's depicted.

But as I explained, a person of ordinary skill would understand that any set of appropriate

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memory control signals can be used there.

Q. Now, a DDR2 memory device would not be used with two clock signal lines, CFM and CTM, would it?

MR. CHANDLER: Objection to form.

THE WITNESS: Not with two clock signal name -- lines that have those names. It instead would use the clock signal lines that are appropriate to DDR2, as explained in Exhibit 1064.

BY MR. WARRICK:

Q. And Exhibit 1064 is the DDR2 specification; correct?

A. Correct.

Q. But the example depicted in Figure 4B of Perego is showing a Rambus-style memory architecture if you interpret it literally; correct?

MR. CHANDLER: Objection. Form.

THE WITNESS: If you interpret it literally, it is illustrating the Rambus signal names.

But as I said, Perego is very clear in expressing to a person of ordinary skill that other kinds of memory modules or memory

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devices can be used as well.

BY MR. WARRICK:

Q. Now, you can't just swap out each of the Rambus-style memory devices in Figure 4B for DDR2 memory devices and have a working memory module, can you?

MR. CHANDLER: Object to form.

THE WITNESS: It depends what you mean by "just swap out." You can't just physically remove one and replace it with the other.

But as a person of ordinary skill, it would not require any invention to replace one with the other. I would simply follow the specifications.

BY MR. WARRICK:

Q. And when you say "the specifications," what specifications are you referring to?

A. Generally, Exhibit 1064. But in practice, I would also obtain the specifications for the particular brand of memory devices that I was using to see if they deviate in any way from Exhibit 1064.

Q. You would also have to make modifications to the memory channels; correct?

MR. CHANDLER: Objection to form.

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THE WITNESS: "Memory channel" is really just a description of the interconnect for the memory.

So a person of ordinary skill would ordinarily -- when changing out one memory type for another, would change the connectivity to match the specifications for the desired memory type. And just by changing the connectivity and the behavior of the interface to match the documented specification, one would be changing the channel.

BY MR. WARRICK:

Q. And when you say "changing the interface," that would include, for example, changing the CFM and CTM lines depict -- depicted in Figure 4B; correct?

MR. CHANDLER: Objection. Form.

THE WITNESS: Those particular names are specific to the Rambus interface. They would be substituted by the specific names and specific interconnect wires that are disclosed in Exhibit 1064. That's an ordinary thing to do.

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BY MR. WARRICK:

Q. You would also, for example, have to add chip select lines; correct?

MR. CHANDLER: Objection. Form.

THE WITNESS: You would make the interface compatible with the JEDEC specification in Ex. 1064, that includes a number of lines that are described on page 6 of JEDEC standard 79-2.

You would simply substitute one well-known interface for another.

BY MR. WARRICK:

Q. Are you characterizing Perego as a well-known interface?

A. No. I'm characterizing the DDR2 device interconnect interface and the Rambus device interconnect interface as well-known interfaces.

Q. And one of the changes you would have to make is to add chip select lines in order to be compliant with the JEDEC standard for DDR2; correct?

MR. CHANDLER: Objection. Form.

THE WITNESS: Chip select lines are one of the aspects of the DDR2 standard.

And if you substituted one well-known

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standard for another, you would have to remove all of the connections from the first standard and replace them with all of the connections from the second standard.

BY MR. WARRICK:

Q. And that would include chip select lines that are not depicted in Figure 4B; correct?

MR. CHANDLER: Object to form.

THE WITNESS: The JEDEC connections are not literally depicted in Figure 4B. But as we've discussed a number of times, Perego informs a person of ordinary skill in the art that they can be used as an alternative to the Rambus interconnect.

MR. CHANDLER: Phil, whenever it's a good time for a break -- we've been going about an hour -- so that we can sequence this to get three sessions before lunch if possible.

MR. WARRICK: Yes.

BY MR. WARRICK:

Q. Dr. Wolfe, would you mind if I ask just a couple more questions and then we take a break?

A. That's fine.

Q. I just want to make sure I understand. From your explanation, Figure 4B is depicting a

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well-known Rambus-style interface between the buffer and the memory devices; yes?

A. That Figure 4B literally illustrates a well-known Rambus-style interface between the buffer and the memory devices. And Perego elsewhere explains that other memory interfaces can be used instead.

Q. And if you were to use DDR2 memory devices in Figure 4B of Perego, you would also have to change the interconnects between those devices and the buffer; correct?

MR. CHANDLER: Objection. Form.

THE WITNESS: You would replace the well-known Rambus interface with the well-known DDR2 interface.

BY MR. WARRICK:

Q. And isn't it correct you would also have to make changes to the design of the buffer in Figure 4B of Perego if you substituted DDR2 memory devices?

A. Correct. You would -- you would take aspects of the buffer that were designed to be compliant with the public Rambus standard, and you would change them to be compliant with the public DDR2 standard.

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MR. WARRICK: Okay. We can take a break.

MR. CHANDLER: Five minutes is fine here.

(Short break taken.)

THE WITNESS: Can I clarify one of my prior answers?

BY MR. WARRICK:

Q. What answer is that, Dr. Wolfe?

A. You asked me a number of questions about whether or not the illustration on Figure 4B was literally Rambus. And now that I've had another chance to look at the patent, at the end of the description at the bottom of Column 9 and the top of Column 10, it's pretty clear that one's intended to interpret those labels more broadly than Rambus. Specifically, the RQ control lines are described as that they can be individual control lines, including row address strobe, column address stroke, etc., which are DDR-style signals.

And, in fact, if you go on to the rest of that paragraph, it points one to Figure 6A, where it says that you can have individual device-select lines as well, which would be chip selects.

Q. So just to be clear, you're talking about the paragraph that spans the bottom of Column 9

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and the top of Column 10 in Perego?

A. Generally. It's actually from about line 34 in Column 9 through line 4 in Column 10.

Q. Well, in Column 9, starting around line 58, it talks about the control lines, which I think you referenced earlier, RQ.

And that's in the context of alternate embodiments; correct?

A. Yes. But also it's part of a section that talks about being -- with reference to Figures 4A, 4B, and 4C.

Q. And that particular paragraph references 6A, as you mentioned, as depicting one such alternate embodiment; right?

A. Later in the paragraph, it does.

Q. So again, Figure 4A -- 4 -- strike that.

Figure 4B of Perego is one example and what you are highlighting to me as text in Perego talking about other embodiments; correct?

A. My understanding in context would be that that's intended to describe the range of embodiments that are represented by Figures 4A, 4B, and 4C.

Q. And, Dr. Wolfe, we just came back from a brief break.

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Did you have discussions with counsel during that break?

A. I did not communicate with anyone in any way during the break.

Q. Okay. So going back to your proposed construction for rank in the context of the '417 and '215 patents. We had been looking at that earlier in paragraph 126 of your '417 patent declaration, for example.

Do you recall that?

A. Yes.

Q. And part of your construction is that the memory devices act together to read or write the full bit width of the memory module; correct?

A. That one or more memory devices act together to read or write the full bit width of the memory module. In the context of memory modules, I believe that's correct.

Q. And, in your view, how does one know the full bit width of the memory module?

A. It's defined by the design.

Q. Is it a fixed number for any given memory module?

MR. CHANDLER: Objection. Form.

THE WITNESS: I wouldn't say that it's

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not possible to have a configureable memory module, but once the module's been figured, the full bit width, I think, is a -- is established.

Now, as I mentioned, sometimes computer systems will perform a partial read and write. That doesn't change what we mean when we use the word "rank."

BY MR. WARRICK:

Q. When you say "a partial read and write," do you mean a read or write that involves less than all of the memory devices within a given rank?

MR. CHANDLER: Objection. Form.

THE WITNESS: In some computer systems, that is a capability, that a rank can read or write some or all of its bits. People would still ordinarily call that a "rank," even -- even if not every single memory transaction used every bit.

BY MR. WARRICK:

Q. You mentioned that some memory modules could be configured in terms of the bit width of the module.

Is Perego describing such a system?

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A. Perego has a configurable interface. I don't think the sizes of ranks are configurable. But it's the interface width. It's not the size of the memory module transaction.

But again, I haven't relied on the configurability. Perego clearly defines -- or clearly describes modules which have been pre-configured to have the width of the memory module be equal to the width of the rank.

Q. So backing up, what I'm asking about right now is the bit width of the module itself separate from the bit width of any ranks within it.

And what I'm asking is, how does one know the bit width for a given memory module?

MR. CHANDLER: Object to form.

THE WITNESS: In practice, one would read the specifications of how it -- how it operates.

BY MR. WARRICK:

Q. Is it tied to the maximum number of bits that could be output from the memory module simultaneously?

A. Again, we have to look at it in context. But typically the maximum number of bits in a

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1 particular configuration would be the bit width of
2 the module.
3 Q. Having reviewed Perego, do you have a
4 view on the full bit width of the memory module
5 depicted in Figure 4B?
6 A. I don't think it's restricted in any way.
7 One would make it -- I mean, in one illustration
8 of the example, in 4B, it's 16 bits.
9 But again, if you read the text, it's
10 clear that one can pick any number of bits up to
11 and including the bit width of a rank.
12 Q. It can't be more than the bit width of a
13 rank?
14 MR. CHANDLER: Objection. Form.
15 THE WITNESS: Perhaps it can. Again, I
16 didn't have to consider all those cases
17 because it clearly discloses that it can be
18 the bit width of a rank. And that's the only
19 embodiment that one needs to understand that
20 the asserted claims are obvious -- or the
21 challenged claims are obvious.
22 BY MR. WARRICK:
23 Q. So under your proposed construction,
24 memory devices that are acting together to read or
25 write less than the full bit width of a memory

module would not be a rank; correct?

MR. CHANDLER: Objection. Form.

THE WITNESS: Again, I think it would be -- a person of ordinary skill would use common sense. The fact that in one memory transaction only a portion of the memory module bit width was used would not make that memory stop being a rank. If it had the ordinary capability to read and write the full bit width of the memory module in response to command signals, including chip select signals, then a person of ordinary skill would understand that to be a rank.

The fact that it could potentially do other things, as well, would not make it stop being a rank.

BY MR. WARRICK:

Q. What about memory devices that act together to read or write more than the full bit width of the memory module, would those not qualify as a rank under your definition?

A. I'd have to look at a particular design, but I think that they probably would be a rank.

Q. Well, for example, if Figure 4B, if we assume that it depicts a module with a full bit

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width of 16, and you have memory devices within 4B that act together to read or write 32 bits, that wouldn't be a rank under your definition, would it?

MR. CHANDLER: Objection. Form.

THE WITNESS: Again, that's not an embodiment that I relied on. But I think a rank can be bigger than the interface and still be a rank.

Again, you know, a person of ordinary skill in the art doesn't use the term in some prosecutorial manner, where it's trying to -- to do more than -- than assist a person in understanding the art.

What we're trying to do is distinguish the memory devices that are accessed together to provide a read or a write from the ones that are accessed separately to provide a read or a write.

BY MR. WARRICK:

Q. And I believe you said earlier today that when you say "access together," you mean at approximately the same time and in response to the same command signals; yes?

A. Yes. In the way that an ordinary person

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of skill would understand being accessed together in a memory system so that within reasonable engineering parameters they are responding at the same time.

Q. Now, the bit width of the memory module is tied to the buffer data path width; am I right about that?

MR. CHANDLER: Objection. Form.

THE WITNESS: I'm not sure what context you're speaking in.

BY MR. WARRICK:

Q. In the context of Figure 4B in Perego, for example.

A. Ask me one more time, please.

Q. Well, in Figure 4B of Perego, the buffer has a data path width; correct?

MR. CHANDLER: Objection. Form.

THE WITNESS: I'm not exactly sure what you're referring to. The width of which particular set of signals?

BY MR. WARRICK:

Q. Well, let's look at -- towards the bottom of Figure 4B, you see some up and down arrows and the number 16?

A. Yes.

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Q. Is that referring to the number of pins or lines connected to the buffer?

A. In an exemplary embodiment, yes; the number of -- of data pins that are connected in an exemplary embodiment of Figure 4B.

Q. And so 16 pins, would that imply a 16-bit memory module bit width?

A. In an exemplary embodiment, yes.

Q. And is it true that the memory module bit width could also be greater than 16 in that context if you had a serialization ratio greater than 1:1?

MR. CHANDLER: Object to form.

THE WITNESS: It depends how you're defining "bit width of the module."

Again, Perego doesn't intend to be limiting. He describes a variety of different interface widths that can be implemented.

BY MR. WARRICK:

Q. Well, let's bring it back to your proposed construction, because what I really want to understand, Dr. Wolfe, is what you mean in your proposed construction by the "full bit width of the memory module."

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Perego is one example. But generally, for your construction, how do we determine the full bit width of a memory module?

A. It's usually, as I said, defined for the memory module; but it would typically be defined as the size of a standard read or write operation to that module.

Q. And is the size of a standard read or write operation for a given module tied to the number of contacts on the module used for data?

MR. CHANDLER: Objection. Form.

THE WITNESS: In the most common cases, it is, but I don't know that it necessarily needs to be.

BY MR. WARRICK:

Q. I want to go back to this concept in your proposed construction of memory devices acting together.

And if we look at Figure 4B of Perego as an example, your view is that all of the memory devices across the top of Figure 4B that are connected to Channels 415c and 415d comprise one rank; correct?

A. Yes, in certain disclosed embodiments.

Q. And that is in part because, in your

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view, those memory devices act together in response to command signals to read or write the full bit width of the memory module?

A. Yes. Again, in certain embodiments.

Q. Now, in Figure 4A on the other hand, in your view, each rank has half the number of memory devices as the ranks you identified in Perego 4B; correct?

MR. CHANDLER: Object to form.

THE WITNESS: In certain exemplary embodiments, yes.

BY MR. WARRICK:

Q. Now, does it follow that in those embodiments the full bit width of the memory module in Figure 4A is less than the full bit width of a memory module in Figure 4B?

A. Not necessarily. The individual memory devices can be twice as wide.

Q. You mentioned earlier that there's this concept of partial reads and writes; is that right?

A. In some commercial systems.

Q. If we look at Figure 4B and the memory devices that are connected to Channels 415c and 415d, if half of those devices, for example, the

memory devices on Channel 415c, are acting together to read or write the full bit width of the memory module, does that become a separate rank?

MR. CHANDLER: Objection. Form.

THE WITNESS: I don't know. That's not the embodiment I relied on. So I would have to look at what changes you're actually proposing in detail.

BY MR. WARRICK:

Q. Well, I'm just asking, Dr. Wolfe, if those four memory devices on the upper left of Figure 4B, connected to Channel 415c, act together to read or write the full bit width of the memory module, then that would be a "rank" under your understanding of the term; yes?

MR. CHANDLER: Objection. Form.

THE WITNESS: That would be a different embodiment than the one I relied on. It would operate differently, and I would have to understand how it operated in detail.

BY MR. WARRICK:

Q. Now, Perego is titled "Configurable Width Buffered Module"; correct?

A. Correct.

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Q. What does that mean in the context of Perego, to have a configurable width buffered module?

A. That means that in addition to disclosing rank multiplication, Perego also discloses, as illustrated in Figure 5C, that one feature of his module is that the interface width can be configured to more than one different option in some embodiments.

Q. When you say the "interface width," are you describing the width of the interface into the buffer or from the buffer to the memory devices?

A. In the interface, as what's shown as Interface 596 on Figure 5B, for example.

Q. And so Perego has a configurable serialization circuit that's capable of varying the data path width; is that right?

MR. CHANDLER: Object to form.

THE WITNESS: In some of his embodiments, he does.

BY MR. WARRICK:

Q. Going back to Figure 4B of Perego, I think I understood from you earlier that all of the memory devices connected to Channel 415a and 415b comprise one rank; is that right?

A. In at least one embodiment, that would be true.

Q. So in that embodiment, they would operate simultaneously to satisfy a single memory read or write command; correct?

A. Correct.

Q. And those eight memory devices in that embodiment would be working together to output data to -- 16 bits of data on the DQ lines?

MR. CHANDLER: Objection. Form.

THE WITNESS: No. This -- this Figure 4A is not -- 4B or is not limited to 16 bits. Could be 32 bits or 64 bits or 128 bits. Those are all disclosed in Perego.

BY MR. WARRICK:

Q. But literally Figure 4B shows a bit width of 16; correct?

A. It's literally what's shown in the example. But again, the content -- the patent itself tells you that that's not a limitation of Figure 4B.

Q. So in that context of an example that has a 16-bit width memory module, the eight memory devices connected to Channels 415a and 415b are working together to output 16 bits of data;

correct?

MR. CHANDLER: Object to form.

THE WITNESS: There would be no reason to limit it to 16 bits. But if one were to choose to limit the buffer-to-host connection to 16 bits and to decide that there were eight module memory devices in each rank, then they would work together to supply 16 bits.

BY MR. WARRICK:

Q. You mentioned the concept of rank multiplication a minute ago.

A. Yes.

Q. It's your contention that Perego discloses rank multiplication.

Am I understanding that correctly?

A. I don't recall if I reached that conclusion.

Q. Well, let me ask you, then. Do you have -- have you offered an opinion in this -- in these proceedings about whether or not Perego discloses rank multiplication?

A. Yeah. Paragraph 241 of my '417 declaration, I did conclude that, "Perego teaches that the 'logic' in the buffer device can perform

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'rank multiplication'..."

Q. So, to me, that sounds a little bit different.

I see in paragraph 241 of your '417 patent declaration, "Perego teaches that the 'logic' in the buffer device can perform 'rank multiplication'..."

Do the words "rank multiplication" appear in Perego?

A. Not that I can recall.

Q. For that matter, does the term "rank" appear in the Perego reference?

A. I don't recall the term being used, but the concept is there.

Q. So if, in your view, Perego is disclosing rank multiplication, am I understanding correctly that Perego can present fewer ranks than actually exist as physical ranks?

A. I'm not sure what it means to -- I don't even remember the word you used.

Did you say "present ranks"? Is that the term you used?

Q. Yes.

A. I'm not sure I know what it means to "present ranks."

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It can --

Q. Let me ask this, then. Can Perego, in your view of what you're describing as the rank multiplication disclosed in Perego, make more than one physical rank appear as only one rank to the rest of the system?

A. In essence, yes. Because what it can do is it can take a memory request that is too large to be serviced by one physical rank and have it serviced by two physical ranks in a way that the original host can't tell the difference.

Q. And it's your view that that concept is disclosed by Perego?

A. Yes.

Q. So would an example of that be, in Figure 4B, Perego making what you call the two ranks appear as just a single rank to the memory controller?

MR. CHANDLER: Object to form.

THE WITNESS: If by the "memory controller," you mean the memory controller in an external host, essentially, yes.

BY MR. WARRICK:

Q. I want to go back to the example we were discussing in Figure 4B, where I asked about the

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1 context of the module bit width being 16 and the
2 eight memory devices on Channels 415a and 415b
3 working together to output 16 bits.
4 Do you recall that?
5 A. I recall the question.
6 Q. So in that example, just so I understand,
7 is it correct that each of those eight memory
8 devices would be outputting two bits each?
9 MR. CHANDLER: Object to form.
10 THE WITNESS: In that example, that would
11 be the case.
12 But again, there is nothing special about
13 those numbers with respect to 4B.
14 A person of ordinary skill in the art who
15 implemented Figure 4B in light of the JEDEC
16 standard in Exhibit 1064 would likely choose
17 different specific values.
18 BY MR. WARRICK:
19 Q. In Figure 4B of Perego, does the bit
20 width of the memory module change depending on how
21 many of the channels are working together?
22 MR. CHANDLER: Object to form.
23 THE WITNESS: I don't believe so. I
24 believe that it's just the interface -- if
25 we're talking about the same bit width of the

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module, I believe it's only the interface that changes.

BY MR. WARRICK:

Q. If all 16 memory devices depicted in Figure 4B of Perego are operating simultaneously to read or write the full bit width of the module, does that mean that there would be just a single rank in that example?

A. I don't believe I -- I don't recall seeing a description of such an embodiment in Perego.

Q. Am I correct that Perego has the flexibility to configure a rank in that way?

A. I'm not sure what you're asking. Certainly, you can have a single-rank embodiment of Figure 4A; that is described in Perego. But I don't believe that a single-rank embodiment of 4B is actually described in Perego.

Q. What I ask is whether Perego would permit a skilled artisan to configure a single-rank embodiment in the context of Figure 4B.

A. I don't know. I haven't considered that. I -- I relied on the two-bank -- or the two-rank embodiment that was actually described in Perego.

Q. When Perego is allegedly performing rank

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multiplication, in your view, and it's making two physical ranks appear as one rank to the external memory controller, what differentiates those two ranks such that they are not really just one larger rank?

A. I think in that particular case, they would be accessed by different control signals at different times.

Q. You said a minute ago that you hadn't contemplated the possibility of a single-rank embodiment in the context of Perego 4B. But if we were to change Figure 4B from a 16-bit memory module to a 64-bit memory module, would that imply a single-rank embodiment, all else being equal?

A. I don't know what you mean by "all else being equal." I would not do it that way. If I were to make a 64-bit-wide host interface on an embodiment of 4B, and I would do that using DDR2 interfaces, as I've suggested, I would use 8-by-8 chips in each rank to provide a 64-bit response.

Q. So let's say you did use eight-bit memory devices; and in total in Figure B there are 16 of them; and let's assume that the context is a 128-bit module width. Would that be a single-rank example?

A. It might be. But again, that's not really following what's taught about Figure 4B. If I were using by-8 chips, I would put 16 in each rank to get 128-bit host interface, or I would use 8-by-16 chips if I wanted each rank to provide 128 bits to 128-bit interface.

So that's the natural conclusion that I would reach in implementing Figure 4B in a JEDEC DDR2-compliant environment.

Could a person of ordinary skill do other things? Yes, probably.

Q. So memory devices on separate channels can act together to respond to command signals to read or write the full width -- bit width of the memory module; correct?

A. Depending on how you define a channel. If you define that as a set of wires, then yes, that's correct, as long as the signals are duplicated across both sets of wires -- or specifically the control signals are duplicated across both sets of wires.

Q. So for example, in Perego 4B, in your understanding, the memory devices connected to Channels 415c and 415a could act together to form a single rank?

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MR. CHANDLER: Objection. Form.

THE WITNESS: Not consistently with the description of Perego. A person of ordinary skill could probably modify it that way. But in Perego -- the way it's described in Perego, my understanding is that it's 415c and 415d that would have duplicate control signals and 415a and 415b that would have duplicate control signals.

BY MR. WARRICK:

Q. Are you saying it's not disclosed in Perego that one could send the same control signals to the memory devices on Channels 415c and 415a in Figure 4B?

A. I don't recall that disclosure. But again, it's not really relevant to my conclusions, because whether or not someone could do something different in Perego doesn't have anything to do with what it discloses with respect to the claims.

Q. Is that an important distinction?

A. Is what an important distinction?

Q. Between what Perego actually discloses and what someone theoretically could do in view of the disclosure.

A. Both are valuable in assessing

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obviousness. But once one has concluded that Perego discloses or renders obvious the claims, it's not necessary to make a determination as to whether or not other things are also obvious.

Q. In Perego, if you could look, please, at Column 15, around line 45, there's a reference to:

"...grouping memory devices into multiple independent target subsets (i.e. more independent banks)."

Do you see that?

A. That's the paragraph that starts at line 31?

Q. Correct.

A. Let me read it, please.

Okay.

Q. You've read the -- the paragraph in Column 15?

A. Yes.

Q. So I'm specifically interested in the last sentence of that paragraph, Column 15, lines 43 to 45.

It talks about "...grouping memory devices into multiple independent target subsets (i.e. more independent banks)."

Do you see that?

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A. Yes.

Q. Is Perego referencing ranks in that discussion, in your view?

A. Yes.

Q. So your understanding is that grouping -- the reference to "grouping memory devices into multiple independent target subsets," is, in fact, grouping memory devices into "ranks," under your understanding of that term?

MR. CHANDLER: Object to form.

THE WITNESS: Yes. Under some conditions, that would be true.

It's important to understand that -- that this entire paragraph is both conditional and permissive.

But I do believe that he's discussing the possibility of, in some cases, increasing the number of ranks.

BY MR. WARRICK:

Q. What's your understanding of what Perego means by a "more independent bank"?

MR. CHANDLER: Objection to form.

THE WITNESS: My understanding is that he's saying that there could be alternative embodiments that have more ranks than the

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embodiment that he's previously described, under certain conditions and if one chooses.

BY MR. WARRICK:

Q. Is Perego referencing a rank, in your view, when it says "independent banks"?

A. I think broadly he is -- is talking about the same general concept.

Q. Generally speaking, if multiple memory devices output data that collectively is part of a single memory device transfer operation, is that potentially a "rank," under your understanding of the term?

MR. CHANDLER: Object to form.

THE WITNESS: Can I hear that one more time?

BY MR. WARRICK:

Q. Yes.

Generally speaking, if multiple memory devices output data that is part of a single memory device transfer operation, is that potentially a "rank," under your understanding of the term?

MR. CHANDLER: Objection. Form.

THE WITNESS: I think that could be a rank, depending on other factors.

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Again, a person of ordinary skill in the art is really trying to make a determination of whether or not their memory chips are in the same rank or in different ranks.

They are not trying to, in some hypercritical way, define a "rank" so narrowly that -- that something that operates essentially like a rank is excluded because of some minor technicality.

BY MR. WARRICK:

Q. So a "rank" is a flexible concept, under your understanding, in this context?

MR. CHANDLER: Objection. Form.

THE WITNESS: No. I think in this context, it's a descriptive term that helps us to understand whether or not memory devices are activated together or separately.

BY MR. WARRICK:

Q. When you --

MR. CHANDLER: Sorry. I was just going to say, you know, if we want to have a third session before lunch, we should probably take a break whenever is convenient.

MR. WARRICK: Okay. I think we would be near a good stopping point soon.

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BY MR. WARRICK:

Q. Dr. Wolfe, you said that -- you referenced memory devices being activated together or separately in your last answer?

A. Right.

Q. What do you mean by "activated"?

A. Responding to control signals, including a chip select.

Q. You mean "activated," in your view, is distinct from responding to a read or write command; is that right?

MR. CHANDLER: Objection. Form.

THE WITNESS: No. It's simply a word that I used to mean "responding to a read or write command."

BY MR. WARRICK:

Q. So you were not referencing, for example, the concept of row activation?

A. No.

Q. In your view, does row activation play any role in the configuring of a rank?

MR. CHANDLER: Objection to form.

THE WITNESS: Not necessarily. It would be common to have all of the devices in a rank respond together to a row activation and

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1 devices in a different rank have a separate
2 row activation, but it's not definitional.
3 BY MR. WARRICK:
4 Q. Does a memory device have to be activated
5 before it can respond to read or write memory
6 commands?
7 MR. CHANDLER: Objection. Form.
8 THE WITNESS: Not in general. But DDR2
9 DRAM devices do.
10 MR. WARRICK: Okay. I think we could
11 take a break here. Is five minutes good
12 again?
13 MR. CHANDLER: Sure. Good for me.
14 MR. WARRICK: All right.
15 (Short break taken.)
16 BY MR. WARRICK:
17 Q. Dr. Wolfe, before the break, we were
18 talking about row activation, and you noted that
19 in DDR2 SDRAM implementations and embodiments,
20 there has to be a row activation command before
21 reads and writes can be performed; is that
22 accurate?
23 A. Correct.
24 Q. And in the example of Perego, the buffer
25 will select the target subset channels based on

address bits; is that right?

MR. CHANDLER: Object to form.

THE WITNESS: Looking at something particular in Perego?

BY MR. WARRICK:

Q. Perego generally. Just based on the disclosures of Perego.

A. I think it can select based on address bits.

Q. So in Perego, is it correct that all of the memory devices in the possible target subset channels have to be activated together?

MR. CHANDLER: Object to form.

THE WITNESS: If in an embodiment of Perego you're going to have multiple memory devices respond to the same read or write operation, they both need to have the same row activated. Normally you would do that together, but they could be done sequentially.

BY MR. WARRICK:

Q. Does Perego disclose selecting target subsets based on anything other than address bits?

A. I don't recall it explicitly saying that, but it also doesn't in any way limit it to the

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address bits. And a person of ordinary skill, when looking at the JEDEC standard in Exhibit 1064, would understand that you can select portions of memory or memory devices from a set using either address bits or bank address inputs.

Bank address inputs are essentially simply extended address bits for many purposes.

Q. Okay. So let's consider the example of having two channels and each is a possible target subset. In that case, is it correct that you have to send an activation command to all of the DRAMs on all of the target subset channels?

MR. CHANDLER: Objection. Form.

THE WITNESS: If you're using a DDR2 implementation, you need to activate rows before you read or write them in all cases.

BY MR. WARRICK:

Q. And so my question is, in that context of a DDR2 implementation, if you have two channels that are potential target subsets, you would need to activate the rows in all of those memory devices in both channels; correct?

MR. CHANDLER: Objection. Form.

THE WITNESS: Not clear to me what you're -- how you're using the word "target

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subsets" in the question.

BY MR. WARRICK:

Q. In the context of the Perego disclosure we had been looking at before the break, in Column 15, about multiple independent target subsets.

A. Well, again, that's only one permitted embodiment of Perego. If you want to access a row across a group of memory devices, the same row needs to be activated in each memory device that you're going to access using the signal read or write command.

Q. Can we look at the abstract of Perego for a minute?

A. Okay.

Q. And the third sentence of the abstract, I'm going to read, if you could follow along with me.

It says, "The configurable width buffer device includes a interface and a configurable serialization circuit capable of varying a data path width or a number of contacts used at the interface of the configurable width buffer device in accessing the at least one memory device."

Did I read that correctly?

A. Yes.

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Q. And based on that disclosure in the abstract, is it correct that Perego permits configuration of both the data path and the contacts of the interface?

MR. CHANDLER: Object to form.

THE WITNESS: In some embodiments, Perego permits that. In other embodiments, he talks about a one-to-one serialization ratio and he talks about determining the configuration and manufacturing time.

BY MR. WARRICK:

Q. Can we look at Column 21, please, of Perego, and the paragraph that starts on line 16 of Column 21.

A. Okay.

Q. So again, specifically, the first sentence, starting on line 16 of Column 21 of Perego, says [as read]: "Any number of channels 415a through 415d, for example; two Channels 415c and 415d may transfer information simultaneously and the memory devices on the other two channels 415a and 415b remain in a ready or standby state until called upon to perform memory access operations."

Did I read that correctly?

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A. I believe so.

Q. Am I -- is it your understanding of that disclosure that if two channels in Perego are transferring information simultaneously, the other channels are in a ready or standby state at that time?

MR. CHANDLER: Objection. Form.

THE WITNESS: My understanding is that that's permitted. This is all permissive language.

I think this is supportive of a two-rank configuration of Figure 4B in which channels 4c and 4d are accessed together and 4a and 4b are waiting for the next access.

BY MR. WARRICK:

Q. Now, am I correct that that example is the partial rank access that you were describing earlier today?

A. No. In that case, there's a full rank, c and d, that's being accessed, and a second rank, a and b, that's not being accessed.

Q. Can we look for a second at paragraph 269 of your declaration for the '417 patent.

Do you have that in front of you?

A. Yes.

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Q. And in paragraph 269 of your declaration, in the prior paragraph, you reference the same portion of Perego that we were just reading, but you reference the concept of keeping channels "in a ready or standby state."

Is that different than keeping the devices on the channels in a ready or standby state?

A. It would be slightly different, but they are intended to describe the same operation. When the devices are in a standby state, one would describe the channel as being in a standby state.

Q. And when you say that, are you saying that specifically for the context of Perego or as a more general matter for memory devices?

A. I think in general, if all of the devices connected to a channel are in a standby state, a person of ordinary skill would -- might say that that channel is in a standby state.

Q. Are you aware of a separate concept in the memory art of having a channel in a ready or standby state as distinct from the memory devices on the channel being in that state?

MR. CHANDLER: Object to form.

THE WITNESS: I can't recall seeing that

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formally. But I think less formally, one might use the descriptive term that a channel is in a standby state to mean that all the devices on the channel, including the host, are in a standby -- well, in this case, "host" might be misleading.

That all the devices connected to the channel, whether they be memory devices or control devices, are in a standby state, where, at least hypothetically, individual devices on a channel can be in a standby state while other devices are not.

BY MR. WARRICK:

Q. Going back to the sentence that we started with on Column 21 of Perego, starting on line 16, I just want to make sure I understand the partial rank access concept that you've mentioned a couple of times today.

I believe you said just a few minutes ago that you understand this sentence to be talking about one rank, including two channels, to be transferring information while another rank, including the other two channels, being in this standby state; is that right?

A. That's my understanding of the example in

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Column 1 -- I'm sorry.

That's my understanding of the example in Column 21 starting at line 16.

Q. So what I'd like to understand is how is that different than having a single rank, including all four channels, that's being partially accessed?

A. Because there's no capability described here that -- that all four channels can respond to a single request.

Again, in a -- in a basic memory system, if we have a 32-bit memory system, in some memory systems that are commercially used, there is an additional capability to only write 8 bits out of the 32. But a person of ordinary skill would not describe that as no longer being a 32-bit memory interface just because it has that additional capability.

This is not being described as an additional capability of a larger interface. This is being described as its primary mode of operation, that channels a and b operate together in response -- in response to a memory access operation, and Channels c and d can operate together in response to a different memory

operation.

Q. Maybe it would be simpler if we looked at Figure 4A of Perego.

And as I understood you earlier today, Dr. Wolfe, you indicated that the embodiment depicted in 4A could include either one rank or two ranks; is that right?

A. No. I said that the patent describes a one-rank embodiment of Figure 4A, and the patent also describes a two-rank embodiment of Figure 4A.

Q. So as between those two embodiments, what is the distinction, in your view, between the two-rank embodiment and a partial access of the one-rank embodiment that involves only one of the channels?

A. Well, we don't know that there is a partial access capability in any of these embodiments. They are not described in Perego, and they may not exist.

So the primary difference would be that in normal operation a one-rank embodiment would access all eight memory devices, and a two-rank embodiment would either access the four memory devices on the left or alternatively access the four memory devices on the right.

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In a two-rank embodiment, one could either access the four on the left or the four on the right. In normal operation, in a one-rank embodiment, all eight would be accessed.

Now, independent of any of the teachings of Perego, if in addition to having the capability of having one rank access all eight you had the capability to only access one memory device, a person of ordinary skill would no -- wouldn't say, "Well, that's no longer a one-rank because it has an additional capability," because a basic read operation would access every memory device. That's what makes it one rank.

Q. Just so I understand, your view is that Perego does not disclose a partial access capability?

A. I don't recall seeing one with respect to a single-rank embodiment of Figure 4A.

Q. Do you recall seeing one in connection with any embodiments of Perego?

A. Not off the top of my head.

Q. Let's look, if we could, at paragraph 48 of your declaration in connection with the '417 patent.

Do you have that in front of you?

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A. I do. It's long, but I have the two pages in front of me.

Q. And in this portion of your declaration, you're describing your view of the person of ordinary skill in the art in the context of the '417 patent; correct?

A. Yes.

Q. And am I right that you propose the same person of ordinary skill in the art in your declaration for the '215 patent?

A. Let me look exactly. They are very similar, but I don't recall if they are exactly the same. The dates may differ a little bit.

It appears to be the same.

Q. And just so it's clear, I suppose that that is also Exhibit 1003 but Exhibit 1003 from the '215 patent IPR.

In this paragraph, you indicate that the hypothetical person of ordinary skill in the art "would have been familiar with various standards of the day including the JEDEC industry standards."

That's your view; correct?

A. Yes.

Q. And would be it fair to say that that

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familiarity with various standards of the day would also extend to Rambus-style DRAMs?

A. I'm not quite sure what you mean by "Rambus-style," but the public Rambus specifications would be known.

Q. Okay. And that would include specifications for XDR, for example?

MR. CHANDLER: Objection to form.

THE WITNESS: I don't remember the exact date for XDR. There were a number of Rambus standards.

BY MR. WARRICK:

Q. But, in your view, those would also be known to the person of ordinary skill in the art in the context of the '417 and the '215 patents?

A. The publicly disclosed Rambus standards at the time would also be known to -- by a person of ordinary skill in the art.

Q. I would like to talk for a little bit -- or more precisely ask you some questions about CAS latency. And perhaps we could start by just asking you to explain your understanding of CAS latency in the concept of memory modules.

A. The exact details of what CAS latency means has varied from memory generation to memory

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generation. But "CAS" stands for "column address strobe." In early memories, it literally was a pulse that was used to capture the column address from the memory controller to the memory devices. In more recent memory technologies, it was a control signal or a command that was used to indicate that on a specific clock cycle the column address should be captured by memory devices.

In general, the CAS signal, in whatever form that it had, was used to indicate the timing of the arrival of the column address information.

Now, sometimes the term is used, a little bit sloppily, to refer to the CAS-to-data-delay value that is also a property of various memory technologies.

Q. So your answer described various different potential interpretations of the term "CAS latency," depending on context. I think maybe it would be helpful for us to talk about the '417 and '215 patents specifically.

Both the '417 and the '215 patent claims reference the overall CAS latency of the memory module.

And what is your understanding of that particular term in the context of the '417 and

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'215 patents?

A. So there seems to be a presumption that there's only one in the claim, which is not necessarily true in certain memory technologies.

Typically, there's a read-latency, which is a function -- which is described often as a CAS latency for reads. And that is the amount of time, again, depending on the technology, from the CAS signal until data starts being returned from the memory module to the host.

In a synchronous memory, it would be defined in clock cycles or half-clock cycles. In an asynchronous memory, it would be defined in a time unit, like nanoseconds.

Oftentimes, there's a different latency for a write operation that would describe how long after the CAS signal the host should send data.

And on some memory technologies, the read CAS latency and the write CAS latency are the same; and in some memory technologies, they are different by a known amount; and in some memory technologies, they are different by a configurable amount.

By "known," I guess I mean "predetermined."

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Q. In the context of DDR or DDR2 SDRAMs -- well, first, those are synchronous; correct?

A. DDR and DDR2 JEDEC-compliant DRAMs are synchronous DRAMs.

Q. And in DDR and DDR2 SDRAMs, the CAS control signal that you mentioned in a prior answer is an integral part of the command bus to the SDRAMs; correct?

MR. CHANDLER: Objection. Form.

THE WITNESS: I don't know what you mean by "integral," but it is a part of the normally used command bus.

BY MR. WARRICK:

Q. In your view, could you have a JEDEC-compliant DDR or DDR2 implementation without the CAS control signal being part of the command bus?

MR. CHANDLER: Objection. Form.

THE WITNESS: There's a variety of JEDEC specifications. The DDR memory chip device requires a CAS signal, and the standard JEDEC DDR2 DIMMs also require a CAS control signal.

BY MR. WARRICK:

Q. So if the DDR or DDR2 memory devices require a CAS signal, does it not follow that that

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signal has to be delivered to the memory devices through the interface?

MR. CHANDLER: Objection. Form.

THE WITNESS: You can have chips in between and still be JEDEC compliant. But there are two different places where CAS signals are required. Their specifications are described within each corresponding JEDEC specification. And in a simple, unbuffered DIMM, it would be common to directly connect them.

BY MR. WARRICK:

Q. So is it correct that an SDRAM will look at the CAS latency -- I'm sorry. Start over.

Is it correct that the SDRAM, in the context of DDR or DDR2, will look at the CAS command signal potentially in combination with other command bus signals to determine the timing of operations?

MR. CHANDLER: Objection to form.

THE WITNESS: For some operations, that is correct, with respect to the CAS signal that is coming into that particular chip.

BY MR. WARRICK:

Q. I want to go back to this language that's

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in the claims of both the '417 and the '215 patents, of the overall CAS latency of the memory module. And I just want to make sure I understand your view of what that means in -- in the context of those two patents. And if you think it's different for the patents, feel free to respond separately.

A. So again, the patents seem to be written based on an assumption that there's a single CAS latency for the module -- the memory module and a single CAS latency for each memory device, which may not be the case in certain real-world technologies.

But the way I would interpret it in the claims is that the CAS latency of the memory device, again, corresponding to the memory device's specification -- you would look at it in the context of the memory device's specification. But in general, it's the amount of time -- in the context of a read operation, it would be the number of clock cycles between the assertion of the CAS signal and the return of data.

So in the case of the memory device, it would be the number of clock cycles between the assertion of the CAS signal at the memory device

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and the return of data from the memory device in response to that particular transaction.

In the case of the module, it would be the number of clock cycles between the assertion of the CAS signal at the input to the module and the return of data corresponding to that CAS signal at the output of the module. And there would be a similar definition for write operations, but they would involve when data is provided to the module and to the chip rather than returned from the module or from the chip.

Q. So when you were talking about the memory device in your last answer, are you referring to the parts of the claims in both the '215 and '417 patents that talk -- that discuss the actual operational CAS latency of each of the memory devices?

A. Yes. That's generally what I was referring to.

Q. Okay. And in both of your definitions for "CAS latency of the memory device" or "the module," you reference the assertion of the CAS signal?

A. Yes.

Q. Is that distinct from the presentation of

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the column access command, i.e., a read or a write command?

MR. CHANDLER: Objection. Form.

THE WITNESS: I believe -- I believe that it can be. There are read and write commands that can happen in DDR2 separately from a CAS assertion.

BY MR. WARRICK:

Q. When you say a "CAS assertion," could you just explain to me what you mean by that term.

A. So it's a term of art. It means that the CAS signal is set at a voltage level that indicates that it is present.

So in particular, in DDR2, the actual signal is not CAS. The actual signal is CAS bar. And it is asserted, meaning the end device is to understand that it is time for a column address strobe when it has the value of zero; and it is unasserted, meaning essentially it's not being communicated, when it has the value of one.

So to avoid confusion between it being there and it not being there, we talked about it being asserted when it's there, even if that's a zero voltage.

Q. So am I correct that in the context of

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DDR2, a read or a write command is really defined by the states of various -- including CAS --

A. I'm sorry. I didn't hear the entire question. Sorry about that.

Q. I'll restate.

There are various states that collectively define commands such as read or write in the context of DDR2; correct?

MR. CHANDLER: Objection. Form.

THE WITNESS: What do you mean by "read" -- I'm sorry. What do you mean by "states"?

BY MR. WARRICK:

Q. Maybe it would help if we go to Exhibit 1064, which is the JEDEC DDR2 specification.

A. Yes.

Q. If we go to page 49, that's -- Table 10 is a "Command truth table"?

A. Yes.

Q. And, for example, NOTE 1 of Table 10 says, "All DDR2 SDRAM commands are defined by states of CS, RAS, CAS, WE and CKE..."?

A. Yes. That's not a -- not a conventional use of the word "states," but it is understandable by a person of ordinary skill in the art.

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Q. And it's that collection of states, as described in Table 10, anyway, that define the read and write commands; correct?

A. It defines the presence of a read or write command, yes.

Q. So a CAS signal alone does not cause a column access operation; correct?

MR. CHANDLER: Object to form.

THE WITNESS: Well, I believe it may cause a column access but not necessarily a read or a write.

I guess in the case of the extended mode register set operation, then there's probably no column access. That's probably a special case.

BY MR. WARRICK:

Q. But a CAS state alone does not trigger a read or write operation; correct?

MR. CHANDLER: Objection. Form.

THE WITNESS: Not alone. It requires certain other signals to have certain other values.

BY MR. WARRICK:

Q. So what I want to make sure I understand is that in an earlier answer, you were describing

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your understanding of these CAS latency terms in the '417 and '215 patents either for a memory device or for the module as a whole. And in that answer, you were referring to the timing of the CAS assertion.

And I'm trying to understand what you mean by that; if you're saying that the CAS latency timing begins when the CAS state first takes on a particular value. Is that what you're saying?

A. Well, in the first place, "CAS latency" is defined for each memory technology; right? There's not a single definition that applies across the industry, and it's just been sloppily claimed.

But if we do our best to understand what it means and assume that it refers to the common technologies of the day, the CAS latency is exactly the way I defined it for transactions that are properly formed.

If you misform a read or a write operation, which means that they are not really a read operation -- write operation, and assert CAS, then the data will not be returned.

Q. If you could look specifically at Claim 1

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of the '417 patent.

A. Okay.

Q. The end of Claim 1 of the '417 patent states:

"...wherein data transfers through the circuitry are registered for an amount of time delay such that the overall CAS latency of the memory module is greater than an actual operational CAS latency of each of the memory devices."

Do you see that?

A. Yes.

Q. What's your understanding of data transfers through the circuitry being registered for an amount of time delay?

A. So I think that this is intended to talk about a clocked system. That's why things are being registered. "Registered" means being stored in a register, stored in a -- in a data storage element. And the amount of time delay in the context of -- of a registered system, the most reasonable interpretation of that would be that it would be some number of clock cycles, one or more.

And what it's saying is that if you delay the response of the memory module by one or more

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cycles over and above the response time of the chip, then the CAS latency, which is a descriptor of the response delay, would increase by that same amount.

Q. When you say the "CAS latency" would increase by the same amount, you're referring to the CAS latency of the memory module; correct?

A. Correct.

So if there is a delay -- a time delay between the memory device response and the memory module response, then the CAS latency of the module will be greater than the amount of that delay in the CAS latency of the device. I mean, it's almost a tautology.

Q. Does Perego, in your view, disclose registering data transfers for this type of time delay such that one or more clock cycles are being added to the CAS latency of the module?

MR. CHANDLER: Object to form.

THE WITNESS: I think it does. Perego discloses that its data output is registered. And a person of ordinary skill would understand that when you delay the output from a device or from a system by registering it, you need to increase any descriptors of

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that delay by the amount of the delay. You can't delay something and not have it be delayed.

BY MR. WARRICK:

Q. Am I to understand you correctly, that by registering the output, you are necessarily delaying the output?

A. When you register it in the ordinary manner, where it is going to exit the register in a subsequent clock to when it enters the register, which is what would ordinarily happen and what is described in Perego, you are necessarily delaying it with respect to the non-registered alternative.

Q. I assume, Dr. Wolfe, that you're familiar with what a latch is?

A. Yes.

Q. How is a latch different from a register?

A. A latch can be used with different clocking structures. And with a latch, rather than delaying -- well, I shouldn't say that.

Rather than delaying the output from a full -- by a full clock cycle, you can merely delay by a propagation delay, which could be less than a full clock cycle, and then you retain that value.

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Q. And when you were describing Perego earlier, you were talking about a register as distinct from a latch; is that right?

MR. CHANDLER: Objection. Form.

THE WITNESS: Yes. I think that that's a disclosed embodiment. And because there's no disclosure in Perego of slowing down the clock or anything like that. And if you had a latch, in Perego's system, you would need to slow it down.

So I think that whether or not Perego explicitly describes using a register, it can use -- it would be obvious to a person of ordinary skill to build a registered DIMM using Perego's technique in order to maintain the data rate, especially in the context of a DDR2 implementation.

BY MR. WARRICK:

Q. Right.

So that would be different than being expressly disclosed in Perego; right?

MR. CHANDLER: Objection to form.

BY MR. WARRICK:

Q. Let me restate.

Dr. Wolfe, Perego does not expressly

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disclose registering the data output as distinct from using latches; correct?

MR. CHANDLER: Object to form.

THE WITNESS: Not explicitly. But what it does describe is generating clocks, clock alignment, to use the latches in a way so there is still a delay in the way that there wouldn't be with a register. And that's why it would be obvious to a person of ordinary skill to use a register, as well.

BY MR. WARRICK:

Q. If we look at Figure 5C of Perego, do you see there are a series of boxes labeled 597f through 597m?

Do you see those?

A. I do.

Q. And towards the bottom of Column 17 of Perego, it's describing Figure 5C, and it references Output Latches 597f through m?

A. Correct.

Q. So that we are on the same page, 597f through m in Figure 5C of Perego are latches; correct?

A. They are. In that embodiment, they are latches.

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Q. And it's data that's flowing through those latches; correct?

A. In those embodiments, that's correct. Of course, in a DDR2 embodiment, you would also have to deal with strobes, which would not be able to be latched.

Q. And just to be clear, Perego itself does not expressly disclose adding an additional clock cycle such that the CAS latency of the module is greater than the CAS latency of the individual memory devices; correct?

MR. CHANDLER: Object to form.

THE WITNESS: It's not that narrow, but it shows adding the latches, which would add a delay. When you're adding a delay, you either have to have the same number of clock cycles with each clock cycle being longer; that would increase the CAS latency; or you have to have more clock cycles with them being the same size; that would also increase the CAS latency.

BY MR. WARRICK:

Q. And what about Exhibit 1064, the JEDEC DDR2 specification, does that expressly disclose adding additional clock cycle?

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A. It discloses the timing in such a way that a person of ordinary skill in the art would know that you either need to -- if you add delay to a memory device -- again, 1064 is just a device specification. It's not the module specification.

But if you read this in -- if you read this in conjunction with the module specification, what you'll see is that you can't simply add delay; that if you are going to have to add delay, you would have to use a registered module, which would need a longer CAS; or you would need to slow down the clock cycle, as is shown on page 64, where it shows the various timings; and there, you can keep the number of clock cycles.

So for example, it shows that if you run something at 533 rates, you might have a CAS latency of 3, with each cycle being longer; or if you ran a chip at 667 rates, the CAS latency might be 4, with each being shorter.

But in either case, you've got to have a certain amount of time involved in order for the device to work.

Q. You mentioned a registered module, but isn't it correct that a JEDEC-registered DIMM does not add any delay to the data path?

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A. I don't think that's true. I think that -- I don't think you can build a registered DIMM that responds in the same amount of time as the underlying memory chip. That just doesn't seem possible. It may be documented in different ways. It may be that the memory controller, knowing that it's using a registered DIMM, adds that extra clock of latency on its own, but the latency is still there.

Q. But a JEDEC-registered DIMM only delays the control and address path, which are separate from the data path; correct?

A. It depends which JEDEC standards you're looking at. If you're looking at, for example, a fully buffered DIMM, it does both.

Q. You referenced a module specification a minute ago.

A. Yes.

Q. Were you referencing a particular module specification?

A. No. Depending on what kind of module you wanted to build, you would pick the right module specification. There have been several of them, I believe, with each generation of -- of DIMM.

Q. Exhibit 1064, which is the JEDEC DDR2

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SDRAM specification, that's not a module specification; correct?

MR. CHANDLER: Objection. Form.

THE WITNESS: Exhibit 1064 is a device specification.

BY MR. WARRICK:

Q. And a device specification is distinct from a module specification; correct?

MR. CHANDLER: Object to form.

THE WITNESS: In the JEDEC form, although there is data in a device specification that would be informative to a module designer.

BY MR. WARRICK:

Q. And what is the JEDEC specification for a DDR2 module?

A. As I said, I believe there are a variety of them.

Q. Are any of them referenced in the Perego reference?

A. I don't recall. Let me look.

There are several of them in the IDS.

Q. Can you give me an example, please.

A. I see JEDEC Standard 21C, and I also see the JEDEC FB-DIMM specification.

Q. Now, earlier, another concept you

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referenced from one of your answers was a fully buffered DIMM?

A. Yes.

Q. Did those exist at the time of the priority date for the '417 patent?

MR. CHANDLER: Objection. Form.

THE WITNESS: I don't know. I'm familiar with the specification being published in 2006, but I don't know when they were first known in the industry.

BY MR. WARRICK:

Q. Does your declaration in the '417 patent IPR reference fully buffered DIMMs?

A. No.

Q. Does your declaration in connection with the '215 patent IPR reference fully buffered DIMMs?

A. I don't see a reference right now.

Q. Okay. I'm on the East Coast, but I know -- I understand you're on the West Coast; so it's probably getting close to lunchtime for some folks. We could either break now, or I could go for another five or ten minutes.

Dr. Wolfe, what's your preference?

A. Another five or ten minutes is fine.

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Q. Okay. Are you familiar, Dr. Wolfe, with the concept of additive latency?

A. Yes. But again, each generation has a slightly different definition.

Q. Well, so, I mean, for example, we could look at Exhibit 1064, the DDR2 spec.

A. Yes.

Q. And if we look at page 14, there's a reference to "Additive Latency" there in the figure.

A. There is.

Q. Do you have an understanding of what additive latency is in the context of DDR2?

A. Generally. I've only had to understand it to the extent that it's applied to issues that I've been interested in. And, of course, these are very complicated specifications, but I think I understand at least most of what it does.

Q. Is it correct that additive latency is a subset of the operational CAS latency of each memory device?

A. Depends what you mean by "operational CAS latency." In DDR2, for ordinary read and write operations, the read latency is calculated based on the CAS latency plus the additive latency.

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The write operation -- the write latency is calculated based on the additive latency plus the CAS latency minus an offset.

I believe there are other less common functions in which the CAS latency is used without the additive latency. And of course, the additive latency can always be set to zero and, in fact, commonly is, in which case it's irrelevant.

Q. Understood.

But my question is: To the extent there is a non-zero additive latency, that is a subset of the memory device CAS latency; correct?

MR. CHANDLER: Objection to form.

THE WITNESS: No, it's not correct. The previous explanation is how it works.

BY MR. WARRICK:

Q. Well, in your answer that you're referencing, you distinguish between CAS latency for reads and writes; correct?

MR. CHANDLER: Objection to form.

THE WITNESS: No, I don't think I did.

BY MR. WARRICK:

Q. So in your prior answer, you referenced read latency and write latency as two distinct concepts; correct?

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A. Two distinct values that are specified in Exhibit 1064.

Q. So your understanding of the read latency is the CAS latency plus the additive latency; is that right?

MR. CHANDLER: Object to form.

THE WITNESS: That's how it's defined in Exhibit 1064 for ordinary read operations.

BY MR. WARRICK:

Q. And that is the read latency of the DDR2 memory device; correct?

A. Correct. Exhibit 1064 is a specification for a DDR2 memory device.

Q. And based on your prior answer, the write latency is the additive latency plus the CAS latency minus an offset; is that right?

MR. CHANDLER: Object to form.

THE WITNESS: That is correct for the memories described in Exhibit 1064 with respect to an ordinary write operation.

BY MR. WARRICK:

Q. So in the context of DDR2, which was described in Exhibit 1064, that write latency is the write latency of the DDR2 memory device; correct?

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A. The write latency defined in Exhibit 1064 is the write latency of a particular DDR2 memory device.

MR. WARRICK: I think I'm at a good stopping point there. So if it's fine with everyone, we can take a break. I'm flexible on timing.

Dr. Wolfe, do you have a preference?

THE WITNESS: 40, 45 minutes would be good.

MR. WARRICK: 45 minutes is fine if that works for everyone else.

MR. CHANDLER: Okay. So 1:10 p.m.

(Short break taken.)

BY MR. WARRICK:

Q. All right. Dr. Wolfe, welcome back.

Before we took a break, we were talking about CAS latency, and I would like to circle back to that for a few questions more.

We talked about the fact that the '417 and '215 patent claims include this phrase [as read]: "Actual operational CAS latency of a memory device."

And I don't know that we had a clear answer from you as to whether you have a view on

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the meaning of that particular phrase.

A. Clearly, it refers to the CAS latency of a memory device independently of whether or not it's been used an a memory module or any particular type of module. As we discussed before, it's somewhat awkward in that it kind of makes an assumption that there's a single CAS latency.

But other than that, I've simply assumed for purposes of my opinions that it refers to the documented CAS latency of the particular memory device that one would use in an implementation.

Q. So for a read operation, for example, under your understanding, would the actual operational CAS latency of a memory device include the additive latency plus the CAS latency?

A. I wouldn't read it that way since there's no discussion of additive latency in the -- in the '417 patent. But since the additive latency can be zero, and often is, in some cases, they could be the same.

Q. And did I understand you correctly earlier today that read latency is the delay between when the memory device receives a read command and when it outputs the requested data?

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A. In DDR2 memory devices compliant with Exhibit 1064, read latency is the number of clocks between the provision of the CAS signal assertion to the memory device and the beginning of providing data in response to that CAS signal.

Q. Okay. So let's shift gears a little bit. So I want to stick with Perego, though. So if we could turn to that. And let's start at Figure 5A in Perego, Exhibit 1071.

A. Okay.

Q. And what does Figure 5A represent?

A. A block diagram of a buffer device according to another embodiment of the present invention.

Q. And you see a box within 5A labeled 560?

A. Yes.

Q. And it's also labeled "OPTIONAL DATA CACHE & TAGS"; correct?

A. Yes.

Q. How does the cache, if it is present, affect the operation of the module?

A. Well, I didn't have to consider that since it's optional. So it's taught as being either present or not present. So I did not analyze that particular case.

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Q. If you look at Column 12, lines 4 through 9 of Perego, it indicates that, "Employing a cache 560 may improve memory access time by providing storage of most frequently referenced data and associated tag addresses with lower access latency characteristics than those of the memory devices."

A. I see that.

Q. And if that's true, how would the presence of such a cache affect the operation of the Perego memory module?

MR. CHANDLER: Objection to form.

THE WITNESS: Again, Perego discloses embodiments without a cache, and that's what I relied on. But if a cache were present, then it's possible that some portion of memory reads and writes could be directed to the cache rather than the memory devices.

BY MR. WARRICK:

Q. So when there's a read request, for example, the data can come from either the memory devices or it could come from this data cache; correct?

MR. CHANDLER: Objection to form.

THE WITNESS: In certain embodiments that I did not rely on, that's correct.

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BY MR. WARRICK:

Q. In Figure 5A, within 560, there's another box labeled 565?

A. Correct.

Q. Do you know what that is?

A. Computation Block 565. And it's rather broad as to what it can comprise. Again, it's optional.

Q. And there's also a Box 550 labeled "WRITE BUFFER" in Figure 5A of Perego?

A. I see that.

Q. And if you look at Column 12, roughly lines 9 through 12, there's some description of that?

A. Yes.

Q. Or 12 through 19 -- or 9 through 12. I'm sorry. Or no --

A. This section goes through 19.

Q. Yes. Thank you. I'm sorry. I misspoke.

Referencing that discussion in Column 12, how does the write buffer affect the operation of the module?

A. The write buffer is described here as an ordinary write buffer, as was known in the prior art. It is also optional. It is only present in

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certain embodiments.

But if it was present, it would have the capability to, at times, defer writing certain data into memory until a later time.

Q. Does Perego say the write buffer is optional?

A. He says it's only in some embodiments. So that would mean that it's not in all embodiments.

Q. Going back to the data cache, 560, is it correct that if in response to a read request, the data is delivered from the cache rather than the memory devices, it will be delivered sooner than if it had come from the memory devices?

MR. CHANDLER: Objection. Form.

THE WITNESS: Again, the cache is optional. It's not the embodiment that I relied on.

If that were the case, again, it would depend on design details. But presumably one would only use the cache if it returned data sooner than the memory devices. It would be a special case, again, in that optional configuration.

///

BY MR. WARRICK:

Q. All right. Could we -- could you turn, please, Dr. Wolfe, to Exhibit 1062.

A. Sure. That's the '417?

Q. Yes. Well, I believe it's actually the same exhibit in both IPRs.

A. Okay.

Q. And you recognize that document?

A. Yes.

Q. What's Exhibit 1062?

A. Exhibit 1062 is the registered DIMM specification for DDR not DDR2 memories.

Q. And you're familiar with this specification?

A. Generally. It's got thousands of parameters. I don't know them all. But I have used it before.

Q. And you cited it in your declarations; correct?

A. Yes.

Q. Do any of the modules disclosed in this specification include a cache?

A. In the same manner as in Perego?

Q. Well, I guess we could start with at all, first.

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A. The way that a person of ordinary skill would normally define a "cache," no.

Q. And do any of the modules disclosed in Exhibit 1062 disclose a cache that is similar to the one disclosed in Perego in Figure 5A?

A. No. Again, I think that's why Perego makes it optional, is that would have been unusual to include it on a memory module at that time.

Q. Do any of the modules disclosed in Exhibit 1062 include a write buffer?

A. Not that I'm aware of. Again, by the time of Exhibit 1062, although it was known to put a cache or a write buffer on a memory module, it was not very efficient to do it that way.

So that's, again, that's why I believe Perego made it optional; both the cache and the write buffer, by 2002, would most commonly be placed closer to the processor than the memory module.

Q. What about a computational engine? Any of the modules in Exhibit 1062 disclose that?

A. No. Again, that's probably why it's optional in Perego, is that it would have been unusual.

Q. In Exhibit 1062, the JEDEC specification,

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is it correct that the delay in cycles between a column access command and the data is fixed based on the particulars of the DRAMs present on the module?

MR. CHANDLER: Objection. Form.

THE WITNESS: It is fixed based on the DRAM -- well, no, that's not the case. It depends what speed you're running the device at.

BY MR. WARRICK:

Q. For any given speed is that a true statement?

MR. CHANDLER: Objection. Form.

THE WITNESS: No. I believe it's still configurable.

BY MR. WARRICK:

Q. And how would you configure that within the context of Exhibit 1062?

A. I don't have the DDR memory spec in front of me, but I believe that there was a configuration register that would be programmable on each of the devices.

Q. So is it your view that according to the JEDEC spec there can be variability in the timing of data relative to the commands?

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MR. CHANDLER: Objection. Form.

THE WITNESS: I'm not sure what you mean by "variability," but not every system needs to set the cache latency for particular devices the same way.

BY MR. WARRICK:

Q. Well, you used the word "configurability" earlier.

Maybe a better question is: In your view, there's configurability within the timing of the data relative to the commands in the modules defined in Exhibit 1062?

MR. CHANDLER: Objection. Form.

THE WITNESS: Yes, they can be configured.

BY MR. WARRICK:

Q. Is it correct that in the modules defined in Exhibit 1062, the memory controller will know when read data will be returned to it?

MR. CHANDLER: Objection. Form.

THE WITNESS: In operation it will, yes.

BY MR. WARRICK:

Q. Is it fair to say the controller is in complete command of the module in terms of the timing?

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MR. CHANDLER: Objection. Objection to form.

THE WITNESS: No. I think that's a stretch. I think that it would be compatible. Because the module is compliant with a standard, it would be able to predict the behavior of the module once the module has been configured.

BY MR. WARRICK:

Q. So in the Perego embodiments that include the data cache, they are very different than the JEDEC modules defined in the specification of Exhibit 1062; correct?

A. Well, I didn't rely on the embodiments that include the data cache. It's optional. I wouldn't say they were very different. I would say they have an additional feature that's not present in 1062 if the optional data cache is -- is included in Perego.

But it need not be.

Q. And we can look at Figure 5B of Perego.

And you see, you have the Interface 596 towards the bottom of Figure 5B?

A. I see that.

Q. Is there any indication that the

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character or capabilities of that Memory Bus Interface 596 or the memory bus depend on whether or not the cache is present?

A. I don't recall Perego being specific about it one way or the other.

Again, Perego's very open-ended in explaining that all kind of memory interfaces can be used there, including standard memory interfaces.

Q. Well, let me ask this: In embodiments of Perego that do include the data cache, in the circumstance where there is a cache hit, it's correct that the data will be returned more quickly than the memory controller would expect, compared to a module that does not have such a cache?

MR. CHANDLER: Objection. Form.

THE WITNESS: One would expect that if someone chose to use a data cache -- which, again, I did not rely on any embodiments with the data cache on the memory module. But if one chose to use that embodiment, presumably one would choose to use an interface that could receive the results back at different times, because there would be no point in

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using an optional data cache unless one could take advantage of the improved speed.

So one would choose, in that particular circumstance, a host interface that could recognize that particular situation.

BY MR. WARRICK:

Q. And just so we're clear, the write buffer, unlike the data cache of Perego, is not an optional feature; correct?

MR. CHANDLER: Objection. Form.

THE WITNESS: It clearly is, because Perego teaches that some embodiments have the write buffer and other embodiments don't.

BY MR. WARRICK:

Q. The write buffer, however, is not described as optional in the context of the embodiments of Figures 5A or Figure B of Perego; correct?

A. I think it is. The patent refers you to those figures and then says that in some embodiments the write buffer is present. It doesn't say embodiments other than 5A and 5B. I think a person of ordinary skill would understand that as being a completely optional feature.

And even if Perego hadn't stated it, a

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1 person of ordinary skill in the art would
2 understand that in this particular environment, a
3 write buffer would be optional.
4 Q. You would agree at minimum, though, that
5 the Write Buffer 550 in Figure 5A is not labeled
6 as optional in the same manner as Data Cache 560;
7 correct?
8 MR. CHANDLER: Object to form.
9 THE WITNESS: It's not labeled that way
10 on the drawing. It doesn't say the word
11 "optional." It's a smaller box. But it's
12 clear from the text that it is optional and
13 that the signals to it are optional. They
14 are actually even described as optional.
15 BY MR. WARRICK:
16 Q. Let's talk about the '215 patent, if we
17 could. That is Exhibit 1001 from the '215
18 patent's IPR.
19 A. Okay.
20 Q. And if we look at Claim 1 of the '215
21 patent, you'll see one of the elements begins
22 with:
23 "A register coupled to the print -- to
24 the printed circuit board and configured to
25 receive and buffer first command and address

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signals."

Do you see that?

A. I see that.

Q. Now, Perego does not disclose this register in Claim 1 of the '215 patent, does it?

A. I think a person of ordinary skill would understand Buffer Device 350 to include a register.

Q. Did you express that view in your declaration for the '215 patent IPR?

A. Yes. Paragraphs 251, 252.

All the way through somewhere around 255 or 256.

Q. Can you point me to where you specifically offer the view that the Buffer 350 from Perego includes a register.

A. Paragraph 251. "Perego discloses that a 'register' in its buffer device (e.g., 350) is coupled to the printed circuit board..."

And then it goes on from there.

And then in particular, at the end of paragraph 254, I quote the portion of Perego where it explains that [as read]:

"'...buffers disposed on conventional DIMM modules are employed to buffer or

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register control signals or address signals.'"

Q. Is there a difference, in your view, between a buffer and a register?

A. There can be in different contexts. But I believe in this context, especially in light of Perego's disclosure in Column 6, that he is expressing the view that his buffer can be a register.

Q. Turning back to Perego, we discussed the fact earlier that Perego describes a configurable width module; correct?

A. Right. Perego does describe that some of his embodiments have configurable width modules that can be configured in various ways.

Q. Can you have a configurable bit width module that is compliant with JEDEC specifications?

A. I would think so, because if you read Perego, he indicates that one of the ways of configuring it is to have a resistor or a jumper that's installed at manufacture time that configures it to a fixed bit width. In that case, I think it can certainly be JEDEC compliant.

Q. Well, in that case, if you have something

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that's constraining an embodiment of Perego to a fixed bit width, it's no longer a configurable bit width module; correct?

MR. CHANDLER: Objection. Form.

THE WITNESS: It's a matter of semantics. You know, I mean, it's what Perego calls a variable -- a configurable bit width module.

But I would agree that once it's been configured, especially if it's been configured at manufacturing time, then a reasonable person might no longer treat it as configurable. But that's exactly what's described in Column 16 of Perego.

BY MR. WARRICK:

Q. Are you aware of any JEDEC-compliant memory modules that have configurable bit width?

A. I can't point you to one off the top of my head, but I'm quite certain they are out there. I'm also completely certain that they are out there.

For example, there are modules that -- that work at 64 or 72 bits.

Q. And in that particular context, is that a function of whether or not error correction is being employed?

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A. In many cases, that would be the reason but not necessarily.

Q. We discussed earlier that some of the figures in Perego depict what you would describe, I believe, as a well-known Rambus memory bus; is that right?

MR. CHANDLER: Objection. Form.

THE WITNESS: Yes. That would be my understanding.

BY MR. WARRICK:

Q. And a Rambus bus is very different than a JEDEC SDRAM bus; correct?

MR. CHANDLER: Objection. Form.

THE WITNESS: Depends what you mean by "very different."

My recollection is that Rambus thought there were enough similarities to file a few dozen lawsuits.

BY MR. WARRICK:

Q. Do you view a Rambus bus and a JEDEC SDRAM bus as similar?

A. Again, I haven't tried to do that comparison, but my understanding is there are some features that are quite similar and some features that are quite different.

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Q. Is it true a Rambus bus is generally narrower than a JEDEC bus?

A. Debatable. A number of people would say that's why it failed; that in practice, in order to get equivalent performance, by the time you set up multiple channels of Rambus memory in a device, you would typically have the same number of wires as if you set up a single, wider DDR bus. It's just a question of the details of how those wires are behaving.

Q. A Rambus uses a packet protocol, doesn't it?

MR. CHANDLER: Objection to form.

THE WITNESS: A direct Rambus certainly used a packet protocol for certain functions, as did the later fully buffered modules in DDR.

BY MR. WARRICK:

Q. The DDR and DDR2 specifications we've looked at today, however, do not include a packet protocol; correct?

A. Depends how you define a "packet protocol." There certainly are packetized bursts of data that are sent, but it's not packetized control or address protocol in the same way as

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Rambus.

Again, I think that's why Perego made it clear that there were various kinds of memory that would work with his invention.

Q. So I don't know if this is what you're referring to, but Column 8, lines 1 through 9, of Perego mentions several different types of memory devices and claims that those could be used within the modules it discloses.

A. More specifically within the described embodiments.

Q. So for example, Column 8 of Perego mentions DDR. It also mentions XDR, SRAM, FRAM, MRAM, Flash, ROM.

Those various types of memory devices are not freely interchangeable, are they?

A. Depends what you mean by "freely interchangeable." You cannot remove one and replace it with another in certain cases, but a person of ordinary skill would know how to redesign an interface using routine methods to replace one with another; and they are all designed to speak to a microprocessor.

Q. And we discussed earlier that in Perego, if you were to use JEDEC-compliant DDR2 memory

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devices, you would, in fact, have to modify other parts of the memory module to make it work; correct?

MR. CHANDLER: Object to form.

THE WITNESS: Yes. You would need to make modifications at the detail level that are routine within the industry.

BY MR. WARRICK:

Q. When you say "routine within the industry," are you referring to others who have modified a Rambus bus module to use JEDEC SDRAM memory devices?

A. No. Because, again, Perego tells us that his embodiments are compatible with DDR. A person of ordinary skill would know how to build a memory interface for a variety of different known memory types by following the specifications.

And there's no reason, in view of Perego, why they would necessarily need to use a Rambus-compatible memory interface. Perego teaches that the interface need not be a Rambus-compliant interface, either.

So a person of ordinary skill would be fluent in designing memory controllers and memory interfaces and would be able to take the teachings

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of Perego and use them for at least any of the recited types of memory.

Q. Well, I believe you stated earlier that in order to use DDR2 devices with Perego, you would you need to make changes to the interface, as well as the buffer device of Perego; is that right?

A. No. If that's what I said, I misunderstood the question.

I thought you asked me, if one were to take a Perego embodiment that used Rambus and replace that with DDR, would you need to make changes? In that case, you would need to make some changes, but they are changes that are routine.

You could not implement Perego using Rambus without looking up the Rambus spec, and you could not implement Perego with DDR or DDR2 without looking up the corresponding specs. There's too much detail to be able to do it without using the public specifications.

Q. So I think I understand your view that someone of ordinary skill in the art would be able to construct either a Rambus interface or a JEDEC-style interface and that that would be

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routine.

I just want to be clear, are you saying it's also routine to adapt a Rambus interface to work with DDR2 memory devices?

A. I don't think Perego requires that in any way, but I think Perego teaches it. So together with the teachings of Perego, I think it would be routine.

Q. Are you aware of anyone doing that?

A. Well, it only would have been interesting in 2006. So I don't recall whether anybody did it back then. Maybe even earlier, starting in maybe '99 through 2007. I don't recall whether or not anybody did it then, but --

Q. You're not aware of anyone?

A. Not off the top of my head. But again, that would have -- that would have been primarily for economic reasons that DDR memory was just cheaper. And most manufacturers, particularly PC manufacturers, would -- would provide you your choice of a Rambus or DDR memory controller.

Q. If we started with one of the Rambus modules of Perego and substituted DDR2 memory devices and then made the changes to the interface and the buffer that you referenced earlier would

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be necessary, or a working module, what aspects of Perego would be left in such a device?

MR. CHANDLER: Objection. Form.

THE WITNESS: Well, I'm not sure anybody would ever need to go through that process, because Perego teaches you how to directly implement his -- his invention with a variety of memory types.

But if you decided to take Perego and implement it with a non-Rambus memory type, as is taught, you would still have, perhaps, factory configurability. You would have -- perhaps have the ability to have a buffer that performs rank multiplication across two different ranks. So there would be a number of advantages.

BY MR. WARRICK:

Q. Would you still have a configurable width buffer?

A. It depends on what time. Again, that's a feature that he teaches. But he also teaches that it can be fixed at manufacturing time.

Q. But if you took the Rambus embodiment and, again, substituted the DDR2 memory devices and made the necessary changes to the interface

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and buffer to work with those devices, would you still have a configurable bit width buffer?

A. Well, again, I'm not sure why you would do that rather than applying the teachings of Perego directly to DDR as he suggests.

But if you did go through that process, I think you could certainly still have a configurable bit width buffer, because you could -- you could configure it in different ways, as suggested by Perego.

I don't know that -- I mean, I haven't relied on that kind of embodiment. I've relied on the embodiment that's taught, in which you would fix the bit width at manufacturing time.

Q. Just so we're all on the same page, can you refer me to the particular part of Perego you're referencing when you talk about fixing the bit width at manufacturing time?

A. Column 16, lines 53 through 65. It talks about [as read]:

"...state storage -- various types of state storage are possible, including but not limited to manual jumpers and switch settings and module presence detection or type detection mechanisms. The latter class may

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include pull-up or pull-down resistor networks" -- which one would provide at manufacturing time - "tied to a particular logic value (high or low), which may change state when a module is added or removed from the system."

And again, that is all permissive language. So it certainly could be fixed as well.

Q. And am I understanding you correctly that this embodiment of Perego -- or should I say embodiments of Perego that include this permissive feature of fixing the bit width at manufacturing, those are the only embodiments in Perego on which you rely?

MR. CHANDLER: Objection. Form.

THE WITNESS: No. I relied on all the teachings of Perego. But certainly Perego talks about embodiments with a serialization ratio of one-to-one, either factory fixed or in operation as configured at run time, and I think either of those would make the '215 obvious, and the '417.

BY MR. WARRICK:

Q. So is it fair to say that you're only relying on Perego embodiments that, in your view,

include a fixed width module?

MR. CHANDLER: Objection to form.

THE WITNESS: I mean, there's 800 pages in the report. We would have to go through and look at every dependent claim.

But for the independent claims, the one-to-one operation is enough to make the independent claims obvious.

BY MR. WARRICK:

Q. I want to go back to the modifications that would be necessary for Perego to utilize DDR2 memory devices, which I believe you indicated would be routine, in your view --

A. No, that's wrong. I never said it would require modifications to Perego to use DDR2.

What you asked me is if you implemented Perego with Rambus first and then switched to DDR2, would you need to make modifications; and you would.

But Perego teaches you how to make DDR2 embodiments. You would not need to modify Perego to make DDR2 embodiments.

Q. So I understand there are portions of Perego that indicate that one could use different types of memory devices. And, for example, we had

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1 looked at Column 8 a few minutes ago, which
2 mentioned a lot of those devices.
3 But it's your view that Perego also
4 teaches a person of ordinary skill how to
5 implement a Perego module using DDR2 specifically?
6 A. Yes, based on a person of ordinary skill
7 in the art's existing knowledge of DDR2. Perego
8 is explicit that none of the things that he shows
9 in an exemplary way are limiting. He talks about
10 how you could have point-to-point links or bus
11 topologies. He's clearly not limiting it to an
12 RDRAM. He talks about different kinds of control
13 signals, including individual selects, again,
14 helping someone to understand how they would
15 implement it with a DDR.
16 So as a person of ordinary skill reading
17 this disclosure with Perego's additional
18 disclosures that the features that are
19 Rambus-specific are not limiting, would understand
20 how to apply these concepts in a DDR2
21 implementation, based on what Perego teaches.
22 Q. Well, you would agree that not limiting
23 the scope of what's described in Perego is not the
24 same thing as teaching someone how to construct a
25 particular embodiment for a particular type of

memory device; right?

MR. CHANDLER: Object to form.

THE WITNESS: It's not the same, but it's also not what I said.

A person of ordinary skill would already know how to build the individual components that are DDR2-specific, how to build DDR-specific -- -2-specific interface; what DDR2 control signals look like; what DDR2 timing looks like.

And Perego specifically tells the reader that that's within the scope of this invention. So therefore, when Perego uses an example, the person of ordinary skill would apply that example to their existing knowledge and not try to interpret Perego's example as limiting the embodiments or instructing the reader not to apply that existing knowledge that's already been suggested.

BY MR. WARRICK:

Q. I apologize if you can hear the noise. I am in Washington, D.C., at our office, and there seems to be some sort of --

A. We're not hearing it.

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MR. CHANDLER: I don't hear. It just you. No protesters.

MR. WARRICK: Okay. It's a common event here. It's a hazard of the location.

BY MR. WARRICK:

Q. Okay. So, Dr. Wolfe, I understand you to be saying that a person of skill would know how to build a system that would work with these different types of memory devices; and that Perego indicates to such a person that any number of memory devices could be used; and that generally, a skilled artisan would know how to construct a system according to Perego that would work with those different types of memory devices.

Is that a fair summary?

A. I think that's generally correct, yes.

Q. But is there anything in Perego that specifically teaches a person of ordinary skill how to implement its modules with DDR2 memory devices specifically?

A. Yes. At the level of instruction that a person of ordinary skill needs, simply describing where the interfaces are, what order things happen in, how things are generally interconnected, is enough. It's not necessary for a person of

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ordinary skill to list out the signals. It's not necessary for Perego to repeat the contents of Exhibit 1064 to a person of ordinary skill, because that's already within their knowledge.

Q. Now, Exhibit 1064 is the specification for the memory devices themselves; correct?

A. Correct.

Q. Not for the JEDEC DIMM?

A. No. But they would convey a lot of operational details. There are other JEDEC compliance factors, like pin capacitance and such, that would be specific to some other specification.

Q. Well, there are some key aspects of a DDR2 or a DDR-compliant module that are not disclosed in Perego, such as chip select signals; correct?

MR. CHANDLER: Objection. Form.

THE WITNESS: Well, it does disclose that you can have individual select signals to the individual devices.

It also points to DDR, which any person of ordinary skill would understand requires a chip select signal.

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BY MR. WARRICK:

Q. But a DDR memory device requires a chip select signal; correct?

A. It does. But also, DDR-compliant DIMMs all have chip select signals.

Q. And, in fact, they require chip select lines as well; correct?

A. DDR-compliant DIMMs do have chip select lines.

Q. And those chip select lines are not disclosed in Perego; correct?

MR. CHANDLER: Objection. Form.

THE WITNESS: It talks about individual module control lines in Column 1, with respect to a conventional memory system. I think it's disclosed there.

I think it -- the RQ scroll lines, it says, may comprise individual control lines, including selection lines.

And if we look at the figures in Perego, it describes the external connections as RQ lines.

So I do think it's disclosed.

BY MR. WARRICK:

Q. But you would have to agree that chip

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select lines are not expressly disclosed in Perego; correct?

A. It says the control lines RQ can have individual device select lines.

As a person of ordinary skill, I would understand those to be chip select lines.

MR. CHANDLER: Whenever is convenient. It's been about an hour.

MR. WARRICK: Yeah, we can pause here, and maybe this commotion will die down by the time we come back.

(Short break taken.)

BY MR. WARRICK:

Q. Dr. Wolfe, before, we were talking about the teachings of the Perego reference and specifically the possibility of using different types of memory devices with Perego.

And we had referenced Column 8, which discloses DDR, along with several other types of memory devices.

And I believe it was your opinion that any of those could be used with Perego, in view of the knowledge of the skilled artisan; is that right?

A. Yes, in at least some embodiments of

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Perego; but specifically DDR, which is listed in that first category, along with direct Rambus.

Q. Is it the case that even with something like flash memory, that a skilled artisan would be able to incorporate that into Perego as a routine matter?

A. Yes. The -- there would be more differences between a flash memory implementation and a Rambus implementation than between a DDR implementation and a Rambus implementation.

But this has to all be considered from the perspective of a person of ordinary skill in the art, who, by this time, you know, the art of interfacing memories to microprocessors is certainly more than 30 years old and was quite broad.

Q. Before the break, we were talking about chip select signals and chip select lines.

And you agree that those are necessary for a DDR2 implementation of Perego; correct?

MR. CHANDLER: Objection. Form.

THE WITNESS: An implementation of Perego using JEDEC-compliant DDR chips would have chip select lines.

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BY MR. WARRICK:

Q. Now, in Perego, I would like to look specifically at Column 10; and Column 10, lines 63 through 67. It's at the bottom of Column 10.

And Perego says, "Different types of memory devices may be included on different modules within a memory system, by employing buffer device 405 to translate protocols employed by controller 310 to the protocol utilized in a particular memory device implementation."

Did I read that correctly?

A. I believe so.

Q. So is this part of the -- I'll rephrase.

Is this the teaching of Perego that you referenced earlier when you discussed Perego teaching the skilled artisan how to incorporate DDR2?

A. No. Perego teaches that DDR2 can be used generally, but he also teaches that in some embodiments one can choose a different protocol for the host interface than one does for the individual device interface. It teaches them both.

Q. Would you agree this would be a simpler modification of Perego than modifying the entire

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module to use DDR2?

MR. CHANDLER: Objection. Form.

THE WITNESS: It's not necessary to modify the module to use DDR2; only to implement it that way, as Perego teaches.

BY MR. WARRICK:

Q. Is there any disclosure in Perego that teaches you how to perform the translations that are described at the bottom of Column 10?

MR. CHANDLER: Objection. Form.

THE WITNESS: Not specifically. Translating from one memory protocol to another is not required by Perego, but it would be within the skill of a person of ordinary skill in the art.

BY MR. WARRICK:

Q. So, in your view, a person of skill in the art could take an incoming signal to the Perego buffer that is not JEDEC-compliant and then translate that into the signals necessary for a DDR2 memory device?

MR. CHANDLER: Objection to form.

THE WITNESS: A person of ordinary skill in the art could do that, but that's not necessary in order to implement Perego with

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DDR2.

BY MR. WARRICK:

Q. But that's what this particular embodiment is describing in Perego; correct?

A. That is within the scope of that one particular embodiment discussed in that one particular paragraph.

Q. And in that embodiment, the buffer of Perego would not receive chip select signals, for example, from the memory controller; correct?

MR. CHANDLER: Object to form.

THE WITNESS: I disagree. The Rambus protocol, for example, does include chip select signals. They are simply multiplexed on to the same wires as other signals, in a packetized form.

BY MR. WARRICK:

Q. Now, Column 9 of Perego talks about "control lines (RQ)."

And it says they "...may comprise individual control lines, for example, row address strobe, column address strobe, etc., and address lines."

I believe you referenced that earlier?

A. Yes.

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Q. And Perego, in that context, is referring to the interface between the buffer and the memory devices; correct?

A. I don't know -- I don't know why we would assume that. He has two different place where -- places where he uses the label "RQ."

Q. That same paragraph in Perego discusses the need in some cases to "increase the number of parallel signal connection paths"; correct?

A. In some cases, yes.

Q. And Perego says that that would increase the "system layout resource requirements"; right?

A. With respect to a narrow packet protocol approach, not necessarily with respect to other approaches.

Q. Would you agree that system layout resource requirements would be a factor when one is deciding how to implement a memory module?

A. It could be a factor. But we know both at that time and prior and subsequently, the vast majority of -- the majority of the market chose to use parallel signal connection paths and not a narrow packet protocol approach.

Q. You mentioned earlier that Rambus included chip select signals.

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Did I read that correctly?

A. It does include chip select signals in -- in its packetized information. And, in fact, Figure 6A essentially confirms that, if we assume that it can describe a Rambus-like implementation, because we see the packetized information coming in on 620a and then being distributed as chip select signals on 633a and 633b.

Q. But Rambus does not include chip select lines; correct?

MR. CHANDLER: Objection to form.

THE WITNESS: Rambus protocols at that time did not include distinct chip select wires, as far as I know.

But at the same time, Columns 9 and 10 do teach that they could be used in that kind of an environment.

BY MR. WARRICK:

Q. Going back to your proposed claim construction for the term "rank" in the '417 and '215 patents, one thing we didn't discuss earlier specifically is the fact that it includes chip select signals.

And specifically, again, your proposed construction is "...an independent set of one

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or more memory devices on a memory module that act together in response to command signals, including chip select signals, to read or write the full bit-width of the memory module"; correct?

A. Yes.

Of course, it's important to understand that when we talk about chip select signals, a rank select signal is often called a chip select signal, in practice, in the industry. A chip select signal is not limited to selecting a single chip.

Q. So under your construction, for a set of memory devices to constitute a rank, is it necessary for a chip select signal to be applied to all of those devices?

A. They all need to know that it's their turn to respond. So there would need to be a chip select signal or some equivalent.

Q. And is it correct that all the memory devices within a given rank have to have the same chip select signals applied to them?

A. No. They just need corresponding chip select signals. If you replicate a signal or something else similar that tells them all that

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they need to respond at the same time, they are still a rank.

Q. So why -- why are chip select signals a part of your proposed construction for these two patents?

A. Again, I'm trying to describe the way the -- the way the word "rank" is ordinarily used in the context of these patents with a memory module.

And part of that ordinary meaning with respect to this patent is that the chips respond together or perform a write operation together when they are told it's their turn and not at some random time. So I was trying to describe that.

And again, that's consistent with what the '417 patent says.

Q. Are you aware of examples where different memory devices within the same rank receive different chip select signals?

A. It depends what you mean by "different chip select signals." It's certainly true that when a rank gets large, it is common to replicate the chip select signals so that there are a bunch that all operate at the same time.

Q. If you had two groups of memory devices

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that are supplied with different chip select signals, then those devices would not be considered to be part of the same rank, would they?

A. Depends what you mean by "different chip select signals." Certainly, the way that I described before, they would.

If they never operate together in response to command signals, then they would not be in the same rank.

Q. But, in your view, they would not necessarily have to receive -- I'll rephrase that.

In your view, the memory devices within a rank do not necessarily have to receive the same chip select signals in order to be part of the same rank?

MR. CHANDLER: Objection to form.

THE WITNESS: Again, it depends how you're defining those words. They have to receive corresponding chip select signals so that they know that they are being selected at the same time. But they don't -- there doesn't need to be one physical wire connecting them all. Chip select signal can be replicated.

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BY MR. WARRICK:

Q. And are the replicated chip select signals identical to the original chip select signals?

A. They are identical enough for their suited purpose.

Q. And so memory devices within a rank would have to receive chip select signals that have at least that degree of identity; correct?

A. No. I mean, again, the purpose of the word "rank" is to help a person of ordinary skill identify which devices are in the same rank and which devices are in different ranks.

And the ones that are acting together in response to command signals, including chip select signals, to read or write the full bit width of the memory module, are the ones that are in the same rank.

And if they are acting together in response to the chip select signals, to read or write the full bit width of the memory module, then they are in the same rank, even if there are tiny differences between copies of the chip select signals.

Q. I believe in your declaration for the

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'417 patent, Dr. Wolfe, you indicated that for Ellsberry, the separate reference, the individual memory devices could receive something different than a chip select signal to indicate whether or not they are participating in a rank; is that fair?

MR. CHANDLER: Objection to form.

THE WITNESS: The particular portion of my declaration that you're referring to?

BY MR. WARRICK:

Q. Just a second. I apologize. I think I have a mistake in my notes. Let me ask you more generally, though.

For Ellsberry, does Ellsberry include chip select signals?

A. I don't recall off the top of my head. I'd have to go through my -- my report.

Q. Okay --

A. But again, I didn't rely on Ellsberry alone. So I only relied on Ellsberry in combination with Perego and JEDEC, and they both disclose chip select signals.

Q. So are you saying you did not rely on Ellsberry for the disclosure of chip select signals?

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A. No. I just said I don't recall if I also rely on Ellsberry for the disclosure of chip select signals.

But they are disclosed in the two base references, as well.

Ellsberry is 1073?

Q. Correct. And it should be in the Exhibit Share, as well.

A. I mean, Ellsberry definitely has chip select signals.

Q. And, my question, then, is: Do the chip select signals in Ellsberry play a role in which memory devices participate in a given rank?

A. Yes. In Ellsberry alone, that would be true.

Q. What about the no-operation function?

A. Ellsberry -- Ellsberry also teaches that one can use a no-op command as a rank select.

Q. So your understanding is that Ellsberry could use either a chip select or a no-op command for rank selection?

A. My understanding is that that's what a person of ordinary skill would understand with respect to Ellsberry.

Q. In your declaration, you cited a textbook

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that describes ranks as including memory devices that operate in lockstep.

Do you agree that memory devices within a rank have to operate in lockstep with each other?

A. Do you recall the exhibit number?

Q. It's in -- if you look at your '417 patent declaration at paragraph 128, it references Exhibit 1070.

A. I think it was around page 9; is that right?

Q. It's page 104, paragraph 128 of the '417.

A. The page in the reference -- I want to make sure I get the exact language out of the book -- page 6.

Q. So what I'm referencing, if you look at your declaration, it has a quote --

A. Oh, page 413.

Q. 413 from Exhibit 1070. And you have it quoted in a parenthetical.

The quote is, "Essentially a rank of memory is a 'bank' of one or more DRAM devices that operate in lockstep in response to a given command"?

A. Right. And that's what's important, if it says, "one or more DRAM devices."

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So, yes, the "one or more DRAM devices" have to operate in lockstep. But clearly that can be either one or more.

Q. So I want to circle back to the "one or more." But, first, operating in lockstep, that is equivalent to the "acting together" portion of your proposed construction of the term "rank"?

A. Yes. It does say in "a given command." So my "acting together" is specific to the read and write commands.

Q. Understood.

Now, in terms of "one or more," does Perego disclose a memory module with only a single memory device per rank?

MR. CHANDLER: Objection. Form.

THE WITNESS: It certainly seems to claim one. I don't see anything in the claim that requires multiple memory devices in a rank.

BY MR. WARRICK:

Q. But do any of the embodiments described in the specification of Perego include only a single memory device per rank?

MR. CHANDLER: Objection to form.

THE WITNESS: I don't recall. It was certainly nothing that -- I mean, the

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abstract says that the buffer device is coupled to at least one memory device.

The first line of the "DETAILED DESCRIPTION" says, [as read]: "...one or more memory -- semiconductor memory devices coupled to a buffer device."

BY MR. WARRICK:

Q. But of the specific embodiments described, do any of them include only a single memory device per rank?

MR. CHANDLER: Objection to form.

THE WITNESS: Column 7, line 62, in describing the Figure 3C embodiment, it says that you can access data from one or more of the memory devices.

I mean, it's pretty consistent that Perego doesn't care whether you have one or more memory devices in a rank, either in his abstract or his specification body or his claims.

BY MR. WARRICK:

Q. But you agree that there's not a specific embodiment described that shows one memory device per rank; correct?

MR. CHANDLER: Objection to form.

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THE WITNESS: I just told you Figure 3C is described as having at least one memory device, both at Column 7, line 63, and again at line 67.

Column 12, line 16, again, with respect to an embodiment, refers to [as read], "at least one memory device over an interface."

Column 15, line 1, it talks about having an embodiment with "one or more memory devices."

And again, later in that paragraph.

BY MR. WARRICK:

Q. I think that's slightly different from what I'm asking. But I think it's best that we move on.

Sticking with Perego, though, I think we covered earlier that Perego teaches using address signals to select specific signal lines for responding to a read or write command; is that right?

MR. CHANDLER: Objection. Form.

THE WITNESS: It does describe that with respect to the specific embodiments, yes, person of -- but it's permissive.

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BY MR. WARRICK:

Q. So in that context, is it correct that not all the devices within the rank need to participate in responding to a read or write command?

A. I don't know what you mean by they "need to," but in a straightforward, ordinary embodiment, they would.

Q. Well, is it possible, for example, in that case, for all of the devices within the rank to receive a low chip select signal, and then the address signals would specify which devices would provide a data burst?

A. No. It just doesn't work that way.

Q. Let's look at Halbert for a few minutes, if we could. That's Exhibit 1078. It should also be in the Exhibit Share.

A. Okay.

Q. And you're familiar with this document as well?

A. Yes.

Q. And Figure 4 in Halbert is an embodiment of the alleged invention of Halbert; correct?

A. It's a block diagram for a memory module, according to one embodiment of the invention.

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Q. Okay. And Figures 5 and 6 show the operation of that embodiment; correct?

A. Yes, under certain circumstances.

Q. Now, looking at Figure 4 of Halbert -- in the upper right corner within what's labeled a "MEMORY DEVICE ARRAY," we have "Rank 140" and "Rank 142"?

A. Yes.

Q. And those together form the memory device array, correct, in Halbert?

A. Yes.

Q. And the memory device array in Figure 4 of Halbert is presented with an address and command bus, specifically RADD/RCMD, from the module controller; correct?

A. Yes.

Q. And as a result of being presented with a common command and address bus, specifically RADD/RCMD, do you agree that Rank 140 and Rank 142 operate in lockstep with each other?

MR. CHANDLER: Objection. Form.

THE WITNESS: Sometimes they do, and sometimes they don't. If you look at Figure 6, you can see a situation where they are not in lockstep.

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BY MR. WARRICK:

Q. Would you call the memory device array of Halbert a single rank?

MR. CHANDLER: Objection. Form.

THE WITNESS: No. I think they receive separate control signals.

BY MR. WARRICK:

Q. And what's your basis for saying that?

A. They are selected based on -- well, let me check here.

No, actually, that happens elsewhere.

I do think in the way that I've defined "rank," those would be separate -- those would be a single rank. This particular patent has its own definition of "rank."

Q. Right. I should have clarified. I meant according to your proposed construction of "rank."

And so if I understand you correctly, you're saying you do think that the memory device array of Halbert Figure 4 is a "rank," according to your construction?

MR. CHANDLER: Objection. Form.

THE WITNESS: Yes.

BY MR. WARRICK:

Q. Now, if we look at the specification in

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Column 4, it indicates that each of the memory devices, which it calls "ranks 140 and 142," are each capable of performing m-bit-wide data transfers?

That's Column 4, around line 54.

A. Yes.

Q. And if you look a little bit further down, also describing Figure 4 in Column 4, around line 62, it describes [as read]: "An m-bit-wide path through buffer 122 that receives and drives data signals DQ on the system memory data bus."

So in view of those disclosures, am I correct that the Halbert Figure 4 has an m-bit-wide data path, but that the memory device array can return, effectively, 2 m data bits?

A. Yes.

MR. CHANDLER: Objection to form.

BY MR. WARRICK:

Q. So in view of your proposed construction, which requires memory devices, among other things, to act together in response to command signals to read or write the full bit width of the memory module, isn't the memory device array actually reading or writing double the full width -- bit width of the memory module?

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MR. CHANDLER: Objection to form.

THE WITNESS: It's still doing the full width of the memory module. I mean, we would still call it a "rank" because it's doing the full width of the memory module.

Again, the point there is to distinguish it from something that can't do the full width of the memory module.

BY MR. WARRICK:

Q. So a set of memory devices that -- that output something greater than the whole bit width of the memory module can still constitute a rank, in your view?

MR. CHANDLER: Objection. Form.

THE WITNESS: If it meets the other criteria and it's supplying the full width of the memory module, then I think it meets the construction.

BY MR. WARRICK:

Q. Going back to Figure 6, you mentioned that -- that they are not in lockstep in certain aspects of Figure 6.

Can you just identify for me which portions of Figure 6 you're relying on.

A. Yeah. I think I was a little bit off

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there. The data returned is returned to the host in two pieces out of step, but it does come out of the array in lockstep.

MR. WARRICK: Okay. All right. Could we take a brief break, just, say, five minutes.

(Short break taken.)

BY MR. WARRICK:

Q. All right. Dr. Wolfe, if we could go to your declaration -- and we could go to your declaration for the '417 patent, to paragraph 65.

Do you have that in front of you?

A. Yes.

Q. And this is in a portion of your declaration addressing the '087 provisional, which is one of the applications to which the '417 patent claims priority; correct?

A. Yes.

Q. Now, in paragraph 65 of your declaration, could you read the second sentence for me, please.

A. "For example, a Skilled Artisan would have understood that, for DDR SDRAM devices, a data transfer is preceded by a 'preamble' on the DQS stroke lines, and the data transfer through the buffer can be controlled in response to such preambles."

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Q. Thank you.

I'd like to ask you some questions about that.

Specifically, is it your view that the data transferred through the buffer could be controlled in response to such preambles?

A. I think it could. But I think a better way to say it would be -- "could be controlled to manage such preambles."

Q. I'm sorry. I'm not sure if I follow, Dr. Wolfe. You're saying that the -- maybe if you could just restate.

What I was trying to understand is whether the preambles could control the data transfer through the buffer.

A. I think they could, but I don't think that's what I was trying to say here.

I think what I was trying to say here is that there could be data buffer control signals to control the buffer during the time when those preambles are present.

Q. So I was just re-reading your answer, Dr. Wolfe, in an effort to understand.

You said, "I think what I was trying to say here is that there could be data buffer

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control signals to control the buffer during the time when those preambles are present."

So that is different than the preambles controlling the data transfer through the buffer; correct?

MR. CHANDLER: Objection. Form.

THE WITNESS: It is. As I said, I think the preambles could control it in some cases, but that wasn't what I was trying to say here.

I think what I was trying to say is the data transfer through the buffer can be controlled to respond to such preambles, not in response to such preambles. I think that would be clearer.

BY MR. WARRICK:

Q. Bear with me just a minute, if you would, please.

All right. Let's go back to Exhibit 1064, if we could, please, the JEDEC DDR2 standard.

A. Okay.

Q. And actually, before we do that, just to clarify. The same discussion about the '087 provisional is also contained in your declaration

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pertaining to the '215 patent; correct?

A. That's my recollection.

Q. Okay. And so your answers to these recent questions, would they apply equally to the discussion in your '215 patent declaration?

A. Yes.

Q. So turning to Exhibit 1064, I'd like to go specifically to page 26.

A. Okay.

Q. And on page 26, there is Figure 23.

Do you see that?

A. Yes.

Q. And I believe that Figure 23 was also referenced in that same paragraph of your declaration?

A. Yes.

Q. And --

A. And also Figure 29.

Q. Am I correct that Figure 23 in Exhibit 1064 shows the timing for data transfers that result from a read operation in DDR2?

A. Yes. But it should probably be read or viewed in conjunction with 25, 26, and 27, to understand some of the context.

Q. Are you referring to Figures 25, 26, and

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27?

A. Yes.

Q. Okay. So in Figure 23 of Exhibit 1064, the preamble that we were discussing earlier from your declaration, is the period while DQS is low prior to the first rising transition on DQS that accompanies the first piece of data, the burst; is that right?

A. Generally, yes, the rising edge of DQS slightly precedes the first piece of data; but that's generally correct.

Q. And in Figure 23, tRPRE indicates the duration of the preamble; yes?

A. Generally. We'd have to look at the definition to see if it's a minimum, maximum, or typical duration.

Q. And because Figure 23 illustrates read data timing, in Figure 23, CK, which is the differential clock, is an input to a DDR2 SDRAM, and DQS and DQ are outputs from the DDR2 SDRAM in response to a read command; correct?

MR. CHANDLER: Objection to form.

THE WITNESS: I think that's generally correct.

///

BY MR. WARRICK:

Q. And if we look specifically at the DQS signal trace in Figure 23, the SDRAM drives DQS to a low voltage during the preamble; and then after the preamble, the SDRAM alternates between driving the DQS signal line to a high voltage and to a low voltage, as the burst is output from the SDRAM; is that right?

A. Correct.

Q. And remaining with Figure 23, before the preamble, and after -- strike that.

In Figure 23, Dr. Wolfe, following the end of the burst, the diagram shows that the DQS signal trace is at an intermediate level.

Do you see that?

A. No. That's a misinterpretation.

Q. Okay. In what way?

A. That's to represent that in this particular case, where there -- where there is no immediate subsequent transaction, it would return to a -- I believe, to a high impedence level.

Q. Okay. So am I understanding correctly that when we see the DQS on the right side of Figure 23 represented by a flat line, that's representing a high impedence state?

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MR. CHANDLER: Objection. Form.

THE WITNESS: In this diagram, I believe that's correct.

BY MR. WARRICK:

Q. And when DQS is in that state, the SDRAM isn't driving it high or low. It's just not being driven at all; correct?

A. Not being driven by the SDRAM. It could be being driven by something else.

Q. Okay.

A. Including another SDRAM.

Q. So just to make sure I have this correct, in Figure 23, when we see DQS on the right side of the figure in what appears to be a flat line, it's not showing a voltage that's, for example, halfway between the VSS and VDD; it's not showing the voltages at half VDD; but only that the DQS output driver of the SDRAM is in a high impedant state.

Do I have that right?

A. Yes, I believe that's correct.

MR. WARRICK: All right, Dr. Wolfe. I don't believe I have any further questions for you at the moment.

Turn it over if Counsel has any redirect.

MR. CHANDLER: We'll go off the record.

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But before we do that, to be clear, I mean, this was a separate two days for both IPRs. And so you're finished with your direct for both IPRs now; you're turning over to me for any redirect on both IPRs; is that correct?

MR. WARRICK: That's correct.

MR. CHANDLER: Okay. Yeah. Why don't we go off the record; and maybe ten minutes. I'll check my notes.

MR. WARRICK: Okay.

(Short break taken.)

EXAMINATION

BY MR. CHANDLER:

Q. To start, I want to follow up on some questions at the beginning about the claim construction for rank. And there was a colloquy where -- the following question and answer, which I'll try to put in the chat. I'll also read it to you. But sometimes -- maybe I can't put it in the chat. That's fine. I'll read it to you slowly, and then I'll ask my question.

So this is just an earlier question and answer to refresh your recollection about the part of the testimony that I'm asking about.

So Netlist's counsel asked you:

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"So maybe we can try this differently. If a set of memory devices are on the memory module and they respond in approximately the same time to the same command signals, including chip select signals, to read or write the full bit width of the memory module, then that would fit your definition of a 'rank,' at least for purposes of these patents; correct?

"ANSWER: In an ordinary situation, it would be. If you're trying to describe something that's strange or unusual, I would have to see it to know.

"Again, these are -- these constructions are intended to be understood by a reasonable person who is familiar with the art."

So do you have that question and answer in mind for my follow-up question and answer?

A. Yes.

Q. So my question is simply, when you were asked if a set of memory devices fits your definition of "rank," where your definition of "rank" is one or more memory devices, were you trying to change your claim construction for rank?

MR. WARRICK: Objection. Form.

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THE WITNESS: No. You can have one thing in a set. But -- technically, you can have zero things in a set, but you can't have zero things that respond in the way the rest of that question said.

BY MR. CHANDLER:

Q. And at any point in response to the questions from Netlist's counsel, were you trying to change your construction for rank that appears in your expert declarations?

MR. WARRICK: Objection to form. Leading.

THE WITNESS: No. That -- that is the correct construction with respect to these patents.

BY MR. CHANDLER:

Q. Okay. I want to go to a different colloquy now, about Perego.

And, you know, to the extent it helps, I'll put the time stamp for the previous colloquy, which was -- it looks like it started at 9:00 a.m., 18 minutes and 32 seconds.

So I'll just put that in the record to help us try to find it later on.

Now I want to move to a different

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colloquy about Perego, where the time stamp, at least in the rough, is 11:00 a.m., 17 minutes and 9 seconds. And again, I'll read you the question and answer that I'm trying to follow up on, and then we'll ask my follow-up question.

So counsel for Netlist asked you [as read]:

"Question: Does Perego disclose selecting target subsets based on anything other than address bits?

"Answer: I don't recall it explicitly saying that, but it also doesn't in any way limit it to the address bits. And a person of ordinary skill, when looking at the JEDEC standard Exhibit 1064, would understand that you can select portions of memory or memory devices from a set using either address bits or bank address inputs.

"Bank address inputs are essentially simply extended address bits for many purposes."

Do you remember that question and answer?

A. Yes.

Q. So my follow-up question is, when performing rank multiplication with Perego, would that be performed only with address bits and with nothing else?

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MR. WARRICK: Objection. Form.

THE WITNESS: No. You still need to send the proper commands, and you still need to select the proper chips with the proper chip select values.

BY MR. CHANDLER:

Q. And so in Perego -- if you look at Column 15, line 37 to 40 -- and let me know when you have that in front of you.

A. I do.

Q. In Perego at Column 15, line 37 to 40, where there's a discussion of "...the target subset of secondary channel signal lines may be selected via address bits provided as part of the primary channel request," in that example, would it be only the address bits that would be used -- or would it be used in conjunction with something else? And in which case, what would the "something else" be?

MR. WARRICK: Objection. Form.

THE WITNESS: No. As I explained before, you can't use address bits to get some devices to respond and other devices not to respond. You have to use commands and chip selects to get that to happen.

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Otherwise, you would just get -- all the chips would respond; they would just respond from different addresses. And that would cause collisions and wouldn't perform rank multiplication in the way that's described in these examples.

BY MR. CHANDLER:

Q. Could you turn to the '215 and '417 patents, and --

A. One at a time.

Q. I have a question about both of them.

And maybe as a preliminary matter, is it correct that the figures and specifications of the '215 and '417 are substantially similar, if not identical?

A. As far as I can tell, yes.

Q. So my question is for both patents.

Do the '215 and '417 patents refer to FB-DIMMs?

A. They do. We talked about before that they show up in the IDS; but also in the text -- let's see. In the '215, I see it in Column 21, line 17. '417, I see it at Column 23, line 32.

Q. Do you believe that at the time of the '215 and '417 patents that FB-DIMMs were known to

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a person of ordinary skill in the art?

MR. WARRICK: Objection. Form. Leading.

THE WITNESS: I think they were.

BY MR. CHANDLER:

Q. Follow up on a different colloquy. Try to be precise. And actually -- so I'm going to follow up on some questions about Halbert. And it spans a few questions, so I won't give you a specific question to start with.

Could you pull up the Halbert reference? Let me know when you have it. I think it was --

A. 1078? I've got it.

Q. Yeah. I think 1078 was the version that Netlist's counsel was asking you questions about. I think there's also the Halbert publication that's an exhibit, which has the same disclosure, but we'll stick with 1078.

Let me know when you have it.

A. Yes.

Q. So in Column 4 of Exhibit 1078, starting at line 57, do you see Halbert teaches that, "Generally, multiple ranks will receive the same address and commands, and will perform memory operations with the interface circuit concurrently"?

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A. I see that.

Q. In your opinion, is Halbert limited in its teachings to only that specific example, where multiple ranks receive -- receive the same address and commands and perform memory operations with the interface circuit concurrently?

MR. WARRICK: Objection. Form. Leading.

THE WITNESS: I don't think so. I think that's why I was a little bit confused before. I think that memory device array can be a single rank when it does receive the same address and commands.

But Halbert seems to explain that not all embodiments do that. And if they receive different commands and different -- in particular, then they would be two ranks.

BY MR. CHANDLER:

Q. Would you turn to your '417 expert declaration marked as Exhibit 1003 and go to page 149. And let me know when you're there.

A. I am there.

Q. And just to make it simpler, can you also at the same time pull up your other expert declaration from the '215 IPR marked as Exhibit 1003 and go to page 152 of that expert

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declaration.

A. Okay.

Q. And do you see on page 149 of Exhibit 1003 in the '417 IPR and also page 152 of Exhibit 1003 of the '215 IPR you have an annotated version of Figure 4 of Halbert that shows Rank 140 in green and Rank 142 in blue?

A. Yes.

Q. For clarity, can Rank 140 in Halbert and Rank 142 in Halbert, in at least some embodiments, be two separate ranks?

MR. WARRICK: Objection. Form. Leading.

THE WITNESS: Yes. That's what I was indicating in these sections of the report.

MR. CHANDLER: Okay. Nothing further from me.

And as a reminder, we would like the final by Friday, November 10, and the opportunity to review and make any corrections.

MR. WARRICK: Okay. If we could get the final by the 10th, as well, that would be good.

(TIME 4:21 p.m.)

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DECLARATION UNDER PENALTY OF PERJURY

I, DR. ANDREW WOLFE, do hereby certify under penalty of perjury that I have read the foregoing transcript of my deposition taken on NOVEMBER 5, 2023; that I have made such corrections as appear noted herein; that my testimony as contained herein, as corrected, is true and correct.

DATED this day of , 2023, at .

_____

DR. ANDREW WOLFE

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STATE OF CALIFORNIA)
(ss.
COUNTY OF LOS ANGELES)

I, RENEE HARRIS, do hereby certify that I am a licensed Certified Shorthand Reporter, duly qualified and certified as such by the State of California;

That prior to being examined, the witness named in the foregoing deposition was by me duly sworn to testify to tell the truth, the whole truth, and nothing but the truth;

That the said deposition was by me recorded stenographically;

And the foregoing pages constitute a full, true, complete and correct record of the testimony given by the said witness;

That I am a disinterested person, not being in any way interested in the outcome of said action, or connected with, nor related to any of the parties in said action, or to their respective counsel, in any manner whatsoever.

DATED: 11/10/2023

Renee Harris, CSR, CCR, RPR
CA CSR No. 14168,
NJ CRR No. 30XI00241200

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THEODORE W. CHANDLER, ESQ.
ted.chandler@bakerbotts.com

November 10, 2023

RE: SAMSUNG ELECTRONICS CO. vs. NETLIST, INC.
November 5, 2023, DR. ANDREW WOLFE, JOB NO. 6294218
The above-referenced transcript has been
completed by Veritext Legal Solutions and
review of the transcript is being handled as follows:

__ Per CA State Code (CCP 2025.520 (a)-(e)) – Contact Veritext to schedule a time to review the original transcript at a Veritext office.

__ Per CA State Code (CCP 2025.520 (a)-(e)) – Locked .PDF Transcript - The witness should review the transcript and make any necessary corrections on the errata pages included below, notating the page and line number of the corrections. The witness should then sign and date the errata and penalty of perjury pages and return the completed pages to all appearing counsel within the period of time determined at the deposition or provided by the Code of Civil Procedure.

__ Waiving the CA Code of Civil Procedure per Stipulation of Counsel - Original transcript to be released for signature as determined at the deposition.

__ Signature Waived – Reading & Signature was waived at the time of the deposition.

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_X_ Federal R&S Requested (FRCP 30(e)(1)(B)) – Locked .PDF Transcript - The witness should review the transcript and make any necessary corrections on the errata pages included below, notating the page and line number of the corrections. The witness should then sign and date the errata and penalty of perjury pages and return the completed pages to all appearing counsel within the period of time determined at the deposition or provided by the Federal Rules.

__ Federal R&S Not Requested - Reading & Signature was not requested before the completion of the deposition.

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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.,

Petitioner,

v.

NETLIST, INC.,

Patent Owner.

IPR2023-00454
Patent 11,093,417

ERRATA TO THE DEPOSITION OF ANDREW WOLFE (NOVEMBER 4, 2023)

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.,

Petitioner,

v.

NETLIST, INC.,

Patent Owner.

IPR2023-00455
Patent 9,858,215

ERRATA TO THE DEPOSITION OF ANDREW WOLFE (NOVEMBER 4, 2023)

I, ANDREW WOLFE, have read the transcript of my deposition taken on November 4, 2023. Listed below are changes to the transcript that I wish to make and the reasons for making them:

Page:Line	**Now Reads**	**Should Read**	**Reason for Change**
1:24 2:19 5:2	November 5, 2023	November 4, 2023	My deposition was on Saturday, November 4, 2023, not November 5th.
2:12–:13	Case No. IPR2020-01624 Patent No. 6,975,132	Case No. IPR2023-00454 Patent No. 11,093,417 - and - Case No. IPR2023-00455 Patent No. 9,858,215	Typographical error. *See* 1:12–:16.

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Page:Line	**Now Reads**	**Should Read**	**Reason for Change**
15:18–16:6	Q. If a set of memory devices are on the memory module and they respond in approximately the same time to the same command signals, including chip select signals, to read or write the full bit width of the memory module, then that would fit your definition of a "rank," at least for purposes of these patents; correct? A. In an ordinary situation, it would be. If you're trying to describe something that's strange or unusual, I would have to see it to -- to know. Again, these are -- these constructions are intended to be understood by a reasonable person who is familiar with the art.	[see note]	No change, but this was further clarified at 174:20–175:15.
29:16–:19	I would say that <u>configureable</u> bit widths are a feature of his invention but not a required feature of his disclosure.	I would say that <u>configurable</u> bit widths are a feature of his invention but not a required feature of his disclosure.	Typographical error

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Page:Line	**Now Reads**	**Should Read**	**Reason for Change**
32:9–:13	Q. And you've said earlier that Perego allows you to configure the ranks; correct? MR. CHANDLER: Object to form. THE WITNESS: That is a feature of some of his embodiments.	[see note]	This was clarified in the next question and answer. *See* 32:15–:22 ("It's the interface that it is configurable width. I don't think I've considered whether or not the ranks can be configured….").
32:19–:20	It's the interface that it is configurable <u>with</u>.	It's the interface that it is configurable <u>width</u>.	Typographical error
41:10–:12	Perego, in that context, illustrates a set of <u>input sig- --</u> and output signals to a memory device	Perego, in that context, illustrates a set of <u>input signals</u> and output signals to a memory device	Typographical error

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42:15–47:25	Q. But the example depicted in Figure 4B of Perego is showing a Rambus-style memory architecture if you interpret it literally; correct? MR. CHANDLER: Objection. Form. THE WITNESS: If you interpret it literally, it is illustrating the Rambus signal names.... …. Q...From your explanation, Figure 4B is depicting a well-known Rambus-style interface between the buffer and the memory devices; yes? A. That Figure 4B literally illustrates a well-known Rambus-style interface between the buffer and the memory devices. And Perego elsewhere explains that other memory interfaces can be used instead. Q. And if you were to use DDR2 memory devices in Figure 4B of Perego, you would	[see note]	No change, but this was further clarified at 48:4-49:23, 133:3–:21, 134:22–135:8, 135:23–136:5, 138:10–140:20, 146:24–147:5.

Page:Line	Now Reads	Should Read	Reason for Change
	also have to change the interconnects between those devices and the buffer; correct? MR. CHANDLER: Objection. Form. THE WITNESS: You would replace the well-known Rambus interface with the well-known DDR2 interface. Q. And isn't it correct you would also have to make changes to the design of the buffer in Figure 4B of Perego if you substituted DDR2 memory devices? A. Correct. You would -- you would take aspects of the buffer that were designed to be compliant with the public Rambus standard, and you would change them to be compliant with the public DDR2 standard.		
48:18	column address <u>stroke</u>	column address <u>strobe</u>	Typographical error

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Page:Line	Now Reads	Should Read	Reason for Change
50:25–51:4	I wouldn't say that it's not possible to have a configureable memory module, but once the module's been figured, the full bit width, I think, is a -- is established.	I wouldn't say that it's not possible to have a configurable memory module, but once the module's been configured, the full bit width, I think, is a -- is established.	Typographical errors
53:18–:21	And that's the only embodiment that one needs to understand that the asserted claims are obvious -- or the challenged claims are obvious.	And that's the only embodiment that one needs, to understand that the asserted claims are obvious -- or the challenged claims are obvious.	Typographical error
62:18–:21	It's literally what's shown in the example. But again, the content -- the patent itself tells you that that's not a limitation of Figure 4B.	It's literally what's shown in the example. But again, the context -- the patent itself tells you that that's not a limitation of Figure 4B.	Typographical error
68:19–:20	I would use 8-by-8 chips in each rank to provide a 64-bit response.	I would use eight x8 chips in each rank to provide a 64-bit response.	Typographical error
69:3–:6	If I were using by-8 chips, I would put 16 in each rank to get 128-bit host interface, or I would use 8-by-16 chips if I wanted each rank to provide 128 bits to 128-bit interface.	If I were using x8 chips, I would put 16 in each rank to get 128-bit host interface, or I would use eight x16 chips if I wanted each rank to provide 128 bits to 128-bit interface.	Typographical errors

Page:Line	**Now Reads**	**Should Read**	**Reason for Change**
76:24–78:1	Q. And in the example of Perego, the buffer will select the target subset channels based on address bits; is that right? . . . . A. I think it can select based on address bits. . . . . Q. Does Perego disclose selecting target subsets based on anything other than address bits? A. I don't recall it explicitly saying that, but it also doesn't in any way limit it to the address bits.	[see note]	No change, but this was further clarified at 160:16–161:14, 176:22–178:6.
79:7–:11	If you want to access a row across a group of memory devices, the same row needs to be activated in each memory device that you're going to access using the <u>signal</u> read or write command.	If you want to access a row across a group of memory devices, the same row needs to be activated in each memory device that you're going to access using the <u>single</u> read or write command.	Typographical error

Page:Line	**Now Reads**	**Should Read**	**Reason for Change**
80:7–:10	In other embodiments, he talks about a one-to-one serialization ratio and he talks about determining the configuration and manufacturing time.	In other embodiments, he talks about a one-to-one serialization ratio and he talks about determining the configuration at manufacturing time.	Typographical error
81:11–:14	I think this is supportive of a two-rank configuration of Figure 4B in which channels 4c and 4d are accessed together and 4a and 4b are waiting for the next access.	I think this is supportive of a two-rank configuration of Figure 4B in which channels 415c and 415d are accessed together and 415a and 415b are waiting for the next access.	Misspoke. *See* 80:16–81:1.
95:21–:24	So to avoid confusion between it being there and it not being there, we talked about it being asserted when it's there, even if that's a zero voltage.	So to avoid confusion between it being there and it not being there, we talk about it being asserted when it's there, even if that's a zero voltage.	Typographical error

Page:Line	Now Reads	Should Read	Reason for Change
100:9–:13	So if there is a delay -- a time delay between the memory device response and the memory module response, then the CAS latency of the module will be greater than the amount of that delay in the CAS latency of the device.	So if there is a delay -- a time delay between the memory device response and the memory module response, then the CAS latency of the module will be greater by the amount of that delay in the CAS latency of the device.	Typographical error
102:25–:10	Q….Dr. Wolfe, Perego does not expressly disclose registering the data output as distinct from using latches; correct? MR. CHANDLER: Object to form. THE WITNESS: Not explicitly. But what it does describe is generating clocks, clock alignment, to use the latches in a way so there is still a delay in the way that there wouldn't be with a register. And that's why it would be obvious to a person of ordinary skill to use a register, as well.	Q….Dr. Wolfe, Perego does not expressly disclose registering the data output as distinct from using latches; correct? MR. CHANDLER: Object to form. THE WITNESS: Not explicitly. But what it does describe is generating clocks, clock alignment, to use the latches in a way so there is still a delay in the way that there would be with a register. And that's why it would be obvious to a person of ordinary skill to use a register, as well.	Typographical error

Page:Line	Now Reads	Should Read	Reason for Change
107:25–108:10	Q. Now, earlier, another concept you referenced from one of your answers was a fully buffered DIMM? A. Yes. Q. Did those exist at the time of the priority date for the '417 patent? MR. CHANDLER: Objection. Form. THE WITNESS: I don't know. I'm familiar with the specification being published in 2006, but I don't know when they were first known in the industry.	[see note]	No change, but this was further clarified at 178:17–179:3.
113:2–:5	it refers to the CAS latency of a memory device independently of whether or not it's been used <u>an</u> a memory module or any particular type of module	it refers to the CAS latency of a memory device independently of whether or not it's been used <u>in</u> a memory module or any particular type of module	Typographical error
118:11–:12	Exhibit 1062 is the registered DIMM specification for <u>DDR not DDR2 memories</u>.	Exhibit 1062 is the registered DIMM specification for <u>DDR, not DDR2, memories</u>.	Typographical error

Page:Line	Now Reads	Should Read	Reason for Change
121:3–:5	not every system needs to set the cache latency for particular devices the same way	not every system needs to set the CAS latency for particular devices the same way	Typographical error
131:24–132:7	Q. And we discussed earlier that in Perego, if you were to use JEDEC-compliant DDR2 memory devices, you would, in fact, have to modify other parts of the memory module to make it work; correct? MR. CHANDLER: Object to form. THE WITNESS: Yes. You would need to make modifications at the detail level that are routine within the industry.	[see note]	No change, but this was further clarified at 133:3–134:8.
138:3–:4	there's 800 pages in the report	there's 800 pages in the reports	Typographical error
143:17	RQ scroll lines	RQ control lines	Typographical error
157:24–:25	And that's what's important, if it says, "one or more DRAM devices."	And that's what's important, is it says, "one or more DRAM devices."	Typographical error

Page:Line	**Now Reads**	**Should Read**	**Reason for Change**
160:16–:24	Q....Sticking with Perego, though, I think we covered earlier that Perego teaches using address signals to select specific signal lines for responding to a read or write command; is that right? MR. CHANDLER: Objection. Form. THE WITNESS: It does describe that with respect to the specific embodiments, yes, person of -- but it's permissive.	[see note]	No change, but this was further clarified at 161:9–:14, 176:22–178:6.
163:18–:23	Q....And so if I understand you correctly, you're saying you do think that the memory device array of Halbert Figure 4 is a "rank," according to your construction? MR. CHANDLER: Objection. Form. THE WITNESS: Yes.	[see note]	No change, but this was further clarified at 179:20–181:14.
166:23	DQS <u>stroke</u> lines	DQS <u>strobe</u> lines	Typographical error

Page:Line	**Now Reads**	**Should Read**	**Reason for Change**
172:18	high impedant state	high impedance state	Typographical error

I hereby certify that the transcript of my deposition on November 4, 2023, as corrected above, is a true and accurate transcription of my testimony.

I, Andrew Wolfe, do hereby declare and state, that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, under Section 1001 of Title 18 of the United States Code.

Executed on: December 5, 2023

Andrew Wolfe

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