

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.,

Petitioner,

v.

NETLIST, INC.,

Patent Owner

IPR2023-00455

Patent 9,858,215 B1

**PETITIONER'S REPLY
TO PATENT OWNER'S RESPONSE**

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TABLE OF AUTHORITIES

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 Cases	
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<i>CareFusion Corp. v. Baxter Int’l Inc.</i> , IPR2016-01463, Paper 40 (PTAB June 13, 2018)	2
<i>Continental Auto. Sys., Inc. v. Intellectual Ventures II LLC</i> , IPR2022-00972, Paper 49 (PTAB Dec. 5, 2023)	22
<i>Dynamic Drinkware, LLC v. National Graphics, Inc.</i> , 800 F.3d 1375 (Fed. Cir. 2021)	22
<i>DyStar Textilfarben GmbH v. C.H. Patrick Co.</i> , 464 F.3d 1356 (Fed. Cir. 2006)	4
<i>Ecolochem, Inc. v. S. Cal. Edison Co.</i> , 227 F.3d 1361 (Fed. Cir. 2000)	30
<i>Gen. Hosp. Corp. v. Sienna Biopharms., Inc.</i> , 888 F.3d 1368 (Fed. Cir. 2018)	12
<i>Geo. M. Martin Co. v. Alliance Machine Sys. Int’l LLC</i> , 618 F.3d 1294 (Fed. Cir. 2010)	30
<i>Homeland Housewares, LLC v. Whirlpool Corp.</i> , 865 F.3d 1372 (Fed. Cir. 2017)	2
<i>Intel Corp. v. PACT XPP Schweiz AG</i> , 61 F.4th 1373 (Fed. Cir. 2023)	13, 17
<i>Intelligent Bio-Sys., Inc. v. Illumina Cambridge Ltd.</i> , 821 F.3d 1359 (Fed. Cir. 2016)	14
<i>Iron Grip Barbell Co. v. USA Sports, Inc.</i> , 392 F.3d 1317 (Fed. Cir. 2004)	12

<i>Koninklijke Philips N.V. v. Google LLC</i> , 948 F.3d 1330 (Fed. Cir. 2020)	13, 14
<i>Lockwood v. Am. Airlines, Inc.</i> , 107 F.3d 1565 (Fed. Cir. 1997)	27
<i>Qualcomm Inc. v. Apple Inc.</i> , 24 F.4th 1367 (Fed. Cir. 2022)	21
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<i>Rambus Inc. v. Infineon Techs. AG</i> , 318 F.3d 1081 (Fed. Cir. 2003)	10
<i>Rivera v. ITC</i> , 857 F.3d 1315 (Fed. Cir. 2017)	23
<i>Univ. of Md. Biotech. Inst. v. Presens Precision Sensing GmbH</i> , 711 F. App'x 1007 (Fed. Cir. 2017)	15
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35 U.S.C. § 120	23
35 U.S.C. § 301	21, 22
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EXHIBIT LIST

Exhibit #	Description
1001	U.S. Patent No. 9,858,215 (issued January 2, 2018)
1002	File History of U.S. Patent No. 9,858,215 (filed May 18, 2015)
1003	Declaration of Dr. Andrew Wolfe
1004	Curriculum Vitae of Dr. Andrew Wolfe
1005	U.S. Provisional Application No. 60/645,087 (filed Jan. 19, 2005)
1006	U.S. Provisional Application No. 60/588,244 (filed July 15, 2004)
1007	U.S. Provisional Application No. 60/550,668 (filed March 5, 2004)
1008	U.S. Provisional Application No. 60/575,595 (filed May 28, 2004)
1009	U.S. Provisional Application No. 60/590,038 (filed July 21, 2004)
1010	File History of U.S. Patent No. 7,286,436 (filed March 7, 2005)
1011	U.S. Patent No. 7,286,436 (issued Oct. 23, 2007)
1012	U.S. Patent No. 7,289,386 (issued Oct. 30, 2007)
1013	Affirmance of the Examiner's Decision on Reexamination of '386 Patent (Feb. 25, 2015)
1014	Reexamination Certificate for '386 Patent (Aug. 19, 2016)
1015	U.S. Patent No. 7,619,912 (issued Nov. 17, 2009)
1016	Decision on Reexamination of '912 Patent (June 6, 2016); Decision Under 37 C.F.R. § 41.77(f) (July 27, 2018); and Decision on Rehearing (Jan. 31, 2019)
1017	Reexamination Certificate for '912 Patent (Feb. 8, 2021)
1018	Petition for <i>Inter Partes</i> Review of U.S. Patent No. 7,619,912 (Feb. 17, 2022)

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1019	Patent Owner Preliminary Response to Petition for <i>Inter Partes</i> Review of U.S. Patent No. 7,619,912 (July 21, 2022)
1020	Declaration of Michael C. Brogioli, Ph.D. in Support of Patent Owner Preliminary Response to Petition for <i>Inter Partes</i> Review of U.S. Patent No. 7,619,912 (July 21, 2022)
1021	Reply to Patent Owner Preliminary Response to Petition for <i>Inter Partes</i> Review of U.S. Patent No. 7,619,912 (Aug. 26, 2022)
1022	Sur-Reply to Patent Owner Preliminary Response to Petition for <i>Inter Partes</i> Review of U.S. Patent No. 7,619,912 (Sept. 9, 2022)
1023	Decision Granting Institution of <i>Inter Partes</i> Review of U.S. Patent No. 7,619,912 (Oct. 19, 2022)
1024	Patent Owner's Request for Rehearing of Decision Granting Institution of <i>Inter Partes</i> Review of U.S. Patent No. 7,619,912 (Nov. 2, 2022)
1025	Order of <i>Sua Sponte</i> Director Review of Decision Granting Institution of <i>Inter Partes</i> Review of U.S. Patent No. 7,619,912 (Jan. 5, 2023)
1026	U.S. Patent No. 7,864,627 (issued Jan. 4, 2011)
1027	Decision on Appeal of Reexamination of '627 Patent (May 30, 2016); Decision Under 37 C.F.R. § 41.77(f) (May 31, 2018)
1028	Reexamination Certificate for '627 Patent (Nov. 5, 2018)
1029	U.S. Patent No. 8,756,364 (issued June 17, 2014)
1030	IPR2017-00549 Final Written Decision ('364 Patent) (May 3, 2018)
1031	IPR Certificate for '364 Patent (May 26, 2020)
1032	U.S. Patent No. 7,532,537 (issued May 12, 2009)
1033	IPR2017-00667 Final Written Decision ('537 Patent) (July 18, 2018)

Exhibit #	Description
1034	IPR2017-00668 Final Written Decision (’537 Patent) (July 18, 2018)
1035	IPR Certificate for ’537 Patent (Apr. 27, 2020)
1036	U.S. Patent No. 7,636,274 (issued Dec. 22, 2009)
1037	Decision on Appeal of Reexamination of ’274 Patent (May 9, 2017)
1038	Reexamination Certificate for ’274 Patent (Nov. 5, 2018)
1039	U.S. Patent No. 7,881,150 (issued Feb. 1, 2011)
1040	IPR2014-00882 Final Written Decision on Remand (’150 Patent) (March 29, 2018)
1041	IPR2014-01011 Final Written Decision on Remand (’150 Patent) (March 29, 2018)
1042	IPR2015-01020 Final Written Decision (’150 Patent) (Sept. 28, 2016)
1043	IPR Certificate for ’150 Patent (Mar. 6, 2019)
1044	File History of U.S. Patent No. 7,916,574 (filed Nov. 29, 2010)
1045	U.S. Patent No. 7,916,574 (issued Mar. 29, 2011)
1046	U.S. Patent No. 8,081,536 (issued Dec. 20, 2011)
1047	IPR2014-00883 Final Written Decision on Remand (’536 Patent) (March 29, 2018)
1048	IPR2015-01021 Final Written Decision (’536 Patent) (Sept. 28, 2016)
1049	IPR Certificate for ’536 Patent (Mar. 11, 2019)
1050	File History of U.S. Patent No. 8,516,188 (filed Nov. 1, 2011)
1051	U.S. Patent No. 8,516,188 (issued Aug. 20, 2013)

Exhibit #	Description
1052	File History of U.S. Patent No. 9,037,774 (filed Aug. 20, 2013)
1053	U.S. Patent No. 9,037,774 (issued May 19, 2015)
1054	File History of U.S. Patent No. 10,489,314 (filed Dec. 28, 2017)
1055	U.S. Patent No. 10,489,314 (issued Nov. 26, 2019)
1056	Decisions Granting Institution of <i>Inter Partes</i> Reviews of U.S. Patent No. 10,489,314 (Nov. 1, 2022)
1057	File History of U.S. Patent No. 11,093,417 (filed Nov. 25, 2019)
1058	U.S. Patent No. 11,093,417 (issued Aug. 17, 2021)
1059	File History of U.S. Patent Application No. 17/403,832 (filed Aug. 16, 2021)
1060	JEDEC JESD79 standard for DDR SDRAM (June 2000)
1061	[intentionally omitted]
1062	JEDEC JESD21-C design specification for DDR SDRAM Registered DIMM (January 2002)
1063	[intentionally omitted]
1064	JEDEC JESD79-2 standard for DDR2 SDRAM (Sept. 2003)
1065	Declaration of Julie Carlson (JESD79-2)
1066	JEDEC JESD21-C design specification for DDR2 SDRAM Registered DIMM, Rev. 3.2 (Oct. 4, 2005)
1067	[intentionally omitted]
1068	Harold S. Stone, <u>Microcomputer Interfacing</u> (1982)
1069	Bruce Jacob, <i>Synchronous DRAM Architectures, Organizations, and Alternative Technologies</i> (Dec. 10, 2002)

Exhibit #	Description
1070	Bruce Jacob et al., <u>Memory Systems: Cache, DRAM, Disk</u> (2008)
1071	U.S. Patent No. 7,363,422 to <u>Perego</u> et al. (filed Jan. 28, 2004)
1072	U.S. Patent No. 7,155,627 to <u>Matsui</u> (filed Aug. 22, 2003)
1073	U.S. Patent Application Publication No. 2006/0277355 to <u>Ellsberry</u> et al. (filed June 1, 2005)
1074	IPR2018-00362 Final Written Decision (June 27, 2019) ('907 Patent)
1075	U.S. Patent No. 9,606,907 (all claims cancelled)
1076	Decision Granting Institution of <i>Inter Partes</i> Review of U.S. Patent No. 10,949,339 (Oct. 19, 2022) (child of U.S. Patent No. 9,606,907, Exhibit 1075)
1077	U.S. Patent Application Publication No. 2002/0112119 to <u>Halbert</u> et al. (published Aug. 15, 2002)
1078	U.S. Patent No. 7,024,518 to <u>Halbert</u> et al. (filed Mar. 13, 2002)
1079	U.S. Patent Application Publication No. 2006/0117152 to <u>Amidi</u> et al. (filed Jan. 5, 2004)
1080	U.S. Patent No. 8,250,295 to <u>Amidi</u> et al. (filed Jan. 5, 2004)
1081	U.S. Patent. No. 5,513,135 to <u>Dell</u> et al. (issued Apr. 30, 1996)
1082	U.S. Patent Application Publication No. 2003/0039151 to <u>Matsui</u> (published Feb. 27, 2003)
1083	[intentionally omitted]
1084	[intentionally omitted]
1085	Amended Complaint in <i>Netlist, Inc. v. Samsung Electronics Co., Ltd. et al.</i> , No. 2:22-cv-00293 (E.D. Tex. filed Aug. 15, 2022)
1086	Waiver of Service in <i>Netlist, Inc. v. Samsung Electronics Co., Ltd. et al.</i> , No. 2:22-cv-00293 (E.D. Tex. filed Aug. 31, 2022)

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1087	[intentionally omitted]
1088	Amended Complaint in <i>Netlist, Inc. v. Micron Technology, Inc. et al.</i> , No. 2:22-cv-00294 (E.D. Tex. filed Aug. 15, 2022)
1089	Micron’s Answer in <i>Netlist, Inc. v. Micron Technology, Inc. et al.</i> , No. 2:22-cv-00294 (E.D. Tex. filed Sept. 7, 2022)
1090	[intentionally omitted]
1091	<i>Interim Procedure for Discretionary Denials in AIA Post-Grant Proceedings with Parallel District Court Litigation</i> (June 21, 2022)
1092	Federal Court Management Statistics (Mar. 31, 2022), available at https://www.uscourts.gov/statistics/table/na/federal-court-management-statistics/2022/03/31-1
1093	Email from counsel for Samsung to counsel for Patent Owner re: stipulation not to pursue certain invalidity defenses if an IPR proceeding is instituted
1094	U.S. Patent & Trademark Office, <i>Changes Under Consideration to Discretionary Institution Practices, Petition Word-Count Limits, and Settlement Practices for America Invents Act Trial Proceedings Before the Patent Trial and Appeal Board</i> , 88 Fed. Reg. 24,503 (Apr. 21, 2023)
1095 [NEW]	Transcript of deposition of Steven Przybylski (Feb. 15–16, 2024)
1096 [NEW]	Redline comparing Steven Przybylski’s declaration in IPR2023-00454 (EX2024) to his declaration in IPR2023-00455 (EX2024)
1097 [NEW]	Excerpts from Przybylski, Steven A., “NEW DRAM TECHNOLOGIES, A Comprehensive Analysis of the New Architectures,” Second Edition, ©1996
1098 [NEW]	Final Written Decision, <i>Samsung Electronics Co., Ltd. v. Lynk Labs, Inc.</i> , IPR2022-00149, Paper 33 (PTAB June 26, 2023), <i>appeal docketed</i> , No. 23-2346 (Fed. Cir. Aug. 31, 2023)

Exhibit #	Description
1099 [NEW]	Final Written Decision, <i>Patent Quality Assurance, LLC v. VLSI Tech. LLC</i> , IPR2021-01229, Paper 129 (June 13, 2023)
1100	[intentionally omitted]
1101 [NEW]	Transcript of deposition of Michael C. Brogioli, Ph.D. (Oct. 3, 2023) [Samsung's EX1101 in IPR2022-00615]
1102 [NEW]	Declaration of Michael C. Brogioli, Ph.D. [Netlist's EX2062 in IPR2022-00615]
1103 [NEW]	Netlist's Technology Tutorial
1104 [NEW]	JEDEC JESD79D standard for DDR SDRAM (January 2004), < http://web.archive.org/web/20040611184458/http://www.jedec.org/DOWNLOAD/search/JESD79D.pdf >
1105	[intentionally omitted]
1106	[intentionally omitted]
1107 [NEW]	Final Written Decision, <i>Samsung Electronics Co., Ltd. v. Netlist, Inc.</i> , IPR2022-00639, Paper 45 (PTAB Oct. 18, 2023)
1108 [NEW]	Decision Denying Patent Owner's Request on Rehearing of Final Written Decision, <i>Samsung Electronics Co., Ltd. v. Netlist, Inc.</i> , IPR2022-00639, Paper 48 (PTAB Feb. 9, 2024)
1109 [NEW]	Micron, 256MB, 512MB, 1GB (x72, ECC, SR) 240-Pin DDR2 SDRAM RDIMM Features (2003) [Netlist's EX2057 in IPR2022-00615]
1110	[intentionally omitted]
1111	[intentionally omitted]
1112	[intentionally omitted]

Exhibit #	Description
1113 [NEW]	U.S. Patent No. 7,002,378 to Srikanth et al.

CLAIM LISTING

Ref. #	Listing of Challenged Claims
1.a.1	1. A memory module
1.a.2	operable in a computer system to communicate data with a memory controller of the computer system via a memory bus in response to memory commands received from the memory controller,
1.a.3	the memory commands including a first memory command and a subsequent second memory command, the first memory command to cause the memory module to receive or output a first data burst and the second memory command to cause the memory module to receive or output a second data burst,
1.a.4	the memory module comprising:
1.b	a printed circuit board having a plurality of edge connections configured to be electrically coupled to a corresponding plurality of contacts of a module slot of the computer system;
1.c	a register coupled to the printed circuit board and configured to receive and buffer first command and address signals representing the first memory command, and to receive and buffer second command and address signals representing the second memory command;
1.d.1	a plurality of memory integrated circuits mounted on the printed circuit board and arranged in a plurality of ranks including a first rank and a second rank, the plurality of memory integrated circuits including at least one first memory integrated circuit in the first rank and at least one second memory integrated circuit in the second rank,
1.d.2	wherein the first rank is selected to receive or output the first data burst in response to the first memory command and is not selected to communicate data with the memory controller in response to the second memory command, and
1.d.3	wherein the second rank is selected to receive or output the second data burst in response to the second memory command and is not selected to communicate data with the memory controller in response to the first memory command;
1.e	a buffer coupled between the at least one first memory integrated circuit and the memory bus, and between the at least one second memory integrated circuit and the memory bus; and

Ref. #	Listing of Challenged Claims
1.f.1	logic coupled to the buffer and configured to respond to the first memory command by providing first control signals to the buffer to enable communication of the first data bust between the at least one first memory integrated circuit and the memory controller through the buffer,
1.f.2	wherein the logic is further configured to respond to the second memory command by providing second control signals to the buffer to enable communication of the second data burst between the at least one second memory integrated circuit and the memory controller through the buffer, the second control signals being different from the first control signals.
2	The memory module of claim 1, wherein the buffer is configured to isolate both the at least one first memory integrated circuit and the at least one second memory integrated circuit from the memory bus when the memory module is not being accessed by the memory controller.
3	The memory module of claim 1, wherein the memory module has an overall CAS latency greater than an actual operational CAS latency of each of the plurality of memory integrated circuits.
4	The memory module of claim 1, further comprising an SPD device that reports an overall CAS latency of the memory module to the memory controller, the overall CAS latency having one more clock cycle than an actual operational CAS latency of each of the plurality of memory integrated circuits.
5	The memory module of claim 1, wherein the memory module is a dual in-line memory module (DIMM), and wherein the plurality of memory integrated circuits are double-data-rate dynamic random access memory (DRAM) circuits.
6	The memory module of claim 1, further comprising determining a latency value, wherein the communication of the first data burst between the at least one first memory integrated circuit and the memory controller is enabled in accordance with the latency value.

Ref. #	Listing of Challenged Claims
7	The memory module of claim 1, wherein the memory module is further coupled to the memory controller using an on-die-termination (ODT) bus, wherein each of the plurality of memory devices includes an ODT circuit, the memory module further comprising a termination circuit external to any of the plurality of memory devices, wherein the termination circuit is coupled to the ODT bus and to the ODT circuit of at least one of the plurality of memory devices, wherein the termination circuit is configured to provide external termination of the at least one of the plurality of memory devices in response to an ODT signal on the ODT bus, and wherein the ODT circuit in the at least one of the plurality of memory devices is disabled.
8	The memory module of claim 1, wherein the buffer comprises combinatorial logic, registers, and logic pipelines, and is configured to register an additional clock cycle for transferring the first data burst or the second data burst through the buffer.
9	The memory module of claim 1, wherein the first memory command includes at least one first chip select signal and the second memory command includes at least one second chip select signal.
10	The memory module of claim 9, wherein the memory module produces at least third and fourth chip select signals in response to the first memory command, the third chip select signal being provided to the at least one first memory integrated circuit and having an active value to cause the at least one first memory integrated circuit to receive or output data signals in response to the first memory command, the fourth chip-select signal being provided to the at least one second memory integrated circuit and having a non-active value to keep the at least one second memory integrated circuit from receiving or outputting data signals in response to the first memory command.

Ref. #	Listing of Challenged Claims
11	The memory module of claim 10, wherein the memory module produces at least fifth and sixth chip select signals in response to the second memory command, the fifth chip select signal being provided to the at least one first memory integrated circuit and having a non-active value to keep the at least one first memory integrated circuit from receiving or outputting data signals in response to the first [sic: second] memory command, the sixth chip select signal being provided to the at least one second memory integrated circuit and having an active value to cause the at least one second memory integrated circuit to receive or output data signals in response to the second memory command.
12	The memory module of claim 1, wherein the first memory command is a first read command and the second memory command is a second read command, wherein the first read command and the second read command are back to back adjacent read commands, and wherein the memory module outputs the first data burst together with a first burst of data strobe signals in response to the first read command, wherein memory module outputs the second data burst together with a second burst of data strobe signals in response to the second read command, wherein the second data burst follows the first data burst on the memory bus, and wherein the buffer is configured to prevent the first burst of data strobe signals and the second burst of data strobe signals from colliding with each other.
13	The memory module of claim 12, wherein each of the first burst of data strobe signals and the second burst of data strobe signals includes a pre-amble interval and a post-amble interval, and wherein the buffer is configured to combine the first burst of data strobe signals into a combined burst of data strobe signals that does not include the post-amble interval of the first burst of data strobe signals and the pre-amble interval of the second burst of data strobe signals.
14	The memory module of claim 1, wherein the buffer includes circuit components configurable to provide a first data path or a second data path depending on whether the first rank or the second rank is selected to communicate data with the memory controller.
15	The memory module of claim 14, the at least one of the circuit components is configured to provide the first data path in response to the first control signals, and is configured to provide the second data path in response to the second control signals.

Ref. #	Listing of Challenged Claims
16	The memory module of claim 1, wherein the logic is configured to enable the communication of the first data burst between the at least one first memory integrated circuit and the memory controller in accordance with a latency value.
17	The memory module of claim 16, wherein the buffer comprises combinatorial logic, registers, and logic pipelines and is configured to register an additional clock cycle for transferring the first data burst through the buffer.
18	The memory module of claim 16, wherein the logic is further configured to determine the latency value.
19	The memory module of claim 16, wherein the logic is further configured to enable the communication of the second data burst between the at least one second memory integrated circuit and the memory controller in accordance with the latency value.
20	The memory module of claim 19, wherein the buffer comprises combinatorial logic, registers, and logic pipelines and is configured to register an additional clock cycle for transferring the second data burst through the buffer.
21.a	A method of operating a memory module coupled to a memory controller via a memory bus, the memory module comprising memory integrated circuits arranged in ranks and mounted on a printed circuit board having a plurality of edge connections coupled to the memory bus, the memory integrated circuits including at least one first memory integrated circuits including at least one second memory integrated circuit in a second rank, the method comprising:
21.b	receiving at one or more circuits coupled to the printed circuit board a first set of input command and address signals representing a first memory command from the memory controller via the memory bus, the first memory command to cause the memory module to receive or output a first data burst;
21.c	generating a first set of output command and address signals in response to the first set of input command and address signals, the first set of output command and address signals selecting the first rank to receive or output the first data burst;

Ref. #	Listing of Challenged Claims
21.d	receiving at the one or more circuits a second set of input command and address signals representing a second memory command from the memory controller via the memory bus, the second memory command to cause the memory module to receive or output a second data burst;
21.e	generating a second set of output command and address signals in response to the second set of input command and address signals, the second set of output command and address signals selecting the second rank to receive or output the second data burst;
21.f	in response to the first memory command, providing first control signals to a buffer to enable communication of the first data burst between the at least one first memory integrated circuit and the memory controller through the buffer; and
21.g	in response to the second memory command, providing second control signals to the buffer to enable communication of the second data burst between the at least one second memory integrated circuit and the memory controller through the buffer, the second control signals being different from the first control signals.
22	The method of claim 21, further comprising isolating the at least one first memory integrated circuit and the at least one first memory integrated circuit and the at least one second memory integrated circuit from the memory bus when the memory module is not being accessed by the memory system.
23	The method of claim 21, wherein the first set of input command and address signals include at least one input chip-select signal, the method further comprising generating a first chip select signal and a second chip select signal in response to the first set of input command and address signals, the first chip-select signal being provided to the at least one first memory integrated circuit and having an active value to cause the at least one first memory integrated circuit to receive or output data signals in response to the first memory command, the second chip-select signal being provided to the at least one second memory integrated circuit and having a non-active value to keep the at least one second memory integrated circuit from receiving or outputting data signals in response to the first memory command.

Ref. #	Listing of Challenged Claims
24	The method of claim 21, wherein the memory module has an overall CAS latency greater than an actual operational CAS latency of the memory integrated circuits.
25	The method of claim 21, further comprising reporting an overall CAS latency of the memory module to the memory controller, the overall CAS latency having one more clock cycle than an actual operational CAS latency of the memory integrated circuits.
26	The method of claim 21, wherein the buffer includes circuit components configurable to provide a first data path or a second data path depending on whether the first rank or the second rank is caused to communicate data with the memory controller.
27	The method of claim 21, wherein the memory module is a dual in-line memory module (DIMM), and wherein the plurality of memory integrated circuits are double-data-rate dynamic random access memory (DRAM) circuits.
28	The method of claim 21, wherein the first memory command is a first read command and the second memory command is a second read command, wherein the first read command and the second read command are back to back adjacent read commands, and wherein the memory module outputs the first data burst together with a first burst of data strobe signals in response to the first read command, wherein the memory module outputs the second data burst together with a second burst of data strobe signals in response to the second read command, wherein the second data burst follows the first data burst on the memory bus, the method further comprising combining the first burst of data strobe signals and the second burst of data strobes to form a third burst of data strobe signals on the memory bus.
29	The method of claim 28, wherein each of the first burst of data strobe signals and the second burst of data strobe signals includes a pre-amble interval and a post-amble interval, and wherein the third burst of data strobes does not include the post-amble interval of the first burst of data strobe signals and the pre-amble interval of the second burst of data strobe signals.

I. INTRODUCTION

The Institution Decision (“ID”) correctly found claims 1-29 obvious.

Netlist’s Patent Owner Response (“POR”) merely repeats many of the arguments that the ID already rejected.

II. ARGUMENT

A. Level of Skill (POR 8)

The Board agreed with Samsung’s proposed level of skill, except for the qualifier “at least.” ID 9; Pet. 9-10. Netlist also agreed, except Netlist argued a POSITA would not know about the *internal design* of memory devices. POR 8; EX2024, ¶¶68-70; EX1095, 143:11-145:16. But on cross, Netlist’s expert admitted that “was clearly in error,” EX1095, 148:3-:10, 149:9-:16, given that both the Jacob textbook and his own book teach the *internals* of DRAM, *id.* 151:2-154:19, 163:15-:22, 168:4-169:8; EX1070, 353-496; EX1097, 41-68.

B. Claim construction for “*rank*” (POR 8-9) and lack of credibility of Netlist’s expert

With respect to the term “*rank*,” the Board agreed with Samsung that “a rank may have *only one* memory device,”¹ ID 13, consistent with the District Court, other decisions by the Board, the intrinsic evidence, and Jacob textbook, *see* EX2030, 11-14; EX1023, 29-33; EX2023, 4-6; Pet. 27-30; EX1070, 413-14.

¹ All emphases in quotes and color annotations in figures have been added.

Surprisingly, Netlist’s expert still testified that “*rank*” requires “*more than one* memory device.” EX1095, 97:23-99:17. But that contradicts his *own* book, which defines “rank” as “one or more DRAMs.” EX1097, 497; *see also* EX1095, 106:21-107:9, 166:16-167:14, 168:4-:12, 389:15-393:10.² Netlist has wisely given up on this issue. ID 13; POR 8-9.³ Netlist knows the Board will “disregard the testimony of an expert that is plainly inconsistent with the record.” *Homeland Housewares, LLC v. Whirlpool Corp.*, 865 F.3d 1372, 1378 (Fed. Cir. 2017); *CareFusion Corp. v. Baxter Int’l Inc.*, IPR2016-01463, Paper 40, at 4 (PTAB June 13, 2018) (similar).

² Netlist’s expert also argued that JEDEC’s SPD standard prohibits 8-bit wide memory devices, EX1095, 458:15-460:12 (discussing EX2031, 8), contrary to the testimony of another Netlist expert, the document itself, and Figure 10 of Ellsberry, *see* EX1101, 149:10-:13, 152:4-:19; EX1095, 386:4-:15, 388:8-:15, 499:9-505:6 (discussing EX2031, 13).

³ Netlist briefly suggests that the District Court’s construction is inconsistent with “Dr. Wolfe’s description of ‘rank.’” POR 8-9 (citing EX2033, 154:7-:24). To the contrary, both agreed a “*rank*” can have just *one* memory device. EX2033, 6:14-8:8, 157:18-158:10, 174:20-175:15; EX1003, ¶¶124-31; EX2030, 11-14.

C. Ground 1 (POR 1-3, 9-13, 19-39)

1. Netlist ignores Perego's teaching of JEDEC-style implementations (POR 1-3, 9-13, 19-20)

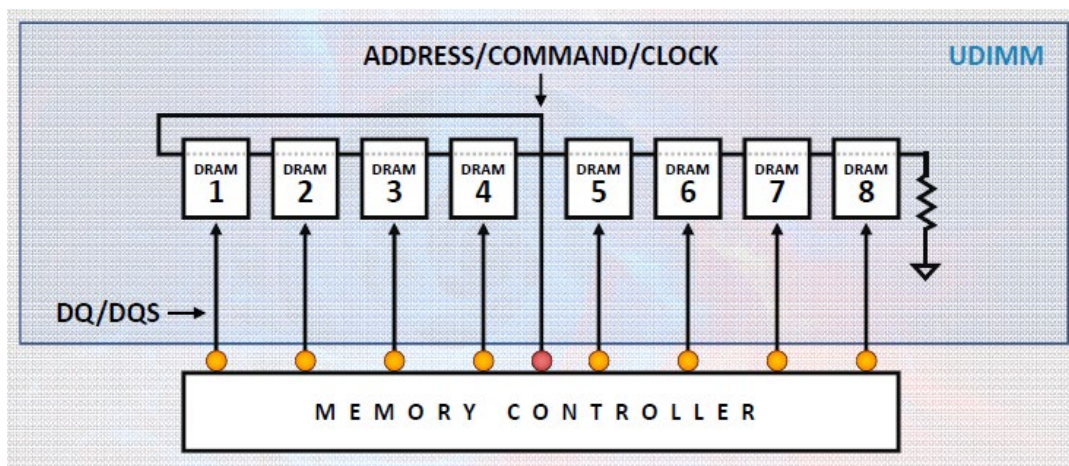
The Board correctly found that “a person of ordinary skill in the art would have combined the teachings of Perego and JESD79-2,” ID 14, which is relevant to all Grounds, Pet. 5, 30-35, 112-16, 126-28, 131-32. JESD79-2 is the JEDEC standard for DDR2 memory devices, *see* EX1064, and “Perego discloses using DDR2 memory devices,” ID 14 (citing EX1071, 10:56-:59), making the combination straightforward.

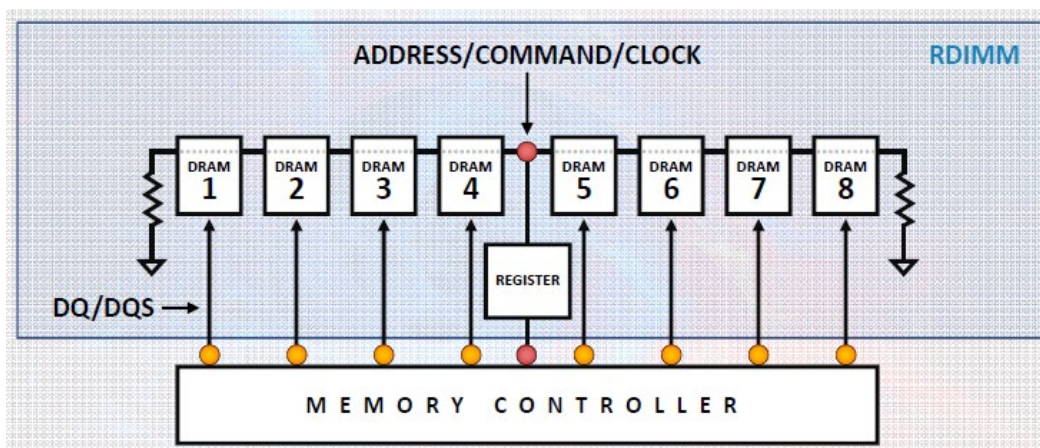
In response, Netlist argues that “Perego discloses Rambus-style modules that...are fundamentally different than the conventional memory bus required by JEDEC module standards and do not include chip-select lines or otherwise convey chip-select signals.” POR 1; EX1095, 467:12-468:6. But the teachings of Perego are not limited to Rambus, as the Board correctly found, ID 14-15, and providing chip-select signals to Perego's module would have been obvious based on JESD79-2 *and the knowledge of other JEDEC standards*, including JESD21-C, which show pins for receiving chip select signals at the memory module. *See* EX1062, 6; EX1066, 6-7; *see also* Pet. 30-35, 37-42, 48-54, 96-99.

Netlist argues that JESD21-C and other standards for “JEDEC *modules*” were not part of the proposed combinations, POR 1-2, 13, but they are still relevant to show that combining Perego with a conventional memory bus including chip-

select lines was obvious, because “[t]he motivation need **not** be found in the references sought to be combined, but may be found in any number of sources, including **common knowledge**, the prior art as a whole, or the nature of the problem itself.” *DyStar Textilfarben GmbH v. C.H. Patrick Co.*, 464 F.3d 1356, 1361 (Fed. Cir. 2006).

Here, there is no dispute a POSITA “would have been familiar” with the JEDEC standards, Pet. 10, including for memory modules, such as EX1062. *See* EX1095, 68:16-69:13, 139:22-141:22. Examples of well-known JEDEC memory modules included UDIMM and RDIMM, illustrated below, both of which receive chip-select signals from the memory controller (as part of “Address/Command” lines represented by the red dots below), as **required** by the JESD79-2 standard for the DDR2 memory devices on the module, *see* EX1064, 6 (“Chip Select:...for external Rank selection....CS is considered part of the **command** code”):





EX1103, 7-9; EX1095, 57:2-:9, 111:24-113:23, 115:16-117:2, 120:12-121:3; EX1062, 6 (“chip select lines” for RDIMM), 12 (“REGISTER” for RDIMM receiving chip select lines “S0” and “S1”); *see also* EX1001, 5:63-6:3, 21:14-:17 (identifying UDIMM, RDIMM, and FBDIMM as compatible with the 215 Patent); EX2024, ¶¶19-36 (admitting POSITA knew about chip select signals, UDIMM, and RDIMM); EX1095, 53:4-:23, 55:9-:22.

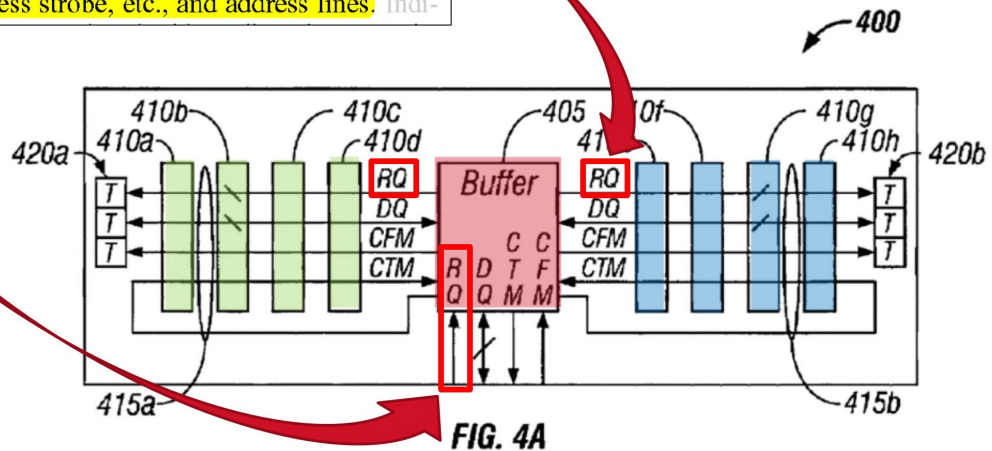
Furthermore, JESD79-2 governs DDR2 memory devices on *all* types of modules, EX1095, 117:18-120:11, and thus JESD79-2 is relevant to *any* memory module with DDR2 memory devices, including Perego. It was also well-known that the “chip-select bus[] is *essential* in a JEDEC-style memory system,” EX1069, 2-3, as admitted by Netlist’s expert, EX1095, 194:15-196:19 (“[I]t is essential.”), 202:10-204:6; *see also* EX2033, 142:5-143:9 (“DDR-compliant DIMMs all have chip select signals”).

JEDEC-compliant modules were dominating the industry by 2004-2005, as

admitted by Netlist’s expert, providing additional motivation for the proposed combination. *See* EX2024, ¶72 (“the vast majority of the DRAM devices **and modules** sold would have been compliant with one of the JEDEC standards”); EX1095, 145:17-146:24 (similar), 181:23-182:14, 185:9-189:10, 283:18-286:15 (“the JEDEC way of doing things...won out” and “the industry did select the JEDEC approach and reject the Rambus approach” by 2004-2005); EX1070, 21; EX2033, 149:7-:23 (“vast majority”); *see also Rambus Inc. v. FTC*, 522 F.3d 456, 459-60 (D.C. Cir. 2008) (“90%”).

Perego itself provides a motivation for connecting chip-select lines to the module because Perego expressly discloses embodiments where “control lines (RQ) may comprise **individual** control lines, for example, row address strobe [i.e., RAS], column address strobe [i.e., CAS], etc., and address lines,” EX1071, 9:58-:60; Pet. 32-33, 41-42, which a POSITA would recognize as the individual control lines (including “CS” chip-select lines) standard in a JEDEC-style memory bus:

In alternate embodiments, control lines (RQ) may comprise individual control lines, for example, row address strobe, column address strobe, etc., and address lines.



EX1071, 9:58-:60 & Fig.4A.

In one embodiment, memory devices 410a-410h are Rambus® Dynamic Random access Memory (RDRAM) devices operating at a data rate of 1066 Mbits/sec. Other memory devices may be implemented on module 400, for example, Double Data Rate 2 (DDR2) DRAM devices and Synchronous DRAM (SDRAM) devices. Utilizing buffer

In accordance with an embodiment of the present invention, control lines (RQ) transport control (e.g., read, write, precharge . . .) information and address (e.g., row and column) information contained in packets. By bundling control and address information in packets, protocols required to communicate to memory devices 410a-410h are independent of the physical control/address interface implementation.

In alternate embodiments, control lines (RQ) may comprise individual control lines, for example, row address strobe, column address strobe, etc., and address lines.

 ADVANCE INFORMATION Direct RDRAM™ 64/72-Mbit (256Kx16/18x16d)			
RQ7..RQ5 or ROW2..ROW0	I	RSL	Row access control. Three pins containing control and address information for row accesses.
RQ4..RQ0 or COL4..COL0	I	RSL	Column access control. Five pins containing control and address information for column accesses.
DQB8..DQB0	I/O	RSL	Data byte B. Nine pins which carry a byte of read or write data between the channel and the RDRAM.

EX2025 at 3

No individual “row address strobe, column address strobe, [...] and address lines”

JEDEC DDR2 SDRAM SPECIFICATION

CS	Input	Chip Select: All commands are masked when CS is registered HIGH. CS provides for external Rank selection on systems with multiple Ranks. CS is considered part of the command code.
ODT	Input	On Die Termination: ODT (registered HIGH) enables termination resistance internal to the DDR2 SDRAM. When enabled, ODT is only applied to each DQ, DQS, DQS, RDQS, RDQS, and DM signal for x4, x8 configurations. For x16 configuration ODT is applied to each DQ, UDQS/UDQS, LDQS/LDQS, UDM, and LDM signal. The ODT pin will be ignored if the Extended Mode Register (EMRS) is programmed to disable ODT.
RAS, CAS, WE	Input	Command Inputs: RAS, CAS and WE (along with CS) define the command being entered.

EX1064 (JESD79-2) at 6

EX1071, 9:58-:60, 10:54-:59; EX1064, 6; EX2025, 3; see also EX1003, ¶¶226-27; EX2033, 141:6-145:24, 148:18-149:6.

The reference in Perego above to “individual control lines” such as RAS and CAS *cannot* be to a Rambus-style interface because Rambus does not have such

lines, as Netlist's expert admitted. EX1095, 235:1-236:25. Indeed, Perego elsewhere uses a similar phrase — “control signals such as RAS, and CAS, etc., and address signals,” EX1071, 6:27-:30 — while citing to the following patent, which confirms that “CHIP SELECT” lines would also be received by the “DIMM” module:

168 PIN SDRAM DIMM		
PIN NAME	#PINS	PIN FUNCTION
A0–A13	14	ADDRESS INPUT
DQ0–DQ79	80	DATA IN/DATA OUT
CS0–CS4	4	CHIP SELECT
WE0	1	WRITE ENABLE
CLK0, CLK1	2	CLOCK
CKE	1	CLOCK ENABLE
Vref	2	POWER SUPPLY FOR REFERENCE
Vcc	17	POWER SUPPLY
Vss	18	GROUND
PD	9	PRESENCE DETECT
ID	4	DIMM ID BIT
SCAS	1	SYNCHRONOUS COLUMN ADDRESS STROBE
SRAS	1	SYNCHRONOUS ROW ADDRESS STROBE
PDE	1	PRESENCE DETECT ENABLE
DQM	4	DATA INPUT/OUTPUT MASK
(DQMB)	(8)	(DATA INPUT/OUTPUT MASK BYTE)
RFU	1	RESERVED FOR FUTURE USE
DU	4	DON'T USE

fig. 3

EX1081, Fig.3 (cited by Perego, EX1071, 6:27-:30).⁴

Furthermore, Perego is not limited to Rambus-style “point-to-point” connections between the memory controller and the memory module, as suggested by Netlist, *see* POR 1-2, 9-12, because Perego expressly discloses using multi-drop *busses*, as was common with JEDEC-style modules. Pet. 37-42; EX1071, 1:50-:53, 3:41-:44, 8:42-:43, 15:9-:11; EX2033, 29:3-:11.

Netlist also argues that Perego’s reference to “translat[ing] protocols” means that there would be no motivation to use a JEDEC interface on the module, and instead the only motivation would be to use a Rambus interface and then to “translate” between the Rambus protocol and the JEDEC protocol used by the DDR2 memory devices, POR 2-3 (citing EX1071, 10:63-:67), as was done in the prior art, EX1095, 364:11-366:21 (discussing EX1071, Fig.2A). But Perego teaches translating protocols in general, and does not require using a Rambus

⁴ The Board correctly recognized in IPR2023-00454 that Perego at 6:27-:33 “draws a distinction based on the lack of buffered data lines in a conventional DIMM,” but Perego does not “discount[] all DIMM teachings” and instead has the goal “to preserve ‘[b]ackward compatibility with existing generations of memory devices,’ of which DIMM was one at that time.” IPR2023-00454, Paper 11, at 20; *see also* ID 16 (agreeing Perego could be implemented in a DIMM).

protocol. EX1071, 10:59-:67; EX2033, 131:24-136:14 (“Perego teaches that the interface need not be a Rambus-compliant interface....[M]ost manufacturers...would provide you your choice of a Rambus or DDR memory controller.”), 146:2-148:2; EX1095, 369:12-370:18. For example, Perego’s “translation” functionality permits a JEDEC interface to implement rank multiplication with DDR2 memory devices, Pet. 10-14, 70-80, which the 215 Patent itself describes as requiring “translation logic.” EX1001, 21:8-:20; EX1095, 344:18-348:9, 478:3-481:17; EX2033, 135:9-:16 (“Perego...with a non-Rambus memory type, as is taught...would still have....a buffer that performs rank multiplication”), 176:22-178:6 (explaining how Perego teaches rank multiplication).

More generally, Netlist is incorrect that a Rambus interface is “fundamentally different” than the JEDEC module standards, POR 1, as recognized by the Board, ID 14-15 (citing EX1069, 11-12). Rambus-style interfaces also had data lines (DQ) separate from signal lines (RQ) for communicating address and control information, EX1095, 233:4-234:25 (discussing EX2025, 3), including “chip-select information,” EX1069, 7, 11-13; EX2033, 23:20-24:22, 148:3-16, 149:24-150:17; EX1097, 821-22 (“DeviceId”); EX1095, 191:19-193:24 (“selected”), 215:15-216:20 (“signals”); *see also Rambus Inc. v. Infineon Techs. AG*, 318 F.3d 1081, 1084-85 (Fed. Cir. 2003) (discussing

relevance of Rambus patents to JEDEC standards).

Thus, using the well-known and popular JEDEC bus in Perego was obvious and well within the level of skill.

2. It would have been obvious to combine Perego and JESD79-2 for JEDEC-style implementations of Perego (POR 20-30)

All of Netlist's arguments against the combination of Perego and JESD79-2 are variations of the arguments above, *see* POR 20-30, and thus incorrect for the same reasons above (pp.3-11).

First, Netlist argues that Perego and JESD79-2 are not directed to "JEDEC-standardized memory *modules*," POR 21, which is incorrect as explained above (pp.3-9).

Second, Netlist argues that Rambus modules were fundamentally different than the RDIMMs defined in JESD21-C. POR 22-24. However, as discussed above (pp.3, 6-9), this argument is flawed from the start, since Perego does disclose using DDR2 memories and JEDEC-style memory busses, similar to those in JESD21-C. As Netlist admits, DDR2 memories are organized in ranks, and chip select signals are required to select one of the ranks on the module for a given read or write command in a JEDEC-style memory system. POR 22-23. Netlist argues that Perego "never mentions a chip-select signal line," POR 22, but Netlist does not dispute that chip-select lines were well known, as explained above (pp.6-9).

Netlist also argues that Perego uses "variable width interfaces" and point-to-

point topology, while JEDEC uses a “fixed buffer width” with a multi-drop bus. POR 23-24. But that mischaracterizes Perego again, since Perego is not limited “variable width interfaces,” EX2033, 29:12-31:6, 79:12-80:10, 127:10-129:2, 135:18-138:8 (width can be fixed at manufacturing time or using 1:1 serialization), and a point-to-point topology is an option not a requirement in Perego as discussed above (p.9). As correctly recognized by the Board, “Perego discloses a serialization ratio of 1:1, meaning that....each rank would match the full bit-width of the memory module as in Petitioner’s proposed construction,” ID 20, and “it is not clear how a device that can have many configurations, one of which satisfies the limitations of a claim, would **not** render obvious the subject matter of that claim merely because it is capable of additional configurations,” ID 22; *Gen. Hosp. Corp. v. Sienna Biopharms., Inc.*, 888 F.3d 1368, 1373-74 (Fed. Cir. 2018); *Iron Grip Barbell Co. v. USA Sports, Inc.*, 392 F.3d 1317, 1320-23 (Fed. Cir. 2004).

Netlist admits that Perego discloses “retaining backward compatibility with existing generations of memory devices” and compatibility for “new generations of memory devices,” POR 24, but ignores that Perego explains that this compatibility and flexibility also applies to existing and future **memory “controllers,”** EX1071, 6:34-:43, which were overwhelmingly JEDEC-compliant at the time, as Netlist’s expert admitted above (pp.5-6), providing further motivation to implement Perego in a JEDEC-style memory system, as recognized by the Board above (p.9, n.4).

Netlist also argues that Perego had a “high-performance Rambus-style primary channel,” POR 24, which is a “superior solution” over the “inferior” JEDEC system, POR 27-28, but Netlist ignores that JEDEC’s DDR modules had equally high performance, thus providing yet another motivation to use them:

TABLE Ov.3 Cross-comparison of SDRAM, DDR SDRAM, and DRDRAM memory systems

DRAM Technology	Operating Frequency (Data Bus)	Pin Count per Channel	Peak Bandwidth	Sustained BW on StreamAdd	Bits per Pin per Cycle (Peak)	Bits per Pin per Cycle (Sustained)
SDRAM	133	152	1064 MB/s	540 MB/s	0.4211	0.2139
DDR SDRAM	2 * 200	171	3200 MB/s	1496 MB/s	0.3743	0.1750
DRDRAM	2 * 600	117	2400 MB/s	1499 MB/s	0.1368	0.0854

EX1070, 23; EX1095, 163:15-:22, 181:23-182:14, 230:23-232:16, 283:8-286:15.

Furthermore, the Petition identified a number of additional benefits for the combination, including JEDEC compatibility, isolation of memories, and cost-effective upgrade capabilities. Pet. 30-35. In any event, the combination does not have to be superior, it just has to be a “suitable option.” *Intel Corp. v. PACT XPP Schweiz AG*, 61 F.4th 1373, 1380-81 (Fed. Cir. 2023).

Third, Netlist argues that the Petition fails to identify JESD21-C in any ground. POR 25-26. But as discussed above (p.4), the motivation to combine can be found outside the references being combined, such as in JESD21-C and Ellsberry, both of which taught that the memory module receives from the memory controller chip-select lines, which are required by JESD79-2. Pet. 33-35, 112-16. The *Philips* case cited by Netlist, POR 25-26, expressly permitted a reference

(“Hua”) to be used to show the “general knowledge” of a POSITA even though it was not part of the grounds in the Petition. 948 F.3d at 1335-38 (affirming obviousness). This is not a situation like *Intelligent Bio-Systems*, POR 25-26, where the “evidence” was not identified in the Petition “with particularity,” 821 F.3d at 1369; 35 U.S.C. §312(a)(3). Here it was all explained with particularity in the Petition, Pet. 33-35, 37-62, 112-16, and discussed by the Institution Decision, ID 17-22.

Fourth, Netlist again argues that Perego teaches “translation” so that DDR2 memory devices can be used with a Rambus architecture. POR 26-29. But that is just a prior-art option, which is not required by Perego’s “translation” capability, as discussed above (pp.9-10). Perego also teaches using a JEDEC bus with individual lines, as discussed above (pp.6-9).

Fifth, Netlist argues that a JEDEC-style implementation would sacrifice Perego’s benefits and alter Perego’s basic principle. POR 29-30. But that is clearly not the case, since Perego itself expressly discloses using DDR2 memory devices and a JEDEC-style bus, as discussed above (pp.3, 6-9). There is no need to redesign Perego, that is a disclosed embodiment. EX2033, 40:25-41:16, 133:3-136:14, 138:10-140:20, 148:18-149:6. The “Configurable Width” functionality includes a 1:1 serialization compatible with JEDEC, as discussed above (pp.11-12). And the combination retains Perego’s benefits, including a data buffer that

isolates electrical load, thus permitting high performance like a “Ferrari” as well as rank multiplication. Pet. 30-35, 80; EX1095, 124:23-126:21, 129:5-131:8, 132:20-137:11. Thus, this is like the *University of Maryland* case cited by Netlist, POR 29, where the Federal Circuit affirmed a finding of obviousness because the primary reference’s “principle of operation” was not altered by the secondary reference. 711 F. App’x at 1010-11.

3. Perego and JESD79-2 teach JEDEC-style implementations of Perego (POR 31-35)

Netlist argues that the combination of Perego and JESD79-2 “fail[s] to disclose several important claim limitations,” such as chip-select signals, POR 31-35, but Netlist’s arguments are just a variation of the arguments above, and thus incorrect for the same reasons above (pp.3-15).

First, Netlist argues there would be no chip-select signals input to Perego’s module. POR 31-32. That is incorrect as discussed above (e.g., pp.3-9, 10).

Second, Netlist argues that Perego does not disclose ranks receiving chip select signals with different values. POR 33-35. This argument ignores the undisputed disclosure by Perego of using DDR2 devices, which JESD79-2 teaches are organized into ranks by chip select signals (with the non-targeted rank(s) for a given read/write command receiving a different chip-select value corresponding to a “NOP”). Pet. 27-30, 54-63; EX1095, 202:10-204:6 (discussing EX1069, 2-3).

Netlist also contradicts its own argument in IPR2022-00615, where Netlist

admitted that Figure 4B of Perego discloses at least two ranks, one rank corresponding to channels 415a and 415b, and another rank corresponding to channels 415c and 415d. EX1019, p.43; EX1020, ¶¶93-94; EX1102, ¶131. As the Petition explained, Perego discloses that each channel can correspond to a rank when only the memory devices in a single channel respond to a read or write command. Pet. 59-63. Furthermore, Perego discloses that each channel can be as wide as the memory module itself, using a 1:1 serialization. Pet. 56-60; ID 20.

Netlist's arguments to the contrary are without merit. For example, Netlist argues that the memories 410 depicted in Figures 4A-C are Direct RDRAM devices, POR 33, ignoring that Perego expressly states that memories 410 can be "DDR2" devices, EX1071, 10:54-:67. Netlist admits Figure 3C could be used with DDR2 devices, but argues that all of those devices would act together as a single rank, POR 34, ignoring Perego's disclosure that each read or write operation can be limited to only "*one*" of the channels, resulting in *multiple* ranks (one per channel). Pet. 59-63; EX1071, 6:15-:24. Netlist also mischaracterizes Dr. Wolfe's testimony in a related case, POR 34-35, where he explained that "Perego does not use the specific word ['rank'] even though he clearly discloses the concept [of rank]." EX2003, 204:12-:21; *see also id.* 79:17-82:3, 82:14-84:13 ("The address bits...would be one of the factors to decide which rank to select....a [POSITA] would understand that the chip select is also used"); EX2033, 71:5-73:7, 160:16-

161:14, 176:6-178:6.

4. Claims 8, 17, and 20: Perego and JESD79-2 disclose a buffer configured to register an additional clock cycle for transferring data through the buffer (POR 35-38)

Perego (like Ellsberry and Halbert), in combination with JESD79-2, teaches a data buffer on the module that registers the data signals, thus adding one clock cycle to the data transfer, resulting in a larger CAS latency for the memory module than for the memory devices on the module. Pet. 73-76, 81-83, 95-96, 110-11.

Netlist also argues that Registered DIMMs only register — and thus delay by one clock cycle — the address and command signals (not the data signals), POR 35-36 (citing EX1062, 68 n.1),⁵ but the Petition pointed to that disclosure to show that if *any* signal is registered on a memory module — including data signals as in Perego — it was obvious to delay the signal for one full clock cycle to allow enough time for the functions of the register. Pet. 81-83, 86-87, 119-21; *see also Intel*, 61 F.4th at 1380-81 (“known technique”). Indeed, Netlist’s expert admitted that putting a buffer on the data path would result in “some delay,” and “[t]here are many examples of a register or buffer that includes *a cycle* of delay.” EX1095,

⁵ Netlist also suggests “no similar language” exists for DDR2 RDIMM memory modules, POR 36, which is incorrect. EX1109, 1 (“registered mode will add one clock cycle to CL [CAS latency]” for DDR2 RDIMM).

132:20-135:17; *see also* EX2033, 100:15-103:10 (“When you register...you are necessarily delaying”). And he admitted there was a motivation to put a buffer on the data path (even if that would add one clock cycle of delay), because it would then permit higher “operating frequency,” similar to a “Ferrari” that may take a little longer to warm up but once it gets going is much faster than a “Volkswagen.” EX1095, 136:3-137:11.

Netlist’s expert also admitted that under JESD79-2, the values for CAS Latency (“CL”) and Additive Latency (“AL”) — which together determine the latency for read and write operations — *must* be configured during initialization and are measured in *one-clock-cycle* increments, such as 2, 3, 4, or 5 clock cycles for CAS Latency, and 0, 1, 2, 3, or 4 clock cycles for Additive Latency. EX1095, 249:17-254:16 (discussing EX1064, 12, 14, 24), 441:9-:15 (admitting CAS latency “dates back to...the 1960s”); EX2031, 16; Pet. 84-87.⁶

Netlist does not dispute that this feature of JESD79-2 — a “programmable CAS latency,” which is “programmed at system initialization” and “never set again

⁶ AL can be set to 0. *See, e.g.*, EX1064, 23 (“Additive latencies of 0...are supported”); *id.* 25, 27, 30, 36 (“AL = 0”). Thus, a read latency of 4 clock cycles can be achieved, for example, by setting CL=4 and AL=0, or CL=3 and AL=1. EX1064, 24 (“RL=AL+CL”), 34, 36.

while the machine is running” — was well known. EX1069, 15; *see also Infineon*, 318 F.3d at 1085 (“programmable CAS latency”). “The primary benefit of programmable CAS latency is *flexibility*” EX1069, 16.

Netlist argues that “Additive Latency (AL)” is only relevant to the memory devices, not “latency at the module level.” POR 36-37. But the Petition merely cited “Additive Latency” to show that latency is measured in *full* clock cycles for DDR2 memory devices, Pet. 81-83, which Netlist does not dispute as discussed above. Netlist also does not dispute that AL can be set to 0, in which case read latency (RL) is equal to CAS Latency (CL), as explained above (p.18 & n.6).

Netlist also disputes whether the clock signals controlling the data latches 597f-m in Perego (blue below) come from the internal clock circuit 570a-b (purple below). POR 37-38.

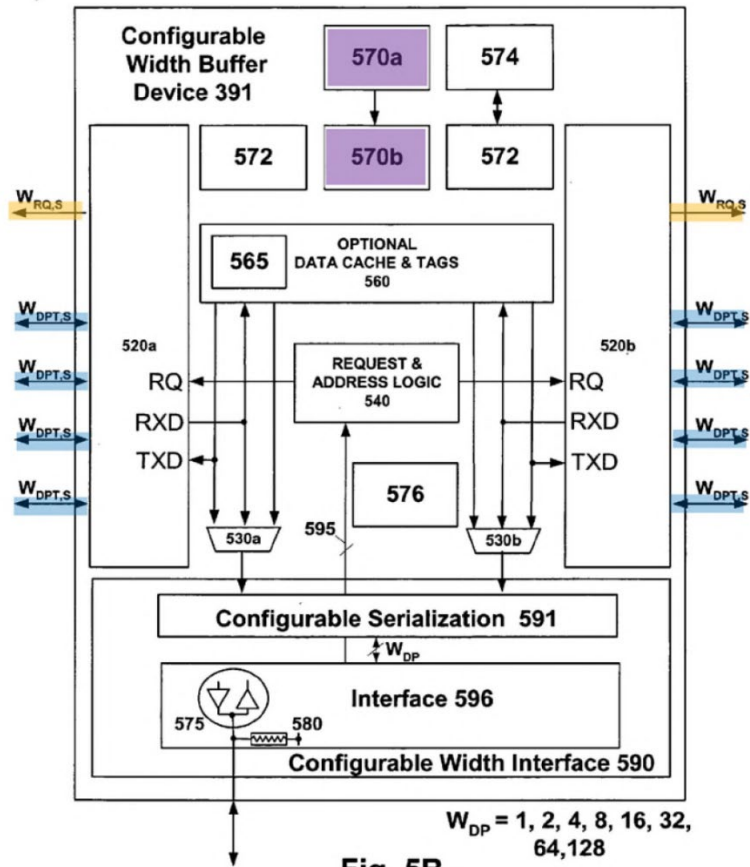


Fig. 5B

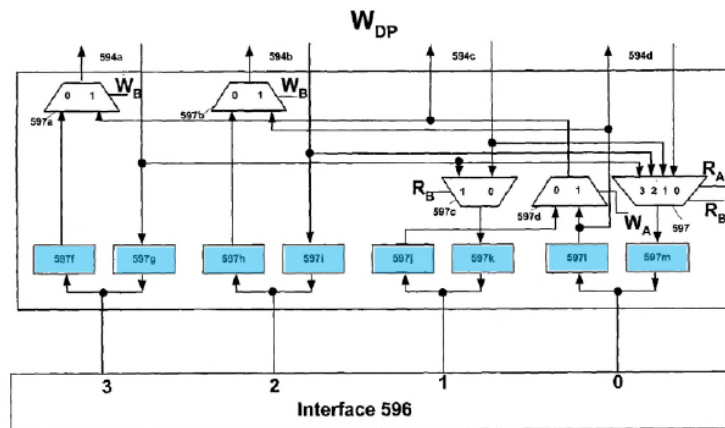


Fig. 5C

EX1071, Fig.5B; Pet. 82-83. Netlist admits, however, that “clock circuits 570a-b” are needed for proper “data capture” by Perego’s data buffer above. POR 37. And Dr. Wolfe explained, and neither Netlist nor its expert disputes, that “latching of

the data signals and the use of internal synchronizing clock signals adds a predetermined amount of time delay for each data transfer through the buffer” and “such registering of the data signals would require the addition of a fixed time delay, such as one clock cycle.” EX1003, ¶335.

5. Claims 4 and 25 (POR 38)

Netlist’s arguments about claims 4 and 25 of the 215 Patent (requiring “one more clock cycle”) are incorrect for the same reasons discussed directly above (pp.17-21).

6. Claims 14-15 and 26 (POR 38-39)

Netlist’s arguments about claims 14-15 and 26 of the 215 Patent are incorrect because they assume Perego is limited to a *single* rank, which is incorrect as discussed above (pp.15-17). Perego renders obvious a “fork in the road” with *multiple* ranks. Pet. 63-72, 107-10, 112.

D. Ground 2 adding Ellsberry to Ground 1 (POR 3, 13-15, 39-52)

1. Ellsberry is a “printed publication” under §311(b) (POR 39-40)

Netlist’s argument that Ellsberry is not a “printed publication” under 35 U.S.C. §311(b) as of its pre-AIA §102(e) date is legally incorrect, as the Board has repeatedly held. ID 29; EX2023, 7-10; EX1099, 27-29; EX1098, 10-12; *see also* MPEP §2217 (confirming pre-AIA §102(e) is applicable to similar language in pre-AIA §301); *Qualcomm Inc. v. Apple Inc.*, 24 F.4th 1367, 1375 (Fed. Cir. 2022)

(“[W]hen Congress enacted the ‘prior art consisting of patents or printed publications’ proviso for IPRs in section 311(b), it is presumed to have done so with reference to the same specialized provision in the reexamination statute [§301].”) (cleaned up).

2. Ellsberry (filed June 1, 2005) is prior art to the ’215 Patent (POR 41-50)

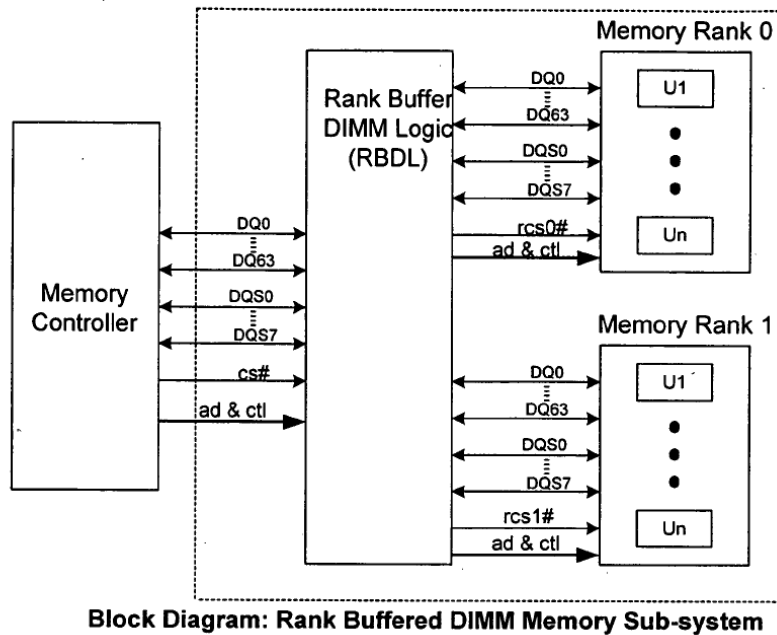
The Petition showed that Ellsberry predates the application for the ’215 Patent. Pet. 5-8. In response, Netlist incorrectly asserts that it only needs to show §112 support in its provisional application for “[*first/second*] control signals to the buffer” and “[t]here is no further burden on Netlist to show that *all* elements of *all* claims are present.” POR 45-46; *see also* EX1095, 495:17-496:12. That is incorrect: “The burden of production...shifts to Patent Owner to show that *the subject matter of [the] claim[s]*...is supported by its priority applications such that Ellsberry is not prior art.” EX1023, 26 (citing *Dynamic Drinkware, LLC v. National Graphics, Inc.*, 800 F.3d 1375, 1379 (Fed. Cir. 2021)). “Petitioner was not required to rebut *in advance* Patent Owner’s argument and evidence alleging priority to the [earlier] application.” *Continental Auto. Sys., Inc. v. Intellectual Ventures II LLC*, IPR2022-00972, Paper 49, at 28 (PTAB Dec. 5, 2023).

Tacitly conceding its burden, Netlist provided a chart purporting to identify support for all the claim limitations. POR 46-50. But that chart is insufficient, for at least two reasons. First, it mixes and matches different applications for different

limitations (e.g., EX1005, EX1006, EX1007, EX1008, EX1009, EX1011), which does not work for §112 because those applications have different inventors and do not cross reference or incorporate each other, and only the 087 Provisional (EX1005) discloses data buffers. 35 U.S.C. §§ 111(b)(7), 120. Netlist's chart is making an *obviousness* combination, which is insufficient under *Ariad* and *Rivera*. See Pet. 8. Second, Netlist's chart has only string citations without any explanation anywhere else in the document, which is impermissible. TPG 35-36; 37 C.F.R. §42.6(a)(3).

With respect to the limitation “[*first/second*] control signals to the buffer,” Netlist admits that this is not expressly disclosed by the 087 Provisional. POR 42; EX1095, 453:23-454:21. Instead, Netlist argues that this limitation is implied by the combination of the box in Figure 1 (shown below) labeled “Rank Buffer DIMM Logic (RBDL),” the JEDEC standards, and the passing references to a “data path multiplexer/demultiplexer.” POR 42-43; EX1095, 263:6-267:5 (arguing a MUX/DEMUX “*necessarily* has to have control signals”).

FIGURE 1:



EX1005, 10.

The problem with Netlist's argument is that it fails to take into account the *selective* nature of the data transfer required by the claims (e.g., “the second control signals [to the buffer to enable communication of the second data burst] being *different* from the first control signals [to the buffer to enable communication of the first data burst]” and “wherein the first rank is selected...in response to the first memory command **and is not selected**...in response to the second memory command, and wherein the second rank is selected...in response to the second memory command **and is not selected**...in response to the first memory command”). For write operations, Netlist does not dispute that data can be sent through the RBDL to *both* ranks (rather than just one rank as required by the

claims), in which case the chip select signals rcs0# and rcs1# could select one rank of memory to perform the write operation, as was done in the prior art. EX1062, 12 (“RS0” and “RS1”); EX1069, 2-3. Thus Netlist fails to show §112 support in the write direction. *See* POR 44 (focusing only on the “read” direction).

In the read direction, Netlist asserts that the MUX/DEMUX must necessarily select “the *one* addressed Rank,” POR 44, which would be an obvious goal to avoid a collision, but is not actually disclosed anywhere in the 087 Provisional. *Cf.* EX1095, 406:5-408:6. More significantly, there is no disclosure that the MUX/DEMUX makes such a selection in response to “[*first/second*] control signals” that were output *from the “logic” on the “memory module”* in “respon[se] to the [*first/second*] memory command,” as required by the claims. Instead, any selection by the MUX/DEMUX could be made in response to other signals from outside the logic on the memory module, such as control signals directly from the memory controller, or the DQS preamble from the memory devices, *see* EX1064, 26 (t_{RPRE}); EX1095, 245:1-247:14. It is not sufficient for Netlist to explain away the DQS preamble, POR 44-45, because that still leaves open other possibilities, such as control signals from the memory controller. And Netlist’s arguments against the DQS preamble are without merit, because they are based on the premise that it would be *impossible* for a POSITA to detect such a preamble. POR 44-45; EX1095, 287:2-292:9 (“It’s not that he wouldn’t try to; it’s

that he can't.”). But that premise is directly refuted by a contemporaneous patent by Intel (published in 2002), which expressly discloses and claims “a technique which can identify a valid READ PREAMBLE.” EX1113, 1:49-2:11, 3:48-:67 & Fig.2, 6:12-:37; EX1095, 121:21-122:10, 314:16-315:13, 325:20-335:7.

For at least these reasons, Netlist failed to satisfy its burden of production to show that each and every limitation of the claims is supported by an application (such as EX1005) filed before Ellsberry on June 1, 2005.

3. A POSITA would have combined Perego and JESD79-2 with Ellsberry (POR 50-52)

Assuming Ellsberry is prior art, the Board correctly found a motivation to combine Ellsberry with Perego and JESD79-2. ID at 30-32; Pet. 112-16.

Netlist's arguments to the contrary are without merit. POR 50-52. First Netlist repeats its argument that Perego is limited to a Rambus-style, point-to-point, variable width interface, that cannot perform rank multiplication, POR 50-51, which is incorrect as discussed above (pp.3-17). Perego's buffer device “may feasibly render the type of memory device *transparent* to the system,” EX1071, 10:59-:63, thus permitting rank multiplication (as discussed above, pp.10, 15) where “it appears to the memory controller that two or more memory devices are actually one larger device,” POR 51. The 215 Patent itself describes rank multiplication as “a fully *transparent* operational conversion from the ‘system memory’ density domain of the computer system to the ‘physical memory’ density

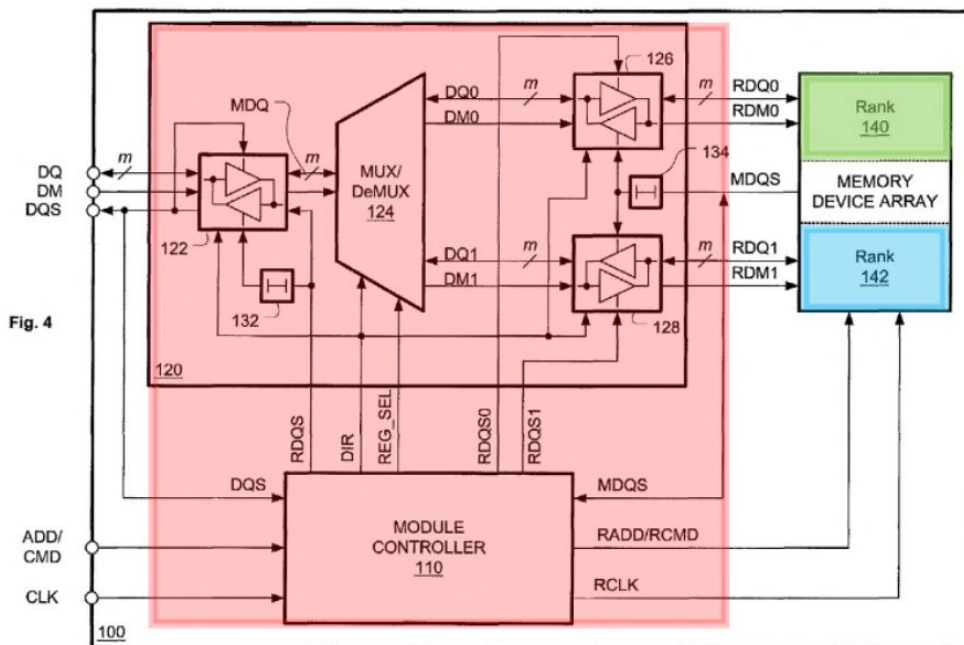
domain of the memory module.” EX1001, 22:61-:64.

Second, Netlist argues that Ellsberry’s distributed data buffers are different from Perego’s centralized buffer. POR 51-52. Netlist, however, does not dispute the advantages of data buffering, or that both centralized (*e.g.*, Perego) and distributed (*e.g.*, Ellsberry) approaches were known alternatives at the time, as confirmed by Halbert teaching both options, EX1078, 7:31-:53, Fig.4 (centralized buffer, m-bits wide), Fig.7 (distributed buffers, m/2-bits wide), rendering obvious using either approach. Netlist argues that the Petition should have addressed differences raised in a white paper *10 years after* the 215 Patent’s priority date, POR 51-52 (citing EX2010), which is nonsense, since that white paper did not exist at the time, and neither the 215 Patent nor its claims address any of those issues, either. “[T]he [215] patent itself does not disclose the level of detail that [Netlist] would have us require of the prior art.” *Lockwood v. Am. Airlines, Inc.*, 107 F.3d 1565, 1570 (Fed. Cir. 1997).

E. Ground 3 adding Halbert to Ground 1 (POR 3, 15-18, 52-54)

Ground 3 combines Ground 1 with Halbert. Pet. 126-31; ID 32-33. Netlist does not dispute that Halbert describes two “ranks” 140 and 142 (green and blue below) each having a respective data bus RDQ0 and RDQ1 having the same bit width (m) as the module, POR 17, but Netlist argues that those two ranks receive the same commands, thus they are not separate “*ranks*” according to Petitioner’s

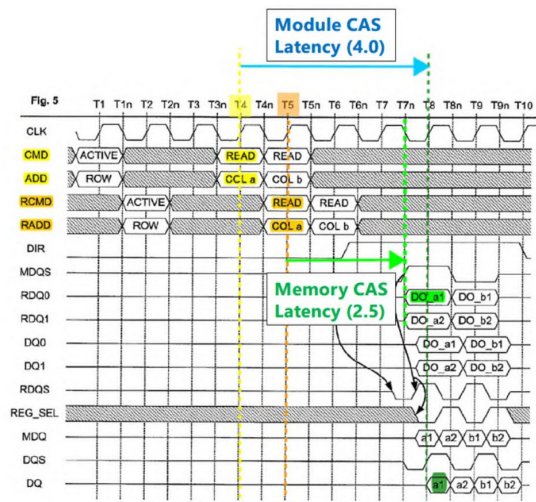
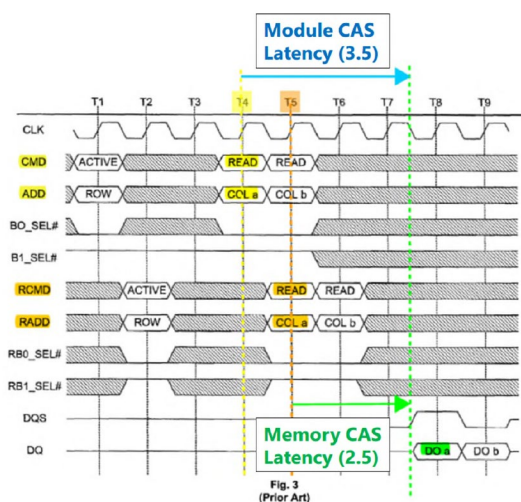
proposed construction. POR 52-54. That is incorrect. Halbert is not limited to the embodiment cited by Netlist. Indeed, as Netlist admits, POR 54, Halbert explains that “multiple ranks will receive the same address and commands” only “[g]enerally,” not always. EX1078, 4:57-:59. “Halbert’s use of the word ‘generally’ means that it is not always the case that memory ranks perform memory operations concurrently.” EX1107, 27. Contrary to Netlist’s mischaracterization, the testimony of Dr. Wolfe is consistent with this understanding of Halbert. EX2033, 179:20-181:14; *see also* EX1095, 421:20-424:1.



Pet. 128-29; EX1003, ¶¶202, 278.

For dependent claim 3, Netlist does not dispute that Halbert renders obvious “an overall CAS latency greater than an actual operational CAS latency of each of

the plurality of memory integrated circuits.” Pet. 129-31. The Petition specifically compared the module’s overall CAS latency *without* data buffering (3.5 clock cycles in Fig. 3, below left), to that *with* data buffering (4.0 clock cycles in Fig. 5, below right), thereby identifying an amount of delay caused by the data buffer (e.g., 0.5 clock cycles). *See id.*; see also EX1003, ¶¶343-44 (explaining the time delay caused by data registers 122, 126 and 128 in Halbert’s data buffer); EX1095, 132:20-133:6 (“Inevitably, there’s some delay”), 434:6-435:15, 437:20-438:6.



Pet. 130-31. As discussed above (p.18), a POSITA would have understood that, in the context of the DDR2 memories disclosed by Perego, latencies are measured in *full* clock cycles, thus motivating her to delay the data signals by *one* clock cycle to avoid synchronization issues and to be compatible with JEDEC standards. EX1003, ¶¶334-36. Furthermore, it was well known to use registers to delay signals by one clock cycle. *See, e.g.*, EX1078, Fig. 5 (above right, showing data signal DO_a2 being delayed by one clock cycle from T7n to T8n); EX1095, 133:8-

135:17 (“There are many examples of a register or buffer that includes *a cycle* of delay.”).

F. Ground 4 adding Matsui2 to Ground 1 (POR 55)

Netlist’s arguments against Ground 4 depend entirely on its arguments against Ground 1, *see* POR 55, and thus they are incorrect for all the reasons above (pp.3-21) and as explained in the Petition, Pet. 131-34.

G. Simultaneous invention (POR 55-56)

Netlist is incorrect, as a legal matter, that “*anticipatory* references” are needed to show “simultaneous invention.” POR 56. Simultaneous invention concerns “obviousness” not anticipation. Pet. 135; *Geo. M. Martin Co. v. Alliance Machine Sys. Int’l LLC*, 618 F.3d 1294, 1305-06 (Fed. Cir. 2010); *Ecolochem, Inc. v. S. Cal. Edison Co.*, 227 F.3d 1361, 1379 (Fed. Cir. 2000).

Similarly, it does not matter whether the claims of the 215 Patent are *limited* to “rank multiplication,” POR 55-56, because that is certainly an embodiment of the claims, Pet. 10-15, 112-20; EX1003, ¶¶603; EX1095, 341:8-348:9, 472:14-474:12.

Netlist’s argument that Perego does not disclose rank multiplication is again based on the false premise that Perego is limited to a Rambus architecture, EX2024, ¶¶182-83, which is incorrect as discussed above (pp.3-17). And Netlist’s expert admitted that Ellsberry implements rank multiplication in a manner

“similar” to the 215 Patent, EX1095, 414:8-416:7, 416:22-418:25, which is strong evidence of simultaneous invention, which applies regardless of whether Ellsberry is prior art or a “printed publication.”

III. CONCLUSION

For the reasons set forth above and in the Petition, Samsung respectfully requests that claims 1-29 be canceled as unpatentable.

Dated: March 9, 2024

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CERTIFICATE OF COMPLIANCE

I hereby certify that this **Petitioner's Reply to Patent Owner's Response** complies with the type-volume limitations of 37 C.F.R. § 42.24(c)(1) because it contains 5,501 words (as determined by the Microsoft Word word-processing system used to prepare the petition), excluding the parts of the reply exempted by 37 C.F.R. § 42.24(c).

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CERTIFICATE OF SERVICE

Pursuant to 37 C.F.R. § 42.6(e), I certify that on this 9th day of March, 2024, **Petitioner's Reply to Patent Owner's Response and Exhibits 1095–1099, 1101–1104, 1107–09, and 1113** were served by email on the following counsel for Patent Owner:

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