UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

_____

SAMSUNG ELECTRONICS CO., LTD.

Petitioner,

v.

NETLIST, INC.,

Patent Owner

_____

IPR2023-00455

Patent 9,858,215

_____

IPR2023-201428
Patent 8,787,060

_____

IPR2023-00454
Patent 11,093,417

Remote video-recorded deposition of

STEVEN PRZYBYLSKI, PH.D.,

Volume 1

REPORTED BY:
Gail L. Inghram Verbano:
Registered Diplomate Reporter,
Certified Realtime Reporter,
Certified Shorthand Reporter-CA (No. 8635)

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Patent Owner

WHEREUPON, the remote video-recorded deposition of STEVEN PRZYBYLSKI, Ph.D., Volume 1, was held via Zoom videoconferencing, on Thursday, February 15, 2024, beginning at approximately 8:07 a.m., the proceedings being recorded stenographically by Gail Inghram Verbano, Registered Diplomate Reporter, Certified Realtime Reporter, Certified Shorthand Reporter-CA (No. 8635), and transcribed under her direction.

A P P E A R A N C E S

A P P E A R A N C E S:

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C O N T E N T S

EXAMINATION OF:

PAGE

STEVEN PRZYBYLSKI, Ph.D.

By Attorney Chandler 8

E X H I B I T S

NUMBER: PAGE

Exhibit 1096 Redline comparison of the 14
Declarations of Dr. Przybylski

Exhibit 1097 Second of edition of textbook 167
by S. Przybylski, "New DRAM
Technologies: A Comprehensive
Analysis of the New
Architectures" (451 pages)

Exhibit 1103 PowerPoint presentation re: 63
Netlist's Technology Tutorial,
5-8-17 (CDX-200.1 to 200.11)

///

Samsung Ex. 1095, p. 4
Samsung Electronics Co., Ltd. v. Netlist, Inc., IPR2023-00455

E X H I B I T S (Cont'd)

NUMBER PAGE

Exhibit 1104 JEDEC Standard for DDR SDRAM, ...77
JESD79D, January 2004
(86 pages)

Exhibit 1106 JEDEC Standard 21-C for DDR 79
SDRAM (36 pages)

(Exhibits 1098 through 1102 not identified.)

PREVIOUSLY MARKED EXHIBITS REFERENCED:

NUMBER PAGE

Exhibit 1001 9
Exhibit 1005 254
Exhibit 1060 45
Exhibit 1062 46
Exhibit 1064 37
Exhibit 1069 193
Exhibit 1070 100

Samsung Ex. 1095, p. 5
Samsung Electronics Co., Ltd. v. Netlist, Inc., IPR2023-00455

Exhibit 1071 36
Exhibit 1072 43
Exhibit 1073 40
Exhibit 1078 41
Exhibit 1079 44
Exhibit 1082 42
Exhibit 2020 70
Exhibit 2024 11
Exhibit 2025 232
Exhibit 2031 71

Thursday, February 15, 2024; 8:07 a.m.

- - -

THE VIDEOGRAPHER: Good morning. We're now on the record at 8:07 a.m. Pacific Time on February 15th, 2024.

This begin the video-conferenced deposition of Steven Przybylski, taken in the matter of Samsung Electronics Company, Ltd., versus Netlist, Incorporated, filed before the Patent Trial and Appeal Board, Case Number IPR2023-00454 and IPR2023-00455.

My name is Dana Bachman. I'm your videographer today. Our court reporter is Gail Verbano. We are both representing Esquire Deposition Solutions.

Will everyone present please identify themselves, beginning with our witness, Mr. Przybylski.

DR. PRZYBYLSKI: Steven Przybylski.

THE VIDEOGRAPHER: Thank you.

Counsel, please.

ATTORNEY CHANDLER: Good morning. This is Theodore Chandler from Baker Botts on behalf of the Petitioner, Samsung Electronics

Co., Ltd. And with me is my colleague Dr. Ferenc Pazmandi.

ATTORNEY WARRICK: Philip Warrick with Irell & Manella on behalf of Patent Owner Netlist, Inc. And with me is Dr. Anita Zhong, also with Irell & Manella.

THE VIDEOGRAPHER: Thank you very much.

Madam Reporter, would you please swear in our witness.

WHEREUPON,

STEVEN PRZYBYLSKI, Ph.D.,

being first duly sworn or affirmed to testify to the truth, the whole truth, and nothing but the truth, was examined and testified as follows:

EXAMINATION

BY ATTORNEY CHANDLER:

Q. Good morning. Please state your name for the record and spell your last name.

A. Steven Przybylski, P-R-Z-Y-B-Y-L-S-K-I.

Q. What do you do for a living, Dr. Przybylski?

A. I am an intellectual property consultant, principally.

Q. Dr. Przybylski, were you retained by Netlist to provide opinions in this case related to Netlist's '417 patent?

A. Yes.

(Exhibit Number 1001 was previously marked for identification.)

BY ATTORNEY CHANDLER:

Q. And the '417 patent is marked as Exhibit 1001 in IPR2023-00454 and is U.S. Patent Number 11,093,417; correct?

A. Correct. Technically, I'm not retained by Netlist but through an intermediary, but it doesn't make any real difference.

Q. Dr. Przybylski, were you also retained by Netlist, at least indirectly, to provide opinions in this case related to Netlist's '215 patent?

A. Yes.

Q. And the '215 patent is marked as Exhibit 1001 in IPR2023-00455 and is U.S. Patent Number 9,858,215; correct?

A. Yes.

Q. The '417 and '215 patents are

related to each other and have substantially the same figures and written description; correct?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: Yes, that's correct.

BY ATTORNEY CHANDLER:

Q. Given that this is a remote deposition, meaning that we're not in the same physical room together, there are a few questions I need to ask, starting with where are you physically located right now during this deposition?

A. Ann Arbor, Michigan.

Q. Is there anyone else in the room with you right now?

A. No.

Q. Given that I cannot see the room that you are in, will you please let us know if someone enters the room that you're in at any time before this deposition ends?

A. I will do so.

Q. Dr. Przybylski, did you bring anything with you to your deposition today?

A. I have clean copies -- hard

copies of the two declarations from the two IPRs.

(Exhibit Number 2024 was previously marked for identification.)

BY ATTORNEY CHANDLER:

Q. Marked as Exhibit 2024 in each IPR?

A. Correct.

Q. And is there anything on your computer related to these IPRs in front of you?

A. On the screen, you mean?

Q. Correct.

A. I have the Zoom that's going on. You also bade me to download redlines, and I have one of those two visible to me right now.

Q. Okay.

A. I also have a window -- Explorer window up where it's showing the folder in which that downloaded redline exists.

Q. Given that I cannot see whether you have anything in front of you, will you please let us know if you or anyone else puts anything in front of you at any time before this deposition ends?

A. Of course.

Q. I will take breaks throughout your deposition, but I want to remind you that during those breaks, under the rules of the PTAB, you should not consult with your counsel about the substance of your testimony.

Do you understand?

A. I do.

Q. During deposition, I would ask that you do not look things up on the internet or do other things on your computer or your phone that we cannot see on the camera.

Do you understand?

A. I do.

Q. And you also understand that during your deposition, you should not be emailing or texting with other people?

A. Of course.

Q. Approximately how many times have you been deposed before?

A. Somewhere between 15 and 20.

Q. Do you have any questions for me about the procedure for today's deposition?

A. Not at this time.

Q. My questions to you today are intended to cover your opinions in both

IPR2023-00454 and IPR2023-00455.

Understood?

A. Yes.

Q. And unless you tell me otherwise, I will understand your answers to my questions to apply equally to both IPRs.

Is that fair?

A. So is it your intent, then, to bounce back and forth between the two IPRs or to deal with one and then the other?

Q. To cover both at the same time.

A. Okay. I understand.

ATTORNEY WARRICK: Counsel, I would just ask on the record that you be clear when you're asking questions that are specific to one patent or the other, given that they are distinct patents with different claim language, among other things.

BY ATTORNEY CHANDLER:

Q. So, Dr. Przybylski, again, to be clear, unless I state otherwise, my questions are intended to cover both patents and both IPRs at the same time.

Understood?

A. Understood. I will endeavor to

refer to both declarations in parallel in order to make sure I'm answering for both IPRs.

(Whereupon, Exhibit Number 1096 in both IPRs was marked for identification and is attached hereto.)

BY ATTORNEY CHANDLER:

Q. And to that end, I have marked a new exhibit numbered 1096 in each IPR, which I've uploaded into the chat so that everyone can have a copy. And Exhibit 1096 in both IPRs is a computer-generated redline comparing your declaration in IPR2023-00454, marked as Exhibit 2024 to your declaration, and IPR2023-00455, marked as Exhibit 2024.

Do you understand?

A. Are you representing that those two files are identical?

Q. The two Exhibit 1096 files are identical except for the stamp on the bottom right that provides the IPR number.

A. And they both are a redline of the '417 showing the changes for the '215.

Is that accurate?

Q. Correct.

A. Understood.

Q. As shown in the redline marked as Exhibit 1096, there are many paragraphs in your declaration marked as Exhibit 2024 in IPR2023-00454 that are substantively identical to your declaration marked as Exhibit 2024 in IPR2023-00455.

Is that fair?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: Yes, that's fair.

I will note that there are -- can you look at page 21 of 225 in the redline document. It's not rendering properly for me. Is that also on your end?

BY ATTORNEY CHANDLER:

Q. Yes. So to be clear, it's a computer-generated redline, and computers are not imperfect.

A. Tell me about it.

Okay. So I will -- where coming across those issues, I will be referring to the master documents, the declarations, to understand exactly what's -- what the redline is trying to convey.

Q. Fair enough.

And that's what I was going to get at, which is, if it's helpful to you during the deposition today, please feel free to use Exhibit 1096 if you need to find the corresponding paragraph number in your other declaration. For example, towards the end of your declaration, the paragraph numbering between the two declarations starts to diverge, even though there are still many paragraphs toward the end of your declaration that are substantively identical.

Understood?

A. I see that, yes.

ATTORNEY WARRICK: Counsel, I just want to state for the record that, based on at least page 21, as identified by the witness, this is not a completely accurate redline of the two declarations.

BY ATTORNEY CHANDLER:

Q. Dr. Przybylski, in general, to be clear, I'll be asking you questions today that are not unique to one IPR or the other IPR and, instead, are relevant to both IPRs.

Understood?

A. Yes, understood.

Q. What did Netlist ask you to do in this matter?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: Attorneys for Netlist asked me to review the IPRs and the documents therein and to formulate opinions vis-a-vis the assertions made therein and in the declarations associated with them.

BY ATTORNEY CHANDLER:

Q. And when you say "review the IPRs," are you referring to the petition that was filed in each IPR, or to something else?

A. To the petitions, yes -- and, as I mentioned, the declarations and the exhibits attached thereto.

Q. Did anyone help you with your work in these two IPRs?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: To the extent that I did communicate with counsel for Netlist on the work as it was progressing.

BY ATTORNEY CHANDLER:

Q. And when you say "counsel for

Netlist," are you referring to the lawyers at Irell & Manella or to someone else?

A. Yes, to those two.

Q. And to be clear, when you say "those two," you're referring to the lawyers at the law firm named Irell & Manella?

A. Yes, correct.

Q. What did you do to prepare for today's deposition?

A. I reviewed my declaration and the -- some of the principal references referred to in the petition. Those are the -- I did also glance at the petitions and declarations but not to review them in detail.

Q. And to be clear, you referred to your declaration in the singular; but you actually have two declarations, one for each IPR. Those declarations overlap, but they're not entirely identical to each other; correct?

A. Correct.

Q. And did you meet with anyone in preparation for today's deposition?

A. Yes.

Q. And who attended that meeting?

A. Philip Warrick and Annita Zhong.

Q. Anyone else?
A. No.
Q. And when was that meeting, and how long was it?
A. We had three meetings over the course of the last several days this week.
Q. And for approximately how many hours did you meet to prepare for today's deposition?
A. For the meetings per se, they were on the order of about four hours total, I would say.
Q. And did you also prepare on your own time by yourself for today's deposition?
A. Yes, I did.
Q. And for approximately how long?
A. Preparation in earnest began last Friday through the weekend and through the first part of this week. So I would say probably around 10 hours or so, maybe a little bit more. I don't know.
Q. So within the last two to three weeks, approximately how many hours in total have you spent preparing for today's deposition?
A. My answer was for the total

Samsung Ex. 1095, p. 19
Samsung Electronics Co., Ltd. v. Netlist, Inc., IPR2023-00455

amount.

Q. So in the last two to three weeks, you believe you spent a total of about 10 hours preparing for today's deposition, including both time spent preparing on your own and time spent meeting with the lawyers at Irell & Manella; is that correct?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: It's probably a little bit more in that counting the meetings with the attorneys from Irell; so call it 15 hours approximately. Maybe a little bit more.

BY ATTORNEY CHANDLER:

Q. So in the past two to three weeks, you believe you spent a total of approximately 15 hours preparing for today's deposition.

Is that fair?

A. That's fair. I'd have to review my notes to get a more accurate number, but that's a good estimate as we stand right here.

Q. As part of your work for Netlist on this matter, did you personally talk to anyone else, such as the inventors or anyone

else with experience in the field?

A. I don't recall any other meetings other than with the attorneys at Irell.

Q. How much are you charging per hour for your time spent on these two IPRs?

A. My billing rate for these IPRs is $550 an hour.

Q. In total, approximately how many hours have you spent working as an expert in these two IPRs?

A. Including the creation of the declarations, you mean --

Q. Yes.

A. -- and the preparation for this deposition?

Q. Correct.

A. The creation of the declarations was a while ago. I don't remember exactly how long -- how much time, but that's -- for the two IPRs together, it was probably on the order of 100 hours or so. I don't know. Don't remember well.

Q. And approximately how much in total have you billed for the time you have spent working as an expert in these two IPRs?

A. That would be the hours spent multiplied by 550, so presumably that's somewhere around $50,000. But, again, I don't have my invoices in front of me.

Q. Aside from these two IPRs, are there other matters where you are engaged by Netlist, either directly or indirectly, to provide expert opinions?

ATTORNEY WARRICK: Objection; form and scope.

THE WITNESS: Yes.

BY ATTORNEY CHANDLER:

Q. And could you summarize those other matters.

ATTORNEY WARRICK: Same objections.

THE WITNESS: There are additional IPRs that I have offered declarations in that are -- my involvement in those have concluded.

BY ATTORNEY CHANDLER:

Q. Anything else related to Netlist besides the other IPRs that have concluded?

A. I believe I offered a claim construction opinion, but that was like two

years ago.

Q. Anything else?

A. Not that I can recall.

Q. And the other IPRs where you were engaged by Netlist, either directly or indirectly, what was the general subject matter of those patents?

ATTORNEY WARRICK: Objection; form, scope.

THE WITNESS: They were IPRs related to other Netlist patents.

BY ATTORNEY CHANDLER:

Q. And were those other Netlist patents related to the '417 and '215 patents in these IPRs?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: Well, they're related in that they have common ownership. There are certainly concepts that were common to both, but I don't recall specifically whether the claims overlapped substantially or whether the specifications were identical.

There are also pieces of prior art that were common across some of these other

cases.
BY ATTORNEY CHANDLER:
Q. And the other IPRs that you're referring to, were those other IPRs related to each other?
ATTORNEY WARRICK: Objection to form.
THE WITNESS: Again, they were related to each other based on common ownership. At least two were related to the same patent. Beyond that, I have no specific recollection.
BY ATTORNEY CHANDLER:
Q. Before this case, when did you first do any work for Netlist? Approximately what time frame?
A. I don't recall any engagement for Netlist prior to the immediately precursor IPRs that we just discussed.
Q. And so approximately when did you first do any work for Netlist, to your recollection?
A. So to my best recollection today is that it would be somewhere in the 2001 -- I'm sorry -- 2021 time frame -- yeah, approximately.
Q. Before you were first engaged by

Netlist around the year 2021, were you familiar with Netlist as a company?

A. Yes.

Q. How so?

A. As an expert in the DRAM field, I'm aware of lots of activities within that whole industry; and Netlist has certainly been a participant in that over the years.

Q. And could you be more specific as to what you recall or knew about Netlist before you were first engaged by Netlist as an expert around the year 2021.

ATTORNEY WARRICK: Objection; form.

THE WITNESS: I was aware that they participated in the development of novel memory modules, and I believe they directly sold those as well. But I don't know if that was only indirectly or whether it was licensing.

BY ATTORNEY CHANDLER:

Q. And did you develop that awareness of Netlist as a participant in the industry or as a professor or as a participant in the standards-setting organization? What was the sort of context of your awareness?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: Principally, as an industry expert that consulted and taught and wrote about the industry.

BY ATTORNEY CHANDLER:

Q. Before you were first engaged by Netlist around the year 2021, did you know any of the named inventors on the '417 and '215 patents identified as Jeffrey C. Solomon and Jayesh R. Bhakta?

A. No, I have no recollection of ever having encountered them personally.

Q. Do you own any Netlist stock or stock options?

A. No.

Q. Is your compensation in this case contingent in any way on the outcome of the case?

A. No.

Q. Are your expert declarations, marked as Exhibit 2024 in these two IPRs, complete? Meaning do they provide a complete statement of all the opinions you intend to express in these IPRs, along with the basis and

reasons for those opinions?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: Yes, they include all of my opinions. The basis for those opinions includes my knowledge as an industry expert, not all of which is written down within the four corners of the declarations.

BY ATTORNEY CHANDLER:

Q. Are your expert declarations marked as Exhibit 2024 in these two IPRs accurate, meaning they do not have any mistakes as far as you know?

A. I certainly encountered the usual number of typographical and other proofreading errors, but nothing of substance.

Q. Do you have any present plans to correct or supplement your expert declarations, marked as Exhibit 2024 in these two IPRs?

A. No, I have no plans as of this moment.

Q. Please look at your CV at the end of your declarations marked as Exhibit 2024 in the two IPRs, and let me know when you're ready to proceed.

A. I have in front of me Appendix A of the '0455 IPR -- i.e., attached to the -- related to the '215 patent.

Q. And as shown in Exhibit 1096, your CV appears to be the same in both of your expert declarations, marked as Exhibit 2024; correct?

A. Yes, that is correct.

Q. Your CV at the end of your expert declarations, marked as Exhibit 2024 in both IPRs, does not list any of your prior expert testimony; correct?

A. That's correct.

Q. Why not?

A. It is just not part of my CV that I normally keep and distribute.

Q. Do you have a list of your prior expert engagements in which you were either deposed or testified at trial?

A. I have an informal running list, yes.

Q. And do you have access to that now?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: I don't have a hard copy of it, no.
BY ATTORNEY CHANDLER:
Q. But on your computer you have access to such a list; correct?
ATTORNEY WARRICK: Objection; form.
THE WITNESS: Yes.
BY ATTORNEY CHANDLER:
Q. Could you please summarize for us your prior expert engagements in which you were either deposed or testified at trial.
A. So I have been involved in litigation support generally for quite a long while and have been engaged in upwards of 50 different matters, of which I have offered testimony in approximately 20 of them and been deposed on either a -- for an IPR or for infringement or invalidity on the order of 15 to 20 times, sometimes multiple times per engagement; and have appeared at ITC hearings. And that is an accurate summary.
Q. Do you have access to a list of the cases in which you were engaged as an expert and either deposed or testified at trial?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: I don't keep track of case identifiers. I do keep track of participants.

BY ATTORNEY CHANDLER:

Q. Sure.

So starting with the most recent time frame, can you just go back chronologically and tell us the case participants in which you were the expert and the name of your client.

A. I'll have to bring up the file to answer that question.

ATTORNEY WARRICK: Counsel, I just want to say, to the extent you're asking the witness to go searching for files, that's not necessarily -- first of all, that's not the same as bringing documents to a deposition and should not be construed as a waiver of any sort of protections that might apply to those documents.

BY ATTORNEY CHANDLER:

Q. So, Dr. Przybylski, are you able to answer the question?

A. I am bringing up my list for --

so I can answer your question.

Okay. So repeat your question, please.

Q. Starting from today and going back chronologically, can you tell us the case participants in which you're the expert and the name of your client?

And to keep things orderly, why don't we only take a few years at a time. So I don't need you to tell me your whole life's story, but let's go back in time as to who you've been engaged as an expert by and what the case was and whether you were deposed or testified at trial in that case.

A. Okay. So testifying experience most recently is Nelson Bumgardner Conroy PC, and that was Xueshan v. Renaissance.

Most recent after that was Freitas & Weinberg LLP. That was in the -- offered a claim construction declaration.

Prior to that, the client was Amin Turocy & Watson, LLP.

Q. For clarification, so, for example, in the claim construction declaration that you offered, who was the party that you

offered the claim construction for and who was the opposing party?

A. That was Polaris Innovations, Inc., v. Xilinx.

Q. Okay.

A. Prior to that was -- as I said, Amin, Turocy & Watson, LLP, representing AusTech Computer International and AusTech -- I'm sorry -- and Asus Computer, Inc., and this was offering a rebuttal expert report.

Prior to that --

Q. And when you say "prior to that," it would be helpful if you give an approximate time frame. I understand cases --

A. We're in 2001 -- I'm sorry. 2021-2022 time frame.

Q. Uh-huh.

A. The Fabricant LLP. Rampart Asset Management, LLC, was the party involved versus NXP. And I offered a claim construction declaration in that matter.

Prior to that was Skiermont Derby LLP for Micron, offering a claim construction declaration and four IPR declarations and corresponding depositions.

Q. And to be clear, was the client Micron or was the adverse party Micron?
A. The adverse party was Micron.
Q. And who was the client?
A. Netlist. I thought I said that. Perhaps I didn't.
Q. Okay. Before that?
A. Prior to that, the client was Venable LLP. The client that I was working for was HD Silicon Solutions LLP -- no. I'm sorry.
That one I believe was -- Microchip Technology was the party I was working for, and HD Silicon Solutions was the adverse party. And there were seven IPRs in that engagement.
Q. And approximately what time frame?
A. 2021 to 2022.
Q. Okay.
A. You want me to keep going?
Q. Yeah, why don't you keep going back until at least 2018.
A. Okay. There's only a few more to get to that time frame.
The previous one to that, I

think, is Freitas & Weinberg LLP for Aquila Innovations versus AMD, Inc., total of six IPRs, with declarations and depositions accordingly.

Prior to that was DLA Piper, representing Toyota Motor Corporation, et al., versus Broadcom. That was an ITC matter. So it was involving -- I was a testifying expert on domestic industry, my expert report, deposition and at hearing.

And prior to that were before 2018.

Q. I apologize. Could you actually go back to 2016. My mistake.

A. 2016.

So prior to that was Laurence & Phillips LLP -- IP Law LLP for Polaris versus NVIDIA, eight IPRs in that engagement, corresponding declarations and depositions.

And that's the list of my current file. I'd have to go find another file to go beyond that. That was for 2017 and 2018. Is that adequate?

Q. For now.

Why don't you go ahead and put that aside, and let me know when you're ready

for the next question.

A. I have closed that window.

Q. Dr. Przybylski, have you carefully read Netlist's '417 and '215 patents marked as Exhibit 1001 in each of the IPRs?

A. Not recently, no.

Q. But in the past?

A. It depends on what you mean by "carefully." Certainly there are aspects of it that I paid closer attention to than others, but I did read them to some degree of thoroughness.

Q. Did you read them completely?

A. I would say I scanned them completely. I read portions of them completely.

Q. Do you believe that you understand the '417 and '215 patents in these IPRs?

A. Do I understand the disclosure of the specifications? Yes, I do.

Q. Do you believe you understand the figures of the '417 and '215 patents?

A. You want me to review a specific figure?

Q. No. I'm just asking you, when you did review Netlist '417 and '215 patents in

Samsung Ex. 1095, p. 35
Samsung Electronics Co., Ltd. v. Netlist, Inc., IPR2023-00455

the past, do you believe that you understood the figures of the '417 and '215 patents?

A. With your permission, I'll pull up the '417 patent and quickly look at the figures to make sure I can answer that accurately.

Is that all right?

Q. Sure.

A. Yes, I understand the figures of the '417 and '215 patents.

Q. And do you believe that you understand the claims at the end of the '417 and '215 patents marked as Exhibit 1001 in these two IPRs?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: Yes, I understand all of the terms that are in the various elements of the claims of those two patents.

(Exhibit Number 1071 was previously marked for identification.)

BY ATTORNEY CHANDLER:

Q. Please turn to Exhibit 1071, which is the same exhibit in both IPRs, and let me know when you're there.

A. 1071. Hold on. Is that one of the ones you put in chat?
Q. You know, I thought I did, but now that I'm looking --
A. There it is. 1071, yes. I'm just going to pull it off of chat rather than trying to -- so that's Perego; right?
Q. Yes. Yes.
A. I have 7,363,422 to Perego up on one of my screens.
Q. Dr. Przybylski, have you carefully read the Perego prior art reference marked as Exhibit 1071 in both IPRs?
A. Yes.
Q. And do you believe that you understand the Perego reference marked as Exhibit 1071 in both IPRs?
A. Yes.
(Exhibit Number 1064 was previously marked for identification.)
BY ATTORNEY CHANDLER:
Q. Please turn to Exhibit 1064, which is the same in both IPRs, and let me know when you're there.
A. 1064.

Q. It should be in the chat as well.
A. Yes. Sorry. I spoke over you. I'm downloading it now.
So I have JEDEC standard JEDS79-2 from September 2003 in front of me.
Q. So, Dr. Przybylski, have you carefully read the JESD79-2 JEDEC standard from September 2003 marked as Exhibit 1064 in both IPRs?
A. Have I read all of it? No, I've never read every single word of this standard. I certainly have been familiar with it since before it was introduced, but -- and I'm very familiar with its contents; but every footnote of every figure, no.
Q. And when you say that you were familiar with it since before it was introduced, what do you mean by that?
A. The DDR2 standard was discussed in the industry prior to its being issued formally by JEDEC and the EIA. So I was aware of its imminent arrival.
Q. Were you a member of JEDEC at that time?
A. No. JEDEC's members are

companies, not individuals.

Q. And what were you doing at that time that the DDR2 standard was being discussed in the industry? Were you teaching or consulting or what were you doing?

A. I was consulting and staying current with developments in the industry generally.

Q. And if you weren't a member of JEDEC at the time and you were consulting, how did you become aware of the development of the DDR2 standard before it was finalized in September of 2003?

A. I don't know if there were press reports or not. I have no recollection of that. But certainly with -- in conversation with individuals -- again, not able to recall specific ones; but, in general, the next generation of standard SDRAMs is that its coming is -- is known within the industry, and it's not a secret process.

The deliberations are secret and the voting is within the companies, but people talk.

Q. And what type of consulting were

you doing in the early 2000s?

A. Certainly throughout the 1990s and into the 2000s, I was working with semiconductor vendors and systems companies to understand the DRAM marketplace and the changes that were happening within it across the main memory and other -- as applicable to systems that are PC servers and embedded systems.

(Exhibit Number 1073 was previously marked for identification.)

BY ATTORNEY CHANDLER:

Q. Could you please turn to Exhibit 1073, which is the same in both IPRs, and let me know when you have it up on the screen. It's in the chat for everyone's ease of reference.

A. I have U.S. Patent Application Publication US 2006/0277355 to Mark Ellsberry in front of me.

Q. Dr. Przybylski, have you carefully read the Ellsberry prior art reference marked as Exhibit 1073 in both IPRs?

A. Yes, but not recently.

Q. Do you believe that you understand the Ellsberry prior art reference

marked as Exhibit 1073 in both IPRs?
A. Yes.
(Exhibit Number 1078 was previously marked for identification.)
BY ATTORNEY CHANDLER:
Q. Please turn to Exhibit 1078, which is the same in both IPRs, and let me know when you're there. There should be a copy in the chat for everyone's ease of reference.
A. There it is.
So now I have U.S. Patent 7,024,518, to John Halbert, et al., in front of me.
Q. Dr. Przybylski, have you carefully read the Halbert prior art reference marked as Exhibit 1078 in both IPRs?
A. Yes, but not recently.
Q. Do you believe that you understand the Halbert prior art reference marked as Exhibit 1078 in both IPRs?
A. Yes.
Q. Have you known John Halbert at Intel?
A. I don't believe I've ever met him.

Q. Have you known Mark Ellsberry, the first named inventor on Exhibit 1073?

A. That name is very familiar to me. I believe I've crossed paths with him sometime in the 1990s. But, again, the context I wouldn't recall.

Q. Have you known Richard Perego, Fred Ware or Ely Tsern from Rambus, the named inventors on Exhibit 1071?

A. I've met Fred Ware on a couple of occasions. The others -- let me see. I don't believe I've met Richard Perego or Ely Tsern.

(Exhibit Number 1082 was previously marked for identification.)

BY ATTORNEY CHANDLER:

Q. Please turn to Exhibit 1082, which is the same in both IPRs, and let me know when you have it on your screen. There should be a copy in the chat for everyone's ease of reference.

A. I have U.S. Patent application publication 2003/0039151 in front of me.

Q. Dr. Przybylski, have you carefully read the Matsui prior art reference, marked as Exhibit 1082 in both IPRs?

A. Yes, but not recently.
Q. Do you believe that you understand the Matsui prior art reference marked as Exhibit 1082 in both IPRs?
A. I certainly did when I was reviewing it for the purposes of the declaration. I presume that hasn't changed since then.
(Exhibit Number 1072 was previously marked for identification.)
BY ATTORNEY CHANDLER:
Q. Please turn to Exhibit 1072, which is the same in both IPRs, and let me know when you're there.
It looks like there's a copy in the chat for everyone's convenience.
A. This is U.S. Patent 7,155,627 to Matsui. I have that in front of me.
Q. Dr. Przybylski, have you carefully read the Matsui prior art patent marked as Exhibit 1072 in both IPRs?
A. This one is less familiar to me, so it was not something I reviewed in great detail when preparing the declarations.
Q. Do you believe that you

understand the Matsui prior art patent marked as Exhibit 1072 in both IPRs?

A. I believe that if I reviewed it, again, in detail, I would be able to understand it, yes. But exactly what it's teaching, I don't have in front of mind right now.

(Exhibit Number 1079 was previously marked for identification.)

BY ATTORNEY CHANDLER:

Q. Please turn to Exhibit 1079, which is the same in both IPRs, and let me know when you have it in front of you. There is a copy of it in the chat for everyone's convenience.

A. I have in front of me U.S. Patent application publication 2006/0117152 to Amidi in front of me.

Q. Dr. Przybylski, have you carefully read the Amidi prior art reference marked as Exhibit 1079 in both IPRs?

A. I don't believe I've read it carefully. I did review it in -- briefly when preparing my declaration, but that was a while ago. I have not reviewed it recently.

Q. Do you believe that you

understand the Amidi prior art reference marked as Exhibit 1079 in both IPRs?

A. I don't recall specifically what it's teaching, but I do firmly believe that on reviewing it, I would understand it.

(Exhibit Number 1060 was previously marked for identification.)

BY ATTORNEY CHANDLER:

Q. Please turn to Exhibit 1060, which is the same in both IPRs, and let me know when you have it in front of you. There is a copy of it in the chat for everyone's convenience.

A. I have in front of me JEDEC standard, JESD79 from June 2000 related to double data rate, DDR, SDRAMs.

Q. Dr. Przybylski, have you carefully read the JESD79 standard for DDR SDRAMs dated June 2000 marked as Exhibit 1060 in both IPRs?

A. As with the previous JEDEC standard, I wouldn't say that I read every footnote of every figure, but I certainly understand the design and operation of DDR SDRAMs as specified by this standard.

Q. So to be clear, do you believe that you understand the JESD79 JEDEC standard for DDR SDRAMs dated June 2000 marked as Exhibit 1060 in both IPRs?

A. Yes.

(Exhibit Number 1062 was previously marked for identification.)

BY ATTORNEY CHANDLER:

Q. Please turn to Exhibit 1062, which is the same in both IPRs, let me know when you have it in front of you. There's a copy in the chat for everyone's convenience.

A. I have in front of me a portion of JEDEC standard now called JESD21-C, a portion totaling 82 pages, beginning at page 4.20.4-1.

Q. Dr. Przybylski, have you carefully read the JEDEC21-C prior art reference marked as Exhibit 1062 in both IPRs?

A. Again, it's pretty duplicative across the different versions of the RDIMM standard that's being specified here, so not every page has been examined carefully. But I certainly do understand the structure and operation of the RDIMMs that are specified here.

Q. So to be clear, do you believe

that you understand the JEDEC21-C prior art reference marked as Exhibit 1062 in both IPRs?

A. Yes.

ATTORNEY CHANDLER: All right. How about we -- we've been going about an hour, so how about we take a break. Go off the record.

THE WITNESS: Very good. How long?

ATTORNEY CHANDLER: Ten minutes?

THE WITNESS: Ten minutes.

THE VIDEOGRAPHER: Off the record at 9:04 a.m. Pacific Time.

(Recess taken from 9:04 a.m. to 9:16 a.m.)

THE VIDEOGRAPHER: On the record at 9:16 a.m. Pacific Time.

BY ATTORNEY CHANDLER:

Q. Dr. Przybylski, are there any corrections or clarifications you'd like to make to your answers so far?

A. Not at this time.

Q. And just to confirm, during the break, did you consult with anyone?

A. Mr. Warrick called me just to

make sure everything was going smoothly on my end. I said "yes," and that was the extent of the call.

Q. Understood.

And are you ready to proceed?

A. I am.

Q. Dr. Przybylski, I'd like to ask you some questions about the hypothetical person of ordinary skill in the art, starting with the relevant time frame for such a person.

So do you have that in mind? And then I'll ask you some more specific questions.

A. So I'm turning to page 46 of my declaration for the '417, where that subject matter is addressed.

Q. That's fine. And I think as shown in Exhibit 1096, this section of your declaration is the same in both IPRs. But go ahead and get oriented and let me know when you're ready to proceed.

A. Yes, I see those sections are essentially the same within the two declarations; and I have, as I said, the '417 in front of me.

Q. In the section that you are

referring to in your two expert declarations marked as Exhibit 2024 are paragraphs 66 through 72 where you discuss the person of ordinary skill in the art; correct?

A. Yes. Those are the paragraphs relating to that topic.

Q. Now, Samsung's expert, Dr. Wolfe, has taken the position that the effective filing date for the '417 and '215 patents is no earlier than July 1st, 2005.

I understand that you contend that the claims in the '417 and '215 patents are entitled to a priority date of at least January 19th, 2005, which is the filing date of the '087 provisional application; but in paragraph 72 of your expert declarations marked as Exhibit 2024, you refer to the 2004 to 2005 time frame when discussing the person of ordinary skill in the art.

Do you see that?

A. I see paragraph 72 begins. I note that in the 2024-2025 time frame, et cetera, yes.

Q. To be clear, it's not 2024-2025.

A. I'm sorry.

Q. 2004 through 2005.
A. My apologies. Yes, 2004 to 2005.
Q. Okay. Unless stated otherwise, can you please answer my questions today from the perspective of a person of ordinary skill in the art in the 2004 to 2005 time frame?
ATTORNEY WARRICK: Objection; form.
THE WITNESS: To the best of my ability, I will try to be clear, about the perspective from which I'm answering your questions.
BY ATTORNEY CHANDLER:
Q. And just so I'm clear, the -- please understand that my questions are intended to be asked with respect to the person of ordinary skill in the art in the 2004 to 2005 time frame.
Understood?
A. I understand.
ATTORNEY WARRICK: Objection; form.
Counsel, Dr. Przybylski is here as an expert, which is his role in these proceedings; and so I would ask that you be

specific if you're going to ask him about the perspective of the hypothetical person of ordinary skill in the art.

BY ATTORNEY CHANDLER:

Q. Dr. Przybylski, did you answer my question by saying, "I understand"? Did I hear that correctly?

A. Yes, I understand that that's the perspective on which you will generally be asking questions, but not -- not necessarily all questions.

ATTORNEY CHANDLER: And, Mr. Warrick, I would like to remind you that on pages 127 to 130 of the Consolidated Trial Practice Guide dated November 2019, speaking objections are strictly prohibited.

Understood?

ATTORNEY WARRICK: I am familiar with the Practice Guide.

BY ATTORNEY CHANDLER:

Q. Dr. Przybylski, could you please answer my questions today in a way that is consistent with the ordinary and accustomed meaning of words to a person of ordinary skill in the art in the 2004 to 2005 time frame?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: I would endeavor to do that or to be clear when I'm not doing that, to the best of my ability.

BY ATTORNEY CHANDLER:

Q. Could you please turn toward the beginning of your expert declaration marked as Exhibit 2024 to the section titled "Technology Background," which spans paragraphs 12 through 57, and let me know when you're there.

And while you're doing that, I'll note that Exhibit 1096 indicates that the substance of paragraphs 12 through 57 is substantially the same in both of your expert declarations.

A. Yes. I see that there are some differences between those -- in those paragraphs between those declarations, but they do not have a great deal of substance to them.

I am currently looking at page 7 of my '417 declaration.

Q. And paragraphs 12 through 57 of your expert declarations marked as Exhibit 2024 provide a technology background for purposes of

these IPRs?

A. That is the heading for this section, "Technology Background," yes.

Q. In your opinion, are the background technologies summarized in paragraphs 12 through 57 of your expert declaration marked as Exhibit 2024 something that a person of ordinary skill in the art would have known about?

A. Yes, I think generally that is an accurate statement.

Q. In your opinion, would a person of ordinary skill in the art reading the contents of the Perego reference, marked as Exhibit 1071, have known about the background technologies summarized in paragraphs 12 through 57 of your expert declarations marked as Exhibit 2024?

A. I think I answered the previous question by saying that, yes, a person of ordinary skill in that time frame would be familiar with this material, regardless of whether they're reading Perego or not.

Q. In your opinion, would such a person of ordinary skill in the art have taken

into consideration the background technologies summarized in paragraphs 12 through 57 of your expert declaration marked as Exhibit 2024 when trying to understand the contents of the Perego reference marked as Exhibit 1071?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: I'm not sure what you mean by "taking into account." It's -- this background technology that I refer to is something that a person of ordinary skill would be familiar with while reading Perego or otherwise. To the extent that they're taking any of it in particular into account, I'm not -- have not rendered an opinion on that.

BY ATTORNEY CHANDLER:

Q. In your opinion, would a person of ordinary skill in the art have taken into consideration the background technologies summarized in paragraphs 12 through 57 of your expert declaration marked as Exhibit 2024 when trying to understand the contents of the '417 and '215 patent applications?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: Again, this background material is something that a person of ordinary skill would have been generally familiar with. I do not know specifically what aspects of that they would necessarily have to call on in order to understand the patents at issue here.

BY ATTORNEY CHANDLER:

Q. In your opinion, is the technology background summarized in paragraphs 12 through 57 of your expert declaration marked as Exhibit 2024 relevant to the field of art for the '417 and '215 patents?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: The technology background is there principally to help the board understand the technologies at issue here. They do -- the content of that section does generally relate to the subject matter of the '417 and the '215 and the prior art references cited by the petitions.

Beyond that, I have nothing further to add.

///

BY ATTORNEY CHANDLER:

Q. Please turn to paragraph 32 of your expert declarations marked as Exhibit 2024. Let me know when you're there.

And while you're doing that, I'll note that Exhibit 1096 indicates that the substance of paragraph 32 is the same in both of your expert declarations.

A. I am at paragraph 32.

Q. In paragraph 32 of your expert declarations marked as Exhibit 2024, you referred to DIMMs, UDIMMs and RDIMMs; correct?

A. I don't actually call them RDIMMs. I called them registered DIMMs at the top of page 23 of my '417 declaration.

But that minutia apart, that is generally true. I referred to DIMMs, UDIMMs or unbuffered DIMMs and registered DIMMs in that paragraph.

Q. And to be clear, registered DIMMs are commonly referred to by persons of ordinary skill in the art as RDIMMs; correct?

A. Yes. There are many acronyms that are very similar in this whole art, but RDIMM is one that is principally used to refer

to JEDEC standardized, registered DIMMs.

Q. In your opinion, would a person of ordinary skill in the art have known about DIMMs, UDIMMs and RDIMMs?

A. Yes. It's within the scope of knowledge or familiarity of a person of ordinary skill to at least be familiar with those types of memories and, generally speaking, what they are about.

Q. And could you pull up the '417 and '215 patents marked as Exhibit 1001. And in the '417 patent, go to Column 6 starting around line 46. And let me know, and I'll point you to the similar location in the other patent.

A. All right. So I have the '417 up, Column 6.

Do you want me to talk about this first, or do you want me to bring up the other one in parallel?

Q. I'll -- let's bring up the other one in parallel because the specifications of the two patents are the same, so I want to cover both patents at the same time.

A. Sure.

Q. So in the '215 patent, the

corresponding text starts at Column 5, line 66.

A. Give me a second to bring that one up, please.

Did you put the '215 in chat? I didn't believe we actually pulled that one down?

Oh, I see. They're both there. That's the '417. That's the '215. Okay.

Q. So do you have in front of you the '417 patent, Column 6, line 46, and then also '215 patent at Column 5, line 66?

A. Just getting there with respect to the '215. Half a second more.

Yes, I have both of them up in front of me now.

Q. And the '417 and '215 patents both refer to DIMMs, UDIMMs and RDIMMs; correct?

A. Among others, yes.

Q. The '417 and '215 patents also refer to other types of memory modules, such as SO-DIMMs, FB-DIMMs, and RBDIMMs; correct?

A. Yes, they do.

Q. In your opinion, would a person of ordinary skill in the art have known about SO-DIMMs, FB-DIMMs and RBDIMMs?

A. SO-DIMMs, certainly. They were

relatively common and important. FB-DIMMs are much rarer and would -- a POSITA in that time frame might not have had any familiarity with FB-DIMMs as a course of their employment.

Similarly, RBDIMMs are -- I'm not familiar exactly with what that is referring to. It's not a JEDEC standardized DIMM, so -- that I'm familiar with.

Q. So if I understand correctly, SO-DIMMs and FB-DIMMs were known, but SO-DIMMs were more widely known than FB-DIMMs? Would that be fair?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: That's not quite what I said. I think that a POSITA in 2004-2005 would not necessarily have had any exposure to FB-DIMMs. They would have had some exposure, most likely, with SO-DIMMs.

I'm not even familiar when the FB-DIMMs were formally standardized. I think it was after this time frame. I'm not sure.

BY ATTORNEY CHANDLER:

Q. The inventors of the '417 and '215 patents knew about FB-DIMMs; correct? They

put it in their patent application.
ATTORNEY WARRICK: Objection; form.
THE WITNESS: Yes, they did mention them in Columns 5 and 6 respectively. But, again, what I said is I don't know formally when those standards were issued by JEDEC.
BY ATTORNEY CHANDLER:
Q. Were SO-DIMMs and FB-DIMMs known by the time of the '417 and '215 patents, regardless of whether JEDEC had formally issued standards for them?
ATTORNEY WARRICK: Objection; form.
THE WITNESS: In the time frame 2004-2005, I don't know whether they were known -- FB-DIMMs were known at that time or not.
BY ATTORNEY CHANDLER:
Q. But they were known to the inventors?
ATTORNEY WARRICK: Objection to form.
THE WITNESS: I don't know at what point in the prosecution history those

particular references were added to the specification or whether it was a result of a -- the initial filings or whether those particular references were added later. I'm just not familiar.

BY ATTORNEY CHANDLER:

Q. Do you have patents yourself?

A. Yes.

Q. And you understand that once a patent application is filed, it's not permitted to add to the patent specification; correct?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: There are provisional applications from which priority is given; and then there are the full, nonprovisional applications that are a more complete description of the subject matter of the invention. So there is a clear difference between those two, at least.

BY ATTORNEY CHANDLER:

Q. You provided the opinion that the '417 and '215 patents are entitled to a priority date of January 19th, 2005.

As of that date, January 19th,

2005, in your opinion, do the claims of the '417 and '215 patents cover memory modules that are either SO-DIMMs or FB-DIMMs?

ATTORNEY WARRICK: Objection; form.

BY ATTORNEY CHANDLER:

Q. Or do you not know?

A. Whether -- by "covered," do you mean that those types of modules infringe those claims? Is that what you're meaning?

Q. Well, it's usually, rather than the word "infringe," we would say are "embodiments." So could an SO-DIMM or an FB-DIMM embody the claims of the '417 and '215 patents as of January 19th, 2005, the date that you say the claims are entitled to a priority date of?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: That's not a terminology that I'm familiar with. I think that it -- the way that it would normally be expressed is: Are those types of modules within the scope of the claims at issue? And that's not a subject of my opinions in this matter.

BY ATTORNEY CHANDLER:

Q. It's a little bit different, so I want to just be clear about this.

So when you provided the opinion that the claims were entitled to a priority date of January 19th of 2005, you were indicating that there was support in the specification for those claims.

And my question is: Is there support in the specification for the claims of the '417 and '215 patents, as of January 19th, 2005, with respect to an SO-DIMM or an FB-DIMM that practices the claims or embodies the claims?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: That's not something I've opined on, and I don't know that off the top of my head, sitting here today.

ATTORNEY CHANDLER: I'd like to introduce a new exhibit in the chat, which I'll mark as Exhibit 1103.

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(Whereupon, Exhibit Number 1103 in both IPRs was marked for identification and is attached hereto.)

BY ATTORNEY CHANDLER:

Q. It should be coming to everyone. It's the same document in both IPRs. I've provided two copies. The only difference in the two copies is the case number in the stamp in the bottom right.

Please let me know when you have Exhibit 1103 in front of you.

A. I have Netlist Technology Tutorial dated May 8th, 2017.

Q. Correct. Exhibit 1103 is the technology tutorial prepared by Netlist.

Have you seen Exhibit 1103 before?

A. I've seen the cover page before. I have not reviewed it in detail, no.

Q. Please turn to page 2 of Exhibit 1103, and let me know when you're there.

A. I am at page 2.

Q. Does page 2 of Exhibit 1103 show a picture of a DIMM, which is to say a dual in-line memory module?

A. It appears to show a memory module that it's claiming is a DIMM. It's not clear whether that's a JEDEC standardized DIMM. It appears not to be, but I don't know for a fact one way or the other. It has the right form factor to be a considered a DIMM in the most general understanding of that term.

Q. Does page 3 of Exhibit 1103 show a DIMM memory module at the bottom?

A. Yes. This appears to be a Samsung-manufactured DIMM. It looks like an RDIMM, but I don't know for a fact. I'd have to look up the product numbers to be sure exactly what it is.

Q. Do you agree that SDRAM memory devices emerged in the 1990s and have been standardized by JEDEC?

A. Have to be careful with regard to the term "SDRAM," because sometimes it's referring just to any variety of synchronous DRAM. So synchronous with a small s.

If it's a JEDEC standardized device, it's all caps, and the S is standing for synchronous with a capital S. And those are the devices that are standardized by JEDEC.

There are a great many nonstandardized, small s, synchronous, dynamic random-access memories that are not covered by JEDEC standards.

Q. Do you agree that SDRAM, all caps, has evolved in several generations, including DDR and DDR2?

ATTORNEY WARRICK: Objection; form; also scope as to the question and as to the exhibit, 1103.

THE WITNESS: Yes. There are -- have been a number of SDRAM standards developed by JEDEC, one of which is called DDR SDRAM, short for double data rate synchronous dynamic random-access memory, as well DDR2 and so forth.

ATTORNEY CHANDLER: And I'll note for the court reporter, I said D -- as in dog.

(Incidental comments made off the stenographic record.)

THE WITNESS: We'll be saying "DDR" a lot.

BY ATTORNEY CHANDLER:

Q. Dr. Przybylski, DDR and DDR2 were JEDEC standards that a person of ordinary skill in the art knew about by the time of the '417

and '215 patents; correct?

A. Again, you have to be careful with the terminology, because DDR, standing for double data rate, applies to many different contexts. To be clear that you're talking about the JEDEC standard, you should say DDR SDRAM JEDEC standard.

Q. So to be clear, the DDR SDRAM JEDEC standard and DDR2 SDRAM JEDEC standard were known to a person of ordinary skill in the art by the time of the '417 and '215 patents; correct?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: Yes. We looked at JEDEC standardizing documents that predate the 2004-2005 time frame that we're talking about and so that they -- a POSITA in that time frame would have been familiar with them.

BY ATTORNEY CHANDLER:

Q. For example, please turn back to Exhibit 1060, the JEDEC JESD79 standard for DDR SDRAM dated June 2000. Let me know when you have it in front of you.

A. I have the cover page of that in

front of me.

Q. You do not dispute that a person of ordinary skill in the art would have known about the JEDEC JESD79 standard for DDR SDRAM dated June 2000 marked as Exhibit 1060 in both IPRs; correct?

ATTORNEY WARRICK: Objection to form.

THE WITNESS: I do not dispute that.

BY ATTORNEY CHANDLER:

Q. And please turn to Exhibit 1062. Let me know when you have that in front of you.

A. I have the first page of Exhibit 1062 in front of me.

Q. You do not dispute that a person of ordinary skill in the art would have known about the JEDEC JESD21-C design specification for DDR SDRAM registered DIMM dated January 2002 marked as Exhibit 1062 in both IPRs; correct?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: Again, you have to be careful with terminology, because the JEDEC Standard 21-C is about 3,000 pages in total.

What this exhibit is, is one small portion of that overall standard, the design specification for PC2100 and PC1600 DDR SDRAM registered DIMMs dated January 2002.

BY ATTORNEY CHANDLER:

Q. And you do not dispute that a person of ordinary skill in the art would have known about that, which is marked as Exhibit 1062 in both IPRs; correct?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: I do not dispute that.

BY ATTORNEY CHANDLER:

Q. Please turn to Exhibit 1064. Let me know when you have it in front of you.

A. I have the first page of the JEDEC standard JESD79-2 for DDR2 SDRAM specification dated September 2003 in front of me.

Q. And you do not dispute that a person of ordinary skill in the art would have known about that standard, which is marked as Exhibit 1064 in both IPRs; correct?

ATTORNEY WARRICK: Objection;

form.

THE WITNESS: I do not dispute that.

(Exhibit Number 2020 was previously marked for identification.)

BY ATTORNEY CHANDLER:

Q. Take a look at Exhibit 2020, which I'll put in the chat. It was previously marked by Netlist, but I'll try to put it in the chat for everyone's ease of reference. It's the same exhibit in both IPRs. And let me know when you have it.

A. It has not shown up for me yet.

Oh, 2020, here we go.

I have in front of me the first page of Exhibit 2020 titled "JEDEC Standard for DDR2 SDRAM Specification," Standard Number JESD79-2B, dated January 2005.

Q. And you do not dispute that a person of ordinary skill in the art would have known about that JEDEC standard marked as Exhibit 2020 in both IPRs; correct?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: This standard was

publicized in 2005. The time frame that we're generally discussing is 2004-2005. So certainly by the end of that time frame, this particular revision of the JESD79-2 standard would have become into the general knowledge of a POSITA at that time -- in that time frame.

(Exhibit Number 2031 was previously marked for identification.)

BY ATTORNEY CHANDLER:

Q. Please take a look at Exhibit 2031 that you cited in your declaration. And I'll also put a copy in the chat for ease of reference. It's the same exhibit in both IPRs. Let me know when you have it in front of you.

A. Downloading now.

Okay. I'm looking at JEDEC Standard Number 21-C, page 4 dash -- sorry -- page 4.1.2.10-1. The first page of "Appendix X: Specific SPDs for DDR2 SDRAMs."

Q. And you cited Exhibit 2031 in your declarations marked as Exhibit 2024; correct?

A. Yes. I see at least one reference to Exhibit 2031 on page 46 of my '417 declaration.

Q. And you do not dispute that a person of ordinary skill in the art would have known about the JEDEC standard for specific SPDs for DDR2 SDRAM, marked as Exhibit 2031 in both IPRs; correct?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: This standard was made public with Release 13 of JEDEC Standard 21-C. There's no specific date on it that I see at the top. So without referring specifically to the release notes for Release 13, can't say precisely when this becomes into the public domain.

We may be able to determine that from looking at the standard for the DIMM that you're saying with the DDR2 SDRAM DIMMs and see if it refers to this particular standard.

BY ATTORNEY CHANDLER:

Q. And did you review the standard for DDR2 DIMMs -- you just referred -- I'm trying to understand.

Did you review the standard that you just referred to in your last answer?

A. In my last answer, I referred

generically to DDR2 SDRAM DIMM standards, of which there are several; and I didn't refer to any one in particular.

Q. Explain your last answer a little bit more, then.

A. I'm sorry. Was that a question?

Q. Yes. Could you please clarify what you were trying to convey with your last answer, then.

ATTORNEY WARRICK: Objection; form.

THE WITNESS: My last answer was the one where I was referring to the plurality of DDR2 SDRAM DIMM standards. Is that the question that you want me to clarify -- the answer that you want me to clarify? I'm really quite confused at this point.

BY ATTORNEY CHANDLER:

Q. I was just trying to understand what you were trying to convey with respect to my question of whether a person of ordinary skill in the art would have known about Exhibit 2031, which you cited in your expert declarations.

ATTORNEY WARRICK: Objection;

form.

THE WITNESS: My first answer with regard to that is that we don't have in front of us documentation of when Release 13 was made public. So we can't say with certainty whether a POSITA of the 2004-2005 time frame would have access to this particular Appendix X.

BY ATTORNEY CHANDLER:

Q. I guess I'm a little confused, then. Why were you citing Exhibit 2031 in your expert declarations marked as Exhibit 2024?

And the related question is: Do you believe a person of ordinary skill in the art would know about Exhibit 2031?

(Interruption by the court reporter to clarify the record.)

BY ATTORNEY CHANDLER:

Q. And a related question is: Do you believe a person of ordinary skill in the art would have known about Exhibit 2031?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: So there's two questions pending. Can we deal with one at a time, please.

BY ATTORNEY CHANDLER:

Q. Sure.

A. So with regard to my citation to Exhibit 2023 --

Q. No. 2031.

A. 2031 -- oh, I'm sorry. Yes. My apologies. Look at the wrong thing.

2031.

I at least refer to it in the -- in context of paragraph 65 of my '417 declaration where I'm using it to support the idea that the Court's construction of rank is not consistent with the plain and ordinary meaning, as captured by this section of JESD21-C.

Q. And you cite Exhibit 2031 elsewhere in your declaration as well; correct?

A. I'm checking.

I see a reference to that exhibit in paragraph 182.

Q. And also the next paragraph as well; right?

A. Yes, but not by number there; in paragraph 183, yes.

Q. So getting back to my original

question, in your opinion would a person of ordinary skill in the art have known about the JEDEC standard marked as Exhibit 2031 in both IPRs?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: I believe that a person of ordinary skill would be familiar with generally the concept of SPDs, determining -- or helping the memory controller understand the nature and characteristics of the module it's controlling.

I, again, I don't have a specific date in front of me for this particular revision. So without that, can't know for sure whether it falls within the specified time frame or not.

BY ATTORNEY CHANDLER:

Q. But at least when you were preparing your expert declarations marked as Exhibit 2024, you thought that it was reasonable to cite to Exhibit 2031 for purposes of claim construction of the '417 and '215 patents and also for purposes of understanding the Perego prior art reference; correct?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: I did, in fact, cite to this document in both those portions of my declaration, yes.

(Whereupon, Exhibit Number 1104 in both IPRs was marked for identification and is attached hereto.)

ATTORNEY CHANDLER: I'd like to mark a new exhibit, which will be Exhibit 1104, same document in both IPRs, only difference being the case number stamped in the bottom right. I'll put copies of Exhibit 1104 in the chat.

Again, the two copies are the same, so you're welcome to open either one. Just let me know when you have it on your screen.

THE WITNESS: I am looking at the cover page of "JEDEC Standard, JESD79D" from January 2004, "Double Data Rate (DDR), SDRAM Specification."

BY ATTORNEY CHANDLER:

Q. And you do not dispute that a person of ordinary skill in the art would have

known about the JESD79D standard for DDR SDRAM marked as Exhibit 1104 in both IPRs; correct?

ATTORNEY WARRICK: Objection; form. Also objection; scope, as to the question and the exhibit, 1104.

THE WITNESS: No, I don't dispute that. We've already seen JESD79 from the year 2000, if I remember correctly. And this is just a revision of that original specification standard.

BY ATTORNEY CHANDLER:

Q. And, in fact, if you search the '417 and '215 patents for "79D," you'll see the patents incorporate by reference the JEDEC standard JESD79D, which I've now marked as Exhibit 1104; correct?

A. I don't know that off the top of my head. If you want to point me to a column and line number, then we can confirm that.

Q. Sure. The fastest thing is just search for "79D"; or if you want to scroll, go to Column 23 of the '417 patent, line 52; or you can go to Column 21 of the '215 patent, line 37 or so.

A. Yes. At least in the '417, it's

incorporated by reference, as you said.

Q. And also the '215 patent, Column 21, line 37, 38, around there? The JESD79D standards incorporate by reference the same standard that I marked as Exhibit 1104; correct?

A. I will make a note that the specification of the '417 and, presumably, the '215 have the date wrong for that particular standard. They show it as February of 2004. But on the cover sheet, it -- it's listed as January. So I don't know why that error is there, but just noting it for the record.

(Whereupon, Exhibit Number 1106 in both IPRs was marked for identification and is attached hereto.)

ATTORNEY CHANDLER: Let me mark another exhibit. It will be 1106. Again, it will be the same document in both IPRs, the only difference being the case number that's stamped in the bottom right. I've put both copies of Exhibit 1106 in the chat.

BY ATTORNEY CHANDLER:

Q. Please let me know when you have Exhibit 1106 open.

A. I am looking at JEDEC Standard 21-C, page 4.1.2.4-1, which is the first page of Appendix D of that -- of some larger portion of that standard.

Q. And Exhibit 1106 is similar to Exhibit 2031 that we looked at earlier and that you cited in your expert declarations; however, Exhibit 1106 is for DDR SDRAM; whereas, Exhibit 2031 that you cited is for DDR2 SDRAM; correct?

ATTORNEY WARRICK: Objection; form. Also, objection; scope as to the question and the exhibit, 1106.

THE WITNESS: Can you repeat the question, please. I lost it in the objection.

BY ATTORNEY CHANDLER:

Q. Exhibit 1106 is similar to Exhibit 2031 that we looked at earlier and that you cited in your expert declaration; however, Exhibit 1106 is for DDR SDRAM; whereas, Exhibit 2031 that you cite is for DDR2 SDRAM; correct?

ATTORNEY WARRICK: Same objections.

THE WITNESS: These two documents

Samsung Ex. 1095, p. 80
Samsung Electronics Co., Ltd. v. Netlist, Inc., IPR2023-00455

are, in fact, similar. They have -- principally consist of a table with similar but not identical elements within them, or at least the name has changed over time. But -- yeah, so you're correct in that they are similar.

BY ATTORNEY CHANDLER:

Q. And both the '417 and '215 patents refer to the SPD, which refers to serial presence detect; correct? For example, the bottom of Column 19 of the '417 patent and the bottom half of Column 17 of the '215 patent.

A. Yes. I see in the '417 Column 19, starting at line 56, that memory modules typically include a serial presence detect device 240; and then it goes on to describe how it's effected and what it characterizes.

Q. And there's a corresponding disclosure in the '215 patent starting in the middle of Column 17 and carrying over to the next column; correct?

A. 17.

Yes, the disclosures appear to be identical.

Q. In the discussion of the SPD in

the '417 and '215 patents, there's reference to various bytes, such as byte 3, defining the number of row address bits, byte 4, defining the number of column address bits, et cetera; is that correct?

A. Yes. That's how it's described in the specification of the '417 and '215.

Q. And Exhibit 1106 provides the -- the corresponding information about those bytes; correct?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: Byte 3 --

(Witness reviews document.)

So there are some differences between how the fields of the SPD are described in the specifications of the '417 and '215 relative to their textual descriptions in Exhibit 1106. But there -- at least to the extent that I've reviewed, they are referring to the same general concepts.

Good time for another break?

BY ATTORNEY CHANDLER:

Q. Almost.

Do you believe a person of

ordinary skill in the art would be familiar with the --

A. I'm sorry.

Q. Do you believe a person of ordinary skill in the art would be familiar with Exhibit 1106 in both IPRs?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: Well, again, we don't have a date related to Release 11 of JEDEC Standard 21-C, which would clarify exactly when this became into the public domain; but it is highly likely that a POSITA, as of 2004-2005, would be familiar with at least the existence, if not the details, of Exhibit 1106.

ATTORNEY CHANDLER: Why don't we go ahead and take a break.

THE WITNESS: Very good. Ten minutes again?

ATTORNEY CHANDLER: Sure.

THE VIDEOGRAPHER: Off the record at 10:17 a.m. Pacific Time.

(Recess taken from 10:17 a.m. to 10:28 a.m.)

THE VIDEOGRAPHER: On the record

at 10:28 a.m. Pacific Time.
BY ATTORNEY CHANDLER:
Q. Please turn to page 4 of Exhibit 1103, and let me know when you're there.
A. 1103. We're referring back to the tutorial; correct?
Q. Yes.
A. And page 4?
Q. Yes.
A. "SDRAM Fundamentals"; correct?
Q. Yes.
A. Very good.
Q. Do you agree that a given SDRAM memory device contains several sections called banks, with a B, as in boy?
ATTORNEY WARRICK: Objection; form, scope.
THE WITNESS: You're referring specifically to JEDEC standardized SDRAMs?
BY ATTORNEY CHANDLER:
Q. As an example, yes.
ATTORNEY WARRICK: Same objections.
THE WITNESS: Yes, JEDEC standardized SDRAMs include sections called

banks.
BY ATTORNEY CHANDLER:
Q. With a B, as in boy; correct?
A. Correct.
Q. And do you agree that each bank with an SDRAM memory device consists of rows and columns of memory?
ATTORNEY WARRICK: Objection; form, scope.
THE WITNESS: Yes, generally speaking, DRAMs are logically organized into banks containing rows and columns.
BY ATTORNEY CHANDLER:
Q. Do you believe a person of ordinary skill in the art would have known what is shown here on page 4 of Exhibit 1103?
ATTORNEY WARRICK: Objection; form, scope.
THE WITNESS: In the time frame we're talking about, 2004-2005, I believe that a POSITA would generally be familiar with the internal logical structure of DRAMs generally and JEDEC standardized SDRAMs in particular.
BY ATTORNEY CHANDLER:
Q. And you used the term "POSITA,"

Samsung Ex. 1095, p. 85
Samsung Electronics Co., Ltd. v. Netlist, Inc., IPR2023-00455

which is an abbreviation for a person of ordinary skill in the art; correct?

A. Are you okay with my using the acronym?

Q. I am. I just want to make clear that we're referring to the same thing.

A. Yes, we are.

Q. Turning to page 5 of Exhibit 1103 -- let me know when you have that in front of you.

A. Page 5, yes.

Q. Do you agree that a rank, with an R, is a set of DRAMs that are written to or read from together?

ATTORNEY WARRICK: Objection; form, scope.

THE WITNESS: That's not one of the constructions that's being considered in this particular set of IPRs, but it's a colloquial understanding for the purposes of this technology overview.

In the context of DIMM that's shown in the bottom half of that figure, it illustrates two ranks of memory devices that are, in fact, read or written together.

BY ATTORNEY CHANDLER:

Q. Is it common for a rank of memory devices to be written to or read from together?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: It's -- yes, it's common that that is how the DRAMs in a rank are used. It is not exclusively how they're used, in particular with regard to certain memory structures. Certain DIMM types, you could have partial rank reads and writes.

BY ATTORNEY CHANDLER:

Q. Could you explain that a little bit more, what you're referring to.

A. If you wish to write less than 64 bits at a time -- in other words, to only involve a subset of the DRAMs in a rank -- you can do that. There are mechanisms in place within the JEDEC standardized DIMMs in particular. And so you can write them all together, but you don't have to.

Q. And at a high level, what is the mechanism that you're referring to in the JEDEC standard that permits writing to less than the full rank of memory devices?

A. The way it's implemented within the JEDEC standardized DRAMs and DIMMs, there is a write mask feature that facilitates that functionality.

Q. When the write mask feature is being used, would it still be common to refer to all of the DRAMs that together form the width of the memory module to refer to those as a rank, even if in a given write operation, the mask results in only a subset of those DRAMs being written to?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: Yes, because the JEDEC standard -- certain -- certain of the JEDEC standards refer to those collections of DRAMs as "ranks." So a POSITA looking to the standard for the meaning of the terminology in that context, those collections of 8 DRAMs are referred to formally as a rank in that context.

BY ATTORNEY CHANDLER:

Q. In the example where a mask is being used as part of a write command such that only a subset of the memory devices in a rank actually write the data to memory, am I correct

that all of the memory devices in the rank receive the write command; but in addition to that, there's a subset of the memory devices that receive the mask, and it's the mask that results in only a subset of the memory devices in the rank actually writing the data to memory? Is that a generally fair description?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: Generally speaking, in the context of the JEDEC standardized SDRAMs and the DIMMs that use them, that is an accurate description of how partial word writes are implemented.

BY ATTORNEY CHANDLER:

Q. Do you agree that a rank of DRAMs share all of the command and address input signals, including the chip-select signal?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: Again, within the scope of these JEDEC standardized SDRAMs and module types, that is accurate, again, in that context.

///

BY ATTORNEY CHANDLER:

Q. And that context would include the JEDEC standard for DDR SDRAM and DDR2 SDRAM; correct?

A. We would have to look at specific module types -- there are actually a great many different types of DDR2 SDRAM modules. I'm not sure all of them implement partial word reads and writes in that same fashion.

This particular picture shows a -- what would be called a UDIMM. And in the context of a UDIMM, that is accurate.

Q. Is it also accurate in the context of an RDIMM?

A. Okay. So I've lost track of what the original thing we're talking about is. So could you repeat the question with the preamble.

Q. Do you agree that a rank of DDR SDRAMs, whether in an UDIMM or an RDIMM, share all of the same command and address input signals, including the chip-select signal?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: So the question changed from DDR2 to DDR. Is your intent to ask

Samsung Ex. 1095, p. 90
Samsung Electronics Co., Ltd. v. Netlist, Inc., IPR2023-00455

about DDR?
BY ATTORNEY CHANDLER:
Q. We can start with DDR1 SDRAM, but I'm also interested in DDR2 SDRAM to the extent you think there's a difference in the answer to my question.
A. Okay. And just as an aside, with regard to terminology, there's really no such thing as DDR1. It is an error that some people persist in using. But the standards are DDR, DDR2 and so forth.
Anyways, so let's --
Okay. So looking at Exhibit 1062, which is the DDR SDRAM RDIMM standard, Version 1.3, January 2002, we see that -- for example, on page 11, we have the -- the commands going to all of the devices and the single chip-select, which is S0 going into the register and chip-select RS0 becoming chip-select going to the SDRAM.
So in this particular module, for example, that your statement is accurate.
Q. And for clarity, you were looking at the register on the bottom left of page 11 of Exhibit 1062; is that correct?

A. Yes. That is the register that gives the registered DIMM its name.

Q. Could you turn back to Exhibit 1103, page 5, and let me know when you have it in front of you.

A. I am back at page 5, yes.

Q. Do you agree that the DRAMs in a rank will respond to commands together and provide data to the full width of the module?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: So each of the DRAMs respond to their command and chip-select signals. To the extent that a particular memory module has those signals shared amongst all of the DRAMs in a rank, then that would be true.

Your language is a little bit imprecise, because togetherness implies a temporal togetherness; and that's not always the case with regard to, in particular, later iterations of JEDEC standardized DIMMs.

BY ATTORNEY CHANDLER:

Q. And when you are talking about later iterations of JEDEC standardized DIMMs, are you talking about after 2005?

A. Yes. They would be after 2005.

Q. So to be clear, again, just for clarity, in general, my questions are intended to be asked with respect to the time frame 2004-2005, from the perspective of a person of ordinary skill in the art.

Understood?

A. Understood, yes.

So with regard to the DDR2 SDRAM-based DIMMs that are standardized by JEDEC, the DRAMs on the DIMM within a single rank are operating slightly out of phase with each other, but not substantially so that it is an issue for the lower frequencies that are at play in that generation of memories and modules.

Q. On page 5 of Exhibit 1103, do you see the last bullet point says, "Need 8 DRAMs in a rank to provide the 64 bits at once"?

A. I see that bullet.

Q. Do you believe that statement is generally accurate, taking into account that the time frame of "at once" may not be precisely at once down to the zillionth of a second, but would be "at once" given the clock frequencies of the memory modules of the day?

ATTORNEY WARRICK: Objection; form, scope.

THE WITNESS: Yes. It is a tutorial and, thus, speaks in generalities. And so I do not take exception with what the bullet point is trying to teach.

BY ATTORNEY CHANDLER:

Q. Now, in your expert declarations marked as Exhibit 2004, you have offered the opinion that the term "rank," with an R, requires more than one memory device; correct?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: In my paragraph 61 of the declaration for the '417, I say that Netlist, in contrast, proposed that a rank is a predetermined group of memory devices on a memory module that can send or receive a fixed number of data bits via a fixed-width data bus in response to read or write commands and independently from other memory devices on the memory module.

That is -- there are, in fact, three different proposed constructions at play here, and that is the one that Netlist has

proposed.
BY ATTORNEY CHANDLER:
Q. And do you agree with Netlist's proposed construction --
A. It's not --
Q. -- for the term "rank," with an R?
A. It's a fine construction. I've been asked to apply it in this declaration, and I have done so.
Q. In the context of the '417 and '215 patents, in your opinion, does the term "rank," with an R, require more than one memory device to be in the rank?
ATTORNEY WARRICK: Objection; form, scope.
THE WITNESS: Give me a second.
(Witness reviews document.)
In the context of at least the '417, the ranks as they are claimed require a plurality of memory devices within an N-bit-wide rank.
BY ATTORNEY CHANDLER:
Q. What about the context of the '215 patent?

ATTORNEY WARRICK: Same objections.

THE WITNESS: Too many PDFs open.

(Witness reviews document.)

In the context of the '215, the plurality of ranks that are claimed in Claim 1 require at least one memory device in each rank.

With regards to the construction that Netlist is proposing, that would still require a plurality of memory devices that -- in the rank.

BY ATTORNEY CHANDLER:

Q. In your opinion, in the context of the '215 patent, can a rank, with an R, include just one memory device?

ATTORNEY WARRICK: Objection; form, scope.

THE WITNESS: Not according to the construction proposed by Netlist.

BY ATTORNEY CHANDLER:

Q. And that was not my question. My question is whether, in your opinion, in the context of the '215 patent, can a rank, with an R, include just one memory device?

ATTORNEY WARRICK: Same

objections.

THE WITNESS: In my opinion, the term "rank" is used and misused in a variety of different ways and a variety of different contexts, both in the time frame 2004-2005 in particular, since it was still a -- the term was only a decade old at that time. And so there is -- without the benefit of a proposed construction, it's difficult to say what a POSITA would have understood in that time frame as whether or not it's limited to one or two -- whether -- I'm sorry -- whether a rank can have a single memory device or it necessarily has to have a plurality of memory devices.

Certainly in that time frame and with the memory device -- devices that were common at the day, all ranks, as the term was used, would have involved more than one memory device. That would have been the context that a POSITA would have used in order to understand what the term means.

BY ATTORNEY CHANDLER:

Q. So is it fair to say that your opinion is that in the context of the '417 and '215 patents, a person of ordinary skill in the

art would understand the term "rank," with an R, to require more than one memory device?

ATTORNEY WARRICK: Objection; form, scope.

THE WITNESS: Yes. It is my opinion that a POSITA in 2004-2005 would understand that ranks include more than one memory device.

BY ATTORNEY CHANDLER:

Q. And not just include more than one memory device, but must have more than one memory device.

So to be clear, the -- the dispute is whether a rank can only have one memory device. I think everyone agrees that a rank can have more than one memory device. The issue is whether a rank can have just one memory device.

What's your opinion on that question with respect to the '417 and '215 patents?

ATTORNEY WARRICK: Objection; form, scope.

THE WITNESS: It's -- my opinion is not what's relevant here. It's -- you've

instructed me to answer in the context of what a POSITA would understand in 2004-2005.

In that context, a POSITA would not have encountered anything called a rank with less -- with only a single memory device. So it would have been a significant leap on the part of a POSITA to think that there might be something called a rank that only had one -- it would be outside of his or her experience.

BY ATTORNEY CHANDLER:

Q. And you're sure about that?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: Based on my review of the documents of the day that are at -- in the record of this -- these IPRs, that is my considered opinion.

BY ATTORNEY CHANDLER:

Q. In forming your opinion in these IPRs as reflected in your expert declaration marked as Exhibit 2024, did you use the understanding of the term "rank" as we just discussed in which a rank requires more than one memory device?

ATTORNEY WARRICK: Objection;

form.

THE WITNESS: In drafting these declarations, I considered the proposed constructions by the parties and by the board and outlined my thoughts about them and then principally used the Netlist proposed construction as indicated by counsel.

BY ATTORNEY CHANDLER:

Q. And to be clear, Netlist proposed construction requires more than one memory device in a rank; correct?

A. To be clear, it says that a rank is a predetermined group of memory devices on a memory module.

So in that context, yes.

(Exhibit Number 1070 was previously marked for identification.)

ATTORNEY CHANDLER: I'm going to put Exhibit 1070 in the chat. It's the same exhibit in both IPRs. It's been marked previously, but I'll just put it in the chat for ease of reference.

BY ATTORNEY CHANDLER:

Q. Please open it up and let me know when you have it open, and you can go to

page 413 of Exhibit 1070.

A. So I have the cover page of "Memory Systems, Cache, DRAM, Disk" by Jacob, Ng, and Wang.

Q. And have you seen the Jacob textbook marked as Exhibit 1070 before?

A. Yes.

Q. And were you familiar with the Jacob textbook marked as Exhibit 1070 before you were engaged by Netlist in around the year 2021?

A. Yes.

Q. In what context were you familiar with the Jacob textbook marked as Exhibit 1070?

A. I generally buy all memory subsystem books that come on the market that I become aware of. This one was published in 2008, I believe, so in that time frame. And so I probably purchased my copy in that time frame as well -- yes, copyright 2008.

Q. Please turn to page 413 of Exhibit 1070, and let me know when you're there. If you're using Adobe Acrobat, you can type control, shift, N, type in 413, press enter, and it should jump right there.

A. I'm on page 413.

Q. Now, you understand that Professor Jacob, as shown on Exhibit 413 as Exhibit 1070, has defined the term "rank" as including one or more DRAM devices, contrary to Netlist's proposed construction of "rank" that requires more than one memory device; correct?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: So reading from page 413, the authors say, "Essentially, a rank is -- a rank of memory is a 'bank' of one or more DRAM devices that operating in lockstep in response to a given command."

BY ATTORNEY CHANDLER:

Q. Do you agree with that sentence in Exhibit 1070, page 413?

A. I think that it is not a good sentence. It's internally inconsistent in that if you have two things operating in lockstep, they are necessarily more than one of them.

So it's not a good sentence that I would agree with.

Q. To be clear, you disagree with Professor Jacob's statement on page 413 as well as page 414 of Exhibit 1070 that a rank can have

just one memory device?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: We're on page 414, are you referring to?

BY ATTORNEY CHANDLER:

Q. The end of the first full paragraph on the left above the heading 10.2.3.

A. So as of 2008 and in the context of embedded systems that do not use memory modules, that statement on page 414 has validity.

However, when you ask me in the context of a POSITA in 2004-2005, whether one device can operate in lockstep with itself and only itself, there become problems. And the distinction that the authors make here between the two uses on page 413 and 414 are at tension with each other.

And so I remain of the opinion that a POSITA, in 2004-2005 in the context of the JEDEC standardized modules, would understand a rank to have more than one device.

Q. Are the '417 and '215 patents limited to JEDEC standardized modules?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: So the scope of the claims of these patents are not limited to JEDEC standardized modules.

BY ATTORNEY CHANDLER:

Q. So I want to focus on this question of whether a rank can have just one memory device or whether it requires more than one memory device. So it's a pretty simple sort of mathematical question. Like, is one memory device sufficient to be a rank, or do there need to be two or more memory devices?

Do you understand the issue that I'm focused on?

A. Yes, I do.

Q. At the time of the Jacob book in 2008, do you believe a rank could have just one memory device?

ATTORNEY WARRICK: Objection; form, scope.

THE WITNESS: So in this case particularly, you're not asking me to answer in the context of a POSITA of 2004-2005; is that accurate?

BY ATTORNEY CHANDLER:

Q. Correct. And just so you understand where I'm going to go with the next question -- I'm trying to understand, is there some change in the meaning of "rank" from 2004-2005 to 2008? And I'm also interested in a little bit before 2004-2005, whether there was some change in the meaning of the term "rank."

But to start, let's just start with 2008, since we've got the Jacob textbook. And he says pretty clearly that a rank can have just one memory device.

Is that consistent with your understanding of the term "rank" in the year 2008, that it could have just one memory device?

ATTORNEY WARRICK: Objection; form, scope.

THE WITNESS: Again, this is not something that I've really dealt with in my declaration, since I've been using the proposed constructions by the parties as directed to by staff -- by counsel, rather.

The important point with regard to your underlying question is that Jacob's context, specifically on page 414, is embedded

systems, which have sometimes as few as a single memory device; but the context for all of your other questions of a POSITA in 2004-2005, thinking about memory modules with ranks on them, the concept of a single memory device rank would be completely foreign to that POSITA.

BY ATTORNEY CHANDLER:

Q. And is there something special in the answer you just gave me about the term "rank" in the year 2004 and 2005, or would your answer be the same with respect to the understanding of a person of ordinary skill in the art in the year 2000 or the year 1995, for example?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: So you're asking me -- a POSITA in an earlier time frame, what would they think?

BY ATTORNEY CHANDLER:

Q. Yes. I'm trying to understand whether you're suggesting that the term "rank," with an R, changed its meaning over time as you go from 1995 to 2000 to 2005 to, you know, 2008 and so forth; or whether the term "rank," with

an R, had the same meaning throughout that time frame.

ATTORNEY WARRICK: Objection; form.

THE WITNESS: There was no change to the meaning as understood by a POSITA for all of those previous time frames that you're considering in the context of memory modules containing synchronous DRAMs.

BY ATTORNEY CHANDLER:

Q. Okay. Could you turn to page 6 of Exhibit 1103 and let me know when you're there.

A. 1106?

Q. No. Exhibit 1103, which is the tutorial, and then on page 6. And let me know when you're there.

A. I apologize.

Tutorial, page 6, I am there.

Q. Do you believe a person of ordinary skill in the art would have known about the DQS, data strobe signal, and the DQ, data signal?

ATTORNEY WARRICK: Objection; form, scope.

(Witness reviews document.)
THE WITNESS: Yes, in the context of a POSITA in 2004-2005, they would certainly have been familiar with the concept of a bidirectional data line, DQ; and in the context of a DDR2 memory, they would be familiar with the idea of a data strobe signal, DQS.
BY ATTORNEY CHANDLER:
Q. And the DQS, strobe signal, was also used with DDR SDRAM memory; correct?
A. Let me be double-check. I believe that's true, but let me double-check. DDR.
Q. That's shown, for example, on Exhibit 1060, page 7, about two-thirds down.
A. I looked at the standard. And for DDR SDRAMs, DQS was not differential, so this figure would not apply. But the concept of a data strobe signal would apply, yes.
Q. And so when you use the term "differential," you're referring to the idea shown on page 6 of Exhibit 1103 that you could have a DQS strobe signal and a DQS-bar strobe signal that's essentially the opposite?
Is that fair?

ATTORNEY WARRICK: Objection; form, scope.

THE WITNESS: I would take exception to the word "could." Certainly most of the -- I believe the DDR2 required both to be present, but I'm not 100 percent sure of that. Certainly the DDR did not have the complementary signal line.

BY ATTORNEY CHANDLER:

Q. Why don't you put it in your own words, the distinction you're trying to draw with respect to the DQS strobe signal for DDR SDRAM versus DDR2 SDRAM.

A. So if we look at Exhibit 1104, which is the DDR standard, and we look at the page 1 of that standard, it talks about a DQS signal. But there's no reference in that standard to DQS-bar. So the -- in that generation of SDRAMs, the DQS was single-ended, is the terminology that we use.

In contrast, in the DDR2 standard, Exhibit 1064, we see, for example, on page 6 of that standard that DQS and DQS-bar are both defined and are -- and so the figure of the tutorial, page 6, applies to DDR2 but not to DDR

SDRAMs.

Q. And do you believe a person of ordinary skill in the art would have known the information you just gave me in your last answer?

A. The information that I gave you in my last answer comes straight from the standards, which we have previously determined would be within the knowledge set of -- or at least the familiarity set of a POSITA in 2004-2005.

Q. Looking at page 7 of Exhibit 1103, do you agree page 7 of 1103 illustrates an unbuffered DIMM, also known as a UDIMM?

ATTORNEY WARRICK: Objection; form, scope.

THE WITNESS: Yes, but this is not a DDR2 UDIMM or a DDR UDIMM?

BY ATTORNEY CHANDLER:

Q. And why do you say that?

A. Because I know what the clock and command and address topology indicates, that this is the topology that is present in DDR3 UDIMMs, not in DDR2 UDIMMs.

Q. And how would the topology of a DDR2 UDIMM differ from what's shown on page 7 of Exhibit 1103?

ATTORNEY WARRICK: Objection -- sorry. Objection; form, scope.

(Witness reviews document.)

THE WITNESS: So which exhibit is -- okay. So this is the RDIMM.

Exhibit 1062 is the JEDEC standard for DDR SDRAM RDIMMs, not DDR2, but the same ideas will apply.

For example, if you look at page 64 of that standard, it shows you the prescribed topology of address and control signals for raw cards A and B, but it applies equally for the other variants of this standard. So this does not include a fly-by, as the topology that's shown in the tutorial, page 6 or 7, whichever it was we were looking at. And this tree-like topology was the norm for the earlier generations of JEDEC standardized modules.

BY ATTORNEY CHANDLER:

Q. Turning back to page 7 of Exhibit 1103, do you believe a person of

ordinary skill in the art would have known about UDIMM memory modules in general?

ATTORNEY WARRICK: Objection; form, scope.

THE WITNESS: I believe we have an exhibit that is a UDIMM standard for DDR2. Is that accurate?

BY ATTORNEY CHANDLER:

Q. I'm not sure that we do.

A. In the record?

Well, certainly we've identified UDIMM in the specification of the patents at issue here and have acknowledged that UDIMM is one of the acronyms that a POSITA would have known about in 2004-2005 in the context of a DDR SDRAM UDIMM or a DDR2 SDRAM UDIMM.

Q. And how would you --

A. Perhaps not the latter.

I think we -- we'd have to go back and check the record of this deposition to see if we established that for DDR2 UDIMMs. But certainly with regard to DDR SDRAM UDIMMs, it was within the experience of and knowledge of a POSITA in 2004-2005. I apologize for not ending that answer cleanly.

Q. How would you explain to a layperson what a UDIMM memory module is?

A. As shown in page 7, the figure on page 7, a UDIMM is a DIMM, so it's a dual in-line memory module, that's standardized by JEDEC that includes DRAMs of the appropriate generation and no other substantial integrated circuits, excluding, of course, the SPD device, if that's on there as well, but not shown in this particular figure.

Q. And you're referring to page 7 of Exhibit 1103; correct?

A. I am.

Q. So page 7 of Exhibit 1103 shows a memory controller at the bottom sending DQ and DQS signals to the memory devices on the module as well as address commands and clock signals to the memory devices on the memory module.

Is that a fair summary?

ATTORNEY WARRICK: Objection; form, scope.

THE WITNESS: That does describe what is shown on page 7 of Exhibit 1103.

BY ATTORNEY CHANDLER:

Q. And is it generally fair to say

that with a UDIMM memory module, the memory controller sends data signals, address signals, command signals and clock signals directly to the DRAM memory devices without any intermediary integrated circuits along the way?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: I'll take exception to the characterization, as indicated in this figure, that the memory controller sends DQ and DQS. It, in fact, sends and receives DQ and DQS. And there are other aspects to the UDIMM interface that are -- that ignored, both in this figure and in your characterization, that are not central to the essential understanding of what a UDIMM is.

BY ATTORNEY CHANDLER:

Q. So, in your words, what is sort of central to the essential understanding of what a UDIMM is, then?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: I think I answered that a couple of questions ago; that the UDIMM has on it the DRAMs and perhaps the NSPE device

but no additional integrated circuits.
BY ATTORNEY CHANDLER:
Q. If I understand the clarification that you are trying to make to my question, with a UDIMM, the memory controller can both send and receive DQ and DQS signals directly with the memory devices and can also send address command and clock signals directly to memory devices.
Is that fair?
ATTORNEY WARRICK: Objection; form.
THE WITNESS: I think that's fair, yes. I think you accurately summarized the previous answer.
BY ATTORNEY CHANDLER:
Q. Do you agree that page 8 of Exhibit 1103 illustrates a registered DIMM, also known as RDIMM?
ATTORNEY WARRICK: Objection; form, scope.
THE WITNESS: Yes. Page 8 of Exhibit 1103 shows a figure that's labeled "RDIMM."
BY ATTORNEY CHANDLER:
Q. And how would you explain to a

layperson what an RDIMM memory module is?

A. In general, a JEDEC standardized RDIMM includes a register for the address and command fields or signals in addition to the DRAMs on the module.

Q. And the register you're referring to is the box labeled "Register" shown in the middle of page 8 of Exhibit 1103.

Is that fair?

A. Yes, that's true. And we also saw an RDIMM in the figure we referenced -- or the exhibit we referenced a few minutes ago, which was an actual JEDEC standardized RDIMM in its full glory.

Q. Okay. Is it fair to say that an RDIMM does not register or buffer the DQ and DQS signals; instead, it only registers the address command and clock signals going to the memory devices?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: Certainly the RDIMM that's shown on page 8 of Exhibit 1103 does not have anything along the DQ or DQS paths between the memory controller and the DRAMs. And we saw

comparable organization when we looked at the DDR2 RDIMM exhibit earlier.

BY ATTORNEY CHANDLER:

Q. Can the same type of memory devices be used on both the UDIMM memory module and an RDIMM memory module?

ATTORNEY WARRICK: Objection; form.

BY ATTORNEY CHANDLER:

Q. For example, DDR SDRAM memory devices or DDR2 SDRAM memory devices?

A. So if you look at the standards for a DDR2 UDIMM module and a DDR2 RDIMM module, you'll see that they specify the use of the same types of DDR2 SDRAMs, all standardized by JEDEC. And we can look at those specific standards to confirm that, if you so choose.

Q. I just want to be clear at a high level. It's not like JEDEC has one standard for DDR memory devices that are intended for a UDIMM and a different standard for DDR memory devices intended for an RDIMM; instead, JEDEC has one standard for the memory device; and that same memory device may be used on different types of memory modules. Maybe it's a UDIMM. Maybe it's

an RDIMM. Maybe it's something else.

Is that fair?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: JEDEC has standardized SDRAMs of different flavors. It's also standardized modules that use those DRAMs that are standardized. So the -- and the names of the module standards indicate which type of DRAMs are applicable for use in those modules. Not all DDR SDRAMs are usable within a particular DDR2 UDIMM, but some are. And certainly there are other nonstandardized memory configurations, proprietary memory configurations that also use JEDEC standardized DRAMs.

But, in general, your assertion is accurate, that the generations of modules and the generations of SDRAMs, both as standardized by JEDEC, go hand in hand.

BY ATTORNEY CHANDLER:

Q. So to take a concrete example, Exhibit 1060 is the JEDEC standard for the DDR SDRAM memory device.

A. Yes.

Q. And there's only one JEDEC standard for DDR SDRAM memory devices. It's not like you've got one JEDEC standard for DDR SDRAM memory devices intended for a UDIMM and a different JEDEC standard for DDR SDRAM memory devices intended for RDIMMs.

Instead, there's just one JEDEC standard for DDR SDRAM memory devices, and those memory devices may find themselves in a variety of different types of memory modules; is that fair?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: So if you look at page 1 of the DDR SDRAM specification JESD79, you'll see that it doesn't define one DRAM. It defines a whole family of DRAMs. Some of that family will find reference to them in the -- the DDR UDIMM standard.

Others may or may not. We'd have to check to see exactly which of these plurality of defined DDR SDRAMs are acceptable or are usable in specific DDR RDIMM modules.

So, yes, there's one SDRAM standard that feeds into or is referenced by

both the UDIMM and the RDIMM standards, but not every DDR SDRAM may have a home in any one particular type of module.

BY ATTORNEY CHANDLER:

Q. And the answer you just gave, it also applies to DDR2 memory devices and the JESD79-2 standard that we looked at marked as Exhibit 1064; correct?

A. Yes. That's a general characterization of how JEDEC goes about standardizing things.

Q. If you look back at the tutorial marked as Exhibit 1103 and sticking on page 8, for example, how would you explain to a layperson what the memory controller is, which is indicated at the bottom of that figure?

ATTORNEY WARRICK: Objection; form, scope.

THE WITNESS: Well, in this figure of Exhibit 1103, page 8, the memory controller is the circuitry that controls the memory that is on the RDIMM. It's -- the memory is not -- only responds to commands that are provided to it; and it is the memory control that is responsible for controlling the memories

according to the standard that they comply with and to send data and to receive data when appropriate.

BY ATTORNEY CHANDLER:

Q. And at the time frame of the '417 and '215 patents, were there certain companies that typically manufactured memory controllers that you were familiar with?

ATTORNEY WARRICK: Objection to form.

THE WITNESS: In the 2004-2005 time frame, memory controllers were either designed and sold independently or part of a chipset or were designed and sold as a design that was then licensed and then used by other companies.

So there are a wide variety of companies that participate in the memory controller side of the entire DRAM community.

BY ATTORNEY CHANDLER:

Q. Did you have familiarity with memory controllers at the time of the '417 and '215 patents?

A. Oh, certainly.

Q. And what memory controllers were

you most familiar with at that time frame?

A. That was, what? 20 years ago. So I would be hard-pressed to remember specific part numbers.

But certainly, you know, Intel was a dominant force in architecting PCs in that time frame. And so their memory controllers that they put into their northbridge devices or hub devices were ones that I was specifically familiar with.

Q. Were you familiar with memory controllers at the time of the '417 and '215 patents that were compatible with either a UDIMM memory module or an RDIMM memory module? In other words, the purchaser of the computer could later decide whether to plug in a UDIMM memory module or an RDIMM memory module; and either way, the memory controller would still work? Is that something that you were familiar with?

A. Again, that's 20 years ago. I don't have a specific recollection of such a memory controller that was ambidexterous with regard to UDIMMs and RDIMMs.

Q. What do you believe a person of ordinary skill in the art would have known about

that question?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: Again, that's outside the scope of the questions I had to consider for these declarations. I'm not familiar with any particular memory controllers that would have that characteristic, so I am not confident that a POSITA would either.

So, again, the passage of time makes answering that question difficult.

BY ATTORNEY CHANDLER:

Q. Let me ask the opposite.

Are you familiar with any memory controllers at the time of the '417 and '215 patents which would only work with a UDIMM but not work with an RDIMM or, conversely, would only work with an RDIMM and wouldn't work with a UDIMM?

A. Yeah. That was the norm.

Q. Could you turn to page 9 of Exhibit 1103 and let me know when you're there.

A. "Fully-Buffered DIMM," yes.

Q. Does page 9 of Exhibit 1103 illustrate a fully buffered DIMM, also known as

an FB-DIMM?

ATTORNEY WARRICK: Objection; form, scope.

THE WITNESS: Again, looking at page 9 of Exhibit 1103, it is labeled "Fully-Buffered-DIMM" and shows a box labeled such.

BY ATTORNEY CHANDLER:

Q. How would you explain to a layperson what an FB-DIMM memory module is?

A. So as illustrated in this figure on page 9, the essential aspect of an FB-DIMM that you would try to convey to a layperson is that there is an AMB chip on the FB-DIMM that couples address command and data between the memory controller and the individual DRAMs on that module.

Q. And what -- what does AMB stand for?

A. I think it stands for advanced memory buffer, but we'd have to look at the standard defining it to be certain.

Q. What's the benefit of buffering the data lines on the memory module?

ATTORNEY WARRICK: Objection;

form.

THE WITNESS: You're referring to in general or in the context of FB-DIMMs in particular?

BY ATTORNEY CHANDLER:

Q. Really, in general. If you want to answer in the context of the FB-DIMM in particular, I'll take it. But let's start with in general.

A. So if you --

ATTORNEY WARRICK: Same objection.

THE WITNESS: Let's go back to page -- page 5 of 1103, which just takes the address and command aspect of the DIMM out of the question -- it doesn't show that at all. It just shows two ranks.

But the principal characteristic that this figure does show is that the DQ signals communicate data and the DQS signals for the data strobe, communicates those signals between the memory controller and a plurality of DRAMs in a typical memory system.

And so that topology makes it difficult to run the DQ signals at high

frequency. So buffering the DQ signals on the memory module is one solution to solving that essential problem with the JEDEC style of memory -- memory module and memory system.

BY ATTORNEY CHANDLER:

Q. And is the answer you just gave me something that you think the person of ordinary skill in the art would have known at the time?

As a reminder, I mean, Perego has a buffer --

A. Yeah, right. So the -- in the context of the JEDEC standardized modules, the answer, I think, is no. But with -- in the context of the prior art generally and the references in -- in the record here, I think that that -- the existence of buffers between the memory controller and the DRAMs on the DQ lines would have been something that a POSITA would have been generally familiar with as a possibility in the 2004-2005 time frame.

ATTORNEY WARRICK: Counsel, sorry. Sorry to interrupt. I don't know if it would be approaching a good time for a break. We've been going over an hour.

ATTORNEY CHANDLER: Soon.
BY ATTORNEY CHANDLER:
Q. Dr. Przybylski, do you believe a person of ordinary skill in the art would have understood, as you said a moment ago, that putting the buffer on the data lines may permit the DQ data signals to run at a higher frequency?
ATTORNEY WARRICK: Objection; form.
THE WITNESS: I think that that's not quite accurate, because the -- in the context of any specific module, the operating frequency is specified as part of the definition of that module; but the POSITA would have been aware that some memory standards in the pantheon of memory standards and module standards at play in 2004-2005, that ones with -- that took into account signal integrity and signal topology are able to provide higher bandwidth or performance than ones that do not.
BY ATTORNEY CHANDLER:
Q. How would you explain to a layperson why a buffer on the data line may permit higher bandwidth or performance as

compared to a memory module that does not have a buffer on the data line.

ATTORNEY WARRICK: Objection; form.

THE WITNESS: That's very difficult to do for a layperson without going into a significant amount of electronics and signal integrity issues. But -- so I will try not to do that.

BY ATTORNEY CHANDLER:

Q. But do you think a person of ordinary skill in the art would understand that a buffer on the data line may permit higher bandwidth or performance as compared to a memory module that did not have a buffer on the data line?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: We'd have to look at a particular example to understand what a POSITA would or would not have understood about that. In terms of a general concept, a POSITA would understand that some memory devices, some memory module topologies are able to run much faster than others. And to the extent that

buffering plays a role in that, a POSITA may or may not have had the insight to come to that conclusion.

BY ATTORNEY CHANDLER:

Q. In your declaration as well as the prior art references, there's reference to the concept of a load on a electrical line.

Are you familiar with the concept of a load?

A. Yes.

Q. How would you explain what that is?

A. A load is a weight, an electrical weight. It's a signal that, in conveying information from one point to another, has at its destination a receiver that will present to the signal a resistance or capacitance or inductance that influences the communication of that information.

Q. And you believe a person of ordinary skill in the art would have known what you just told me in your last answer?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: In general, yes.

Its -- as its applicability to memory modules and buffering of DQ in particular, that's a different question that I did not seek to address in my declarations.

BY ATTORNEY CHANDLER:

Q. What impact does a higher electrical load have on data signals that are being transmitted to and from a memory controller?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: Again, that's a question that requires a substantial amount of electronics and math to answer properly. Just say that higher loads are more challenging and have negative impacts.

BY ATTORNEY CHANDLER:

Q. To be clear, was your answer that -- that, in general, higher loads are more challenging and have negative impacts?

A. In general, yes, but it's all extremely context-specific.

Q. And what impact does a buffer on the data lines have with respect to loads on the data signals?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: Again, within the context of 2004-2005 and the knowledge and experience of a POSITA, the general idea that reducing or otherwise managing loads to minimize their impact on data communications is a good thing.

BY ATTORNEY CHANDLER:

Q. Now, I've been sometimes told that there can be too much of a good thing.

And so if you look at the tutorial, Exhibit 1103, and you look at pages 7, 8 and 9, a UDIMM doesn't buffer any of the signals; an RDIMM buffers the address command and clock signals, but not the data signals; and an FB-DIMM buffers all -- all of the signals. Right?

ATTORNEY WARRICK: Objection; form, scope.

THE WITNESS: Again, in the context of these figures at this time, that is an accurate assessment. However, as an example of how context-sensitive this is, the DDR3 UDIMM with its unique topology would generally provide

in small- to medium-sized memory systems better performance than the comparable RDIMM.

So it is very difficult to generalize across time and across DRAM standards and across module standards.

BY ATTORNEY CHANDLER:

Q. That's what I wanted to get at, which is, there is some trade-off to whether you include a buffer on the signal line; it's not always going to be better; right?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: What do you mean by "better"? There's better in terms of performance. There's better in terms of reliability. There's better in terms of cost. So there's -- engineering is the art of the trade-off.

BY ATTORNEY CHANDLER:

Q. If you include a buffer on the data line of a memory module, would that buffer normally add a latency to the data signal as it passes through the buffer?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: Inevitably, there's some delay, depending on the type of buffer and its characteristics internally. It can be very small or it can be substantial. It all depends, again, on the unique characteristics of the circumstance we're talking about.

BY ATTORNEY CHANDLER:

Q. For example, is it possible that if you put a buffer on a data line, that the buffer could add a latency of one clock cycle?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: To what?

BY ATTORNEY CHANDLER:

Q. To what would have existed if the buffer had not been put on the data line.

A. So specifically --

ATTORNEY WARRICK: Objection; form.

THE WITNESS: We're specifically talking about data lines at this point?

BY ATTORNEY CHANDLER:

Q. Yes.

A. Okay. So in the context of 2004-2005 and the knowledge of a POSITA, I think

a POSITA would understand that a -- a buffer generally could add a small amount or a larger amount of latency, and depending on what's inside of it.

So -- and that would apply to data as well as anything else that the POSITA is dealing with.

Q. And within the range of latencies created by the data buffer, which you characterize as between a small amount and a large amount, the latency could be, for example, one clock cycle. That would be within the range of reasonable possibilities; is that fair?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: Again, for a POSITA in 2004 to 2005, it would recognize that a buffer or a buffer with a register or whatever is being in the path of the communication of a signal, the amount of that delay depends on the characteristics and nature of the buffer and the entire clocking and paradigm that's at play. So this is not an idea that's unique to memory modules or memory systems, but it's a general concept.

BY ATTORNEY CHANDLER:

Q. Was it common for a register for a buffer to delay a signal by one clock cycle?

ATTORNEY WARRICK: Objection to form.

THE WITNESS: There are --

ATTORNEY WARRICK: Objection; form.

THE WITNESS: There are many examples of a register or buffer that includes a cycle of delay. There are many examples that include many cycles of delay; and there are examples that have fractions of a cycle of delay.

Again, it all depends on the context and of the nature of the buffer that's in the signal path.

ATTORNEY WARRICK: Counsel, I suggest again that it might be a good time for a break.

THE WITNESS: It's been an hour and a half, so let's -- I would appreciate a break.

ATTORNEY CHANDLER: Let me -- just a few more questions. I want to sort of

wrap this up on this question.
BY ATTORNEY CHANDLER:
Q. Let's take the example of a data buffer that adds a latency of one clock cycle to the data signal on the memory module.
Do you have that in your mind?
A. Yes.
Q. As a layperson, to me it's a little bit counterintuitive as to why you would want to put a data buffer on a memory module if that data buffer is going to delay the signal by one clock cycle. And yet if I understand your earlier testimony, there's situations in which the data buffer can improve performance.
So how would you explain to me why adding a data buffer, which delays the data signal by one clock cycle, actually improves the performance of the memory module?
ATTORNEY WARRICK: Objection; form.
THE WITNESS: Well, let's say you have two cars, a Ferrari and a Volkswagen Beetle.
The Ferrari takes ten minutes to warm up before you get to drive it; but once

you're driving, you're going faster. So depending on how far you're going, either the Volkswagen Beetle or the Ferrari will get there faster.

It's the same sort of trade-offs that exist in the digital world, where the trade-off between operating frequency and latency is very poignant, and different solutions make sense in different domains for different types of memory systems, for different types of modules and different system types.

ATTORNEY CHANDLER: Why don't we take a break.

THE VIDEOGRAPHER: Off the record at 11:57 a.m. Pacific Time.

(Luncheon recess taken from 11:57 a.m. to 12:48 p.m.)

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P R O C E E D I N G S

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THE VIDEOGRAPHER: On the record at 12:48 p.m. Pacific Time.

EXAMINATION (Cont'd)

BY ATTORNEY CHANDLER:

Q. Dr. Przybylski, are there any clarifications or corrections you'd like to make to any of your testimony from before lunch?

A. Not at this time, no.

Q. Could you please turn to paragraph 66 of your expert declarations marked as Exhibit 2024, and let me know when you're there. And while you're doing that, I'll note that Exhibit 1096 indicates that the substance of paragraph 66 is the same in both of your expert declarations.

A. Okay. I'm there.

Q. In paragraph 66 of your expert declarations marked as Exhibit 2024, you quote Dr. Wolfe's opinion about the person of ordinary

skill in the art, sometimes referred to as a skilled artisan or a POSITA; correct?

A. Yes, I do quote Dr. Wolfe.

Q. Dr. Wolfe provided the opinion that a skilled artisan would have:

"An advanced degree in electrical or computer engineering and at least two years working in the field; or a bachelor's degree in such engineering disciplines and at least three years working in the field. Additional training can substitute for educational or research experience and vice versa."

Did I read that accurately?

A. I believe so.

Q. Do you dispute that part of Dr. Wolfe's opinion about a person of ordinary skill in the art that I just read?

A. I don't dispute it. I've accepted it as is.

Q. Dr. Wolfe continued by stating:

"Such a hypothetical person would have been familiar with various standards of the day,

including the JEDEC industry standards."

Did I read that accurately?

A. Yes.

Q. Do you dispute that part of Dr. Wolfe's opinion about a person of ordinary skill in the art that I just read?

A. Give me a second.

(Witness reviews document.)

No. Reading from my paragraph 68, I say:

"I believe a POSITA here would be knowledgeable about the operation of standardized DRAM and SDRAM memory devices and memory modules, including those commercially available devices and how those devices and modules interacted with memory controllers of a computer system."

Q. Dr. Wolfe goes on to state:

"Specifically, he or she would have been knowledgeable about the JEDEC DDR and DDR2 SDRAM standards used to standardize the

functioning of memory devices and the JEDEC21-C standard used to standardize different possibilities for the physical layout of memory devices on a module as well as difference possibilities for density and organization of the memory devices to achieve a given memory capacity."

Did I read that accurately?

A. You did.

Q. Do you dispute that part of Dr. Wolfe's opinion about the person of ordinary skill in the art that I just read?

A. As we discussed at the very outset of today's deposition, the JESD21-C standard is a huge amalgamation of many, many standards, only some of which are related to memory devices and -- and memory modules.

And so that statement is overly broad. But given that caveat, there's -- I have no dispute with it.

Q. Dr. Wolfe goes on to state that a skilled artisan:

"Would also have been

familiar with the structure and operation of circuitry used to access and control computer memories, including sophisticated circuits such as ASICs (application-specific integrated circuits) and CPLDs (complex programmable logic devices) and more low-level circuits such as tristate buffers, flip-flops and registers."

Did I read that accurately?

A. Yes.

Q. Do you dispute that part of Dr. Wolfe's opinion about the person of ordinary skill in the art that I just read?

A. I don't have any difficulty with it.

Q. Could you turn to paragraph 68 of your expert declarations marked as Exhibit 2024. Let me know when you're there. And, again, I believe Exhibit 1096 indicates that paragraph 68 is substantively the same in both of your expert declarations.

A. I'm looking at 68.

Q. In paragraph 68 of your expert

declarations marked as Exhibit 2024, you indicate that Dr. Wolfe provided the opinion that a person of ordinary skill in the art would be knowledgeable about the design and operation of standardized DRAM and SDRAM memory devices and memory modules and how they interacted with the memory controller of a computer system.

Did I read the portion of your paragraph 68 accurately?

A. Yes.

Q. That portion of Dr. Wolfe's opinion is the only part of Dr. Wolfe's opinion about the person of ordinary skill in the art that you specifically disagreed with in your expert declarations marked as Exhibit 2024; is that fair?

A. Specifically with regard to the DRAM internals and the ability to create a new DRAM device, yes.

Q. And that's what I want to follow up on.

It's your opinion that a person of ordinary skill in the art would not be knowledgeable about the design of memory devices or memory modules; instead, in your opinion, a

person of ordinary skill would be knowledgeable about the operation of standardized DRAM and SDRAM memory devices and memory modules, including those commercially available devices and how these devices and modules interacted with memory controllers of a computer system.

Is that a fair summary?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: Yes. As I've indicated in that section of my report, I view the design of memory devices and the use of memory devices in memory systems as being two separate fields of art and that the POSITA in this case is familiar with the latter and not with the former.

BY ATTORNEY CHANDLER:

Q. And then in paragraph 70 of your expert declarations marked as Exhibit 2024, you state that:

"With this restriction to the scope of knowledge and experience of a POSITA, I apply Samsung's proposed level of knowledge in my analysis."

Is that correct?

A. That's what paragraph 70 says, yes.

Q. And so do I understand correctly that all of your opinions in your declarations marked as Exhibit 2024 are based on Samsung's proposed level of skill in the art with the one restriction we just discussed, which is that, in your opinion, a person of ordinary skill in the art would not be knowledgeable about the design of memory devices and memory modules?

A. As far as the knowledge of a POSITA in 2004-2005, they know how to use the DRAMs. They knew a little bit about the organization of and the logical specification of the DRAMs, but they know very little about what's going on under the hood, so to speak.

Q. In paragraph 72 of your expert declarations, marked as Exhibit 2024, you state that the "Vast majority of the DRAM devices and modules sold would have been compliant with one of the JEDEC standards."

Did I read that accurately?

A. Yes.

Q. I have seen estimates that around 90 percent of the DRAM memory devices sold in

this time frame complied with the JEDEC standards for DDR or DDR2 memory devices.

Does that sound like a reasonable estimate to you?

A. 90 percent for those two standards in particular?

Q. Yes. For the --

A. Or 90 percent for all JEDEC standard DRAMs?

Q. Well, why don't you tell me what you think is reasonable and what you intended by the phrase "the vast majority."

A. Well, certainly I did not have access to market data from that time frame anymore. So it was based on my understanding of what the market conditions were in 2004-2005. I don't feel comfortable putting a particular number on it, whether it's 90 percent for those two DRAM types or if it's 95 for those two DRAM types or 98 for all JEDEC-defined SDRAMs. I don't have any data. So I'm comfortable with saying that the vast majority, like more than 75 percent; but specifically how much more, I do not know.

Q. In paragraph 71 of your expert

declarations marked as Exhibit 2024, you refer to "commercially available memory devices."

In forming your opinions, did you assume that a person of ordinary skill in the art would be familiar only with commercially available memory devices?

A. Not explicitly. However, a POSITA in 2004-2005 would not have had enough time to really come to -- come in contact with any noncommercially available DRAM devices except possibly ones that are written about in papers here and there that they might have come in contact with. But certainly the principal frame of reference for a POSITA's thinking about these things would have been the commercially available devices and modules.

Q. In paragraph 69 of your expert declarations marked as Exhibit 2024, you cite to Exhibit 1070, the textbook by Professor Jacob that we looked another a little bit earlier, to support your opinion that a person of ordinary skill in the art would not be knowledgeable about the internal operation or structure of memory devices; correct?

A. Yes. We'd have to look at those

Samsung Ex. 1095, p. 147
Samsung Electronics Co., Ltd. v. Netlist, Inc., IPR2023-00455

pages, 316, 317, to be clear. But that is what I do say in that paragraph.

Q. You state that in the Jacob textbook marked as Exhibit 1070, there are 285 pages about the design and operation of memory systems using DRAMs, of which only two pages and one figure describe the internal operation and structure of a DRAM in the most superficial manner; correct?

A. Those are my words, yes.

Q. And the 285 pages that you're referring to are pages 315 through 598 of Exhibit 1070, which is Chapters 7 through 15 in Part 2 of the textbook; is that fair?

A. I don't have the specific page numbers listed there in that paragraph. I'm happy to take your word for it, if that -- the page numbers that you outlined total 285.

Q. So if you open Exhibit 1070 and you go to the table of contents on page Romanette xiii, you see that there's Part II DRAMs starting on page 313 with Chapter 7 and that Part II runs through Chapter 15 that ends on page 598; correct?

A. Yes, I see that.

Q. Could you turn to page 353 of the Jacob textbook marked as Exhibit 1070. This is the start of Chapter 8. And let me know when you're there.

A. Page 353, Chapter 8.

Q. And Chapter 8 runs through page 376; correct?

A. Yes.

Q. Chapter 8 of the Jacob textbook marked as Exhibit 1070, starting on page 353 and ending on page 376, describes the internal operation and structure of DRAM memory devices; correct?

A. Generally speaking, that's true. So I was clearly in error when I said the two pages in one figure.

Q. A person of ordinary skill in the art would have been familiar with the general information contained in Chapter 8 of the Jacob textbook marked as Exhibit 1070 about the internal operation and structure of DRAM memory devices; correct?

A. No, I wouldn't necessarily go that far. This textbook was written and released in 2008. Prior to this textbook, there

were separate textbooks about the DRAM internals and textbooks and papers about the internals and -- so that it's a leap to say that a POSITA in 2004-2005 would be familiar with all of the contents of Chapter 8.

Q. Well, to be clear, you're the one that cited to Exhibit 1070 in your expert declarations marked as Exhibit 2024; correct?

A. I did.

Q. And also to be clear, you would agree now that a person of ordinary skill in the art would have been familiar with information about the internal operation and structure of DRAM memory devices; correct?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: My principal argument is that the design of DRAMs and the design of memory system using DRAMs are two separate bodies of art and that the POSITA that we are considering here with relatively little experience and the experience being principally related to the design of memory systems would not be necessarily familiar with all of the material of Chapter 8.

BY ATTORNEY CHANDLER:

Q. Turn to page 355 of Exhibit 1070, the textbook that you cited in your expert declarations, and let me know when you're there.

A. 355?

Q. Yes.

A. Section 8.2, "DRAM Storage Cells"?

Q. Yes.

In your opinion, would a person of ordinary skill in the art have been familiar with the DRAM storage cells internal to the memory devices?

A. At a fundamental level, the 1T1C storage cell is the basis for DRAMs, yes, they'd be familiar with it because they would be cognizant that these storage cells need to be refreshed.

Q. Turn to page 358 of Exhibit 1070. Let me know when you're there.

A. I'm at 358.

Q. In your opinion, would a person of ordinary skill in the art have been familiar with the concept of RAM array structures internal to the memory device?

A. In my opinion, a person of ordinary skill would have been aware of RAM array structures at the level of detail articulated by Figure 8.7 on page 359, that the memory storage cells are logically arranged into rows and columns and that word lines and bit lines are what are used to access the -- to perform activates and then reads and write commands; but above and beyond that, I'm not confident of that.

Q. Turn to page 366 of Exhibit 1070. Let me know when you're there.

A. Which page? I'm sorry.

Q. 366.

A. 366.

I'm there.

Q. In your opinion, would a person of ordinary skill in the art have been familiar with decoders internal to the memory device?

A. A person of ordinary skill would know that there were decoders in there, because the row and column addresses need to get decoded into individual word lines and collections of bit lines; but their specific characteristics and certainly the whole topic of redundancy

would have been beyond them.

Q. Turn to page 368 of Exhibit 1070. Let me know when you're there.

A. Yes.

Q. In your opinion, would a person of ordinary skill in the art have been familiar with control logic internal to the memory device?

A. Again, within the context of a POSITA of 2004-2005, principally concerned with SDRAMs of different varieties standardized by JEDEC, would have been cognizant of control logic as depicted in Figure 8.18, which is control logic for a synchronous DRAM, because that sort of figure exists in the data sheets for those commercially available DRAMs. So to that level, yes.

Q. Please turn to page 372 of Exhibit 1070. Let me know when you're there.

A. I'm at page 372.

Q. In your opinion, would a person of ordinary skill in the art have been familiar with data I/O structures internal to the memory device?

A. Again, if you look at the next

page, page 373, there is a drawing of a data I/O structure from a DDR SDRAM. This figure is duplicated by and large in the data sheets for DDR SDRAMs. And so our person of ordinary skill as of 2004-'5 would be familiar with this level of the I/O structures.

Q. In your opinion, would a person of ordinary skill in the art have been familiar with DRAM device packaging?

A. Again, the JEDEC standards for the DRAMs specify the device -- the packages that each is to be packaged in and delivered in, including the pin-outs. And so the -- the person of ordinary skill might not be familiar with the historical DIP and SOJ packages that are shown in Figure 8.22 but would be comfortable with the TSOP and BGA -- not BGA -- the TSOP packages that were common in 2004 and 2005.

Q. Please turn to page 457 of Exhibit 1070 and let me know when you're there.

A. 457, so going backwards?

Q. No. Forwards, 457.

A. 457. I'm sorry. My apologies.

457.

Q. It's the start of Chapter 12. Just let me know when you're there.

A. Yes.

Q. Chapter 12 of the Jacob textbook marked as Exhibit 1070, starting on page 457, describes the evolutionary developments of DRAM device architecture; correct?

A. Yes. That's a terminology I introduced.

Q. And a person of ordinary skill in the art would have been familiar with the evolutionary developments of DRAM device architecture up to the 2004 and 2005 time frame; correct?

A. Given that we are assuming that our POSITA entered the workforce around 2001-ish/2002-ish and entered school in the late 1990s, their familiarity with the ancient history of the field is not something we can rely on.

Q. In forming your opinions in your expert declaration marked as Exhibit 2024, did you consider whether the hypothetical person of ordinary skill in the art is knowledgeable about all of the prior art in the field of the '417

and '215 patents? Or did you limit the hypothetical person of ordinary skill in the art to only what existed between the late 1990s and 2004 to 2005?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: My process was to rebut the arguments in the petitions and the corresponding declarations. To the extent that there was need to consider that particular aspect of a POSITA's knowledge, I would have done so; but I don't recall any circumstances where that came into play.

BY ATTORNEY CHANDLER:

Q. Turn to page 458 of Exhibit 1070, and there's a Figure 12.1 at the top. Let me know when you have that in front of you.

A. I have 458 up.

Q. So page 458 of Exhibit 1070 at the top and Figure 12.1 refers to different types of memory devices, including SDRAMs, DDR SDRAMs, and different Rambus DRAMs; correct?

A. Are you reading from the text or from the figure?

Q. I'm looking at the figure.

A. I don't see any reference to Rambus DRAMs in the figure.
Q. In the upper right.
A. Oh, D-RD and XDR. You're right, yes.
Q. And a person of ordinary skill in the art --
A. So what's the question now again, please?
Q. Simply that Figure 12.1 on the top of page 458 of Exhibit 1070 refers to different types of memory devices, including SDRAMs, DDR SDRAMs and different Rambus DRAMs; correct?
A. Yes. Once you recognize that D-RD and XDR refer to Rambus DRAMs, yes.
Q. And, in your opinion, a person of ordinary skill in the art would have been familiar with SDRAMs, DDR SDRAMs and Rambus DRAMs; correct?
A. Yes, and probably the GDDR graphics DRAMs as well, but those have not come into play in this matter.
Q. Turn to page 465 of Exhibit 1070. Let me know when you're there.

A. Yes.
Q. As we've discussed, a person of ordinary skill in the art would have been familiar with SDRAMs, with a capital S; correct?
A. Yes.
Q. As shown, for example, on page 467 of Exhibit 1070 in Figure 12.10 at the top, a person of ordinary skill in the art would have known about SDRAM device architecture with four banks; correct?
A. Yes.
ATTORNEY WARRICK: Objection to form.
THE WITNESS: This represents the logical presentation of the memory device to the outside world.
BY ATTORNEY CHANDLER:
Q. Please turn to page 471 of Exhibit 1070. Let me know when you're there.
A. 471, yes.
Q. And there's a leaf blower outside. Is it bothering you? Do you hear it?
A. You're cutting out once in a while as a result, but not much.
Q. A person of ordinary skill in the

art would have been familiar with DDR SDRAMs; correct?

A. We did verify this morning that the DDR SDRAM standard, the first one became public in 2005, I think. What did we see?

Q. It was 2000 for DDR and then 2003 for DDR2; correct?

A. Right. And then 79-B2 -- 2B -- sorry -- was January 20th, 2005, so, yes.

Q. And then if you turn to page 474 of Exhibit 1070, you agree a person of ordinary skill in the art would have been familiar with DDR2 SDRAMs; correct?

A. To the extent that they were referenced in other documents, yes. I think we were not clear whether the -- right. So the -- I'm sorry. So the DDR2 SDRAMs were early enough. So, yes.

Q. And then if you turn to page 475 of Exhibit 1070, do you agree a person of ordinary skill in the art would have been familiar with some of the protocol and architectural differences between DDR SDRAMs and DDR2 SDRAMs?

ATTORNEY WARRICK: Objection;

form.

THE WITNESS: Yes. Those are the difference that would have -- are essential to building memory systems and memory modules out of these devices. So the protocol and architectural differences are principally what the POSITA of 2004-2005 is concerned with.

BY ATTORNEY CHANDLER:

Q. It you turn to page 477 of Exhibit 1070, do you agree that a person of ordinary skill in the art would have been generally familiar with the scaling trends of DDR and DDR2 SDRAM memory devices?

ATTORNEY WARRICK: Objection; form.

(Witness reviews document.)

THE WITNESS: Some of the content of Section 12.3.6 relating to the evolution of the JEDEC standard DRAMs would have been known to a POSITA of 2004-2005.

BY ATTORNEY CHANDLER:

Q. And if you look at page 480 of Exhibit 1070, do you agree a person of ordinary skill in the art would have been familiar with Rambus DRAMs?

A. Yes.

Q. And, for example, as shown on page 482 of Exhibit 1070 and Figure 12.24, a person of ordinary skill in the art would have been generally familiar with the internal bank architecture of a Rambus direct RDRAM device; is that fair?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: Certainly would be generally aware that there was a plurality of ranks -- of banks -- sorry, my apologies. And that is a distinction between the JEDEC standardized devices and the Rambus devices.

And, again, this is a logical representation of the internal architecture of those devices. And so the -- it is the general purview of what a POSITA would be familiar with to some extent.

BY ATTORNEY CHANDLER:

Q. Please look back at your expert declaration marked as Exhibit 2024, specifically paragraphs 5 through 11. Let me know when you're there.

And while you're doing that, I'll

note that Exhibit 1096 shows that the substance of paragraphs 5 through 11 is the same in both of your expert declarations.

A. I am there.

Q. Starting with paragraph 5 of your expert declarations marked as Exhibit 2024, you describe your qualifications and experience relevant to these IPRs; correct?

A. Referring to Appendix A, yes.

Q. And you consider yourself qualified to provide expert opinions in these IPRs; correct?

A. Yes.

Q. Do you consider Samsung's expert, Dr. Wolfe, to be qualified to provide expert opinions in these IPRs concerning the '417 and '215 patents?

A. That's not a question that I've been asked to opine on.

Q. But I'm asking you.

A. I haven't reviewed his CV recently, so I don't know.

Q. Do you know Dr. Wolfe?

A. I have had occasion to bump into him from time to time over the years, yes.

Q. Would you consider him, based on your interaction with him, to be an expert with respect to the fields of the '417 and '215 patents?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: Again, I haven't reviewed his detailed work experience and qualifications that relate to memory subsystems in particular, so I don't know.

BY ATTORNEY CHANDLER:

Q. Have you heard of Dr. Michael Brogioli?

A. I do not know the man, no.

Q. Do you consider Professor Bruce Jacob to be an expert in the field of the '417 and '215 patents, the author of the textbook marked as Exhibit 1070?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: Yes. He's certainly quite knowledgeable in this field.

BY ATTORNEY CHANDLER:

Q. In paragraph 9 of your expert declarations marked as Exhibit 2024, you state

that you worked on cache hierarchies; correct?

A. Yes.

Q. Did the cache hierarchies that you worked on use memory modules?

A. My doctoral dissertation involved cache memory design and main memory design. Modules were a level of conceptual detail below it, which I was working on.

Q. Can you explain that a little bit more, what you mean by "level of conceptual detail below."

A. The simulations that I was doing with regard to main memory performance did not capture whether a particular style of main memory was in one form of module or another.

In that time frame, all of the DRAMs that were commercially available were all asynchronous and the modules were basically all unbuffered DIMMs. So there was no issue with regard to whether the memory systems I was simulating used one variety of module or another.

Q. But focusing on the cache hierarchies, what kind of memories -- what kind of memory modules, if any, were involved in the

cache hierarchies that you were working on?

A. So the cache hierarchies in that era were all SRAM-based.

Q. And were those cache hierarchies that were SRAM-based organized on to a memory module?

A. They could have been. It was not -- again, it was not part of the -- it was not one of the dimensions that I was investigating.

Q. And what is an SRAM memory device?

A. Stands for static random-access memory.

Q. Were SRAM memory devices known and commercially available before the 2004-2005 time frame?

A. Yes.

Q. And is an SRAM memory device different from a DRAM memory device?

A. Yes.

Q. In paragraph 9 of your expert declaration marked as Exhibit 2024, you also state that you worked on MIPS computer systems, M-I-P-S; correct?

A. Correct.
Q. Did the MIPS computer systems that you worked on use memory modules?
A. Yes, they did.
Q. Did the MIPS computer systems that you worked on use DRAM memory devices?
A. Yes.
Q. And what kind of DRAM memory devices?
A. In that era, again, we were pre-SDRAM. And so we were all dealing with fast page mode devices.
(Interruption by the court reporter to clarify the record.)
BY ATTORNEY CHANDLER:
Q. In paragraph 11 of your expert declarations marked as Exhibit 2024, you mentioned that you wrote and revised a book entitled "New DRAM Technologies: A Comprehensive Analysis Architectures"; correct?
A. Yes; two editions of it.
Q. And to what extent is that book that you wrote relevant to your qualifications for being an expert in these IPRs?
A. That book analyzed not just

SDRAMs but all of the variety of DRAM architectures, both internally and externally, all those architectures that were available in the early 1990s through the -- the second edition came out in the later half of the 1990s. And so it's presented for the reader how these devices differed internally and how their interfaces were different at a very granular level, and then explored how their performances in systems varied as a result of their different characteristics.

Q. And that's relevant to these IPRs?

A. Yes.

(Whereupon, Exhibit Number 1097 in both IPRs was marked for identification and is attached hereto.)

ATTORNEY CHANDLER: I'd like to mark a new exhibit, which will be 1097. It's the same document in both IPRs, the only difference being the stamp in the bottom right, the case number.

I put it in the chat for everyone's convenience.

BY ATTORNEY CHANDLER:

Q. Please let me know when you have Exhibit 1097 open.
A. I got the whole thing, yes.
Q. Do you recognize the cover of Exhibit 1097 as the cover of the second edition of your book entitled "New DRAM Technologies: A Comprehensive Analysis of the New Architectures"?
A. Yes.
Q. And did you write this book marked as Exhibit 1097 yourself?
A. Yes.
Q. Please turn to page 41 of Exhibit 1097, which is Chapter 3 of your book, and let me know when you're there.
A. I'm at Chapter 3.
Q. Do you believe a person of ordinary skill in the art would have known about DRAM basics as explained starting on page 41 of your book marked as Exhibit 1097?
ATTORNEY WARRICK: Objection; form.
THE WITNESS: The POSITA that we've been discussing vis-à-vis 2004 and 2005 would have been familiar with some of the topics

in my Chapter 3, just as we reviewed Jacob's book from 2008, and that some of the topics related to the DRAM internals would have been within the purview of such a POSITA.

But I think there are some aspects that are in my Chapter 3 that would not necessarily have been at the fingertips of our POSITA.

BY ATTORNEY CHANDLER:

Q. Please turn to page 69 of Exhibit 1097, which is the start of Chapter 4, and let me know when you're there.

A. I'm there.

Q. Do you believe a person of ordinary skill in the art would have known about single in-line memory modules, or SIMMs?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: Again, by the time we were in the 2000s, which is when our POSITA is learning about these things, SIMMs are no longer being used and we are purely in the domain of DIMMs and other more-advanced memory module structures. So they may or may not be familiar with the prior generations of modules.

BY ATTORNEY CHANDLER:

Q. Well, to be clear, a person of ordinary skill had to go to college and get the equivalent of an advanced degree, and as part of that training, they would have been taught about SIMMs; correct?

A. Maybe. Maybe not.

Again, the transition from SIMMs to DIMMs happened in -- if I recall correctly, it was in the middle 1990s. So after this edition came out -- at least I think so. We'd have to go back and check the dates on various standards.

But, you know, the -- our POSITA may be familiar with SIMMs, maybe not. I don't know. It -- it certainly didn't come up with regard to my opinions in this matter.

Q. The '417 and '215 patents specifically refer to SIMMs as within the scope of the memory modules that the '417 and '215 patents relate to; right?

ATTORNEY WARRICK: Objection; form.

BY ATTORNEY CHANDLER:

Q. As shown, for example, in

Samsung Ex. 1095, p. 170
Samsung Electronics Co., Ltd. v. Netlist, Inc., IPR2023-00455

Column 6 of the '417 patent at line 45, and also shown, for example, in Column 5 of the '215 patent at line 65; correct?

A. Yeah, that's true.

Q. Turning back to your book marked as Exhibit 1097, you discuss SIMMs starting on page 70; correct?

A. Correct.

Q. And then, for example, on page 71 of your book marked as Exhibit 1097, you show a figure at the top of the page of a standard 30-pin SIMM; correct?

A. That's what the caption of Figure 4-1 indicates.

Q. You think a person of ordinary skill in the art would have known about standard 30-pin SIMMs?

A. Possibly. It's -- again, since we're dealing with someone who came out of school in the early 2000s, perhaps or perhaps not. I mean, it's -- there were certainly enough textbooks in that time frame that talked about SIMMs, so it's quite plausible that they would have.

Q. You state on page 71 of your book

marked as Exhibit 1097 that the most common SIMM memory modules were x8 and x9 organizations; correct?

A. And also x32 and x36 on larger ones.

Q. And even though we're pronouncing it "by 8," it's written lowercase x and then the number 8; correct?

A. Well, technically, it's a multiplication symbol. But if we don't have access to that, we use a lowercase x, yes.

Q. And what does x8 and x9 mean?

A. So with regard to my Figure 3-8 showing a 512Kx8 DRAM on page 56 of the new DRAM technologies, Version 2, it shows 8 DQ signals exhibiting the DRAM. So the x8 means 8 DQ signals.

Q. Please turn to page 129 of Exhibit 1097. Let me know when you're there.

A. 129, you said?

Q. Yes.

A. Chapter 5?

Q. Yes.

A. I'm there.

Q. Starting on page 129 of your book

marked as Exhibit 1097, you describe new DRAM architectures; correct?

A. Yes.

Q. And do you believe a person of ordinary skill in the art would have known about the new DRAM architectures described in your book marked as Exhibit 1097 starting on page 129?

ATTORNEY WARRICK: Objection; form.

(Witness reviews document.)

THE WITNESS: So Chapter 5 begins with a discussion of improvements to the existing interface and talks about new packaging varieties and new organizations and then gets into some of the new architectures that were becoming -- or being proposed as architectures that -- to replace the fast page mode and burst EDO architectures that were common in the early half of that decade. Some of these caught on; some of them fell by the wayside.

I think a POSITA in the mid 2000s would certainly have heard of some of these, but not all of them.

For example, on page 152, we -- I

categorize synchronous DRAMs in the collection of DRAMs that are new, as they were in 1994 and 1996. So, obviously, the POSITA in 2004-2005 would have been familiar with these; but some of the other ones never got any commercial traction and fell by the wayside. Similarly for the revolutionary approaches in Section 5.6.

BY ATTORNEY CHANDLER:

Q. Please turn to page 157 of your book marked Exhibit 1097. Let me know when you're there.

A. I am there.

Q. Starting on page 157 of your book marked as Exhibit 1097, you describe conventional alternatives to DRAM memory devices; correct?

A. "Conventional" being the DRAM architectures that were in place or just minor modifications to the DRAMs that were in place in around 1993-1994.

Q. A person of ordinary skill in the art would have known about conventional alternatives, such as EDO DRAMs, as described in your book marked as Exhibit 1097; correct?

ATTORNEY WARRICK: Objection;

form.

THE WITNESS: They may have heard the term, but they would never have had an opportunity to design with them.

BY ATTORNEY CHANDLER:

Q. Please turn to page 171 of your book marked Exhibit 1097. Let me know when you're there.

A. Chapter 7, Evolutionary Approaches -- Alternatives, rather?

Q. Yes. Starting on page 171 of your book marked as Exhibit 1097, you describe evolutionary alternatives to DRAM, such as synchronous DRAMs; correct?

A. Yes. The synchronous DRAMs that were coming into the fore in the mid 1990s I categorized as evolutionary.

Q. And as we've discussed, a person of ordinary skill in the art would have known about these evolutionary alternatives to DRAM at the time, such as synchronous DRAM; correct?

A. But the synchronous DRAMs that I address in my book predate the DDR and DDR2 DRAMs -- SDRAMs that are at issue in this matter.

The previous version, which came to be known as SDR SDRAMs are -- had a relatively short lifespan because of some issues with them; and so a POSITA probably would have heard of SDR SDRAMs, but maybe not.

Q. But, again, the '417 and '215 patents specifically refer to RAM, DRAM, SDRAM, SDR, DDR, and DDR2, correct, as shown, for example, in Column 6 of the '417 patent around lines 51 through 55 and also Column 6 of the '215 patent around lines 4 through 8; correct?

A. Yes. It does mention SDR as one of the varieties of SDRAMs there, yes.

Q. And also DRAM and RAM, even older technologies; correct?

A. Well, "RAM" is a general term referring to all random-access memory, so including SRAMs and DRAMs and so that's a generic placeholder.

Then it refers to DRAMs, which, again, is generic, not specifically referring to the previous generations. And then SDRAMs in its varieties being an example of DRAMs, DRAMs being an example of RAMs. That's how I interpret that sentence.

Q. Do you interpret the '417 and '215 patents as limiting themselves to memory devices that are SDRAM and newer, or do you interpret the disclosure of the '417 and '215 patent as trying to be broader and encompassing older generations of memory devices as well?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: So the disclosure of the '417 only mentions by name in this sentence the SDR -- I'm sorry -- the SDRAMs in its various flavors, including SDR SDRAMs.

It doesn't mention by name that I can find here any of the names of the previous generations of memory architecture with the exception of the reference to SIMMs in the previous paragraph.

So with regard to the disclosure of the specification, there is a failure to disclose anything other than those more recent architectures in this portion of the specification. So there's no mention of fast page mode or EDO or any of the other architectures that, for example, I enumerate in the new DRAM technologies book.

BY ATTORNEY CHANDLER:

Q. Starting on page 204 of your book marked as Exhibit 1097, you have a section numbered 7.4 devoted to synchronous SDRAMs, also known as SDRAMs with a capital S; correct?

A. Sorry. What was the page number again?

Q. 204.

A. 204.

Yes, I see that section.

Q. And you indicate that JEDEC, specifically the JC42.3 committee, developed standards for SDRAMs; correct?

A. I'm sorry. Repeat the question.

Q. You indicate on page 204 of your book marked as Exhibit 1097 that JEDEC, specifically the JC42.3 committee of JEDEC, develops standards for SDRAMs; is that correct?

A. Yes. So in that first paragraph of Section 7.4, I do note that the JC42.3 standards committee is working on a proposed standard for SDRAMs.

Q. And did you personally ever participate in the JEDEC JC42.3 committee?

A. As I mentioned earlier, the

members of JEDEC are companies, not individuals. Some of my clients in that period were members of that committee and other committees, and I would occasionally participate as a guest of one of those clients. But I was not a voting member or anything like that.

Q. So even though you were not a member of JEDEC, you attended some meetings of the JEDEC JC42.3 committee during the standardization process for SDRAMs; is that fair?

A. I don't recall which versions of the SDRAM standards I was -- I attended. I only attended a couple of meetings of JEDEC, because, as I said, I myself was not a member and could only attend as a guest of another member.

So I think that answered your question.

Q. Please turn to page 242 of your book. Let me know when you're there.

A. I am at 242.

Q. On page 242 of your book marked as Exhibit 1097, you list out some of the strengths and weaknesses of SDRAMs; correct?

ATTORNEY WARRICK: Objection;

form.

THE WITNESS: Yes. This specifically is for the SDR variety of SDRAMs.

BY ATTORNEY CHANDLER:

Q. And do you believe a person of ordinary skill in the art would have known about the strengths and weaknesses of SDRAMs, as listed on page 242 of your book marked as Exhibit 1097?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: Certainly by the time we reach 2004 and 2005 and the subsequent versions of SDRAMs standardized by JEDEC, most of -- or some of these weaknesses have dissipated, are no longer in play. So they would not necessarily be front of mind for a POSITA in 2004-2005.

And certainly -- you know, of the five weaknesses there, the middle three would certainly be something a POSITA would be aware of; the first and the last, probably not.

BY ATTORNEY CHANDLER:

Q. With respect to the strengths of SDRAMs listed on page 242 of your book marked as

Exhibit 1097, did those strengths remain true in the 2004-2005 time frame?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: It mentions there a dual-bank architecture. By the time we're in the mid-2000s, we migrated beyond dual-bank to quad-bank and higher-bank counts for some of the other memory types. So that would be no longer precisely accurate.

And so with regard to the first strength, it says, "Likely to become a commodity part."

By 2004 and '5, it is -- the JEDEC standardized DRIMMS sic are the commodity parts, so that's modified over time. And the commodity marketplace does provide for interchangeable parts across vendors. And the other strengths, including, obviously, the DIMM standard, became a significant strength over time as well.

BY ATTORNEY CHANDLER:

Q. So would it be fair to say both at the time of your book marked as Exhibit 1097, which is around 1996, as well as the time of the

'417 and '215 patents in the 2004-2005 time frame, that a person of ordinary skill in the art knew that strengths of DDR SDRAMs and DDR2 SDRAMs included that they were standardized by JEDEC; they were commodity parts; they were interchangeable parts; and that high bandwidth was possible?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: Yes. However, what constitutes high bandwidth in 2000 -- I'm sorry -- 1996 is different than what passes for high bandwidth in 2004 and '5. But, generally speaking, that's true.

BY ATTORNEY CHANDLER:

Q. Please turn to page 259 of your book. Let me know when you're there.

A. I'm there.

ATTORNEY CHANDLER: And I should ask -- we've been going a little bit more than an hour -- if you want to take a break now or if you want to keep going through your book.

THE WITNESS: Yes, let's take a break.

ATTORNEY CHANDLER: Okay.

THE VIDEOGRAPHER: Off the record at 2:00 p.m. Pacific Time.

(Recess taken from 2:00 p.m. to 2:11 p.m.)

THE VIDEOGRAPHER: On the record at 2:11 p.m. Pacific Time.

BY ATTORNEY CHANDLER:

Q. Dr. Przybylski, starting at on 259 of your book marked as Exhibit 1097, you describe what you characterize as revolutionary alternatives to DRAM, such as Rambus DRAMs; correct?

A. Yes.

Q. And a person of ordinary skill in the art would have known about these so-called revolutionary alternatives to DRAM, such as Rambus DRAMs; correct?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: The Rambus DRAMs that I talked at length about in this chapter predate the versions of Rambus memory devices that are at issue in this matter, which were the direct and the XDR generations.

This device here is -- did not

survive very long, and so the specifics of this particular Rambus device probably would not be something that a POSITA of 2004-2005 would have had contact with.

BY ATTORNEY CHANDLER:

Q. But it was described in your book, and a person of ordinary skill in the art had access to your book; correct?

A. The distribution of the book was pretty limited to various companies and a few libraries. But as far as whether a POSITA in 2004-2005 would have had access to this limited-edition book from a decade earlier, not at all clear to me.

Q. Well, it's also described in Professor Jacob's book and his paper from 2002; correct?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: What was described?

BY ATTORNEY CHANDLER:

Q. Rambus DRAMs, including the version that you're talking about, starting on page 259 of Exhibit 1097; right?

A. Yes. There's some overlap

between this particular device, and it is mentioned in passing in Jacob's article.

Q. Turn to page 305 of your book marked as Exhibit 1097. Let me know when you're there.

A. Page 305?

Q. Yes.

A. I'm there.

Q. On page 305 of your book marked as Exhibit 1097, you list strengths and weaknesses of Rambus DRAMs; correct?

A. I do.

Q. For example, some of the listed weaknesses of Rambus DRAMs include "high latency," "limited parallelism," and "not an evolutionary technology"; correct?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: Yes, those are things that I mention.

BY ATTORNEY CHANDLER:

Q. You also mention that another weakness of Rambus DRAM was a "negative industry perception of the royalty structure."

Could you explain that a little

bit more.

A. So the JEDEC committees were working to standardize DRAM interfaces and module interfaces.

Rambus had a different business model, which involved designing memory devices and modules and then licensing those designs to semiconductor manufacturers; and there was, at the time, a significant perception that the Rambus royalty structure was going to be detrimental to the industry.

Q. And did that negative perception of the royalty structure of Rambus memory devices persist through the 2004-2005 time frame?

A. To some extent. I don't remember the details. But by the time we were dealing with XDR and direct Rambus, there was still some concern about the price comparison between Rambus DRAMs and, for example, the SDRAMs of the day. And so it was an issue to some extent. It's hard to quantify how much of an issue it was.

Q. If I understand correctly, would it be fair to say that the SDRAM memory devices

in the 2004 and 2005 time frame, including SDR, DDR and DDR2, did not have a negative industry perception with respect to any royalty structures?

A. Not with regard to --

ATTORNEY WARRICK: Objection to form.

THE WITNESS: There was not a negative perception with regard to a royalty structure, because although there was a lot of cross-licensing with royalties amongst the companies involved in the DRAM industry, it wasn't of the same style and business model that Rambus had.

There were other issues with the JEDEC standardized memory modules that resulted in negative perceptions of other varieties not specifically about the royalty structure that I mentioned here for Rambus.

BY ATTORNEY CHANDLER:

Q. If I understand your earlier testimony, by the 2004-2005 time frame, the vast majority of memory devices were JEDEC standard SDRAM types of memory devices; correct?

A. Yes, that was my testimony.

Q. And -- but at the time of your book marked as Exhibit 1097, the mid 1990s, it sounds like back then you were writing a book because perhaps it was not quite clear at that point in time whether the Rambus DRAMs or the JEDEC DRAMs or perhaps even another type of memory device would win out in popularity.

Is that fair?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: Yes, there was a great deal of uncertainty. Between 1992 or so and 1997, there were probably 15 or 20 different proposals for different DRAM architectures of various sorts.

Everyone knew that what the industry had been doing vis-a-vis the fast page mode devices, which had been the staple for a decade, was no longer adequate. But it was not at all clear what direction the industry should go in, and that was the motivation for the book.

BY ATTORNEY CHANDLER:

Q. But by the 2004 to 2005 time frame, if I understand your testimony correctly, it sounds like the JEDEC SDRAM memory devices

had proven themselves the most popular and widely accepted; and the Rambus DRAM memory devices were not nearly as popular by that time frame.

Is that fair?

A. By that time frame, that's fair. Technically, the Rambus memory architectures were still superior to the SDRAMs vis-a-vis bandwidth in particular; but from a commercial perspective, you're correct.

Q. Please turn to page 337 of your book marked as Exhibit 1097. Let me know when you're there.

A. "Chip-Level Comparison." I am there.

Q. A person of ordinary skill in the art would have known about the chip-level comparison of the different types of DRAM described in your book in Chapter 9 starting on page 337 in Exhibit 1097.

Is that fair?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: Certainly, a POSITA in 2004-2005 would have been keenly aware that

the interfaces for these different memory types were all different and not interchangeable; and to the extent that, consequently, the POSITA would understand that a chip-level comparison of those interfaces would be required in order to make any sort of decision between one or another or how to use one or another, so in that respect, yes.

Having a comprehensive comparison, as I lay out in Chapter 9, of all of the different varieties, that would probably be not something a POSITA would have had the time or inclination to prepare themselves.

BY ATTORNEY CHANDLER:

Q. Please turn to page 353 of Exhibit 1097. Let me know when you're there.

A. System-Level Comparison, I am there.

Q. A person of ordinary skill in the art would have known about the system-level comparison of different types of DRAM as described in Chapter 10 of your book starting on page 353 of Exhibit 1097; correct?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: Generally speaking, to the same extent as we discussed for the chip-level comparison, the -- a POSITA would, again, be looking at a system-level comparison for understanding the relative merits of different DRAM architectures.

BY ATTORNEY CHANDLER:

Q. All right. Please go pretty much towards the end of Exhibit 1097 and sort of back up to page 809 and let me know when you're there.

A. 809.

Yes.

Q. Starting on page 809 of your book marked as Exhibit 1097, you include a copy of a Rambus DRAM data sheet that runs through page 840 of your book; correct?

A. Yes.

Q. On page 821 of your book marked as Exhibit 1097, you provide a description of the registers used by a Rambus DRAM to store configuration information; is that correct?

A. I'm sorry. Which page was that?

Q. 821.

A. Yes. I list -- the data sheet

that I copied into the book with permission of Rambus does list the register types, yes.

Q. So, for example, as shown in Table 7 on page 821 of Exhibit 1097, the register 0 of a Rambus DRAM stores the device type; correct?

A. That's what it says there.

Q. Register 1 of a Rambus DRAM stores the device ID, which is used to specify the base address for the memory device; correct?

A. That's what it says.

Q. Register 2 of a Rambus DRAM stores the delay, which is used to specify the CAS timing parameters; correct?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: CAS timing parameters, register 2; yes.

BY ATTORNEY CHANDLER:

Q. And there are a number of other registers listed in Table 7 on page 821 of your book marked as Exhibit 1097; correct?

A. Yes. They're all listed there.

Q. On page 822 of Exhibit 1097, the data sheet provides more detail about some of

the registers that were listed on the previous page in Table 7; correct?

A. It appears that way, yes.

Q. For example, at the top of page 822 of Exhibit 1097, it shows that the device ID field in register 1 of a Rambus DRAM as compared to address 35:21 of a request packet to determine if that particular memory device has been selected; correct?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: That's what it says there, yes.

BY ATTORNEY CHANDLER:

Q. As another example in the middle of page 822 of Exhibit 1097, it shows that the delay register 2 of a Rambus DRAM includes a byte 1 that sets a read delay that is normally 7-bus clocks, and it also includes a byte 3 that sets a right delay that is normally 1-bus clock; correct?

A. Right. And, again, all of this stuff is for the 16-megabit base, I believe, RDRAM.

///

(Exhibit Number 1069 was previously marked for identification.)

BY ATTORNEY CHANDLER:

Q. All right. Could you pull up Exhibit 1069, which I might not have previously put in the chat, so let me just put it in there. May be duplicative, but it's the --

A. I don't have that up, so it will be helpful.

Q. It's the same exhibit in both IPRs, and it's the paper written by Professor Jacob in 2002. It's in the chat. Let me know when it up on your screen.

A. I have that up on my screen.

Q. And have you reviewed Exhibit 1069, Professor Jacob's article about "Synchronous DRAM Architectures," dated December 10th, 2002?

A. I have read it all in past -- in the past. In this matter, I reviewed portions of it more extensively than other portions.

Q. All right. Please turn to page 2 of Exhibit 1069 and carrying over to page 3 where Professor Jacob discusses chip-select signals, and let me know when' you're there.

A. I'm on page 2.

Q. Professor Jacob explains on the bottom right of page 2 of Exhibit 1069 in the third sentence that "The chip-select bus contains a separate wire for every rank of DRAM in the system."

Correct?

A. And this is in the context of JEDEC-style organizations that he's referring to in the previous paragraph; yes.

Q. Is the description by Professor Jacob of the chip-select signal on the bottom right of page 2 of Exhibit 1069 consistent with the understanding of a person of ordinary skill in the art?

A. Again, a person of ordinary skill in the art in 2004-2005 would understand that for JEDEC-style organizations being discussed here in this page of Jacob's article, that for a plurality of ranks, there's a separate chip-select for each rank, generally speaking.

Q. And at the beginning of that paragraph in the bottom right of page 2, Exhibit 1069, the Professor Jacob states that the chip-select bus is essential in a

JEDEC-style memory system; correct?

A. Unless you only have one rank. In this case, it's only a single signal. But, yes, if you have a plurality of ranks, you need a plurality of chip-select signals and, therefore, a chip-select signal bus.

Q. And do you believe it's consistent with the understanding of a person of ordinary skill in the art that the chip-select bus is essential in a JEDEC-style memory system?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: Yes. Because JEDEC-style -- JEDEC-defined and standardized SDRAMs have chip-select inputs, you need to have a mechanism for feeding those signals, so it is essential. If you don't have some mechanism for triggering the chip-select inputs of the SDRAMs, they will not operate as you expect.

BY ATTORNEY CHANDLER:

Q. On page 3 of Exhibit 1069 in the first full sentence, Professor Jacob states:

"Even though all DRAMs in the system are connected to the same address and control buses and could,

in theory, all respond to the same request at the same time, the chip-select bus prevents this from happening."

Did I read that accurately?

A. Yes, you did. Yes, you have.

Q. Is that description by Professor Jacob consistent with the understanding of a person of ordinary skill in the art with respect to a JEDEC-style memory system?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: No, not entirely, because clearly there are memory subsystems with modules where all the DRAMs are not connected to the same address and control buses and that there is a -- in some circumstances, a plurality of address and control buses for different ranks. It's highly variable. This is a simplification for the purposes of pedagogy on Dr. Jacob's part.

BY ATTORNEY CHANDLER:

Q. To be clear, are you saying that in JEDEC-style memory systems, such as DDR and

DDR2, that different memory devices get different address lines?

A. No, that's not what I said.

Q. In the context of JEDEC-style memory systems, do you agree with the first full sentence on page 3 of Exhibit 1069?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: Again, as I said a moment ago, this sentence is a simplification and generalization for the purposes of pedagogy on Dr. Jacob's part. It is not universally true.

BY ATTORNEY CHANDLER:

Q. Is it true with respect to DDR SDRAM and DDR2 SDRAM?

A. Often but not always.

Q. So to be clear, your opinion is that it's typically the case in a JEDEC-style memory system that all the DRAMs in the system are connected to the same address and control buss and could in theory respond to all the same requests at the same time, but the chip-select bus prevents that from happening? Is that a fair summary of your opinion?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: So, again, talking about what a POSITA would understand in 2004 and 2005, a POSITA would understand that, depending on the size of the memory system employing JEDEC standardized memories, you could have a single memory bus -- I'm sorry -- a single control and address bus that wound its way to all of the memory devices; but you could also have a plurality of parallel address and control buses, each of which service a subset of the totality of JEDEC-compliant SDRAMs.

BY ATTORNEY CHANDLER:

Q. What was the more typical arrangement?

A. There was -- it was all a matter of what type of system we're talking about. There was no one typical arrangement.

Q. For UDIMMs and RDIMMs, there was no typical arrangement for the address lines, control lines and chip-select lines?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: That's not what I

said.
BY ATTORNEY CHANDLER:
Q. Were UDIMMs and RDIMMs common examples of memory modules in the 2004-2005 time frame?
A. UDIMMs, certainly.
RDIMMs, not so much, by my recollection; but, again, we'd have to look at some market data to see.
Q. For a single memory module with multiple ranks of memory devices, do you agree with the statement in the first sentence of page 3 of Exhibit 1069?
A. That single module --
ATTORNEY WARRICK: Objection; form.
THE WITNESS: That's a JEDEC standardized module of some type.
BY ATTORNEY CHANDLER:
Q. I would use Professor Jacob's phrase, which is a JEDEC-style memory system.
ATTORNEY WARRICK: Same objection.
THE WITNESS: So with that clarification, would you repeat the question,

please.
BY ATTORNEY CHANDLER:
Q. For a single memory module with multiple ranks of memory in a JEDEC-style memory system, do you agree that even though all the DRAMs in the system are connected to the same address and control buses and could in theory all respond to the same requests at the same time, the chip-select bus prevents this from happening?
ATTORNEY WARRICK: Objection; form.
THE WITNESS: I don't think that question is well phrased, because it's conflating multiple ranks on a JEDEC-style module and then a chip-select bus, which generally would refer to the bus that's outside of the module; but -- so I'm going to stop there.
BY ATTORNEY CHANDLER:
Q. Okay. I'm using the phrase as in Professor Jacob's paper from 2002, who I believe you said earlier was an expert in the field.
A. And he's a professor. So he's teaching here and is not saying things that are

necessarily universally true, but we're just saying he's trying to get across a particular point about the function of chip-selects and how they're used in systems. So I do not believe that he's making a general absolute statement about how all memory subsystems using SDRAMs are constructed, one module or multiple modules, one rank or multiple ranks.

Q. Let me ask more generally, then.

Do you believe a person of ordinary skill in the art would have the general understanding provided by Professor Jacob at the bottom of page 2 of Exhibit 1069, carrying over to the top of page 3, about chip-selects?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: Yes. Reading Professor Jacob's paper, a POSITA would understand that Dr. Jacob is talking about the function of chip-selects relative to the function of the address and control buses and how together they determine which memories do what in any particular circumstance.

BY ATTORNEY CHANDLER:

Q. Is it fair to say that Professor

Jacob is teaching that it's normal or common for all of the memory devices on a memory module that receive the same address signal and the same command signal, even if those memory devices are in different ranks?

A. I think it is understood by a POSITA that that's certainly possible, if not common, but not necessarily true.

Q. And what Professor Jacob is teaching in the bottom of page 2, carrying over to the top of page 3 of Exhibit 1069, is even though it's common for all the memory devices to receive the same address and command signals, despite being in different ranks, there is a chip-select wire for each rank of memory devices that enables one rank of memory devices to respond to a read or write command while the other ranks are not selected to respond to the read or write command.

Is that a fair summary of what Professor Jacob is trying to teach here with this paper?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: It's a fair

summary. And, in particular, the important aspect is that when there's multiple ranks, one of the chip-selects is active and the others are not active in order to get one rank to perform an operation and the other ranks to not perform the same operation.

BY ATTORNEY CHANDLER:

Q. Turn to page 7 of Exhibit 1069 and let me know when you're there.

A. 7? I am there.

Q. On page 7 of Exhibit 1069 on the left side starting at Section 1.3, there's a description of contemporary DRAM architectures; including in Section 1.3.1 DDR SDRAMs; and then in 1.3.2, Rambus DRAMs; correct?

A. Correct.

Q. And in Section 1.3.1 on page 7 of Exhibit 1069, Professor Jacob states that DDR SDRAMs double the bandwidth by transferring data at both edges of the clock; correct?

A. Double the data rate relative to SDRAM -- SDRAMs is what's missing from that sentence. And it's relative to both -- it's twice per clock period. The transmission of the data is not relative to the edges of the clock

but relative to edges of the data strobe.

So, again, for succinctness, Professor Jacob is taking a few liberties with the precision of his statements.

Q. And is everything that you just said in your last answer something that you believe a person of ordinary skill in the art would have understood?

ATTORNEY WARRICK: Objection to form.

THE WITNESS: As we have discussed many times, the -- in 2004 and 2005, a POSITA would have been familiar with double data rate SDRAMs and, therefore -- and how they operate. So, yes.

BY ATTORNEY CHANDLER:

Q. Professor Jacob goes on to state in the middle of Section 1.3.1 on page 7 of Exhibit 1069, that "DDR DRAM are very similar to single data rate SDRAM in all other characteristics."

Correct?

A. He does say that. I disagree with it, but he does say that.

Q. And then in Section 1.3.2 on the

Samsung Ex. 1095, p. 205
Samsung Electronics Co., Ltd. v. Netlist, Inc., IPR2023-00455

bottom left of page 7 of Exhibit 1069, Professor Jacob discusses Rambus DRAM abbreviated RDRAM; correct?

A. That is the first of the three types of Rambus DRAM that he discusses in his paper.

Q. And the three types of Rambus DRAM that he discusses in Exhibit 1069 are RDRAM, concurrent RDRAM and direct RDRAM; correct?

A. That's correct, yes.

Q. In Section 1.3.2 at the bottom left of page 7 of Exhibit 1069, Professor Jacob explains that Rambus DRAM:

"Does not use dedicated lines for address, control, data and chip-select-select signals -- but, instead, the bus is fully multiplexed, which means that address, control, data, and chip-select-select information all travel over the same set of electrical wires but at different times."

Correct?

A. That's what he says. I don't think it's particularly accurate.

Q. Do you think the description that Professor Jacob provided that I just read from the bottom of page 7 of Exhibit 1069 about Rambus DRAM was consistent with the understanding of a person of ordinary skill in the art?

A. No. I think the person of ordinary skill that did happen to know about the original RDRAMs would recognize that there's no chip-select information in that architecture, that everything is address-based.

Q. When you say everything is address-based, there are certain address signals that select the chip?

A. As we saw it when we looked at the RDRAM data sheet that was attached to my book, we saw that the register defined the base address of -- that a particular RDRAM would respond to.

Do you remember that?

Q. Yes.

A. Okay. So the -- there is no chip-select-select signal as it exists in any of

the JEDEC standardized memory devices; instead, there is only the -- the memory controller throws the address out there. And whichever RDRAM matches the address or the -- that the accessed address is within the range of that RDRAM, that RDRAM says, oh, it's for me; I'm going to do something. So there's no chip-select signal, and there's no chip-select information per se in the command packet for that generation of RDRAM.

Q. But as indicated by Professor Jacob, and if I understand your explanation correctly, with Rambus DRAM, it's still possible that only a subset of the memory devices are selected to perform a read or write operation; correct?

A. There is, in fact, a single one that, if everything is programmed correctly -- it's a caveat -- that a single RDRAM will respond to a command, based purely on a decoding of the address and no additional information other than the address.

Q. But regardless of whether you call it address or something else, the net result is that one or more chips are selected to

perform the memory commands in a Rambus DRAM system; correct?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: Again, I'm going to take issue with your terminology.

The memory device is not selected by the memory controller, as is typical when we use the term "chip-select," as a signal that goes from the memory controller to the individual DRAM or DRAMs.

In this case, the DRAM autonomously decides that the transaction that has been requested can only be handled by it. And it's an internal decision based on an address information, which is profoundly different from a chip-select information or -- that is being inaccurately called out here by Jacob.

BY ATTORNEY CHANDLER:

Q. In fairness, the Rambus DRAM are not autonomous. They don't decide on their own whether to --

A. Yes, they do. They do. They receive a packet that has a --

(Simultaneous cross-talk.)
Q. The memory controller determines the address; right? The memory controller says, I want to write to this address.
A. Yes, but it doesn't say --
ATTORNEY WARRICK: Objection to form.
BY ATTORNEY CHANDLER:
Q. Go ahead.
A. The memory controller doesn't say, I want the third DRAM to respond.
It says, I have an address; whoever is responsible for this address, deal with it.
Q. But let's back up a little bit.
It's the memory controller that programs the registers in the Rambus DRAM memory devices; right?
A. Correct.
Q. So the memory controller programs the Rambus DRAM memory devices with those registers, and then the memory controller sends out the address information that's going to select one or more of the Rambus DRAM memory devices. So it's the memory controller that is

in control; right? It's not like the Rambus DRAMs are totally autonomous; it's the memory controller that's controlling things.

A. In this --

ATTORNEY WARRICK: Objection; form.

THE WITNESS: In this particular architecture, the RDRAMs are essentially autonomous and that when the -- granted, the memory controller has initialized the memory subsystem. And you keep saying "one on more RDRAMs respond." Exactly one RDRAM responds to any transaction on the channel.

BY ATTORNEY CHANDLER:

Q. The memory controller can program the register in the Rambus DRAM; right? So it's up to the memory controller to decide how those registers in the RD program are programmed and, therefore, how the memory devices will act.

The memory devices aren't autonomous in the sense that they can disregard what the memory controller tells them. The memory controller programs them. The memory controller sends the address signal. And then the memory devices are required to follow what

the memory controller has done; right?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: But they're also autonomous in that the memory devices determine when to respond to the request. And there is a profound conceptual difference between an address and the chip-select. And you see that pervasively throughout the JEDEC standardization -- standards for SDRAMs and for all other devices that have chip-select inputs. They were conceptually and temporally -- not -- they are conceptually different from addresses.

In this case, for the RDRAMs being described in this paragraph, there are no chip-select signals; there's no chip-select signal lines. The memory controller, when it's sending out an address as part of a packet, a command packet, it's not even cognizant of which memory is going to respond, because that's handled a priori in the programming of the registers.

So the whole concept of chip-select is dramatically different in this generation of RDRAMs.

BY ATTORNEY CHANDLER:

Q. In your opinion, but apparently not in the opinion of Professor Jacob. Fair?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: I don't think this is a matter of opinion. This is a matter of fact. This is exactly how the RDRAMs operate -- operated, since they don't exist anymore. And the fact that Jacob has preferred to cast this -- using the language of SDRAMs instead of the language of RDRAMs -- again, is either pedagogical or an error. And you can decide which. But it is, in fact, not accurate.

BY ATTORNEY CHANDLER:

Q. I want to push back on your statement about Rambus DRAM being autonomous.

When you say they're autonomous, the reality is that the memory controller first programs them and the memory controller knows how they're going to act based on that programming. And then the memory controller later will send signals, including address information, and the memory controller knows how the Rambus DRAM will act in response to those

signals. And so it's not really fair to say that the memory device is autonomous.

A. Well --

Q. The memory device is still being controlled by the memory controller, and the memory controller in its own way is able to select the memory devices that it wants.

ATTORNEY WARRICK: Objection to form.

THE WITNESS: The question is: What do you mean by "autonomous"?

If you get into an autonomous vehicle today and you say, "Go home," is the car autonomously taking you home or is it responding to your command?

And the same distinction is happening within the Rambus RDRAMs in that the RDRAMs are watching for control packets. When they see a control packet, they look at the address in that control packet and decide whether it's for me or not. That's purely autonomous.

If the memory controller sent out an address that was outside of the range of all of the memories on the channel, no one would

respond. Nothing would happen.

The response to the command packet and the decoding of the address therein and determining what to do and when to do it -- that's the critical part here -- is purely localized within the RDRAM. And the memory controller accepts the result. It gets back an indication when that data is going to come back.

Or in particular, the memory device can mask the entire transaction and say, I can't do this right now. And if that's not a sign of autonomy, then, you know, I'm not sure what is.

BY ATTORNEY CHANDLER:

Q. You just referred to a packet. And on page 7 of Exhibit 1069 on the upper right, Professor Jacob also refers to a packet transaction.

What's a packet transaction?

A. A packet transaction would be a transaction that is initiated by a command packet.

Q. Can you explain a little bit more. Seems a bit circular.

A. Well, the -- there are

transactions. In SDRAMs, transactions are initiated by commands on the command bus and -- and the chip-select; and the details of it are determined by the address bus.

In Rambus-style memory devices, such as the RDRAM, concurrent RDRAM or direct RDRAM, the control information is not sent over individual wires but are aggregated into multiple time periods over a multiplexed command bus, and they vary between the different Rambus devices and that each signal wire has multiple purposes at different points in time, whether it's command or address or something else, masked in some cases.

Q. Are the packet transactions used by Rambus memory devices transmitted on electrical wires using signals?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: Yes.

BY ATTORNEY CHANDLER:

Q. On page 7 of Exhibit 1069, in both the heading 1.3.2 that we looked at as well as the text, there are those three different types of Rambus DRAM: The original RDRAM,

concurrent RDRAM and direct RDRAM.

And my question is: In your opinion, would a person of ordinary skill in the art have known about those three different types of Rambus memory devices?

A. By 2004-2005, the original RDRAM was long gone. The concurrent RDRAM was also gone, and direct RDRAM was the principal Rambus device that was in the marketplace. And there's also the XDR RDRAMs that were also in the marketplace that's referred to in, I believe, one of the patents at issue here. Let me double-check that.

I think it's Perego that refers extensively to XDR.

Q. On page 7 of Exhibit 1069 on the right side in the middle paragraph, Professor Jacob explains that the original Rambus DRAM design was changed because it did not have separate segments of the bus dedicated to separate functions and, thus, it was not considered well suited to the TC main memory market; correct?

A. Yes, it says that.

Q. Is that consistent with your

understanding?

A. Well, he's citing my work. So, presumably, he found it somewhere in there.

The original base RDRAM, the autonomy of the DRAMs was difficult to control by the memory controller, and the scheduling of the bus was very challenging. So in that sense, he is accurate with regard to the original RDRAM.

Q. And then Professor Jacob goes on to explain on the right side of page 7 of Exhibit 1069, in the second paragraph, that the next generation of Rambus memory called concurrent RDRAM had a "bus that was divided into separate address, command and data segments reminiscent of a JEDEC-style DRAM organization."

Correct?

A. I don't think that that's an accurate characterization of "concurrent." I think it's another instance where he's made a mistake, but we'd have to look at a concurrent RDRAM data sheet to verify that.

Q. In concurrent RDRAM, the width of the data bus segment was 1 byte, or 8 bits; correct?

A. 8 or 9 bits; yes.

Q. And then Professor Jacob goes on to explain on the bottom right paragraph of page 7 of Exhibit 1069, that the next generation of Rambus DRAM called direct RDRAM, increased the width of the data segment of the bus to 2 bytes, or 16 bits; but the segments remained separate and dedicated similar to a JEDEC-style organization.

Correct?

A. Which paragraph are you reading from? The last paragraph on page 7? Right.

Q. Yes.

A. Let me read that again.

(Witness reviews document.)

Yeah, so this paragraph or this portion of this paragraph explicitly mischaracterizes the direct RDRAM control structure and that the -- it calls the address segment 5 bits and the control segment 3 bits. That's completely inaccurate.

In fact, the control portion of the direct RDRAM architecture has 3 bits for column commands, including column commands and column addresses, and 3 bits for row commands

and row addresses.

So his characteristics of those 5-bits and 3-bit segments, as being for address of control, that's just flat-out inaccurate. Not a matter of interpretation or pedagogy.

Q. A person of ordinary skill in the art knew about Rambus direct RDRAM; correct?

A. We have agreed that based on the timing and the reference in, for example, Perego, that, yes, a POSITA in 2004-2005 would have familiarity with direct RDRAM.

Q. Could you turn back to Exhibit 1070, the Jacob textbook, and go to page 21. Let me know when you're there.

A. Okay. Which page again, please?

Q. 21.

A. At the very beginning?

Q. Yes.

A. I'm on page 21.

Q. On page 21 of Exhibit 1070, Professor Jacob compares SDRAM and Rambus architectures both in the figure at the bottom of the page as well as in the text starting at the bottom left and carrying over to the right side of the page; correct?

A. Does appear that way.
Q. And as shown on the left side of the figure on page 21 of Exhibit 1070, an example of SDRAM is DDR memory, which, as we discussed, had been standardized by JEDEC; correct?
A. That's how he's labeled it, yes.
Q. Professor Jacob explains on the right side on page 21 of Exhibit 1070 that Rambus uses fewer address and command pins than SDRAM and, thus, incurs an additional latency at the command level; correct?
A. That's what he says.
Q. And a person of ordinary skill in the art would have understood that about the Rambus architecture; correct?
A. No, I don't think a POSITA in 2004-2005 would recognize that the delay from the first portion of a command arriving at a DRAM on a direct RDRAM channel to the last portion of that command arriving on the same portion or the same column or row command bus constitutes a -- an additional latency.
Q. Dr. Jacob explains on the right side of page 21 of Exhibit 1070 that Rambus's

longer channel results in longer read command latencies and longer bus turnaround times; correct?

A. There is a longer -- let me restart that answer.

The appropriate comparison is the maximum length of the direct RDRAM channel. And the longest signal trace length in a memory -- JEDEC SDRAM-compliant multimodule memory implementation, as shown in Figure Ov.7 on the left-hand side.

In fact, four DDR SDRAMs, the maximum signal path length for address is going to be shorter than the maximum channel length for a direct RDRAMs; but in direct RDRAM systems, if you don't have a full-length channel, you don't suffer this problem. And most direct RDRAM channels would have been significantly shorter than the maximum length.

So the comment with regard to longer read command latencies is not universally true and, in fact, most often not true.

The longer bus turnaround times is also inaccurate, because in the direct -- in the SDRAM and DDR SDRAM memory systems, the

clock cycle is very much longer. So a single cycle of bus turnaround time is much longer than a comparable turnaround time on the direct channel.

So both halves of this sentence are, again, sometimes true -- in the worst case, probably true -- but in the typical case, not likely to be true.

So, again, from a pedagogical perspective, the sentence is not false; but it is a simplification of the reality of the situation.

Q. In the figure on the bottom of page 21 of Exhibit 1070, Professor Jacob compares a JEDEC-style memory system on the left with 8 memory devices to a Rambus memory system on the right is 8 memory devices; right?

A. Yes, it does.

Q. And Professor Jacob teaches that the JEDEC-style memory system on the left has a short and wide channel; whereas, in comparison, the Rambus-style memory system on the right has a long and narrow channel; correct?

A. He says that, but it's not precisely accurate. The length of the signal

lines for the command and address and chip-select on the memory system on the left, the SDRAM memory system, is the full width of the module plus the length of the trace from the controller to the start of the module, which in contrast for the Rambus style -- for the direct Rambus memory system, the maximum length of the channel is two module lengths.

And these modules are the same size, because the RIMMs, which are the Rambus module, are the same width as the DIMMs -- the DDR and SDRAM DIMMs that were in place at the time.

So the difference in the trace length between -- the worst-case trace length between these two examples is relatively small. And certainly if you end up with a single-module memory system, in both cases, the Rambus-style architecture will be better. It will have a shorter worst-case signal path length.

Q. But most computers have at least two memory slots or two memory modules; right?

A. "Most" is a, I think, an overgeneralization, particularly since the Rambus -- direct Rambus memory systems, the

memory controllers for that typically had a single controller for each module, which was practical, because the total number of signals was very much smaller.

So for the same number of pins on the controller, you could have two Rambus channels in fewer pins than you had one x64 SDRAM memory system as per the figure on the left of Figure O.v.7.

So for most -- it's actual circumstances where the apples-to-apples comparison is a comparable number of pins on the controller; the direct Rambus JEDEC-style memory system is preferred, has shorter maximum signal lengths.

And in that respect, Jacob's sentence in the middle of the right column of page 21 is not accurate for most cases. It's pedagogically a reasonable thing to teach, but it's not necessarily accurate.

Can we take a break, please?

Q. Can you go a few more minutes so we can sort of finish the discussion on this page, or do you want to take a break right now?

A. It's been almost an hour and a

half, so I would prefer we -- if it's one more question, go for it. If it's more than one, we should stop.

ATTORNEY CHANDLER: I won't make any promises, so let's take a break.

THE WITNESS: Okay. Break it is. Ten minutes, please.

THE VIDEOGRAPHER: Off the record at 3:21 p m. Pacific Time.

(Recess taken from 3:21 p.m. to 3:35 p.m.)

THE VIDEOGRAPHER: On the record at 3:35 p.m. Pacific Time.

THE WITNESS: May I add a sentence to my last answer?

BY ATTORNEY CHANDLER:

Q. Yes. And I was actually going to ask you more generally if there are any corrections or clarifications you'd like to make to any of your testimony earlier today to far.

A. So not generally. But with regard to this last interchange about Jacob's writing, it's really difficult to make real apples-and-apples comparisons across memory types. And I'm not criticizing Jacob for making

these bold generalizations, because he's writing a textbook.

But when we're doing -- in this venue when we are trying to be as precise as possible, it's important to really try hard to think about what the proper comparison really is.

And I'm sure you'd find it in my own writing if you looked hard enough where in order to fit into a reasonable-sized-length article, you make some statements that are true most of the time or even some of the time or that get a particular point across.

But here when you're asking me questions about a comparison between an SDRAM and a direct Rambus memory system, it's a very complicated comparison. That's all.

Q. Would it be fair to say that a person of ordinary skill in the art would understand the trade-offs between a DDR memory system and a Rambus memory system, as summarized, for example, on page 21 of the Jacob textbook marked as Exhibit 1070?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: A person of ordinary skill in 2004-2005 on first blush would understand some of these trade-offs; and as a detailed comparison was undertaken towards a specific design, the trade-offs would clarify and become more nuanced.

So the trade-offs expressed here by Jacob on page 21 are a very high level and not necessarily accurate in most or even many circumstances.

BY ATTORNEY CHANDLER:

Q. On page 21 of Exhibit 1070, is it fair to say that one of the trade-offs that Professor Jacob is trying to convey is that a DDR memory system as shown in the bottom left has what he would characterize as a short and wide channel; whereas, a Rambus-style memory system, as illustrated on the right, has what he would characterize as a long and narrow channel?

At a high level, do you think a person of ordinary skill in the art would understand that difference between a DDR-type memory system and a Rambus-type memory system?

A. Yes. A person of ordinary skill in the art would understand that the topologies

are dramatically different, but that person of ordinary skill would also recognize that an SDRAM memory system of the style shown on the left consumes about 120 pins on the controller; whereas, at Rambus-style architecture on the right consumes about 30 pins.

And, therefore, if your particular design has a shortage of pins or if the cost of the pins is factored into the equation, it completely upsets that simplistic comparison that Jacob undertakes here.

Q. In fairness, on the right side of page 21 of Exhibit 1070, about -- several sentences up from the bottom, Jacob explains that the width and depth of the memory channels impact the bandwidth, the latency, the pin count and various cost components of the respective memory systems; correct?

A. But what he doesn't say is that the consequence of those parameters being different means that his previous statement is not accurate all the time.

Q. Would it be fair to say a person of ordinary skill in the art would understand that if you change the width and depth of the

memory channels, that there will be impacts on bandwidth, latency, pin count and cost components of the memory system?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: Yes. A POSITA reading this entire section would understand that the entire trade-off is complicated and relies on a great many factors and that generalizations, such as about the longer channel, doesn't necessarily hold in their particular case.

So, again, you can't rely on just one sentence within a longer section about this comparison.

BY ATTORNEY CHANDLER:

Q. On page 23 of Exhibit 1070 in the table in the middle of the page labeled Table Ov.3, Professor Jacob provides the comparison of SDRAM, DDR SDRAM and direct Rambus DRAM memory systems; correct?

A. Yes, I see that.

Q. And in this comparison on page 23 of Exhibit 1070, the DDR memory system in the second row had a better peak bandwidth than the

direct Rambus DRAM memory system; correct?

A. That's what he shows here, yes.

Q. And the DDR memory system in this table on page 23 of Exhibit 1070 has a sustained bandwidth that's nearly identical to that of the direct Rambus DRAM system -- DRAM system; correct?

A. But, again, consuming or utilizing a great many more pins on the memory controller. I'm not sure where he got the 117 number for the direct Rambus. It's not at all what I remember, but I'll take his word for it for now.

Q. And do you believe a person of ordinary skill in the art would have known about these types of comparisons of DDR memory systems to Rambus-style memory systems?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: I'm sorry. I was trying to digest the table. Would you please repeat the question for me.

BY ATTORNEY CHANDLER:

Q. Do you believe a person of ordinary skill in the art would have known about

these types of comparisons of DDR memory systems to Rambus-style memory systems along the lines of what's shown in the table on the middle of page 23 on Exhibit 1070?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: So certainly a POSITA in 2004-2005 embarking on a specific design where the choice of memory type was a decision to be made would go through an exhaustive comparison, much more detailed than would be shown here in Table Ov.3 to fully understand for the particular design being undertaken what the bandwidth, cost and power, for example, trade-offs would be and physical area as well, obviously.

(Exhibit Number 2025 was previously marked for identification.)

BY ATTORNEY CHANDLER:

Q. Could you please pull up Exhibit 2025, which -- I don't think we've talked about before, and I don't think I've put in the chat before.

So let me go ahead and just put it in the chat, even if this may be redundant,

so that you can see it. And let me know when you have it up on your screen.

A. I have it on my screen.

Q. Have you reviewed Exhibit 2025 before, the Rambus direct RDRAM data sheet?

A. There was certainly -- there was certainly a time when I knew it very well. I have looked at parts of it relatively recently, but I haven't studied it carefully in the last week.

Q. On page 3 of Exhibit 2025, which, to be clear, is the same exhibit in both IPRs, Table 1, provides the pin description for a Rambus direct RDRAM memory device; correct?

A. It's -- Table 1 is described as "Pin Descriptions."

Q. And you see in the middle of Table 1 of Exhibit 2025, there's a row for DQA; and then at the bottom, there's a row for DQB; and then directly above that, there are some rows for RQ.

A. Yes.

Q. The Rambus direct RDRAM memory device had dedicated data lines for the data signals DQA and for the data signals DQB;

correct?

A. That's what this table shows.

Q. And then separate and apart from the DQA and DQB data lines, the Rambus direct RDRAM memory devices also had dedicated lines for RQ0 through RQ7, which carried the signals containing address and control information; correct?

A. What this table shows is that those RQ0 to RQ7 are conceptually divided into two portions, one for row axises and the other for column axises, as we discussed before the break.

Q. RQ0 through RQ7 are separate lines from DQA and DQB; correct?

A. Yes, they are.

Q. And RQ0 through RQ7, just to treat them as a group -- I understand that there may be a subdivision; but if you take RQ0 through RQ7 as a group, they would carry the signals containing address and control information; correct?

A. Yes. Those eight signal lines carry all address and control information for row axises and column axises respectively.

Q. And to be clear, then, the Rambus direct DRAM memory devices do not have dedicated address lines for address signals in the way that a JEDEC-style memory system would have; correct?

A. That's correct. The -- on the RQ0 to RQ4 and RQ5 through RQ7, there are packets of command -- command packets, which include command op codes and addresses for the corresponding row and column axises.

Q. The Rambus direct DRAM memory devices do not have dedicated control lines for control signals in contrast, for example, for the JEDEC-style memory system?

A. The lines -- the traces on the channel are -- carry both control and address on each of them.

Q. So, for example, the DDR memory device would have a pin dedicated to a row address strobe signal while a Rambus direct DRAM does not; correct?

A. You have to be careful, because for the JEDEC standardized, SDRAMs of all varieties, we have signal names that are archaic, persisting in the definition of the

memory device. So when you refer to a row address signal, that is the name of one signal in the command bus. And it by itself doesn't signify anything in particular; just like RQ7 doesn't signify anything in particular by itself, the same idea applies to the JEDEC standardized memory devices as well.

Q. And just to be clear, I think you said "row address signal," and I think my question was --

A. I misspoke. Row address -- the RAS signal, row address, which is a -- it's not called that anymore, but its history is that it came from a row address strobe signal that had that name. It got, over the decades, turned into an acronym, RAS; and that name, RAS, persists even though it's one bit of a command.

So I apologize if I misspoke with the first answer.

Q. All right. So to be clear, a DDR memory device has a pin dedicated to a RAS signal and has a pin dedicated to a CAS signal; whereas, a Rambus direct DRAM does not; is that fair?

A. That is fair.

Q. Could you pull up Exhibit 1064 which is the JESD79-2 standard for DDR2 SDRAMs that we've discussed a little bit, and let me know when you have it in front of you.

A. I'm sorry. I missed the exhibit number, please.

Q. 1064.

A. 1064. There it is.

Q. This is the JESD79-2 standard for DDR2 SDRAMs, dated September 2003.

Do you have it in front of you?

A. I do.

Q. On page 6 of Exhibit 1064 is a table under the heading "Package Pinout & Addressing, Input/Output Functional Description."

Correct?

A. Yes.

Q. And starting with the first line on page 6 of Exhibit 1064, CK and CK-bar are differential clock inputs for DDR2 memory devices; correct?

A. Yes.

Q. With DDR2 memory devices, all address and control input signals are sampled on

the crossing of CK and CK-bar; correct?
A. That's what it says, yes.
Q. And a person of ordinary skill in the art would know and understand that; correct?
A. Yes.
Q. More generally, as I think we've discussed, but just to be clear, would it be fair to say that a person of ordinary skill in the art would know and understand what's on page 6 of Exhibit 1064 in this table that provides the input/output functional description for DDR2 memory devices?
ATTORNEY WARRICK: Objection; form.
THE WITNESS: So this describes all the pins; it doesn't really describe the full functional description of the memory device. But that aside, the textual explanations would be clear to a POSITA of the 2004-2005 time frame, and they would have no difficulty in understanding what each of these signals of the SDRAM are for.
BY ATTORNEY CHANDLER:
Q. A couple of lines down on page 6 of Exhibit 1064 is a row for the chip-select

input, abbreviated CS; correct?

A. Yes, I see that.

Q. And for DDR2 memory devices, the chip-select input provides for external rank selection on systems with multiple ranks; correct?

A. That's what it says.

Q. And for DDR2 memory systems, the chip-select input is considered part of the command code; correct?

A. Yes, that's what it says.

Q. A little bit further below that on page 6 of Exhibit 1064 are other command inputs called RAS, CAS and WE, which along with the chip-select, define the command being entered into the DDR2 memory device when the clock signals cross; is that fair?

A. We wouldn't wall it "WE." We'd call it "write enable." But sure. Go ahead.

Q. So is it correct that as shown on page 6 of Exhibit 1064, the other command inputs called RAS, CAS and write enable, along with the chip-select, define the command being entered into the DDR2 memory devices when the clock cycles cross?

A. Yes, that's generally true.
Q. And RAS, I think you said earlier, stands for row address strobe, at least historically; is that correct?
A. Historically. Presently, it doesn't anymore; it's just called RAS and CAS and write enable.
But as it says here, they are all part of a command bus; and their historical meaning of row address strobe and column address strobe and write enable have been lost to antiquity.
Q. Now, page 6 of Exhibit 1064 lists a number of other signals received by a DDR2 memory device that do not define the command; correct?
A. Yes, that's correct.
Q. For example, a DDR2 memory device receives an ODT signals, which stands for on-die termination, but that signal is not used to define the command; correct?
A. That's correct. It does not contribute to the definition of the command; but it is a command signal -- it is a control signal; it's not a data signal.

Q. DDR2 memory devices also receive the DM signal which stands for data mask. And that's another example of a signal that's not used to define the command; correct?

A. Yes.

Q. DDR2 memory devices receive DQ data signals and DQS strobe signals, but those signals are not used to define the command; correct?

A. Yes, that's correct.

Q. In the middle of page 6 of Exhibit 1064, there's a row for bank address inputs, labeled BA0 to BA2; correct?

A. Correct.

Q. The BA0 to BA2 pins can receive bank address signals defining which bank inside of a DDR2 memory device that a read or write command applies to.

Is that fair?

A. It's not precisely how it's worded but, yes, it's accurate.

Q. And then for mode register set commands, the same BA0 to BA2 pins can also carry information determining which of the mode registers inside the DDR2 memory device are

accessed.

Is that fair?

A. Accessed as in being written; yes.

Q. And then a little further down on page 6 of Exhibit 1064, there are individual address inputs, A0 to A15, for the DDR2 memory device; and those address inputs, A to 015, are separate from the BA0 to BA2 bank address inputs; correct?

A. Correct. And the address bits convey data that's going into the mode registers; and they also convey some control information, such as the precharge bit.

Q. So you're referring to the line that's labeled A10 and in certain circumstances, carry a precharge command for DDR2 memory devices; correct?

A. It's more of a precharge modifier to a read or write command as opposed to a command in its own right. So it's a nuanced difference. Perhaps a difference without a distinction -- I don't know -- or the vice versa.

Q. And the address inputs A0 to A15

can carry either row address or column address for the DDR2 memory devices, depending on the type of command.

Is that fair?

A. Yes. And elsewhere there is a command truth table that specifies exactly for each memory type -- for each size and width of memory, which pins are carrying which piece of information for row axises and column axises.

Q. The next row down on page 6 of Exhibit 1064 shows that for DDR2 memory devices, there are also data input/output lines labeled DQ, which are separate from the address and control lines; correct?

A. Yes, they are separate.

Q. And the next row down on page 6 of Exhibit 1064 shows that DDR2 memory devices also have DQS strobe lines; correct?

A. Yes, they do.

Q. Now, we talked a little bit earlier about single data rate SDRAMs, and those older single data rate SDRAMs do not have DQS strobe signals; correct?

A. That's correct. That's a very important addition between SDR and DDR -- SDRAM.

Q. And the purpose of the DQS strobe signal for DDR2 memory devices is to indicate to the recipients that the data signal is present and valid. Is that fair?

A. Where are you getting the invalid part?

Q. From our friend, Professor Jacob, Exhibit 1069, page 2, note 2.

A. Okay. So, again, a pedagogical simplification. The DQS indicates when to try and capture the data. It doesn't guarantee that the data is, in fact, valid and have sufficient signal integrity to be captured.

If everything is designed properly, the two are synonymous; but it is the definition of the DQS signal that now is when you should try to capture it. Or that's at least the case for write data for the DRAMs, for the phase of the signal is different for read data.

Q. The DQS strobe signal travels from the source to the destination along with the data signal; correct?

A. Yes. And there are rules about how different those trace lengths can be.

Q. The DQS strobe signal for DDR2 memory devices has a preamble; correct?

A. If we want to pull up one of the timing diagrams, we could talk more precisely about the relative location of edges on DQS relative to data.

Q. Sure. How about if you look at page 60 of Exhibit 10 -- I'm sorry. Not page 60 -- page 26 of Exhibit 1064.

A. "Data Output (Read) Timing."

So that these are signals being output by the SDRAM, the DDR SDRAM in this cease, DDR2 SDRAM in this case. Sorry.

Q. So a person of ordinary skill in the art would understand that DQS strobe signals have a preamble; correct?

A. Yes, and the different versions of the JEDEC standards define the preamble differently.

Q. The preamble for the DQS strobe signal is transmitted before the actual data signals; correct?

A. Again, it depends on whether you're talking about reads or writes and whether the recipient is the memory controller or the

DRAM. But that is, again, a statement that is probably pedagogically accurate, if not precisely accurate in every respect.

Q. To be clear, the word "preamble" is referring to the beginning.

Is that fair?

A. Yes, and the start of the preamble is always before the start of the first data, regardless of whether it's read data or write data. But it's not always all the way before.

Q. The preamble for the DQS strobe signal lasts approximately one full clock cycle, according to DDR2 standard.

Is that fair?

A. We would have to look at the specification for TRPRE, which is the specified time for the preamble from its formal start to the first rise in transition of DQS; but this figure would indicate that it's approximately one full cycle. It could be slightly less or slightly more, depending on how the TRPRE is defined.

Q. And if you search for TRPRE, you will see on page 65 of Exhibit 1064 that the

preamble for the DQS strobe signal for a read is specified to be between 0.9 and 1.1 clock cycles; correct?

A. Exactly. So it could be slightly less; it could be slightly more.

Q. And during the length of the preamble of the DQS strobe signal, which, as just discussed, will be approximately one full clock cycle, the DQS signal is driven low while the DQS-bar signal is driven high; correct?

A. In Figure 23, based on read data -- in other words, data coming out of the DRAMs -- the DRAM drives DQS low and DQS-bar high for the bulk of the preamble period.

Q. And would that also be true in the right direction, that you have a preamble of the DQS strobe signal that's approximately one clock cycle long where the DQS signal is low and the DQS-bar signal is high?

A. If you look at Figure 29 of that DDR2 JEDEC standard, you see that the DQS signals are defined differently for write data than for read data.

Q. But is it still the case that for write data, there's a preamble to the DQS strobe

signal where the DQS signal is driven low and the DQS-bar signal is driven high?

A. What Figure 29 is depicting is that in order for the DRAM to be guaranteed to capture the data, the DQS signal has to be stable in its preamble state for a given period of time prior to the first rising edge of DQS and the first falling edge of DQS-bar.

Q. And so, for example, in Figure 30 of the DDR2 standard on page 30 of Exhibit 1064, we see a preamble for the DQS strobe signal where DQS is low for approximately one clock cycle, while DQS-bar is high for approximately one clock cycle before the first piece of write data.

Is that a fair description of what's shown in Figure 30?

A. That's shown in Figure 30. If we look at page 65 again, we see that the write preamble is necessarily more than one-quarter clock cycle. It can be any amount of time longer than that.

Q. So for both a read command and a write command in the -- to a DDR2 or from a DDR2, memory system that will be a DQS strobe

signal with a preamble of a certain length where the DQS signal is low and the DQS-bar signal is high; is that fair?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: Yes; otherwise, it's not guaranteed that the DRAM for write data will be able to capture the -- the data properly. And for read data, it's saying that the DRAM will provide enough of a preamble that will allow the memory controller to find the center of the data eye.

BY ATTORNEY CHANDLER:

Q. Please turn to page 12 of Exhibit 1064. Let me know when you're there.

A. I'm on page 12.

Q. As shown on page 12 of Exhibit 1064, DDR2 memory devices include registers, one of which is called the mode register; correct?

A. I think that -- yes, it refers to this particular register as the mode register; and the other one is called the extended mode register.

So the term "mode register"

refers specifically to this register, even though both registers are, in fact, mode registers.

Q. The mode register of the DDR2 memory device is normally programmed during initialization; and the programmed values can then be used during normal operation.

Is that fair?

A. It's stronger than that. It's required to be set during initialization.

Q. The values for the mode register are carried by the address lines going to the DDR2 memory device; correct? During the initialization process.

A. When --

ATTORNEY WARRICK: Objection; form.

THE WITNESS: When the command bus indicates a mode register set command, the bank address bits show which mode register of the two is being programmed, per the box in the lower left corner of figure on page 12; and the other contents of the fields of the mode register are provided on address A0 through A12 is the last one that's useful. The rest are

reserved for future use.
BY ATTORNEY CHANDLER:
Q. For example, CAS latency can be programmed in the mode register of a DDR2 memory device during initialization; correct?
A. The CAS latency has to be programmed during the initialization phase of -- it's getting the memory system and the SDRAMs functional and operational.
Q. And how would you explain what CAS latency is?
A. It is defined within the four corners of the standard.
Q. And can you explain that a little more.
A. There are figures and tables that show what the CAS latency is relative to commands and data for -- and its applicability for reads and writes. And then -- yeah.
Q. On page 12 of Exhibit 1064, there's a table on the right that's labeled "CAS Latency." And there are different rows; and the column labeled "Latency" says "2(Optional), and then there's a row for 3, a row for 4 and a row for 5; correct?

A. That's what the table says, yes.
Q. And in the context of CAS latency, does the 2, 3, 4 and 5, refer to clock cycles?
A. Yes. In DDR2, the latency is measured in clock cycles. But we can refer to the timing diagrams, to be clear about that.
Q. And so, for example, on page 24 of Exhibit 1064, there's a timing diagram that gives an example of CAS latency and additive latency and how they relate to read latency as well as write latency; is that fair?
A. Yes. To be specific, AL refers to additive latency; CL refers to CAS latency; RL refers to the total read latency; and WL refers to the write latency -- all from within that figure.
Q. And in the text above that figure, the -- on page 24 of Exhibit 1064, the DDR2 standard specifies that the read latency is defined as additive latency plus CAS latency; correct?
A. The exact language there is that the read latency is controlled by the sum of AL and CL. So it's a nuance.

Q. I'm looking at the language three lines up: Read latency is defined as the sum of additive latency because CAS latency -- and it has a little equation, "RL=AL+CL"; correct?

A. Oh, I see, down towards the bottom of that paragraph. Let me read that.

Yes, that's what it says there on that last three lines of that paragraph.

Q. And then write latency, abbreviated WL, is defined as read latency minus 1; correct?

A. Yes. For DDR2 SDRAMs, that is how it's defined. All SDRAM -- all DDR2 SDRAMs expect write data then and will deliver read data correspondingly.

Q. On page 14 of Exhibit 1064, we can see that DDR2 memory devices also include another register called the extended mode register; correct?

A. Yes, they do.

Q. And the extended mode register in DDR2 memory device is used to specify the value for the additive latency; correct?

A. That is one of the things that is set via the extended mode register, yes.

Q. And the additive latency can be 0 clock cycles, or 1, 2, 3 or 4 clock cycles; correct?

A. That is what the table on page 14 specifies.

Q. And so under the DDR2 standard, it's possible to set the additive latency to be 0, in which case the CAS latency is what would impact the read latency and the write latency; correct?

A. Well, the CAS latency, as specified in the mode register, always impacts the read latency and the write latency. If you happen to set the additive latency to 0, the CAS latency is the only thing that's determining what the read latency and the write latency are.

(Exhibit Number 1005 was previously marked for identification.)

BY ATTORNEY CHANDLER:

Q. Could you pull up Exhibit 1005. And, again, I'm not sure if we talked about it before, so I'll just put it in the chat for ease of reference.

A. It's not up, so I presume we have not looked at it yet.

Q. Yeah. Let me know when you have it on the screen. It's the '087 provisional.

A. I have that provisional up.

Q. All right. Have you reviewed Exhibit 1005, the provisional application 60/645087, which has been referred to as the '087 provisional?

A. Yes, I have.

Q. The '087 provisional, marked as Exhibit 1005, is the only provisional application that you formed an opinion about with respect to whether it provides support for the claims of the '417 and '215 patents; correct?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: My task was to rebut the arguments relative to the '087 provisional that were in the petition and declaration, and I did that. It was not necessary for me to do anything more vis-a-vis rebutting those arguments.

BY ATTORNEY CHANDLER:

Q. In your expert declaration marked as Exhibit 2024, in Footnote 2, paragraph 81 of

the '417 IPR and the paragraph 34 84 the '215 IPR, you state that you were asked only to render an opinion on Petitioner's arguments regarding the '087 provisional; correct?

A. What page are you on again, please?

Q. It's paragraph 81.

A. Paragraph 81. All right.

Q. And then --

A. And there's the Footnote 2. Yes, I see Footnote 2.

Q. So to be clear, it's only the '087 provisional marked as Exhibit 1005 that you provide any opinions about with respect to whether any of the provisionals provide support for the claim for the '417 and '215 patents; correct?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: Turning to paragraph 92 of my declaration that's for the '417, I say that:

"I understand that Petitioner has not identified any other limitations of the '417 patent

allegedly not supported by the '087 provisional. I take that to mean that Dr. Wolfe and Petitioner concede that the '087 provisional provides support for the other limitations.

"Nevertheless, for completeness, I following the follow exemplary citations in the following claim chart for the remaining limitations and -- when viewed through the eyes of a POSITA and the knowledge of the state of the art, including translation JEDEC standards -- indicate that the inventors had possession of the claimed subject matter."

And in that following table, I do refer to other citations other than Exhibit 1005. I would have to go back and see which of those are provisional applications and which of those are other documents that a POSITA would have access to.

BY ATTORNEY CHANDLER:

Q. So I guess I'm a little confused

by your Footnote 2 as well as the table that you just cited where you cite to things other than Exhibit 1005.

So is it your opinion that there are other provisionals other than Exhibit 1005 that provide support for all the claims of the '417 and '215 patents?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: I would have to review those provisionals to identify the support that you're suggesting.

BY ATTORNEY CHANDLER:

Q. And to be clear, I'm not suggesting. I'm trying to ask you if you're trying to offer an opinion that there's more than just Exhibit 1005 that provides support for all of the claims of the '417 and '215 patents.

So what are your opinions? Are they that it's only Exhibit 1005 that you're relying on to provide support? Or are you trying to say that it's Exhibit 1005 plus other provisionals? Or are you trying to say that there are other provisionals besides Exhibit 1005 that provide support for the claims

of the '417 and '215 patents?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: So what I'm saying in that footnote and in that section of the declaration is that, by looking at the '087 provisional by itself, I've rebutted all of the arguments presented in the petition and Dr. Wolfe's declaration vis-a-vis the '087 not providing support; and I'm saying that it does supply adequate support for all of those arguments that were presented in the petition.

I'm also providing additional support for the various claim elements in other references, but those are not necessary in order to rebut the arguments in the petition.

BY ATTORNEY CHANDLER:

Q. I understand the point you're providing about the '087 provisional and that, in your opinion, Exhibit 1005 is sufficient to provide support for all the claims. And I'll ask questions about that in a little bit.

But I'm still a little confused by your statement that you're providing additional support for various claim elements

and other references.

Are you suggesting that those other references are sufficient to support the claims? Or are you just pointing to other examples and other references where, you know, certain elements may be present but not necessarily support for the entire claim language?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: So, again, what I am saying is that the '087 by itself rebuts the arguments in the petition and that if that's inadequate for the board to find support for all of the claim elements, I'm providing this additional support across multiple references to -- that might help them come to a conclusion that the inventors had full support for the claims, as drafted.

BY ATTORNEY CHANDLER:

Q. And all of what you just described is in the table which -- on Exhibit 2024 of IPR 2023-00454, runs from pages 62 through 64; and in IPR2023-00455, runs from pages 58 through 61; correct?

A. Correct. Those are the pages on which those tables exist.

Q. And there's nothing besides those tables that you're pointing to with respect to this notion of additional support in other references that might help the board come to the conclusion that the inventors had full support of the claims; is that fair?

A. Correct. I mean, the bulk of the section is specifically rebutting the arguments in the petition, and that is done solely with the '087 provisional. And the table is additional support, generally speaking.

Q. Turning back to Exhibit 1005, the '087 provisional, that provisional has only one figure shown on page 10 of the Exhibit 1005; correct?

A. Yes. There's only one figure labeled "Block Diagram: Blank Buffered DIMM Memory Sub-system."

Q. The figure in the '087 provisional on page 10 of Exhibit 1005 is a block diagram in which a block of rank buffered DIMM logic, abbreviated RBDL, is shown in the middle of the figure; correct?

A. Yes, it's generally in the middle of the figure.

Q. The figure in the '087 provisional on page 10 of Exhibit 1005 shows that the block of rank buffered DIMM logic only receives from the memory controller on the left data signals DQ0 through DQ63, data strobe signals DQS0 through DQS7; a chip-select signal cs#; and address and control signals identified as ad & ctl; correct?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: Yeah, I'm not sure the cs signal is necessarily viewed by the POSITA as a single signal or a bus of signals. But that -- other than that quibble, your recitation of the names attached to the lines and buses is accurate.

BY ATTORNEY CHANDLER:

Q. And then the figure in the '087 provisional on page 10 of Exhibit 1005 shows on the right side two ranks of memory, each of which receive a similar set of signals from the block of rank buffered DIMM logic; correct?

ATTORNEY WARRICK: Objection;

form.

THE WITNESS: The names are different with regard to rcs0# and rcs1#; but they are, in fact, similar.

BY ATTORNEY CHANDLER:

Q. The figure in the '087 provisional on page 10 of Exhibit 1005 does not show any of the internal structure of the block of rank buffered DIMM logic; correct?

A. The figure does not, but the text does speak to some of its internal structure.

Q. Paragraph 5 of the '087 provisional marked as Exhibit 1005 refers to a multiplexer/demultiplexer; correct?

A. Yes, it does.

Q. But that paragraph does not mention any control signals for that multiplexer/demultiplexer; correct?

A. It doesn't mention control signals for the multiplexer/demultiplexer, but that doesn't mean those signals are not inherent in -- in that any multiplexer/demultiplexer needs to have control signals to determine its behavior.

Q. Paragraph 8 of the '087

provisional, marked as Exhibit 1005, also refers to a multiplexer/demultiplexer; correct?

A. There it's specifically called the data path multiplexer/demultiplexer, as it is in paragraph 5 also, by the way. So it's the same thing. And it's a multiplexer/demultiplexer in the data path between the memory controller and the ranks on the module.

Q. But that paragraph also does not mention any control signals for the multiplexer/demultiplexer; correct?

A. Again, it doesn't have to because any multiplexer/demultiplexer necessarily has to have control signals in order to have its behavior determined.

Q. Paragraph 17 of the '087 provisional marked as Exhibit 1005 also refers to a multiplexer/demultiplexer; correct?

A. Where in that paragraph?

Oh, there it is, yes.

Here it's the multiplexer/demultiplexer, presumably referring back to the same data path, multiplexer/demultiplexer of the previous

paragraphs, yes.

Q. And, again, that paragraph does not mention any control signals for the multiplexer/demultiplexer; correct?

A. And, again, it doesn't need to, because any multiplexer/demultiplexer necessarily has to have control signals in order to determine its behavior in real time.

Q. In the '087 provisional marked as Exhibit 1005, neither paragraph 5 nor 8 nor 17 tell you which control signals or any other signals to use as inputs to the multiplexer/demultiplexer -- the control multiplexer/demultiplexer; correct?

ATTORNEY WARRICK: Objection to form.

(Interruption by the court reporter to clarify the record.)

BY ATTORNEY CHANDLER:

Q. In the '087 provisional marked as Exhibit 1005, neither paragraph 5 nor 8 nor 17 tell you which control signals or other signals to use as inputs to the multiplexer/demultiplexer to control the multiplexer/demultiplexer; correct?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: So I cover this in detail in paragraph 82 of my declaration, where I list all of the implications of the figure and those paragraphs in the provisional '087 and what a POSITA of our time period would understand from that disclosure.

And, in particular, in the -- reading from Item 5 of that list in that paragraph, the claimed circuitry is at least part of said multiplexer/demultiplexer, which a POSITA would understand necessarily would receive control signals from the command decode circuitry and would understand necessarily that the module described in the '087 provisional would receive commands from the external memory controller and would decode that -- and would include command decode circuitry to interpret those commands and so forth.

In particular, I will note in addition that a POSITA reading the phrase "data path multiplexer/demultiplexer" would understand what a multiplexer/demultiplexer is and that they would necessarily be control signals that

determine which path is being selected and which direction the multiplexer/demultiplexer is sending data. So in total, it's clear that the data buffer control signals are supported by the '087 provisional.

ATTORNEY CHANDLER: Could we go off the record? But don't run away because I want to talk about tomorrow.

THE VIDEOGRAPHER: Off the record at 4:43 p.m. Pacific Time.

(Recess taken from 4:43 p.m. to 4:48 p.m.)

THE VIDEOGRAPHER: On the record at 4:48 p.m. Pacific Time.

ATTORNEY CHANDLER: Dr. Przybylski, as discussed, let's reconvene tomorrow at 7:00 a.m. Pacific, 10:00 a.m. Eastern, for the continuation of my questioning of you in both IPRs. And as a reminder, under the PTAB rules, you're not permitted to discuss the substance of anything with your counsel overnight.

THE WITNESS: I understand.

THE VIDEOGRAPHER: Counsel, would you like us to conclude the video deposition at

this point?

ATTORNEY CHANDLER: I'd like to recess until tomorrow morning.

THE COURT REPORTER: While we're still on the record, do you both want rough drafts tonight?

ATTORNEY CHANDLER: Sure, I'll take a rough draft. And just so you have it, I would like the final drafts one week later from today, so Thursday, February 22nd.

THE COURT REPORTER: Okay.

Mr. Warrick?

THE VIDEOGRAPHER: Counsel, does anyone need a copy of the video?

ATTORNEY CHANDLER: Phil, go ahead.

ATTORNEY WARRICK: I do not need the video. The rough would be great. And I guess I don't know -- what's the normal turnaround on the final transcript?

THE COURT REPORTER: Two weeks. It's usually two weeks from today.

ATTORNEY WARRICK: That's fine.

THE VIDEOGRAPHER: All right. This concludes Volume 1 of the deposition of

Samsung Ex. 1095, p. 268
Samsung Electronics Co., Ltd. v. Netlist, Inc., IPR2023-00455

Steven Przybylski. We're off the video record at 4:49 p.m. Pacific Time on February 15, 2024.

(Whereupon, at 4:49 p.m. the proceedings adjourned.)

INSTRUCTIONS TO DEPONENT

After reading this volume of your deposition, indicate any corrections or changes to your testimony and the reasons therefor on the Errata Sheet supplied to you and sign it. DO NOT make marks or notations on the transcript volume itself.

E R R A T A

I wish to make the following changes, for the following reasons:

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C E R T I F I C A T I O N

I hereby certify that I have read the foregoing transcript of my deposition testimony, and that my answers to the questions propounded, with the attached corrections or changes, if any, are true and correct.

STEVEN PRZYBYLSKI, PH.D.

CERTIFICATE OF SHORTHAND REPORTER

I, Gail Inghram Verbano, Registered Diplomate Reporter, Certified Realtime Reporter, Certified Shorthand Reporter (CA) and Notary Public, the officer before whom the foregoing proceedings were taken, do hereby certify that the foregoing transcript is a true and correct record of the proceedings; that said proceedings were taken by me stenographically and thereafter reduced to typewriting under my supervision; and that I am neither counsel for, related to, nor employed by any of the parties to this case and have no interest, financial or otherwise, in its outcome.

Gail Inghram Verbano, CSR, RDR, CRR
CA-CSR No. 8635

UNITED STATES PATENT AND TRADEMARK OFFICE

_____

BEFORE THE PATENT TRIAL AND APPEAL BOARD

_____

SAMSUNG ELECTRONICS CO., LTD.

Petitioner,

v.

NETLIST, INC.,

Patent Owner

_____

IPR2023-00455

Patent 9,858,215

_____

IPR2023-201428
Patent 8,787,060

_____

IPR2023-00454
Patent 11,093,417

Remote video-recorded deposition of

STEVEN PRZYBYLSKI, PH.D.

Volume 2

REPORTED BY:
Gail L. Inghram Verbano:
Registered Diplomate Reporter,
Certified Realtime Reporter,
Certified Shorthand Reporter-CA (No. 8635)

UNITED STATES PATENT AND TRADEMARK OFFICE

_____

BEFORE THE PATENT TRIAL AND APPEAL BOARD

_____

SAMSUNG ELECTRONICS CO., LTD.

Petitioner,

v.

NETLIST, INC.,

Patent Owner

WHEREUPON, the remote video-recorded deposition of STEVEN PRZYBYLSKI, Ph.D., Volume 2, was held via Zoom videoconferencing on Friday, February 16, 2024, beginning at approximately 6:59 a.m. Pacific Time, the proceedings being recorded stenographically by Gail Inghram Verbano, Registered Diplomate Reporter, Certified Realtime Reporter, Certified Shorthand Reporter-CA (No. 8635), and transcribed under her direction.

A P P E A R A N C E S

A P P E A R A N C E S:

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I N D E X

- - -

EXAMINATION OF: PAGE

STEVEN PRZYBYLSKI, PH.D.,

By Attorney Chandler 280

By Attorney Warrick 447

By Attorney Chandler 468

E X H I B I T S

NUMBER PAGE

(Exhibits 1107 through 1112 not identified.)

Exhibit 1113 U.S. Patent Number 7,002,378 292
re: IPR2022-01428 and
IPR2022-01428 (9 pages)

PREVIOUSLY MARKED EXHIBITS REFERENCED: PAGE

Paper 1 427
Exhibit 1012 484

DEPOSITION SUPPORT INDEX

QUESTIONS INSTRUCTED NOT TO ANSWER:

PAGE LINE

(None)

REQUEST FOR PRODUCTION OF DOCUMENTS

PAGE LINE

(None)

STIPULATIONS

PAGE LINE

(None)

QUESTIONS MARKED

PAGE LINE

(None)

REPORTER'S NOTE:

QUOTATION MARKS ARE USED FOR CLARITY AND DO NOT NECESSARILY REFLECT A DIRECT QUOTE.

Friday, February 16, 2024; 6:59 a.m.

- - -

THE VIDEOGRAPHER: Good morning. We're now on the record. It's 6:59 a.m. Pacific Time on February 16th, 2024.

This begins the video conferenced deposition of Steven Przybylski, Volume 2, taken in the matter of Samsung Electronics Co., Ltd. versus Netlist Incorporated, filed before the Patent Trial and Appeal Board; Case Numbers IPR2023-00454, and IPR2023-00455.

My name is Dana Bachman. I'm your videographer today. Our court reporter is Gail Verbano. We are both representing Esquire Deposition Solutions.

Will everyone present please identify themselves beginning with our witness, Mr. Przybylski.

THE WITNESS: Steven Przybylski.

THE VIDEOGRAPHER: Thank you. Counsel, please.

ATTORNEY CHANDLER: Good morning. Theodore Chandler from Baker Botts on behalf of the Petitioner Samsung Electronics Co., Ltd.,

and with me is my colleague, Dr. Ferenc Pazmandi.

ATTORNEY WARRICK: Phillip Warrick with Irell & Manella on behalf of patent owner Netlist, Inc.

THE VIDEOGRAPHER: Thank you.

Madam Court Reporter, would you please re-swear our witness.

WHEREUPON,

STEVEN PRZYBYLSKI, PH.D.,

being first duly resworn or reaffirmed to testify to the truth, the whole truth, and nothing but the truth, was examined and testified further as follows:

EXAMINATION (Cont'd)

BY ATTORNEY CHANDLER:

Q. Dr. Przybylski, do you have any clarifications or corrections to your previous testimony so far?

A. I would like to add something to our discussion at the end of yesterday with regard to the chapter -- the overview chapter in the Jacob textbook where we were looking at the

tables that compared direct Rambus and DDR SDRAM on page 23 of Exhibit 1070, if I may.

Q. Okay.

A. At the time yesterday I was skeptical of some of the numbers in that comparison table, and I was incredulous, in particular, about the 117-pin count per channel for the direct Rambus in Table 0V.3.

It didn't look right, so I checked some of the other references in the record here. And, in particular, the article Exhibit 2001, by Richard Crisp shows the -- what the interface looks like on the memory controller and says that the proper number there is, I think, 65 or so -- I'm sorry -- 76 or something. In the low 70s. We can pull that up if you would like. It's up to you.

And so that number is wrong in this table. There's no explanation as to how the authors got to 117.

The operating frequency is also at 600 megahertz, whereas the data sheets show it going up to 800 megahertz.

So this -- this comparison is not -- at least there's questions about it. And

I think I would beseech the board to be careful with regard to using Jacob's work in comparisons of the DDR JEDEC -- DRR SDRAM and JEDEC standardized memory subsystems and the direct Rambus. There's significant questions there between the -- what -- the analysis that he does. That's all.

Q. Do you agree that DDR SDRAM, at a given operating frequency, could have a peak bandwidth greater than the peak bandwidth for Rambus memory?

A. I think that in this table, the peak bandwidth of the direct Rambus is listed based on a 600 megahertz operating frequency. And if the data sheets are to be believed, then the peak operating frequency is 800, not 600. So that, in this case, the peak bandwidth of a single channel of Rambus -- direct Rambus DRAM would be greater than that -- what's shown as the peak bandwidth.

Or the peak bandwidth would at least be comparable, I think, probably -- 6 to 8 --

Yeah, it would be the same in the two. But then if you normalize it on a per-pin

basis for the controller, the peak bandwidth for the direct Rambus apples-to-apples comparison would be another 50 percent higher than this.

So under that analysis, the peak bandwidth of direct Rambus would be substantially greater than that of a direct SDRAM memory subsystem.

Q. The operating frequency of DDR has continued to increase, right, such that it's much faster than 200 megahertz today?

A. Well, the operating frequency of DDR hasn't gone up. There are subsequent generations of SDRAMs that operate at higher frequency, but I don't know if JEDEC has changed the specification of DDR SDRAM as cited in this table to above the 200 megahertz operating frequency listed here.

Q. But the way JEDEC works is that by the 2004 to 2005 time frame, the DDR2 specification had been published and finalized, and it provided for speeds that were much faster than the prior generation of the specification DDR -- sometimes referred to as DDR1; and furthermore, the 2004-2005 time frame, JEDEC was already thinking about and working on the next

generation of the standard DDR3, which would have even faster speeds than DDR2, and even faster or greater bandwidth; right?

Isn't that the way JEDEC was working and continues to work today?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: Yes, JEDEC aims for about a factor of two performance increase per generation of standard, and then going up from there.

But no one stands still; right? The direct Rambus, as compared in this table is -- had follow-ons, as we know with the XDR and other high-performance memory sub systems. Ultimately, the JEDEC way of doing things, from a business perspective and a industry/community perspective, won out, and we all now use JEDEC standardized memories for essentially everything.

And -- but my point is that this particular table and the other analyses we've seen from these authors does not appear to appropriately capture the comparison as of -- as it's portrayed in this table.

BY ATTORNEY CHANDLER:

Q. But my point is that, by 2004-2005, there was a recognition in the industry that Rambus was not going to be some revolutionary new technology that could leapfrog the JEDEC DDR approach that, by 2004-2005, the writing was on the wall that the JEDEC DDR approach had won out and would continue to win out because it was at least comparable in performance to the Rambus approach and it had all the advantages of cost and widespread adoption. Isn't that fair?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: But I would say, having lived through that period as a consultant following the industry very closely, it was the latter set of characteristics, the business side of things, that were ultimately the reason why we're not using Rambus DRAMs today for anything of note, and that the DRAM manufacturers and principal system vendors, you know, decided to adopt and use the SDRAMs as being adequate for the different applications even though, as shown by this table, that the direct or -- at least

Samsung Ex. 1095, p. 285
Samsung Electronics Co., Ltd. v. Netlist, Inc., IPR2023-00455

the revision of this table that was more accurate -- but the direct RDRAM still had superior performance over the DDR during the time frame when that -- there was uncertainty about which way the industry was going to go.

But you're absolutely correct that the industry did select the JEDEC approach and reject the Rambus approach.

BY ATTORNEY CHANDLER:

Q. And that was known by the 2004-2005 time frame?

A. Yeah. It was clear earlier than that even that it was not going to become the mainstream memory type for PCs and servers, at least.

Q. Could you turn back to your expert declarations marked as Exhibit 2024. And the chat has been cleared out. I'm hoping you still have everything on your screen, but if you need anything from the chat, let me know, and I can drop it in if that's more efficient.

A. So I walked away from my computer last night and have returned to it, so all of the PDFs that I opened are still open.

Q. Good. We'll pick up where we

Samsung Ex. 1095, p. 286
Samsung Electronics Co., Ltd. v. Netlist, Inc., IPR2023-00455

left off.

So open -- turn to paragraph 88 of your first expert declaration, paragraph 91 of your second expert declaration, and those paragraphs begin with the words:

"Therefore, at least some of the time, there is no discernible transition in the voltage on the DQS signal at the start of the preamble."

Do you see that?

A. I do.

Q. So in your opinion, for at least some of the time there's no discernible transition in the voltage on the DQS signal at the start of the preamble; correct?

A. Yes. The start of the preamble is not discernible by the receiver of the DQS and the DQ signals, and so it's not a reliable indicator of anything. It's just shown in the standard to specify the minimum length of the preamble that's a requirement to ensure that the rising edge is captured -- is useable properly by the receiver.

Q. There's a little ambiguity in my

Samsung Ex. 1095, p. 287
Samsung Electronics Co., Ltd. v. Netlist, Inc., IPR2023-00455

mind as to what you're saying in the sentence where you say there's "no discernible transition at the start of the preamble."

The word "start" could be referred to the very first moment in time where the signal drops low; or the word "start" could be referring to the first time period of the preamble where the signal is low for a certain amount of time.

What did you mean?

A. If we look at the JEDEC standard, for reads and writes it specifies either a minimum length or a bounds -- a minimum length of a preamble on outbound DQS from the DRAM's perspective or a requirement for an inbound DQS. And by "start of the preamble," I was referring to the standard specified minimum time.

So, for example, on inbound DQS signals to the SDRAM, the formal start of the preamble is somewhere between .9 and 1.1 clock cycles ahead of the first transition on DQS. So that would be what I refer to as the start of the preamble, regardless of whether there's an actual voltage transition there.

Q. I'm still a little unclear as to

what you're saying. And maybe it would help for us to both look at a picture together.

So could you turn to the DDR2 standard, Exhibit 1064, and go to page 26, as an example, and let me know you're there.

A. 1064, page what again, please? Sorry.

Q. 26.

A. 26, thank you.

So this is the data outbound read timing, and so it specifies the DRAM's behavior on a read as a result of executing a read command.

Q. On page 26 of Exhibit 1064 in Figure 23 there's a preamble to the DQS strobe signal; correct?

A. Yes. It does specify that the DRAM will guarantee that DQS is low for between .9 and 1.1 cycles ahead of the first rising edge of DQS.

Q. And the recipient of the preamble of the DQS strobe signal is able to discern that what it is receiving is, in fact, the preamble; correct?

A. No. That's not how it works.

Because the DQS could be low to start with, before the first time period shown here, there is nothing on that signal trace in terms of a voltage change that would indicate to the receiver that it is, in fact, in a preamble.

It's -- go ahead.

Q. To be clear, so you're not relying solely on the lack of a discernible transition from when the line is drawn in the middle to where the line drops low; you're saying that even when the line for the DQS strobe signal is low for up to a full clock cycle, that that is not discernible as a preamble either; is that fair?

A. Yes. The purpose of the preamble is to make sure that there is no false transitions on DQS in advance of the first real transition, and it's only the transitions that signify the beginning of -- in the case of a read transaction, the beginning of the first bit period on the DQs.

It does -- if you don't have a transition, there's nothing to detect in this sense. There -- if -- if the voltage on the DQS has been low for 15 clock cycles, it's not the

preamble of anything in particular, but the receiver and the memory controller can't use the fact that it's low to do anything. It's just make the -- the specification is saying that it has to be low for a clock cycle plus or minus ahead of the first transition in order to make sure that the first transition is clean.

Q. So in your opinion, a person of ordinary skill in the art would not be trying to detect the preamble itself? Is that sort of the basis for your opinion in your declaration, starting on paragraph 88 of the '417 IPR and paragraph 91 of the '215 IPR?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: Much stronger than that. It's not that he wouldn't try to; it's that he can't. There's nothing to grab onto to say "I'm in the preamble now."

Because this -- the signal is unchanged, for example, for a long period of time in advance of this actual transaction on the DQ and DQS signals, and you're not in the preamble for many, many cycles. The preamble is defined as that last cycle in advance.

But you can't -- as the receiver, you can't do anything as a result of being in, quote, the preamble, unquote. The period of time when the receiver -- when the transmitter, the DRAM in this case, is actively driving it low as opposed to it just happening to be low. So that the -- the transition on DQS, which is the actual point that we're interested in, that that's clean and discernible.

(Whereupon, Exhibit Number 1113 in both IPRs was marked for identification and is attached hereto.)

BY ATTORNEY CHANDLER:

Q. I'd like to mark a new exhibit, which will be 1113 in both IPRs. It's the same document, the only difference being the stamp in the bottom right with the case number.

I've dropped the exhibit into the chat. Please go ahead and open up Exhibit 1113 and let me know when you have it in front of you.

A. I'm looking at patent 7,002,378 to Srikanth.

Q. Yes. Exhibit 1113 is U.S. Patent Number 7,002,378 to Srikanth at Intel, filed on

December 29th, 2000; correct?

A. The priority is -- yes. Item 22 on the front page says filed December 29th, 2000.

Q. And then just below that it says that it was published on the 4th of July 2022; correct?

A. Yes. Item 65 says, "Prior publication date, U.S.," et cetera, "July 4th, 2002."

Q. And as shown in the title of this patent, marked as Exhibit 1113, as well as the abstract, this patent teaches a technique for detecting a valid data strobe; correct?

A. That is the title of this patent, yes.

Q. And then turn to Column 1 of the patent marked as Exhibit 1113.

A. Yes, I'm at Column 1.

Q. The first sentence of this patent marked as Exhibit 1113, Column 1, line 5 teaches continuously monitoring a data strobe signal and detecting when it indicates valid data is available; correct?

ATTORNEY WARRICK: Objection;

form.

(Witness reviews document.)

THE WITNESS: You're talking about the field?

BY ATTORNEY CHANDLER:

Q. Yes.

A. Column 1, lines 4 through 10; right?

Q. Yes.

A. I don't see the word "available" there.

"The present invention relates to a valid data strobe detection technique and to -- more particularly to a technique for continuously monitoring the data strobe signal from a double-data-rate synchronous DRAM, for example, for validating the strobe signal for subsequent use."

That's what it says.

Q. Turn to Column 3 of the patent marked as Exhibit 1113 and go to the start paragraph starting around line 47. Let me know when you're there.

A. Line 47 starting, "A typical strobe waveform."

Q. And you may want to just briefly look at Figure 2, and let me know when you're ready.

A. So I looked at Figure 2.

Q. So in Column 3 starting around line 47 of Exhibit 1113, there's a discussion of Figure 2 and a read preamble; correct?

A. Yes. It says a "minimum read preamble period would be equal to nine nanoseconds." That's in the middle of that paragraph, yes.

Q. Exhibit 1113 teaches that the read preamble may be set equal to 0.9 to 1.1 clock periods, and that read preamble period may be used in accordance with the JEDEC specifications for validating the read preamble; correct?

A. Yeah, I think we would have to be very careful of what he means by "validating" the preamble," but those are the words there.

Q. And then in the next paragraph of Column 3 of Exhibit 1113, towards the end of the paragraph at the bottom of the column, the

inventors at Intel teach that when the DQS strobe signal is low for a certain amount of time, "then a valid read preamble is presumed to have been detected"; correct?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: Those are the words in Column 3. Again, the -- this solution will detect a valid preamble well in advance of the actual preamble most of the time.

So the valid preamble, in the author's own words, is between .9 and 1.1 clock cycles in advance of the first rising edge. And we recognize that the start of the period of time when the voltage on the DQS signal is low can be way in advance of the start of the valid preamble, to use this author's words.

So the statement that a valid read preamble is presumed when a low voltage is detected is inaccurate because, by this terminology, they are presuming to detect a valid preamble well in advance of the actual preamble.

So there is tremendous tension here between what the author is saying and --

and the words he's using about detecting a valid preamble and the reality of the circuitry in a real system. The transition -- the transition from a midpoint to a low can happen at any time in advance of 1.1 cycles ahead of the first rising transition of DQS.

So I think that a POSITA reading this paragraph would understand that this author is detecting a valid read preamble well in advance of the actual preamble, as specified in the JEDEC standard.

BY ATTORNEY CHANDLER:

Q. In the JEDEC standard, as we discussed yesterday, the preamble is required to start between 1.1 and 0.9 clock cycles before the valid data signal?

A. That's correct. And, in fact, the -- the -- what is meant by the valid preamble that is between .9 and 1.1 cycles is that the DRAM is driving that signal low during that period. It's not saying anything about any transition at the start of that period or that the DQS signal has not been at a low value for an eternity in advance of that.

Q. Both the JEDEC standard that we

looked at before, marked as Exhibit 1064, as well this patent, marked as Exhibit 1113, specify that the preamble must start no earlier than 1.1 clock cycles in advance; correct?

A. And you have to understand what that means. Per the JEDEC standard, which defines the behavior of the DRAM, the standard says that the DRAM has to drive the DQS low no later than .9 cycles ahead of the first DQS rising transition.

It's not saying anything about what is on the DQS signal before that. And I think Dr. Wolfe confirmed that that midpoint indicator on the timing diagram that we looked at previously from the JEDEC standard does not -- only says that it's -- the value of -- that the DRAM is not driving the DQS in advance of the start of the preamble.

The drivers in the DRAM are in a tri-state mode, not driving high or low. Which means the voltage -- the actual voltage on the DQS signal is -- I don't care as far as the DRAMs are concerned; it's not part of their specification. It could be driven by some other device in terms of a write transaction or some

other DRAMs that sharing the DQS line.

The standard doesn't -- is only saying what the DRAM will do during the preamble, not what happens before the preamble. And, in fact, this '378 patent is not accurate with regard to the language of the bottom of Column 3, because this author is detecting a valid read preamble potentially well in advance of the actual preamble, as determined by the behavior of the DRAM.

Q. But you think the folks at Intel are just wrong when they wrote the patent marked as Exhibit 1113 and that their invention wouldn't work?

A. Well, I have not read the entire patent or looked at it in any detail. I don't know exactly what they are claiming to have been their invention. But I do know that the language at the bottom of Column 3, which we've looked at together, is internally inconsistent with the language higher up in Column 3 and more specifically is at odds with the JEDEC standard.

Q. Could you turn back to the JEDEC standard marked as Exhibit 1064, page 26, the Figure 23 that we were looking at previously,

and let me know when you're there.

A. I have that back up in front of me.

Q. Did you say that, previously in your answer a moment or two ago, that your understanding of the DQS strobe signal is that before the start of the preamble shown in Figure 23, when the line in the figure for DQS is in the middle, it's not low and it's not high -- did you say that at that point in time the DQS strobe signal would be tri-stated? Or I believe the terminology used sometimes is that the signal would be in a high impedance state? Is that correct?

A. You have to be more precise in your language.

The drivers are in a tri-state or high impedance mode. The voltage on the signal is indeterminate, is unknowable from the perspective of the SDRAM because that's what this document is about.

This document says how the DRAM will behave. Figure 23 is saying that prior to the start of the preamp period -- preamble period, sorry -- the drivers on the DRAM that

are driving the DQS signal are in a high impedance state, or tri-state state if you prefer; and that the DRAM is not driving the DQS line to any particular voltage; and that the volt -- the actual voltage on that signal -- and there is one -- is not determined by this DRAM but is determined by something else or something else that happened in the past and that is lingering on that line, because nothing has changed the voltage on that line.

Q. But just so I understand, the -- according to the JEDEC standard marked as Exhibit 1064, as illustrated on page 26, before the start of the DQS preamble, the DQS line will not be driven by the DRAM, because the DRAM will be in a high impedance state.

Is that correct so far?

A. So far so good.

Q. And then according to the JEDEC standard, no earlier than 1.1 clock cycles before the data the DQS strobe line must go low as part of the preamble?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: It would be no

later than .9. So the -- the DQS is -- I'm sorry. Let me start again.

BY ATTORNEY CHANDLER:

Q. It's -- between 1.1 and 0.9 clock cycles before the data the DQS strobe signal must go low?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: Let me say that a little more precisely.

What the JEDEC standard says is that the SDRAM is required to drive the DQS signal low, actively drive it to a low voltage, sometime between .9 and 1.1 cycles ahead of the first rising edge of DQS. That's all it says.

BY ATTORNEY CHANDLER:

Q. But it says a little bit more than that, because not only do you have to drive it low starting 1.1 to 0.9 clock cycles ahead of the data, you have to keep it low for that time period; right?

A. You have to actively drive it low for that period of time, starting between -- between 1.1 and .9 cycles ahead of the rising edge of DQS. So it can't drive it low more than

1.1 cycles in advance, and it has to be driving it low at .9 cycles ahead of the rising DQS signal. The first --

(Simultaneous cross-talk.)

Q. If we turn back to the Intel patent marked as Exhibit 1113, in Column 3 between lines 47 and 67, those inventors are assuming the same setup; correct? That the read preamble will be equal to a period of 0.9 to 1.1 clock cycles, as stated in the JEDEC standards; correct?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: Again, I haven't read this whole patent. I'm really not comfortable interpreting what the mindset of the inventors are or what their actual invention is.

I do know that whoever wrote these paragraphs is not being precise about how systems actually work and that the portion at the very bottom of Column 3 that we discussed previously, where it says that a valid read preamble is presumed to have been detected -- I think the word "presumed" here is carrying a lot of weight, because these inventors are presuming

to have detected a valid preamble when they are not actually in the preamble of an upcoming transaction.

So the -- we have to be very careful about reading the '378 patent in its entirety to understand what exactly they're inventing here and how it relates to the JEDEC standard and how it would actually work in a system.

You've only asked me to read, you know, 20 lines in the middle of a patent. I know that these 20 lines are internally inconsistent and inconsistent with the JEDEC standard; and that the word "presumed" to have been detected is very troubling, because you can presume to detect a preamble when you're not actually in a preamble.

BY ATTORNEY CHANDLER:

Q. I think you said at one point in your last answer that the inventors of Exhibit 1113 were detecting something before the preamble.

But to be clear, the bottom of Column 3, the inventors of Exhibit 1113 are talking about detecting the read preamble

itself, the read preamble that both they and the JEDEC standard say will be equal to 0.9 to 1.1 clock cycles; correct?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: Again, I haven't read this document. I don't know the invention. I do know that the paragraph that you're asking me to read in isolation does not say that.

What they say is that they're presuming that they're in a read preamble when they're not actually in a read preamble.

BY ATTORNEY CHANDLER:

Q. Let me summarize what I think I'm hearing from you and what I think I'm reading in Exhibit 1113, just to make sure that we're clear.

So your opinion was and sounds like still is, that you don't think a preamble for a DQS strobe signal can be detected; whereas the inventors of Exhibit 1113, bottom of Column 3, lines 66 to 67, state that they have a technique where a valid read preamble is presumed to have been detected. Is that fair?

ATTORNEY WARRICK: Objection;

form.

THE WITNESS: Again, I would need to read the entire document to see what actions they take as a result of presuming that they're in a preamble even when they're not in a preamble. Because that's clear from the JEDEC standard and the basic physics of digital systems, that they will be detecting that they are in a preamble based on the voltage on the DQS signal being low for an extended period of time, and they are presuming that they're in a preamble and they're doing some action as a result.

But they're not actually in a preamble. It's not a reliable -- the point in time when they're detecting a presumed preamble is well in advance, most of the time, of a actual preamble; because, again, the JEDEC standard specifies the world from the SDRAM's perspective, not from the memory controller's perspective.

BY ATTORNEY CHANDLER:

Q. But as I listen to your answer, it sounds to me like you are presuming that they're not in a preamble; whereas, when I read

Exhibit 1113, Column 3, lines 47 to 67, they're saying they are in a preamble, and this preamble exists from 0.9 to 1.1 clock cycles before the data, and that they have a technique to sample the strobe signal repeatedly in that time frame, and that if they sample it enough times and it's low enough times in a row, then they have a reasonable level of confidence or presumption that this is the true, valid read preamble and not a fluke.

Isn't that what they're saying here?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: I think you are reading a great deal into there that's not actually in those words.

They're saying that they're sampling the DQS -- and, again, I need to reiterate that I've not read this document in its entirety, I haven't looked at -- I don't know what they're doing as a result of being in a presumed read preamble.

But it's clear from the JEDEC standard, from the DRAM's perspective and the

nature of the DQS line and how it's shared amongst reads and writes in multiple DRAMs, that their presumption of being in a preamble is not the same as being in a preamble; that the actual start of the preamble is not reliably detectable.

BY ATTORNEY CHANDLER:

Q. But let me back up there, because you seem to be putting a lot of the weight on the word "presumption."

You're saying their presumption of being in a preamble is not the same as being in a preamble; whereas, when I read Exhibit 1113, their invention, what I take away from it is they have a technique which, according to them, will reliably detect the true, valid read preamble; even if no one is telling them directly that this is the true read preamble, they have a way to figure it out.

Isn't that what they are saying?

Now, you're pushing back and saying, well, you know, I don't believe that this technique would actually figure out the true preamble. Maybe it's wrong, but what they're teaching is, their technique allows them

to detect the actual read preamble. Right?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: No, that's not what these paragraphs in Column 3 say. And perhaps it's clarified elsewhere within the specification. I don't know. I haven't read the specification.

But if you are presuming that you're in a preamble and you're going to continue to presume you're in a preamble for 27 cycles, while the signal is low and then at some point -- don't interrupt me, please -- it's -- the voltage on the DQS signal is low for 6 or 7 samples in a row, they're going to presume they're in a preamble. It's going continue to be low for another 20 cycles. They are going to continue to presume they are in a read preamble.

At some point, they're right in that they are in a read preamble and, lo and behold, a rising transition on DQS happens that's used to capture the data.

But there -- it -- the underlying question that we haven't answered -- because I haven't read the entire document -- is what do

they do as the result of being presumptively in a preamble even when they're not in an actual preamble?

BY ATTORNEY CHANDLER:

Q. But you keep assuming that this may not be a preamble, and you're changing the assumptions. Because you just said, well, what if it's 20 cycles where it's low; but the JEDEC standard precludes it being from 20 cycles. The JEDEC standard says it can only be low for up to 1.1 clock cycles.

A. No --

ATTORNEY WARRICK: Objection; form.

THE WITNESS: That's not what the JEDEC standard says.

You have to understand the four corners of the JEDEC standard, which is, the DRAM is not allowed to drive the DQS signal more -- low more than 1.1 cycle ahead of the rising edge of DQS that it will generate, and it has to drive the DQS signal low no less than .9 cycles ahead of that transition.

The standard says nothing about the voltage on the DQS signal in advance of that

beginning of driving the signal by the SDRAM.
BY ATTORNEY CHANDLER:
Q. So --
A. I'm not finished yet.
The voltage on the DQS signal is dependent on what's happened before -- a read transaction, a write transaction by this DRAM or some other DRAM. And the standard only says what happens as a result of the DRAM's actions one cycle -- approximately one cycle ahead of when the DRAM is starting to drive data.
Q. The DQS strobe signal is driven by the DRAM; right?
A. Some of the time, but not all of the times.
Q. But the JEDEC standard tells us when the DRAM can and cannot drive the DQ strobe signal; right?
ATTORNEY WARRICK: Objection; form.
THE WITNESS: And, in particular, as we've reiterated numerous times here already, prior to 1.1 cycles ahead of the rising transition of DQS, the DRAM is explicitly specified not to drive the DQS signal; that the

voltage on the DQS signal is dependent not on the behavior of this DRAM but is dependent on what happened before, by something else.

BY ATTORNEY CHANDLER:

Q. And the "something else" is also governed by the JEDEC standard; right?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: No. It's -- it's -- it --

In general, yes, in the sense that the only things in a real system that are driving the DQS system is either a memory controller or a DRAM.

The behavior of the memory controller is indirectly specified in that -- the behavior of the DQS as its arrived at the DRAM in a write transaction, is specified by the standard; but you could have crazy systems where there's other stuff going on on those lines that's not related to the memory system. It's plausible, given the standard.

The standard only cares about how you stimulate the DRAM and what it's going to do as a result. The system designer is free to do

anything else.
BY ATTORNEY CHANDLER:
Q. That's not entirely fair, because every DRAM needs to comply with the JEDEC standard. The JEDEC standard says, when your turn is up, you need to tri-state and stop driving the DQS strobe signal, let someone else take a turn; right?
ATTORNEY WARRICK: Objection; form.
THE WITNESS: Or you could have another turn next yourself.
The -- that Figure 23 of the JEDEC DDR2 standard that we were looking at before -- which exhibit was that? 1064.
So what it says is that at the end of the burst read transaction, that the DRAM has to tri-state its drivers at the end, and it specifies a time after the last falling edge of DQS, at which point it has to stop driving the signal.
The voltage on the line will not change until something else drives it again. So it will stay low indefinitely, because it's low just before the tri-state period, and

it's -- you know, the signals have capacitance, they have inertia as far as the voltage is concerned.

So this DRAM is driving the DQS signal low during the last bit period. It's saying, I'm not driving it anymore. The voltage is going to stay low until something else, perhaps this DRAM again, in another read transaction, drives it to a different state again.

BY ATTORNEY CHANDLER:

Q. The controller --

A. Not necessarily the controller.

Q. No, I was starting a new sentence.

The memory controller -- the memory controller tells each rank of DRAM when to perform a read command and, therefore, when to drive the DQS strobe signal; correct?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: Yes, essentially.

BY ATTORNEY CHANDLER:

Q. So the memory controller has a hand in what's happening on the DQS strobe

signal; correct?

A. And, in fact, most memory controllers know when to expect a memory transaction incoming from a DRAM and don't employ any technique such as described within the '378 patent. They don't need to detect the preamble, per se, because they know when it's coming. They know when approximately -- when the first rising edge is going to be.

Q. But to be clear, the JEDEC standard required a preamble. That's an important part of the standard; right?

A. Yes, it does.

ATTORNEY WARRICK: Objection to form.

Sorry, Dr. Przybylski, just make sure to give me a chance to interject if necessary.

THE WITNESS: My apologies. I'm getting too wrapped up in this.

ATTORNEY CHANDLER: My apologies as well.

ATTORNEY WARRICK: It's exciting subject matter.

THE WITNESS: Well, it's --

there's subtly here that's important for this situation, because the -- Dr. Wolfe said some things in his declaration and repeated in the petition that are not accurate and that your -- vis-a-vis the behavior of the DQS signal and the DRAMs at issue here. And it's important that the Board understand what's really being specified by the standard and how the systems really work.

Go ahead.

BY ATTORNEY CHANDLER:

Q. It's also important for the Board to understand what a person of ordinary skill in the art at the time would have understood. And contemporaneous patents, such as Exhibit 1113, are reasonable evidence of what was understood at the time; correct?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: Yes. And you have to make sure your understanding of these references are consistent with reality.

And so when the authors of the '378 say, "We presume we're in a read preamble," is not the same as saying, "We know we're in a

preamble."
BY ATTORNEY CHANDLER:
Q. Again, I think you're drawing a distinction between presuming to be in a preamble and knowing to be in a preamble, when it sounds like they're just shades of gray, which is, you're assuming that knowing that you're in a preamble is 100 percent certainty; whereas, the inventors of Exhibit 1113 have come up with the technique -- they used the word "presumed," but they're using the word "presumed" to indicate a sufficiently reliable method where it may not be 100 percent certainty but it's some very close level of certainty that they're able to accomplish detecting, with a reasonable amount of certainty, the read preamble.
Is that fair?
ATTORNEY WARRICK: Objection; form.
THE WITNESS: Apologies.
No, that's not fair, because we haven't reviewed the entire patent. We don't know what they're doing as a result of this presumption. In fact, the probability that

their initial presumptive detection is an actual preamble is extremely low. Because of the electrical behavior of the DQS line, as we've described together over the last ten minutes or so, the DQS signal will stay low after the end of one transaction.

So if you're a memory controller and you've just received a read transaction, the DQS signal is low; the next read transaction, for example, might be 20 clock cycles later, the technique of the '379 as it's articulated in the bottom of Column 3 -- and, again, I haven't read the entire thing -- it will immediately start registering a presumed preamble, immediately after the end of the last read transaction and will continue to presume to be in a read transaction throughout that 20-cycle period until the actual rising edge of the next read transaction from this -- the same DRAM for a different DRAM.

So the probability that the presumption of being in a read preamble is actually in a read preamble is very low, depending on the actual utilization of the memory bus.

BY ATTORNEY CHANDLER:

Q. I think we discussed earlier that Intel was one of the companies that made memory controllers; right?

A. Yes.

Q. They made a lot of memory controllers in the early 2000s; right?

A. Very successfully, yes.

Q. And it's the memory controller for a read command that needs to detect the preamble of the DQS strobe signal -- in other words, it's Intel product that needs to detect when there's a read command that has a DQS preamble; correct?

A. No.

ATTORNEY WARRICK: Objection; form.

THE WITNESS: No. That's not -- that is, in fact, not how it works.

What the memory controller has to do is detect the rising edge of DQS at the end of the preamble and use that to capture the data.

The purpose of the preamble is to ensure that the rising edge of DQS that

signifies the first piece of data is clean and valid. That's the only purpose of the preamble.

And that's why the preamble is specified to be of different lengths, inbound and outbound, because the start of the preamble is not significant. It's just saying that the DRAM manufacturers are necessarily going to drive the DQS low for one cycle ahead of the rising edge of DQS, in order to ensure that -- at the other end -- at the memory controller, the rising edge of DQS will be clean and useable to capture the data.

BY ATTORNEY CHANDLER:

Q. Intel makes the memory controllers that receive the DQS strobe signal on a read command; correct?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: Yes. All memory controllers have to receive the DQS signal in order to receive the rising and falling edges that signify the transmission of data.

BY ATTORNEY CHANDLER:

Q. In the patent by Intel, marked as Exhibit 1113, in Column 1, line 56 through 59,

the inventors state there is a need for a technique which can identify a valid read preamble; correct?

A. Where are you reading again, please? Column 1 what?

Q. Line 56 through 59 or so.

The inventors at Intel, the company that makes the memory controller that received the read commands and receives the DQS strobe signal from the read command state in Column 1 starting around line 56 of Exhibit 1113, "There is a need for a technique which can identify a valid read preamble"; correct?

A. Those are the words in that short snippet of Column 1. We don't know what that need is. It may be a need specific to the internals of their particular memory controller.

What I'm saying is that the JEDEC standard specifies the read preamble in terms of the DRAM's behavior in order to make sure that the rising edge of DQS is cleanly discernible in order to use it to capture the data. Certainly there are many memory controllers out there that don't detect a preamble in order to do anything

in particular; they just wait for the DQS and they capture the data as a result.

So the authors of the '317 saying there's a need to do that is at odds with -- let me start that sentence again.

The fact that the authors of the '378 are saying that they have a need specific to their design to detect the start of a preamble is not the same as saying that all memory controllers need to detect the start of a preamble. In fact, that's not the case.

Q. I understand your opinion that you believe it's not possible to discern the preamble of the DQS strobe signal; but these inventors at Intel, in Exhibit 1113, state that there's a need to identify a valid read preamble, and they purport to disclose a technique for doing that. So there's a little disagreement between you and your opinion and what's being disclosed in Exhibit 1113.

A. I think --

ATTORNEY WARRICK: Objection to form.

BY ATTORNEY CHANDLER:

Q. Is that fair?

A. No, I don't think that's fair, because the way that these DQS signals operate in a signal -- in a system is not a matter of opinion; it's a matter of fact. And the fact -- and that the authors of this patent have said they have a need to do something doesn't alter those facts.

And the fact -- and then later in Column 3 where they say, well, we can detect that the signal is low and we're going to presume that that is, in fact, a preamble and perhaps do something as a result of that presumption is not inconsistent with the reality of the DQS signal and the JEDEC standards, which says that the DQS is continuously low between transactions most of the time except for -- you know, for extremely low -- long periods of idleness, the voltage on the DQS signal may drift.

But in any reasonably busy memory system, the DQS will be low continuously between memory transactions; and the technique that is articulated at the bottom of Column 3 of the '378 patent will continuously indicate a presumption of a preamble in advance of the

actual preamble.

The memory controller knows when the actual preamble is approximately going to show up; but they're doing this presumptive preamble well in advance of that.

Or at least we believe so. Again, I haven't read the whole thing. Maybe they're qualifying it by when they expect the preamble to show up in their memory controller, because they know what the read latencies are and they know what the -- what the general structure of the memory system is.

So I think when you try and rationalize their words with the reality of memory systems, you understand that their presumption of being in a preamble is different and not the near 100 percent that you wish, but that it is an indication that we're between two transactions and that there will be another one coming sometime.

Q. Everything you just said, that's not anywhere in Exhibit 1113; right?

A. That's -- what I just said is a natural consequence of 1064 and 1113 taken together, because they relate to each other;

Samsung Ex. 1095, p. 324
Samsung Electronics Co., Ltd. v. Netlist, Inc., IPR2023-00455

right? The -- this is specifically about DDR SDRAMs, which, I think, is what you were having me look at. 1064 is DDR2.

So, again, we have a little disconnect there, but the basic physics of DQS signals doesn't change.

The JEDEC standard and physics says what goes on on the DQS signal at the memory controller during the read transactions. You have to read the '378 in light of that reality, and that's what a POSITA would be able to do.

ATTORNEY WARRICK: Could I suggest this may be a good time for a break? We've been going well over an hour.

THE WITNESS: I agree.

ATTORNEY CHANDLER: Almost. Let me just -- follow up.

BY ATTORNEY CHANDLER:

Q. Do you agree with the statement in Column 1 of Exhibit 1113 starting at line 60 that the existing DDR SDRAM protocol does not provide a feedback to the memory controller indicating when to look for the data strobe?

A. So reading the entire paragraph

that that one sentence is a part of, or at least the following sentences, it goes on to say, "rather the memory controller launches a read command and then somehow knows -- somehow identifies the arrival of the DQS signal."

In fact, the memory controller knows, based on the programs read latency of the DRAMs approximately when the DQS is going to be arriving.

So it's clear that -- from the perspective of the authors of the '378 patent that their memory controller is not using all of the information at its disposal to know when to expect data to return. Because as you've noted, the memory controller knows all that stuff. It's the -- it's in charge.

So for some reason, they've -- the context of their invention and their memory controller is that the memory controller is going to presume to be in a preamble well in advance of an actual preamble and then somehow be ready for a DQS signal arriving at some random time; but, in fact, it's not at a random time and the memory controller knows when it's going to be coming, approximately.

So, again, you have to read the '378 as a POSITA would in the context of the JEDEC standard and the reality of memory subsystems to understand what the authors of the '378 are actually saying.

Q. But is it correct that in a DDR SDRAM system, there's not some separate signal that tells the recipient, such as the memory controller in this situation, when to look for the data strobe?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: Yes, that's true; there is no such signal. And you have to ask why, is there no such signal?

If there was a need -- a pervasive need for such a signal, the JEDEC committee would have put it in. But there isn't one, because the memory controller knows when the data is going to be coming back, modulus the transmission delays along the signal lines.

So the memory controller knows when it sent the read command. It knows what the read latency of these DRAMs is. It knows how -- in the DDR world, less so.

Samsung Ex. 1095, p. 327
Samsung Electronics Co., Ltd. v. Netlist, Inc., IPR2023-00455

But it -- it knows roughly the time delay associated with communicating with the DRAMs, and so it knows approximately when to expect a DQS rising edge, signifying the return of the data that it asked for.

Go ahead.

BY ATTORNEY CHANDLER:

Q. You say the memory controller knows approximately when the strobe and then the data should arrive.

But the whole point of Exhibit 1113 is that knowing approximately when the strobe and when the data is going to arrive isn't good enough, because we're starting to get at higher speeds; and at the bottom of Column 1, top of Column 2 what the inventors are talking about is that there's going to be uncertainty due to flight time and other routing of the signals. And so you can't count on when the strobe and the data is supposed to arrive; you can't count on approximately when it's going to arrive. They are proposing a technique that doesn't rely on any of that, but instead relies on when the strobe itself has a preamble that arrives. Isn't that correct?

Samsung Ex. 1095, p. 328
Samsung Electronics Co., Ltd. v. Netlist, Inc., IPR2023-00455

ATTORNEY WARRICK: Objection; form.

THE WITNESS: No, that's not correct. Because the -- let me read.

(Witness reviews document.)

The uncertainty that's talked about and the variance that's talked about in the following paragraphs of the background of the '378 patent -- which, again, I haven't read in its entirety -- is on the order of a fraction of a clock cycle. Because in the DDR SDRAM generation, the operating frequencies were low by today's comparisons, and so the flight time delays are fractions of a cycle and not multiple cycles.

In contrast, their technique for presumptively detecting a preamble has many, many cycles of uncertainty between the presumptive preamble and the actual preamble.

So, in fact, their technique will have some value for them. It is not universal. If this missing wire was important, it would have been included in this SDRAM standard and all subsequent SDRAM standards; but, in fact, there are sufficient techniques, including the

memory controller knowing how many cycles of latency it programmed the SDRAMs to have, so that the -- for most memory controllers, there is no need to presumptively try and determine whether you're in a preamble or not.

BY ATTORNEY CHANDLER:

Q. So, in your opinion, the controller will know, for the read command, approximately when the strobe signal and the data signal should arrive; correct?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: The memory controller will know in which cycle the data is going to come back. The actual phase relationship between the rising edge of the DQS signal indicating the start of the first piece of data on the DQ lines and the memory controller's clock signal, that phase relationship, will vary from instance to instance, from one memory system design to another, from one DRAM to another, from one rank to another. But that's all a fraction of a cycle.

The memory controller can know,

and does know in most cases, which cycle the data is going to come back in, particularly in the DDR SDRAM regime.

BY ATTORNEY CHANDLER:

Q. So, in your opinion, a memory controller will know approximately when the strobe and data signals will arrive within approximately one clock cycle; and then Exhibit 1113 teaches that it's possible to detect whether that strobe signal is a preamble by repeatedly sampling the signal to see if it's low for a certain amount of time. Is that fair?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: No, that's not fair. There are a couple of inaccuracies in that long question.

The first was that the cycle in which the data is coming back is not approximately known; it's precisely known. The only uncertainty or variability, to use the language at the top of Column 2 of the '378 patent -- which again I haven't read in its entirety -- is only related to flight time delays between the memory controller and the

DRAM, and those in the DDR regime are a fraction of a cycle.

So the memory controller knows which cycle the data is going to be coming back in. Precisely when in that cycle is the variability.

In contrast, the technique of the '378 patent is about presumptively detecting a preamble way, way in advance of that.

For some reason that's known to these inventors, they had a need for it. Most -- every other memory controller that I've looked at or had exposure to in detail doesn't do this. There's no need -- presumptive need or universal need to do this. If there was, this signal that they're referring to -- that they're feeling a lack of would have been included by JEDEC.

And Intel is a JEDEC member, by the way. So if the memory controller designers at Intel said, hey, we need this signal that's missing, Intel would have ensured that it was part of the standard.

The standard is complete and adequate in its own right, as verified by

Intel's votes on the matter.

And so you're inferring a great detail about the fact that these guys are employed by Intel. They have a particular need for their particular memory controller to do something presumptively. It's not universal.

BY ATTORNEY CHANDLER:

Q. Do you agree that adding a pin to a controller would increase costs, and that, oftentimes, companies like Intel and organizations like JEDEC will avoid adding a pin in a signal if they have another way to get the job done that doesn't require the additional pin and additional signal?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: That's a generally true statement.

With regard to this situation, the counter example is that the DQS signals were added because they were required. They needed to be added to make the systems work at high frequency, relative to the previous generations of DRAMs.

So the JEDEC committee, including

Intel, knew that the standard that they created with the -- with the behavior of the DQS signal as from the DRAM's perspective was sufficient to facilitate accurate capturing of data. And there was no need for this additional line because they recognized that the memory controllers knew when the data was coming back, and there was no need to presumptively, well in advance of an actual preamble say, oh, we might be in a preamble now; we might be in a preamble now; we might be in a preamble -- for cycles and cycles on end before the actual preamble.

What the authors of the '378 are doing as a result of that presumption is not clear, because I haven't read the whole thing. It may be trivial. It may be something unique to their particular memory controller. But regardless, it's this -- this presumed need is specific to them and not a universal characteristic of DDR SDRAM memory systems.

And we really should take a break at this point.

BY ATTORNEY CHANDLER:

Q. Do you think a person of ordinary skill in the art would have known about

Exhibit 1113 -- is it fair to say it's in the prior art?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: It is fair to say it was published in advance of the 2004-2005 time frame that we are focusing on.

ATTORNEY CHANDLER: Okay, let's take a break.

THE VIDEOGRAPHER: Off the record at 8:26 a.m. Pacific Time.

(Recess taken from 8:26 a.m. to 8:37 a.m.)

THE VIDEOGRAPHER: On the record at 8:37 a.m. Pacific Time.

BY ATTORNEY CHANDLER:

Q. Please pull up the '417 and '215 patents marked as Exhibit 1001, and let me know when you have them.

A. I have the '417 up.

Q. And go ahead and pull up the '215 as well. We'll cover them both at the same time.

A. Okay, hold on.

Q. Then you can go to Column 1 of

both to start.

A. Okay. I'm looking at Column 1 of both of '417 and '215.

Q. In Column 1 of both the '417 and '215 patents, toward the middle of the column there's the field of invention, which indicates that the '417 and '215 patents relate "generally to memory modules of a computer system"; correct?

A. The field of the invention of both patents is:

"Relates generally to memory modules of a computer system, and more specifically to devices and methods for improving the performance, the memory capacity, or both, of memory modules."

Q. The '417 and '215 patents are not limited to JEDEC-compliant memory systems; correct?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: You're referring to the scope of the claims and what that is, I think that's outside of -- I haven't made any

opinions about infringement or the scope of the claims.

BY ATTORNEY CHANDLER:

Q. But the scope of the claims is the same whether we're talking about infringement or invalidity; right?

A. Yes, the scope of the claims is the scope of the claims. It's a matter -- the -- my opinions have been to rebut the arguments of the petition and the corresponding declaration that seek to invalidate those claims.

Q. Let's start with the specification of the '417 and '215 patents.

Nothing in the specification of the '417 and '215 patents limits those patents to JEDEC-compliant memory systems; correct?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: There are certain embodiments that relate to JEDEC standardized devices of modules. I don't know whether they are, in fact, limiting or not to that specific set of embodiments. That's not something that I've opined on.

BY ATTORNEY CHANDLER:

Q. So you have not offered the opinion that either the claims or the specification of the '417 and '215 patents are limited to JEDEC-compliant memory systems; is that fair?

A. Let me review my declaration.

(Witness reviews document.)

In looking at Section 6 of my declarations vis-a-vis the '417 and '215 patents, I'm not seeing an opinion that relates to whether anything in the specification is formally limiting the scope of the claims to JEDEC-compliant memories and modules.

Q. Please turn to Figure 1 of the '417 and '215 patents marked as Exhibit 1001. Let me know you're there.

A. Yes, I'm looking at Figure 1 in both patents.

Q. Figure 1 of the '417 and '215 patents, marked as Exhibit 1001, shows a memory module 10, which is the big dashed box, including memory devices 30 on the left and a buffer circuit 40 in the middle; correct?

ATTORNEY WARRICK: Objection;

form.

THE WITNESS: Yes, that's generally accurate.

BY ATTORNEY CHANDLER:

Q. Please turn to Column 6 of the '417 patent starting around line 43, and the corresponding location in the '215 patent is Column 5 starting around line 63. And let me know when you're there.

A. I have those columns up in front of me.

Q. The '417 and '215 patents teach that memory modules 10, "compatible with embodiments described herein, include, but are not limited to," and then there's a list of different types of memory modules; correct?

A. Yes, those are the words of Column 6 of the '417.

Q. And then a little bit further below that, the '417 and '215 patents teach that memory devices 30 "compatible with embodiments described herein, include, but are not limited to," and then it goes onto list various types of memory devices; correct?

A. Yes, in Column 6 of '417 it does

list a variety of JEDEC standardized memory devices and refers to them with regard to some embodiments.

Q. The '417 and '215 patents explicitly do not limit either the memory module or the memory devices to any particular JEDEC standard or to JEDEC at all; correct?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: The patent does refer to the JEDEC standards specifically in some places. It does, as you indicated, indicate that the modules and the memories are not limited to the one specifically listed. It could include others as well.

BY ATTORNEY CHANDLER:

Q. Please turn to Column 23 of the '417 patent, starting around line 22, and the corresponding language in the '215 patent is in Column 21 starting around line 8. And let me know when you're there.

A. I'm look at including 23 of the '417.

Q. And do you have the '215 around Column 21 as well?

A. Let me look at 21. They're identical?

Q. Yes. I mean, they're identical as far as I can see.

A. Yes, they both have a paragraph starting, "In certain embodiments utilizing memory density multiplication embodiments," yes.

Q. Are you familiar with the concept of rank multiplication?

A. Generally yes; and as it's described within this patent specification, yes.

Q. The '417 and '215 patents disclose a buffer circuit 40 with translation logic for performing what's commonly known as rank multiplication; is that fair?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: So the last sentence of that paragraph in Column 23 of the '417 beginning at line 32 of that column says:

"Furthermore, in certain embodiments, the translation logic equations vary depending on whether the implementation multiplies memory devices per rank or multiplies the

number of ranks per memory module."

So to that extent, for certain embodiments, they do claim rank multiplication as a part of the logic -- the translation logic.

BY ATTORNEY CHANDLER:

Q. And the two sentences before what you are reading -- for example, Column 23 of the '417 patent starting at line 26 -- is discussion of circuit 40 using translation logic to perform what we commonly refer to now as rank multiplication; correct?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: I think the sentence that I read was the end of that paragraph more accurately summarizes the idea that the memory devices 10 can include, in certain embodiments, implementations of a rank multiplication of the number of ranks, which is what we would call rank multiplication, or --

BY ATTORNEY CHANDLER:

Q. And --

A. Yeah, go ahead.

Q. Do you understand the concept of a density transition bit?

A. Yes, the term "density transition bit" occurs in several places in the specification of the '417 and '215. I think it is not a term that has a lot of use, if any use, outside of the specification.

But within the context of this specification, it's clear what the inventors mean by it.

Q. And what's the relationship, in the '417 and '215 patents, between the density transition bit and rank multiplication?

A. Reading from the Column 24 of the '417, it says that the "Table 4 lists the corresponding density transition bits for the density transitions between DDR2 memory densities of Table 3."

So they are identifying in Table 4 which address or bank bits change in terms of the width of the various fields between one density of memory device and another; and that has bearing on their rank multiplication implementation.

Q. At the top of Column 23 of the '417 patent it states:

"The term 'density transition

bit' is used to refer to the additional address signal bit which is used to access the additional memory by selecting which rank of memory devices is enabled for a read or write transfer operation."

Correct?

A. So what line did you start reading at on 23? Or you were paraphrasing not reading; correct?

Q. No, I was reading starting around line 7 of 23 of the '417 patent.

A. Okay, let me find that exactly.

Oh, I see where it is. Okay. Just one moment, please. [Reading sotto voce].

Yeah, so you accurately read that portion of the Column 23.

Q. So how is the density transition bit used to perform rank multiplication? How does it work?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: In brief the -- when using smaller devices to simulate larger devices, the address bits that are different

between -- in terms of the width of the row or bank addresses that are different between the two densities are the ones that need to be -- that play an important role in the simulation of a larger density by two smaller densities devices, which is the central idea of rank multiplication.

BY ATTORNEY CHANDLER:

Q. And then turning back to line 22 -- or the paragraph beginning at line 22 of Column 23 of the '417 patent, as well as in the '215 patent it's the paragraph starting at line 8 of Column 21.

The buffer circuit 40 has translation logic for performing rank multiplication using the density transition bit; correct?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: First of all, 40 is just the circuit, it's not called the buffer circuit, which -- just for precision.

Yes, it says, starting at line 26:

"The circuit 40 of certain

embodiments utilize the implied -- utilizes implied translation logic equations having variations depending on whether the density transition bit is a row or a column or internal bank address bit."

So the specific density transition bit for different density transitions is a factor in circuit 40's translation logic equations.

BY ATTORNEY CHANDLER:

Q. In the '417 and '215 patents, the translation logic in circuit 40 will receive chip-select signals and address signals; correct?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: If we refer back to Figure 1 of the two patents, it shows that between the circuit 40 and the -- I think the controller 20, there are address and control and chip-select signals indicated.

BY ATTORNEY CHANDLER:

Q. And so what signals are used to perform rank multiplication? How are they used?

So what are the inputs, the translation logic in circuit 40, and what's the output? What are you trying to accomplish?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: The goal of rank multiplication is, as I noted earlier, to make lower density memory devices that are available and cost-effective appear to be a larger density device that may be less cost-effective at the present time, at the point of decision of an engineer making selections of memory density devices. So that's the purpose of rank multiplication.

It's based on the addresses, and there is -- the addresses in and the addresses out such that the memory controller perceives one set of memory devices, even though that is a deception on the part of the circuit 40.

BY ATTORNEY CHANDLER:

Q. And what happens with respect to the number of chip-select signals when you're performing rank multiplication?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: For the embodiments utilizing rank multiplication, there would be a change in the number of chip-select signals, as we see in some of the figures -- for example, in -- starting at Figure 9, you see examples of different embodiments with different numbers of chip-selects coming into the module and different numbers of ranks being controlled by circuit 40.

BY ATTORNEY CHANDLER:

Q. Figure 1 shows that as well; correct?

A. Figure 1 is less precise. It doesn't -- it shows chip-select signals going to the different ranks 32 from circuit 40; and it shows at least some chip-select signals between memory controller 20 and circuit 40.

Some of the later figures are more precise with regard to exactly how many chip-select signals are received by the module 10 from the memory controller and how many chip-selects are generated towards the ranks within the module 10.

Q. Figure 1 in the '417 and '215 patents shows twice as many chip-select signals

being output by circuit 40 compared to the number of chip-select signals being input to the circuit 40; correct?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: I don't think that the illustration of Figure 1 necessarily shows rank multiplication. If I'm reading from Column 6 of the '215 beginning at line 30 -- no, not line 30, sorry.

Yes, I'm sorry. Reading '215 starting Column 6, line 30:

"In certain embodiments, the plurality of memory devices 30 are arranged in a first number of ranks. For example, in certain embodiments, the memory devices 30 are arranged in two ranks, schematically illustrated in Figure 1. In other embodiments, memory devices are arranged in four ranks."

So that limited description of Figure 1 does not imply that the number of ranks is different. And under that portion of Column 6, you would understand that there are

more than one chip-selects coming into -- potentially, at least, into circuit 40.

BY ATTORNEY CHANDLER:

Q. I understand that there may be more than one chip-select being input to circuit 40.

My question is: Circuit 40 in Figure 1 doubles the number of chip-selects; right?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: I don't think that the embodiment of Figure 1 is necessarily performing rank multiplication, since elsewhere it said that only in certain embodiments are we having rank multiplication and that the embodiment of Figure 1 is not limited to that circumstance.

And so it does not necessarily change the number of chip-selects.

BY ATTORNEY CHANDLER:

Q. And I'm focused on the discussion in Column 23 of the '417 patent and Column 21 of the '215 patent where circuit 40, as we discussed earlier, does perform rank

multiplication using translation logic based on the density transition bit. And what I'm trying to understand from you is: How does that work?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: In the embodiments that include a circuit 40 that include -- or that implement rank multiplication, there would be a change -- let me start again. My apologies.

In at least some embodiments that implement rank multiplication that include a circuit 40, there would be a change in the number of chip-selects, as the address translation is performed to implement the address -- the rank multiplication. I don't believe that all implementations -- all embodiments involving a circuit 40 necessarily include that feature.

BY ATTORNEY CHANDLER:

Q. And when you say "that feature," you're referring to rank multiplication?

A. Yes, I am.

Q. All right. Sticking with the embodiment of circuit 40, as shown, for example,

in Figure 1 of the '417 and '215 patents where there is translation logic for performing rank multiplication, what are the necessary inputs? How does the logic work, and then what's the output?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: Well, the implementation of rank multiplication in all of the embodiments of these patents span a variety of different implementations depending on which density transition they're talking about, as articulated in Tables 3 and 4 of the specifications.

Yeah, 3A, 3B and 4.

And so, for example, in the embodiment of Figure 10A there's a change in the row address bits but not of the chip-select bits. And Figure 10B illustrates exactly how that is going to be affected.

And then there are other implementations described in subsequent figures. So it's hard to summarize all of the inputs and all of the outputs for the rank multiplication because it varies according to the density

transition being considered.
BY ATTORNEY CHANDLER:
Q. I was asking about Figure 1 in the embodiment of circuit 40 where the translation logic performs rank multiplication using the density transition bit.
And in Figure 1 there's twice the number of chip-select signals coming out of circuit 40 as coming in. And I'm trying to understand from you how that works: What are the necessary inputs to the translation logic, what does the translation logic do to perform rank multiplication, and then what are the outputs?
ATTORNEY WARRICK: Objection; form.
THE WITNESS: I don't believe that the Figure 1 shows only rank multiplication embodiments. It's a generic figure that is applicable to many embodiments within the specification.
One of the embodiments that I talked about that conforms to the general rubric of Figure 1, which is exemplified -- explained in more detail with regard to Figure 10, has no

change in the number of chip-selects.

Others would necessarily have a change in the number of chip-selects depending on the address -- the density transition that's being manipulated and what the density transition bit is for that indication -- for that particular transition. Again, it varies depending on the embodiments.

And, for example, if we look at Column 25 of the '215, it refers to an embodiment with a circuit 40, one particular circuit 40, where there is a piece of Varilog code that's quite long that implements, in part, the memory density multiplication from 256 megabytes to 512 megabytes of a DDR2 SDRAM device, and it describes how the CAS signals are changed.

We can go through that Varilog line by line if you want. I'm not sure that would be productive.

BY ATTORNEY CHANDLER:

Q. In the embodiment of circuit 40 in Figure 1 of the '417 and '215 patents, where circuit 40 is using translation logic to perform rank multiplication, is an example of rank

multiplication where there is one chip-select signal coming in to circuit 40 and two chip-selects coming out? Would that be an example of rank multiplication?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: So to be clear, circuit 40 is indicative of a wide variety of different implementations, some of which do rank multiplication, some of which do not.

For example, in Figures 3 and 4 --

BY ATTORNEY CHANDLER:

Q. But to be clear, I'm focusing on the embodiment where circuit 40 does perform rank multiplication.

I understand your point that circuit 40 in other embodiments doesn't. But as I think I've been clear, but I just want to make clear, let's focus on the embodiment of circuit 40 that is performing rank multiplication. Understood?

A. Okay. So as long as we are stipulating that the circuit 40 embodies many -- includes many embodiments, some of which do rank

multiplication and some of which do not.

Given that stipulation, the -- where there is a change in the number of chip-selects as a result of rank multiplication, the new chip-selects would be determined based on the row and bank address bits, or the density transition bit, in particular, for the density transition being implemented in that embodiment.

Q. In that embodiment, does the translation logic of circuit 40 generate additional chip-select signals based on the density transition bit which is either the address signal or the bank address signal?

ATTORNEY WARRICK: Objection form.

THE WITNESS: Yes, according to Table 3B, which enumerates the JEDEC standardized densities for the DDR2 SDRAMs, it indicates that, from one density to another, we have either a change in the number of row address bits or the number of bank address bits; and according to Table 4, it indicates which bits, in particular, are significant with regard to the change in density, and those are the ones that would be utilized in implementing rank

multiplication in those specific embodiments.
BY ATTORNEY CHANDLER:
Q. Turning back to the same paragraph that we've been focused on for a little bit now, which is Column 23 of the '417 patent starting at line 22, and Column 21 of the '215 patent starting at line 8.
The '417 and '215 patents teach, in the next sentence, that the translation logic equations of certain embodiments vary depending on the type of memory module 10 -- for example, UDIMM, RDIMM, FB-DIMM, et cetera; correct?
ATTORNEY WARRICK: Objection; form.
THE WITNESS: So reading from Column 23, starting at line 29, the text of the specification is:
"In addition, the translation logic equations of certain embodiments vary depending on the type of memory module 10 (e.g., UDIMM, RDIMM, FB-DIMM, et cetera.)"
BY ATTORNEY CHANDLER:
Q. And as we discussed earlier, the '417 and '215 patents are not limited to

particular types of memory modules; correct?
ATTORNEY WARRICK: Objection; form.
THE WITNESS: Yes, we did have questions and answers about that earlier.
BY ATTORNEY CHANDLER:
Q. And at the time of the '417 and '215 patents, Rambus-style memory modules were known to a person of ordinary skill in the art; correct?
A. Yes. We addressed that question yesterday.
Q. And nothing in the '417 and '215 patents says that the claimed inventions do not work with memory modules that use a Rambus-style protocol to communicate with the host computer; right?
ATTORNEY WARRICK: Objection; form.
THE WITNESS: Well, certainly the concept of rank multiplication doesn't work within a Rambus-style -- for example, specifically a direct Rambus-style memory module, since there's no memory controller -- no buffer or translation circuitry on such a module

to effect a rank multiplication even if you wanted to do that.

There's no -- the way that the direct Rambus channel is architected, there's no advantage to trying to fool the memory controller into thinking it's got one density when it's actually got a different density under its control.

BY ATTORNEY CHANDLER:

Q. But let me make sure I understand what you're saying, because I thought the benefit of rank multiplication is that sometimes lower-density memory devices could be a lot cheaper than higher-density memory devices.

So far am I correct there?

A. The premise of rank multiplication is that sometimes the cost per bit of a lower-density device is, for a period of time, lower than the cost per bit of a higher-density design; yes.

In a direct Rambus-style memory system, you just go ahead and use the lower-density devices. There's no need to fool the memory controller into thinking that they are higher-density devices under its control.

There's no advantage to doing that.

Q. Hold on. You're assuming that it's a Rambus memory system with Rambus memory devices.

Let's focus on the reality of the time frame, which is, in 2004 and 2005, as we discussed earlier, the most popular types of memory devices were DDR memory devices; correct?

A. In that time frame, that's true.

Q. So does the invention of the '417 and '215 patent exclude the possibility of a memory module with low-density DDR memory devices, that includes a circuit 40 translation logic for performing rank multiplication, connected to a Rambus-style communication protocol to the host computer?

ATTORNEY WARRICK: Objection; form.

BY ATTORNEY CHANDLER:

Q. Is there anything in the '417 and '215 patent that says our invention doesn't work with that?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: There's nothing in

the '417 patent that I'm aware of that would suggest to a POSITA that that sort of hybrid system would make sense with the assumption that you're trying to fool the memory controller into believing that it's controlling a different type of memory than it actually is, regardless of --

When you say that it's connected over a direct Rambus-style interface with a direct -- an actual direct Rambus channel and its protocol, there is any motivation for doing the rank multiplication that's described within the '417 vanishes.

So the hypothetical embodiment that you're suggesting would not make any sense to a POSITA.

BY ATTORNEY CHANDLER:

Q. The '417 and '215 patents teach performing rank multiplication with an FB-DIMM-type memory module; correct?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: I'm sorry. Repeat your question, please.

BY ATTORNEY CHANDLER:

Q. The '417 and '215 patents teach

performing rank multiplication with an FB-DIMM-type memory module; correct? As an example.

ATTORNEY WARRICK: Objection to form.

THE WITNESS: Is there -- is there a particular portion of the specification that teaches that that you would like me to read?

BY ATTORNEY CHANDLER:

Q. The same one that we've been looking at, which is Column 23, of the '417 patent starting at paragraph around line 22, and then the '215 patent Column 21 paragraph starting on line -- around line 8.

A. So yes, FB-DIMMs are listed in that list of module types at line 32 of Column 23 of the '417.

There are no specifics or more elaborated embodiments that are specifically related to FB-DIMMs that I'm aware of.

Q. But nothing in the '417 and '215 patent says don't perform rank multiplication with an FB-DIMM. To the contrary, the '417 and '215 patents specifically list FB-DIMM as a

Samsung Ex. 1095, p. 362
Samsung Electronics Co., Ltd. v. Netlist, Inc., IPR2023-00455

memory module that's compatible with the disclosed inventions; correct?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: There is the implication that, within the context of an FB-DIMM -- i.e., with an FB-DIMM channel in and memory devices organized on that channel -- can be -- can make use of the address -- the translation logic equations that it's talking about throughout the specification.

BY ATTORNEY CHANDLER:

Q. Could we turn to the Perego reference marked as Exhibit 1071, which I believe I put in the chat yesterday. If you need it again in the chat, let me know.

A. It's still up.

Q. Have you reviewed Exhibit 1071, the Perego reference?

A. Yes, I have.

Q. And did you review it thoroughly?

ATTORNEY WARRICK: Objection to form.

(Interruption by the court reporter to clarify the record.)

ATTORNEY CHANDLER: And I'm not sure I heard the answer.

THE WITNESS: I said, "I believe so."

BY ATTORNEY CHANDLER:

Q. Please turn to Figure 2A of the Perego reference marked as Exhibit 1071, and let me know when you're there.

A. I'm looking at Figure 2A of the Perego reference.

Q. Figure 2A of the Perego reference marked as Exhibit 1071 discloses a memory system that was known in the prior art, as indicated under the text Figure 2A; correct?

A. Yes, Figure 2A refers specifically to an S-RIMM module, which was a real proposal of Rambus in the time frame of the DDR -- I'm sorry -- direct Rambus transition.

Q. Figure 2A of the Perego reference marked as Exhibit 1071 shows multiple memory modules where each module has synchronous DRAM devices on it, as indicated on the upper right of the figure; correct?

A. Yes. So this figure shows a Rambus channel connecting three memory modules,

each of which have a memory translator hub, MTH, on an S-RIMM module using synchronous DRAMs.

Q. And are synchronous DRAMs sometimes referred to as "SDRAM" for short?

A. Yes. SDRAMs for short refer to, as we've talked about at length, a plurality of different standardized memory devices, as dictated by JEDEC.

Q. And the SDRAM memory devices shown in Figure 2A of the Perego reference marked as Exhibit 1071, those are not what we would refer to as Rambus memory devices; correct?

A. Correct.

Q. Instead, as I think you said just a moment ago, SDRAM memory devices were standardized by JEDEC. And at this time frame, DDR SDRAM memory devices were common; correct?

A. In our time frame of 2004-2005, yes, the synchronous DRAMs were common.

Q. And specifically, the DDR SDRAMs were common and had been standardized as of 2000; correct?

A. DDR SDRAMs were standardized before 2004-2005, yes.

Q. And specifically, the first DDR SDRAM standard was finalized in 2000, as shown, for example, by Exhibit 1060; and then the DDR2 standard was finalized by 2003, as shown, for example, by Exhibit 1064; correct?

A. Yes. The original DDR SDRAM is -- yes, June of 2000 is the date on the cover of that, as you said.

Q. In Figure 2A of the Perego reference marked as Exhibit 1071, the memory modules are connected to a Rambus channel, even though the memory devices are not Rambus memory devices, they're SDRAM memory devices, standardized by JEDEC; correct?

A. Yes, a I described a couple of questions ago, Figure 2A shows a Rambus channel connecting three modules, each of which has a memory translator hub, MTH, controlling a rank of synchronous DRAMs, which could be understood by a POSITA to be the DDR-type, but not necessarily.

Q. I apologize. There's some gardening tools or something outside my window. Is it -- and I never know if it gets picked up by the microphone.

Do you hear it or is it making me cut out?

A. It's -- I'm not hearing it, but you are cutting out a bit. Maybe we can a short break now and resume after they've moved on.

ATTORNEY CHANDLER: Yeah, why don't we go ahead and do that.

ATTORNEY WARRICK: Okay.

ATTORNEY CHANDLER: Thanks.

THE VIDEOGRAPHER: Off the record at 9:35 a.m. Pacific Time.

(Recess taken from 9:35 a.m. to 9:52 a.m.)

THE VIDEOGRAPHER: On the record at 9:52 a.m. Pacific Time.

BY ATTORNEY CHANDLER:

Q. Please turn to Column 10 of the Perego reference marked as Exhibit 1071, and look at the paragraph starting around line 54. Let me know when you're there.

A. I'm on Column 10.

Q. Down in the bottom right line, 54?

A. Yes.

Q. The Perego marked as Exhibit 1071

discloses embodiments using SDRAM and DDR2; correct?

A. What Column 10, starting at line 54 says is that:

"In one embodiment, memory devices 410a through 410h are Rambus DRAMs, operating at a data rate of 1066 megabits per second. Other memory devices may be implemented on module 400, for example double-data-rate 2 (DDR2) DRAM devices and synchronous DRAM (SDRAM) devices."

Q. And so if you turn to Figure 4 of Perego, Figures 4A and 4B, Perego is teaching, in the paragraph that we just looked at, that those memory devices, in Figures 4A, 4B and 4C could be Rambus memory devices or they could be DDR2 memory devices.

Is that fair?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: What I interpret the Figure 4, in its three subfigures in conjunction with that paragraph we just read, is

that the modules depicted in 4A, 4B and 4C use a Rambus-style -- a direct Rambus channel for each of 405 -- I'm sorry -- 415a through -- a and b in the case of Figure 4A; and, therefore, those memory devices in that illustration are direct Rambus RDRAMs.

The subsequent sentence of that paragraph in Column 10 indicates that you could build a device like this with SDRAMs but it wouldn't be this exact device.

BY ATTORNEY CHANDLER:

Q. And then the paragraph that we're looking at, at the bottom of Column 10 of the Perego reference marked as Exhibit 1071, indicates, at the very bottom of Column 10, that buffer device 405 can translate protocols employed by controller 310 to the protocol utilized in a particular memory device implementation, which, as we discussed, may be a Rambus memory device or may be a DDR2 memory device.

Is that fair?

A. So reading continuing from where I left off, says as you say:

"Utilizing buffer device 405

between the memory devices and the controller in accordance with the present invention may feasibly render the type of memory device transparent to the system. Different types of memory devices may be included on different modules within a memory system by employing memory buffer device 405 to translate protocols employed by the controller and the protocols utilized by the particular memory device implementations."

So, yes, this idea that the buffered device on the modules can translate protocols and provide for a unique level of multi-device-type flexibility within a single memory system is -- is unique and important.

Q. I don't know what you have in front of you right now, but I want to look at Figure 4B, and then I also want to talk about -- a little further up in Column 10. So maybe just look at Figure 4B and then turn back to Column 10 and let me know when you're ready.

A. Okay.

So I've looked at Figure 4B. It shows a module 450 that has a buffer 405 and four direct Rambus channels, and a total of 16 Rambus -- direct Rambus RDRAMs, all connected to a Rambus -- a direct Rambus channel at the bottom.

So turning back, as you asked, to Column 10. I'm now ready to consider Column 10.

Q. Column 10 of the Perego reference marked as Exhibit 1071, starting around line 22, talks about Figure 4B; correct?

A. Yes. Starting at line 22 it says, "Figure 4B illustrates a quad-channel module 450 with channels 415a to 415d."

Q. So Figure 4B of the Perego reference marked as Exhibit 1071 shows the buffer 405 communicating with the memory devices via four channels labeled 415a, 415b, 415c and 415d; correct?

A. Yes. 415a through 415d are Rambus-style channels, RDRAM -- direct RDRAM channels.

Q. And then Column 10 of the Perego reference marked as Exhibit 1071, a little bit

below line 22 goes onto explain that the channels in Figure 4B may operate in pairs; correct?

A. Are you referring to the text at line 31 in particular, or is there something else you want me to look at?

Q. It's a little bit further up, around line 25 where -- I mean, it is -- it is related to that. But it indicates 415c and 415d can be routed in parallel with 415a and 415b. And then, as you say down in 31 and -- lines 31 and 32 of Column 10, there's a discussion that channels 415a and 415b may operate simultaneously with 415c and 415d.

A. Yes. So to read it in its entirety, starting at line 32, it says:

"In alternative embodiments, channels 415a and 415b may operate simultaneously with channels 415c and 415d to realize greater bandwidth."

Q. So does Perego marked as Exhibit 1071 teach that in Figure 4B, that one embodiment is you have four separate independent channels; another embodiment is two channels

working together at a given time; and then a third embodiment is all four channels working together at the same time?

Is that a fair understanding of what Perego is disclosing in Column 10 of Exhibit 1071?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: The principal motivation for the structure of Figure 4B is given in terms of capacity and the number of memory devices that's articulated in lines 26 through 31 of Column 10.

It also subsequently talks about operating pairs of channels together, or pairs of pairs operating together.

BY ATTORNEY CHANDLER:

Q. I'm a little unclear if you're agreeing or disagreeing with --

A. I'm just reading the text of the patent.

I'm not seeing any reference to an embodiment in which there are two channels 415a and 415d, where those are operating independently. But if you have such a

citation --

Q. I thought I heard you say a and d like "dog"; whereas, I think my question was a and b like "boy."

A. I meant -- I meant to say b like "boy."

I'm not reading anything that suggests that 415a and 415b, where they both exist on the module, operating independently, that they are essentially two halves of one pair. But if there's some -- if I've missed something, then please point me to it.

Q. Well, there's Figure 4B, there's Column 10 that we've been looking at, and there's knowledge of person of ordinary skill in the art.

And what I'm trying to understand is: Is your opinion that Figure 415b is limited to only a certain use of the four channels; or does Column 10, along with the knowledge of a person of ordinary skill in the art, teach that those four channels may be used independently; or alternatively, in a different embodiment, may be used simultaneously?

ATTORNEY WARRICK: Objection;

form.

THE WITNESS: My interpretation of the disclosure of Column 10 vis-a-vis Figures -- 4B in particular, is that when there are four channels, they operate all together to provide greater bandwidth. And that's why you have multiple channels, as opposed to more devices on a single channel, or a pair of channels 415a and 415b.

So there is both the advantage of increased capacity beyond what a single pair of direct Rambus channels can support; and in additionally, there is the advantage of simultaneous operation, per line 31, 32 of Column 10.

BY ATTORNEY CHANDLER:

Q. I want to make sure I understand.

At one extreme in implementation of Figure 4B there could just be one memory device with one channel dedicated to that memory device.

Is that fair? It's taught, for example, at Column 10, line 18 or so?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: Yes, Column 15 and 16 of Column 10, referring to Figure 4A, says that you can have a single channel 415a, or it can be organized as a pair of channels 415a and 415b.

BY ATTORNEY CHANDLER:

Q. And then are you limited to -- going in the other direction, are you limited to just the pair of channels 415a or 415b, or can you actually have four channels all working together?

A. With regard to the embodiment depicted in Figure 4B, there are four channels that are working together, at least in that alternative embodiment, yes.

Q. And the Perego reference marked as Exhibit 1071 teaches that the memory devices in Figures 4A, 4B, 4C may be DDR2 memory devices; correct?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: No. It's saying that you could design something comparable to the embodiments of Figure 4A through 4C that use DDR SDRAMs.

But the memory -- the buffer device would have to be different. The signal names would be different. The signal topologies would be different. There would be little in common between such a -- the actual -- the depiction of Figures 4A and 4B to a comparable device with a different buffer circuit that provide -- that interfaces with double-data-rate DDR2 SDRAMs.

BY ATTORNEY CHANDLER:

Q. But the Perego reference marked as Exhibit 1071, you agree, does disclose an embodiment where the memory module has memory devices that are DDR memory devices; correct?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: Yes, the disclosure at the bottom of Column 10 says that although the depicted devices 410a through 410h are direct Rambus memory devices, you could build something comparable of the same general structure with a memory translation buffer device to translate the primary channel protocol to a DDR2 SDRAM protocol in order to effect a plurality of memory types within a single memory

system.
BY ATTORNEY CHANDLER:
Q. Okay. I want to ask about a different aspect of Perego, so to avoid confusion, I'm not going to be talking about the memory devices. Instead, I want to talk about the communications between the memory module and the host computer.
Do you understand what I'm focused on now?
A. Yes. That generally goes by the name of "the primary channel and the protocol thereon," within the disclosure of Perego.
Q. In your opinion, can the memory modules disclosed by Perego in Exhibit 1071 be used with the host computer that uses a JEDEC-style bus for address control and data signals between the host computer and the memory module?
ATTORNEY WARRICK: Objection; form.
THE WITNESS: Perego discloses a principal embodiment of a point-to-point link between the memory controller and the memory modules such that there's a single module at the

end of each point-to-point link.

It also discloses some details about how that primary channel in a point-to-point configuration can be effected, either multiplexed or not.

It also discusses, in a couple of places, the potential of using a bus structure instead of a point-to-point structure, and that would be something similar to the embodiment of Figure 2A.

But in no case is there an implication that it's a JEDEC-style, as you say, not conforming with any JEDEC standard, as the implementation of the primary channel that I'm aware of.

BY ATTORNEY CHANDLER:

Q. So to be clear, your opinion is that the Perego reference marked as Exhibit 1071 never disclosed any memory module that communicates with the host computer using a JEDEC-style bus for address control and data signals going between the host computer and the memory module.

Is that fair?

A. Is there something that you want

to point me to within Perego that would suggest that?

Q. No, I want your opinion.

A. So far we've looked at the bottom portion of Column 10, which talks about the memory devices being consistent with the use of JEDEC-style -- JEDEC standardized memory devices. I've talked a bit about the range of embodiments of the primary channel.

I've not talked at all about the use of a JEDEC standardized primary channel.

Q. So in informing your opinions in your declaration marked as Exhibit 2024, you did not talk about or form any opinions on the assumption that the Perego reference marked as Exhibit 1071 discloses a primary channel that's a JEDEC-style bus, meaning that the address data control signals between the host computer and the memory module would be a JEDEC-style bus.

Is that fair?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: What exactly do you mean by "a JEDEC-style bus"?

///

BY ATTORNEY CHANDLER:

Q. Well, I was trying to use your language. But what was the term that you were using to refer to the communications between the host computer and the memory module that comply with the JEDEC standard?

A. I believe I used the phrase "JEDEC standardized primary channel," but the court reporter could confirm that, perhaps.

Q. Do you understand -- when I say "JEDEC-style bus" to refer to address signals, control signals and data signals going between the host computer and the memory module, is that understandable to you?

A. For me, "JEDEC-style" would include more than just that. Those three elements being separate is not restricted to JEDEC standardized devices or modules.

So when you use "JEDEC-style," there's more baggage that goes along with that terminology than just the separation of address control and data.

Q. Can you explain that a little bit more, what you're trying to say.

A. Well, if you look at the JEDEC

standardized modules that used DDR2 SDRAMs, for example, there is a lot to the standard of the module and the constituent SDRAMs that make it JEDEC-style, in my view.

For example, the use of DQS signals, the use of chip-select signals and so forth, the ODT functionality, all of the features that are within those standards that make for a complete embodiment and useable memory module, all of that comes along with the moniker of "JEDEC-style."

So I think it's much more than just the multiplexing or the non-multiplexing of address control and data.

Q. Okay. So with that understanding of "JEDEC-style bus," the first question, just to be clear, is: At the time of Perego, JEDEC-style buses were known; correct?

A. Correct. As defined then, yes.

Q. And in your expert opinion marked as Exhibit 2024, you base your opinions on the assumption that the Perego reference marked as Exhibit 1071 does not disclose memory modules that communicate with the host computer using a JEDEC-style bus; correct?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: Given the understanding of "JEDEC-style bus," as we've just agreed to, involving more than just demultiplexing address data and control, it's -- I want to review my declaration, but it's my understanding, before I do so, that I'm not aware of any embodiments of Perego that use a JEDEC-style primary channel.

BY ATTORNEY CHANDLER:

Q. And when you say "primary channel," you're referring to the communications between the memory module and the host computer?

A. Yes, that's the -- using "primary channel" to refer to that communication path as it's used in Perego.

Q. In your opinions in your declaration marked as Exhibit 2024, you concluded that the memory modules disclosed by Perego would use a Rambus protocol for communications between the memory module and the host computer, which I understand you refer to as "the primary channel"; is that correct?

ATTORNEY WARRICK: Objection;

form.

THE WITNESS: There are certainly specific embodiments within Perego -- for example, the embodiments of Figures 4A, B and C, where the channel is, through the signal names, indicated to be a direct Rambus channel.

For other embodiments, such as those of -- let's see.

So the embodiments that utilize the buffer of Figure 5B with its configurable width interface, a POSITA would recognize that as referring to an XDR-style memory module -- sorry primary channel that incorporates that variable width capacity or feature.

BY ATTORNEY CHANDLER:

Q. And your opinion is that Figure 5B of Perego and Figures 4A through C of Perego marked as Exhibit 1071 do not use a primary channel that's a JEDEC-style bus for communications between the host computer and the memory module; correct?

A. That is -- I believe that is what I said, yes.

Q. And that was the understanding that you used in forming your opinions in your

expert declarations, marked as Exhibit 2024?

A. In part, yes. Obviously, I relied on a lot of stuff in forming my opinions, but that's one aspect of it.

Q. Please pull up the Ellsberry reference marked as Exhibit 1073.

A. Yes, I'm looking at 1073.

Q. And have you reviewed the Ellsberry referenced marked as Exhibit 1073 in both IPRs?

A. Not in detail recently; but previously, for preparing the declaration, I have.

Q. So, for example, in paragraph 199 of your expert declaration, marked as Exhibit 2024 in the '417 IPR, you referred to Ellsberry; and the corresponding cite for the other expert declaration is paragraph 204.

A. 199 of the '417, is that what you said?

Q. Yeah, and paragraph 204 of the '215 declaration marked as Exhibit 2024.

A. Let me read that paragraph to refresh my memory.

(Witness reviews document.)

Is there a question pending?

Q. Are you ready to proceed?

A. Yes.

Q. In your opinion, Figure 10 of the Ellsberry discloses a x8 module of fixed width and singular memory type with two ranks; correct?

A. That's what I say in Figure -- in paragraph 199.

You could view Figure 10 as also showing a part of a wider module, as shown, for example, in Figure 5 of Perego. I don't believe -- I'd have to look at the text with regard to Figure 10 to confirm that, but I can do that if you would like.

Q. But in your opinion, Figure 10 of Ellsberry discloses an embodiment of a x8 module -- which is to say and 8-bit-wide module -- with two ranks; correct?

I think I understood you to say just a moment ago that Figure 10 is also compatible with other types of modules. But focusing on the example you're discussing here in your expert declaration marked as Exhibit 2024, your opinion is that Figure 10 of

Ellsberry discloses an embodiment of a x8 module, which is to say an 8-bit-wide module, with two ranks; is that correct?

A. I'm just reviewing the text of Ellsberry vis-a-vis Figure 10, so give me a second.

(Witness reviews document.)

Do you know where in Ellsberry it talks about Figure 10 in particular?

Q. Well, you cite to paragraph 53 of Exhibit 1073.

A. Okay, let me look at 53. Yes, that's ...

That seems to be the only reference to Figure 10 within the specification of Ellsberry.

(Witness reviews document.)

Q. Are you waiting for me?

A. No, I'm trying to find additional insight in Ellsberry for the disclosure of Figure 10.

There is a reference to it in paragraph 21 that refers to Figures 10, 11, 12 and 13 as illustrating different configurations of memory modules, e.g., DIMMs.

A POSITA reading that would understand that there's two ways to interpret Figure 10, either as an 8-bit-wide module, which doesn't make a lot of sense in the time frame we're talking about, or as a portion of a wider structure. Typically -- DIMMs are typically 64 bits wide, so a POSITA might view it either way.

Q. All right. Let's stick with the way disclosed in your expert declaration marked as Exhibit 2024, which is that Figure 10 of Ellsberry discloses an 8-bit-wide memory module with two ranks.

Understood?

A. Technically, that's all that's visible within Figure 10, yes.

Q. In that embodiment of Figure 10 of the Ellsberry reference marked as Exhibit 1073, the two ranks are denoted as 1006 and 1008; is that correct?

A. In paragraph 53 of Ellsberry, it calls them banks, not ranks.

But other than that, yes, it -- the exact term -- language of paragraph 53 is:

"Figure 10 illustrates a single chip-select memory

configuration in which one control unit 1002 and one bank switch 1004 are used to control two memory banks 1006 and 1008, each memory bank having two memory devices 1010 and 1012 in separate data buses 1014 and 1016."

Q. The two ranks that you were referring to in your expert declaration marked as Exhibit 2024 are those identified as 1006 and 1008 in Figure 10 of the Ellsberry reference marked as Exhibit 1073; correct?

A. Yes, which Ellsberry refers to as "banks."

Q. And on that issue of banks versus ranks, you understand that there was a change in terminology where originally the word "banks" with a B was used more broadly to refer to different types of things, one of which we now more commonly refer to as rank with an R; correct?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: Yes, I am familiar with the transition of the terminology from

"banks" to "ranks," since I initiated it.
BY ATTORNEY CHANDLER:
Q. And in what year did you initiate it?
A. The -- it was in the 1996 time frame. We looked at my "New DRAM Technologies" report yesterday. It was in the creation of that report that I recognized the need for a new term, and I started using it in my talks and writings. And it was, over time, accepted and propagated through the industry, although clearly, as far as Ellsberry is concerned, they didn't quite get the message.
Q. Well, to be fair to Ellsberry, in the original DDR SDRAM standard it uses the term "bank with a B; and then it was in the next version of the standard, the DDR2 standard, that JEDEC at least transitioned to using the term "rank" with an R; correct?
A. Yes. It took time for the industry to recognize the value of having two separate terms.
Q. But it's not just that it took time for the industry; it's that the DDR standard -- which still exists today, right? --

says "bank" with a B, and it used it in the way that the DDR2 standard says "rank" with an R; correct?

A. Yes, because it predated -- the creation of the DDR standard predated the more widely -- wider acceptance of the term "rank" to mean what it does today.

Q. And the DDR -- the DDR standard still exists? There are still DDR memory devices; right?

A. You can still buy them and the standard still is valid. They obviously -- not in their interest to go back and change the terminology of an existing standard. That would just create confusion.

Q. So in fairness to Ellsberry, when Ellsberry wrote "bank" with a B, that was the terminology that was correctly used in the DDR standard.

Now, Ellsberry also refers to DDR2. In that context, "rank" with an R would be the terminology used, and a person of ordinary skill in the art would understand all of that; correct?

A. Yeah. A person of ordinary skill

in the art at the time of 2004-2005 would appreciate that there are still references out there that are using "bank" where more properly "rank" might have been used.

Q. And this transition of terminology from "bank" with a B to "rank" with an R, that's discussed, for example, in the Jacobs textbook that we looked at previously, Exhibit 1070, on page 413; correct?

A. You want me to pull it up and confirm that?

Q. Sure. Just look at it quickly. I'm pretty sure he's talking about the same thing you're talking about, but why don't you go ahead and double-check.

A. What was the page number again?

Q. 413.

A. There we go, yeah, sorry. I was on 14.

Yes, we discussed this yesterday, and it is about the term "rank" and how it's changed over -- from "bank" to "rank" over time.

Q. And in the figure on page 413 of Exhibit 1070 on the right-hand side, Jacob

crosses out "bank" and puts an arrow to "rank"; correct?

On the right-hand side, do you see that big X over the word "bank"?

A. Yes, that is what he depicts in the figure. He doesn't really describe what he's doing there in the text, but that is exactly what he has done in the figure, crossing out the word "bank" and an arrow pointing to the word "rank."

Q. So turning back to Figure 10 of Ellsberry in Exhibit 1073, there are two ranks -- using the term "rank" as we currently understand it -- and those are identified as 1006 and 1008; correct?

A. My recollection is that Ellsberry accesses one of its banks at a time. Each transaction goes to one bank or the other bank, and that would make them ranks. If I'm incorrect about that, then they would together be a single rank, per the normal usage of that term.

But that's my understanding, sitting here today.

Q. The two ranks that you were

referring to in your expert declaration marked as Exhibit 2024 are 1006 and 1008 in Figure 10 of the Ellsberry reference marked as Exhibit 1073; and we can see that 1006 gets chip-select signal CS0A, and rank 1008 gets a different chip-select signal, CS0B; correct?

A. Yes, that's what's shown in Figure 10.

Q. And then Figure 10 of the in Ellsberry reference marked as 1073 shows that rank 1006 has a data bus 1016, and then rank 1008 has a different data bus 1014; correct?

A. Correct. They are two separate data busses -- actually, 10 -- the arrows point to the DQS of one half and the DQA of the other. So let me double-check the text to see if it clarifies.

I doubt -- it refers to -- in figure -- I'm sorry -- in paragraph 53, that data buses 1014 and 1016 come from the two banks of memory devices 1010 and 1012.

Q. In Figure 10 of the Ellsberry reference marked as Exhibit 1073, data bus 1016 is 8 bits wide and connected to switch ASIC 1004, and Exhibit 10 -- sorry -- data bus 1014

is also 8 bits wide and is also connected to the switch ASIC 1004; correct?

A. Yes. The data buses include both data signals and DQS signals in both cases, yes.

Q. And then in Figure 10 of the Ellsberry reference marked as Exhibit 1073, on the left side of the switch ASIC 1004 there's another data bus that's only 8 bits wide; correct?

A. Yes. The data bus on the left side of the switch ASIC has a data bus that's listed as a 8-bit-wide, DQ0 through 7, and DQS0 and DQS1. It's -- the data portion of that is divided into two halves, because there are separate DQS signals for the top and half nibbles of that byte.

Q. And so in summary, in Figure 10 of the Ellsberry reference marked as Exhibit 1073, the switch ASIC 1004 has an 8-bit data bus on the left side of the figure, but then on the right side of the figure has got two separate 8-bit data buses; correct?

A. Yes, where the data buses include DQs and DQSs, yes.

It's been about an hour since

we've been going. Can we have another break, please?

ATTORNEY CHANDLER: Sure, yeah. Just a few minutes.

THE WITNESS: Okay.

THE VIDEOGRAPHER: I'm sorry, Counsel. Did you want to break now?

ATTORNEY CHANDLER: Yeah, just for a few minutes.

THE VIDEOGRAPHER: Off the record at 10:47 a.m. Pacific Time.

(Recess taken from 10:47 a.m. to 10:54 a.m.)

THE VIDEOGRAPHER: On the record at 10:54 a.m. Pacific Time.

BY ATTORNEY CHANDLER:

Q. Do you have Figure 10 of Ellsberry marked as Exhibit 1073 in front you?

A. Yes, I do.

Q. Are you familiar with the concept of a data collision?

A. Generally, yes.

Q. How would you explain what a data collision is?

A. A data collision, generally

speaking, is when two drivers on a single wire are trying to communicate simultaneously and, thereby, neither of them getting their message across.

Q. In Figure 10 of the Ellsberry reference, marked as Exhibit 1073, if the switch ASIC were to be operated incorrectly or unwisely such that it were to receive read data from rank 1006 at the same time that it receives data from rank 1008 and if it were to try to drive the data from both 1006 and 1008 onto the data bus to the left of switch ASIC 1040, is that an example of something that could result in a data collision?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: Well, first of all, it would be the control unit ASIC that would be misbehaving if that were to happen, not necessarily the switch ASIC of Figure 10.

It's not really a data collision in the same sense that I articulated it with two drivers on a single wire. It's more of a matter of -- there -- the switch ASIC being unable to select both pieces of data simultaneously to

drive onto a single wire or bus on the other side of its multiplexing function.

BY ATTORNEY CHANDLER:

Q. So if I understand you correctly, in Figure 10 of the Ellsberry reference marked as Exhibit 1073, the control ASIC on the bottom left of the figure controls the switch ASIC on the upper left of the figure; correct?

A. There is a connection between the two shown, which a POSITA would understand to be a -- how control information is sent from the control units to the switch ASIC. A POSITA might reasonably assume that that control tells the switch ASIC which of the two data buses is to be driven at a given point in time onto or from the ASIC DQs on the other side.

So if there is an error here, it's on the part of the control unit, and the switch ASIC would just do what it's told: Select one or the other, but it could not select both at the same time, for obvious reasons.

Q. So to avoid a data collision in Figure 10 of the Ellsberry reference marked as Exhibit 1073, the control ASIC needs to send control signals to the switch ASIC to operate

the switch ASIC in the proper manner to avoid a data collision.

Is that fair?

ATTORNEY WARRICK: Objection to form.

THE WITNESS: Again, I don't think you're using "data collision" the same way that I was, and I don't find that word within Ellsberry. So it's -- I'm confused as to why you continue to call this a data collision scenario.

BY ATTORNEY CHANDLER:

Q. The switch ASIC in Ellsberry receives a signal and then drives it out the other side of the switch ASIC; correct?

A. That's a simplistic and narrow view of what the switch ASIC does, but that's a first step in describing its functionality.

Q. And in particular, sticking with Figure 10 of the Ellsberry reference marked as Exhibit 1073, the switch ASIC has a total of 16 DQ data lines coming into it and only 8 DQ data lines going out of it, and each one of the 16 DQ data lines coming into the switch ASIC has a driver; correct?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: The drivers are on the DRAMs or on the ASIC? I'm sorry, I didn't follow your question.

BY ATTORNEY CHANDLER:

Q. Both.

So there's 16 DQ data lines coming into the switch ASIC. Those signals are driven by the DRAMs. But then once those 16 data signals are inside the switch ASIC, each one of those 16 data lines has a driver ready and able to drive that signal out to the left of the switch ASIC, shown in Figure 10 of Exhibit 1073; correct?

A. Yes. So wherever there is a data flow on a signal wire, there is a driver to effectuate that.

The fact that you have more DQs on one side of the switch ASIC than on the other means that either one or the other is used at a time, sequentially, or there is some form of frequency multiplication going on that allows both to be interleaved within a single data burst, as you see in the Halbert reference, for

example.

Q. But sticking with the Ellsberry reference, Figure 10 of Exhibit 1073, if all 16 drivers in the switch ASIC were to drive data at the same time onto the 8 data lines coming out to the left of the switch ASIC, that would cause a collision; right?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: It's -- that's an inaccurate use of the word "collision" as it's normally understood by a POSITA in that you don't -- what you're describing is a -- the inability of the switch ASIC to drive two bits onto one line at the same time, which is generally true although not universally true.

In this case, if both banks of DRAMs are trying -- have been told to output devices simultaneous -- I'm sorry -- have been told by the control unit ASIC to output read data at the same time towards the switch ASIC, either the switch ASIC is going to ignore one of the two or it has some mechanism for interleaving the two temporally within the burst. And that -- I don't see any -- not

sufficiently familiar with Ellsberry to say that that's ruled out, but that's not how a normal JEDEC-compliant DIMM would operate.

So it's not a data collision as it is normally understood.

BY ATTORNEY CHANDLER:

Q. But the reason there's no data collision in Figure 10 of the Ellsberry reference marked as Exhibit 1073 is because the control unit ASIC at the bottom properly controls the switch ASIC; is that fair?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: There is -- there would be no collisions within the operation of the embodiment of Figure 10 provided the switch ASIC is not trying to write write data at the same time that either of the banks is trying to write read data onto data buses 1016 or 1014.

That would be a description of a collision where two drivers are trying to drive something onto the same wires at the same time.

BY ATTORNEY CHANDLER:

Q. And let me put it this way.

I'm not saying a person of

ordinary skill in the art would do this, but just to understand the importance of the control unit ASIC in Figure 10 of Exhibit 1073, if we wanted to, we could program that control unit ASIC in Figure 10 of Exhibit 1073 to cause a collision; right?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: Presumably, yes. But if the control unit ASIC simultaneously caused the ASIC -- switch ASIC to believe that a write was happening and that it should drive whatever it received on its ASIC DQ signals and to drive them onto one or the other or both, conceivably, of the data buses 1016 and 1014, and simultaneously told the banks of DRAMs 1006 -- I'm sorry -- 1006 and 1008 to simultaneously drive write -- read data onto those same data buses, that would be causing a data collision on those data buses, and that would not yield proper operation of either the reads or the writes.

BY ATTORNEY CHANDLER:

Q. And another example of proper operation, which you wouldn't want to do but in

theory could happen is if the control unit ASIC were programmed in a certain way, in Figure 10 of Exhibit 1073, the control until ASIC could tell the switch ASIC to simultaneously drive 16 data lines out to the left of the switch ASIC onto 8 data lines, and the result would be nothing useable to the recipient.

Is that fair?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: I think your statement precluding your question is not well formed, because unless we're talking about a multi-valued communication system, you can't drive 2 bits onto one line in a binary-communication setup. So the -- unless there's some frequency multiplication going on here, the -- you can't drive 2 bits onto one line at the same time. The driver just is unable to do that. It's -- and so your -- your hypothetical is nonsensical in that sense.

Also, it's not a matter of programming the control unit ASIC; it's matter of designing it with a flaw. It's not likely to be a highly programmable unit.

BY ATTORNEY CHANDLER:

Q. You said just a moment ago you can't drive 2 bits onto one line at the same time. And I understand that you wouldn't want to do that, but I'm a little confused by your suggestion that it can't be done.

I mean, I can have one wire with two drivers both pointed on to the wire, and they could both drive at the same time and that would cause a collision; right?

A. That is what I've been describing as a collision: Two things driving onto one wire at the same time.

That's different from one driver driving 2 bits at the same time, which is what your previous hypothetical described, where you had -- you were trying to get the ASIC switch to drive 16 bits of data onto 8 bits of data bus. And that is possible, certainly, within the context of different nonbinary communication systems, or in the context of transmission line communication systems, where you have bits flowing past each other on the same wire without there being a problem associated with the communication therein.

But in regard to memory subsystems of the type that we're talking about here, in the time frame we're talking about here, the -- that's not typically possible.

Q. Take a look at Figure 4 of the Ellsberry reference marked as Exhibit 1073.

A. Figure 4.

Q. Looking at Figure 4 do you see in Figure 4 that there are two read drivers, one in box 402 and the other in box 404?

A. Yes.

Q. If we turned on those two read drivers 402 and 404 at the same time, is it fair to conclude that a collision may result?

A. Yes.

ATTORNEY WARRICK: Objection to form.

THE WITNESS: Yes, if there was a circumstance where they both were driving different bits of information at the same time, then that would represent a collision on the DQ line shown there.

However, the decode -- config decode and the read/write logic in boxes 406 and 408 would be designed to not do that and to

drive -- have either one or the other driver drive data at a time.

It's also unlikely that you would implement it this way, since the drivers in the read buffers of 402 and 404 are large and expensive circuits, and you provide the multiplexing functionality upstream from that.

But conceptually, this is a reasonable interpretation of what's going on.

BY ATTORNEY CHANDLER:

Q. So turn back to Figure 10 of the Ellsberry reference marked as Exhibit 1073.

Do you have that in front of you?

A. I'm back at 10.

Q. In theory, the switch ASIC in Figure 10 of Exhibit 1073 could have 16 read drivers all driving at the same time onto the 8-bit data bus coming out to the left of the switch ASIC, and in that situation there would be some collisions.

Is that fair?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: There -- if you have 16 read drivers connected in pairs to 8

lines, and you -- and the control functionality within the switch ASIC was flawed and caused both of a pair of read drivers, in your hypothetical, to drive simultaneously onto a single wire, that would constitute a collision on that bus, if the bits were different.

BY ATTORNEY CHANDLER:

Q. And so to avoid a data collision in Figure 10 of the Ellsberry reference marked as Exhibit 1073, the control unit and the switch ASIC need to operate properly with correct timing and correct direction so that only 8 of the 16 read drivers and the switch ASIC are driving read data out to the left onto the 8-bit data bus; is that fair?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: Again, and that's true in the context of DDR SDRAMs and DDR SDRAM modules.

There are communication systems where you can drive different drivers simultaneously without error, either through an open collector-type system or, as I said, with a transmission line, but that would involve

transmitters at different locations.

But certainly with regard to an open collector communication system or signaling system, there would be no collision. It would -- per se, that would be a different function for that -- the effect of the wire and the two drivers happening -- driving simultaneously.

So, in short, a collision is not strictly necessary, but in the context of this particular figure and the DDR SDRAMs, a collision would happen in that circumstance.

BY ATTORNEY CHANDLER:

Q. And this particular figure, being Figure 10 of the Ellsberry reference marked as Exhibit 1073?

A. The Figure 10 of 1073, if implemented according to the structure of Figure 4, which as I noted is not practical, but which is conceptual in this case, if that conceptual implementation of a pair of drivers per bit line was implemented in Figure 10, then yes, under that contrived circumstance, there would be a collision.

Q. And I think you said a moment ago

something about open collector-type system.

A. Yes.

Q. To be clear, DDR memory devices do not use open collector for the data signals; correct?

A. Yes, that -- I did indicate that in my answer.

Q. So do you agree that DDR memory devices do not use open collectors for data?

A. DDR SDRAMs do not use open collector drivers; correct.

Q. And Figure 10 of the Ellsberry reference marked as Exhibit 1073, the address and control signals AC and CS go to the control ASIC 1002 at the bottom; correct?

A. Yes, the control unit ASIC is marked as unit number 1002, and it has AC and CS inputs on its left-hand side.

Q. And the switch ASIC 1040 in Figure 10 of the Ellsberry reference marked as Exhibit 1073 does not receive the address and control signals AC and CS from the memory controller; correct?

A. In this figure, Figure 10, the exact form of the information communicated

between the control unit ASIC and the switch ASIC is not presented or described. So it's plausible that the chip-selects and the address and control information is just forwarded to the switch ASIC and it determines what's going on; or alternatively, the control unit is doing some pre-decode and sending a different but equivalent sets of information from the control unit ASIC to the switch ASIC.

Q. But either way, the address and control signals AC and CS, they first go to the control unit 1002 in Figure 10 of the Ellsberry reference marked as Exhibit 1073; correct?

A. Yes. Figure 10 illustrates the AC and CS inputs to the control unit Item 1002 and not such inputs to the switch ASIC 1004 and only the ASIC pipe connections between those two units.

Q. And the control unit -- or, rather, control unit ASIC 1002 -- would be able to determine, from the address and control signals, which rank of memory would need to output data to the switch ASIC; correct?

A. Is there a particular paragraph or set of paragraphs in the specification of

Ellsberry that deals with the functionality of the control unit ASIC that I should review?

Q. I'm basing this on your opinions and your previous review of how things work.

A. Then I should take some time to study this reference a little bit longer then; because there are different ways it might be done, and I don't remember off the top of my head today exactly what Ellsberry says about the operation of control unit ASIC.

Do you want me to do that?

Q. Respectfully, you spent over 15 hours preparing for this deposition; right?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: As I indicated, I had not spent much of that time looking at Ellsberry. So I am not as familiar with it as I have been with some of the other references that you have put in front of me.

BY ATTORNEY CHANDLER:

Q. Ellsberry was one of the references used in the grounds of both petitions; correct?

A. That is correct.

Q. Then it is a reference that you reviewed and opined on in your expert declarations marked as Exhibit 2024; correct?

A. Yes, I did review it and opined on it back when this -- my declaration was drafted, and I have said I have not reviewed it in detail since.

Q. Am I correct that in a JEDEC-style memory system, the address and control signals, including the chip-select signal, will tell you which rank of memory needs to output data in response to a read command?

A. Certainly, if we bring up a JEDEC standard for a UDIMM multi-rank memory module, we will see that it is the chip-select inputs, called the S inputs, to the modules that determine -- or indicate to the module which of the plurality of ranks are to be involved in the present transaction.

Q. And Figure 10 of the Ellsberry reference marked as Exhibit 1073 teaches to a person of ordinary skill that the control unit receives chip-select signals and then outputs chip-select signals, and the two ranks of memory devices receive the output of chip-select

signals; correct?

A. What's not clear to me without further review is whether this is implementing a JEDEC standardized module or something else with different behavior than what I described pertaining to the UDIMMs that are standardized by JEDEC.

Q. Well, Ellsberry marked as Exhibit 1073 implements rank multiplication; right?

ATTORNEY WARRICK: Objection; form.

(Witness reviews document.)

BY ATTORNEY CHANDLER:

Q. Are you not sure about this? I mean, you did read Ellsberry; right?

A. As I said, months ago, when I was preparing the declaration, I did, yes. I'm reading portions of it again now.

Q. For example, in the abstract, last sentence, Ellsberry marked as Exhibit 1073 teaches "making two smaller-capacity memory devices emulating a single higher-capacity memory device"; correct?

A. Yes, the last sentence of the abstract is:

"That is, the invention expands the addressable memory banks on a module by making two smaller-capacity memory devices emulate a single higher-capacity memory device."

And in the context of the JEDEC -- SDRAM memory systems generally, that is what we call rank multiplication.

Q. And, for example, on Figure 7A, 7B, 7C, 7D, E and F, Ellsberry teaches the use of what the '417 and '215 patents refer to as a density transition bit, but which Ellsberry labels a physical bank select, in the column second from the right; correct?

A. That's what the column second from the right is called, "physical bank select bit." And it refers to a column or row address bit accordingly to -- depending on the configuration specified in the different rows of that table.

Q. And that's similar to the density transition bit in the '417 and '215 patents that we looked at a little bit earlier; correct?

ATTORNEY WARRICK: Objection;

form.

THE WITNESS: Similar, yes. I don't know if it's precisely identical in all cases. We'd have to look at the different configurations that are being talked about in the two references. But the general idea appears to be similar.

BY ATTORNEY CHANDLER:

Q. Turning back to Figure 10 of the Ellsberry reference marked as Exhibit 1073, the control unit ASIC 1002 is going to receive the address and control signals including one chip-select signal; and it can perform rank multiplication, meaning that it will output two chip-select signals, labeled CS0A and CS0B; correct?

ATTORNEY WARRICK: Objection; form.

BY ATTORNEY CHANDLER:

Q. Or are you not sure?

A. Repeat the question, please.

Q. In Figure 10 of the Ellsberry reference marked as Exhibit 1073, the control unit ASIC 1002 is going to receive an address and control signals including one chip-select

signal, and the control unit can perform rank multiplication, meaning that it will output two chip-select signals, labeled CS0A and CS0B; correct?

ATTORNEY WARRICK: Objection; form, form.

THE WITNESS: Yes, it seems that the control unit ASIC is selecting one of the two banks, as they're referred to here, according to the table of Figure 7.

BY ATTORNEY CHANDLER:

Q. And again, for clarity, what you just referred to as a bank is what today we would refer to as a rank with an R; correct?

A. Generally speaking, that's true.

Q. And the control unit in Figure 10 of the Ellsberry reference marked as Exhibit 1073 will assert one of the two chip-select signals to select one of the two ranks, 1006 or 1008, to perform the read operation; correct?

A. Yes, that's my understanding, based on my quick review of Ellsberry, that the read or write transactions involve one or the other of Ellsberry's banks 1000- -- in Figure 10, 1006 and 1008.

Q. And then the control unit ASIC in Figure 10 of the Ellsberry reference marked as Exhibit 1073 needs to tell the switch ASIC 1004 what to do at that point in time to properly drive the read data from the targeted rank onto the 8-bit data bus coming out to the left of the switch ASIC.

Is that generally fair, at a high level?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: Per the disclosure of Figure 10 in particular, where the only connection between those two ASICs is the ASIC pipe and the control information associated with the command and the address, in particular, is presented initially only to the control unit ASIC, it is -- somewhere, either in the switch ASIC or in the control unit ASIC, there is going to be a sequencing that goes on in order to control the data paths within the switch ASIC to do -- and the drivers and the receivers and all the other associated circuitry to effect the proper data transfers into and out of the module.

BY ATTORNEY CHANDLER:

Q. If you turn to the Halbert reference marked as Exhibit 1078. Let me know when you have it in front of you.

A. I have the front page of patent , , to Halbert in front of me.

Q. And John Halbert was at Intel; correct?

A. At the time it appears to be the case, yes.

Q. And did you know any of these named inventors on the Halbert reference marked as Exhibit 1078?

A. I have no recollection of having met any of them. So I perhaps did, perhaps did not.

Q. And you reviewed the Halbert reference marked as Exhibit 1078; correct?

A. Yes.

Q. And you believe you understand the Halbert reference --

A. Yes.

Q. -- marked as Exhibit 1078?

A. I do believe I understand the Halbert reference.

Q. Take a look at Figure 4 in the Halbert reference as marked as Exhibit 1078. And am I correct it illustrates a memory module 100 that is m bits wide? M as in Mary.

A. Yes, on Figure 4 of Halbert we have a box around the whole thing, 100; and we have a DQ bus, that is lowercase m bits wide exiting and entering that box 100 on its left-hand side.

Q. M as in Mary; right?

A. M as in Mary; correct.

Q. And in Figure 4 of the Halbert reference marked as Exhibit 1078, the memory module 100 includes, on the right side, two ranks of memory, 140 and 142, each of which is also m bits wide -- M as in Mary; correct?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: Just as we were struggling with terminology issues with Ellsberry, we have terminology issues here as well.

The Halbert calls unit 140 a rank and unit 142 a rank even though they operate together as a 2-m-bit-wide structure, which we

would call a single rank consistently with how we've been using the term yesterday and today.
BY ATTORNEY CHANDLER:
Q. As a technical matter, however, it would be within the skill of a person of ordinary skill in the art to operate rank 140 and rank 142 in Figure 4 of Halbert marked as Exhibit 1078 as two separate ranks. If the person of ordinary skill in the art wanted to, they could do that, for example, using two separate chip-select signals; correct?
ATTORNEY WARRICK: Objection; form.
THE WITNESS: So that would require a modification of the device in multiple respects, and it would be an entirely different disclosure and it would not be satisfying the principal motivation as articulated in Halbert.
BY ATTORNEY CHANDLER:
Q. Because as a technical matter, it's not that hard to make two ranks operate independently from each other; correct? That was known and done?
ATTORNEY WARRICK: Objection; form.

THE WITNESS: Two ranks generally operate independently from each other.

In this case, they are not independent of each other. If you were to dramatically change the purpose and functionality and timing and everything with respect to the disclosure of Figure 4 of Halbert and how it operates, as illustrated by Figures 5 and 6, then, you know, you would have an entirely different device with two ranks and a multiplexer, which would be -- the multiplexer would be irrelevant at that point and you would end up with a standard UDIMM, as defined by JEDEC.

BY ATTORNEY CHANDLER:

Q. Or you would end up with something like Figure 10 of Ellsberry marked as Exhibit 1073 that we were just looking at; right?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: Yes. If you make enough changes to Halbert, you end up with something that looks similar to Ellsberry, but without the dual-read drivers that you were

insisting upon for inclusion in Ellsberry's ASIC -- data path ASIC in order to get your collisions that you were clearly wanting to establish.

BY ATTORNEY CHANDLER:

Q. I don't want collisions. I'm not trying to say I want collisions. I was just trying to understand the hypothetical. So I'm not pro-collision.

A. Right. So --

Q. I'm anti-collision.

A. Well, we're not driving autonomous vehicles yet, so -- I'm not in favor of automotive collisions either, and I try to avoid data collisions in my designs as well.

But the point being that the data path circuit 120 -- I forget its formal name -- hold on.

Q. Data interface.

A. Data interface circuit. Yes, thank you.

So as it's structured, the data interface circuit has a single driver onto the DQ bus that is m bit wide so it cannot have a collision onto that bus, as we had been

hypothesizing about Ellsberry.

Q. Fair to say there can be a collision within data interface circuit 120. If you are one of those crazy pro-collision types of people, you could have 126 and 128 inside data interface circuit 120, both driving at the same time, and that could cause problems if your MUX/DeMUX isn't doing what it should be doing.

I mean, there's all sorts of room for collisions, if that's what you're looking for in life; isn't that fair?

ATTORNEY WARRICK: Objection; form. Also scope as to questions regarding data collisions.

THE WITNESS: With regard to data collisions, as we agreed, it was defined and used by a POSITA in 2004-2005, you would not have collisions within the data interface circuit 120. The MUX/DeMUX 124 would necessarily select or drive one or the other of the DQ0, DQ1 buses, but those two buses would not be connected physically together in order to cause a data collision -- i.e., the simultaneous driving of a single wire by both register 126 and register 128.

BY ATTORNEY CHANDLER:

Q. And is that arrangement of two drivers connected to a MUX to avoid a data collision, was that a typical arrangement at the time?

A. Well, certainly whenever you have a 2-to-1 multiplexing and that is bidirectional, you need a MUX/DeMUX. So this is a circuit that was well known in the art and a POSITA would understand its function and operation.

Q. In Figure 4 of the Halbert reference marked as Exhibit 1078, memory module 100 includes a data interface circuit 120, which is coupled to rank 140 by an m-bit-wide data bus RQ0, and is also coupled to rank 142 by another m-bit-wide data bus RDQ1; correct? That's literally what's drawn in Figure 4?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: It's drawn as two separate m-bit-wide buses RDQ0 and RDQ1. But if, for example, you look at Figure 5 and the timing of those two lines, you see that they are effectively two halves of a single 2-m-bit-wide RDQ bus.

BY ATTORNEY CHANDLER:

Q. In Figure 4 of the Halbert reference marked as Exhibit 1078, the data interface circuit 120 includes data registers 126 and 128, multiplexer/demultiplexer 124 and, towards the left, buffer 122; correct?

A. Among other things, yes.

Q. And those are controlled by control signals coming from the module controller 110 below them in Figure 4; correct?

A. Yes, there's a plurality of signals that are shown going from the module controller 110 into the data interface circuitry 120 to control its constituent parts.

Q. The control signals in Figure 4 of the Halbert reference marked as Exhibit 1078 coming from the module controller 110 include a DIR signal -- spelled D-I-R -- which determines the direction of the data transfer; a REG_SEL signal, which selects either the data coming from rank 140 or the data coming from rank 142; and RDQS, RDQS0, and RDQS1 signals that control buffer 122, register 126 and register 128; correct?

ATTORNEY WARRICK: Objection;

form.

THE WITNESS: So RDQS0 and RDQS1 only control registers 126 and 128. I don't think that's what you said.

BY ATTORNEY CHANDLER:

Q. RDQS, RDQS0 and RDQS1 --

A. I'm sorry. Right, I will -- yes. RDQS controls 122. So your question was well formed.

If you would -- I think, the answer is yes, you described that accurately.

Q. I want to look at an annotated version of Figure 5 of Halbert which is in the petition. Do you have the petition handy or do you want me to put it in the chat?

A. If it's not already open, I would appreciate you put it in the chat, please.

ATTORNEY CHANDLER: All right. So I'll put Paper 1 from each IPR into the chat.

(Exhibit Number P001 was previously marked for identification.)

BY ATTORNEY CHANDLER:

Q. All right. So go ahead and open both petitions, and I'll tell you where to go after you got them both open.

A. Okay.

Q. So in the petition for the '417 patent, go to page 126. And then in the petition for the '215 patent, go to page 131. And you should see the same annotated figure in both places. It's an annotation of Figure 5 of the Halbert reference marked as Exhibit 1078.

A. And I'm sorry, the page number in the '215 was, again?

Q. 131.

A. Yes, I see that those figures are identical in the two petitions.

Q. And you understand that those figures in the two petitions are taking Figure 5 of the Halbert reference marked as Exhibit 1078 and then are adding color annotations. So in other words, everything in black and white was from the original Figure 5 of the Halbert reference marked as Exhibit 1078, and everything in color has been added.

Understood?

A. Yes, I understand that.

Q. And you see that there's the label "Module CAS Latency (4.0)" in the annotated figures on page 126 of the '417

petition and page 131 of the '215 petition?
A. Yes.
Q. And then there's also the annotation that says "Memory CAS Latency (2.5)"?
A. I see the annotation.
Q. Those annotations are they understandable to you, what they're referring to?
A. They are referring to temporal differences between different clock edges.
Q. Can you explain that a little bit more, what you mean.
A. Well, the -- annotation for the module CAS latency is showing the temporal difference between T4 and T8; and the memory CAS latency annotation is showing the temporal difference between T5 and T7n.
Q. So at a high level, is it accurate that in the -- in Figure 4 of the Ellsberry reference marked as Exhibit 1073, when you have a read command with the timing as shown in Figure 5, that the memory module receives the read command at time T4 and starts to output the data from the module to the host computer starting at time T8?

A. Yes. The R command and RADD buses are captured at T5 by the memory devices in both 140 and 142, and they output their data beginning at T7n for capture at T8.

Q. But before T5, the read command is received by the module controller on the memory module at time T4; correct?

A. Yes, that's correct. It takes a full cycle, between T4 and T5, for the command and address information to flow through the module controller 110 of Figure 4 of Halbert.

Q. So Halbert's memory module receives the read command at time T4, but the memory devices don't get the read command until time T5.

Is that fair?

A. They don't capture the read command until the rising edge of clock indicated at T5.

Q. And so there's a one-clock-cycle delay in the memory module of Halbert marked as Exhibit 1078 between the time when the memory controller sends the read command to the memory module, which is happening around time T4; and the time when the memory devices get the read

command, which is going to be around time T5.

Is that fair?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: A more precise formulation of that sentence would be it is one cycle difference between when the memory controller 110 captures the read command and when the DRAMS that are in 140 and 142 together capture the read command at T5.

BY ATTORNEY CHANDLER:

Q. And then in the Halbert reference marked as Exhibit 1078, after the memory devices capture the read command at time T5, it takes those memory devices 2.5 clock cycles, according to Figure 5, to output the first piece of read data from the memory devices? Is that -- I'm sorry.

It takes a total of 2.5 clock cycles from the time the memory devices receive the read command for them to output the read data and for that read data to go through the data interface circuit 120 and to come out the other side off the module; is that correct?

ATTORNEY WARRICK: Objection;

form.

THE WITNESS: I'm sorry --

BY ATTORNEY CHANDLER:

Q. I'm sorry. I messed it up.

A. Yeah, I thought so.

Q. There are a lot of arrows.

A. There are many.

Q. In the DRAM memory devices in the Halbert reference marked as Exhibit 1078, those memory devices, as shown in Figure 5, take 2.5 clock cycles from the time the memory device receives the read command until the time that the first piece of data is output from those memory devices.

Is that fair?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: I would use "captures" instead of "receives" because it's clearer and less ambiguous.

But -- so if we say it's 2.5 -- 2-1/2 cycles from when the memory devices in 140 and 142 together capture the read command at T5 to when the DQS signal is asserted on the MDQS line, indicating the start of the first bit

period of the data coming out of those memory devices.

BY ATTORNEY CHANDLER:

Q. And then after the data first comes out of the memory devices, according to Figure 5 of the Halbert reference marked as Exhibit 1078, there will be an additional delay of approximately 0.5 clock cycles for that data to travel from the right side of the data interface circuit 120 to the left side of the data interface circuit 120, as shown in Figure 4?

Is that a fair summary?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: It's actually less than that, because the data on the RDQ0 and RDQ1 buses is not captured until T8, and they -- it flows through the circuit -- data interface circuit 120 very quickly. And it's the -- the strobe on the DQS signal 2, the memory controller is asserted on -- at the same clock edge T8 initiating the output of that first piece of data.

So the actual delay through the

data interface circuit 120 is, depending on how you count, about a quarter of a cycle from the center of the eye input to the center of the eye on the output.

BY ATTORNEY CHANDLER:

Q. But the net result, as shown in Figure 5 of the Halbert reference marked as Exhibit 1078, is that the module controller captures the read command at time T4, and it's a total of 4 clock cycles until time T8 that the memory module starts outputting the first piece of read data back to the host computer; correct?

A. Yes. The time difference between T4, when the module captures the read command and the rising edge of DQS on the output DQS signal indicating the availability of data A1, is four cycles.

Q. And then just focusing on the DRAM memory devices, as we discussed though, the delay from the time that the DRAM memory device captures the read command until the time that it outputs the first piece of read data is 2.5 clock cycles, in the Figure 5 of the Halbert reference marked as Exhibit 1078?

A. Correct?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: Yes. What this figure shows is that the time difference between the DRAM capturing the read command and when the rising edge on MDQS, indicating the beginning of the first bit period on the RDQ0 and RDQ 1, is 2-1/2 cycles.

The difference between the two is one cycle of latency through the memory controller 110, half a cycle of communication delay between the memories and the data interface circuitry 120, and about a quarter of a cycle of latency through the data interface circuitry 120.

ATTORNEY WARRICK: Counsel, would it be a good time to perhaps have a longer break? I know it's about noon on the West Coast and later for those of us further east.

THE WITNESS: Unless you're about to wrap up entirely. Otherwise, yes, I'd like a lunch break.

ATTORNEY CHANDLER: Well, I mean, I heard both of you. Let me at least try to finish up with this figure.

BY ATTORNEY CHANDLER:

Q. Do you still have the annotated version of Figure 5 of Halbert in front of you?

A. Yes, I do.

Q. I was trying to listen to your last answer, and I think we agreed that the total there a from start to finish is 4 clock cycles. I guess I was having a little trouble following what you were saying, because it didn't seem to add up to 4.

A. So the communication delay between the output of MDQS strobe signal, indicating the start of the data transmission from the DRAM to the data interface circuitry 120 is -- and then there's a half-cycle delay between that transition and when the data is actually captured by the data interface circuit 120. And then there's a nominal delay within the memory device between when it captures that data and when it immediately starts to send the data.

The reason that the totals were slightly more than one cycle is because of the difference between when the DQS signals are asserted for read data and when the center of

the eye, indicating where the data is capture-able.

But what is clear is that the bulk of the difference between those two annotated times comes from the delay of the command and address through the memory controller 110; and through the communication on the MDQS and RDQ0 and RDQ1 buses and that the amount of delay through the data interface circuit 120 is relatively small.

Q. But if you add up all of the delays that you just referred to, it's a total delay of four clock cycles; is that fair?

A. That's how we measure latency in -- read latency for JEDEC standard memory devices from the capture of a read command on the rising edge of clock to the rising edge of DQS, indicating the start of a bit period for the first piece of data of a burst.

Q. I'm still a little unclear if you're agreeing with me or disagreeing with me.

A. I'm agreeing with you that the annotated differences of 4 cycles and 2-1/2 cycles correspond to how latencies are measured within JEDEC standardized SDRAMs and SDRAM

modules, and that the annotations are for 4 cycles and 2-1/2 cycles respectively.

Q. And you're referring to the annotation on page 126 of the '417 petition and page 131 of the '215 petition; correct?

A. Correct, yes.

Q. Netlist did not invent SDRAM memory devices; correct?

A. Is this a new topic or just wrapping up?

Q. It's wrapping up. Potentially it's not a long series of questions, but, I mean -- unfortunately, I don't -- I don't -- it's like 10 questions depending on --

ATTORNEY WARRICK: Counsel, I mean, I just want to note we've had several occasions where the witness has asked for a break and --

(Simultaneous cross-talk.)

ATTORNEY CHANDLER: I'm trying to wrap up.

THE WITNESS: If the 10 questions are all of the nature of "Netlist didn't invent," then we can deal with those quickly. If you're going to get into technical details,

then we should break for lunch.

ATTORNEY CHANDLER: I'm not going to get to the technical details, but, unfortunately, I can't totally control what you're going to tell me.

THE WITNESS: No, of course not.

BY ATTORNEY CHANDLER:

Q. Netlist did not invent SDRAM memory devices; correct?

A. I do not know if they were JEDEC members through the development of those standards. If they were, then they had a hand in it. I don't know.

Q. Netlist's '417 and '215 patents do not purport to have invented SDRAM memory devices; correct?

A. Which variety of SDRAM devices are you talking about?

Q. Any variety.

A. I'm not aware of any references within the specifications of those patents that would attribute the invention of an SDRAM-style memory to Netlist.

Q. Netlist's '417 and '215 patents do not purport to have invented DDR1 or DDR2

SDRAM memory devices; correct?

A. I'm not aware of any statements to that effect within the specifications of the '417 or '215 patents.

Q. Netlist's '417 and '215 patents did not invent ranks of memory devices -- ranks with an R -- correct?

A. No. As we've seen many times over the last two days, those concepts date back to the 1990s and before.

Q. Netlist's '417 and '215 patents did not invent the memory controller for the computer system; correct?

A. Memory controllers have been in existence for as long as there have been memories; and so no, the concept of a memory controller was not invented by Netlist.

Q. Netlist did not invent, in the '417 or '215 patents, address signals, control signals or data signals; correct?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: Those general categories of signal types were not invented by Netlist and have, again, been around as long as

there have been memories and memory systems.
BY ATTORNEY CHANDLER:
Q. Netlist's '417 and '215 patents did not invent chip-select signals; correct?
A. Chip-select signals have been associated with memory devices since at least the 1960s, so they are not novel to anything invented in the 2000s.
Q. Netlist's '417 and '215 patents did not invent CAS latency; correct?
A. CAS latency.
So the concept of a CAS latency dates back to the very first DRAMs in the 1960s, so that concept was not novel to Netlist in the 2000s.
Q. Netlist's '417 and '215 patents did not invent the DIMM memory module or the RDIMM memory module; correct?
A. You're referring to the JEDEC standardized UDIMM and RDIMMs in particular?
Q. Well, they certainly didn't invent those; right?
A. Again, they may have been part of the JEDEC standard-forming procedures or processes for those modules and so may have had

a hand in that. They certainly are not claiming to have done so within the specification of the '417 and '215 as such.

Q. And Netlist's '417 and '215 patents do not purport to have invented buffered memory modules where the data signals are buffered; correct? That was known prior to the '417 and '215 patents?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: The -- I'm sorry. You're referring to buffered modules in particular or -- just repeat the question, please.

BY ATTORNEY CHANDLER:

Q. Netlist's '417 and '215 patents do not purport to have invented memory modules with buffers for the data signals; those were known before the '417 and '215 patents; correct?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: There were modules that included buffers prior to the filing date of the -- or the priority date of the '417 and '215. The specifics of the additional circuitry

on the modules is the essential aspect of the novel features -- claimed features of the '417 and '215 patents.

BY ATTORNEY CHANDLER:

Q. And some examples that we've talked about of memory modules with buffers for the data signals include the Perego reference marked as Exhibit 1071, the Ellsberry reference marked as Exhibit 1073, and the Halbert reference marked as Exhibit 1078; correct?

A. I take --

ATTORNEY WARRICK: Objection; form.

THE WITNESS: I take exception with Ellsberry being characterized as prior art. I thought we had gone through the provisional -- the arguments about the provisional not supporting all of the claim elements at issue. And if that is, in fact, true, then Ellsberry, by my understanding, today is not prior art.

Certainly Halbert, I think if it's prior art, includes a buffer circuit. Perego, if it's a prior art, includes a buffer circuit as well.

///

BY ATTORNEY CHANDLER:

Q. Putting aside whether or not they're prior art, the Perego reference marked as Exhibit as 1071, the Ellsberry reference marked as Exhibit 1073, and the Halbert reference marked as Exhibit 1078 are all memory modules with buffers for the data signals; correct?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: Again, I've been -- let me start again.

Putting aside the issue entirely of which of those are prior art and which of them are not prior art, they all include some degree of circuitry on the data paths of those modules.

BY ATTORNEY CHANDLER:

Q. Do you have any corrections or clarifications you'd like to make to any of the testimony that you've given to me today or yesterday?

A. None that come to mind at present, but we'll see during redirect.

ATTORNEY CHANDLER: I'll pass the

witness.

If we can do this -- if we could go off the record and then, Phil, if you could just put in the chat how long you want me to go away for -- and I realize it may take you a moment to decide that question. But if you could just tell me when you want me to come back, just put it in the chat, and I'll be back.

ATTORNEY WARRICK: Well, I mean, I think it would probably make sense for us to plan for a longer break so the folks who want to get food can do so.

ATTORNEY CHANDLER: Why don't you --

THE VIDEOGRAPHER: Counsel, would you like to go off the record?

ATTORNEY CHANDLER: No, I want us all to be on the same wavelength here.

Why don't you talk, Phil, to whoever you need to talk to, and then let us all know in the chat how quickly you want us to come back. Because if it's -- you know, I don't want to go away for an hour if you're just going to come back with a couple of questions, so ...

ATTORNEY WARRICK: Well, I think

it's fair to say between -- it's -- it's not just going to be a couple of questions.

ATTORNEY CHANDLER: Okay. So we'll go off the record and you can tell us what time to come back then.

ATTORNEY WARRICK: Okay.

THE VIDEOGRAPHER: Off the record at 12:18 p.m. Pacific Time.

(Luncheon recess taken from 12:18 p.m. to 1:35 p.m.)

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P R O C E E D I N G S

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THE VIDEOGRAPHER: On the record at 1:35 p.m. Pacific Time.

EXAMINATION

BY ATTORNEY WARRICK:

Q. Dr. Przybylski, do you recall being asked yesterday various questions by Petitioner's counsel related to claim construction?

A. Yes, generally.

Q. And I believe you stated yesterday that for purposes of your declarations, Exhibit 2024 in these two IPRs, that you applied Netlist's proposed claim construction for the term "rank."

Do you recall that?

A. Yeah, I think I misspoke in that answer.

Q. What claim construction for the term "rank" did you apply in your declarations, both marked 2024 in these IPRs?

A. So with regard to, for example, paragraph 165 of my declaration in the '417, I specifically say that I'm applying the Petitioner's proposed construction, not Netlist's.

Q. Is that true for the entirety of your declaration in the '417 patent IPR?

A. Yes.

Q. Is that also the case for your declaration in the '215 patent IPR?

A. Yes.

Q. And Petitioner's proposed construction -- part of Petitioner's proposed construction, I should say, suggests that a rank could be one or more memory devices; correct?

A. I believe that to be the case. I don't remember what paragraph I -- here it is.

Paragraph 62 I talk about the Court's construction, and 60 I talk about the Petitioner's construction. "One or more memory devices," yes.

Q. And am I correct that in forming your opinions in these IPRs and in preparing the declarations marked 2024 in these two IPRs, that you apply this construction, including the

concept that a -- that one on more memory devices on a memory module could constitute a rank?

A. Yes. I applied Petitioner's proposed construction in its entirety, which is an independent set of one or more memory devices on a memory module that act together in response to command signals, including chip-select signals, to read or write full-bit width of the memory module.

Q. Would your opinions in these two declarations, Exhibit 2024, be different had you applied your personal understanding, as articulated yesterday, that a rank requires a plurality of memory devices?

A. No. First of all, that personal understanding was based on the perspective of a POSITA in 2004 and '5.

But to answer your question more directly, no, my opinions that the arguments put forward in the petition and declaration are -- fail to invalidate or render obvious any of the claims of the -- these two patents would remain the same regardless.

Q. And in your declarations, did you

provide any opinions regarding claim construction for any terms in the '417 or '215 patents?

A. No, I did not provide any new claim construction. I list the proposed constructions that are in the record, and I applied Petitioner's -- I did not render an opinion as to which or any of those were a correct construction.

Q. Now, yesterday you were also asked some questions about SO-DIMMs.

Do you recall that?

A. SO-DIMMs were one of the DIMM types that were in the list of -- enumerated DIMM types or memory module types in one of the references.

Q. And do you recall also being asked questions yesterday about FB-DIMMs?

A. Yes, similarly.

Q. Can I have you take a look at the '417 patent, Column 6, beginning around line 43. And this is a paragraph we've looked at both yesterday and today.

A. Yes, I have that in front of me.

Q. And you'll recall that there is

identical text in the '215 patent?

A. Yes. Mr. Chandler pointed that out.

Q. I'd like to ask you a couple of questions about the sentence that begins around line 43. I'm going to read it:

"Furthermore, memory modules 10 compatible with embodiments described herein include, but are not limited to, single in-line memory modules (SIMMs), dual in-line memory modules (DIMMs), small-outline DIMMs (SO-DIMMS), unbuffered DIMMS (UDIMMs), registered DIMMs (RDIMMs), fully-buffered DIMMs, (FB-DIMM-DIMMs), rank-buffered DIMMS, (RBDIMMs), mini-DIMMs, and micro-DIMMs."

Did I read that correctly?

A. Yes, you did.

Q. So when the patents say that these various types of memory modules are compatible with embodiments described in the patent specifications, what does that mean to

you?

A. It means that these style of modules, which are literally compatible with the embodiments disclosed in the specification of the '417 and '215. In other words, if you were to take the SO-DIMM outline and you could create a new module that incorporates features from the specification of the '417 and '215 patents and create a new SO-DIMM, that would not be a standard -- standardized SO-DIMM but would have that form factor, and in that way these module types are compatible with the embodiments disclosed in these specifications.

Q. And that's, to be clear, not the same as being an embodiment of the claimed invention; correct?

A. No. There are not embodiments that are disclosed that fit any of those physical parameters for the -- or -- of those module types.

Q. So, for example, were -- would the POSITA have been aware of any SO-DIMMs at the time of the invention that would constitute embodiments of the '417 or '215 patents' claimed inventions?

A. Well, the JEDEC standards for SO-DIMMs have not been brought into the record here. I haven't reviewed those in a long time, but it's my recollection that as of 2004 and 2005 there were not any SO-DIMMs with, for example, buffers on the DQ lines, that they were more along the line of UDIMMs, the DRAMS were just connected directly out to the contacts of the SO-DIMMs.

Q. And do you understand the claimed inventions of the '215 and '417 patents to require such buffers on the DQ lines?

A. Yes. It's -- it's -- there is the -- there are numerous elements within these patents that recite buffers and the like that require circuitry between the DRAMs and the pins of the modules.

Q. This portion of the specifications also reference FB-DIMMs. Do you recall when FB-DIMMs were standardized?

A. It's my recollection that FB-DIMMs were first standardized in 2007.

Q. Now, you have opined that the priority date for the '215 and '417 patents should be at least as early as January of 2005;

correct?

A. More precisely what I've opined on is that the arguments within the petition and the corresponding declaration that attempt to invalidate or set the priority date of the claims to be after -- some point after the date associated with the '087 provisional are rebutted effectively; and that's so the claims at issue deserve that priority date absent any additional arguments to the contrary.

Q. And in that '087 application, from -- that was filed in January of 2005, the inventors did not include all of the same exact text that is included in the specifications of the '417 and '215 patents; right?

A. Indeed. That's how provisionals work. You're allowed -- between the provisional and the final application, you're allowed to flesh out and fully teach the invention. There's no expectation that the full text of the patent be present within the provisional.

Q. And --

ATTORNEY CHANDLER: Phil and Dr. Przybylski, if you could leave time between the question and answer for me to object.

I have an objection to that last question that it was leading.

THE WITNESS: I will try.

BY ATTORNEY WARRICK:

Q. Dr. Przybylski, do you recall if the '087 provisional included any disclosures regarding FB-DIMMs?

A. I don't recall specifically, but we can check and search for FB-DIMM in there. I don't think there was any -- I don't recall any reference to the FB-DIMMs per se in the '087.

Q. And so is it possible that the language regarding FB-DIMMs in the specifications of the '417 and '215 patents was added subsequent to that January 2005 provisional application?

ATTORNEY CHANDLER: Objection; leading.

THE WITNESS: Yeah, it's clear -- if the language is not in the provision, it was -- provisional application, it must have been added at some point during the prosecution after that time.

BY ATTORNEY WARRICK:

Q. What understanding, if any, do

you have about the relationship between embodiments that are disclosed in a patent specification and embodiments that are claimed in those patents?

A. Not all disclosed embodiments are claimed; not all claims encompass all disclosed embodiments.

Q. Now, yesterday you may recall there were questions from Petitioner's counsel regarding Exhibit 2031, which you cited in your declarations.

Do you recall that?

A. 2031 being Appendix -- Appendix X of -- at -- at Section 4.1.2.10 of JEDEC standard 21-C, Release 13.

Q. Yes. And I believe you testified yesterday that you were not aware of the specific publication date of that document, Exhibit 2031; is that right?

A. Yes. This document doesn't have a date on it; it only has a release date -- a release number. And Counsel didn't provide any documentation vis-a-vis the date of this -- of Release 13.

Q. When you cited Exhibit 2031 in

your declarations, Exhibit 2024 in these two IPRs, was it your belief that the cited information reflected the knowledge of a POSITA at the time of the invention?

A. Yes. Generally speaking, the idea of SPDs containing information about the modules predates the DDR2 instantiation of that standard, and so it's -- I think I opined to the effect that the -- the idea of SPDs generally and their contents would have been known to a POSITA in the 2004-2005 time frame.

Q. And would that include the specific information that you cited in Exhibit 2031 in your declarations in these two IPRs?

A. Yes, it would.

Q. And is that the case regardless of when Exhibit 2031 was published?

A. Yes. Of the -- the two references to 2031 in my declarations, the contents -- the portions that I cite to from 2031 would have been in the -- in the knowledge of a POSITA of 2004-2005.

Q. I'd like to look at Exhibit 2031 if we can. Could you pull that up, please.

A. I'm looking at 2031, the first page of it at least.
Q. Can you look at page 8, please.
A. Page 8.
I'm looking at page 8.
Q. And on page 8 we have a table that appears to be related to module data width. Is that right?
A. Yes. "Byte 6: Model Data Width" is the heading on the top of page 6.
Q. And do you recall answering questions yesterday about module data width in the context of the JEDEC21-C standard?
A. Generally, yes.
Q. And in this table on page 8 of Exhibit 2031, we have various entries with different possible -- with different data width values provided, such as 32, 33, 64, et cetera. Is that right?
A. Yes.
Q. And some of the lines on this table have dashes rather than a number provided for the data width column of the table.
Do you see that?
A. I do.

Q. Do you know what that indicates?
A. The -- only some of the values of the 8-bit field represented by bit 0 through bit 7 are allowed; and rather than only listing the allowed ones, the authors of this standard have put in rows of the table with dashes to signify to the reader that there are gaps in the values that are allowed. And any values that are in those gaps are not allowed and, therefore, are indicated as such with dashes.
Q. So in light of this table on page 8 of Exhibit 2031 under the JEDEC21-C standard, would a 4-bit module data width be permitted?
ATTORNEY CHANDLER: Objection; leading.
THE WITNESS: So what this table says is that the SPD does not define a 4-bit-width module type. So it's not proper to attempt to identify the module width to be 4 bits.
BY ATTORNEY WARRICK:
Q. What about 8 bits?
A. Similarly.
Q. Were 4- or 8-bit-width

JEDEC-compliant modules known to a POSITA at the time of the invention of the '417 and '215 patent?

ATTORNEY CHANDLER: Object to form.

THE WITNESS: Not DIMMs. There were 8-bit-wide SIMMs that were archaic. I don't even know if they predate JEDEC's involvement in the standardization of modules. They may just have been industry standard without being JEDEC industry standard modules. I don't know that.

BY ATTORNEY WARRICK:

Q. You also answered questions yesterday regarding the definition of the POSITA, or the person of ordinary skill in the art, for purposes of your declarations related to the '417 and '215 patents.

Do you recall that?

A. Generally speaking, yes.

Q. And I believe at various times you indicated that certain technologies or potential prior art may have predated that hypothetical POSITA by some number of years; is that right?

A. Yes, I remember questions along those lines.

Q. And how, if at all, did it impact your analysis for purposes of your declarations, Exhibit 2024 in these two IPRs, that any potential prior art may have come -- may have existed in time substantially before the -- let me -- let me rephrase that question. I apologize.

How, if at all, did the age of any potential prior art affect your analysis for purposes of your declarations, Exhibit 2024 in these two IPRs?

A. I'm not aware of any archaic prior art that was older than the professional experience of a POSITA, as we discussed yesterday, having any impact on the analysis in my declarations.

Q. So you did not ignore any prior art by reason of it being too old?

A. No.

Q. And is it your view that a POSITA, at the time of the invention of the '417 and '215 patents, would have ignored any potential prior art by reason of it being too

old?

A. No. The POSITA would not ignore ideas or prior art because it's too old.

Q. Today you were asked questions by Petitioner's counsel about the concept of rank multiplication.

Do you recall that?

A. Yes.

Q. Is it your understanding that the claims of the '417 and '215 patents are directed to the concept of rank multiplication?

A. No, I don't think that the independent claims of these patents relate to rank multiplication at all.

Q. On the topic of rank multiplication, Petitioner's counsel asked you a lot of questions about Figure 1 of the Perego reference, which is Exhibit 1070.

Do you recall that?

A. Let me bring up 1070.

ATTORNEY CHANDLER: I'm sorry. What figure did you say?

ATTORNEY WARRICK: Figure 1.

THE WITNESS: 1070 is Jacobs' book.

BY ATTORNEY WARRICK:

Q. I apologize.

A. Perego is 1071.

Q. Yeah, I apologize. So strike that.

Did not mean Perego.

A. You mean the --

Q. Of the '417 and '215 patents.

A. Yes, that makes more sense.

Q. So you recall being asked questions about rank multiplication in the context of Figure 1 of the '417 and '215 patents, yes?

A. Yes, correct.

Q. Is there anything in Figure 1 of the '215 and '417 patents that would be indicative of rank multiplication to a POSITA at the time of the '417 and '215 patent inventions?

A. Repeat that back for me, please.

Q. Sure.

Is there anything in Figure 1 of the '215 and '417 patents that would be indicative of rank multiplication to a POSITA at the time of the inventions?

A. To the extent that there's a

single chip-select shown going in and a POSITA viewed that as a single chip-select as opposed to a plurality of chip-select signals going in and a plurality of chip-selects going out, that might be indicative of some form of rank multiplication going on. But there are -- that's not the only possible interpretation of Figure 1.

Q. When you say "a chip-select signal going in," are you referring to a signal being input to what's labeled as 40 in Figure 1?

A. Yeah. The -- between memory controller 20 and circuit 40, there's a line that's drawn as bidirectional, labeled CS with a pound sign, CS bar, between those two. That's what I'm referring to.

Q. And, in your opinion, how would a POSITA at the time of the invention interpret that CS# label in Figure 1 of the '417 and '215 patents?

A. There are a range of possibilities. Its bidirectionality would be a point of confusion to a POSITA, because chip-select signals don't generally flow back from a module towards a memory controller. It

may be also that the chip-select CS# line could be a chip-select bus, as the address and control lines are obviously buses and are labeled identically.

So there are a number of possibilities that would come to mind of a POSITA looking at Figure 1.

Q. In your opinion, are there embodiments of the '417 and '215 patents that do not include rank multiplication?

A. Yes. As I talk about in paragraph 78 of my '417 declaration, rank multiplication is just one of the ideas found in the specification of the '417 and is generally restricted to a range involving the Verilog examples. But it's not a concept that's found within the claims of the '417 or '215.

Q. You were also asked questions today by Petitioner's counsel regarding Rambus-style memory modules and memory devices; is that right?

A. Yes.

Q. Do the '417 and '215 patents provide any indication to a POSITA at the time of the inventions that the claimed inventions of

the '417 and '215 patents could be used in a Rambus-style environment?

ATTORNEY WARRICK: Objection; leading.

THE WITNESS: No, there's -- there's really no suggestion of that within the figures or specification of the '417 or '215.

BY ATTORNEY WARRICK:

Q. Is there any indication in the -- or suggestion in the '417 and '215 patents that embodiments of the claimed inventions could incorporate both JEDEC-style SDRAM memory devices and a Rambus-style primary channel?

A. I don't find any support for the idea that embodiments of the '417 and '215 could -- would use a Rambus channel of any of the flavors that we are familiar with in this matter. It's all directed towards -- the embodiments are all directed towards variations of the SDRAMs and the other JEDEC standardized devices and modules.

Q. You were also asked questions today about the Perego reference, which is Exhibit 1071.

A. Yes.

Q. Does Perego contain any suggestion to a POSITA that its claimed invention could be implemented with a JEDEC-style primary channel?

A. Perego's claims?

Q. Correct.

A. I have not paid a lot of attention to Perego's claims since it was referenced as prior art. Only to the extent that the claims are part of the original.

Q. Let me ask you a better question.

Does Perego contain any suggestion to a POSITA that the embodiments disclosed in Perego included a JEDEC-style primary channel?

A. In my discussions with Mr. Chandler, we characterized JEDEC-style primary channel as one that not just had separate address control and data signals but which also embodied the other features and aspects of DDR2 SDRAM modules. And as a result -- or with that view of what a JEDEC-style primary channel might be, there is no suggestion within Perego that I'm aware of that suggests a JEDEC-style primary channel.

Q. Does Perego provide any suggestion to a POSITA that the disclosed embodiments in Perego could be used with a JEDEC-style primary channel?

A. I'm not aware of any such suggestions within the specification of Perego.

ATTORNEY WARRICK: I have no further questions at this time.

ATTORNEY CHANDLER: Take a break for about ten minutes?

ATTORNEY WARRICK: Sure.

ATTORNEY CHANDLER: And then I'll have at least some questions.

THE VIDEOGRAPHER: Off the record at 2:15 p.m. Pacific Time.

(Recess taken from 2:15 p.m. to 2:26 p.m.)

THE VIDEOGRAPHER: On the record at 2:26 p.m. Pacific Time.

FURTHER EXAMINATION

BY ATTORNEY CHANDLER:

Q. Dr. Przybylski, I want to follow up with you first with respect to claim construction for the term "rank." All right?

A. Yes.

Q. And so you understand there's a disagreement where Samsung has taken the position that "rank" can include one or more memory devices, and Netlist has taken the position that "rank" requires two or more memory devices.

Understood?

A. Yes.

Q. Did I hear you correctly say, in response to questions from Netlist's counsel, that you are not offering any opinion disagreeing with Samsung's proposed claim construction for the term "rank" with respect to Samsung's position that the term "rank" can include just one memory device?

A. I've not been instructed to offer any particular opinions with regard to claim construction, so I presented the different alternatives. And as I noted in redirect, the -- I applied Petitioner's construction to the "rank" element of the independent claims.

Q. So to be clear, in these IPRs you are not offering any opinions disagreeing with Samsung's proposed construction for the term

"rank"; correct?

A. I'm not offering any opinions disagreeing or agreeing with Samsung's construction of "rank."

Q. Can you pull up the '417 and '215 patents again.

A. Both or just one?

Q. Well, I want to cover both. It's up to you whether you want to look at both or just want to focus on one, with the understanding that the specification in the figures are the same in both.

A. All right. I'm looking at the '417 right now.

Q. You were asked questions about whether the claims of the '417 and '215 patents concern rank multiplication, by counsel for Netlist.

ATTORNEY WARRICK: Objection; form.

THE WITNESS: That was a statement or a question?

BY ATTORNEY CHANDLER:

Q. Do you recall a moment ago being asked by counsel for Netlist about whether or

not the claims of the '417 and '215 patents require rank multiplication?

A. I remember some questions on redirect about that. I think they were phrased a little bit differently, but yes, I understand what you're talking about.

Q. The '417 and '215 patents disclose rank multiplication; correct?

A. As I describe in my declaration, the rank multiplication is one of the aspects of the embodiments -- or some of the embodiments of the '417 and '215, but there are other ideas and disclosures and embodiments as well.

Q. And I think you said that in your opinion, the independent claims -- or at least some of the independent claims, the '417 and '215 patents do not require rank multiplication; correct?

A. There is a single independent claim for the '415. There are --

Q. You said '415.

A. I apologize. '417. It's been a long two days. My apologies.

There's a single independent claim for the '417, and there are only two

independent claims for the '215. And it was my answer to counsel that rank multiplication is not a essential feature of either -- of any of those claims.

Q. But there's a difference between "essential feature" and whether the claim encompasses rank multiplication; right?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: "Encompasses" -- would you clarify what you mean by "encompasses."

BY ATTORNEY CHANDLER:

Q. What I'm getting at, and I think you understand, is that the way independent claims work is that they're broader than the dependent claims. So you can have an independent claim in the '417 and '215 patents that covers two embodiments, one of which is rank multiplication, one of which is not; and then there can be dependent claims that further limit the independent claim to one of those two embodiments, such as rank multiplication; correct?

A. Yes. That's a general statement

of how dependent claims work.

Q. And there are at least some dependent claims in the '417 and '215 patents that require rank multiplication; right?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: You want to point me to a specific dependent claim that we are talking about?

BY ATTORNEY CHANDLER:

Q. Sure. Look at dependent Claims 9 through 11 of the '215 patents.

A. I'll bring up the '215, one moment, please.

And you said Claim 9?

Q. 9, 10, 11.

(Witness reviews document.)

A. None of these use the word "rank multiplication." You have to -- I haven't looked at these particular claims in a long while, so I'd have to spend some time studying them to understand whether these plurality of different chip-select signals constitute rank multiplication or some broader concept that was also enabled by the specification of these

patents.

Q. But the point is, you have never offered the opinion and you're not trying to offer the opinion now that the claims of the '417 and '215 patents are somehow such that they do not include rank multiplication; right?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: I have not offered any opinions as to whether the scope of these claims do or do not include modules that implement rank multiplication.

BY ATTORNEY CHANDLER:

Q. Could you turn to Column 23 of the '417 patent and Column 21 of the '215 patent.

A. I have the '215 in front of me. What lines of Column 21?

Q. I'll just ask it more generally. It's the same point, which is, in Figure 1 of the '215 and '417 patents, to be clear, that Figure 1 of the '417 and '215 patents can include rank multiplication.

Now, you're saying there may be other embodiments where it doesn't have rank

multiplication; but the flip side is the patent makes clear that it can implement rank multiplication; correct?

A. There are definitely columns that talk about -- and the tables and the like that talk about rank multiplication and how do you implement it vis-a-vis the density transition bits and so forth.

Q. And that can all be done in Figure 1 of the '417 and '215 patents; correct?

A. Yes. Figure 1 is sufficiently generic that it could show embodiments including -- that include rank multiplication, as well as others that do not.

Q. Could you turn to Column 6 of the '417 patent, and I think it's also Column 6 of the '215 patent. Bottom of Column 5, top of Column 6 of the '215 patent. Let me know when you're there.

A. You're referring to the load isolation section or something else?

I'm looking at the Column 6 of the '417.

Q. It's the same section that counsel for Netlist was asking you about. It's

talking about all the different types of memory modules and all the different types of memory devices that are compatible with the '417 and '215 patents.

A. Yes.

Q. So Column 6, lines 43 or so; and then in the '215 patent, Column 5, line 63 or so.

A. Yes, I see that section of Column 6 of the '417.

Q. And there were some questions that you were asked about SO-DIMM and FB-DIMM and whether those were compatible with the disclosed invention of the '417 and '215 patents.

Do you recall those colloquies?

A. Yes.

Q. And your testimony was that an SO-DIMM in the prior art would not satisfy the claimed invention.

Instead, if I understand your point correctly, your point was that you could take an SO-DIMM from the prior art and then modify it to practice the inventions disclosed by the '417 and '215 patents.

Is that fair?

A. I think the essence of my testimony was that these terms refer either to form factors or to JEDEC standardized specific modules.

To the extent that this list of buffer types is referring to just the form factors, you could have a POSITA take the inventions of -- or embodiments of the '417 and implement them on a SO-DIMM form factor, for example; but that the standardized SO-DIMMs of the 2004-2005 time frame do not, for example, include buffers on the data paths.

Q. Okay. So in your opinion, as of January 19th, 2005, the priority date that you have said applies, in your opinion, a person of ordinary skill in the art would be able to implement rank multiplication on an SO-DIMM; is that correct?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: SO-DIMMs are constrained in the amount of area that they have on them relative to standard DIMMs; but in theory, that's -- that's generally true.

The ...
BY ATTORNEY CHANDLER:
Q. And to take another example, in your opinion, a person of ordinary skill in the art as of January 19th, 2005, would be able to take a UDIMM, which is to say an unbuffered memory module, and that person could implement rank multiplication on the UDIMM; correct?
ATTORNEY WARRICK: Objection; form.
THE WITNESS: Given the teachings of the '417 and '215 in front of them, they would have the teaching necessary to implement the rank multiplication units in the circuit 40 or 42, et cetera, depending on the particular figures we are talking about. And just as they could in a full-sized DIMM module -- the UDIMMs are the same size, so they would be able to modify a UDIMM to incorporate the additional integrated circuits and other -- and features that are disclosed with the rank multiplication embodiments of the '417 and '215.
BY ATTORNEY CHANDLER:
Q. And so if you took a UDIMM as of January 19th, 2005, and tried to implement

rank multiplication as taught by the '215 and '417 patents, you would need to add buffers to the data lines; is that right?

Because those don't exist on a UDIMM; right? There's no buffers on the data lines of a UDIMM, so you would have to add new data buffers to the UDIMM to implement the rank multiplication taught by the '417 and '215 patents; correct?

A. That would certainly be one way to accomplish the inclusion of rank multiplication features onto a UDIMM. I'm not prepared to say that's the only way. There are certainly figures that suggest that they're not required in the teaching of the '417, but, again, this is not a concept that I've thought a lot about to this point.

Q. But, in your opinion, a person of ordinary skill in the art would know how to put data buffers on a UDIMM, and would also know how to put the circuit 40 of the translation logic to implement rank multiplication, as of January 19th, 2005, without any of that Verilog code; correct?

ATTORNEY WARRICK: Objection;

form.

THE WITNESS: I'm sorry. What about the Verilog code? I didn't catch that.

BY ATTORNEY CHANDLER:

Q. The Verilog code is not something the person of ordinary skill needs, right to implement the rank multiplication? Or do you think they do need it?

A. Well, certainly the Verilog code is part of the disclosure of the '417 and includes -- is part of the embodiments of that specification. To the extent --

Q. But it's not -- but not -- I'm focused on January 19th, 2005; right? The '087 didn't have any Verilog code.

A. I see your point.

Yeah, it would be more of a challenge for a POSITA. But I think that a POSITA would be able to re-create that Verilog code from the concepts of a rank multiplication in the context of adding that to a UDIMM.

Q. Right. So in your opinion, a person of ordinary skill in the art as of January 19th, 2005, looking at the '087 provisional marked as Exhibit 1005 had the skill

to take a UDIMM, add data buffers to the data lines, add logic to perform rank multiplication based on the density transition bit, and would have the skill to create the Verilog code to program that logic to operate correctly.

Is that fair?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: I want to pull up the '087. Do you have the exhibit number for that?

BY ATTORNEY CHANDLER:

Q. 1005.

A. There it is. Sorry.

Yes, I believe there's sufficient disclosure in the '087 for a POSITA to do that.

Q. You were asked some questions about when FB-DIMM was standardized and when it was known.

Do you recall those questions?

A. In general, yes.

Q. I think you said that your recollection is that FB-DIMM was standardized in 2007. But clearly the inventors of the '417 and

'215 patent were talking about it before 2007; right?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: What we established was that the '087 provisional application does not mention the FB-DIMMs and that at some point during the provision -- the transformation from the provisional to the final specification, discussion of the FB-DIMMs were added. I do not know at what point in the prosecution of the '417 and '215 that particular language was added.

BY ATTORNEY CHANDLER:

Q. But you understand that the '417 and '215 patents haven't changed with respect to the specification in the discussion of FB-DIMM since the nonprovisional application was filed; right?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: I'm sorry. I have not looked carefully at the full prosecution history, so I don't know when the last continuation-in-part or the non- -- the -- which

version of the -- which application actually contains that language for the first time.

BY ATTORNEY CHANDLER:

Q. And my point is a little broader than that, which is: Regardless of when FB-DIMM was finally standardized by JEDEC, which may have been in 2007, persons of ordinary skill in the art before that time, they would have known about FB-DIMM and that it was coming; right?

A. Not necessarily. The -- it would have been discussed within JEDEC committee meetings prior to that; and senior engineers within the companies participated in the particular JEDEC committee that was thinking about standardizing FB-DIMMs would clearly have been aware of the proposal and the various ballots being voted on with regard to the ultimate standard.

But a POSITA outside of that select group would not necessarily have heard the term or been aware of it prior to the release of the standard. Or at least a -- at least of press releases foreshadowing that release.

And, again, none of that is in

the record here, so we don't know when that happened.

(Exhibit Number 1012 was previously marked for identification.)

BY ATTORNEY CHANDLER:

Q. We'll take a look at Exhibit 1012, which I put in the chat, which is the nonprovisional application filed July 1st, 2005.

A. This is patent number '386. That one?

Q. Yes. And that's part of the priority chain of the family of patents.

A. Okay, I have that up.

Q. So Exhibit 1012, filed July 1st 2005, refers to FB-DIMM in Column 6, line 8 or so; correct?

A. Yes. The FB-DIMMs are mentioned there at -- across lines 8 and 9.

Q. And the language in Column 6 of Exhibit 1012, from approximately lines 1 through 30, about how the memory module is compatible with embodiments described in Exhibit 1012 include DIMM, SO-DIMM, FB-DIMM, et cetera, that's the same language that appears in the

'417 and '215 patents marked as Exhibit 1001; correct?

A. It appears to be. I haven't actually compared them word by word, but the general list is the same, yes.

Q. And that's not surprising, that a person of ordinary skill in the art would have known about FB-DIMMs even before JEDEC finished the standards for FB-DIMMs; correct?

A. No, my testimony of a few moments ago is that a POSITA would not necessarily have heard of FB-DIMMs well in advance -- certainly years in advance of the release of the standard, unless there was a product that the standard was following in the marketplace -- and I'm certainly not aware of that -- or press accounts that foreshadowed the release of the standard.

With this language in the Column 6 of the '386 or the '417 or the '215 indicates to me is that most likely Netlist was a member of JEDEC and that the inventors of this -- listed on this patent application were either participating in or were talking with Netlist representatives at the JEDEC meetings and, therefore, were aware of a forthcoming

standard that was not yet widely in the public domain.

Q. But how can you say it wasn't widely in the public domain when I'm looking at it in a patent application filed July 1st, 2005?

A. I said not widely in the public domain. Clearly, the inventors had heard the term, may have known more than just the name of it. We don't know.

We knew that there was something called FB-DIMM that was being worked on at some -- by someone either in a company somewhere or within JEDEC. We have no knowledge of exactly how that term came to be known by the inventors and put into the language of the specification as of the middle of 2005.

Q. So do you disagree with Exhibit 1012 when it says as of July 1st, 2005, that a person of ordinary skill in the art could implement rank multiplication in an FB-DIMM?

ATTORNEY WARRICK: Objection; form.

///

BY ATTORNEY CHANDLER:

Q. That's what -- that's what Exhibit 1012 is saying; right? Is "Memory module 10 compatible with embodiments described herein" includes DIMM, SO-DIMM and FB-DIMM.

And I'm trying to understand if you're sort of fighting what the inventors are telling us about whether a person of ordinary skill in the art reading this application could actually do what they're saying.

A. Well, your previous question --

ATTORNEY WARRICK: Objection to form.

THE WITNESS: Your previous question was all in the context of UDIMMs, which were, in fact, widely known by POSITAs in the 2004-2005 time frame.

To the extent that an FB-DIMM was not widely known within -- in July of 2005 and that in only -- and that a POSITA would have only had full access to the details of a -- what an FB-DIMM actually is until later means that the migration of the features of this specification into an FB-DIMM would have required two things: First of all, a knowledge

of this specification, and a knowledge of FB-DIMMs.

If the latter was not widely known until sometime after 2005, that is when a POSITA would have been able to undertake such a task.

BY ATTORNEY CHANDLER:

Q. There were a lot of "ifs" in your answer, and so it's a little unclear to me what your position is about whether or not a person of ordinary skill in the art as of July 1st, 2005, could have implemented rank multiplication in an FB-DIMM, as stated by Netlist patent marked as Exhibit 1012 in Column 6 line 8.

A. What my answer --

ATTORNEY WARRICK: Object to form.

THE WITNESS: What my answer tried to convey is that if a POSITA in July 2009 [sic] had full knowledge of what an FB-DIMM was going to be, then, yes, it would have been possible.

But if a POSITA was not aware of what the details of an FB-DIMM were or were going to be at that time, then one half of the

equation is not present.
BY ATTORNEY CHANDLER:
Q. Could a POSITA have joined JEDEC to get information about the FB-DIMM if they didn't have it already?
A. No.
ATTORNEY WARRICK: Objection to form.
THE WITNESS: As we discussed yesterday, the members of JEDEC are companies, and they are bound by nondisclosure agreements. So some random Joe can't walk in off the street and attend a meeting.
BY ATTORNEY CHANDLER:
Q. Not some random Joe: A person of ordinary skill in the art, which is, you know, the field of art that JEDEC is concerned about.
A. Well, with regard to the JEDEC meetings, a POSITA engineer that's relatively green is not necessarily someone that can come in, even as a representative of his parent company, the company that he or she works for.
But the -- it is the senior members of the engineering and marketing teams of the member companies that routinely

participate in the JEDEC meetings, because it's their expertise that helps direct the standard-setting process.

Q. So are you suggesting that the inventors at Netlist, when they disclosed on July 1st, 2005, FB-DIMM in Exhibit 1012, did that violate some JEDEC policy?

A. I'm not aware of the specifics of the JEDEC policy with regard to the naming terminology of future standards.

There's also the possibility that there is a product or a product plan of some company that was putting that terminology into the public domain with or without disclosing full details of it. We -- we have nothing to go on except for these four words in Column 6.

Q. Well, it's not entirely true. I mean, we have the level of ordinary skill in the art to go on; right?

A. Yes, but your questions premised around a modification of something. And if you don't know what you're modifying, you can't effect that.

So the specification of the '417, '215, et al., teaches the features that are

going to be added to something, in your hypothetical; but without -- this specification doesn't tell us about what the FB-DIMM is.

It ultimately comes into the public domain clearly when JEDEC standardizes it. And we don't have any information in front of us to help us understand when the details of FB-DIMMs do come into the public domain widely other than the 2007 release of the standard.

Q. You were not a member of JEDEC, but you told me that you went to some JEDEC meetings; right?

A. I think two, as the guest of a client of mine.

Q. Did you sign a nondisclosure agreement when you went to those JEDEC meetings?

A. I had nondisclosure agreements with my clients.

Q. But not with JEDEC?

A. Indirectly so, I guess. But they did not -- there were -- the agreements that I was aware of were between JEDEC and the companies, not specifically with the individual representatives of those companies. So I guess --

(Simultaneous cross-talk.)
Q. Hold on. There are no nondisclosure agreements in JEDEC.
A. I'm sorry?
Q. There are no nondisclosure agreements in JEDEC; right?
ATTORNEY WARRICK: Objection; form.
THE WITNESS: I -- as far as I'm aware -- and, again, I'm not a member of JEDEC and have only observed the process -- is that the proceedings of the meetings are not to be widely disseminated. Whether that's enforced by a nondisclosure agreement or by whatever mechanism the membership meeting agreement for the member companies, I'm not privy to that.
BY ATTORNEY CHANDLER:
Q. A person of ordinary skill in the art can form their own company and join JEDEC; right?
ATTORNEY WARRICK: Objection; form, also scope.
THE WITNESS: I don't know what the membership requirements are for joining JEDEC. I have no knowledge about that.

BY ATTORNEY CHANDLER:

Q. You told me a moment ago that you did know, that -- you said a person can't do it, a company has to do it.

A. Well, yes, I know that it's companies, but I don't know if there are any other requirements other than that, or whether, you know, a company that's not actively involved in the industry is -- is invited or is allowed to participate. I don't know. I have no knowledge of that.

Q. Isn't it true that basically every company that you've ever heard of is a member of JEDEC, in this field?

ATTORNEY WARRICK: Objection; form. Objection; scope.

THE WITNESS: No, that's not at all the case, that there are -- there are a large number of companies in this field, and not all of them are JEDEC members. I'm pretty sure of that. I don't know precisely which are and which are not, but the membership list of JEDEC is not in the thousands.

BY ATTORNEY CHANDLER:

Q. It's in the hundreds though;

right?

ATTORNEY WARRICK: Same objections.

THE WITNESS: I don't know that. I certainly don't know that with regard to the specific committees that are involved for these standards. I would be surprised if it was hundreds. The --

BY ATTORNEY CHANDLER:

Q. And you know that Rambus was a member of JEDEC; right?

A. For a while it was, yes.

Q. And Intel was a member of JEDEC?

A. I believe so. I don't know for sure, but I presume so.

Q. Are you aware of any company that was ever rejected from joining JEDEC?

ATTORNEY WARRICK: Objection; form. Objection; scope.

THE WITNESS: I have no knowledge about any of that.

BY ATTORNEY CHANDLER:

Q. To be clear, you are not offering an opinion today that FB-DIMMs were unknown to a person of ordinary skill in the art as of

July 1st, 2005; correct?

A. No, I'm not forming an opinion to that effect, no.

Q. And you're not offering an opinion today that FB-DIMMs were unknown to a person of ordinary skill of the art as of January 19, 2005; correct?

A. It's -- my opinions in this matter are related to the validity of these claims and the arguments put forward by the Petitioners and their expert; and I have rebutted those arguments that seek to invalidate the claims in question.

I do not offer any opinions outside of those four corners of the task in front of me.

Q. So if I understand correctly, you viewed your task as starting with the assumption that the claims were entitled to a priority of January 9th [sic], 2005; and then looking at the arguments presented by the petition and Dr. Wolfe, and responding to those arguments and offering the opinion of whether, in your view, the arguments by the Petitioner and the opinions by Dr. Wolfe were sufficient.

ATTORNEY WARRICK: Objection; form.

THE WITNESS: I would say it's the other way around.

I start the process with an open mind as far as the validity and the valid priority date of the application. I looked at the arguments put forward by -- in the petition. I found them lacking and, therefore, presumed that there is no reason provided in the position [sic] to amend the apparent priority date, per the front page of the patents.

BY ATTORNEY CHANDLER:

Q. There were some questions about the '417 and '215 patent and Rambus.

Do you recall those?

A. There were some questions not about Rambus the company but with regard to Rambus channels as -- in general.

Q. And by the time of the '417 and '215 patents, Rambus channels, in general, were known to a person of ordinary skill in the art; correct?

A. Yes. We came to that conclusion yesterday.

Q. And nothing in the '417 and '215 patents explicitly excludes Rambus channels from being within the scope of the embodiments of the '417 and '215 patents; correct?

ATTORNEY WARRICK: Objection; form.

THE WITNESS: Nothing specifically excludes them. But the fact that Rambus rims are not in the list of modular types enumerated is an indicator that at least for the inventors the Rambus channels were not front of mind as far as the implementation space of their invention, that their invention is applicable to.

So there's nothing -- there's nothing explicit, but there are indications.

BY ATTORNEY CHANDLER:

Q. But there are also indications going the other way, and the most notable being that the inventors are very clear that the list of memory modules they say "includes but are not limited to"; right?

A. Yes, and so --

ATTORNEY WARRICK: Objection; form.

THE WITNESS: So it's not explicit.

But the fact that they -- out of, you know, 32 pages of specification, they didn't add an additional word about a module type that they were aware of but didn't include with the other module types, that's kind of a strong indication -- although not definitive, I will grant you that -- it's a strong indication as to what the inventors understood to be the applicability of their inventions.

BY ATTORNEY CHANDLER:

Q. And it may also be a strong indication, by the 2004-2005 time frame, that the vast majority of the industry was using JEDEC-style memory devices and JEDEC-style buses; correct?

ATTORNEY WARRICK: Objection to form.

THE WITNESS: They did include FB-DIMM, which was not commercially available yet. So the volume is not an idea that clearly played a role in determining what they put in that list and what they didn't.

(Simultaneous cross-talk.)

(Interruption by the court reporter to clarify the record.)

BY ATTORNEY CHANDLER:

Q. FB-DIMM was JEDEC; correct?

A. But there are other DIMM types in this list that, as far as I know, are not JEDEC.

Q. Could you pull up Exhibit 2031, and let me know when you have it.

A. I have in front of me Exhibit 2031, which is a portion of Release 13 of JEDEC Standard 21-C starting at page 4.1.2.10-1.

Q. And counsel for Netlist asked you some questions about page 8 of Exhibit 2031. So if you could go there, let me know when you have it.

A. I am looking at page 8.

Q. So on page 8 of Exhibit 2031 there's a table, and some of the rows of the table have dashes or hyphens; correct?

A. Yes. We discussed that.

Q. And when I look at the table and I see a row for 0 and then a dash in the next row, and then a row following that for 32, I read that to mean that any value between 0 and

32 is permissible.

But if I understood your testimony, you're trying to say that all the values between 0 and 32 are impermissible. Is that correct?

(Witness reviews document.)

A. It is my presumption going into this document, consistent with the other JEDEC documents, that dashes are impermissible values, and there's no language that I see elsewhere within the document that would define it otherwise.

So that there are permissible values, and there are other -- some of which are currently used, somewhere are effectively for future expansion; and then there are other values that are impermissible and that are not anticipated to be presently used or ever used in the future.

Q. So you've interpreted the dash in Exhibit 2031 as indicating values that are impermissible; correct?

A. Yes. In other words, a memory controller reading a particular value out of the SPD encountering a value that is -- that would

normally fall into one of the dashed rows would not be required to be able to interpret that value.

It's a -- this standard is a listing of what the memory module vendors are allowed to put into the SPD and what the memory controllers are required to be able to interpret as either valid or invalid or -- and correspondingly the dashed lines are outside of that agreement that this standard represents between module makers and systems companies buying them.

Q. You sure about that?

A. As I said, there's no --I'm not finding any language to dissuade me of that general impression of that's how JEDEC standards are formulated.

Q. Please turn to page 13 of Exhibit 2031.

You agree that the DRAM memory devices can be x4, x8, x16 or x32; correct? Which is to say a width of 4 bits, 8 bits, 16 bits or 32 bits.

A. Most of them are, yeah. I think there have been some -- there may have been some

in history that are -- have additional bits. Certainly the Rambus-style devices were also in x9 and x18, but I don't know whether there were standardized or nonstandardized SDRAMs that had other widths than that.

Q. The table on page 13 of Exhibit 2031 has a dash between 15 and 254; it does not have any row for an SDRAM that's 16 bits wide, 18 bits wide, 32 bits wide or 36 bits wide, even though the text on page 13 of Exhibit 2031 makes clear those are all permissible widths; correct?

(Witness reviews document.)

A. There's something odd about this table, and I don't understand why it's constructed the way it is and why there are not values for x60 and x30 enumerated in the lower portion of the table. I would have expected that to occur. Maybe this was revised in a subsequent release. I don't know.

Q. Or maybe dashes don't indicate an impermissible value.

A. That's plausible at this point, but, again, I don't know. We'd have to be sure and look at other SPDs documents.

I do know that in other JEDEC documents, dashes are generally listed -- values that are not within the agreed-upon set of values that are permitted from either the vendor side or the consumer side. So I do not understand why this table appears to be different.

But regardless of what it is -- whether it's different or if, as you suggest, my understanding of the table on Figure 8 is inadequate, it still doesn't affect any of my opinions in this matter.

Q. Including your opinion that Ellsberry discloses an 8-bit-wide memory module; correct?

A. I believe my testimony with regard to Ellsberry is that it's -- the previous figures in Ellsberry show a full 64-bit module with a plurality of slices that were narrower; and that by the time we got to Figure 10, it shows a control unit ASIC, a switch ASIC and 8 bits of data to a POSITA that would be what's shown as a complete module x8, but it doesn't make much sense commercially or technically; and instead the Figure 6 of Ellsberry is more

indicative of what a full module would look like.

So my testimony previously, as I recall it, was that it could be interpreted either way by a POSITA.

Q. Including an 8-bit-wide memory module.

ATTORNEY WARRICK: Objection; form.

THE WITNESS: Again, Figure 10, if viewed by a POSITA as a complete module, would be an 8-bit module. But there are -- by the time we get to 2004-2005, there are no commercially viable 8-bit modules in the marketplace that use JEDEC standard SDRAMs. All of the standardized and high-volume modules of that time frame are x32 or majority are x64.

BY ATTORNEY CHANDLER:

Q. If I understand your testimony in response to questions from counsel for Netlist, a person of ordinary skill in the art does not forget the earlier prior art; right? They still have in their knowledge prior art that's more than a few years old; correct?

A. The -- my testimony with counsel

for Netlist was that if there's a piece of prior art that is relevant to an argument that happens to predate the experience of a POSITA, we don't discount that prior art and discard it because it's too old. We still consider it valid prior art.

ATTORNEY CHANDLER: Thank you, Dr. Przybylski. No further questions. That concludes the deposition of today and yesterday. Thank you.

THE COURT REPORTER: You gentlemen both want your rough drafts again today?

ATTORNEY CHANDLER: Yes, please. And just as a reminder, a final draft by Thursday, February 22nd, please.

THE WITNESS: Gail, do you need any clarification of unintelligible?

THE COURT REPORTER: I don't believe so, but hang on.

Mr. Warrick, you want the rough draft today?

ATTORNEY WARRICK: Yes, please.

THE COURT REPORTER: And do you need regular delivery of the final?

Samsung Ex. 1095, p. 505
Samsung Electronics Co., Ltd. v. Netlist, Inc., IPR2023-00455

ATTORNEY WARRICK: That's fine.

THE COURT REPORTER: Okay.

THE VIDEOGRAPHER: And Counsel, I apologize but I have to ask again: Does anyone need a copy of the video?

ATTORNEY CHANDLER: My answer will be the same unclear answer, which is: Eventually yes, but not right now.

THE VIDEOGRAPHER: Perfect. That's fine.

Mr. Warrick, sir?

ATTORNEY WARRICK: Not at this time.

THE VIDEOGRAPHER: Thank you very much.

This concludes today's deposition of Steven Przybylski, Volume 2. We're off the video record at 3:29 p.m. Pacific Time on February 16th.

(Whereupon, at 3:29 p.m. the proceedings concluded.)

Samsung Ex. 1095, p. 506
Samsung Electronics Co., Ltd. v. Netlist, Inc., IPR2023-00455

INSTRUCTIONS TO DEPONENT

After reading this volume of your deposition, indicate any corrections or changes to your testimony and the reasons therefor on the Errata Sheet supplied to you and sign it. DO NOT make marks or notations on the transcript volume itself.

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C E R T I F I C A T I O N

I hereby certify that I have read the foregoing transcript of my deposition testimony, and that my answers to the questions propounded, with the attached corrections or changes, if any, are true and correct.

STEVEN PRZYBYLSKI, PH.D.,

CERTIFICATE OF SHORTHAND REPORTER

I, Gail Inghram Verbano, Registered Diplomate Reporter, Certified Realtime Reporter, Certified Shorthand Reporter (CA) and Notary Public, the officer before whom the foregoing proceedings were taken, do hereby certify that the foregoing transcript is a true and correct record of the proceedings; that said proceedings were taken by me stenographically and thereafter reduced to typewriting under my supervision; and that I am neither counsel for, related to, nor employed by any of the parties to this case and have no interest, financial or otherwise, in its outcome.

Gail Inghram Verbano, CSR, RDR, CRR
CA-CSR No. 8635