UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.,

Petitioner,

v.

NETLIST, INC.,

Patent Owner,

_____

Case No. IPR2022-00615

Patent No. 7,619,912

_____

REMOTE VIDEOTAPED DEPOSITION BY VIRTUAL ZOOM OF

ANDREW WOLFE, PH.D.

WEDNESDAY, JANUARY 4, 2023

Reported by:

Ashala Tylor, CSR #2436, CLR, CRR, RPR

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Videotaped deposition of ANDREW WOLFE, PH.D., taken via virtual Zoom, commencing at 9:04 a.m. and ending at 6:38 p.m., on Wednesday, January 4, 2023, before Ashala Tylor, CSR No. 2436, RPR, CRR, CLR.

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A P P E A R A N C E S (continued)

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Wednesday, January 4, 2023

9:04 a.m.

--o0o--

ANDREW WOLFE, PH.D.

being first duly sworn or affirmed to testify to the truth, the whole truth, and nothing but the truth, was examined and testified as follows:

EXAMINATION

BY MS. ZHONG: 09:04

Q. Dr. Wolfe, can you pull up Exhibit 1032, 09:04

Exhibit 1029, Exhibit 1030. You have them on your 09:05

local computer and -- 09:05

THE REPORTER: I'm sorry, Ms. Zhong, I'm 09:05

having a difficult time hearing you. 09:05

BY MS. ZHONG: 09:05

Q. Okay. Dr. Wolfe, can you pull up 09:05

Exhibits 1032, 1030 and 1029. 09:05

(Exhibit 1029 was marked for 09:05

identification and attached 09:05

hereto.) 09:05

(Exhibit 1030 was marked for 09:05

identification and attached 09:05

hereto.) 09:05

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(Exhibit 1032 was marked for identification and attached hereto.)

THE WITNESS: All three of them you want me to pull up?

BY MS. ZHONG:

Q. Yes. You have them on your local computer, correct?

A. I do.

Q. Okay. Let me know when you have them.

A. I have them.

Q. What is Exhibit 1032?

A. It is the PC2100 and PC1600, DDR SDRAM Registered DIMM, D-I-M-M, Design Specification, Revision 1.3 from January 2002. And we often refer to it as a version of JEDEC Standard 21-C.

Q. How does JEDEC Standard 21-C differ from Exhibit 1030?

A. They are different documents describing different things.

Q. What does Exhibit 1030 describe?

A. That is the JESD79 standard or specification from June 2000. And it describes various aspects of double-data-rate DRAM chips primarily.

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Q. Okay. So Exhibit 1030 is directed to the SDRAM's memory device itself, correct? 09:07

A. Primarily, yes. 09:07

Q. Okay. And Exhibit 1032 describes the memory module level, correct? 09:07

A. For one particular type of memory module, that is correct. 09:07

Q. Okay. So Exhibit 1032 describes in particular the registered DIMM memory module, correct? 09:07

A. A particular type or a particular set of types of registered DIMM memory modules. There's other information in there as well, but that's its primary purpose. 09:07

Q. Okay. And the operation of DDR SDRAM device itself you refer to Exhibit 1030; is that right? 09:08

A. Exhibit 1030 includes a multitude of specific characteristic specifications for a packaged double-data-rate SDRAM chip at that time. 09:08

Q. Okay. Why don't we go to Exhibit 1032, page 16. 09:08

A. Okay. 09:08

Q. On page 16, lower left corner, do you see a bunch of signals that's going into an element 09:08

called a register? Do you see that diagram there? 09:08

A. I do see that diagram. 09:08

Q. Okay. And what is a register shown on 09:09

page 16 of Exhibit 1032? 09:09

A. Well, what a register is always depends on 09:09

context. But in this particular context, that would 09:09

be a component on this module that can temporarily 09:09

store signal values. 09:09

So it would store the input values based 09:09

on certain values of the PCK, which stands for 09:09

clock, and PCK bar signals, and make those available 09:09

at the outputs on the right. 09:09

Q. Okay. So the signals on the left of the 09:09

register are input signals that -- (indiscernible.) 09:09

THE REPORTER: I'm sorry, Counsel. I'm 09:10

having a difficult time hearing you. One more time, 09:10

please. 09:10

BY MS. ZHONG: 09:10

Q. So the signals to the left of the element 09:10

of register are input signals received by the DIMM 09:10

from the computer system; is that correct? 09:10

A. In this diagram, the signals that are on 09:10

the left of the box marked "Register" would come 09:10

from -- they are input signals to the DIMM, and in 09:10

most cases they would come from a computer system. 09:10

Q. Okay. And the signals that's to the right of the box labeled "Register," those are output signals; is that correct? 09:10

A. From the perspective of this particular register they are output signals. They would be input signals to some other device. 09:10 09:11 09:11

Q. Okay. And so the signals to the right of the register are output signals from the perspective of the register and -- but they are input signals to the SDRAM devices; is that correct? 09:11 09:11 09:11 09:11

A. They -- each of those would be an input signal to one or more SDRAM devices. 09:11 09:11

Q. So the answer to my question is "yes"; is that correct? 09:11 09:11

A. I don't know whether or not we're saying the same thing. 09:11 09:11

The register will output each of the signals shown to the right of the register. Those are then provided -- but some are provided to some SDRAM devices. Some are provided to others. Some are provided to all of them. 09:11 09:11 09:11 09:11 09:11

Q. Okay. And there are different types of DIMMs; is that correct? 09:11

A. In the world, that is true, there are different type of DIMMs in the world. 09:12 09:12

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Q. Okay. Are you familiar with a type of DIMM called RIMM, which I believe is specific to the Rambus-designed memory modules? 09:12

A. I don't recall it by that name, but there were a number of Rambus memory modules in the 2000-2005 time frame typically. 09:12

Q. Okay. Do you recall what kind of input signals do those RIMMs receive? 09:12

A. Not in detail. The RIMM -- the Rambus DRAM memory modules used a packetized communication scheme that used a narrower communication channel than the most common other DIMMs at the time. 09:13

Q. Okay. So, for example, the Rambus memory module -- let me rephrase that. 09:13

So the Rambus DRAM memory module do not receive, for example, chip select signal, band address signal, RAS bar, CAS bar, WE bar, and address this as shown on page 16 of Exhibit 1032; is that correct? 09:14

MR. CHANDLER: Objection. Form. 09:14

THE WITNESS: Again, I would need to look at that specification to recall all the details. It's been 20-plus years since I've read it. But my recollection is that the same information was conveyed but not in the exact same physical form. 09:14

BY MS. ZHONG: 09:14

Q. Okay. Let me see -- let me introduce a document and see if this will jog your memory. 09:14

(Exhibit 2100 was marked for identification and attached hereto.) 09:15

BY MS. ZHONG: 09:15

Q. So, Dr. Wolfe, can you please refresh your Exhibit Share link? 09:15

A. Yes. 09:15

Q. And do you see a newly marked Exhibit 2001 -- 2100, EX2100? 09:15

A. EX2100. 09:15

Q. Yes. Can you please open it or download it. 09:15

A. Okay. 09:15

Q. Exhibit 21 -- okay. Do you have it? 09:15

A. I do. 09:15

Q. So Exhibit 2100 is a Samsung data sheet for RIMM, R-I-M-M, module based on 256 megabits or 288 megabits, 32 bank, 16K/32ms Rambus DRAMs. 09:15

Can you go to pages 2, 3, 4, and take a look. 09:16

MR. CHANDLER: And, Annita, let me just lodge an objection to the exhibit. It's -- appears 09:16

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to be outside the scope of his declaration. Also doesn't appear to be -- it doesn't appear to be evidence that I can -- appears to be hearsay. 09:16

BY MS. ZHONG: 09:16

Q. Dr. Wolfe, can you please take a look at pages 2 through 4. 09:16

A. I see them. 09:16

Q. Okay. The signals listed on pages 2 through 4, the input signals to the DIMM, for this particular DIMM. 09:16

A. I'm sorry, I didn't understand the question. 09:17

Q. So on page 2 through 4 there are a number of pins listed on those pages, correct? 09:17

A. They are called pads in this case. But there are a number of connections to a module that are described on these pages. 09:17

Q. Okay. So the pads that's listed on those pages are the -- how do you say? -- the input and output pads for the -- for the memory module; is that correct? 09:17

A. Some of them probably are. To get into the details, I think, requires reviewing other documents. 09:17

Q. Okay. Can you tell me which pin would be 09:17

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check select signal coming in from? 09:18
A. Not from a cursory review of this document 09:18
I can't, no. There are other documents, the ones 09:18
intended to review together with this, that describe 09:18
how these signals are used in more detail. 09:18
Q. Okay. Do you see any reference to chip 09:18
select signal here in this document? 09:18
A. There may or may not be. Again, I 09:18
don't -- I don't know the definition of the 09:18
functionality of every pin from this document alone. 09:18
There are other documents that were 09:18
supplied at the time by Rambus that would describe 09:18
how each pin was used. And for this particular kind 09:18
of a DIMM, my recollection was that the DIMMs -- 09:18
that pins or pads had multiple functions. 09:18
Q. Okay. Are the signals -- you mentioned 09:19
that for Rambus memory module the address and the 09:19
control signals are packetized; is that correct? 09:19
THE REPORTER: I'm sorry, are what? I'm 09:19
sorry, Counsel, the last part of your question? 09:19
BY MS. ZHONG: 09:19
Q. You mentioned that the Rambus memory 09:19
module -- let me withdraw and reask. 09:19
So in the Rambus memory module, the 09:19
control and address information is packetized; is 09:19

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that correct? 09:19

MR. CHANDLER: Objection. Form. 09:19

THE WITNESS: That was my recollection as 09:19
to certain Rambus memory modules that I was familiar 09:19
with in the early 2000s. I don't know, from what 09:19
I've seen here right now, whether or not this 09:20
particular module is consistent with the ones that I 09:20
previously studied. 09:20

BY MS. ZHONG: 09:20

Q. And how does a packetized control and 09:20
address information differ from the signaling 09:20
protocol that we see on page 16 of Exhibit 1032? 09:20

A. There are similarities and there are 09:20
differences, and it would depend on the specifics of 09:20
the specific situation. 09:20

But I think that the biggest difference is 09:20
that in the Rambus protocols that I was familiar 09:20
with at the time, there was -- there were more pins 09:20
that had multiple functions. 09:20

Q. So is there a discrete chip select signal 09:21
as in Exhibit 1032? 09:21

A. Does what have a discrete chip select 09:21
signal? 09:21

Q. Let me put it this way. When the control 09:21
and address information is set by the computer 09:21

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system -- let me reask. 09:21

What do you mean by the control and 09:21

address information is packetized? 09:21

A. I'm not sure what you're referring to. 09:21

Q. Well, you said in the Rambus memory module 09:21

the control and address information is packetized, 09:21

correct? 09:22

A. I don't recall if that's exactly what I 09:22

said. But in the Rambus memory modules that I was 09:22

familiar with at one point in time, which again are 09:22

only a subset of the Rambus products, the control 09:22

and address -- as best as I can recall, I don't have 09:22

that protocol in front of me -- the control and 09:22

address data would be broken up into chunks, I 09:22

believe, 8 bits at a time, and sent as a sequence 09:22

over a limited number of wires and then 09:22

reconstituted on the module itself into individual 09:22

signals. 09:22

Q. Okay. So in the Rambus memory module that 09:22

you are familiar with from the early 2000s, the 09:22

control and address information is set in bits and 09:22

reconstituted by a larger component on the memory 09:23

module; is that correct? 09:23

MR. CHANDLER: Object to form. 09:23

THE WITNESS: Now, first understanding 09:23

clearly that this is -- that the module in Exhibit 2100 is not one that I'm familiar with. 09:23

But my recollection is that, as I stated before, that in the Rambus protocol for the devices that I was familiar with, control and address information would be sent along a relatively narrow channel as a sequence of packets and then reconstituted into individual signals by the logic functions on the -- within the Rambus chips. 09:23

BY MS. ZHONG: 09:24

Q. Okay. 09:24

A. But again, I haven't seen those documents in a long time, so I really can't tell you any of the details about it without reviewing them again. 09:24

Q. When you say "reconstituted into individual signals by the logic function within the Rambus chips," what do you mean by "reconstituted"? 09:24

A. Again, it's been a long time since I reviewed this protocol. But my best recollection is that the individual selection signals to select columns, rows, banks, and die would be reconstituted within some logic somewhere on the memory module. 09:25

Q. So the form in which the logic function receives the information from the memory system -- let me withdraw it and reask. 09:25

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So the input -- inputs that the logic function receives from the computer system differs from the output of that logic function; is that correct?

MR. CHANDLER: Object to form.

THE WITNESS: I don't understand your question.

BY MS. ZHONG:

Q. Which part don't you understand?

A. I don't understand what the question is.

Q. So the logic function on the Rambus DIMMs that you are familiar with receives packetized control and address information; is that correct?

A. In a very general sense. Again, I haven't -- I haven't reviewed that protocol in decades.

Q. Okay. And that logic function then reconstitute those that receive the packetized information and generates signals for output to the DRAMs; is that correct?

MR. CHANDLER: Objection. Form.

THE WITNESS: Yeah, it depends how you're defining some of those terms. I'm not sure what -- what -- I mean I answered the question using language I was comfortable with, but I don't know

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how -- what -- how you're defining some of the words in your question. 09:26 09:26

BY MS. ZHONG: 09:27

Q. Which words don't you understand? 09:27

A. Can you go through your question again? In particular, I don't understand what you mean when you say the signals go to the DRAM. 09:27 09:27 09:27

Q. And the logic function on the Rambus memory module you're familiar with then reconstitutes the control and address information that it receives and it generates output signals; is that correct? 09:27 09:27 09:27 09:27 09:27

A. It depends what you mean by output signals. But in the very broadest sense where there is at least some logic gate that outputs that signal, that would be true based on my recollection without reviewing the protocol. 09:27 09:27 09:27 09:27 09:27

Q. Okay. And the signals that are output by the logic function, where do they go? 09:27 09:27

A. I don't remember. Again, I haven't seen this design in decades. I'd have to see the actual design to give you any more details. 09:28 09:28 09:28

Q. Do they go to the memory devices on the module? 09:28 09:28

A. Like I said, I don't -- I don't recall. 09:28

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Q. And is the -- and is the information that's output by the logic function still packetized? 09:28

MR. CHANDLER: Objection. Form. 09:28

THE WITNESS: Where and when? 09:28

BY MS. ZHONG: 09:28

Q. Pardon? 09:28

A. Where and when? 09:28

Q. You mention that the logic function would take the packetized control and address information it receives and reconstitute to generate the output signal. So is that output signal still packetized? 09:29

MR. CHANDLER: Objection. Form. 09:29

THE WITNESS: Again, you know, at some point the details become important and we have to look at an actual circuit and look at an exact spot in the circuit. 09:29

But eventually those -- that information about control and addresses is not in the same packetized form that it is transmitted over the Rambus channel. But -- but, you know, it still -- it's sequential. But at some point we would probably not describe it as packetized anymore. 09:29

BY MS. ZHONG: 09:29

Q. Okay. So when the information is sent to 09:29

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the DRAM, is it still packetized? 09:30
MR. CHANDLER: Objection. Form. 09:30
THE WITNESS: We need to look at an actual 09:30
circuit. I'm not sure what -- we'd have to identify 09:30
exactly where we're talking about and draw 09:30
boundaries around what you're calling the DRAM and 09:30
what you're not. 09:30
And again, I don't -- I don't recall the 09:30
exact signal paths on those chips from 20 years ago. 09:30
BY MS. ZHONG: 09:30
Q. Okay. What about in Perego, what kind of 09:30
address control information format does Perego stem 09:30
receive? 09:30
Let me withdraw and ask -- reask. 09:30
So the Perego, P-R-E-G-O [sic], what kind 09:30
of address control information -- 09:31
MR. CHANDLER: Just to be clear, Annita, 09:31
P-E-R-E-G-O. The transcript picked it up the wrong 09:31
way, so I think the primary reference was 09:31
misspelled. 09:31
BY MS. ZHONG: 09:31
Q. Okay. Then let me just withdraw and 09:31
reask. 09:31
So for Perego, which I believe is 09:31
Exhibit 1034 -- 09:31

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A. 1035. 09:31
(Exhibit 1035 was marked for 09:31
identification and attached 09:31
hereto.) 09:31
BY MS. ZHONG: 09:31
Q. 1035. So Exhibit 1035, Perego, 09:31
P-E-R-E-G-O, in what format is the control address 09:31
information received from the computer system by 09:31
Perego's memory module? 09:31
A. I'm not sure what you mean by format. 09:31
Perego contemplates a wide variety of different 09:31
memory technologies, including various kinds of 09:32
memory, including synchronous DRAMs, DDR DRAMs, 09:32
direct Rambus memory devices, XDR memory devices, 09:32
SRAM, which stands for static RAM, ferroelectric 09:32
RAM, magnetoresistive RAM, flash memory or ROM. 09:32
And while there are certain 09:32
characteristics of the DIMM that are described in 09:32
various embodiments, I don't think that there's a 09:32
particular format that's required for all those 09:32
different memory types. 09:32
Q. Does Perego ever describe that its DIMM 09:32
received the type of information as shown in 09:32
Exhibit 1032, page 16? 09:33
A. As I said, Perego contemplates a variety 09:33

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of different input specifications. In fact, that's one of the whole points of Perego is that it contemplates a wide variety of different DIMM connection widths. 09:33

Q. But the DIMM -- 09:33

A. It does describe conventional DIMM modules. I don't recall off the top of my head whether or not he specifically refers to the module that is described in JEDEC Standard 21-C. That was disclosed in the IDS for Perego. 09:33 09:34

And certainly a person of ordinary skill in the art at the time would have been familiar with JEDEC Standard 21-C. And I think that it is consistent with and compatible with Perego, but I don't recall a specific disclosure of using that exact standard together with Perego. 09:34 09:34 09:34 09:34

Q. And Perego actually does not want to use the control and address bus architecture? It moves for the point-to-point connection architecture; is that correct? 09:34 09:34 09:35 09:35

A. Are you pointing -- are you talking about a specific statement in Perego? I -- I -- that doesn't ring a bell at the moment. 09:35 09:35

Q. What kind of architecture does Perego use? 09:35

A. What do you mean by architecture? 09:35

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Perego describes architecture as including a configurable width buffered module having a configurable width buffer device. 09:35

Q. And it's using a point-to-point connection instead of a multidrop bus connection; is that correct? 09:35

MR. CHANDLER: Objection. Form. 09:35

BY MS. ZHONG: 09:36

Q. Dr. Wolfe, can you answer the question? 09:36

A. I'm looking. I mean, certainly at least the bulk of the embodiments in Perego connect to the computer with a point-to-point connection. I don't recall whether or not there's any indication limiting Perego to a point-to-point connection. 09:36

And certainly JEDEC Standard 21-C can be compatible with a point-to-point connection such as Perego. 09:36

Q. Perego actually specifically only mentions packetized signaling, correct? 09:37

A. I'd have to go back through the entire reference to confirm that. That's certainly -- 09:37

Q. Why don't you look at -- 09:37

A. -- not true because -- 09:37

THE REPORTER: I'm sorry, one at a time, please. 09:37

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BY MS. ZHONG: 09:37

Q. Can you please a look at Exhibit 1035, column 9, line -- 09:37

MR. CHANDLER: I don't think he was finished. 09:37

THE WITNESS: I didn't finish my previous answer. I disagree with your previous answer -- with your previous question. 09:37

So column 9, 53? 09:37

BY MS. ZHONG: 09:37

Q. Column 9, lines 50 to 53. 09:37

A. Yes. 09:38

Q. What kind of a format is the control information/address information provided in this disclosure? 09:38

A. Well, this is a disclosure in accordance with an embodiment. And in this particular embodiment, information -- control information and addresses are contained in packets. 09:38

Q. Okay. And can you also take a look at column 13, lines 49 to 59. 09:38

In what format is the control and address information provided in this disclosure? 09:38

A. This is -- well, let me make a number of comments about this. One, this is, again, an 09:39

embodiment. Also, it's filled with permissive language. But this says any multiplexed combination of control, address information, and data intended for memory devices. 09:39

And, of course, the traditional DIMMs like JEDEC Standard 21-C do use multiplexed combinations of control, address and data. 09:39

Q. And in the -- in the traditional DIMM, is the multiplex control and address information demuxed from the data? 09:39

THE REPORTER: I'm sorry, Counsel. The last part of your question? 09:40

MS. ZHONG: Demux, D-E-M-U-X. 09:40

THE WITNESS: No, not in a traditional DIMM that would be compliant with JEDEC Standard 21-C. It would not have that characteristic. 09:40

BY MS. ZHONG: 09:40

Q. Okay. So this is not really describing a standard JEDEC compliant DIMM control and address signaling protocol, correct? 09:40

MR. CHANDLER: Objection. Form. 09:40

THE WITNESS: No, I think that's incorrect. As I said, this is an embodiment. It's permissive. And the language that you asked about in your question is only in a "for example." So I 09:40

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think that it -- 09:41
BY MS. ZHONG: 09:41
Q. Well, okay -- 09:41
A. I'm sorry, you can't keep interrupting my 09:41
answers. 09:41
Q. You are not answering my question. So 09:41
let's try it again. 09:41
So in the specific example -- 09:41
A. I'm sorry, I didn't finish answering the 09:41
last question. If you're not going to let me answer 09:41
them, could you please strike the questions? 09:41
Q. So in the specific example given here, we 09:41
agree that a standard JEDEC compliant DIMM does not 09:41
perform the step of extracting address and control 09:41
information from the data; is that correct? 09:41
MR. CHANDLER: Objection. Form. 09:41
THE WITNESS: When you say "here," exactly 09:41
what line are you talking about? 09:41
BY MS. ZHONG: 09:41
Q. For example, column 13, lines 49 through 09:42
54. Do you see the discussion of extracting address 09:42
and control information from the data? Do you see 09:42
that disclosure? 09:42
A. On lines 53 and 54 I see -- 09:42
Q. Okay. 09:42

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A. -- a permissive statement that says "which may, for example, extract the address and control information from the data." 09:42

Q. Okay. And does the standard JEDEC compliant memory module extract address and control information from the data? 09:42

MR. CHANDLER: Objection. Form. 09:42

THE WITNESS: There are many JEDEC standards. 09:42

BY MS. ZHONG: 09:42

Q. Are you aware of any that actually does this? 09:42

A. I don't recall one way or another. 09:43

Q. Are you aware of any JEDEC compliant memory module when the signaling scheme that you relied on in your declaration that actually does the extraction of address and control information from the data? 09:43

MR. CHANDLER: Objection. Form. 09:43

THE WITNESS: I don't recall any JEDEC standard that I relied on as an exhibit for my declaration that extracts the address and control information from the data. 09:43

BY MS. ZHONG: 09:43

Q. Okay. And do you recall of any JEDEC 09:43

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standards you relied on in which control information and address information is decoded and separated from multiplex data? 09:44

MR. CHANDLER: Objection. Form. 09:44

THE WITNESS: I don't recall that being in any of the JEDEC specifications that I relied on as exhibits to my declaration. 09:44

BY MS. ZHONG: 09:44

Q. Do you recall that being the case in any of the exhibits that you relied on? 09:44

A. Well, sure. It's in Perego. 09:44

Q. Okay. So aside from Perego, do you recall whether any of the memory modules in any references other than Perego that actually does control information, address information, decoding and separation from multiplex data? 09:44

A. I don't recall one way or the other. 09:45

THE REPORTER: Ms. Zhong, could you sit up so I can see you? It would make it easier to hear you. Thank you. 09:45

MS. ZHONG: It may be difficult because that's taking away from -- that's kind of forcing me to face away from the phone. 09:45

Q. Can you turn to column 21, line 46 to 50? 09:46

A. Of Perego? 09:46

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Q. Yes. 09:46
A. Okay. 09:46
Q. Okay. So in the specific example here, 09:46
again it is discussing this decoding packetized 09:46
transmission from controller; is that correct? 09:46
A. Column 21, lines 46 through 50, does talk 09:46
about an embodiment where repeaters decode packets 09:46
transmitted from the controller which are then 09:46
directed over one or more, or none of repeater 09:46
links. 09:47
Q. Okay. So do any of the JEDEC 09:47
specifications you relied on utilize packetized 09:47
transmission from controllers? 09:47
A. Yes. If you -- if you use that term 09:47
broadly, yes. 09:47
Q. When you say "use that term broadly," what 09:47
do you mean? 09:47
A. There are packets that are transmitted 09:47
from controllers to memory modules in DDR SDRAM 09:47
designs. 09:47
Q. It's transmitted to DDR SDRAM. What about 09:47
to the module? Is it also packetized? 09:47
A. There are portions of the information that 09:47
are packetized. 09:47
Q. Can you please give me an example with 09:47

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reference to Exhibit 1032 which portion is packetized. 09:47

A. Well, the protocol is not described in Exhibit 1032. 1032 is about the physical structure of the module. So you need to read that together with other documents to understand the protocol. 09:47 09:48 09:48 09:48

Q. So which documents indicate there is packetized control and address information being sent from the -- from the controller? 09:48 09:48 09:48

A. Well, that's a different question than you asked before. 09:48 09:48

Q. Okay. So when you say there's packetized transmission, what kind of information was packetized? 09:48 09:48 09:48

A. The one I'm familiar with off the top of my head is -- are data bursts. 09:48 09:48

Q. What about control and address information? So in the JEDEC standards you relied on, is any of the control and address information packetized and transmitted from the controller to the DIMMs? 09:48 09:48 09:48 09:48 09:48 09:48

A. I don't recall. It wasn't important to my analysis, so I haven't looked. 09:49 09:49

Q. Sitting here today, are you aware of any JEDEC standards at the time of the invention that 09:49 09:49

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actually used packetized transmission of control and address information? 09:49

A. I don't recall one way or another. There are lots of JEDEC standards at the time that I was familiar with, and there are lots of pages in them, and that's a very narrow issue that was not relevant to my analysis in. 09:49

Q. And you cannot point to any of the exhibits you relied on that actually discusses packetized transmission of a control and address information for a JEDEC compliant memory module; is that correct? 09:49

A. I can't point to one right now off the top of my head, no. 09:50

Q. And for a packetized control and address information that's being sent from the controller, logic on the memory module will need to decode them and reconstitute those signals; is that correct? 09:50

A. Not necessarily, no. 09:50

Q. Why not? 09:50

A. It may not be necessary to decode those signals. 09:50

Q. So if on the -- so if on the memory module the memory module uses JEDEC compliant SDRAMs, do those information need to be decoded and 09:50

depacketized? 09:51
A. It would depend which DRAM and how the 09:51
information was encoded in the first place. 09:51
Q. The DDR2, DDR SDRAM specification you 09:51
relied on, those DRAMs. Do they receive packetized 09:51
input? 09:51
A. They can receive packetized data inputs. 09:51
Q. Can they receive packetized control and 09:51
address inputs? 09:51
A. I haven't looked to see whether or not 09:51
they sometimes do or not. 09:51
Q. Well, you are the expert here. You cited 09:51
those documents, specification. 09:51
What kind of a control and address 09:51
information do those JEDEC compliant DDR and DDR2 09:51
memory devices receive? 09:51
A. There's not a single name for it. That's 09:51
why we use a 80-page document to describe the 09:52
protocol. There's a complex protocol for those 09:52
signals and it is described in documents. 09:52
So, for example, Exhibit 1029 describes 09:52
the address and control protocols for DDR2 DRAM 09:52
devices at the time. 09:52
Q. So point me to somewhere in Exhibit 1029 09:52
where the control and address information for the 09:52

SDRAM is received as a packet. 09:52

A. I haven't done that analysis. 09:52

Q. Well, you're familiar with the document, 09:52

right? 09:52

A. I am. 09:52

Q. And you know what a POSITA would have 09:52

known in 2004 and 2005, correct? 09:53

A. With respect to the '912 patent, yes. 09:53

Q. And also with respect to what they would 09:53

have known regarding the JEDEC standards, correct? 09:53

A. Yes. 09:53

Q. Okay. So from a POSITA's perspective, 09:53

would they have known that the SDRAMs that's 09:53

compliant with JEDEC would receive packetized 09:53

control and address information? 09:53

A. It depends how you define "packetized." 09:53

There are packetized aspects to it. 09:53

Q. What's your definition of packetized? 09:53

A. It depends on context. And there was just 09:53

no need to have a definition with respect to the 09:53

JEDEC standards. The actual information is 09:53

disclosed in the documents. So there was no need 09:53

for me to characterize it as packetized or 09:53

nonpacketized. 09:54

Certainly there are packets and 09:54

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information that are sent. So, for example, the activate command is sent separately from the read command. And one could consider those to be packets in certain contexts. 09:54

Q. In what context would they be considered to be packetized? 09:54

A. If you define packets as bundles of information that are sent at different times on the same wire, which would be a pretty common general definition of that term. 09:54

Q. Why don't you go to your declaration, page 93, Table 10. 09:54

A. Okay. 09:54

THE REPORTER: Counsel, what exhibit number is that? 09:55

BY MS. ZHONG:

Q. So in Table 10 --

THE REPORTER: Counsel, what exhibit number is that?

MS. ZHONG: Exhibit 1003. 09:55

(Exhibit 1003 was marked for identification and attached hereto.) 09:55

THE WITNESS: Okay. 09:55

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BY MS. ZHONG: 09:55

Q. So in Table 10, for each of the row lists the signals needed for a particular operation; is that correct? 09:55

MR. CHANDLER: Objection. Form. 09:55

THE WITNESS: With respect to a particular set of commands for memory devices that are consistent with Exhibit 1029, that is correct. 09:55

BY MS. ZHONG: 09:56

Q. Okay. Are those signals received in packetized form? 09:56

MR. CHANDLER: Objection. Form. 09:56

THE WITNESS: Again, it depends how you define packetized form. But in the broad sense of the word "packetized," some of them are. 09:56

BY MS. ZHONG: 09:56

Q. Which ones are? 09:56

A. A15 through A0. 09:56

Q. You mean like the address bits? 09:56

A. Well, A10 is -- 09:56

Q. Go ahead. 09:56

A. A10 is both an address bit and a control bit depending on how it's used at various times. So there are multiple pieces of information that are transmitted in -- in bursts along those wires. 09:56

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Other information like the bank address, although it's shown in this table in a very simple form, is actually only valid at -- at certain times. 09:57

There are also commands that are not listed in this portion of the table. 09:57

Q. Are there separate address pins on which the information is sent? 09:57

MR. CHANDLER: Objection. Form. 09:57

THE WITNESS: On which what information is sent? 09:57

BY MS. ZHONG: 09:57

Q. So that's separate address pins A0 through A15; is that correct? 09:57

A. Memory devices that are compliant with Exhibit 1029 do have distinct pins for A0 through A15. 09:58

Q. So the information listed in each row is sent in parallel on each of the discrete pins; is that correct? 09:58

A. In Table 10 the information -- no, I don't believe that that's -- let's see. 09:58

Let's see. In a bank activate command -- I'm not sure I understand the question. 09:58

Each command works a little bit differently. And the information that's in Table 10 09:59

would be triggered by the same clock edge would be a more precise way to say it. 09:59

Q. But the CS bar, RAS bar, CAS bar, and WE, you don't contend those are packetized signals, correct? 09:59

MR. CHANDLER: Objection. Form. 09:59

THE WITNESS: Again, it depends how you define "packetized." But -- 09:59

BY MS. ZHONG: 09:59

Q. What's your definition of "packetized"? 09:59

A. Well, I think it depends on context. 10:00

Q. Well, in the context of DRAMs or DIMMs, what's the definition of packetized? 10:00

A. I don't think it has a single definition for -- for the entire field of DRAMs or DIMMs. It's a word that can be useful in describing certain things. But we tend to use much more precise descriptions such as the timing diagrams that are provided in Exhibit 1029. 10:00

Q. When you say the Rambus memory modules you are familiar with were using packetized format for the control and address information, what did you mean? 10:00

A. There I'm referring to the way Rambus used that term in their commercially available 10:00

information at the time, which was that they used a single communication channel to provide bundles of information that could include control, address or data sharing the same channel at that time. 10:01

Q. And that differs from how JEDEC compliant, for example, registered DIMM operates; is that correct? 10:01

A. JEDEC compliant registered DIMMs such as the ones in JESD21-C do not use the precise same protocol as the commercial Rambus DIMMs that I'm familiar with from earlier. 10:01

Q. What about SODIMMs? Do they use something similar to what the Rambus does? Like JEDEC compliant small-outline DIMMs, do they use protocol similar to what Rambus uses? 10:01

A. There are many varieties of SODIMMs that have been through the years. 10:02

Q. Are you aware of any small outlying DIMMs that's JEDEC compliant and uses Rambus packetized control and address information signaling protocol? 10:02

A. I don't know one way or the other. I'm not aware of one off the top of my head. 10:02

Q. Okay. What about at the time of invention, which is 2004 and 2005 time period? Are you aware of any JEDEC compliant memory module that 10:02

uses Rambus packetized signaling scheme?

A. I don't know one way or the other. 10:03

Q. Can you think of any? 10:03

A. I just am not aware of whether or not -- 10:03

I'm aware of memory modules that used it. I just 10:03

don't know off the top of my head whether or not 10:03

there was a corresponding JEDEC standard at the 10:03

time. 10:03

Q. Which ones are you thinking of? 10:03

A. I don't remember them by name. But I can 10:03

go to a number of different memory model 10:03

manufacturers and get Rambus compliant memory 10:03

modules in the 2000 to 2005 time period. 10:03

Q. I'm not talking about Rambus compliant. 10:03

I'm talking about JEDEC compliant memory modules. 10:03

A. What I said is I don't know whether or not 10:03

there's a corresponding JEDEC standard off the top 10:03

of my head. 10:03

Q. For the JEDEC standards you relied upon, 10:04

are you aware of any modules that actually used 10:04

packetized signaling scheme that a Rambus used? 10:04

A. For the JEDEC standards that I relied on 10:04

as exhibits to my declaration, I'm not aware of any 10:04

of them using a Rambus compliant signaling protocol. 10:04

Q. Can you point me to an express disclosure 10:04

in Perego where it said that it's using JEDEC signaling scheme on a module level? 10:04

A. I don't think I am aware of, right now, of an express disclosure in Perego that one would use a JEDEC compliant memory module by name. 10:06

There are simply a lot of disclosures in Perego about the breadth of applicability and the characteristics of the memory module that would lead a person of ordinary skill to understand that a JEDEC compliant memory module is compatible with the invention described in Perego. 10:07

Q. Okay. Does a JEDEC compliant memory module have configurable buffer width? 10:07

THE REPORTER: I'm sorry, configurable? 10:07

MS. ZHONG: Buffer, B-U-F-F-E-R, width, W-I-D-T-H. 10:07

THE REPORTER: Thank you. 10:07

THE WITNESS: Not ordinarily. So one would need then to incorporate that teaching from Perego into the JEDEC module. 10:07

Also there are many teachings in Perego that apply to a fixed width buffer as well as a configurable one as well. So there's no requirement to implement all the teachings of Perego that you have the ability to configure the buffer width as 10:08

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opposed to simply selecting one in advance. And if you selected one in advance, then it would be much closer to the existing JEDEC modules at the time. 10:08 10:08 10:08

BY MS. ZHONG: 10:08

Q. What's the bit width of JEDEC compliant memory modules at the time? 564? 10:08 10:08

A. There were many different kinds that are contemplated. JESD21 is exemplary, and it talks about widths of 64 and 72. 10:08 10:08 10:09

But if you look at the underlying standards for the chips, JESD79-2, for example, or JESD79, they contemplate capability probably everywhere from 4, 8, 16, 32, 64, or even more. 10:09 10:09 10:09

Q. Did you cite any JEDEC module standard with x4, x8, x16 bit width? 10:09 10:09

A. I don't recall if I cited a specific module standard. One would understand that from the chip standards. 10:09 10:09 10:09

Q. I'm asking you are you aware of any JEDEC standards at the time that specifies a x4, x6, x8, x16 memory module width? 10:09 10:10 10:10

A. Yes, but I can't give you the specific standard number off the top of my head. 10:10 10:10

Q. Are those for the DRAMs DIMMs? 10:10

A. They are for DRAM DIMMs. 10:10

Q. And what was the width; do you recall? 10:10
A. Not specifically, but I do recall that they were x8 DIMMs. 10:10
Q. And what kind of chip would they use? 10:10
A. A variety of different kinds of DRAM chips depending on the date. 10:10
Q. So they can be x16 DRAM chips? 10:10
A. Not on a x8 module, no. A x8 module would use x1, x4, or x8 chips. 10:10
Q. When was that extended; do you have any recollection? 10:11
A. It was in the 1990s, but I don't recall the exact dates. It may have been later. 10:11
Q. Okay. Are you aware of any JEDEC standards in the early 2000s that use -- still use x8, x16 memory module widths? 10:11
A. Well, as I said, those are contemplated in JESD79-2. The physical dimensions of the module are not described in the JESD79.2 but the functionality is. 10:11
Q. I'm asking about the memory module definition. 10:12
A. Well, there are many aspects to a memory module definition. I -- I'm not aware one way or the other whether or not there's a physical form 10:12

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factor specification from JEDEC, but the functionality is described in JESD79 and JESD79-2. 10:12

Q. Okay. For Exhibit 1032, which you say has a bit width of x64 or x72, how many DRAMs would there be in a rank if each DRAM is x4? 10:12

A. Depending on the implementation, typically there would be either 16 or 18. But there can be more. 10:13

Q. Okay. So how many DRAMs would there be for a x64 memory module if the SDRAM used is x8? 10:13

A. Typically 8. 10:13

Q. And what about x16? So if you use a x16 SDRAM for a x64 DIMM, how many DRAM devices are there in rank? 10:13

A. There would typically be 4 per rank. 10:13

Q. When is the concept of rank introduced in JEDEC standards? 10:14

A. I'm sorry, I missed a word, the concept of? 10:14

Q. When is a concept -- concept of rank introduced in JEDEC standards? 10:14

MR. CHANDLER: Object to form. 10:14

THE WITNESS: I think the concept predates JEDEC standards and is probably in some of the very earliest ones. But there are issues of vocabulary. 10:14

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In the 1980s and 1990s the word "bank" -- with a "B" -- was typically used for that concept. And somewhere in the 2000 to 2010 time frame, practitioners transitioned from using the word "bank" most commonly to describe a set of one or more chips that would respond to the same command or chip select signal to using the word "rank."

The concept didn't change but the vocabulary changed. And the reason for that is because it became more common for individual memory die to contain multiple banks on them. So there was a motivation to distinguish the vocabulary, but there was no new concept that was introduced at that time.

BY MS. ZHONG:

Q. What do you mean by "it became more common for individual memory dies to contain multiple banks on them"? What are you referring to by the "banks" there?

A. In the case of an individual memory die, in the earlier days there would be one memory array with rows and columns. And in the case of DRAM, an entire row would be read to something that would typically be called something like a page register.

As DRAM densities increased, in order to

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maintain speed, manufacturers began to build two relatively independent memory arrays on the same semiconductor die, each of which could independently have a row read out to one of two page registers. And those were called banks because they had very similar characteristics to the physical module banks of memory that had been known in the art before. 10:16

And as memory densities increased, we began to get chips with 4 and 8 banks on them. So because there was a desire to distinguish the vocabulary for that kind of a memory bank from the earlier kind of a memory bank, memory providers started to use the word "rank" to describe the one or more chips on a module that would simultaneously respond to a command. 10:16 10:17

Q. Perego also mentions a concept called "channel." Do you recall that? 10:17

A. Yes. 10:17

Q. What is the term "channel" in the context of Perego? 10:17

A. It's simply one or more wires that are used to convey information. 10:17

Q. So in Perego Figure 4A, how many channels are there? 10:18

MR. CHANDLER: Object to form. 10:18

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THE WITNESS: So you're referring to the channels from the host computer to the module or the channels from the buffer chip 405 to the various memory devices. 10:18 10:18 10:19 10:19

BY MS. ZHONG: 10:19

Q. So in Figure 4A of Perego, it describes channels 415a and 415b, correct? 10:19 10:19

A. I don't see those labeled on the drawing. We can look to the text. 10:19 10:19

Q. You don't see them labeled on the drawing? Like don't you see 415a on the lower left corner and 415b on the lower right corner of Figure 4A? 10:19 10:19 10:19

A. You're saying 415? 10:19

Q. Yes. 10:19

A. Oh. Yes, I do see 415a and 415b. 10:19

Q. Okay. So -- 10:20

A. The text -- 10:20

Q. -- with respect to -- 10:20

A. The text says that it's not necessary to have two, that you could have one. But the illustration shows two. 10:20 10:20 10:20

Q. Okay. So in this context, what is a channel? 10:20 10:20

MR. CHANDLER: Objection. 10:20

THE WITNESS: In the context of 415a and 10:20

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415b, it is the set of wires that is used to communicate from one or more of the DRAM chips to the buffer chip. 10:20

BY MS. ZHONG: 10:20

Q. How many ranks are there, Exhibit [sic] 4A? 10:20

THE REPORTER: I'm sorry. What was your question? 10:20

THE WITNESS: A what? 10:20

BY MS. ZHONG: 10:20

Q. How many ranks of memory chips are there in Figure 4A? 10:20

MR. CHANDLER: Objection. Form. 10:20

THE WITNESS: I believe that what's illustrated is two ranks. But, again, the text explains that one could have a different number. 10:21

BY MS. ZHONG: 10:21

Q. Why do you believe in Figure 4A there are two ranks of memory devices? 10:21

A. Actually, let me think about that for another minute. 10:21

I'm not sure that we're given enough information about Figure 4A to make an exact determination there. 10:24

Figure 4A is illustrating certain aspects. 10:24

But if you read it in context, it can be used with a lot of different kinds of memory modules. 10:24

I believe that in certain embodiments it's certainly intended to represent two ranks, but there could be some implementations or some embodiments in which it's more. 10:24 10:24 10:24 10:25

Q. And in Figure 4B, how many channels are there? 10:25 10:25

MR. CHANDLER: Object to form. 10:25

THE WITNESS: Well, there again, there are lots of different kinds of channels. But there are -- in Figure 4B there are four channels going out to DRAM devices and a fifth channel going off to the memory controller. 10:25 10:25 10:25 10:25 10:25

BY MS. ZHONG: 10:25

Q. Okay. And how many ranks are there in Figure 4B? 10:25 10:25

A. Again, it depends which variety of memory one were to implement. But I think that in at least some of the embodiments that are described in the specification, that would be a four-rank implementation. 10:25 10:25 10:25 10:25 10:25

Q. In which embodiment described in Perego would this be a four-rank implementation? 10:25 10:25

A. For example, if those were DDR memory 10:25

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devices. 10:26

Q. So why would there be four-rank -- let me 10:26

reask. 10:26

Why would Figure 4B involve a four-rank 10:26

implementation if the devices are DDR memory 10:26

devices? 10:26

MR. CHANDLER: Objection. Form. 10:26

THE WITNESS: Well, because if we look at 10:26

it in context, you know, Figure 4C is probably the 10:26

better illustration, because -- 10:26

BY MS. ZHONG: 10:26

Q. Okay. 10:26

A. -- what it shows is something that might 10:26

be kind of specific to a DDR -- 10:26

Q. Okay. 10:26

A. -- to implementation. 10:26

And that is that there seems to be an 10:26

intention there that an entire channel would be 10:26

selected and respond to the same command at one time 10:27

whether it had one device or more than one device on 10:27

that channel. 10:27

Q. So if you only have a single channel, how 10:27

many ranks would there be if the memory devices are 10:27

DDR basic devices? 10:27

A. Again, there are a variety of embodiments 10:27

that are described. But my understanding would be 10:27
that if there was only a single channel, then -- you 10:27
could put more than one rank on a channel, but I 10:27
think what's basically described would be probably, 10:27
in the simplest implementation, would be one rank 10:27
per channel. 10:28
Q. Okay. So in a one-rank-per-channel 10:28
implementation, there is only one physical rank, 10:28
correct, for a single channel? 10:28
A. If you have -- 10:28
MR. CHANDLER: Objection. Form. 10:28
THE WITNESS: If you have one channel and 10:28
one rank per channel, then you would only have one 10:28
physical rank. 10:28
BY MS. ZHONG: 10:28
Q. Okay. So in that implementation, there 10:28
would be -- the concept of rank multiplication would 10:28
not apply; is that right? 10:28
MR. CHANDLER: Objection. Form. 10:28
THE WITNESS: You'd have to look at the 10:28
entirety of the memory system, but that's certainly 10:28
not the intent of rank multiplication. I think the 10:28
intent of rank multiplication is to make a larger 10:28
number of ranks appear to be a smaller number of 10:28
ranks. 10:29

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BY MS. ZHONG: 10:29

Q. So if there's only a single physical rank, then the concept of rank multiplication would not apply? 10:29

A. If your entire system only has one physical rank, then you are not practicing rank multiplication. 10:29

Q. And you say like in Perego, the intention is one rank per channel in general, correct, at least for DDR compliant language? 10:29

So in Perego, the intention is one rank per channel for JEDEC compliant DDR devices; is that correct? 10:29

MR. CHANDLER: Objection. Form. 10:29

THE WITNESS: I think that's the simplest implementation that a person of ordinary skill would understand under those particular circumstances. 10:29

BY MS. ZHONG: 10:30

Q. Anywhere in your declaration that you describe multiple ranks per channel for Perego's implementation? 10:30

A. I don't recall. 10:30

Q. You can't find any right now, correct? 10:30

A. Not at the moment. 10:30

Q. Can you please turn to column 14 of 10:31

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Perego. 10:31

THE REPORTER: Counsel, excuse me, what 10:31

exhibit number is that? 10:31

MS. ZHONG: Exhibit 1035. 10:31

THE REPORTER: Thank you. 10:31

BY MS. ZHONG: 10:31

Q. Can you please take a look at the example 10:31

described in column 14, lines 41 to 43. 10:31

A. Okay. 10:32

Q. So in column 14, lines 41 to 43, in that 10:32

example, the memory device access width is 128 bits, 10:32

correct? 10:32

A. In that particular example, that is the 10:32

case, yes. 10:32

Q. And what does that mean, the memory access 10:32

width is 128 bits? 10:32

A. I believe that it means that the 10:33

collection of memory devices in that particular 10:33

embodiment produced data 128 bits at a time. 10:33

Q. Okay. Let me see what I can understand. 10:33

You believe that means for a single read 10:33

or write operation, 128 bits will be transferred 10:33

from the memory devices on the module; is that 10:33

correct? 10:33

MR. CHANDLER: Objection. Form. 10:33

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THE WITNESS: Can I hear the exact question again? 10:33

BY MS. ZHONG: 10:33

Q. Is it correct that a memory device access width of 128 bits means that in a single read or write operation, 128 bits of data will be transferred from the memory devices on the module? 10:34

MR. CHANDLER: Objection. Form. 10:34

THE WITNESS: It means that the memory devices on the module will output 128 bits or input 128 bits for a single read or write operation. 10:34

BY MS. ZHONG: 10:35

Q. Okay. But the configurable width buffer device interface width is only 16 bits in this particular example, correct? 10:35

A. In this particular example, that is correct. 10:35

Q. And that means there are only 16 pins to transfer data at a time; is that correct? 10:35

A. In this particular example, yes, that only 16 pins are used. 10:35

Q. So how can you transfer 128 bits in a single read and write operation if there are only 16 pins? 10:35

A. That operation would have eight phases in 10:35

that particular situation. You would transfer the first 16 bits, then the next 16 bits, then the next 16 bits, then the next 16 bits. That's a very common technique in digital electronics. 10:35

Q. Okay. So what you mean is that the 128 bits will be transferred in eight cycles from the 16 pins? 10:36

MR. CHANDLER: Objection. Form. 10:36

THE WITNESS: It depends how you define a cycle. Usually at this point in time, we would be talking about double data rate. 10:36

So we would have two pieces of information per cycle, but each transfer would be 16 bits. And there would be 8 transfers on the memory controller to module bus. And those 8 transfers would transfer in total 128 bits. 10:36

BY MS. ZHONG: 10:36

Q. So regardless of the buffer width -- 10:36

THE REPORTER: I'm sorry, Counsel, one more time. I lost a word in there. 10:36

BY MS. ZHONG: 10:36

Q. So regardless of the width of the configurable buffer, 128 bits will be transferred for each read and write operation; is that correct? 10:37

MR. CHANDLER: Object to form. 10:37

THE WITNESS: No. Maybe I'm not sure what you're asking. 10:37

The 128 bits is a characteristic of this particular example. And in this particular example, the configurable width buffer device interface width is 16 bits. So I don't know what it means to disregard that portion of the example. 10:37

BY MS. ZHONG: 10:37

Q. So if we keep the memory device access width constant and change the configurable buffer width, all that changes is the number of transfers that are needed to transfer out the 128 bits; is that correct? 10:37

A. There are other things that change. But the primary thing that would change would be the number of transfers required, and that's what's referred to as the serialization ratio. 10:38

Q. Can you also turn to column 15? There is a reference to another serialization ratio in column 15, if you can take a look at that. 10:38

A. I'm not sure which one you're talking about. You're talking about around line 6, 7? 10:38

Q. Starting from lines 6 to line 30. 10:38

A. Okay. 10:39

Q. How is serialization ratio different from 10:39

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the serialization ratio that's described in column 14? 10:39

A. I don't believe it is. I think it's simply another description of the same concept. 10:39

Q. Okay. So the primary link -- 10:39

A. Let me -- let me correct that. Let me correct that. 10:40

Q. Okay. 10:40

A. The description in 15 takes into account the possibility that these channels could be running at different speeds. So, therefore, in the example that we talked about before, we would take 128 bits and break it into eight 16-bit portions. 10:40

That's happening here as well, but what it's saying is if you want to have matched bandwidth, which means if you want to have the same capacity over time for each channel, that the channel that communicates in eight steps should be eight times as fast so that it can communicate 128 bits in the same amount of time. 10:40

Q. So when you say "channel," which channel are you referring to? 10:41

A. The narrower -- in that particular statement, I was referring to the narrower channel. 10:41

In other words, if we want each of the 10:41

channels -- and this is particularly the channel 370, which is the channel between the memory device and the buffer device and the -- what's called here the primary channel, which is the channel between the buffer device and the host computer. 10:41 10:41 10:41 10:41 10:41 10:41

What this is saying is if they have different widths and yet we still want them to have the same capacity, then if we make the width of the narrow channel N times narrower, it must also be N times faster in order to have the same capacity over time. 10:41 10:41 10:41 10:41 10:41 10:42

Q. So you are saying that if the secondary channel can output 128 bits and the primary channel is only 16 bits wide, then that primary channel needs to be eight times faster than the secondary channel; is that right? 10:42 10:42 10:42 10:42 10:42

A. If you want to also have the requirement, which is optional, that they have equivalent bandwidth. 10:42 10:42 10:42

Q. Okay. What is the meaning of the memory module bit width? 10:42 10:43

A. What is the meaning of the memory module bit width? 10:43 10:43

Q. Uh-huh. 10:43

A. Again, it would depend on the context. But normally that term is used to describe the number of bits that are communicated in a single read or write operation between the memory module and the host computer. 10:43

Q. So in the example that we discussed in column 14, lines 40 to 43, what is the bit width of the memory module then? 10:43

A. Again, I don't think there's a standard definition. But I think that most engineers would probably describe that as a 128-bit-wide memory module because that's the size of the transfers. But there could be variation in how that vocabulary is used. 10:43

Q. Okay. What is the difference between control and control address information versus control signal and address signal? 10:44

A. Again, that would depend on the context. Typically, the signal would be something physical, but not always. And information would be the knowledge contained in that signal. But depending on context, they can be used in different ways or interchangeably. 10:44

Q. Okay. So, for example, when you packetize the control and address signal in a multiplex with 10:45

data, then it doesn't really contain a physical manifestation of a control signal as you would, for example, in a registered DIMM shown in Exhibit 1032; is that right? 10:45

A. I don't think I agree. There's still a physical manifestation. In both cases there's a period of time that's important, and the voltages on a wire are going to vary during that period of time to convey information. 10:45

Q. But in the packetized form, the information is serialized, and you have to decode it in order to extract that information; isn't that right. 10:45

A. You don't necessarily need to decode it. What you have to do is implement it at the proper time. But you always need to implement a memory communication signal at the proper time. 10:46

The real difference is whether or not you're using the same wires to convey address and data signals or whether you're using two sets of wires to convey address and data signals. 10:46

In either case, there are multiple signals being multiplexed on there for multiple transactions, for example. So everything has got to be measured and effectuated at the appropriate time. 10:46

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Q. What do you mean by "the real difference is whether or not you are using the same wires to convey address and data signals or whether you're using two sets of wires to convey address and data signals"? 10:47

A. The difference between the system that Rambus described as packetized in their commercial products and the more commonly used SDRAM DIMMs that were not Rambus compliant was that Rambus would use the same wires for address control and data, while non-Rambus-compliant DIMMs would generally use distinct wires for data. 10:47

Q. And the non-Rambus JEDEC compliant DIMMs would also have dedicated pads or pins for chip select signals; is that right? 10:48

A. Dedicated? Let me take a quick look. 10:48

Q. You can take a look at Exhibit 1032. 10:48

A. That's certainly the case for Exhibit 1032 is there were dedicated chip select signals on that particular DIMM. 10:48

Q. Is it necessarily the case that the signals sent to the SDRAM are the same as the signals that's received from the computer system? 10:49

A. I don't understand that question. 10:49

Q. So according to JEDEC Standard 79-2, 10:49

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certain signals have to be sent to the SDRAM, for example, band address signals, chip select signals, CAS bar, RAS bar, and right enable bar, correct? 10:49

A. Are you asking do they need to be sent to the SDRAM module or to the SDRAM device? 10:49

Q. To the SDRAM device. 10:49

A. They would ordinarily be used to control the SDRAM device. It's up to the module designer whether or not to send them directly or whether or not they can be passed through some logic function first. 10:49 10:50 10:50 10:50

Q. Okay. But do the exact same signals have to be received on the DIMM, or can they be received in an encoded form and then decoded to send those signals out to the SDRAM? 10:50 10:50 10:50 10:50

MR. CHANDLER: Objection. Form. 10:50

THE WITNESS: I'm not sure what you're asking. The symbols that are shown -- the signals that are shown on page 7 of Exhibit 1032 are signals at the connector of the DIMM as specified. 10:50 10:50 10:50 10:50

BY MS. ZHONG: 10:50

Q. But you said there are many different DIMMs, right, and the signaling scheme does not have to be the same, as shown in this JEDEC specification; is that correct? 10:50 10:50 10:51 10:51

A. Sure. Not every DIMM has the same signals as JESD21-C. 10:51

Q. Okay. So, for example, the information can be received in a packetized form and then demultiplexed or decoded to extract the signals; is that correct? 10:51

MR. CHANDLER: Objection. Form. 10:51

THE WITNESS: I'm not sure what we're talking about. This is on some hypothetical DIMM? 10:51

BY MS. ZHONG: 10:51

Q. Can that be done? 10:51

A. Sure, conceivably one could do that. 10:51

Q. And, for example, Perego's DIMM uses -- at least in some of the embodiments, they use packetized format to convey the control and address information, correct? 10:51 10:52 10:52 10:52

A. In some embodiments. But Perego contemplates a wide variety of -- of embodiments and he talks about things well beyond just point-to-point links. 10:52 10:52 10:52

Q. And in those preferred embodiments that you relied on, those are point-to-point links; is that right? 10:52 10:52

MR. CHANDLER: Objection. Form. 10:52

THE WITNESS: No. They're described as 10:52

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something that could be implemented as a point-to-point link, but there's also a discussion of other kinds of links as well. 10:52

MR. CHANDLER: We have been going about two hours. Whenever you are at a good breaking point, it might be a nice time for a break. 10:52 10:53 10:53

MS. ZHONG: Sure. 10:53

Q. Why don't we take a look at your declaration, Exhibit 1003, page 77, paragraph 133. 10:53 10:53

Are you there? 10:53

A. Yes. 10:53

Q. So for the specific citation that you quoted here, which I believe we discussed earlier, that is a distinct signaling scheme from the JEDEC compliant signaling scheme; is that correct? 10:53 10:53 10:54 10:54

MR. CHANDLER: Objection. Form. 10:54

THE WITNESS: As I said, I'm not familiar off the top of my head with every JEDEC standard. But the particular example that's quoted in paragraph 133 that's from column 13, line 54, is describing something that's distinct from JESD21-C. 10:54 10:54 10:54 10:54 10:54

BY MS. ZHONG: 10:54

Q. So what's described -- what you quoted in paragraph 133 is a different signaling scheme than that is used for the RDIMM described in 10:54 10:54 10:54

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Exhibit 1032; is that correct? 10:55

A. It is not an identical signaling 10:55

mechanism, but it does have teachings that are 10:55

applicable to the signaling mechanism used for DDR2. 10:55

Q. Okay. So, for example, it does not have 10:55

the CS signal, the CAS, RAS -- let's go to page 16 10:55

of Exhibit 1032. 10:55

A. Uh-huh. 10:55

Q. For example, the signaling scheme 10:55

described in 133 would not have the signals that's 10:55

listed on the left-hand side of the register box; is 10:55

that correct? 10:56

A. I think it would have those signals. It 10:56

just wouldn't necessarily have them in the exact 10:56

same physical form. It would have them in a way 10:56

that has a different physical implementation. But 10:56

certainly a person of ordinary skill in the art 10:56

would understand how the teachings apply to both. 10:56

Q. Okay. So they will be a different 10:56

physical implementation that's different than what's 10:56

described on Exhibit 1032, page 16; is that right? 10:56

A. That's true with respect to that one 10:56

particular statement. If you look at the teaching 10:56

as a whole, it's broad enough to encompass what's in 10:56

1032. 10:56

MS. ZHONG: We can take a break. How long do you want it to be? 10:56

Why don't we get off the record and then we can discuss how long the breaks needs to be. 10:57

MR. CHANDLER: Okay. 10:57

(Recess.) 11:08

(Off record: 10:57 a.m.) 11:08

(On record: 11:16 a.m.) 11:08

MS. ZHONG: We can go back on the record. 11:16

Q. Dr. Wolfe, can you go back to your declaration, Exhibit 1003, page 93? 11:17

A. Okay. 11:17

Q. Do you see Table 10, the command truth table? 11:17

A. Yes. 11:17

Q. Is the content in that command truth table something that had a person of ordinary skill in the art would be familiar with at the time of the '912 inventions? 11:17

A. Yes. 11:18

Q. So, for example, they would know, for a DDR SDRAM, a write operation would include bank address information; is that correct? 11:18

A. Yes, for things that are compliant within JEDEC Standard 79-2. 11:18

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Q. So they would know that in order for the SDRAM to perform a write operation the DIMM has to receive the bank address signals, correct? 11:18

A. Was the question that the DIMM has to receive the bank address signals? 11:18

Q. Correct. 11:18

A. That's from JESD79-2, which does not require a DIMM. But if that particular chip were on a DIMM, then the DIMM would need to receive the bank address signals. 11:19

Q. Okay. And so if a DDR or DDR2 device is on the DIMM, does that DIMM have to receive a bank address signal in order to perform a read operation? 11:19

A. If you're using a JEDEC Standard 79-2 memory on a DIMM, then that DIMM would need a bank address signal. 11:19

Q. Are you aware of DRAMs that do not use bank address signals for read or write operation? 11:19

A. Yes. 11:20

Q. Which kind of DRAMs do not use bank address signals for read and write operation? 11:20

A. I'd have to go back and look at the specific specifications. But, based on my recollection, perhaps the Burst EDO DRAMs may not have used them, or it may be a previous generation. 11:20

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Q. Okay. What about DDR2, DDR SDRAMs? Are you aware of any such memory devices that do not use bank address signals for read or write operation? 11:20

A. If by DDR and DDR2 you mean things that are compliant with JESD79 or JESD79-2, in that case I'm not aware of any that don't use a bank address signal at the memory chip device itself. It doesn't necessarily have to be provided to anything else on the DIMM. 11:20 11:21

Q. So how can the bank address signals be provided to the SDRAM if the signal is not sent to the DIMM on which the SDRAM is sent on? 11:21

A. There are lots of different ways. You could do a design. You could generate them on the DIMM hypothetically, depending on what you were using the DIMM for and what you were trying to accomplish. 11:21

Q. Okay. So according to you, it is not necessary for DIMM to receive, for example, bank address signals, RAS, CAS -- let me withdraw and ask. 11:21 11:22

Is -- would it also be the case that for a read and write operation that's to be performed by a DDR, a DDR2 SDRAM, it is not necessary for the DIMM on which the SDRAM is set on to receive a chip 11:22

select signal? 11:22

A. It would not be necessary, but it would be ordinary for the DIMM to receive a chip select signal. 11:22

Q. And would it be ordinary for the DIMM to receive a bank address signal for a read and write operation? 11:23

A. If it were a memory DIMM that used memory chips compliant with JESD79 or JESD79-2, it would be ordinarily for that DIMM to be provided with a bank address signal. That bank address signal, in the simplest case, would go directly to the memory devices. 11:23

Q. What if it is a registered DIMM? Would that bank address signal go to the register on the DIMM side then? 11:23

A. Again, we'd have to look at the particular standards. But in the case of, for example, the JESD21-C registered DIMMs, bank address signals would go to a register typically. 11:24

Q. Were DDR2 or DDR SDRAMs common at the time of the '912 invention? 11:24

A. By "common" do you mean generally available? 11:24

Q. When someone says a DRAM device in 2004 11:24

and 2005, would the person of ordinary skill in the art that DDR2 -- (indiscernible.) 11:24 11:24

THE REPORTER: I'm sorry. Excuse me, Counsel. I lost you on that one. Repeat your question, please. 11:25 11:25 11:25

BY MS. ZHONG: 11:25

Q. So in 2004 and 2005, when a person with ordinary skill in the art mentions a DRAM device, would others understand that the DRAM device they refer to would include DDR2 or DDR device? 11:25 11:25 11:25 11:25

A. I think they would understand that it could include a DDR or DDR2 device, especially if they were in the context of a general purpose computer. 11:25 11:25 11:25 11:26

Q. Okay. And if the person -- the description for that DRAM device also include things such as chip select signals, would that also be consistent with the reference to a DDR or DDR2 device? 11:26 11:26 11:26 11:26

A. If I understand your question correctly, the use of chip select signals on a DDR or DDR2 memory device is ordinary. 11:26 11:26 11:26

Q. What do you mean by "ordinary"? 11:26

A. For the most commonly available devices would -- that are DDR or DDR2 in the 2004, 2005, 11:27 11:27

2006 time frame -- would be compliant with JESD79 or JESD79-2 and would include a chip select input. 11:27

Q. So if a DRAM device is described as including a chip select signal, would that indicate to a person of ordinary skill in the art that device is likely a DDR2 or DDR device? 11:27

A. No, that would generally not be a identifying or distinguishing characteristic. 11:28

Q. And you said that if the DRAM device was used in connection with a personal computer, then a person of ordinary skill in the art would understand that a DRAM device could be a DDR2 or DDR device, correct? 11:28

A. That would be true in the 2000 to 2006 time frame. 11:28

Q. Okay. And then they would understand that if those are DDR and DDR2 device, in order for the DDR -- in order for the memory device to perform a read, write, bank activation operation, it would be ordinary for the computer system to send signals such as bank address signals, chip select signals, CAS bar, RAS bar, and write enable bar; is that correct? 11:29

A. It would be ordinary to send those to an ordinary personal computer in DDR or DDR2 module at 11:29

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that time. 11:30

Q. What do you mean by "It would be ordinary to send those to an ordinary personal computer in DDR or DDR2 module"? 11:30

A. One could -- one can use these chips in many different ways and build many different kinds of memory modules. But there were typical memory modules at the time that were JEDEC compliant with various JEDEC standards. 11:30

Q. Are you saying those CAS bar, RAS bar, WE, and chip select and bank address signals are sent to the personal computer instead of being sent from the personal computer to the memory modules? 11:30

MR. CHANDLER: Vague. 11:31

THE WITNESS: No. 11:31

BY MS. ZHONG: 11:31

Q. Hello? 11:31

A. Yes. I answered, "no." 11:31

Q. You are saying that it would be ordinary for a personal computer to send CAS bar, RAS bar, WE bar, chip select signals and bank address signals to the memory module for a read and write operation at the time of the invention; is that correct? 11:31

A. Yes, I think that's fair. And then one would have to look at how those are then connected 11:32

on the memory module to figure out whether or not that's at all relevant to these claims. 11:32

Q. Is that something a person of ordinary skill in the art would understand? 11:32

A. Yes. 11:32

Q. Can you pull up Exhibit 1034. 11:33

(Exhibit 1034 was marked for identification and attached hereto.) 11:33

THE WITNESS: Okay. 11:33

BY MS. ZHONG: 11:33

Q. Can you please go to page 2 of Exhibit 1034. 11:33

A. Okay. 11:33

Q. The last paragraph on the right hand, "disables the chip select bus." Do you see that? 11:33

A. Yes. 11:33

Q. So according to this paper, the chip select bus is essential in the JEDEC-style memory system. Do you agree with that? 11:33

A. In the context that's being used in this paper where it's talking about DIMMs in a traditional computer, I do think that the chip select bus is essential in as far as it needs to exist. 11:34

Q. In the Rambus memory module that you are familiar with, there isn't a chip select bus; is that correct? 11:34

A. There is not a distinct chip select bus. It's subsumed into the -- into the Rambus channel. 11:34

Q. And what's your understanding of the chip select bus in the context of Exhibit 1034? 11:35

A. I think that it's simply saying that in a conventional PC-type memory system as of 2002 -- and by "conventional," that's not the Rambus type -- that there is a chip select signal provided for every rank of memory in order to control the timing of that rank with respect to responding to commands. 11:35

Q. So what's the difference between a bus versus the point-to-point architecture described in Perego? 11:36

A. A bus can be used broadly here. I think in this particular reference, I think "bus" simply is being used to refer to a collection of wires. 11:36

The -- again, and Perego does disclose buses as alternatives to point-to-point. It discloses both kinds of embodiments numerous times. 11:36

But in his point-to-point description in Perego, he talks about things that have one transceiver on each end, where in Perego buses used 11:36

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a thing -- described things that can have more than one transceiver. 11:36

I'm not sure that it's being used in exactly the same way here. It's quite possible that -- that this particular chip select bus the way it would normally be implemented would be point-to-point. 11:36

And it's also common to use the term "bus" to simply refer to a collection of wires. And I believe that's what's being done in 1034 in the area that we referred to. 11:37

Q. Okay. So in the 2004 and 2005 time period, a conventional PC system would send chip select signals, CAS bar, RAS bar, write enable bar, clock, bank address signals to a DIMM; is that correct? 11:37

A. I don't know if it would send all of those. 11:37

Q. Which signals you don't think it would send? 11:38

A. I don't think it's just a clock at that time frame. I think it tends to be a little more complicated, and there are a number of -- 11:38

Q. Okay. 11:38

A. -- timing signals that are sent. 11:38

Q. So in the 2005 and 2005 {sic} time period, a conventional PC system would send chip select signals, CAS bar, RAS bar, write enable bar, bank address signals to a DIMM for a read and write operation; is that correct? 11:38

A. That would be typical. And, again, then it would depend on the implementation as to what the DIMM did with those signals. 11:38

Q. Would those same signals be sent to a DIMM by a conventional PC for bank activation -- row activation operation in the 2004 and 2005 time period? 11:38

A. They wouldn't all be used for row -- for row activation, but they would be physically present. 11:39

Q. Okay. And for bank activation, would those -- would those same signals be sent from a conventional PC system to a memory module in the 2004 and 2005 time period? 11:39

A. Again, I don't know what you mean by signals being sent. They would be physically connected, but they could be -- some of those signals could be dormant in a bank -- in a bank activation. 11:39

Q. What do you mean by some of the signals 11:39

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would be dormant? 11:39

A. They may not be doing anything. There may 11:39

not be any information being provided on some of 11:39

those signals during a bank activate. 11:39

Q. Okay. But those signals would be sent and 11:40

received, just that they would not be used. Is that 11:40

what you mean? 11:40

A. From the perspective of the DIMM, I think 11:40

that is -- that's -- that would be common. 11:40

Q. Okay. So it would be common in 2004 and 11:40

2005 time period for a memory module to receive chip 11:40

select signals, bank address signals, CAS bar, RAS 11:40

bar, write enable bar for memory operation such as 11:40

read, write, and bank activation; is that correct? 11:40

A. Yes, from the perspective of the DIMM 11:40

itself they would be received. 11:40

Q. Can you pull up Exhibit 1035 Perego, 11:41

column 15, lines 37 to 40. 11:41

Are you there, Dr. Wolfe? 11:41

A. Give me the line numbers again. 11:41

Q. 37 to 40. 11:41

A. Okay. 11:42

Q. So according to the description there, 11:42

"According to a preferred embodiment, the target 11:42

subset of secondary channel signal lines may be 11:42

selected via address bits provided as part of the primary channel request." 11:42

Do you see that, Dr. Wolfe? 11:42

THE REPORTER: I'm sorry, Counsel. I'm sorry, Counsel. Could you repeat that and read it slowly. 11:42

BY MS. ZHONG: 11:42

Q. According to the description here, being a preferred embodiment, "the target subset of secondary channel signal lines may be select via address bits provided as part of the primary channel request." 11:42

Do you see that, Dr. Wolfe? 11:42

A. I do. 11:42

Q. Are address bits the same as chip select signals? 11:42

MR. CHANDLER: Objection. Form. 11:42

And I didn't hear the question either. 11:42

BY MS. ZHONG: 11:42

Q. Are address bits the same as chip select signals? 11:42

A. It depends on the context. 11:43

MR. CHANDLER: Court Reporter, I said address bits, B-I-T-S. 11:43

THE REPORTER: I'm sorry, spell that 11:43

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again. 11:43

MS. ZHONG: Bits, B-I-T-S. 11:43

THE REPORTER: Thank you. 11:43

BY MS. ZHONG: 11:43

Q. When you say "It depends on the context," 11:43

when are address bits the same as chip select 11:43

signals? 11:43

A. One can define -- one can design a memory 11:43

system where an address bit is used as a chip select 11:43

signal. 11:43

Q. But that would not be JEDEC compliant; is 11:43

that correct? 11:43

MR. CHANDLER: Object to form. 11:43

THE WITNESS: It depends. It could be 11:43

compliant with certain JEDEC specifications 11:43

depending on how it was done. 11:43

BY MS. ZHONG: 11:43

Q. Would it be compliant with the JEDEC 11:43

specifications that you relied on? 11:44

A. Yes, it could be compliant, for example, 11:44

with Exhibit 1029. Again, it depends what you're 11:44

trying to build and what the context is. 11:44

Q. How would it be compliant with 11:44

Exhibit 1029? 11:44

A. Well, because Exhibit 1029 describes the 11:44

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functionality of the chip select signal. It doesn't tell you what to connect it to or what you must connect it to. 11:44

Q. So you disagree with Exhibit 1034 comment that JEDEC -- JEDEC-style memory system has to have a dedicated chip select bus? 11:44

A. No, I don't disagree with them. A JEDEC-style memory system is more than -- in this context, is more than just something that uses a JEDEC compliant chip. 11:45

I think if you read this in context, it's talking about using a JEDEC compliant DIMM as is described in the previous paragraph. 11:45

Q. And in this description, column 15, lines 37 to 40, are the address bits used to define a rank? 11:45

A. In this particular embodiment, which I believe is not the one that I relied on in my declaration, the address bit can be one of the factors that's used in selecting a rank. 11:46

Q. Can you go to paragraph 96 -- page 96 to 97 and take a look at your paragraph 155? 11:46

What paragraph are you relying on? Which passage from Perego are you relying on? 11:47

A. That is column 15, 31 through 45. 11:47

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Q. And that includes the passage we just discussed, correct? 11:47

A. It does. 11:47

Q. Okay. So are you relying on the embodiment that we just discussed in your declaration? 11:47

A. For that particular teaching, yes. 11:47

Q. And in this particular teaching, the -- according to you, the rank is selected using address bits and not a specific chip select signal, correct? 11:47

A. No, no. The address bits in this particular case would be one of the factors to decide which rank to select. It would not be the only factor. 11:48

Q. And 155 you state, "Both Perego and Amidi teach using the address signals to select the target rank," correct? 11:48

A. Correct, but not exclusively. 11:48

Q. Did you say Perego and Amidi teach using the address signals in part to select the target rank? 11:48

A. No, I didn't say that. I just said that they use them, and they do use them. It doesn't say that they don't use other signals as well. 11:48

Q. And in this paragraph or elsewhere did you 11:48

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discuss what other information is used to select the target rank other than the address signals for this embodiment? 11:48 11:49 11:49

A. Well, this is part of a very extensive discussion. Let me see if I can find a better answer. 11:49 11:49 11:49

Q. Let's just discuss this preferred embodiment in particular. What other information in this preferred embodiment is used to select a target rank other than the address bits? 11:50 11:50 11:50

A. I think a person of ordinary skill would understand that the chip select is also used in this particular situation. 11:51 11:51 11:51

Q. And where does the word "chip select signal" appear in Perego? 11:51 11:51

A. In one place their individual device. Let me see. 11:51 11:51

I don't think there's an explicit description of a chip select line. I think a person of ordinary skill would have to use their knowledge of the computer system to incorporate that. 11:52 11:53 11:53

If you look, for example, at the general disclosures that say that you can have multiple modules on a bus, clearly there would have to be some indication of which module was being selected. 11:53 11:53 11:53

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And, in particular, if, as I've suggested, you would implement it with JEDEC compliant technology, then you would incorporate that feature from the JEDEC specifications. 11:53

Q. You were talking about selecting different modules. Is module the same as a rank? 11:53

A. It's not. But you wouldn't select a rank on a module unless the module itself was being selected. 11:54

Q. Okay. So you -- the PC will first select which module to communicate with -- 11:54

A. There's no -- 11:54

Q. -- and the chip select signal -- go ahead. 11:54

A. I mean, there's no sequence there. Only a single rank is going to be selected to respond from the PC's perspective. 11:54

Q. Okay. 11:54

A. And that rank will be on a specific module. 11:54

Q. I see. 11:54

Can you take a look at Perego Figure 6B, for example. 11:54

Are you there? 11:54

A. Yes. 11:54

Q. So there are -- so there are 400a, 400b 11:54

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and 400c. Each is a memory module; is that correct?

A. Correct. 11:55

Q. And there are two ranks in each of the memory module; is that correct? 11:55

A. Correct. 11:55

Q. Is that the same for 6A, Figure 6A? 11:55

A. There are only two modules in 6A, but otherwise that's the same. 11:55

Q. Okay. So in 6A there are two modules with two ranks each? 11:55

A. Correct. 11:55

Q. And the chip select signal would be selecting an entire rank; is that right? 11:55

A. It depends where you're looking at it. 11:56

Q. What do you mean, like, where you're looking at it? 11:56

A. If you are looking at it from the perspective of the processor, it's selecting a module. And then, depending on the implementation, you would either use a bank address signal or an address signal to determine the actual rank. 11:56

Q. But it would be -- let's take one step back. 11:56

Let's look at the configuration in Figure 6B. 11:56

A. Okay. 11:56
Q. Let's assume that 400a is selected. And 11:56
when a chip select signal is applied, four of the 11:56
devices will be selected at a time; is that correct? 11:57
MR. CHANDLER: Objection. Form. 11:57
THE WITNESS: Ultimately that is what's 11:57
going to happen. But the chip select signal going 11:57
to 400a would inform the buffer that it should 11:57
either select the left-hand or right-hand rank. 11:57
And then, again, depending on the 11:57
embodiment, the buffer would then use additional 11:57
information combined with the chip select 11:57
information to decide whether to select the 11:57
left-hand rank or the right-hand rank. 11:57
BY MS. ZHONG: 11:57
Q. Okay. And when a rank is selected, it 11:57
will be selected in a group of four for the 11:57
embodiments shown in Figure 6B; is that correct? 11:57
A. If you have a four wide -- four device 11:57
wide rank, that will be the case. Figure 6B is 11:57
illustrative, and I don't think it only applies to 11:58
four device slide ranks. 11:58
Q. If you only have a single device per 11:58
channel, the memory capacity would be one-fourth of 11:58
that other memory module having four memory devices 11:58

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per channel, assuming that the memory device all have the same capacity; is that fair? 11:58

A. That's fair. If you assume that the memory devices all have the same capacity, then having four memory devices would give you four times the capacity of one device. 11:58

Q. Okay. So if you -- if you have a memory module with places for four memory devices per rank, and if your goal is to expand the capacity of that memory module, it would not really make any sense for you to only place a single device in that rank; is that right? 11:58

A. That just doesn't seem consistent with my understanding of the way memory modules are designed. You design a memory module based on how many chips you want to have and how wide you want it to be, and you custom design it for that one situation. 11:59

Q. So, like, let's take a look at the Figure 6B configuration shown here. This shows there are eight memory devices -- 11:59

A. Yes. 11:59

Q. -- on one side of that device, correct? 11:59

A. That seems to -- what's illustrated is four to the left and four to the right in this 12:00

particular illustration. 12:00

Q. Okay. And so if I want to expand the 12:00

memory capacity, it would not make any sense for me 12:00

to get rid of six of the eight memory devices on 12:00

that module; is that correct? 12:00

A. That's correct. Assuming that you wanted 12:00

to expand the capacity of this particular module as 12:00

opposed to designing a module for a different 12:00

purpose that would be disclosed in Perego. 12:00

Q. Okay. And assuming that I only want to 12:00

use two chips to achieve the same capacity as using 12:00

eight chips, the density per chip has to increase by 12:00

a factor of four? Does that sound correct? 12:00

MR. CHANDLER: Object to form. 12:01

THE WITNESS: If you make all those 12:01

assumptions, that would be correct. But again, 12:01

those aren't always valid assumptions. 12:01

BY MS. ZHONG: 12:01

Q. And a memory chip with four times the 12:01

memory density would be more costly than a memory 12:01

chip that is 1x density? Does that sound fair? 12:01

A. That's not always true, but it's true in 12:01

certain market segments. 12:01

Q. In which market segments is that true? 12:01

A. It's true when the lower-capacity chip is 12:01

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a mainstream chip and the higher-capacity chip is just entering production. 12:01 12:01

Q. Okay. So let's take a look at your declaration. Why don't we go to page 92 of your declaration. 12:02 12:02 12:02

Do you see a Table 2 and Table 3 on that page? 12:02 12:02

A. I do. 12:02

Q. Okay. What is showing in Tables 2 and 3? 12:02

A. These are examples of JESD79-2 compliant memory configurations. 12:02 12:02

Q. And in Table 2, those are SDRAMs with 512-megabit density; is that correct? 12:02 12:02

A. Correct. 12:02

Q. And what is the difference between by x4, x8, and x16 format? 12:03 12:03

A. The number of data pins that are present on each individual device. 12:03 12:03

Q. Can you be more specific? What do you mean by the number of data pins that are present on each individual device? What's the difference between x4, x8, and x16? 12:03 12:03 12:03 12:03

A. x4 has four data pins per individual device. X8 has eight data pins per individual device. And x16 has 16 data pins per individual 12:03 12:03 12:03

device. 12:03

Q. Okay. So let's take a look at Figure 2, 12:03

the 512-megabit DRAM devices. 12:03

What does 32 megabits mean in the 12:03

configuration on the right-hand side for the x16 12:03

configuration? 12:04

A. In Table 2? 12:04

Q. Yes. Table 2. So Table 2 -- 12:04

A. It means there are -- 12:04

Q. -- means 32 megabits -- I'm sorry. 12:04

A. It means there are 32 million entries in 12:04

that memory, each of which contains 16 bits. 12:04

Q. And what's the cost difference between a 12:04

32Mbx16 DRAM device versus a 62 -- 64Mbx8 device? 12:04

A. It depends on the market at the time. 12:04

Q. What's the market at the time? What's the 12:04

cost difference? 12:04

A. I don't know. I mean, it could vary from 12:04

week to week, and depending on manufacturing 12:04

shortages and trends and what's common in various 12:04

computers. 12:05

Usually early in introductions, 64Mbx8 is 12:05

cheaper, and then over time the 32Mbx16 becomes 12:05

cheaper. 12:05

Q. So initially 64Mbx8 is actually cheaper 12:05

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than the 32Mbx16? 12:05

A. It's ordinarily what happens. 12:05

Q. And is 124Mbx4 initially cheaper than the 64Mbx8 and the 32Mbx16 initially then? 12:05

A. It depends on the exact details or the timing of when these parts get introduced versus when new operating systems get introduced. Sometimes it's cheaper, sometimes it's not. 12:05

Q. What's the cost difference between four 32Mbx16 versus two 64Mbx16 SDRAM device? 12:06

A. Again, it depends when. 12:06

Q. Let's just say in mass production. 12:06

A. Depends where they are in the cycle. 12:06

Sometimes Table 3 devices can be more expensive, especially early on in the cycle, and sometimes they can be less expensive. That's why they are both in the market is because it's hard to predict which is going to be more expensive in practice. 12:06

Q. So the 128Mbx8 device is not necessarily more expensive than the 64Mbx8 device; is that right? 12:06

A. Not -- you're saying per device or per unit of memory? 12:07

Q. Per device. 12:07

A. Not necessarily. But usually the 128x8 is going to be more expensive than the 64x8. 12:07

Q. What about per memory? 12:07

A. That will vary over time. 12:07

Q. How does it vary over time? 12:07

A. Based on yields, supply and demand, when the 128x8s are rare and hard to get, they can cost more than two 64Mbx8s. But as they become more mature and more common, they can get cheaper than two 64Mbx8s. 12:07

Q. So it really depends on the cycle? 12:07

A. Yes. 12:07

Q. So by 2004, 2005, do you have any sense as to which memory device would be cheaper per memory unit? 12:08

A. I don't recall the exact pricing from that time period. But I would expect that there would be examples on the market that would be commonly known where high-density memory was more expensive than using low-density memory for the same capacity. And there would be examples of the opposite as well. 12:08

Q. So when would you use, for example, four 32Mbx16 DRAM device on a -- on a module instead of two 64Mbx16 DRAM device? 12:09

A. There are two situations. One is if you 12:09

wanted to build a x64 module, then you would do that. The other example is when four 32Mbx16 chips is cheaper than two 64Mbx16 chips or more readily available, you might do it in that situation as well. 12:09

Q. And reason number one, you are assuming a x64 memory module as well as all four of the DRAM devices would be used in one rank; is that correct? 12:10

A. In that particular situation, yes. 12:10

Q. So what if you are using a x16 memory module width and you are trying to build a 2-gigabit memory -- let's take one step back. 12:10

Let's say that you are trying to build a memory module with x16 bit width. Do you get that? 12:11

A. Okay. 12:11

Q. Then each of the x16 device would need to be in its own rank by your definition, correct? 12:11

A. Yes, that would normally be what you would do. 12:11

Q. Okay. So in that situation, when would you be using a four 32Mbx16 device organized in supposedly four ranks versus two 64Mbx16 DRAM device organized in supposedly two ranks? 12:11

A. There would be a number of motivations to do it. One would be a pricing analysis. 12:11

Q. Okay. 12:12
A. Another would be a performance analysis 12:12
based on the fact that having more ranks will 12:12
typically allow you to have more pages open at a 12:12
time. Those would be the two primary things that 12:12
you would consider. 12:12
Q. What about power consumption? Would there 12:12
be any difference? 12:12
A. So the choice is two ranks -- or four 12:12
ranks of 32Mb versus two ranks. Yes, the four ranks 12:12
would have lower power consumption under typical use 12:12
conditions. 12:12
Q. Why is that? 12:12
A. Because the number of chips responding to 12:12
any individual command would be smaller. That would 12:12
be the primary reason. And the increased number of 12:12
available pages would be the other reason. 12:12
Q. What do you mean by the increased number 12:13
of available pages? 12:13
A. You have one page register per bank. So 12:13
in the case of four 32Mbx16, you would have 16 banks 12:13
of memory, with a "B," 16 bits wide, where in the 12:13
case of four 64Mbx8s arranged in two ranks, you 12:13
would have eight banks -- with a "B" -- with eight 12:13
page registers, each 16-bit wide. So that's a 12:13

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little bit lower performance in most situations and -- 12:13

(Simultaneous speakers.) 12:13

Q. Then -- 12:14

A. -- power -- 12:14

Q. Okay. Then would the 64Mbx8 and the 32Mbx16, would they have similar power consumption? 12:14

A. It depends what you mean by "similar." I think generally, in the configurations that we talked about in the last question, the 32Mbx16 would be the lower power option. But there are various trade-offs one has to look at depending on whether it's buffered or unbuffered and cost. 12:14

Q. When you say buffered and unbuffered, what do you mean? 12:14

A. You have to look at the actual loading on individual signal lines in an unbuffered device, and that may limit your options or it may limit the speed of some of your options. You have to look at the details. In a buffered device, that's less of an issue. 12:14

Q. When you say buffered, what buffer are you talking about? Data buffer? Control signal buffer? 12:15

A. Any -- any of those. You would have to analyze them all. 12:15

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Q. In Perego's case are there buffers? 12:15
A. Yes, in Perego's case I believe everything is buffered. 12:15
Q. And did you perform an analysis for that buffered DRAM as to the power consumption and the performance difference for -- for a memory module with four x8 device versus a memory module with four x30 -- x16 device? 12:15
A. No. That would be an ordinary engineering task. It would depend on the -- on the very detailed specifications of the individual devices that you were using, and it would be part of any engineering implementation to do that analysis. Not to see which one's better but just to make sure that both choices are viable. 12:16
Both choices would definitely be viable under certain conditions. You'd have to look at the conditions for your particular design. 12:16
And as I mentioned, there are fundamental principles that would indicate that the x16 simply involves fewer chips and has more banks, and therefore, would generally be preferable in terms of power consumption. 12:16
Q. So we're talking about 4x4 -- let me withdraw that. 12:17

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We're talking about four 32Mbx16 chip versus four 16Mbx8 chips, correct? 12:17

A. Correct. 12:17

Q. So they would have the same number of chips and banks? 12:17

A. No. I can see why that would be confusing. 12:17

The fact is, if you were to use the 64Mbx8 in a x16 configuration, you would have to use the chips in pairs for each access. So you would not get 16 banks. You would only get eight. 12:17

Q. But if you use 16Mbx16, that will be the same number of chips as when you used 32Mbx16; is that right? 12:18

A. 16Mbx16 versus 32Mbx16? 12:18

Q. No, 64Mbx16. So the last entry in Table 3. 12:18

A. It would be the same number of chips but different capacity, yes. 12:18

Q. Okay. So -- and there are more banks per chip for the 64Mbx16 than the 32Mbx16, correct? 12:18

A. In this generation, that was correct, yes. 12:18

Q. So wouldn't that mean the 64Mbx16, it would be -- actually consume less power per memory unit than the 32Mbx16? 12:18 12:19

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A. Ordinarily that would be the case, but you would have to look at the details. It would depend on -- it would depend on a lot of details. 12:19

Q. Okay. So ordinarily, if you use two 64Mbx16 memory module, it will consume less power than a memory module with four 32Mbx16 devices, assuming that the module bit width is 16. 12:19

Does that sound right? 12:19

A. Again, it depends on the details, but that would ordinarily be the case or most commonly be the case. The reason one would not do that is it might cost 10 times as much at certain points in the product cycle. 12:20

Q. Okay. But once they both get to the mass production phase, the memory cost would at least be comparable, if not cheaper, for the 64Mbx16; is that right? 12:20

A. At some point that usually happens, but it's not necessarily when they both meet -- hit mass production. Because it could be that still that the yields are lower. On the -- on the higher-density device, the tooling is more expensive. At some point, historically prices have always crossed over. But it's not always at the point where they both reach mass production. 12:20

Q. Okay. And do you know the price difference per memory unit in the 2004 and 2005 time period? 12:20 12:21 12:21

A. It would have varied week to week. 12:21

Q. But do you know what the general trend was? 12:21 12:21

A. No, not off the top of my head. 12:21

Q. And ordinarily would a memory module with two 64Mbx16 memory device perform better than a memory module with four 32Mbx16 device, assuming the bit width is x16 for the memory module? 12:21 12:21 12:21 12:21

A. In the majority of cases for these generations, I believe that it would. But again, it may be cost prohibitive. 12:21 12:21 12:21

Q. Okay. We've been talking about memory modules. What is your understanding of what a memory module is? 12:22 12:22 12:22

A. In the context of these patents, it's typically a printed circuit board that has one or more memory chips soldered on it along with potentially one or more supporting components. 12:22 12:22 12:22 12:22

Q. So if you have a PCI card with memory disposed on them, are they memory modules? 12:22 12:22

A. It depends on the time frame and the concept -- context. Certainly the PCI replaced the 12:22 12:22

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ISA bus. And in the early days of the ISA bus, there were certainly memory modules that went onto an ISA bus. 12:22

But by the 2004-2005 time frame, I think the intent, or the usage of that term in the '912 patent seems to be consistent with a memory module that was intended to go into a dedicated memory slot and not a general-purpose IO slot. 12:22 12:23 12:23 12:23

Q. Okay. So like by 2004-2005 time period, if a person of ordinary skill in the art at one time was talking about memory module, they are thinking about a printed circuit board that's going to be inserted into a memory slot rather than a general-purpose bus slot. 12:23 12:23 12:23 12:23 12:23

Does that sound right? 12:23

MR. CHANDLER: Objection. Form. 12:23

THE WITNESS: I think that would be the most common, but I think they would be familiar with both. 12:23 12:23

BY MS. ZHONG: 12:23

Q. I'm just asking you, when a person of ordinary skill in the art hear the word "memory module," what would they understand it to be? 12:24 12:24

A. I think they'd look for context. And in the context of the '912 patent, I think that they 12:24 12:24

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are looking for something that would go into a dedicated memory slot. But in another context, they may be looking for something broader. 12:24

Q. And in what context would they understand it to be something broader? 12:24

A. There are many historical systems I can think of. The VME bus computers. The IDE bus computers in which memory modules were commonly placed in general-purpose slots. Again, I think it just depends on what the context of the system is. 12:24

Q. And when you say VME bus computers, IDE bus computers, those were old computer systems predating -- before like 2000; is that correct? 12:25

A. They were predominantly before 2000. They were still in use in 2000, but they weren't popular. 12:25

Q. Would they have been phased out by the 2007-2008 time period? 12:25

A. I don't know. They wouldn't have been common on desktops, but they survived for a long time in -- in industrial applications. 12:25

Q. '912 deals with the concept of rank multiplication, correct? 12:26

A. It does. 12:26

Q. When is rank multiplication used? 12:26

Let me withdraw and reask. 12:26

When would a person of ordinary skill in the art apply the rank multiplication concept? 12:26

A. Whenever they had any reason to use a larger number of low-density memory devices instead of a smaller number of high-density devices, or in some cases where only the devices -- where there's not a distinction in terms of density but there's a distinction in terms of availability. 12:26

Q. When you say "availability," what availability? 12:27

A. In other words, if I have two kinds of memories that have the same density. And I could potentially use one without rank multiplication and one with rank multiplication. But the one that would be used without rank multiplication isn't available in the quantities that I need. Then I could use the rank multiplication instead. 12:27

Q. So for commodity SDRAMs, the second reason for availability is less of a concern; is that correct? 12:27

A. No. Historically commodity SDRAMs have been cyclical in terms of their price and availability. So there are periodic shortages. That's one of the things that has actually driven variations in memory module implementation. 12:27

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Q. And when would you use lower-density memory devices instead of high-density memory devices? 12:28

A. There could be a number of reasons. But primarily it's either because you get a lower cost per unit or you have improved availability. 12:28

Q. When you say "lower cost per unit," what's a unit, memory unit? 12:28

A. Yeah, unit of storage. 12:28

Q. And when wouldn't you use rank multiplication? 12:29

A. There's a number of considerations. If you wanted to use a small number of memory devices and that was your cheapest approach, that could be a reason not to use rank multiplication. 12:29

If you wanted to build a very simple device that had the smallest amount of additional logic on the DIMM, that could be motivation. 12:29

But again, usually the motivation is total cost per unit memory, which can change over time. So often in the late stages of a generation of memory devices, you can build a complete DIMM with one or two or four or eight devices in a single rank cheaply. And at that point, rank multiplication may not solve the problem for certain customers. 12:30

Q. But if you have -- but if there's only a single device per rank, would cost still be a consideration? 12:30 12:30 12:31

A. Could be. So, for example, if I'm -- if I'm making computers for 3rd graders and I can have them run the software using a one-rank, one-device memory system, that could be very cheap and effective. 12:31 12:31 12:31 12:31 12:31

Q. Why would you even have a memory module if there's only a single device per rank? Can't you just connect the DRAM directly to the memory system? 12:31 12:31 12:31

A. You can, but there are many reasons why you may not want to. One of those may be you want to repurpose the same computer system for different markets. So you may want to have a version with more memory that you sell to 6th graders than the one that you sell to 3rd graders. 12:31 12:31 12:32 12:32 12:32

Another version -- reason may be, as you said, memory tends to be a commodity so you don't want to commit to a particular chip at the time that you're making the boards. Instead, at the time that you sell the computer out the door, you want to purchase your memory on a module just in time since you don't have the carrying costs to that memory. 12:32 12:32 12:32 12:32 12:32 12:32

Those are some of the common reasons. 12:32

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MS. ZHONG: Do you want to take a lunch break right now?

THE WITNESS: We can do that.

MS. ZHONG: Do you want to take an hour?

MR. CHANDLER: That's fine.

(Whereupon a luncheon recess was had.)

(Off record: 12:33 p.m.)

(On record: 1:30 p.m.)

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1:30 p.m. 01:30

01:30

MS. ZHONG: We can go back on the record. 01:30

EXAMINATION (resumed) 01:30

BY MS. ZHONG: 01:31

Q. Dr. Wolfe, can you pull up Exhibit 1004 {sic}, which is U.S. Provisional Application 60/588244. 01:31

(Exhibit 1005 was marked for identification and attached hereto.) 01:31

BY MS. ZHONG: 01:31

Q. Do you have that document? 01:31

A. Give me the exhibit again. 01:31

Q. Exhibit 1005. Exhibit 1005. 01:31

MR. CHANDLER: Can we pause for a moment? My colleague got kicked out from the Zoom and he's coming back in. 01:31

MS. ZHONG: So let's go off the record while waiting for him then. 01:31

(Brief pause in proceedings.) 01:31

BY MS. ZHONG: 01:32

Q. Do you have Exhibit 1005, Dr. Wolfe? 01:32

A. Yes. 01:32

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Q. You are familiar with this document, correct? 01:32
A. Yes. 01:32
Q. Can you please take a look at paragraph 10 through 19. 01:32
A. Okay. 01:32
Q. Do you see there's a Table 1 in paragraph 11? 01:33
A. Yes. 01:33
Q. In Table 1, follows 2, 3, 4 and 5 have the headings CS0, CS1, An+1 and Control. 01:33
Do you see that? 01:33
A. I do. 01:33
Q. Are those input signals received from the memory system in order to select the rank? 01:33
A. A subset of them are in some cases. 01:34
Q. Are those the signals that's received by the ASIC depicted in Figure 1? 01:34
A. They appear to be with the distinction that in Table 1 there's only a single control signal. And in the text it explains that only a single control signal is required. 01:34
Q. What do you mean by only a single control signal is required? 01:34
A. Let me see if I can find that. 01:35

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Paragraph 10, it says at least one control signal. 01:35

Q. Okay. If you look at paragraph 11, note 4, that describes what the control in Table 1 refers to; is that correct? 01:35

A. Yes. 01:35

Q. Okay. So in Table 1, the control refers to a number of control signals that define operations such as refresh, precharge, and other operations, correct? 01:35

A. That is what note 4 says. 01:35

Q. And what would those control signals be if the DRAM is JEDEC compliant on the DRAM -- 01:35

THE REPORTER: I'm sorry. "If the DRAM is"... 01:36

BY MS. ZHONG: 01:36

Q. And what would those control signals be if the DRAM is a JEDEC compliant DRAM device? 01:36

A. Well, there are many different kinds of JEDEC compliant DRAM devices, but a typical example could be RAS, CAS, and write enable. 01:36

Q. Does it need to have chip select signal? 01:36

A. No, because the chip select signals are separately defined CS0 and CS1. 01:37

Q. Okay. And for read and write operation, 01:37

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does it also need to -- does bank address information also need to be provided? 01:37

A. Again, there's nothing that needs to be provided other than something that performs the function. But I would not expect bank address to be provided. I don't -- I'm not aware right now of a situation where bank address defines operation such as refresh and precharge. 01:37

Q. So you mean -- what about a read and a write? 01:37

A. What about them? 01:37

Q. So are read and write operation, do bank addresses need to be provided in order to define the operation? 01:38

A. They may need to be provided to the memory chip in order to identify where the operation should take place, but they don't need to be provided to the ASIC decoder that's shown in Figure 1. 01:38

Q. The ASIC decoder says the control involves control signals that define operations, correct? 01:38

A. No, that's what Table 1 says. 01:38

Q. And paragraph 19 says, "The 'Control' column of Table 1 represents the various commands that a DRAM device can execute, examples of which include, but are not limited to, activation, read, 01:38

write, precharge, and refresh," correct? 01:39

A. Correct. 01:39

Q. And we discussed earlier that for a JEDEC compliant SDRAM, the command for a read and write operation and activation would include bank address signals, correct? 01:39

A. We're talking about different things here. 01:39

So, one -- there's nothing in Figure 1 that indicates that that's a JEDEC compliant DRAM. But even so, the discussions we had before were about what the DIMM module would receive, not what an ASIC decoder on a DIMM module would receive. And those are two different issues. 01:39

Q. Okay. I'm just asking the control information of the command signals that a DRAM -- let me withdraw and ask. 01:39

The commands that a DRAM device can execute includes a read operation command, correct? 01:40

A. It would depend what kind of DRAM device. But that would be true for most DRAM devices is that there's some type of a read operation. 01:40

Q. Okay. So let's say, since you are only citing the JEDEC compliant DRAM devices, for those DRAM devices, the commands for a read and write operation includes bank address information, 01:40

correct? 01:40

A. Let's be clear. I'm not only citing JEDEC 01:40

compliant DRAM devices. And where I do cite them, 01:40

it's to illustrate the obviousness issues with 01:41

respect to particular references. The -- I would 01:41

not rely on the JEDEC compliant DRAM specification 01:41

as a way to understand what's disclosed in 01:41

Exhibit 1005. 01:41

Q. The DRAMs in Exhibit 1005 are to be used 01:41

with a general personal computer, correct? 01:41

A. Yes. 01:41

Q. And we agree that a JEDEC compliant DDR or 01:41

DDR2 DRAM device in order to execute -- let's 01:42

withdraw -- let me withdraw and reask. 01:42

So the commands are for a read operation 01:42

for a DRAM device that is compliant with JEDEC 01:42

standard would include bank address information; is 01:42

that correct? 01:42

A. As I said, there are many, many JEDEC 01:42

standards. I can't generalize about all of them. 01:42

Q. Okay. The JEDEC standards you cited. 01:42

A. I would not consider the bank addresses to 01:42

be part of the command, no. They are supplied along 01:42

with a command, but in the -- for example, 01:42

Exhibit 1029, when I look at a command like the bank 01:43

activate command, the bank activate command is issued by holding CAS bar and write enable bar high with chip select bar and RAS bar low at the rising edge of the clock. 01:43

Q. And bank address signal is supplied with those commands in order to execute the bank activation? 01:43

A. It is supplied to the DRAM chip along with the command. It is neither part of the command nor is it something that necessarily would go through a separate logic circuit. 01:43

Q. Okay. And I think you mentioned earlier that it is not necessary for the larger component to actually receive the bank address signal. All it requires for a JEDEC compliant SDRAM is for the DRAM itself to receive the bank address; is that correct? 01:44

A. In order to use a DRAM chip such as the kind that's described in Exhibit 1029, that is correct. 01:44

Q. Okay. So the bank address signal need not be received by a larger element? 01:44

A. Not in every utilization of a DDR2 device, no. 01:44

Q. Okay. And so is there anything in Perego actually mentions the bank address signal being 01:45

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passed to the buffer address -- buffer device? 01:45
A. I believe all the signals that are 01:45
communicated in Perego from the host are passed 01:45
through buffer devices. 01:45
Q. Does Perego actually mention a bank 01:45
address in particular? 01:45
A. It mentions memories that have banks. And 01:45
it mentions specific memory types like DDR that 01:46
would -- a person of ordinary skill would understand 01:46
has a bank address. 01:46
Q. So if you mention DDR or DDR2, does that 01:46
necessarily mean a JEDEC compliant DDR or the DDR2 01:46
device? 01:46
A. No, not always. But it would certainly 01:46
cause a person of ordinary skill to find the use of 01:46
one obvious. 01:46
Q. So in Figure number 1, how would the bank 01:47
-- (indiscernible.) 01:47
THE REPORTER: I'm sorry, Counsel. 01:47
Counsel, can you speak more to your right? We're 01:47
losing you. Thank you. 01:47
BY MS. ZHONG: 01:47
Q. So in Figure number 1, if the DRAM device 01:47
is a DDR or DDR2 JEDEC compliant device, how would 01:47
the bank address information be provided to that 01:47

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DRAM device? 01:47

A. Figure 1 of Perego? 01:47

Q. No, Figure 4, Exhibit 1005. 01:48

A. So, again, there's no mention of JEDEC standard devices. But if one were to choose to implement Figure 1 of 1005 with DDR2 JEDEC compliant devices like in Exhibit 1029, they would have to consult Exhibit 1029 to figure out how to connect them up. 01:48

And presumably they would simply take the bank address signals directly from the host bus and connect them directly to each memory device. That would certainly be the simplest way to implement it. 01:48

Q. Would the bank address information be required to operate a JEDEC compliant DDR or DDR2 device? 01:49

A. I don't know that I could look -- I'd have to think about it. 01:50

No, I mean, it's not required in all circumstances. But if one were to build an ordinary PC memory module, one would -- typically at that time, the simplest thing to do would be to connect the bank address signals directly from each memory device to the host computer memory controller. 01:50

Q. Even when you have a register? 01:50

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A. Well, it depends why you have a register. 01:50
In this particular case, the register is quite 01:50
limited and is only used for a subset of address 01:50
signals. 01:50
Q. What about on the -- (indiscernible.) 01:50
THE REPORTER: I'm sorry? 01:51
THE WITNESS: What about on the what? 01:51
BY MS. ZHONG: 01:51
Q. On the (indiscernible) -- 01:51
THE REPORTER: I don't -- 01:51
MS. ZHONG: It's on Exhibit 1032. 01:51
MR. CHANDLER: Are you saying registered 01:51
DIMM, the letter R DIMM? 01:51
MS. ZHONG: Yes. 01:51
MR. CHANDLER: Okay. 01:51
THE WITNESS: And what's the question 01:51
about the registered DIMM? 01:51
BY MS. ZHONG: 01:51
Q. Okay. So for the DIMM that's described in 01:51
Exhibit 1032 -- 01:51
A. Yes. 01:51
Q. -- where are the advance signals sent? 01:51
A. In the DIMMs that are described in 01:51
Exhibit 1032, the bank signals from the host 01:51
computer are registered. And then the registered 01:51

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copies of those signals are sent to each of the SDRAM chips. 01:52

Q. For the registered DIMM shown in Exhibit 1032, does that register have any logic function? 01:52

A. Not in the way I would normally use that term, no. It's simply register. 01:52

Q. How would you use -- what's your definition of a logic element? 01:52

A. Well, again, it depends on context. But in the context of something like the '912 patent or Exhibit 1005, I would think that a logic element performs logic functions by combining multiple signals for the purpose of incorporating a logic equation and not simply delaying a signal. 01:52 01:53

Q. Okay. And what is sequential logic? 01:53

A. What is sequential logic? 01:53

Q. Yes. 01:53

A. Sequential logic -- again, you have to look at the context. Normally it describes a combination of logic functions and registers. 01:53

Q. What do you mean by "It describes a combination of logic functions and registers"? 01:53

A. I don't know how to simplify this down to a single statement. It takes us hours or days to 01:53

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explain it to students. 01:54

But sequential logic implements what we 01:54

call state machines, which are time-variant logic 01:54

functions that can perform different logic equations 01:54

at different points in time based on the storage of 01:54

what we call state partial results. 01:54

Q. Okay. So in order to implement a 01:54

sequential logic, normally you would need to have 01:54

both electrical elements that execute the logic 01:54

function and also storage elements that store the 01:54

state of the device? 01:54

Does that sound correct? 01:54

A. It would normally -- 01:54

MR. CHANDLER: Objection. Form. Also 01:54

incomplete hypothetical. 01:54

THE WITNESS: Generally, to perform a 01:55

sequential logic function the way that I've defined 01:55

it, you would need both state storage in the form of 01:55

a register or an equivalent, plus some what we call 01:55

combinational logic functions. 01:55

That doesn't mean that the same signals 01:55

are provided to both, or it doesn't mean that they 01:55

work in any particular way, but they would both 01:55

somehow be present. 01:55

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BY MS. ZHONG: 01:55

Q. Okay. What is combinatorial logic? 01:55

A. Combinatorial logic is logic that does not store results, basically. 01:55

Q. So basically it's -- it generally only refers to the logic operation without the storage unit? 01:55

A. Correct. Generally, a change in input would be reflected as a change in output and a clock is not required. 01:55

Again, you know, it gets more complicated than that when you dig into the details, but that's kind of a -- a very high-level overview. 01:56

Q. Okay. Is that something a POSITA would have understood in 2004 and 2005 as to what sequential logic and combinatorial logic is? 01:56

A. They would have understood the textbook definitions, yes. 01:56

Q. You said that the -- why don't you pull up Exhibit 1009, the patent ending with '436. 01:56

A. Okay. 01:57

(Exhibit 1009 was previously marked for identification and attached hereto.) 01:57

BY MS. ZHONG: 01:57

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Q. Is it your opinion that '436 patent does not describe the solution for the back-to-back adjacent reads with cross memory device boundary? 01:57

A. It does not. 01:57

Q. And what is a back-to-back adjacent read command issue that we're talking about? 01:58

A. That when commonly available protocols at the time, such as the DDR and DDR2 protocols, were used together with a very simple rank multiplication scheme, there was a problem when a read command went to one rank and a subsequent read command went to another rank in that certain signals were driven for a longer time period than it would take to simply respond or to simply provide the data in response; that there were preambles and postambles in the response signals. 01:58

And if one simply connected up two ranks to be sequentially accessed, those signals could conflict with each other. And some mechanism had to be introduced in order to distinguish those signals or to block one of those signals so that there would be no interference. 01:59

Q. So it's -- is it essentially a DQS bus conflict situation then? 01:59

A. Did you say d2s? 01:59

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Q. DQS, Q as in quiet. 01:59
A. Let me look at the actual signal name there, yes. 01:59
That's -- that's the -- the significant one. There's DQS and DQS bar in some generations. And that's where the preamble and postambles would exist. 01:59 02:00
And one of them -- either the timing needs to be adjusted between the two ranks or one of those DQS response signals to a read needs to be blocked or they need to be combined. 02:00
Q. Okay. So basically we're talking about a DQS bus conflict situation, how to resolve it? 02:00
A. That's the most common situation that would come up, yes. 02:00
Q. Okay. Let's see. 02:00
Can you pull up Exhibit 1030, page 19. 02:00
A. Yes. 02:01
Q. And you reference the Figure 8 in your discussion of the read -- the back-to-back read situation. 02:01
Is Figure 8 depicting a back-to-back read that's across rank boundaries? 02:01
A. So the -- the -- the simplest interpretation of Figure 8 is that it represents 02:01

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burst read operation to a single device. However, if one were to implement a system in which two ranks are made to appear as if they are one larger device, then this same protocol would be used across ranks but in a way that would not operate properly unless some accommodations were made. 02:01 02:01 02:02 02:02 02:02 02:02

Q. But it says -- on Figure 8 it says, "Read commands shown must be to the same device," correct? 02:02 02:02

A. It does. And the reason that that's still apropos in a system that uses rank multiplication is that the host believes that the read command is going to the same device and, therefore, expects to use this protocol, when in fact the actual read commands would be duplicated as part of the rank multiplication and, therefore, go to separate devices. That's what causes the conflict that must be resolved. 02:02 02:02 02:02 02:02 02:02 02:02 02:02 02:03 02:03

Q. And so your interpretation of the same device refers to the device in the same rank; is that correct? 02:03 02:03 02:03

MR. CHANDLER: Objection. Form. 02:03

THE WITNESS: No. When it says "same device" on page 19, it means that this protocol is intended to support back-to-back reads on the same device. However, as I mentioned -- 02:03 02:03 02:03 02:03

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BY MS. ZHONG: 02:03

Q. When the -- 02:03

A. -- already, if the host believes that two ranks are in fact the same device, then this protocol would be expected by the host as well. 02:03

Q. When you say "the same device," are you referring to a single D rank or a rank of D rank devices? 02:03

A. In practice, it would be a rank. 02:04

Q. Okay. And so for the back-to-back read conflict that you were discussing, if there are ways to resolve DQS bus conflict situation, then that problem would be solved; is that correct? 02:04

A. It is a solvable problem, but additional mechanisms need to be added to the very simplest rank multiplication schemes. 02:04

Q. Okay. So if there are schemes to solve the bus -- DQS bus conflict problem, then it's not an issue, correct? 02:04

A. If you incorporate a mechanism to solve the problem, then it is no longer a problem. 02:05

Q. And the problem is a DQS bus conflict problem, correct? 02:05

A. That would be the problem that I would be most concerned about is the DQS or DQS bar bus 02:05

conflict. 02:05

Q. Okay. Can you also pull up Exhibit 1029? 02:05

A. Yes. 02:05

Q. Page 28 or 29? Page -- which is the one 02:05

cited for the back-to-back read. Give me a second. 02:05

So on page -- can you go to page 28 and 02:06

29. 02:06

A. Okay. 02:06

Q. And do you see Figure 27 -- 02:06

A. Yes. 02:06

Q. -- on page 28? 02:06

Right above the caption it says, "This 02:06

operation is allowed regardless of same or different 02:06

banks as long as the banks are activated." 02:06

Do you see that? 02:06

A. Yes. 02:06

Q. And the banks here refer to the internal 02:06

independent memory arrays in the DRAM device and not 02:06

a rank; is that correct? 02:06

A. I don't recall whether or not ranks are 02:07

excluded here. It certainly covers -- let's see. 02:07

Burst -- back-to-back bursts. 02:07

Q. So my question is more what does bank mean 02:08

here? Does it mean the bank that we discussed this 02:08

morning referring to the internal device 02:08

organization or it refers to rank? 02:08
A. It refers to the internal device 02:08
organization. But I would have to do some more 02:08
research to determine whether or not this particular 02:08
diagram -- this particular sequence requires that 02:08
the banks be in the same chip. 02:08
Q. So by 2000 -- by the time of Exhibit 1029, 02:08
generally banks in a JEDEC document refers to the 02:08
internal bank organization; is that correct? 02:08
MR. CHANDLER: Objection. Form. 02:08
THE WITNESS: I haven't looked at all the 02:08
documents, but certainly in at least some cases they 02:08
did. 02:09
BY MS. ZHONG: 02:09
Q. You are familiar with this document, 02:09
correct? 02:09
A. I am. 02:09
Q. So what's the use of a bank in this 02:09
document? What is it referring to? 02:09
A. Give me a minute to look it over. 02:09
I'm sorry, I'm having some trouble with 02:10
the viewer here. Give me just a second. 02:10
Looking at 1029? 02:10
Q. Correct. 02:10
A. Certainly that language transition had 02:10

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started by this point. I don't recall whether or not it's a 100 percent consistent throughout the document. 02:10

Q. When it talks about bank address inputs, is it talking about the internal memory array organization within a device? 02:10

A. In 1029 it is, because it's usually talking about a specific device. 02:10

Q. And when it talks about bank activation or writing to the same bank, that also refers to the bank within the same device; is that right? 02:11

A. It refers to a bank within a device. Depends on the context as to whether or not it's the same device. 02:11

Q. It's not referring to the bank in that context? 02:11

A. No. It's referring to a specific bank. But depending on context, that bank may also be in a different rank. 02:11

Q. In Figure 27 on page 28, when it says the banks are activated, that would be referring to the internal organization of a memory device; is that right? 02:11

MR. CHANDLER: Object to form. 02:12

THE WITNESS: In Figure 27 when it says 02:12

"banks are activated," that means that an individual memory array within one or more memory devices has been -- has been activated. 02:12

BY MS. ZHONG: 02:12

Q. Can you pull up Exhibit 1007, which is a provisional application ending with 59- -- actually, pull up Exhibit 1006, provisional application ending with 668. 02:13

(Exhibit 1006 was marked for identification and attached hereto.) 02:13

THE WITNESS: Okay. 02:13

BY MS. ZHONG: 02:13

Q. Can you please go to Figures 1 and 2? 02:13

A. Okay. 02:13

Q. What is -- what is depicted in Figures 1 and 2? 02:13

A. Figure 1 schematically illustrates a configuration in which a DQS pin of a first device is connected to a DQS pin of a second device. 02:14

Figure 2 is a timing diagram of the voltages applied to the two DQS pins due to nonsimultaneous switching. 02:14

Q. Okay. So that is one situation where there can be DQS bus conflict, correct? 02:14

A. Well, the conflict would be where you have simultaneous switching. 02:14

Q. So, for example, if one DQS is driven high while the other is driving -- driven low and there's some overlap in those time periods, that could be a problem? 02:14 02:15 02:15 02:15

A. It could. You could end up with -- 02:15

Q. That -- go ahead. 02:15

A. Yes, you could end up with an indeterminate value. 02:15 02:15

Q. And that could also cause a DQS burn, bus burn, situation? 02:15 02:15

A. DQS bus? 02:15

Q. Basically like a DQS bus conflict situation. 02:15 02:15

A. Yes, it could be a conflict. 02:15

Q. And can you take a look at Figures 3 and 4 of the '668. 02:15 02:15

A. Yes. 02:16

Q. Okay. So shown in Figure 4, is that a solution to address the potential DQS bus conflict by using current-limiting resistors? 02:16 02:16 02:16

A. My understanding is that it could prevent permanent damage to the device, but it would not ensure operation in the back-to-back read situation 02:16 02:16 02:16

that was of concern. 02:16

Q. So the solution would prevent damage to 02:17
the DQS bus, correct? 02:17

A. I haven't done analysis to figure out 02:17
whether or not it's effective, but that's what it's 02:17
purported to do, and it's quite plausible that it 02:17
would do that. 02:17

Q. Okay. But you say it would not ensure 02:17
operation in the back-to-back read situation. So 02:17
what do you mean by that? 02:17

A. In the situation that I describe in my 02:17
declaration where a burst is -- involves one rank, 02:17
and immediately a subsequent burst goes to a second 02:17
rank, there would still be a signal conflict in 02:17
which the value of the signal, the voltage of the 02:17
signal, would not be at an appropriate level for 02:17
proper operation. 02:17

Q. And in Figures 1 and 2, if one DQS is 02:18
driven high while the other is driven low at the 02:18
same time, that would also cause a similar situation 02:18
as in the back-to-back read scenario you're 02:18
concerned with, correct? 02:18

A. There would be similarities and 02:18
differences. The similarity would be that there 02:18
would be an electrical conflict. The difference is 02:18

that in this situation there's no explanation that it's important to maintain the pulse timing and to not have out of spec voltages on the line. 02:18 02:18 02:18

So there are physical similarities but there are operational differences. 02:18 02:19

Q. So the main difference is more a timing issue? So for Figures 1 and 2, timing is less of a concern, while for the back-to-back read operation the timing of the DQS pulses are more important? 02:19 02:19 02:19 02:19

Is that what you're saying? 02:19

A. Somebody might describe it that way. Or it might also be useful to describe it as in the Exhibit 1006, the presence of an intermediate voltage is not important at the time that it occurs, where in rank multiplication using DDR or DDR2 DIMMs an intermediate voltage as would occur in Exhibit 1006 is unacceptable. 02:19 02:19 02:19 02:19 02:19 02:19 02:20

Q. Okay. So it is more a signaling level issue at the particular time; is that correct? 02:20 02:20

A. It is a signaling level at a particular time. 02:20 02:20

Now, there is also a concern about physical damage, but 1006 mitigates the physical damage issue. 02:20 02:20

Q. Okay. So 1006 does involve the physical 02:20

damages issue? 02:20

A. It appears to. It appears to, but it does not maintain proper operation. 02:20

Q. Okay. So the concern now is whether the proper voltage level is provided at the right time in order for you to have the right alignment between the DQS and DQ. Does that sound correct? 02:20

A. That is generally the problem, yes. 02:21

Q. Dr. Wolfe, can you please refresh your Exhibit Share and see whether you see an Exhibit 2101. And that is Provisional Application 60/590038. 02:21

(Exhibit 2101 was marked for identification and attached hereto.) 02:22

THE WITNESS: Okay. I have that. 02:22

BY MS. ZHONG: 02:22

Q. Can you open it? 02:22

A. I did. 02:22

Q. Okay. Can you please take a look at Figures 1 and 2 of this exhibit, Exhibit 2101? 02:22

MR. CHANDLER: And let me just lodge an objection as to relevance. I don't think we've seen this exhibit. And perhaps you can explain the relevance to anything that was in Dr. Wolfe's direct 02:22

testimony or the '912 patent. But I'm not sure it's relevant. 02:22

MS. ZHONG: You don't think -- you don't think the priority document 4436 is relevant? 02:22

MR. CHANDLER: Well, that's -- I apologize. I haven't memorized all the provisional application numbers. So it would be helpful to tie this provisional to whatever it was we were talking about. 02:23

BY MS. ZHONG: 02:23

Q. Dr. Wolfe, can you please take a look at Figures 1 and 2 of this document? 02:23

A. I see them. 02:23

MR. CHANDLER: And so then I'll just go on with the objection. 02:23

I mean, if it's not tied to something in his report, I'd object to outside the scope. And also we'd have issues of authenticity and hearsay. 02:23

MS. ZHONG: You can object to the board and see what the board says. 02:23

Q. So for these two Figures 1 and 2, does -- do Figures 1 and 2 also offer solutions to the DQS bus conflict issue? 02:23

A. I haven't really spent time studying that aspect of this. I'm not sure if I've seen this 02:24

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before. 02:24

Q. Okay. 02:24

A. They appear to deal with issues related to termination impedence, which would be a different problem than the one that I was talking about before. 02:24

Q. Okay. But it would at least prevent damages to the device, correct? 02:24

A. Not necessarily. I think it's supposed to impact signal reflections. 02:24

Q. What do you mean by signal reflections? 02:24

A. High-speed signals can have what are called termination networks to prevent the signal from reflecting, from bouncing back when it gets to the end of a wire. And that seems to be the subject matter here. 02:25

Q. And what's the problem associated with signal bouncing? 02:25

A. There can be numerous problems. But the primary one is that it would inject noise into the signal, which would cause erroneous data to be communicated. 02:25

The paragraph -- 02:25

Q. Okay. 02:25

A. -- at the end talks about the signal 02:25

reflection problem. 02:25

Q. Okay. So basically one issue associated 02:25

with signal reflection is incorrect voltage levels 02:25

would show up and, therefore, cause data errors; is 02:25

that correct? 02:26

A. Yes. If you have an improperly terminated 02:26

high-speed signal, the reflections can cause 02:26

transient voltage deviations, which could cause data 02:26

communication errors. 02:26

Q. Do you have any evidence that the solution 02:26

offered here would not work with remedial of the 02:26

signal reflection errors that we just discussed? 02:26

A. I don't know one way or another. It's a 02:26

quantitative analysis and I haven't done it. 02:26

Q. And you have not considered this document 02:26

in particular; fair? 02:26

A. I did not consider this document, as far 02:27

as I can recall. It does not seem to deal with the 02:27

issues related to my declaration. 02:27

Q. Okay. Can you please take a look at the 02:27

'436 patent, and the cover page in particular. 02:27

A. That's Exhibit 1009? 02:27

Q. Correct. Exhibit 1009, cover page. 02:27

A. Yes. 02:27

Q. And '436 claimed priority to Provisional 02:27

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Application 60/590038, correct? 02:27

A. Correct. 02:27

Q. And that is Exhibit Number 2101, correct? 02:28

MR. CHANDLER: Objection. Lack of foundation. 02:28

THE WITNESS: I don't know how to find the provisional number on Exhibit 2101. 02:28

BY MS. ZHONG: 02:28

Q. So I direct your attention to the cover page of Exhibit 2101. Are you there? 02:28

A. Yes. 02:28

Q. Do you see barcode on the right -- top right-hand corner? 02:28

A. Yes. 02:28

Q. And do you see next to the barcode there is a series of numbers, 60/590038? 02:28

A. I see that. 02:29

Q. That number matches up with the number that's beside it on the cover page of the '436 patent, correct? 02:29

A. It does. 02:29

Q. Okay. And if you can go to column 1 of the '436 patent. 02:29

A. Okay. 02:29

Q. In the field with the title "Claim of 02:29

Priority," it says that this particular provisional application 6590038 is incorporated in its entirety by reference herein, correct? 02:29

A. It does. 02:29

Q. So the description in 6590038 is part of the '436 patent? 02:29

A. I'm not an attorney, but that would be my understanding. 02:30

MS. ZHONG: Let's take a 10-minute break. 02:30

MR. CHANDLER: Okay. 02:30

(Recess.) 02:30

(Off record: 2:31 p.m.) 02:30

(On record: 2:46 p.m.) 02:30

BY MS. ZHONG: 02:30

Q. Dr. Wolfe, do you have Exhibit 1009, the '436 patent, with you? 02:46

A. Yes. 02:46

Q. Can you please go to PDF page 13, Figure 11A and 11B. 02:46

A. Yes. 02:46

Q. So 11A depicts to a person of ordinary skill in the art a situation called rent multiplication? 02:46

MR. CHANDLER: Objection to form. 02:47

THE WITNESS: I think -- I think a person 02:47

of ordinary skill in the art might characterize that as rank multiplication, yes. 02:47

BY MS. ZHONG: 02:47

Q. And if take a look at Exhibit 11B {sic}, do you see that on the right-hand side, there are four signals: CAS0a, CAS0b, CAS1a, and -- 02:47

THE REPORTER: I'm sorry, Counsel, you were cut off. 02:47

BY MS. ZHONG: 02:47

Q. -- four signals: CAS0a, CAS0b, CAS1a, and CAS1b? Do you see that, Dr. Wolfe? 02:47

A. Yes. 02:47

Q. Those are the four chip select signals for each of the ranks depicted in Figure 11A; is that correct? 02:47

MR. CHANDLER: Objection. Form. 02:48

BY MS. ZHONG: 02:48

Q. Dr. Wolfe? 02:48

A. Yeah, I'm looking at some details to give you a precise answer. 02:48

There's an example given with respect to Figure 11A in which that can be a four-rank system. And in that case, in that one particular example that's related to Figure 11A, then the four CAS signals coming out of element 640 would represent 02:48 02:48 02:49 02:49

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select signals for each of the four ranks. 02:49

Q. Okay. And the four CAS signals that's coming out of 640 are based on input signals to the left of the box 640; is that correct? 02:49

A. It's based on a subset of those input signals. It's not completely clear what. But the suggestion would be that, for example, it might be similar to what's in Figure 10 where it's only the address signal that actually participates. 02:50

Q. The input signal to 640 includes BNK0, BNK1, RAS/CAS/WE, CS0, CS1 and A13; is that correct? 02:50

MR. CHANDLER: Objection. Form. 02:50

THE WITNESS: Those are all connected to 640. There's no description as to whether or not they are actually used by 640. 02:50

BY MS. ZHONG: 02:50

Q. So the signals I just listed, BNK0, BNK1, RAS/CAS/WE, CS0, CS1 and A13, are all input signals to 640, correct? 02:50

MR. CHANDLER: Object. Form. 02:51

THE WITNESS: Again, it depends how you define an input signal. They're all connected to 640, but there's no teaching as to whether or not they're used as inputs. 02:51

BY MS. ZHONG: 02:51

Q. And the output from 640 are the four CAS signals on the left, correct? On the right, sorry. 02:51

So the output from 640 are the four CAS signals on the right, correct? 02:51

A. Correct. 02:51

Q. What is A13? 02:51

A. What is A13? Is that the question? 02:51

Q. Yes. 02:51

A. I believe it's one of the address bits. 02:51

Q. So it's either a row or a column that addresses it? 02:52

MR. CHANDLER: Objection. Form. 02:52

And I didn't hear the question at the beginning. 02:52

BY MS. ZHONG: 02:52

Q. It is either a row or a column address it? Is that correct, Dr. Wolfe? 02:52

A. Yes, or depending on the particular DRAM generation. It could be both. 02:52

Q. So it is a row, column, or both a row and column address it? 02:52

A. That would be my understanding of what's intended. 02:52

Q. And what is CS0 and CS1? 02:52

A. Those would be DIMM level chip selects. 02:53

Q. And BNK1 and BNK0? 02:53
A. Those appear to be the pass-through bank selects to -- to the individual DRAM chips. 02:53
I need to -- I need to clarify my previous answer. 02:53
So the outputs are not actually chip selects. They are gated column address select signals. 02:53
Q. Okay. But they are sent to each of the corresponding memory mod- -- corresponding rank; is that correct? 02:53
A. Correct, as gated column address signals. The chip selects are separate. They are shown up in Figure 11A. 02:53
Q. So if you look at column 17, starting from line 66 to column 18, line 2, the enabled CAS signal that's being outputted from 640 is able to select which of the four ranks, 620, 625, 630 and 635, as active; is that correct? 02:54
A. Yes, in that embodiment for certain operations, that's true. 02:55
Q. Okay. So basically it is used -- it has a similar function as a chip select signal, which is to decide which of the rank will be activated and chosen; is that correct? 02:55

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MR. CHANDLER: Objection. 02:55

THE WITNESS: Not really. A chip select 02:55
signal determines whether or not to pay attention to 02:55
the command in a DDR environment. So it has a -- it 02:56
has a different scope. And that's why the chip 02:56
select signals are also provided to the various 02:56
ranks. 02:56

BY MS. ZHONG: 02:56

Q. And if you look at column 18, lines 3 02:56
through 11, it says that the PLD 642 can also 02:56
generate gated chip select signals instead of gated 02:56
CAS signals; is that correct? 02:57

A. It does say that. 02:57

Q. What is your understanding of what a rank 02:57
is? 02:57

A. In what context? 02:57

Q. A rank of memory module -- sorry. Let me 02:58
withdraw. 02:58

In the context of a '912, what is a rank? 02:58

A. I think it would be an independent set of 02:58
one or more memory devices on a memory module that 02:58
act together in response to command signals, 02:58
including chip select signals, to read or write the 02:58
full bit width of the memory module. 02:58

Q. Okay. How can a single memory device act 02:58

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together? 02:58

A. It acts consistently. 02:58

Again, that's just an artifact of English 02:58
when we say one or more. If I -- you know, just 02:58
like if I said one or more children jumping up and 02:58
down together, that would make sense in English even 02:58
though if it's one, they are just jumping up and 02:59
down. 02:59

So the word "together," I guess, is only 02:59
important if there's more than one. But -- but if 02:59
there's one, then it simply needs to act. 02:59

Q. You mentioned earlier that there are x8 02:59
memory modules. Do you recall that testimony? 02:59

A. I do. 02:59

Q. Are those DDR memory modules? 02:59

A. The ones that I'm thinking of are not DDR, 02:59
but I don't know of any reason why you can't build a 02:59
x8 DDR memory module. 02:59

Q. For JEDEC compliant memory modules, are 02:59
you aware of any x8 DDR memory modules? 03:00

A. Well, it certainly would be compliant with 03:00
Exhibit 1029. I don't know whether or not there's a 03:00
form factor definition for a DDR2x8 memory module. 03:00

Q. Are you aware of any x8 DDR2 memory 03:00
modules that's JEDEC compliant, JEDEC standard 03:00

compliant? 03:00

A. Like I said, they would be standard with 03:00
certain JEDEC protocols like 79-2. But I don't know 03:00
whether or not there's a separate JEDEC protocol for 03:00
the form factor of a x8 DDR2 memory module. 03:00

Q. When you say a form factor x8, what do you 03:00
mean? 03:00

A. Well, when you have a specification in 03:00
JEDEC for a memory module, there's portions that 03:01
describe how it should operate. And then there's 03:01
other portions that describe its physical 03:01
characteristics. 03:01

If we were to look, for example, at 03:01
Exhibit 1032, large portions of that specification 03:01
have to do with physical characteristics: The 03:01
dimensions of the card, the placement of the chips, 03:01
the physical order of the pins. 03:01

And I just don't know one way or another 03:01
whether or not that specification exists for the 03:01
combination of -- of x8 memory module and DDR2. But 03:01
I certainly know that based on Exhibit 1029, 03:01
somebody could build a DDR2 8-bit-wide memory 03:01
module. 03:01

Q. I'm asking a different question. 03:02

Are you aware of any JEDEC memory module 03:02

standards that specify a x8 or x16 memory module? 03:02

A. I don't think that that's a simple 03:02

question. There are many JEDEC standards. I am 03:02

aware of standards like Exhibit 1029 that would tell 03:02

you the operational characteristics, many of the 03:02

operational characteristics, of a x16 or x8 memory 03:02

module for DDR2. 03:02

I do not know whether or not the remaining 03:02

characteristics, such as the physical dimensions or 03:02

the power consumption specifications, are part of 03:02

another JEDEC specification or not. 03:02

Q. So you did not cite any single JEDEC 03:03

specification or document that showed the use of a 03:03

x8 DDR or DDR2 memory module; is that correct? 03:03

Other than Perego. 03:03

A. As I said, many of the characteristics, 03:03

enough to allow one to build such a module, are in 03:03

Exhibit 1029. But I did not specify -- I did not 03:03

cite to a JEDEC standard document that provides the 03:03

physical characteristics of such a module. 03:03

Q. Are you even aware of any memory modules 03:03

with -- let me withdraw and ask. 03:04

Are you aware of any DDR2 memory modules 03:04

with a x8 or x16 memory module bit width other than 03:04

what's described in Perego? 03:04

A. Can I have the question one more time? 03:04
Q. Are you aware of any DDR2 memory modules with a memory bit width of x16 or x8 other than what's described in Perego? 03:04
A. I can't identify one with specificity, but it would not surprise me at all if I could find one. 03:04
Q. Have you used one with a x8 memory -- x8 bit width with a JEDEC compliant DDR2 device on it? 03:05
A. Not that I can recall. 03:05
Q. Okay. Have you ever used a memory module with a bit width of x16 that includes a JEDEC compliant DDR2 device on it? 03:05
A. No, I don't recall ever having used that particular combination. I have used DDR2 memory modules and I have used x16 memory modules, but I don't recall having used those two together personally. 03:05
Q. When you say you have used x16 memory modules, what kind of DRAM devices are on the memory module? 03:06
A. I don't recall specifically. It would have been something older than DDR. 03:06
Q. So something like SDRAM? 03:06
A. Like SDRAM or fast page mode, something 03:06

like that. 03:06

Q. Okay. But you don't recall ever having 03:06
used a memory module with DDR or newer generations 03:06
of DRAMs that's 16 bit wide or below, correct? 03:06

A. I don't personally recall ever having used 03:06
that in a module. But it certainly would be quite 03:06
within ordinary skill levels to design one. 03:06

Q. How long have you been working in the 03:06
memory industry? 03:06

A. It depends what you define as "in the 03:06
memory industry." I have been working with memory 03:07
chips in various ways for almost 40 years. 03:07

Q. Okay. And when was DDR first introduced? 03:07

A. Oh, boy. I don't know. Somewhere around 03:07
2002. 03:07

Q. DDR or DDR2? 03:07

A. I believe -- let me see if I have 03:07
something that can refresh my memory here. 03:07

Maybe a little bit earlier. It became 03:07
popular around 2002, but it may have been available 03:07
a year or two earlier than that. 03:07

Q. Okay. So DDR has been available for at 03:07
least 20 years? 03:07

A. Yes. 03:07

Q. Okay. And in those 20-plus years, you 03:07

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don't recall ever having used a memory module that's 16 bit wide or lower and have DDR or newer generations of JEDEC compliant memory devices on them; is that correct? 03:07 03:08 03:08 03:08

A. That's correct. I don't personally recall using one of those. 03:08 03:08

Q. Do you recall such a memory module described anywhere? 03:08 03:08

A. Well, I think a person of ordinary skill would understand it from Exhibit 1029. 03:08 03:08

Q. I'm asking a different question. 03:08

You review journal articles, correct? 03:08

A. Yes. 03:08

Q. You read journal articles. Are you -- do you recall any journal articles describing a memory module with DDR or newer generations of the SDRAM that is 16 bits wide and lower? 03:08 03:09 03:09 03:09

A. Not that I can give you off the top of my head. It would have been such an ordinary thing that it wouldn't have been something that I would specifically remember. 03:09 03:09 03:09 03:09

Q. The answer is that you don't recall any single reference? 03:09 03:09

A. No. I mean that's just a detail that I don't recall whether or not I've specifically seen 03:09 03:09

that combination. 03:09

Q. Do you recall seeing combinations of 03:09

x64-bit-wide memory modules with DDR or newer 03:09

generations of DRAM devices on them? 03:09

A. Yes. 03:09

Q. Well, if that's such a trivial detail, why 03:09

did you recall that? 03:10

A. Because it happens to be what's in the 03:10

computer that's sitting on my desk. 03:10

Q. So x64 is the most common -- the commonly 03:10

used bit width for memory modules; is that correct? 03:10

A. Or desktop personal computers, that is the 03:10

case. 03:10

Q. When is x8 or x16 bit-wide memory modules 03:10

used, in what applications? 03:10

A. Generally when you wanted a system to be 03:10

very small. So, you know, in industrial 03:10

applications or portable applications or small 03:11

devices would be the most common usage today. 03:11

Historically it was used when memory chips 03:11

were larger and you could only fit a small number of 03:11

them on a DIMM. 03:11

Q. When you say industrial applications, what 03:11

do you have in mind? 03:11

A. If you are building a factory control or 03:11

PC or an automotive application, something where you're very constrained in terms of power and size and you want it to be very efficient, or you may want to use a relatively small amount of memory, it would be common to use a narrower memory module. 03:11

Q. And when you say portable applications, what do you refer to? 03:11 03:12

A. Any small handheld device, some type of a hand-carried sensor or, you know, a measurement instrument, those kinds of things. 03:12 03:12 03:12

Q. Okay. But not in PCs or server systems; is that correct? 03:12 03:12

A. They're not used today in the PCs or servers that I'm familiar with. 03:12 03:12

Q. And they haven't been used since the late 1990s, correct? 03:12 03:12

A. I don't know. I know that that's the last time I'm personally familiar with them being used. But as I said, these technologies often linger for a long time. 03:12 03:12 03:12 03:12

Q. And in 2004 and 2005, the PC systems used x64 bit-wide bus, correct? 03:12 03:13

A. Desktop PCs generally did. 03:13

Q. What about servers? 03:13

A. They would generally use a 72. Or I think 03:13

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there might have been some 144-wide modules. But again, there's variations throughout the industry. 03:13

THE REPORTER: Counsel, I need to go off the record and reboot my system. So how about five minutes; is that okay? 03:13

MS. ZHONG: So why don't we take a break now so you can reboot your system. 03:14

(Recess.) 03:14

(Off record: 3:14 p.m.) 03:14

(On record: 3:34 p.m.) 03:14

MS. ZHONG: Let's go back on the record. 03:33

Q. Dr. Wolfe, do you have '912 patent, Exhibit 1001 with you? 03:33

A. Yes. 03:34

(Exhibit 1001 was marked for identification and attached hereto.) 03:34

BY MS. ZHONG: 03:34

Q. Can you turn to Claim number 16? I believe it's Exhibit Number 44. 03:34

A. Again, if you don't mind, can I look at it in my declaration where it's a little bit easier to read? 03:34

Q. Sure. Where are you looking? 03:34

A. Pages 31 and 32. 03:34

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THE REPORTER: What exhibit number, please, for the record? 03:34

THE WITNESS: 1003. 03:34

THE REPORTER: Thank you. 03:34

BY MS. ZHONG: 03:34

Q. Can you take a look at Element 16.c.iii on page 31. 03:34

A. Okay. 03:34

Q. Do you see the limitation, "The circuit generating a set of output signals in response to the set of input signals"? Do you see that limitation? 03:34

A. Yes. 03:35

Q. And the set of input signals would include at least one row column address signal, bank address signals, and at least one chip select signals, correct? 03:35

A. Correct. 03:35

Q. Okay. And what's your interpretation of generating a set of output signals in response to the set of input signals? 03:35

A. The -- 03:35

Q. Let me ask you. Does the output signal need to be generated using every single one of the row/column address signals, bank address signals, 03:35

and one chip select signal that's recited in 16.c.i? 03:35

A. I've analyzed it both ways in my 03:36

declaration. But my understanding is that, based on 03:36

the prosecution history, that is a requirement here 03:36

because in order to obtain allowance it was argued 03:36

that that was a requirement. 03:36

Q. Can you point me to where it's argued in 03:36

the prosecution history that's a requirement? 03:36

A. I believe it's in my report -- let me see 03:36

if I can find where. 03:36

If you look at page 26 of my declaration, 03:37

Exhibit 1003, there's a citation of the comments 03:37

that were made to the examiner. Well, in this case 03:37

it's the examiner's response to those comments. 03:37

There may be others as well. And it also continues 03:37

to paragraph 63. 03:38

Q. Okay. But basically on page 26 and 27 03:38

that's where you laid out your interpretation in 03:39

response to? 03:39

A. Yes. And, of course, this is not my 03:39

decision. This is a decision that the board will 03:39

have to make as a matter of law. And they've 03:39

analyzed it under both assumptions. 03:39

Q. And I'm asking you how would a person of 03:39

ordinary skill in the art understand? 03:39

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A. I think a person of ordinary skill in the art, based on the prosecution history as intrinsic evidence, would understand that this claim has been limited to a logic element that generates chip select signals in response to all four of the enumerated signals in Claim 1 or in this Claim 16. 03:39

Q. Where does the PLL clock signal come from? 03:39

A. Where does the PLL clock signal in the claim come from? 03:40

Q. Yeah. 03:40

MR. CHANDLER: Objection. Form. It's -- 03:40

BY MS. ZHONG: 03:40

Q. Does Claim 16 even recite a clock signal? 03:40

A. It does not. It claims a -- a connection between the phase locked loop and the DDR memory device, the logic element and the register. So -- 03:40

Q. So -- 03:40

A. But certainly in the case of Claim 16, I think that one would have to reasonably understand the arguments to the examiner to be that the signal must be -- the output signal must be generated in response to the enumerated input signals in 16.c.i. 03:40

Q. And what's the indication in '436 that those signals are not used? 03:41

A. I think the real question is what's the 03:41

indication that those signals are used? There would be no need to use them. 03:41

If you read through the patent and look at the teachings of Figure 10, for example, you can see that A13 is sufficient to generate the signals that are needed, or that A12 and A13 are, or that some subset is. 03:41

It's not necessary to use bank address signals. There's no reference to using the bank address signals. They are separately provided to all of the ranks. So there's just simply no reason to conclude that there's any teaching that each of the signals is used. It would be speculation. 03:42

Q. You didn't really answer my question. 03:42

What's the indication that they would not be used? 03:42

A. I didn't look because I don't think that that's the requirement for priority date. The question is -- 03:42

Q. It's not -- it's not really what you believe is a requirement. Just answer my question. 03:43

A. That's not the analysis that I did. 03:43

Q. I'm not here to -- okay. 03:43

Can you call up Ellsberry, which is Exhibit 1035? 03:43

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A. I'm sorry, did you ask me to look at Exhibit 1035? 03:43
Q. No, 1037. Ellsberry. 03:43
A. Okay. 03:43
(Exhibit 1037 was marked for identification and attached hereto.) 03:43
BY MS. ZHONG: 03:43
Q. Ellsberry deals with JEDEC compliant memory modules; is that correct? 03:43
A. That's certainly within the scope of Ellsberry, yes. 03:43
Q. And I think we discussed in last session that you are not aware of any x8 memory modules using JEDEC compliant DDR2 or DDR devices, correct? 03:44
A. I'm not personally aware of one, no. But, you know, I'll stick with my previous answers as to how a person of ordinary skill would understand that from the JEDEC specification. 03:44
Q. And I think you also said that you are not -- you cannot recall any journal papers that describes x8 memory modules using JEDEC compliant DDR2 or DDR devices, correct? 03:44
A. I can't recall one that specifically says that off the top of my head. 03:44

Q. Okay. And you have been in the memory industry for 40 years? 03:44 03:45

A. I've been using memory devices and designing products that interact with memory devices for 40 years. 03:45 03:45 03:45

Q. And you have been familiar with the DDR -- the JEDEC standards for DDR2 and DDR for over 20 years? 03:45 03:45 03:45

A. With respect to JESD79 and 79-2, that is correct. 03:45 03:45

Q. Are you aware of any other JEDEC standards for DDR or DDR2 devices? 03:45 03:45

A. I believe there are other ones. They have to do with other aspects other than the functional characteristics. And then there are all kinds of variations of DDR and DDR2 devices that are -- that are in separate standards as well. 03:45 03:45 03:45 03:46 03:46

Q. And you did not cite any of those, correct? 03:46 03:46

A. Correct. It wasn't necessary. 03:46

Q. Okay. Can you take a look at Figure 2 of Ellsberry? 03:46 03:46

A. Figure 2 of Ellsberry? 03:46

Q. Correct. 03:46

A. Yes. 03:46

Q. In Figure 2 of Ellsberry, there are more than one DRAM devices per rank, correct? 03:46

A. Not necessarily. If you read Ellsberry, it indicates that -- that Figure 2 is designed to illustrate one or more Switch ASICs with DRAMs attached to it. So literally the illustration here is of more than one. But if you read it in the context of the text, it's intended to communicate one or more. 03:47

Q. As shown in Figure 2, it's intended to show N DRAM devices per rank, correct? 03:47

A. No. It's actually N plus 1. But if you read it in the context of the specification, it indicates that N plus 1 is one or more. 03:47

Q. Okay. And in Figure 2 as drawn here, it's intended to show there are N plus 1 memory devices per rank, correct? 03:48

A. No. It is intended to show that there can be N plus 1. But as I said, if you read it in the context of the specification, it's clear that this is intended to refer to one or more switch ASICs connected to one or more sets of memory. 03:48

Q. I'm talking about what's literally drawn here. Can you answer the question? 03:48

A. I think I did answer the question. 03:48

There are -- there are clearly a variety of options drawn here, but there's also text that describes this drawing. And if you'll read the text and understand this drawing in the context of its description and specification, it is one or more switch ASICs. 03:48 03:48 03:48 03:48 03:49 03:49

Q. Can you tell me where it says it's one or more? 03:49 03:49

A. Yeah. So there's some places -- let's see. I can certainly find some of them. 03:49 03:49

If you look at paragraph 28 -- 03:49

Q. Okay. 03:49

A. -- which is where Figure 2 begins its description. 03:49 03:49

Q. Okay. 03:49

A. And the last sentence it says, "The capacity-expanding feature of the invention is accomplished by a combination of a control unit 204 and one or more memory bank switches, 206 and 208." 03:49 03:49 03:49 03:49

There are other places as well. Did you want me to find them all? 03:49 03:49

Q. Well, it says memory banks 206 and 208. That means two, correct? 03:49 03:50

A. No. I think the proper reading, especially if you read it in the context of 03:50 03:50

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everything else, for example, paragraph 26 where it says, "The invention permits two separate SRAM DDR devices to appear as a single higher-capacity SDRAM DDR device to a source device," that indicates that there can be only two devices. And it can appear as one device. So that would be a one-switch situation. 03:50

There are other examples in paragraph 31 through 33 where it's clear that, if you read that, it's possible to only have data written to memory bank 212 and not 226. So, again, that would be a configuration -- 03:50

Q. That's all right. I was disconnected audio -- from the audio, so I couldn't hear what you said. 03:51

THE REPORTER: And, Counsel, I'm having trouble with my audio on this end, too. I don't know whether it's the Internet feed or exactly what it is. 03:51

MR. CHANDLER: I heard it fine. I haven't had any problems. I heard all three of you just fine just now, so for what it's worth. 03:51

MS. ZHONG: I was disconnected for five minutes, so at least while he was answering. So do you mind repeat your answer? 03:51

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MR. CHANDLER: Well, I mean, if Dr. Wolfe doesn't have the realtime and the court reporter does, maybe the court reporter can just read it. Is that possible? 03:51

(Off the record discussion.) 03:52

BY MS. ZHONG: 03:52

Q. So paragraph 28 states that its memory bank 206 and 208. And that would mean two banks, correct? 03:52

A. I don't believe so. I think that it's simply referring you to the fact that you only need one or more switches. 206 and 208 are both candidates to be one or more. 03:52

If I read that in the context of paragraphs 26 or in the context of paragraphs 31 through 33, in the context of -- for example -- let's see. 03:53

I think paragraph 34, paragraph 46, there are a number of indications that you don't need multiple switches, that you can have only a single switch embodiment, and that you can have as few as two devices which appear as one. 03:53

Q. Now, each of the switch ASIC has four banks connected to it, correct? 03:53

A. There are four banks illustrated in Figure 03:53

2, although, again, in the text, there are indications that one could also have a two-bank variation as well. 03:53

Q. What is a bank? 03:53

So let me ask, when it comes to Ellsberry, what is Bank 0 to Bank 3? Is it internal memory organization or something else? 03:54

A. No, those would be what we would today call banks. 03:54

Q. And when Ellsberry activates a bank, how does it do that? 03:54

MR. CHANDLER: Objection. Form. 03:54

THE WITNESS: Well, I mean, that's described with some detail in the specification. It has multiple embodiments. And if one looks at, for example, Figure 8A, you can see that in the row/Bank mode, a bank is activated in one of two phases, either Phase A or Phase B of a read or write operation -- I'm sorry -- an activated operation by sending an activate command to either Bank A or Bank B. 03:55

BY MS. ZHONG: 03:55

Q. Okay. So why don't we take a look at Figure 10. Are you referring to the AC -- are you referring to the ACA and ACB command? 03:55

Hello? 03:56

A. Yeah, I'm looking. 03:56

Those are signals, not commands. 03:56

Q. Okay. What's the difference between command and signal? 03:56

A. A signal is an electrical value in a wire generally in this context, where a command is -- a command is more general. It's the communication of an action. 03:56

Q. Okay. So the ACA signal that's sent to, for example, device 1012 and 1010, is that a signal that's activate that particular rank on 1006? 03:56

A. I'm not quite sure how that signal is defined in that drawing. Let me see if it says. 03:57

I don't think we're given a definition of that particular signal. 03:57

Q. As a person or ordinary skill in the art, how would you interpret it? 03:58

A. I don't know whether or not that's intended to be the command. 03:58

And, again, when we look at this in the context of the DDR specification, the DDR commands are well-defined in Exhibit 1029. So we know what an activate command, for example, looks like, and what particular bits are used. 03:58

I referred you to it earlier in the deposition, but let me see if I can find it again. 03:58

Q. I'm asking in specific about Ellsberry. So as a person of ordinary skill in the art, what is ACA that's being output from the control unit ASIC -- 03:58

(Simultaneous speakers.) 03:58

A. I don't -- 03:59

Q. -- that's being sent to -- 03:59

A. I don't know at the moment -- 03:59

THE REPORTER: I'm sorry, one at a time. 03:59

BY MS. ZHONG: 03:59

Q. So you have no idea what ACA and ACB commands mean? 03:59

MR. CHANDLER: Objection. Form. 03:59

THE WITNESS: I don't see them described as commands. I don't think Ellsberry specifies particularly what that particular signal is used for. But this simply explains in Table 8 that the commands are sent to the various devices. And in the context of DDR, they would be sent in the ordinary way. So, for example, an activate command is sent using CAS bar and WE bar, and CS bar, and RAS bar. 03:59

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BY MS. ZHONG: 03:59

Q. In Table -- in Figure 8A, activate for the -- for Bank A, it says sent to DDR A activate command. 03:59 04:00

A. I don't understand what the question is. 04:00

Q. So are you saying that in the -- in Figure 8 in the column "Activate," you think those are the JEDEC standard command combinations? 04:00 04:00 04:00

A. In the row that says "Activate" under where it says "Row/Bank Mode," I think a person of ordinary skill would understand that those could be the JEDEC standard activate commands. 04:00 04:00 04:00 04:00

Q. And what does DDR A and DDR B refer to? 04:00

A. I believe it's referring to the DDR on Port A and Port B in a two-rank configuration. 04:01 04:01

Q. What is a port? 04:01

A. A collection of wires -- or collection of pins, maybe. Those can be seen in Figure 10, 11, and 12. 04:01 04:01 04:01

Q. 10, 11 and 12. 04:01

Okay. So let's go to Figure 10. Where is a port? 04:01 04:01

A. The outputs of the switch ASIC that end in A are Port A. That would be the memory devices grouped together as 1006. And Port B would be the 04:01 04:01 04:01

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memory devices grouped together as 1008. 04:01

Q. So the port is on the -- is downstream 04:02
from the ASIC? 04:02

A. No. I would think of the port as being 04:02
the connection to the ASIC. 04:02

Q. So the wire 1016 that's between the 04:02
right-hand side of the switch -- switch ASIC box and 04:02
to the side of DRAM 1012 and 1010, for example, 04:02
that's Port A? 04:02

A. That's a portion of it. That's the data 04:02
bus. And then there are also the strobe shown in 04:02
Figure 10 as well. 04:02

Q. What is the strobe that you are referring 04:03
to? DQS0A and DQS1A? 04:03

A. And DQS1A, yeah. 04:03

Q. Okay. So it's the -- it's the line that's 04:03
connected to the signal DQS1A? 04:03

MR. CHANDLER: Object to form. 04:03

THE WITNESS: And we're starting to get 04:03
into semantics a little bit. But technically the 04:03
port is the connection between the ASIC and the 04:03
outside world. 04:03

So it would be -- Port A would be in the 04:03
switch ASIC. And Figure 10 would be the first four 04:03
elements listed on the top left of the switch ASIC. 04:03

And Port B would be the bottom four elements. 04:03
BY MS. ZHONG: 04:03
Q. Okay. And by the first four elements and 04:03
the bottom four elements, you are referring to 04:03
the -- so for the -- when you say the first four 04:04
elements, you are referring to the four lines 04:04
connected between DQA and DRAM 1012, DQS0A, DQA724, 04:04
DQS1A and the DRAM group 1006; is that right? 04:04
MR. CHANDLER: Object to form. 04:04
THE WITNESS: I'm actually referring to 04:04
the connections to the ASIC. And although it's 04:04
illustrated as four lines, it would be illustrating 04:04
10 connections. 04:04
BY MS. ZHONG: 04:04
Q. Okay. So basically all the connections 04:04
that's between the output of the ASIC switch and the 04:04
input of the DRAM boot; is that right? 04:04
MR. CHANDLER: Objection. Form. 04:04
THE WITNESS: Yes, in this particular case 04:04
it would be the -- the connections denoted by 1016 04:04
connecting to the DRAM group 1006. 04:05
BY MS. ZHONG: 04:05
Q. Okay. And then for Port B, that will be 04:05
the -- all the lines that's connecting to the output 04:05
of the switch ASIC and group 1008 of the DRAMs; is 04:05

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that right? 04:05
MR. CHANDLER: Object to form. 04:05
THE WITNESS: It's not all the lines, but 04:05
it's the four that are named at the bottom -- the 04:05
four sets of lines that are named in the bottom 04:05
right: DQB, DQS0B, and DQS1B. 04:05
BY MS. ZHONG: 04:05
Q. Is it possible for you to mark those lines 04:05
on your local copy and email it to the -- email it 04:05
to your counsel so we can make a record of it? 04:05
A. That's up to counsel. 04:06
Q. I'm requesting you to do that. Can you do 04:06
that? 04:06
Maybe you can first share your screen with 04:06
us. And I just want to make sure that my 04:06
understanding is correct. And if you can point to 04:06
the four lines that we're just discussing. 04:06
Is that possible? Can you do that? 04:06
A. If that's okay with counsel. I think I've 04:06
answered the question already. 04:06
THE WITNESS: But is it okay with you, 04:06
Ted? 04:06
MR. CHANDLER: If you can do it. 04:06
THE WITNESS: Host disabled, participant 04:06
screen sharing, so apparently I cannot. 04:06

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(Off the record discussion.) 04:07

BY MS. ZHONG: 04:07

Q. Okay. So for Port A, can you just 04:07

indicate which four lines you're referring to? 04:07

A. These four here -- oh, sorry. 04:07

Q. Can you just draw a box around them? I 04:07

see the cursor moving. 04:07

A. Let's see. 04:07

Q. I think it's comment. Yep, this one. 04:08

A. That would be Port A. 04:08

Q. Okay. 04:08

MR. CHANDLER: So how are we going to get 04:08

this in the record? 04:08

MS. ZHONG: I can do a screen -- let me do 04:08

this. Let me do a screen capture. 04:08

MR. CHANDLER: So, Annita, you'll do a 04:08

screen capture and upload that as a PDF as an 04:08

exhibit? 04:08

MS. ZHONG: Yeah, let me do that. If it 04:08

allows me to save. Let me see if it allows me to 04:08

pull that thing over. 04:09

Q. Can you refresh your Exhibit Share and see 04:09

whether a PNG file called Exhibit 2102 Capture has 04:09

shown up? 04:10

A. I have that. 04:10

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(Exhibit 2102 was marked for identification and attached hereto.)

BY MS. ZHONG:

Q. Okay. Can you take a look at it and see if that reflects what you drew on the screen?

A. It does.

Q. So I have a question. Does it include a portion of the ASIC switch or only including the portion that's in the ASIC switch in order to capture the signals that's labeled here?

A. No. When I would typically talk about a port, I would be talking about the -- the point of interconnection between the ASIC switch and the outside world.

Q. So it's from the output of the ASIC switch to the outside world? It doesn't include the inside world.

A. It is the output. I mean, port is from the same root word as portal. It basically means a door. It means the actual point at which you would enter or exit the switch.

Q. Okay. So port is actually the point of exit from the ASIC to the outside world?

A. Yes.

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Q. What does it mean by enable or disable a port? 04:11

A. Where? 04:11

Q. 1037. Let me see. I believe it's paragraph 31. 04:11

So paragraph 31 it talks about, for example -- 1, 2, 3, 4 -- from the end of the fifth line, if you can read that sentence. 04:11

A. I think in context it means not used. 04:12

There are two ranks here. And what this is saying is that in this situation only the rank connected to Port B would be used and the rank connected to Port A would not be used and would not send out commands. 04:12

Q. Okay. But the activation and deactivation that's described in 31 is with respect to the memory bank; is that right? 04:12

MR. CHANDLER: Object to form. 04:13

THE REPORTER: I'm sorry, respect to the what? I'm sorry. 04:13

BY MS. ZHONG: 04:13

Q. Is with respect to the memory bank. 04:13

A. Yes, my understanding that memory bank in paragraph 41 is referring to what we would typically call a rank today. 04:13

Q. Okay. And if you can take a look at Figure 4 of Exhibit 1037. 04:13
A. Yes. 04:13
Q. Is the description of Figure 4 of 1037, especially where Port A and Port B are labeled, consistent with the understanding that you just described? 04:13
A. Yes. 04:13
MR. CHANDLER: Objection. Form. 04:13
BY MS. ZHONG: 04:13
Q. Okay. So Port A and Port B in each of the page refers to the point of exit from the ASIC? 04:13
A. Yes. 04:14
MS. ZHONG: Can we take a break for ten minutes? 04:14
MR. CHANDLER: Yes. 04:14
(Recess.) 04:15
(Off record: 4:14 p.m.) 04:15
(On record: 4:29 p.m.) 04:15
BY MS. ZHONG: 04:29
Q. Dr. Wolfe, can you pull up Exhibit 1036, which is Amidi? 04:29
A. Okay. 04:29
(Exhibit 1036 was marked for identification and attached.) 04:29

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BY MS. ZHONG: 04:29

Q. What is the title of 1036? 04:29

A. Transparent Four Rank Memory Module for Standard Two Rank Sub-Systems. 04:29

Q. What does it mean by standard two rank subsystems? 04:29

A. I think one of the objectives of Amidi was to be able to put four ranks of memory physically into a computer that only provided two chip selects from the memory controller. 04:30

Q. And if you look at Figure 1 of Amidi, it says "Overall Block Diagram of Standard Memory Interface." 04:30

Do you see that? 04:30

A. Yes. 04:30

Q. And by "standard," is it referring to JEDEC standard? 04:30

A. There were certain JEDEC standards that it would have been compliant with, but I think that's probably reading too much into the actual application. I think when they say "standard" here, they just mean common or conventional, well-known. 04:31

Q. And JEDEC compliant memory interface in the modules were well-known and common at the time; is that correct? 04:31

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A. Various kinds of JEDEC standard modules were well-known and common at the time. 04:31

In fact, if you actually look at the description of Figure 1, it does use the term "common" rather than "standard." 04:31

Q. Does Amidi use parallel bus architecture as in JEDEC standards or it uses more point-to-point architecture as Perego? 04:32

A. Well, remember, Perego discloses both point-to-point end buses, but the primary embodiments that are described in Amidi are using a traditional multidrop bus connection for the data lines between the controller and the memories. 04:32

Q. And what's the bit width using Amidi? Memory modules. What's the bit width of the memory modules using Amidi? 04:32

A. I don't recall every disclosure, but certainly the diagrams are, such as Figure 4, are directed to a 72-bit example. 04:33

Q. So in Amidi there are more than one memory device, correct? 04:33

A. In the embodiment that's illustrated in Figure 4, that would be the case. 04:33

Q. Are you aware of any illustrated example where only one memory device per rank is shown? 04:34

A. I don't recall a complete example of one memory device per rank being shown in Amidi, but the teachings would be applicable. 04:34
Q. What is a DIMM? 04:34
A. What is a DIMM, is that the question? 04:34
Q. Correct, yes. 04:34
A. In the context of something like the '912 patent, DIMM stands for dual inline memory module, which basically means a circuit board with connectors on two surfaces where the connectors consist of multiple paths that are lined up. 04:34 04:35
Q. Using industrial applications with x8 -- let me withdraw and ask. 04:35
You mentioned that certain industrial application and small portable application might use x8 or x16 memory modules. 04:35
Do you recall that discussion? 04:35
A. Yes. 04:35
Q. Are DIMMs used in such applications? 04:35
A. I would expect that it's likely that they are, but I don't know for certain. Certainly a person of ordinary skill would know how to design one. 04:35 04:36
Q. I'm sorry, have you seen one being used in those applications? 04:36

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A. I've seen DIMMs used in industrial computing devices.

Q. What about are DIMMs used in handheld devices?

A. I've seen DIMMs used in handheld devices.

Q. DDR2 DIMMs?

A. I can't say for certain one way or another.

Q. Have you seen x8 DDR2 devices used in handheld devices?

A. Yes.

Q. DDR2 DIMM x8 bit width for the memory module.

A. What's the question?

Q. You say you are aware of DDR2 DIMM width with x8 bit width memory module being used in handheld devices.

A. No, I am not aware of that in particular, but I'm certain that a person of ordinary skill could easily build that.

Q. I'm just asking you. You are not aware of any such DIMM modules being built and used in handheld devices?

A. I am not aware of an 8-bit-wide DIMM using DDR memory that's been used in a handheld device,

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but that doesn't mean it hasn't happened. 04:37

Q. Okay. And you are not aware of any 04:38

8-bit-wide DIMM module being built and used in 04:38

industrial applications with DDR or DDR2 devices, 04:38

correct? 04:38

A. I'm not aware of a DIMM module being used 04:38

with those specific specifications. 04:38

Q. Are you aware of any 8-bit-wide DIMM 04:38

module being built and used in industrial 04:38

applications with DDR3, DDR4, or DDR 5 devices? 04:38

A. No. I'm aware of memory modules, but they 04:38

are not necessarily DIMMs. 04:38

Q. Okay. What kind of other memory modules 04:38

are there? 04:39

A. There are small form factor memory modules 04:39

where the memory die are placed on printed circuit 04:39

boards. 04:39

Q. Are they SIMMs or do they have another 04:39

name? 04:39

A. No. They have various kinds of names. 04:39

Some of them don't have a name. Some of them would 04:39

be called things like FCBGAs, I believe, where 04:39

they're -- they're printed circuit boards with a 04:39

memory die soldered on top. 04:39

Q. Okay. But you would not call them as 04:39

DIMMs? 04:39

A. No, I would not call those particular 04:39

devices as DIMMs. I would call them memory modules, 04:39

but not DIMMs. 04:39

Q. Okay. Ellsberry is about 04:40

capacity-expanding memory modules such as DIMMs, 04:40

correct? 04:40

MR. CHANDLER: Objection. Form. 04:40

THE WITNESS: It's one of the motivations 04:40

that's mentioned in -- in Ellsberry is to expand the 04:40

capacity of the computer. 04:40

BY MS. ZHONG: 04:40

Q. Okay. So if you only have a single device 04:40

per rank, how is that going to achieve the bit 04:40

capacity expansion objective of Ellsberry? 04:40

A. Because you could expand from a one-device 04:40

DIMM to a two-device DIMM by having two ranks. 04:40

Q. Why can't you just have those two devices 04:41

in a single rank and expand the bandwidth as -- 04:41

(indiscernible.) 04:41

THE REPORTER: I'm sorry, Counsel. Repeat 04:41

your question. "Two devices in a single"... 04:41

BY MS. ZHONG: 04:41

Q. -- rank and expand the bandwidth as a 04:41

result? 04:41

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A. That would require more pins on the memory bus. It would require a physical modification to an existing computer. 04:41 04:41 04:41

Q. Can you please take a look at Figure 4 of Ellsberry. 04:41 04:42

A. Yes. 04:42

Q. In this configuration -- take a look at Figure 4, then read paragraph 12 to yourself. 04:42 04:42

A. Okay. 04:42

Q. Do you see that in paragraph 12, it says in Ellsberry, "The load on the bus is not increased because the memory bank switches present a single load to the bus." 04:42 04:42 04:42 04:42

Do you see that sentence? It starts with "Moreover," the sixth line in paragraph 12. 04:42 04:42

A. I don't see that in paragraph 12. 04:43

Q. Ellsberry, paragraph 12, one, two, three, four, five -- sixth line. "Moreover, the load on the bus is not increased because the memory bank switches present a single load to the bus." 04:43 04:43 04:43 04:43

Do you see that sentence? 04:43

A. I'm sorry, I'm looking at the wrong patent. 04:43 04:43

THE REPORTER: Do you know what exhibit number you're referring to? 04:43 04:43

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MS. ZHONG: 1037. 04:43
THE WITNESS: I do see that. 04:43
BY MS. ZHONG: 04:43
Q. Can we go back to Figure 4 of Ellsberry? 04:43
A. Yes. 04:44
Q. So in Figure 4 of Ellsberry, at the -- at the point of where DQ (7:0) and DQS is, there's only a single load; is that right? 04:44
A. That's what Ellsberry tells us. 04:44
Q. How does Ellsberry manage to do that? 04:44
MR. CHANDLER: Objection. Form. 04:44
THE WITNESS: I would think it has to do with his definition of a load and the detailed design of his switches. 04:44
I think what he's really saying is that there's not a memory bank load on there; that there's -- there's not the load of the memory chips on that port. There will be some increased load, some de minimis increase in load from the switches 402 and 404. 04:45
BY MS. ZHONG: 04:45
Q. Okay. So there are two different ranks, at least two different ranks, each connected to a port A and a port B; is that right? 04:45
A. Correct. 04:45

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Q. Okay. But the memory controller would only see the load corresponding to a single rank, is that what Ellsberry is saying? 04:45

A. Generally. I think what he's doing is he's recognizing that the vast majority of the load comes from the physical presence of pins and not from internal circuits. And what he's done is now he no longer has two sets of pins on those wires but only one set of pins from the switch chip in Figure 4. 04:45 04:46

Q. When you say "the pins," which pins are you referring to? 04:46

A. So instead of having the pins 234 and 236 both physically connected to the host, now he only has the pins 230 physically connected to the host. 04:46

Q. Ah. Okay. 04:46

And if during the operation only one of the bands is activated, that would also help with the fact that the memory controller is only seeing a single -- the load corresponding to a single rank; is that right? 04:46 04:47

A. It can. But again, I think that what he's saying is that it's the physical presence of pins on the connector that dominates the loading. 04:47

Q. Okay. So what Ellsberry is saying is that 04:47

by merging the 234 and the 236 into the 230 type, respectively, the memory device is only seeing a single load? 04:47

MR. CHANDLER: Objection. Form. 04:47

THE WITNESS: By combining them using a switch in the way that he's described in Figure 4, that has the effect of reducing the load from approximately 2 to approximately 1. 04:47

BY MS. ZHONG: 04:47

Q. Okay. And by "switch," which switch are you referring to? 04:47

A. 402 and 404 act as a switch in Ellsberry. It allows -- 04:47

Q. What do you mean by -- go ahead. 04:48

A. It allows -- in a read it allows either 402 or 404 to be driving bus 230. And in a write, it allows the information on 230 to be routed to either 234 or 236. 04:48

Q. The square where "write" is written, is that a delayed flip-flop? 04:48

A. I don't know what you mean by "delayed flip-flop." It is a flip-flop or a latch. 04:48

Q. It has a word "D" in there, so that means it's a delayed flip-flop? 04:48

A. No. "D" stands for data. That just means 04:48

it's the input. 04:48

Q. Oh, okay. 04:48

So the write is -- the control for the 04:48

write is implemented as a flip-flop? And the 04:48

triangle for read, that's a driver; is that right? 04:49

MR. CHANDLER: Objection. Form. 04:49

THE WITNESS: Let me see what it says. 04:49

It's described in the text as 04:49

bidirectional signal drivers, but there is a 04:49

flip-flop that's illustrated in the figure. 04:49

BY MS. ZHONG: 04:49

Q. Is -- go ahead. 04:49

A. That's enough. 04:49

Q. Are those tri-state buffers? 04:49

A. Yes, I believe those are tri-state 04:49

buffers. The bidirectional buffers, I believe. 04:49

They're -- they're buffers that can be disabled. I 04:50

would generally refer to those as tri-state buffers. 04:50

Q. So what's your understanding of tri-state 04:50

buffers? 04:50

A. It has three states normally: High, low 04:50

and disengaged. Or high impedence is the way we 04:50

technically talk about it. 04:50

Q. How do you know, like, these ones can be 04:50

disabled? 04:50

A. I believe it tells us that in the text. Let's see.

I'm not finding it right now.

My recollection was that the description of that as being an implementation of switch 206 where it calls those signal drivers that operate as a switch, along with the drawing, indicated to me that those are tri-state drivers. Because that would be a very common configuration as to how one would build a switch.

Q. Are those FET switches?

A. It depends what you mean by FET switches. Everything in these systems is made of FETs.

When Ellsberry refers to FET switches, which I think he's referring to a very specific kind of prior art FET switch. I think that more normally somebody would call those -- call this a distributed multiplexor or a tri-state driver.

Q. And when you say like everything in the system is made of FET switches, what do you mean by that? By FET, do you mean transistors?

A. FET stands for field effect transistors.

MR. CHANDLER: Objection. Form.

THE WITNESS: All of the logic in these systems is comprised of field effect transistors.

But Ellsberry uses the term "FET switch" in a very common way where he's talking about what we would call a -- a passthrough FET or a transmission gate where he's talking about a very specific configuration of a FET as was used in some of the prior art references. 04:55

It's very clear when you read Ellsberry as a whole that he's building switches out of this circuit and it's comprised of FETs, but it's not what he calls a FET switch. 04:55 04:56

BY MS. ZHONG: 04:56

Q. What is a passthrough FET? 04:56

MS. ZHONG: F-E-T, Court Reporter. 04:56

THE WITNESS: It's where you connect a signal between the source and the drain of the FET as opposed to connecting the signal to the gate of the FET. It's a different configuration. 04:56

And it can be used in certain circumstances. And Ellsberry refers specifically to something even narrower, to a stand-alone FET chip that was used in the prior art. 04:56

And he wanted to use a different configuration that was faster of using these tri-state drivers or this distributed multiplexor that wouldn't commonly be called a FET switch. It 04:56 04:57

would commonly be called by another name. 04:57
BY MS. ZHONG: 04:57
Q. And you also mentioned a transmission gate 04:57
FET switch; is that correct? 04:57
A. Yes. Again, that's just another name for 04:57
the configuration where the source and drain are 04:57
used to couple a signal rather than driving the 04:57
signal through the gate. 04:57
It's essentially a configuration in which 04:57
you don't power the output signals, and therefore, 04:57
it can -- it can have limited utility, where this is 04:57
a configuration where you would power the output 04:57
signals and would be faster. 04:57
Q. You did not find any disclosure upon your 04:58
review just now of disabling the flow 2 and flow 3; 04:58
is that right? 04:58
MR. CHANDLER: Objection. Form. 04:58
THE WITNESS: No, I wouldn't say I didn't 04:58
find it, in those words. But I -- it certainly 04:58
talks about them comprising a switch 206, which 04:58
would mean that one's operating and one's not. 04:58
And also, if you look at Figure 8 and 04:58
understand its operation, you would understand that 04:58
as well. 04:58
And then if you look at the description of 04:58

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the digital drivers described in paragraph 31 which would correspond to these, then you would understand that only one of them is driving the bus 230 at a time during a read operation. 04:58 04:59 04:59 04:59

It also describes them in paragraph 33 that the ports are multiplexed onto the DIMM interface 202, which corresponds to 230. And multiplexing means switching one at a time. 04:59 04:59 04:59 04:59

BY MS. ZHONG: 04:59

Q. And paragraph 33 is an implementation where write data is sent to both ports A and B, right? 05:00 05:00 05:00

A. Yes, in what's described in that embodiment in paragraph 33. At the beginning of the paragraph that's how it works. At the end of the paragraph it describes the other embodiment. 05:00 05:00 05:00 05:00

Q. You're talking about alternatively when row/bank mode addressing is used, read and write commands -- (indiscernible.) 05:00 05:00 05:01

THE REPORTER: I'm sorry, Counsel. Repeat your question, please. 05:01 05:01

BY MS. ZHONG: 05:01

Q. You are referring to alternatively when row/bank mode addressing is used, read and write commands are sent only to the targeted memory device 05:01 05:01 05:01

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and a no-op operation is sent to the nontarget memory device? 05:01

A. Yes. 05:01

Q. That's referring to sending commands to the targeted memory device, not data, right? 05:01

A. In the case of -- it's essentially -- it's exactly what's described in Figure 8. So it's describing how the commands are sent. The command is sent to only one of the banks in that situation. The data operates -- 05:01

Q. But the data -- 05:02

A. The data -- it doesn't really matter whether or not the data is sent to both banks on a write operation, but it would be multiplexed as described in that paragraph on a read operation. 05:02

Q. Okay. So the data is multiplexed and is sent to both banks because -- because only one of the bank receives a read and write command, only one of the bank will actually read that data; is that right? 05:02

MR. CHANDLER: Objection. Form. 05:02

THE WITNESS: You don't send data to a bank on a read command. 05:02

BY MS. ZHONG: 05:02

Q. Sorry. So let's say it's a write 05:02

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operation, and the write command is only sent to one rank, and a no-op command is sent to the other rank. So even though data is sent to both of them, only the rank that receives the write command will actually read the data; is that right -- will actually write the data? 05:02 05:02 05:03 05:03 05:03

MR. CHANDLER: Objection. Form. 05:03

THE WITNESS: If that's how it's built, that would be true. It's silent as to whether or not it sends the write data to both ports because it doesn't matter. 05:03 05:03 05:03 05:03

It's clear that the read data is only forwarded from one port through the switch. And it's clear that the command -- for example, a write command -- would only be sent to one port at a time. 05:03 05:03 05:03 05:03

BY MS. ZHONG: 05:03

Q. Okay. But in that operation, for example, where the write data is sent to both port A and port B, would there be a problem of bus conflict? 05:03 05:03 05:04

MR. CHANDLER: Objection. Form. 05:04

THE WITNESS: No, because on a write -- 05:04

BY MS. ZHONG: 05:04

Q. Why not? 05:04

A. -- the memory chips are listening, and the DQs all come from the host and would all be 05:04

replicated. So it could operate that way without a conflict in that particular case. 05:04

Q. Okay. So when you have a write operation, you can have both -- let's go back to Figure 4. 05:04

When you have a write operation, you can have 402 and 404 being turned on at the same time without having to worry about a write conflict -- or a bus conflict? 05:04 05:05

A. What do you mean being turned on? They could drive ports 234 and 236 conceivably without a conflict. The conflict happens in the other direction on a read. 05:05

Q. Okay. So when -- so when people talk about bus conflict, it's more about the read operation, not the write operation? 05:05

MR. CHANDLER: Objection. Form. 05:05

THE WITNESS: Correct. That's the critical case. 05:05

BY MS. ZHONG: 05:05

Q. Okay. So let me just understand. I'm getting a little confused. 05:05

When you have a write operation, theoretically you can have -- let's say the data pass between 230 and 236 and the data pass between 230 and 234 are at the same time without having to 05:05

worry about a bus conflict; is that right? 05:05
MR. CHANDLER: Objection. Form. 05:06
THE WITNESS: Conceivably you could do 05:06
that in a write. The problem is when you have a 05:06
read. And that's why you need the switches, the 05:06
multiplexing function that's described between 402 05:06
and 404. 05:06
BY MS. ZHONG: 05:06
Q. Okay. So the 402 and 404 multiplexing is 05:06
more important for the read. Write is less of a 05:06
concern because the device would be listening to it, 05:06
and the device has their own controls that they can 05:06
turn things off to avoid burning the bus. 05:06
MR. CHANDLER: Objection. Form. 05:06
THE WITNESS: That would be my 05:06
understanding. 05:06
BY MS. ZHONG: 05:06
Q. But then why in the -- why in modern DDR 05:07
devices the write path, once you are done with the 05:07
write, you kind of turn off -- let me withdraw and 05:07
ask a question. 05:07
You are familiar with DDR4 -- 05:07
(indiscernible.) 05:07
THE REPORTER: I'm sorry. Your question, 05:07
please? 05:07

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THE WITNESS: I have some familiarity with DDR4, but I don't have it in front of me. 05:07

MR. CHANDLER: Objection. It's outside of the scope. DDR4 is not in the declaration, so it's definitely outside the scope of the direct. 05:07

MS. ZHONG: Can you stop coaching the witness by using speaking objections? 05:07

MR. CHANDLER: I apologize. Object to scope and direct. 05:07

BY MS. ZHONG: 05:07

Q. Dr. Wolfe, are you familiar with DDR4 -- (indiscernible.) 05:07

A. Generally, but I certainly can't recall the entirety of the specification. 05:08

MR. CHANDLER: Objection. Outside the scope of the direct. 05:08

Counsel, you're going to run out of time, so... 05:08

BY MS. ZHONG: 05:08

Q. So in DDR4 are the -- during a write operation, the write path in the data buffer is turned on. And then after the write operation that data path is turned off. Do you know why that is needed? 05:08

MR. CHANDLER: Objection. Outside the 05:08

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scope of direct. 05:08
THE WITNESS: I don't recall that 05:08
specifically. I'd have to look at the specification 05:08
in detail. 05:08
BY MS. ZHONG: 05:08
Q. Can you pull up Exhibit 1033. 05:08
(Exhibit 1033 was marked for 05:09
identification and attached 05:09
hereto.) 05:09
THE WITNESS: Okay. 05:09
BY MS. ZHONG: 05:09
Q. Can you go to page 413? 05:09
Are you there? 05:09
A. Yes. 05:09
Q. Do you see that at the end of the first 05:09
paragraph for Section 10.2.2 it says, "The word 05:09
'rank' is now used to denote a set of DRAM devices 05:09
that operate in lockstep to respond to a given 05:09
command in a memory system"? 05:09
A. I see that. 05:09
Q. What does "in lockstep" mean? 05:09
A. It means if the set of DRAMs includes more 05:10
than one, they are producing their data outputs and 05:10
output clocks at the same time. 05:10
You have to read it in the context at the 05:10

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beginning of the paragraph where it's talking about one or more. 05:10

Q. Can you go to Exhibit 1035, Perego? 05:10

A. Okay. 05:10

Q. Can you go to column 7? Can you read the paragraph starting in line 48 and ends in line 64? 05:10 05:11

A. I see that. 05:11

Q. Can you explain what Perego means by the description in column 7, lines 54 to 64? 05:11 05:11

A. Perego is explaining that one of the things that he teaches is the ability to change the width of the communication bus between the memory module and the host. And that if you implement that feature, then when you change the bit width you are not abandoning a portion of the memory. You are increasing the serialization ratio. So you can still access the same amount of memory. You would simply do it in a larger number of steps. Or if you were to make the -- the module width wider, you don't access more memory. You simply can access it in a fewer number of steps. 05:11 05:11 05:12 05:12 05:12 05:12 05:12 05:12 05:12 05:12

Q. Okay. So what this passage means is that the memory access bit width would be constant. It's just the number of transfers that you have to do varies, depends on the considerable bit width of the 05:12 05:12 05:13 05:13

processor; is that right? 05:13
A. In some of Perego's embodiments, that 05:13
would be the case. 05:13
Q. Okay. And the memory access bit width, 05:13
that's the number of bits the memory module would 05:13
output in response to a single read or write 05:13
operation, right? 05:13
A. Say the phrase again. 05:13
Q. So the number of bits that -- and the 05:13
memory access bit width, that is the number of bits 05:14
the memory module would output in response, for 05:14
example, to a single read operation command, 05:14
correct? 05:14
MR. CHANDLER: Objection. Form. 05:14
THE WITNESS: Can you point me to a 05:14
particular column and line? 05:14
BY MS. ZHONG: 05:14
Q. I'm just asking you in this paragraph. 05:14
A. Remind me the -- the range again? 05:14
Q. 7, 54 to 64. 05:14
A. I'm not finding that particular phrase. 05:14
Am I missing it? 05:15
Q. I thought what you said your understanding 05:15
of what's described in this passage is that the 05:15
amount of memory access is not changed. The only 05:15

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thing that's changed is the serialization ratio. 05:15

A. Correct, and that's -- 05:15

Q. Is that what you -- 05:15

A. Yes, that's when you change what Perego 05:15

calls the configured buffer device interface width. 05:15

Q. But in that situation what Perego calls 05:15

the WA, or the memory access bit width, that is not 05:15

changed; is that right? 05:16

A. In certain embodiments that would be true. 05:16

Q. Okay. And the memory access bit width, 05:16

WA, that is the number of bits the memory module 05:16

would output in response, for example, to a single 05:16

read command from the computer system; is that 05:16

right? 05:16

MR. CHANDLER: Objection. Form. 05:16

THE WITNESS: Yes, but Perego calls it the 05:16

memory device access width. 05:16

BY MS. ZHONG: 05:16

Q. So the memory device access width, WA, 05:16

that is the number of bits the memory module would 05:16

output in response to a single read command from the 05:16

computer system, correct? 05:16

MR. CHANDLER: Object to form. 05:16

THE WITNESS: No. That's the number of 05:16

bits that one rank would output at a time in 05:16

response to a single read request. 05:16
BY MS. ZHONG: 05:17
Q. Okay. So the memory device access width, 05:17
WA, is the number of bits that one rank of memory 05:17
devices would output at a time in response to a 05:17
single read request, correct? 05:17
A. I believe so, yes. 05:17
Q. And the memory device access width, WA, is 05:17
also the number of bits that one rank of memory 05:17
devices would score at a time in response to a 05:17
single write request; is that right? 05:17
A. Yes. 05:17
Q. What other WAs that's described in Perego, 05:17
what are the specific memory device access width 05:18
that's referenced in Perego? 05:18
Let me withdraw and ask you a different 05:18
question. 05:18
So if you can go to Perego, column 14, 05:18
lines 10 through 15. 05:18
A. Okay. 05:19
Q. In this example, what is the memory access 05:19
bit width -- or memory device access width? 05:19
A. In this particular example it's 64 bits. 05:19
Q. It's 64 bits for each of the interface 05:19
520A and 520B, right? 05:19

A. Yes. 05:19
Q. So why isn't it 128? 05:19
A. Oh, yeah, it could be, yep. 05:19
Q. So the interface 520A and 520B can be operating concurrently; is that right? 05:19
A. Not concurrently. Sequentially, I believe. 05:19
Q. Sequentially? 05:19
A. Yeah. 05:19
Q. Okay. 05:19
A. I believe that -- 05:19
Q. They can't -- 05:19
A. I believe Perego describes both. 05:19
Q. Okay. When you say he describes both, what do you mean? Both as referring to what? 05:19 05:20
A. I believe that he says that they can operate either concurrently or one at a time. 05:20 05:20
Q. And is each interface 520A and 520B a channel as shown in Figure 4A or 4B then? 05:20 05:20
A. It's one or more channels. 05:20
Q. In Perego Figure 4A, do the channels operate concurrently or do they always operate at different times? 05:20 05:20 05:20
A. They certainly can operate at different times. I thought I recall a disclosure in Perego 05:21 05:21

that as an alternative they can operate concurrently. 05:21

Q. So if the channels are operating concurrently, say, in Figure 4A, how many ranks are there? 05:21

A. If they're operating concurrently there's only one. That would not be the embodiment that I relied on. 05:21

Q. Okay. So you have the line item embodiment where the channels are not operating concurrently? 05:22

MR. CHANDLER: Objection. Form. 05:22

THE WITNESS: I'm relying on an embodiment where each channel is one rank. 05:22

BY MS. ZHONG: 05:22

Q. Okay. So I think you mentioned that each channel can also operate sequentially. So if the sequential operation is in response to a single read request, does that mean there are two ranks of memory devices or just a single rank? 05:22

A. It wouldn't be a single request at the memory device. They could have been derived from a single request at the host because the host believes there's one rank. That's the core -- 05:23

Q. Okay. 05:23

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A. -- idea of rank multiplication is that the host believes it's talking to one rank. But in fact the logic splits the commands into two sets of commands so that in fact there are physically two ranks. 05:23

Q. Okay. So when you say they operate sequentially, that means one channel is responding to one of the -- how should I say it? -- decoded read request, and the second channel is responding to the second decoded read request; is that right? 05:23

MR. CHANDLER: Objection. 05:23

THE WITNESS: I think generated is a better term than decoded. But with that substitution, I would agree. 05:23

BY MS. ZHONG: 05:24

Q. So when you define a rank to say that it is "a subset of one or more memory devices on a memory module that act together in response to command signals, including chip select signals, to read or write the full bit width of the memory module," which command signals are you referring to? The command signal that's being sent from the host or the one that's regenerated? 05:24

A. The one that's provided to the memory devices, which in the case of the claimed devices 05:24

would be the one that's being generated. 05:24

Q. Does that mean the command signal that's received from the host system is different from a command signal that's being sent to the memory device then? 05:25

MR. CHANDLER: Objection. Form. 05:25

THE WITNESS: It can be. It can be. Because it believes that it's talking to a single rank when in fact it's talking to multiple ranks in -- in the real world. So that may require just replicating the signal at different times or it may require modifying it. 05:25

BY MS. ZHONG: 05:25

Q. But I thought you said a command signal only does not include bank addresses or row addresses. It only includes signals like chip select and RAS, CAS, and WE; is that right? 05:25

A. Correct. So the alteration would be the time at which those pins are asserted. That's how they're generated as being -- by having them be asserted at a different time for the different ranks. 05:26

Q. And you also said that for -- to send the command signals to DDR2 or DDR device, chip select signals need not be received, but it can be 05:26

generated internally by some logic on the memory module; is that correct? 05:27

MR. CHANDLER: Objection. Form. 05:27

THE WITNESS: I'm not sure I understand the question. 05:27

BY MS. ZHONG: 05:27

Q. Okay. I thought you mentioned earlier that the -- in response to description in Perego, that Perego is using addresses to select a subset of the memory devices. I thought you said chip select signals can be generated based on those received address bits and there need not be a separate chip select signal; is that correct? 05:27

MR. CHANDLER: Objection. Form. 05:27

THE WITNESS: I don't recall the context of that comment. 05:28

I think what I might have said is that there doesn't have to be a separate chip select wire in every embodiment. But there has to be a -- something that selects the chip. 05:28

BY MS. ZHONG: 05:28

Q. But the chip select signal can be generated internally on the memory module in response to the information it receives; is that correct? 05:28

MR. CHANDLER: Objection. Form. 05:28
THE WITNESS: Again, it depends on the 05:28
embodiment, but I think that that could -- could be 05:29
done. Not necessarily that that would be the normal 05:29
way that anybody would implement Perego, but I think 05:29
conceivably that could be done. 05:29
BY MS. ZHONG: 05:29
Q. Okay. So let's go back to Perego, column 05:29
15, line 37 to 40. Are you there? 05:29
A. Yes. 05:29
Q. So in that instance, the subset of the 05:29
signal lines are selected via address bits; is that 05:29
right? 05:29
MR. CHANDLER: Objection. Form. 05:29
THE WITNESS: In that one very special 05:30
case and that one embodiment, you can select a 05:30
target subset of secondary channel signal lines via 05:30
address bits and -- 05:30
BY MS. ZHONG: 05:30
Q. By selecting -- 05:30
MR. CHANDLER: Objection. I don't think 05:30
he was done. I don't think he was done with his 05:30
answer. 05:30
THE WITNESS: I don't think you would 05:30
enable specific devices based on address bits alone. 05:30

BY MS. ZHONG: 05:30

Q. Okay. But by selecting a subset of 05:30

secondary channel signals, are you selecting a 05:30

particular group of devices to respond to a single 05:30

read or write request? 05:30

MR. CHANDLER: Objection. Form. 05:31

THE WITNESS: I don't think so. Not in 05:31

that situation. I think that that's specific to 05:31

channel signal lines. 05:31

BY MS. ZHONG: 05:31

Q. So you don't think this is describing 05:31

grouping devices into independent target subsets? 05:31

MR. CHANDLER: Objection. Form. 05:31

BY MS. ZHONG: 05:31

Q. So why don't you read a few lines down, 05:31

column 7, lines 40 to 45. 05:31

A. Again, I don't think it has to do with 05:31

enabling or disabling devices. I think it simply 05:31

has to do with being able to impact the number of 05:31

independent banks that are open at a time. 05:31

Q. When you say "independent banks," which -- 05:31

what do you mean? 05:31

A. It would mean the number of page registers 05:32

which can be activated corresponding to different 05:32

addresses. 05:32

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Q. But all these are in a single rank? 05:32
A. No. I think this is talking about 05:32
throughout the system. 05:32
Q. So you don't think this paragraph has 05:32
anything to do with grouping devices into different 05:32
ranks? 05:32
MR. CHANDLER: Objection. Form. 05:32
THE WITNESS: I do not think that this 05:32
paragraph specifies how ranks are selected or 05:32
enabled. 05:32
BY MS. ZHONG: 05:32
Q. Does Perego discuss how different ranks 05:32
are selected or enabled? 05:32
A. I believe so. You have to look back at 05:33
what I referenced in my declaration. 05:33
Q. I did a search for the word "rank" in 05:33
Perego and I came up empty handed. Do you recall -- 05:33
A. I think that's right. I think we already 05:33
talked about this. I believe Perego does not use 05:33
the specific word even though he clearly discloses 05:33
the concept. 05:33
Q. And the concept being in response to a 05:33
single read or write operation it outputs a certain 05:33
number of bits? Is that what you're referring to? 05:33
A. Yes, one or more memory devices that 05:33

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respond to a single operation. 05:33

Q. So if Perego uses DDR or DDR2 devices, how many address bits would it need in order to perform a read -- like how many control signal bits would it need in order to perform a read operation, for example? 05:34

MR. CHANDLER: Objection. Form. 05:34

THE WITNESS: That would depend on the particular devices that were chosen and how many of them were chosen. 05:34

BY MS. ZHONG: 05:34

Q. So let's say it's a x8 DDR2 device. 05:34

A. It still depends on how many of them are used, how many are used per rank, and what the capacity of each device is. 05:35

Q. I thought for a read operation all the devices in a rank are deselected, correct? 05:35

A. Yes, but the number of address bits that are involved varies based on a number of factors that I've mentioned. 05:35

Q. Okay. So why don't we go to page 92 of your declaration. 05:35

A. Okay. 05:35

Q. And on page 92 you have listed six types of DDR2 device, correct? 05:35

A. Correct. 05:35
Q. Let's say for the 32Mbx16 DDR2 device for 05:35
a read operation, how many control address bits do 05:36
you need for a single read operation? 05:36
MR. CHANDLER: Objection. Form. 05:36
THE WITNESS: I'm not sure what you mean 05:36
by "control address bit." 05:36
BY MS. ZHONG: 05:36
Q. Oh, a command address bit. 05:36
MR. CHANDLER: Objection. Form. 05:36
THE WITNESS: I also don't know what you 05:36
mean by "command address bit." 05:36
BY MS. ZHONG: 05:36
Q. Well, on page 93 you have a command truth 05:36
table, correct? 05:36
A. Yes. 05:36
Q. So for a read and write operation you need 05:36
all the signals that's listed here, correct? 05:36
MR. CHANDLER: Objection. Form. 05:36
THE WITNESS: Not necessarily. It depends 05:37
how much memory you have. 05:37
BY MS. ZHONG: 05:37
Q. When you say depends on -- we are talking 05:37
about 32Mbx16 device? 05:37
A. Correct. For example, that device does 05:37

not use a 15, which is shown in Table 10. 05:37

Q. Okay. I'm just asking you, like, how many 05:37

bits do you need in order to define a read operation 05:37

for a memory module with 32Mbx16? 05:37

MR. CHANDLER: Objection. Form. 05:37

THE WITNESS: Are you asking me to assume 05:37

that that's the only memory chip on the module? 05:37

BY MS. ZHONG: 05:37

Q. Yes. 05:37

A. If you had a memory module with only a 05:37

single 32Mbx16 memory chip on it, then with respect 05:37

to the command and address signals that are shown in 05:38

Table 10, you would need one, two, three, four -- 05:38

five command signals, plus two bank address signals, 05:38

plus 13 address signals. 05:38

Q. So it's 13 plus 2 is 15, plus, you said, 05:38

five? 05:38

A. Of the signals that are listed -- of the 05:38

signals that are listed here. We'd have to go back 05:38

to Exhibit 1029. I'm sure there's other signals 05:38

that get provided that are more ancillary. 05:38

Q. Okay. If you have two 32Mbx16 memory 05:38

devices on the memory module, how many signal bits 05:38

do you need in order to perform a read operation? 05:39

A. It depends how they're configured. If 05:39

they're configured, you know, x32 configuration as a single rank, then you would need the same number of control and address signals from those listed in Table 10. 05:39

Q. So, again, 20 signals -- signal bits? 05:39

A. Correct. 05:39

Q. Would they be arranged in what you call two-rank configuration or a x16 bit width module? 05:39

MR. CHANDLER: Objection. Form. 05:39

THE WITNESS: Then you would need an additional chip select at least. 05:39

BY MS. ZHONG: 05:40

Q. Okay. So about 21. And so if I had four 32Mbx16 in four ranks, then I would need about 23 signals -- 05:40

A. From among those that are discussed. 05:40

MR. CHANDLER: Objection. Form. 05:40

BY MS. ZHONG: 05:40

Q. -- for a read -- okay. 05:40

A. From those discussed in Table -- sorry. 05:40

MR. CHANDLER: Objection. Form. 05:40

BY MS. ZHONG: 05:40

Q. And we're talking about x16 bit wide configurable -- but we're talking about a Perego memory module with 16 bit wide path, and you're 05:40

talking about using 23 signal bits? 05:40

MR. CHANDLER: Objection. 05:40

BY MS. ZHONG: 05:40

Q. How can you do that? 05:40

A. Well, none of your earlier questions had anything to do with Perego for the -- for one. But Perego contemplates a variety of different kinds of buses that can be used to connect to the host. 05:40 05:41 05:41

BY MS. ZHONG: 05:41

Q. I'm talking about Perego's configurable -- (indiscernible.) 05:41 05:41

THE REPORTER: I'm sorry. I'm sorry, Counsel, repeat your question, please. 05:41 05:41

BY MS. ZHONG: 05:41

Q. So in Perego with a WDP of 16, how would the 23 bits needed for a single read operation be sent or received by the memory module? 05:41 05:41 05:41

A. If you were to make all those assumptions and make that decision about Perego, Perego contemplates both interfaces to the host in which data and address share the interface or also where it's only the data that is configurable. 05:41 05:41 05:41 05:42 05:42

So certainly Perego contemplates modules in which the address and control lines are distinct from the configurable data lines. 05:42 05:42

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Q. Okay. So what you're saying is that when you say WDP is 16, it's only for the data bits? It doesn't include the control and signal bits; is that right? 05:42

A. In at least some of the embodiments that are disclosed by Perego. 05:42

Q. And the control and signal bits are sent on separate wires? 05:42

A. In at least some embodiments, yes. 05:42

Q. Okay. So in the x16 embodiment that you are relying on, if we are talking about data like memory bus, you are going to have a 23 bit wide -- at least a 23 bit wide control and signal pins and a 16 bit wide data path? 05:42 05:43 05:43

Is that what you're saying? 05:43

MR. CHANDLER: Object to form. 05:43

THE WITNESS: If you intended -- you would have -- at least in a JEDEC-style interface, you would have at least 23 command and address signals and at least 16 data signals in the situation in which you decided to have a 16 bit wide data bus in an embodiment of Perego. 05:43 05:43 05:43 05:43 05:43

BY MS. ZHONG: 05:43

Q. And the 16 bit wide data bus is the one you relied on in your example, correct? 05:44 05:44

A. I did rely on that in some of my examples. 05:44
Q. And did you discuss how the control and 05:44
address signals are sent and received by Perego's 05:44
DIMMs? 05:44
A. To the extent that they're tied to the 05:44
claim language I did. 05:44
Q. Can you point me to that? 05:44
A. Boy, you know, it's throughout my 50-plus 05:44
pages of description of how Perego matches the 05:44
claims. 05:45
One example is in paragraph 119. 05:45
Q. Okay. 05:45
A. But I discuss it repeatedly throughout 05:45
that section. Discussed it in paragraph 124, you 05:45
know. I know I extensively map it to the claims in 05:45
paragraphs 107 through 187. 05:45
Q. Okay. So in paragraph 119 did you discuss 05:45
whether the control address information on 05:45
controller is received in a packetized fashion or 05:45
whether it is -- (indiscernible.) 05:45
THE REPORTER: I'm sorry, Counsel, you're 05:46
fading again. "Controller is received"... 05:46
BY MS. ZHONG: 05:46
Q. So in paragraph 19 did you discuss whether 05:46
the control and address information is received in a 05:46

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packetized format, a parallel bus format, or otherwise? 05:46

A. Not in that particular paragraph I don't, no. 05:46

Q. Okay. 124, do you discuss it there? 05:46

A. I do. For example, I quote in -- on page 68 where Perego says that the "control lines may comprise individual control lines, for example, row address strobe, column address strobe, and address lines." 05:46 05:47

Q. Is that referring to the RQ between the secondary channel and device? 05:47

A. I think it's applicable to both RQs. Both the ones between the secondary channels and the device and also between the second device and the host. 05:47

Q. Does it call out a chip select signal? 05:47

A. Not in that particular citation it does not. 05:47

Q. And you have confirmed earlier that you don't see a description of chip select signal in Perego, correct? 05:48

MR. CHANDLER: Objection. Form. 05:48

THE WITNESS: I think I said that I didn't see a specific recitation of a -- of a signal called 05:48

chip select, but that a person of ordinary skill would understand that one is necessary if one implements it using the JEDEC standard for DDR memory devices. 05:48

BY MS. ZHONG: 05:48

Q. But then not the specific chip select wire; is that correct? 05:48

MR. CHANDLER: Objection. Form. 05:48

BY MS. ZHONG: 05:49

Q. Is that correct? 05:49

A. There's not one with that name. But that capability is, I believe, disclosed. And again, a person of ordinary skill would look to the JEDEC standard for the particular name of that signal with respect to implementing Perego. 05:49

Q. But there need not to be a specific pin for chip selection, correct? 05:49

MR. CHANDLER: Objection. Form. 05:49

THE WITNESS: Perego doesn't require one. But a person of ordinary skill in the art understanding JEDEC would be motivated to implement one. Certainly Perego talks about individual signals for control -- individual wires or lines for control signals. 05:49

BY MS. ZHONG: 05:49

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Q. Why would someone implement using -- 05:49
implement a memory module with only 16-bit-wide data 05:49
path but 23 bit and higher control path? 05:50
A. Because it can be economical and effective 05:50
to do so. Those are two independent decisions. 05:50
The control path is based on how many 05:50
different commands and how many different addresses 05:50
one needs to implement. And the data path is based 05:50
on the data bandwidth. 05:50
We can look at a real-world example in 05:50
Exhibit 1029 where JEDEC recommends building chips, 05:50
for example, that have more than 16 control signals 05:50
but only 16 data signals. 05:50
Q. That's on the device side but not on the 05:51
memory side? 05:51
THE REPORTER: I'm sorry, Counsel, one 05:51
more time. 05:51
BY MS. ZHONG: 05:51
Q. That's on the device side but not on the 05:51
memory module side, correct? 05:51
A. With respect to Exhibit 1029, that's true, 05:51
it is discussing devices. But the motivations would 05:51
be the same. 05:51
MS. ZHONG: Let's take a five-minute 05:51
break. 05:51

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MR. CHANDLER: All right. 05:51
(Recess.) 05:55
(Off record: 5:51 p.m.) 05:55
(On record: 5:55 p.m.) 05:55
MS. ZHONG: Thank you very much, 05:55
Dr. Wolfe. 05:55
I pass the witness. 05:55
MR. CHANDLER: Let's go off the record. 05:55
Let me review my notes to see what questions I may 05:55
have. 05:55
(Recess.) 05:59
(Off record: 5:59 p.m.) 05:59
(On record: 6:13 p.m.) 05:59

EXAMINATION

BY MR. CHANDLER: 06:12
Q. Dr. Wolfe, I'd like to follow up on 06:12
questions that counsel for Netlist asked you. 06:13
Starting with Exhibit 1037, the Ellsberry 06:13
reference. Could you pull up Exhibit 1037 and let 06:13
me know when you have it in front of you? 06:13
A. Okay. I have it. 06:13
Q. With reference to paragraph 31, as well as 06:13
Figure 2 and Figure 4, I want to ask some follow-up 06:13
questions to the questions you were asked. 06:13
Do you have that paragraph and those 06:13

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figures in front of you? 06:13

A. Yes. 06:13

Q. Does Ellsberry disclose an embodiment where for a write operation, the switch ASIC routes the data only through one port such as port B and not through the other port such as port A? 06:13 06:13 06:14 06:14

MS. ZHONG: Objection. Form. Leading. 06:14

THE WITNESS: It does. You can see it in paragraph 31. You can see it in Figure 8. And then I believe it's also claimed in Claim 1. 06:14 06:14 06:14

BY MR. CHANDLER: 06:14

Q. In your opinion, does Ellsberry in all of its embodiments always send write data through both port A and port B? 06:14 06:14 06:15

A. No. If you look at Figure 8, you can see that on a write, it enables -- it sends the data through port A on the first cycle and then through port B on the second cycle. And I think that that's suggesting that it's only that port during those cycles. 06:15 06:15 06:15 06:15 06:15

It also talks in paragraph 31 about disabling one of the ports so that it's written to the correct memory bank. 06:15 06:15 06:15

And then in Claim 1 it specifically says that it directs the data information to one of a 06:15 06:15

plurality of physical memory banks. 06:15

Q. Now, you were asked some questions about 06:15
paragraph 33. Is there an embodiment in 06:15
paragraph 33 where write data is sent to both 06:16
ports A and B? 06:16

A. Yes. It's the -- the -- let's see if I 06:16
remember what it's called. It's -- it's the 06:16
column-based embodiment. 06:16

Q. Okay. And is the column-based embodiment 06:16
of Ellsberry where data is sent through both ports A 06:16
and B, is that the only embodiment in Ellsberry or 06:16
is there a different embodiment where write data is 06:16
sent through only one port and the other port is 06:16
disabled? 06:16

A. Yeah, there's another embodiment -- 06:16

MS. ZHONG: Objection. 06:16

THE WITNESS: I'm sorry. 06:16

MS. ZHONG: Objection. Form. Leading. 06:17

THE WITNESS: There's another embodiment 06:17
that we talked about before that's described at the 06:17
end of paragraph 33 that says, "When row/bank mode 06:17
addressing is used, read and write commands are sent 06:17
only to the targeted memory device. A no-op 06:17
operation command is sent to the non-targeted memory 06:17
device." 06:17

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If you look at that particular mode in Figure 8, you can see that the data as well is only sent to a particular port. 06:17

BY MR. CHANDLER: 06:17

Q. Is the row/bank mode used for both write operations and read operations in Ellsberry? 06:17

A. Yes. 06:17

Q. When using the row/bank mode in Ellsberry for a write operation, does Ellsberry disclose an embodiment where one port is enabled to transfer the data to the memory devices but the other port is disabled and does not transfer the data to the memory devices? 06:17

MS. ZHONG: Objection. Form. Leading. 06:18

THE WITNESS: Yes, it's my understanding that it does. 06:18

BY MR. CHANDLER: 06:18

Q. Could you look at paragraph 12 and Figure 4? I want to follow up on some questions you were asked about presenting a single load to the bus. 06:18

Just let me know when you have that paragraph and Figure 4 in front of you. 06:18

A. Okay. 06:19

Q. Does Figure 4 as drawn present exactly a 06:19

single load to the bus going to the memory controller on the host computer? 06:19

A. Well, as I said before, I think a person of ordinary skill in the context of the patent would understand that it does because they would understand that the load is from the pin. 06:19

And pins on a chip always have a pin driver circuit. One would presume that there is one here. And it would be that pin driver circuit at 230 that actually provides the load. And that would be a -- in this case because it's bidirectional -- a transceiver. It would be a circuit that could do both tri-state driving and also input buffering. 06:19

Q. Does Figure 4 of Ellsberry expressly draw the pin driver circuit that you just described that would present only a single load on bus 230 to the host computer? 06:19

MS. ZHONG: Objection. Form. Leading. 06:20

THE WITNESS: No. It -- it shows the pins, but it doesn't expressly show the pin driver. It doesn't expressly show pin drivers for any of the pins, but one would expect them to be there. 06:20

BY MR. CHANDLER: 06:20

Q. If there was no pin driver in Figure 4, and instead bidirectional drivers 402 and 404 were 06:20

connected directly to bus 230 to the memory controller on the host computer, would that present precisely a single load to the host computer? 06:20

MS. ZHONG: Objection. Form. Leading. 06:21

THE WITNESS: No. As I mentioned before in my testimony, there would be some additional load from having those two devices directly connected there. 06:21

BY MR. CHANDLER: 06:21

Q. So if a person of ordinary skill in the art wanted to implement Figure 4 of Ellsberry and present precisely a single load on bus 230 to the memory controller on the host computer, would they need to include the pin driver circuit that you mentioned in addition to the other circuitry expressly shown in Figure 4? 06:21

MS. ZHONG: Objection. Form. Leading. 06:22

THE WITNESS: Yes, they would, if you wanted to have exactly one load -- and this is commonly done -- you would have a pin driver circuit. 06:22

Again, since this is bidirectional, we would typically call it a pin driver. But to be specific, it would include both a pin driver and an input buffer. 06:22

BY MR. CHANDLER: 06:22

Q. How would that pin driver compare to whatever circuitry would be on the memory device at its input/output pins? 06:22

MS. ZHONG: Objection. Form. 06:23

THE WITNESS: To my knowledge, all memory devices use a pin driver, so it would be essentially identical. 06:23

BY MR. CHANDLER: 06:23

Q. And what would be the benefit of having a pin driver in Figure 4 of Ellsberry on the bus 230 connecting to the memory controller, that would be, in your words, essentially identical to the pin driver that would exist on the memory device itself? 06:23

MS. ZHONG: Objection. Form. Leading. 06:23

THE WITNESS: By this point in time, memory controllers are very highly tuned in their signaling. So they expect a particular loading at the other end of the wire. And the advantage would be that it would be consistent with connecting memory chips directly to the memory controller in the way that one would do if they didn't have rank multiplication. So it would be much more likely to be compatible. 06:24

MR. CHANDLER: Thank you, Dr. Wolfe. 06:24

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Pass the witness. 06:24

FURTHER EXAMINATION

BY MS. ZHONG: 06:24

Q. Dr. Wolfe, did you speak with your counsel during break? 06:24

A. Yes. 06:24

Q. Did the discussion have anything to do with the redirect that we just had? 06:25

MR. CHANDLER: Objection. Privileged. 06:25

Instruct the witness not to answer. 06:25

THE WITNESS: I'm going to comply with my counsel's instructions. 06:25

BY MS. ZHONG: 06:25

Q. Did you rely on any of the discussion with counsel in your response in the redirect? 06:25

A. No. 06:25

Q. Did you have an understanding as to the kind of questions you would be asked during the redirect? 06:25

MR. CHANDLER: Objection. Privileged. 06:25

Instruct the witness not to answer. 06:25

MS. ZHONG: Well, I'm asking what his understanding is. 06:25

Q. So, Dr. Wolfe, did you have an understanding as to what kind of questions you would 06:25

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be asked during redirect? 06:25
MR. CHANDLER: Objection. Privileged. 06:26
Instruct the witness not to answer. 06:26
THE WITNESS: I'm going to comply with the 06:26
instruction not to answer. 06:26
BY MS. ZHONG: 06:26
Q. Dr. Wolfe, you are not answering because 06:26
you had an inkling of what questions would be asked, 06:26
correct? 06:26
MR. CHANDLER: Objection. Privileged. 06:26
Instruct the witness not to answer. 06:26
THE WITNESS: I'm not answering because I 06:26
was instructed not to answer. 06:26
MS. ZHONG: We will move and ask the Court 06:26
to have you be reproduced to answer the questions. 06:26
I'll make it clear on the record. 06:26
Q. Dr. Wolfe, how much additional load would 06:26
the driver -- let's go back to Figure 4 of 06:26
Exhibit 1037. 06:26
A. Yes. 06:26
Q. You stated, without the pin driver a 06:27
person of ordinary skill in the art would still 06:27
consider the load at 230 as a single load, correct? 06:27
MR. CHANDLER: Objection. Form. 06:27
THE WITNESS: I think what I already said 06:27

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is that there would normally be a pin driver. If there was not one, then you could have a higher load based on the connection to multiple circuits. 06:27

BY MS. ZHONG: 06:27

Q. And my understanding is that you said there would be the two -- by combining 234 and 236 into 230, there would exactly be one load plus some loads for 402 and 404; is that correct? 06:27

MR. CHANDLER: Objection. Form. 06:27

THE WITNESS: No. If I said that, I was not being precise. By combining them, what you're doing is having them share the same pin driver. And if you have them share the same pin driver, then there would be one load. If somehow you designed it without a pin driver, then -- then there would be more than one load. 06:27 06:28 06:28 06:28

BY MS. ZHONG: 06:28

Q. How many loads? 06:28

A. It depends on the details of the circuit, but nominally somewhere around two. 06:28

Q. And a port is the exit -- is at the exit of ASIC, correct? 06:28

A. I didn't get the last couple words. I'm sorry. 06:28

Q. A port is at the exit of the ASIC; is that 06:28

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correct? 06:28

A. It's at the interface. It could be an 06:28

exit. It could be an entrance. It could be both. 06:29

It's -- it's at -- the port is -- is at the pin. 06:29

It's the interface between the ASIC and the outside 06:29

world. 06:29

Q. Okay. And I think you analogized a port 06:29

as a bowl to the ASIC; is that correct? 06:29

A. I don't know if I analogized it, but I did 06:29

say that that was the historical derivation of the 06:29

word from my understanding. 06:29

Q. So when you disable a port, you can 06:29

basically just shut that door as the interface; is 06:29

that correct? 06:29

A. In a very general sense. In this case, it 06:29

would be more like turning off the drivers at the 06:29

pin. 06:29

Q. Are you referring -- when you say "the 06:30

drivers," you are not referring to the drivers 402 06:30

and 404, are you? 06:30

A. No. Usually they would be pin drivers. 06:30

Q. Okay. So you are referring to the pin 06:30

drivers at port A and B? 06:30

A. Yeah, that would be the normal way to do 06:30

it. 06:30

Q. Okay. So when port A is disabled, that just means the pin driver connected to the port A pad is disabled; is that right? 06:30

A. Yes, that's generally the case. If we're talking about the output functions of port A, then that would be what we would be talking about. 06:30

Q. And when you have a write operation, even if data is only sent to the memory rank connected to port A, can the data path on port B still be open? 06:30

MR. CHANDLER: Objection. Form. 06:31

THE WITNESS: I'm not sure what you mean by "open." 06:31

BY MS. ZHONG: 06:31

Q. You said 404 could be disabled, correct? 404 -- 06:31

A. There is an embodiment in Perego where in a write operation port A is enabled and port B is disabled on the first cycle. And then on the subsequent cycle, port B is enabled and port A is disabled. 06:31

Q. Okay. And port A is enabled means the pin driver is enabled, and the port B is disabled means the pin driver for port B is disabled; is that right? 06:32

A. In that particular situation, it's 06:32

correct. 06:32

Q. Okay. But the path between 230 and 234 06:32

can still be open as well as a path between 230 and 06:32

236, correct? Just that the -- 06:32

MR. CHANDLER: Object. 06:32

BY MR. TEZYAN: 06:32

Q. -- to the memory bank, that one can be 06:32

shut down -- shut, correct? 06:32

MR. CHANDLER: Objection. Form. 06:32

THE WITNESS: I don't think it would make 06:33

sense to do that because -- well, in part, if -- 06:33

if -- well, you're definitely driving the signal out 06:33

to port 234. 06:33

It could be latched in the flip-flop in 06:33

404, but it's not being sent out of port B. In 06:33

other words, it's not -- it's not going to be 06:33

leaving the chip on a second port. So it's -- it's 06:33

irrelevant. 06:33

BY MS. ZHONG: 06:33

Q. And it could be -- 06:33

A. I don't think you would enable the entire 06:33

path because 236 includes the external of the chip. 06:33

But you could have a portion of the path that was 06:33

operable. 06:33

Q. Okay. So can I enable up to the exit of 06:33

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the ASIC on 236 and just basically turn off the pin driver at the point of exit? 06:33

MR. CHANDLER: Objection. Form. 06:33

THE WITNESS: I don't see that disclosed, but you could. As long as you don't drive it off the chip, nothing outside the chip -- or actually nothing would ever know what you were doing on that particular wire because it would be disabled and it's not connected to anything. 06:34

BY MS. ZHONG: 06:34

Q. Okay. So -- so long as that wire 236 reaches the chip anywhere before that if I turned it off, then that would comply with the description of data is only sent to port A but not to port B? 06:34

MR. CHANDLER: Objection. Form. 06:34

THE WITNESS: So 236 isn't a single wire. It's -- it's a bus. And it -- it's going to involve some wires going to the port pins and then some wires extending from the port pins off to the memory. And if the port pins are disabled, as long as you don't send anything from -- off the chip. As long as you don't send anything to the memories, it doesn't matter what you would do on the disconnected wires internally. But again, I don't see any disclosure that you do drive anything there. 06:34 06:35 06:35 06:35 06:35

BY MS. ZHONG: 06:35

Q. Okay. So you can -- Ellsberry does not -- 06:35

is kind of being different as to where the 06:35

disablement occurs. For example, it can occur 06:35

outside of the ASIC on bus 236 so long as it's 06:35

before it reaches the memory bank; is that right? 06:35

MR. CHANDLER: Objection. Form. 06:35

THE WITNESS: No. Ellsberry is specific. 06:35

It happens at the port. It happens at the point 06:35

that signals are able to leave the chip. So that is 06:35

what is disabled. 06:36

BY MS. ZHONG: 06:36

Q. Okay. So if -- so if it is disabled at 06:36

the exit, which is the interface, that's what 06:36

Ellsberry is teaching? 06:36

MR. CHANDLER: Objection. Form. 06:36

THE WITNESS: In the embodiment in which 06:36

ports A and ports B are sequentially disabled, they 06:36

are disabled at the port, at the interface to the 06:36

chip, to the ASIC chip, so that signals do not enter 06:36

or leave the chip on that port. 06:36

BY MS. ZHONG: 06:36

Q. Okay. So it's at the interface of the 06:36

chip? It's not internal to the chip? 06:36

MR. CHANDLER: Objection. Form. 06:36

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THE WITNESS: The teaching is that it's disabled at the interface. There's no specific teaching as -- as to what happens on wires that go to the interface. 06:36

BY MS. ZHONG: 06:36

Q. Okay. So all Ellsberry said when he disabled the port, a person of ordinary skill in the art would understand that means disabling the bus at the point of the interface? 06:37

MR. CHANDLER: Objection. Form. 06:37

THE WITNESS: Yes, in such a way that those signals are not provided anywhere where the port is disabled. 06:37

BY MS. ZHONG: 06:37

Q. Okay. So the disablement occurs at the ASIC interface, correct? 06:37

MR. CHANDLER: Objection. Form. 06:37

THE WITNESS: That is the teaching, yes. It may occur in other places as well for engineering reasons. 06:37

BY MS. ZHONG: 06:37

Q. But what's expressly disclosed in Ellsberry is the disablement occurs at the interface of the ASIC chip? 06:37

MR. CHANDLER: Object to form. 06:38

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THE WITNESS: Yes, in such a way that those signals are not provided to any other device or any other circuit. 06:38

MS. ZHONG: Okay. I don't have any further questions other than the questions that you refused to answer. 06:38

And this concludes today's deposition. 06:38

MR. CHANDLER: And we'd like a copy of the transcript to be able to review, make corrections, if appropriate, by Friday. 06:38

(At the time of 6:38 p.m. the deposition was concluded.)

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DECLARATION

I hereby declare I am the deponent in the within matter; that I have read the foregoing transcript and know the contents thereof; and I declare that the same is true of my knowledge except as to the matters which are therein stated upon my information or belief, and as to those matters, I believe them to be true.

I declare under the penalties of perjury under the laws of the United States that the foregoing is true and correct.

This declaration is executed this _____ day of _____, 20___, at

_____ _____

CITY STATE

_____

ANDREW WOLFE, PH.D.

C E R T I F I C A T E

I, the undersigned, a Certified Shorthand Reporter for the State of California, do hereby certify:

That the foregoing proceedings were taken before me at the time and place herein set forth; that a verbatim record of the proceedings was made by me using machine shorthand, which was thereafter transcribed under my direction; further, that the foregoing is an accurate transcription thereof.

I further certify that I am neither financially interested in the action nor a relative or employee of any attorney of any of the parties.

IN WITNESS THEREOF, I have this date subscribed my name this 6th day of January, 2023.



ASHALA TYLOR, CLR, RPR, CRR, CSR #2436

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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD., MICRON TECHNOLOGY, INC., MICRON SEMICONDUCTOR PRODUCTS, INC., and MICRON TECHNOLOGY TEXAS LLC,[†]

Petitioner,

v.

NETLIST, INC.,

Patent Owner.

IPR2022-00615

Patent 9,619,912 B2

ERRATA TO THE DEPOSITION OF ANDREW WOLFE (JANUARY 4, 2023)

[†] Micron Technology, Inc., Micron Semiconductor Products, Inc., and Micron Technology Texas LLC filed a motion for joinder and a petition in IPR2023-00203 and have been joined as petitioners in this proceeding.

I, ANDREW WOLFE, have read the transcript of my deposition taken on January 4, 2023. Listed below are changes to the transcript that I wish to make and the reasons for making them:

Page:Line	**Now Reads**	**Should Read**	**Reason for Change**
1:16, 2:16	Videotaped deposition	Deposition	I don't think the deposition was videotaped.
16:1	check select signals	chip select signals	Typographical error
16:3–:5	There are other documents, the ones intended to review together with this, that describe how these signals are used in more detail.	There are other documents, that one's intended to review together with this, that describe how these signals are used in more detail.	Typographical error
34:6–:7	that was not relevant to my analysis in.	that was not relevant to my analysis.	Typographical error
41:18	small outlying DIMMs	small outline DIMMs	Typographical error
42:10–:13	But I can go to a number of different memory model manufacturers and get Rambus compliant memory modules in the 2000 to 2005 time period.	But I can go to a number of different memory module manufacturers and get Rambus compliant memory modules in the 2000 to 2005 time period.	Typographical error
44:5–:6	What's the bit width of JEDEC compliant memory modules at the time? 564?	What's the bit width of JEDEC compliant memory modules at the time? x64?	Typographical error

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Page:Line	**Now Reads**	**Should Read**	**Reason for Change**
48:9–:15.	And as memory densities increased, we began to get chips with 4 and 8 banks on them. So because there was a desire to distinguish the vocabulary for that kind of a memory bank from the earlier kind of a memory bank, memory providers started to use the word "rank" to describe the one or more chips on a module that would simultaneously respond to a command.	[see note]	No change, but for clarity, "the earlier kind of a memory bank" refers to the discussion at 46:20–47:7.
59:3–:4	I think it's simply another description of the same concept.	[see note]	No change, but this was clarified at 59:6–:20.
64:2–:3	band address signals, chip select signals, CAS bar, RAS bar, and right enable bar	bank address signals, chip select signals, CAS bar, RAS bar, and write enable bar	Typographical errors

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Page:Line	Now Reads	Should Read	Reason for Change
67:5–:8	Q. Okay. So, for example, it does not have the CS signal, the CAS, RAS -- let's go to page 16 of Exhibit 1032. A. Uh-huh.	[see note]	No change, but for clarity, I was not answering the unfinished question here, I was just agreeing to the request to look at page 16, and my answer to the question was provided at 67:13–:18.
71:9–:11	it would be ordinarily for that DIMM to be provided with a bank address signal	it would be ordinary for that DIMM to be provided with a bank address signal	Typographical error
73:24–74:1	It would be ordinary to send those to an ordinary personal computer in DDR or DDR2 module at that time.	It would be ordinary to send those from an ordinary personal computer to DDR or DDR2 modules at that time.	Typographical errors
80:10–:11	may be select via address bits	may be selected via address bits	Typographical error
80:23–:24	MR. CHANDLER: Court Reporter, I said address bits, B-I-T-S	MS. ZHONG: Court Reporter, I said address bits, B-I-T-S	Typographical error
87:22	four device slide ranks	four device wide ranks	Typographical error
105:24	costs to that memory	costs of that memory	Typographical error
108:10	In Table 1, follows 2, 3, 4, and 5 have the headings CS0, CS1, An+1 and Control.	In Table 1, columns 2, 3, 4, and 5 have the headings CS0, CS1, An+1 and Control.	Typographical error

Page:Line	Now Reads	Should Read	Reason for Change
116:22	where are the advance signals sent	where are the address signals sent	Typographical error
117:7	It's simply register.	It's simply a register.	Typographical error
118:2–:6	But sequential logic implements what we call state machines, which are time-variant logic functions that can perform different logic equations at different points in time based on the storage of what we call state partial results.	But sequential logic implements what we call state machines, which are time-variant logic functions that can perform different logic equations at different points in time based on the storage of what we call state register values.	Typographical error
123:7	single D rank or a rank of D rank	single DRAM or a rank of DRAM	Typographical error
136:22–:23	rent multiplication	rank multiplication	Typographical error
137:24–138:1	the four CAS signals coming out of element 640 would represent select signals for each of the four ranks	[see note]	No change, but this was later clarified at 140:4–141:7.

Page:Line	Now Reads	Should Read	Reason for Change
139:16–:21	Q. It is either a row or a column address it? Is that correct, Dr. Wolfe? A. Yes, or depending on the particular DRAM generation. It could be both. Q. So it is a row, column, or both a row and column address it?	Q. It is either a row or a column address bit? Is that correct, Dr. Wolfe? A. Yes, or depending on the particular DRAM generation, it could be both. Q. So it is a row, column, or both a row and column address bit?	Typographical errors
140:18–:19	which of the four ranks, 620, 625, 630 and 635, as active	which of the four ranks, 620, 625, 630 and 635, is active	Typographical error
148:12	Or desktop personal computers	On desktop personal computers	Typographical error
149:25	They would generally use a 72.	They would generally use x72.	Typographical error
160:7–:8	paragraph 28 states that its memory bank 206 and 208	paragraph 28 states that it's memory bank 206 and 208	Typographical error
161:8–:9	those would be what we would today call banks	those would be what we would today call ranks	Typographical error
161:19	activated operation	activate operation	Typographical error
166:17	DRAM boot	DRAM group	Typographical error

Page:Line	**Now Reads**	**Should Read**	**Reason for Change**
170:23–:25	Yes, my understanding that memory bank in paragraph 41 is referring to what we would typically call a rank today.	Yes, my understanding is that memory bank in paragraph 41 is referring to what we would typically call a rank today.	Typographical error
173:9–:10	Perego discloses both point-to-point end buses	Perego discloses both point-to-point and buses	Typographical error
174:11	multiple paths	multiple pads	Typographical error
179:6–180:10	Q. So in Figure 4 of Ellsberry, at the -- at the point of where DQ (7:0) and DQS is, there's only a single load; is that right? A. That's what Ellsberry tells us. …. I think what he's doing is he's recognizing that the vast majority of the load comes from the physical presence of pins and not from internal circuits. And what he's done is now he no longer has two sets of pins on those wires but only one set of pins from the switch chip in Figure 4.	[see note]	No change, but this was later clarified at 218:18–221:24, 223:21–224:20.

Page:Line	**Now Reads**	**Should Read**	**Reason for Change**
180:17–:18	only one of the bands is activated	only one of the ranks is activated	Typographical error
193:25	depends on the considerable bit width	depends on the configurable bit width	Typographical error
195:10–:17	And the memory access bit width, WA, that is the number of bits the memory module would output in response, for example, to a single read command from the computer system; is that right? MR. CHANDLER: Objection. Form. THE WITNESS: Yes, but Perego calls it the memory device access width.	[see note]	No change, but this was clarified at 195:19–196:7.
196:10	would score	would store	Typographical error
205:16–:17	for a read operation all the devices in a rank are deselected	for a read operation all the devices in a rank are selected	Typographical error
207:1	not use a 15	not use A15	Typographical error
225:7–:8	you analogized a port as a bowl	you analogized a port as a door	Typographical error

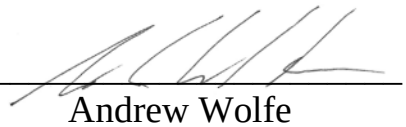
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Page:Line	**Now Reads**	**Should Read**	**Reason for Change**
226:16–:18	There is an embodiment in Perego where in a write operation port A is enabled and port B is disabled	There is an embodiment in Ellsberry where in a write operation port A is enabled and port B is disabled	Misspoke

I hereby certify that the transcript of my deposition on January 4, 2023, as corrected above, is a true and accurate transcription of my testimony.

I, Andrew Wolfe, do hereby declare and state, that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, under Section 1001 of Title 18 of the United States Code.

Executed on: August 9, 2023



Andrew Wolfe

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Federal Rules of Civil Procedure

Rule 30

(e) Review By the Witness; Changes.

(1) Review; Statement of Changes. On request by the deponent or a party before the deposition is completed, the deponent must be allowed 30 days after being notified by the officer that the transcript or recording is available in which:

(A) to review the transcript or recording; and

(B) if there are changes in form or substance, to sign a statement listing the changes and the reasons for making them.

(2) Changes Indicated in the Officer's Certificate. The officer must note in the certificate prescribed by Rule 30(f)(1) whether a review was requested and, if so, must attach any changes the deponent makes during the 30-day period.

DISCLAIMER: THE FOREGOING FEDERAL PROCEDURE RULES ARE PROVIDED FOR INFORMATIONAL PURPOSES ONLY. THE ABOVE RULES ARE CURRENT AS OF APRIL 1, 2019. PLEASE REFER TO THE APPLICABLE FEDERAL RULES OF CIVIL PROCEDURE FOR UP-TO-DATE INFORMATION.

VERITEXT LEGAL SOLUTIONS
COMPANY CERTIFICATE AND DISCLOSURE STATEMENT

Veritext Legal Solutions represents that the foregoing transcript is a true, correct and complete transcript of the colloquies, questions and answers as submitted by the court reporter. Veritext Legal Solutions further represents that the attached exhibits, if any, are true, correct and complete documents as submitted by the court reporter and/or attorneys in relation to this deposition and that the documents were processed in accordance with our litigation support and production standards.

Veritext Legal Solutions is committed to maintaining the confidentiality of client and witness information, in accordance with the regulations promulgated under the Health Insurance Portability and Accountability Act (HIPAA), as amended with respect to protected health information and the Gramm-Leach-Bliley Act, as amended, with respect to Personally Identifiable Information (PII). Physical transcripts and exhibits are managed under strict facility and personnel access controls. Electronic files of documents are stored in encrypted form and are transmitted in an encrypted fashion to authenticated parties who are permitted to access the material. Our data is hosted in a Tier 4 SSAE 16 certified facility.

Veritext Legal Solutions complies with all federal and State regulations with respect to the provision of court reporting services, and maintains its neutrality and independence regardless of relationship or the financial outcome of any litigation. Veritext requires adherence to the foregoing professional and ethical standards from all of its subcontractors in their independent contractor agreements.

Inquiries about Veritext Legal Solutions' confidentiality and security policies and practices should be directed to Veritext's Client Services Associates indicated on the cover of this document or at www.veritext.com.