

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD, MICRON TECHNOLOGY, INC.,
MICRON SEMICONDUCTOR PRODUCTS, INC., and
MICRON TECHNOLOGY TEXAS LLC,
Petitioner,

v.

NETLIST, INC.,
Patent Owner.

IPR2023-00454 (Patent 11,093,417 B2)
IPR2023-00455 (Patent 9,858,215 B1)

Record of Oral Hearing
Held: May 3, 2024

Before GEORGIANNA W. BRADEN, JON M. JURGOVAN, and
DANIEL J. GALLIGAN, *Administrative Patent Judges*.

IPR2023-00454 (Patent 11,093,417 B2)

IPR2023-00455 (Patent 9,858,215 B1)

APPEARANCES:

ON BEHALF OF THE PETITIONER:

THEODORE CHANDLER, ESQ.

Baker Botts L.L.P.

101 California Street

Suite 3200

San Francisco, CA 94111-5802

ted.chandler@bakerbotts.com

(415) 291-6259

ON BEHALF OF THE PATENT OWNER:

MICHAEL HEIM, ESQ.

Heim Payne & Chorush

609 Main Street

Suite 3200

Houston, TX 77002

mheim@hpcllp.com

(713) 221-2001

The above-entitled matter came on for hearing on Friday, May 3, 2024, commencing at 12:00 p.m., via video teleconference.

P R O C E E D I N G S

- - - - -

JUDGE GALLIGAN: This is an oral argument for IPR2023-00454 and IPR 2023-00455, which involve respectively U.S. Patents 11,093,417 B2 and 9,858,215 B1. The Petitioner is Samsung Electronics Company Limited, and we have joined Petitioners Micron Technology Inc., Micron Semiconductor Products Inc., and Micron Technology, Texas, LLC. The Patent Owner is Netlist, Inc. I'm Administrative Patent Judge Galligan, and with me are APJs Braden and Jurgovan. Can we have appearances starting with Petitioner for counsel for Petitioner Samsung, please?

MR. CHANDLER: Good morning, Your Honor. This is Ted Chandler from Baker Botts on behalf of the Petitioner, Samsung. With me is lead counsel Eliot Williams and our colleague, Dr. Ferenc Pazmandi. Counsel for Micron is also on the line, and I believe would like to introduce himself.

JUDGE GALLIGAN: Micron, sorry, Micron's counsel, please.

MR. YAQUIAN: Hi, Your Honors. This is Juan Yaquian here from Winston and Strawn on behalf of Micron.

JUDGE GALLIGAN: Thank you. And Mr. Chandler, Samsung's counsel will be presenting, correct?

MR. CHANDLER: Correct. I'll be presenting on behalf of the Petitioner.

JUDGE GALLIGAN: Great. And Patent Owner, please.

MR. HEIM: Yes. Michael Heim with Heim Payne & Chorush, representing the Patent Owner, Netlist. With me today is lead counsel, Annita Chong, and Chris Limbacher from Heim Payne & Chorush as well.

1 JUDGE GALLIGAN: Thank you, Mr. Heim. So, in the oral
2 hearing order, we granted each side 90 minutes of argument time for these
3 cases combined and our first priority is your right to be heard. So, if at any
4 time during the hearing, you encounter technical or other difficulties that
5 you feel undermine your ability to adequately represent your client, please
6 let us know immediately. And you may do this by contacting the team that
7 provided you with the hearing information.

8 If you stop hearing and drop off, please let us know or try to note
9 what was being discussed and so we can figure out where to pick up. Please
10 mute your microphone and only unmute when you're speaking. Please
11 identify yourself when you speak so that the transcript accurately reflects the
12 speaker. When referring to an item in the record, please do so with
13 specificity so that the panel can follow along and for clarity in the transcript.
14 So, even if you're presenting the slides, please note the slide number. There
15 is a public line for this, and we are not aware of any confidential
16 information. And finally, I wanted to ask Patent Owner just to pronounce
17 the name of your technical declarant. I wanted the record to reflect, and I
18 want to make sure that I get it right when I refer to him.

19 MR. HEIM: I think you're referring to Dr. Przybylski.

20 JUDGE GALLIGAN: Przybylski. Great. Okay. That's it. Thank
21 you very much.

22 MR. HEIM: Yes.

23 JUDGE GALLIGAN: And actually, for the court reporter's
24 benefit, can you please spell that? I think I have it here.

25 MR. HEIM: It's going to be a test. Let me see if I can.

26 JUDGE GALLIGAN: Never mind. I can do it real quick. I just

1 wanted the court reporter to know what we're referring to. It's Steven and
2 then it's P-R-Z-Y-B-Y-L-S-K-I. And that's Przybylski.

3 MR. CHANDLER: And it's also on slide 24 on the screen on the
4 bottom left.

5 JUDGE GALLIGAN: Thank you counsel. Great. Okay. With
6 that I just want to make sure I got that correct with that. Petitioner you have
7 90 minutes. You will begin. You have the burden of production, or sorry,
8 you have the burden of persuasion in this case, so you present first. You
9 may reserve some -- hold on one second. You may reserve some time for
10 rebuttal and then Patent Owner. If Petitioner has a rebuttal, you may have a
11 brief sur-rebuttal. But Petitioner, would you like to reserve any time for a
12 rebuttal?

13 MR. CHANDLER: Yes, 30 minutes please.

14 JUDGE GALLIGAN: Okay. And we may because of the
15 length of hearing may take a break after Petitioner's case, and before we start
16 with Patent Owner. So, I'm going to get my clock started, but please keep
17 time separately and I'll try to give you a heads up around one hour. But
18 you'll be in charge of keeping time and we'll cut it off after 90 minutes. You
19 may begin.

20 MR. CHANDLER: Thank you, and Judge Galligan, are you able
21 to see the demonstratives on the screen and hear my voice okay?

22 JUDGE GALLIGAN: Yes, we can. Thank you.

23 MR. CHANDLER: All right. Thank you. May it please the
24 Board. Slide 5 shows the cover page of the '215 Patent as shown by the red
25 highlighting. The '215 Patent claims priority to various applications filed in
26 2004 and 2005. But our contention is that the claims of the '215 Patent are

1 not entitled to priority before any application filed by July 1, 2005. The
2 dispute about priority only matters for Ground 2 in both IPRs, which
3 involves the Ellsberry reference as I'll discuss in more detail later. The
4 dispute about priority does not matter for any other ground in the two IPRs.

5 Slide 6 shows the cover page of the '417 Patent, which is a
6 continuation of the '215 Patent and has the same dispute about priority,
7 which again only matters for Ground 2 involving the Ellsberry reference.
8 Slide 7 provides an overview of the problem identified by the '417 and '215
9 Patents, which was that high-density memory cost much more than low-
10 density memory. Normally, you would expect that if you doubled the
11 density of a memory device that the cost would also double, but at the time
12 of the '417 and '215 Patents, the cost was much more than double, which
13 created an enormous economic incentive to replace one higher-density
14 memory device with two lower-density memory devices.

15 For example, imagine that a 1 Gb memory chip cost \$1,000, while
16 a 512 Mb memory chip cost only \$100. In this example, if you could make
17 two 512 megabit memory chips act like one 1 gigabit memory chip, you
18 could save \$800 and still have 1 gigabit of memory. So that's what the '417
19 and '215 Patents propose doing using a technique referred to as rank
20 multiplication, where two ranks of low-density memory act like one rank of
21 high-density memory. Slide 8 shows Figure 1 from the Patents on the left,
22 which provides an example of rank multiplication. In the middle of Figure 1
23 is a buffer circuit highlighted in red with the number 40. The buffer circuit
24 in red in Figure 1 receives on the right side one chip select signal highlighted
25 in purple, corresponding to one rank of memory devices. The buffer circuit
26 in red outputs on the left side two chip select signals highlighted in purple,

1 going to two ranks of memory labeled rank one and rank two.

2 The result is that the host computer believes that there's one rank
3 of high-density memory devices on the memory module, when in reality
4 there are two ranks of low-density memory devices on the memory module
5 that emulate the one rank of high-density memory devices. This is an
6 example of rank multiplication. One other thing to note about Figure 1 is
7 that the buffer circuit in red creates what the parties have referred to as a
8 fork in the road layout for the data lines highlighted in green. For each data
9 line on the right side of the buffer circuit, there are two data lines on the left
10 side of the buffer circuit. The buffer circuit acts like a switch and routes the
11 data to and from only one of the ranks of memory devices. The reason for
12 this fork in the road layout is to avoid collisions as explained on the next
13 slide.

14 Slide 9 shows that there can be collisions during rank
15 multiplication if the two ranks of memory share the same data strobe lines.
16 The collision can occur when there are back-to-back read commands, which
17 are highlighted on the left in the blue and green rectangles. If the two ranks
18 share the same data strobe lines, that can result in a collision as shown by the
19 red rectangle. The solution taught by the '417 and '215 patterns is the fork in
20 the -road layout shown on the right in Figure 1. In Figure 1, the buffer
21 circuit in red with the number 40 can switch the connection between the two
22 ranks so that only one rank of memory at a time can drive the data strobe
23 line going to the host computer on the right side, thus preventing any
24 collision with the data strobe from the other rank of memory.

25 Slide 10 shows that the buffer circuit in red adds a delay of one
26 extra clock cycle to the data signals going through the buffer circuit. So, to

1 take a concrete example, the bottom of this slide in the middle shows that a
2 memory device might normally require 3 clock cycles to output data. The
3 Patent on the bottom left refers to this as a CAS latency of 3. The buffer
4 circuit in red adds 1 extra clock cycle of delay to the data signals, resulting
5 in a total delay of 4 clock cycles in this example, which the Patent refers to
6 as an overall CAS latency of 4 on the left side.

7 Slide 12 shows the Instituted Grounds.

8 JUDGE GALLIGAN: Counsel, this is Judge Galligan. I had one
9 just sort of housekeeping item I wanted to ask you. In, was it paragraph 3? I
10 forget what paragraph it was. Dr. Wolf's declaration, he defines CAS
11 latency. And I just want to make sure that was, I don't think it was disputed.
12 367 he says, a skilled artisan would have understood that a CAS latency is
13 the delay in clock cycles between the registration of a read command and the
14 availability of the first piece of output data. Is that, to your mind,
15 undisputed? That's what a CAS latency is, or do you, are you aware that
16 Patent Owner has disputed that?

17 MR. CHANDLER: I don't believe the Patent Owner has disputed
18 that. The JEDEC standard shows -- the CAS latency comes from the
19 JEDEC standard, and the JEDEC standard, for example, is shown on slide
20 14 on the bottom right. And the JEDEC standard gives timing diagrams that
21 show exactly how you calculate the CAS latency. So, in this example, on
22 the bottom right of slide 14, at time T3, there's a read command. The CAS
23 latency CL, in this example, is 3 clock cycles. And what that means is that
24 at time T6, the first piece of read data comes out on the DQ line, or the DQ
25 pin, rather, of the memory device. So, that's the definition of CAS latency in
26 the standard. And I believe that's the same definition that our expert is

1 using. And I don't believe that Netlist disputes it.

2 JUDGE GALLIGAN: Okay, thanks. This is Judge Galligan, and
3 I'll ask Patent Owner when he presents if there's any dispute. I just want to
4 make sure we're all on the same page on terminology and assuming that's
5 consistent with the Patent as well. But that's my understanding. I just want
6 to make sure we're on the same page. Thanks.

7 MR. CHANDLER: So, turning back to slide 12, Grounds 1
8 through 3 highlighted in yellow are the same in both IPRs, and they all rely
9 on the Perego reference as the primary reference. Ground 2 adds the
10 Ellsberry reference, which is noted in the upper right is the subject of a
11 dispute about priority. Ground 4 highlighted in green only applies to the
12 '215 Patent. Netlist has not raised any arguments specific to Ground 4. So,
13 for the most part, I will not discuss Ground 4 during my argument today.

14 Slide 13 provides an overview of the Perego reference marked as
15 Exhibit 1071, which is the primary reference in all grounds. As shown in
16 red, Perego discloses a data buffer on a memory module that provides a high
17 degree of flexibility because it's compatible with different generations of
18 memory devices and memory controllers.

19 Slide 14 provides an overview of the JEDEC JESD79-2 standard
20 marked as Exhibit 1064, which is a secondary reference in all the grounds.
21 The JESD79-2 standard provides a lot of detail about this signaling used for
22 DDR2 memory, as shown on the left, as well as the timing for those signals
23 as shown on the right. I will discuss the signals and timing in more detail
24 later, but two things you'll hear a lot about are the chip select signal, shown
25 in the upper left in the red box, and CAS latency, which we've already talked
26 about, shown on the right, including in the little red box around the number

1 three, indicating a CAS latency of 3 clock cycles in that example.

2 JUDGE BRADEN: Counsel, I believe that Patent Owner has
3 disputed whether JESD79-2 is applicable to memory modules and the bus,
4 rather than just to a memory device itself. What is Petitioner's stance on
5 that?

6 MR. CHANDLER: It's applicable to both, Your Honor, because,
7 for example, as shown on slide 42, the purpose of the JESD79-2 standard is
8 so that the memory controller can communicate with the memory devices on
9 the module. So, both the memory controller and the memory devices need
10 to use the same protocol to talk to each other. And as shown here, every
11 time the memory controller sends a command, such as a read or write
12 command, that command has to include a chip select signal, and it also has
13 to be sent with the proper timing, which would include the CAS latency.
14 And therefore, if you look at the bottom left and the bottom right, the
15 standards for DIMM memory modules include chip select lines, just like the
16 standard for the memory devices. Because again, the memory controller and
17 the memory devices, they have to communicate with each other, and it's
18 JESD79-2 that specifies all of that, again, including the chip select and the
19 CAS latency, which are the two disputed terms.

20 JUDGE BRADEN: Thank you, counselor.

21 MR. CHANDLER: Slide 15 provides an overview of the Ellsberry
22 reference marked as Exhibit 1073, which is part of Ground 2. Ellsberry was
23 filed on June 1st, 2005, which we contend is at least one month before the
24 earliest possible priority date of the claims of the '417 and '215 Patents.
25 Ellsberry is all about rank multiplication, and it's remarkably similar to the
26 '417 and '215 Patents. As shown on the bottom right, Ellsberry teaches

1 making two smaller capacity memory devices emulate a single higher
2 capacity memory device, just like the '417 and '215 Patents.

3 Slide 16 provides an overview of the Halbert reference marked as
4 Exhibit 1078, which is part of Ground 3. Halbert teaches a data buffer
5 shown on the left in red, and Halbert also provides detailed timing diagrams
6 for signals going through the data buffer, as shown on the right. Slide 17
7 provides an overview of the Matsui2 reference marked as Exhibit 1082.
8 This is only relevant to Ground 4, so for the most part I won't discuss this
9 reference today.

10 Slide 19 shows the level of ordinary skill proposed by Petitioner in
11 both IPRs. Netlist only disputes one word in this proposal, specifically the
12 word design, because according to Netlist, a person of ordinary skill in the
13 art did not know about the internal design of memory devices and memory
14 modules. But slide 20 shows that Netlist's expert admitted that books in the
15 field, including his own book on the bottom right, taught about the internal
16 design of memory devices and memory modules. This disagreement about
17 the level of ordinary skill may not matter for the invalidity grounds
18 presented in the petitions, but it is relevant to judging the credibility of
19 Netlist's expert.

20 JUDGE GALLIGAN: Counsel, this is Judge Galligan. I do want
21 to spend a moment on the level of skill because there is some dispute about
22 it, but I wanted to narrow the issues because as reading the briefing, I think
23 maybe there is a more nuanced position the Patent Owner is taking, and I
24 would welcome Patent Owner and I will ask Patent Owner about this. But
25 Patent Owner in its brief, page 8 of the Patent Owner response says that they
26 do dispute the knowledge about memory devices and memory modules

1 design part. They say that it would be knowledgeable about the operation of
2 standardized RAM, DRAM, and SDRAM memory devices and memory
3 modules. But in Dr. Przybylski's declaration, he takes a slight I think maybe
4 he takes a slightly different view where he says that a person of skill in the
5 art, and this is paragraph 68 of his declaration, Exhibit 2024. He says a
6 person of skill in the art with an ordinary skill level in the design of memory
7 modules wouldn't possess the training, knowledge, or expertise to attempt to
8 design semiconductor memory design—that may be a typo.

9 But I understood his position and I'll get Patent Owner's
10 clarification to be that design of memory modules is fairly within the scope
11 of the level skill in the art. I mean that's what the claim is directed to
12 anyway, but maybe you don't need to know the design of the DRAM chip,
13 you know, maybe a commodity of sorts because you get the spec, and the
14 spec tells you the pins it connects to. So, as long as you know the design,
15 how to design a memory module, you don't need to know the internal
16 design. You don't need to know how to design the memory, the DRAM
17 memory device. And if that's Patent Owner's position, is that generally
18 workable? I mean, is that an acceptable position for a Petitioner?

19 MR. CHANDLER: I believe you accurately stated Dr.
20 Przybylski's position. And I believe that the dispute raised by Dr.
21 Przybylski does not affect any of Petitioner's arguments, given that the claim
22 language is to the memory module and not the internals of the DRAM
23 memory device. But even as shown on slide 20, the prior art teaches the
24 internal design of DRAMs as well. And so, with respect to the credibility of
25 Netlist's expert, it's undercut by the fact that his own textbook contradicts the
26 position that he took about a person of ordinary skill in the art, not knowing

1 anything about the internal design of the DRAM. Both the Jacob textbook
2 on the upper right, as well as his textbook on the bottom right, teach how a
3 DRAM works.

4 JUDGE GALLIGAN: Yeah, and I guess just to nail this down a
5 little bit, you're talking about the internal design, and I guess, you know, if
6 we look at it as a box, and there's a spec to it, and there's lines that go into it,
7 and, you know, the DRAM chip, not the memory module, the DRAM chip
8 has certain functionality, and it's spec'd out. So, as long as you know what
9 you're going to get out of that device, you don't necessarily care, the internal,
10 you know, layout maybe. If that's Patent Owner's position, is that acceptable
11 to Petitioner, just to say that it's -- so basically, your level of skill with
12 design and operation of memory modules, and knowledge of the operation
13 and, you know, workings of the DRAM itself inside the memory module, is
14 that acceptable to Petitioner for the purpose of the 103 analysis?

15 MR. CHANDLER: I think it would be. I don't think there are
16 many details of the internal design of the DRAM that affects the claim
17 language.

18 JUDGE GALLIGAN: That's my understanding. And that's why I
19 kind of want to just narrow it down and eliminate a dispute, if possible,
20 because I think the dispute is about something else. So, I just want to make
21 sure that you're amenable to that. I'll get Patent Owner's position, and then
22 in rebuttal you can comment on it. Because I do think there's not as much
23 daylight between these positions as maybe the briefing laid out. So, I'll let
24 you continue. Thank you.

25 MR. CHANDLER: All right. As shown on slide 22, there is a
26 claim construction dispute about the claim construction for rank. Our

1 contention is that a rank includes one or more memory devices. Netlist
2 disputed that, took the position that a rank required two or more memory
3 devices. The Board has repeatedly rejected Netlist's position, has agreed
4 with our position that a rank includes one or more memory devices as shown
5 on slide 22.

6 The District Court also agreed with our claim construction of one
7 or more memory devices as shown on slide 23. And Netlist's own expert
8 wrote a book and as shown on the left of slide 24, his book also agrees that a
9 rank is one or more memory devices. It appears that Netlist has wisely given
10 up on this claim construction argument, but we maintain that a rank is one or
11 more. Are there any questions the Board has on claim construction?
12 Otherwise I'll keep moving forward.

13 JUDGE GALLIGAN: This is Judge Galligan. The only question
14 is that, like you said, it sounds like the Patent Owner no longer disputes that
15 in this case. So, there's -- my understanding is there's no argument about the
16 patentability of the claims of the '417 and '215 that depends on the one or
17 more construction, whether it can be one or whether it needs to be multiple.
18 Is that correct?

19 MR. CHANDLER: Well, there was. I mean, that was --

20 JUDGE GALLIGAN: There was, but there's currently no longer
21 one.

22 MR. CHANDLER: The way I understand it is Netlist is agreeing
23 with our construction. So, it's not that there's a dispute about whether the
24 construction matters. My understanding is Netlist is agreeing with our
25 construction for purposes of this IPR and Netlist is saying, well, you know,
26 we've got other arguments that don't depend on the claim construction.

1 JUDGE GALLIGAN: Thank you.

2 MR. CHANDLER: As shown on slide 30, Ground 1 in both IPRs
3 is the combination of Perego and JESD79-2. Slides 31 through 34 provide a
4 summary of Ground 1. Slide 32 shows that Perego on the left is similar to
5 the '417 and '215 Patents on the right. Both disclose the buffer device shown
6 in red that electrically isolates the memory devices shown in green and blue
7 from the memory controller shown in white. Slide 33 shows that Perego's
8 buffer device in red not only provides electrical isolation, it also provides
9 added functionality. In particular, Perego's buffer device allows for flexible,
10 cost-effective, and transparent upgrades while providing for high bandwidth,
11 and this specifically includes the use of DDR2 memory devices with existing
12 and new generations of memory controllers.

13 Slide 34 summarizes the combination of Ground 1. Perego on the
14 left discloses a buffered memory module with DDR2 memory devices that's
15 compatible with existing memory controllers, and then on the right,
16 JESD79-2 is the JEDEC standard that provides details about DDR2 systems,
17 including their signaling and their timing. Slides 31 through 51 respond to
18 Netlist's arguments that Perego is not compatible with JEDEC-style
19 implementations, specifically with chip select signals going into the memory
20 module. Slide 36 shows that Netlist argues that Ground 1 does not render
21 obvious chip select signals being sent to the memory module. Slide 37
22 shows that the institution decision on the left correctly found that it was
23 obvious for Perego's memory module on the upper right to receive JEDEC-
24 style signals, including chip select signals, as shown on the bottom right, as
25 disclosed by the JESD79-2 standard as well as JEDEC standards for DIMM
26 memory modules.

1 Slide 38 shows that Perego expressly discloses an embodiment
2 with individual control lines labeled RQ, which are in the red boxes on the
3 right, and those individual control lines, according to Perego on the bottom
4 left, include row address strobe, column address strobe, et cetera. Now, row
5 address strobe is abbreviated RAS and is a standard DDR2 signal as shown
6 at the bottom. Column address strobe is abbreviated CAS and is a standard
7 DDR2 signal as shown at the bottom. And then Perego's use of the word et
8 cetera shows that Perego understood that all of this was well known and did
9 not need to be spelled out in detail, consistent with the statement on the
10 bottom right from MPEP 2164.01 that a patent need not teach and preferably
11 omits what is well known in the art.

12 As shown at the bottom, the other well-known signals besides RAS
13 and CAS included WE, which stands for write enable, and CS, which stands
14 for chip select signal. And the reason those signals were well known is
15 because they defined the command for JEDEC style memory devices. So, in
16 particular, every read and every write command for DDR2 memory device
17 requires a chip select signal, making it obvious that the RQ control lines in
18 Perego, highlighted in red, would also include chip select signals. And that
19 is true both for the RQ lines going into the bottom of the buffer in red, as
20 well as the RQ lines coming out of the buffer and going to the memory
21 devices on the left and right, highlighted in green and blue. Slide 39, it
22 shows on the upper left.

23 JUDGE JURGOVAN: Counsel, can we go back one slide for a
24 minute?

25 MR. CHANDLER: Yes, Your Honor.

26 JUDGE JURGOVAN: So, my question here is, you know, maybe

1 the chip select is taught by the JEDEC standard, but the chip select, there's
2 more to it than that, right? It goes through the buffer, and there has to be
3 four control lines, right? Well, let's say you have one chip select. In the
4 case that you're showing here, there's four different control lines for each
5 chip on each, in each rank. Does that make sense?

6 MR. CHANDLER: There are.

7 JUDGE JURGOVAN: If you have a chip select coming in, it's a
8 two-bit signal, and that has to be extended to four bits and then select one of
9 the chips. And so, I guess my question is, is all of that architecture really
10 implied by the mere mention of chip select and JEDEC standard?

11 MR. CHANDLER: A couple things, Your Honor. So, what
12 Perego says on the bottom left is that there are individual control lines,
13 which means there's one wire for RAS, there's another wire for CAS, there's
14 a third wire for write enable, there's a fourth wire for chip select, and then
15 there may be additional chip select signals depending on how many ranks
16 the host computer thinks there are. So, those are the individual control lines
17 that go in through what's labeled RQ. So, RQ might be shown as just one
18 arrow, but what Perego is teaching is an embodiment where there are
19 multiple control lines, individual control lines, and that corresponds to the
20 JEDEC approach of having multiple wires for these different control lines.
21 And then the same wires will come out of the buffer and go to each memory
22 device. That is what was well known in the art. That was the dominant
23 approach because JEDEC had 90 percent of the market. So, for both the
24 memory devices and the wires going on in the memory module, there would
25 be individual control lines, individual address lines, and also individual data
26 lines.

1 JUDGE JURGOVAN: Okay. So, in our example here, you'd have
2 two chip selects coming in, and then that would be enhanced, or that would
3 activate individual -- one of four individual lines to select the chip. Correct?

4 MR. CHANDLER: In the -- so, Perego teaches rank multiplication
5 and so I think you're referring to the example of rank multiplication. Yes,
6 there would be two chip select wires coming in, and then four chip select
7 wires coming out. Now, in this particular image we're only showing two
8 ranks in green and blue, but if there are two chip select wires coming in and
9 four chip select wires coming out then you'd have four ranks on the memory
10 module.

11 JUDGE JURGOVAN: Okay. Thank you.

12 MR. CHANDLER: So, slide 39 shows in the upper left another
13 quote from Perego that again refers to RAS, CAS, et cetera, and we know
14 what et cetera is referring to because Perego gives a citation to this patent
15 which I've shown on the right which explicitly lists out all of the signals, not
16 just RAS and CAS, but all the other signals, which includes the chip select
17 signal. All of those signals are received by the DIMM memory module, and
18 that's consistent with the JEDEC standard from the bottom left for DIMM
19 memory modules, which include RAS, CAS, write enable, as well as chip
20 select signals.

21 Slide 40 shows that Perego's reference on the bottom left to
22 individual control lines does not correspond to Rambus, as admitted by
23 Netlist's expert on the bottom right. So, Perego discloses two embodiments.
24 One is Rambus, and I have an arrow to that in the upper right, but then
25 there's this other embodiment in the bottom left, which is individual control
26 lines. The Rambus embodiment in the upper right, does not have individual

1 row address strobe, which is RAS, or column address strobe, which is CAS,
2 as admitted by Netlist's expert on the right. What does have individual RAS,
3 CAS, and chip select signals is JEDEC, as shown on the bottom left.

4 Slide 42 is the one I touched on earlier with Judge Braden, which
5 is that the JESD79-2 standard is relevant to the memory module and not just
6 the DDR2 memory devices on that module. And the reason is that the
7 JESD79-2 standard requires every command to include a chip select signal.
8 So, as indicated by the two big red arrows on this slide, when the memory
9 controller on the host computer sends a read or write command to the
10 memory module, that command will include a chip select signal as specified
11 by the JESD79-2 standard. And that's confirmed at the bottom of this slide
12 by the JEDEC standards for the DIMM memory modules, which not
13 surprisingly show that the memory modules with DDR2 memory devices
14 need pins on the memory module to receive those chip select signals from
15 the memory controller.

16 JUDGE GALLIGAN: Counsel, this is Judge Galligan. I want to
17 touch on this and maybe going back to Judge Braden's point earlier. So,
18 we're -- in this slide 42, Exhibit 1064 is the JESD79-2. That's the DDR2
19 device spec, not the module spec. This command is for -- it's the command
20 going to the DRAM device. Correct?

21 MR. CHANDLER: Correct, which is on the module.

22 JUDGE GALLIGAN: Right. So, I think Patent -- and just to, just
23 to flesh this out a little bit, I think Patent Owner's argument would be yeah,
24 that's totally disclosed in Perego, you can use DDR2, but the interface
25 between the module and the memory controller is a Rambus interface. And
26 therefore, absent some teaching of chip select signal there, the combination

1 falls short of—the combination of Perego and JESD79-2 falls short because
2 that could just be the Rambus style packetized chip select information. I
3 know Patent Owner disputes that to some extent, but there's some
4 information that goes in a packet. So, what's your response to that?

5 MR. CHANDLER: Again, as shown on slide 38, Perego discloses
6 two embodiments. One is Rambus, the other is JEDEC. And JEDEC is
7 both for RQ at the bottom of the buffer, as well as RQ going to the memory
8 devices. Furthermore, Perego emphasizes that the whole point of his
9 invention is to be compatible, as shown on slide 46, with existing and new
10 generations of memory controllers, which as Netlist's expert admits on the
11 right, the vast majority of which were JEDEC. The industry as shown on the
12 bottom right rejected the Rambus approach, adopted the JEDEC approach,
13 and that was known by 2004 at the time of the '417 and '215 Patents, which
14 also at the time of the Perego Patent, which was filed in 2004.

15 So, it was obvious that if you are Perego and you have this buffer
16 device that's intended to be compatible with existing and new generations of
17 controllers, that all of those controllers, or 90 percent of them, are JEDEC.
18 And so, we think it's both explicitly taught, as shown on slide 38 on the
19 bottom left, with the description of RQ lines that are individual control lines,
20 which cannot be Rambus, because Rambus does not have individual control
21 lines. We think that's an explicit teaching of the JEDEC approach, and it's
22 certainly obvious, given that JEDEC was the dominant standard. And with
23 respect to this distinction between the module and memory device, what the
24 JEDEC DIMM standards on the bottom of slide 42 teach is that the signals
25 going to the module will match the signals going to the memory device. On
26 the upper left is a UDIMM, which means there's no buffers at all. And so,

1 the signals from the memory controller must match the signals going to the
2 memory device because there's no way to translate it.

3 On the upper right is a registered DIMM where the command
4 signals go through a register. But JEDEC teaches that the signals going into
5 the register are the same types of signals coming out of the register. So, if
6 you've got a chip select coming in, you also have a chip select going out.
7 So, it was the obvious approach that the memory controller would send the
8 signals going to the memory device. And there's nothing in Perego that
9 precludes that obvious approach. The contrary is shown on slide 38. We
10 believe that Perego expressly adopts it. And there's -- there's more to it as
11 well, Your Honor. I can I mean I can keep going we've got a lot of slides on
12 it, but -- but those are some of the high points.

13 JUDGE BRADEN: Well, before you get to that what I'd like to tie
14 in Judge Jurgovan and Judge Galligan's questions kind of putting that
15 together with the chip select signals and trying to figure out where you get to
16 the rank multiplication from these select signals in Perego. Where do you
17 get the two that come together -- the two command signals that go to the
18 different low density memory parts, where do you get that and do the rank
19 multiplication? I'm not seeing that from Perego's teachings. You've said
20 you've got the individual lines, and you answered Judge Jurgovan's question
21 saying look you've got these individual chip select lines but I'm not seeing
22 where you put them together to get the rank multiplication.

23 MR. CHANDLER: All right. So, Ground 2 with Ellsberry clearly
24 teaches the rank multiplication, that's what Ellsberry is all about. So, you
25 know, the strongest teaching --

26 JUDGE BRADEN: We're talking about Ground 1.

1 MR. CHANDLER: Right.

2 JUDGE BRADEN: We're talking about Perego with the JEDEC.

3 MR. CHANDLER: Right. And so, slide 50 gets to this sort of
4 Perego on the bottom line of slide 50 teaches that you can target a subset
5 using address bits and that is how rank multiplication works and that is
6 corroborated by the knowledge of what was known at the time as shown in
7 slide 51, which is the Amidi reference from early January 2004, which
8 identifies the same issue of you want to use two lower density memory
9 devices because they're cheaper in place of one higher density memory
10 device and it shows you right here in Figure 5 in the middle of slide 51 to
11 use the combination of the address bit and two chip select lines to generate
12 as shown on the right four chip select lines.

13 And so, we believe that the teaching of Perego on the bottom right
14 of slide 50 would be sufficient suggestion in combination with what was
15 known in the art as confirmed by Amidi that you would want -- you have
16 motivation to perform rank multiplication given that there was this
17 enormous economic incentive. And then if you want to, you know, go
18 beyond that, we've got Ground 2 from -- from Ellsberry, which spells it out
19 in extraordinary detail about exactly how you go about rank multiplication
20 and all the different permutations, how you can do it. And this and by the
21 way, I mean, slide 50, this is discussed in our petitions as well. So, there's --
22 there's a lot of detail on this in the petitions. But that's the general answer
23 that Perego teaches that you can create subsets using address bits.

24 JUDGE BRADEN: All right. Thank you, counselor.

25 MR. CHANDLER: So, slide 44 shows that Netlist's expert in the
26 upper left admitted to a person of ordinary skill in the art knew about both

1 the JEDEC standards for memory devices, as well as those for memory
2 modules as shown on the right. The JEDEC DIMM standards. And those
3 standards include chip select signals, and this is relevant as a legal matter,
4 because as shown on the bottom left, the DyStar case from the Federal
5 Circuit shows the motivation to combine need not be found on the references
6 being combined, but can be found elsewhere, making this admission by
7 Netlist's expert relevant to whether it's obvious for the memory module in
8 Ground 1 to include chip select signals.

9 JUDGE GALLIGAN: Counsel, this is Judge Galligan. I wanted
10 to ask a question about the JESD21-C spec and Patent Owner makes a -- has
11 an argument that -- several arguments, maybe that this wasn't included in the
12 ground and therefore the ground is deficient because you need that for the
13 chip select signal that comes into the module. Let's assume, I just want to
14 assume for the sake of argument that the chip select signal is accounted for
15 that goes into the module. Is there anything else in this petition that requires
16 reference to or reliance on JESD21-C?

17 MR. CHANDLER: Well, JESD21-C also renders obvious that you
18 add 1 clock cycle if you're registering a signal.

19 JUDGE GALLIGAN: Okay. Thank you.

20 MR. CHANDLER: Slide 45 shows that Netlist's expert admitted
21 on the right that a chip select signal is essential for a JEDEC style memory
22 system. And again, it's essential because it's part of every command as
23 shown at the top of this slide. And this is also explained by the Jacob paper
24 on the left as to why it's essential. Chip-select is part of the command and
25 chip-select is what selects the rank of memory devices that will respond to
26 the command. The other memory devices that don't receive the active chip-

1 select signal will ignore the command. So, again, chip-select is essential to a
2 JEDEC-style system with DDR2.

3 Slide 46, I touched on this before a little bit, which is that another
4 reason it's obvious for the memory module to receive chip-select signals is
5 because Perego teaches on the left that his invention was intended to be
6 compatible with both existing and new generations of memory controllers.
7 And as admitted on the right, the vast majority of those were JEDEC
8 controllers. And so, the vast majority of the signals, the vast majority of the
9 computers, would be sending chip-select signals to the memory module.

10 Slide 47 shows at the top that the JEDEC standards permitted high
11 bandwidth, even better than Rambus. And as explained on the right by
12 Netlist's expert, high bandwidth was one of the known strengths of the
13 JEDEC approach. Other strengths included that it was standardized, unlike
14 Rambus. And again, one of Perego's goals was high bandwidth. And so,
15 this provides a further motivation to combine for Ground 1, which is that
16 JEDEC was high bandwidth.

17 Slide 48 shows that Perego discloses two different ways to
18 communicate signals. One is a bus with individual lines consistent with
19 JEDEC. And then the other approach was point to point, which is like
20 Rambus. So again, Perego is teaching two different approaches. One is
21 Rambus, which Netlist focuses on, but Netlist ignores the other approach,
22 which is the bus approach with individual lines consistent with JEDEC. I'll
23 move forward just in the interest of time.

24 Slide 51 again, with this question about rank multiplication, says
25 that the Amidi reference, which was known at the time, teaches the
26 motivation as well as the solution for performing rank multiplication, which

1 is to use the address bit to generate additional chip-select signals on the
2 module.

3 Slide 53 shows the institution's decision correctly found a
4 motivation to combine Perego with JESD79-2, given the express disclosure
5 of DDR2 memory devices in Perego, as shown on the bottom right. Netlist
6 admits, on slide 54 on the upper right, that if you have chip-select signals,
7 you're going to have ranks, because the definition of a chip-select signal as
8 shown on the bottom right, is that that is the signal for rank selection. So,
9 the two go hand in hand. If you've got chip-selects, you're going to have
10 ranks.

11 Slide 55 is important. So, Netlist argues that Perego's configurable
12 width interface would be incompatible with JEDEC. And I want to pause on
13 this for a moment because it's really quite the opposite. The configurable
14 width interface, as you can see in this red rectangle, shows that the width of
15 the data bus can be 64 bits. Sixty-four bits was the most common width for
16 JEDEC. Rambus does not use a 64-bit bus going to the host computer. I
17 mean, that's the whole point of Rambus. If Rambus has a very narrow bus
18 that would never use 64 bits of data. So, the focus on the configurable width
19 interface is actually quite compelling evidence that Perego was intended to
20 be used with his buffer, was intended to be compatible with JEDEC, because
21 only JEDEC has the 64-bit data bus that was so common. Rambus did not
22 have such a wide data bus.

23 And this is talked about, for example, in -- well, it looks like my
24 Acrobat is having problems. But in the Jacob paper marked as Exhibit 1069,
25 which was cited in the institution decision and also cited in the petition,
26 Jacob talks about this, that the big difference between Rambus and JEDEC is

1 that Rambus has this very narrow data bus, whereas JEDEC, you know, has
2 32 or 64 bits was the most common width memory modules. So, this
3 configurable width the interface and the fact that Perego specifically says
4 that it can be 64 bits wide is actually very compelling evidence in our favor
5 that Perego was intended to be compatible with JEDEC and was not limited
6 to the narrow Rambus approach. Apologize my acrobat just crashed. Let
7 me open that up again and pick up where I left off. Judge Galligan, are you
8 able to see the slides again?

9 JUDGE GALLIGAN: Yes, we are. Thank you.

10 MR. CHANDLER: Thank you. All right. So, slide 56 shows that
11 the institution decision, the upper left picked up on this and recognized that
12 the configurable width data buffer could be 64 bits wide when using a
13 serialization ratio of one to one. And so again, 64 bit interface with 64 bit
14 ranks, that is the common JEDEC approach that does not apply to the
15 Rambus approach. There's no evidence of Rambus ever using a 64 bit
16 interface or 64 bit ranks.

17 Again, slide 57 is similar, which is that Perego was intended to be
18 compatible with current and future generations of memory controllers.
19 Slides 62 through about 70 talk about this issue of ranks. One of the Netlist
20 arguments is that Perego supposedly does not disclose ranks. Really this
21 argument, again, is based on the chip select signal because Netlist is trying
22 to say that there are no chip-select signals and therefore, no ranks on Perego.
23 That's incorrect. And in fact, as shown on slide 63, Netlist and its previous
24 expert both admitted on the left that Perego on the right discloses multiple
25 ranks of memory devices with one rank highlighted in green on this slide
26 and the other rank highlighted in blue. I'm going to skip forward in the

1 interest of time.

2 JUDGE JURGOVAN: Counsel, can I ask one question?

3 MR. CHANDLER: Yes.

4 JUDGE JURGOVAN: Can we go back to that figure that was in
5 red showing -- one forward. You just passed it.

6 MR. CHANDLER: Yes, slide 64?

7 JUDGE JURGOVAN: Yeah. So, the line down on the bottom,
8 that is receiving a serial signal, right? Serial data and control signals at the
9 bottom.

10 MR. CHANDLER: No. No. It's, I mean, it's not -- the point of
11 WDP is it could be one bit wide, in which case everything would be serial.
12 But it can also be these other widths, including 64 bits wide.

13 JUDGE JURGOVAN: I see. Okay.

14 MR. CHANDLER: Which is all 64 bits would come at the same
15 time. And so, what Perego is teaching is that his buffer is, you know, highly
16 flexible. So, you could have a narrow, Rambus approach with only, say,
17 eight data lines, or however many there were in Rambus. And so, what
18 Rambus does is it packetizes the information, and it sends information in a
19 serial fashion. Perego's buffer can do that because you can set it to eight bits
20 wide. But Perego's buffer can also be set to 64 bits wide, which is the
21 standard, JEDEC approach where all 64 bits arrive at the same time. And
22 then you have this serialization ratio of one-to-one, which means that all 64
23 bits that come in is the same thing that goes out to the memory devices.

24 JUDGE JURGOVAN: Yeah, I think Patent Owner's argument
25 here is that, you know, you have 64 on both sides of the buffer, you know,
26 on the input side and the output side of the buffer, which meets the claim

1 limitation. But their point is, why would you do that? That you're, I guess
2 they're saying that Perego has this flexibility, but then you're not using that
3 flexibility. You're just setting it to 64 on both sides. And so, why use
4 Perego, I think, is how I understand their argument. And how do you
5 respond to that?

6 MR. CHANDLER: My response is Perego explicitly teaches that.
7 That's what's shown in the middle of slide 64, is a serialization ratio of one-
8 to-one. So, the flexibility includes doing what was the most common
9 approach. So, Perego doesn't limit you to the most common approach of a
10 serialization ratio of one-to-one was 64 bits that's JEDEC. You know,
11 Perego is more flexible than that, but Perego does not exclude the most
12 obvious approach, which is JEDEC. That's my response, and it's an explicit
13 disclosure in Perego, serialization of one-to-one and 64-bit data width.
14 Those are both express disclosures.

15 JUDGE JURGOVAN: Thank you.

16 MR. CHANDLER: I'll pause briefly on slide 69. One of the
17 limitations is that the chip-select signal is different for the different ranks of
18 memory devices. That's taught by the JESD79-2 standard at the bottom, as
19 admitted by Netlist's expert on the right, and is explained by the Jacob paper
20 on the left. The way it works is you've got multiple ranks of memory
21 devices under the JESD79-2 standard, one rank. We'll get the active chip-
22 select signal, the other ranks will not, and they therefore ignore the read or
23 write command.

24 I want to turn briefly to this notion of CAS latency and adding one
25 additional clock cycle. So, this starts at slide 70. And slide 71 is just a
26 refresher on what the issue was in the '417 and '215 Patents, which is that the

1 data buffer requires one extra clock cycle. Slide 72 shows that Perego
2 teaches the data buffer. The reason for the data buffer is isolation of
3 electrical signals. And as explained by Netlist's expert on the right, the
4 reason that you want to isolate the signals is because that can reduce the
5 electrical load and improve the performance.

6 As explained on slide 73, if you have a data buffer, it was known
7 that would add some delay. It would add some latency, such as one clock
8 cycle. Netlist's expert admitted on the left on slide 73, a person of ordinary
9 school would understand that that, you know, the data buffer will add some
10 delay. And then slide 74, Netlist's expert on the right gives this sort of
11 colorful explanation as to why you would add the data buffer, even if it adds
12 one clock cycle of delay. And he gave this comparison of a Ferrari to a
13 Volkswagen, which is maybe the Ferrari takes a little bit longer to warm up,
14 but once it gets going, it can go at a higher speed. And that's the same thing
15 with the data buffer. The data buffer might add one clock cycle of latency,
16 but once it's warmed up, once it's gotten past that one clock cycle, it is then
17 able to transfer data at a higher speed.

18 And so, you would have this motivation to add the data buffer for
19 higher speed, even though it adds a delay of one clock cycle. The
20 institution's decision on slide 75 correctly found a motivation for Perego's
21 data buffer to add a delay of one clock cycle, increasing the overall CAS
22 latency of the module by one cycle. As shown in the middle of the slide,
23 Perego's data buffer on the right has these latches highlighted in blue, and
24 those latches highlighted in blue would add delay, as explained by our
25 expert, and is quoted by the institution decision on the left, and the delay
26 would be, for example, one clock cycle. And this is discussed more in the

1 following slides in more detail. So, for example, on slide 76, Netlist admits
2 in the upper left that the buffer has these clocks in purple, and the purpose of
3 the clocks in purple is so that the latches in blue will capture the data at the
4 precise time that's correct, and then those latches in blue will delay the data
5 because the latch will add time.

6 And as our expert explained on the right, the delay from the latches
7 would be a fixed time delay, such as one clock cycle. And so, where do you
8 get the one clock cycle from? That comes from slide 77, which is the
9 JESD79-2 standard, and the important point here is that under that standard,
10 latencies are measured in integer values, so whole numbers. So, you can
11 have a latency of 3, or you can have a latency of 4, but as shown in the
12 middle on the right, DDR2 doesn't support half-clock latencies. So, you
13 cannot have a fraction of a clock cycle delay under JESD79-2. If there's
14 going to be any delay, it needs to be in an integer value of one full clock
15 cycle.

16 And so, for example, as taught on slide 78, and at the top here, the
17 standard approach was when you have a register for signals, you would add
18 one clock cycle of delay, and that's true both for DDR on the upper left,
19 DDR2 in the upper right, and Netlist's expert admits on both the left and the
20 right that, yes, you have delay, and yes, one clock cycle is a common
21 amount of delay. And so, if you wrap it all together, slide 79 sort of
22 summarizes the point, which is on the left. Perego's buffer has those latches
23 in blue that add delay, and then on the right, you've got JESD79-2, which
24 tells you that any additional delay has to be by an integer number of clock
25 cycles. And so it's going to be one clock cycle. Before I go on the next
26 topic, any questions about that?

1 JUDGE GALLIGAN: Yes. This is Judge Galligan. I had a quick
2 question, and I just want to just make sure I'm on the same page with the
3 technology and the parties. So, paragraph 32 of Dr. Przybylski's
4 Declaration, Exhibit 2024, he testifies that registered DIMMs include a
5 register device for buffering the address and command, but not the data bus.
6 I just want to make clear. So, the JEDEC, a register in RDIMM, I know
7 your combination has registering of data, but the RDIMM as just the
8 standard would register address and control, but not data, correct?

9 MR. CHANDLER: Correct, but the RDIMM is relevant for two
10 reasons. One is shown here on slide 78 in the upper left, which is that it
11 teaches that if you're gonna register any signal, whether it's data or address,
12 that that registering should be a delay of one clock cycle because again,
13 JEDEC has integer values for latency. You don't have fractional delays. So,
14 that's one reason it's relevant. And --

15 JUDGE GALLIGAN: Counsel, this is Judge Galligan. I just
16 wanted to point something out on that. So, I thought I just heard you say
17 that the DDR specification allowed fractional half clock cycle delays. And
18 this is the DDR RDIMM standard, right? So, this would allow a fractional
19 delay, but the DDR2 wouldn't?

20 MR. CHANDLER: Correct.

21 JUDGE GALLIGAN: Okay.

22 MR. CHANDLER: Yeah.

23 JUDGE GALLIGAN: All right. Thanks.

24 MR. CHANDLER: Anything else on CAS latency delays?

25 JUDGE GALLIGAN: Nothing right now. Thanks.

26 MR. CHANDLER: All right. So, the '215 Patent, there are no,

1 these dependent claims, all of Netlist's arguments for the dependent claims
2 refer back to what we've been discussing. So, there's no argument specific
3 to the dependent claims. So, I'll move on then to Ellsberry, which is Ground
4 2. And the first issue is a legal issue about whether Ellsberry is a printed
5 publication under Section 311(b). And on slide 88, the Board has repeatedly
6 agreed with our position that patent applications are printed publications and
7 are entitled to their section 102(e) filing date under Section 311(b). This
8 case in the middle, the Lynk Labs case marked as Exhibit 1098, is up on
9 appeal to the Federal Circuit.

10 And just this morning today, May 3rd, 2024, the director of the
11 Patent Office filed a brief with the Federal Circuit, completely agreeing with
12 our position that published patent applications are printed publications under
13 § 311(b), and they are entitled to their 102(e) filing date. So, there's, by our
14 count, there are 10 judges on the Board who have all agreed with our
15 position. We're not aware of a single judge that has ever agreed with
16 Netlist's position. And just today, the Director of the Patent Office came out
17 with a brief in our position. This is Federal Circuit Appeal Number 23-
18 2346, paper number 36 filed today by Director Vidal. Any questions on the
19 legal issue of 311(b)?

20 JUDGE GALLIGAN: No questions. Thank you.

21 MR. CHANDLER: All right. So, then we go starting on slide 90
22 to this question of whether Ellsberry is prior art, and we say yes because
23 Netlist had a burden of production to show that the provisional application
24 provided 112 support and we don't believe that Netlist met its burden of
25 production. So, slide 91 shows in the upper left that under Dynamic
26 Drinkware, Netlist had a burden of production to show that the subject

1 matter of the claims is supported by its priority applications such that
2 Ellsberry is not prior art, and as explained in the upper right by the
3 Continental decision Petitioner, that's us, was not required to rebut in
4 advance Patent Owner's argument and evidence alleging priority to the
5 earlier application. And so, slide 92 shows on the left what Netlist did.

6 Netlist, in its Patent Owner response included this claim chart
7 purporting to show, you know, purporting to satisfy its burden of production,
8 but this claim chart is insufficient for numerous reasons. The first reason is
9 shown in the upper right under the Federal Circuit's Ariad decision is that
10 obviousness does not satisfy the written description requirement. So, what
11 Netlist has done on the left is it's mixing and matching a whole bunch of
12 different applications trying to show support for each claim limitation.
13 That's an obviousness argument, and that does not work. Another problem
14 is that under 35 U.S.C. § 111(b)(7) provisional applications are not entitled
15 to earlier priority from any other document, so you can only rely on the next
16 provision on this slide, which is 35 U.S.C. § 120.

17 But that's only true if there's a specific reference to the earlier
18 application. Netlist hasn't done that. Netlist hasn't shown that these various
19 applications cross-reference to each other, so there are all sorts of problems.
20 And then on the bottom right of this slide is another problem, which is that
21 the Board's regulations prohibit incorporating arguments by reference.
22 Netlist did not provide any explanation for what all of these citations mean,
23 and that does not satisfy its burden of production, just give a bunch of
24 citations without any explanation.

25 Slide 94 shows that in the sur-reply, Netlist sort of retreated and
26 said, okay, we're only going to rely on Exhibit 1005, which is the provisional

1 application filed January 19th, 2005, to try to show 112 support for the
2 claims. But there's still the problem that Netlist is making an obviousness
3 argument, which again under Ariad is insufficient. And then there's also this
4 problem that Netlist is essentially trying to incorporate by reference or, you
5 know, circumvent the word limit by not giving any explanation for what any
6 of these citations mean. There's just a big list of paragraph numbers without
7 any explanation of how that satisfies the burden of production.

8 Slide 95 focuses on one example of a claim limitation that is in the
9 claims of the '417 and '215 Patents but is not taught in the provisional
10 application marked as Exhibit 1005. And that limitation is highlighted in
11 green. It's data buffer control signals in the '417 Patent on the left. On the
12 '215 Patent on the right, the corresponding limitation is first control signals.
13 And then in red, there's also second control signals to the buffer. It's the
14 same issue, which is that in the middle of this slide 95, the provisional
15 application does not disclose any control signals. There are no control
16 signals disclosed going to the data buffer. So, we've quoted paragraph 7,
17 which talks about logic, which is in this red rectangle, RBDL is the logic.
18 And then paragraph 5 talks about a multiplexer, but there's no disclosure of
19 any control signals for any of that. And Slide 96 shows in the center that
20 Netlist's expert admitted that the provisional application marked as Exhibit
21 1005 does not mention any control signals. Instead, he argued that such
22 signals are inherent, but that is incorrect as discussed on the following slides.

23 So, Slide 97 shows that the data buffer control signals are required
24 to transfer data to one of the ranks, but there's nothing inherent about
25 transferring data to one of the ranks. Instead, data could be sent to both
26 ranks, which was the approach in JEDEC at the top of this screen on slide

1 97. So, there's nothing inherent about only sending data to one rank rather
2 than two ranks, and there's no disclosure of how the provisional application
3 marked as Exhibit 1005 would send control signals to route data to only one
4 of the two ranks. And again, remember this fork in the road and routing data
5 to only one of the two ranks, this was important for rank multiplication.
6 This was the approach disclosed in the '417 and '215 Patents to avoid
7 collisions. None of that is discussed in Exhibit 1005, the provisional
8 application. There's no discussion about collisions and routing data and
9 using control signals to do any of that. And it's not inherent. That's not the
10 only way that you need to send data to multiple ranks. It could be sent to
11 both ranks.

12 Slide 98 shows another problem with the provisional application,
13 which is that the data buffer control signals, according to the claim language,
14 need to come from the logic on the memory module. So, the logic has to
15 generate these data buffer control signals in response to the read or write
16 memory commands. And it's not inherent that logic on the memory module
17 needs to generate data buffer control signals. It would be possible and it's
18 typical that usually control signals come from outside the memory module.
19 Usually, it's the memory controller is what's sending all the control signals
20 telling the module what to do.

21 And so, there's nothing inherent about the memory module itself
22 having logic to generate its own control signals. You could have control
23 signals coming directly from the memory controller as shown by the orange
24 arrow. Another possibility discussed by our expert is that the memory
25 devices could be sending DQS preambles. And so, in the redirection, the
26 DQS preamble could be used to control the data buffer. Again, the point is

1 that there's nothing inherent about the logic on the memory module being
2 what controls the data buffer.

3 JUDGE GALLIGAN: Counsel, this is Judge Galligan. I just want
4 to let you know you're an hour and two minutes in, and it's your time to use.
5 I just want to give you a heads up.

6 MR. CHANDLER: Got it. I'll just briefly go through Ground 2.
7 So, Netlist doesn't really have any argument against the combination of
8 Ground 2. Their primary argument is that Ellsberry is not prior art.
9 Ellsberry, as shown on slide 103, is all about rank multiplication. And so,
10 it's very, very, very close to what the '417 and '215 Patents are doing. And
11 that's also why we've got this secondary consideration of simultaneous
12 invention, which is that Ellsberry, which was filed a month before the
13 earliest filing date of Netlist patents, is teaching rank multiplication in
14 literally like the exact same way as what Netlist later disclosed and claimed
15 in its Patents. So, the combination of Ellsbury and Perego is quite powerful.
16 And of course, Ellsberry has chip-select signals coming into the memory
17 module. Ellsberry is compatible with JEDEC. Ellsberry actually
18 incorporates by reference the JEDEC standards. Was there a question?

19 JUDGE GALLIGAN: Counsel, this is Judge Galligan. I wanted
20 to ask you about the simultaneous invention, you know, Patent Owner's
21 response, at least in the 454 involving the '417 is that, look, rank
22 multiplication isn't even claimed, for one thing. But, you know,
23 simultaneous invention really seems to be more directed to, you know, the
24 level of skill in the art, whether someone, you know, meaning is it really,
25 you know, just because someone knew about rank multiplication and that
26 really isn't claimed? Is that going to show something is obvious, or is that

1 just showing, look, a person of skill in the art would have understood rank
2 multiplication and I don't think, I'm not sure that's really disputed.

3 MR. CHANDLER: Well, I pushed back, Your Honor, on the idea
4 that rank multiplication is not claimed. So, the independent claims of the
5 '417 and '215 Patents might be broad enough to cover both rank
6 multiplication and non-rank multiplication, but clearly rank multiplication is
7 an embodiment of both the '417 and '215 Patents. And there are dependent
8 claims that require rank multiplication and they're also in the '215 Patent.
9 They're also dependent claims that talk about collisions due to back-to-back
10 or avoiding collisions due to back-to-back adjacent read commands. So,
11 rank multiplication is sufficient to satisfy all of the claims of the '417 and
12 '215 Patents.

13 And so, if you have Ellsberry, which is teaching rank
14 multiplication that satisfies or at least renders obvious the claims of the '417
15 and '215 Patents, I do think that's relevant under simultaneous invention, and
16 in this notion about the level of skill here, you're right as a legal matter is
17 shown on slide 120 that the legal relevance of simultaneous invention is it
18 shows, you know, what the level of skill was. That's relevant because it
19 shows that yes, people recognize the problem of higher density memory
20 chips. They also recognize the solution of rank multiplication, and Ellsberry
21 shows that they have the skill level and capability to implement it with the
22 fork in the road to avoid collisions, and all of that was known before, or at
23 least very close in time to when Netlist filed its patents. And so, I mean I do
24 think that Ellsberry is as good an example of simultaneous invention as you
25 can find in case law.

26 JUDGE GALLIGAN: This is Judge Galligan. So, did you say that

1 Ellsberry itself alone renders obvious other claims?

2 MR. CHANDLER: I mean, I think it would.

3 JUDGE GALLIGAN: We don't have a record for that do we?

4 MR. CHANDLER: Pardon me?

5 JUDGE GALLIGAN: This is Judge Galligan. We don't have a
6 record for that because you didn't assert that right?

7 MR. CHANDLER: That's right. That's right. No, we rely on
8 Perego plus Ellsberry.

9 JUDGE GALLIGAN: I had another question. Great. I had
10 another question on Ellsberry, and you may be getting to this. If the -- so
11 you've got your JESD21-C, which you rely on for a one cycle delay. Does
12 Ellsberry fill in that gap?

13 MR. CHANDLER: Yes. Ellsberry teaches in Figure 8B that
14 adding one clock cycle to the CAS latency and Netlist does not appear to
15 dispute that Ellsberry teaches that. Netlist did not present any argument in
16 his Patent Owner response, or it's sur-reply disputing that Ellsberry teaches
17 consistent with JESD21-C that if there's a data buffer on the memory module
18 that will add one clock cycle delay. And so, the CAS latency goes up by
19 one. So, we like Ellsberry. I mean Ellsberry is, again, as close as you can
20 get to what the '417 and '215 Patents we're talking about.

21 Just real briefly on Halbert, starting on slide 109. So, Ground 3 is
22 the combination of Perego, JESD79-2 and Halbert. This combination is
23 summarized on slide 111. And Halbert has a data buffer, so it's very similar
24 to Perego. And what Halbert adds is it has these timing diagrams, which
25 show that the data buffer adds delay to the data signal. And Halbert also
26 shows two separate ranks, which we've highlighted in the right here as green

1 and blue. And as shown on slide 113, the institution decision recognized the
2 motivation to combine Halbert with Ground 1, including multiple ranks.

3 And that the data buffer would increase the CAS latency.

4 And then I'll pause here on slide 114. So, Netlist's primary
5 response is that Halbert says that generally, in the upper right here on slide
6 114, generally, the multiple ranks will act concurrently, but that is not
7 always required as recognized by the Board in the upper left in Exhibit 1107
8 at page 27. Generally, means that it's not always the case that the memory
9 ranks perform memory operations concurrently. As explained by our expert
10 on the bottom left, ranks 140 and 142 can be two separate ranks, which is
11 consistent with the normal approach under JEDEC, which is that the two
12 ranks are separately controlled by separate chip-select signals.

13 And then, finally, on slide 115, there are these timing diagrams in
14 Halbert. The timing diagram on the left from Figure 3 shows how many
15 clock cycles there would be without a data buffer. And so, in this example,
16 it's three and a half clock cycles. And then Figure 5 of Halbert on the right
17 of slide 115 shows that if you add a data buffer, the overall CAS latency
18 goes up. In this example from Halbert, it goes up by half a clock cycle, but
19 Halbert is a slightly older reference back when DDR1 existed, which
20 permitted half clock cycles. In the combination we're relying on, there's
21 DDR2, which is shown on slide 116 on the right, does not permit half clock
22 cycles, only permits full integer clock cycles. Unless there are any
23 questions, I'll reserve the remainder of my time for rebuttal.

24 JUDGE GALLIGAN: Hearing nothing from the panel, we will --
25 I'll stop the watch. And you've used one hour and 10 minutes. So, before
26 we get started with Patent Owner, it might be a good idea just to take a five

1 minute break. And let me make a note that you have a little under 20
2 minutes remaining. So, let's do, let's reconvene at 1:20 Eastern time. And
3 Patent Owner you may begin. Thank you.

4 MR. HEIM: Thank you.

5 JUDGE GALLIGAN: Okay. This is Judge Galligan. We're back
6 on the record. Madam court reporter can you hear us?

7 COURT REPORTER: Yes, sir. I can hear you guys.

8 JUDGE GALLIGAN: Great. Thank you. Okay. Patent Owner,
9 you have 90 minutes to present your arguments. If Petitioner has a rebuttal,
10 you may have a sur-rebuttal. Would you like to reserve any time for that?

11 MR. HEIM: Yes, please. Twenty minutes.

12 JUDGE GALLIGAN: Twenty minutes. And like I said to Mr.
13 Chandler, please keep time. I'll keep a stopwatch here and try to give you a
14 heads up about an hour and 10 minutes in. And also, just as a reminder,
15 point out the slides for the slide number for us for the record. Thank you
16 very much. You may begin.

17 MR. HEIM: Michael Heim for the Patent Owner, Netlist. May it
18 please the Board. Let's go to slide number 2. And just to confirm, can
19 everybody see the PowerPoint display that's on the screen?

20 JUDGE GALLIGAN: Yes, we can. Thank you.

21 MR. HEIM: Okay. So, I provided a roadmap for the presentation
22 today, time allowing. I'm gonna begin by speaking briefly about the '417
23 and '215 Patents. We're then gonna spend a fair amount of time talking
24 about Perego and its operation, how it works. And then we'll address the
25 critical issues relative to Grounds 1, 2, and 3.

26 Let me just pause right here. So, there were two questions that

1 were asked. The first was about CAS latency. That's defined in Dr.
2 Przybylski's declaration, Exhibit 2024 at paragraphs 29 and 30. And what
3 he said is that CAS latency is the delay between the receipt of a read
4 command and the output of the first piece of data of the data burst. And then
5 secondly, I think there was a question about the level of skill in the art,
6 which as was noted by the Board, Dr. Przybylski raised in paragraph 67 and
7 some subsequent paragraphs. Here's his point. I think it's really simple.
8 And that is that he is saying that a person of ordinary skill in the art would
9 not be one who would be redesigning ASICs. So, if there's a redesign that's
10 required of the memory controller, that's beyond the skill level of the person
11 of ordinary skill in the art.

12 Let's go back to slide number 4 -- slide number 3, I'm sorry. So, as
13 processors and computers become more complex, there's a need for more
14 and faster memory. The problem is, is that when you try to solve that
15 problem, you run into a cascade of problems that develop. Every time you
16 solve one problem, another problem develops. So, you want to add memory.
17 When you do that, it raises a host of other issues. So, if you want to add
18 ranks of memory, you're limited by the number of chip-select, dedicated
19 chip-select signals that are available on the module. If you fix that to have
20 more ranks, then you have load issues. That's going to slow down
21 operations. It's going to compromise the signal integrity on the memory bus
22 as communications go back and forth between the memory controller and
23 the memory module. If you add circuitry to try to fix that issue and isolate
24 loads, then you develop timing issues, timing problems relative to the very
25 strict JEDEC timing requirements that are in the standard.

26 So, you have this cascade of issues problem. Let's go to the next

1 slide. What the '417 and '215 Patents do is they provide a fully integrated
2 solution for adding memory to a memory module. And so, what's shown
3 here is Figure 1, and the memory module includes multiple ranks of
4 memory, a plurality of ranks. It includes a circuit 40 that is going to receive
5 and register input, address, and control signals, including active and non-
6 active chip-select signals that are received from an external memory
7 controller on the memory bus to produce registered signals. Then the
8 circuitry is going to generate those registered signals, including a registered
9 chip-select signal, a plurality, one active, and the others are non-active. It
10 also adds a buffer on the data path. First time anybody has done this in the
11 JEDEC world. And then they add logic, which controls the transfer and
12 timing of the data through the data buffer to and from the ranks of memory.
13 And they perform a registered data transfer, and they hide that delay by
14 increasing the CAS latency. So, there was CAS latency of the memory
15 device. You're now going to add a cycle and hide that delay in this new
16 CAS latency value. So, it's not just, oh, there's a delay. We know we need
17 more time. It's hiding it in the CAS latency. So, result, JEDEC compliant.
18 It follows what's required in the JEDEC standard relative to timing. It
19 isolates the electrical load between the memory devices and the memory
20 controller. By doing the registering, you can regenerate data signals to
21 improve the quality of the signal. And you can support more memory that
22 operates faster. And that's the Ferrari analogy that our expert gave. They
23 want to say that shows a motivation to combine.

24 Well, if you look at it in 2023 it's definitely not showing a
25 motivation to combine, because they're looking at the wrong time period.
26 You've got to go back in 2004 and 2005, and you've got to determine what

1 would have been obvious at that time when the JEDEC standards, the
2 RDIMMS that we talked about, don't have a data buffer. Let's go to the next
3 slide, slide 5. Figure 8 is one embodiment of adding a data buffer. It's one
4 example, and it includes a data buffer 120, and the transfer is being
5 controlled by the logic 122 that provides the signal to the data buffer. Now,
6 slides 6 through 10 are detailed mappings of Claim 1 versus some of the
7 embodiments in the figure. We're going to skip those in the interest of time.
8 So, let's go to slide number 11.

9 JUDGE GALLIGAN: Counsel, this is Judge Galligan. Are you
10 going to revisit the level of skill in the art, because I did want to touch on
11 that again. Or was that the argument?

12 MR. HEIM: That was pretty much it Judge, but I can explain why
13 I think it's relevant.

14 JUDGE GALLIGAN: Yeah, no, I, I want to know. Well, I do
15 want to know that. But I wanted to know what the dispute is between the
16 parties. So, as I mentioned in the Patent Owner response at pages 7 to 8, you
17 have this discussion of the skill level. And it says, you take issue with
18 Petitioner's contention that a person of skill in the art would have been
19 knowledgeable about the design and operation of DRAM and SDRAM
20 memory devices and memory modules. And you say that the person of skill
21 in the art would have been knowledgeable about the operation of
22 standardized DRAM and SDRAM memory devices and memory modules,
23 including those commercially available.

24 And then we go to Dr. Przybylski's declaration, and he's -- his
25 point seems to be, look there's a difference in memory module design and
26 memory device design. You know the DRAM chips themselves or, you

1 know, their spec'd out, whatever. So, a person of skill in the art would have
2 experience in the design of memory modules. Would not -- that person
3 would not possess the training knowledge or expertise to attempt to design
4 semiconductor memory design. I think that's a typo. So, my understanding
5 of Dr. Przybylski's position is that he thinks that a person of ordinary skill in
6 the art, as relevant to this, the person of skill in the art we're talking about
7 would have knowledge of the design of memory modules. Is that correct?

8 MR. HEIM: They would in the communications between the
9 module and the memory controller in the memory devices, but not
10 necessarily the skill level to be able to redesign, you know, to design the
11 ASIC and the other pieces that are going to be required if you start changing
12 things.

13 JUDGE GALLIGAN: Well, let's follow up on that a little bit
14 because I think this is some, you know, somewhat of an important point.
15 103 is obviously judged from the standpoint of the level of skill. From the
16 patent there's -- in the '417 Patent, there are various passages talking about
17 what can be, what a person of skill in the art might know or would be able to
18 do, you know, at paragraph or column 7, line 1 to 3. Persons of skill in the
19 art, a person of skill in the art can select appropriate memory devices in
20 accordance to certain embodiments. Okay. We go to column 17, 2 to 5.
21 Persons skilled in the art are able to select a phase lock loop device and a
22 register compatible with embodiments described herein. 26, 3 to 6. It says
23 persons skilled in the art are able to provide additional logic translation
24 equations compatible with embodiments and they're talking about this back-
25 to-back adjacent read command situation. You go to 33, 44 to 47, it says --
26 34, column 34, 44 to 47, a person skilled in the art can select an appropriate

1 PLD, presumably programmable logic device, 42 and appropriate OR logic
2 elements in accordance with embodiments.

3 Column 40, 38 to 40, person skilled in the art can provide a
4 termination assembly in accordance with embodiment described herein. So,
5 I mean this is a person who, and then the catch-all language, various
6 modifications and applications may occur to the persons skilled in the art
7 without departing, that's 42, 2 to 4. I mean the point is, the person of skill in
8 the art has got to be able to build a memory module, right? And the patent
9 itself is giving the person of skill in the art some leeway in choosing certain
10 things. So, whether or not the person's designing an ASIC from scratch,
11 they're going to have to be able to, for instance, pick a programmable logic
12 device. So, that's what I'm trying to get at. What is the Patent Owner's
13 position? Is the design of a memory module within the scope of the --
14 within the knowledge of a person of ordinary skill in the art?

15 MR. HEIM: Based upon the teachings, absolutely, yes. Yes, you
16 can do that.

17 JUDGE GALLIGAN: Okay. And so, and so I think, and I'm
18 going to have, if Petitioner has a rebuttal, I'll ask Petitioner's counsel. So, if
19 we took the, because I, you know, we're here to resolve disputes, and we
20 want to do that if there's an actual dispute, but if the parties are talking past
21 each other and we can kind of narrow the issues, that's what I want to do.
22 So, my takeaway from Dr. Przybylski's position and presumably it's your
23 position, it's Patent Owner's position is that person of ordinary skill in the art
24 would have knowledge of the design of memory modules. And, you know,
25 so basically we narrow it to Petitioner's position was knowledge and
26 operation of design of memory modules and memory devices. And we

1 would just excise maybe the design of memory devices. So, they'd know
2 about the operation. But a person of skill in the art is going to know about
3 the design and operation of memory modules, and the operation of memory
4 devices within those modules. Is that a fair characterization? Is that what
5 the parties are kind of getting to or what Patent Owner is getting to?

6 MR. HEIM: Yes.

7 JUDGE GALLIGAN: Okay. And I'll have Petitioner, if it has a
8 rebuttal, I'll have it confirm that. And I think that takes -- that just focuses
9 the—we know what the level of skill is, and we can go from there. Thank
10 you very much.

11 MR. HEIM: Yes. Let's quickly go to slide, yes, slide 12. So, the
12 issues that we're going to raise relative to Ground 1 are the three claim
13 limitations, the plurality of input chip select-signals, plurality of ranks, no
14 CAS latency. And then we're going to spend a fair amount of time talking
15 about the motivation to combine, which I think is really critical here. And as
16 listed here, there are three really important points. Incompatible
17 architectures, destroying the principle of operation of Perego, and Perego
18 already provides support for DDR2. We have additional positions on two
19 and three. We'll address those when we get there.

20 But let's go to slide 21. Slide 21 is showing Perego. And this is
21 really just to make sure we're all using the same language. So, Perego
22 discloses a memory module, and external to the memory module it has a set
23 of signal lines that are referred to as primary links or primary channels,
24 shown in blue. And those primary links are going to connect the buffered
25 module in Perego to the memory controller. So, that's the external part.
26 Internally, and the primary links are shown, as I said, in blue. And they

1 come out the bottom, if you will, of figure 3C and figure 4A, from the buffer
2 to an external memory controller. Internally, there are memory devices that
3 form part of the module. That's in the figure on the right, 410A through H.
4 And Perego includes an internal set of signal lines that it refers to as the
5 secondary channels. And so, there are two shown, for example, in 3C, and
6 also two shown in more detail in figure 4A. 4B will show four of those
7 secondary channels. And they're sometimes referred to as a subset of
8 secondary channels to indicate that there's multiples of those. 415a is one, is
9 a subset, 415b, 415c, 415d.

10 So, let's go to slide 24, and let's talk about Perego. So, Perego,
11 interestingly enough, provides examples of prior art memory systems. And
12 one of the memory systems it identifies as prior art is in Figure 1. And what
13 it describes is a JEDEC-style memory system. It's got multiple memory
14 modules, 120A through C. It's got a memory bus. And that memory bus
15 includes a shared control address bus, shared data bus -- a multi-drop bus.
16 So, the same data bus, the same address and control bus are going to be
17 shared by each of those memory modules. And because they're shared, only
18 one memory module can read or write data at a particular time or there's
19 going to be a collision, a conflict on the bus. And so, the way that's handled
20 in this conventional-style memory system is to include separate module
21 control lines. And there are three shown, one for each of the modules. Now,
22 if we're talking about if one of those module had ranks, then that dedicated
23 module control would be two chip-select lines. That's what would be
24 required in the JEDEC standard.

25 Now, if we go to slide 26, there's another prior art system that's
26 described. And it's a Rambus-style architecture. It includes a Rambus

1 channel that's indicated in Figure 2A that connects to three memory
2 modules. They're in a daisy chain connection. And again, only one memory
3 module can respond at a particular time because they all share this same
4 connection. Each module includes a buffer.

5 Now, let's go to slide 27. So, Perego is really clear in its design
6 goals. It is looking for a system architecture or interconnect topologies that
7 provide flexible and cost-effective upgrade capabilities while providing high
8 bandwidth. So, that's the design goal. How do they do that? If we go to the
9 next slide, slide 28, we can see figure 3 and an excerpt from Perego at 5, 32
10 through 55. And this is what Perego is saying. It's identifying what the new
11 architecture and topology are. And what it describes is a dynamic point-to-
12 point topology that includes a unique configurable memory controller. It's
13 not JEDEC compliant. It has a number of configurable ports, 378A and N.
14 So, you see the memory controller 310 and Figure 3B to the right. There is a
15 number of configurable ports, 378A through N on the right side of that
16 memory controller. And they connect directly to different memory modules
17 in this example, 330A through 330C. And what it describes is that's a
18 primary link with link connections, 320A through 320N.

19 So, what this passage describes is, you could have a first plurality
20 of point-to-point link connections 320A between memory controller and the
21 first module 330A, and you can have a second plurality of point-to-point link
22 connections 320B between the memory controller and the second module
23 330B. Then interestingly enough, Perego describes a key aspect of its
24 invention. It says, if the second memory module is removed, if 330B is
25 unplugged from the connector 380B, and that's what's shown in figure 3B,
26 there's a distance now between them. If that happens and it's removed from

1 the system, then the primary link connections 320B that were being used
2 with the second module 330B via the port 378B can be reconfigured, they
3 can be reallocated, and those primary link connections on that port can then
4 be used with the first memory module. So, the primary link to the memory
5 module 330A now would include both its original link connections, 320A,
6 plus the primary link connections that were being used for 320B. So, you
7 can redirect all the system bandwidth to one module because you have this
8 dynamic point-to-point topology that's configurable. That's significantly
9 different from what we saw in figure 1 and 2A. And that's only part of the
10 story.

11 If we go to the next slide, slide 29, same passage, the bottom part
12 talks about a unique new configurable width buffer for the memory module.
13 It supports that dynamic point-to-point topology in which the system
14 bandwidth can be reallocated among different modules, and it provides, as
15 the specification says, it provides the flexibility to configure the module
16 width to connect to both the first plurality of point-to-point connections and
17 now also, that second plurality of point-to-point link connections that I
18 talked about before. Unique buffer design, not JEDEC compliant.

19 So, let's go to slide 30. This is a summary of the key aspects of
20 Perego's high bandwidth memory system that I just talked about. So, I'm not
21 going to repeat myself, but here it is, it's laid out. Slide 32, let's go to slide
22 32. One other aspect of Perego that I think is very important. The memory
23 controller, as indicated in the blue highlighting, the memory controller is
24 going to provide address information on the primary link as part of a primary
25 channel memory request. So, that's what occurs between the memory
26 controller and the module. The buffer module in Perego receives that

1 address and determines the target subset of secondary channel signal lines to
2 select. So, the buffer is going to receive the address and let's say there's four
3 different sub-channels in the module, 415A, 415B, 415C, 415D. It's up to
4 the buffer to determine which of those sub channels is going to be used for
5 that particular transaction. So, the memory controller has all the available
6 space of all the different potential locations for memory devices, but it
7 doesn't know exactly on which memory device a particular address is
8 located. It sends its memory request to a desired address space that's
9 received by the buffer. It selects the appropriate secondary channel to
10 transmit the request to the appropriate memory device, and then the request
11 and address is received by the memory device associated with that particular
12 address. The memory controller does not use or send a chip-select signal
13 because there's no reason to do that because the address command identifies
14 the device specifically. So, let's --

15 JUDGE BRADEN: Counsel?

16 JUDGE JURGOVAN: This is Judge -- oh, go ahead, Judge
17 Braden, really.

18 JUDGE BRADEN: Well, I was going to ask, are you going to
19 address Perego's DDR2 embodiment and the combination with JESD79-2
20 and the chip-select signals there that Petitioner has put forward in their
21 challenge? Because this doesn't seem -- I feel like we're talking past each
22 other. I don't feel like this is really addressing the issue.

23 MR. HEIM: Yeah, let me back up for a second and go to slide 22,
24 and then we'll get into it. Slide 22, so what they're proposing and what is
25 disclosed quite frankly is the DRAM devices, all the embodiments primarily
26 are focused on Rambus DRAM, but it certainly talks about the possibility of

1 having DDR2 or RDRAMs as part of the signaling. And so, let's assume for
2 a second that there are chip-select signals as they are postulating that are
3 provided to the DRAM device. The point is that is done by translation logic
4 in that buffer on the memory device. There is not, there is not going to be --
5 there's no modification that's going to occur to the primary link in the Perego
6 system for a multitude of reasons that --

7 JUDGE GALLIGAN: Counsel, this is Judge Galligan. So, to
8 follow up on Judge Braden's point, I think that's the key right there on page
9 22 of your slides. Petitioner's contention is that one would make the Perego
10 module JEDEC compliant, in which case you plug this thing in, and the
11 computer is going to send chip-select signals, the memory controller on the
12 computer because it says I have a JEDEC compliant memory module. So,
13 your position would then be that you would not make it JEDEC compliant.
14 But Petitioner's position would be, Petitioner's position is that it is JEDEC
15 compliant. Therefore, I don't think there's any dispute that in a JEDEC
16 compliant -- a JEDEC compliant module receives chip-select signals from
17 the memory controller because that's what the memory controller would
18 send, right?

19 MR. HEIM: That's a JEDEC module. It's going to receive chip-
20 select signals on dedicated signal lines. That's the way it's going to work.
21 The issue is, are you destroying the principles of operation of Perego when
22 you do that, when you go from a flexible topology that is disclosed as one of
23 the primary, if not the primary focus of that invention, and now all of a
24 sudden you have to have fixed dedicated chip-select signal lines. And so,
25 that's why it's so important to understand Perego and understand that its
26 operation, because what they're proposing is going to destroy the principles

1 of operation of Perego, because you can't do that reallocation if you have
2 dedicated signal lines. That's it, right? That's it in a nutshell.

3 Let me turn to slide 35, and I just want to quickly address the chip-
4 select signals in just two points of clarification. First, the Board in its
5 institution decision referred to the Jacobs reference to suggest that Rambus
6 architecture can provide chip select information. I just want to respond to
7 that very quickly. Secondly, Petitioner repeatedly is taking the position that
8 Perego is suggesting individual control lines to apply to the primary channel
9 of Perego, and that again is not the way that Perego works. And so, if I
10 could just quickly address those two issues.

11 Let's go to slide 44 please. And so, this is the institution's
12 decision. It's the comment. I just want to make the point very quickly. Dr.
13 Przybylski has clearly refuted the notion that there's a chip-select
14 information that's going to be used in the Rambus architecture. So, to the
15 extent Jacobs is saying otherwise that's, it's just wrong. It's inaccurate. And
16 if we go to slide 47, Dr. Przybylski, he confirms in paragraph 47 that
17 Rambus works as described in the primary link of Perego with each Rambus
18 DRAM having its own unique identification number that's used to send
19 signals to that specific device. And then he shows the Rambus, you know,
20 what's going to be included in a command and it's the address information.
21 It identifies a single device. It doesn't identify a rank. And so, just to be
22 clear on this issue, to the extent there's a question, Rambus does not do that.

23 And then I just want to follow up on the second point. So, we saw
24 repeatedly in the slides of Petitioner. They focus on this last paragraph that
25 is shown at the bottom of column 9 of Perego that talks about the control
26 lines RQ may comprise individual control lines and they say, well, that's

1 referring to the primary link, not the secondary link. And you can see by the
2 context of the prior two paragraphs that that's absolutely incorrect. The first
3 paragraph that starts on 934 is describing an alternative embodiment in
4 which the individual control lines refer to a possible change to the secondary
5 channel 415A and B. And in fact, you can see the bottom highlighting in
6 that paragraph says signal lines of channels 415A and B include control
7 lines, RQ. So, we're talking about the control lines on the secondary
8 channel.

9 JUDGE GALLIGAN: Counsel, this is Judge Galligan. I'm
10 looking at your slide 47.

11 MR. HEIM: Yeah, it should be slide 49. Slide 49.

12 JUDGE GALLIGAN: Forty-nine. Okay. It's not showing up on
13 my computer, but I may have a lag.

14 MR. HEIM: So let me just go back. They're focused on this last
15 paragraph over here. The control lines may comprise individual control
16 lines, the first sentence. The point is if you look at the preceding two
17 paragraphs, it's clear that the control lines RQ being referenced are the ones
18 on the secondary channels. That's the entire context of this discussion. It
19 says in that first paragraph, the signal lines of channels 415a and 415b
20 include control lines RQ. So, it's referring to the control lines on the
21 secondary channel, not the primary channel. And so, Petitioner keeps trying
22 to take the position based on that one sentence, as I think Judge Braden
23 identified, you're building a lot into that. Well, exactly, they're building a lot
24 into it and they're pointing to the wrong location. It's the secondary channel
25 that's being discussed here. It's not the primary channel. And if we go to the
26 next slide, slide 50, I'm sorry. So, slide 50 is this figure 6A, and that's the

1 rest of the paragraph that they continuously refer to. And this is what it says.
2 It says, in the embodiment of 6A, you could have individual device select
3 lines 633a and b that are employed to perform device selection.

4 So, let's say we have a JEDEC system on the secondary channel.
5 How is that system going to work? And Perego tells us this right here and
6 shows it in figure 6A. What he says is there will be, in this instance, if we
7 don't send, if we're just not using the regular Rambus addressing scheme, if
8 we need to send information so that a particular, let's say it's JEDEC, DDR
9 RAM on this device, on this particular module, how is that going to work?
10 Well, this is what the buffer does. The buffer will take that incoming
11 transmission on the primary link, which doesn't have any sort of chip select.
12 It's got the address. But the buffer is going to convert that, if necessary, into
13 these particular individual device select lines. And so, there's no
14 modification that's necessary on the primary channel in Perego. It can
15 already accept the Rambus signaling, which is going to occur over multiple
16 clock cycles because the command and the address and the data are all
17 multiplexed together. So, that's going to come into the buffer. It's going to
18 take that apart. It's going to perform the serialization that we discussed
19 earlier because it's sending in a lot of information over multiple clock cycles
20 as part of a packet. I mean, that's the key. And so, it does that. The buffer
21 then will independently be the device that sends out the select signals. And
22 so that's what the buffer is doing. That's why it's there.

23 Let's go to the next slide. Slide 51. And let's talk about the
24 motivation to combine. And let's go to 52. This is their position. I mean
25 they're saying that a person of skill in the art is effectively going to modify
26 the memory controller in Perego to provide multiple chip-select signals to

1 the memory module. That's what they're arguing. If we go to the next slide,
2 we just saw that the buffer can take signals and can provide the necessary
3 device select signals on the secondary channel to the device. But they're not
4 proposing -- so, it exists on the secondary channel. But this is what they're
5 proposing. They're proposing, let's modify the Perego memory controller
6 310 to generate chip-select signals. It's saying, let's modify the point-to-
7 point link 320 to transmit chip-select signals. And then let's modify the
8 buffer to receive those chip-select signals. And they're even going further
9 than that, I think.

10 And that is, let's even change the translation logic inside the buffer
11 circuit so instead of taking Rambus and converting to other sorts of memory
12 devices like DDR2, let's flip that now because I've changed everything else
13 in the system to JEDEC. So now let's have that logic translate from JEDEC
14 to something else, or JEDEC to JEDEC, or JEDEC to Rambus. I mean, this
15 is a wholesale redesign, reconstruction of the Perego system that they are
16 proposing in their obviousness contention. So, let's talk about each. Let's
17 break it down. So, first of all, the next slide, slide 54, there's three things I
18 want to talk about. A, they're fundamentally different architectures, JEDEC
19 and Rambus, fundamentally different. Second, it would -- modifying Perego
20 in this fashion would destroy its principles of operation. And C, Perego
21 already provides a solution to accommodate DDR2 devices.

22 If we go to slide 55, I'll just start with Dr. Przybylski very quickly.
23 He indicates that the patent talks about using JEDEC-compliant DRAMs in a
24 multi-drop memory bus with conventional signal trace topologies. The
25 essential and radically different approach of Perego is the focus on dynamic
26 point-to-point topology, configurable data width paths, the ability to

1 reallocate data lines on the primary channel without losing the ability to
2 access all the storage locations.

3 Let's go to slide 56. We saw this slide already, but this is what Dr.
4 Przybylski is referring to, the dynamic point-to-point topology, the ability to
5 reconfigure. So, extreme cases that are described. What if you -- you could
6 have one module that gets all 128 connection links. You have 128 modules
7 that get one connection link. And so, you have signaling that occurs on one
8 line. None of those features that are the focus of Perego are compatible with
9 the JEDEC-style implementation. JEDEC has a fixed-width interface for the
10 memory controller. It has a fixed-width bus. It cannot reallocate bus lines
11 or interface connections among different modules. And it includes a
12 dedicated chip-select signal for the memory module that cannot be
13 reallocated.

14 We go to slide 57. The flip side is at the buffer device. It's a
15 unique configurable-width buffer device. And it works hand-in-hand with a
16 dynamic point-to-point topology. It's not JEDEC compliant. It has a fixed
17 width with a multi-drop bus, just as we saw in Perego Figure 1. They're
18 saying, hey, let's throw out all of this new stuff, this great new stuff, the
19 dynamic point-to-point topology, and let's go back to Figure 1 and let's use
20 that. I mean, that's what they're arguing. Fifty-eight, again, none of these
21 points or advantages exist in JEDEC standard implementation. They all
22 have to be changed. And as Dr. Przybylski says on slide 59, a person skilled
23 in the art would not be motivated to combine together the architectures for
24 various reasons. And so, one other point relative to the compatibility issue,
25 paragraph 51, slide 60, in JEDEC-style DIMMs, the DRAMs are ganged
26 together in parallel to provide the necessary aggregate bandwidth, right?

1 That's the rank concept. In direct, in the Rambus system, the memory
2 devices, they span the entire channel, and the CPU accesses each device
3 independently so that one device can add to the others. And so, only one
4 device can talk at a time. That's the point in this system in Perego.

5 Slide 61. Let's go to point number two, which is that modifying
6 Perego with a JEDEC-type memory controller, memory bus, memory
7 module interface is going to require a substantial redesign of Perego. It's
8 going to change the basic principles under which it operates, and it's no
9 longer operable for its intended purpose. Let's go to slide 63. Slide 63, this
10 is what you're changing by moving to a JEDEC system as they're proposing.
11 You're losing the dynamic point-to-point topology. You're losing the
12 configurable width memory controller. In fact, what they're pointing to, I
13 believe it was slide 55 in their slide deck. The answer, according to Dr.
14 Wolfe is, let's take some jumper pins and just make it a fixed width memory
15 module. I mean, that's the answer to how -- that's how drastically they have
16 to redesign this system. They are literally going in and if you can see, he's
17 saying that I can make it JEDEC compliant, and one of the ways of doing it
18 is to configure it to have a resistor or jumper that's installed at manufacturing
19 time that configures it to a fixed bit width.

20 In that case, I can make it JEDEC compliant. I -- this -- it's
21 amazing the amount of changing of Perego that they have to talk about to try
22 to make Perego a JEDEC compliant device. Why, because they, they can't
23 find a buffer in a JEDEC compliant device. They go to Perego and then they
24 change everything about Perego. So much so that they push Perego back to
25 Figure 1 at the end of the day. Let's talk about the next slide, 64. So, let's
26 talk about what it is they're proposing. So, in Perego, if a connector or slot

1 becomes unpopulated, Perego can retain the full system bandwidth. And it
2 also retains the complete addressable space to all the memory in the system.
3 Now, if you modify this Perego memory controller and primary link to be
4 compliant with JEDEC and includes -- to include a plurality of chip-select
5 signals, so the primary link is modified to conform to JEDEC-style
6 signaling. That means each socket now has dedicated chip-select signals.
7 So, a CS 0 and a CS 1. And the second module has chip-select signals. And
8 so, if a memory module is now removed from slot 380B, for example, there's
9 no ability to dynamically redirect the link connections that are associated
10 with those chip-select signals to a different socket or connector. The chip-
11 select signals are dedicated lines to specific sockets. You can't dynamically
12 reallocate the chip-select signals. They're not switchable.

13 So, only connector 3ADB can support the chip-select 2 and 3. You
14 can't modify to include more chip-select lines in connector 3ADB. So, what
15 does that mean? You lose the bandwidth. If you remove that module, you
16 have lost the bandwidth to be able to -- that you were using on module
17 330B. It's just gone. And so, again, the basic operating principles of Perego
18 are the ability to retain that bandwidth, to operate at the high bandwidth,
19 even as system conditions are changing, including this chip-select,
20 dedicated chip-select lines, takes away that capability. And it goes hand-in-
21 hand. Next slide, 65. It goes hand-in-hand with a dynamic width interface.
22 If you change one thing in the system to make it JEDEC compliant, you've
23 got to change everything. You've got to change the memory. If you change
24 the memory controller, you've got to change the primary link. To have a 64-
25 bit wide bus that you can't dynamically reconfigure, you get a buffer that can
26 no longer have a configurable width. And so, it all falls apart like a house of

1 cards when you start doing what they're proposing and changing the system
2 to a JEDEC-style architecture.

3 And all it does is it kicks you right back to Figure 1, of Perego,
4 because that's where you end up. And so, the next slide, 66, Dr. Przybylski
5 is confirming that if you make the changes that are proposed by the
6 Petitioner, you're going to change the operating principles of Perego. The
7 addressing scheme is going to have to be done differently. You're going to
8 have to use chip-select signaling now with the dedicated signal lines.
9 You're going to have two memory modules, each with two ranks. If you
10 lose one module, you lose the ability to access that module completely and
11 its two ranks.

12 JUDGE GALLIGAN: Counsel, this is Judge Galligan. I had one
13 question to follow up, or an issue to follow up on. That disclosure in
14 Perego, column 9, lines 58 to 60, Petitioner's position is that that refers to
15 control lines to go to the module. Does Dr. Przybylski opine on that?

16 MR. HEIM: Yes, I believe so. I have to find that for you. I can
17 give it to you after in rebuttal to talk about that. But there's a lot of evidence
18 on that, I believe.

19 JUDGE GALLIGAN: Okay. Thank you. Just -- just let us know
20 in the sur-rebuttal. Thank you.

21 MR. HEIM: Yes, that would be great. So, slide 71. So, this is the
22 legal point, right. This is what it's all about. So, the seminal case is In re
23 Ratti, decided a long time ago by the CCPA 1959. And what they said is
24 there's no motivation to combine if the suggested combination would require
25 a substantial reconstruction and redesign of the elements in a reference and
26 change its base, as well as changing its basic principles under which it was

1 designed to operate. It's a principle that's cited all the time, cited by the
2 Board all the time. It was cited recently I believe in the Samsung vs. Mojo
3 case. If you change the basic principles under which a reference is designed
4 to operate, that's an indication that you don't have a proper obviousness
5 position. And that's the issue. I mean, it's a key issue. Then slide 72.

6 JUDGE JURGOVAN: Counsel, can I interrupt for a second?

7 MR. HEIM: Yes, of course.

8 JUDGE JURGOVAN: And that is to ask, you know, when column
9 9 of Perego 422 is discussing these individual device select lines. Isn't that a
10 different sort of architecture than the addressing of individual devices you
11 were explaining earlier?

12 MR. HEIM: Absolutely. Absolutely it is. And so, if I -- was there
13 another question, I'll follow up on that?

14 JUDGE JURGOVAN: Well, I, I'm, I'm just wondering, you know,
15 that seems to me to be JEDEC compliant, is it not? I mean using chip-select
16 signals and then those pass through as these individual select lines and then
17 select one particular device, but in Perego 422.

18 MR. HEIM: Let me just clarify. So, what is received on the
19 primary channel is not going to include chip-select information. It's not
20 necessary.

21 JUDGE JURGOVAN: Well, it will if it's connected to a JEDEC-
22 style memory controller, correct?

23 MR. HEIM: If you completely redesign the memory controller,
24 the primary link, and the module to be able to accept those signals, then if
25 you -- and if you do all those things, then you have input chip-select signals.
26 Then --

1 JUDGE JURGOVAN: And then they could use these individual
2 device select lines. Correct?

3 MR. HEIM: It -- so then you don't even need the buffer, right?
4 You have -- if you have those individual -- if you already have the chip-
5 select, then the buffer doesn't need to do the translation. It's just going to --
6 you've taken out what the buffer is doing. The entire -- they say this, they
7 say, well, don't worry about it. The translation logic in the buffer is optional.
8 You don't have to have that. And so, again, they're changing another piece
9 of this. But if you have, let's follow the hypothetical, if you have chip-select
10 signals that are coming into the buffer, they can be passed to the end, in that
11 example, they would be passed to the individual devices, and you would tear
12 out that buffer translation logic capability.

13 JUDGE JURGOVAN: Well, you can't tear it out because let's say
14 you have eight devices, you're gonna need three different incoming signals
15 to select one of those eight, right?

16 MR. HEIM: Well, no, the JEDEC standard only allowed two to
17 come in, I think at that time. But let's say that --

18 JUDGE JURGOVAN: Let's say it's two.

19 MR. HEIM: Let's say you need more than what you have, then the
20 buffer is going to do what was being done in Figure 1 at the end of the day,
21 it's gonna do exactly what was done in Figure 1. I mean, there's -- well,
22 there's no buffer in Figure 1, but it's going to provide the same signals as the
23 memory controller effectively, and just pass those chip signals onto the
24 ranks. Now, there's a separate issue, of course, whether or not those are
25 ranks that I'm going to get to, because they're not. But --

26 JUDGE JURGOVAN: Well, let's say I want to use, for whatever

1 reason, I want to use Perego 422, as the Figure 1 embodiment. I want to use
2 its flexibility to emulate the figure one embodiment. What's wrong with
3 that?

4 MR. HEIM: The how and why. How and why are you going to
5 take this fixed system in Figure 1 and be able to use all this great new
6 reconfigurability that exist in Perego? That's the missing piece. That's
7 another missing piece of that. They -- they just ignore all of these principles
8 of operation and revert back to effectively Figure 1 at the end of the day. All
9 they're doing is putting the buffer in there. You're left with the buffer of
10 Perego in the system is what they're trying to suggest I think at the end of the
11 day.

12 JUDGE JURGOVAN: Okay. But I mean, isn't there some value
13 in having something that's reconfigurable and maybe in one application use
14 it in, you know, a Rambus-style system and then another application you use
15 it in a JEDEC-style system?

16 MR. HEIM: But you can't do that because it has to be fixed. You
17 have to have to have it fixed for the JEDEC-style system. You have to
18 have --

19 JUDGE JURGOVAN: It needs to be fixed? Why? Why do you
20 have to have -- I mean if you have dedicated lines, that's fine, but you can
21 undedicate them, couldn't you? Use them in a different context?

22 MR. HEIM: Not according to JEDEC. I mean, the JEDEC
23 standard is very strict. You have --

24 JUDGE JURGOVAN: And I understand. I understand that. But
25 if I take that module out now, I can plug it into a different computer system,
26 a Rambus style system and configure it up to operate with that computer

1 system. You don't see any value to that?

2 MR. HEIM: I don't -- nobody has explained how that would be
3 done. There is zero evidence in this case of how you would redesign the
4 system to be able to do that.

5 JUDGE JURGOVAN: Okay. Thank you.

6 JUDGE GALLIGAN: Counsel, this is Judge Galligan. I wanted
7 to follow up on that a little bit going back to that disclosure in column 9, and
8 I'll look forward to Dr. Przybylski's testimony on why those RQ lines don't
9 apply to the primary interface. But I, you know, I understand your argument
10 is that there's this wholesale redesign. And one thing that gives me pause
11 about that is that Figure 6A basically says we have, you know, first of all,
12 we're focusing a lot that the assignee is Rambus and I understand Rambus
13 generated this different kind of addressing system, a packetized sort of
14 addressing system within memory. But then in Figure 6A, Perego basically
15 says, yeah, just do dedicated lines. That, to me, says you can ignore what
16 we said and, you know, do JEDEC style, too.

17 Now, to take your point, your point is that that doesn't say it on the
18 primary channel between the memory controller and the module. But that is
19 sort of a wholesale reconstruction, and Perego says to do it. So, that's where,
20 and, you know, if there's some reason, like, for instance, JEDEC is the
21 dominant standard. So, to Judge Jurgovan's point, why wouldn't you want
22 something that plugs into a memory controller that, you know, spits out
23 JEDEC control signals? So that's kind of the, putting aside whether 958,
24 column 9, 58 to 60 is applying only to the internal chip-select network.
25 Let's, for lack of a better word, it does seem like it's proposing sort of a
26 redesign or sort of going against the Rambus grain there. So how would you

1 address that?

2 MR. HEIM: Let's go to slide 73. So, what is being shown in
3 Figure 6A -- 73. So, what is being shown in Figure 6A is this notion that I
4 could have JEDEC-style memory devices, and I'm going to figure out how
5 to deal with it. And it's up to the buffer to figure out how to deal with it.
6 And the passage in Perego at 10, 54 through 67 indicates that the buffer
7 device can render the type of memory device transparent to the system. The
8 memory controller doesn't even know what type of memory device it is,
9 right? The primary link doesn't know what type of memory device it is.
10 And so, different types of memory devices can be included by employing the
11 buffer device 405 to translate protocols employed by the controller to that of
12 the memory device. And so, it's the translation that exists in Perego that is
13 going to do that. And the reason you get those signals on the secondary
14 channel is because you have this buffer translation capability that exists.

15 So, the notion that I have this buffer translation capability that
16 exists already, I'm going to, even though we can translate to JEDEC-style
17 signaling, I'm now also going to include it on the primary channel. When I
18 have that capability, the reason you have that translation capability is to
19 allow this super flexible and dynamic primary channel and memory
20 controller. And then leave it to the buffer that, in a sense, is kind of a mini
21 memory controller. It's its own controller that's able to take the signals and
22 figure out, take the incoming signals from the memory controller. But then
23 it performs all of its own operations in order to work with the memory
24 devices. And so, that's the answer to the question, is it's in there already.
25 And so, let's say you take that out and you just do a straight pass through.

26 At the end of the day, what you're doing is, is you're turning

1 Perego into Figure 1 prior art that they spent a lot of time and effort
2 describing a much better system and it's being all stripped away. Why? It's
3 being stripped away so we can match it up with the claims of the '417 Patent.
4 That's, I mean, it's just a hindsight reconstruction, redesigning the entire
5 system. If we can go to slide 74. Just a quick point, I mean, throughout
6 their presentation, there are misrepresentations that occur. This is one
7 example. They keep saying that Perego supports new generations of
8 controllers. If you look at the passage, you can see that's not what it says.
9 What it says is backward and forward compatibility with memory devices,
10 high degree of flexibility, and then relative to the controllers, new
11 generations of controllers may be phased in, which exploit features of the
12 new generations of memory devices while retaining backward compatibility
13 with memory devices. It's not saying you need to have backward
14 compatibility with the memory controllers, some of future controllers. Why
15 would you, again, why would you take this great new memory controller
16 that you've designed with all these capabilities in order to make it
17 compatible with past generations like Figure 1 and Figure two 2A, it defies
18 logic.

19 Let's go to slide 78 and just, again, I want to go back to this Figure
20 6A since you mentioned it. So, Perego's buffer is performing the translation
21 that's necessary to accommodate the other types of memory devices. It's not
22 necessary, and there's no modification that's required on the primary channel
23 to do that. So, you can leave the primary link point-to-point, not JEDEC
24 style. You don't have to change the primary channel to make it JEDEC
25 compliant, and you can use DDR2-type memory with it, so the system can
26 do that already.

1 Okay, if we may, unless there's any other questions, I'll go to the
2 CAS latency limitations on slide 79. And on 80 and 81, we show the CAS
3 latency limitations. On 80, just I want to highlight that the CAS latency that
4 we're talking about is due in part to the delay through the circuitry, through
5 the data path, and not to registering the control or address command signals
6 coming in. Or the delay relative to the memory devices themselves. And so,
7 let's go to slide 82. Petitioner refers to Exhibit 1062, the DDR RDIMM
8 standard. Next slide, slide 83. This is the RDIMM standard. What it shows
9 is a register. There's no data buffer on the RDIMM. There's only a register.
10 What does the register do? You can see it in the figure in the right. All it's
11 going to do is receive address and command signals, and it's going to output
12 address and command signals. You can look a long time, and you're not
13 going to see any data coming in or data coming out in that register.

14 Slide 60, I'm sorry, slide 84. They also refer to the DDR2
15 SDRAM specification. If we go to slide 85, it's talking about the bank, this
16 slide from Exhibit 1062 is referring to the additive latency that must be
17 programmed into the device to delay when the read-write command is
18 issued. Again, posted CAS. The command is held for the time of the
19 additive latency. Clearly, these do not specify the module-level timing
20 delays. And as indicated, it's referring to the commands. It's not referring to
21 the data. That's passing through a data buffer. So, it indicates the command
22 is held for the time of the additive latency.

23 Let's go to the next slide, 86. So, in Ground 1, the petition is also
24 making a conclusory argument. It would have been obvious to add one
25 clock cycle to Perego for the same reason as additive latency. And so, it's
26 just hindsight. With regard to Perego, there's no concept of CAS latency at

1 all. It doesn't use CAS signals. The memory controller in Perego doesn't
2 issue a CAS signal. As we said, it's not JEDEC compliant. There's no
3 reason to provide CAS latency in Perego in the Perego memory controller,
4 even if DDR2 memory is used on the secondary channel, because that's
5 generated by the buffer. So, there's no strict timing requirements in Perego.
6 And so, to tie this additional registering and the transfer of the data to CAS
7 latency in Perego, is just hold out a thin cloth. And that's all they cite, is
8 Perego for this. So, where is it coming from? It's not coming from Perego.
9 Well, they cite three passages along the bottom of the petition on 95. None
10 of them support its position that registering data transfers through the
11 circuitry is for an amount of time delay related to an overall CAS latency.

12 So, let's go to slide 87. In paragraph 184 of Dr. Przybylski, he
13 analyzes the three paragraphs. He said none are applicable to the issue here
14 relative to registering data signals for the interfaces 520 A and B with
15 latches 597 F through M using an internal clocks circuit. So, relative to the
16 first passage, discussed it, and that's 12, 65 through 13, 5 of Perego. Dr.
17 Przybylski makes it clear this relates to a global clock source for the buffer.
18 And what it's doing is it's adjusting two clock signals, an external and an
19 internal one, so that they meet phase requirements. So that the rising edge
20 matches, the falling edge matches. So, it's used for synchronization. If we
21 go to slide 89, it again indicates that it's being used for this phase alignment
22 purpose. And further, if you look at, you can see in the middle of this page,
23 he cites Exhibit 2035 at one. If you look at that exhibit, last sentence on that
24 page, it specifically says that the phase alignment allows data to be
25 transferred across clock boundaries without incurring any additional latency,
26 no additional latency. That is the reason that you're doing this phase

1 alignment.

2 If we go to slide 90, paragraphs 186 of Dr. Przybylski, he
3 addresses the other two passages that are cited, 1761 through 63 only relates
4 to the structure of the multiplexer and deep multiplexer. And it has nothing
5 to do with its timing. And the passage at 18, 65 through 19, 3 is about
6 whether the multiplexer de-multiplexer is implementing a full or cross or a
7 partial crossbar. That means every input can match every output has nothing
8 to do with timing.

9 Let's go to slide 95 and let's talk about ranks. So --

10 JUDGE GALLIGAN: Counsel, this is Judge Galligan. I had a
11 question on the CAS latency before we move on.

12 MR. HEIM: Yes.

13 JUDGE GALLIGAN: In the Patent Owner's response at page
14 37, it says it's the last sentence of the first paragraph. And if you can bring it
15 up, it's good. It's in the in the '454 case.

16 MR. HEIM: You said page 31?

17 JUDGE GALLIGAN: Sorry, page 37 of the '454 Patent Owner
18 response.

19 MR. HEIM: Yes.

20 JUDGE GALLIGAN: Yeah, it's that. So, that sentence of the very
21 last sentence of the first paragraph, it says, moreover, the concept of using
22 the additional clock cycle caused by delay through RCD for delaying data on
23 the path, on the data path, comes from the inventors, citation to column 22,
24 41 to 56. And it's improper to use the inventor's hindsight inside against
25 them. I wanted to ask about that. So, I was looking at that passage, and at
26 22, 41 to 56. And it seems so that on 22 line 46, it says the extra cycle of

1 time in certain embodiments advantageously provides sufficient time budget
2 to add a buffer which electrically isolates the ranks of memory devices from
3 the controller memory controller.

4 MR. HEIM: I'm sorry, can I interrupt you? Where were you, 21?

5 JUDGE GALLIGAN: Sure.

6 MR. HEIM: Where were you, 21?

7 JUDGE GALLIGAN: Yeah, sorry. The column that you cited in
8 the brief column 22.

9 MR. HEIM: Okay.

10 JUDGE GALLIGAN: And I was looking at on 22 line 46. I think
11 what's cited is column 22 lines 41 to 56. And the line 46 there, it says this
12 extra cycle of time in certain embodiments advantageously provides
13 sufficient time budget to add a buffer which electrically isolates the ranks of
14 memory devices from the memory controller. So, that's, I mean, putting
15 aside whether Ellsberry's prior art, buffering seems to—data buffering, you
16 know, was in Halbert, for instance. And it talked about isolating memory
17 devices from the memory controller. And then it says in certain
18 embodiments, two sentences down, the buffer adds a one clock cycle time
19 delay, which is equivalent to a registered DIMM to accomplish the address
20 decoding. So, I was wondering, that sounds like what it's saying is you're
21 going to buffer data because there's a, it gives you a way to, if you put a
22 buffer in there and it isolates the memory devices from the memory
23 controller and the memory bus, that's all good. But if you just match what
24 was already in the RDIMM spec, that doesn't sound like -- it sounds like the
25 inventor's insight was adding buffering. It doesn't sound like the inventor's
26 insight was the delay because the delay is admitted to be the RDIMM delay.

1 Can you address that, please?

2 MR. HEIM: Yes. So, the RDIMM delay is not relative to the data
3 path. The RDIMM delay is relative to you get input control and address
4 signals. And you're going to register them. That's going to produce a clock
5 cycle delay. And then that's going to be applied. That registered signal is
6 going to be applied to the memory devices. Okay. So, the additional clock
7 cycle we're talking about is relative not to the data path, it's relative to the
8 address and command signals. Okay? So, what this passage is saying is
9 what we can do is fool the system and we can add a clock cycle to the CAS
10 latency that we report, the module reports to the memory controller, to say,
11 hey, even though our memory module has, let's say, a four cycle latency,
12 we're going to add a data path buffer. We're going to take a full cycle to
13 register the data, clean it up, do whatever we need to do, and we're going to
14 then report -- we're going to hide that. We're going to report that the CAS
15 latency is actually five cycles. So, that's what's being described here. The
16 only analogy to RDIMM is you're taking a cycle, but the RDIMM is
17 registering an entirely different signal and it's doing it really before the
18 period of the CAS latency. That would be, you know, for example, an
19 additive latency sort of period.

20 JUDGE GALLIGAN: Okay. So, this is Judge Galligan. Just to
21 clarify, I understand that the RDIMM doesn't -- you know, previously the
22 RDIMM didn't buffer data, it buffered address and control. So, this isn't
23 saying to just use what was already the delay caused by the buffering of the
24 address and control. And then you just take advantage of that delay because
25 you want to buffer, and the buffer provides isolation. You're saying you
26 take, there's already, RDIMM already has a CAS latency that's one greater

1 than memory devices. And now it's going to be two greater because you're
2 adding another cycle of time for the data buffering? Is that what you're
3 saying?

4 MR. HEIM: Yes, absolutely. That's correct.

5 JUDGE GALLIGAN: Okay. So, the CAS latency of the memory
6 device is, sorry, the CAS latency of the memory module is two clock cycles
7 more than the CAS latency of each memory device?

8 MR. HEIM: The CAS latency, well, first of all, the claim is not
9 directed to the address -- delaying the address or control signals. It does
10 require registering, doesn't talk about any timing requirement relative to the
11 registering of the address and control signals. But let's assume that there is
12 registering that occurs that the claim requires it. Let's assume that you're
13 going to take a clock cycle to do that. What this claim is requiring is on the
14 data path side, right, it's very specific to the buffer on the data path side and
15 you're going to add a cycle to the CAS latency period based upon that data
16 buffer. If you take it all together relative to the memory module, that could
17 produce a two clock cycle difference, but just understand that CAS latency is
18 usually measured from the time that the command is received at the memory
19 device.

20 JUDGE GALLIGAN: Okay. I think I understand. Thank you.

21 MR. HEIM: Yes. If we could, let's go to slide 98. So, Petitioner
22 is proposing that Perego discloses ranks. And what it does is it identifies
23 various ranks that it refers to, and it highlights them in green as one rank and
24 blue as another rank. And so, the question is, do these green and blue
25 memory devices, do they act together in response to a memory command?
26 Does the memory command include one active chip-select signal and one

1 non active chip-select signal? And do the selected green or blue memory
2 devices that are reading or writing, do they do so consistently with a full bit
3 width of the memory module? And so, the petition in slide 99 is proposing
4 that you could arrange these memory devices in an aggregate width that
5 would be 64 bits, 16'x4', 8'x8', 4'x16'.

6 Let's go to the next slide, slide 100. So, Perego does not disclose
7 or have any concept of rank. And relative to the issues of whether the
8 memory devices, the green ones, and the blue ones, whether the green ones
9 work together or the blue ones work together, the answer is they don't. Each
10 of the memory devices on a particular channel are accessed and will operate
11 independently. They're addressed independently. They decode the address
12 and execute the command that's intended for it. They respond by
13 independently reading or writing data only to one device. And because they
14 all share the same data lines, it's the same multi-drop bus, only one of those
15 devices can receive or output data signals at any given time to avoid
16 solutions.

17 JUDGE GALLIGAN: Counsel, this is Judge Galligan. I wanted
18 to ask you about Perego column 6 starting at line 19. It says one or more
19 memory devices of memory devices 360 may respond by transmitting data
20 to the buffer device, you know, on a memory, on a read command. So, why
21 isn't that saying that there could be multiple devices acting together?

22 MR. HEIM: I'm sorry, you were referring to column 6?

23 JUDGE GALLIGAN: Yeah, Perego, column 6 starting at line 19.
24 Does one or more of memory devices may respond—that sounds like
25 multiple memory devices could, you know, act on a read, for instance, and
26 provide and act together.

1 MR. HEIM: Yeah, let me respond to that. So, in the instance
2 where you have, let's look at Figure 4A in this slide 100. So, 4A, what you
3 can have is one memory device can respond on channel 415A, and you can
4 have one memory device that is responding on 415B. So, across the
5 multiple channels, yeah, you could have one or more devices. Within a
6 channel, you can only have one memory device that's responding because of
7 the fact that these are shared data lines. The DQ line is shared. It's a multi-
8 drop bus. Otherwise, you're going to have data collisions. And so, Dr.
9 Przybylski testified to this Exhibit 1095, page 211, exactly one memory
10 device responds to any transition on the channel at a time. So, the devices
11 that Petitioner is identifying as a rank don't work together in response to a
12 memory command. They work independently.

13 Let's go to the next slide 101. If, so let's take their example. Let's
14 assume there's 4'x16' devices in green, 4'x16, devices in blue in Figure 4A.
15 So, with the two channels, 415 A and 415 B. If the memory device with --
16 so each of these devices, again, they share the same DQ lines. So, one green
17 memory device can read or write data. And if it does, it'll have a width of 16
18 bits. It does not produce an output of 64 bits. If you have another read or
19 write that occurs to the blue, the memory devices on 415 B, again, you're
20 gonna get 16 bits of output. If you look at Figure 4B, those are 8'x8's, the
21 way that they have identified them in green. Again, even if they're, if they're
22 acting together, you're gonna get eight bits out. If both 415c and 415d are
23 operating together, you would get 16 bits out. Now, that puts aside the
24 requirement that you can only have one active chip select. So, let's say now
25 we're talking about JEDEC, and we've got this channel arrangement. Only
26 one of those channels can be active according to the claim language. You

1 can't have more than one active. That means you only get one of these
2 channels and you'll only get one of those devices in the situation where you
3 can only have one active chip-select and one inactive chip-select.

4 Now, if we go to slide 102, the Petitioner is very focused on the
5 passage at 15, 37 through 45 in Perego. And so, let's go to slide 103 and
6 address that. And they're focused on that another benefit sentence. Let's
7 back up and talk about what the benefits are and where they're coming from.
8 What this paragraph is describing is that the secondary channels, 370 can be
9 arranged with subsets of secondary channels. That's 415a is a subset, 415b
10 is a subset. And then Figure 4B will also add two additional channels. So,
11 you might have four subchannels in that example in Figure 4B. So, the first
12 benefit is you can use only, let's say one of the subsets, only 415a, and you
13 could say power. You don't have to supply power to the b, c, and c, 415b, c,
14 and d.

15 The second benefit is you can group memory devices into multiple
16 independent target subsets based on the subset of channels. What's the
17 point? So, what it's saying is that you can increase the number of
18 independent target subsets by having more of these channels. So, you could
19 have four of them, and now you can access one device in each of those four
20 subsets of channels. So, it's not saying that you're getting more ranks that
21 are going to work together. It's just saying, if I have the architecture with
22 more sub channels, I've got more memory devices that I can access. That's
23 all its saying. It doesn't mean that the memory devices in these independent
24 banks work together. They can only operate one at a time. So, let's go to
25 104.

26 JUDGE GALLIGAN: Counsel, this is Judge Galligan. I just want

1 to give you a heads up. You're at an hour and 12 minutes in. It's your time.

2 Use it however you like. Thank you.

3 MR. HEIM: Okay. I'll just go a few more minutes. So, Dr.

4 Wolfe, slide 104, he essentially admitted this in a different case. Now he's

5 got a different testimony in this case, but in the prior case, when he was

6 asked about the independent banks, he says that means the number of page

7 registers which can be activated corresponding to different addresses. He's

8 saying in Technospeak exactly what I just said. That is, if I have multiple

9 channels, I can open a page on each of those channels to access one device.

10 Slide 105, Dr. Przybylski confirms the passage, has nothing to do with

11 ranks.

12 So, in last slide on ranks, and then I'll stop. So, the issue has come

13 up relative to the simultaneously language in Perego. That occurs in 10, 22

14 through 40. And so, it indicates that in alternate embodiments, channels

15 415a and 415b operate simultaneously with channels 415c and 415d to

16 realize greater bandwidths. That allows memory devices on two channels,

17 or if you use all four channels to be able to be used at the same time. Again,

18 that's referring to one memory device per channel. But in addition, the

19 claim requires that a rank can receive an active chip-select value while all

20 the others receive a non-active chip-select value. If these are JEDEC

21 memory devices, what that means is to get this simultaneous capability, you

22 have to have multiple chip-select signals that are active, even if you're using

23 a JEDEC style system in this architecture.

24 And with that, let me just go on and cover one point very quickly

25 relative to Ellsberry. If we could go to slide 122, I believe, is what it is. So,

26 Ellsberry relative to CAS latency. This is it. What's highlighted is it. If CL

1 mode equals subtract CL equals CL minus 1 to DDRs, there's no explanation
2 in Ellsberry whatsoever about what any of that means. It raises more
3 questions than it answers. The petition refers to four passages. Paragraph
4 44 of Ellsberry, which refers to a squelch function of EMRS. Paragraph 30
5 refers to memory banks, a switch coupled to memory, I'm sorry, a memory
6 bank switch coupled to memory banks. It refers to clocking information
7 received from a DIMM interface, and 48 refers to an external phase lock
8 loop that provides a clock signal to the memory module. None of those
9 explain what this means, what CL means. So, what, you know, what's the
10 explanation? The most likely explanation is that Ellsberry is trying to have
11 its circuit appear to the memory controller as a registered DIMM device.
12 And so, what -- that's Exhibit 1062, we talked about that earlier. So, what's
13 being done is to account for the register delay of the address and control
14 signals is the most reasonable conclusion relative to this. And so, with that,
15 I'll reserve the rest of my time. Thank you.

16 JUDGE GALLIGAN: Counsel, this is Judge Galligan. I do want
17 to ask you about the priority issue and going back to the '087 provisional.

18 MR. HEIM: Yes.

19 JUDGE GALLIGAN: So, as you can imagine, I spent some time
20 on this and at first I was trying to figure out what the path was back to the
21 '087, but it appears in one of your slides, you said now the path is back
22 through the '537 Patent. Is that correct?

23 MR. HEIM: That's absolutely correct, Judge. If we go to slide
24 109, you can see straight line continuations from '215 and '417 all the way
25 back to the application that issued as the '537 filed January 19th, 2006,
26 exactly one year after the '087 provisional. And if you go to the very next

1 slide, you can see that the '537 Patent claims priority to the '087 and
2 incorporates it by reference.

3 JUDGE GALLIGAN: Yeah, thanks. So, with that and I didn't see
4 that in the brief and that's what the briefs and that's what I was, you know
5 there's a million paths here and I think in the other cases we had there were
6 two paths. So, I mean it's helpful to spell out what the path is because some
7 of the citations, for instance, in the chart you give it looked like they were to
8 unbuffered—like Provisionals that talk about unbuffered DIMMs, which I
9 wouldn't think would have much relevance here, but I did want to talk about
10 the issue of this.

11 MR. HEIM: Can I respond to that just very quickly?

12 JUDGE GALLIGAN: Sure, sure.

13 MR. HEIM: If you look, every single limitation has a site to the
14 '087 provisional. Every single one of them. Look at their own slides. Every
15 single one of them provides a citation to every single limitation that satisfies
16 Dynamic Drinkware. We -- they went through, they did a mapping,
17 identified the paragraphs from the '087 provisional, that include every single
18 limitation.

19 JUDGE GALLIGAN: I appreciate that. Yeah, thank you. This is
20 Judge Galligan. So, what is a little frustrating is that there's no citation to
21 the '537 Patent. And the reason I say that is because there was disclosure
22 added to the '537. So, the '087 says what it says, and there's this data path
23 multiplexer, but the '537 then has more detail. And so, for instance, so I
24 wanted to just run this down with you. In Dr., I think it's Dr. Przybylski who
25 has maybe a better description of this. But the data path, I just wanted to
26 make sure I understand, the Patent Owner's contention is that the data path

1 multiplexer in the '087 Patent is what receives the data buffer control
2 signals. Is that correct?

3 MR. HEIM: That is correct. Slide 113. That's exactly what it is,
4 113, 114. That's absolutely correct. There's the logic you see in a figure
5 that looks very similar to Figure 1. And what seven says is that figure has a
6 logic translation element that's going to perform address decoding logic for
7 rank multiplication. So, it knows where the signals are going to go to, which
8 rank it's going to go to. Next paragraph says it also includes a data path
9 multiplexer, demultiplexer. And then on 17 next slide, what it says is that --
10 it says the multiplexer, demultiplexer provides DQ paths for each rank of
11 memory devices and the data transfers are registered for the additional clock
12 cycle. What Dr. Przybylski says, I believe on the next, is it the next slide?
13 No, it's on slide -- there it is. Slide 115. He explains that because you have
14 this decoding logic, the logic is -- a person skilled in the art would
15 understand that because you have this address decoding logic to figure out
16 which rank you need to go to, that that device is -- and it provides -- it's
17 going to provide the control signal to the multiplexer, demultiplexer. You
18 have to have a control signal. There's no debate about that to a multiplexer,
19 demultiplexer. A person skilled in the art would know that's where it's
20 coming from. That's what Dr. Przybylski says. It's at paragraph 82 of his
21 declaration.

22 JUDGE GALLIGAN: So, I wanted to follow up on that briefly.
23 This is Judge Galligan. And the reason I say it would be helpful to cite the
24 '537 is that the '537, for instance, and this is Exhibit 1032, '537 Patent
25 column 8, line 30 says, well, it talks about how the switches can be a data
26 path multiplexer, demultiplexer, and says the switches receive control

1 signals from the logic element. But that isn't in the '087 Patent. And
2 Petitioner says, well, you could get, for a multiplexer, you could get control
3 signals from outside. That they could just come from the memory
4 controller. And if you look at, for instance, Figure 10B of the '537 Patent,
5 and I don't know if you want to bring it up, but it shows these multiplexers,
6 and it actually uses the column -- the CAS to column address strobe signal
7 as the control signal. But that comes from the memory controller. That
8 doesn't come from the logic. So, why is it an unreasonable position to say,
9 given the lack of disclosure, why can't this signal just come from the
10 memory controller?

11 MR. HEIM: So, first of all, what Figure 10B is showing is the
12 address bit, A13, or A12. One of those is going to be the signal that
13 indicates to the circuitry which rank is being accessed. And so, if you're
14 controlling the data buffer, the multiplexer, demultiplexer, one skilled in the
15 art would understand that it's that device, the logic that's going to do that.
16 To answer your question, and I'm sorry to wander off for a second there, Dr.
17 Przybylski explains in slide 116 that, for reads, the CAS signal isn't going to
18 select the data coming from the one address rank and transfer it to the data
19 bus. So, the CAS signal isn't going to work for that. And secondly, CAS
20 isn't going to give you the when information about when you have to
21 transfer to the data buffer control signals consistent with the Provisional's
22 explanation. They also talk about another possibility that you could use the
23 strobe signal. And again, Dr. Przybylski explains why that wouldn't fly as
24 well, because it's at an indeterminate state. It's not driven high or low.

25 JUDGE GALLIGAN: Yeah. This is Judge Galligan again. I just
26 wanted to clarify. So, it's not out -- I mean it's not out of the realm of

1 possibility that a multiplexer in the data path multiplexer could be controlled
2 by something from the memory controller because it's multiple -- I mean, the
3 CAS signal controls multiplexer and Figure 10B of the '537 Patent.

4 MR. HEIM: It is -- it's not possible because of the rank
5 multiplication that is being performed. The memory controller that's
6 invisible. It doesn't know that there's another rank of memory behind there.
7 The only device that knows that is the logic. That's why Dr. Przybylski is
8 explaining that what is disclosed would be, it would be apparent to a person
9 skilled in the art that that's the only device that's able to -- to decode that
10 address in order to figure out where that signal is going to go. And yes,
11 there is additional figures in the Patent, but they, they literally are -- are
12 showing what is being described. When you connect the dots relative to the
13 address translation and knowing which rank is going to be, it's going to be
14 the appropriate one.

15 JUDGE GALLIGAN: Okay. Thank you.

16 MR. HEIM: I'll reserve the rest of my time. Thank you.

17 JUDGE GALLIGAN: Okay. Thank you. You've used an hour
18 and 24 minutes. I'll stop the clock. Petitioner, you have a little under 20
19 minutes. Reset, and you may begin. Thanks.

20 MR. CHANDLER: Thank you, Your Honor. I want to pick up on
21 the last point about the priority issue and -- and so forth. And Judge
22 Galligan, you said that you had looked into the '537 Patent and try to figure
23 out the chain of priority and whatnot. And I just want to direct the Board's
24 attention to the Federal Circuit's decision in Parus, 70 F.4th 1365 at page
25 1371 to 1372, which makes clear that it is not the Board's responsibility to
26 have to dig into the priority chain. That is Netlist's responsibility as part of

1 their burden of production under Dynamic Drinkware and the Federal
2 Circuit use some colorful language that said judges are not like pigs hunting
3 from truffles buried in briefs. The Board should not be forced to play
4 archeologist with the record. And then they went on to say at page 1372,
5 the burden of production cannot be met without some combination of citing
6 the relevant record evidence with specificity and explaining the significance
7 of the produce material in briefs.

8 So, it's not enough for Netlist to just give this claim chart with no
9 explanation that just has a bunch of citations, not even in the '537 Patent, but
10 to, you know, a bunch of paragraphs of Exhibit 1005. If they want to get
11 priority for all their claims, they need to explain how what they cite actually
12 gives support for all the claim limitations, including the data buffer control
13 signals, and including the issue that you were discussing with Netlist about
14 well, how do we know that those data buffer control signals come from the
15 logic rather than from outside of the module, you know, from the memory
16 controller. None of that's explained in their brief, in their charts. And so,
17 we think, you know, both technically, but also as a legal matter that they've
18 failed on their burden of production priority and therefore Ellsberry's prior
19 art.

20 There are a number of things I could respond to, but were there
21 questions in particular, Your Honors, that you would like me to turn to first?

22 JUDGE GALLIGAN: Yes. This is Judge Galligan. I want you to
23 address Perego column 9, lines 58 to 60, particularly evidence that you have,
24 well, declaration testimony or anything, saying that that is referring to the
25 line that goes to the module from the memory controller and not the internal
26 workings of the module. And address that line of argumentation from Patent

1 Owner, please.

2 MR. CHANDLER: Yes. So, one thing that I think is really
3 important is, again, for example, we look at slide 64, which shows the buffer
4 of Perego. And there was a lot of discussion about, well, why would you
5 make the buffer in Perego compatible with JEDEC, JEDEC is prior art?
6 And I think Judge Galligan, that you and Judge Jurgovan were correct that
7 the reason that it makes sense for Perego is Perego is trying to be flexible
8 and have a buffer that, you know, you build the buffer, and you can put that
9 memory module in a JEDEC computer, and the buffer will adjust and work,
10 or you can take it out and put it in a different computer, which might be a
11 Rambus computer and the buffer would work.

12 And I think slide 64 is really important, again, because 64-bit data
13 width is expressly disclosed, and a serialization ratio of one-to-one is
14 expressly disclosed. And that means a 64-bit primary channel for the data
15 and a 64-bit ranks on the secondary channel. And that only makes sense
16 with JEDEC. Rambus does not have the 64-bit data buffer or 64-bit data
17 width and does not have 64-bit ranks. Rambus is this narrow protocol. And
18 so, you got to read, you know, Perego as a whole. So, you reference to 15,
19 38 it's talking about the same data buffer shown here on slide 64, which
20 would be compatible both, which can be configured to be compatible with
21 JEDEC.

22 JUDGE GALLIGAN: And this is Judge Galligan. What was
23 Rambus's data width, for lack of a better word?

24 MR. CHANDLER: It was, I think it might have been like 10. So,
25 again, the paper by Jacobs. So, if you look at Exhibit 1069, page 12, he says
26 on the left that in the Rambus specification, there are nine lines to carry all

1 necessary information, including address, command, chip-select, and data.
2 So, nine lines total for everything. Whereas JEDEC is something like, I
3 mean, I can't do the math, but it's like 80 lines because you've got 64 lines
4 for data, plus you got like a dozen lines for address, plus you got RAS, CAS,
5 WE, and chip select. So, you know, JEDEC has many, many more lines, but
6 if you just focus on the data lines, I mean, that's the big giveaway here that
7 what Netlist is arguing makes no sense because Rambus had fewer than nine
8 lines for everything, including the data.

9 JUDGE GALLIGAN: Okay. Thanks, counsel. I wanted you to
10 respond to Patent Owner's argument that in Figure 4, for instance, when it's
11 talking about the channels can transfer simultaneously, you'd have one
12 device on each channel doing that. Therefore, when you identify, for
13 instance, four devices in green in Figure 4A or B, whatever it is, and I'm sure
14 you've got a slide on it, as being, yeah, that one, figure, all the devices in,
15 and this is slide 63 we're referring to, all the device -- in Petitioner's deck, all
16 the devices connected to 415c and 415d are part of a rank. And what Patent
17 Owner says is, well, in Perego, the channels operate simultaneously, but
18 only one device transmits on the channel, therefore those devices aren't
19 operating together as a rank would. Can you address that?

20 MR. CHANDLER: Oh yeah. So, our slide 63 shows that Netlist
21 and its expert admitted that Perego has channels, and that Figure 4 would
22 show multiple channels. The passage, Judge Galligan, that you referred to,
23 Perego teaches that there can be one or more devices, one or more channels,
24 and that one or more channels can operate at a time. So, Perego is flexible,
25 as we've been discussing about how it would work. There's no dispute that
26 Perego has a DDR2 embodiment, and when you have DDR2 memory

1 devices, it's required that they have chip-select signals, and that means it's
2 required that they're organized in ranks because the chip-select signal is
3 what creates the rank, and this is shown, for example, on slide 69. So, at the
4 top of slide 69, JEDEC standard from chip-select says, chip-select is rank
5 selection, and Netlist's expert admits on the right that if you have chip-
6 selects, you got ranks and so forth. So, once you're in the world of DDR2
7 memory devices, you're in the world of chip-selects, you're in the world of
8 ranks, and then it gets to this question of, okay, well, how many memory
9 devices are responding at a time? And then we get to slide 64 with this
10 serialization ratio of one-to-one and the data width of 64. That means you
11 have 64-bit ranks, so that's 64 bits. We know they're DDR2 memory
12 devices, and the JEDEC standard says that they can be by 4 memory devices
13 or by 8 memory devices.

14 And so if they're by 8 memory devices, you know, eight times
15 eight is 64, so you'd have eight memory devices in the rank. But that's how
16 you get there. Perego's flexible in the number of channels and memory
17 devices, and how many respond. Perego's explicit about DDR2 memory
18 devices, is explicit about 64-bit data width, both for the primary channel and
19 for the secondary channel. That means you have 64-bit ranks, and so 64-bit
20 rank as explained on slide 69 means the chip-select is going to select all the
21 memory devices that make up 64 bits, and, you know, a common way to do
22 that would be eight memory devices, each eight bits wide.

23 JUDGE GALLIGAN: Thanks counsel. I had another question.
24 Patent Owner called out one of the Petitioner's points about backward
25 compatibility and there's a slide on it. I think it's referring to column 6 in
26 Perego, but their contention, I believe, is that when it's referring to a memory

1 controller, it's referring to the controller on the module not being, I could be
2 wrong, but I think they said, well, that's not referring to being compatible
3 with memory controllers, like a JEDEC memory controller, for instance, in
4 the computer because, obviously, if it says it would be compatible with the
5 JEDEC memory controller, then, you know, that's good for your side. So, I
6 think that they were, yeah, they were disputing maybe what the controller
7 means there. Could you address? If I understood their argument, and
8 maybe you can comment on it.

9 MR. CHANDLER: Yeah. So, slide 57, our slide 57 addresses this
10 argument. Perego says on the left, you know, flexibility with respect to
11 controller 310. Controller 310 is the memory controller in the computer.
12 It's not the buffer device, 350, 310, I think. Acrobat is letting me down. So,
13 there's another figure in Perego, I think, Figure 4A that shows 310 is the
14 memory controller, and I discussed it at the beginning of my slides, that 310
15 is the memory controller in the host computer.

16 JUDGE GALLIGAN: Okay, thanks. And I think we've arrived at
17 an acceptable definition of the level of skill in the art for everyone. Did
18 Patent Owner's response put you at ease? So, I think what they're saying is,
19 a person of skill in the art knows the design and operation of memory
20 modules and knows the operation of memory devices. So is that, I mean, so
21 basically from your definition excise the design of memory devices because
22 they're just -- just presumably just plugged into this memory module, you
23 need to know how to interact with them, but you don't need to know the
24 internal design of them. Is that something that we can agree on?

25 MR. CHANDLER: I think what you just said is fine with us
26 because you're correct that both Perego and all these references, the patents,

1 Perego, Halbert, Ellsberry, they're all just plugging in DDR2 memory
2 devices. None of them is changing the internals of the memory device. So,
3 the person of ordinary skill in the art doesn't need to change the internals of
4 the memory device. However, counsel for Netlist then went on to say, well,
5 the person with ordinary skill doesn't have the wherewithal to change that
6 ASIC on the memory module, and that's what we would strongly disagree
7 with. And I mean, our undisputed portions of the level of skill as shown on
8 slide 19 on the right side, says the personal of ordinary skill would know
9 about ASIC application, specific integrated circuits and CPLDs. So, that's
10 undisputed that a person of ordinary skill in the art would know about that.

11 And then furthermore, in the deposition of Netlist's expert, as
12 shown in Exhibit 1095, starting at page 480 line 22, I'll just read the question
13 and answer because this gets into the priority issue. Because remember,
14 Netlist's expert needs to say that the person of ordinary skill can take that
15 provisional marked as Exhibit 1005 and have enough skill to make the
16 claimed invention. And the claimed invention requires a data buffer, and it
17 requires logic on the memory module to control that data buffer. And so, I
18 asked him.

19 So, this is Exhibit 1095, page 480, starting at line 22. Question.
20 So, in your opinion, a person of ordinary skill in the art as of January 19,
21 2005, looking at the '087 provisional marked as Exhibit 1005, had the skill
22 to take a UDIMM, that stands for unbuffered DIMM. It means there's
23 nothing on the module besides the memory devices. Add data buffers to the
24 data lines, add logic to perform rank multiplication based on the density
25 transition bit, and would have had the skill to create the Verilog code to
26 program that logic to operate correctly. And the answer was on page 481,

1 line 15, yes, I believe there's sufficient disclosure in the '087 for a POSITA
2 to do that. Exhibit 1005 has no Verilog code.

3 You know, that was added later in the July 1, 2005, application,
4 and then there's some more added in the '537 application. So, when we start
5 to get in the argument that a person of ordinary skill in the art wouldn't have
6 this skill to design an ASIC on the module to perform data buffering, to
7 perform rank multiplication. We would disagree with that. And we think
8 that Netlist's expert has conceded that a person of ordinary skill on the art
9 did have the skill to do that type of design.

10 JUDGE GALLIGAN: And counsel, I have one other question that
11 I'm just thinking through my notes and things. So, we talked about the '417
12 Patent, the disclosure in column 22, that Patent Owner cited as sort of the
13 inventive leap, which is that you could register things for a clock cycle, and
14 it would be equivalent -- or it talks about this equivalent to an RDIMM. My
15 understanding of the Petitioner's position is that in the combination, the CAS
16 latency of the memory module is one more than the CAS latency of the
17 memory device. And in that time, data are buffered. And, you know,
18 they're buffered for a clock cycle. Is that correct?

19 MR. CHANDLER: Yes.

20 JUDGE GALLIGAN: Okay. So, it's not that there's, you know,
21 there's registration of the address and control signals on an RDIMM. And,
22 you know, no data buffering, but that's the combination you're proposing is
23 data buffering. So, there's not two extra clock cycles, but it's just using the
24 RDIMM standard, using the teachings in, for instance, JESD21C, Ellsberry,
25 talking about adding that the CAS latency of the memory module will be one
26 more than the CAS latency of the device. That is your contention.

1 MR. CHANDLER: Correct. That's our contention. And that's
2 also the way that it's described in the passage of the patents that you're
3 referring to, which is shown on our slide 71. And at the bottom of that
4 passage, as we've highlighted in the bottom left, it's the way the patent is
5 using the term CAS latency and overall CAS latency is an example where
6 the memory device has a CAS latency of three. And then the buffer adds
7 one clock cycle. So, the overall CAS latency is four. And as counsel for
8 Netlist indicated, the way you measure CAS latency is from the time when
9 the memory device gets the read command. And so, you start counting CAS
10 latency regardless of whether it's an RDIMM or a UDIMM or anything else.
11 You start counting from when the memory device gets the read command,
12 not when the read command may have been sent by the memory controller.
13 So, that's where you start counting for CAS latency. And then when the data
14 comes out, that's the CAS latency of the memory device, for example, three
15 clock cycles. And then if there's a data buffer, data buffer adds one more
16 clock cycle, so then the data comes out of the memory module at time four
17 in that example.

18 JUDGE GALLIGAN: And then, this is Judge Galligan, and then,
19 so you've got, I'm just trying to understand this. So, you've got an extra
20 clock cycle because you're registering the address control signals in an
21 RDIMM, you've got an extra clock cycle on the module, and then the data
22 come out on a read command, for instance, the data come out of the memory
23 devices, then they're buffered. Would there not be an additional clock cycle
24 on there, or is it that would account for the full latency of the module? Or is
25 that, am I misunderstanding? I'm clearly misunderstanding something. So,
26 if you could explain that to me.

1 MR. CHANDLER: Yeah, again, it's when you start counting for
2 CAS latency. And the way you start counting for CAS latency is when the
3 memory device gets the read command, regardless of how long it took the
4 read command to get to the memory device. That's a separate issue. So,
5 once the memory, and this is shown on slide 80, for example, it's shown on a
6 lot of other slides as well. Actually, a better slide, I think, is slide 77. So,
7 once the memory device gets the read command, which on the example of
8 slide 77 on the bottom right is at time 3, that's when you start your counting
9 for CAS latency.

10 And you can see below my red highlighting of the read command,
11 there's the arrow that says CL equals 3. So, you know, the arrow starts when
12 the read command is received at the memory device at time 3. You go
13 forward three clock cycles to T6, and that's when the data starts coming out
14 of the memory device on the DQ line. So, that's the way JEDEC defines
15 CAS latency for the memory device. And then the patent introduces this
16 concept of an overall CAS latency, the module that includes the data buffer,
17 which adds one more clock cycle, which means that the data comes out of
18 the memory module one clock cycle later at, you know, 4. And the example
19 is shown on slide 71.

20 JUDGE GALLIGAN: Okay. And I'm just trying to truly
21 understand this. So, the module has latency because the command comes
22 into the module, and then it's sent to the device. The device then sends the
23 data. At that point, the DRAM device has a certain latency. The data come
24 out, and then the data come out at the end of the module. So, you know, I
25 get the latency is when the command comes in to when the data come out.
26 So, is there -- and does the buffering cause -- so the data come out of the

1 DRAM device, for instance, and then they are buffered, correct? In the
2 memory module?

3 MR. CHANDLER: If you have a memory module with a data
4 buffer, that would be correct. So, in both.

5 JUDGE GALLIGAN: But does that add Perego?

6 MR. CHANDLER: It's true in the Perego, Halbert, '417, Patent,
7 and so forth.

8 JUDGE GALLIGAN: But does that add an additional clock cycle
9 in addition to what was already the latency without the buffer?

10 MR. CHANDLER: Not for CAS latency. So, I think what you're
11 getting at is, if you have an RDIMM, let's say, going back to slide 77, if you
12 have an RDIMM where the read command is registered, the memory
13 controller would send the read command at time T2. It would be registered.
14 Then it would arrive at the memory device at time T3. Then you start your
15 CAS latency counting of three clock cycles. In this example, data comes
16 out at time T6 in this example. But then if there's a data buffer, then the data
17 gets delayed by one more clock cycle. And so, using this example on slide
18 77, the data would come out of the memory module at time T7.

19 JUDGE GALLIGAN: All right. Great. That's helpful. I just
20 wanted to understand what's going on there. Okay. We're a little over. But
21 I want to make sure we get all the questions answered. And we'll give
22 Patent Owner equivalent time. Judges Jurgovan and Braden, do you have
23 anything additional?

24 JUDGE JURGOVAN: Just one question about Figure 6A of
25 Perego 422. And that is, if you look at the bottom module, that's showing
26 that the data select lines there, which is kind of a JEDEC-style module. But

1 one up above it doesn't have those data select lines. So, I'm wondering, you
2 know, is it -- is what -- I guess my question is -- is Perego 422 here
3 disclosing that you can have one memory module that's faster because it's
4 using these select lines? And then it also connects to other types of memory
5 modules, like the one up at top 400A.

6 MR. CHANDLER: So, I guess my first response is that this
7 argument about Figure 6A that Netlist has raised, for example, on their slide
8 50, this is a brand new argument. There was no discussion of Figure 6A in
9 any of their papers. You can search for 6A in their Patent Owner response
10 and in their sur-reply, and it doesn't come up. So, I don't believe there's
11 testimony from either expert about Figure 6A and the question that you
12 asked, Judge Jurgovan, about, you know, how does it impact the speed of
13 things? My reaction --

14 JUDGE JURGOVAN: I was just gonna add that, you know, I see
15 some advantage to a memory controller that can interface with both JEDEC
16 style and let's say Rambus style memory modules, which is what I'm
17 guessing this Figure 6A is disclosing. Right? The bottom one is kind of a
18 JEDEC style module. The top one looks like, you know, the point-to-point
19 type of addressing that's described in Perego.

20 MR. CHANDLER: That may be but would I -- the way I see it is
21 what Figure 6A is trying to teach is what you and Judge Galligan were
22 getting at, which is you can have a buffer that has all these, this flexibility so
23 that the memory module with the buffer could be plugged into one computer
24 that complies with JEDEC. And that might be like what's shown at the
25 bottom of Figure 6A, or you could take that same memory module and plug
26 it into a different computer with a Rambus type of memory controller and

1 the buffer from Perego is flexible enough to adjust because it's got that
2 configurable with data buffer to adjust to work with Rambus-style signals
3 and maybe that's more of what's shown at the top of the figure.

4 JUDGE JURGOVAN: I see.

5 MR. CHANDLER: That's the way I took away from it.

6 JUDGE JURGOVAN: Thank you.

7 JUDGE GALLIGAN: Okay. Any other questions from the panel?
8 Hearing nothing. Okay. We are -- Petitioner's case is submitted. We went
9 five minutes over on that. So, Patent Owner, you get an extra five minutes,
10 you have 20 minutes left. So, you get 25 minutes. Reset my timer. And,
11 Patent Owner, you may begin. And I wanted to ask while we're thinking
12 about and just to remember to address the evidence regarding the
13 interpretation of Perego column 9, lines 58 to 60, please. Thank you.

14 MR. HEIM: Yes. Michael Heim for Patent Owner Netlist. To
15 respond to that question to begin with. So, Exhibit 2024, Dr. Przybylski's
16 declaration discusses that passage of both paragraph 150 and at 111. And
17 then there's some certainly at least some -- some overlapping discussion in
18 paragraph 130. So, if you want, we can look through those, but I'll just refer
19 you to that unless there's any other follow-up on that.

20 JUDGE GALLIGAN: That's good. I just wanted citations. Thank
21 you very much.

22 MR. HEIM: Yeah. Understood. So 150, 111, 130. Secondly,
23 there was a discussion about the width of Rambus. Let's talk about the
24 width in Perego, because what Perego says at column 14, lines 19 through
25 23, is it's 128 pins. So, the primary link that Perego is describing is 128
26 links, and they can be used across various modules in that dynamic

1 reconfiguration sort of description that we talked about at length during my
2 initial presentation. Thirdly, relative to Figure 6A, if we could pull up slide,
3 I believe it's 78. 78, please. Yes. So, the question was spot on. What is
4 being described here are different types of memory devices on two different
5 modules. So, perhaps it could be JEDEC in 400B, and it could be a different
6 sort of memory device in 400A. That's, you know, I believe that is what
7 Perego is describing. So, you have the benefit where you're not stuck with
8 just one type of memory device, you can communicate with multiple types.
9 And so, 400A could be a Rambus DRAM sort of device that is described,
10 you know, throughout the specification. Whereas 400B could be a JEDEC
11 style DDR2 sort of device. The buffer has the flexibility to be able to do
12 both of those with its translation capabilities. If we go to, let's go to the slide
13 you just had, slide 100 on the width issue.

14 So, as shown, for example, in Figure 4B -- 4A, all of those show
15 the common data line in a multi-drop configuration. Only one of those
16 devices can talk at a time so that you can only produce on any one of those
17 channels the width of one of those devices. That's all that's available. And
18 so, the suggestion that you somehow get all of the width of all of those
19 devices is absolutely not supported. Let's go to -- so, there was a question as
20 well -- I'm sorry. There was a discussion with respect to an expert for
21 Netlist in a prior case. And if you look at paragraph 94 of Exhibit 1020, this
22 is the way that he starts his discussion. Even under Petitioner's construction,
23 neither of these arrangements allows for the possibility of single device
24 ranks. The discussion that they're citing and saying that he conceded that
25 Perego had ranks, it was conditioned on following their logic. So, he didn't
26 admit that Perego had multiple ranks. What we do have is an admission

1 from Dr. Wolfe, the same expert in this case, in a prior case, that the passage
2 in Perego talking about multiple banks is not referring to multiple ranks.
3 Multiple banks is not referring to multiple ranks.

4 So, with respect to the memory controller, it's clear that what
5 Petitioner is advancing in their obviousness contention is a substantial
6 redesign in their combination. It's beyond the level of skill in the art. It is
7 changing the basic operating principles of Perego. Relative to CAS latency,
8 let's go to their slide 115 and let me just try to clarify so that we're all on the
9 same page. CAS latency doesn't start, even if you register, CAS latency
10 doesn't start until the memory device gets the command. So, the period of
11 registering before that occurs, before the memory device gets it, it's not part
12 of CAS latency. CAS latency applies to the period after. I want to go to
13 Halbert very quickly.

14 So, on their slide 115, they suggest that Halbert is increasing the
15 module CAS latency. And what they show is without a data buffer, the
16 module CAS latency would be three and a half clock cycles. And then with
17 a data buffer, it would be four clock cycles. There's all kinds of problems in
18 the way that they've done this, but let's take what they say at face value.
19 They say you have to round up to the next whole integer. That means
20 Halbert is going to have a module like CAS latency of four cycles in both of
21 those examples, because you, according to them, you have to round it up.
22 So, how do you get an extra clock cycle from Halbert according to their own
23 petition when they say you have to round up? You don't get it. It's going to
24 end up with the same answer at the end of the day. And then I think at that
25 point, I'm happy to answer any questions that the Board still has, if there's
26 anything still remaining.

1 JUDGE GALLIGAN: Let me check my notes and see. I'm not, I
2 don't think I have anything.

3 MR. HEIM: In the interim, let's go to slide -- let's go to slide 101
4 just to clarify. So, again, the notion that each of these channels defines a
5 rank of multiple devices is simply wrong. They don't act together in
6 response to any memory command. And even if you take multiple ranks,
7 what that means is you're going to have multiple active chip-selects if we're
8 talking about JEDEC devices. And so, that raises yet another problem. And
9 so, relative to their arguments that you're going to meet the requirements of a
10 rank, it's simply not true. And then the third point is the width. As we said,
11 they keep talking about a 64-bit width. The width, and again, they're not
12 showing a width of 64 bits. They're showing much less than 64 bits. But
13 just to understand, again, the input signals that are coming in from the
14 Rambus memory controller, those are packetized signals.

15 So, you could have 100 clock cycles that include address
16 information, control information, data information, the header that goes with
17 that, all that's coming in. The reason you have a serializer is because you
18 have a serial stream of data. It may be wide. Let's say it's 16 bits wide or
19 128 bits wide, but you can get multiple packets that are coming in. So, what
20 Perego has to do is it has to unpack all that. It has to take what came in
21 serially across multiple clock cycles, and it has to do address and control
22 decoding. It's got logic to do that. And then it also has to take all the data
23 information, and it has to arrange that. It can stay in a serial fashion if it's
24 going to a Rambus device. In the JEDEC world, that would then have to be
25 converted into the right width, let's say 64 bits. And so, the notion that this
26 one-to-one serialization is some sort of, you know, magic solution for them,

1 it's ignoring the fact we're talking about packets that are being received at
2 that buffer device, and the fact that you have to do additional logic and
3 decoding. And that's one of the reasons that the buffer doesn't care about
4 CAS latency because what happens in a Rambus system is the memory
5 controller will specify on a transaction by transaction basis, this is the
6 latency that I want for a response to this signal. And unless there's any
7 questions, I'll stop.

8 JUDGE GALLIGAN: Counsel, this is Judge Galligan. I have one
9 follow-up on that. On my understanding of Perego's disclosure of the
10 serialization ratio, for instance, it discloses a one-to-one serialization ratio in
11 column 17, lines 26 to 28, and it talks about the serialization in column 14.
12 Is that it's talking about the memory device access width as a ratio to the
13 buffer device interface width. So, we're talking about the data there, right? I
14 mean, we're not talking about address, you know, signals being serialized. I
15 thought they were talking about the data being serialized, or for instance, if
16 you have a 16 to one width, you'd have to have parallel to serial converters.

17 MR. HEIM: So, first of all it's not entirely clear that we're only
18 talking about data, but let's assume that we are. You're still gonna have
19 headers on the packet. You're still gonna have other information. It's just
20 not a straight width of data that's coming in. It's gonna be across multiple
21 cycles. Relative to the memory access width, it's entirely unclear if they're
22 talking about, what I believe they're talking about is the aggregate width
23 across different memory channels. It's not entirely clear, you know, if you're
24 talking about one device in this channel, one device in this channel, or if
25 you're talking about the number of devices in a particular channel. And the
26 petition, the Petitioner has never clarified exactly what any of that means.

1 JUDGE GALLIGAN: Okay. You still have 15 minutes or 14
2 minutes. Are you finished?

3 MR. HEIM: That's it. That's -- that's all I have.

4 JUDGE GALLIGAN: Okay. Great. And I don't think the panel
5 has anything further. This is Judge Galligan again. We appreciate counsels'
6 presentations. You both were very well prepared, and we appreciate your
7 ability to answer our questions with citations to the record. So, thanks for
8 that. We are now adjourned.

9 (Whereupon the above-entitled matter went off the record at 3:24
10 p.m.)

IPR2023-00454 (Patent 11,093,417 B2)

IPR2023-00455 (Patent 9,858,215 B1)

PETITIONER:

Eliot Williams

Theodore Chandler

Ferenc Pazmandi

John Gaustad

Brianna Potter

BAKER BOTTS L.L.P.

eliot.williams@bakerbotts.com

ted.chandler@bakerbotts.com

ferenc.pazmandi@bakerbotts.com

john.gaustad@bakerbotts.com

brianna.potter@bakerbotts.com

Juan Yaquian

Winston & Strawn LLP

jyaquian@winston.com

PATENT OWNER:

Hong Zhong

Jonathan Lindsay

Philip Warrick

IRELL & MANELLA LLP

hzhong@irell.com

jlindsay@irell.com

pwarrick@irell.com