UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD, MICRON TECHNOLOGY, INC., MICRON SEMICONDUCTOR PRODUCTS, INC., and MICRON TECHNOLOGY TEXAS LLC,[1]
Petitioners,

v.

NETLIST, INC.,
Patent Owner.

Case No. IPR2023-00455
Patent No. 9,858,215 B1

PATENT OWNER'S REQUEST FOR DIRECTOR REVIEW

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[1] Micron Technology, Inc., Micron Semiconductor Products, Inc., and Micron Technology Texas LLC filed a motion for joinder and a petition in IPR2023-01142 and have been joined as petitioners to this proceeding.

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Pursuant to 37 C.F.R. § 42.71(d) and the Revised Interim Director Review Process, Patent Owner Netlist, Inc., respectfully requests Director Review of the Board's Final Written Decision (Paper 45, "FWD"), in which the Board determined that claims 1-29 of U.S. Patent No. 9,858,215 B1 (EX1001, "the '215 Patent") are unpatentable as obvious over a combination of the Perego reference (EX1071) and the JESD79-2 reference (EX1064).

I. INTRODUCTION

The Board's final written decision presents an important issue of law and policy related to the Board's treatment of the grounds of unpatentability asserted in a petition for *inter partes* review. Director Review is necessary to clarify that the Board should not find claim limitations satisfied by a reference—here JESD21-C (EX1062 and EX1066)—not included in any asserted ground and disclaimed by Petitioners in connection with teaching those limitations.

Petitioners invited this error by citing JESD21-C repeatedly in their Petition and throughout the IPR proceedings to fill the gaps left by the references actually identified in the sole ground decided by the Board (Perego and JESD79-2). *See, e.g.*, Reply (Paper 27) 3 (relying on JESD21-C for "receiving chip select signals at the memory module," which is not disclosed in Perego or JESD79-2).

Petitioners argued that JESD21-C need not be included in the grounds because they cited it ***only*** for purposes of supporting an alleged ***motivation*** to combine

Perego and JESD79-2. *See* Reply 3-4, 13-14. If that were true, the Board should not have relied on JESD21-C for any missing limitations (i.e., any limitations not taught by Perego or JESD79-2) of the '215 Patent's challenged claims. Yet the Board did precisely that, rejecting Netlist's arguments regarding the use of JESD21-C without addressing legal precedent and citing and relying upon JESD21-C extensively throughout the Final Written Decision. *See* FWD 7, 14, 16, 19, 24, 25, 28, 30, 34-36, and 41.

That was legal error. The Board does not "enjoy[] a license to depart from the petition," which "is supposed to guide the life of the litigation." *SAS Inst. Inc. v. Iancu*, 138 S. Ct. 1348, 1356 (2018) (citing 35 U.S.C. § 316(a)(8)). "[T]he statute tells us that the petitioner's contentions, not the Director's discretion, define the scope of the litigation all the way from institution through to conclusion." *Id.* at 1357. Further, the Board lacks "authority … to raise, address, and decide unpatentability theories never presented by the petitioner." *In re Magnum Oil Tools Int'l, Ltd.*, 829 F.3d 1364, 1381 (Fed. Cir. 2016); *see also Koninklijke Philips N.V. v. Google LLC*, 948 F.3d 1330, 1336 (Fed. Cir. 2020) (holding that "the Board erred when it instituted inter partes review based on a combination of prior art references Google did not advance in its petition"). Director Review is necessary to clarify that the Board is not permitted to craft new grounds inconsistent with the Petition and Petitioners' arguments.

II. BACKGROUND

The ’215 Patent claims a novel memory module that includes a data buffer and is designed to be compatible with specifications issued by JEDEC, an industry standards body. For example, challenged claims 9-11 require, among other things, a “memory module,” including a “register … configured to receive and buffer … the first memory command,” which includes “at least one first chip select signal,” EX1001, 37:13-31, 38:40-67. Similarly, challenged claim 23 requires, among other things, a “method of operating a memory module,” including “receiving … a first set of input command and address signals … from the memory controller,” including “at least one ***input chip-select signal***.” *Id.* at 39:54-67, 40:33-46 (emphasis added). Petitioners admit that these input chip select signals are “***essential*** in a JEDEC-style memory system.” Reply 5.

In the sole ground decided by the Board (*see* FWD 46), Petitioners expressly relied on a combination of Perego (which discloses a non-JEDEC memory module) and JESD79-2 (which discloses specifications for certain JEDEC memory devices). The Board’s obviousness determination, however, additionally and expressly relies on the JESD21-C reference (*e.g.*, FWD 35-36 (citing EX1062, 6)), which Petitioners cited extensively throughout the Petition and the IPR. As Petitioners acknowledged, they did not include JESD21-C in any asserted ground. *See* Reply 3-4.

Exhibits 1062 and 1066 are variations of the JESD21-C memory ***module***

specifications issued by JEDEC. JESD21-C is distinct from the JESD79-2 specification (EX1064), which relates to the individual memory ***devices*** (i.e., chips) that typically are soldered onto the printed circuit board that comprises the memory module and serves as an interface between the memory devices and the host computer's memory controller. So it is not surprising that details related to the connections between the memory controller and module are disclosed in JESD21-C, not JESD79-2. *See* EX2033 (Petitioners' expert's deposition transcript), 105:4-5 ("[JESD21-C] is just a device specification. It's not the module specification.").

Nor is it surprising that Perego—which discloses non-JEDEC memory modules—does not disclose a memory module that receives input chip-select signals from a memory controller. While Perego discloses compatibility with JEDEC memory devices, the protocol translation functionality in Perego's on-module buffer generates any chip-select signals expected by the memory devices. *See* POR (Paper 22) 26-27; EX2024, ¶¶137; EX1071, 9:54-57, 10:54-67.

After Netlist identified Petitioners' failure to include JESD21-C in their proposed grounds (*see* POR 1-2, 13, 25-26), Petitioners replied by arguing that JESD21-C need not be included in the grounds because they cited it ***only*** for purposes of supporting an alleged ***motivation*** to combine Perego and JESD79-2. *See* Reply 3-4 (arguing that JESD21-C is "relevant to show that combining Perego with a conventional memory bus including chip-select lines was obvious, because '[t]he

motivation need not be found in the references sought to be combined ….'" (quoting *DyStar Textilfarben GmbH v. C.H. Patrick Co.*, 464 F.3d 1356, 1361 (Fed. Cir. 2006)); Reply 13 ("[T]he motivation to combine can be found outside the references being combined, such as in JESD21-C …."). As such, the Board should not have relied on JESD21-C for any claim limitations not taught by Perego or JESD79-2.

In its Final Written Decision, the Board addressed Netlist's arguments regarding the impropriety of relying on JESD21-C and correctly stated Netlist's position that the relied-upon reference "JESD79-2 … relates to memory devices, not memory modules," and "that the asserted combination of references does not teach the recited 'input chip select signals,' which are inputs to the module, not to individual memory devices." FWD 30 (citing POR 1, 20, 24-25, 31). Yet the Board rejected Netlist's arguments without addressing any of the legal precedent cited in Netlist's briefs. The Board concluded that a skilled artisan would be familiar with JESD21-C's teachings, and that the skilled artisan would be motivated to implement input chip select signals "based on the knowledge of JEDEC standards, including JESD21-C." FWD 35-36. Even if true, those statements do not explain why the Board was justified in relying on a reference that Petitioners plainly chose to exclude from the proposed grounds and for which Petitioners claimed to rely upon only for

motivation to combine Perego and JESD79-2.[2] The Board nonetheless expressly relied on JESD21-C in Final Written Decision, including its disclosure of "SDRAM chip select lines" for modules. FWD 35-36 (finding that JESD21-C discloses a memory module configurable to receive input chip-select signals, as required by claims 9-11 and 23). Moreover, the Board referenced JESD21-C throughout its Final Written Decision. *See* FWD 7, 14, 16, 19, 24, 25, 28, 30, 34-36, and 41.

III. ARGUMENT

A. The Board Legally Erred by Relying on the JESD21-C Reference Not Identified in Any Asserted Ground and Relied upon by Petitioners Solely to Support Motivation to Combine Arguments

Despite Petitioners' numerous citations to JEDEC memory module standards,

[2] The Board also wrongly stated that JESD79-2 "discloses that chip select signals are received at the module." FWD 36. It does no such thing. The cited portion of JESD79-2 describes "Input/Output" for memory ***devices*** and merely states that chip select signals "provide[s] for external Rank selection on systems with multiple Ranks" and is considered "part of the command code." EX1064, 6. This disclosure does not imply that chip select signals are necessary at the ***module*** level. Indeed, Perego discloses a non-JEDEC module without input chip select signals that uses JEDEC-standardized memory devices through the use of protocol translation in its buffer. *See, e.g.*, POR 26-27; EX2024, ¶¶137; EX1071, 9:54-57, 10:54-67.

the Petition identified only three grounds, none of which includes a JESD21-C reference. *See* FWD 46. Therefore, the Board should not have permitted Petitioners to rely on EX1062 or EX1066 as though they had included them in the grounds. Yet the Board did just that: it relied on JESD21-C for its purported teachings of specific limitations, such as the claimed input chip-select signals, *see* FWD 35-36, 37-38.

As the Supreme Court has held, in an IPR "the petitioner is master of its complaint and normally entitled to judgment on ... the claims it raises, not just those the decisionmaker might wish to address." *SAS*, 138 S. Ct. at 1355. "Congress chose to structure a process in which it's the petitioner, not the Director, who gets to define the contours of the proceeding." *Id.*; *see also id.* ("[R]ather than create (another) agency-led, inquisitorial process for reconsidering patents, Congress opted for a party-directed, adversarial process."). That decision is consistent with the statutory framework that requires a petition to identify "with particularity" "the grounds on which the challenge to each claim is based." 35 U.S.C. § 312(a)(3); *see also* 37 C.F.R. § 42.104(b) (requiring petitioners to identify "the patents or printed publications relied upon for each ground" and "where each element of the claim is found in the prior art patents or printed publications relied upon").

Because "the petitioner's contentions … define the scope of the litigation all the way from institution through to conclusion," *SAS*, 138 S. Ct. at 1357, the Federal Circuit has held that "the Board erred by instituting inter partes review based on a

combination of prior art references not advanced in [the] petition." *Koninklijke Philips*, 948 F.3d at 1335. The Board is not limited by the "exact language of the petition," but it does not "enjoy[ ] a license to depart from the petition and institute a ***different*** inter partes review of his own design." *Id.* at 1336 (quoting *SAS*, 138 S. Ct. at 1356). In *Koninklijke Philips*, the Federal Circuit held that the Board erred in instituting a ground that included a reference ("Hua") "because Google did not advance such a combination of references in its petition." *Id.* at 1337.

The *Koninklijke Philips* Court did permit Google to rely on Hua to demonstrate the state of the art and supply a missing claim limitation in a ground where Google expressly relied upon it for that purpose, *id.* at 1334 (noting that Google cited "Hua and an expert declaration" to argue that a "pipelining" claim limitation was generally known in the art), but that is not the case here. In this IPR, Petitioners not only failed to advance a combination of references that included JESD21-C in any of their proposed grounds, but also cabined the use of JESD21-C to evidence of a motivation to combine Perego and JESD79-2. *See* Reply 3-4, 13-14. While courts have permitted the Board to rely on references beyond the proposed grounds to meet claim limitations in circumstances where Petitioners specifically advance such arguments, here—despite pervasive citation to JESD21-C—Petitioners disclaimed reliance on JESD21-C for anything beyond evidence of a purported motivation to combine Perego and JESD79-2. Yet the Board expressly

relied on JESD21-C for its disclosure of specific claim limitations. *See, e.g.*, FWD 32, 35. It therefore should have been in the grounds, and the Board should have held Petitioners to the required showing of a motivation to combination with a reasonable expectation of success for all three references. *Intelligent Bio-Sys., Inc. v. Illumina Cambridge Ltd.*, 821 F.3d 1359, 1369 (Fed. Cir. 2016) ("It is of the utmost importance that petitioners in the IPR proceedings adhere to the requirement that the initial petition identify "with particularity" the "evidence that supports the grounds for the challenge to each claim." (quoting 35 U.S.C § 312(a)(3))).

The Federal Circuit's decision in *Apple Inc. v. MPH Techs. Oy*, No. 2021-1355, 2022 WL 4103286 (Fed. Cir. Sept. 8, 2022), is also instructive. There, the Court affirmed the Board's decision not to consider a prior-art reference in connection with two grounds because petitioner Apple raised that reference only in a separate ground. *See id.* at *7. In other words, Apple's inclusion of the reference in only one ground and not the others reflected a choice that the Board is not free to second-guess. In rejecting Apple's contention that "the Board exalted 'form over substance' by requiring Apple to include [the reference] in Grounds 1 and 3," the Court noted that "these requirements have a practical impact," including the need to provide reasons that a skilled artisan would be motivated to combine the teachings of the itemized references with those of the additional reference. *Id.* Because Apple failed to include the relevant reference in two of its grounds, the Court held that the

"Board did not err by declining to consider arguments that Apple did not make." *Id.* Here, by expressly relying on JESD21-C, the Board made the error of considering an argument inconsistent with Petitioners' representation that they cited JESD21-C to support a motivation to combine rather than for its alleged disclosure of specific claim limitations. As in *MPH*, the Board should have respected that choice.

By adopting an argument at odds with Petitioners' reply argument, the Board failed to "base its decision on arguments that were advanced by a party, and to which the opposing party was given a chance to respond." *Axonics, Inc. v. Medtronic, Inc.*, 75 F.4th 1374, 1381 (Fed. Cir. 2023); *see also Magnum Oil*, 829 F.3d at 1377, 1381 (reversing the Board's decision holding all challenged claims unpatentable for obviousness because the Board relied on a prior art combination that was different from the combination asserted in the petition). In *Magnum Oil*, for example, the Federal Circuit expressly rejected the USPTO's argument that the Board is permitted to address obviousness arguments that "could have been included in a properly-drafted petition." *Magnum Oil*, 829 F.3d at 1380. Because IPR is "predicated on a petition followed by a trial in which the petitioner bears the burden of proof," the Board may not "adopt arguments on behalf of petitioners that could have been, but were not, raised by the petitioner during an IPR." *Id.* at 1381. "Instead, the Board must base its decision on arguments that were advanced by a party, and to which the opposing party was given a chance to respond." *Id.* The facts here are even more

egregious than in *Magnum Oil*: Petitioners disavowed the notion that they had relied on JESD21-C for any purpose beyond supporting a motivation to combine the Perego and JESD79-2 references, and then the Board relied on JESD21-C for disclosure of specific claim limitations anyway.

It is not clear why the Board went astray in this manner. But portions of the Board's analysis suggest that it believed its reliance on JESD21-C was permissible because an obviousness analysis may rely on the "background" knowledge of a skilled artisan. *See, e.g.*, FWD 35-36 (stating that a person of skill in the art would have had "knowledge of JEDEC standards, including JESD21-C," and purporting to rely on that knowledge to supply the missing element of input chip-select signals). Missing limitations, however, can be filled in with "background knowledge" only when "the limitation in question [is] unusually simple and the technology particularly straightforward," *Arendi S.A.R.L. v. Apple Inc.*, 832 F.3d 1355, 1362 (Fed. Cir. 2016)—conditions that are not satisfied here. The references actually included in Petitioners' grounds lacked any disclosure of input chip-select signals, and—particularly in a case like this involving complex technology like this one—that should have been fatal to the Petition. Only by reaching outside the grounds and crafting a new obviousness argument not found in the Petition and in direct tension with Petitioners' reply arguments was the Board able to salvage Petitioners' obviousness arguments. That was error.

B. Director Review Is Necessary to Clarify the Board's Obligation to Decide IPRs Based on the Actual Grounds Proposed by Petitioners

The Board's deviation from Petitioner's grounds requires correction by the Director. As the Supreme Court has noted, "Congress chose to structure a process in which it's the petitioner, not the Director, who gets to define the contours of the proceeding." *SAS*, 138 S. Ct. at 1355. Consistent with that binding guidance, the Federal Circuit has expressly rejected the notion that the Board may "adopt arguments on behalf of petitioners that could have been, but were not, raised by the petitioner during an IPR." *Magnum Oil Tools*, 829 F.3d at 1381. The Board here erred by expressly relying for missing limitations on a reference not included in any ground that Petitioners claimed was only cited to support a motivation to combine the references identified in the grounds. Director Review provides an opportunity to clarify the importance of adhering to the asserted grounds and not relying on new grounds not advanced by any party.

IV. CONCLUSION

For these reasons, the Director should grant review and reverse the Board's final written decision finding claims 1-29 unpatentable.

Dated: August 29, 2024

Respectfully submitted,

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CERTIFICATE OF SERVICE

I hereby certify, pursuant to 37 C.F.R. § 42.6, that on August 29, 2024, a complete copy of **PATENT OWNER'S REQUEST FOR DIRECTOR REVIEW** was served upon the following, by ELECTRONIC MAIL:

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